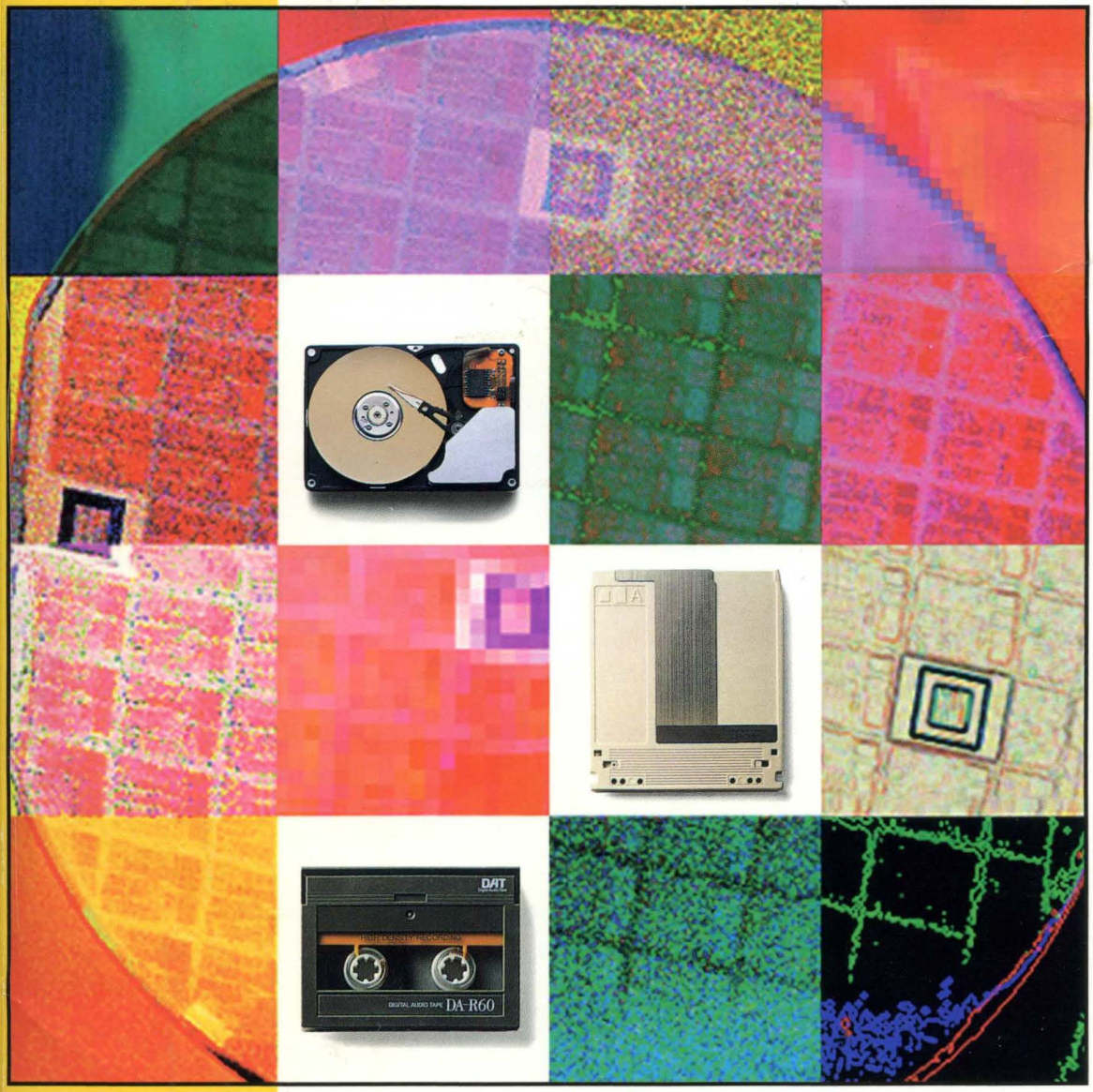
Silicon Systems Storage Products 1992 Data Book

INTEGRATED CIRCUITS FOR

STORAGE PRODUCTS



1992 Data Book

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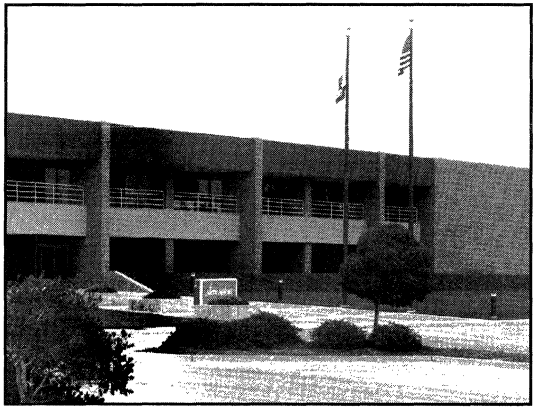
The Company



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The company, which is headquartered in California, 30 miles south of Los Angeles, was founded in 1972 as a design center. It soon entered into manufacturing and today has three fabrication facilities in California and 2,000 employees worldwide. Additional operations include assembly and test facilities in California and Singapore and design engineering centers in California as well as in Tokyo and Singapore.

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In this data book the following conventions are used in designating a data sheet "Advanced" or "Preliminary:"

Advance Information–
Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

Preliminary Data–
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The following parts are no longer supplied or supported by Silicon Systems. Please note alternate sources.

Part #	Alternate Source	Part #	Alternate Source
SSI 32B450A	SSI 32B451	SSI 32P541A	SSI 32P541B
SSI 32B451	None	SSI 32P542	None
SSI 32B453	None	SSI 32R108M, 32R122	None
SSI 32B545	None	SSI 32R114	SSI 32R525R
SSI 32C452A	None	SSI 32R115	None
SSI 32D531	None	SSI 32R188	None
SSI 32D536	SSI 32D5362A	SSI 32R502	None
SSI 32D537	SSI 32D5371/5372	SSI 32R514	None
SSI 32D5381	Signetics	SSI 32R515	None
SSI 32H567	SSI 32H6210	SSI 32R526R	None
SSI 32H568	SSI 32H6220	SSI 32R529	None
SSI 32H4630	None	SSI 32R5111	None
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STORAGE PRODUCTS REFERENCE

Device Number	Head Type	Number of Channels	Max Input Noise (nV/√Hz)	Max Input Capacitance (pF)	Read Gain (typ)	Write Current Range (mA)	Power Supplies (V)	Write Data Ports	Min. Head Swing (V)
HDD READ/WRITE AMPLIFIERS									
SSI 32R117/117R	3 Terminal	2, 4, 6	2.1	20	100	10 to 50	+5, +12	TTL	8.0 (0-pk)
SSI 32R501/501R	3 Terminal	4, 6, 8	1.5	23	100	10 to 50	+5, +12	TTL	7.5 (0-pk)
SSI 32R510A/510AR	3 Terminal	2, 4, 6	1.5	20	100	10 to 40	+5, +12	TTL	7.0 (0-pk)
SSI 32R511/511R	3 Terminal	4, 6, 8	1.5	20	100	10 to 40	+5, +12	TTL	7.0 (0-pk)
SSI 32R516	3 Terminal	4, 6, 8	1.3	18	120	10 to 60	+5, +12	TTL	7.0 (0-pk)
SSI 32R5161R	3 Terminal	10	1.3	18	150	10 to 60	+5, +12	TTL	7.0 (0-pk)
SSI 32R1200/1201	3 Terminal	2, 4	1.2	17	200	15 to 50	+5	TTL	6.0 (0-pk)
SSI 32R1220/21/22	3 Terminal	2, 4	0.8	17	250	15 to 40	+5	TTL	6.0 (0-pk)
SSI 32R512/512R	2 Terminal	8, 9	0.85	35	150	10 to 40	+5, +12	TTL	7.0 (pk-pk)
SSI 32R5121/5121R	2 Terminal	14	0.85	35	250	10 to 40	+5, +12	TTL	7.0 (pk-pk)
SSI 32R521/521R	2 Terminal	6	0.9	65	150	20 to 70	+5, +12	TTL	3.4 (pk-pk)
SSI 32R5211	2 Terminal	6	0.9	65	250	20 to 70	+5, +12	TTL	3.4 (pk-pk)
SSI 32R522/522R	2 Terminal	4, 6	1.0	32	100	6 to 35	+5, +12	TTL	3.4 (pk-pk)
SSI 32R524R	2 Terminal	8	0.75	60	100	20 to 60	+5, +12	TTL	7.0 (pk-pk)
SSI 32R525R	2 Terminal	4	0.8	35	150	25 to 40	+5, –5	Differential / Differential	3.8 (pk-pk)
SSI 32R528R	2 Terminal	8, 9	0.85	35	150	10 to 40	+5, +12	Differential	7.0 (pk-pk)
SSI 32R5281R	2 Terminal	14	0.85	35	250	10 to 40	+5, +12	Differential	7.0 (pk-pk)
SSI 32R2010R/2011	2 Terminal	10, 16	0.84	26	150	10 to 25	+5, +12	Differential	7.0 (pk-pk)
SSI 32R2015R	2 Terminal	10, 16	0.84	26	150	10 to 25	+5, +12	TTL	7.0 (pk-pk)
SSI 32R2020R/2021R	2 Terminal	2, 4, 10	0.8	20	300	5 to 35	+5	TTL	3.4 (pk-pk)
SSI 32R2030A/2031A	2 Terminal	2, 4	0.85	35	250	10 to 35	+5	TTL	3.4 (pk-pk)
SSI 32R4610A/4611A	2 Terminal	2, 4, 8	0.85	35	200	10 to 35	+5	TTL	3.4 (pk-pk)

Device Number	Circuit Function	Features
HDD PULSE DETECTION		
SSI 32P541	Read Data Processor	AGC, Amplitude & Time Pulse Qualification, RLL Compatible
SSI 32P541B	Read Data Processor	32P541 pin compatible, 32P541A w/ Increased Data Rate to 24 Mbit/s
SSI 32P544	Pulse Detector	32P541-type Pulse Detector w/ Embedded Servo Electronics
SSI 32P547	Pulse Detector	32P544-type Pulse Detector w/ Filter Multiplexer, Pulse Slimming Support
SSI 32P549	Read Data Processor	32P541 pin compatible, Low Power, +5V only, Enhanced Write to Read Recovery
SSI 32P5491	Read Data Processor	32P549 pin compatible, 5 mW Idle Mode power, Pd = 170 mW
SSI 32P3000	Pulse Detector / Programmable Filter	48 Mb/s Pulse Detector w/9-27 MHz Bessel filter, +5V only
SSI 32P3010	Pulse Detector / Programmable Filter	48 Mb/s Pulse Detector w/9-27 MHz Bessel filter, 4-burst servo capture
SSI 32P3030	Pulse Detector / Servo Demodulator	Pulse Detector w/2-burst servo demodulator, +5V only
SSI 32P3040	Pulse Detector / Programmable Filter	24-32 Mbit/s Pulse Detector w/2.5-13 MHz Bessel Filter, +5V only

STORAGE PRODUCTS REFERENCE

HDD READ CHANNEL COMBINATION DEVICES		
SSI 32D4420	Programmable Filter / Time Base Generator	7-pole Equiripple Filter, Control DACs, 72 MHz Frequency Synthesizer
SSI 32P548	Pulse Detector / Data Synchronizer	32P544-type w/ 2, 7 Synchronizer, Low Power, +5V only, <700 mW
SSI 32P5481	Pulse Detector / Data Synchronizer	Low power 32P548-type device (375 mW)
SSI 32P5482	Pulse Detector / Data Synchronizer	Low power 32P548-type device (350 mW), no Write Precompensation
SSI 32P4620	Pulse Detector / Data Separator	32P541-type + 32D537-type Data Separator w/Pulse Slimming & Constant Density Recording Support
SSI 32P4622	Pulse Detector / Data Separator	32P541-type + 32D537-type, no Filter Section, 52-pin QFP, 900 mW
SSI 32P4720	Pulse Detector / Data Separator	32P548-type + 1, 7 ENDEC, Window Shift, Power-down, 52-pin QFP, 650 mW
SSI 32P4721	Pulse Detector / Data Separator	32P4720 @12 to 24 Mbit/s, <700 mW
HDD ACTIVE FILTERS		
SSI 32F8000	Programmable Channel Filter	7-Pole Equiripple Active Filter, Programmable Cutoff Frequency / Pulse Slimming, 9 - 27 MHz
SSI 32F8011	Programmable Channel Filter	7-Pole Bessel Active Filter, Programmable Cutoff Frequency / Pulse Slimming, 5 - 13 MHz
SSI 32F8020	Programmable Channel Filter	7-Pole Equiripple Active Filter, Programmable Cutoff Frequency / Pulse Slimming, 1.5 - 8 MHz
SSI 32F8030	Programmable Channel Filter	7-Pole Equiripple Active Filter, Programmable Cutoff Frequency / Pulse Slimming, 250 kHz - 2.5 MHz
SSI 32F8120	Digitally Programmable Filter	32F8020 with serial port and DACs
SSI 32F8130/31	Digitally Programmable Filter	32F8030 with serial port and DACs / 32F8131 = 150 kHz < Fc < 1.5 MHz
HDD DATA RECOVERY		
SSI 32D4010	Data Separator	Data Synchronizer / 1, 7 RLL ENDEC 12 to 24 Mbit/s / Write Precompensation / Window Shift / Low Power
SSI 32D5321	Data Separator	Data Synchronizer / 2, 7 RLL ENDEC 7.5 to 10 Mbit/s
SSI 32D5322A	Data Separator	Data Synchronizer / 2, 7 RLL ENDEC 7.5 to 13 Mbit/s
SSI 32D534A	Data Separator	Data Synchronizer / MFM ENDEC / Write Precompensation
SSI 32D5351A	Data Separator	Data Synchronizer / 2, 7 RLL ENDEC / Write Precompensation 8 to 18 Mbit/s
SSI 32D5362A	Data Separator	Data Synchronizer / 1, 7 RLL ENDEC / Write Precompensation 10 to 20 Mbit/s
SSI 32D5371/2	Data Separator	Data Synchronizer / 1, 7 RLL ENDEC / Write Precompensation 12 to 24 Mbit/s
SSI 32D5373/4	Data Separator	Data Synchronizer / 1, 7 RLL ENDEC / Write Precompensation 15 to 32 Mbit/s
SSI 32D539	Data Separator	Data Synchronizer / 1.7 RLL ENDEC / 8-bit parallel NRZ 24 to 48 Mbit/s
SSI 32D5391	Data Separator	Data Synchronizer / 1, 7 RLL ENDEC / Serial NRZ 24 to 40 Mbit/s
SSI 32D5392	Data Separator	Data Synchronizer / 1, 7 RLL ENDEC / Dual-bit NRZ 24 to 48 Mbit/s
SSI 32D4660/1/2	Time Base Generator	Up to 100 MHz Reference Frequency PLC for Constant Density Recording
HDD HEAD POSITIONING		
SSI 32H101	Preamplifier -Ferrite head	AV = 93, BW = 10 MHz, e_n = 7.0 nV/√Hz
SSI 32H116A	Preamplifier -Thin Film head	AV = 250, BW = 20 MHz, e_n = 0.94 nV/√Hz
SSI 32H523R	Servo Read/Write	Single-channel Thin Film Read/Write Device
SSI 32H566R	Servo Read/Write	Single-channel Ferrite Read/Write Device
SSI 32H569	Servo Motor Driver	Head Parking, Spindle Motor Braking
SSI 32H4631/32	Combo Servo & Motor Speed Control	Embedded & Hybrid Servo, Hall Sensor-less Motor Speed Control, +5V only, 3600 RPM (4631) 5400 RPM (4632)
SSI 32H6110	Preamplifier -Thin Film head	AV = 250 or 300, BW = 20 MHz, e_n = 0.85 nV/√Hz
SSI 32H6210	Servo Demodulator	Di-bit Quadrature Servo Pattern; PLL Synchronization AGC Adjustment
SSI 32H6220	Servo Controller	Track & Seek Mode Operation; Microprocessor Interface

Device Number	Circuit Function	Features
HDD HEAD POSITIONING (Continued)		
SSI 32H6230	Servo Motor Driver	Head Parking, Spindle Motor Braking, Voltage Clamp
SSI 32H6240	Servo Motor Driver	Predriver for Bipolar H-bridge
SSI 32H6510	Servo 5V Driver	Low Voltage Retract, 1Ω drivers
SSI 32H6520	Servo Acquisition and D/A	10-bit A/D D/A circuits, DSP interface
HDD SPINDLE MOTOR CONTROL		
SSI 32M593A	3-Phase Motor Speed Control	±0.037% Speed Accuracy; Bipolar Operation, 5 1/4" Drives
SSI 32M594	3-Phase Motor Speed Control	±0.037% Speed Accuracy; Bipolar Operation, 3 1/2" & 5 1/4" Drives
SSI 32M595	3-Phase Sensor-less MSC	Hall Sensor-less; Motor Speed Control
SSI 32M7010	Motor Speed Control 5V Driver	Hall Sensor-less; Commutator Digital Speed Control, 5V 1Ω Driver
SSI 32M7011	Motor Speed Control 5V Commutator	Hall Sensor-less; Commutator, 5V 1Ω Driver
HDD CONTROLLER/INTERFACE		
SSI 32C260	PC AT/XT Combo Controller	15 Mbit/s Combo Buffer Manager/Disk Controller/AT/XT
SSI 32C261	PC AT/XT Combo Controller	(RLL 2, 7 ENDEC: SH-260 Compatible) / AT/XT Interface
SSI 32C4650	PC AT/XT Combo Controller	26 Mbit/s Disk Controller/AT/XT; SH-265 compatible
SSI 32C4651	PC AT/XT Combo Controller	26 Mbit/s Disk Controller/AT/XT; SH-266 compatible; EISA Type-B Demand Mode Support
SSI 32C9000	High Perf. PC AT Combo Controller	32 Mbit/s; High Performance AT Disk Controller
SSI 32C9001	PC AT Combo Controller	48 Mbit/s
SSI 32C9010	High Perf. SCSI Combo Controller	32 Mbit/s; SCSI-2 compatible; Fast SCSI; single ended
SSI 32C9020	High Perf. SCSI Combo Controller	48 Mbit/s; SCSI-2 compatible; Fast SCSI; single ended
SSI 32C9022	Combo SCSI Controller	Dual-Bit NRZ, 48 Mbit/s
SSI 32C9301	High Perf. AT Combo Controller	3V operation, 30 Mbit/s
FLOPPY DISK DRIVES		
SSI 34D441	Data Separator	High Performance Analog Data Separator, NEC 765 Compatible
SSI34P553	Pulse Detector / Data Synchronizer	0.6 - 1.6 Mbit/s data rate, MFM or 2, 7 RLL code
SSI 34R575	Read/Write	2, 4 Channel Read/Write Circuit
SSI 34B580	Support Logic	Port Expander, Includes SA400 Interface Drivers/Receivers

Section 1

HDD READ/WRITE AMPLIFIERS

silicon systems®
A TDK Group Company

SSI 32R510A/510AR
4, 6 Channel Read/Write Devices

1

November 1991

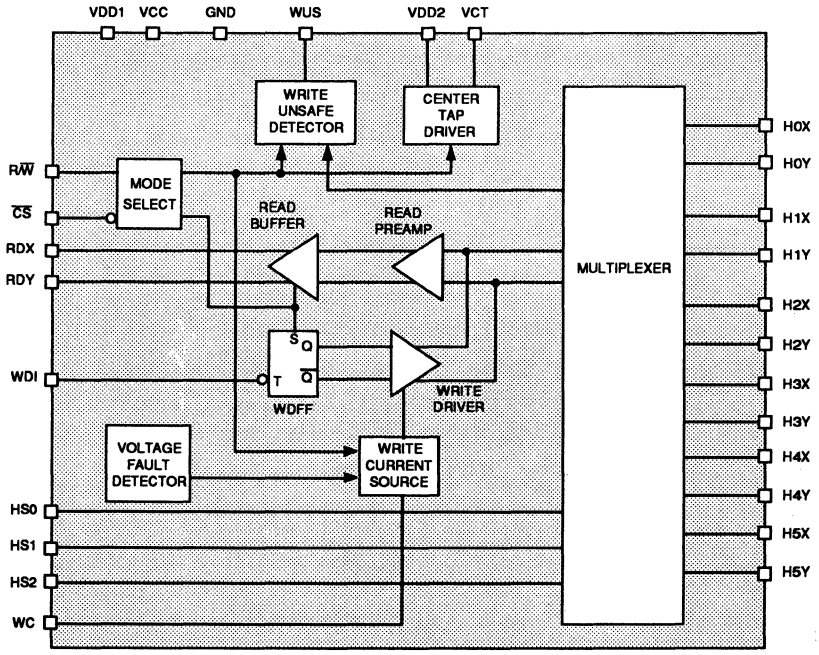
DESCRIPTION

The SSI 32R510A/510AR Read/Write devices are bipolar monolithic integrated circuits designed for use with center-tapped ferrite recording heads. They provide a low noise read amplifier, write current control and data protection circuitry for as many as six channels. The R option provides internal 750Ω damping resistors. Power supply fault protection is provided by disabling the write current generator during power sequencing. System write to read recovery time is significantly improved by controlling the read channel common mode output voltage shift in the write mode. They are available in a variety of package and channel configurations.

FEATURES

- **High performance:**
  - **Read mode gain = 100 V/V (32R510A)**
  - **Input noise = 1.5 nV/√Hz max.**
  - **Input capacitance = 20 pF max.**
  - **Write current range = 10 mA to 40 mA**
- **Enhanced system write to read recovery time**
- **Power supply fault protection**
- **Plug compatible to the SSI 32R117**
- **Designed for center-tapped ferrite heads**
- **Programmable write current source**
- **Write unsafe detection**
- **TTL compatible control signals**
- **+5V, +12V power supplies**

BLOCK DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

CIRCUIT OPERATION

These devices address up to six center-tapped ferrite heads providing write drive or read amplification. Head selection and mode control is accomplished with pins HSn, $\overline{CS}$, and R/$\overline{W}$, as shown in Tables 1 & 2. Internal resistor pullups, provided on pins $\overline{CS}$ and R/$\overline{W}$, will force the device into a non-writing condition if either control line is opened accidentally.

TABLE 1: Mode Select

$\overline{CS}$	R/$\overline{W}$	MODE
0	0	Write
0	1	Read
1	X	Idle

TABLE 2: Head Select

HS2	HS1	HS0	HEAD
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	X	None

0 = Low level 1 = High level X=Don't care

WRITE MODE

The write mode configures the device as a current switch and activates the Write Unsafe (WUS) detection circuitry. Write current is toggled between the X and Y side of the selected head on each high to low transition of the Write Data Input (WDI).

The magnitude of the write current (0-pk) is programmed by an external resistor RWC, connected from pin WC to ground and is given by:

$$Iw = \frac{K}{RWC}$$

where K is the Write Current Constant. In multiple device applications, a single RWC resistor may be made common to all devices.

Power supply fault protection improves data security by disabling the write current generator during a voltage fault or power supply sequencing. Additionally, the write unsafe detection circuitry monitors voltage transitions at the selected head connections and flags any of the conditions listed below as a high level on the open collector output pin, WUS. Two negative transitions on pin WDI, after the fault is corrected, are required to clear the WUS flag.

- Head open
- WDI frequency too low
- Device not selected
- Head center tap open
- Device in read mode
- No write current

To reduce internal power dissipation, an optional external resistor, RCT, given by RCT ≤ 130Ω x 40/Iw (Iw in mA), is connected between pins VDD1 and VDD2. Otherwise connect pin VDD1 to VDD2.

To initialize the Write Data Flip Flop (WDFF) to pass current through the X-side of the head, pin WDI must be low when the previous read mode was commanded.

READ MODE

The read mode configures the device as a low noise differential amplifier and deactivates the write current generator and write unsafe circuitry. The RDX and RDY outputs are emitter followers and are in phase with the "X" and "Y" head ports. These outputs should be AC coupled to the load. The RDX, RDY common mode voltage is maintained in the write mode, minimizing the transient between write mode and read mode, substantially reducing the write to read recovery time in the subsequent pulse detection circuitry.

IDLE MODE

The idle mode deactivates the internal write current generator, the write unsafe detector, and switches the RDX, RDY outputs into a high impedance state. This facilitates multiple device applications by enabling the read outputs to be wire OR'ed and the write current programming resistor to be common to all devices.

PIN DESCRIPTION

NAME	I/O	DESCRIPTION
HS0-HS2	I	Head Select
$\overline{CS}$	I	Chip Select: a low level enables device
R/$\overline{W}$	I	Read/Write: a high level selects Read mode
WUS	O*	Write Unsafe: a high level indicates an unsafe writing condition
WDI	I	Write Data In: negative transition toggles direction of head current
H0X-H5X H0Y-H5Y	I/O	X,Y head connections
RDX, RDY	O*	X, Y Read Data: differential read signal output
WC	*	Write Current: used to set the magnitude of the write current
VCT	-	Voltage Center Tap: voltage source for head center tap
VCC	-	+5V
VDD1	-	+12V
VDD2	-	Positive power supply for the center-tap voltage source
GND	-	Ground

*When more than one R/W device is used, these signals can be wire OR'ed.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND. Currents into device are positive.)

PARAMETER		VALUE	UNITS
DC Supply Voltage	VDD1	-0.3 to +14	VDC
DC Supply Voltage	VDD2	-0.3 to +14	VDC
DC Supply Voltage	VCC	-0.3 to +6	VDC
Digital Input Voltage Range	VIN	-0.3 to VCC + 0.3	VDC
Head Port Voltage Range	VH	-0.3 to VDD1 + 0.3	VDC
WUS Pin Voltage Range	Vwus	-0.3 to +14	VDC
Write Current (0-pk)	Iw	60	mA
RDX, RDY Output Current	Io	-10	mA
VCT Output Current	IVCT	-60	mA
WUS Output Current	Iwus	+12	mA
Storage Temperature Range	Tstg	-65 to 150	°C
Lead Temperature PDIP, (10 sec Soldering)		260	°C
Package Temperature PLCC, SO (20 sec Reflow)		215	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
VDD1	DC Supply Voltage		10.8	12.0	13.2	VDC
VCC	DC Supply Voltage		4.5	5.0	5.5	VDC
Lh	Head Inductance		5		15	µH
RD	Damping Resistor	32R510A	500		2000	Ω
RCT*	RCT Resistor	Iw = 40 mA	123	130	137	Ω
Iw	Write Current (0-pk)		10		40	mA
Tj	Junction Temperature Range		+25		+135	°C

*For Iw = 40 mA. At other Iw levels refer to Applications Information that follows this specification.

DC CHARACTERISTICS

(Recommended operating conditions apply unless otherwise specified.)

POWER SUPPLY

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VCC Supply Current	Read/Idle Mode			35	mA
	Write Mode			30	mA
VDD Supply Current	Idle Mode			20	mA
(sum of VDD1 and VDD2)	Read Mode			35	mA
	Write Mode			20 + Iw	mA
Power Dissipation (Tj = +135°C)	Idle Mode			400	mW
	Read Mode			600	mW
	Write Mode, Iw = 40 mA, RCT = 0Ω			800	mW
	Write Mode, Iw = 40 mA, RCT = 130Ω			600	mW

DC CHARACTERISTICS (continued)

DIGITAL I/O

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VIL Input Low Voltage				0.8	VDC
VIH Input High Voltage		2.0			VDC
IIL Input Low Current	VIL = 0.8V	-0.4			mA
IIH Input High Current	VIH = 2.0V			100	µA
VOL WUS Output Low Voltage	IOL = 8 mA			0.5	VDC
IOH WUS Output High Current	VOH = 5.0V			100	µA

WRITE MODE

VCT Center Tap Voltage	Write Mode 32R510A		6.0		VDC
Head Current (per side)	Write Mode, 0 ≤ VCC ≤ 3.7V, 0 ≤ VDD1 ≤ 8.7V	-200		200	µA
Write Current Range		10		40	mA
Write Current Constant "K"		2.375		2.625	
Iwc to Head Current Gain			0.99		mA/mA
Unselected Head Leakage Current				85	µA
RDX, RDY Output Offset Voltage	Write/Idle Mode	-20		+20	mV
RDX, RDY Common Mode Output Voltage	Write/Idle Mode		5.3		VDC
RDX, RDY Leakage	RDX, RDY = 6V Write/Idle Mode	-100		100	µA

READ MODE

VCT Center Tap Voltage	Read Mode		4.0		VDC
Head Current (per side)	Read or Idle Mode 0 ≤ VCC ≤ 5.5V 0 ≤ VDD1 ≤ 13.2V	-200		200	µA
Input Bias Current (per side)				45	µA
Output Offset Voltage	Read Mode 32R510A	-440		+440	mV
Common Mode Output Voltage	Read Mode	4.5		6.5	VDC

DYNAMIC CHARACTERISTICS AND TIMING

Iw = 35 mA, Lh = 10 µH, Rd = 750Ω; f(WDI) = 5 MHz, CL(RDX, RDY) ≤ 20 pF. Recommended operating conditions apply unless otherwise specified.

WRITE MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Differential Head Voltage Swing		7.0			V(pk)
Unselected Head Transient Current				2	mA(pk)
Differential Output Capacitance				15	pF
Differential Output Resistance	32R510A	10K			Ω
	32R510AR	600		960	Ω
WDI Transition Frequency	WUS = low	250			KHz

READ MODE

Differential Voltage Gain 32R510A	Vin = 1 mVpp @ 300 kHz ZL(RDX), ZL(RDY) = 1 kΩ	85		115	V/V
Dynamic Range	DC Input Voltage, Vi, Where Gain Falls by 10% Vin = Vi + 0.5 mVpp @ 300 kHz	-2		+2	mV
Bandwidth (-3dB)	|Zs| < 5Ω, Vin = 1 mVpp	30			MHz
Input Noise Voltage	BW = 15 MHz, Lh = 0, Rh = 0			1.5	nV/√Hz
Differential Input Capacitance	f = 5 MHz			20	pF
Differential Input Resistance	32R514, f = 5 MHz	3.2K			Ω
	32R514R, f = 5 MHz	500		1000	Ω
	32R510A, f = 5 MHz	2K			Ω
	32R510AR, f = 5 MHz	460		860	Ω
Common Mode Rejection Ratio	Vcm = VCT + 100 mVpp @ 5 MHz	50			dB
Power Supply Rejection Ratio	100 mVpp @ 5 MHz on VDD1, VDD2 or VCC	45			dB
Channel Separation	Unselected Channels: Vin=100 mVpp @ 5 MHz; Selected Channel: Vin = 0 mVpp	45			dB
Single Ended Output Resistance	f = 5 MHz			30	Ω
Output Current	AC Coupled Load, RDX to RDY	±2.1			mA

DYNAMIC CHARACTERISTICS AND TIMING (continued)

SWITCHING CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
R/$\overline{W}$ To Write Mode	Delay to 90% of Write Current			1.0	µs
R/$\overline{W}$ to Read Mode	Delay to 90% of 100 mV, 10 MHz Read Signal Envelope or to 90% decay of Write Current			1.0	µs
$\overline{CS}$ to Select	Delay to 90% of Write Current or to 90% of 100 mV, 10 MHz Read Signal Envelope			1.0	µs
$\overline{CS}$ to Unselect	Delay to 90% Decay of Write Current			1.0	µs
HS0 - HS2 to any head	Delay to 90% of 100 mV 10 MHz Read Signal Envelope			1.0	µs
WUS, Safe to Unsafe - TD1	Iw = 35 mA, see Figure 1	1.6		8.0	µs
WUS, Unsafe to Safe - TD2	Iw = 35 mA, see Figure 1			1.0	µs
Head Current (Lh = 0 µH, Rh = 0Ω, see Figure 1)					
Prop. Delay - TD3	From 50% Points			25	ns
Asymmetry	WDI has 50% Duty Cycle and 1ns Rise/Fall Time			2	ns
Rise/Fall Time	10% - 90% Points			20	ns

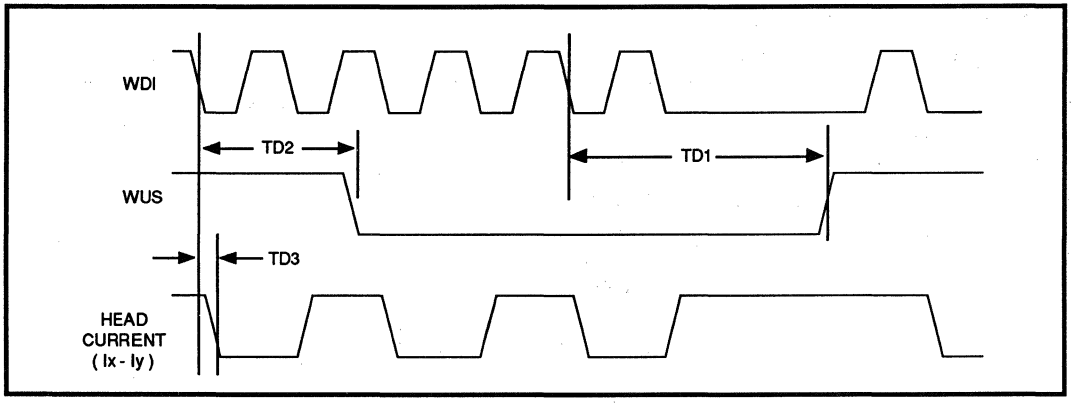


FIGURE 1: Write Mode Timing Diagram

APPLICATIONS INFORMATION

The specifications, provided in the data section, account for the worst case values of each parameter taken individually. In actual operation, the effects of worst case conditions on many parameters correlate. Tables 3 & 4 demonstrate this for several key parameters. Notice that under the conditions of worst case input noise, the higher read back signal resulting from the higher input impedance can compensate for the higher input noise. Accounting for this correlation in your analysis will be more representative of actual performance.

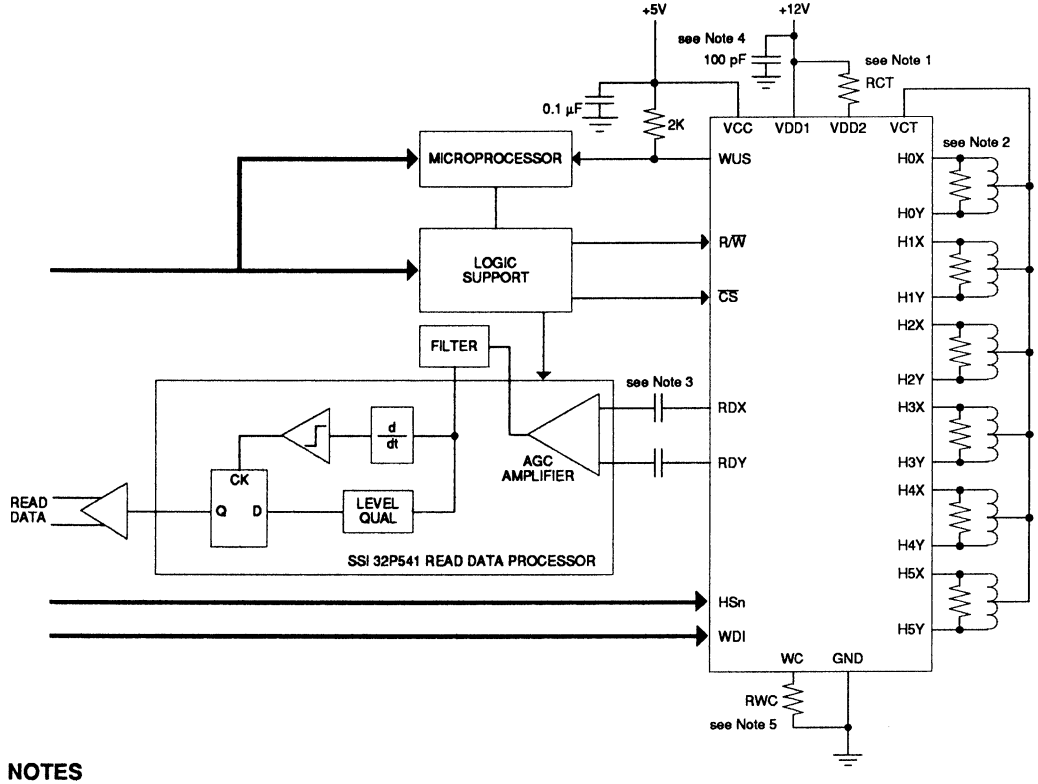
TABLE 3: Key Parameters Under Worst Case Input Noise Conditions

PARAMETER		Tj=25°C	Tj=135°C	UNITS
Inputs Noise Voltage (max.)		1.1	1.5	nV/√Hz
Differential Input Resistance (min.)	32R510AR	850	1000	Ω
	32R510A	15.4	29.4	KΩ
Differential Input Capacitance (max.)		11.6	10.8	pF

TABLE 4: Key Parameters Under Worst Case Input Impedance Conditions

PARAMETER		Tj=25°C	Tj=135°C	UNITS
Inputs Noise Voltage (max.)		0.92	1.2	nV/√Hz
Differential Input Resistance (min.)	32R510AR	500	620	Ω
	32R510A	3.2	6.1	KΩ
Differential Input Capacitance (max.)		10.1	10.3	pF

APPLICATIONS INFORMATION (continued)



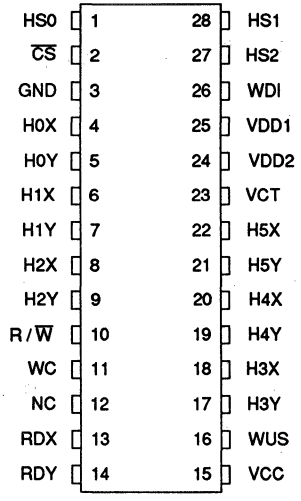
NOTES

1. An external resistor, RCT, given by; RCT ≤ 130 (40/Iw) where Iw is the zero-peak write current in mA, can be used to limit internal power dissipation. Otherwise connect VDD2 to VDD1.
2. Damping resistors not required on R versions.
3. Limit DC current from RDX and RDY to 100 µA and load capacitance to 20 pF. In multi-chip application these outputs can be wire OR'ed.
4. The power bypassing capacitor must be located close to the device with its ground returned directly to device ground, with as short a path as possible.
5. To reduce ringing due to stray capacitance this resistor should be located close to the device. Where this is not desirable a series resistor can be used to buffer a long WC line. In multi-chip applications a single resistor common to all chips may be used.

FIGURE 2: Typical Application Diagram

SSI 32R510A/510AR
4, 6-Channel
Read/Write Devices

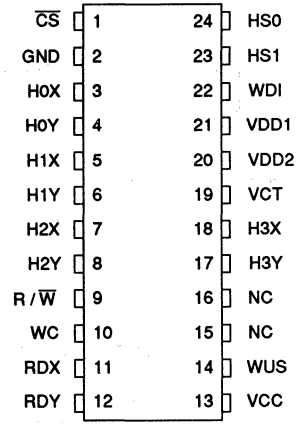
PACKAGE PIN DESIGNATIONS
(Top View)



6-CHANNEL
28-LEAD SOL

THERMAL CHARACTERISTICS

PACKAGE		θja
24-Lead	SOL	80°C/W
28-Lead	SOL	70°C/W



4-CHANNEL
24-LEAD SOL

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32R510A		
4-Channel SOL	32R510A-4CL	32R510A-4CL
6-Channel SOL	32R510A-6CL	32R510A-6CL
SSI 32R510AR with Internal Damping Resistor		
4-Channel SOL	32R510AR-4CL	32R510AR-4CL
6-Channel SOL	32R510AR-6CL	32R510AR-6CL

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SSI 32R512/512R
8 & 9-Channel Thin Film Read/Write Device

1

November 1991

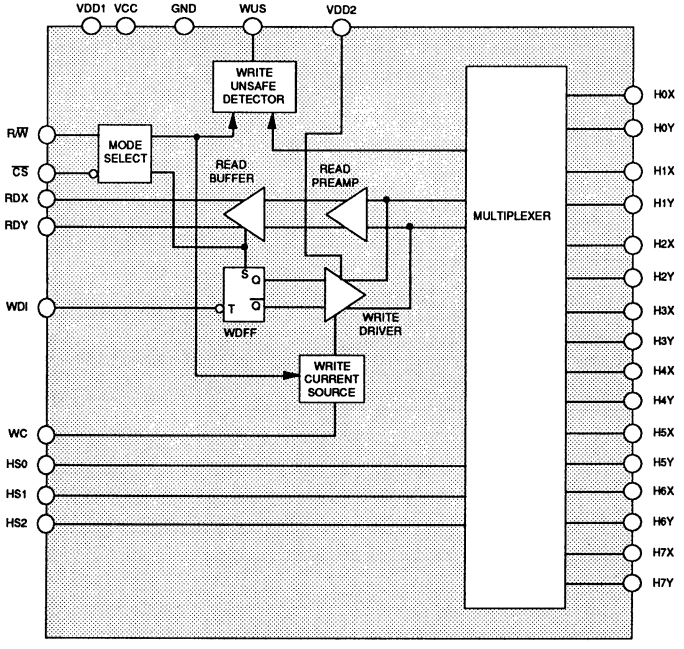
DESCRIPTION

The SSI 32R512/512R Read/Write devices are bipolar monolithic integrated circuits designed for use with two terminal thin film recording heads. They provide a low noise read amplifier, write current control and data protection circuitry for eight or nine channels. Power supply fault protection is provided by disabling the write current generator during power sequencing. System write to read recovery time is significantly improved by controlling the read channel common mode output voltage shift in the write mode. They require +5V and +12V power supplies and are available in a variety of package configurations. A mirror image pinout option is available to simplify flex circuit layout in multiple R/W device applications. The SSI 32R512R option provides internal 1000Ω damping resistors.

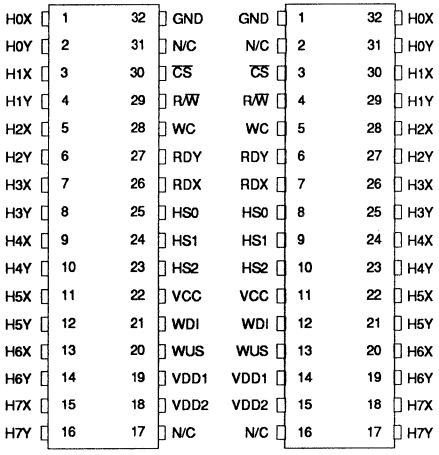
FEATURES

- **High performance:**
  - **Read mode gain = 150 V/V**
  - **Input noise = 0.85 nV/√Hz max.**
  - **Input capacitance = 35 pF max.**
  - **Write current range = 10 mA to 40 mA**
  - **Head voltage swing = 7 Vpp**
  - **Write current rise time = 9 ns**
- **Enhanced system write to read recovery time**
- **Power supply fault protection**
- **Plug compatible to the SSI 32R501 & SSI 32R511**
- **Compatible with two & three terminal thin film heads**
- **Write unsafe detection**
- **+5V, +12V power supplies**
- **Mirror image pinout option**

BLOCK DIAGRAM



PIN DIAGRAM



32-LEAD SOW **32-LEAD SOW MIRROR**

CAUTION: Use handling procedures necessary for a static sensitive component.

CIRCUIT OPERATION

The SSI 32R512 addresses up to nine two-terminal thin film heads providing write drive or read amplification. Head selection and mode control is accomplished with pins HSn, $\overline{CS}$ and R/$\overline{W}$, as shown in Tables 1 & 2. Internal resistor pullups, provided on pins $\overline{CS}$ and R/$\overline{W}$ will force the device into a non-writing condition if either control line is opened accidentally.

WRITE MODE

The write mode configures the SSI 32R512 as a current switch and activates the Write Unsafe (WUS) detection circuitry. Write current is toggled between the X and Y direction of the selected head on each high to low transition on pin WDI, Write Data Input.

A preceding read operation initializes the Write Data Flip Flop (WDFF) to pass write current in the X-direction of the head.

The magnitude of the write current (0-pk) given by:

$$Iw = \frac{Vwc}{RWC}$$

where Vwc (WC pin voltage) = 1.65V ± 5%, is programmed by an external resistor RWC, connected from pin WC to ground. In multiple device applications, a single RWC resistor may be made common to all devices. The actual head current Ix, y is given by:

$$Ix,y = \frac{Iw}{1 + Rh/Rd}$$

where:
Rh = head resistance + external wire resistance, and
Rd = damping resistance.

Power supply fault protection improves data security by disabling the write current generator during a voltage fault or power supply sequencing. Additionally, the write unsafe detection circuitry will flag any of the conditions listed below as a high level on the open collector output pin, WUS. Two negative transitions on pin WDI, after the fault is corrected, are required to clear the WUS flag.

- WDI frequency too low
- Device not selected
- Device in read mode
- No write current

Power dissipation in Write Mode may be reduced by placing a resistor, Rw, between VDD1 and VDD2. The resistor value should be chosen such that Iw Rw ≤ 3.0V for an accompanying reduction of $(Iw)^2$ Rw in power dissipation. If a resistor is not used, VDD2 should be connected to VDD1. Note that Rw will also provide current limiting in the event of a head short.

READ MODE

The read mode configures the SSI 32R512 as a low noise differential amplifier and deactivates the write current generator and write unsafe detection circuitry. The RDX and RDY outputs are emitter followers and are in phase with the "X" and "Y" head ports. These outputs should be AC coupled to the load. The RDX, RDY common mode voltage is maintained in the write mode, minimizing the transient between write mode and read mode, substantially reducing the write to read recovery time in the subsequent Pulse Detection circuitry.

IDLE MODE

The idle mode deactivates the internal write current generator, the write unsafe detector and switches the RDX, RDY outputs into a high impedance state. This facilitates multiple device applications by enabling the read outputs to be wire OR'ed and the write current programming resistor to be common to all devices.

TABLE 1: Mode Select

$\overline{CS}$	R/$\overline{W}$	MODE
0	0	Write
0	1	Read
1	0	Idle
1	1	Idle

TABLE 2: Head Select

HS3	HS2	HS1	HS0	HEAD
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8

0 = Low level 1 = High level

PIN DESCRIPTIONS

NAME	TYPE	DESCRIPTION
HS0 - HS3	I	Head Select
$\overline{CS}$	I	Chip Select: a low level enables the device
R/$\overline{W}$	I	Read/Write: a high level selects Read mode
WUS	O*	Write Unsafe: Open collector output, a high level indicates an unsafe writing condition
WDI	I	Write Data In: a negative transition toggles the direction of the head current
H0X - H8X H0Y - H8Y	I/O	X, Y Head Connections: Current in the X-direction flows into the X-port
RDX, RDY	O*	X, Y Read Data: differential read data output
WC	*	Write Current: used to set the magnitude of the write current
VCC	-	+5V Logic Circuit Supply
VDD1	-	+12V
VDD2	-	Positive Power Supply for Write current drivers
GND	-	Ground

*When more than one R/W device is used, these signals can be wire OR'ed.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETER		SYMBOL	VALUE	UNITS
DC Supply Voltage		VDD1, 2	-0.3 to +14	VDC
		VCC	-0.3 to +7	VDC
Write Current		Iw	100	mA
Digital Input Voltage		Vin	-0.3 to VCC +0.3	VDC
Head Port Voltage		VH	-0.3 to VDD2 +0.3	VDC
WUS Pin Voltage Range		Vwus	-0.3 to +14	VDC
Output Current	RDX, RDY	Io	-10	mA
	WUS	Iwus	+12	mA
Storage Temperature		Tstg	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNITS
DC Supply Voltage	VDD1	12 ± 10%	VDC
	VDD2	VDD1 - 3.0 to VDD1	VDC
	VCC	5 ± 10%	VDC
Operating Temperature	Tj	+25 to +135	°C

DC CHARACTERISTICS

Unless otherwise specified, recommended operating conditions apply.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VDD1 Supply Current	Read Mode	-	-	34	mA
	Write Mode	-	-	38	mA
	Idle Mode	-	-	14	mA
VDD2 Supply Current	Read Mode	-	-	200	µA
	Write Mode	-	-	IW+0.4	mA
	Idle Mode	-	-	200	µA
VCC Supply Current	Read Mode	-	-	75	mA
	Write Mode	-	-	56	mA
	Idle Mode	-	-	60	mA
Power Dissipation (Tj = +135°C)	Read Mode	-	-	800	mW
	Write Mode: Iw = 20 mA, VDD2 = VDD1	-	-	1000	mW
	Write Mode: Iw = 40 mA, VDD1 - VDD2 = 3.0V	-	-	1140	mW
	Idle Mode	-	-	500	mW
Input Low Voltage (VIL)		-	-	0.8	VDC
Input High Voltage (VIH)		2.0	-	-	VDC
Input Low Current (IIL)	VIL = 0.8V	-0.4	-	-	mA
Input High Current (IHL)	VIH = 2.0V	-	-	100	µA
WUS Output Low Voltage (VOL)	Iol = 8 mA	-	-	0.5	VDC
VDD Fault Voltage		8.5	-	10.0	VDC
VCC Fault Voltage		3.5	-	4.2	VDC
Head Current (HnX, HnY)	Write Mode, 0≤ VCC ≤3.5V 0 ≤ VDD1 ≤ 8.5V	-200	-	+200	µA
	Read/Idle Mode 0 ≤ VCC ≤ 5.5V 0 ≤ VDD1 ≤ 13.2V	-200	-	+200	µA

WRITE CHARACTERISTICS
Unless otherwise specified, recommended operating conditions apply, Iw = 20 mA, Lh = 1.0 µH, Rh = 30Ω and f(WDI) = 5 MHz.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
WC Pin Voltage (Vwc)		1.57	1.65	1.73	V
Differential Head Voltage Swing		7	-	-	Vpp
Unselected Head Current		-	-	1	mA(pk)
Differential Output Capacitance		-	-	25	pF
Differential Output Resistance	32R512R	800	1000	1350	Ω
	32R512	4	-	-	kΩ
WDI Transition Frequency	WUS = low	1.7	-	-	MHz
Write Current Range		10	-	40	mA

READ CHARACTERISTICS
Unless otherwise specified, recommended operating conditions apply CL (RDX, RDY) < 20pF and RL (RDX,RDY) = 1 kΩ.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Differential Voltage Gain		Vin=1mVpp @ 300 kHz	125	-	175	V/V
Bandwidth	-1dB	|Zs|<5Ω, Vin=1 mVpp @ 300 kHz	25	-	-	MHz
	-3dB	|Zs|<5Ω, Vin=1 mVpp @ 300 kHz	45	-	-	MHz
Input Noise Voltage		BW = 15 MHz, Lh = 0, Rh = 0	-	0.62	0.85	nV/√Hz
Differential Input Capacitance		Vin = 1 mVpp, f = 5 MHz	-	-	35	pF
Differential Input Resistance	32R512R	Vin = 1 mVpp, f = 5 MHz	390	-	-	Ω
	32R512	Vin = 1 mVpp, f = 5 MHz	640	-	-	Ω
Dynamic Range		DC input voltage where gain falls to 90% of its 0 VDC value, Vin = VDC +0.5 mVpp, f = 5 MHz	-3	-	3	mV
Common Mode Rejection Ratio		Vin = 0 VDC+100 mVpp @ 5 MHz	54	-	-	dB
Power Supply Rejection Ratio		100 mVpp @ 5 MHz on VDD1 100 mVpp @ 5 MHz on VCC	54	-	-	dB
Channel Separation		Unselected channels driven with 100 mVpp @ 5 MHz, Vin = 0 mVpp	45	-	-	dB
Output Offset Voltage			-360	-	+360	mV
RDX, RDY Common Mode		Read Mode	2.2	2.9	3.6	VDC
Output Voltage		Write Mode	-	2.9	-	VDC
Single Ended Output Resistance		f = 5 MHz	-	-	30	Ω
Output Current		AC Coupled Load, RDX to RDY	3.2	-	-	mA

5SWITCHING CHARACTERISTICS (See Figure 1)
Unless otherwise specified, recommended operating conditions apply, Iw = 20 mA, Lh = 1.0 µH, Rh = 30Ω and f (WDI) = 5 MHz.

PARAMETER	CONDITIONS	MIN	MAX	UNITS
R/$\overline{W}$				
R/$\overline{W}$ to Write Mode	Delay to 90% of write current	-	0.6	µs
R/$\overline{W}$ to Read Mode	Delay to 90% of 100 mV 10 MHz Read signal envelope or to 90% decay of write current	-	0.6	µs
$\overline{CS}$				
$\overline{CS}$ to Select	Delay to 90% of write current or to 90% of 100mV 10MHz Read signal envelope	-	0.6	µs
$\overline{CS}$ to Unselect	Delay to 90% of write current	-	0.6	µs
HSn				
HS0, 1, 2 to any Head	Delay to 90% of 100 mV 10 MHz Read signal envelope	-	0.4	µs
WUS				
Safe to Unsafe - TD1		0.6	3.6	µs
Unsafe to Safe - TD2		-	1	µs
Head Current				
Prop. Delay - TD3	From 50% points, Lh=0µh, Rh=0Ω	-	32	ns
Asymmetry	WDI has 50% duty cycle and 1ns rise/fall time, Lh=0µh, Rh=0Ω	-	1	ns
Rise/Fall Time	10% - 90% points, Lh=0µh, Rh=0Ω	-	9	ns

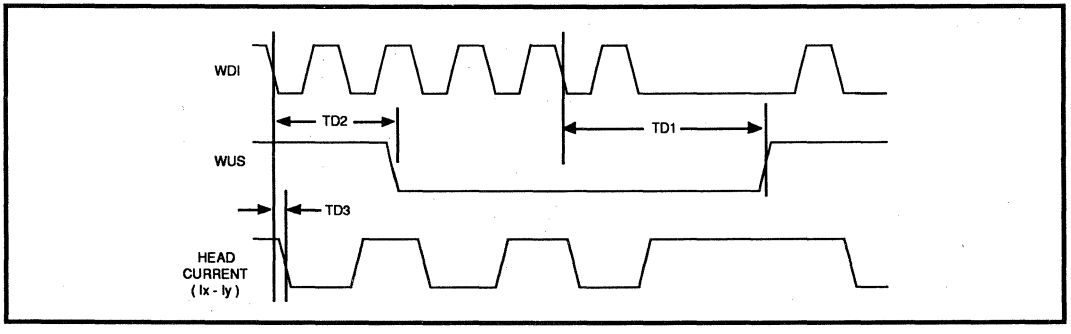


FIGURE 1: Write Mode Timing Diagram

APPLICATIONS INFORMATION

The specifications, provided in the data section, account for the worst case values of each parameter taken individually. In actual operation, the effects of worst case conditions on many parameters correlate. Tables 3 & 4 demonstrate this for several key parameters. Notice that under the conditions of worst case input noise, the higher read back signal resulting from the higher input impedance can compensate for the higher input noise. Accounting for this correlation in your analysis will be more representative of actual performance.

TABLE 3: Key Parameters Under Worst Case Input Noise Conditions

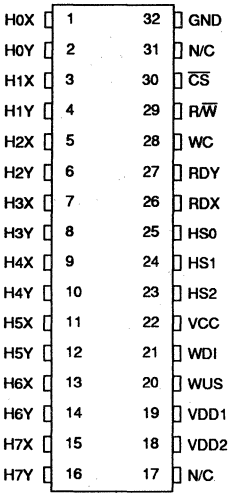
PARAMETER		Tj = 25°C	Tj = 135°C	UNITS
Input Noise Voltage (Max.)		0.70	0.85	nV/√Hz
Differential Input Resistance (Min.)	32R512R	539	595	Ω
	32R512	1200	1500	Ω
Differential Input Capacitance (Max.)		32	34	pF

TABLE 4: Key Parameters Under Worst Case Input Impedance Conditions

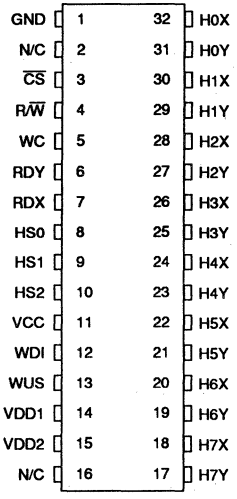
PARAMETER		Tj = 25°C	Tj = 135°C	UNITS
Input Noise Voltage (Max.)		0.58	0.71	nV/√Hz
Differential Input Resistance (Min.)	32R512R	391	458	Ω
	32R512	643	846	Ω
Differential Input Capacitance (Max.)		33	35	pF

SSI 32R512/512R
8 & 9-Channel Thin Film Read/Write Device

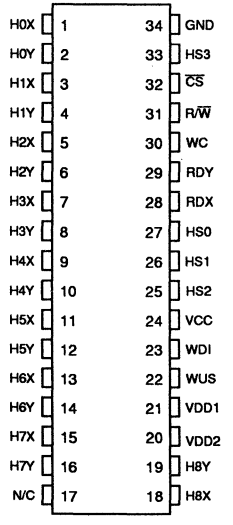
PACKAGE PIN DESIGNATIONS (Top View)



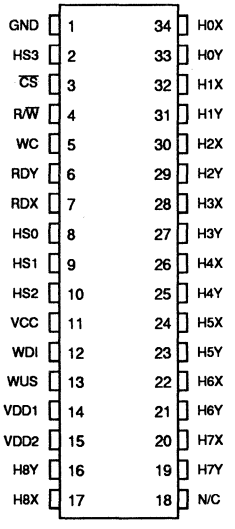
8-Channel 32-Lead SOW



8-Channel 32-Lead SOW Mirror



9-Channel 34-Lead SOL



9-Channel 34-Lead SOL Mirror

THERMAL CHARACTERISTICS: Øja

32-Lead SOW	55°C/W
34-Lead SOL	60°C/W

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32R512 Read/Write IC		
8-Channel SOW	32R512-8CW	32R512-8CW
9-Channel SOL	32R512-9CL	32R512-9CL
SSI 32R512R with Internal Damping Resistor		
8-Channel SOW	32R512R-8CW	32R512R-8CW
9-Channel SOL	32R512R-9CL	32R512R-9CL
SSI 32R512M Mirror Image		
8-Channel SOW	32R512M-8CW	32R512M-8CW
9-Channel SOL	32R512M-9CL	32R512M-9CL
SSI 32R512RM Mirror Image with Damping Resistor		
8-Channel SOW	32R512RM-8CW	32R512RM-8CW
9-Channel SOL	32R512RM-9CL	32R512RM-9CL

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 731-7110, FAX (714) 573-6914

Notes:

silicon systems®
A TDK Group Company

SSI 32R5121/5121R
14-Channel Thin Film Read/Write Device

Advance Information

1

November 1991

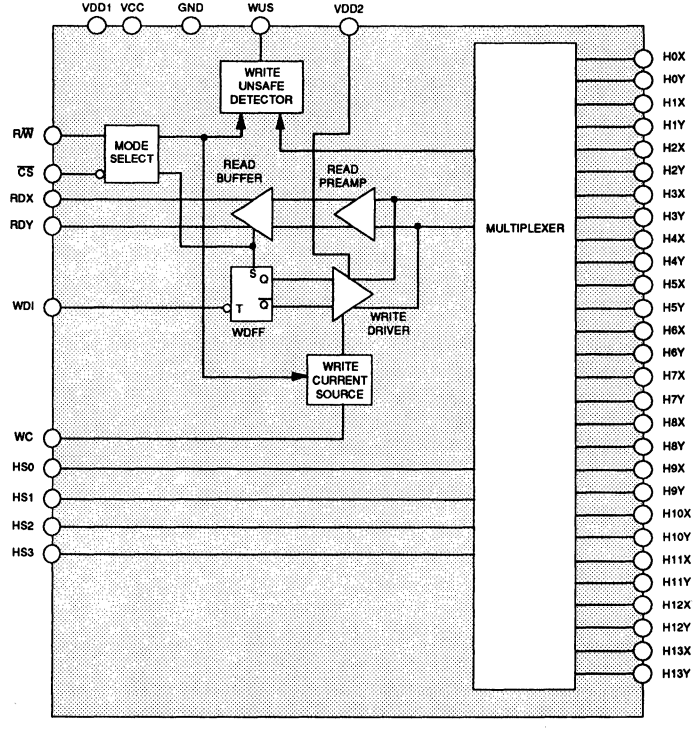
DESCRIPTION

The SSI 32R5121/5121R Read/Write devices are bipolar monolithic integrated circuits designed for use with two terminal thin film recording heads. They provide a low noise read amplifier, write current control and data protection circuitry for up to 14 channels. Power supply fault protection is provided by disabling the write current generator during power sequencing. System write to read recovery time is significantly improved by controlling the read channel common mode output voltage shift in the write mode. They require +5V and +12V power supplies and are available in a variety of package configurations.The SSI 32R512R option provides internal 180Ω damping resistors.

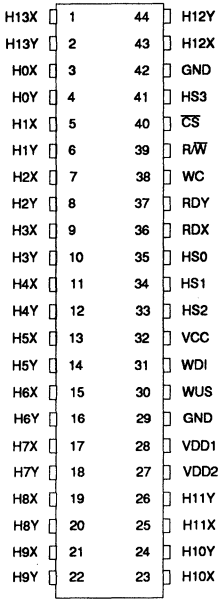
FEATURES

- **High performance:**
  - **Read mode gain = 250 V/V**
  - **Input noise = 0.85 nV/√Hz max.**
  - **Input capacitance = 35 pF max.**
  - **Write current range = 10 mA to 40 mA**
  - **Head voltage swing = 7 Vpp**
  - **Write current rise time = 9 ns**
- **Enhanced system write to read recovery time**
- **Power supply fault protection**
- **Compatible with two & three terminal thin film heads**
- **Write unsafe detection**
- **+5V, +12V power supplies**

BLOCK DIAGRAM



PIN DIAGRAM



44-LEAD SOM

CAUTION: Use handling procedures necessary for a static sensitive component.

CIRCUIT OPERATION

The SSI 32R5121 addresses up to 14 two-terminal thin film heads providing write drive or read amplification. Head selection and mode control is accomplished with pins HSn, $\overline{CS}$ and R/$\overline{W}$, as shown in Tables 1 & 2. Internal resistor pullups, provided on pins $\overline{CS}$ and R/$\overline{W}$ will force the device into a non-writing condition if either control line is opened accidentally.

WRITE MODE

The write mode configures the SSI 32R5121 as a current switch and activates the Write Unsafe (WUS) detection circuitry. Write current is toggled between the X and Y direction of the selected head on each high to low transition on pin WDI, Write Data Input.

A preceding read operation initializes the Write Data Flip Flop (WDFF) to pass write current in the X-direction of the head, i.e., into the X-port.

The magnitude of the write current (0-pk) given by:

$$Iw = \frac{Vwc}{RWC}$$

where Vwc (WC pin voltage) = 1.65V ± 5%, is programmed by an external resistor RWC, connected from pin WC to ground. In multiple device applications, a single RWC resistor may be made common to all devices. The actual head current Ix, y is given by:

$$Ix,y = \frac{Iw}{1 + Rh/Rd}$$

where:
Rh = head resistance + external wire resistance, and
Rd = damping resistance.

Power supply fault protection improves data security by disabling the write current generator during a voltage fault or power supply sequencing. Additionally, the write unsafe detection circuitry will flag any of the conditions listed below as a high level on the open collector output pin, WUS. Two negative transitions on pin WDI, after the fault is corrected, are required to clear the WUS flag.

- WDI frequency too low
- Device not selected
- Open head
- Device in read mode
- No write current

Power dissipation in Write Mode may be reduced by placing a resistor, Rw, between VDD1 and VDD2. The resistor value should be chosen such that Iw Rw ≤ 3.0V for an accompanying reduction of $(Iw)^2$ Rw in power dissipation. If a resistor is not used, VDD2 should be connected to VDD1. Note that Rw will also provide current limiting in the event of a head short.

READ MODE

The read mode configures the SSI 32R5121 as a low noise differential amplifier and deactivates the write current generator and write unsafe detection circuitry. The RDX and RDY outputs are emitter followers and are in phase with the "X" and "Y" head ports. These outputs should be AC coupled to the load. The RDX, RDY common mode voltage is maintained at the write mode valve, minimizing the transient between write mode and read mode, substantially reducing the write to read recovery time in the subsequent Pulse Detection circuitry.

IDLE MODE

The idle mode deactivates the internal write current generator, the write unsafe detector and switches the RDX, RDY outputs into a high impedance state. This facilitates multiple device applications by enabling the read outputs to be wire OR'ed and the write current programming resistor to be common to all devices.

TABLE 1: Mode Select

$\overline{CS}$	R/$\overline{W}$	MODE
0	0	Write
0	1	Read
1	0	Idle
1	1	Idle

TABLE 2: Head Select

HS3	HS2	HS1	HS0	HEAD
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
HS0 - HS3	I	Head Select
$\overline{CS}$	I	Chip Select: a low level enables the device
R/$\overline{W}$	I	Read/Write: a high level selects Read mode
WUS	O*	Write Unsafe: Open collector output, a high level indicates an unsafe writing condition
WDI	I	Write Data In: a negative transition toggles the direction of the head current
H0X - H13X H0Y - H13Y	I/O	X, Y Head Connections: Current in the X-direction flows into the X-port
RDX, RDY	O*	X, Y Read Data: differential read data output
WC	*	Write Current: used to set the magnitude of the write current
VCC	-	+5V Logic Circuit Supply
VDD1	-	+12V
VDD2	-	Positive Power Supply for Write current drivers
GND	-	Ground

*When more than one R/W device is used, these signals can be wire OR'ed.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETER		SYMBOL	VALUE	UNITS
DC Supply Voltage		VDD1, 2	-0.3 to +14	VDC
		VCC	-0.3 to +7	VDC
Write Current		Iw	100	mA
Digital Input Voltage		Vin	-0.3 to VCC +0.3	VDC
Head Port Voltage		VH	-0.3 to VDD2 +0.3	VDC
WUS Pin Voltage Range		Vwus	-0.3 to +14	VDC
Output Current	RDX, RDY	Io	-10	mA
	WUS	Iwus	+12	mA
Storage Temperature		Tstg	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNITS
DC Supply Voltage	VDD1	12 ± 10%	VDC
	VDD2	VDD1 - 3.0 to VDD1	VDC
	VCC	5 ± 10%	VDC
Operating Temperature	Tj	+25 to +135	°C

DC CHARACTERISTICS

Unless otherwise specified, recommended operating conditions apply.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VDD1 Supply Current	Read Mode	-	24	36	mA
	Write Mode	-	34	46	mA
	Idle Mode	-	11	16	mA
VDD2 Supply Current	Read Mode	-	0	200	µA
	Write Mode	-	Iw	Iw + 0.4	mA
	Idle Mode	-	0	200	µA
VCC Supply Current	Read Mode	-	52	73	mA
	Write Mode	-	35	54	mA
	Idle Mode	-	43	58	mA
Power Dissipation (Tj = +135°C)	Read Mode	-	-	800	mW
	Write Mode: Iw = 20 mA, VDD2 = VDD1	-	-	1000	mW
	Write Mode: Iw = 40 mA, VDD1 - VDD2 = 3.0V	-	-	1150	mW
	Idle Mode	-	-	500	mW
Input Low Voltage (VIL)		-	-	0.8	VDC
Input High Voltage (VIH)		2.0	-	-	VDC
Input Low Current (IIL)	VIL = 0.8V	-0.4	-	-	mA
Input High Current (IHL)	VIH = 2.0V	-	-	100	µA
WUS Output Low Voltage (VOL)	Iol = 8 mA	-	-	0.5	VDC
VDD Fault Voltage		8.5	-	10.0	VDC
VCC Fault Voltage		3.5	-	4.2	VDC
Head Current (HnX, HnY)	Write Mode, 0 ≤ VCC ≤ 3.5V 0 ≤ VDD1 ≤ 8.5V	-200	-	+200	µA
	Read/Idle Mode, 0 ≤ VCC ≤ 5.5V 0 ≤ VDD1 ≤13.2V	-200	-	+200	µA

WRITE CHARACTERISTICS
Unless otherwise specified, recommended operating conditions apply, Iw = 20 mA, Lh = 500 nH, Rh = 30Ω and f(WDI) = 5 MHz.

PARAMETER	CONDITIONS	MIN.	NOM	MAX	UNITS
WC Pin Voltage (Vwc)		1.57	1.65	1.73	V
Differential Head Voltage Swing	Iw = 40 mA	7	-	-	Vpp
Unselected Head Current		-	-	1	mA(pk)
Differential Output Capacitance		-	-	25	pF
Differential Output Resistance	32R5121R	140	180	220	Ω
	32R5121	4K	-	-	Ω
WDI Transition Frequency	WUS = low	1.7	-	-	MHz
Write Current Range		10	-	40	mA

READ CHARACTERISTICS
Unless otherwise specified, recommended operating conditions apply CL (RDX, RDY) < 20pF and RL (RDX,RDY) = 1 kΩ.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Differential Voltage Gain		Vin=1mVpp @ 300 kHz	210	250	290	V/V
Bandwidth	-1dB	|Zs|<5Ω, Vin=1 mVpp @ 300 kHz	-	30	-	MHz
	-3dB	|Zs|<5Ω, Vin=1 mVpp @ 300 kHz	27	45	-	MHz
Input Noise Voltage		BW = 15 MHz, Lh = 0, Rh = 0	-	0.62	0.85	nV/√Hz
Differential Input Capacitance		Vin = 1 mVpp, f = 5 MHz	-	-	35	pF
Differential Input Resistance	32R5121R	Vin = 1 mVpp, f = 5 MHz	115	-	-	Ω
	32R5121	Vin = 1 mVpp, f =5 MHz	640	-	-	Ω
Dynamic Range		Peak-to-peak AC input voltage where gain falls to 90% of its small signal value, f = 5 MHz	2.0	-	-	mVpp
Common Mode Rejection Ratio		Vin = 0 VDC+100 mVpp @ 5 MHz	54	-	-	dB
Power Supply Rejection Ratio		100 mVpp @ 5 MHz on VDD1 100 mVpp @ 5 MHz on VCC	54	-	-	dB
Channel Separation		Unselected channels driven with 100 mVpp @ 5 MHz, Vin = 0 mVpp	45	-	-	dB
Output Offset Voltage			-600	-	+600	mV
RDX, RDY Common Mode		Read Mode	2.2	2.9	3.6	VDC
Output Voltage		Write Mode	-	2.9	-	VDC
Single Ended Output Resistance		f = 5 MHz	-	-	30	Ω
Output Current		AC Coupled Load, RDX to RDY	3.2	-	-	mA

SWITCHING CHARACTERISTICS (See Figure 1)
Unless otherwise specified, recommended operating conditions apply, Iw = 20 mA, Lh = 500 nH, Rh = 30Ω and f(WDI) = 5 MHz.

PARAMETER	CONDITIONS	MIN	MAX	UNITS
R/$\overline{W}$				
R/$\overline{W}$ to Write Mode	Delay to 90% of write current	-	0.6	µs
R/$\overline{W}$ to Read Mode	Delay to 90% of 100mV 10MHz Read signal envelope or to 90% decay of write current	-	0.6	µs
Write Current				
WC Turn-on Time	Lr = 30Ω, Lh = 1µH, Iw = 20 mA		320	ns
WC Turn-off Time	Lr = 30Ω, Lh = 1µH, Iw = 20 mA		160	ns
$\overline{CS}$				
$\overline{CS}$ to Select	Delay to 90% of write current or to 90% of 100mV 10MHz Read signal envelope	-	0.6	µs
$\overline{CS}$ to Unselect	Delay to 90% of write current	-	0.6	µs
HSn				
HS0, 1, 2 to any Head	Delay to 90 % of 100mV 10MHz Read signal envelope	-	0.4	µs
WUS				
Safe to Unsafe - TD1		0.6	3.6	µs
Unsafe to Safe - TD2		-	1	µs
Head Current				
Prop. Delay - TD3	From 50 % points, Lh=0µh, Rh=0Ω	-	32	ns
Asymmetry	WDI has 50 % duty cycle and 1ns rise/fall time, Lh=0µh, Rh=0Ω	-	1	ns
Rise/Fall Time	10% - 90% points, Lh=0µh, Rh=0Ω	-	9	ns

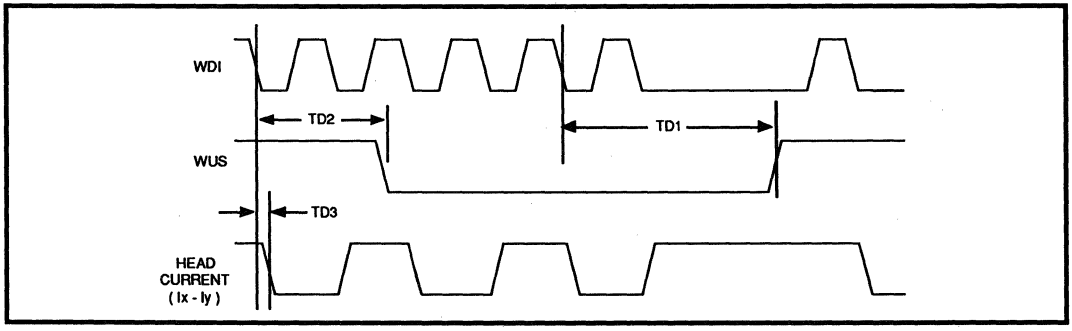


FIGURE 1: Write Mode Timing Diagram

APPLICATIONS INFORMATION

The specifications, provided in the data section, account for the worst case values of each parameter taken individually. In actual operation, the effects of worst case conditions on many parameters correlate. Tables 3 & 4 demonstrate this for several key parameters. Notice that under the conditions of worst case input noise, the higher read back signal resulting from the higher input impedance can compensate for the higher input noise. Accounting for this correlation in your analysis will be more representative of actual performance.

TABLE 3: Key Parameters Under Worst Case Input Noise Conditions

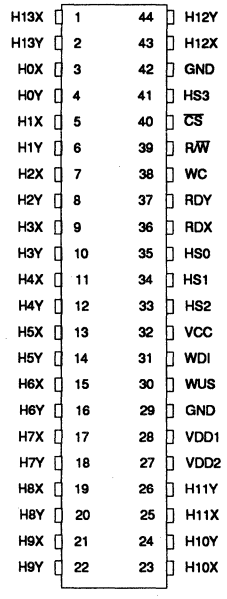
PARAMETER		Tj = 25°C	Tj = 135°C	UNITS
Input Noise Voltage (Max.)		0.70	0.85	nV/√Hz
Differential Input Resistance (Min.)	32R5121R	165	185	Ω
	32R5121	1200	1500	Ω
Differential Input Capacitance (Max.)		32	34	pF

TABLE 4: Key Parameters Under Worst Case Input Impedance Conditions

PARAMETER		Tj = 25°C	Tj = 135°C	UNITS
Input Noise Voltage (Max.)		0.58	0.71	nV/√Hz
Differential Input Resistance (Min.)	32R5121R	115	125	Ω
	32R5121	640	850	Ω
Differential Input Capacitance (Max.)		33	35	pF

SSI 32R5121/5121R
14-Channel Thin Film Read/Write Device

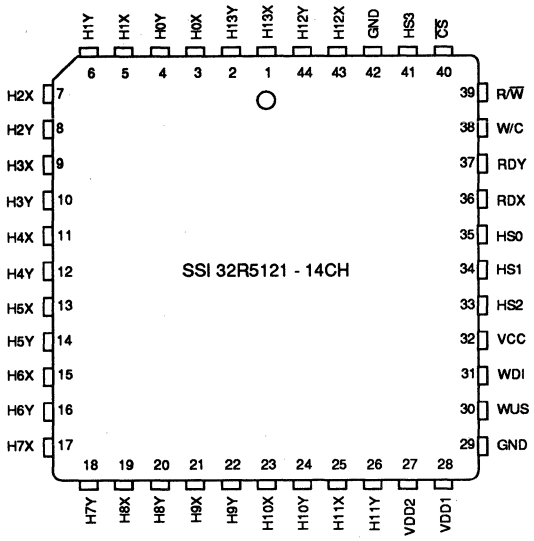
PACKAGE PIN DESIGNATIONS
(Top View)



44-Pin SOM

THERMAL CHARACTERISTICS: Øja

44-Lead SOL	50°C/W
44-PLCC	60°C/W



44-Pin PLCC

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 731-7110, FAX (714) 573-6914

SSI 32R516/516R
4, 6, 8-Channel Ferrite/MIG Read/Write Device

Preliminary Data

November 1991

DESCRIPTION

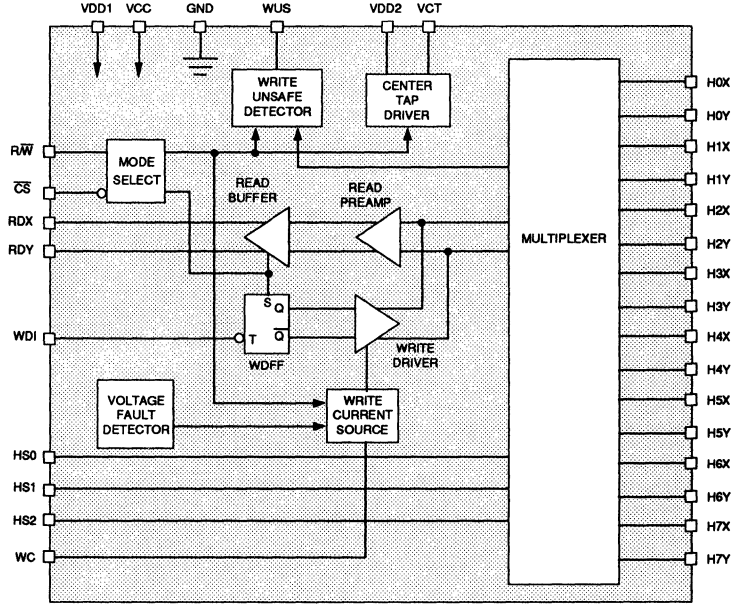
The SSI 32R516 is a bipolar monolithic integrated circuit designed for use with a center-tapped ferrite or MIG recording heads. The SSI 32R516 offers the performance upgrades of the SSI 32R511 along with improved head port characteristics and increased read gain. It provides a low noise read path, write current control, and data protection circuitry for as many as 8 channels. The SSI 32R516 requires +5V and +12V power supplies and is available in a variety of packages.

The SSI 32R516R performs the same function as the SSI 32R516 with the addition of internal 650Ω damping resistors. The SSI 32R516M and SSI 32R516RM are functionally equivalent to the SSI 32R516 and SSI 32R516R however, they have the mirror image pin arrangement to simplify layout when using multiple devices.

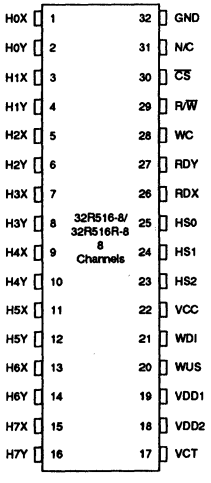
FEATURES

- **High performance**
  - **Read mode gain = 120 V/V**
  - **Input noise = 1.3 nV/√Hz maximum**
  - **Input capacitance = 18 pF**
  - **Write current range = 10 mA to 60 mA**
- **Enhanced system write to read recovery time**
- **Power supply fault protection**
- **Pin compatible with the SSI 32R501 & SSI 32R511**
- **Designed for center-tapped ferrite or MIG heads**
- **Programmable write current source**
- **Easily multiplexed for larger systems**
- **Includes write unsafe detection**
- **TTL compatible control signals**
- **+5V, +12V power supplies**
- **Mirror image pin arrangements**

BLOCK DIAGRAM



PIN DIAGRAM



32-LEAD SOW

CAUTION: Use handling procedures necessary for a static sensitive component.

CIRCUIT OPERATION

The SSI 32R516 gives the user the ability to address up to 8 center-tapped ferrite heads and provide write drive or read amplification. Head selection and mode control is accomplished using the HSn, $\overline{CS}$ and R/$\overline{W}$ inputs as shown in tables 1 & 2. Internal pullups are provided for the $\overline{CS}$ & R/$\overline{W}$ inputs to force the device into a non-writing condition if either control line is opened accidentally.

TABLE 1: Mode Select

$\overline{CS}$	R/$\overline{W}$	MODE
0	0	Write
0	1	Read
1	X	Idle

TABLE 2: Head Select

HS2	HS1	HS0	HEAD
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

0 = Low level 1 = High level

WRITE MODE

Taking both $\overline{CS}$ and R/$\overline{W}$ low selects write mode which configures the SSI 32R516 as a current switch and activates the Write Unsafe (WUS) detector circuitry. Write current is toggled between the X and Y side of the selected head on each high to low transition of the Write Data Input (WDI). Note that a preceding read mode selection initializes the Write Data Flip-Flop, WDFF, to pass write current through the "X" side of the head. The zero-peak write current magnitude is programmed by an external resistor Rwc from pin WC to GND and is given by:

Iw = K/Rwc, where K = Write Current Constant

The Write Unsafe detection circuitry monitors voltage transitions at the selected head connections and flags any of the following conditions as a high level on the Write Unsafe open collector output:

- Head open
- Head center tap open
- WDI frequency too low
- Device in read mode
- Device not selected
- No write current

Two negative transitions on WDI, after the fault is corrected, will clear the WUS flag.

To further assure data security a voltage fault detection circuit prevents application of write current during power loss or power sequencing.

To enhance write to read recovery time the change in RDX, RDY common mode voltage is minimized by biasing these outputs to a level within the read mode range when in write mode.

Power dissipation in write mode may be reduced by placing a resistor (RCT) between VDD1 & VDD2. The optimum resistor value is 82Ω x 60/Iw (Iw in mA). At low write currents (<15 mA) read mode dissipation is higher than write mode and RCT, though recommended, may not be considered necessary. In this case VDD2 is connected directly to VDD1.

READ MODE

Taking $\overline{CS}$ low and R/$\overline{W}$ high selects read mode which configures the SSI 32R516 as a low noise differential amplifier for the selected head. The RDX and RDY outputs are driven by emitter followers and are in phase with the "X" and "Y" head ports. These outputs should be AC coupled to the load. The internal write current source is gated off in read mode eliminating the need for any external gating.

Read mode selection also initializes the Write Data Flip-Flop (WDFF) to pass write current through the "X" side of the head at a subsequent write mode selection.

IDLE MODE

Taking $\overline{CS}$ high selects the idle mode which switches the RDX, RDY outputs into a high impedance state and deactivates the internal write current source. This facilitates multi-device installations by allowing the read outputs to be wire OR'ed and the write current programming resistor to be common to all devices.

PIN DESCRIPTIONS

NAME	I/O	DESCRIPTION
HS0-HS2	I	Head Select
$\overline{CS}$	I	Chip Select: a low level enables device
R/$\overline{W}$	I	Read/Write: a high level selects read mode
WUS	O*	Write Unsafe: a high level indicates an unsafe writing condition
WDI	I	Write Data In: negative transition toggles direction of head current
H0X-H7X H0Y-H7Y	I/O	X,Y head connections
RDX, RDY	O*	X, Y Read Data: differential read signal out
WC	*	Write Current: used to set the magnitude of the write current
VCT	-	Voltage Center Tap: voltage source for head center tap
VCC	-	+5V
VDD1	-	+12V
VDD2	-	Positive power supply for the center tap voltage source
GND	-	Ground

*When more than one R/W device is used, these signals can be wire OR'ed.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (All voltages referenced to GND. Currents into device are positive.)

PARAMETER		VALUE	UNITS
DC Supply Voltage	VDD1	-0.3 to +14	VDC
DC Supply Voltage	VDD2	-0.3 to +14	VDC
DC Supply Voltage	VCC	-0.3 to +6	VDC
Digital Input Voltage Range	VIN	-0.3 to VCC + 0.3	VDC
Head Port Voltage Range	VH	-0.3 to VDD1 + 0.3	VDC
WUS Pin Voltage Range	Vwus	-0.3 to +14	VDC
Write Current Zero Peak	IW	90	mA
RDX, RDy Output Current	Io	-10	mA
VCT Output Current	IVCT	-90	mA
WUS Output Current	Iwus	+12	mA
Storage Temperature Range	Tstg	-65 to 150	°C
Lead Temperature PDIP, Flat Pack (10 sec Soldering)		260	°C
Package Temperature PLCC, SO (20 sec Reflow)		215	°C

RECOMMENDED OPERATION CONDITIONS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
DC Supply Voltage	VDD1		10.8	12.0	13.2	VDC
DC Supply Voltage	VCC		4.5	5.0	5.5	VDC
Head Inductance	Lh		5		10	µH
Damping Resistor	RD	32R516 only	500		2000	Ω
RCT Resistor	RCT*	Iw = 60 mA		82		Ω
Write Current	IW		10		60	mA
Junction Temperature Range	Tj		+25		+135	°C

*For Iw = 60 mA. At other Iw levels refer to Applications Information that follows this specification.

DC CHARACTERISTICS
(Unless otherwise specified, recommended operating conditions apply.)

POWER SUPPLY

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VCC Supply Current	Read/Idle Mode			30	mA
	Write Mode			30	mA
VDD Supply Current	Idle Mode			20	mA
(sum of VDD1 and VDD2)	Read Mode			40	mA
	Write Mode			20 + Iw	mA
Power Dissipation (Tj = +125°C)	Idle Mode			400	mW
	Read Mode			620	mW
	Write Mode, IW = 45 mA, RCT = 0Ω			800	mW
	Write Mode, IW = 45 mA, RCT = 110Ω			610	mW
	Write Mode, IW = 60 mA RCT = 82Ω			680	mW

DC CHARACTERISTICS (continued)

DIGITAL I/O

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
VIL	Input Low Voltage				0.8	VDC
VIH	Input High Voltage		2.0		VCC + 0.3	VDC
IIL	Input Low Current	VIL = 0.8V	-0.4			mA
IIH	Input High Current	VIH = 2.0V			100	µA
VOL	WUS Output Low Voltage	IOL = 8 mA			0.5	VDC
IOH	WUS Output High Current	VOH = 5.0V			100	µA

WRITE MODE

Center Tap Voltage VCT	Write Mode		6.9		VDC
Head Current (per side)	Write Mode, 0 ≤ VCC ≤ 3.7V, 0 ≤ VDD1 ≤ 8.7V	-200		200	µA
Write Current Range		10		60	mA
Write Current Constant "K"	IW = 10 - 45 mA	2.375		2.625	
Write Current Constant "K"	IW = 45 - 60 mA	2.3		2.625	
Iwc to Head Current Gain			0.99		mA/mA
Unselected Head Leakage Current				85	µA
RDX, RDY Output Offset Voltage	Write/Idle Mode	-20		+20	mV
RDX, RDY Common Mode Output Voltage	Write/Idle Mode		5.5		VDC
RDX, RDY Leakage	RDX, RDY = 6V Write/Idle Mode	-100		100	µA

READ MODE

Center Tap Voltage	Read Mode		4.2		VDC
Head Current (per side)	Read or Idle Mode 0 ≤ VCC ≤ 5.5V 0 ≤ VDD1 ≤ 13.2V	-200		200	µA
Input Bias Current (per side)				45	µA
Input Offset Voltage	Read Mode	-4		+4	mV
Common Mode Output Voltage	Read Mode	4.5	5.5	6.5	VDC

DYNAMIC CHARACTERISTICS AND TIMING
(Unless otherwise specified, recommended operating conditions apply and IW = 35 mA, Lh = 5 µH, Rd = 750Ω (32R516) only, f(WDI) = 5 MHz, CL(RDX, RDY) ≤ 35 pF.)

WRITE MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Differential Head Voltage Swing		7.0			V(pk)
Unselected Head Transient Current				2	mA(pk)
Differential Output Capacitance				15	pF
Differential Output Resistance	32R516	10K			Ω
	32R516R	430	650	870	Ω
WDI Transition Frequency	WUS = low	125			kHz

READ MODE

Differential Voltage Gain	Vin = 1 mVpp @ 300 kHz, RL(RDX), RL(RDY) = 1 KΩ	100	120	140	V/V
Dynamic Range	AC Input Voltage, Vi, Where Gain Falls by 10%. V + f = 300 KHz	-3			mVpp
Bandwidth (-3dB)	|Zs| < 5Ω, Vin = 1 mVpp	30			MHz
Input Noise Voltage	BW = 15 MHz, Lh = 0, Rh = 0		1.0	1.3	$nV/\sqrt{Hz}$
Differential Input Capacitance	f = 5 MHz		14	18	pF
Differential Input Resistance	32R516, f = 5 MHz	2K			Ω
Differential Input Resistance	32R516R, f = 5 MHz	350		800	Ω
Common Mode Rejection Ratio	Vcm = VCT + 100 mVpp @ 5 MHz	50			dB
Power Supply Rejection Ratio	100 mVpp @ 5 MHz on VDD1, VDD2 or VCC	45			dB
Channel Separation	Unselected Channels: Vin=100 mVpp @ 5 MHz; Selected Channel: Vin = 0 mVpp	45			dB
Single Ended Output Resistance	f = 5 MHz			30	Ω
Output Current	AC Coupled Load, RDX to RDY	±2.1			mA

DYNAMIC CHARACTERISTICS AND TIMING (continued)

SWITCHING CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
R/$\overline{W}$ To Write	Delay to 90% of Write Current		.15	.7	µs
R/$\overline{W}$ to Read	Delay to 90% of 100 mV, 10 MHz Read Signal Envelope or to 90% decay of Write Current		.25	.7	µs
$\overline{CS}$ to Select	Delay to 90% of Write Current or to 90% of 100 mV, 10 MHz Read Signal Envelope		.2	1.0	µs
$\overline{CS}$ to Unselect	Delay to 90% Decay of Write Current		.1	1.0	µs
HS0 - HS2 to any head	Delay to 90% of 100 mV, 10 MHz Read Signal Envelope		.25	1.0	µs
WUS, Safe to Unsafe - TD1	Iw = 35 mA	1.6		8.0	µs
WUS, Unsafe to Safe - TD2	Iw = 35 mA			1.0	µs
Head Current (Lh = 0 µH, Rh = 0Ω)					
Prop. Delay - TD3	From 50% Points			25	ns
Asymmetry	WDI has 50% Duty Cycle and 1ns Rise/Fall Time			1	ns
Rise/Fall Time	10% - 90% Points			20	ns

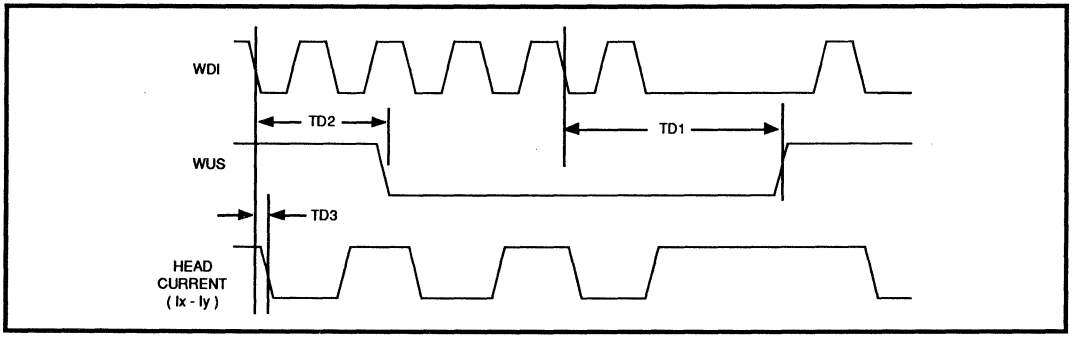
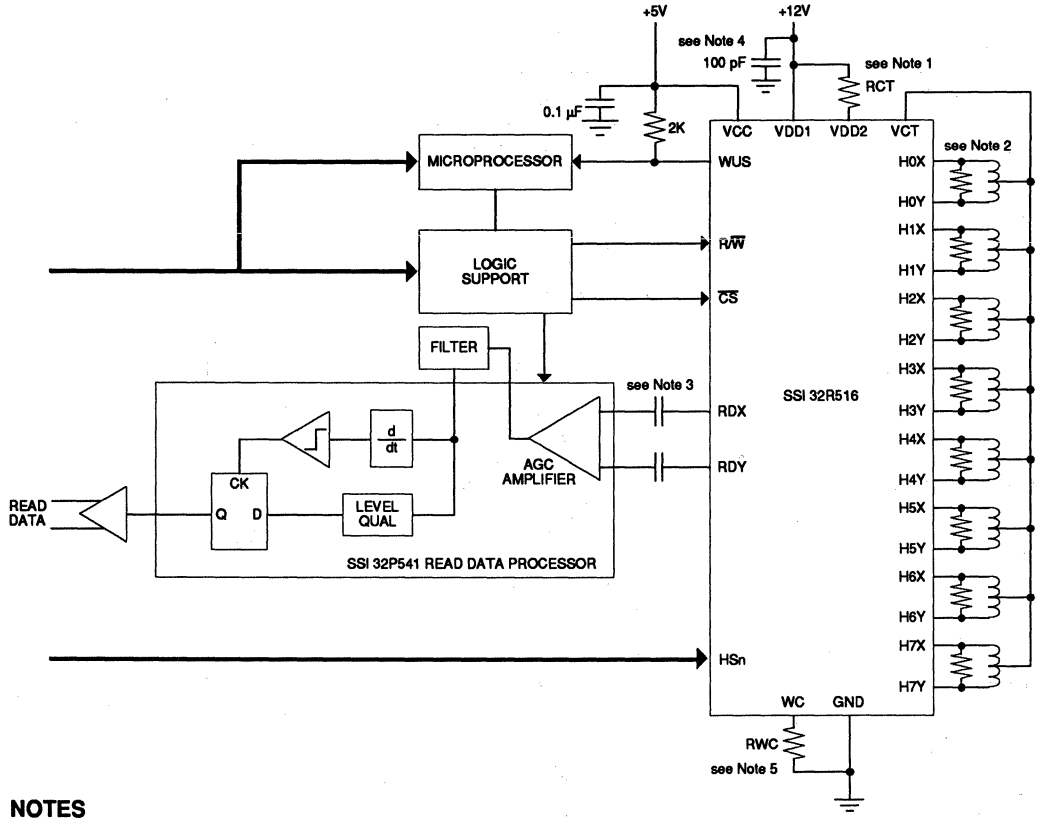


FIGURE 1: Write Mode Timing Diagram

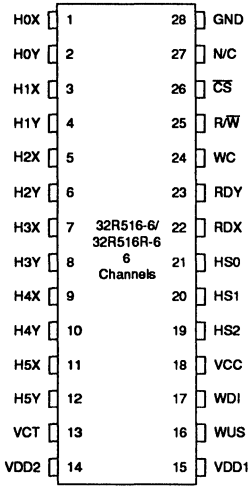


NOTES

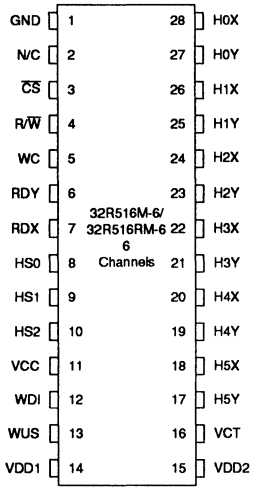
1. An external resistor, RCT, given by; RCT = 82 (60/Iw) where Iw is the zero-peak write current in mA, can be used to limit internal power dissipation. Otherwise connect VDD2 to VDD1.
2. Damping resistors not required on 32R516R versions.
3. Limit DC current from RDX and RDY to 100 µA and load capacitance to 20 pF. In multi-chip application these outputs can be wire-OR'ed.
4. The power bypassing capacitor must be located close to the 32R516 with its ground returned directly to device ground, with as short a path as possible.
5. To reduce ringing due to stray capacitance this resistor should be located close to the 32R516. Where this is not desirable a series resistor can be used to buffer a long WC line. In multi-chip applications a single resistor common to all chips may be used.

FIGURE 2: Applications Information

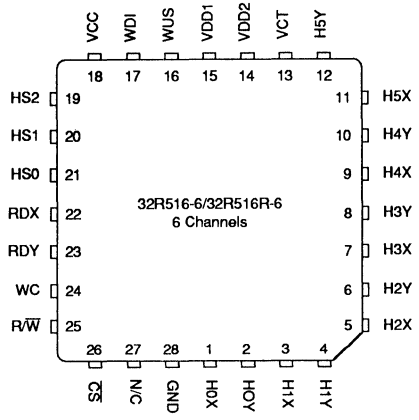
PACKAGE PIN DESIGNATIONS (Top View)



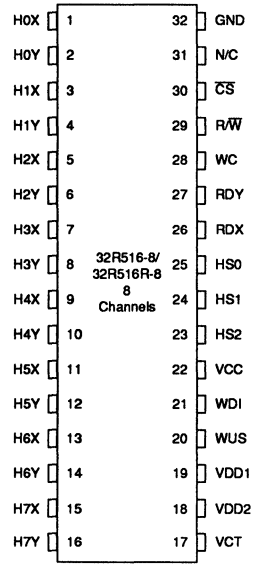
28-Lead SOL



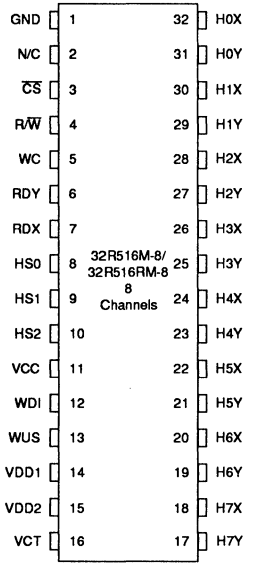
28-Lead SOL
Mirror Image



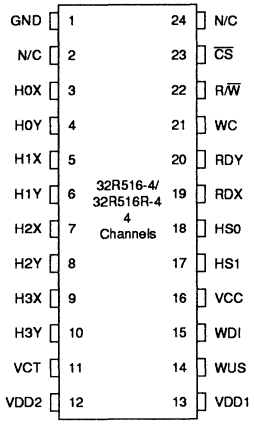
28-Lead PLCC



32-Lead SOW

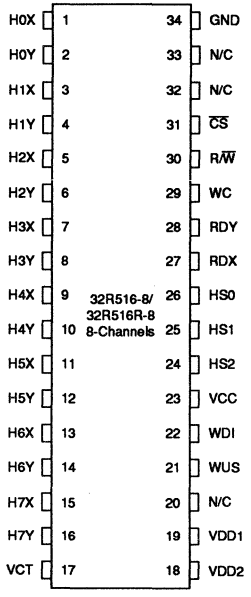


32-Lead SOW
Mirror Image

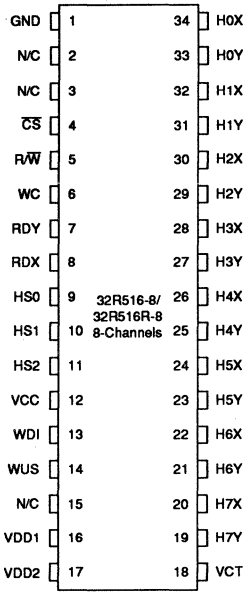


24-Lead SOL

PACKAGE PIN DESIGNATIONS (Continued)



34-Lead SOL



34-Lead SOL
Mirror Image

THERMAL CHARACTERISTICS: Øja

24-lead	SOL	80°C/W
28-lead	PLCC	65°C/W
	SOL	70°C/W
32-lead	SOW	55°C/W
34-lead	SOL	50°C/W
44-lead	PLCC	60°C/W

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32R516		
4-Channel SOL	32R516-4CL	32R516-4CL
6-Channel PLCC	32R516-6CH	32R516-6CH
6-Channel SOL	32R516-6CL	32R516-6CL
8-Channel SOW	32R516-8CW	32R516-8CW
8-Channel SOL	32R516-8CL	32R516-8CL
SSI 32R516R		
4-Channel SOL	32R516R-4CL	32R516R-4CL
6-Channel PLCC	32R516R-6CH	32R516R-6CH
6-Channel SOL	32R516R-6CL	32R516R-6CL
8-Channel SOW	32R516R-8CW	32R516R-8CW
8-Channel SOL	32R516R-8CL	32R516R-8CL
SSI 32R516M		
6-Channel SOL	32R516M-6CL	32R516M-6CL
8-Channel SOW	32R516M-8CW	32R516M-8CW
8-Channel SOL	32R516M-8CL	32R516M-8CL
SSI 32R516RM		
6-Channel SOL	32R516RM-6CL	32R516RM-6CL
8-Channel SOW	32R516RM-8CW	32R516RM-8CW
8-Channel SOL	32R516RM-8CL	32R516RM-8CL

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 731-7110, FAX (714) 573-6914

Notes:

silicon systems®
A TDK Group Company

SSI 32R5161R
10-Channel Ferrite/MIG Read/Write Device

Preliminary Data

1

November 1991

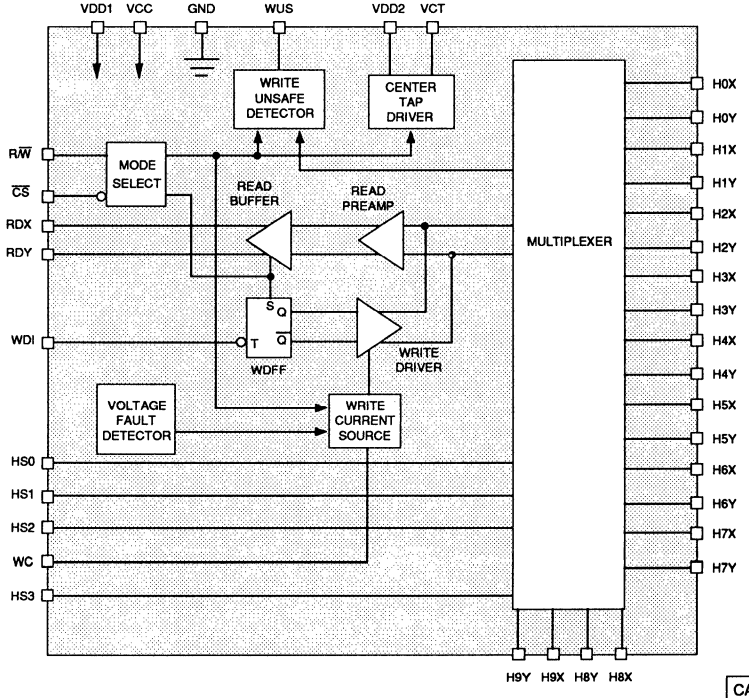
DESCRIPTION

The SSI 32R5161R is a bipolar monolithic integrated circuit designed for use with a center-tapped ferrite or MIG recording heads. The SSI 32R5161R offers the performance upgrades of the SSI 32R511 along with improved head port characteristics and increased read gain. It provides a low noise read path, write current control, and data protection circuitry for as many as 10 channels. The SSI 32R5161R requires +5V and +12V power supplies and is available in a variety of packages.

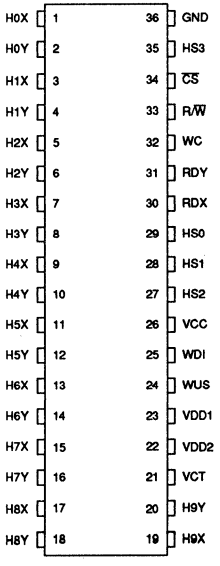
FEATURES

- **High performance**
  - **Read mode gain = 150 V/V**
  - **Input noise = 1.3 nV/√Hz maximum**
  - **Input capacitance = 18 pF**
  - **Write current range = 10 mA to 60 mA**
- **Enhanced system write to read recovery time**
- **Power supply fault protection**
- **Designed for center-tapped ferrite or MIG heads**
- **Programmable write current source**
- **Easily multiplexed for larger systems**
- **Includes write unsafe detection**
- **TTL compatible control signals**
- **+5V, +12V power supplies**

BLOCK DIAGRAM



PIN DIAGRAM



36-LEAD SOM

CAUTION: Use handling procedures necessary for a static sensitive component.

SSI 32R5161R
10-Channel Ferrite/MIG
Read/Write Device

CIRCUIT OPERATION

The SSI 32R5161R gives the user the ability to address up to 10 center-tapped ferrite heads and provide write drive or read amplification. Head selection and mode control is accomplished using the HSn, $\overline{CS}$ and R/$\overline{W}$ inputs as shown in tables 1 & 2. Internal pullups are provided for the $\overline{CS}$ & R/$\overline{W}$ inputs to force the device into a non-writing condition if either control line is opened accidentally.

TABLE 1: Mode Select

$\overline{CS}$	R/$\overline{W}$	MODE
0	0	Write
0	1	Read
1	X	Idle

TABLE 2: Head Select

HS3	HS2	HS1	HS0	HEAD
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9

0 = Low level 1 = High level

WRITE MODE

Taking both $\overline{CS}$ and R/$\overline{W}$ low selects write mode which configures the SSI 32R5161R as a current switch and activates the Write Unsafe (WUS) detector circuitry. Write current is toggled between the X and Y side of the selected head on each high to low transition of the Write Data Input (WDI). Note that a preceding read mode selection initializes the Write Data Flip-Flop, WDFF, to pass write current through the "X" side of the head. The zero-peak write current magnitude is programmed by an external resistor Rwc from pin WC to GND and is given by:

Iw = K/Rwc, where K = Write Current Constant

The Write Unsafe detection circuitry monitors voltage transitions at the selected head connections and flags any of the following conditions as a high level on the Write Unsafe open collector output:

- Head open
- Head center tap open
- WDI frequency too low
- Device in read mode
- Device not selected
- No write current

Two negative transitions on WDI, after the fault is corrected, will clear the WUS flag.

To further assure data security a voltage fault detection circuit prevents application of write current during power loss or power sequencing.

To enhance write to read recovery time the change in RDX, RDY common mode voltage is minimized by biasing these outputs to a level within the read mode range when in write mode.

Power dissipation in write mode may be reduced by placing a resistor (RCT) between VDD1 & VDD2. The optimum resistor value is 82Ω x 60/Iw (Iw in mA). At low write currents (<15 mA) read mode dissipation is higher than write mode and RCT, though recommended, may not be considered necessary. In this case VDD2 is connected directly to VDD1.

READ MODE

Taking $\overline{CS}$ low and R/$\overline{W}$ high selects read mode which configures the SSI 32R5161R as a low noise differential amplifier for the selected head. The RDX and RDY outputs are driven by emitter followers and are in phase with the "X" and "Y" head ports. These outputs should be AC coupled to the load. The internal write current source is gated off in read mode eliminating the need for any external gating.

Read mode selection also initializes the Write Data Flip-Flop (WDFF) to pass write current through the "X" side of the head at a subsequent write mode selection.

IDLE MODE

Taking $\overline{CS}$ high selects the idle mode which switches the RDX, RDY outputs into a high impedance state and deactivates the internal write current source. This facilitates multi-device installations by allowing the read outputs to be wire OR'ed and the write current programming resistor to be common to all devices.

PIN DESCRIPTION

NAME	I/O	DESCRIPTION
HS0-HS2	I	Head Select
$\overline{CS}$	I	Chip Select: a low level enables device
R/$\overline{W}$	I	Read/Write: a high level selects read mode
WUS	O*	Write Unsafe: a high level indicates an unsafe writing condition
WDI	I	Write Data In: negative transition toggles direction of head current
H0X-H7X H0Y-H7Y	I/O	X,Y head connections
RDX, RDY	O*	X, Y Read Data: differential read signal out
WC	*	Write Current: used to set the magnitude of the write current
VCT	-	Voltage Center Tap: voltage source for head center tap
VCC	-	+5V
VDD1	-	+12V
VDD2	-	Positive power supply for the center tap voltage source
GND	-	Ground

*When more than one R/W device is used, these signals can be wire OR'ed.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (All voltages referenced to GND. Currents into device are positive.)

PARAMETER		VALUE	UNITS
DC Supply Voltage	VDD1	-0.3 to +14	VDC
DC Supply Voltage	VDD2	-0.3 to +14	VDC
DC Supply Voltage	VCC	-0.3 to +6	VDC
Digital Input Voltage Range	VIN	-0.3 to VCC + 0.3	VDC
Head Port Voltage Range	VH	-0.3 to VDD1 + 0.3	VDC
WUS Pin Voltage Range	Vwus	-0.3 to +14	VDC
Write Current Zero Peak	IW	90	mA
RDX, RDy Output Current	Io	-10	mA
VCT Output Current	IVCT	-90	mA
WUS Output Current	Iwus	+12	mA
Storage Temperature Range	Tstg	-65 to 150	°C
Lead Temperature PDIP, Flat Pack (10 sec Soldering)		260	°C
Package Temperature PLCC, SO (20 sec Reflow)		215	°C

RECOMMENDED OPERATION CONDITIONS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
DC Supply Voltage	VDD1		10.8	12.0	13.2	VDC
DC Supply Voltage	VCC		4.5	5.0	5.5	VDC
Head Inductance	Lh		5		10	µH
RCT Resistor	RCT*	Iw = 60 mA		82		Ω
Write Current	IW		10		60	mA
Junction Temperature Range	Tj		+25		+135	°C

*For Iw = 60 mA. At other Iw levels refer to Applications Information that follows this specification.

DC CHARACTERISTICS

(Unless otherwise specified, recommended operating conditions apply.)

POWER SUPPLY

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VCC Supply Current	Read/Idle Mode			30	mA
	Write Mode			30	mA
VDD Supply Current	Idle Mode			20	mA
(sum of VDD1 and VDD2)	Read Mode			40	mA
	Write Mode			20 + Iw	mA
Power Dissipation (Tj = +125°C)	Idle Mode			400	mW
	Read Mode			620	mW
	Write Mode, IW = 45 mA, RCT = 0Ω			800	mW
	Write Mode, IW = 45 mA, RCT = 110Ω			610	mW
	Write Mode, IW = 60 mA RCT = 82Ω			680	mW

DC CHARACTERISTICS (continued)

DIGITAL I/O

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
VIL	Input Low Voltage				0.8	VDC
VIH	Input High Voltage		2.0		VCC + 0.3	VDC
IIL	Input Low Current	VIL = 0.8V	-0.4			mA
IIH	Input High Current	VIH = 2.0V			100	µA
VOL	WUS Output Low Voltage	IOL = 8 mA			0.5	VDC
IOH	WUS Output High Current	VOH = 5.0V			100	µA

WRITE MODE

Center Tap Voltage	VCT	Write Mode		6.9		VDC
Head Current (per side)		Write Mode, 0 ≤ VCC ≤ 3.7V, 0 ≤ VDD1 ≤ 8.7V	-200		200	µA
Write Current Range			10		60	mA
Write Current Constant "K"		IW = 10 - 45 mA	2.375		2.625	
Write Current Constant "K"		IW = 45 - 60 mA	2.3		2.625	
Iwc to Head Current Gain				0.99		mA/mA
Unselected Head Leakage Current					85	µA
RDX, RDY Output Offset Voltage		Write/Idle Mode	-20		+20	mV
RDX, RDY Common Mode Output Voltage		Write/Idle Mode		5.5		VDC
RDX, RDY Leakage		RDX, RDY = 6V Write/Idle Mode	-100		100	µA

READ MODE

Center Tap Voltage	Read Mode		4.2		VDC
Head Current (per side)	Read or Idle Mode 0 ≤ VCC ≤ 5.5V 0 ≤ VDD1 ≤ 13.2V	-200		200	µA
Input Bias Current (per side)				45	µA
Input Offset Voltage	Read Mode	-4		+4	mV
Common Mode Output Voltage	Read Mode	4.5	5.5	6.5	VDC

DYNAMIC CHARACTERISTICS AND TIMING

(Unless otherwise specified, recommended operating conditions apply and IW = 35 mA, Lh = 5 µH, f(WDI) = 5 MHz, CL(RDX, RDY) ≤ 35 pF.)

WRITE MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Differential Head Voltage Swing		7.0			V(pk)
Unselected Head Transient Current				2	mA(pk)
Differential Output Capacitance				15	pF
Differential Output Resistance		430	650	870	Ω
WDI Transition Frequency	WUS = low	125			kHz

READ MODE

Differential Voltage Gain	Vin = 1 mVpp @ 300 kHz, RL(RDX), RL(RDY) = 1 KΩ	120	150	180	V/V
Dynamic Range	AC Input Voltage, Vi, Where Gain Falls by 10%. V + f = 300 KHz	-3			mVpp
Bandwidth (-3dB)	|Zs| < 5Ω, Vin = 1 mVpp	30			MHz
Input Noise Voltage	BW = 15 MHz, Lh = 0, Rh = 0		1.0	1.3	$nV/\sqrt{Hz}$
Differential Input Capacitance	f = 5 MHz		14	18	pF
Differential Input Resistance	32R5161R, f = 5 MHz	350		800	Ω
Common Mode Rejection Ratio	Vcm = VCT + 100 mVpp @ 5 MHz	50			dB
Power Supply Rejection Ratio	100 mVpp @ 5 MHz on VDD1, VDD2 or VCC	45			dB
Channel Separation	Unselected Channels: Vin=100 mVpp @ 5 MHz; Selected Channel: Vin = 0 mVpp	45			dB
Single Ended Output Resistance	f = 5 MHz			30	Ω
Output Current	AC Coupled Load, RDX to RDY	±2.1			mA

DYNAMIC CHARACTERISTICS AND TIMING (continued)

SWITCHING CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
R/$\overline{W}$ To Write	Delay to 90% of Write Current		.15	.7	µs
R/$\overline{W}$ to Read	Delay to 90% of 100 mV, 10 MHz Read Signal Envelope or to 90% decay of Write Current		.25	.7	µs
$\overline{CS}$ to Select	Delay to 90% of Write Current or to 90% of 100 mV, 10 MHz Read Signal Envelope		.2	1.0	µs
$\overline{CS}$ to Unselect	Delay to 90% Decay of Write Current		.1	1.0	µs
HS0 - HS2 to any head	Delay to 90% of 100 mV, 10 MHz Read Signal Envelope		.25	1.0	µs
WUS, Safe to Unsafe - TD1	Iw = 35 mA	1.6		8.0	µs
WUS, Unsafe to Safe - TD2	Iw = 35 mA			1.0	µs
Head Current (Lh = 0 µH, Rh = 0Ω)					
Prop. Delay - TD3	From 50% Points			25	ns
Asymmetry	WDI has 50% Duty Cycle and 1ns Rise/Fall Time			1	ns
Rise/Fall Time	10% - 90% Points			20	ns

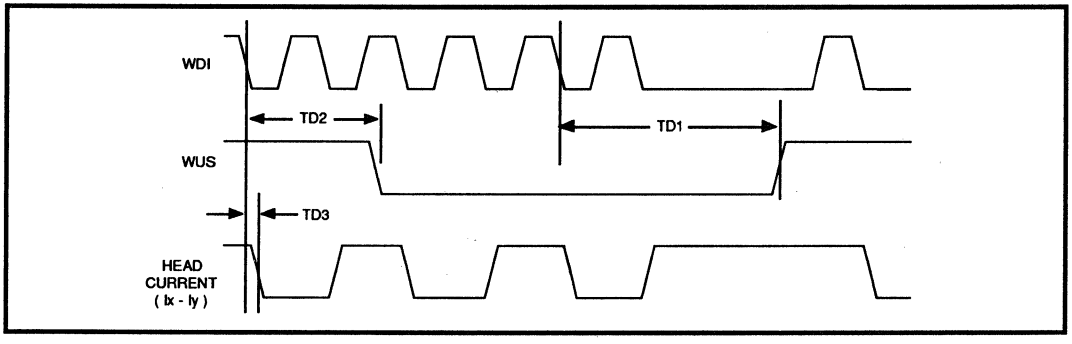
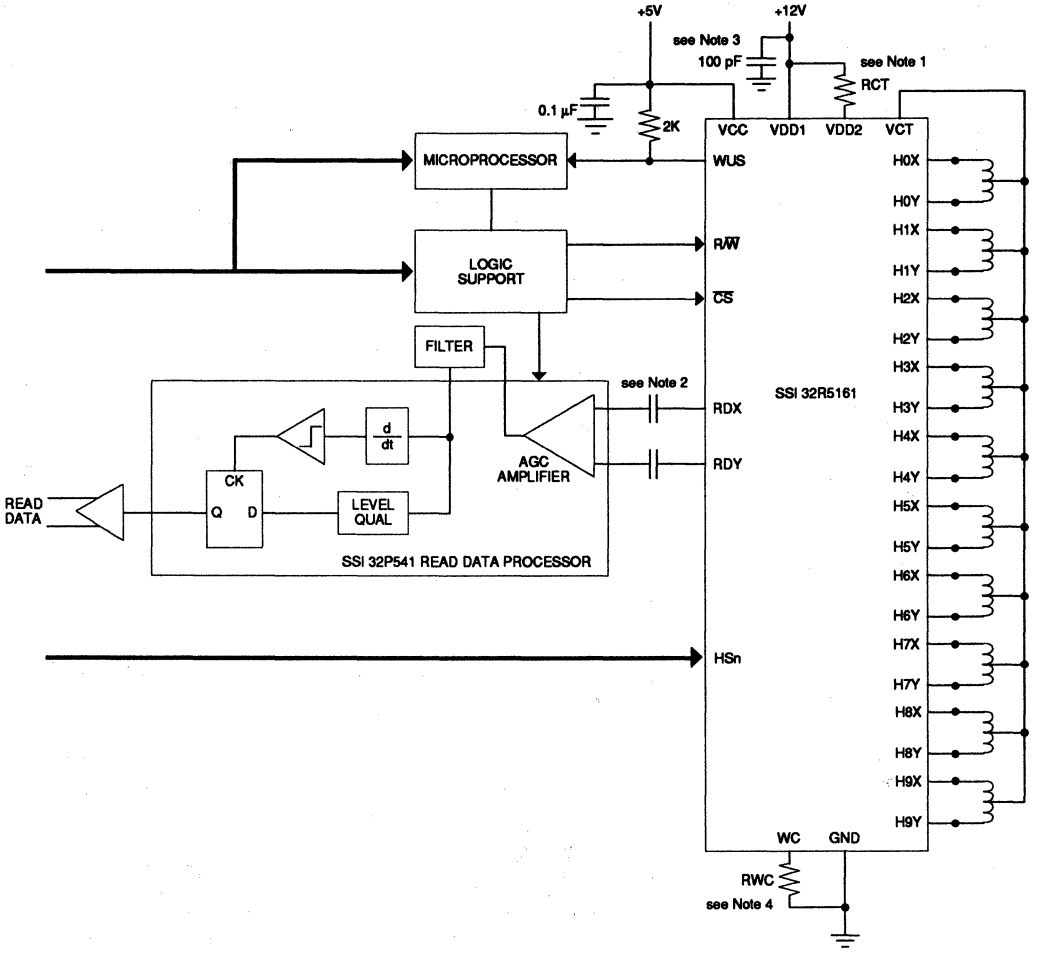


FIGURE 1: Write Mode Timing Diagram



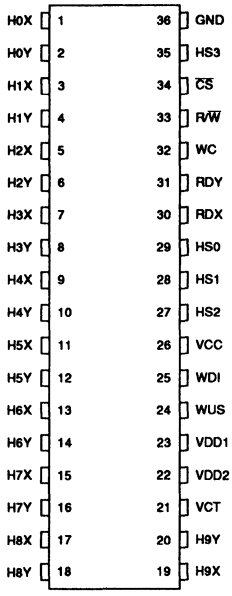
NOTES

1. An external resistor, RCT, given by; RCT = 82 (60/Iw) where Iw is the zero-peak write current in mA, can be used to limit internal power dissipation. Otherwise connect VDD2 to VDD1.
2. Limit DC current from RDX and RDY to 100 µA and load capacitance to 20 pF. In multi-chip application these outputs can be wire-OR'ed.
3. The power bypassing capacitor must be located close to the 32R5161R with its ground returned directly to device ground, with as short a path as possible.
4. To reduce ringing due to stray capacitance this resistor should be located close to the 32R5161R. Where this is not desirable a series resistor can be used to buffer a long WC line. In multi-chip applications a single resistor common to all chips may be used.

FIGURE 2: Applications Information

PACKAGE PIN DESIGNATIONS

(Top View)



36-Lead SOM

THERMAL CHARACTERISTICS: Øja

36-lead	SOM	50°C/W

ORDERING INFORMATION

PART DESCRIPTION	ORDERING NO.	PKG. MARK
SSI 32R5161R Read/Write Device		
10-Channel SOM	32R5161R-10CM	32R5161R-10CM

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 731-7110, FAX (714) 573-6914

Notes:

silicon systems®
A TDK Group Company

SSI 32R524R
8-Channel Thin Film Read/Write Device

1

November 1991

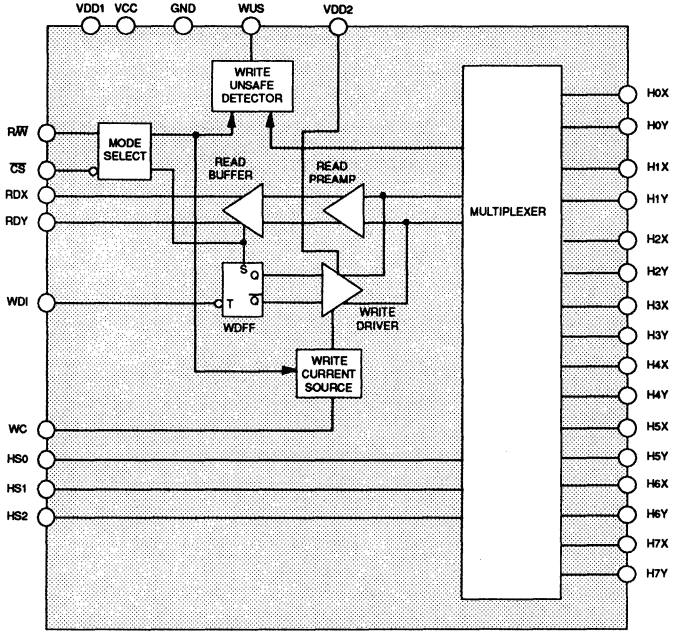
DESCRIPTION

The SSI 32R524R Read/Write device is a bipolar monolithic integrated circuit designed for use with two terminal thin film recording heads. It provides a low noise read amplifier, write current control and data protection circuitry for eight channels. Power supply fault protection is provided by disabling the write current generator during power sequencing. System write to read recovery time is significantly improved by controlling the read channel common mode output voltage shift in the write mode. It requires +5V and +12V power supplies and is available in a variety of package configurations. A mirror image pinout option is available to simplify flex circuit layout in multiple R/W device applications. The SSI 32R524R provides internal 740Ω damping resistors.

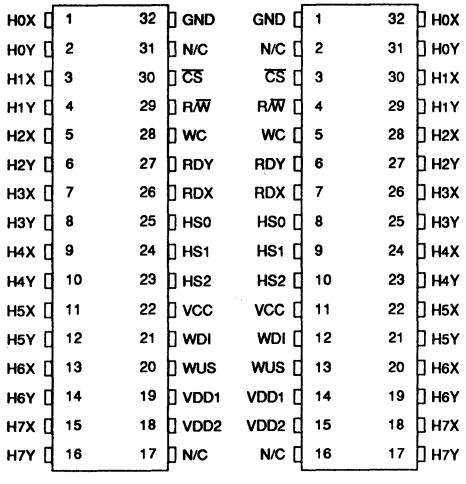
FEATURES

- **High performance:**
  - **Read mode gain = 100V/V**
  - **Input noise = 0.75 nV/√Hz max.**
  - **Input capacitance = 60 pF max.**
  - **Write current range = 20 to 60 mA**
  - **Head voltage swing = 7 Vpp**
  - **Write current rise time = 9 nsec**
- **Enhanced system write to read recovery time**
- **Power supply fault protection**
- **Plug compatible to the SSI 32R501, SSI 32R511 & SSI 32R512**
- **Compatible with two & three terminal thin film heads**
- **Write unsafe detection**
- **+5V, +12V power supplies**
- **Mirror image pinout option**

BLOCK DIAGRAM



PIN DIAGRAM



32-LEAD SOW **32-LEAD SOW MIRROR**

CAUTION: Use handling procedures necessary for a static sensitive component.

CIRCUIT OPERATION

The SSI 32R524R addresses eight two-terminal thin film heads providing write drive or read amplification. Head selection and mode control is accomplished with pins HSn, $\overline{CS}$ and R/$\overline{W}$, as shown in Tables 1 & 2. Internal resistor pullups, provided on pins $\overline{CS}$ and R/$\overline{W}$ will force the device into a non-writing condition if either control line is opened accidentally.

WRITE MODE

The write mode configures the SSI 32R524R as a differential current switch and activates the Write Unsafe (WUS) detection circuitry. Write current is toggled between the X and Y directions of the selected head on each high to low transition on pin WDI, Write Data Input.

A preceding read operation initializes the Write Data Flip Flop (WDFF) to pass write current in the X-direction of the head, which is defined as entering from the Y-side and flowing to the X-side.
The magnitude of the write current (0-pk) given by:

$$Iw = \frac{K}{RWC}$$

where K (Write Current Constant) = 70 ± 5%, is programmed by an external resistor RWC, connected from pin WC to ground. The actual head current Ix, y is given by:

$$Iw,y = \frac{Iw}{1 + Rh/Rd}$$

where:
Rh = head resistance + external wire resistance, and
Rd = damping resistance.

Power supply fault protection improves data security by disabling the write current generator during a voltage fault or power supply sequencing. Additionally, the write unsafe detection circuitry will flag any of the conditions listed below as a high level on the open collector output pin, WUS. Two negative transitions on pin WDI, after the fault is corrected, are required to clear the WUS flag.

- Open head
- WDI frequency too low
- Device not selected
- Device in read mode
- No write current

Power dissipation in Write Mode may be reduced by placing a resistor, Rw, between VDD1 and VDD2. The resistor value should be chosen such that Iw Rw ≤ 3.0V for an accompanying power dissipation reduction of $(Iw)^2$ Rw. If a resistor is not used, VDD2 should be connected to VDD1. Note that Rw will also provide current limiting in the event of a head short.

READ MODE

The read mode configures the SSI 32R524R as a low noise differential amplifier and deactivates the write current generator and write unsafe detection circuitry. The RDX and RDY outputs are emitter followers and are in phase with the "X" and "Y" head ports. These outputs should be AC coupled to the load. The RDX, RDY common mode voltage is maintained in the write mode, minimizing the transient between write mode and read mode, substantially reducing the write to read recovery time in the subsequent Pulse Detection circuitry.

IDLE MODE

The idle mode deactivates the internal write current generator, the write unsafe detector, and switches the RDX, RDY outputs into a high impedance state. This facilitates multiple device applications by enabling the read outputs to be wire OR'ed.

TABLE 1: Mode Select

$\overline{CS}$	R/$\overline{W}$	MODE
0	0	Write
0	1	Read
1	0	Idle
1	1	Idle

TABLE 2: Head Select

HS2	HS1	HS0	HEAD
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

0 = Low level, 1 = High level

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
HS0 - HS2	I	Head Select: selects one of eight heads
$\overline{CS}$	I	Chip Select: a low level enables the device
R/$\overline{W}$	I	Read/Write: a high level selects Read Mode
WUS	O*	Write Unsafe: Open collector output, a high level indicates an unsafe writing condition
WDI	I	Write Data In: a negative transition toggles the direction of the head current
H0X - H7X H0Y - H7Y	I/O	X, Y Head Connections: Current in the X-direction flows into the X-port
RDX, RDY	O*	X, Y Read Data: differential read data output
WC	-	Write Current: used to set the magnitude of the write current
VCC	-	+5V Logic Circuit Supply
VDD1	-	+12V
VDD2	-	Positive Power Supply for Write current drivers
GND	-	Ground
* When more than one R/W device is used, these signals can be wire OR'ed.		

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETER		SYMBOL	VALUE	UNITS
DC Supply Voltage		VDD1, 2	-0.3 to +14	VDC
		VCC	-0.3 to +7	VDC
Write Current		Iw	100	mA
Digital Input Voltage		Vin	-0.3 to VCC +0.3	VDC
Head Port Voltage		VH	-0.3 to VDD2 +0.3	VDC
WUS Pin Voltage Range		Vwus	-0.3 to +14	VDC
Output Current	RDX, RDY	Io	-10	mA
	WUS	Iwus	+12	mA
Storage Temperature		Tstg	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNITS
DC Supply Voltage	VDD1	12 ± 10%	VDC
	VDD2	≥VDD1 - 3.0V	VDC
	VCC	5 ± 10%	VDC
Junction Temperature	Tj	+25 to +135	°C

DC CHARACTERISTICS

Unless otherwise specified, recommended operating conditions apply.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VDD1 Supply Current	Read Mode	-	-	50	mA
	Write Mode	-	-	45	mA
	Idle Mode	-	-	25	mA
VDD2 Supply Current	Read Mode	-	-	200	µA
	Write Mode	-	-	Iw+0.4	mA
	Idle Mode	-	-	200	µA
VCC Supply Current	Read Mode	-	-	60	mA
	Write Mode	-	-	50	mA
	Idle Mode	-	-	45	mA
Power Dissipation (Tj = +135°C)	Read Mode	-	-	900	mW
	Write Mode Iw = 40mA, VDD2 = VDD1	-	-	1300	mW
	Write Mode Iw = 60mA, VDD1 - VDD2 = 3.0V	-	-	1425	mW
	Idle Mode	-	-	500	mW
Input Low Voltage (VIL)		-	-	0.8	VDC
Input High Voltage (VIH)		2.0	-	-	VDC
Input Low Current (IIL)	VIL = 0.8v	-0.8	-	-	mA
Input High Current (IHL)	VIH = 2.0v	-	-	100	µA
WUS Output Low Voltage (VOL)	Iol = 8mA	-	-	0.5	VDC
VDD Fault Voltage		8.5	-	10.0	VDC
VCC Fault Voltage		3.5	-	4.2	VDC
Head Current (HnX, HnY)	Write Mode, 0≤VCC ≤3.5V 0≤VDD1 ≤8.5V	-200	-	+200	µA
	Read/Idle Mode 0≤VCC ≤5.5V 0≤VDD1 ≤13.2V	-200	-	+200	µA

WRITE CHARACTERISTICS
Unless otherwise specified, recommended operating conditions apply, Iw = 40 mA, Lh = 500 nH, Rh = 30Ω and f(WDI) = 5 MHz.

PARAMETER	CONDITIONS	MIN.	NOM	MAX	UNITS
Write Current Constant "K"		66.5	-	73.5	V
Differential Head Voltage Swing		7	-	-	Vpp
Unselected Head Current		-	-	1	mA(pk)
Differential Output Capacitance		-	-	35	pF
Differential Output Resistance		400	740	1000	Ω
WDI Transition Frequency	WUS = low	1.0	-	-	MHz
Write Current Range		20	-	60	mA

READ CHARACTERISTICS
Unless otherwise specified, recommended operating conditions apply, CL (RDX, RDY) < 20 pF and RL (RDX,RDY) = 1 kΩ.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Differential Voltage Gain		Vin=1 mVpp @ 300 kHz	80	100	120	V/V
Bandwidth	-1dB	|Zs|<5Ω, Vin=1 mVpp @ 300 kHz	25	-	-	MHz
	-3dB	|Zs|<5Ω, Vin=1 mVpp @ 300 kHz	45	-	-	MHz
Input Noise Voltage		BW = 15 MHz, Lh = 0, Rh = 0	-	0.55	0.75	nV/√Hz
Differential Input Capacitance		Vin = 1 mVpp, f = 5 MHz	-	-	60	pF
Differential Input Resistance		Vin = 1 mVpp, f = 5 MHz	220	-	-	Ω
Dynamic Range		DC input voltage where gain falls to 90% of its 0 VDC value, Vin = VDC +0.5 mVpp, f = 5 MHz	-3	-	3	mV
Common Mode Rejection Ratio		Vin = 0 VDC+100 mVpp @ 5 MHz	54	-	-	dB
Power Supply Rejection Ratio		100 mVpp @ 5 MHz on VDD1 100 mVpp @ 5 MHz on VCC	54	-	-	dB
Channel Separation		Unselected channels driven with 100 mVpp @ 5 MHz, Vin = 0 mVpp	45	-	-	dB
Output Offset Voltage			-360	-	+360	mV
RDX, RDY Common Mode		Read Mode	Vcc-2.2V	Vcc-1.9V	Vcc-1.6V	VDC
Output Voltage		Write Mode	-	2.9	-	VDC
Single Ended Output Resistance		f = 5 MHz	-	-	30	Ω
Output Current		AC Coupled Load, RDX to RDY	3.2	-	-	mA

SWITCHING CHARACTERISTICS (See Figure 1)
Unless otherwise specified, recommended operating conditions apply, Iw = 40 mA, Lh = 500 nH, Rh = 30Ω and f(WDI) = 5 MHz.

PARAMETER	CONDITIONS	MIN	MAX	UNITS
R/$\overline{W}$				
R/$\overline{W}$ to Write Mode	Delay to 90% of write current	-	0.6	µs
R/$\overline{W}$ to Read Mode	Delay to 90% of 100mV 10MHz Read signal envelope or to 90% decay of write current	-	0.6	µs
$\overline{CS}$				
$\overline{CS}$ to Select	Delay to 90% of write current or to 90% of 100mV 10MHz Read signal envelope	-	0.6	µs
$\overline{CS}$ to Unselect	Delay to 10% of write current	-	0.6	µs
HSn				
HS0, 1, 2 to any Head	Delay to 90% of 100mV 10MHz Read signal envelope	-	0.4	µs
WUS				
Safe to Unsafe - TD1		0.6	5.0	µs
Unsafe to Safe - TD2		-	1	µs
Head Current				
Prop. Delay - TD3	From 50% points, Lh=0µh, Rh=0Ω	-	32	ns
Asymmetry	WDI has 50% duty cycle and 1ns rise/fall time, Lh=0µh, Rh=0Ω	-	1	ns
Rise/Fall Time	10%-90% points, Lh=0µh, Rh=0Ω	-	9	ns
Rise/Fall Time	10%-90% points, R(HnX, HnY)=10Ω	-	10	ns

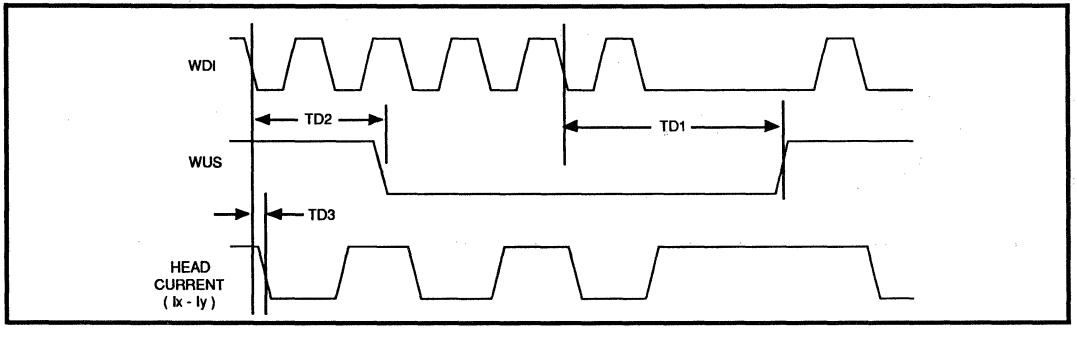


FIGURE 1: Write Mode Timing Diagram

APPLICATIONS INFORMATION

The specifications, provided in the data section, account for the worst case values of each parameter taken individually. In actual operation, the effects of worst case conditions on many parameters correlate. Tables 3 & 4 demonstrate this for several key parameters. Notice that under the conditions of worst case input noise, the higher read back signal resulting from the higher input impedance can compensate for the higher input noise. Accounting for this correlation in your analysis will be more representative of actual performance.

TABLE 3: Key Parameters Under Worst Case Input Noise Conditions

PARAMETER	Tj = 25°C	Tj = 135°C	UNITS
Input Noise Voltage (Max.)	0.5	0.75	$nV/\sqrt{Hz}$
Differential Input Resistance (Min.)	292	318	Ω
Differential Input Capacitance (Max.)	43	48	pF

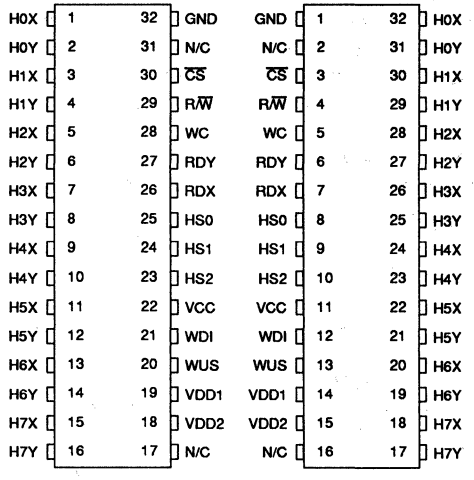
TABLE 4: Key Parameters Under Worst Case Input Impedance Conditions

PARAMETER	Tj = 25°C	Tj = 135°C	UNITS
Input Noise Voltage (Max.)	0.45	0.6	$nV/\sqrt{Hz}$
Differential Input Resistance (Min.)	220	260	Ω
Differential Input Capacitance (Max.)	55	60	pF

SSI 32R524R
8-Channel Thin Film
Read/Write Device

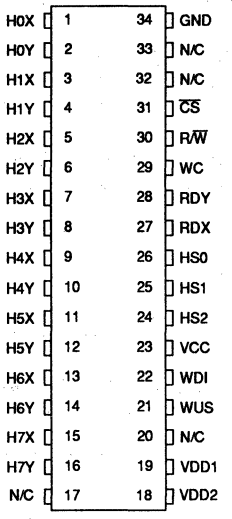
PACKAGE PIN DESIGNATIONS

(Top View)

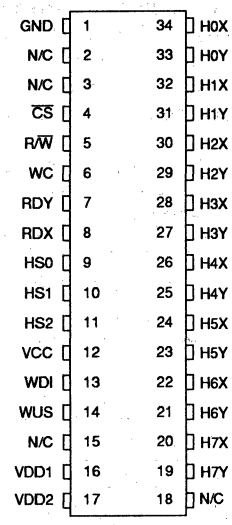


32-LEAD SOW

32-LEAD SOW MIRROR



34-LEAD SOL



34-LEAD SOL MIRROR

THERMAL CHARACTERISTICS: θja

32-Lead SOW	55°C/W
34-Lead SOL	50°C/W

ORDERING INFORMATION

PART DESCRIPTION		ORDER NO.	PKG. MARK
SSI 32R524R	8-Channel SOW	32R524R-8W	32R524R-8W
	8-Channel SOL	32R524R-8L	32R524R-8L
SSI 32R524RM	8-Channel SOW	32R524RM-8W	32R524RM-8W
	8-Channel SOL	32R524RM-8L	32R524RM-8L

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SSI 32R528R
9-Channel Thin Film Read/Write Device
Preliminary Data

1

November 1991

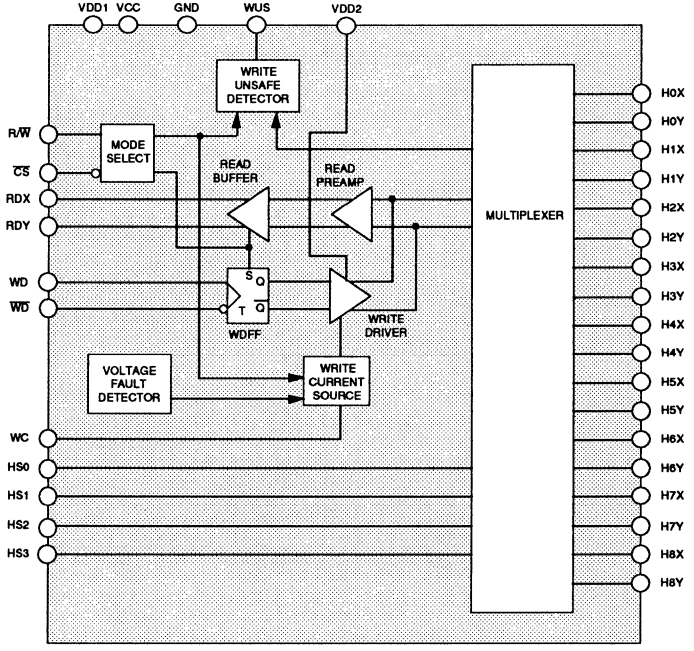
DESCRIPTION

The SSI 32R528R Read/Write device is a bipolar monolithic integrated circuit designed for use with two terminal thin film recording heads. It provides a low noise read amplifier, write current control and data protection circuitry for eight or nine channels. Power supply fault protection is provided by disabling the write current generator during power sequencing. System write to read recovery time is significantly improved by controlling the read channel common mode output voltage shift in the write mode. It requires +5V and +12V power supplies and is available in a 36 SOM package. A mirror image pinout option is available to simplify flex circuit layout in multiple R/W device applications. The SSI 32R528R provides internal 700Ω damping resistors.

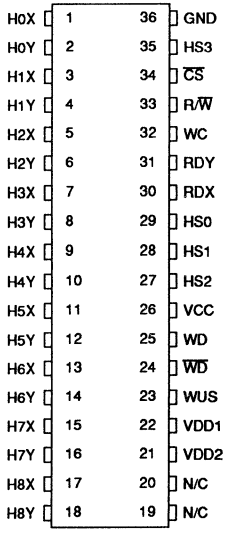
FEATURES

- **High performance:**
  - **Read mode gain = 150 V/V**
  - **Input noise = 0.85 nV/√Hz max.**
  - **Input capacitance = 35 pF max.**
  - **Write current range = 10 mA to 40 mA**
  - **Head voltage swing = 7 Vpp**
  - **Write current rise time = 9 ns**
- **Enhanced system write to read recovery time**
- **Differential ECL-like Write Data input**
- **Power supply fault protection**
- **Compatible with two & three terminal TFH**
- **Write unsafe detection**
- **+5V, +12V power supplies**

BLOCK DIAGRAM



PIN DIAGRAM



36-Lead SOM

CAUTION: Use handling procedures necessary for a static sensitive component.

CIRCUIT OPERATION

The SSI 32R528R addresses up to nine two-terminal thin film heads providing write drive or read amplification. Head selection and mode control is accomplished with pins HSn, $\overline{CS}$ and R/$\overline{W}$, as shown in Tables 1 & 2. Internal resistor pullups, provided on pins $\overline{CS}$ and R/$\overline{W}$ will force the device into a non-writing condition if either control line is opened accidentally.

WRITE MODE

The write mode configures the SSI 32R528R as a current switch and activates the Write Unsafe (WUS) detection circuitry. Write current is toggled between the X and Y direction of the selected head on each low to high transition of the WD, Write Data Input.

A preceding read operation initializes the Write Data Flip Flop (WDFF) to pass write current in the X-direction of the head, i.e. into the X-port.

The magnitude of the write current (0-pk) given by:

$$Iw = \frac{Vwc}{RWC}$$

where Vwc (WC pin voltage) = 1.65V ± 5%, is programmed by an external resistor RWC, connected from pin WC to ground. In multiple device applications, a single RWC resistor may be made common to all devices. The actual head current Ix, y is given by:

$$Ix,y = \frac{Iw}{1 + Rh/Rd}$$

where:
Rh = head resistance + external wire resistance, and
Rd = damping resistance.

Power supply fault protection improves data security by disabling the write current generator during a voltage fault or power supply sequencing. Additionally, the write unsafe detection circuitry will flag any of the conditions listed below as a high level on the open collector output pin, WUS. Two negative transitions on the WD/$\overline{WD}$ lines, after the fault is corrected, are required to clear the WUS flag.

- WD frequency too low
- Device not selected
- Head open
- Device in read mode
- No write current

Power dissipation in Write Mode may be reduced by placing a resistor, Rw, between VDD1 and VDD2. The resistor value should be chosen such that Iw Rw ≤ 3.0V for an accompanying reduction of $(Iw)^2$ Rw in power dissipation. If a resistor is not used, VDD2 should be connected to VDD1. Note that Rw will also provide current limiting in the event of a head short.

READ MODE

The read mode configures the SSI 32R528R as a low noise differential amplifier and deactivates the write current generator and write unsafe detection circuitry. The RDX and RDY outputs are emitter followers and are in phase with the "X" and "Y" head ports. These outputs should be AC coupled to the load. The RDX, RDY common mode voltage is maintained at the write mode value, minimizing the transient between write mode and read mode, substantially reducing the write to read recovery time in the subsequent Pulse Detection circuitry.

IDLE MODE

The idle mode deactivates the internal write current generator, the write unsafe detector and switches the RDX, RDY outputs into a high impedance state. This facilitates multiple device applications by enabling the read outputs to be wire OR'ed and the write current programming resistor to be common to all devices.

TABLE 1: Mode Select

$\overline{CS}$	R/$\overline{W}$	MODE
0	0	Write
0	1	Read
1	0	Idle
1	1	Idle

TABLE 2: Head Select

HS3	HS2	HS1	HS0	HEAD
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8

0 = Low level 1 = High level

PIN DESCRIPTIONS

NAME	TYPE	DESCRIPTION
HS0 - HS3	I	Head Select: TTL level
$\overline{CS}$	I	Chip Select: a low TTL level enables the device
R/$\overline{W}$	I	Read/Write: a high TTL level selects Read mode
WUS	O*	Write Unsafe: Open collector output, a high level indicates an unsafe writing condition
WD, $\overline{WD}$	I	Differential Write Data inputs: a positive transition on WD toggles the direction of the head current
H0X - H8X H0Y - H8Y	I/O	X, Y Head Connections: Current in the X-direction flows into the X-port
RDX, RDY	O*	X, Y Read Data: differential read data output
WC	*	Write Current: used to set the magnitude of the write current
VCC	-	+5V Logic Circuit Supply
VDD1	-	+12V
VDD2	-	Positive Power Supply for Write current drivers
GND	-	Ground

*When more than one R/W device is used, these signals can be wire OR'ed.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation outside these rating limits may permanently damage the device.

PARAMETER		SYMBOL	VALUE	UNITS
DC Supply Voltage		VDD1, 2	-0.3 to +14	VDC
		VCC	-0.3 to +7	VDC
Write Current		Iw	100	mA
Digital Input Voltage		Vin	-0.3 to VCC +0.3	VDC
Head Port Voltage		VH	-0.3 to VDD2 +0.3	VDC
WUS Pin Voltage Range		Vwus	-0.3 to +14	VDC
Output Current	RDX, RDY	Io	-10	mA
	WUS	Iwus	+12	mA
Storage Temperature		Tstg	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNITS
DC Supply Voltage	VDD1	12 ± 10%	VDC
	VDD2	VDD1 - 3.0 to VDD1	VDC
	VCC	5 ± 10%	VDC
Operating Temperature	Tj	0 to +135	°C

DC CHARACTERISTICS
Unless otherwise specified, recommended operating conditions apply.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VDD1 Supply Current	Read Mode	-	-	42	mA
	Write Mode	-	-	50	mA
	Idle Mode	-	-	22	mA
VDD2 Supply Current	Read Mode	-	-	200	µA
	Write Mode	-	-	Iw + 0.4	mA
	Idle Mode	-	-	200	µA
VCC Supply Current	Read Mode	-	-	68	mA
	Write Mode	-	-	48	mA
	Idle Mode	-	-	55	mA
Power Dissipation (Tj = +135°C)	Read Mode	-	-	850	mW
	Write Mode: Iw = 20 mA, VDD2 = VDD1	-	-	1100	mW
	Write Mode: Iw = 40 mA, VDD1 - VDD2 = 3.0V	-	-	1200	mW
	Idle Mode	-	-	550	mW
WD, $\overline{WD}$ Input Low Current (IIL1)	VIL1 = VCC -1.625V			80	µA
WD, $\overline{WD}$ Input High Current (IIH1)	VIH1 = VCC -0.72V			100	µA
WD, $\overline{WD}$ Input Low Voltage (VIL1)		VCC -1.870		VCC -1.625	VDC
WD, $\overline{WD}$ Input High Voltage (VIH1)		VCC -1.00		VCC -0.720	VDC
R/$\overline{W}$, $\overline{CS}$, HS0-HS3	VIL2 = 0.8V	-0.4			mA
Input Low Current (IIL2)					
R/$\overline{W}$, $\overline{CS}$, HS0-HS3 Input High Current (IIH2)	VIH2 = 2.0V			100	µA
R/$\overline{W}$, $\overline{CS}$, HS0-HS3 Input Low Voltage (VIL2)				0.8	VDC
R/$\overline{W}$, $\overline{CS}$, HS0-HS3 Input High Voltage (VIH2)		2.0			VDC

DC CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
WUS Output Low Voltage (VOL)	ILUS = 8.0 mA			0.5	VDC
VDD Fault Voltage		8.5	-	10.0	VDC
VCC Fault Voltage		3.5	-	4.2	VDC
Head Current (HnX, HnY)	Write Mode, 0 ≤ VCC ≤ 3.5V 0 ≤ VDD1 ≤ 8.5V	-200	-	+200	µA
	Read/Idle Mode 0 ≤ VCC ≤ 5.5V 0 ≤ VDD1 ≤ 13.2V	-200	-	+200	µA

WRITE CHARACTERISTICS

Unless otherwise specified, recommended operating conditions apply, Iw = 20 mA, Lh = 1.0 µH, Rh = 30Ω and f(WD) = 5 MHz.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
WC Pin Voltage (Vwc)		1.57	1.65	1.73	V
Differential Head Voltage Swing		7	-	-	Vpp
Unselected Head Current		-	-	1	mA(pk)
Differential Output Capacitance		-	-	25	pF
Differential Output Resistance	32R528R	500	700	950	Ω
WD Transition Frequency	WUS = low	1.7	-	-	MHz
Write Current Range	0 - pk	10	-	40	mA

READ CHARACTERISTICS

Unless otherwise specified, recommended operating conditions apply CL (RDX, RDY) < 20 pF and RL (RDX,RDY) = 1 kΩ.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Differential Voltage Gain		Vin = 1 mVpp @ 1 MHz	125	-	175	V/V
Bandwidth	-1dB	|Zs| < 5Ω, Vin=1 mVpp	25	-	-	MHz
	-3dB	|Zs| < 5Ω, Vin=1 mVpp	45	-	-	MHz
Input Noise Voltage		BW = 15 MHz, Lh = 0, Rh = 0	-	0.62	0.85	nV/√Hz
Differential Input Capacitance		Vin = 1 mVpp, f = 5 MHz	-	-	35	pF
Differential Input Resistance	32R528R	Vin = 1 mVpp, f = 5 MHz	300	-	-	Ω
Dynamic Range		Peak-to-peak ac input voltage where gain falls to 90% of its small signal value, f = 5 MHz	6	-	-	mVpp

READ CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Common Mode Rejection Ratio	Vin = 0 VDC+100 mVpp @ 5 MHz	54	-	-	dB
Power Supply Rejection Ratio	100 mVpp @ 5 MHz on VDD1 100 mVpp @ 5 MHz on VCC	54	-	-	dB
Channel Separation	Unselected channels driven with 100 mVpp @ 5 MHz, Vin = 0 mVpp	45	-	-	dB
Output Offset Voltage		-360	-	+360	mV
RDX, RDY Common Mode	Read Mode	2.2	2.9	3.6	VDC
Output Voltage	Write Mode	-	2.9	-	VDC
Single Ended Output Resistance	f = 5 MHz	-	-	40	Ω
Output Current	AC Coupled Load, RDX to RDY	3.2	-	-	mA

SWITCHING CHARACTERISTICS (See Figure 1)
Unless otherwise specified, recommended operating conditions apply, Iw = 20 mA, Lh = 1.0 µH, Rh = 30Ω and f(WD) = 5 MHz.

PARAMETER	CONDITIONS	MIN	MAX	UNITS
R/$\overline{W}$				
R/$\overline{W}$ to Write Mode	Delay to 90% of write current	-	0.6	µs
R/$\overline{W}$ to Read Mode	Delay to 90% of 100 mV 10 MHz Read signal envelope or to 90% decay of write current	-	0.6	µs
$\overline{CS}$				
$\overline{CS}$ to Select	Delay to 90% of write current or to 90% of 100 mV 10 MHz Read signal envelope	-	0.6	µs
$\overline{CS}$ to Unselect	Delay to 10% of write current	-	0.6	µs
HSn				
HS0, 1, 2, 3 to any Head	Delay to 90% of 100 mV 10 MHz Read signal envelope	-	0.4	µs
WUS				
Safe to Unsafe - TD1		0.6	3.6	µs
Unsafe to Safe - TD2		-	1	µs
Head Current				
Prop. Delay - TD3	From 50% points, Lh=0µh, Rh=0Ω	-	32	ns
Asymmetry	WD has 50% duty cycle and 1ns rise/fall time, Lh=0µh, Rh=0Ω	-	1	ns
Rise/Fall Time	10% - 90% points, Lh=0µh, Rh=0Ω	-	9	ns

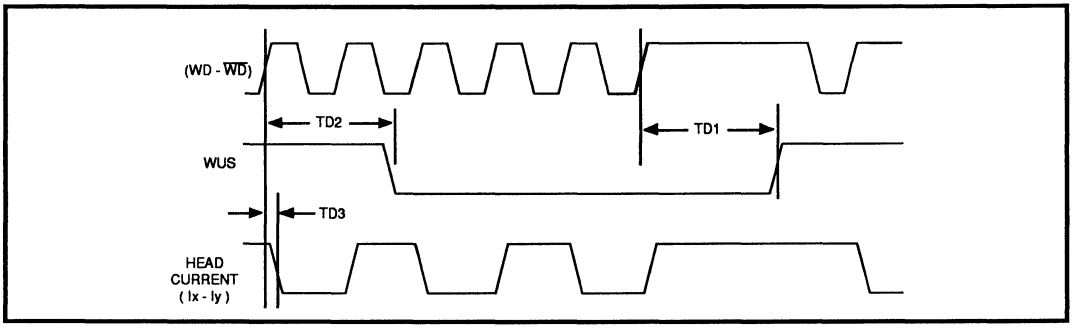


FIGURE 1: Write Mode Timing Diagram

APPLICATIONS INFORMATION

The specifications, provided in the data section, account for the worst case values of each parameter taken individually. In actual operation, the effects of worst case conditions on many parameters correlate. Tables 3 & 4 demonstrate this for several key parameters. Notice that under the conditions of worst case input noise, the higher read back signal resulting from the higher input impedance can compensate for the higher input noise. Accounting for this correlation in your analysis will be more representative of actual performance.

TABLE 3: Key Parameters Under Worst Case Input Noise Conditions

PARAMETER		Tj = 25°C	Tj = 135°C	UNITS
Input Noise Voltage (Max.)		0.70	0.85	nV/$\sqrt{Hz}$
Differential Input Resistance (Min.)	32R528R	390	420	Ω
Differential Input Capacitance (Max.)		32	34	pF

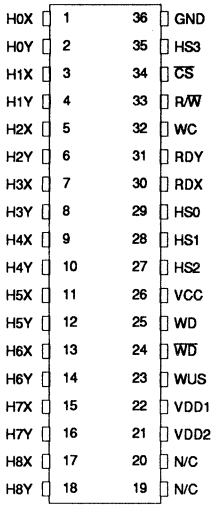
TABLE 4: Key Parameters Under Worst Case Input Impedance Conditions

PARAMETER		Tj = 25°C	Tj = 135°C	UNITS
Input Noise Voltage (Max.)		0.58	0.71	nV/$\sqrt{Hz}$
Differential Input Resistance (Min.)	32R528R	310	350	Ω
Differential Input Capacitance (Max.)		33	35	pF

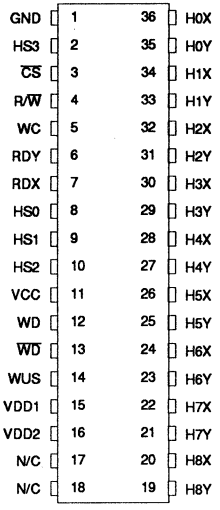
SSI 32R528R
9-Channel Thin Film
Read/Write Device

PACKAGE PIN DESIGNATIONS

(Top View)



36-Lead SOM



36-Lead SOM Mirror

THERMAL CHARACTERISTICS: Ø ja

36-Lead SOM	50°C/W

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32R528R with Internal Damping Resistor		
9-Channel SOM	32R528R-9CM	32R528R-9CM
SSI 32R528R Mirror Image with Damping Resistor		
9-Channel SOM	32R528RM-9CL	32R528RM-9CL

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 731-7110, FAX (714) 573-6914

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SSI 32R5281R
14-Channel Two-Terminal Read/Write Device
Advance Information

1

November 1991

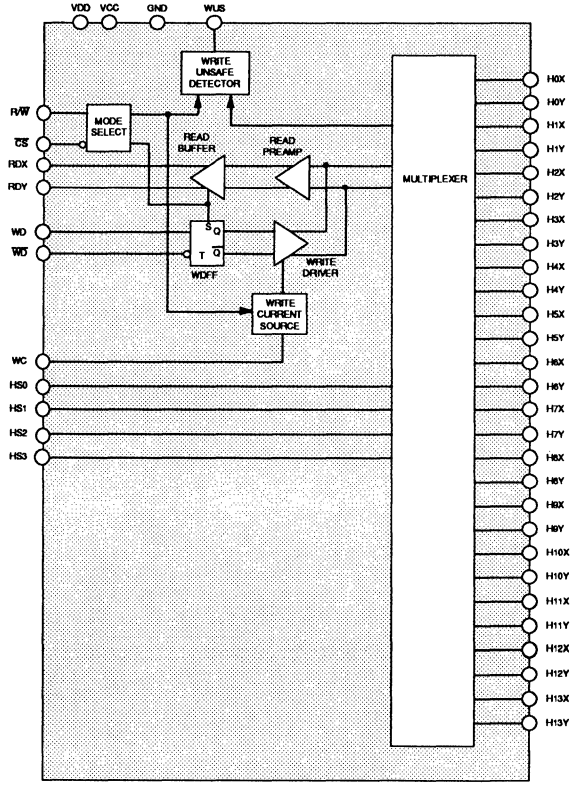
DESCRIPTION

The SSI 32R5281R Read/Write device is a bipolar monolithic integrated circuit designed for use with two-terminal thin-film recording heads. It provides a low noise read amplifier, write current control and data protection circuitry for up to 14 channels. Power supply fault protection is provided by disabling the write current generator during power sequencing. System write to read recovery time is significantly improved by controlling the read channel common mode output voltage shift in the write mode. It requires +5V and +12V power supplies and provides internal 700Ω damping resistors.

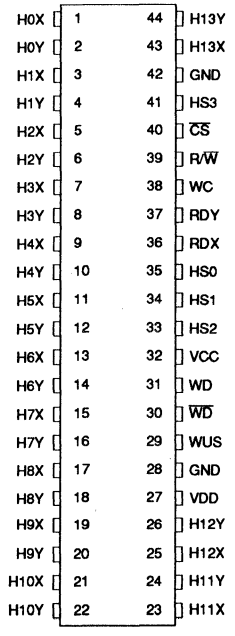
FEATURES

- **High performance:**
  - **Read mode gain = 250 V/V**
  - **Input noise = 0.85 nV/√Hz max.**
  - **Input capacitance = 35 pF max.**
  - **Write current range = 10 mA to 40 mA**
  - **Head voltage swing = 7 Vpp**
  - **Write current rise time = 9 ns**
- **Enhanced system write to read recovery time**
- **Differential ECL-like Write Data Input**
- **Power supply fault protection**
- **Write unsafe detection**
- **+5V, +12V power supplies**

BLOCK DIAGRAM



PIN DIAGRAM



44-LEAD SOM

CAUTION: Use handling procedures necessary for a static sensitive component.

SSI 32R5281R
14-Channel Two-Terminal Read/Write Device

CIRCUIT OPERATION

The SSI 32R5281R addresses up to 14 two-terminal thin film heads providing write drive or read amplification. Head selection and mode control is accomplished with pins HSn, $\overline{CS}$ and R/$\overline{W}$, as shown in Tables 1 & 2. Internal resistor pullups, provided on pins $\overline{CS}$ and R/$\overline{W}$ will force the device into a non-writing condition if either control line is opened accidentally.

WRITE MODE

The write mode configures the SSI 32R5281R as a current switch and activates the Write Unsafe (WUS) detection circuitry. Write current is toggled between the X and Y direction of the selected head on each low to high transition on the WD, Write Data input. (See figure 1.)

A preceding read operation initializes the Write Data Flip Flop (WDFF) to pass write current in the X-direction of the head, i.e., into the X-port.

The magnitude of the write current (0-pk) is given by:

$$Iw = \frac{Vwc}{Rwc}$$

where Vwc (WC pin voltage) = 1.65V ± 5%, is programmed by an external resistor Rwc, connected from pin WC to ground. In multiple device applications, a single Rwc resistor may be made common to all devices. The actual head current Ix, y is given by:

$$Ix,y = \frac{Iw}{1 + Rh/Rd}$$

where:
Rh = head resistance + external wire resistance, and
Rd = damping resistance.

Power supply fault protection improves data security by disabling the write current generator during a voltage fault or power supply sequencing. Additionally, the write unsafe detection circuitry will flag any of the conditions listed below as a high level on the open collector output pin, WUS. Two positive transitions on the WD, Write Data input line, after the fault is corrected, are required to clear the WUS flag.

- WD frequency too low
- Device not selected
- Open head
- Device in read mode
- No write current

READ MODE

The read mode configures the SSI 32R5281R as a low noise differential amplifier and deactivates the write current generator and write unsafe detection circuitry. The RDX and RDY outputs are emitter followers and are in phase with the "X" and "Y" head ports. These outputs should be AC coupled to the load. The RDX, RDY common mode voltage is maintained at the write mode value, minimizing the transient between write mode and read mode, substantially reducing the write to read recovery time in the subsequent Pulse Detection circuitry.

IDLE MODE

The idle mode deactivates the internal write current generator, the write unsafe detector and switches the RDX, RDY outputs into a high impedance state. This facilitates multiple device applications by enabling the read outputs to be wire-OR'ed and the write current programming resistor to be common to all devices.

TABLE 1: Mode Select

$\overline{CS}$	R/$\overline{W}$	MODE
0	0	Write
0	1	Read
1	0	Idle
1	1	Idle

TABLE 2: Head Select

HS3	HS2	HS1	HS0	HEAD
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13

0 = Low level 1 = High level

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
HS0 - HS3	I	Head Select
$\overline{CS}$	I	Chip Select: a low level enables the device
R/$\overline{W}$	I	Read/Write: a high level selects Read mode
WUS	O*	Write Unsafe: Open collector output, a high level indicates an unsafe writing condition
WD, $\overline{WD}$	I	Differential Write Data inputs: a positive transition on WD toggles the direction of the head current
H0X - H13X H0Y - H13Y	I/O	X, Y Head Connections: Current in the X-direction flows into the X-port
RDX, RDY	O*	X, Y Read Data: differential read data output
WC	*	Write Current: used to set the magnitude of the write current
VCC	-	+5V Logic Circuit Supply
VDD	-	+12V
GND	-	Ground

*When more than one R/W device is used, these signals can be wire OR'ed.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation outside these rating limits may permanently damage the device.

PARAMETER		SYMBOL	VALUE	UNITS
DC Supply Voltage		VDD	-0.3 to +14	VDC
		VCC	-0.3 to +7	VDC
Write Current		Iw	100	mA
Digital Input Voltage		Vin	-0.3 to VCC +0.3	VDC
Head Port Voltage		VH	-0.3 to VDD2 +0.3	VDC
WUS Pin Voltage Range		Vwus	-0.3 to +14	VDC
Output Current	RDX, RDY	Io	-10	mA
	WUS	Iwus	+12	mA
Storage Temperature		Tstg	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNITS
DC Supply Voltage	VDD	12 ± 10%	VDC
	VCC	5 ± 10%	VDC
Operating Temperature	Tj	+25 to +135	°C

DC CHARACTERISTICS

Unless otherwise specified, recommended operating conditions apply.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VDD Supply Current	Read Mode	-	30	TBD	mA
	Write Mode	-	39	TBD	mA
	Idle Mode	-	12	TBD	mA
VCC Supply Current	Read Mode	-	50	TBD	mA
	Write Mode	-	32	TBD	mA
	Idle Mode	-	43	TBD	mA
Power Dissipation (Tj = +135°C)	Read Mode	-	-	800	mW
	Write Mode: Iw = 20 mA,	-	-	1000	mW
	Idle Mode	-	360	570	mW
WD, $\overline{WD}$ Input Low Current (IIL1)	VIL1 = VCC -1.625V			80	µA
WD, $\overline{WD}$ Input High Current (IIH1)	VIH1 = VCC -0.72V			100	µA
WD, $\overline{WD}$ Input Low Voltage (VIL1)		VCC -1.870		VCC -1.625	VDC
WD, $\overline{WD}$ Input High Voltage (VIH1)		VCC -1.00		VCC -0.720	VDC
R/$\overline{W}$, $\overline{CS}$, HS0-HS3 Input Low Current (IIL2)	VIL2 = 0.8V	-0.4			mA
R/$\overline{W}$, $\overline{CS}$, HS0-HS3 Input High Current (IIH2)	VIH2 = 2.0V			100	µA
R/$\overline{W}$, $\overline{CS}$, HS0-HS3 Input Low Voltage (VIL2)				0.8	VDC
R/$\overline{W}$, $\overline{CS}$, HS0-HS3 Input High Voltage (VIH2)		2.0			VDC
WUS Output Low Voltage (VOL)	Iol = 8 mA	-	-	0.5	VDC
VDD Fault Voltage		8.5	-	10.0	VDC
VCC Fault Voltage		3.5	-	4.2	VDC

DC CHARACTERISTICS (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Head Current (HnX, HnY)	Write Mode, 0 ≤ VCC ≤ 3.5V 0 ≤ VDD1 ≤ 8.5V	-200	-	+200	µA
	Read/Idle Mode, 0 ≤ VCC ≤ 5.5V 0 ≤ VDD1 ≤13.2V	-200	-	+200	µA

WRITE CHARACTERISTICS

Unless otherwise specified, recommended operating conditions apply, Iw = 20 mA, Lh = 500 nH, Rh = 30Ω and f(WD) = 5 MHz.

WC Pin Voltage (Vwc)		-	1.65 ±5%	-	V
Differential Head Voltage Swing	Iw = 40 mA	7	-	-	Vpp
Unselected Head Current		-	-	1	mA(pk)
Differential Output Capacitance		-	-	25	pF
Differential Output Resistance		500	700	950	Ω
WDI Transition Frequency	WUS = low	1.7	-	-	MHz
	WUS = high	-	-	500	kHz
Write Current Range		10	-	40	mA

READ CHARACTERISTICS

Unless otherwise specified, recommended operating conditions apply CL (RDX, RDY) < 20pF and RL (RDX,RDY) = 1 kΩ.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Differential Voltage Gain		Vin=1mVpp @ 300 kHz	210	250	290	V/V
Bandwidth	-1dB	|Zs|<5Ω, Vin=1 mVpp	25	40	-	MHz
	-3dB	|Zs|<5Ω, Vin=1 mVpp	35	55	-	MHz
Input Noise Voltage		BW = 15 MHz, Lh = 0, Rh = 0	-	0.62	0.85	nV/√Hz
Differential Input Capacitance		Vin = 1 mVpp, f = 5 MHz	-	-	35	pF
Differential Input Resistance		Vin = 1 mVpp, f = 5 MHz	300	-	-	Ω
Dynamic Range		Peak-to-peak AC input voltage where gain falls to 90% of its small signal value, f = 5 MHz	2.0	-	-	mVpp
Common Mode Rejection Ratio		Vin = 0 VDC+100 mVpp @ 5 MHz	54	-	-	dB
Power Supply Rejection Ratio		100 mVpp @ 5 MHz on VDD1 100 mVpp @ 5 MHz on VCC	54	-	-	dB
Channel Separation		Unselected channels driven with 100 mVpp @ 5 MHz, Vin = 0 mVpp	45	-	-	dB

READ CHARACTERISTICS (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Output Offset Voltage		-400	-	+400	mV
RDX, RDY Common Mode Output Voltage	Read Mode or Write Mode	Vcc -2.5	Vcc - 2.1	Vcc -1.7	VDC
Single Ended Output Resistance	f = 5 MHz	-	-	30	Ω
Output Current	AC Coupled Load, RDX to RDY	3.2	-	-	mA

SWITCHING CHARACTERISTICS (See Figure 1)
Unless otherwise specified, recommended operating conditions apply, Iw = 20 mA, Lh = 500 nH, Rh = 30Ω and f(WD) = 5 MHz.

PARAMETER	CONDITIONS	MIN	MAX	UNITS
R/$\overline{W}$				
R/$\overline{W}$ to Write Mode	Delay to 90% of write current	-	0.6	µs
R/$\overline{W}$ to Read Mode	Delay to 90% of 100mV 10MHz Read signal envelope or to 90% decay of write current	-	0.6	µs
$\overline{CS}$				
$\overline{CS}$ to Select	Delay to 90% of write current or to 90% of 100mV 10MHz Read signal envelope	-	0.6	µs
$\overline{CS}$ to Unselect	Delay to 90% of write current	-	0.6	µs
HSn				
HS0, 1, 2, 3 to any Head	Delay to 90 % of 100mV 10MHz Read signal envelope	-	0.4	µs
WUS				
Safe to Unsafe - TD1		0.6	3.0	µs
Unsafe to Safe - TD2		-	1	µs
Head Current				
Prop. Delay - TD3	From 50 % points, Lh=0µh, Rh=0Ω	-	32	ns
Asymmetry	WD has 50 % duty cycle and 1ns rise/fall time, Lh=0µh, Rh=0Ω	-	0.5	ns
Rise/Fall Time	10% - 90% points, Lh=0µh, Rh=0Ω	-	9	ns

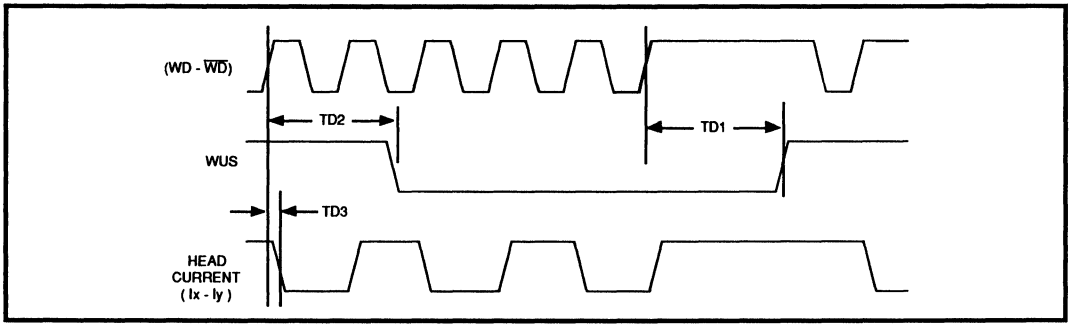


FIGURE 1: Write Mode Timing Diagram

APPLICATIONS INFORMATION

The specifications, provided in the data section, account for the worst case values of each parameter taken individually. In actual operation, the effects of worst case conditions on many parameters correlate. Tables 3 & 4 demonstrate this for several key parameters. Notice that under the conditions of worst case input noise, the higher read back signal resulting from the higher input impedance can compensate for the higher input noise. Accounting for this correlation in your analysis will be more representative of actual performance.

TABLE 3: Key Parameters Under Worst Case Input Noise Conditions

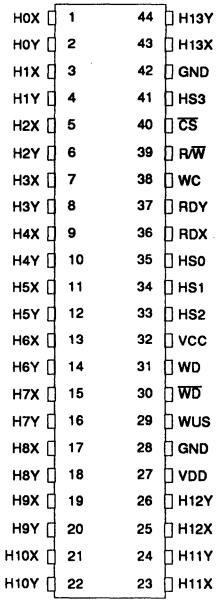
PARAMETER	Tj = 25°C	Tj = 135°C	UNITS
Input Noise Voltage (Max.)	0.70	0.85	nV/$\sqrt{Hz}$
Differential Input Resistance (Min.)	390	420	Ω
Differential Input Capacitance (Max.)	32	34	pF

TABLE 4: Key Parameters Under Worst Case Input Impedance Conditions

PARAMETER	Tj = 25°C	Tj = 135°C	UNITS
Input Noise Voltage (Max.)	0.58	0.71	nV/$\sqrt{Hz}$
Differential Input Resistance (Min.)	310	350	Ω
Differential Input Capacitance (Max.)	33	35	pF

SSI 32R5281R
14-Channel Two-Terminal Read/Write Device

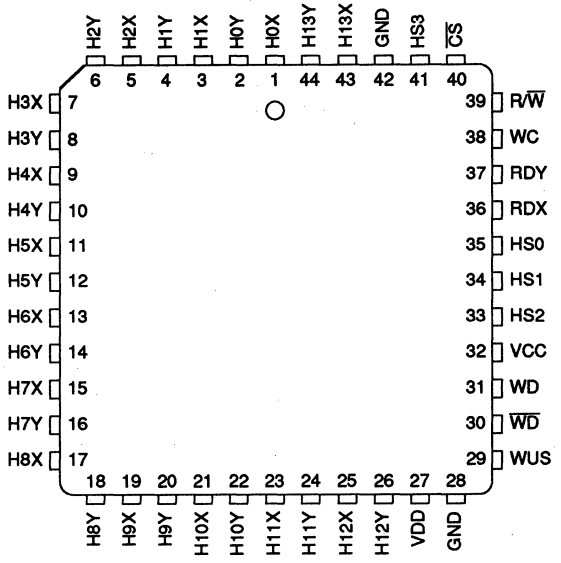
PACKAGE PIN DESIGNATIONS
(Top View)



44-Pin SOM

THERMAL CHARACTERISTICS: Øja

44-Lead SOM	50°C/W
44-PLCC	60°C/W



44-Pin PLCC

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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silicon systems®
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SSI 32R1200/1201
+5V, 2, 4-Channel Ferrite/MIG Read/Write Device

Advance Information

1

November 1991

DESCRIPTION

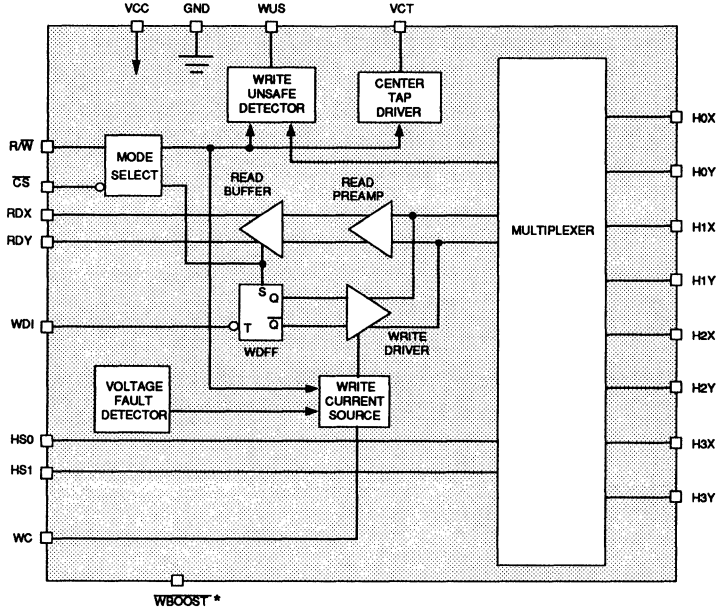
The SSI 32R1200/1201 are bipolar monolithic integrated circuits designed for use with center-tapped ferrite or MIG recording heads. They provide a low noise read path, write current control, and data protection circuitry for as many as 4 channels. Power supply fault protection is provided by disabling the write current generator during power sequencing. A power down mode (idle) is provided to reduce power consumption to less than 10 mW. The SSI 32R1201 option provides a write current boost feature which can be selected without using additional external resistors.

The SSI 32R1200R/1201R option provides internal 750Ω damping resistors. Both devices require only a +5V power supply and are available in surface mount packages.

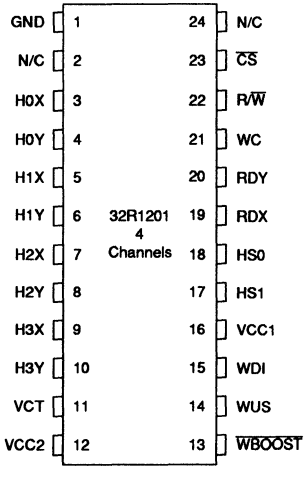
FEATURES

- **+5V only power supply**
- **Low power**
  - **Pd ≤ 200 mW read mode**
  - **Pd ≤ 10 mW idle mode**
- **High Performance**
  - **Read mode gain = 200 V/V**
  - **Input noise = 1.2 nV/√Hz max.**
  - **Input capacitance = 17 pF max.**
  - **Write current range = 15 - 50 mA**
  - **Head voltage swing = 6.0 Vpk**
- **Designed for center-tapped ferrite or MIG heads**
- **TTL selectable write current boost**
- **Power supply fault protection**
- **Includes write unsafe detection**
- **Enhanced Write to Read recovery**

BLOCK DIAGRAM



PIN DIAGRAM



24-Pin SOL, VSOP

CAUTION: Use handling procedures necessary for a static sensitive component.

* Not available in 20-pin SOL

SSI 32R1200/1201
+5V, 2, 4-Channel Ferrite/MIG Read/Write Device

DESCRIPTION

WRITE MODE

A source of recording current is provided to the head center tap by an internal voltage reference, VCT. The current is conducted through the head alternately into an HnX terminal or an HnY terminal according to the state of an internal flip-flop. The flip-flop is triggered by the negative transition of the Write Data Input line (WDI). A proceeding read mode selection initializes the write data flip-flop, WDFF, to pass write current through the "X" side of the head. The write current magnitude is determined by the value of an external resistor Rwc connected between WC terminal and GND, and is given by:

Iw = K/Rwc, where K = Write Current Constant

In addition, this current can be given a 30% boost without switching in additional resistance values by pulling $\overline{\text{WBOOST}}$ low (32R1201/1201R only).

WRITE MODE FAULT DETECT CIRCUIT

Several circuits are dedicated to detecting fault conditions associated with the write mode. A logical high level will be present at the Write Unsafe (WUS) terminal if any of the following write fault conditions are present:

- Head open
- Head center tap open
- Head shorted
- Head shorted to ground
- No write current
- WDI frequency too low
- Device in read or idle mode

The Write Unsafe output is open-collector and is usually terminated by an external resistor connected to VCC. Two negative transitions on WDI, after the fault is corrected, will clear the WUS flag.

Additionally, a power voltage monitoring circuit is used to detect VCC voltage level. If it is too low to permit valid data recording, write current is inhibited. With VCC voltage level above the inhibiting value, control of write current is provided by the mode selection inputs.

READ MODE

In Read Mode, (R/$\overline{\text{W}}$ high and $\overline{\text{CS}}$ low), the circuit functions as a low noise differential amplifier. The read amplifier input terminals are determined by the Head Select inputs. The read amplifier outputs (RDX, RDY) are emitter follower sources, providing low impedance outputs. The amplifier gain polarity is non-inverting between HnX, HnY inputs and RDX, RDY outputs.

IDLE MODE

Taking $\overline{\text{CS}}$ high selects the idle mode which switches the RDX and RDY outputs into a high impedance state and deactivates the device. Power consumption in this mode is held to a minimum.

MODE SELECTION AND INDICATION CIRCUIT

Logical control inputs which select mode and head channel are TTL compatible. Their functions are described in Table1 and Table 2.

TABLE 1: Head Select Table

Head Selected	HS1	HS0
0	0	0
1	0	1
2	1	0
3	1	1

TABLE 2: Mode Select Table

Mode Select		Selected Mode	Indicating & Fault Outputs
$\overline{\text{CS}}$	R/$\overline{\text{W}}$		WUS
1	X	Idle	off
0	1	Read	off
0	0	Write	on

PIN DESCRIPTION

NAME	I/O	DESCRIPTION
HS0-HS1	I	Head Select. Logical combinations select one of four Heads. See Table 1
$\overline{CS}$	I	Chip Select: a low level enables device. Has internal pull-up resistor.
R/$\overline{W}$	I	Read/Write:a high level selects read mode. Has internal pull-up resistor.
WUS	O*	Write Unsafe: a high level indicates an unsafe writing condition
WDI	I	Write Data In: negative transition toggles direction of head current
H0X-H3X H0Y-H3Y	I/O	X, Y head connections
RDX, RDY	O*	X, Y Read Data: differential read signal output
WC	-	Write Current: used to set the magnitude of the write current
$\overline{WBOOST}$**	I	A logic low signal on this pin increases the magnitude of write current by typically 30%
VCT	-	Voltage Center Tap: voltage source for head center tap
VCC	-	+5V
GND	-	Ground

* When more than one R/W device is used, these signals can be wire OR'ed.
** $\overline{WBOOST}$ available in 32R1201 only (16 and 24-pin options)

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND. Currents into device are positive.)

PARAMETER		VALUE	UNITS
DC Supply Voltage	VCC	-0.3 to +6	VDC
Digital Input Voltage Range HS1, HS0, WDI, R/$\overline{W}$, $\overline{CS}$, $\overline{WBOOST}$		-0.3 to VCC + 0.3	VDC
Head Port Voltage Range	VH	-0.3 to VCC + 0.3	VDC
Write Current Pin Voltage	Vwc	-0.3 to VCC + 0.3	VDC
WUS Pin Voltage Range	Vwus	-0.3 to +6.0	VDC
Write Current Zero–Peak	IW	60	mA
RDX, RDY Output Current	Io	-10	mA
RDX, RDY Pin Voltage		VCC + 0.3	VDC
VCT Output Current Range	IVCT	-60 mA to +10 µA	mA
WUS Output Current Range	Iwus	1.0 mA to -10 mA	mA
Storage Temperature Range	Tstg	-65 to 150	°C
Package Temperature (20 sec Reflow)		215	°C

RECOMMENDED OPERATION CONDITIONS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
DC Supply Voltage	VCC		4.75	5.0	5.25	VDC
Head Inductance	Lh		1		15	µH
Damping Resistor	Rd	32R1200/1201 only	500		2000	Ω
Write Current Range	IW		15		50	mA
Junction Temperature Range	Tj		+25		+135	°C

DC CHARACTERISTICS

(Unless otherwise specified, recommended operating conditions apply.)

POWER SUPPLY

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VCC Supply Current (ICC)	Read Mode		28	38	mA
	Idle Mode		1.4	2.0	mA
	Write Mode		27 + Iw	40 + Iw	mA
Power Dissipation	Read Mode		140	200	mW
	Idle Mode		7	10.5	mW
	Write Mode			210 + 5 Iw	mW

DIGITAL I/O

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
VIL	Input Low Voltage $\overline{CS}$, R/$\overline{W}$ WDI, HS0, HS1, $\overline{WBOOST}$				0.8	VDC
VIH	Input High Voltage $\overline{CS}$, R/$\overline{W}$ WDI, HS0, HS1, $\overline{WBOOST}$		2.0			VDC
IIL	Input Low Current $\overline{CS}$, R/$\overline{W}$ WDI, HS0, HS1, $\overline{WBOOST}$	VIL = 0.4V	-0.4			mA
IIH	Input High Current $\overline{CS}$, R/$\overline{W}$ WDI, HS0, HS1, $\overline{WBOOST}$	VIH = 2.7V			20	µA
VOL	WUS Output Low Voltage	IOL = 4.0 mA			0.5	VDC
IOH	WUS Output High Current	VOH = 5.0V			100	µA

WRITE MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Center Tap Voltage VCT	Write Mode		Vcc - 0.9		VDC
Head Current (per side)	Write Mode, 0 ≤ VCC ≤ 3.9V	-200		200	µA
Write Current Range	1.0 kΩ ≤ Rwc ≤ 3.3 kΩ	15		50	mA
Write Current Constant "K"		46	50	54	mA-kΩ
Iwc to Head Current Gain			20		mA/mA
$\overline{\text{WBOOST}}$ - Write Current Boost Factor*	$\overline{\text{WBOOST}}$ = Low	1.25		1.35	mA/mA
Unselected Head Leakage Current				85	µA
RDX, RDY Common Mode Output Voltage		2.0	Vcc - 2.4	3.5	VDC
RDX, RDY Leakage	RDX, RDY = 4V Idle Mode	-100		100	µA

* Not available in 20-pin SOL.

READ MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Center Tap Voltage	Read Mode		Vcc - 1.5		VDC
Input Bias Current (per side)			20	60	µA
Output Offset Voltage	Read Mode	-200		+200	mV
Common Mode Output Voltage	Read Mode	2	Vcc - 2.4	3.5	VDC
Common Mode Output Voltage Change from Write to Read Mode		-100		+100	mV

FAULT DETECTION CHARACTERISTICS

Unless otherwise specified recommended conditions apply, Iw = 30 mA, Lh = 5 µH, Rd = 750Ω. (SSI 32R1200 only), F(WDI) = 10 MHz.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Minimum Rate of WDI Input for Safe condition		500			kHz
Maximum Rate of WDI Input for Unsafe condition				167	kHz
Minimum voltage value for guaranteed write current turn-on		4.4			VDC
Maximum voltage value for guaranteed write current turn-off				3.9	VDC

DYNAMIC CHARACTERISTICS AND TIMING
(Unless otherwise specified, recommended operating conditions apply and Iw = 30 mA, Lh = 5 µH, Rd = 750Ω 32R1200 only, f(WDI) = 5 MHz, CL(RDX, RDY) ≤ 20 pF.)

WRITE MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Differential Head Voltage Swing		6.0	6.4		V(pk)
Unselected Head Transient Current	1µH ≤ Lh ≤ 9.5µH			2	mA(pk)
Differential Output Capacitance				15	pF
Differential Output Resistance	32R1200	10			kΩ
	32R1200R	600		960	Ω

READ MODE

Differential Voltage Gain	Vin = 1 mV RMS @ 1 MHz	160	200	240	V/V
Bandwidth (-3dB)	|Zs| < 5Ω, Vin = 1 mVpp	30	60		MHz
Input Noise Voltage	BW = 15 MHz, Lh = 0, Rh = 0		0.85	1.2	$nV/\sqrt{Hz}$
Differential Input Capacitance	Vin = mV RMS f = 5MHz		14	17	pF
Differential Input Resistance	32R1200 f = 5 MHz	2.0			kΩ
	32R1200R	460		860	Ω
Dynamic Range	AC input voltage where gain falls to 90% of its small signal gain valve, f = 5 MHz	2			mVpp
Common Mode Rejection Ratio	Vcm = 100 mVpp @1 MHz < f < 10 MHz	50	75		dB
Power Supply Rejection Ratio	ΔVcc =100 mVpp @1MHz < f < 10 MHz	45			dB
Channel Separation	Unselected Channels: Vin = 20 mVpp 1 MHz < f < 10 MHz	45	54		dB
RDX,Y Single Ended Output Resistance				30	Ω
Output Current	AC Coupled Load, RDX to RDY	±1.5			mA

DYNAMIC CHARACTERISTICS AND TIMING (continued)

SWITCHING CHARACTERISTICS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
R/$\overline{W}$	Read to Write	R/W to 90% of write current		50	100	ns
	Write to Read	R/W to 90% of 100 mV. 10 MHz Read signal envelope		.15	1.0	µs
$\overline{CS}$	Unselect to Select	$\overline{CS}$ to 90% Ih or to 90% of 100 mV. 10 MHz Read signal envelope		1.0	2.0	µs
	Select to Unselect	$\overline{CS}$ to 10% Ih		.05	0.6	µs
HS0, 1 to any Head		To 90% of 100 mV. 10 MHz Read signal envelope			0.6	µs
WUS	Safe to Unsafe (TD1)		4	8	12	µs
	Unsafe to Safe (TD2)	Write mode, after fault cleared			150	ns
Head Current		Rh = 0, Lh = 0				
	Prop. Delay (TD3)	From 50% points		25	30	ns
	Asymmetry	WDI has 50% Duty Cycle and 1 ns Rise/Fall Time			2	ns
	Rise/Fall Time	10% - 90% Points		4	20	ns

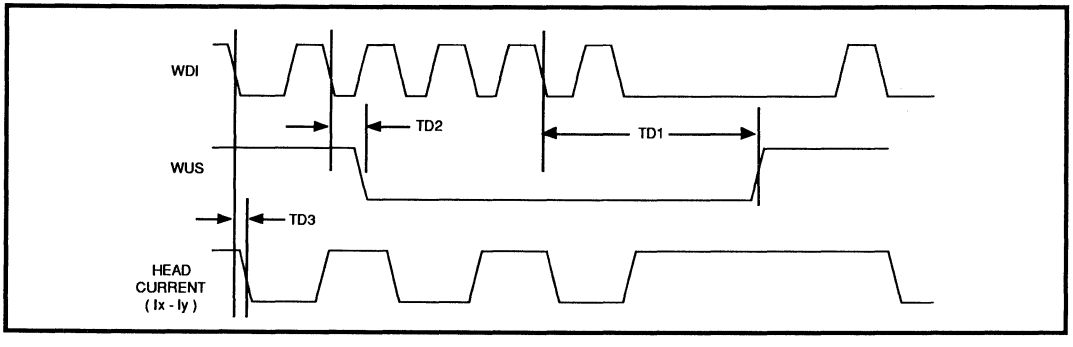
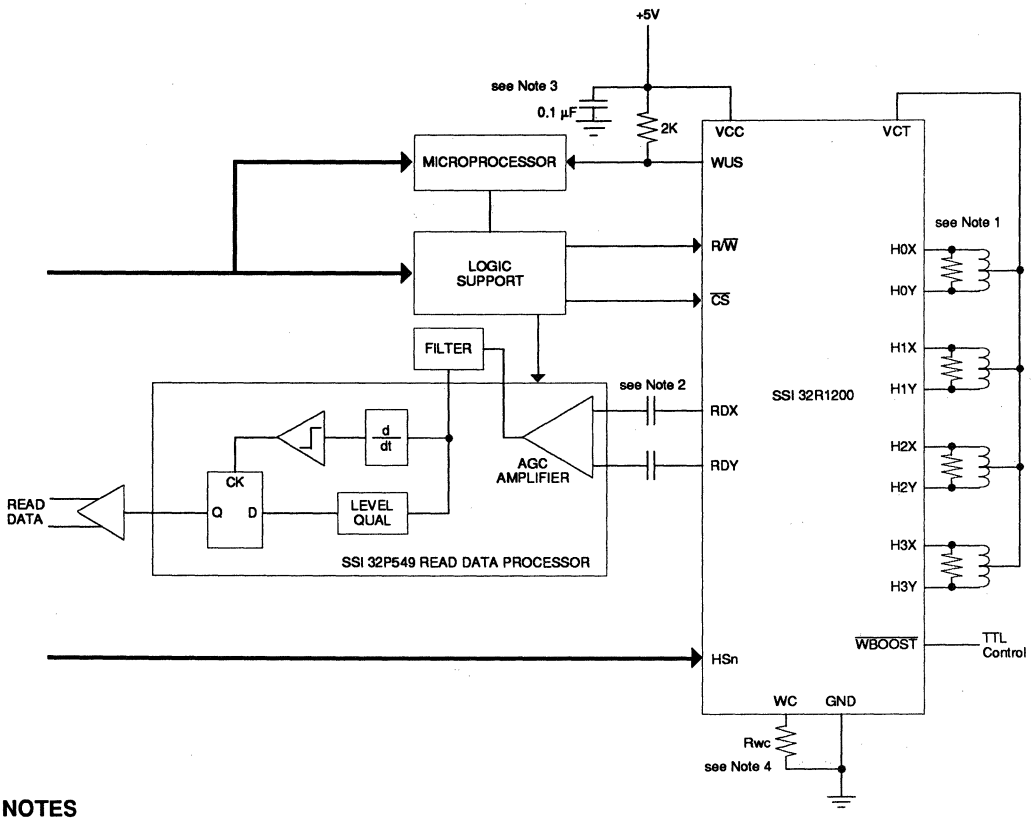


FIGURE 1: Write Mode Timing Diagram



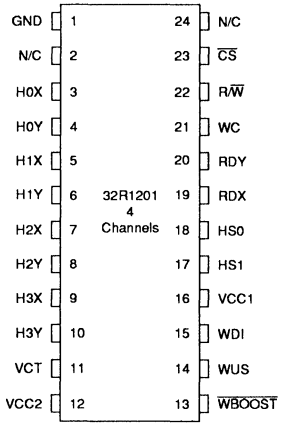
NOTES

1. Damping resistors not required on 32R1200R versions.
2. Limit DC current from RDX and RDY to 100 µA and load capacitance to 20 pF. In multi-chip application these outputs can be wire-OR'ed.
3. The power bypassing capacitor must be located close to the 32R1200 with its ground returned directly to device ground, with as short a path as possible.
4. To reduce ringing due to stray capacitance this resistor should be located close to the 32R1200. Where this is not desirable a series resistor can be used to buffer a long WC line.

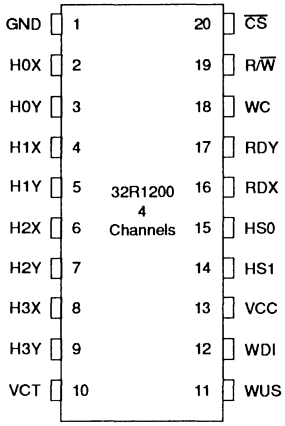
FIGURE 2: Applications Information

PACKAGE PIN DESIGNATIONS

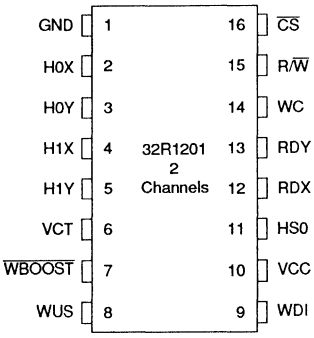
(Top View)



24-Pin SOL, SOV



20-Pin SOL, SOV



16-Pin SOL

THERMAL CHARACTERISTICS: θja

24-lead	SOL	80°C/W
20-lead	SOL	80°C/W
16-lead	SOL	105°C/W
24-lead	VSOP	110°C/W
20-lead	VSOP	125°C/W

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714) 731-7110, FAX: (714) 573-6914

Notes:

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SSI 32R1220/1221/1222
+5V, 2, 4-Channel Ferrite/MIG Read/Write Device

Advance Information

1

December 1991

DESCRIPTION

The SSI 32R1220/1221 are bipolar monolithic integrated circuits designed for use with center-tapped ferrite or MIG recording heads. They provide a low noise read path, write current control, and data protection circuitry for as many as 4 channels. Power supply fault protection is provided by disabling the write current generator during power sequencing. A power down mode (idle) is provided to reduce power consumption to less than 10 mW. The SSI 32R1221 option provides write current boost feature which can be selected without using additional external resistors.

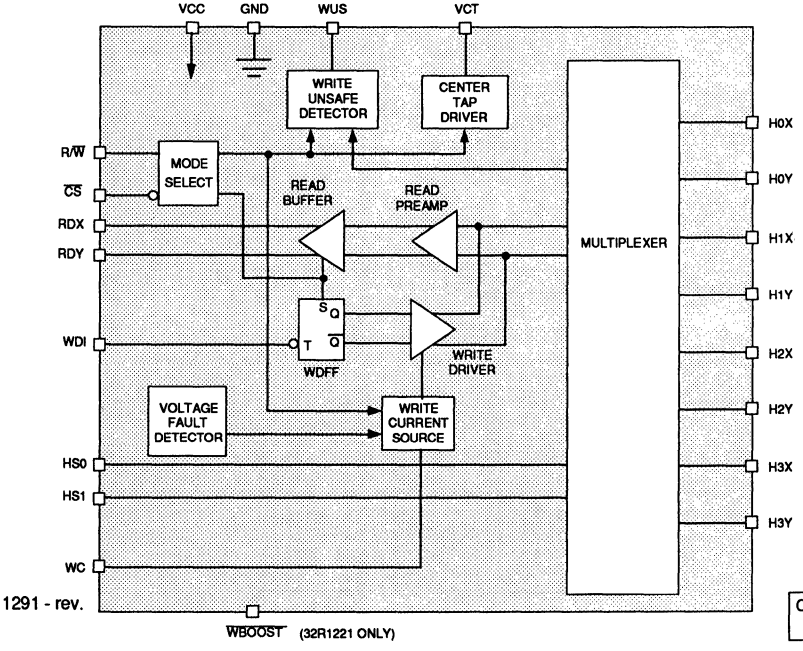
The SSI 32R1222 option provides a bond option compatible with other available three-terminal Read/Write devices.

The SSI 32R1220R/1221R/1222R option provides internal 750Ω damping resistors. Both devices require only a +5V power supply and are available in surface mount packages.

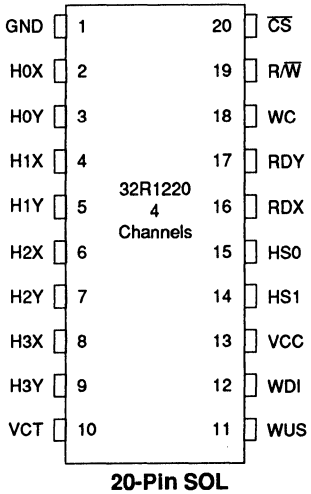
FEATURES

- **+5V (± 10%) only power supply**
- **Low power**
  - **Pd =150 mW read mode (NOM)**
  - **Pd ≤ 5 mW idle mode (NOM)**
- **High Performance**
  - **Read mode gain = 250 V/V**
  - **Input noise = 0.8 nV/√Hz max.**
  - **Input capacitance = 17 pF max.**
  - **Write current range = 15 - 40 mA**
  - **Head voltage swing = 6.0 Vpk**
- **Designed for center-tapped ferrite or MIG heads**
- **TTL selectable write current boost**
- **Pin compatible with 32R1200**
- **Power supply fault protection**
- **Write unsafe detection**
- **Enhanced Write to Read recovery**

BLOCK DIAGRAM



PIN DIAGRAM



20-Pin SOL

1291 - rev.

CAUTION: Use handling procedures necessary for a static sensitive component.

SSI 32R1220/1221/1222
+5V, 2, 4-Channel Ferrite/MIG Read/Write Device

DESCRIPTION

WRITE MODE

A source of recording current is provided to the head center tap by an internal voltage reference, VCT. The current is conducted through the head alternately into an HnX terminal or an HnY terminal according to the state of an internal flip-flop. The flip-flop is triggered by the negative transition of the Write Data Input line (WDI). A proceeding read mode selection initializes the write data flip-flop, WDFF, to pass write current through the "X" side of the head. The write current magnitude is determined by the value of an external resistor Rwc connected between WC terminal and GND, and is given by:

Iw = K/Rwc, where K = Write Current Constant

In addition this current can be given a 30% boost, without switching in additional resistance values, by pulling $\overline{\text{WBOOST}}$ low (32R1221/1221R only).

WRITE MODE FAULT DETECT CIRCUIT

Several circuits are dedicated to detecting fault conditions associated with the write mode. A logical high level will be present at the Write Unsafe (WUS) terminal if any of the following write fault conditions are present:

- Head open
- Head center tap open
- Head shorted
- Head shorted to ground
- No write current
- WDI frequency too low
- Device in read or idle mode

The Write Unsafe output is open-collector and is usually terminated by an external resistor connected to VCC. Two negative transitions on WDI, after the fault is corrected, will clear the WUS flag.

Additionally, a power voltage monitoring circuit is used to detect VCC voltage level. If it is too low to permit valid data recording, write current is inhibited. With VCC voltage level above the inhibiting value, control of write current is provided by the mode selection inputs.

READ MODE

In Read Mode, (R/$\overline{\text{W}}$ high and $\overline{\text{CS}}$ low), the circuit functions as a low noise differential amplifier. The read amplifier input terminals are determined by the Head Select inputs. The read amplifier outputs (RDX, RDY) are emitter follower sources, providing low impedance outputs. The amplifier gain polarity is non-inverting between HnX, HnY inputs and RDX, RDY outputs.

IDLE MODE

Taking $\overline{\text{CS}}$ high selects the idle mode which switches the RDX and RDY outputs into a high impedance state and deactivates the device. Power consumption in this mode is held to a minimum.

MODE SELECTION AND INDICATION CIRCUIT

Logical control inputs which select mode and head channel are TTL compatible. Their functions are described in Table1 and Table 2.

TABLE 1: Head Select Table

Head Selected	HS1	HS0
0	0	0
1	0	1
2	1	0
3	1	1

TABLE 2: Mode Select Table

Mode Select		Selected Mode	Indicating & Fault Outputs
$\overline{\text{CS}}$	R/$\overline{\text{W}}$		WUS
1	X	Idle	off
0	1	Read	off
0	0	Write	on*

* Provided that no fault is detected.

PIN DESCRIPTION

NAME	I/O	DESCRIPTION
HS0-HS1	I	Head Select. Logical combinations select one of four Heads. See Table 1.
$\overline{CS}$	I	Chip Select: a low level enables device. Has internal pull-up resistor.
R/$\overline{W}$	I	Read/Write:a high level selects read mode. Has internal pull-up resistor.
WUS	O*	Write Unsafe: a high level indicates an unsafe writing condition.
WDI	I	Write Data In: negative transition toggles direction of head current.
H0X-H3X H0Y-H3Y	I/O	X, Y head connections.
RDX, RDY	O*	X, Y Read Data: differential read signal output.
WC	-	Write Current: used to set the magnitude of the write current.
VCT	-	Voltage Center Tap: voltage source for head center tap.
VCC	-	+5V
GND	-	Ground
WBOOST**	I	A logic low signal on this pin increases the write current magnitude by typically 30%.

* When more than one R/W device is used, these signals can be wire OR'ed.
** 32R1221 only.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND. Currents into device are positive.)

PARAMETER		VALUE	UNITS
DC Supply Voltage	VCC	-0.3 to +6	VDC
Digital Input Voltage Range HS1, HS0, WDI, R/$\overline{W}$, $\overline{CS}$, $\overline{WBOOST}$		-0.3 to VCC + 0.3	VDC
Head Port Voltage Range	VH	-0.3 to VCC + 0.3	VDC
Write Current Pin Voltage	Vwc	-0.3 to VCC + 0.3	VDC
WUS Pin Voltage Range	Vwus	-0.3 to +6.0	VDC
Write Current Zero–Peak	IW	60	mA
RDX, RDY Output Current	Io	-10	mA
RDX, RDY Pin Voltage		VCC + 0.3	VDC
VCT Output Current Range	Ivct	-60	mA
WUS Output Current Range	Iwus	+12	mA
Storage Temperature Range	Tstg	-65 to 150	°C
Package Temperature (20 sec Reflow)		215	°C

RECOMMENDED OPERATION CONDITIONS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
DC Supply Voltage	VCC		4.5	5.0	5.5	VDC
Head Inductance	Lh		2		15	µH
Damping Resistor	Rd	32R1220/1221 & 32R1222 only	500		2000	Ω
Write Current Range	IW		15		40	mA
Junction Temperature Range	Tj		+25		+125	°C

DC CHARACTERISTICS

(Unless otherwise specified, recommended operating conditions apply.)

POWER SUPPLY

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VCC Supply Current (ICC)	Read Mode		30	40	mA
	Idle Mode Iw = 30 mA		1.0	1.8	mA
	Write Mode		20 + Iw	30 + Iw	mA
Power Dissipation	Read Mode		150	220	mW
	Idle Mode		5	10	mW
	Write Mode		100 + 5 Iw	150 + 5 Iw	mW

DIGITAL I/O

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
VIL	Input Low Voltage $\overline{CS}$, R/$\overline{W}$ WDI, HS0, HS1				0.8	VDC
VIH	Input High Voltage $\overline{CS}$, R/$\overline{W}$ WDI, HS0, HS1		2.0			VDC
IIL	Input Low Current $\overline{CS}$, R/$\overline{W}$ WDI, HS0, HS1	VIL = 0.4V	-0.1			mA
IIH	Input High Current $\overline{CS}$, R/$\overline{W}$ WDI, HS0, HS1	VIH = 2.7V			20	µA
VOL	WUS Output Low Voltage	IOL = 4.0 mA			0.5	VDC
IOH	WUS Output High Current	VOH = 5.0V			100	µA

WRITE MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Center Tap Voltage VCT	Write Mode		Vcc - 0.9		VDC
Head Current (per side)	Write Mode, 0 ≤ VCC ≤ 3.9V	-200		200	µA
Write Current Range	1.0 kΩ ≤ Rwc ≤ 3.3 kΩ	15		40	mA
Write Current Constant "K"		24.6	30	32.4	
Iwc to Head Current Gain			20		mA/mA
Write Current Boost Factor *	$\overline{\text{WBOOST}}$ = Low	1.25	1.30	1.35	mA/mA
Unselected Head Leakage Current				85	µA
RDX, RDY Leakage	RDX, RDY = 4V Idle Mode	-100		100	µA
WDI Pulse Width (see Figure 1)	Vil ≥ 0.2V PWH	15			ns
	PWL	5			ns

* 32R1221 only

READ MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Center Tap Voltage	Read Mode		Vcc - 2.6		VDC
Input Bias Current (Differential)			50	120	µA
Output Offset Voltage	Read Mode	-400		+400	mV
Common Mode Output Voltage	Read Mode	2	Vcc - 2.3	3.5	VDC

FAULT DETECTION CHARACTERISTICS

Unless otherwise specified recommended conditions apply, Iw = 30 mA, Lh = 5 µH, Rd = 750Ω. F(WDI) = 10 MHz.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Minimum Rate of WDI Input for Safe condition		1.25			MHz
Maximum Rate of WDI Input for Unsafe condition				250	kHz
Minimum voltage value for guaranteed write current turn-on		4.25			VDC
Maximum voltage value for guaranteed write current turn-off				3.75	VDC

DYNAMIC CHARACTERISTICS AND TIMING

(Unless otherwise specified, recommended operating conditions apply and Iw = 30 mA, Lh = 5 µH, Rd = 750Ω, f(WDI) = 5 MHz, CL(RDX, RDY) ≤ 20 pF.)

WRITE MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Differential Head Voltage Swing		6.0	6.6	TBD	V(pk)
Unselected Head Transient Current	1µH ≤ Lh ≤ 9.5µH			2	mA(pk)
Differential Output Capacitance				15	pF
Differential Output Resistance	32R1220/1221/1222	10			kΩ
	32R1220R/1221R/1222R	600		960	Ω

READ MODE

Differential Voltage Gain	Vin = 1 mV RMS	200	250	300	V/V
Bandwidth (-3dB)	|Zs| < 5Ω, Vin = 1 mVpp	30			MHz
Input Noise Voltage	BW = 15 MHz, Lh = 0, Rh = 0		0.56	0.8	nV/√Hz
Differential Input Capacitance			13	17	pF
Differential Input Resistance	32R1220/1221/1222 f = 5 MHz	1.2	2.5		kΩ
	32R1220R/1221R/1222R	400		860	Ω
Common Mode Rejection Ratio	Vcm = 100 mVpp@1 MHz < f < 10 MHz	50			dB
Power Supply Rejection Ratio	Vcs =100 mVpp@1 MHz < f < 10 MHz	45			dB
Channel Separation	Unselected Channels: Vin = 20 mVpp 1 MHz < f < 10 MHz	50			dB
Single Ended Output Resistance			20	30	Ω
Output Current	AC Coupled Load, RDX to RDY	1.0	1.5		mA

DYNAMIC CHARACTERISTICS AND TIMING (continued)

SWITCHING CHARACTERISTICS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
R/$\overline{W}$	Read to Write	R/W to 90% of write current			1.0	µs
	Write to Read	R/W to 90% of 100 mV. 10 MHz Read signal envelope			1.0	µs
$\overline{CS}$	Unselect to Select	$\overline{CS}$ to 90% Iw or to 90% of 100 mV. 10 MHz Read signal envelope			1.0	µs
	Select to Unselect				0.6	µs
HS0, 1 to any Head		To 90% of 100 mV. 10 MHz Read signal envelope			0.6	µs
WUS:	Safe to Unsafe (TD1)	Write Mode, loss of WDI	1.6		8	µs
	Unsafe to Safe (TD2)	Write Mode, resumption of WDI			1.0	µs
Head Current		From 50% Points, Lh = 0				
	Prop. Delay - TD3	Rh = 0			30	ns
	Asymmetry	WDI has 50% Duty Cycle and 1 ns Rise/Fall Time			2	ns
	Rise/Fall Time	10% - 90% Points			20	ns

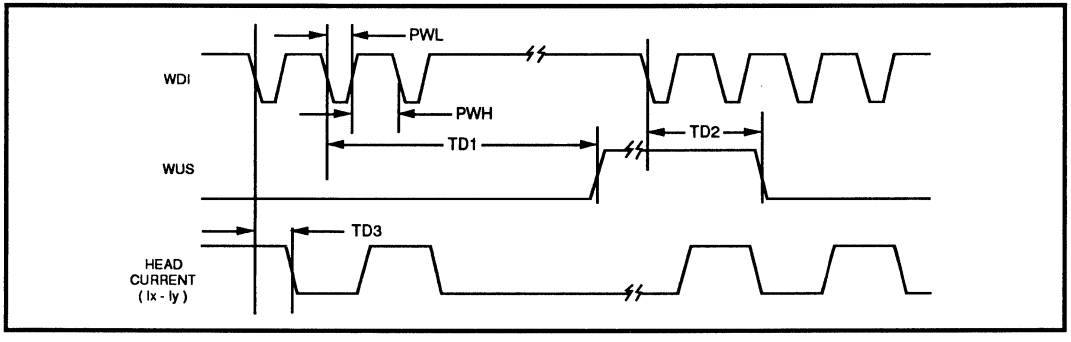
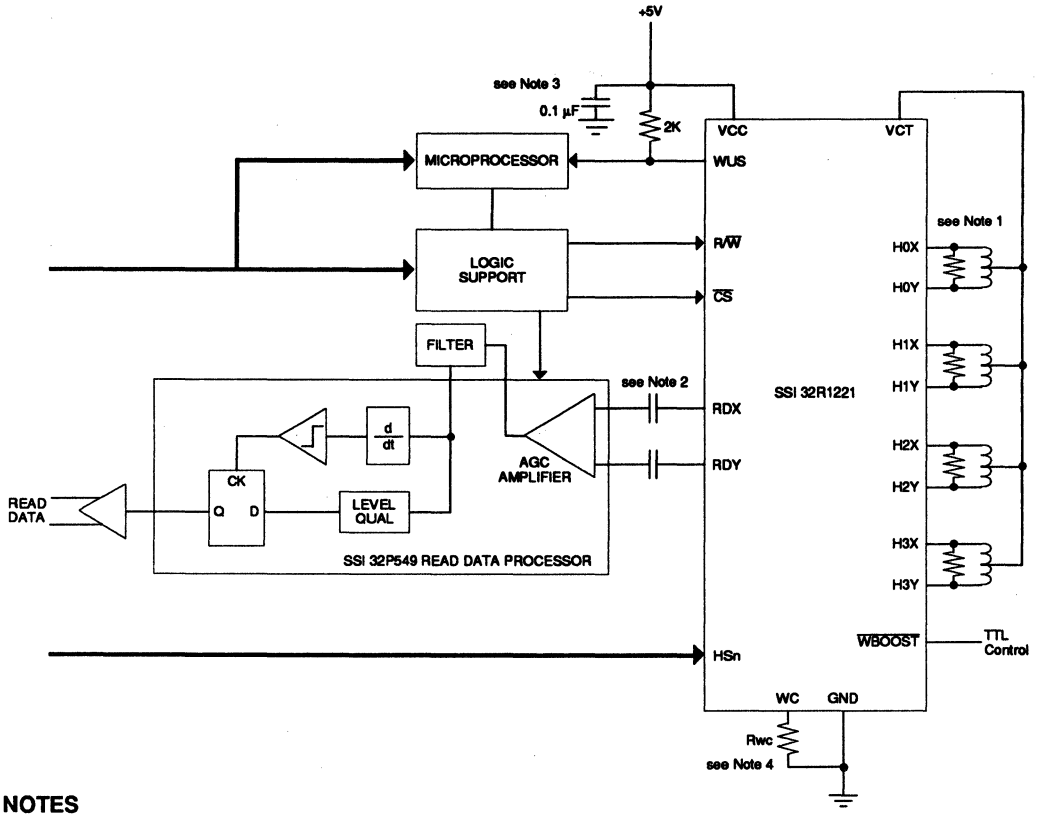


FIGURE 1: Write Mode Timing Diagram



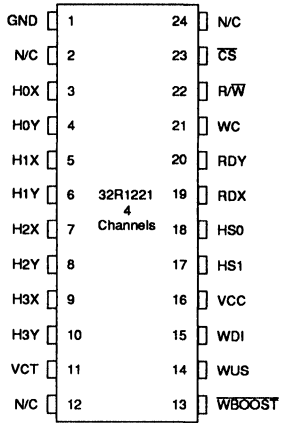
NOTES

1. Damping resistors not required on 32R1220R/1221R/1222R versions.
2. Limit DC current from RDX and RDY to 100 µA and load capacitance to 20 pF. In multi-chip application these outputs can be wire-OR'ed.
3. The power bypassing capacitor must be located close to the device with its ground returned directly to device ground, with as short a path as possible.
4. To reduce ringing due to stray capacitance this resistor should be located close to the device. Where this is not desirable a series resistor can be used to buffer a long WC line.

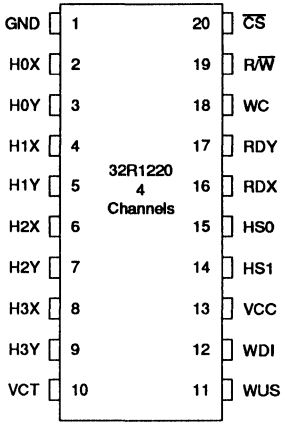
FIGURE 2: Applications Information

PACKAGE PIN DESIGNATIONS

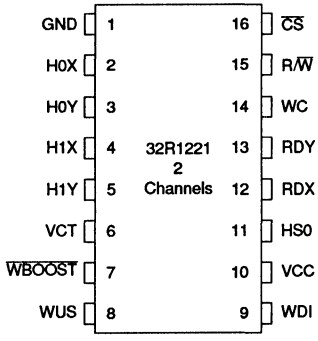
(Top View)



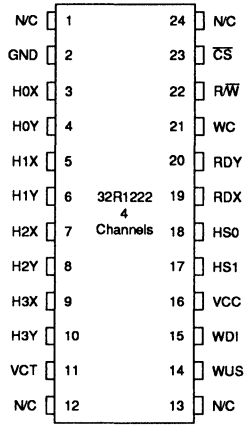
24-Pin SOL, SOV



20-Pin SOL, SOV



16-Pin SOL, SON



24-Pin SOV

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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Notes:

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SSI 32R2010R
10, 16-Channel Thin Film Read/Write Device

Advance Information

1

December 1991

DESCRIPTION

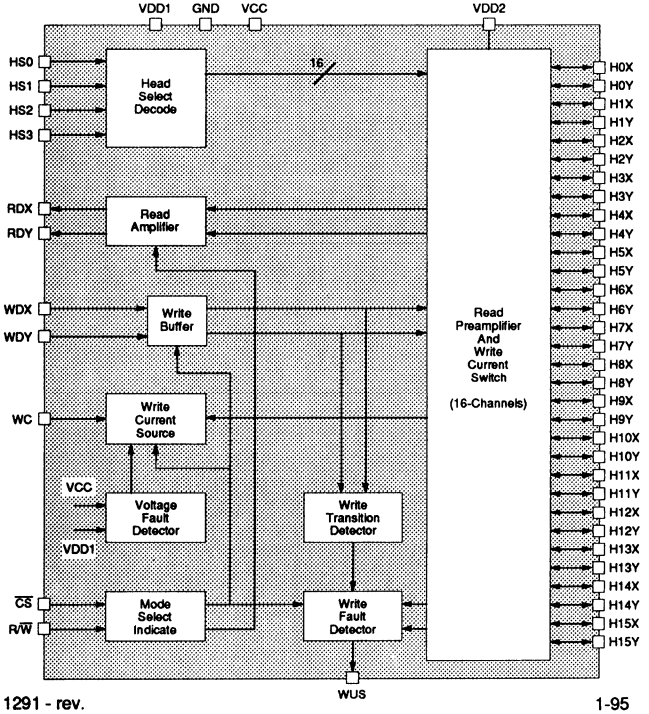
The SSI 32R2010R is an integrated read/write circuit designed for use with two terminal heads in disk drive systems. The device contains up to sixteen channels of read amplifiers and write drivers and also has an internal write current source. An internal 300Ω damping resistor is supplied in write mode, which is switched to 1 kΩ in read mode.

The circuit operates on +5V and +12V power supplies and is available in a 16 channel 52-pin package, or a 10 channel, 36 pin SO package.

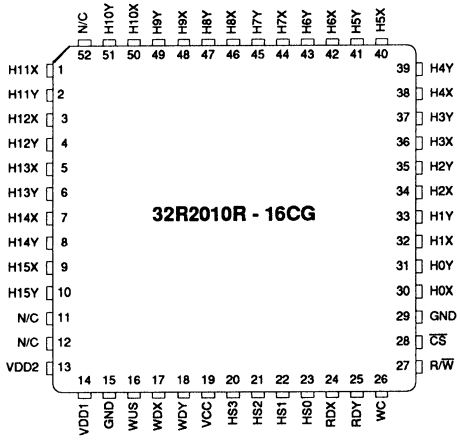
FEATURES

- **High performance**
  - **Read Mode Gain = 150 Typ V/V**
  - **Input Noise = 0.58 nV/√Hz typ.**
  - **Input Capacitance = 15 pF typ.**
  - **Write Current Range = 10 mA to 25 mA**
  - **Write Current Rise Time = 8 ns**
  - **Head Voltage Swing = 7 Vpp min**
- **Write unsafe detection**
- **Differential, ECL-like write data input**
- **Open collector read data output**
- **Switch from 300Ω damping resistor to 1 kΩ read input resistance**
- **Power supply fault protection**
- **+5V, +12V power supplies**

BLOCK DIAGRAM



PIN DIAGRAM



52-Pin Plastic QFP

CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION

The SSI 32R2010R addresses up to 16 channels with logic control inputs which are TTL compatible. Head selection is accomplished as shown in Table 1. Mode selection is accomplished as shown in Table 2. The mode select inputs have internal pull up circuits so that if an input is open it will rise to the upper logic level and force the device into a non-writing condition.

WRITE MODE

In Write Mode (R/$\overline{W}$ and $\overline{CS}$ low) the circuit functions as a current switch. The Head Select Inputs HS0, HS1, HS2 and HS3 determine the selected head. The write data inputs (WDX, WDY) determine the polarity of the head current.

The write current magnitude is adjusted by an external resistor, Rwc, from WC to GND, and is given by:

$$Iwc = Vwc/Rwc$$

Note that actual head current, Ihd, is:

$$Ihd = Iwc / (1 + \frac{Rh}{Rd}) + Ioffset$$

where Rh is head resistance, Rd is write damping resistance and Ioffset is a constant DC offset current.

WRITE MODE FAULT DETECT CIRCUIT

Several circuits are dedicated to detecting fault conditions associated with the write mode. A logical high (off) level will be present at the Write Unsafe (WUS) terminal if any of the following write fault conditions are present:

- Open head circuit
- Head shorted to ground
- Write current transition frequency too low
- Write mode not logically selected

The circuit will turn off write current when the head is shorted to ground to prevent excessive heat dissipation. This results in a pulsating WUS signal.

After the fault condition is removed, two transitions of the write data input lines are required to clear WUS. The Write Unsafe output is open-collector and is usually terminated by an external resistor connected to VCC.

Additionally, power voltage monitoring circuits are used to detect VCC and VDD1 voltage levels. If either is too low to permit valid data recording, write current is inhibited.

READ MODE

In Read Mode, (R/$\overline{W}$ high and $\overline{CS}$ low), the circuit functions as a low noise differential amplifier. The read amplifier input terminals are determined by the Head Select inputs. The read amplifier outputs (RDX, RDY) are open collector, requiring external load resistors connected to VCC. The amplifier gain polarity is non-inverting between HnX, HnY inputs and RDX, RDY outputs.

The switch from write to read modes also changes the resistance across HnX and HnY from its write damping value of 300Ω to its read mode input value of 1 kΩ.

IDLE MODE

Taking $\overline{CS}$ high selects the idle mode which switches the RDX and RDY outputs into a high impedance state and deactivates the internal write current source. This facilitates multi device installations by allowing the read outputs to be wired OR'ed and the write current programming resistor to be common to all devices.

TABLE 1: Head Select

Head Selected	HS3	HS2	HS1	HS0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

TABLE 2: Mode Select

$\overline{CS}$	R/$\overline{W}$	Mode
0	0	Write
0	1	Read
1	0	Idle
1	1	Idle

PIN DESCRIPTIONS

CONTROL INPUT PINS

NAME	TYPE	DESCRIPTION
$\overline{CS}$	I	Chip Select Input. A logical low level enables the circuit for a read or write operation. Has internal pull up.
R/$\overline{W}$	I	Read/write select. A logical low level enables the write mode (when $\overline{CS}$ is low). Has internal pull up.
HS0, HS1, HS2, HS3	I	Head select inputs. Logical combinations select one of sixteen heads. See Table 1. Has internal pull down resistors.
HEAD TERMINAL PINS		
H0X-H15X, H0Y-H15Y	I/O	X, Y Head connections: Current in the X-direction flows into the X-port.
DATA INPUT/OUTPUT PINS		
WDX, WDY	I/O	Differential write data input.
RDX, RDY	I/O	Differential Read Data output. These open collector outputs are normally terminated in 100Ω resistors to VCC.
EXTERNAL COMPONENT CONNECTION PINS		
WC	I/O	Resistor connected to GND to provide desired value of write current.
CIRCUIT MONITOR PINS		
WUS	O	Write Unsafe is an open-collector output with the off-state indicating that conditions are not proper for a write operation.
POWER, GROUND PINS		
VCC	I	+5V Logic circuit supply.
VDD1	I	+12V power supply.
VDD2	I	Positive power supply for write current drivers.
GND	I	Power supply common.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Positive Supply Voltage, VCC	6	VDC
Supply Voltage, VDD1, 2	13.5	VDC
Operating Junction Temperature	-20 to +130	°C
Storage Temperature	-65 to +130	°C
Package Temperature (20 sec. reflow)	215	°C
Input Voltages		
HS0, HS1, HS2, HS3, $\overline{CS}$, R/$\overline{W}$, WDI	-0.2 to VCC + 0.2	VDC
Head Inputs (Read Mode)	TBD	VDC
Outputs		
Read Data (RDX, RDY)	VCC -2.5 to VCC + 0.3	VDC
Write Unsafe (WUS)	-0.2V to VCC + 0.2V	VDC
Current Reference (WC)	-80 mA to 1.0 mA	VDC
Head Outputs (Write Mode)	-80 mA to 1.0 mA	mA

POWER SUPPLY

Unless otherwise specified, 4.65V ≤ VCC ≤ 5.35V, 10.8V ≤ VDD1, 2 ≤ 13.2V, 0°C ≤ T (junction) ≤ 125°C.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Power Dissipation	Idle mode		160	TBD	mW
	Read mode		400	TBD	mW
	Write mode		340 + 10 Iw	TBD	mW
Positive Supply Current (ICC)	Idle Mode		14	TBD	mA
(Includes RDX, RDY currents)	Read Mode		27	TBD	mA
	Write Mode		18	TBD	mA
Positive Supply Current (IDD1)	Idle Mode		7	TBD	mA
	Read Mode		22	TBD	mA
	Write Mode		21	TBD	mA
Positive Supply Current (IDD2)	Idle Mode			TBD	mA
	Read Mode			TBD	mA
	Write Mode			TBD	mA

DC CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
High-level Input Voltage VIH ($\overline{CS}$, R/$\overline{W}$, HS0, HS1, HS2, HS3, WDI)		2.0		-	V
Low-level Input Voltage VIL ($\overline{CS}$, R/$\overline{W}$, HS0, HS1, HS2, HS3)				0.8	V
High-level Input Current IIH ($\overline{CS}$, R/$\overline{W}$, HS0, HS1, HS2, HS3)	VIH = 2.7V			100	µA
Low-level Input Current IIL ($\overline{CS}$, R/$\overline{W}$, HS0, HS1, HS2, HS3)	VIL = 0.4V			-400	µA
High-level Output Voltage VIH (WDX, WDY)		Vcc - 1.10		Vcc - 0.81	V
Low-level Output Voltage VIL (WDX, WDY)		Vcc - 1.45		Vcc - 1.475	V
High-level Output Current IIH (WDX, WDY)				0.5	mA
Low-level Input Current IIL (WDX, WDY)		-0.5			mA
WUS, Low Level Voltage	ILUS = 8 mA (denotes safe condition)			0.5	V
WUS, High Level Current	VHUS = 5.0V (denotes unsafe condition)			100	µA

WRITE MODE

Test Conditions (Unless otherwise specified). VCC = 4.65 to 5.35V, Tj = 0 to +125°C, VDD = 10.8 to 13.2V, Lh = 470 nH, Rh = 25Ω, WDI Tr, Tf < 2 ns, Iw = 20 mA.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Current Range, Iw (±5%)		10		25	mA
Write Current Voltage, Vwc			2.0		V
Differential Head voltage Swing	Iw = 20 mA	7.0			Vpp
Ioffset			0.5		mA
Unselected Head Transient Current	Iw = 20 mA, Lh = 0.8 µH, Rh = 25Ω, Non adjacent heads tested to minimize external coupling effects			1	mA(pk)
Head Damping Resistance			300		Ω
Differential Output Capacitance				30	pF

FAULT DETECTION CHARACTERISTICS

Test conditions same as Write Mode above (unless otherwise specified.)

CHARACTERISTIC	CONDITIONS	MIN	NOM	MAX	UNIT
VCC Value for Write Current Turn off	Ih < 1 mA	3.6	4.0	4.65	V
VDD Value for Write Current Turn off	Ih < 1 mA	8.8	9.8	10.8	V
WDX, WDY Transition Frequency	WUS = Low	1.0			MHz
Max Resistance Head to GND for Short Detect	Iw = 20 mA	TBD			Ω
Voltage Across Head for Open Circuit Detect	Iw = 10 to 25 mA	1.6	2	2.8	V

READ MODE

Tests performed with 100Ω load resistors from RDX and RDY to VCC.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Differential Voltage Gain	Vin = 1 mVpp, f = 300 kHz	120	150	180	V/V
Voltage Bandwidth (-3dB)	Zs < 5Ω, Vin = 1 mVpp	50	70		MHz
(-1dB)		20			MHz
Input Noise Voltage	Zs = 0Ω , Vin = 0V, Power Bandwidth = 20 MHz		0.58	0.84	$nV\sqrt{Hz}$
Differential Input Capacitance	Vin = 0V, f = 5 MHz		15	26	pF
Differential Input Resistance	Vin = 0V, f = 5 MHz	400		1500	Ω
Dynamic Range	Input voltage where AC gain falls to 90% of the gain with 0.5 mVpp input signal	4			mVpp
Common Mode Rejection Ratio	Vin = 100 mVpp, 0V DC f = 5 MHz	50			dB
Power Supply Rejection Ratio	VCC or VDD = 100 mVpp f = 5 MHz	55			dB
Channel Separation	Unselected channels are driven with Vin = 20 mVpp @ 5MHz	43			dB
Output Offset Voltage		-360		360	mV
Output Leakage Current	Idle Mode			20	µA
Output Common Mode Voltage		VCC - 0.9	VCC - 0.5	VCC - 0.3	V
Output Voltage Compliance	Adjust RDX, Y load voltage source for <5% THD of either output.	VCC - 1.5		VCC	V

SWITCHING CHARACTERISTICS

Test conditions same as Write Mode plus RDX, Y connected to VCC through 100Ω resistors, WUS with 1 kΩ to VCC.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Idle to Read/Write Transition Time	Delay to 10 or 90% of Read Output or Write Current			0.4	µs
Read/Write to Idle Transition Time				0.4	µs
Read to Write Transition Time	VLCS = 0.8V, Delay to 90% of Iw			0.4	µs
Write to Read Transition Time	VLCS = 0.8V, Delay to 90% of 10 MHz Read Signal, 100 mV envelope			0.6	µs
Head Select Switching Delay	Read or Write Mode			0.5	µs
Head Current Rise and Fall Times 10% to 90%	Iw = 25 mA, LH = 0 nH Rh = 0Ω			TBD	ns
	Iw = 15 mA, LH = 1 µH Rh = 45Ω			TBD	ns
Head Current Rise and Fall Difference				0.5	ns
Head Current Switching Delay	50% WDI to 50% Iw			30	ns
Head Current Switching Delay Difference (Asymmetry)	WDX, WDY transitions 2 ns, switching time symmetry 0.2 ns			0.3	ns
Unsafe to Safe Delay After Write Data Begins (WUS)	f(data) = 5 MHz Write Mode			0.20	µs
Unsafe to Safe Delay After Write Mode Selected (WUS)				0.5 +Tw*	µs
Safe to Unsafe Delay (WUS)	After write mode fault condition occurs			1.50	µs
Safe to Unsafe Delay (WUS)	After exiting write mode			0.5	µs

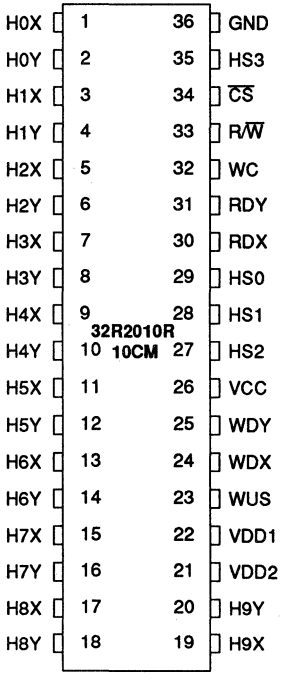
*Tw is the period of the write data input.

SSI 32R2010R
10, 16-Channel Thin Film Read/Write Device

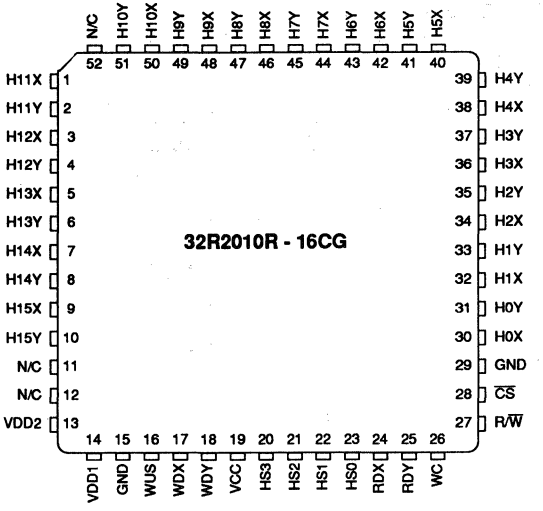
PACKAGE PIN DESIGNATIONS
(Top View)

THERMAL CHARACTERISTICS: Ø ja

52-Lead QFP	50°C/W
36-Lead SOM	45°C/W



36-Pin SOM



52-Pin Plastic QFP

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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SSI 32R2015R
16-Channel Thin Film Read/Write Device

Advance Information

1

December 1991

DESCRIPTION

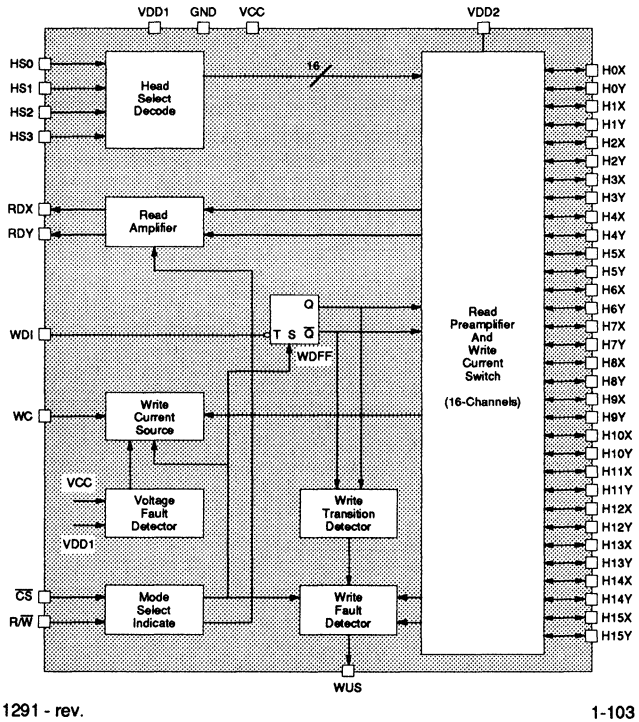
The SSI 32R2015R is an integrated read/write circuit designed for use with two terminal heads in disk drive systems. The device contains sixteen channels of read amplifiers and write drivers and also has an internal write current source. An internal 300Ω damping resistor is supplied in write mode, which is switched to 1 kΩ in read mode.

The circuit operates on +5V and +12V power supplies and is available in a 52-pin package.

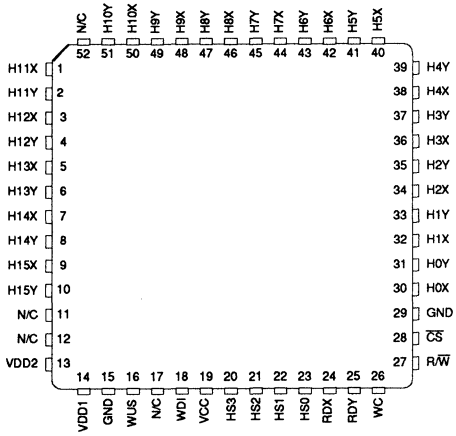
FEATURES

- **High performance**
  - **Read Mode Gain = 150 Typ V/V**
  - **Input Noise = 0.58 nV/√Hz typ.**
  - **Input Capacitance = 15 pF typ.**
  - **Write Current Range = 10 mA to 25 mA**
  - **Write Current Rise Time = 8 ns**
  - **Head Voltage Swing = 7 Vpp min**
- **Write unsafe detection**
- **TTL write data input**
- **Open collector read data output**
- **Switch from 300Ω damping resistor to 1 kΩ read input resistance**
- **Power supply fault protection**
- **+5V, +12V power supplies**

BLOCK DIAGRAM



PIN DIAGRAM



52-Pin Plastic QFP

CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION

The SSI 32R2015R addresses up to 16 channels with logic control inputs which are TTL compatible. Head selection is accomplished as shown in Table 1. Mode selection is accomplished as shown in Table 2. The mode select inputs have internal pull up circuits so that if an input is open it will rise to the upper logic level and force the device into a non-writing condition.

WRITE MODE

In Write Mode (R/$\overline{W}$ and $\overline{CS}$ low) the circuit functions as a current switch. The Head Select Inputs HS0, HS1, HS2 and HS3 determine the selected head. Write current is toggled between the X and Y direction of the selected head on each high to low transition on pin WDI, Write Data Input.

A preceding read operation initializes the Write Data Flip-Flop (WDFF) to pass data in the X-direction of the head. The write current magnitude is adjusted by an external resistor, Rwc, from WC to GND, and is given by:

$$Iwc = Vwc/Rwc$$

Note that actual head current, Ihd, is:

$$Ihd = Iwc / (1 + \frac{Rh}{Rd}) + Ioffset$$

where Rh is head resistance, Rd is write damping resistance and Ioffset is a constant DC offset current.

WRITE MODE FAULT DETECT CIRCUIT

Several circuits are dedicated to detecting fault conditions associated with the write mode. A logical high (off) level will be present at the Write Unsafe (WUS) terminal if any of the following write fault conditions are present:

- Open head circuit
- Head shorted to ground
- Write current transition frequency too low
- Write mode not logically selected

The circuit will turn off write current when the head is shorted to ground to prevent excessive heat dissipation. This results in a pulsating WUS signal.

After the fault condition is removed, two negative transitions of WDI are required to clear WUS.

The Write Unsafe output is open-collector and is usually terminated by an external resistor connected to VCC.

Additionally, power voltage monitoring circuits are used to detect VCC and VDD1 voltage levels. If either is too low to permit valid data recording, write current is inhibited.

READ MODE

In Read Mode, (R/$\overline{W}$ high and $\overline{CS}$ low), the circuit functions as a low noise differential amplifier. The read amplifier input terminals are determined by the Head Select inputs. The read amplifier outputs (RDX, RDY) are open collector, requiring external load resistors connected to VCC. The amplifier gain polarity is non-inverting between HnX, HnY inputs and RDX, RDY outputs.

The switch from write to read modes also changes the resistance across HnX and HnY from its write damping value of 300Ω to its read mode input value of 1 kΩ.

IDLE MODE

Taking $\overline{CS}$ high selects the idle mode which switches the RDX and RDY outputs into a high impedance state and deactivates the internal write current source. This facilitates multi device installations by allowing the read outputs to be wired OR'ed and the write current programming resistor to be common to all devices.

TABLE 1: Head Select

Head Selected	HS3	HS2	HS1	HS0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

TABLE 2: Mode Select

$\overline{CS}$	R/$\overline{W}$	Mode
0	0	Write
0	1	Read
1	0	Idle
1	1	Idle

PIN DESCRIPTIONS

CONTROL INPUT PINS

NAME	TYPE	DESCRIPTION
$\overline{CS}$	I	Chip Select Input. A logical low level enables the circuit for a read or write operation. Has internal pull up.
R/$\overline{W}$	I	Read/write select. A logical low level enables the write mode (when $\overline{CS}$ is low). Has internal pull up.
HS0, HS1, HS2, HS3	I	Head select inputs. Logical combinations select one of ten heads. See Table 1. Has internal pull down resistors.
HEAD TERMINAL PINS		
H0X-H15X, H0Y-H15Y	I/O	X, Y Head connections: Current in the X-direction flows into the X-port.
DATA INPUT/OUTPUT PINS		
WDI	I/O	TTL Write Data Input: a negative transition toggles the direction of the head current.
RDX, RDY	I/O	Differential Read Data output. These open collector outputs are normally terminated in 100Ω resistors to VCC.
EXTERNAL COMPONENT CONNECTION PINS		
WC	I/O	Resistor connected to GND to provide desired value of write current.
CIRCUIT MONITOR PINS		
WUS	O	Write Unsafe is an open-collector output with the off-state indicating that conditions are not proper for a write operation.
POWER, GROUND PINS		
VCC	I	+5V Logic circuit supply.
VDD1	I	+12V power supply.
VDD2	I	Positive power supply for write current drivers.
GND	I	Power supply common.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Positive Supply Voltage, VCC	6	VDC
Supply Voltage, VDD1, 2	13.5	VDC
Operating Junction Temperature	-20 to +130	°C
Storage Temperature	-65 to +130	°C
Package Temperature (20 sec. reflow)	215	°C
Input Voltages		
HS0, HS1, HS2, HS3, $\overline{CS}$, R/$\overline{W}$, WDI	-0.2 to VCC + 0.2	VDC
Head Inputs (Read Mode)	TBD	VDC
Outputs		
Read Data (RDX, RDY)	VCC -2.5 to VCC + 0.3	VDC
Write Unsafe (WUS)	-0.2V to VCC + 0.2V	VDC
Current Reference (WC)	-80 mA to 1.0 mA	VDC
Head Outputs (Write Mode)	-80 mA to 1.0 mA	mA

POWER SUPPLY

Unless otherwise specified, 4.65V ≤ VCC ≤ 5.35V, 10.8V ≤ VDD1, 2 ≤ 13.2V, 0°C ≤ T (junction) ≤ 125°C.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Power Dissipation	Idle mode		160	TBD	mW
	Read mode		400	TBD	mW
	Write mode		340 + 10 Iw	TBD	mW
Positive Supply Current (ICC)	Idle Mode		14	TBD	mA
(Includes RDX, RDY currents)	Read Mode		27	TBD	mA
	Write Mode		18	TBD	mA
Positive Supply Current (IDD1)	Idle Mode		7	TBD	mA
	Read Mode		22	TBD	mA
	Write Mode		21	TBD	mA
Positive Supply Current (IDD2)	Idle Mode			TBD	mA
	Read Mode			TBD	mA
	Write Mode			TBD	mA

DC CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
High-level Input Voltage VIH ($\overline{CS}$, R/$\overline{W}$, HS0, HS1, HS2, HS3, WDI)		2.0		-	V
Low-level Input Voltage VIL ($\overline{CS}$, R/$\overline{W}$, HS0, HS1, HS2, HS3, WDI)				0.8	V
High-level Input Current IIH ($\overline{CS}$, R/$\overline{W}$, HS0, HS1, HS2, HS3, WDI)	VIH = 2.7V			100	µA
Low-level Input Current IIL ($\overline{CS}$, R/$\overline{W}$, HS0, HS1, HS2, HS3, WDI)	VIL = 0.4V			-400	µA
WUS, Low Level Voltage	ILUS = 8 mA (denotes safe condition)			0.5	V
WUS, High Level Current	VHUS = 5.0V (denotes unsafe condition)			100	µA

WRITE MODE

Test Conditions (Unless otherwise specified). VCC = 4.65 to 5.35V, Tj = 0 to +125°C, VDD = 10.8 to 13.2V, Lh = 470 nH, Rh = 25Ω, WDI Tr, Tf < 2 ns, Iw = 20 mA.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Current Range, Iw (±5%)		10		25	mA
Write Current Voltage, Vwc			2.0		V
Differential Head voltage Swing	Iw = 20 mA	7.0			Vpp
Ioffset			0.5		mA
Unselected Head Transient Current	Iw = 20 mA, Lh = 0.8 µH, Rh = 25Ω, Non adjacent heads tested to minimize external coupling effects			1	mA(pk)
Head Damping Resistance			300		Ω
Differential Output Capacitance				30	pF

FAULT DETECTION CHARACTERISTICS

Test conditions same as Write Mode above (unless otherwise specified.)

CHARACTERISTIC	CONDITIONS	MIN	NOM	MAX	UNIT
VCC Value for Write Current Turn off	Ih < 1 mA	3.6	4.0	4.65	V
VDD Value for Write Current Turn off	Ih < 1 mA	8.8	9.8	10.8	V
WDI Transition Frequency	WUS = Low	2.0			MHz
Max Resistance Head to GND for Short Detect	Iw = 20 mA	TBD			Ω
Voltage Across Head for Open Circuit Detect	Iw = 10 to 25 mA	1.6	2	2.8	V

READ MODE

Tests performed with 100Ω load resistors from RDX and RDY to VCC.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Differential Voltage Gain	Vin = 1 mVpp, f = 300 kHz	120	150	180	V/V
Voltage Bandwidth (-3dB)	Zs < 5Ω, Vin = 1 mVpp	50	70		MHz
(-1dB)		20			MHz
Input Noise Voltage	Zs = 0Ω , Vin = 0V, Power Bandwidth = 20 MHz		0.58	0.84	$nV\sqrt{Hz}$
Differential Input Capacitance	Vin = 0V, f = 5 MHz		15	26	pF
Differential Input Resistance	Vin = 0V, f = 5 MHz	400		1500	Ω
Dynamic Range	Input voltage where AC gain falls to 90% of the gain with 0.5 mVpp input signal	4			mVpp
Common Mode Rejection Ratio	Vin = 100 mVpp, 0V DC f = 5 MHz	50			dB
Power Supply Rejection Ratio	VCC or VDD = 100 mVpp f = 5 MHz	55			dB
Channel Separation	Unselected channels are driven with Vin = 20 mVpp @ 5MHz	43			dB
Output Offset Voltage		-360		360	mV
Output Leakage Current	Idle Mode			20	µA
Output Common Mode Voltage		VCC - 0.9	VCC - 0.5	VCC - 0.3	V
Output Voltage Compliance	Adjust RDX, Y load voltage source for <5% THD of either output.	VCC - 1.5		VCC	V

SWITCHING CHARACTERISTICS

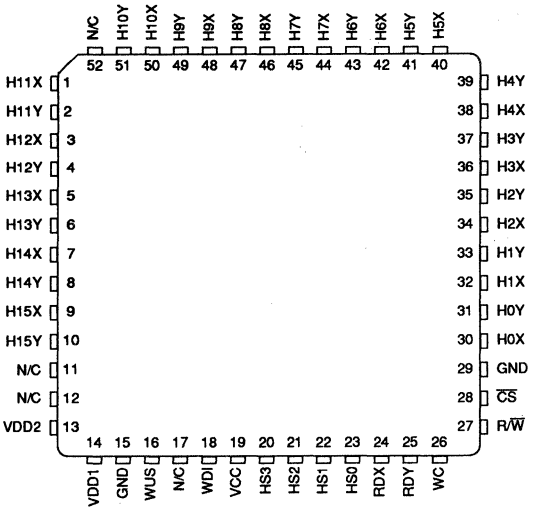
Test conditions same as Write Mode plus RDX, Y connected to VCC through 100Ω resistors, WUS with 1 kΩ to VCC.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Idle to Read/Write Transition Time	Delay to 10 or 90% of Read Output or Write Current			0.4	µs
Read/Write to Idle Transition Time				0.4	µs
Read to Write Transition Time	VLCS = 0.8V, Delay to 90% of Iw			0.4	µs
Write to Read Transition Time	VLCS = 0.8V, Delay to 90% of 10 MHz Read Signal, 100 mV envelope			0.6	µs
Head Select Switching Delay	Read or Write Mode			0.5	µs
Head Current Rise and Fall Times 10% to 90%	Iw = 25 mA, LH = 0 nH Rh = 0Ω			TBD	ns
	Iw = 15 mA, LH = 1 µH Rh = 45Ω			TBD	ns
Head Current Rise and Fall Difference				0.5	ns
Head Current Switching Delay	50% WDI to 50% Iw			30	ns
Head Current Switching Jitter (Asymmetry)	WDI transitions 2 ns, switching time symmetry 0.2 ns			0.3	ns
Unsafe to Safe Delay After Write Data Begins (WUS)	f(data) = 5 MHz			0.20	µs
Unsafe to Safe Delay After Write Mode Selected (WUS)				0.5 +Tw*	µs
Safe to Unsafe Delay (WUS)	After write mode fault condition occurs			1.50	µs
Safe to Unsafe Delay (WUS)	After exiting write mode			0.5	µs

*Tw is the period of the write data input.

SSI 32R2015R
16-Channel Thin Film Read/Write Device

PACKAGE PIN DESIGNATIONS
(Top View)



52-Pin Plastic QFP

THERMAL CHARACTERISTICS: θja

52-Lead QFP	50°C/W

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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SSI 32R2020R/2021R
5V, 2, 4, 6, 10-Channel Thin-Film Read/Write Device
Advance Information

1

December 1991

DESCRIPTION

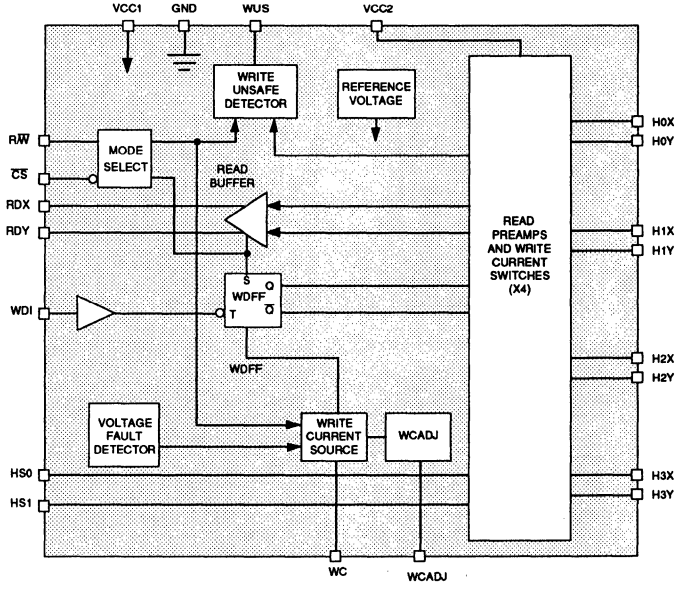
The SSI 32R2020R/2021R are bipolar monolithic integrated circuits designed for use with two-terminal recording heads. They provide a low noise read amplifier, write current control, and data protection circuitry for up to ten channels. The SSI 32R2020R/2021R provide internal 320Ω damping resistors. Damping resistors are switched in during write mode and switched out during read mode. Power supply fault protection is provided by disabling the write current generator during power sequencing. System write to read recovery time is significantly improved by controlling the read channel common mode output voltage shift in the write mode. The 32R2021R option provides the user with a controllable write current adjustment feature.

The SSI 32R2020R/2021R require only +5V power supplies and are available in a variety of packages. They are hardware compatible with the 32R4610A/4611A read/write devices.

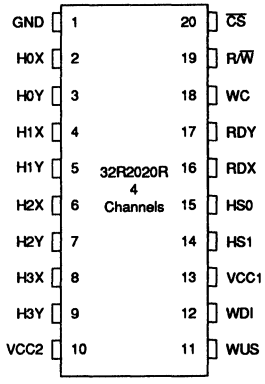
FEATURES

- **+5V ±10% supply**
- **Low power**
  - **PD = 130 mW read mode (Nom)**
  - **PD = 5 mW idle (Max)**
- **High Performance:**
  - **Read mode gain = 300 V/V**
  - **Input noise = 0.56 nV/√Hz (Nom)**
  - **Input capacitance = 15 pF (Nom)**
  - **Write current range = 5-35 mA**
- **Self switching damping resistance**
- **Designed for two-terminal thin-film or MIG heads with inductance up to 5.0 µH**
- **Pin compatible with the 32R4610AR/4611AR**
- **Write unsafe detection**
- **Power supply fault protection**
- **Head short to ground protection**

BLOCK DIAGRAM



PIN DIAGRAM



20-PIN SOL

CAUTION: Use handling procedures necessary for a static sensitive component.

WCADJ available on the 32R2021R 24-pin option only

SSI 32R2020R/2021R
5V, 2, 4, 6, 10-Channel
Thin-Film Read/Write Device

CIRCUIT OPERATION

The SSI 32R2020R/2021R have the ability to address up to 10 two-terminal heads and provide write drive or read amplification. Mode control and head selection are described in Tables 1 and 2. The TTL inputs R/$\overline{W}$ and $\overline{CS}$ have internal pull-up resistors to prevent an accidental write condition. HS0 and HS1 have internal pulldowns. Internal clamp circuitry will protect the IC from a head short to ground condition in any mode.

TABLE 1: Mode Select

$\overline{CS}$	R/$\overline{W}$	Mode
0	0	Write
0	1	Read
1	0	Idle
1	1	Idle

TABLE 2: Head Select

HS3	HS2	HS1	HS0	Head
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
HS0, HS1, † HS2, HS3	I	Head Select: selects one of ten heads
$\overline{CS}$	I	Chip Select: a high inhibits the chip
R/$\overline{W}$ †	I	Read/Write : a high selects Read mode
WUS †	O	Write Unsafe: a high indicates an unsafe writing condition
WDI †	I	Write Data In: changes the direction of the current in the recording head
H0X - H3X; H0Y - H3Y	I/O	X, Y Head Connections
RDX, RDY †	O	X, Y Read Data: differential read data output
WC †		Write Current: used to set the magnitude of the write current
WCADJ* †		Write Current Adjust: Used to fine tune the write current
VCC1	I	+5V Supply
VCC2	I	+5V Supply for Write current drivers
GND	I	Ground

* Available on 32R2021R 24-pin option only

† When more that one R/W device is used, signals can be wire OR'ed

WRITE MODE

Taking both $\overline{CS}$ and R/$\overline{W}$ low selects write mode which configures the SSI 32R2020R/2021R as a current switch and activates the Write Unsafe (WUS) detector circuitry. Head current is toggled between the X and Y side of the selected head on each high to low transition of the Write Data Input (WDI). Note that a preceding read or idle mode select initializes the Write Data Flip-Flop to pass write current through the "X" side of the head. The magnitude of the write current (0-pk) is given by:

$$IW = \frac{K \cdot VWC}{RWC}$$

RWC is connected from pin WC to GND. Note the actual head current Ix, y is given by:

$$Ix, y = \frac{Iw}{1 + Rh/Rd}$$

Where:

Rh = Head resistance plus external wire resistance

Rd = Damping resistance

In write mode a 320Ω damping resistor is switched in across the Hx, Hy ports.

The 32R2021R adds a feature which allows the user to adjust the Iw current by a finite amount. The WCADJ pin is used to adjust write current for write operations on different zones of the disk. It is used by switching a separate write current adjust resistor in and out on the WCADJ pin or by connecting a DAC to that pin to sink a controllable amount of current. The WCADJ pin is nominally biased to VCC/2. Sinking current from this pin to ground will divert a proportional amount of current from the actual head current while maintaining a constant current through the WC resistor and VCC. Allowing WCADJ to float or pulling it high will cut off the circuit and it will have no effect. A TTL gate can be used as a switch with a small degradation in accuracy. The amount of write current decrease is shown below:

Iw head (decrease) (mA) = (29 • V_{WCADJ}/R_{WCADJ})

where:

V_{WCADJ} = Vcc/2 (volts)

R_{WCADJ} = write current adjust setting resistor (kΩ)

Example: For a 7.25 mA head current decrease, R_{WCADJ} = (29 • 2.5) / 7.25 = 10 kΩ

VOLTAGE FAULT

A voltage Fault detection circuit improves data security by disabling the write current generator during a voltage fault or power startup regardless of mode.

WRITE UNSAFE

Any of the following conditions will be indicated as a high level on the Write Unsafe, WUS, open collector output.

- WDI frequency too low
- Device in Read mode
- Chip disabled
- No head current
- Head opened

To insure no false WUS trigger, the product of head current and head resistance (Ixy • R_H) should be between 100 mV and 1.7V.

After the fault condition is removed, one negative transition on WDI is required to clear WUS.

READ MODE

The Read mode configures the SSI 32R2020R/2021R as a low noise differential amplifier and deactivates the write current generator. The damping resistor is switched out of the circuit allowing a high impedance input to the read amplifier. The RDX and RDY output are driven by emitter followers. They should be AC coupled to the load. The (X,Y) inputs are non-inverting to the (X,Y) outputs.

Note that in Idle or Write mode, the read amplifier is deactivated and RDX, RDY outputs become high impedance. This facilitates multiple R/W applications (wired-OR RDX, RDY) and minimizes voltage drifts when switching from Write to Read mode. Note also that the write current source is deactivated for both the Read and Idle mode.

IDLE MODE

Taking $\overline{CS}$ high selects the idle mode which switches the RDX and RDY outputs into a high impedance state and deactivates the device. Power consumption in this mode is held to a minimum.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may permanently damage the device.

PARAMETER		RATING	UNIT
DC Supply Voltage	VCC1	-0.3 to +6	VDC
	VCC2	-0.3 to +6	VDC
Write Current	Iw	60	mA
Digital Input Voltage	Vin	-0.3 to VCC1 +0.3	VDC
Head Port Voltage	VH	-0.3 to VCC2 +0.3	VDC
Output Current: RDX, RDY	I0	-10	mA
WUS		+12	mA
Storage Temperature	Tstg	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

DC Supply Voltage	VCC1 = VCC2	5 ±10%	VDC
Operating Junction Temperature	Tj	+25 to +110	°C
Recommended Head Load Range	Lh	0.3 - 5.0	µH

DC CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VCC1 Supply Current	Read Mode		20		mA
	Write Mode		25		mA
	Idle Mode		0.6		mA
VCC2 Supply Current	Read Mode		7		mA
	Write Mode		4 + Iw		mA
	Idle Mode		0		mA
Power Dissipation	Read Mode		135	TBD	mW
	Write Mode		145 + 4Iw	TBD	mW
	Idle Mode		3	TBD	mW
VCC1 Fault Voltage	Iw < 0.2 mA	3.5	3.9	4.2	VDC

DIGITAL INPUTS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Input Low voltage (VIL)				0.8	VDC
Input High Voltage (VIH)		2.0			VDC
Input Low Current	VIL = 0.8V	-0.4			mA
Input High Current	VIH = 2.0V			100	µA
WUS Output Low Voltage (VOL)	Iol = 2 mA max			0.5	VDC

WRITE CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.

Write Current Constant "K"				.99		
Write Current Voltage (VWC)			1.15	1.25	1.35	V
WCADJ Voltage SSI 32R2021R	I_{WCADJ} = 0 to .5 mA		2.0	VCC/2	3.0	VDC
Ihead(Decrease)/I_{WCADJ} SSI 32R2021R			26	29	32	mA/mA
I_{WCADJ} Range SSI 32R2021R			0.0		0.5	mA
Differential Head Voltage Swing	Ih(p-p) • Rh not to exceed 3.4V (head swing min)		3.4			Vpp
Unselected Head Current					1	mA (pk)
Head Differential Load Capacitance					25	pF
Head Differential Load Resistance (Rd)				320		Ω
WDI Pulse Width	Vil ≥ 0.2V	PWH	10			ns
		PWL	5			ns
Write Current Range (Iw)			5		35	mA

READ CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. CL (RDX, RDY) < 20 pF, RL (RDX, RDY) = 1 kΩ.

Differential Voltage Gain		Vin = 1 mVpp @1 MHz	250	300	350	V/V
Voltage BW	-1dB	|Zs| < 5Ω, Vin = 1 mVpp	20			MHz
	-3dB		35			MHz
Input Noise Voltage		BW = 15 MHz, Lh = 0, Rh = 0		0.56	0.8	nV/√Hz
Differential Input Capacitance		Vin = 1 mVpp, f = 5 MHz		15	20	pF
Differential Input Resistance		Vin = 1 mVpp, f = 5 MHz	720	1200		Ω

READ CHARACTERISTICS (Continued)
Recommended operating conditions apply unless otherwise specified. CL (RDX, RDY) < 20 pF, RL (RDX, RDY) = 1 kΩ.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Dynamic Range	AC input voltage where gain falls to 90% of its small signal gain value, f = 5 MHz	2			mVpp
Common Mode Rejection Ratio	Vin = 0 VDC + 100 mVpp @ 5 MHz	45			dB
Power Supply Rejection Ratio	100 mVpp @ 5 MHz on VCC	40			dB
Channel Separation	Unselected channels driven with Vin = 0 VDC + 100 mVpp	45			dB
Output Offset Voltage				±300	mV
Single Ended Output Resistance	f = 5 MHz			50	Ω
Output Current	AC coupled load, RDX to RDY	1			mA
RDX, RDY Common Mode Output Voltage		2.0	Vcc/2	3.5	VDC

SWITCHING CHARACTERISTICS
Recommended operating conditions apply unless otherwise specified. IW = 20 mA, Lh = 1.0 µH, Rh = 30Ω f(Data) = 5 MHz.

R/$\overline{W}$	Read to Write	R/W to 90% of write current		0.1	0.6	µs
	Write to Read	R/W to 90% of 100 mV Read signal envelope		TBD	1	µs
$\overline{CS}$	Unselect to Select	$\overline{CS}$ to 90% of write current or to 90% of 100 mV 10 MHz		0.15	2	µs
	Select to Unselect	$\overline{CS}$ to 10% of write current		0.11	0.6	µs
HS0,1 to any Head		To 90% of 100 mV 10 MHz Read signal envelope		TBD	1	µs
WUS:	Safe to Unsafe (TD1)	Write mode, loss of WDI transitions. Defines maximum WDI period for WUS operation	0.6	2.0	3.6	µs
	Unsafe to Safe (TD2)	Fault cleared from first neg WDI transition		0.2	1.0	µs
Head Current:		Lh = 0, Rh = 0				
	WDI to Ix - Iy (TD3)	from 50% points		15	32	ns
	Asymmetry	WDI has 1 ns rise/fall time			1.0	ns
	Rise/fall Time	10% to 90% points			9.0	ns

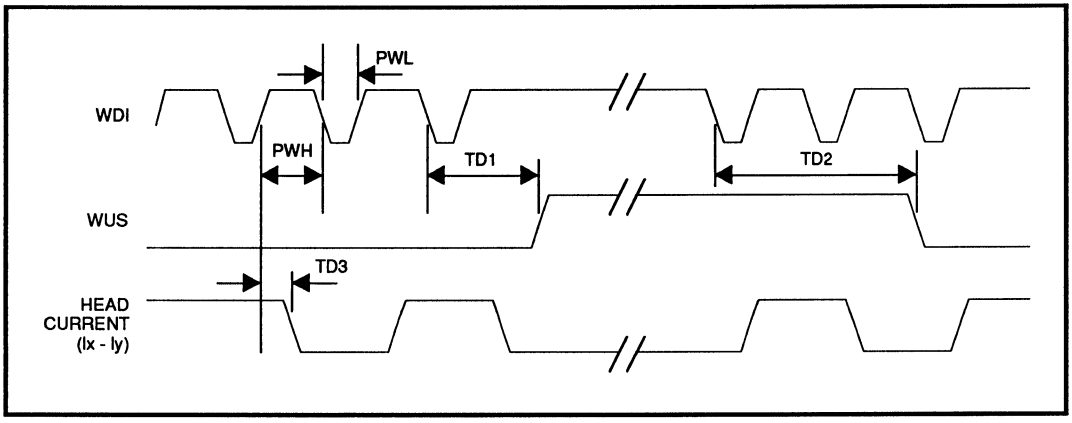


FIGURE 1: Write Mode Timing Diagram

Worst Case Read Input Noise Voltage vs. Input Impedance for SSI 32R2020R/2021R

Case 1: IC Base sheet resistance = Maximum
Hence, IC bias current = Minimum

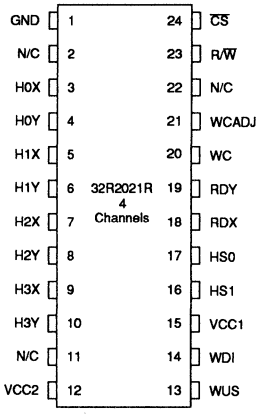
	Tj = 25°C	Tj = 110°C	Units
Vn (Max)	TBD	TBD	$nV/\sqrt{Hz}$
Rin (Min)	TBD	TBD	Ω
Cin (Max)	TBD	TBD	pF

Case 2: IC Base sheet resistance = Minimum
Hence, IC bias current = Maximum

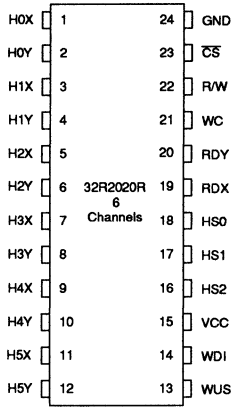
	Tj = 25°C	Tj = 110°C	Units
Vn (Max)	TBD	TBD	$nV/\sqrt{Hz}$
Rin (Min)	TBD	TBD	Ω
Cin (Max)	TBD	TBD	pF

SSI 32R2020R/2021R
5V, 2, 4, 6, 10-Channel
Thin-Film Read/Write Device

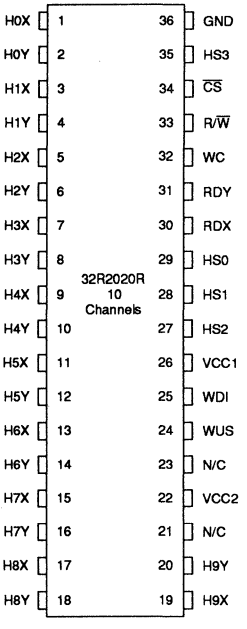
PACKAGE PIN DESIGNATIONS
(Top View)



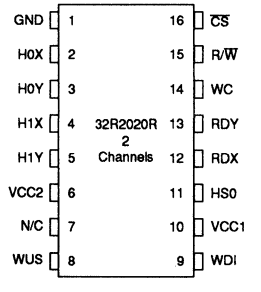
24-Pin SOL, SOV



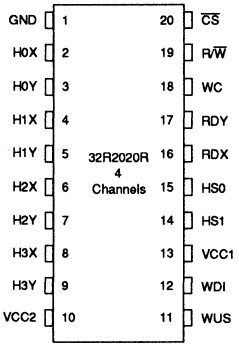
24-Pin SOV



36-Pin SOM



16-Pin SOL



20-Pin SOL, SOV

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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SSI 32R2030A/2031A
5V, 2, 4-Channel Thin-Film Read/Write Device

Advance Information

1

December 1991

DESCRIPTION

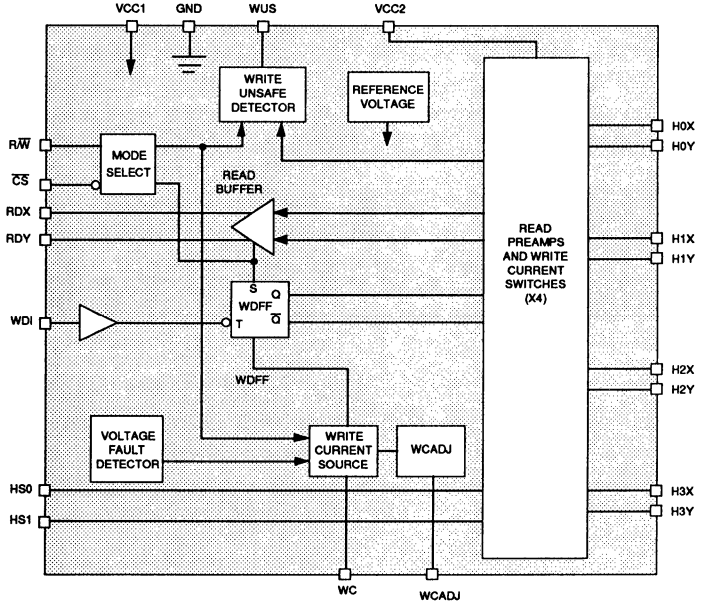
The SSI 32R2030A/2031A are bipolar monolithic integrated circuits designed for use with two-terminal thin-film recording heads. They provide a low noise read amplifier, write current control, and data protection circuitry for up to four channels. The SSI 32R2030AR/2031AR option provides internal 700Ω damping resistors. Power supply fault protection is provided by disabling the write current generator during power sequencing. System write to read recovery time is significantly improved by controlling the read channel common mode output voltage shift in the write mode. The 32R2031A option provides for an additional feature providing the user with a controllable write current adjustment feature.

The SSI 32R2030A/2031A require only +5V power supplies and are available in a variety of packages.

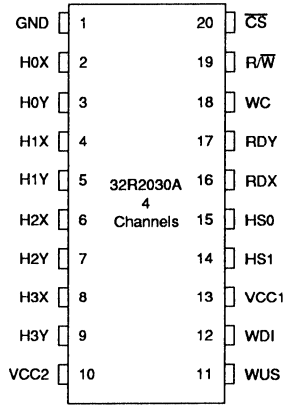
FEATURES

- **5V ±10%**
- **Low power**
  - **PD = 175 mW read mode (Nom)**
- **High Performance:**
  - **Read mode gain = 250 V/V**
  - **Input noise = 0.85 nV/√Hz max**
  - **Input capacitance = 35 pF max**
  - **Write current range = 10-35 mA**
- **Designed for two-terminal thin-film heads or MIG heads up to 5 μH**
- **Programmable write current source**
- **Write unsafe detection**
- **Enhanced system write to read recovery time**
- **Power supply fault protection**
- **Head short to ground protection**

BLOCK DIAGRAM



PIN DIAGRAM



20-PIN SOL

CAUTION: Use handling procedures necessary for a static sensitive component.

WCADJ available on the 32R2031A 24-pin option only

SSI 32R2030A/2031A
5V, 2, 4-Channel Thin-Film Read/Write Device

CIRCUIT OPERATION

The SSI 32R2030A/2031A has the ability to address up to 4 two-terminal thin-film heads and provide write drive or read amplification. Head selection and mode control are described in Tables 2 and 3. The TTL inputs R/$\overline{W}$ and $\overline{CS}$ have internal pull-up resistors to prevent an accidental write condition. HS0, and HS1 have internal pulldowns. Internal clamp circuitry will protect the IC from a head short to ground condition in any mode.

TABLE 1: Mode Select

$\overline{CS}$	R/$\overline{W}$	Mode
0	0	Write
0	1	Read
1	0	Idle
1	1	Idle

TABLE 2: Head Select

HS1	HS0	Head
0	0	0
0	1	1
1	0	2
1	1	3

PIN DESCRIPTION

NAME		TYPE	DESCRIPTION
HS0, HS1		I	Head Select: selects one of four heads
$\overline{CS}$		I	Chip Select: a high inhibits the chip
R/$\overline{W}$	†	I	Read/Write : a high selects Read mode
WUS	†	O	Write Unsafe: a high indicates an unsafe writing condition
WDI	†	I	Write Data In: changes the direction of the current in the recording head
H0X - H7X; H0Y - H7Y		I/O	X, Y Head Connections
RDX, RDY	†	O	X, Y Read Data: differential read data output
WC	†		Write Current: used to set the magnitude of the write current
WCADJ*	†		Write Current Adjust: Used to decrease the write current by a finite amount
VCC1		I	+5V Supply
VCC2		I	+5V Supply for Write current drivers
GND		I	Ground

*Available on 32R2031A 24-pin option only

† These signals can be wire OR'ed

WRITE MODE

Taking both $\overline{CS}$ and R/$\overline{W}$ low selects write mode which configures the SSI 32R2030A/2031A as a current switch and activates the Write Unsafe (WUS) detector circuitry. Head current is toggled between the X and Y side of the selected head on each high to low transition of the Write Data Input (WDI). The WDI input pulse width requirement is amplitude dependent and pull ups are recommended at higher data rates, please refer to the WDI pulse width specifications. Note that a preceding read or idle mode select initializes the Write Data Flip-Flop to pass write current through the "X" side of the head. The magnitude of the write current (0-pk) is given by:

$$IW = \frac{K \cdot VWC}{RWC}$$

RWC is connected from pin WC to GND. Note the actual head current Ix, y is given by:

$$Ix, y = \frac{Iw}{1 + Rh/Rd}$$

Where:

Rh = Head resistance plus external wire resistance

Rd = Damping resistance

Any of the following conditions will be indicated as a high level on the Write Unsafe, WUS, open collector output.

- WDI frequency too low
- Device in Read mode
- Chip disabled
- No write current

After fault condition is removed, one negative transition on WDI is required to clear WUS.

The 32R2031A adds a feature which allows the user to adjust the Iw current by a finite amount. The WCADJ pin is used to adjust write current for write operations on different zones of the disk. It is used by switching a separate write current adjust resistor in and out on the WCADJ pin or by connecting a DAC to that pin to sink a controllable amount of current. The WCADJ pin is nominally biased to VCC/2. Sinking current from this pin to ground will divert a proportional amount of current from the actual head current while maintaining a constant current through the WC resistor and VCC. Allowing WCADJ to float or pulling it high will cut off the circuit and it will have no effect. For example, if the nominal head current is set to 30 mA through WC with WCADJ open, then for a 7.25 mA head current decrease, a 10 kΩ resistor would be connected from the WCADJ pin to ground. A TTL gate could be used as a switch with a small degradation in accuracy. To perform the same function, a DAC could be used, by programming it to sink 0.25 mA from the WCADJ pin.

Iw head (Decrease) = (29 • V_{WCADJ} / R_{WCADJ})

Where:

VWCADJ = Voltage on WCADJ pin = VCC/2

RWCADJ = Write current adjust setting resistor

VOLTAGE FAULT

A voltage Fault detection circuit improves data security by disabling the write current generator during a voltage fault or power startup regardless of mode.

READ MODE

The Read mode configures the SSI 32R2030A/2031A as a low noise differential amplifier and deactivates the write current generator. The RDX and RDY output are driven by emitter followers. They should be AC coupled to the load. The (X,Y) inputs are non-inverting to the (X,Y) outputs.

Note that in Idle or Write mode, the read amplifier is deactivated and RDX, RDY outputs become high impedance. This facilitates multiple R/W applications (wired-OR RDX, RDY) and minimizes voltage drifts when switching from Write to Read mode. Note also that the write current source is deactivated for both the Read and Idle mode.

IDLE MODE

Taking $\overline{CS}$ high selects the idle mode which switches the RDX and RDY outputs into a high impedance state and deactivates the device. Power consumption in this mode is held to a minimum.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may permanently damage the device.

PARAMETER		RATING	UNIT
DC Supply Voltage	VCC1	-0.3 to +7	VDC
	VCC2	-0.3 to +7	VDC
Write Current	IW	80	mA
Digital Input Voltage	Vin	-0.3 to VCC1 +0.3	VDC
Head Port Voltage	VH	-0.3 to VCC2 +0.3	VDC
Output Current: RDX, RDY	I0	-10	mA
WUS		+12	mA
Storage Temperature	Tstg	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		RATING	UNIT
DC Supply Voltage	VCC1	5 ±10%	VDC
	VCC2	5 ±10%	VDC
Operating Junction Temperature	Tj	+25 to +110	°C

DC CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.

PARAMETER	CONDITIONS		MIN	NOM	MAX	UNIT
VCC1 Supply Current	Read Mode	(Vcc ±5%)	23	28	33	mA
		(Vcc ±10%)	19	28	37	mA
	Write Mode	(Vcc ±5%)	21	24	27	mA
		(Vcc ±10%)	17	24	31	mA
**Head Select Pins*	*Idle Mode	(Vcc ±5%)	6	9	12	mA
(HS0, HS1) Floating		(Vcc ±10%)	4	9	14	mA
VCC2 Supply Current	Read Mode	(Vcc ±5%)	5	8	11	mA
		(Vcc ±10%)	4	8	12	mA
	Write Mode	(Vcc ±5%)	6	8 + Iw	10 + Iw	mA
		(Vcc ±10%)	5	8 + Iw	11 + Iw	mA
	Idle Mode	(Vcc ±5%)	0.1	0.2	0.4	mA
		(Vcc ±10%)	0.1	0.2	0.5	mA
Power Dissipation	Read Mode	(Vcc ±5%)		175	230	mW
		(Vcc ±10%)			270	mW

DC CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS		MIN	NOM	MAX	UNIT
Power Dissipation (Continued)	Write Mode	(Vcc ±5%)		150 + 4Iw	190 + 4Iw	mW
		(Vcc ±10%)			230 + 4.4Iw	mW
	Idle Mode	(Vcc ±5%)		50	65	mW
		(Vcc ±10%)			80	mW
VCC1 Fault Voltage	IW < 0.2 mA		3.8	4.0	4.2	VDC

DIGITAL INPUTS

Input Low voltage (VIL)				0.8	VDC
Input High Voltage (VIH)		2.0			VDC
Input Low Current	VIL = 0.8V	-0.4			mA
Input High Current	VIH = 2.0V			100	µA
WUS Output Low Voltage (VOL)	Iol = 2 mA max			0.5	VDC

WRITE CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.

Write Current Constant "K"		.96	.99		
Write Current Voltage (VWC)		1.15	1.25	1.35	V
WCADJ Voltage SSI 32R2031A/2031AR	I_{WCADJ} = 0 to .5 mA	2.0	VCC/2	3.0	VDC
Ihead(Decrease)/I_{WCADJ} SSI 32R2031A/2031AR		26	29	32	mA/mA
I_{WCADJ} Range SSI 32R2031A/2031AR		0.0		0.5	mA
Differential Head Voltage Swing	Ih (p-p) • Rh not to exceed 3.4V (Head Swing Min)	3.4			Vpp
Unselected Head Current				0.02 Iw	mApk
Head Differential Load Capacitance				25	pF
Head Differential Load	SSI 32R2030A/32R2031A	4K			Ω
Resistance (Rd)	SSI 32R2030AR/32R2031AR	560	700	950	Ω
WDI Pulse Width	Vil = 0.2V, Vih = 2.4V PWH	37			ns
(Ref: Figure 1)	PWL	5			ns
	Vil = 0.2V, Vih = VCC PWH	20			ns
	PWL	5			ns
Write Current Range (IW)		10		35	mA

READ CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. CL (RDX, RDY) < 20 pF, RL (RDX, RDY) = 1 kΩ.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Differential Voltage Gain	Vin = 1 mVpp @1 MHz	200	250	300	V/V
Voltage BW -1dB	|Zs| < 5Ω, Vin = 1 mVpp	20	60		MHz
-3dB		35	70		MHz
Input Noise Voltage	BW = 15 MHz, Lh = 0, Rh = 0		0.6	0.85	nV/√Hz
Differential Input Capacitance	Vin = 1 mVpp, f = 5 MHz		27	35	pF
Differential Input Resistance	Vin = 1 mVpp, f = 5 MHz SSI 32R2030A/2031A	835	2600		Ω
	SSI 32R2030AR/2031AR	360	550		Ω
Dynamic Range	AC input voltage where gain falls to 90% of its small signal gain value, f = 5 MHz	3	6		mVpp
Common Mode Rejection Ratio	Vin = 0 VDC + 100 mVpp @ 5 MHz	45	80		dB
Power Supply Rejection Ratio	100 mVpp @ 5 MHz on VCC	40	70		dB
Channel Separation	Unselected channels driven with Vin = 0 VDC + 100 mVpp	45			dB
Output Offset Voltage		-300		+300	mV
Single Ended Output Resistance	f = 5 MHz			40	Ω
Output Current	AC coupled load, RDX to RDY	1.4			mA
RDX, RDY Common Mode Output Voltage		2.0	VCC1/2	3.5	VDC

SWITCHING CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. IW = 20 mA, Lh = 1.0 µH, Rh = 30Ω f(Data) = 5 MHz.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
R/$\overline{W}$	Read to Write	R/W to 90% of write current		0.1	1.0	µs
	Write to Read	R/W to 90% of 100 mV Read signal envelope		0.5	1.0	µs
$\overline{CS}$	Unselect to Select	$\overline{CS}$ to 90% of write current or to 90% of 100 mV 10 MHz		0.4	1.0	µs
	Select to Unselect	$\overline{CS}$ to 10% of write current		0.4	1.0	µs
HS0,1 to any Head		To 90% of 100 mV 10 MHz Read signal envelope		0.2	1.0	µs
WUS:	Safe to Unsafe (TD1)	Write mode, loss of WDI transitions. Defines maximum WDI period for WUS operation	0.6	2.0	3.6	µs
	Unsafe to Safe (TD2)	Fault cleared from first neg WDI transition		0.2	1.0	µs
Head Current:		Lh = 0, Rh = 0				
	WDI to Ix - Iy (TD3)	from 50% points		20	32	ns
	Asymmetry	WDI has 1 ns rise/fall time			1.0	ns
	Rise/fall Time	10% to 90% points		6	12	ns

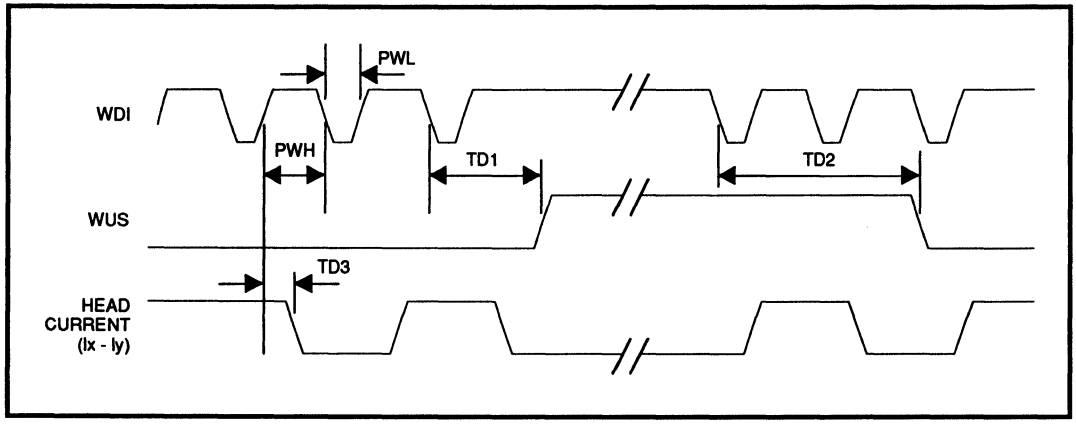


FIGURE 1: Write Mode Timing Diagram

Worst Case Read Input Noise Voltage vs. Input Impedance for SSI 32R2030AR/2031AR

Case 1: IC Base sheet resistance = Maximum
Hence, IC bias Current = Minimum

	Tj = 25°C	Tj = 110°C	Units
Vn (Max)	.7	0.85	$nV/\sqrt{Hz}$
Rin (Min)	450	475	Ω
Cin (Max)	28	30	pF

Case 2: IC Base sheet resistance = Minimum
Hence, IC bias Current = Maximum

	Tj = 25°C	Tj = 110°C	Units
Vn (Max)	.58	.65	$nV/\sqrt{Hz}$
Rin (Min)	360	400	Ω
Cin (Max)	33	35	pF

Worst Case Read Input Noise Voltage vs. Input Impedance for SSI 32R2030A/2031A

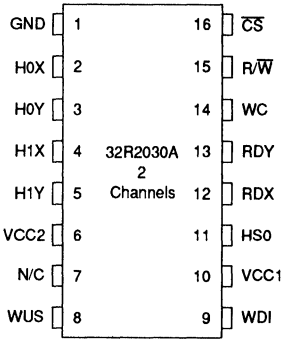
Case 1: IC Base sheet resistance = Maximum
Hence, IC bias Current = Minimum

	Tj = 25°C	Tj = 110°C	Units
Vn (Max)	.7	0.85	$nV/\sqrt{Hz}$
Rin (Min)	1525	1895	Ω
Cin (Max)	28	30	pF

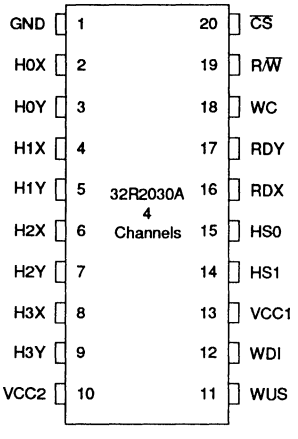
Case 2: IC Base sheet resistance = Minimum
Hence, IC bias Current = Maximum

	Tj = 25°C	Tj = 110°C	Units
Vn (Max)	.58	.65	$nV/\sqrt{Hz}$
Rin (Min)	835	1100	Ω
Cin (Max)	33	35	pF

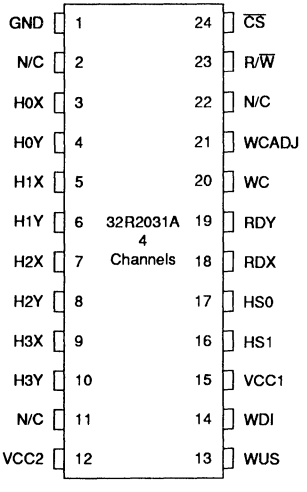
PACKAGE PIN DESIGNATIONS
(Top View)



16-Pin SOL



20-Pin SOL, SOV



24-Pin SOL, SOV

THERMAL CHARACTERISTICS: θja

16-Pin SOL	105°C/W
20-Pin SOL	95°C/W
20-Pin SOV	125°C/W
24-Pin SOL	80°C/W

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do no use for final design.

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Notes:

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SSI 32R4610A/4611A
5V, 2, 4, 8-Channel Thin-Film Read/Write Device

Advance Information

1

December 1991

DESCRIPTION

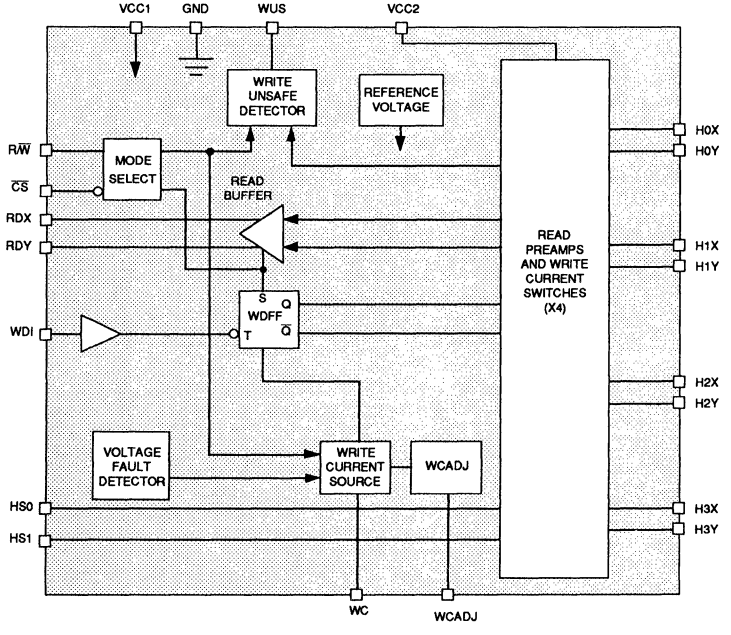
The SSI 32R4610A/4611A are bipolar monolithic integrated circuits designed for use with two-terminal thin-film recording heads. They provide a low noise read amplifier, write current control, and data protection circuitry for up to eight channels. The SSI 32R4610AR/4611AR option provides internal 700Ω damping resistors. Power supply fault protection is provided by disabling the write current generator during power sequencing. System write to read recovery time is significantly improved by controlling the read channel common mode output voltage shift in the write mode. The 32R4611A option provides for an additional feature providing the user with a controllable write current adjustment feature.

The SSI 32R4610/4611 require only +5V power supplies and are available in a variety of packages.

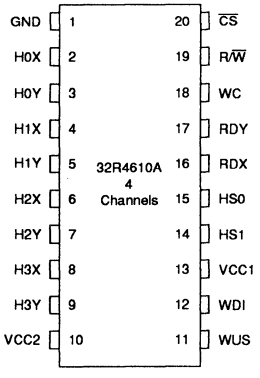
FEATURES

- **5V ±10%**
- **Low power**
  - **PD = 175 mW read mode (Nom)**
- **High Performance:**
  - **Read mode gain = 200 V/V**
  - **Input noise = 0.85 nV/√Hz max**
  - **Input capacitance = 35 pF max**
  - **Write current range = 10-35 mA**
- **Designed for two-terminal thin-film heads**
- **Programmable write current source**
- **Write unsafe detection**
- **Enhanced system write to read recovery time**
- **Power supply fault protection**
- **Head short to ground protection**

BLOCK DIAGRAM



PIN DIAGRAM



20-PIN SOL

CAUTION: Use handling procedures necessary for a static sensitive component.

WCADJ available on the 32R4611A 24-pin option only

SSI 32R4610A/4611A
5V, 2, 4, 8-Channel Thin-Film Read/Write Device

CIRCUIT OPERATION

The SSI 32R4610A/4611A has the ability to address up to 8 two-terminal thin-film heads and provide write drive or read amplification. Head selection and mode control are described in Tables 2 and 3. The TTL inputs R/$\overline{W}$ and $\overline{CS}$ have internal pull-up resistors to prevent an accidental write condition. HS0, HS1 and HS2 have internal pulldowns. Internal clamp circuitry will protect the IC from a head short to ground condition in any mode.

TABLE 1: Mode Select

$\overline{CS}$	R/$\overline{W}$	Mode
0	0	Write
0	1	Read
1	0	Idle
1	1	Idle

TABLE 2: Head Select

HS2	HS1	HS0	Head
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
HS0, HS1, HS2 †	I	Head Select: selects one of four heads
$\overline{CS}$	I	Chip Select: a high inhibits the chip
R/$\overline{W}$ †	I	Read/Write : a high selects Read mode
WUS †	O	Write Unsafe: a high indicates an unsafe writing condition
WDI †	I	Write Data In: changes the direction of the current in the recording head
H0X - H7X; H0Y - H7Y	I/O	X, Y Head Connections
RDX, RDY †	O	X, Y Read Data: differential read data output
WC †		Write Current: used to set the magnitude of the write current
WCADJ* †		Write Current Adjust: Used to decrease the write current by a finite amount
VCC1	I	+5V Supply
VCC2	I	+5V Supply for Write current drivers
GND	I	Ground

*Available on 32R4611A 24-pin option only

† These signals can be wire OR'ed

WRITE MODE

Taking both $\overline{CS}$ and R/$\overline{W}$ low selects write mode which configures the SSI 32R4610A/4611A as a current switch and activates the Write Unsafe (WUS) detector circuitry. Head current is toggled between the X and Y side of the selected head on each high to low transition of the Write Data Input (WDI). The WDI input pulse width requirement is amplitude dependent and pull ups are recommended at higher data rates, please refer to the WDI pulse width specifications. Note that a preceding read or idle mode select initializes the Write Data Flip-Flop to pass write current through the "X" side of the head. The magnitude of the write current (0-pk) is given by:

$$IW = \frac{K \cdot VWC}{RWC}$$

RWC is connected from pin WC to GND. Note the actual head current Ix, y is given by:

$$Ix, y = \frac{Iw}{1 + Rh/Rd}$$

Where:

Rh = Head resistance plus external wire resistance

Rd = Damping resistance

Any of the following conditions will be indicated as a high level on the Write Unsafe, WUS, open collector output.

- WDI frequency too low
- Device in Read mode
- Chip disabled
- No write current
- Head opened

After fault condition is removed, one negative transition on WDI is required to clear WUS.

The 32R4611A adds a feature which allows the user to adjust the Iw current by a finite amount. The WCADJ pin is used to adjust write current for write operations on different zones of the disk. It is used by switching a separate write current adjust resistor in and out on the WCADJ pin or by connecting a DAC to that pin to sink a controllable amount of current. The WCADJ pin is nominally biased to VCC/2. Sinking current from this pin to ground will divert a proportional amount of current from the actual head current while maintaining a constant current through the WC resistor and VCC. Allowing WCADJ to float or pulling it high will cut off the circuit and it will have no effect. For example, if the nominal head current is set to 30 mA through WC with WCADJ open, then for a 7.25 mA head current decrease, a 10 kΩ resistor would be connected from the WCADJ pin to ground. A TTL gate could be used as a switch with a small degradation in accuracy. To perform the same function, a DAC could be used, by programming it to sink 0.25 mA from the WCADJ pin.

Iw head (Decrease) = (29 • V_{WCADJ} / R_{WCADJ})

Where:

VWCADJ = Voltage on WCADJ pin = VCC/2

RWCADJ = Write current adjust setting resistor

VOLTAGE FAULT

A voltage Fault detection circuit improves data security by disabling the write current generator during a voltage fault or power startup regardless of mode.

READ MODE

The Read mode configures the SSI 32R4610A/4611A as a low noise differential amplifier and deactivates the write current generator. The RDX and RDY output are driven by emitter followers. They should be AC coupled to the load. The (X,Y) inputs are non-inverting to the (X,Y) outputs.

Note that in Idle or Write mode, the read amplifier is deactivated and RDX, RDY outputs become high impedance. This facilitates multiple R/W applications (wired-OR RDX, RDY) and minimizes voltage drifts when switching from Write to Read mode. Note also that the write current source is deactivated for both the Read and Idle mode.

IDLE MODE

Taking $\overline{CS}$ high selects the idle mode which switches the RDX and RDY outputs into a high impedance state and deactivates the device. Power consumption in this mode is held to a minimum.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may permanently damage the device.

PARAMETER		RATING	UNIT
DC Supply Voltage	VCC1	-0.3 to +7	VDC
	VCC2	-0.3 to +7	VDC
Write Current	IW	80	mA
Digital Input Voltage	Vin	-0.3 to VCC1 +0.3	VDC
Head Port Voltage	VH	-0.3 to VCC2 +0.3	VDC
Output Current: RDX, RDY	I0	-10	mA
WUS		+12	mA
Storage Temperature	Tstg	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

DC Supply Voltage	VCC1	5 ±10%	VDC
	VCC2	5 ±10%	VDC
Operating Junction Temperature	Tj	+25 to +110	°C

DC CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.

PARAMETER	CONDITIONS		MIN	NOM	MAX	UNIT
VCC1 Supply Current	Read Mode	(Vcc ±5%)	23	28	33	mA
		(Vcc ±10%)	19	28	37	mA
	Write Mode	(Vcc ±5%)	21	24	27	mA
		(Vcc ±10%)	17	24	31	mA
**Head Select Pins*	*Idle Mode	(Vcc ±5%)	6	9	12	mA
(HS0, HS1, HS2) Floating		(Vcc ±10%)	4	9	14	mA
VCC2 Supply Current	Read Mode	(Vcc ±5%)	5	8	11	mA
		(Vcc ±10%)	4	8	12	mA
	Write Mode	(Vcc ±5%)	6	8 + Iw	10 + Iw	mA
		(Vcc ±10%)	5	8 + Iw	11 + Iw	mA
	Idle Mode	(Vcc ±5%)	0.1	0.2	0.4	mA
		(Vcc ±10%)	0.1	0.2	0.5	mA
Power Dissipation	Read Mode	(Vcc ±5%)		175	230	mW
		(Vcc ±10%)			270	mW

DC CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS		MIN	NOM	MAX	UNIT
	Write Mode	(Vcc ±5%)		150 + 4Iw	190 + 4Iw	mW
		(Vcc ±10%)			230 + 4.4Iw	mW
	Idle Mode	(Vcc ±5%)		50	65	mW
		(Vcc ±10%)			80	mW
VCC1 Fault Voltage	IW < 0.2 mA		3.8	4.0	4.2	VDC

DIGITAL INPUTS

Input Low voltage (VIL)				0.8	VDC
Input High Voltage (VIH)		2.0			VDC
Input Low Current	VIL = 0.8V	-0.4			mA
Input High Current	VIH = 2.0V			100	µA
WUS Output Low Voltage (VOL)	Iol = 2 mA max			0.5	VDC

WRITE CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.

Write Current Constant "K"		.96	.99		
Write Current Voltage (VWC)		1.15	1.25	1.35	V
WCADJ Voltage SSI 32R4611A/4611AR	I_{WCADJ} = 0 to .5 mA	2.0	VCC/2	3.0	VDC
Ihead(Decrease)/I_{WCADJ} SSI 32R4611A/4611AR		26	29	32	mA/mA
I_{WCADJ} Range SSI 32R4611A/4611AR		0.0		0.5	mA
Differential Head Voltage Swing	Ih (p-p) • Rh not to exceed 3.4V (Head Swing Min)	3.4			Vpp
Unselected Head Current				0.02 Iw	mApk
Head Differential Load Capacitance				25	pF
Head Differential Load	SSI 32R4610A/32R4611A	4K			Ω
Resistance (Rd)	SSI 32R4610AR/32R4611AR	560	700	950	Ω
WDI Pulse Width	Vil = 0.2V, Vih = 2.4V PWH	37			ns
(Ref: Figure 1)	PWL	5			ns
	Vil = 0.2V, Vih = VCC PWH	20			ns
	PWL	5			ns
Write Current Range (IW)		10		35	mA

READ CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. CL (RDX, RDY) < 20 pF, RL (RDX, RDY) = 1 kΩ.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Differential Voltage Gain		Vin = 1 mVpp @1 MHz	160	200	240	V/V
Voltage BW	-1dB	|Zs| < 5Ω, Vin = 1 mVpp	20	81		MHz
	-3dB		35	91		MHz
Input Noise Voltage		BW = 15 MHz, Lh = 0, Rh = 0		0.6	0.85	nV/√Hz
Differential Input Capacitance		Vin = 1 mVpp, f = 5 MHz		27	35	pF
Differential Input Resistance		Vin = 1 mVpp, f = 5 MHz SSI 32R4610A/4611A	835	2600		Ω
		SSI 32R4610AR/4611AR	360	550		Ω
Dynamic Range		AC input voltage where gain falls to 90% of its small signal gain value, f = 5 MHz	3	6		mVpp
Common Mode Rejection Ratio		Vin = 0 VDC + 100 mVpp @ 5 MHz	45	80		dB
Power Supply Rejection Ratio		100 mVpp @ 5 MHz on VCC	40	70		dB
Channel Separation		Unselected channels driven with Vin = 0 VDC + 100 mVpp	45			dB
Output Offset Voltage			-300		+300	mV
Single Ended Output Resistance		f = 5 MHz			40	Ω
Output Current		AC coupled load, RDX to RDY	1.4			mA
RDX, RDY Common Mode Output Voltage			2.0	VCC1/2	3.5	VDC

SWITCHING CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. IW = 20 mA, Lh = 1.0 µH, Rh = 30Ω f(Data) = 5 MHz.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
R/$\overline{W}$	Read to Write	R/W to 90% of write current		0.1	1.0	µs
	Write to Read	R/W to 90% of 100 mV Read signal envelope		0.5	1.0	µs
$\overline{CS}$	Unselect to Select	$\overline{CS}$ to 90% of write current or to 90% of 100 mV 10 MHz		0.4	1.0	µs
	Select to Unselect	$\overline{CS}$ to 10% of write current		0.4	1.0	µs
HS0,1 to any Head		To 90% of 100 mV 10 MHz Read signal envelope		0.2	1.0	µs
WUS:	Safe to Unsafe (TD1)	Write mode, loss of WDI transitions. Defines maximum WDI period for WUS operation	0.6	2.0	3.6	µs
	Unsafe to Safe (TD2)	Fault cleared from first neg WDI transition		0.2	1.0	µs
Head Current:		Lh = 0, Rh = 0				
	WDI to Ix - Iy (TD3)	from 50% points		20	32	ns
	Asymmetry	WDI has 1 ns rise/fall time			1.0	ns
	Rise/fall Time	10% to 90% points		6	12	ns

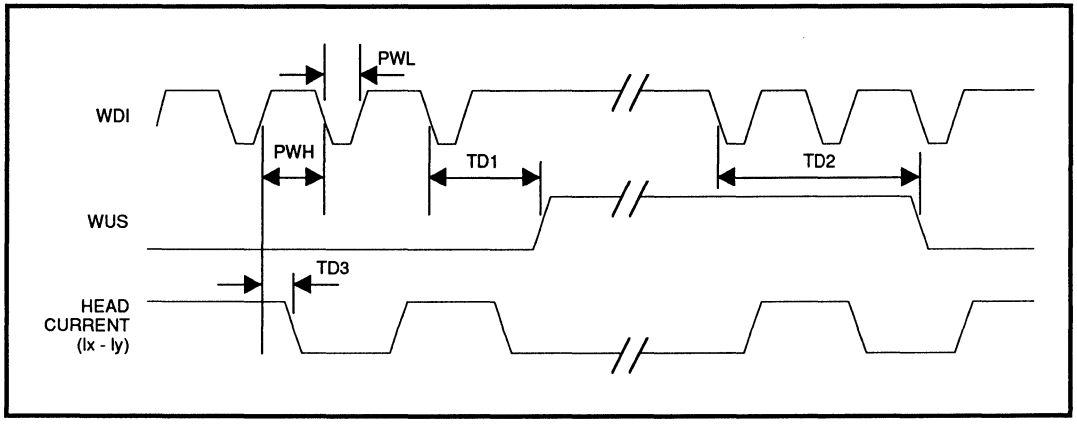


FIGURE 1: Write Mode Timing Diagram

Worst Case Read Input Noise Voltage vs. Input Impedance for SSI 32R4610AR/4611AR

Case 1: IC Base sheet resistance = Maximum
Hence, IC bias Current = Minimum

	Tj = 25°C	Tj = 110°C	Units
Vn (Max)	.7	0.85	$nV/\sqrt{Hz}$
Rin (Min)	450	475	Ω
Cin (Max)	28	30	pF

Case 2: IC Base sheet resistance = Minimum
Hence, IC bias Current = Maximum

	Tj = 25°C	Tj = 110°C	Units
Vn (Max)	.58	.65	$nV/\sqrt{Hz}$
Rin (Min)	360	400	Ω
Cin (Max)	33	35	pF

Worst Case Read Input Noise Voltage vs. Input Impedance for SSI 32R4610A/4611A

Case 1: IC Base sheet resistance = Maximum
Hence, IC bias Current = Minimum

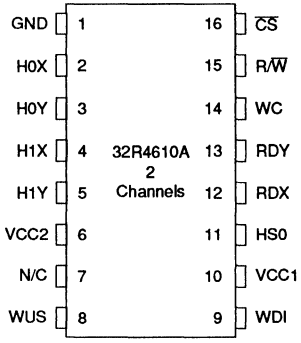
	Tj = 25°C	Tj = 110°C	Units
Vn (Max)	.7	0.85	$nV/\sqrt{Hz}$
Rin (Min)	1525	1895	Ω
Cin (Max)	28	30	pF

Case 2: IC Base sheet resistance = Minimum
Hence, IC bias Current = Maximum

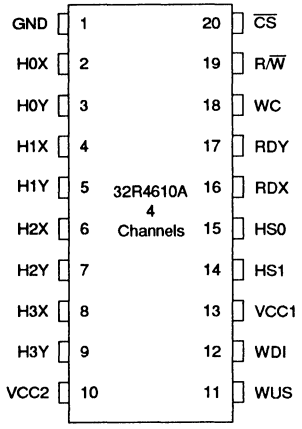
	Tj = 25°C	Tj = 110°C	Units
Vn (Max)	.58	.65	$nV/\sqrt{Hz}$
Rin (Min)	835	1100	Ω
Cin (Max)	33	35	pF

PACKAGE PIN DESIGNATIONS

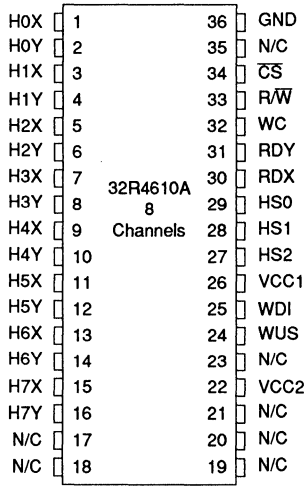
(Top View)



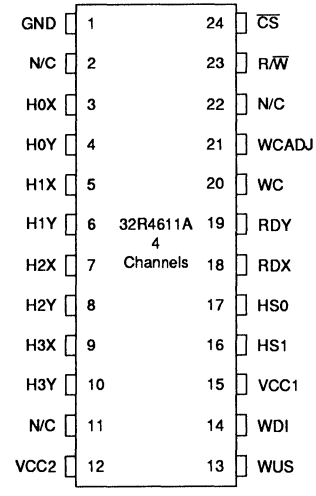
16-Pin SOL



20-Pin SOL, SOV



36-Pin SOM



24-Pin SOL, SOV

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do no use for final design.

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Notes:

Section 2

HDD PULSE DETECTION

silicon systems®
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SSI 32P541
Read Data Processor

February, 1990

2

DESCRIPTION

The SSI 32P541 is a bipolar integrated circuit that provides all data processing necessary for detection and qualification of MFM or RLL encoded read signals. The circuit will handle data rates up to 15 Mbit/s.

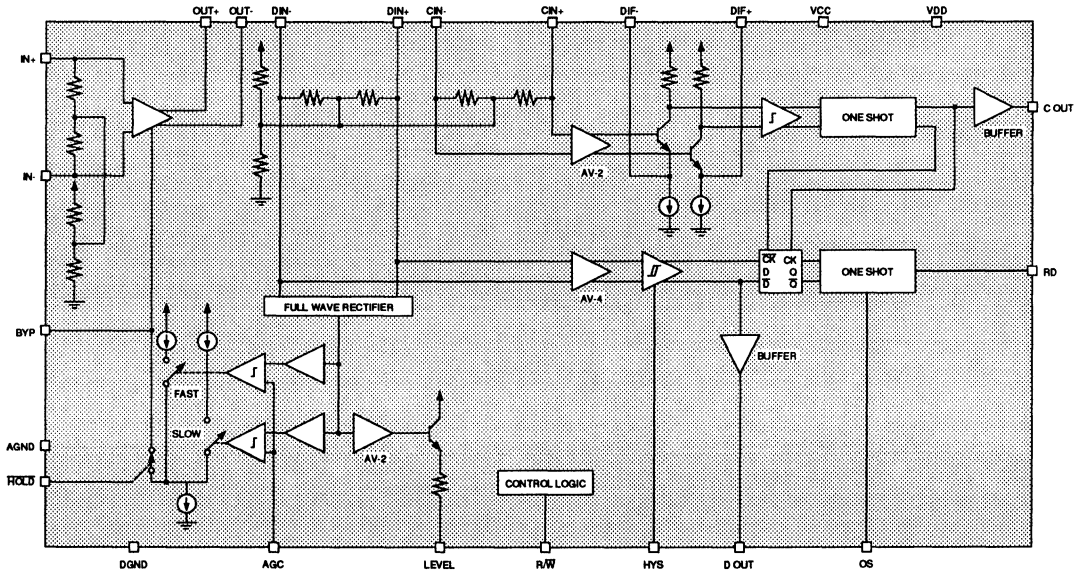
In read mode the SSI 32P541 provides amplification and qualification of head preamplifier outputs. Pulse qualification is accomplished using level qualification of differentiated input zero crossings. An AGC amplifier is used to compensate for variations in head preamp output levels, presenting a constant input level to the pulse qualification circuitry. The AGC loop can be disabled so that a constant gain can be used for embedded servo decoding or other processing needs.

In write mode the circuitry is disabled and the AGC gain stage input impedance is switched to a lower level to allow fast setting of the input coupling capacitors during a write to read transition. The SSI 32P541 requires +5V and +12V power supplies and is available in a 24–pin DIP and 28–pin PLCC.

FEATURES

- **Level qualification supports high resolution MFM and RLL encoded data retrieval**
- **Wide bandwidth AGC input amplifier**
- **Supports data rates up to 15 Mbit/s**
- **Standard 12V ± 10% and 5V ± 10% supplies**
- **Supports embedded servo pattern decoding**
- **Write to read transient suppression**
- **Fast and slow AGC attack regions for fast transient recovery**

BLOCK DIAGRAM



CIRCUIT OPERATION

READ MODE

In the read mode (R/$\overline{W}$ input high or open) the input read signal is amplified and qualified using an AGC amplifier and pulse level qualification of the detected signal peaks.

The amplified head signals are AC coupled to the IN + and IN - pins of the AGC amplifier that is gain controlled by full wave rectifying and amplifying the (DIN+ - DIN–) voltage level and comparing it to a reference level at the AGC pin. A fast attack mode, which supplies a 1.7 mA charging current for the capacitor at the BYP pin, is entered whenever the instantaneous DIN ± level is more than 125% of set level. Between 100% and 125% the slow attack mode is invoked, providing 0.18 mA of charging current. The two attack modes allow rapid AGC recovery from a write to read transition while reducing zero crossing distortion once the amplifier is in range.

The level at the AGC pin should be set such that the differential voltage level at the DIN+, DIN- pins is 1.00 Vpp at the OUT+, OUT- pins which allows for up to 6 dB loss in any external filter connected between the OUT+, OUT- outputs and the DIN+, DIN- inputs.

Gain of the AGC section is nominally

$$\frac{Av2}{Av1} = \exp - \left(\frac{V2 - V1}{5.8 + Vt} \right)$$

Where: Av1 and Av2 are initial and final amplifier gains. V1, V2 are initial and final voltages on the BYP pin.

Vt = (K x T)/q = 26 mV at room temperature.

One filter for both data (DIN+, DIN- input) and clock (CIN+, CIN- input) paths, or a separate filter for each path may be used. If two filters are used, care must be exercised to control time delays so that each path is timed properly. A multi-pole Bessell filter is typically used for its linear phase or constant group delay characteristics.

The filtered data path signal is fed into a hysteresis comparator that is set at a fraction of the input signal level by using an external filter/network between the LEVEL and HYS pins. Using this approach allows setting the AGC slow attack and decay times slow enough to minimize distortion of the clock path signal. This "feed-forward" technique, utilizing a fraction of the rectified data path input available at the LEVEL pin as the hysteresis threshold, is especially useful in the slow decay mode of the AGC loop. By using a short time constant for the hysteresis level, the qualification method can continue as the AGC amplifier gain is slowly ramped up. This level will also shorten the write to read transient recovery time without affecting data timing as the circuit will be properly decoding before the AGC gain has settled to its final value. The comparator output is the "D" input of a D type flip-flop. The DOUT pin provides a buffered test point for monitoring this function.

The filtered clock path signal is differentiated to transform signal peaks to zero-crossings which clock an edge-trigger circuit to provide output pulses at each zero-crossing. The pulses are used to clock the D type flip-flop. The COUT pin is a buffered test point for monitoring this function.

The differentiator function is set by an external network between the DIF+, DIF- pins. The transfer function is:

$$AV = \frac{-2000Cs}{LCs^2 + (R + 92)Cs + 1}$$

Where: C = external capacitor (20 pF to 150 pF)

L = external inductor

R = external resistor

$s = j\omega = j2\pi f$

During normal operation the differentiator circuit clocks the D flip-flop on every positive and negative peak of the signal input to CIN+, CIN-. The D input to the flip–flop only changes state when the signal applied to the DIN+, DIN- inputs exceeds the hysteresis comparator threshold opposite in polarity to the previous peak that exceeded the threshold.

The clocking path, then, determines signal timing and the data path determines validity by blocking signal peaks that do not exceed the hysteresis comparator threshold.

The delays from CIN+, CIN- inputs to the flip-flop clock input and from the DIN+, DIN- inputs to the flip-flop D input are well matched.

WRITE (DISABLED) MODE

In the write or disabled mode (R/$\overline{W}$ input low) the digital circuitry is disabled and the AGC amplifier input impedance is reduced. In addition the AGC amplifier, gain is set to maximum so that the loop is in its fast attack mode when changing back to Read Mode. The lowered input impedance facilitates more rapid settling of the write to read transient by reducing the time constant of the network between the SSI 32P541 and read/write preamplifier, such as the SSI 32R510.

Internal SSI 32P541 timing is such that this settling is accomplished before the AGC loop is activated when going to read mode. Coupling capacitors should be chosen with as low a value as possible, consistent with bandwidth requirements, to allow more rapid settling.

LAYOUT CONSIDERATIONS

The SSI 32P541 is a high gain wide bandwidth device that requires care in layout. The designer should keep analog signal lines as short as possible and well balanced. Use of a ground plane is recommended along with supply bypassing and separation of the SSI 32P541 and associated circuitry grounds from other circuits on the disk drive PCB.

R/$\overline{W}$	$\overline{HOLD}$	MODE
1	1	READ - Read amp on, AGC active, Digital section active
1	0	HOLD - Read amp on, AGC gain held constant Digital section active
0	X	WRITE - AGC gain switched to maximum, Digital section inactive, common mode input resistance reduced

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
VCC	-	5 volt power supply
VDD	-	12 volt power supply
AGND, DGND	-	Analog and Digital ground pins
R/$\overline{W}$	I	TTL compatible read/write control pin
IN+, IN-	I	Analog signal input pins
OUT+, OUT-	O	AGC Amplifier output pins
BYP	-	The AGC timing capacitor is tied between this pin and AGND
$\overline{HOLD}$	I	TTL compatible pin that holds the AGC gain when pulled low
AGC	I	Reference input voltage level for the AGC circuit
DIN+, DIN-	I	Analog input to the hysteresis comparator
HYS	I	Hysteresis level setting input to the hysteresis comparator
LEVEL	O	Provides rectified signal level for input to the hysteresis comparator
DOUT	O	Buffered test point for monitoring the flip-flop D input
CIN+, CIN-	I	Analog input to the differentiator
DIF+, DIF-	-	Pins for external differentiating network
COUT	O	Buffered test point for monitoring the clock input to the flip-flop
OS	-	Connection for read output pulse width setting capacitor
RD	O	TTL compatible read output

ELECTRICAL SPECIFICATIONS

Unless otherwise specified 4.5 ≤ VCC ≤ 5.5V, 10.8V ≤ VDD ≤ 13.2V, 25 °C ≤ Tj ≤ 135 °C.

ABSOLUTE MAXIMUM RATINGS

Operation above absolute maximum ratings may permanently damage the device.

PARAMETER	RATING	UNIT
5V Supply Voltage, VCC	6	V
12V Supply Voltage, VDD	14	V
Storage Temperature	-65 to 150	°C
Lead Temperature	260	°C
R/$\overline{W}$, IN+, IN-, $\overline{HOLD}$	-0.3 to VCC + 0.3	V
RD	-0.3V to VCC + 0.3V or +12	mA
All others	-0.3 to VDD + 0.3	V

POWER SUPPLY

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
ICC - VCC Supply Current	Outputs unloaded			14	mA
IDD - VDD Supply Current	Outputs unloaded			70	mA
Pd - Power Dissipation	Outputs unloaded, Tj = 135°C			730	mW

LOGIC SIGNALS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VIL - Input Low Voltage		-0.3		0.8	V
VIH - Input High Voltage		2.0			V
IIL - Input Low Current	VIL = 0.4V	0.0		-0.4	mA
IIH - Input High Current	VIH = 2.4V			100	µA
VOL - Output Low Voltage	IOL = 4.0 mA			0.4	V
VOH - Output High Voltage	IOH = -400 µA	2.4			V

MODE CONTROL

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Read to Write Transition Time				1.0	µs
Write to Read Transition Time	AGC settling not included, transition to high input resistance	1.2		3.0	µs
Read to Hold Transition Time				1.0	µs

WRITE MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Common Mode Input Impedance (both sides)	R/$\overline{W}$ pin = low		250		Ω

READ MODE

Unless otherwise specified IN+ and IN- are AC coupled, OUT+, and OUT- are loaded differentially with > 600Ω and each side is loaded with < 10 pF to GND, a 2000 pF capacitor is connected between BYP and GND, OUT+ is AC coupled to DIN+, OUT- is AC coupled to DIN-, AGC pin voltage is 2.2 VDC.

AGC AMPLIFIER

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Differential Input Resistance	V(IN+ – IN-) = 100 mVpp @ 2.5 MHz		5K		Ω
Differential Input Capacitance	V(IN+ – IN-) = 100 mVpp @ 2.5 MHz			10	pF
Common Mode Input Impedance	R/$\overline{W}$ pin high		1.8		kΩ
(both sides)	R/$\overline{W}$ pin low		0.25		kΩ
Minimum Gain Range	1.0 Vpp ≤ V(OUT+ – OUT-) ≤ 2.5 Vpp	4.0		83	V/V
Input Noise Voltage	Gain set to maximum			30	nV/√Hz
Bandwidth	Gain set to maximum -3 dB point	30			MHz
Maximum Output Voltage Swing	Set by AGC pin voltage	3.0			Vpp
Maximum AGC Amplifier Output Offset	Vout offset (max. gain) - Vout offset (min. gain) V_{BYP} = 2.5V to 4.5V			600	mV
OUT+ to OUT- Pin Current	No DC path to GND	±3.2			mA
Output Resistance		12		32	Ω
Output Capacitance				15	pF
(DIN+ – DIN-) Input Voltage Swing VS AGC Input Level	30 mVpp V(IN+ – IN-) ≤ 550 mVpp 0.5 Vpp ≤ V(DIN+ – DIN-) ≤ 1.5 Vpp	0.37		0.56	Vpp/V
(DIN+ – DIN-) Input Voltage Swing Variation	30 mVpp V(IN+ – IN-) ≤ 550 mVpp AGC Fixed, over supply & temperature			8	%
Gain Decay Time (Td)	Vin = 300 mVpp–> 150 mVpp @ 2.5 MHz, Vout to 90% of final value Figure 1a		50		µs
Gain Attack time (Ta)	From Write to Read transition to Vout at 110% of final value Vin = 400 mVpp @ 2.5 MHz. Figure 1b		4		µs

AGC AMPLIFIER (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Fast AGC Capacitor Charge Current	V(DIN+ - DIN-) = 1.6V V(AGC) = 2.2V	1.3		2.0	mA
Slow AGC Capacitor Charge Current	V(DIN+ – DIN-) = 1.6V Vary V(AGC) until slow discharge	0.14		0.22	mA
Fast to Slow Attack Switchover Point	$\frac{V(DIN+-DIN-)}{V(DIN+-DIN-)\ Final}$		1.25		
AGC Capacitor Discharge Current	V(DIN+ – DIN-) = 0.0V Read Mode		4.5		µA
	Hold Mode V_{BYP} = 5.0V	-0.2		+0.2	µA
	6.1V<V_{BYP}<8.1V	-0.45		+30	µA
CMRR (Input Referred)	V(IN+) = V(IN-) = 100 mVpp @ 5 MHz,gain at max.	40			dB
PSRR (Input Referred)	ΔVCC or ΔVDD = 100 mVpp @ 5 MHz, gain at max.	30			dB

HYSTERESIS COMPARATOR

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Input Signal Range				1.5	Vpp
Differential Input Resistance	V(DIN+ – DIN-) = 100 mVpp @ 2.5 MHz	5		11	kΩ
Differential Input Capacitance	V(DIN+ – DIN-) = 100 mVpp @ 2.5 MHz			6.0	pF
Common Mode Input Impedance	(both sides)		2.0		kΩ
Comparator Offset Voltage	HYS pin at GND, ≤ 1.5 kΩ across DIN+, DIN-			10	mV
Peak Hysteresis Voltage vs. HYS pin voltage (input referred)	At DIN+, DIN- pins 1V < V (HYS) < 3V	0.16		0.25	V/V
HYS Pin Input Current	1V < V (HYS) < 3V	0.0		-20	µA
Level Pin Output Voltage vs V(DIN+ – DIN-)	0.6 < | V (DIN+ – DIN-) | <1.3 Vpp, 10 kΩ from LEVEL pin to GND	1.5		2.5	V/Vpp
LEVEL Pin Max Output Current		3.0			mA
LEVEL Pin Output Resistance	I(LEVEL) = 0.5 mA		180		Ω
DOUT Pin Output Low Voltage	0.0 ≤ IOL ≤ 0.5 mA	VDD -4.0		VDD -2.8	V
DOUT Pin Output High Voltage	0.0 ≤ IOH ≤ 0.5 mA	VDD -2.5		VDD -1.8	V

ACTIVE DIFFERENTIATOR

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Input Signal Range				1.5	Vpp
Differential Input Resistance	V(CIN+ – CIN-) = 100 mVpp @ 2.5 MHz	5.8		11.0	kΩ
Differential Input Capacitance	V(CIN+ – CIN-) = 100 mVpp @ 2.5 MHz			6.0	pF
Common mode Input Impedance	(both sides)		2.0		kΩ
Voltage Gain From CIN± to DIF±	R(DIF+ to DIF-) = 2 kΩ	1.7		2.2	V/V
DIF+ to DIF- Pin Current	Differentiator Impedance must be set so as not to clip signal at this current level	±1.3			mA
Comparator Offset Voltage	DIF+, DIF- are AC Coupled			10.0	mV
COUT Pin Output Low Voltage	0.0 ≤ IOH ≤ 0.5 mA		VDD -3.0		V
COUT Pin Output Pulse voltage V(high) - V(low)	0.0 ≤ IOH ≤ 0.5 mA		+0.4		V
COUT Pin Output Pulse Width	0.0 ≤ IOH ≤ 0.5 mA		30		ns

OUTPUT DATA CHARACTERISTICS (See Figure 2)
Unless otherwise specified V(CIN+ – CIN-) = V(DIN+ – DIN-) = 1.0 Vpp AC coupled since wave at 2.5 MHz differentiating network between DIF+ and DIF- is 100Ω in series with 65 pF, V (Hys) = 1.8 DC, a 60 pF capacitor is connected between OS and VCC, RD- is loaded with a 4 kΩ resistor to VCC and a 10 pF capacitor to GND.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
D-Flip-Flop Set Up Time (Td1)	Min delay from V(DIN+ DIN-) exceeding threshold to V(DIF+ – DIF-) reaching a peak	0			ns
Propagation Delay (Td3)				110	ns
Output Data Pulse Width Variation	Td5 = 670 Cos, 50 pF ≤ Cos ≤ 200 pF			±15	. %
Pulse Pairing	Td3 - Td4			3	ns
Output Rise Time	VOH = 2.4V			14	ns
Output Fall Time	VOL = 0.4V			18	ns

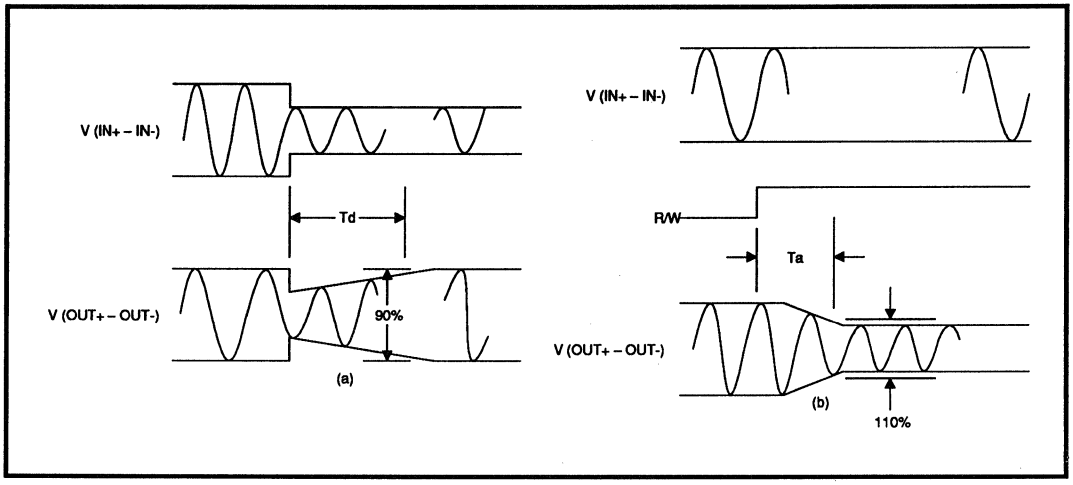


FIGURE 1(a), (b): AGC Timing Diagrams

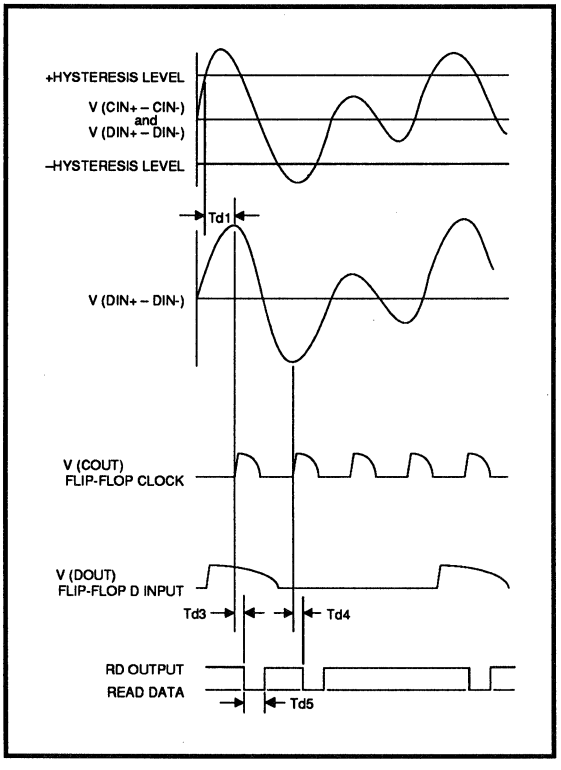
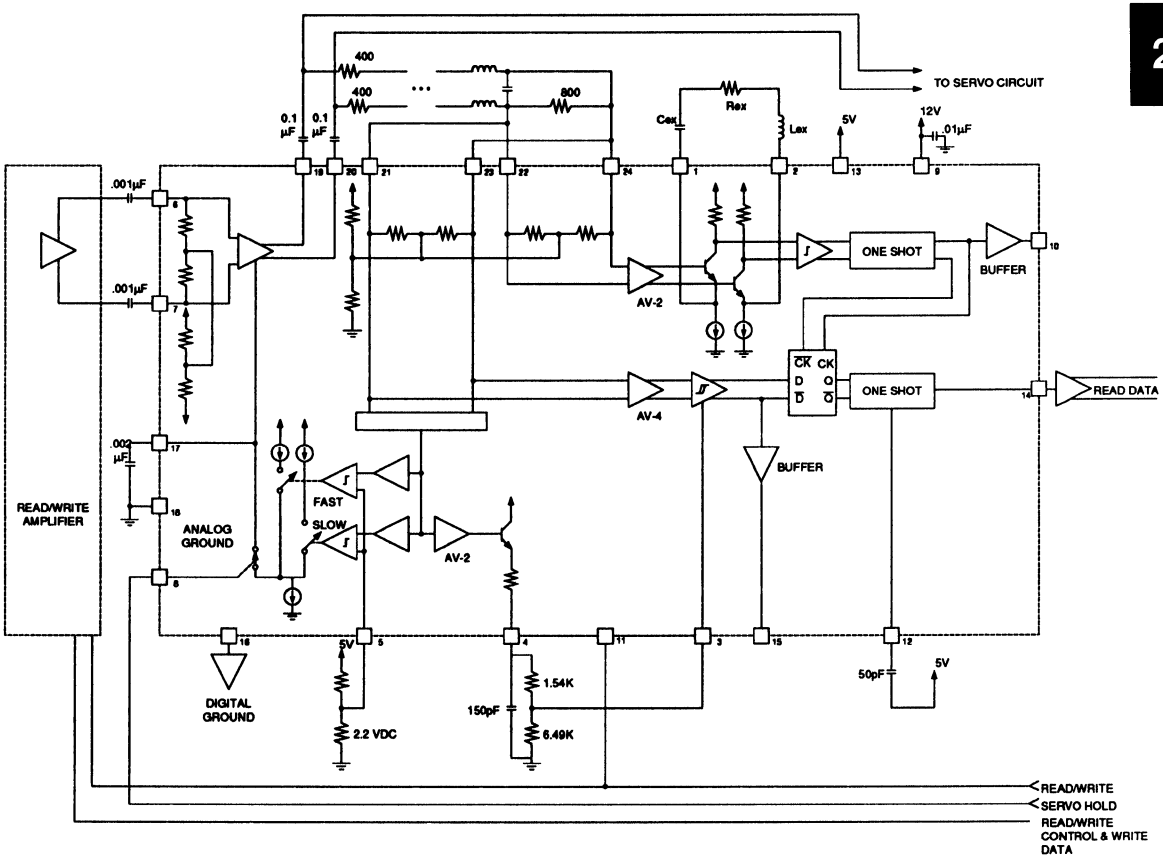


FIGURE 2: Timing Diagram



NOTES: Circuit traces for the 12V bypass capacitor and the AGC Hold Capacitor should be as short as possible with both capacitors returned to the Analog Ground Pin.

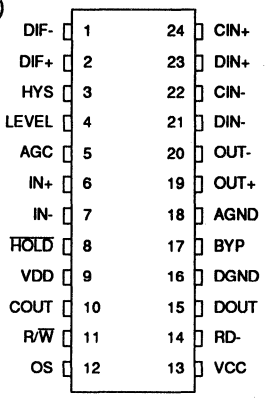
Component values, where given, are for a 5 Mbit/s system.

FIGURE 3: Typical Read/Write Electronics Set Up

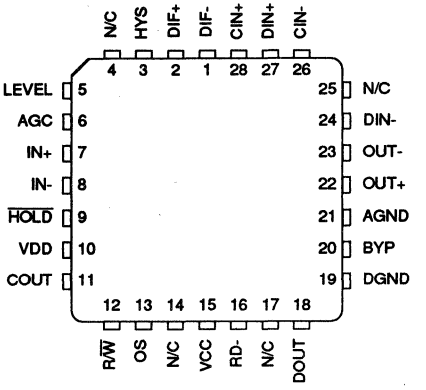
SSI 32P541
Read Data Processor

PACKAGE PIN DESIGNATIONS

(Top View)



24-Lead PDIP, SOL



28-Lead PLCC

THERMAL CHARACTERISTICS: Ø ja

24-Lead PDIP	115°C/W
24-Lead SOL	80°C/W
28-Lead PLCC	65°C/W

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION	ORDERING NUMBER	PACKAGE MARK
SSI 32P541 Read Data Processor		
24-Lead PDIP	32P541-P	32P541-P
28-Lead PLCC	32P541-CH	32P541-CH
24-Lead SOL	32P541-CL	32P541-CL

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714) 731-7110, FAX: (714) 573-6914

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SSI 32P541B
Read Data Processor

July 1991

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DESCRIPTION

The SSI 32P541B is a bipolar integrated circuit that provides all data processing necessary for detection and qualification of MFM or RLL encoded read signals.

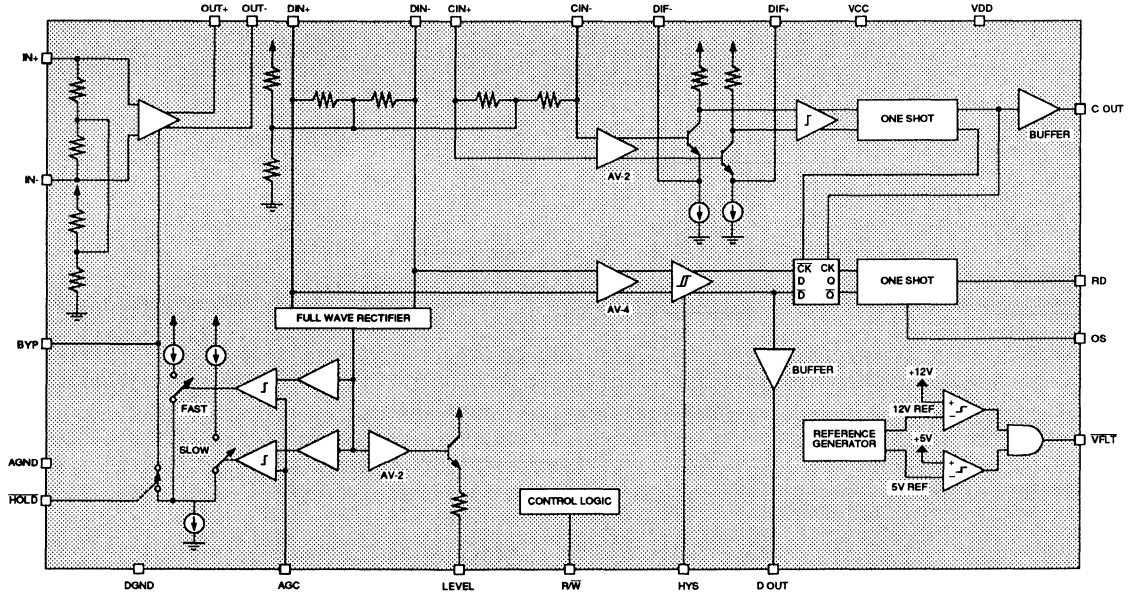
In read mode the SSI 32P541B provides amplification and qualification of head preamplifier outputs. Pulse qualification is accomplished using level qualification of differentiated input zero crossings. An AGC amplifier is used to compensate for variations in head preamp output levels, presenting a constant input level to the pulse qualification circuitry. The AGC loop can be disabled so that a constant gain can be used for embedded servo decoding or other processing needs.

In write mode the circuitry is disabled and the AGC gain stage input impedance is switched to a lower level to allow fast settling of the input coupling capacitors during a write to read transition. The SSI 32P541B requires +5V and +12V power supplies and is available in a 28-pin PLCC, 24-pin DIP and 24-pin SOL.

FEATURES

- **Level qualification supports high resolution MFM and RLL encoded data retrieval**
- **Wide bandwidth AGC input amplifier**
- **Standard 12V ± 10% and 5V ± 10% supplies**
- **Supports embedded servo pattern decoding**
- **Write to read transient suppression**
- **Fast and slow AGC attack regions for fast transient recovery**
- **Internal voltage fault indicator**
- **≤ ±1.0 ns pulse pairing**
- **24 Mb/s operation**

BLOCK DIAGRAM



CIRCUIT OPERATION

READ MODE

In the read mode (R/$\overline{W}$ input high or open) the input read signal is amplified and qualified using an AGC amplifier and pulse level qualification of the detected signal peaks.

The amplified head signals are AC coupled to the IN + and IN - pins of the AGC amplifier that is gain controlled by full wave rectifying and amplifying the (DIN+ - DIN–) voltage level and comparing it to a reference level at the AGC pin. A fast attack mode, which supplies a 1.7 mA charging current for the capacitor at the BYP pin, is entered whenever the instantaneous DIN ± level is more than 125% of set level. Between 100% and 125% the slow attack mode is invoked, providing 0.18 mA of charging current. The two attack modes allow rapid AGC recovery from a write to read transition while reducing zero crossing distortion once the amplifier is in range.

The level at the AGC pin should be set such that the differential voltage level at the DIN+, DIN- pins is 1.00 Vpp at the OUT+, OUT- pins which allows for up to 6 dB loss in any external filter connected between the OUT+, OUT- outputs and the DIN+, DIN- inputs.

Gain of the AGC section is nominally

$$\frac{Av2}{Av1} = \exp -\left(\frac{V2 - V1}{5.8 + Vt}\right)$$

Where: Av1 and Av2 are initial and final amplifier gains. V1, V2 are initial and final voltages on the BYP pin.

Vt = (K x T)/q = 26 mV at room temperature.

One filter for both data (DIN+, DIN- input) and clock (CIN+, CIN- input) paths, or a separate filter for each path may be used. If two filters are used, care must be exercised to control time delays so that each path is timed properly. A multi-pole Bessell filter is typically used for its linear phase or constant group delay characteristics.

HYSTERESIS LEVEL

In level qualification, hysteresis comparator eliminates errors due to low level additive noise, see Figure 4B.

The 32P541B allows two implementations of hysteresis: fixed hysteresis threshold or DIN tracking hysteresis threshold. Fixed hysteresis threshold can be simply done by a setting a DC voltage at HYS pin, such as from a resistor divider from VCC to GND. The hysteresis threshold at the comparator can be computed as: Hysteresis Gain x V_{HYS}. For high performance system application, however, fixed hysteresis threshold is not recommended.

DIN tracking hysteresis has the advantages of shorter write-to-read recovery time and lower probability of error with input amplitude drop out. The hysteresis threshold is designed as a percentage of the DIN peak voltage. This technique can be implemented by feeding the LEVEL output, through a resistor divider network, to the HYS pin (see Figure 4b). The LEVEL output, amplified peak capture of DIN voltage, can be computed as: Level Gain x V(DIN+ - DIN-). With the resistor divider, a fraction of the LEVEL output is presented at the HYS pin. The hysteresis threshold, as a function of DIN, can be summarized as: Level Gain x Resistor Dividing Ratio x Hysteresis Gain x V(DIN+ - DIN-). For a typical case of 1 Vpp differential at DIN± input, assume equal value resistors in the divider network, the hysteresis threshold is 1.95 x 0.50 x 0.19 x 1V = 0.185V. This represents 37% hysteresis on a 1 Vpp signal. While both the Level Gain and Hysteresis threshold vs. HYS bear a moderate tolerance due to typical process variations, they inversely track each other to yield a much tighter hysteresis threshold in a closed loop. In designing the hysteresis threshold, the nominal Level Gain and Hysteresis Gain values should be used. The tolerance on DIN tracking hysteresis threshold is specified as the Tracking Hysteresis Threshold Tolerance in the specification.

While the external resistor divider ratio determines the hysteresis threshold, the total resistance and the peak capture capacitor should be optimized for the system data rate. The RC time constant must be small enough to allow good response to changing DIN± peak-to-peak, but large enough to provide a constant hysteresis threshold in each level qualification.

The filtered clock path signal is differentiated to transform signal peaks to zero-crossings which clock an edge-trigger circuit to provide output pulses at each zero-crossing. The pulses are used to clock the D-type flip-flop. The COUT pin is a buffered test point for monitoring this function.

The differentiator function is set by an external network between the DIF+, DIF- pins. The transfer function is:

Where: C = external capacitor (20 pF to 150 pF)

$$AV = \frac{-2000Cs}{LCs^2 + (R+92)Cs + 1}$$

L = external inductor

R = external resistor

$s = j\omega = j2\pi f$

During normal operation the differentiator circuit clocks the D flip-flop on every positive and negative peak of the signal input to CIN+, CIN-. The D input to the flip–flop only changes state when the signal applied to the DIN+, DIN- inputs exceeds the hysteresis comparator threshold opposite in polarity to the previous peak that exceeded the threshold.

The clocking path, then, determines signal timing and the data path determines validity by blocking signal peaks that do not exceed the hysteresis comparator threshold.

The delays from CIN+, CIN- inputs to the flip-flop clock input and from the DIN+, DIN- inputs to the flip-flop D input are well matched.

WRITE (DISABLED) MODE

In the write or disabled mode (R/$\overline{W}$ input low) the digital circuitry is disabled and the AGC amplifier input impedance is reduced. In addition the AGC amplifier, gain is set to maximum so that the loop is in its fast attack mode when changing back to Read Mode. The lowered input impedance facilitates more rapid settling of the write to read transient by reducing the time constant of the network between the SSI 32P541B and read/write preamplifier, such as the SSI 32R512.

Internal SSI 32P541B timing is such that this settling is accomplished before the AGC loop is activated when going to read mode. Coupling capacitors should be chosen with as low a value as possible, consistent with bandwidth requirements, to allow more rapid settling.

LAYOUT CONSIDERATIONS

The SSI 32P541B is a high gain wide bandwidth device that requires care in layout. The designer should keep analog signal lines as short as possible and well balanced. Use of a ground plane is recommended along with supply bypassing and separation of the SSI 32P541B and associated circuitry grounds from other circuits on the disk drive PCB.

LOW VOLTAGE FAULT DETECTION

A low voltage detection dircuit monitors both supplies and pulls an open collector TTL output low when either supply drops below their trip point. This option is available only in the 28-pin PLCC package.

TABLE 1: Mode Control

R/$\overline{W}$	$\overline{HOLD}$	MODE
1	1	READ - Read amp on, AGC active, Digital section active
1	0	HOLD - Read amp on, AGC gain held constant Digital section active
0	X	WRITE - AGC gain switched to maximum, Digital section inactive, common mode input resistance reduced

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
VCC		5 volt power supply
VDD		12 volt power supply
AGND, DGND		Analog and Digital ground pins
R/$\overline{W}$	I	TTL compatible read/write control pin
IN+, IN-	I	Analog signal input pins
OUT+, OUT-	O	AGC Amplifier output pins
BYP		The AGC timing capacitor is tied between this pin and AGND
$\overline{HOLD}$	I	TTL compatible pin that holds the AGC gain when pulled low
AGC	I	Reference input voltage level for the AGC circuit
DIN+, DIN-	I	Analog input to the hysteresis comparator
HYS	I	Hysteresis level setting input to the hysteresis comparator
LEVEL	O	Provides rectified signal level for input to the hysteresis comparator
DOUT	O	Buffered test point for monitoring the flip-flop D input
CIN+, CIN-	I	Analog input to the differentiator
DIF+, DIF-		Pins for external differentiating network
COUT	O	Buffered test point for monitoring the clock input to the flip-flop
OS		Connection for read output pulse width setting capacitor
RD	O	TTL compatible read output
$\overline{VFLT}$*	O	Open collector output that goes low when a low power supply fault is detected.

*$\overline{VFLT}$ output offered in 28-pin PLCC package only.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified 4.5 ≤ VCC ≤ 5.5V, 10.8V ≤ VDD ≤ 13.2V, 25 °C ≤ Tj ≤ 135 °C.

ABSOLUTE MAXIMUM RATINGS

Operation above absolute maximum ratings may permanently damage the device.

PARAMETER	RATING	UNIT
5V Supply Voltage, VCC	6	V
12V Supply Voltage, VDD	14	V
Storage Temperature	-65 to 150	°C
Lead Temperature	260	°C
R/$\overline{W}$, IN+, IN-, $\overline{HOLD}$, $\overline{VFLT}$	-0.3 to VCC + 0.3	V
RD	-0.3V to VCC + 0.3V or +12	mA
All others	-0.3 to VDD + 0.3	V

POWER SUPPLY

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
ICC - VCC Supply Current	Outputs unloaded			14	mA
IDD - VDD Supply Current	Outputs unloaded			70	mA
Pd - Power Dissipation	Outputs unloaded, Tj = 135°C			850	mW

LOGIC SIGNALS

VIL - Input Low Voltage		-0.3		0.8	V
VIH - Input High Voltage		2.0			V
IIL - Input Low Current	VIL = 0.4V	0.0		-0.4	mA
IIH - Input High Current	VIH = 2.4V			100	µA
VOL - Output Low Voltage	IOL = 4.0 mA			0.4	V
VOH - Output High Voltage	IOH = -400 µA	2.4			V

MODE CONTROL

Read to Write Transition Time				1.0	µs
Write to Read Transition Time	AGC settling not included, transition to high input resistance	1.2		3.0	µs
Read to Hold Transition Time				1.0	µs

WRITE MODE

Common Mode Input Impedance (both sides)	R/$\overline{W}$ pin = low		250		Ω

READ MODE

Unless otherwise specified IN+ and IN- are AC coupled, OUT+, and OUT- are loaded differentially with > 600Ω and each side is loaded with < 10 pF to GND, a 2000 pF capacitor is connected between BYP and GND, OUT+ is AC coupled to DIN+, OUT- is AC coupled to DIN-, AGC pin voltage is 2.2 VDC.

AGC AMPLIFIER

Differential Input Resistance	V(IN+ – IN-) = 100 mVpp @ 2.5 MHz		5K		Ω
Differential Input Capacitance	V(IN+ – IN-) = 100 mVpp @ 2.5 MHz			10	pF
Common Mode Input Impedance	R/$\overline{W}$ pin high		1.8		kΩ
(both sides)	R/$\overline{W}$ pin low		0.25		kΩ
Minimum Gain Range	1.0 Vpp ≤ V(OUT+ – OUT-) ≤ 2.5 Vpp	4.0		83	V/V
Input Noise Voltage	Gain set to maximum			30	nV/$\sqrt{Hz}$

AGC AMPLIFIER (Continued)

PARAMETER	CONDITIONS		MIN	NOM	MAX	UNIT
Bandwidth	Gain set to maximum -3 dB point		30			MHz
Maximum Output Voltage Swing	Set by AGC pin voltage		3.0			Vpp
OUT+ to OUT- Pin Current	No DC path to GND		±3.2			mA
Output Resistance			12		32	Ω
Output Capacitance					15	pF
(DIN+ – DIN-) Input Voltage Swing VS AGC Input Level	30 mVpp ≤ V(IN+ – IN-) ≤ 550 mVpp;	@ 2.5 MHz	0.33		0.43	Vpp/V
		@ 9 MHz	0.44		0.69	Vpp/V
	0.5 Vpp ≤ V(DIN+ – DIN-) ≤ 1.5 Vpp					
(DIN+ – DIN-) Input Voltage Swing Variation	30 mVpp V(IN+ – IN-) ≤ 550 mVpp AGC Fixed, over supply & temp.	@ 2.5 MHz			4	%
		@ 9 MHz			12	%
		@ 9 MHz Cold			14	%
Gain Decay Time (Td)	Vin = 300 mVpp–> 150 mVpp at 2.5 MHz, Vout to 90% of final value Figure 1a			50		µs
Gain Attack time (Ta)	From Write to Read transition to Vout at 110% of final value Vin = 400 mVpp @ 2.5 MHz. Figure 1b			4		µs
Fast AGC Capacitor Charge Current	V(DIN+ - DIN-) = 1.6V V(AGC) = 2.2V		1.3		2.0	mA
Slow AGC Capacitor Charge Current	V(DIN+ – DIN-) = 1.6V Vary V(AGC) until slow discharge		0.14		0.22	mA
Fast to Slow Attack Switchover Point	$\frac{V(DIN+-DIN-)}{V(DIN+-DIN-)\ Final}$			1.25		
AGC Capacitor Discharge Current	V(DIN+ – DIN-) = 0.0V Read Mode			4.5		µA
	Hold Mode		-0.2		+0.2	µA
CMRR (Input Referred)	V(IN+) = V(IN-) = 100 mVpp @ 5 MHz,gain at max.		40			dB
PSRR (Input Referred)	ΔVCC or ΔVDD = 100 mVpp @ 5 MHz, gain at max.		30			dB
Maximum AGC Amplifier Output Offset Variation	V(IN+ - IN-) = 0 Min to max gain				200	mV

HYSTERESIS COMPARATOR

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Input Signal Range				1.5	Vpp
Differential Input Resistance	V(DIN+ – DIN-) = 100 mVpp @ 2.5 MHz	5		11	kΩ
Differential Input Capacitance	V(DIN+ – DIN-) = 100 mVpp @ 2.5 MHz			6.0	pF
Common Mode Input Impedance	(both sides)		2.0		kΩ
Comparator Offset Voltage	HYS pin at GND, ≤ 1.5 kΩ across DIN+, DIN-			10	mV
Hysteresis Gain (see figure 4c)	At DIN+, DIN- pins 1V < V (HYS) < 3V	0.16	0.19	0.22	V/V
HYS Pin Input Current	1V < V (HYS) < 3V	0.0		-20	µA
Tracking Hysteresis Threshold Tolerance	V (Hys) = some % of *V (AGC) or V (LEVEL) 1V < V (Hys) < 3V; f = 0-9 MHz	-15		+15	% Peak
Level Gain (see figure 4d)	0.6 < | V (DIN+ – DIN-) | <1.3 Vpp, 10 kΩ from LEVEL pin to GND	1.7	1.95	2.2	V/Vpp
LEVEL Pin Max Output Current		3.0			mA
LEVEL Pin Output Resistance	I(LEVEL) = 0.5 mA		180		Ω
DOUT Pin Output Low Voltage	0.0 ≤ IOL ≤ 0.5 mA	VDD -4.0		VDD -2.8	V
DOUT Pin Output High Voltage	0.0 ≤ IOH ≤ 0.5 mA	VDD -2.5		VDD -1.8	V

*In an open loop configuration where reference is V(AGC) tolerance can be slightly higher

ACTIVE DIFFERENTIATOR

Input Signal Range				1.5	Vpp
Differential Input Resistance	V(CIN+ – CIN-) = 100 mVpp @ 2.5 MHz	5.8		11.0	kΩ
Differential Input Capacitance	V(CIN+ – CIN-) = 100 mVpp @ 2.5 MHz			6.0	pF
Common mode Input Impedance	(both sides)		2.0		kΩ
Voltage Gain From CIN± to DIF±	R(DIF+ to DIF-) = 2 kΩ	1.7		2.2	V/V
DIF+ to DIF- Pin Current	Differentiator Impedance must be set so as not to clip signal at this current level	±1.3			mA
Comparator Offset Voltage	DIF+, DIF- are AC Coupled			10.0	mV
COUT Pin Output Low Voltage	0.0 ≤ IOH ≤ 0.5 mA		VDD -3.0		V
COUT Pin Output Pulse voltage V(high) - V(low)	0.0 ≤ IOH ≤ 0.5 mA		+0.4		V
COUT Pin Output Pulse Width	0.0 ≤ IOH ≤ 0.5 mA		30		ns

OUTPUT DATA CHARACTERISTICS (See Figure 2)
Unless otherwise specified V(CIN+ – CIN-) = V(DIN+ – DIN-) = 1.0 Vpp AC coupled sine wave at 2.5 MHz differentiating network between DIF+ and DIF- is 100Ω in series with 65 pF, V (Hys) = 1.8 DC, a 33 pF capacitor is connected between OS and VCC, RD- is loaded with a 4 kΩ resistor to VCC and a 10 pF capacitor to GND.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
D-Flip-Flop Set Up Time (Td1)	Min delay from V(DIN+ DIN-) exceeding threshold to V(DIF+ – DIF-) reaching a peak	0			ns
Propagation Delay (Td3)				110	ns
Output Data Pulse Width Variation	Td5 = 11.4 ns + 740 • Cos 50% - 50% 15 pF ≤ Cos ≤ 150 pF			±15	%
Pulse Pairing	|Td3 - Td4|			±1.0	ns
Output Rise Time	From 0.4V to 2.4V level			15	ns
Output Fall Time	From 0.4V to 2.4V level			9	ns

SUPPLY VOLTAGE FAULT DETECTION

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VDD Fault Threshold		9.1		10.3	V
VCC Fault Threshold		4.1		4.4	V
VOL Output Low Voltage	4.5 < VCC < 5.5V, IOL = 1.6 mA			0.4	V
	1.0 < VCC < 4.5V, IOL = 0.5 mA			0.4	V
IOH Output High Current				25	µA

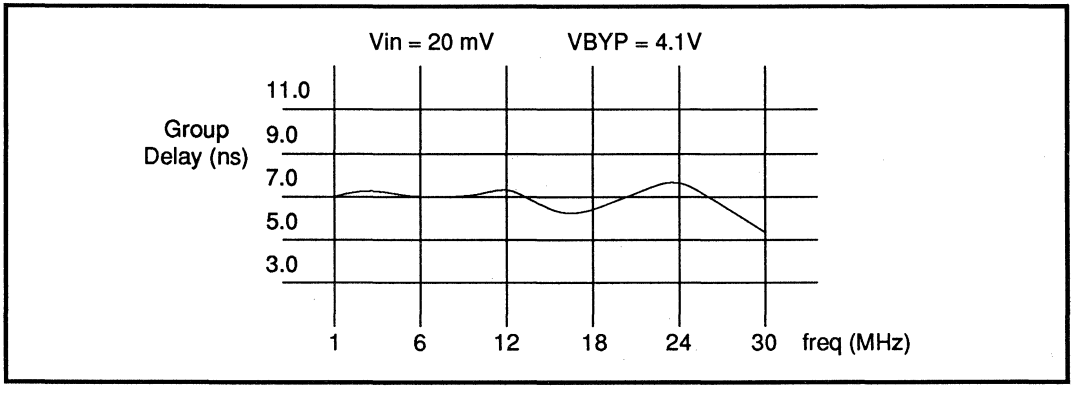


FIGURE 1: AGC Amplifier - Typical Group Delay Variation

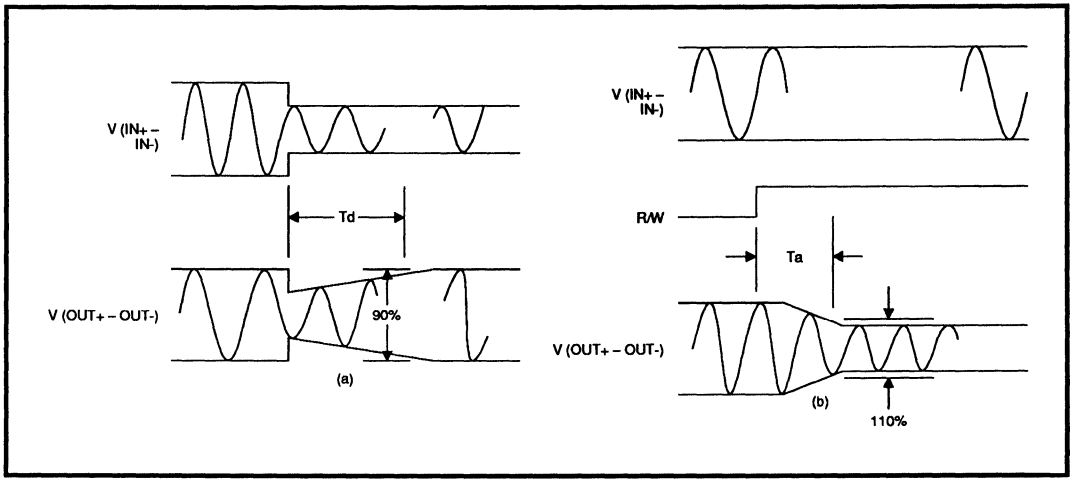


FIGURE 1(a), (b): AGC Timing Diagrams

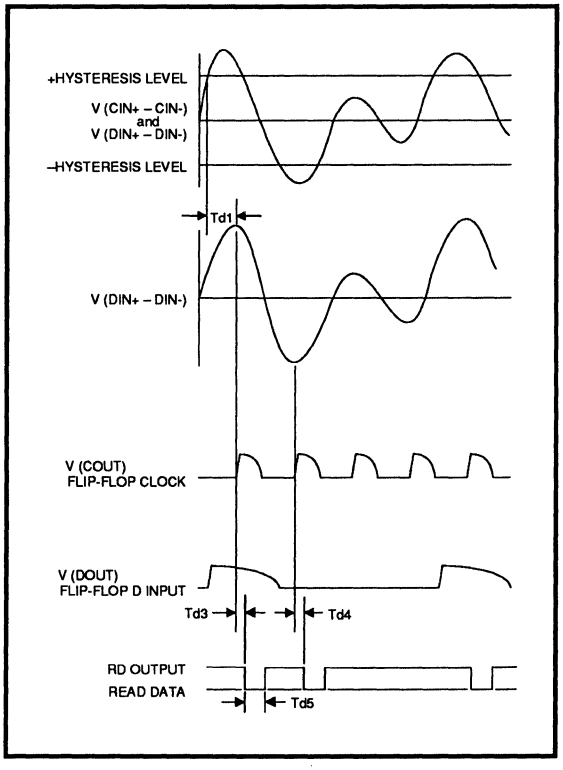
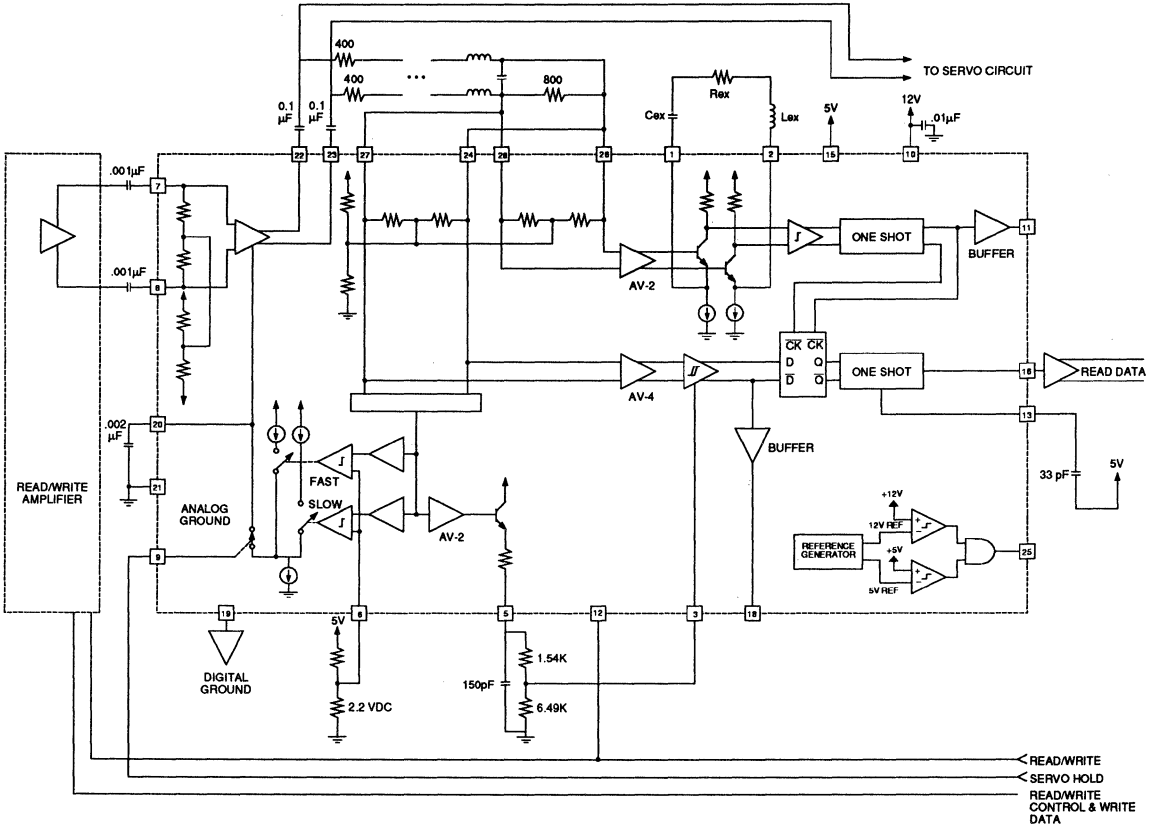


FIGURE 2: Timing Diagram



NOTE: Circuit traces for the 12V bypass capacitor and the AGC Hold Capacitor should be as short as possible with both capacitors returned to the Analog Ground Pin.
Component values, where given, are for a 24 Mbit/s System.
Above pin numbers are for the 28-pin PLCC package.

FIGURE 3: Typical Read/Write Electronics Set Up

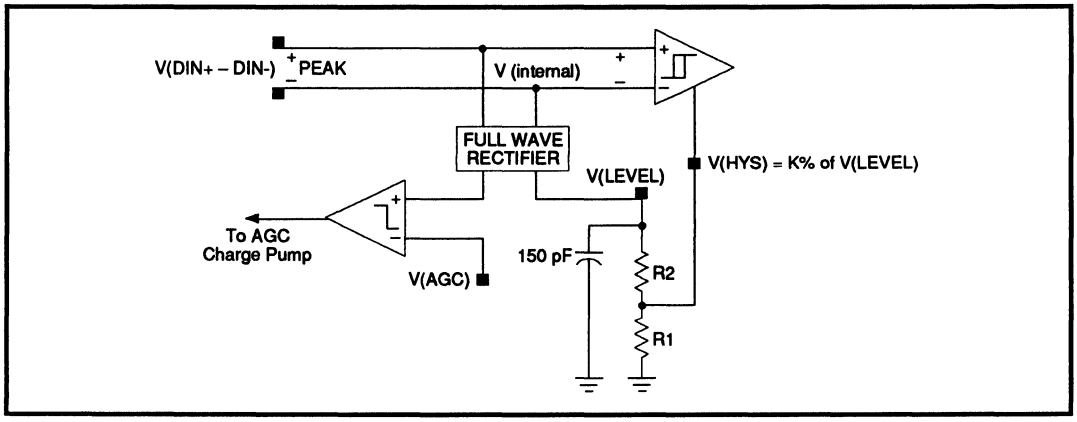


FIGURE 4a: Feed Forward Mode

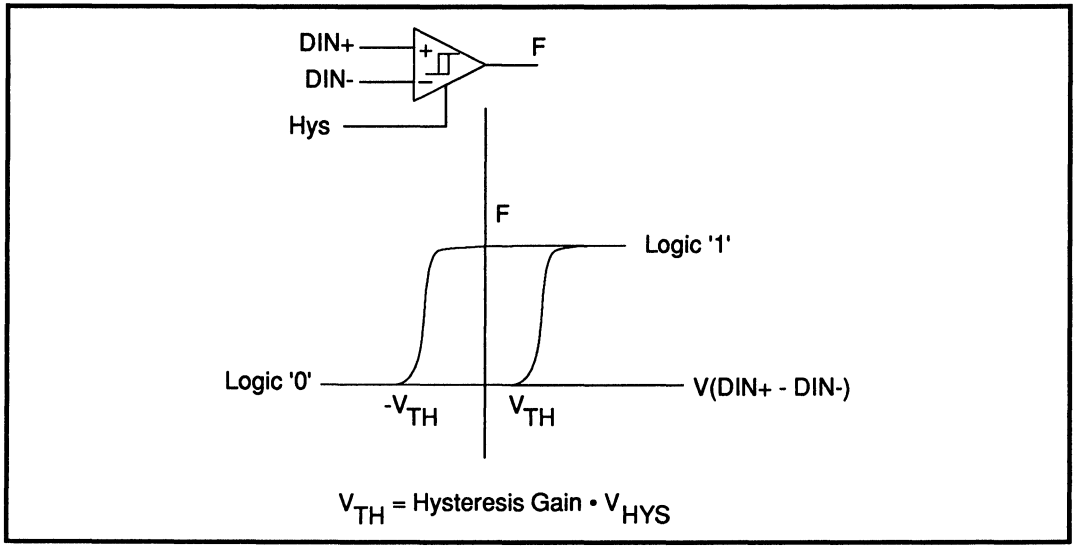


FIGURE 4b: Hysteresis Comparator Transfer Function

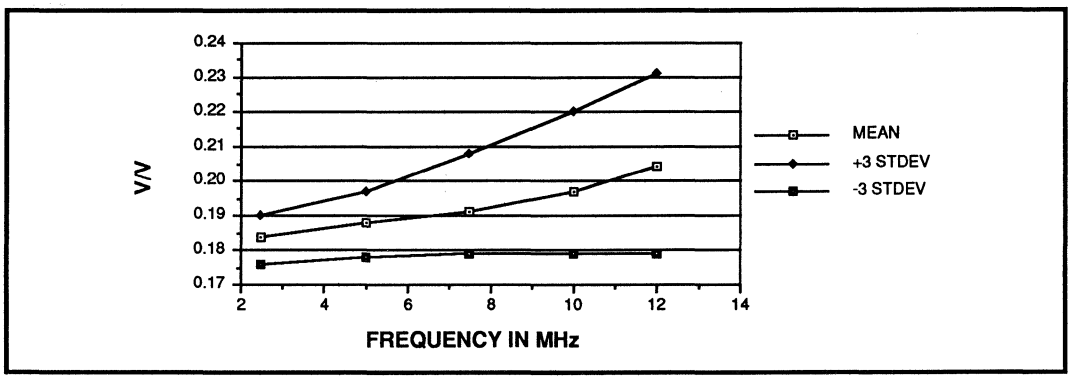


FIGURE 4c: Hysteresis Gain

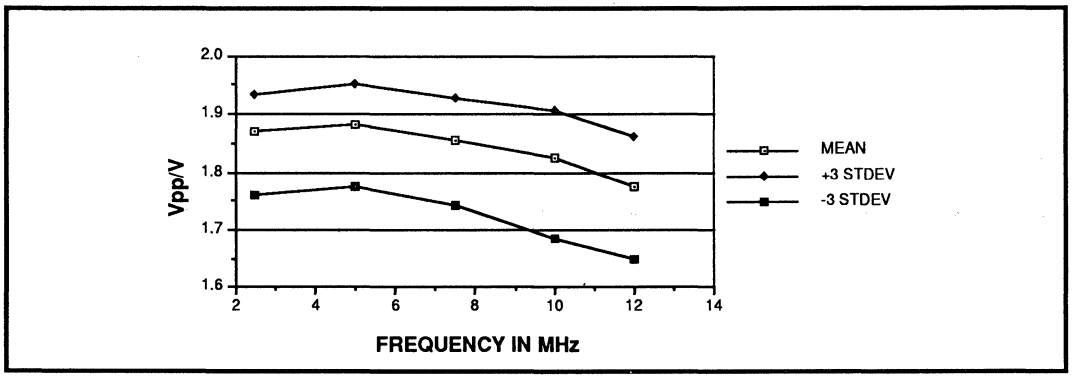


FIGURE 4d: Level Gain

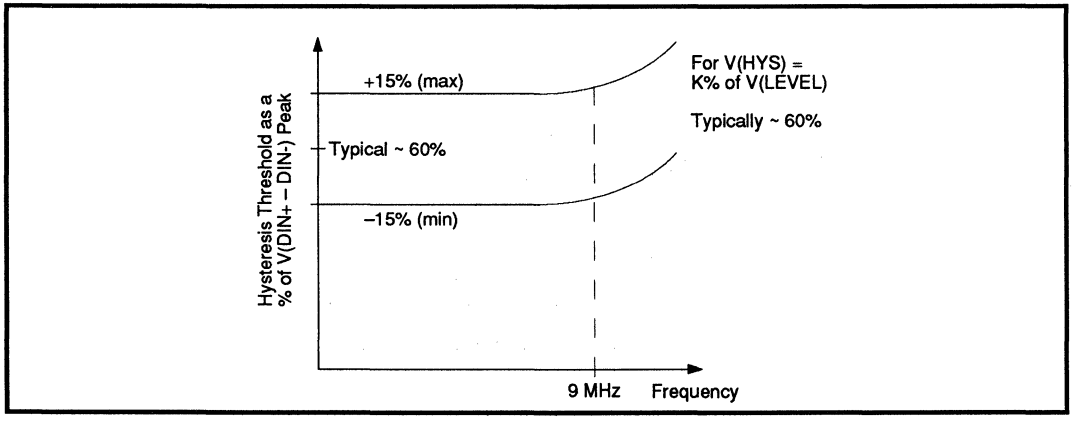
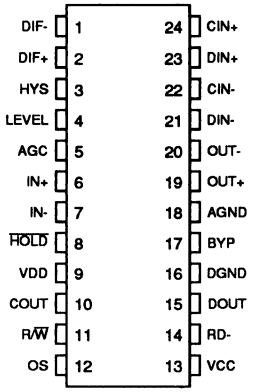


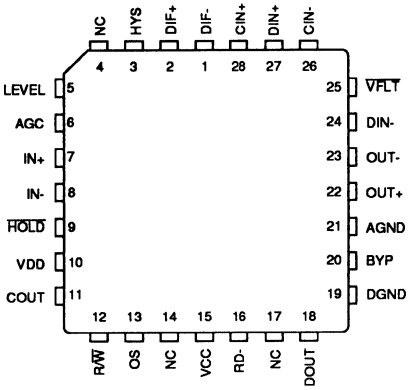
FIGURE 5: Percentage Threshold Versus Frequency

PACKAGE PIN DESIGNATIONS

(TOP VIEW)



24-Lead PDIP, SOL



28-Lead PLCC

THERMAL CHARACTERISTICS: Ø ja

24-Lead PDIP	115°C/W
24-Lead SOL	80°C/W
28-Lead PLCC	65°C/W

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION	ORDERING NUMBER	PACKAGE MARK
SSI 32P541B Read Data Processor		
24-Lead PDIP	SSI 32P541B-P	SSI 32P541B-P
28-Lead PLCC	SSI 32P541B-CH	SSI 32P541B-CH
24-Lead SOL	SSI 32P541B-CL	SSI 32P541B-CL

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 731-7110, FAX (714) 573-6914

Notes:

silicon systems®
A TDK Group Company

SSI 32P5411B
Read Data Processor

Advance Information

December 1991

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DESCRIPTION

The SSI 32P5411B is a bipolar integrated circuit that provides all data processing necessary for detection and qualification of MFM or RLL encoded read signals.

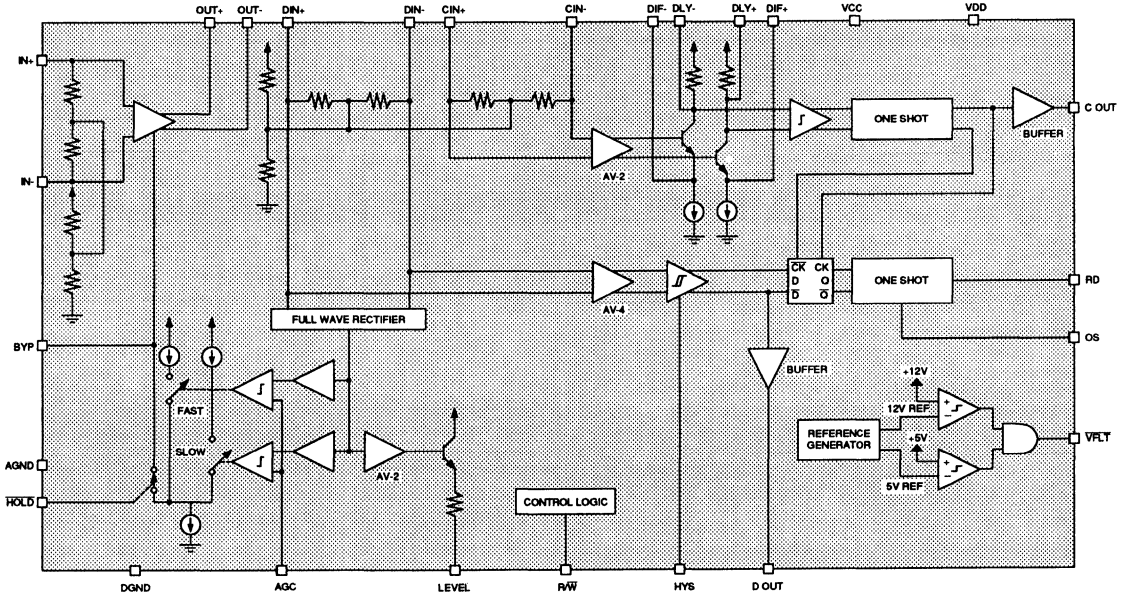
In read mode the SSI 32P5411B provides amplification and qualification of head preamplifier outputs. Pulse qualification is accomplished using level qualification of differentiated input zero crossings. An AGC amplifier is used to compensate for variations in head preamp output levels, presenting a constant input level to the pulse qualification circuitry. The AGC loop can be disabled so that a constant gain can be used for embedded servo decoding or other processing needs. When an external clock signal is provided for time qualification, the signal timing is user selectable.

In write mode the circuitry is disabled and the AGC gain stage input impedance is switched to a lower level to allow fast settling of the input coupling capacitors during a write to read transition. The SSI 32P5411B requires +5V and +12V power supplies and is available in a 28-pin PLCC package.

FEATURES

- **Level qualification supports high resolution MFM and RLL encoded data retrieval**
- **Wide bandwidth AGC input amplifier**
- **Standard 12V ± 10% and 5V ± 10% supplies**
- **Supports embedded servo pattern decoding**
- **Write to read transient suppression**
- **Fast and slow AGC attack regions for fast transient recovery**
- **User selectable data - to-clock timing**
- **Internal voltage fault indicator**
- **≤ ±1.0 ns pulse pairing**
- **24 Mb/s operation**

BLOCK DIAGRAM



CIRCUIT OPERATION

READ MODE

In the read mode (R/$\overline{W}$ input high or open) the input read signal is amplified and qualified using an AGC amplifier and pulse level qualification of the detected signal peaks.

The amplified head signals are AC coupled to the IN + and IN - pins of the AGC amplifier that is gain controlled by full wave rectifying and amplifying the (DIN+ - DIN-) voltage level and comparing it to a reference level at the AGC pin. A fast attack mode, which supplies a 1.7 mA charging current for the capacitor at the BYP pin, is entered whenever the instantaneous DIN ± level is more than 125% of set level. Between 100% and 125% the slow attack mode is invoked, providing 0.18 mA of charging current. The two attack modes allow rapid AGC recovery from a write to read transition while reducing zero crossing distortion once the amplifier is in range.

The level at the AGC pin should be set such that the differential voltage level at the DIN+, DIN- pins is 1.00 Vpp at the OUT+, OUT- pins which allows for up to 6 dB loss in any external filter connected between the OUT+, OUT- outputs and the DIN+, DIN- inputs.

Gain of the AGC section is nominally

$$\frac{Av2}{Av1} = \exp -\left(\frac{V2 - V1}{5.8 + Vt}\right)$$

Where: Av1 and Av2 are initial and final amplifier gains. V1, V2 are initial and final voltages on the BYP pin.

Vt = (K x T)/q = 26 mV at room temperature.

One filter for both data (DIN+, DIN- input) and clock (CIN+, CIN- input) paths, or a separate filter for each path may be used. If two filters are used, care must be exercised to control time delays so that each path is timed properly. A multi-pole Bessell filter is typically used for its linear phase or constant group delay characteristics.

HYSTERESIS LEVEL

In level qualification, hysteresis comparator eliminates errors due to low level additive noise, see Figure 4B.

The 32P5411B allows two implementations of hysteresis: fixed hysteresis threshold or DIN tracking hysteresis threshold. Fixed hysteresis threshold can be simply done by a setting a DC voltage at HYS pin, such as from a resistor divider from VCC to GND. The hysteresis threshold at the comparator can be computed as: Hysteresis Gain x V_{HYS}. For high performance system application, however, fixed hysteresis threshold is not recommended.

DIN tracking hysteresis has the advantages of shorter write-to-read recovery time and lower probability of error with input amplitude drop out. The hysteresis threshold is designed as a percentage of the DIN peak voltage. This technique can be implemented by feeding the LEVEL output, through a resistor divider network, to the HYS pin (see Figure 5b). The LEVEL output, amplified peak capture of DIN voltage, can be computed as: Level Gain x V(DIN+ - DIN-). With the resistor divider, a fraction of the LEVEL output is presented at the HYS pin. The hysteresis threshold, as a function of DIN, can be summarized as: Level Gain x Resistor Dividing Ratio x Hysteresis Gain x V(DIN+ - DIN-). For a typical case of 1 Vpp differential at DIN± input, assume equal value resistors in the divider network, the hysteresis threshold is 1.95 x 0.50 x 0.19 x 1V = 0.185V. This represents 37% hysteresis on a 1 Vpp signal. While both the Level Gain and Hysteresis threshold vs. HYS bear a moderate tolerance due to typical process variations, they inversely track each other to yield a much tighter hysteresis threshold in a closed loop. In designing the hysteresis threshold, the nominal Level Gain and Hysteresis Gain values should be used. The tolerance on DIN tracking hysteresis threshold is specified as the Tracking Hysteresis Threshold Tolerance in the specification.

While the external resistor divider ratio determines the hysteresis threshold, the total resistance and the peak capture capacitor should be optimized for the system data rate. The RC time constant must be small enough to allow good response to changing DIN± peak-to-peak, but large enough to provide a constant hysteresis threshold in each level qualification.

CLOCK SIGNAL PATH

In time qualification, the filtered clock path is to locate the peak of each read data pulse. By taking the time differentiation of the filtered read data pulse, each peak is transformed into zero crossing. Each zero crossing of this time differentiated signal clocks an edge-trigger

circuit to provide output pulses. These output pulses are used to clock the D-type flip-flop. The COUT pin is a buffered test point for monitoring this function.

The time differentiation can be achieved by one of two ways: (1) using the on-chip differentiator circuit, or (2) using external time differentiation function, such as that from the SSi programmable filters.

The on-chip differentiation function is set by an external network between the DIF± pins. The DLY± pins should be left open. The CIN+ should be connected to the DIN+; the CIN- should be connected to DIN-. The transfer function from the CIN± pins to the internal differentiator outputs, which are at the input of the edge triggered one-shot, is:

$$AV = \frac{-2000\ Cs}{LCs^2 + (R+92)\ Cs + 1}$$

where C = external capacitor (20 pF to 150 pF)
L = external inductor
R = external resistor
$s = jw = j\ 2\ \pi\ f$

CLOCK DELAY

When the time differentiation is provided by an external circuit, then the differentiated signal should be applied to the CIN±, separate from the read data signal at the DIN±. To optimize the timing at the D-flip-flop, the user has the flexibility to adjust the clock path delay with an external capacitor setting. Figure 4 illustrates the connections for this application. While C1, C2 and R1 are for DC offset block, to improve pulse pairing performance, Cdelay determines the time delay from CIN± to the clock input of the D-type flip-flop. The delay is given as (3.7 ns / 10 pF) x Cdelay [pF]. The delay will not increase beyond 0.25 / Fclock max. Do not exceed the max Cdelay value of:

$$\text{Cdelay max} = \frac{0.25 / \text{Fclock max.}}{3.7\ \text{ns}} \times 10\ \text{pF}$$

WRITE (DISABLED) MODE

In the write or disabled mode (R/$\overline{W}$ input low) the digital circuitry is disabled and the AGC amplifier input impedance is reduced. In addition the AGC amplifier, gain is set to maximum so that the loop is in its fast attack mode when changing back to Read Mode. The lowered input impedance facilitates more rapid settling of the write to read transient by reducing the time constant of the network between the SSI 32P5411B and read/write preamplifier, such as the SSI 32R512.

Internal SSI 32P5411B timing is such that this settling is accomplished before the AGC loop is activated when going to read mode. Coupling capacitors should be chosen with as low a value as possible, consistent with bandwidth requirements, to allow more rapid settling.

LAYOUT CONSIDERATIONS

The SSI 32P5411B is a high gain wide bandwidth device that requires care in layout. The designer should keep analog signal lines as short as possible and well balanced. Use of a ground plane is recommended along with supply bypassing and separation of the SSI 32P5411B and associated circuitry grounds from other circuits on the disk drive PCB.

LOW VOLTAGE FAULT DETECTION

A low voltage detection circuit monitors both supplies and pulls an open collector TTL output low when either supply drops below their trip point. This option is available only in the 28-pin PLCC package.

TABLE 1: Mode Control

R/$\overline{W}$	$\overline{HOLD}$	MODE
1	1	READ - Read amp on, AGC active, Digital section active
1	0	HOLD - Read amp on, AGC gain held constant Digital section active
0	X	WRITE - AGC gain switched to maximum, Digital section inactive, common mode input resistance reduced

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
VCC		5 volt power supply
VDD		12 volt power supply
AGND, DGND		Analog and Digital ground pins
R/$\overline{W}$	I	TTL compatible read/write control pin
IN+, IN-	I	Analog signal input pins
OUT+, OUT-	O	AGC Amplifier output pins
BYP		The AGC timing capacitor is tied between this pin and AGND
$\overline{HOLD}$	I	TTL compatible pin that holds the AGC gain when pulled low
AGC	I	Reference input voltage level for the AGC circuit
DIN+, DIN-	I	Analog input to the hysteresis comparator
HYS	I	Hysteresis level setting input to the hysteresis comparator
LEVEL	O	Provides rectified signal level for input to the hysteresis comparator
DOUT	O	Buffered test point for monitoring the flip-flop D input
CIN+, CIN-	I	Analog input to the differentiator
DIF+, DIF-		Pins for external differentiating network
COUT	O	Buffered test point for monitoring the clock input to the flip-flop
OS		Connection for read output pulse width setting capacitor
RD	O	TTL compatible read output
$\overline{VFLT}$*	O	Open collector output that goes low when a low power supply fault is detected.

*$\overline{VFLT}$ output offered in 28-pin PLCC package only.

ELECTRICAL SPECIFICATIONS

Unless otherwise specified 4.5 ≤ VCC ≤ 5.5V, 10.8V ≤ VDD ≤ 13.2V, 25 °C ≤ Tj ≤ 135 °C.

ABSOLUTE MAXIMUM RATINGS

Operation above absolute maximum ratings may permanently damage the device.

PARAMETER	RATING	UNIT
5V Supply Voltage, VCC	6	V
12V Supply Voltage, VDD	14	V
Storage Temperature	-65 to 150	°C
Lead Temperature	260	°C
R/$\overline{W}$, IN+, IN-, $\overline{HOLD}$, $\overline{VFLT}$	-0.3 to VCC + 0.3	V
RD	-0.3V to VCC + 0.3V or +12	mA
All others	-0.3 to VDD + 0.3	V

POWER SUPPLY

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
ICC - VCC Supply Current	Outputs unloaded			14	mA
IDD - VDD Supply Current	Outputs unloaded			70	mA
Pd - Power Dissipation	Outputs unloaded, Tj = 135°C			850	mW

LOGIC SIGNALS

VIL - Input Low Voltage		-0.3		0.8	V
VIH - Input High Voltage		2.0			V
IIL - Input Low Current	VIL = 0.4V	0.0		-0.4	mA
IIH - Input High Current	VIH = 2.4V			100	µA
VOL - Output Low Voltage	IOL = 4.0 mA			0.4	V
VOH - Output High Voltage	IOH = -400 µA	2.4			V

MODE CONTROL

Read to Write Transition Time				1.0	µs
Write to Read Transition Time	AGC settling not included, transition to high input resistance	1.2		3.0	µs
Read to Hold Transition Time				1.0	µs

WRITE MODE

Common Mode Input Impedance (both sides)	R/$\overline{W}$ pin = low		250		Ω

READ MODE

Unless otherwise specified IN+ and IN- are AC coupled, OUT+, and OUT- are loaded differentially with > 600Ω and each side is loaded with < 10 pF to GND, a 2000 pF capacitor is connected between BYP and GND, OUT+ is AC coupled to DIN+, OUT- is AC coupled to DIN-, AGC pin voltage is 2.2 VDC.

AGC AMPLIFIER

Differential Input Resistance	V(IN+ – IN-) = 100 mVpp @ 2.5 MHz		5K		Ω
Differential Input Capacitance	V(IN+ – IN-) = 100 mVpp @ 2.5 MHz			10	pF
Common Mode Input Impedance	R/$\overline{W}$ pin high		1.8		kΩ
(both sides)	R/$\overline{W}$ pin low		0.25		kΩ
Minimum Gain Range	1.0 Vpp ≤ V(OUT+ – OUT-) ≤ 2.5 Vpp	4.0		83	V/V
Input Noise Voltage	Gain set to maximum			30	nV/$\sqrt{Hz}$

AGC AMPLIFIER (Continued)

PARAMETER	CONDITIONS		MIN	NOM	MAX	UNIT
Bandwidth	Gain set to maximum -3 dB point		30			MHz
Maximum Output Voltage Swing	Set by AGC pin voltage		3.0			Vpp
OUT+ to OUT- Pin Current	No DC path to GND		±3.2			mA
Output Resistance			12		32	Ω
Output Capacitance					15	pF
(DIN+ – DIN-) Input Voltage Swing VS AGC Input Level	30 mVpp ≤ V(IN+ – IN-)	@ 2.5 MHz	0.33		0.43	Vpp/V
	≤ 550 mVpp;	@ 9 MHz	0.44		0.69	Vpp/V
	0.5 Vpp ≤ V(DIN+ – DIN-) ≤ 1.5 Vpp					
(DIN+ – DIN-) Input Voltage Swing Variation	30 mVpp V(IN+ – IN-)	@ 2.5 MHz			4	%
	≤ 550 mVpp AGC Fixed,	@ 9 MHz			12	%
	over supply & temp.	@ 9 MHz Cold			14	%
Gain Decay Time (Td)	Vin = 300 mVpp–> 150 mVpp at 2.5 MHz, Vout to 90% of final value Figure 1a			50		µs
Gain Attack time (Ta)	From Write to Read transition to Vout at 110% of final value Vin = 400 mVpp @ 2.5 MHz. Figure 1b			4		µs
Fast AGC Capacitor Charge Current	V(DIN+ - DIN-) = 1.6V V(AGC) = 2.2V		1.3		2.0	mA
Slow AGC Capacitor Charge Current	V(DIN+ – DIN-) = 1.6V Vary V(AGC) until slow discharge		0.14		0.22	mA
Fast to Slow Attack Switchover Point	$\frac{V(DIN+-DIN-)}{V(DIN+-DIN-)\ Final}$			1.25		
AGC Capacitor Discharge Current	V(DIN+ – DIN-) = 0.0V Read Mode			4.5		µA
	Hold Mode		-0.2		+0.2	µA
CMRR (Input Referred)	V(IN+) = V(IN-) = 100 mVpp @ 5 MHz,gain at max.		40			dB
PSRR (Input Referred)	ΔVCC or ΔVDD = 100 mVpp @ 5 MHz, gain at max.		30			dB
Maximum AGC Amplifier Output Offset Variation	V(IN+ - IN-) = 0 Min to max gain				200	mV

HYSTERESIS COMPARATOR

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Input Signal Range				1.5	Vpp
Differential Input Resistance	V(DIN+ – DIN-) = 100 mVpp @ 2.5 MHz	5		11	kΩ
Differential Input Capacitance	V(DIN+ – DIN-) = 100 mVpp @ 2.5 MHz			6.0	pF
Common Mode Input Impedance	(both sides)		2.0		kΩ
Comparator Offset Voltage	HYS pin at GND, ≤ 1.5 kΩ across DIN+, DIN-			10	mV
Hysteresis Gain (see figure 5c)	At DIN+, DIN- pins 1V < V (HYS) < 3V	0.16	0.19	0.22	V/V
HYS Pin Input Current	1V < V (HYS) < 3V	0.0		-20	µA
Tracking Hysteresis Threshold Tolerance	V (Hys) = some % of *V (AGC) or V (LEVEL) 1V < V (Hys) < 3V; f = 0-9 MHz	-15		+15	% Peak
Level Gain (see figure 5d)	0.6 < | V (DIN+ – DIN-) | <1.3 Vpp, 10 kΩ from LEVEL pin to GND	1.7	1.95	2.2	V/Vpp
LEVEL Pin Max Output Current		3.0			mA
LEVEL Pin Output Resistance	I(LEVEL) = 0.5 mA		180		Ω
DOUT Pin Output Low Voltage	0.0 ≤ IOL ≤ 0.5 mA	VDD -4.0		VDD -2.8	V
DOUT Pin Output High Voltage	0.0 ≤ IOH ≤ 0.5 mA	VDD -2.5		VDD -1.8	V

*In an open loop configuration where reference is V(AGC) tolerance can be slightly higher

ACTIVE DIFFERENTIATOR

Input Signal Range				1.5	Vpp
Differential Input Resistance	V(CIN+ – CIN-) = 100 mVpp @ 2.5 MHz	5.8		11.0	kΩ
Differential Input Capacitance	V(CIN+ – CIN-) = 100 mVpp @ 2.5 MHz			6.0	pF
Common mode Input Impedance	(both sides)		2.0		kΩ
Voltage Gain From CIN± to DIF±	R(DIF+ to DIF-) = 2 kΩ	1.7		2.2	V/V
DIF+ to DIF- Pin Current	Differentiator Impedance must be set so as not to clip signal at this current level	±1.3			mA
Comparator Offset Voltage	DIF+, DIF- are AC Coupled			10.0	mV
COUT Pin Output Low Voltage	0.0 ≤ IOH ≤ 0.5 mA		VDD -3.0		V
COUT Pin Output Pulse voltage V(high) - V(low)	0.0 ≤ IOH ≤ 0.5 mA		+0.4		V
COUT Pin Output Pulse Width	0.0 ≤ IOH ≤ 0.5 mA		30		ns
Delay Function	RI = 100 kΩ, CI = 7 C2 = 2.2 µF Cdelay (pF) Figure 4	Delay = 3.7 x Cdelay			ns

OUTPUT DATA CHARACTERISTICS (See Figure 2)
Unless otherwise specified V(CIN+ – CIN-) = V(DIN+ – DIN-) = 1.0 Vpp AC coupled sine wave at 2.5 MHz differentiating network between DIF+ and DIF- is 100Ω in series with 65 pF, V (Hys) = 1.8 DC, a 33 pF capacitor is connected between OS and VCC, RD- is loaded with a 4 kΩ resistor to VCC and a 10 pF capacitor to GND.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
D-Flip-Flop Set Up Time (Td1)	Min delay from V(DIN+ DIN-) exceeding threshold to V(DIF+ – DIF-) reaching a peak	0			ns
Propagation Delay (Td3)				110	ns
Output Data Pulse Width Variation	Td5 = 11.4 ns + 740 • Cos 50% - 50% 15 pF ≤ Cos ≤ 150 pF			±15	%
Pulse Pairing	|Td3 - Td4|			±1.0	ns
Output Rise Time	From 0.4V to 2.4V level			15	ns
Output Fall Time	From 0.4V to 2.4V level			9	ns

SUPPLY VOLTAGE FAULT DETECTION

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VDD Fault Threshold		9.1		10.3	V
VCC Fault Threshold		4.1		4.4	V
VOL Output Low Voltage	4.5 < VCC < 5.5V, IOL = 1.6 mA			0.4	V
	1.0 < VCC < 4.5V, IOL = 0.5 mA			0.4	V
IOH Output High Current				25	µA

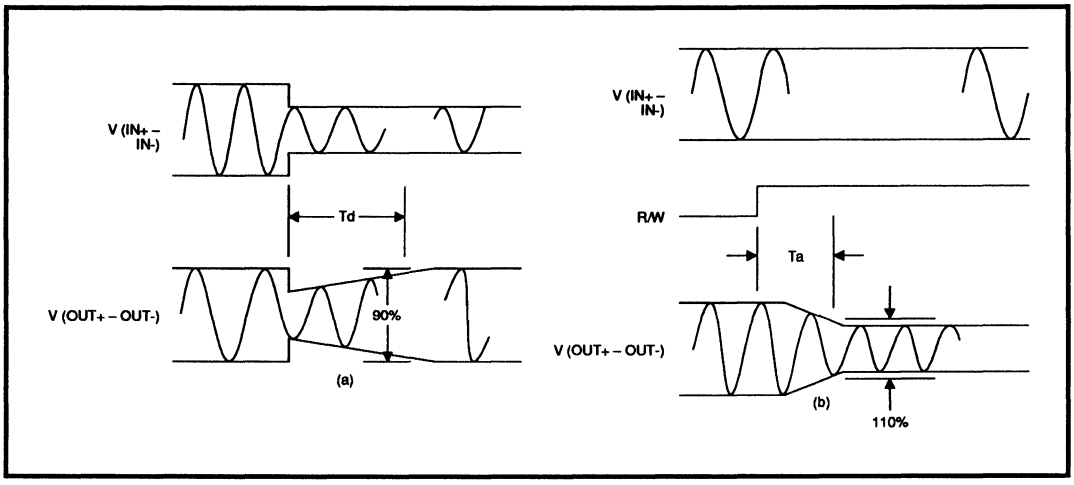


FIGURE 1(a), (b): AGC Timing Diagrams

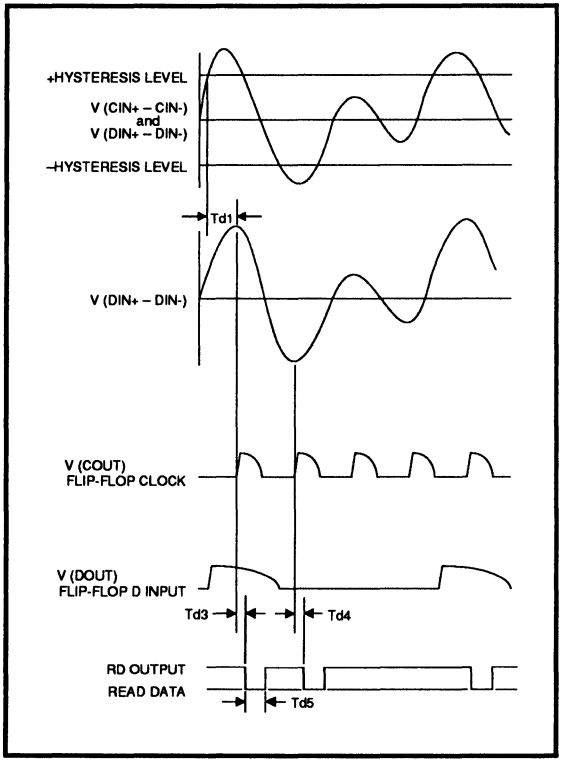
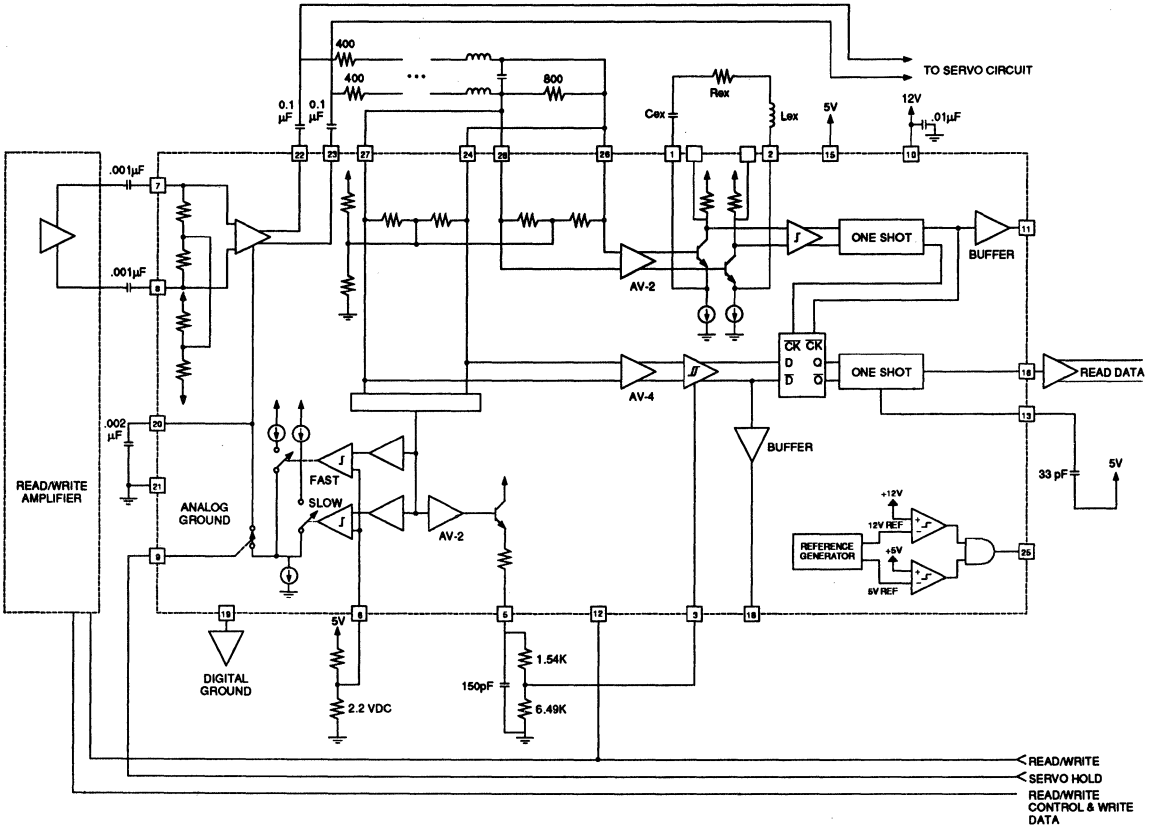


FIGURE 2: Timing Diagram



NOTE: Circuit traces for the 12V bypass capacitor and the AGC Hold Capacitor should be as short as possible with both capacitors returned to the Analog Ground Pin.
Component values, where given, are for a 24 Mbit/s System.
Above pin numbers are for the 28-pin PLCC package.

FIGURE 3: Typical Read/Write Electronics Set Up

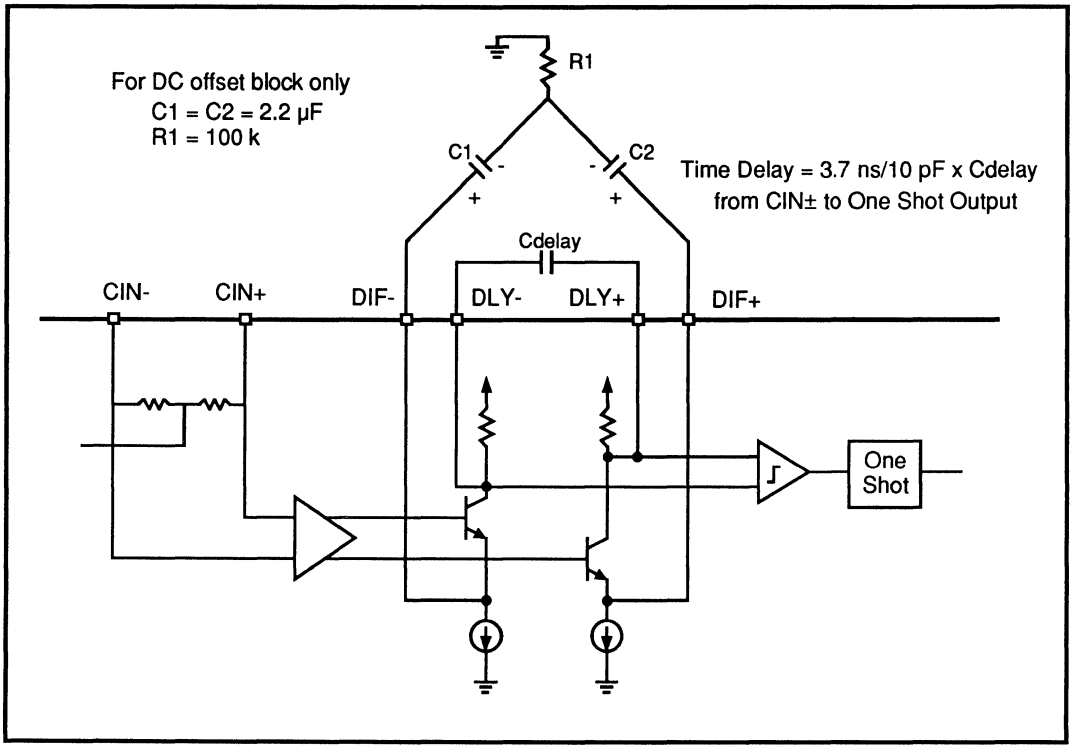


FIGURE 4: SSI 32P5411B Clock Delay Application Diagram

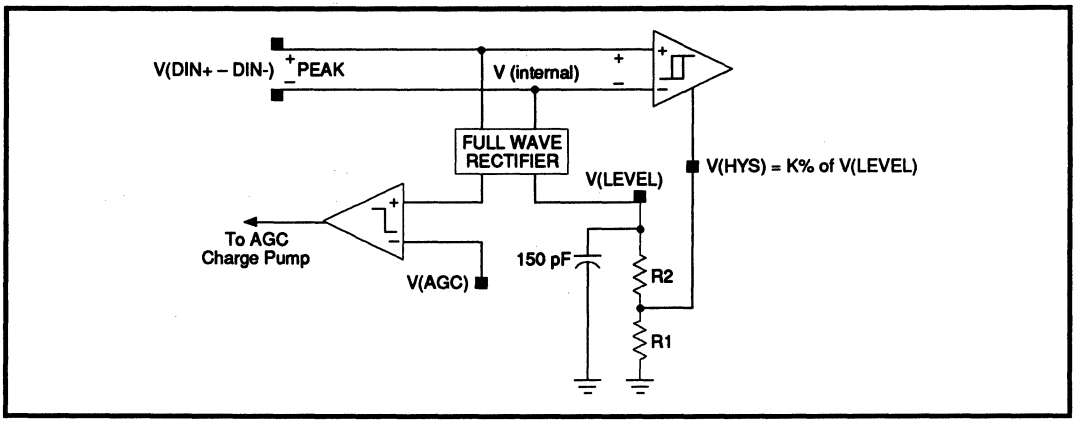


FIGURE 5a: Feed Forward Mode

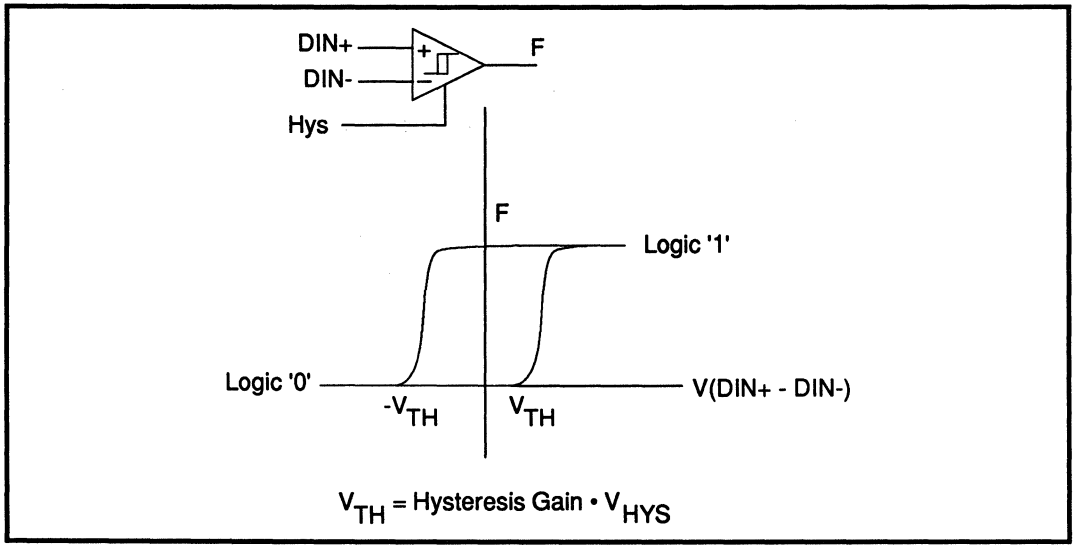


FIGURE 5b: Hysteresis Comparator Transfer Function

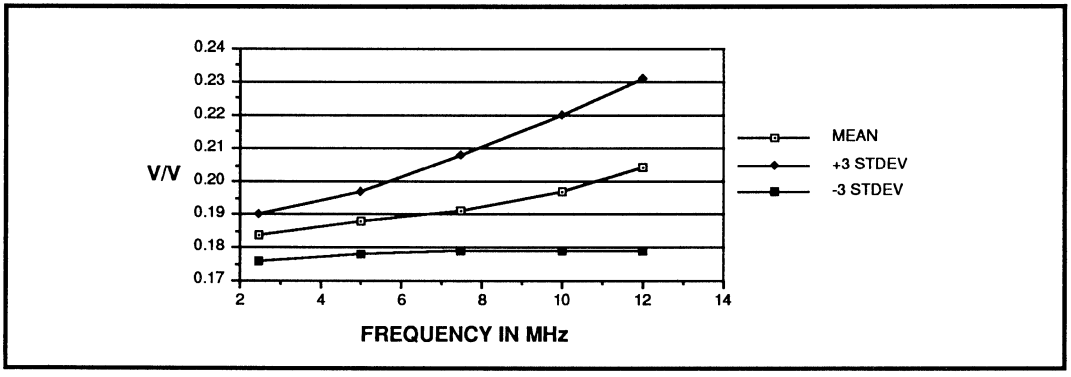


FIGURE 5c: Hysteresis Gain

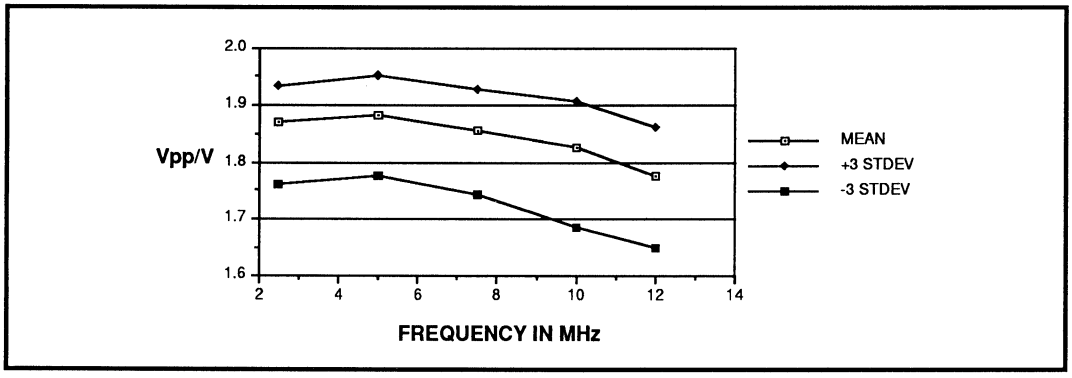


FIGURE 5d: Level Gain

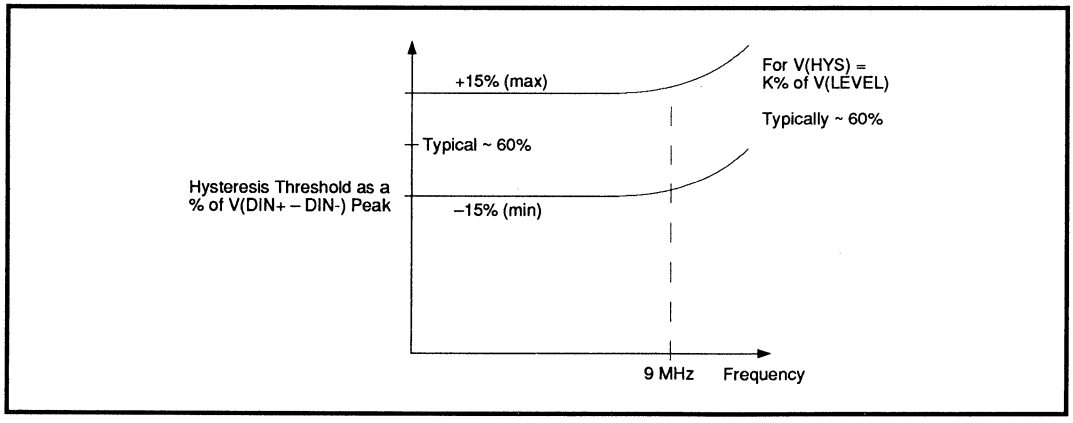


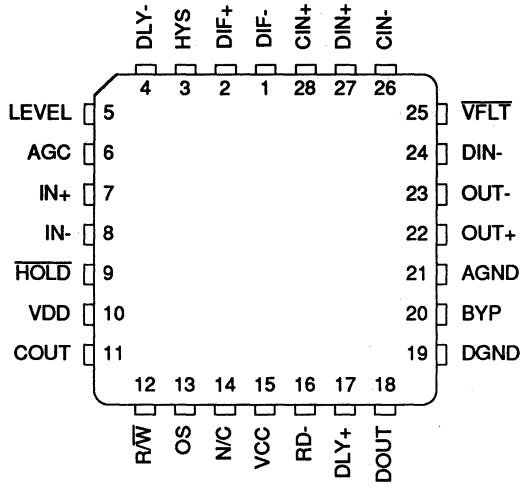
FIGURE 6: Percentage Threshold Versus Frequency

SSI 32P5411B
Read Data Processor

PACKAGE PIN DESIGNATIONS
(Top View)

THERMAL CHARACTERISTICS: θja

28-Lead PLCC	65°C/W



28-Lead PLCC

CAUTION: Use handling procedures necessary for a static sensitive component.

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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SSI 32P544
Read Data Processor and Servo Demodulator

July 1990

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DESCRIPTION

The SSI 32P544 Read Data Processor and Servo Demodulator has a fully integrated bipolar circuit that detects and validates amplitude peaks in the output from a disk drive read amplifier, as well as detecting embedded servo information to provide position error signals used for read head positioning.

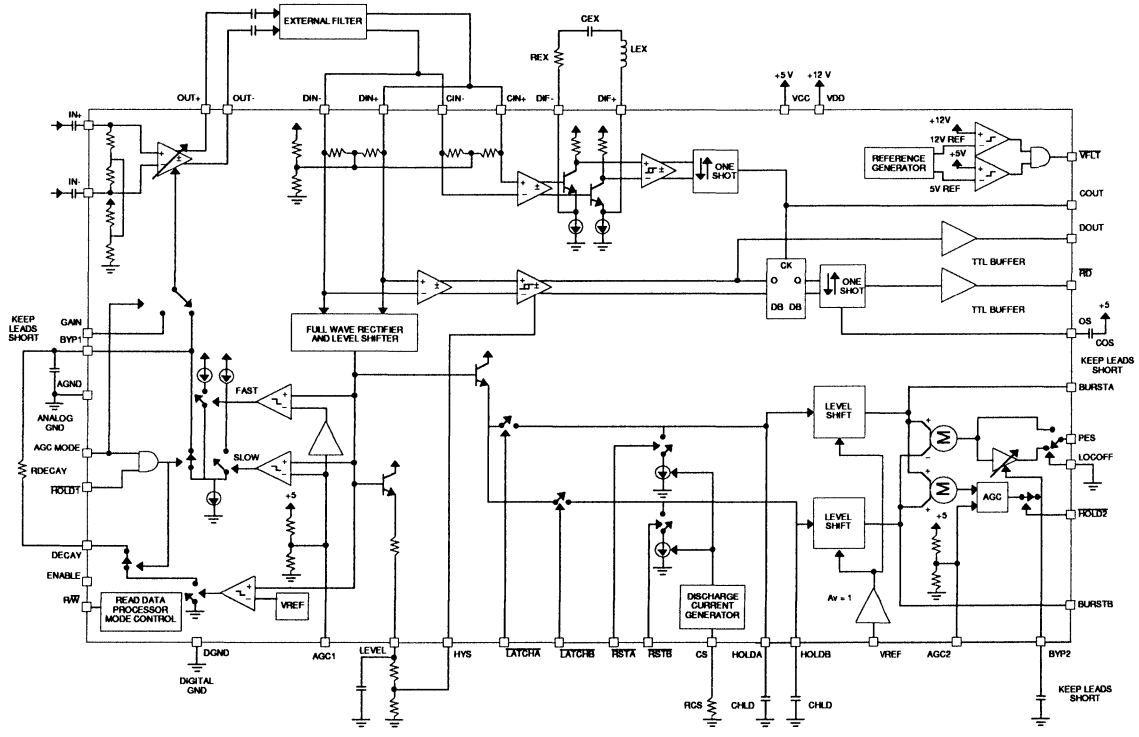
Time and amplitude qualification are used to provide a TTL compatible output that accurately duplicates the time position of input signal peaks. An AGC control loop, using a dual rate charge pump, provides a constant imput amplitude for the level qualifier. Level qualification can be implemented as a fixed threshold or a constant percentage that tracks signal amplitude that enhances qualification during AGC loop transients.

(Continued)

FEATURES

- **Wide bandwidth AGC input amplifier**
- **Level qualification supports MFM and RLL encoded data retrieval**
- **Fast and slow AGC attack and decay regions for fast transient recovery**
- **Embedded servo channel provides servo burst capture and difference circuits**
- **Local servo AGC provided based on servo burst output amplitude sum**
- **Standard ±10%, 12V and 5V supplies**
- **Write to Read transient suppression**

BLOCK DIAGRAM



DESCRIPTION (Continued)

The Servo Demodulator consists of two peak detector channels that capture rectified servo data peaks. Buffered individual channel outputs are provided along with a difference output. Servo channel gain can be controlled by an AGC signal based on maintaining the amplitude of the sum of both channels.

The circuit also provides a voltage fault flag that indicates a low voltage condition on either supply.

The SSI 32P544 requires standard ±10% tolerance +5V and +12V supplies and is available in a 44-pin PLCC package.

CIRCUIT OPERATION

READ MODE

In Read Mode the SSI 32P544 is used to process either data or servo signals. In the Data Read Mode the input signal is amplified and qualified using an AGC amplifier and pulse level qualification of the detected signal peaks. In the Servo Read Mode the input signal is amplified and an error signal based on amplitude comparison is made available.

DATA READ MODE

An amplified head output signal is AC coupled to the IN+ and IN- pins of the AGC amplifier. Gain control is accomplished by full wave rectifying and amplifying the [(DIN+) - (DIN-)] voltage level and comparing it to a reference voltage level at the AGC1 pin.

Two attack modes are entered depending on the instantaneous level at DIN±. For DIN± levels above 125% of desired level a fast attack mode is invoked that supplies 1.7 mA charging current to the network on the BYP1 pin. Between 125% and 100% of the desired level the circuit enters a slow attack mode and supplies 0.18 mA of charging current. This allows the AGC to rapidly recover during a write to read transition but reduces distortion once the AGC amplifier is in range.

Two decay modes are available that apply a discharge current to the BYP1 pin network when DIN± falls below the desired level. An internal decay current sink will supply 4.5 µA of discharge current. Also, if |(DIN+) - (DIN-)| is above 200 mVop a decay current, controlled by a resistor from BYP1 to DECAY, is switched in to decrease decay time. The amount of charge pulled from the AGC timing capacitor on each data pulse is:

$$Q_{DECAY} = K_1(Ton + Ts)/R_{DECAY}$$

Where:

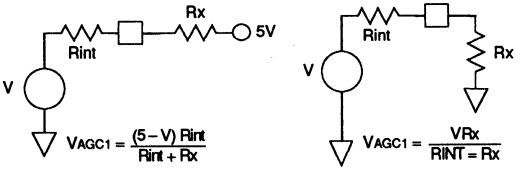
K_1 = 4.0V typ.

Ton = Time in seconds that the data pulse at DIN± is greater than 200 mVop

Ts = Switching time in seconds (<2 µs, max)

The AGC1 pin is internally biased so that the target differential voltage input at DIN± is 1.0 Vpp at nominal conditions. The AGC1 voltage can be modified by tying a resistor between AGC1 and ground or VCC. A resistor to ground decreases the voltage level while a resistor to VCC increases it. The resultant AGC1 voltage level is:

Where:



V = Voltage at AGC1 with pin open (2.2V, nom.)

Rint = AGC1 pin input impedance (6.7 kΩ, typ.)

Rx = External resistor.

The new DIN± input target level is nominally 0.48 Vpp/ V_{AGC1}

The AGC amplifier can swing 3.0 Vpp at OUT± which allows for up to 6 dB loss in any external filter between OUT± and DIN±.

Gain of the AGC amplifier is nominally:

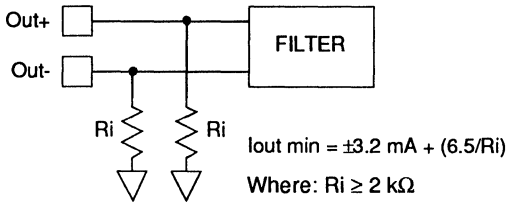
$$Av1/Av2 = e^{[6.9\,(V2 - V1)]}$$

Where:

Av1, Av2 are initial and final amplifier gains.

V1, V2 are initial and final voltages on the BYP1 pin.

The minimum output current from the AGC amplifier is ±3.2 mA. In cases where more current is required to drive a low impedance load the current can be increased by connecting load resistors Ri from OUT± to GND, as shown below.



One filter for both amplitude (DIN± input) and time (CIN± input) channels, or a separate filter for each may be used. If two filters are used, attention must be paid to time delays so that each channel is timed properly. A multi-pole Bessel filter is typically used for its linear phase or constant group delay characteristics.

In the amplitude channel the signal is sent to a hysteresis comparator. The hysteresis threshold level is set so that it will be tripped only by valid signal pulses and not by baseband noise. It can be fixed level or a fraction of the DIN± voltage level.

The latter approach is accomplished by using an external filter/network between the LEVEL and HYS pins. This allows setting the AGC slow attack and decay times slow enough to minimize time channel distortion and setting a shorter time constant for the hysteresis level. The LEVEL pin output is a rectified and amplified version of DIN±, 1.0 Vpp at DIN± results in 2.0 Vop nominally, at the LEVEL pin. A voltage divider is used from LEVEL to ground to set the Hysteresis threshold at a percentage of the peak DIN± voltage. For example, if DIN± is 1.0 Vpp, then using an equal valued resistor divider will result in 1.0 Vop at the HYS pin. This will result in a nominal ±0.210V threshold or a 42% threshold of a ±0.500V DIN± input. The capacitor is chosen to set an appropriate time constant. This "feed forward" technique speeds up transient recovery by allowing qualification of the input pulses while the AGC is still settling. This helps in the two critical areas of write to read and head change recovery. Some care in the selection of the hysteresis level time constant must be exercised so as to not miss pattern (resolution) induced lower amplitude signals. The output of the hysteresis comparator is the "D" input of a D-type flip-flop. The DOUT pin provides a buffered TTL compatible comparator output signal for testing purposes or for use in the servo circuit if required.

In the time channel the signal is differentiated to transform signal peaks to zero crossings which are detected and used to trigger a bi-directional one-shot. The one-shot output pulses are used as the clock input of the D flip-flop. The COUT pin provides the one-shot output for test purposes.

The differentiator function is accomplished by an external network between the DIF+ and DIF- pins. The transfer function from CIN± to the comparator input (not DIF±) is:

$$Av = \frac{-1000(Abuf)(Cs)}{2LCs^2 + C(R+92)s + 1}$$

Where: C, L, R are external passive components
$20\ pF < C < 150\ pF$
Abuf = Gain From CIN± to DIF±
$s = j\omega = j2\pi f$

During normal operation, the time channel clocks the D flip-flop on every positive and negative peak of the CIN± input. The D input to the flip-flop only changes state when the DIN± input exceeds the hysteresis comparator threshold opposite in polarity to the previous threshold exceeding peak.

The time channel, then, determines signal peak timing and the amplitude channel determines validity by blocking signal peaks that do not exceed the hysteresis comparator threshold. The delays in each of these channels to the D flip-flop inputs are well matched.

The D flip-flop output triggers a one-shot that sets the $\overline{RD}$ output pulse width. Width is controlled by an external capacitor from the OS pin to VCC.

SERVO READ MODE

A position error signal (PES) is generated based on the relative amplitude of two servo signals, A and B. Several methods are made available for maintaining channel gain during servo signal processing.

SERVO READ MODE (Continued)

Rectified servo signal peaks are captured on hold capacitors at the HOLDA/B pins. This is accomplished by pulling $\overline{\text{LATCHA}}$ or $\overline{\text{LATCHB}}$ low for a sample period. Additionally, a hold capacitor discharge current of up to 1.0 mA can be turned on by pulling $\overline{\text{RSTA}}$ or $\overline{\text{RSTB}}$ low. The discharge current is determined by a resistor tied between CS and ground. Its magnitude is:

$$I_{CS} = 2.6/(R_{CS} + 750)\ \text{A, typ.}$$

Where: R_{CS} = resistor from CS to ground

Outputs BURSTA/B & PES are referenced to an external reference applied to the VREF pin.

As noted, several methods are used to determine channel gain in Servo Read Mode. These methods make use of the data read mode AGC loop, the servo AGC loop and external or fixed AGC loop gain. Two methods are used that control the channel gain based on maintaining the sum of A & B channel amplitudes.

In one case (see Figure 1) the BYP2 pin is connected to the GAIN pin and the servo channel gain is determined by the read channel gain as controlled by the sum of the A and B amplitudes. In this case a current is sourced/sinked to/from the capacitor on the GAIN/BYP2 pin whenever the $\overline{\text{HOLD2}}$ pin is pulled high. The current magnitude and direction is determined by:

$$I_C = K_4[(K_5 \bullet V_{AGC2}) - Va(DIN)pp - Vb(DIN)pp]$$

Where:

V_{AGC2} = AGC2 pin voltage

K_4 = 650 µA/Vpp

K_5 = 0.39 V/V

Va/b(DIN)pp = peak to peak A or B servo pattern Signal voltages at DIN±

The other case (see Figure 2) controls the channel by fixing the Read Data channel gain by taking $\overline{\text{HOLD1}}$ low and closing the loop about the Servo Channel AGC (LOCOFF is held low for this mode).

$\overline{\text{HOLD2}}$ is used to update the control voltage on the AGC capacitor at the BYP2 pin. This AGC function has a time constant defined by:

$$\text{Time Constant} = K_6 \bullet C_{BYP2}$$

Where: K_6 = 1.64 to 7.5 kΩ

C_{BYP2} = BYP2 pin capacitor value in farads

Another method (see Figure 5) uses either a fixed voltage at the GAIN pin to determine channel gain or a gain based on preamble data amplitude. In this case no AGC methods are used that are based on servo signal amplitudes. Gain, as determined by an external voltage has been covered above. In the preamble method $\overline{\text{HOLD1}}$ is taken low during a preamble and the channel gain, determined by that necessary to maintain DIN± as programmed by the AGC1 voltage, is held during servo data processing.

WRITE MODE

In Write Mode the SSI 32P544 is disabled and preset for the following Read Mode. The digital circuitry is disabled, the input AGC amplifier gain is set to maximum and the AGC amplifier input impedance is reduced.

Resetting the AGC amplifier gain and input impedance shortens system Write to Read recovery times. With the AGC gain at maximum when returning to Read mode the AGC loop is in fast attack mode.

The lowered input impedance improves settling time by reducing the time constant of the network between the SSI 32P544 and a read preamplifier such as the SSI 32R510A. Write to read timing is controlled to maintain the reduced impedance for 1.2 to 3.0 µs before the AGC circuitry is activated. Coupling capacitors should be chosen with as low a value as possible consistent with adequate bandwidth to allow more rapid settling.

POWER DOWN MODE

A power down mode is provided to reduce power usage during the idle periods. Taking ENABLE pin low selects this mode. Recovery from this state can be slow due to the necessity of charging external capacitors.

LOW VOLTAGE FAULT DETECTION

A low voltage detection circuit monitors both supplies and pulls an open collector TTL output low whenever either supply drops below their trip point.

MODE CONTROL

The SSI 32P544 circuit mode is controlled by the ENABLE, R/$\overline{\text{W}}$, AGCMODE, $\overline{\text{HOLD1}}$, $\overline{\text{HOLD2}}$, and LOCOFF pins as shown in Table 1.

Data Read Mode

AGC active and controlled by data, Digital section active

Data Read Mode, Hold

AGC gain held constant, Digital section active. Gain will drift higher at rate determined by C_{BYP1} and Hold mode discharge current.

Servo Read Mode I (See Figures 1 & 3)

The BYP2 and GAIN pins are tied together. Read amplifier AGC control voltage developed from sum of Servo signal levels. $\overline{HOLD2}$ is toggled to update the control voltage after each Servo frame.

Servo Read Mode II (See Figures 2 & 4)

Read amplifier AGC gain held fixed ($\overline{HOLD1}$ low). Servo AGC loop activated with $\overline{HOLD2}$ toggled to update or hold gain based on a constant servo signal sum.

Servo Mode III (See Figure 5)

Read channel gain determined by voltage on GAIN pin.

Write

Read amplifier input impedance reduced. BYP1 pin voltage pulled low to select maximum amplifier gain. Digital section deactivated.

Power Down

Circuit switched to a low current disabled mode.

Note: When AGCMODE is switched to a low state the voltage at the BYP1 pin will be held subject to Hold mode discharge current induced drift. So, when returning to Data Read Mode, the channel gain will be the same as it was prior to AGCMODE switching or slightly higher.

TABLE 1: SSI 32P544 Circuit Mode Control

ENABLE	R/$\overline{W}$	AGC MODE	$\overline{HOLD1}$	$\overline{HOLD2}$	LOCOFF	READ PATH MODES
1	1	1	1	-	-	Data Read Mode
1	1	1	0	-	-	Data Read Mode Hold
1	1	0	-	1	1	Servo Read Mode I
1	1	0	-	0	1	
1	1	1	0	0	0	Servo Read Mode II
1	1	1	0	1	0	
1	1	0	-	-	-	Servo Mode III
1	0	-	-	-	-	Write
0	-	-	-	-	-	Power Down

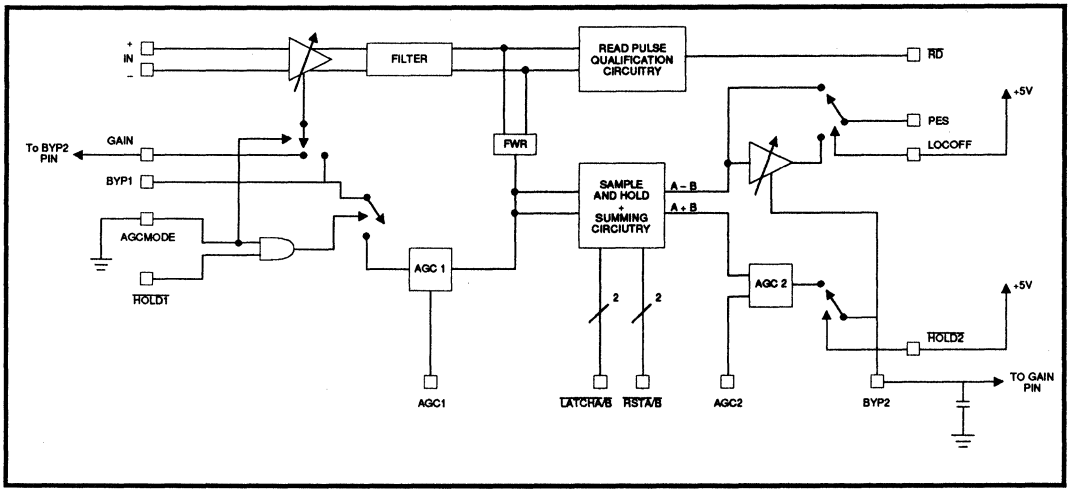


FIGURE 1: Servo Read Mode I

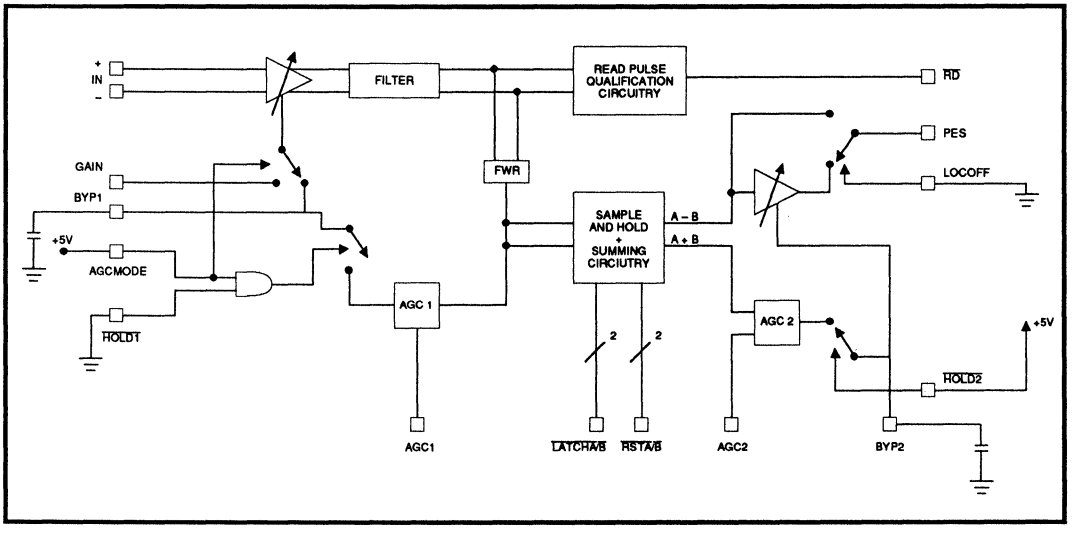


FIGURE 2: Servo Read Mode II

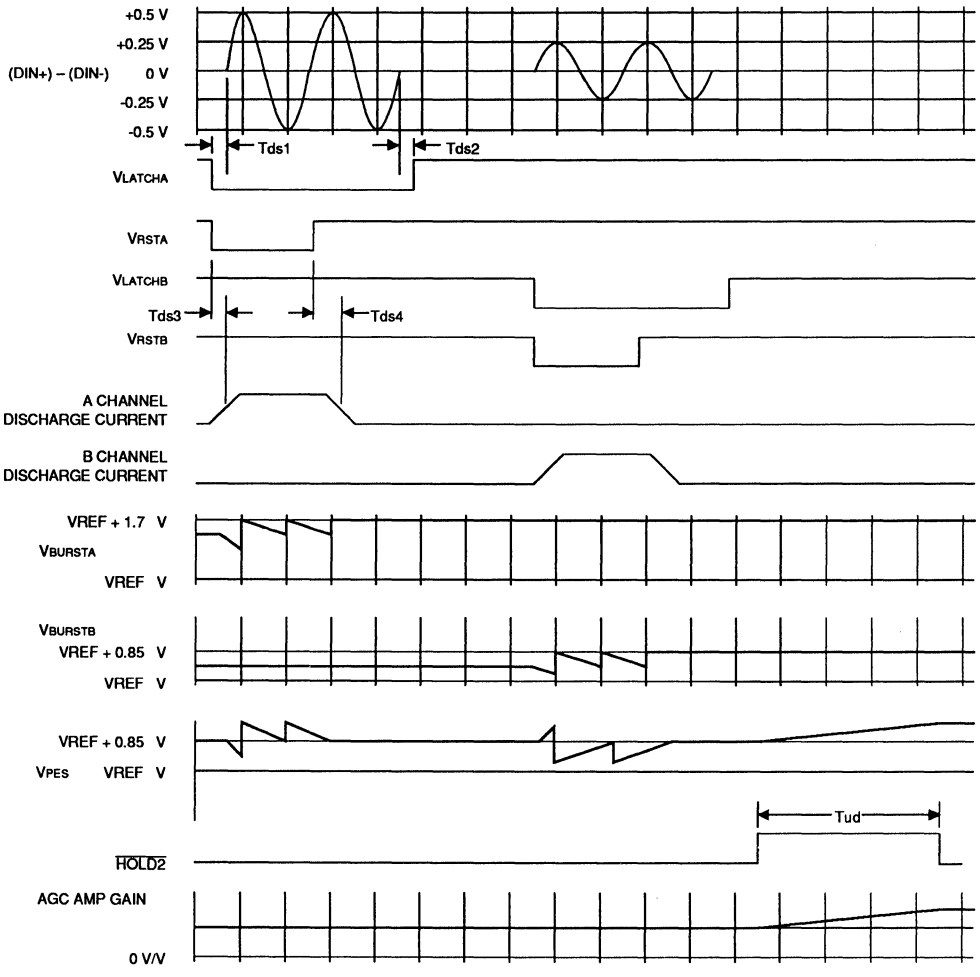


FIGURE 3: Servo Read Mode I Timing Diagram

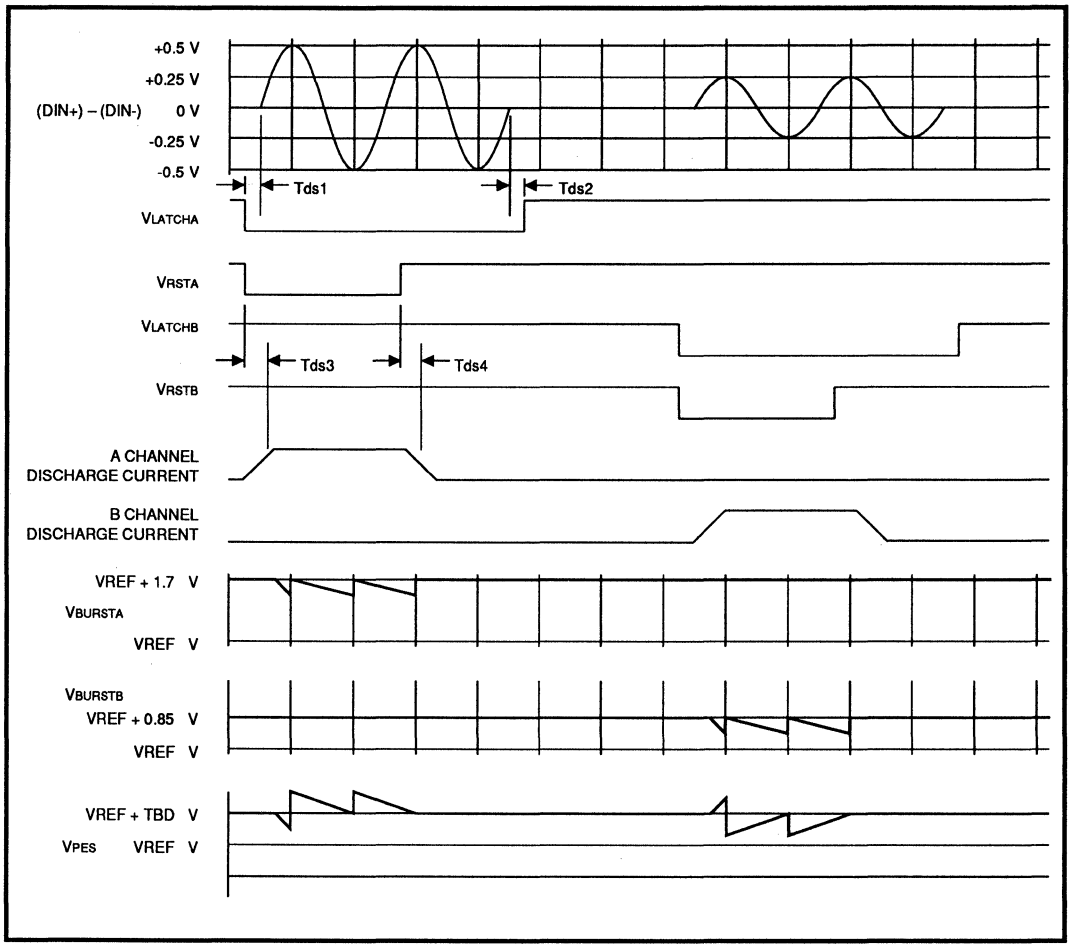


FIGURE 4: Servo Read Mode II Timing Diagram

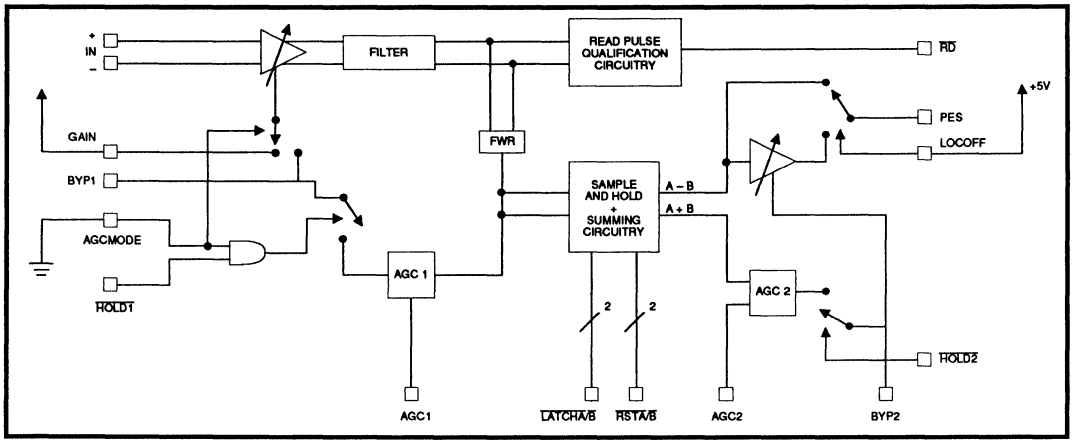


FIGURE 5: Servo Read Mode III

PIN DESCRIPTIONS

POWER SUPPLY AND CONTROL

NAME	DESCRIPTION
VCC	5 volt power supply.
VDD	12 volt power supply.
AGND, DGND	Analog and digital ground pins.
R/$\overline{W}$*	TTL compatible read/write control pin
ENABLE*	TTL compatible power up control pin. A low input selects a low power state.
$\overline{VFLT}$	Open collector output that goes low when a low power supply fault is detected.

AGC GAIN STAGE

IN+, IN-	Analog signal input pins.
OUT+, OUT-	Read path AGC amplifier output pins.
AGC1	Reference input voltage level for the read path AGC loop.
AGCMODE*	TTL compatible pin that selects the AGC loop control input. A high selects BYP1, a low GAIN.
BYP1	An AGC timing capacitor or network is tied between this pin and AGND.
GAIN	A voltage at this pin may be used to control AGC gain.
DECAY	A resistor to control the AGC loop decay time constant may be tied between this pin and BYP1.
$\overline{HOLD1}$*	TTL compatible control pin that holds the read path AGC loop gain constant when low.

PIN DESCRIPTIONS (Continued)

DIGITAL PROCESSING STAGE

NAME	DESCRIPTION
DIN+, DIN-	Analog input to the hysteresis comparator.
CIN+, CIN	Analog input to the differentiator.
DIF+, DIF-	Pins for external differentiating network.
LEVEL	Output from full wave rectifier that may be used for input to the hysteresis-comparator.
HYS	Threshold setting input to the hysteresis-comparator.
DOUT	Buffered TTL output for monitoring the flip-flop D input. Provided for testing or servo use.
COUT	Test point for monitoring the flip-flop clock input.
OS	Connection for output pulse width setting capacitor.
$\overline{RD}$	TTL compatible read output.

SERVO BURST CAPTURE STAGE

$\overline{LATCHA}$, $\overline{LATCHB}$	TTL compatible inputs that switch channels A or B into peak acquisition mode when low.
HOLDA, HOLDB	Peak holding capacitors are tied from each of these pins to AGND.
$\overline{RSTA}$, $\overline{RSTB}$	TTL compatible inputs that enable discharge of Channel A or B hold capacitors when low.
CS	Hold capacitor discharge current magnitude is controlled by a resistor from this pin to ground.
VREF	Reference voltage input for servo outputs.
AGC2	Reference input voltage level for the servo AGC loop.
BYP2	An AGC timing capacitor or network is tied between this pin and AGND.
$\overline{HOLD2}$	TTL compatible control pin that holds the servo AGC loop gain constant when low.
BURSTA, BURSTB	Buffered hold capacitor voltage outputs.
PES	Position error signal A minus B output.
LOCOFF*	TTL compatible input to select path for PES signal. (Local On/Off) Selects between AGC amp. output or A-B output.

* These inputs have internal pull-ups, so an open connection is the same as a high input.

ELECTRICAL SPECIFICATION

ABSOLUTE MAXIMUM RATINGS

Operation outside these rating limits may cause permanent damage to this device.

PARAMETER	RATING	UNIT
5V Supply Voltage, VCC	6.0	V
12V Supply Voltage, VDD	14.0	V
Pin Voltage GAIN, BYP1/2, AGC1/2 LEVEL, HYS, HOLDA/B, VREF BURSTA/B, PES, COUT, DIF±, OUT±	-0.3 to VDD + 0.3	V
Pin Voltage IN±, AGCMODE, $\overline{\text{HOLD1/2}}$, ENABLE, R/$\overline{\text{W}}$, $\overline{\text{LATCHA/B}}$, $\overline{\text{RSTA/B}}$, CS, LOCOFF, OS, CIN±, DIN±	-0.3 to VCC + 0.3	V
Pin Voltage RD, DOUT, DECAY, $\overline{\text{VFLT}}$	-0.3 to VCC + 0.3 or +12 mA	V
Storage Temperature	65 to 150	°C
Lead Temperature (Soldering 10 sec.)	260	°C

RECOMMENDED OPERATING CONDITIONS

Currents flowing into the chip are positive.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VCC	Supply Voltage		4.5	5.0	5.5	V
VDD	Supply Voltage		10.8	12.0	13.2	V
Ta	Ambient Temperature		0		70	°C

ELECTRICAL CHARACTERISTICS

POWER SUPPLY

Recommended conditions apply unless otherwise specified.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
ICC	VCC Supply Current	Outputs unloaded, ENABLE = high or open			20	mA
ICC		ENABLE = low			17	mA
IDD	VDD Supply Current	Outputs unloaded, ENABLE = high or open			90	mA
IDD		ENABLE = low			25	mA

POWER SUPPLY (Continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Pd	Power dissipation	Tj = 145°C, ENABLE = high, Outputs unloaded			1.0	W
		ENABLE = low, Outputs unloaded			0.35	W

LOGIC SIGNALS

VIL	Input Low Voltage		-0.3		0.8	V
VIH	Input High Voltage		2.0		VCC+0.3	V
IIL	Input Low Current	VIL = 0.4V	0.0		-0.4	mA
IIH	Input Low Current	VIH = 2.4V			100	µA
VOL	Output Low Voltage	IOL = 4.0 mA			0.4	V
VOH	Output High Voltage	IOH = 400 µA	2.4			V
	Output rise time	VOH = 2.4V*			15.0	ns
	Output full time	VOL = 0.4V*			9.0	ns

*10 - 90%, 10 pF capacitor to DGND

MODE CONTROL

Enable to/from Disable Transition Time	Settling time of external capacitors not included ENABLE pin high to/from low			10	µs
Read to Write Transition Time	R/$\overline{W}$ pin high to low			1.0	µs
Write to Read Transition Time	R/$\overline{W}$ pin low to high AGC setting not included	1.2		3.0	µs
AGC On to/from AGC Off Transition Time	AGCMODE pin high to/from low			2.0	µs
$\overline{HOLD1}$ On to/from $\overline{HOLD2}$ Off Transition Time	$\overline{HOLD1}$ pin high to/from low			1.0	µs
$\overline{HOLD2}$ On to $\overline{HOLD2}$ Off Transition Time	$\overline{HOLD2}$ pin high to/from low			1.0	µs

WRITE MODE

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Common Mode Input Impedance	R/$\overline{W}$ pin = low		250		Ω

READ MODE

READ PATH AGC AMPLIFIER

Unless otherwise specified, recommended operating conditions apply. Input signals are AC coupled to IN±. OUT± are loaded differentially with >600Ω, and each side is loaded with < 10 pF to AGND, and AC coupled to DIN±. A 2000 pF capacitor is connected between BYP1 and AGND. AGC1 pin is open. R/$\overline{W}$ is high.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Gain Range	1.0 Vpp ≤ (OUT+) – (OUT-) ≤ 3.0 Vpp	4		83	V/V
Output Offset Voltage	Over entire gain range	-400		+400	mV
Maximum Output Voltage Swing	Set by BYP1 pin	3.0			Vpp
Differential Input Resistance	(IN+) – (IN-) = 100 mVpp @ 2.5 MHz		5.0		kΩ
Differential Input Capacitance	(IN+) – (IN-) = 100 mVpp @ 2.5 MHz			10	pF
Common Mode Input Impedance	R/$\overline{W}$ = high		1.8		kΩ
	R/$\overline{W}$ = Low		250		Ω
Input Noise Voltage	Gain set to maximum			30	nV/$\sqrt{Hz}$
Bandwidth	-3 dB bandwidth at maximum gain	28			MHz
OUT+ to OUT- Pin Current	No DC path to AGND	±3.0			mA
Output Resistance		20		50	Ω
CMRR (Input Referred)	(IN+) = (IN-) = 100 mVpp @ 5 MHz, gain set to max	40			dB

READ PATH AGC AMPLIFIER (Continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
PSRR (Input Referred)	VDD or VCC = 100 mVpp @ 5 MHz, gain set to max	30			dB
Externally controlled Gain Constants $AV = K_2 \cdot e^{(K_3 \cdot VGAIN)}$ V/V	K_2, AGCMODE = Low K_3, AGCMODE = Low	.89 1.95		2.3 2.64	
Gain pin parasitic Input current	AGCMODE & $\overline{HOLD1}$ = low	0.2		+0.2	µA
(DIN+) – (DIN-) Input Swing vs. AGC1 Input	30 mVpp ≤ (IN+) – (IN-) ≤ 550 mVpp 0.5 Vpp ≤ (DIN+) – (DIN-) ≤ 1.5 Vpp, AGCMODE & $\overline{HOLD1}$ = high	0.36		0.56	Vpp/V
(DIN+) – (DIN-) Input Voltage Swing Variation	30 mVpp ≤ (IN+) – (IN-) ≤ 550 mVpp			8.0	%
AGC1 Voltage	AGC1 open, $V_{(ACC1)}$ = 2.35V	-5		+5	%
AGC1 Pin Input Impedance		5.0		8.3	kΩ
Fast Decay Threshold (DIN+) – (DIN-)	AGCMODE = high		±0.3		V
Slow AGC Capacitor Discharge Current	(DIN+) – (DIN-) = 0V V_{BYP} = 4.5V		4.0		µA
AGC Capacitor Leakage Current	AGCMODE = high, $\overline{HOLD1}$ = low, 2.5V < V_{BYP} < 5.5V	-0.2		+0.2	µA
Slow AGC Capacitor Charge Current	(DIN+) – (DIN-) = 0.75 VDC, vary AGC1 until slow charge begins	-0.14		-0.22	mA
Fast AGC Capacitor Charge Current	(DIN+) – (DIN-) = 0.75 VDC, V_{AGC1} = 3.0V	-1.3		-2.0	mA
Fast to Slow Attack Switchover Point	[(DIN+) – (DIN-)] – [(DIN+) – (DIN-)]FINAL		0.2		Vpp
Gain Decay Time (Td) (See Figure 6a)	(IN+) – (IN-) = 300 mVpp to 150 mVpp @ 2.5 MHz DECAY pin open, (OUT+) – (OUT-) to 90% final value.		50		µs

READ PATH AGC AMPLIFIER (Continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Gain Attack Time (Ta) (See Figure 6b)	R/$\overline{W}$ = low to high (IN+) – (IN-) = 400 mVpp @ 2.5 MHz, (OUT+) – (OUT-) to 110% final value		4		µs

HYSTERESIS COMPARATOR

Unless otherwise specified, recommended operating conditions apply. Input (DIN+) – (DIN-) is an AC coupled, 1.0 Vpp, 2.5 MHz sine wave. 1.8 VDC is applied to the HYS pin. ENABLE and R/$\overline{W}$ pins are high.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Input Signal Range				1.5	Vpp
Differential Input Resistance	(DIN+) – (DIN-) = 100 mVpp @ 2.5 MHz	10		18.0	kΩ
Differential Input Capacitance	(DIN+) – (DIN-) = 100 mVpp @ 2.5 MHz			4.0	pF
Common Mode Input Impedance (Both Sides)		2.25		5.0	kΩ
Level Pin Output Voltage vs. (DIN+) – (DIN-)	0.6 Vpp < (DIN+) – (DIN-) < 1.5 Vpp, 10K between LEVEL and AGND	1.2		2.2	V/Vpp
Level Pin Output Impedance	I_{LEVEL} = 0.5 mA		180		
Level pin Maximum Output Current		3.0			mA
Hysteresis Voltage at DIN± vs. HYS Pin Voltage	1 V < HYS < 3V	0.16		0.25	V/V
Hysteresis threshold margin as a % of V(DIN+) – (DIN-) peak	V(HYS) = some % of *V(AGC) or V(LEVEL) 1V < V(HYS) < 3V *see Figures 8 & 9	-15		+15	%Peak
HYS Pin Current	1 V < HYS < 3V	0.0		-20	µA
Comparator Offset Voltage	HYS pin at AGND ≤ 1.5 kΩ across DIN±			10.0	mV

* In an open loop configuration where reference is V(AGC) tolerance can be slightly higher.

ACTIVE DIFFERENTIATOR

Unless otherwise specified, recommended operating conditions apply. Input (CIN+) – (CIN-) is an AC-coupled, 1.0 Vpp, 2.5 MHz sine wave. 100Ω in series with 65 pF are tied from DIF+ to DIF-.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Input Signal Range				1.5	Vpp
Differential Input Resistance	(CIN+) – (CIN-) = 100 mVpp @ 2.5 MHz	10		18.0	kΩ
Differential Input Capacitance	(CIN+) – (CIN-) = 100 mVpp @ 2.5 MHz			4.0	pF
Common Mode Input Impedance	Both sides	2.25		5.0	kΩ
Voltage Gain From CIN± to DIF±	(DIF+ to DIF-) = 2 kΩ	1.7		2.2	V/V
DIF+ to DIF- PIn Current	Differentiator impedance must be set so as to not clip the signal for this current level	±1.2			mA
Comparator Offset Voltage	DIF+, DIF- are AC-coupled			10.0	mV
COUT Pin Output Low Voltage	0 ≤ IOL ≤ 0.5 mA		VDD-3.0		V
COUT pin Output Pulse Voltage, V_{HIGH} - V_{LOW}	0 ≤ IOL ≤ 0.5 mA		0.4		V
COUT pin Output Pulse Width	0 ≤ IOH ≤ 0.5 mA		30		ns

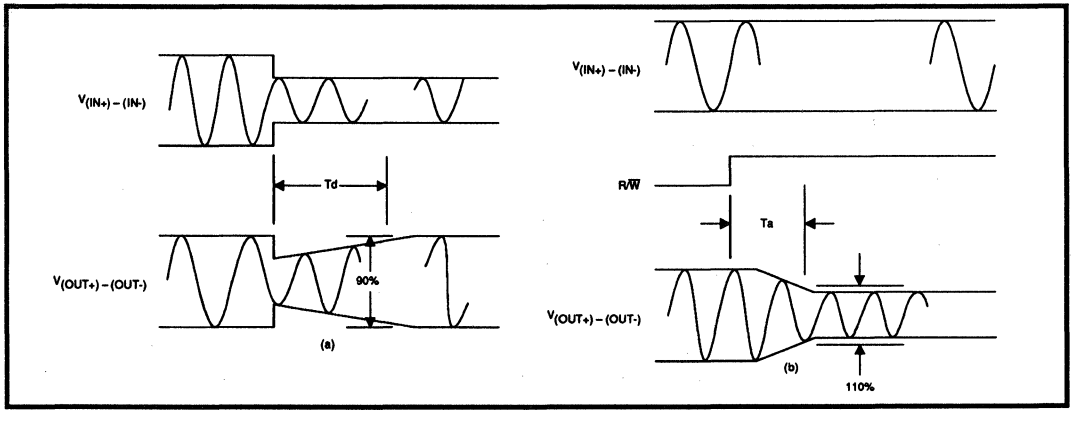


FIGURE 6: AGC Timing Diagram

OUTPUT DATA CHARACTERISITICS (See Figure 7)

Unless otherwise specified, recommended operating conditions apply. Inputs (CIN+) – (CIN-) and (DIN+) – (DIN-) are in-place as a coupled, 1.0 Vpp, 2.5 MHz sine wave. 100Ω in series with 65 pF are tied from DIF+ to DIF-. 1.8V is applied to the HYS pin. A 60 pF capacitor is tied between OS and VCC. $\overline{RD}$ is loaded with a 4 kΩ resistor to VCC and a 10 pF capacitor to DGND. ENABLE and R/$\overline{W}$ pins are high.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Td1	D Flip-Flop Set Up Time	Minimum allowable time delay from (DIN+) – (DIN-) exceeding hysterisis point to (DIF+) – (DIF-) hitting a peak value.	0			ns
Td3	Propagation Delay				110	ns
Td5	Output Pulse Width Variation	Td5 = 800(Cos) @ V_{RD} = 1.4V 50 pF ≤ Cos ≤ 200 pF			±15	%
|Td3-Td4|	Pulse Pairing				1.5	ns

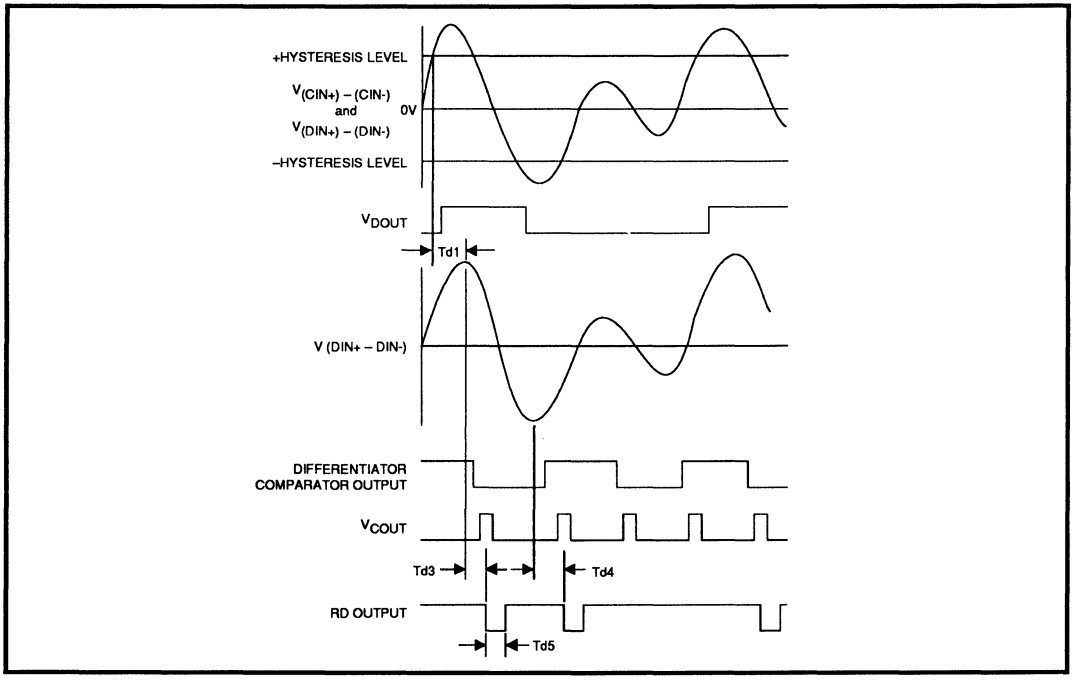


FIGURE 7: Read Mode Digital Section Timing Diagram

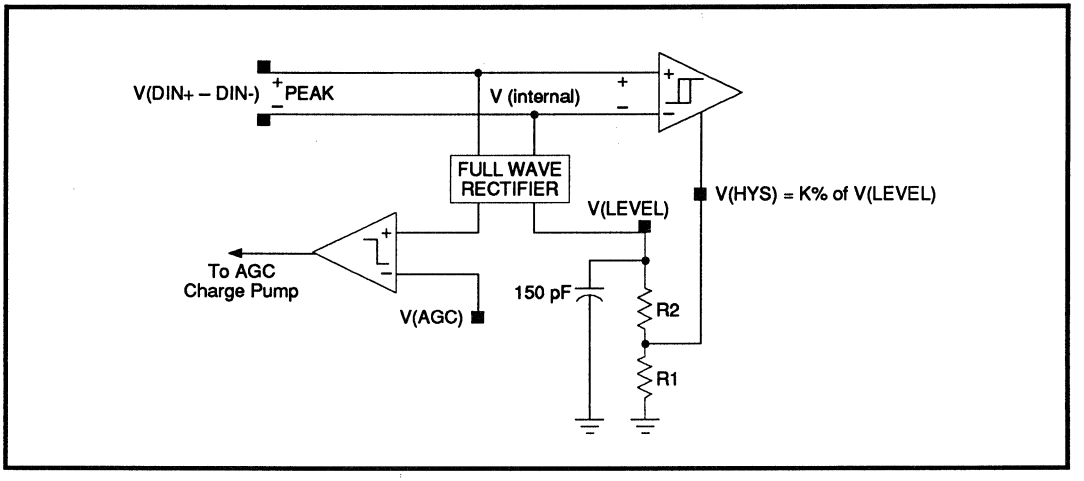


FIGURE 8: Feed Forward Mode

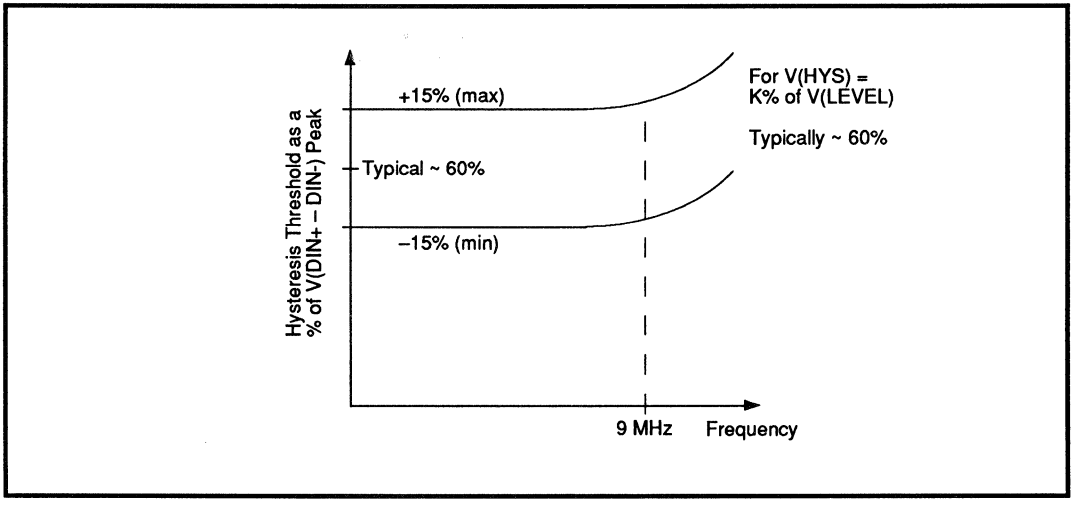


FIGURE 9: Percentage Threshold vs. Frequency

SERVO SECTION (Unless otherwise specified, recommended operating conditions apply.)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VREF Voltage Range		3.9		6.0	V
AGC2 Pin Voltage	AGC2 Pin Open, $V_{(AGC2)}$ = 3.4V	-5		+5	%
AGC2 Pin Input Impedance		5.0		9.1	kΩ
BURSTA/B pin Output Voltage vs (DIN+) – (DIN-)	$\overline{LATCHA/B}$ = Low $\frac{V_{BURSTA/B} - VREF}{(DIN+) - (DIN-)}$ = 1.7 V/Vp-p	-6.5		+6.5	%
BURSTA/B Output Offset Voltage V_{BURST} - VREF	$\overline{LATCHA/B}$ = Low, (DIN+) = (DIN-), RCS = 38.3 kΩ	-80		+80	mV
BURSTA - BURSTB Output Offset Match	$\overline{LATCHA/B}$ = low (DIN+) = (DIN-)	-15		+15	mV
Maximum PES Pin Output Voltage	Controlled by AGC2			5.0	Vpp
PES Pin Output Offset Voltage	V_{PES} - VREF, (DIN+) = (DIN-) $\overline{LATCHA/B}$ = Low After 30 sec. temp. stable	-50		+50	mV
Output Resistance, BURSTA/B & PES pins				20	Ω
Hold A/B Charge Current	$\overline{LATCHA/B}$ = Low	25			mA
HOLDA/B Discharge Current Tolerance	$\overline{RSTA/B}$ = Low, ICS = 2.6V/(RSC + 750Ω)	-15		+15	%
	$\overline{RSTA/B}$ = High, $\overline{LATCHA/B}$ = High	-0.5		+0.5	µA
Load Resistance BURSTA/B, PES pins	Resistors to VREF	10.0			kΩ
Load Capacitance BURSTA/B, PES pins				20	pF
$\overline{LATCHA/B}$ pin set up time	(Tds1 in Figures 3 & 4)	150			ns
$\overline{LATCHA/B}$ pin Hold Time	(Tds2 in Figures 3 & 4)	150			ns
Channel A/B Discharge Current Turn On time	(Tds3 in Figures 3 & 4)			150	ns
Channel A/B discharge Current Turn Off time	(Tds4 in Figures 3 & 4)			150	ns
BYP2 Pin Parasitic Input Current	$\overline{HOLD2}$ = Low LOCOFF = Low LOCOFF = High	 -0.02 -9.0		 +0.02 +9.0	 µA µA

SERVO SECTION (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
BYP2 Pin Charge/Discharge Current $I_C = K_4[(K_5 \cdot V_{AGC2}) - V_{A(DIN)pp} - V_{B(DIN)pp}]$	K_4, $\overline{HOLD2}$ = High	487	650	813	µA/Vpp
	K_5, $\overline{HOLD2}$ = High	0.35		0.43	V/V
*AGC Gain Range	LOCOFF=Low	0.6		6.0	V/Vpp
V_{PES} pp vs. V_{AGC2}	V_{PES} pp/V_{AGC2} LOCOFF = Low	1.24	1.38	1.52	Vpp/V
	LOCOFF = High	1.42	1.5	1.58	
	V_{PES} pp/V_{AGC2} AGC2=Open LOCOFF = Low	5.03	5.3	5.56	Vpp Vpp/V
	LOCOFF = High	5.32	5.6	5.88	
BURSTA/B Pin Output vs. V_{AGC2}	$(V_A + V_B - 2VREF)/V_{AGC2}$ LOCOFF = High		0.77		V/V
	$V_A + V_B$ - 2VREF, AGC2=Open LOCOFF = High		2.85		V

*Av = (VPES - VREF)/($V_{A(DIN)pp}$ + $V_{B(DIN)pp}$)

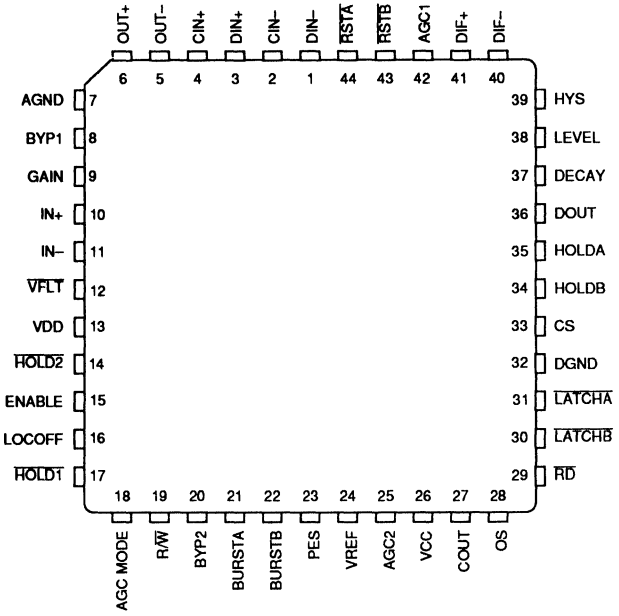
Supply Voltage Fault Detection

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
VDD Fault Threshold		9.1		10.5	V
VCC Fault Threshold		4.1		4.4	V
VOL Output Low	4.5 < VCC < 5.5V, IOL = 1.6 mA			0.4	V
	1.0 < VCC < 4.5, IOL = 0.5 mA			0.4	V
IOH Output High Current				25	µA

2

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



44-pin PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32P544 - 44-pin PLCC	32P544-CH	32P544-CH

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 731-7110, FAX (714) 573-6914

Notes:

silicon systems®
A TDK Group Company

SSI 32P547
High Performance Pulse Detector

November 1991

2

DESCRIPTION

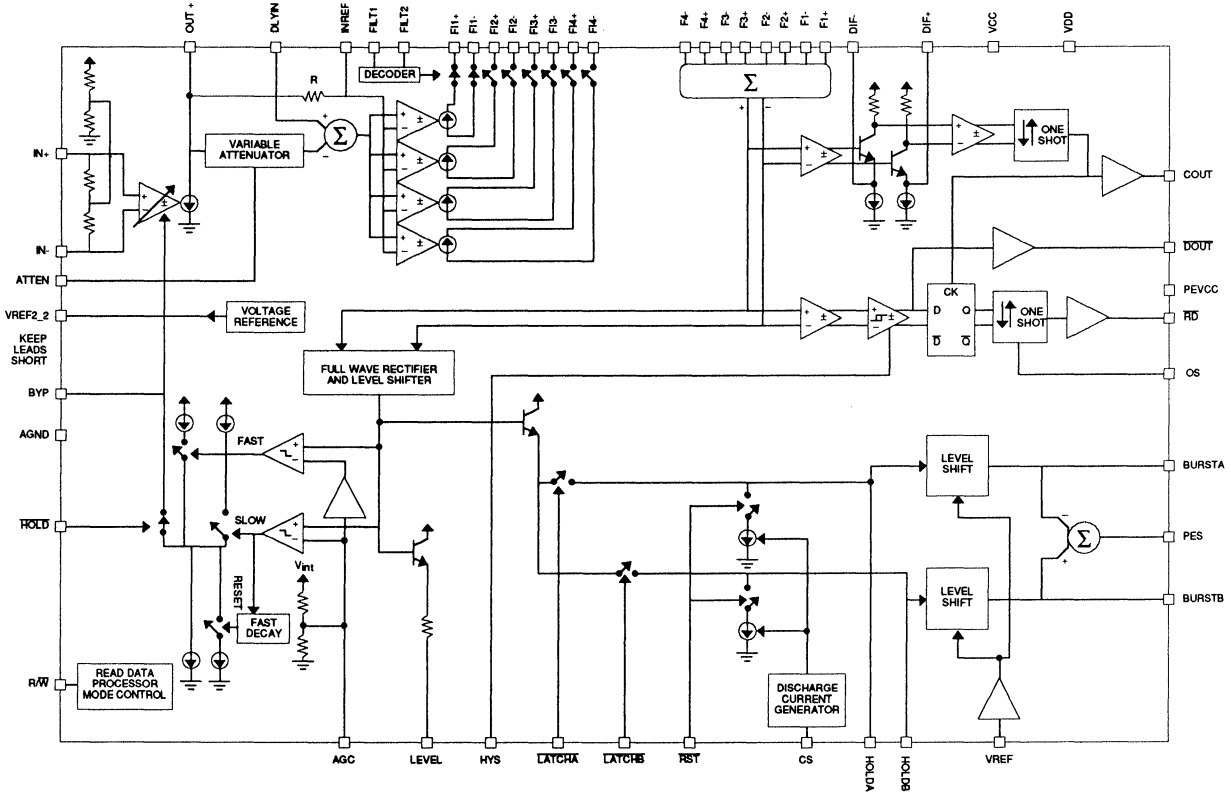
The SSI 32P547 Read Data Processor and Servo Demodulator with Variable Pulse Slimming and Zone Filter Mux is a fully integrated bipolar circuit that detects and validates amplitude peaks in the output from a disk drive read amplifier, as well as detecting embedded servo information to provide position error signals used for read head positioning.

Time and amplitude qualification are used to provide a PECL output that accurately duplicates the time position of input signal peaks. An AGC control loop, using a dual rate charge pump, provides a constant input amplitude for the level qualifier.

FEATURES

- **Wide bandwidth AGC input amplifier**
- **Uses standard +12V and +5V ± 10% supplies**
- **Level qualification supports MFM or RLL codes**
- **Servo burst capture circuit for use in embedded servo**
- **Four input differential filter MUX**
- **Pulse Slimming with Variable Attenuation**

BLOCK DIAGRAM



CIRCUIT OPERATION

Level qualification can be implemented as fixed threshold or a constant percentage that tracks signal amplitude that enhances qualification during AGC loop transients.

The Servo Demodulator consists of two peak detector channels that capture rectified servo data peaks. Buffered individual channel outputs are provided along with a difference output.

The SSI 32P547 requires standard ±10% tolerance +5V and +12V supplies and is available in a 52-pin Quad PLCC package.

MODE CONTROL

The circuit mode is controlled by the R/$\overline{W}$, and $\overline{HOLD}$ as shown in Table 1.

READ MODE

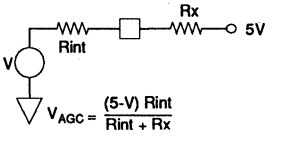
The circuit is placed in the read mode when the R/$\overline{W}$ pin is high or open and is disabled (write mode) when the R/$\overline{W}$ pin is low. In the write mode the digital circuitry is disabled, the AGC amplifier gain is set to maximum and the input impedance of the input analog stage is reduced to allow more rapid settling of the input coupling capacitors from the read/write circuit (such as the SSI 32R510A) upon transition to the read mode. Write to read transition timing is controlled to allow settling of the coupling capacitors between the read/write circuit and the SSI 32P547 before the AGC circuitry is activated when going to the read mode. Coupling capacitors should be chosen with as low a value as possible consistent with adequate bandwidth to allow for more rapid settling. When the R/$\overline{W}$, and $\overline{HOLD}$ pins are high or open the input amplifier is in the read data AGC mode and gain is controlled to keep a constant read data peak level. When the $\overline{HOLD}$ pin is pulled low the gain of the analog circuit is held at the level determined when the $\overline{HOLD}$ pin was high (the gain will slowly drift due to leakage).

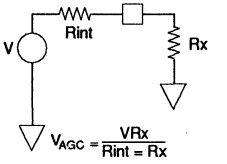
READ DATA AUTOMATIC GAIN CONTROL CIRCUIT

In this mode an amplified head output signal, such as the output of the SSI 32R117, 32R501, or 32R510A read/write circuits, is AC coupled to the IN+ and IN- inputs. In the read mode the level at the Fx +/- pins is controlled by full wave rectifying the level at the summer output and comparing it to a reference level supplied at the AGC pin. When the input level at the filter outputs is greater than 125% of the desired level as set by the AGC pin, the circuit is in a fast attack mode and will supply about 1.4mA of charging current at the BYP pin. When the input level is between 125% and 100% of the desired level, the circuit enters a slower attack mode and will supply about 0.16mA of charging current. This allows the AGC to rapidly recover when going from write to read but reduces zero crossing distortion once the AGC amplifier is in range.

To reduce the effect of gain attack overshoot on settling time (due to offsets) a fast decay mode is entered if slow decay mode exceeds 1.6 µsec (nom). Fast decay discharge current is 0.8 mA and slow decay discharge current is 4.5 µA.

The AGC pin is internally biased so that the level at the filter input pins is 0.83 Vpp. The level at the filter input pins can be increased by tying a resistor from the AGC pin to VCC or reduced by tying a resistor from the AGC pin to GND.





Where:

V = Voltage at AGC with pin open (2.4V, nom.)

Rint = AGC pin input impedance (6.7 KΩ, typ.)

Rx = External resistor.

The new DIN+/- input target level is nominally 0.43 Vp-p/V_{AGC}.

Gain of the AGC section in the AGC mode is approximately: $\left(\frac{Av1}{Av2}\right) = \exp\left[6.9 \times (V2 - V1)\right]$

Where:

Av1, Av2 are initial and final amplifier gains. V1, V2 are initial and final voltages on the BYP pin.

READ DATA PULSE SLIMMING CIRCUIT

The Pulse Slimming Circuit uses an external delay line and an analog controllable Variable Attenuator to implement pulse slimming. Input biasing for this stage is accomplished by low pass filtering the signal at the

OUT+ pin with an on chip resistor and external capacitor tied to the INREF pin and using that signal as a reference to the single-ended-to-differential gain stage which follows.

$$\text{Freq}(-3\text{dB}) = \frac{1}{2\pi RC}$$

Where: R (lowpass) is the on-chip resistor = 6 kΩ nom
C (ext) is the external capacitor

The ratio between the gains of the attenuated and non-attenuated signal paths (K) is controlled by varying the gain of the on-chip attenuator:

K = Av (attenuated) / Av (non-attenuated)
= Ko - G x V (ATTEN) / VREF2_2

Where G is the gain factor, V (ATTEN) is the voltage applied to the ATTEN pin. VREF2_2 is the voltage on the VREF2_2 pin and Ko is the value for K when V(ATTEN) = 0.0V.

SELECTABLE EXTERNAL FILTER DRIVER/RECEIVER

The on-chip circuitry allows four separate filters to be used for support of constant density recording. A filter is selected by using the two TTL input filter select pins; FILT1, and FILT2. Filter selection is as follows:

Filter1	Filter 2	Channel
0	0	FI1
0	1	FI2
1	0	FI3
1	1	FI4

READ MODE DIGITIZING SECTION

In the data path the signal is sent to a hysteresis comparator. The comparator hysteresis level can be set at a fixed level or, with the addition of an external filter network, a fraction of the signal level.

The latter approach allows setting the AGC circuit decay and slow attack times slow enough to minimize distortion of the signal going into the clocking path and setting a short time constant for the hysteresis level. Thus when switching to a head with a different output level or when switching from write to read the circuit is properly decoding data before the AGC circuit gain has settled to its final steady state value. The output of the hysteresis comparator is the "D" input of a D flip-flop. The $\overline{\text{DOUT}}$ pin provides a PECL comparator output digital signal for testing purposes and, if required, for use in the servo circuit.

In the clocking path the signal is sent to a differentiator circuit whose characteristics are set by external components. The differentiator transfer expression from Fx+/- to the comparator input (which is not the DIF+/- output) is:

$$Av = \frac{-2C_{ex}R_i s}{2L_{ex}C_{ex}s^2 + C_{ex}(R_{ex} + 2R_e)s + 1}$$

Where: R_i= on chip resistors = 1.0 KΩ nominally; R_e= emitter resistance seen at DIF+ or DIF- = 46 Ω nominally; C_{ex}= external capacitor, allowable range is 20 pF to 150 pF; R_{ex}= external resistor; L_{ex}= external inductor.

The output of the differentiator circuit is sent to the edge trigger circuit which creates an output pulse on every zero crossing of the output of the differentiator. The output of the edge trigger is the clock input of the D flip-flop. During normal system operation the differentiator circuit clocks the D flip-flop once every positive and negative peak of the input signal.

The data path D input to the flip-flop only changes state when the signal applied to the filter inputs exceeds the hysteresis comparator threshold in a polarity opposite the polarity of the peak which last exceeded the threshold. Therefore, the clocking path determines signal timing and the data path blocks spurious peaks if they do not exceed the hysteresis comparator threshold. Figure 6 shows circuit operation of the digital section. The two digital signal path delays between the Fx+ and Fx- inputs to the flip-flop clock and data inputs are well matched.

SERVO BURST CAPTURE SECTION

Rectified servo data peaks are latched into the A or B servo channels by pulling the TTL compatible inputs $\overline{\text{LATCHA}}$ or $\overline{\text{LATCHB}}$ low, respectively. A chip-generated discharge current is turned on for channels A or B by pulling the TTL compatible input $\overline{\text{RST}}$ low. The magnitude of this discharge current is set by a resistor tied to the CS pin.Outputs of the BURSTA, BURSTB, and PES are referenced to an externally generated reference applied at the VREF pin.

PIN DESCRIPTIONS

POWER SUPPLY AND CONTROL

NAME	I/O	DESCRIPTION
VCC		5 Volt power supply.
PEVCC		Collector of PECL emitter follower output which is to be connected to the 5 volt power supply.
VDD		12 volt power supply
AGND		Analog ground pin
R/$\overline{W}$	I	TTL compatible read/write control pin

AGC GAIN STAGE

IN+,IN-		Analog signal input pins
OUT+		Transconductance output for the AGC amplifier and input to the variable attenuator
DLYIN		Delayed input signal to the pulse slimming amplifier
INREF		Reference DC voltage to the single ended to differential gain stage
VREF2_2		Internally generated voltage used as a reference by the external DAC used to control the attenuator gain
BYP		The AGC timing capacitor is tied between this pin and AGND
$\overline{HOLD}$	I	TTL compatible control pin which holds the input AGC amplifier AGC level when pulled low
ATTEN		An Analog input which controls the attenuation value for the Variable Attenuator
AGC		Reference input voltage for the AGC circuit

SERVO BURST CAPTURE STAGE

$\overline{LATCHA}$ $\overline{LATCHB}$	I	TTL inputs which initiates capture of a servo burst Peak on channel A or B when pulled low
HOLDA HOLDB		Peak holding capacitors are tied from each pin to GND
$\overline{RST}$	I	TTL input which initiates discharge of channel A and B hold capacitors when pulled low
CS		Pin to control magnitude of discharge current during active discharge of channel A and B hold capacitors
VREF		Reference level for servo circuit
BURSTA BURSTB		Buffered burst peak outputs
PES		BURST B minus BURST A output

DIGITAL PROCESSING STAGE

NAME	I/O	DESCRIPTION
Flx± Fx±		Differential filter I/O pins for the four external filters
FILT1 FILT2	I	TTL compatible inputs to control multiplexer for selection of 1 of 4 filters
HYS		Hysteresis level setting input to the hysteresis level detect comparator
LEVEL		Provides rectified signal level for input into the hysteresis circuit
$\overline{DOUT}$	O	A Pseudo ECL D input into D flip-flop provided for testing or servo use
DIF+,DIF-		Pins for external differentiator components
COUT	O	Clock input into D flip-flop provided for testing
OS		Pin for external capacitor in the one shot which determines read channel output one-shot pulse width
$\overline{RD}$	O	A Pseudo ECL (PECL) read output

TABLE 1: Mode Control

MODE	R/$\overline{W}$	$\overline{HOLD}$	CONDITIONS
Read/AGC	1	1	Read amp on, AGC active and controlled by data, Digital section active
Read/Hold	1	0	Read amp on at fixed gain, AGC level held constant Digital section active
Write	0	-	Read amp on with reduced input impedance AGC level pulled low, Digital section deactivated, BYP pin set for maximum AGC gain

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATING

Operation above absolute maximum ratings may permanently damage the device.

PARAMETER	RATING	UNITS
+5V Supply Voltage,VCC, PEVCC	6.0	V
+12V Supply Voltage,VDD	14.0	V
Pin Voltage BYP, AGC, LEVEL, HYS, HOLD A/B, VREF, BURST A/B, PES, DIF+/-, Flx±	-0.3 to VDD+0.3	V
Pin Voltage IN+/-, $\overline{HOLD}$, R/$\overline{W}$, $\overline{RST}$, ATTEN, $\overline{LATCHA/B}$, CS, OS, FILT1-2, Fx±, OUT+, DLYIN, INREF, VREF2_2	-0.3 to VCC+0.3	V

ABSOLUTE MAXIMUM RATING (continued)

PARAMETER	RATING	UNITS
$\overline{RD}$, $\overline{DOUT}$, COUT	-0.3 to VCC+0.3 or +12mA	V
Storage Temperature	-65 to +150	°C
Lead temperature (soldering 10 sec)	260	°C

RECOMMENDED OPERATING CONDITIONS

Currents flowing into the chip are positive.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VCC	Supply Voltage		4.5	5.0	5.5	V
VDD	Supply Voltage		10.8	12.0	13.2	V
Tj	Junction Temperature		25		145	C
Ta	Ambient Temperature		0		70	C

ELECTRICAL CHARACTERISTICS

POWER SUPPLY

Recommended conditions apply unless otherwise specified.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
ICC	VCC Supply Current	Outputs unloaded			50.0	mA
IDD	VDD Supply Current	Outputs unloaded			80.0	mA
Pd	Power dissipation	Ta=70° C Outputs unloaded			1.25	W

MODE CONTROL

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Read-to-Write Transition time	R/$\overline{W}$ Pin High → Low			1.0	µs
Write to Read Transition time	R/$\overline{W}$ Pin Low → High AGC settling not included	1.2		3.0	µs
Hold On ↔ Hold off Transition time	$\overline{HOLD}$ Pin High ↔ Low R/$\overline{W}$ Pin High			1.0	µs

LOGIC SIGNALS ($\overline{HOLD}$, FILT1-2, R/$\overline{W}$, $\overline{LATCHA}$,$\overline{B}$, $\overline{RST}$ Pins)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
VIL	Input Low Voltage		-0.3		0.8	V
VIH	Input High Voltage		2.0		VCC+0.3	V
IIL	Input Low Current	VIL = 0.4V	0.0		* -0.4	mA
IIH	Input High Current	VIH = 2.4V			100	µA

*For $\overline{RST}$ only, limit is -0.8 mA

PECL OUTPUT: $\overline{RD}$, $\overline{DOUT}$ PINS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Output Low Voltage				VCC-1.625	V
Output High Voltage		VCC-1.02			V
Output Rise Time	10 to 90 %			5.0	ns
Output Fall Time	90 to 10 %			5.0	ns

*Output load is a 2.5 kΩ resistor to GND, and a 5 pF capacitor to ground.

AUTOMATIC GAIN CONTROL CIRCUIT

All of the measurements in the AGC gain mode are made with the following conditions unless otherwise stated:

1. The circuit is in the read mode (R/$\overline{W}$, and $\overline{HOLD}$ pins high).
2. The circuit is connected as in Figure 5.
3. The amplifier inputs, IN+ and IN- , are AC coupled.
4. The OUT+ pin is loaded with 100 Ω to Vcc and Fx+, Fx- 200Ω each to VDD (through series capacitors).
5. A 1000 pF capacitor is tied between BYP and GND.
6. The AGC pin is left open.

READ DATA MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Slow AGC Capacitor Discharge Current	V(Fx+ - Fx-)=0.0 Volts Vary V(AGC) until slow discharge begins		4.5		µA
Fast AGC Capacitor Discharge Current	V(Fx+ - Fx-)=0.0 Volts Vary V(AGC) until fast discharge begins		0.8		mA
Fast Decay Hold Off Time	Slow Attack Threshold Not Reached	0.7	1.6	3.0	µs
AGC Capacitor Leakage Current	R/$\overline{W}$ pin high, $\overline{HOLD}$ low	-0.2		0.2	µA

ELECTRICAL CHARACTERISTICS (continued)

READ DATA MODE (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Slow AGC Capacitor Charge Current	V(Fx+ - Fx-)=0.41 Vdc, Vary V(AGC) until slow charge begins	-0.14		-0.22	mA
Fast AGC Capacitor Charge Current	V(Fx+ - Fx-)=0.8 Vdc Vary AGC until fast charge begins	-1.3		-2.0	mA
Fast → Slow Attack Switchover Point	Minimum V(Fx ±) in fast attack mode; Minimum V(Fx ±) in slow attack mode		0.15		V
Gain Attack Time (Ta) See Fig. 1	R/$\overline{W}$ = low → high, changing Vin from 200 to 400 mVpp @ 2.5 MHz, V(Fx±) to 110% of final value		4		µs
Fx+ - Fx- Input Voltage Swing vs AGC Input Voltage	15 mVpp < V(IN+ - IN-) < 250 mVpp, 0.4 Vpp < V(Fx+ - Fx-) < 1.25 Vpp, V(ATTEN) = V(VREF2_2)	0.25		0.48	Vpp/V
Fx+ - Fx- Input Voltage Swing Variation	15 mVpp < V(IN+ - IN-) < 250 mVpp 0.4 Vpp < V(Fx+ - Fx-) < 1.25 Vpp			8.0	%
AGC Pin Input Impedance		5.0		8.3	kΩ
AGC Pin Voltage	AGC pin open	2.28	2.4	2.52	V

AGC AMPLIFIER CHARACTERISTICS

Gain Range	Z Load = 100Ω	0.3		16.5	V/V
Output DC Voltage Variation	V(IN+) = V(IN-); over actual gain range			±150	mV
Maximum Allowable Output Voltage Swing on OUT+ pin				360	mVpp
Differential Input Resistance	V(IN+ - IN-)=100 mVpp @ 2.5 MHz		5.0		kΩ
Differential Input Capacitance	V(IN+ - IN-)=100 mVpp @ 2.5 MHz			10.0	pF
Common Mode Input Impedance	R/$\overline{W}$ pin = high		1.8		kΩ
(Both Sides)	R/$\overline{W}$ pin = low		250		Ω
Input Noise	Gain set to 16 V/V			25	$\frac{nV}{\sqrt{(Hz)}}$

AGC AMPLIFIER CHARACTERISTICS (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Bandwidth	Transconductance (Iout/Vin) ± 3 dB bandwidth, referenced to 2.5 MHz	40			MHz
Common Mode Rejection Ratio (Input Referred)	V(IN+) = V(IN-) = 100 mV, 5 MHz, gain set to 16 V/V	40			dB
Output DC Current on OUT+ Pin	IN+, IN- shorted together		4.5		mA
Output Impedance, OUT+ Pin			50		kΩ
Output Capacitance OUT+ Pin			5		pF
Allowable DC Load Resistance To VCC on OUT+ Pin		88		112	Ω
Allowable AC Load Impedance on OUT+ Pin		88		112	Ω
Power Supply Rejection Ratio (input referred)	ΔV(VDD) or ΔV(VCC) = 100 mVpp, 5 MHz, gain set at 16 V/V	22			dB

PULSE SLIMMER, EXTERNAL FILTER DRIVERS AND VARIABLE ATTENUATOR

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Gain from OUT+ pin to (Flx+ - Flx-)	V (ATTEN) = VREF2_2		9		V/V
Kmin, minimum attenuator gain	V(ATTEN) = VREF2_2			0.05	
Kmax, maximum attenuator gain	V(ATTEN) = 0.0V	0.81			
Gain Factor G Tolerance	G(ideal) = 0.83, V(ATTEN) = VREF2_2	-4		+4	%
Ko Tolerance	Ko(ideal) = 0.84, V(ATTEN) = 0.0V	-4		+4	%
Attenuator Gain K Ratio Linearity	0.0 < V(ATTEN) < VREF2_2 end point method	-0.0		-4	%
OUT+ to INREF pin resistance		5		9	kΩ
Output Voltage Ref VREF2_2 Pin	Iload = 0 to -1 mA	1.95	2.28	2.45	V
Output Voltage Resistance VREF2_2 Pin	Iload = -.7mA		4		Ω
Maximum Output Voltage Swing	Flx±	1.25			Vpp

ELECTRICAL CHARACTERISTICS (continued)

PULSE SLIMMER AND EXTERNAL FILTER DRIVERS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Input Resistance DLYIN Pin			200		kΩ
Input Capacitance DLYIN Pin			5		pF
Bandwidth referenced to 2.5 MHz	Transconductance I(FIx± /V(OUT+)	40			MHz
Allowable External DC Load Resistance	FIx± to VDD	190		210	Ω
Power Supply Rejection Ratio (Input Referred)	ΔV (12) or ΔV (5) = 100 mVpp, 5 MHz delayline shorted	45			dB
Input Resistance ATTEN Pin			200		kΩ
Input Bias Current ATTEN Pin			8		μA

READ MODE DIGITIZING SECTION

All of the measurements in the read mode digital section are made with the following conditions unless otherwise stated:

1. The circuit is in the read mode (R/$\overline{W}$ pin is high).
2. The summer input pins, (Fx+, Fx-) receive AC coupled 2.5 MHz, 0.83 Vpp sine wave input signal.
3. 100 Ω in series with 65 pF are tied between DIF+ and DIF-.
4. A 1.8 Vdc voltage is applied to the HYS pin.
5. OS is tied to the 5V supply with a 60 pF capacitor, Cos.
6. The $\overline{DOUT}$ pin is loaded with a 2.5 kΩ resistor to GND and a 5 pF capacitor to GND.
7. The $\overline{RD}$ pin is loaded with a 2.5 kΩ resistor to GND and a 5 pF capacitor to GND.

SUMMER AND BUFFER

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Allowable Input Signal Range	V(Fx+ - Fx-)			1.25	Vpp
Differential Input Resistance	V(Fx+ - Fx-) =100 mVpp DC	10		18	kΩ
Differential Input Capacitance	V(Fx+ - Fx-) =100 mVpp @2.5 MHz		4.0		pF
Common Mode Input Impedance	On all Fx+ to Fx- Fx+/- tied together	2.5		4.5	kΩ
Bandwidth referenced to 2.5 MHz	V(DIF±)/V(Fx±)	35			MHz

HYSTERESIS COMPARATOR CIRCUIT

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
LEVEL Pin Output Voltage vs Fx+ - Fx- Input Voltage	0.4 < V(Fx+ -Fx-) < 1.25 Vpp, 10 kΩ between LEVEL pin and GND	1.8		3.0	V/Vpp
LEVEL Pin Output Impedance	I(LEVEL) = 0.5 mA		180		Ω
LEVEL Pin Maximum Output Current	V(Fx±) = 0.415V, ΔV(Level) ≤0.8 V	3.0			mA
Comparator and Summer Offset Voltage	HYS pin at GND, ≤1.5 kΩ across Fx+,Fx-.			30	mV
Input referred Hysteresis Voltage (at Fx+ - Fx- Pins) vs HYS Pin Voltage	1 V < V(HYS) < 3 V	0.16		0.25	V/V
Hysteresis threshold tolerance as a % of V(Fx+ - Fx-) peak	Set V(HYS) such that Hysteresis Threshold (Ideal) is 60% of V(Fx±), V(Fx±) = .415V (see Figures 2 & 3)	-15		+15	%
HYS Pin Input Current	1 V < V(HYS) < 3 V	0.0		-20	µA

* In an open loop configuration where reference is V(AGC), tolerance can be slightly higher.

DIFFERENTIATOR CIRCUIT

Voltage Gain from Fx+/- to DIF+/-	R(DIF+ to DIF-) = 2.0 kΩ	2.0		3.06	V/V
DIF+ to DIF- Pin Current	Differentiator impedance must be set so as to not clip the signal for this current level	±1.3			mA
Comparator Offset Voltage	DIF+, DIF- AC coupled not directly measured			10.0	mV
COUT Pin Output Low Voltage	0.0 ≤ Iol ≤ 0.5 mA		VDD-3.0		V
COUT Pin Output Pulse Voltage Swing, V(high) - V(low)	0.0 ≤ Ioh ≤ 0.5 mA		+0.4		V
COUT Pin Output Pulse Width	0.0 ≤ Ioh ≤ 0.5 mA		30		ns
Required DFF Set-up Time, Td1 in Fig. 6	Minimum allowable time delay from V(Fx+,Fx-) exceeding hysteresis point to V(DIF+,DIF-) hitting peak value	0			ns
Propagation Delay, Td3 in Fig. 6				110	ns
Output Data Pulse Width at $\overline{RD}$ Pin, Td5 in Fig. 6	Td5(ideal) = 900 x Cos @ V($\overline{RD}$) = 50% 30 ≤ Cos ≤ 200 pF			±15	%

ELECTRICAL CHARACTERISTICS (continued)

READ DIGITAL SECTION AS SYSTEM

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Pulse Pairing |Td3 - Td4| Fig. 6	0.83 Vpp into Fx+/- pins at 2.5 MHz			1.5	ns
	0.83 Vpp into Fx+/- pins at 9.0 MHz			1.0	ns

SERVO BURST CAPTURE CIRCUIT

All of the measurements are made with the following conditions unless otherwise stated:

1. The circuit is connected as in Figure 5.
2. A and B bursts are sampled onto $\overline{\text{BURSTA}}$ and $\overline{\text{BURSTB}}$ pins.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Allowable VREF Voltage Range		3.9		6.0	V
BURSTA, BURSTB Pin Output Voltage vs (Fx+ - Fx-) Input Voltage	$AV=\frac{V(BURST)-VREF}{V(Fx+-Fx-)}=2.6V/Vpp$ $\overline{\text{LATCHA}}$ or $\overline{\text{LATCHB}}$ = Low			±11	%
BURSTA, BURSTB Output Offset Voltage	V(BURST) - V(VREF), $\overline{\text{LATCHA}}$, $\overline{\text{LATCHB}}$ Low, V(Fx+) = V(Fx-), RCS = 38.3 kΩ, $\overline{\text{RST}}$ low			±60	mV
BURSTA - BURSTB Output Offset Voltage Match	V(BURSTA)-V(BURSTB), $\overline{\text{LATCHA}}$, $\overline{\text{LATCHB}}$ Low, V(Fx+) = V(Fx-)			±15	mV
PES Pin Output Offset Voltage	V(PES) - V(VREF), $\overline{\text{LATCHA}}$, $\overline{\text{LATCHB}}$ Low, V(Fx+) = V(Fx-)			±50	mV
PES Pin Output Voltage vs. Va(Fx)pp - Vb(Fx)pp	$AV=\frac{V(PES)-VREF}{Va(Fx)pp-Vb(Fx)pp}=2.6V/Vpp$			±15	%
Output Resistance BURSTA, BURSTB PES pins				20.0	Ω
HOLDA/B Charge Current		25			mA
HOLDA/B Discharge Current	$\overline{\text{RST}}$ = Low; Idis = 2.6/(RCS + 750)	-15		+15	%
	$\overline{\text{RST}}$ = High, LATCH_A/B = High			±0.5	µA
Allowable Load Resistance; BURSTA/B,PES pins	Resistor to VREF	10.0			kΩ
Allowable Load Capacitance; BURSTA/B,PES pins				20.0	pF

SERVO BURST CAPTURE CIRCUIT (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
$\overline{\text{LATCHA/B}}$ Pin Setup Time (Tds1 in Fig. 2)		150			ns
$\overline{\text{LATCHA/B}}$ Pin Hold Time, (Tds2 in Fig. 2)		150			ns
Channel A/B Discharge Current Turn On Time (Tds3 in Fig. 2)				150	ns
Channel A/B Discharge Current Turn Off Time (Tds4 in Fig. 2)				150	ns

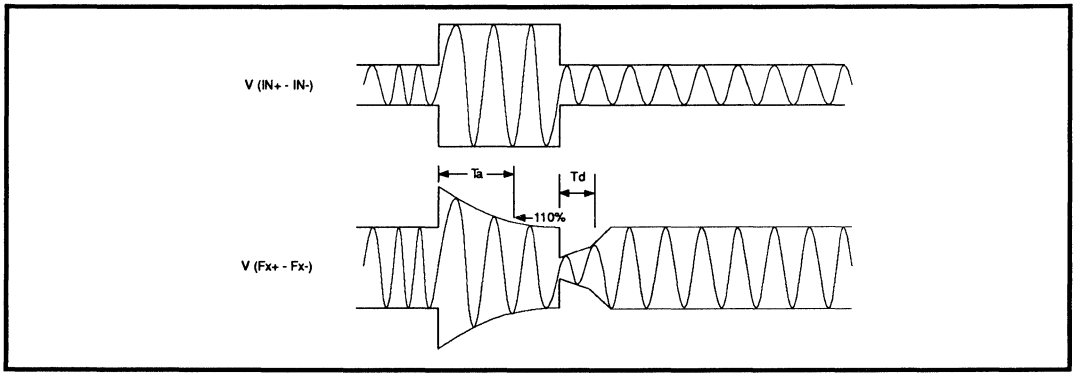


FIGURE 1: AGC Timing Diagram

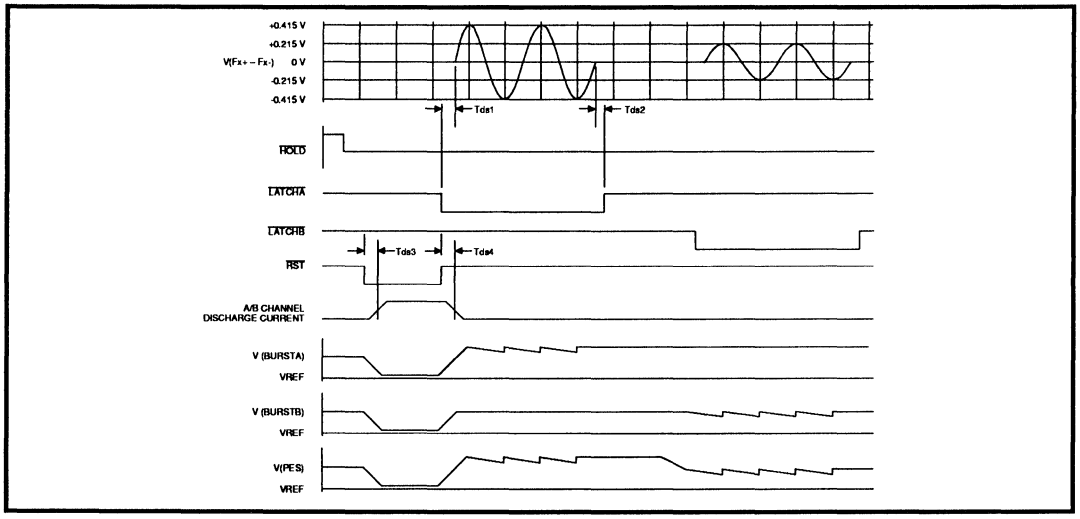


FIGURE 2: Servo Timing Diagram

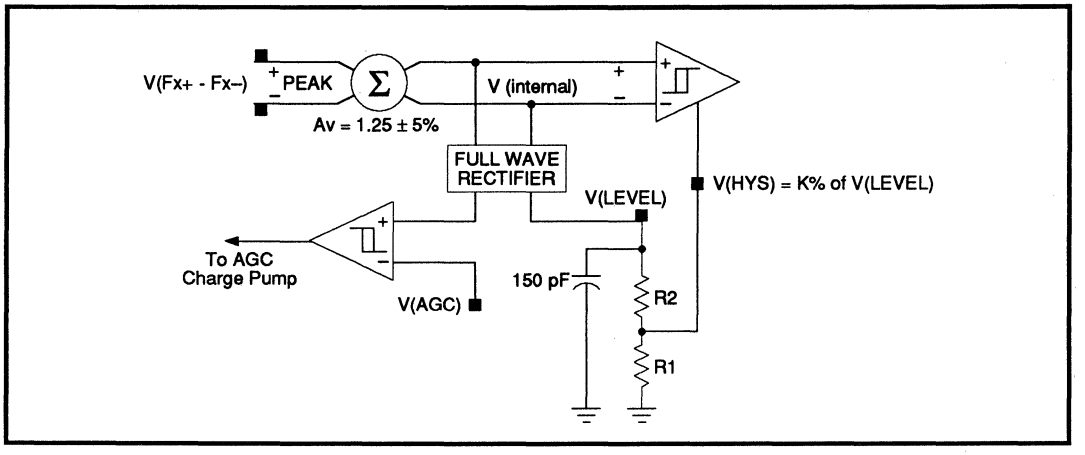


FIGURE 3: Feed Forward Mode

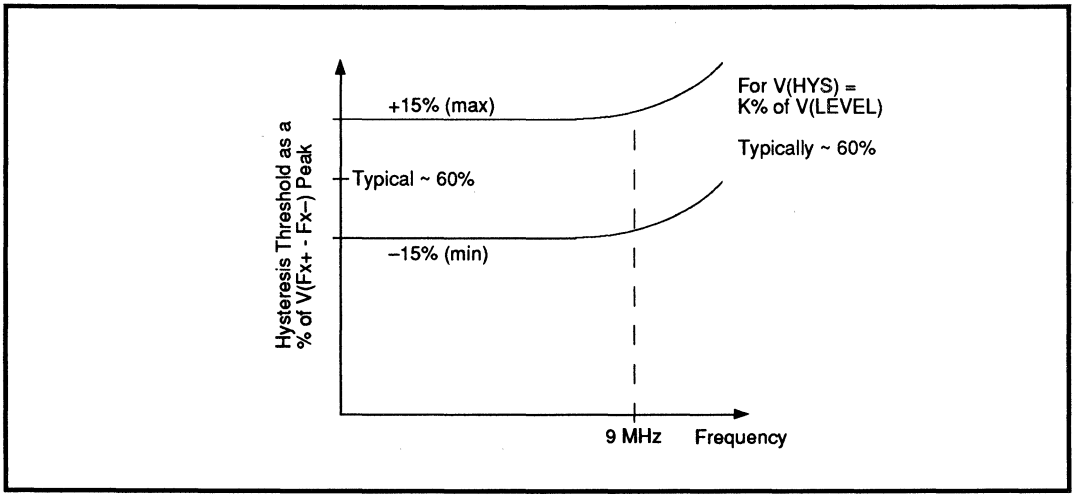


FIGURE 4: Percentage Threshold vs. Frequency

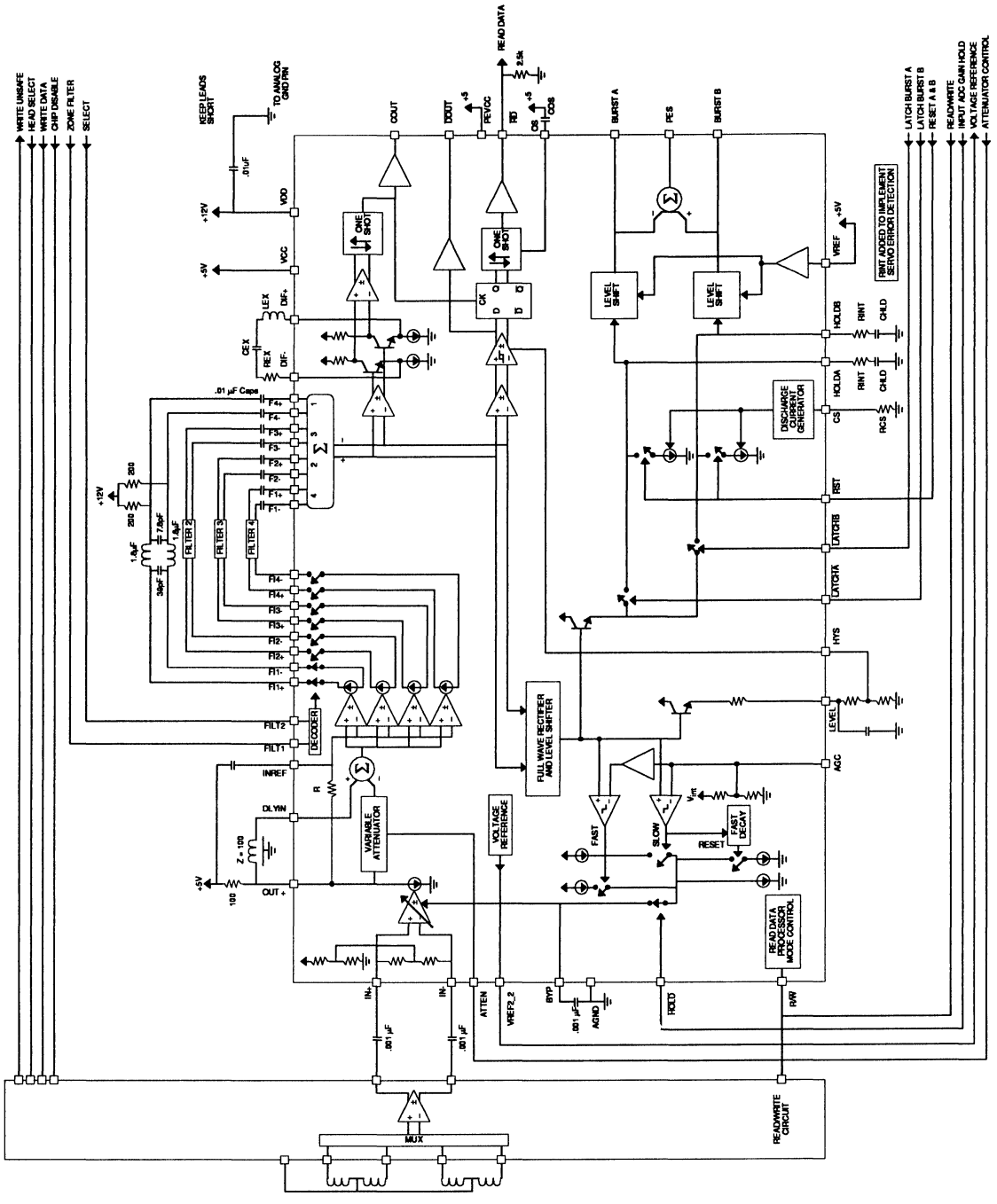


FIGURE 5: Applications Circuit Diagram

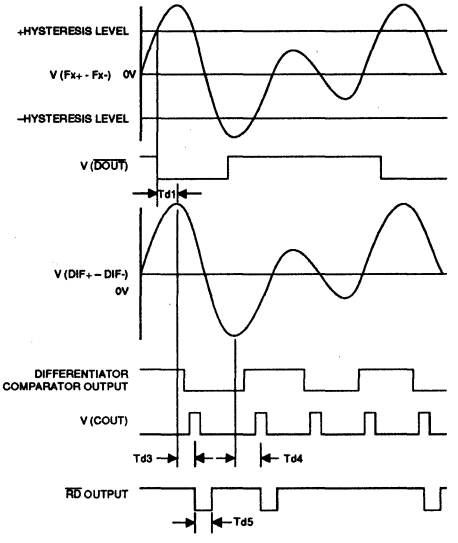


FIGURE 6: Read Mode Digital Section Timing Diagram

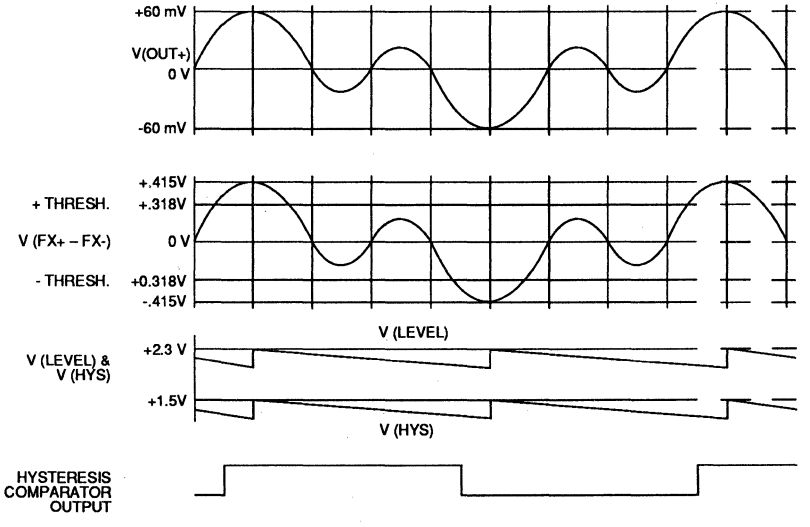
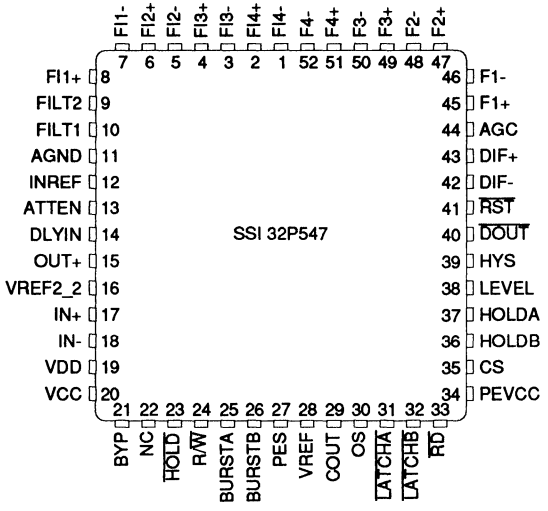


FIGURE 7: Expected Nominal Voltage Levels

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.

2



52-Pin Leaded Chip Carrier

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 731-7110, FAX (714) 573-6914

Notes:

silicon systems®
A TDK Group Company

SSI 32P549
Pulse Detector

December 1991

2

DESCRIPTION

The SSI 32P549 is a bipolar integrated circuit that provides all data processing necessary for detection and qualification of MFM or RLL encoded read signals.

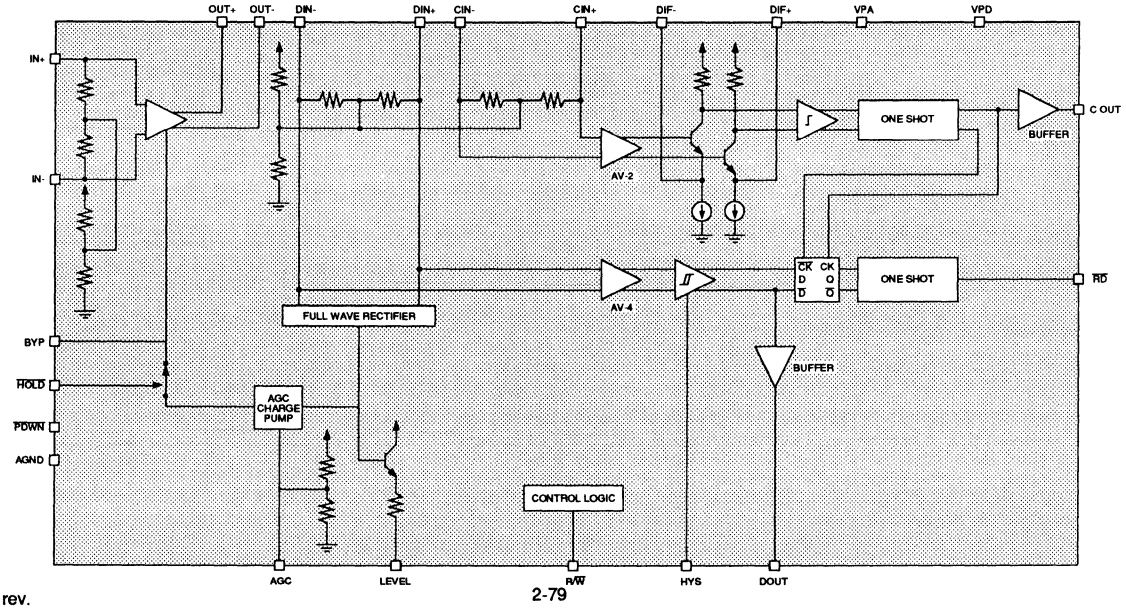
In read mode the SSI 32P549 provides amplification and qualification of head preamplifier outputs. Pulse qualification is accomplished using level qualification of differentiated input zero crossings. An AGC amplifier is used to compensate for variations in head preamp output levels, presenting a constant input level to the pulse qualification circuitry. The AGC loop can be disabled so that a constant gain can be used for embedded servo decoding or other processing needs.

In write mode the read data pulse circuitry is disabled, the AGC gain is held constant, and the AGC gain stage input impedance is switched to a lower level to allow fast settling of the input coupling capacitors during a write to read transition. The SSI 32P549 requires a +5V power supply and is available in a 28-pin PLCC, 24-pin DIP and 24-pin SOL.

FEATURES

- **Level qualification supports high resolution MFM and RLL encoded data retrieval**
- **Wide bandwidth AGC input amplifier**
- **Standard +5V ± 10% supplies**
- **Write to read transient suppression**
- **Fast and slow AGC attack regions for fast transient recovery**
- **≤ ±1.0 ns pulse pairing**
- **16 Mbit/s operation**

BLOCK DIAGRAM



CIRCUIT OPERATION

READ MODE

In read mode (R/$\overline{W}$ input high or open) the input signal is amplified and qualified using an AGC amplifier and pulse level qualification of the detected signal peaks.

An amplified head output signal is AC coupled to the IN+ and IN- pins of the AGC amplifier. Gain control is accomplished by full wave rectifying and amplifying the [(DIN+)-(DIN-)] voltage level and comparing it to a reference voltage level at the AGC pin.

The 32P549 contains a dual rate attack charge pump. The value of the attack current is dependent on the instantaneous level at DIN±. For signal levels above 125% of the desired level a fast attack mode is invoked that supplies a 1.4 mA charge current to the network on the BYP pin. Between 125% and 100% of the desired level the circuit enters a slow attack mode and supplies 0.18 mA of charge current to the BYP pin.

Two decay modes are available and are automatically controlled within the device.

Upon a switch to write mode, the device will hold the gain at its previous value and the AGC input stage is switched into a low impedance state. When the device is then switched back to read mode the AGC holds the gain and stays in the low impedance state for 0.9 µs. It then switches into a fast/slow attack mode if the new gain required is less than the previously held gain or a fast decay mode if the gain required is more than its previous value. The fast decay current is 0.12 mA and stays on for 0.9 µs. After the 0.9 µs time period the device stays in a steady state slow attack, slow decay mode. The slow decay discharge current is 4.5 µA.

The AGC pin is internally biased so that the target differential voltage input at DIN± is 1.0 Vpp under nominal conditions. The voltage on this pin can be modified by tying a resistor between AGC and GND or VPA. A resistor to GND decreases the voltage level, while a resistor to VPA increases it. The resulting AGC voltage level is shown in Figure 1; where:

V = Voltage at AGC w/pin open (2.3V, nom)

Rint = AGC pin input impedance (2.5 kΩ, typ)

Rext = External resistor

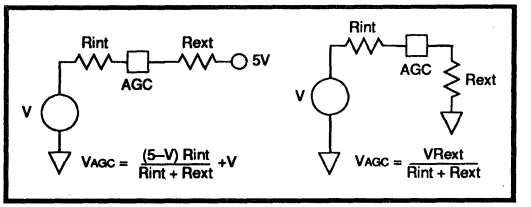


FIGURE 1: AGC Voltage

The new DIN ± input target level is nominally (V_{AGC} - 0.75) • 0.64 Vpp.

The maximum AGC amplifier output swing is 2.6 Vpp at OUT±, which allows for up to 6dB loss, with margin, in any external filter between OUT± and DIN±.

AGC gain is a linear function of the BYP-pin voltage (VBYP) as shown in Figure 2.

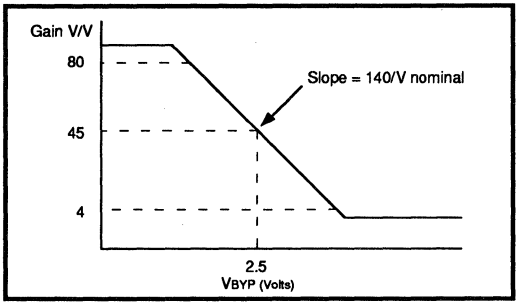


FIGURE 2: AGC Gain

The AGC amplifier has emitter follower outputs and can sink 3.5 mA.

One filter for both amplitude (DIN± input) and time (CIN± input) channels, or a separate filter for each may be used. If two filters are used, attention must be paid to time delays so that each channel is timed properly. A multi-pole Bessel filter is typically used for its linear phase or constant group delay characteristics.

In the amplitude channel the signal is sent to a hysteresis comparator. The hysteresis threshold level is set so that it will be tripped only by valid signal pulses and not by baseband noise. It can be a fixed level or a fraction of the DIN± voltage level.

The latter approach is accomplished by using an external filter/network between the LEVEL and HYS pins. This allows setting the AGC slow attack and decay times slow enough to minimize time channel distortion and setting a shorter time constant for the hysteresis level. The LEVEL pin output is a rectified and amplified version of DIN±, 1.0 Vpp at DIN± results in 1.0 Vo-p nominally, at the LEVEL pin. A voltage divider is used from LEVEL to ground to set the Hysteresis threshold at a percentage of the peak DIN± voltage. For example, if DIN± is 1.0 Vpp, then using an equal valued resistor divider will result in 0.5 Vpk at the HYS pin. This will result in a nominal ±0.18V threshold or a 36% threshold of a ±0.500V DIN± input. The capacitor, from the LEVEL pin to GND, is chosen to set an appropriate time constant. This "feed forward" technique speeds up transient recovery by allowing qualification of the input pulses while the AGC is still settling. This helps in the two critical areas of write to read and head change recovery. Some care in the selection of the hysteresis level time constant must be exercised so as to not miss pattern (resolution) induced lower amplitude signals. Note that there is a built-in 0.05V threshold (10% of 1Vpp) for level qualification even when the HYS pin is grounded. This is to prevent false triggering by baseband noise during a DC erase gap (e.g., address mark). The output of the hysteresis comparator is the "D" input of a D-type flip-flop. The DOUT pin is a comparator output signal for testing purposes only. When testing, it requires an external 3-6 kΩ pull down resistor. If no testing is necessary, the DOUT pin can be pulled up to VPD (+5V) to save power.

In the time channel the signal is differentiated to transform signal peaks to zero crossings which are detected and used to trigger a bi-directional one-shot. The one-shot output pulses are used as the clock input of the D flip-flop. The COUT pin provides the one-shot output for test purposes. It also requires an external 3-6 kΩ pull down resistor for testing.

The differentiator function is accomplished by an external network between the DIF+ and DIF- pins. The transfer function from CIN± to the comparator input (not DIF±) is:

$$Av = \frac{-2000Cs}{LCs^2 + C(R+92)s + 1}$$

where: C, L, R are external passive components
$20\ pF < C < 150\ pF$
$s = j\omega = j2\pi f$

During normal operation, the time channel clocks the D flip-flop on every positive and negative peak of the CIN± input. The D input to the flip-flop only changes state when the DIN± input exceeds the hysteresis comparator threshold opposite in polarity to the previous threshold exceeding peak.

The time channel, then, determines signal peak timing and the amplitude channel determines validity by blocking signal peaks that do not exceed the hysteresis comparator threshold. The delays in each of these channels to the D flip-flop inputs are well matched.

WRITE MODE

In Write Mode the SSI 32P549 Pulse Detector is disabled and preset for the following Read Mode. The digital circuitry is disabled, the input AGC amplifier gain is held at its previous value and the AGC amplifier input impedance is reduced.

Holding the AGC amplifier gain and reducing input impedance shortens system Write to Read recovery times.

The lowered input impedance improves settling time by reducing the time constant of the network between the SSI 32P549 and a head preamplifier such as the SSI 32R1200R. Write to read timing is controlled to maintain the reduced impedance for 0.9 µs before the AGC circuitry is activated. Coupling capacitors should be chosen with as low a value as possible consistent with adequate bandwidth to allow more rapid settling.

POWER DOWN MODE

A power down mode is provided to reduce power usage during the idle periods. Taking $\overline{PDWN}$ low causes the device to go into complete shutdown. When $\overline{PDWN}$ returns high, the device executes the normal Write to Read recovery sequence.

MODE CONTROL

The SSI 32P549 circuit mode is controlled by the $\overline{PDWN}$, $\overline{HOLD}$, and R/$\overline{W}$ pins as shown in Table 1.

R/$\overline{W}$	$\overline{HOLD}$	$\overline{PDWN}$	
1	1	1	Read Mode, AGC Active
1	0	1	Read Mode AGC gain held constant*
0	X	1	Write Mode AGC gain held constant* Input impedance reduced
X	X	0	Power Down - low current disabled mode

* AGC gain will drift at a rate determined by BYP capacitor and Hold mode leakage current.

TABLE 1: Mode Control

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
VPA	I	Analog (+5V) power supply for pulse detector
AGND	I	Analog ground pin for pulse detector block
VPD	I	Digital (+5V) power supply pin
DGND	I	Digital ground pin
IN+, IN–	I	Analog signal input pins
OUT+, OUT–	O	Read path AGC Amplifier output pins
DIN+, DIN–	I	Analog input to the hysteresis comparator
CIN+, CIN–	I	Analog input to the differentiator
DIF+, DIF–	I/O	Pins for external differentiating network
COUT	O	Test point for monitoring the flip-flop clock input
DOUT	O	Test point for monitoring the flip-flop D-input
$\overline{RD}$	O	TTL compatible read output
BYP	I/O	An AGC timing capacitor or network is tied between this pin and AGND1
AGC	I	Reference input voltage for the read data AGC loop
LEVEL	O	Output from fullwave rectifier that may be used for input to the hysteresis comparator
HYS	I	Hysteresis level setting input to the hysteresis comparator
$\overline{HOLD}$	I	TTL compatible pin that holds the AGC gain when pulled low
$\overline{PDWN}$	I	Low state on this pin puts the device in a low power "off" state
R/$\overline{W}$	I	Selects Read or Write mode

2

ELECTRICAL SPECIFICATIONS

Recommended conditions apply unless otherwise specified.

ABSOLUTE MAXIMUM RATINGS

Operation outside these rating limits may cause permanent damage to this device.

PARAMETER	RATING	UNIT
5V Supply Voltage, VPA, VPD	6.0	V
Pin Voltage (Analog pins)	-0.3 to VPA + 0.3	V
Pin Voltage (All others)	-0.3 to VPD + 0.3 or +12 mA	V
Storage Temperature	-65 to 150	°C
Lead Temperature (Soldering 10 sec.)	260	°C

RECOMMENDED OPERATING CONDITIONS

Currents flowing into the chip are positive.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Supply Voltage (VPA & VPD)		4.5	5.0	5.5	V
Junction Temperature, Tj		25		135	°C

POWER SUPPLY

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
IVPA IVPD	Supply Current	Outputs unloaded; $\overline{PDWN}$ = high or open		58	80	mA
Pd	Power dissipation	Ta = 25°C, outputs unloaded; $\overline{PDWN}$ = high		290	440	mW
		Outputs unloaded; $\overline{PDWN}$ = low		100	150	mW

LOGIC SIGNALS

VIL	Input Low Voltage		-0.3		0.8	V
VIH	Input High Voltage		2.0		VPA+0.3	V
IIL	Input Low Current	VIL = 0.4V	0.0		-0.4	mA
IIH	Input High Current	VIH = 2.4V			100	µA
VOL	Output Low Voltage	IOL = 4.0 mA			0.5	V
VOH	Output High Voltage	IOH = -400 µA	2.4			V

* Output load is a 4K resistor to 5V and a 10 pF capacitor to DGND.

ELECTRICAL SPECIFICATIONS (Continued)

MODE CONTROL

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Enable to/from $\overline{PDWN}$ Transition Time	Settling time of external capacitors not included, pin high to/from low			20	µs
Read to Write Transition Time	R/$\overline{W}$ pin high to low			1.0	µs
Write to Read Transition Time	R/$\overline{W}$ pin low to high AGC settling not included	0.4	0.9	1.6	µs
$\overline{HOLD}$ On to/from $\overline{HOLD}$ Off Transition Time	$\overline{HOLD}$ pin high to/from low			1.0	µs

READ MODE (R/$\overline{W}$ is high)

AGC AMPLIFIER

Unless otherwise specified, recommended operating conditions apply. Input signals are AC coupled to IN± and amplitude is between 25 mVpp & 250 mVpp differential. OUT± are loaded differentially with >800Ω, and each side is loaded with < 10 pF to AGND, and AC coupled to DIN±. A 2000 pF capacitor is connected between BYP and AGND. AGC pin is open.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Minimum Gain Range	1.0 Vpp ≤ (OUT+) - (OUT-) ≤ 2.6 Vpp	4		80	V/V
Output Offset Voltage	Over entire gain range	-400		+400	mV
Maximum Output Voltage Swing	Set by BYP pin THD ≤ 5%	2.6			Vpp
Differential Input Resistance	(IN+) - (IN-) = 100 mVpp @ 2.5 MHz	4	5.4	7.5	kΩ
Differential Input Capacitance	(IN+) - (IN-) = 100 mVpp @ 2.5 MHz		4	10	pF
Single Ended Input	R/$\overline{W}$ = high, IN+ or IN- pin	2	2.7	3.8	kΩ
Impedance (Each Side)	R/$\overline{W}$ = low, IN+ or IN- pin		160	250	Ω
Input Noise Voltage	Gain set to maximum		5	15	$nV\sqrt{Hz}$
Bandwidth	-3 dB bandwidth at maximum gain	30			MHz
OUT+ & OUT- Pin Current	No DC path to AGND	±2.5	±3.5		mA
CMRR (Input Referred)	(IN+) = (IN-) = 100 mVpp @ 5 MHz, gain set to max	40	65		dB
PSRR (Input Referred)	VPA, VPD = 100 mVpp @ 5 MHz, gain set to max	30			dB

AGC AMPLIFIER (Continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
(DIN+) - (DIN-) Input Swing vs. AGC Input (DIN+) - (DIN-) = (V_{AGC} - K1) • K2	25 mVpp ≤ (IN+) - (IN-) ≤ 250 mVpp, $\overline{HOLD}$ = high, 0.5 Vpp ≤ (DIN+) - (DIN-) ≤ 1.5 Vpp				
	K1	0.5	0.75	1.00	V
	K2	0.54	0.64	0.74	Vpp/V
(DIN+) - (DIN-) Input Voltage Swing Variation	25 mVpp ≤ (IN+) - (IN-) ≤ 250 mVpp			5	%
AGC Voltage	AGC open	1.8	2.3	2.7	V
AGC Pin Input Impedance		1.8	2.5	3.8	kΩ
Slow AGC Discharge Current	(DIN+) - (DIN-) = 0V, AGC pin open	2.8	4.5	6.5	µA
Fast AGC Discharge Current	Starts at 0.9 µs after R/$\overline{W}$ goes high, stops at 1.8 µs after R/$\overline{W}$ goes high		0.12		mA
AGC Leakage Current	$\overline{HOLD}$ = low, 10 ≤ AGC gain ≤80	-0.2		+0.2	µA
Slow AGC Charge Current	(DIN+) - (DIN-) = 0.563 VDC, AGC pin open	-0.11	-0.18	-0.27	mA
Fast AGC Charge Current	(DIN+) - (DIN-) = 0.8 VDC, AGC pin open	-0.9	-1.4	-2.1	mA
Fast to Slow Attack Switchover Point	$\frac{[(DIN+)-(DIN-)]}{[(DIN+)-(DIN-)]FINAL}$		125		%
Gain Decay Time (Td)	(IN+) - (IN-) = 250 mVpp to 125 mVpp @ 2.5 MHz, (OUT+) - (OUT-) to 90% final value	12	20	36	µs
	(IN+) - (IN-) = 50 mVpp to 25 mVpp @ 2.5 MHz (OUT+) - (OUT-) to 90% final value	38	60	110	µs
Gain Attack Time	R/$\overline{W}$ = low to high (IN+) - (IN-) = 250 mVpp @ 2.5 MHz, (OUT+) - (OUT-) to 110% final value	0.8	2	3.6	µs

WRITE MODE (R/$\overline{W}$ is low)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Single-ended Input Impedance (each side)	IN+ or IN-		160	250	Ω

HYSTERESIS COMPARATOR

Unless otherwise specified, recommended operating conditions apply. Input (DIN+) - (DIN-) is an AC coupled, 1.0 Vpp, 2.5 MHz sine wave. 0.5 VDC is applied to the HYS pin. R/$\overline{W}$ pin is high.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Input Signal Range				1.5	Vpp
Differential Input Resistance	(DIN+) - (DIN-) = 100 mVpp @ 2.5 MHz	8	10	14	kΩ
Differential Input Capacitance	(DIN+) - (DIN-) = 100 mVpp @ 2.5 MHz			5.0	pF
Single Ended Input Voltage at DIN± Impedance (Each Side)	DIN+ or DIN-	4	5	7	kΩ
Level Pin Output Voltage vs. (DIN+) - (DIN-)	0.6 Vpp < (DIN+) - (DIN-) < 1.5 Vpp, 10K between LEVEL and AGND		1		V/Vpp
Level Pin Output Impedance	I_{LEVEL} = 0.2 mA		250		Ω
Level pin Maximum Output Current		1.5			mA
Hysteresis Threshold Voltage at DIN± vs. HYS Pin Voltage	0.3 V < HYS < 1.0V	0.32	0.36	0.44	V/V
HYS Pin Current	0.3 V < HYS < 1.0V	0.0		-10	µA
DOUT Pin Output Low Voltage	5 kΩ from DOUT to DGND		VPD -2		V
DOUT Pin Output High Voltage	5 kΩ from DOUT to DGND		VPD -1.6		V

ACTIVE DIFFERENTIATOR

Unless otherwise specified, recommended operating conditions apply. Input (CIN+) - (CIN-) is an AC-coupled, 1.0 Vpp, 2.5 MHz sine wave. 100Ω in series with 65 pF are tied from DIF+ to DIF-.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Input Signal Range				1.5	Vpp
Differential Input Resistance	(CIN+) - (CIN-) = 100 mVpp @ 2.5 MHz	8	10	14	kΩ
Differential Input Capacitance	(CIN+) - (CIN-) = 100 mVpp @ 2.5 MHz			5.0	pF
Single Ended Input Impedance	CIN+ or CIN-	4	5	7	kΩ
Voltage Gain From CIN± to DIF±	(DIF+ to DIF-) = 2 kΩ		1		V/V
DIF+ to DIF- PIn Current	Differentiator impedance must be set so as to not clip the signal for this current level	±0.7			mA

ACTIVE DIFFERENTIATOR (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
COUT Pin Output Low Voltage	5 kΩ from COUT to DGND		VPD -2		V
COUT Pin Output High Voltage	5 kΩ from COUT to DGND		VPD -1.6		V
COUT Pin Output Pulse Width		22	35	55	ns

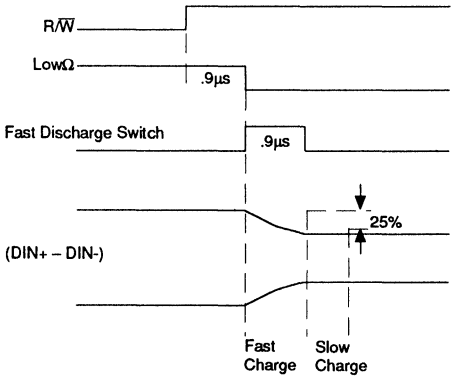


Figure A: AGC Attack Sequence

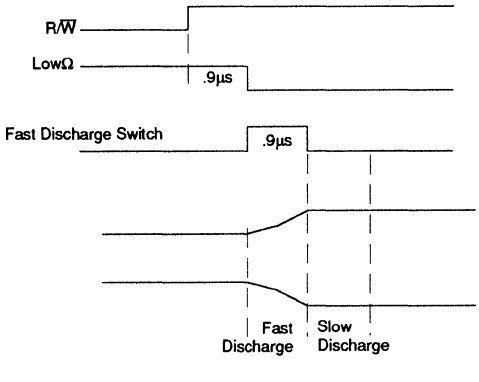


Figure B: AGC Decay Sequence

FIGURE 7: AGC Timing Diagram

QUALIFIER TIMING (See Figure 8)

Unless otherwise specified, recommended operating conditions apply. Inputs (CIN+) - (CIN-) and (DIN+) - (DIN-) are in-place as an AC coupled, 1.0 Vpp, 2.5 MHz sine wave. 100Ω in series with 65 pF are tied from DIF+ to DIF-. 0.5V is applied to the HYS pin. COUT and DOUT each have a 5 kΩ pull-down resistor (for test purposes only.) R/$\overline{W}$ pin is high.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Td1	D Flip-Flop Set Up Time	Minimum allowable time delay from (DIN+) - (DIN-) exceeding hysterisis point to (DIF+) - (DIF-) hitting a peak value.	0			ns
Td3	Propagation Delay			15		ns
Td3-Td4	Pulse Pairing	1.0 Vpp, 2.5 MHz sinewave			2	ns
Td3-Td4	Pulse Pairing	1.0 Vpp, 5 MHz sinewave			1	ns
Td5	$\overline{RD}$ Output Pulse Width		22	35	55	ns

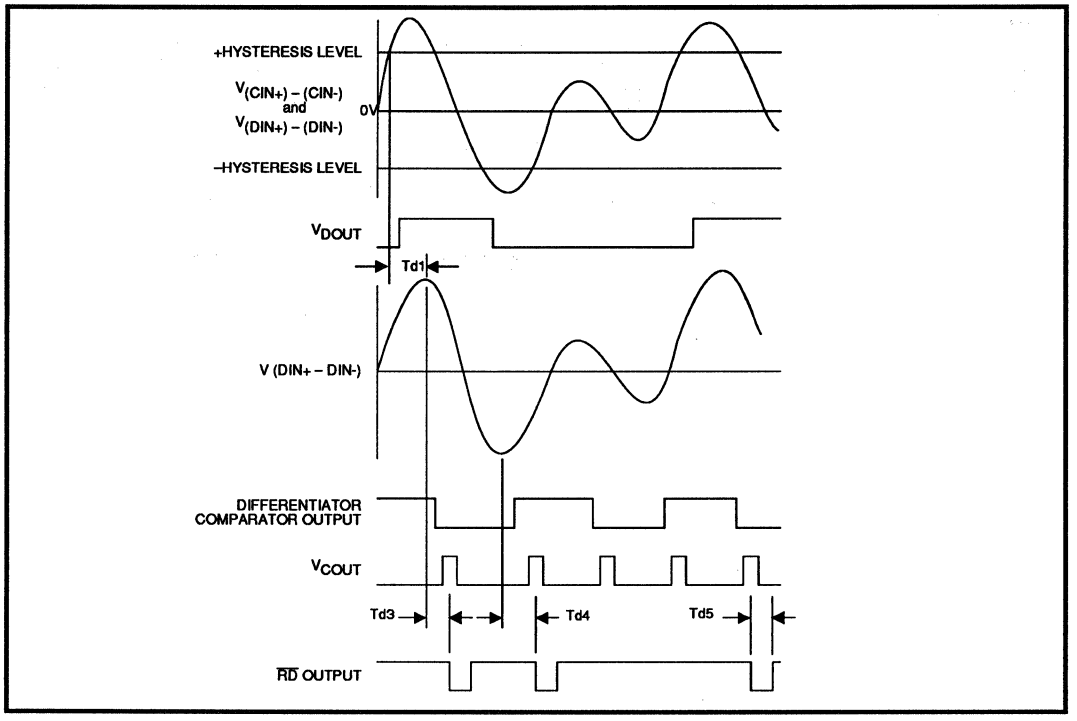
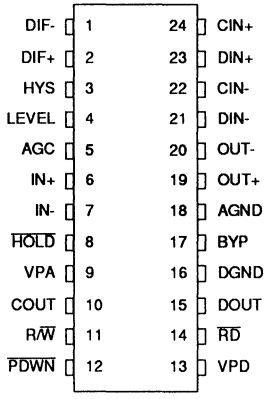


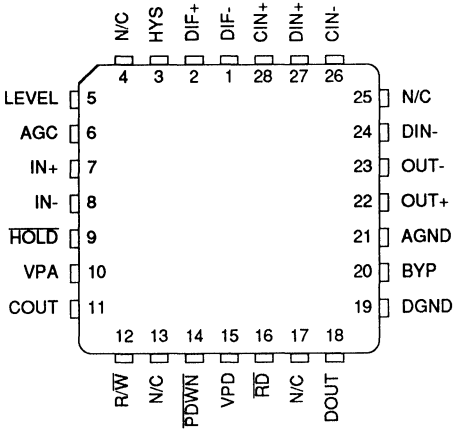
FIGURE 8: Read Mode Digital Section Timing Diagram

PACKAGE PIN DESIGNATIONS

(Top View)



24-Lead PDIP, SOL



28-Lead PLCC

THERMAL CHARACTERISTICS: θja

24-Lead PDIP	115°C/W
24-Lead SOL	80°C/W
28-Lead PLCC	65°C/W

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION	ORDERING NUMBER	PACKAGE MARK
SSI 32P549 Pulse Detector		
24-Pin PDIP	32P549-CP	32P549-CP
24-Pin SOL	32P549-CL	32P549-CL
28-Pin PLCC	32P549-CH	32P549-CH

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 731-7110, FAX (714) 573-6914

Notes:

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SSI 32P5491
Pulse Detector

Advance Information

December 1991

2

DESCRIPTION

The SSI 32P5491 is a bipolar integrated circuit that provides all data processing necessary for detection and qualification of MFM or RLL encoded read signals.

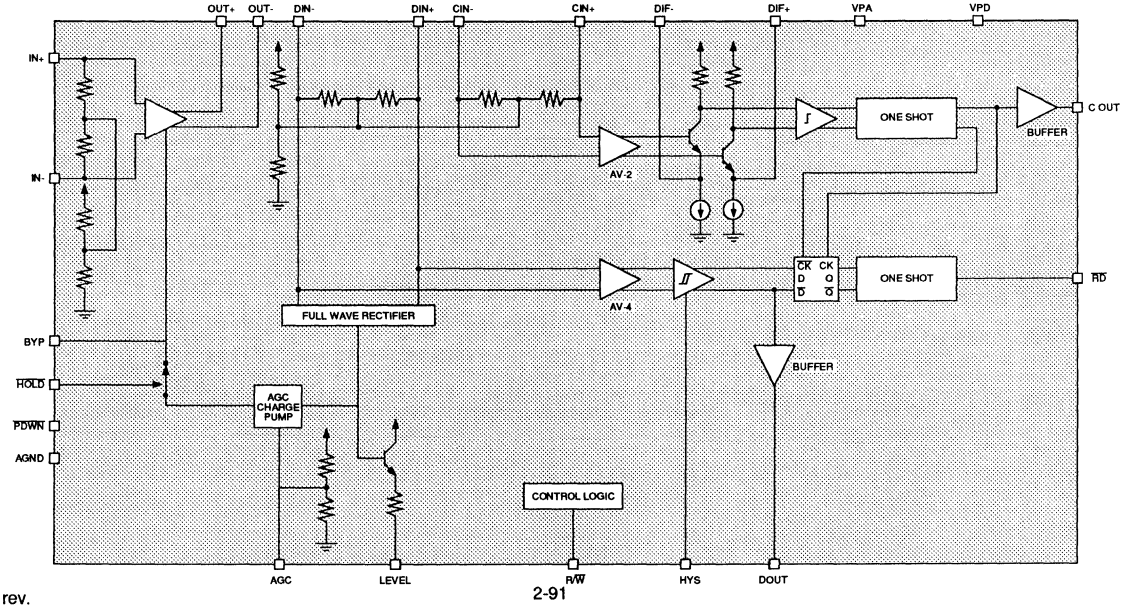
In read mode the SSI 32P5491 provides amplification and qualification of head preamplifier outputs. Pulse qualification is accomplished using level qualification of differentiated input zero crossings. An AGC amplifier is used to compensate for variations in head preamp output levels, presenting a constant input level to the pulse qualification circuitry. The AGC loop can be disabled so that a constant gain can be used for embedded servo decoding or other processing needs.

In write mode the circuitry is disabled and the AGC gain stage input impedance is switched to a lower level to allow fast settling of the input coupling capacitors during a write to read transition. The SSI 32P5491 requires a +5V power supply and is available in a 28-pin PLCC, 24-pin DIP and 24-pin SOL.

FEATURES

- **Level qualification supports high resolution MFM and RLL encoded data retrieval**
- **Wide bandwidth AGC input amplifier**
- **Standard +5V ± 10% supplies**
- **Write to read transient suppression**
- **Fast and slow AGC attack regions for fast transient recovery**
- **≤ ±1.0 ns pulse pairing**
- **24 Mbit/s operation**
- **Power down mode (5 mW maximum)**
- **Low power**

BLOCK DIAGRAM



CIRCUIT OPERATION

READ MODE

In read mode (R/$\overline{W}$ input high or open) the input signal is amplified and qualified using an AGC amplifier and pulse level qualification of the detected signal peaks.

An amplified head output signal is AC coupled to the IN+ and IN- pins of the AGC amplifier. Gain control is accomplished by full wave rectifying and amplifying the [(DIN+)-(DIN-)] voltage level and comparing it to a reference voltage level at the AGC pin.

The 32P5491 contains a dual rate attack charge pump. The value of the attack current is dependent on the instantaneous level at DIN±. For signal levels above 125% of the desired level a fast attack mode is invoked that supplies a 1.3 mA charge current to the network on the BYP pin. Between 125% and 100% of the desired level the circuit enters a slow attack mode and supplies 0.18 mA of charge current to the BYP pin.

Two decay modes are available and are automatically controlled within the device.

Upon a switch to write mode, the device will hold the gain at its previous value. When the device is then switched back to read mode the AGC holds the gain and stays in a low impedance state for 0.9 µs. It then switches into a fast/slow attack mode if the new gain required is less than the previously held gain or a fast decay mode if the gain required is more than its previous value. The fast decay current is 0.12 mA and stays on for 0.9 µs. After the 0.9 µs time period the device stays in a steady state slow attack, slow decay mode. The slow decay discharge current is 4.5 µA.

The AGC pin is internally biased so that the target differential voltage input at DIN± is 1.0 Vpp under nominal conditions. The voltage on this pin can be modified by tying a resistor between AGC and GND or VPA. A resistor to GND decreases the voltage level, while a resistor to VPA increases it. The resulting AGC voltage level is shown in Figure 1; where:

V = Voltage at AGC w/pin open (1V, nom)

Rint = AGC pin input impedance (3.91 kΩ, typ)

Rext = External resistor

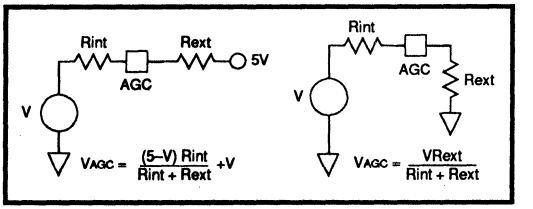


FIGURE 1: AGC Voltage

The new DIN ± input target level is nominally 1.0 Vpp/ VAGC.

The maximum AGC amplifier output swing is 3.0 Vpp at OUT±, which allows for up to 6dB loss in any external filter between OUT± and DIN±.

AGC gain is a linear function of the BYP-pin voltage (VBYP) as shown in Figure 2.

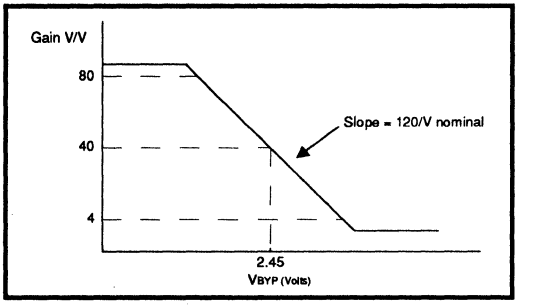


FIGURE 2: AGC Gain

In the amplitude channel the signal is sent to a hysteresis comparator. The hysteresis threshold level is set so that it will be tripped only by valid signal pulses and not by baseband noise. It can be a fixed level or a fraction of the DIN± voltage level.

The latter approach is accomplished by using an external filter/network between the LEVEL and HYS pins. This allows setting the AGC slow attack and decay times slow enough to minimize time channel distortion and setting a shorter time constant for the hysteresis level. The LEVEL pin output is a rectified and amplified version of DIN±, 1.0 Vpp at DIN± results in 1.0 Vo-p nominally, at the LEVEL pin. A voltage divider is used from LEVEL to ground to set the Hysteresis threshold at a percentage of the peak DIN± voltage. For example,

if DIN± is 1.0 Vpp, then using an equal valued resistor divider will result in 0.5 Vpk at the HYS pin. This will result in a nominal ±0.18V threshold or a 36% threshold of a ±0.500V DIN± input. The capacitor is chosen to set an appropriate time constant. This "feed forward" technique speeds up transient recovery by allowing qualification of the input pulses while the AGC is still settling. This helps in the two critical areas of write to read and head change recovery. Some care in the selection of the hysteresis level time constant must be exercised so as to not miss pattern (resolution) induced lower amplitude signals. The output of the hysteresis comparator is the "D" input of a D-type flip-flop. The DOUT pin is a comparator output signal for testing purposes only.

In the time channel the signal is differentiated to transform signal peaks to zero crossings which are detected and used to trigger a bi-directional one-shot. The one-shot output pulses are used as the clock input of the D flip-flop. The COUT pin provides the one-shot output for test purposes.

The differentiator function is accomplished by an external network between the DIF+ and DIF- pins. The transfer function from CIN± to the comparator input (not DIF±) is:

$$Av = \frac{-3536Cs}{LCs^2 + C(R+52)s + 1}$$

where: C, L, R are external passive components
$15\ pF < C < 125\ pF$
$s = j\omega = j2\pi f$

During normal operation, the time channel clocks the D flip-flop on every positive and negative peak of the CIN± input. The D input to the flip-flop only changes state when the DIN± input exceeds the hysteresis comparator threshold opposite in polarity to the previous threshold exceeding peak.

The time channel, then, determines signal peak timing and the amplitude channel determines validity by blocking signal peaks that do not exceed the hysteresis comparator threshold. The delays in each of these channels to the D flip-flop inputs are well matched.

WRITE MODE

In Write Mode the SSI 32P5491 Pulse Detector section is disabled and preset for the following Read Mode. The digital circuitry is disabled, the input AGC amplifier gain is held at its previous value and the AGC amplifier input impedance is reduced.

Holding the AGC amplifier gain and reducing input impedance shortens system Write to Read recovery times.

The lowered input impedance improves settling time by reducing the time constant of the network between the SSI 32P5491 and a head preamplifier such as the SSI 32R1200R. Write to read timing is controlled to maintain the reduced impedance for 0.9 µs before the AGC circuitry is activated. Coupling capacitors should be chosen with as low a value as possible consistent with adequate bandwidth to allow more rapid settling.

POWER DOWN MODE

A power down mode is provided to reduce power usage during the idle periods. Taking $\overline{PDWN}$ low causes the device to go into complete shutdown dissipating a maximum 5 mW of power. When $\overline{PDWN}$ returns high, the device executes the normal Write to Read recovery sequence.

MODE CONTROL

The SSI 32P5491 circuit mode is controlled by the $\overline{PDWN}$, $\overline{HOLD}$, and R/$\overline{W}$ pins as shown in Table 1.

R/$\overline{W}$	$\overline{HOLD}$	$\overline{PDWN}$	
1	1	1	Read Mode, AGC Active
1	0	1	Read Mode AGC gain held constant*
0	X	1	Write Mode AGC gain held constant* Input impedance reduced
X	X	0	Power Down - low current disabled mode

* AGC gain will drift at a rate determined by BYP and Hold mode discharge current.

TABLE 1: Mode Control

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
VPA	I	Analog (+5V) power supply for pulse detector
AGND	I	Analog ground pin for pulse detector block
VPD	I	Digital (+5V) power supply pin
DGND	I	Digital ground pin
IN+, IN–	I	Analog signal input pins
OUT+, OUT–	O	Read path AGC Amplifier output pins
DIN+, DIN–	I	Analog input to the hysteresis comparator
CIN+, CIN–	I	Analog input to the differentiator
DIF+, DIF–	I/O	Pins for external differentiating network
COUT	O	Test point for monitoring the flip-flop clock input
DOUT	O	Test point for monitoring the flip-flop D-input
$\overline{RD}$	O	TTL compatible read output
BYP	I/O	An AGC timing capacitor or network is tied between this pin and AGND1
AGC	I	Reference input voltage for the read data AGC loop
LEVEL	O	Output from fullwave rectifier that may be used for input to the hysteresis comparator
HYS	I	Hysteresis level setting input to the hysteresis comparator
$\overline{HOLD}$	I	TTL compatible pin that holds the AGC gain when pulled low
$\overline{PDWN}$	I	Low state on this pin puts the device in a low power "off" state
R/$\overline{W}$	I	Selects Read or Write mode

ELECTRICAL SPECIFICATIONS

Recommended conditions apply unless otherwise specified.

ABSOLUTE MAXIMUM RATINGS

Operation outside these rating limits may cause permanent damage to this device.

PARAMETER	RATING
5V Supply Voltage, VPA, VPD	6.0V
Pin Voltage (Analog pins)	-0.3 to VPA, + 0.3V
Pin Voltage (All others)	-0.3 to VPD + 0.3V or +12 mA
Storage Temperature	65 to 150°C
Lead Temperature (Soldering 10 sec.)	260°C

RECOMMENDED OPERATING CONDITIONS

Currents flowing into the chip are positive.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Supply Voltage (VPA & VPD)		4.75	5.0	5.25	V
Junction Temperature, Tj		25		135	°C
Ambient Temperature, Ta		0		70	°C

POWER SUPPLY

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
IVPA IVPD	Supply Current	Outputs unloaded; $\overline{PDWN}$ = high or open		34		mA
Pd	Power dissipation	Ta = 25°C, outputs unloaded		170		mW
		$\overline{PDWN}$ = low, Outputs unloaded		2	5	mW

LOGIC SIGNALS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VIL	Input Low Voltage		-0.3		0.8	V
VIH	Input High Voltage		2.0		VCC+0.3	V
IIL	Input Low Current	VIL = 0.4V	0.0		-0.4	mA
IIH	Input High Current	VIH = 2.4V			100	µA
VOL	Output Low Voltage	IOL = 4.0 mA			0.5	V
VOH	Output High Voltage	IOH = -400 µA	2.4			V

* Output load is a 4K resistor to 5V and a 10 pF capacitor to DGND.

MODE CONTROL

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Enable to/from $\overline{PDWN}$ Transition Time	Settling time of external capacitors not included, pin high to/from low		50		µs
Read to Write Transition Time	R/$\overline{W}$ pin high to low			1.0	µs
Write to Read Transition Time	R/$\overline{W}$ pin low to high AGC settling not included	0.5	0.9	1.3	µs
$\overline{HOLD}$ On to/from $\overline{HOLD}$ Off Transition Time	$\overline{HOLD}$ pin high to/from low			1.0	µs

READ MODE (R/$\overline{W}$ is high)

AGC AMPLIFIER

Unless otherwise specified, recommended operating conditions apply. Input signals are AC coupled to IN± and amplitude is between 25 mVpp & 250 mVpp differential. OUT± are loaded differentially with >600Ω, and each side is loaded with < 10 pF to AGND, and AC coupled to DIN±. A 2000 pF capacitor is connected between BYP and AGND. AGC pin is open.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Gain Range	1.0 Vpp ≤ (OUT+) - (OUT-) ≤ 3.0 Vpp	4		80	V/V
Output Offset Voltage	Over entire gain range	-200	0	+200	mV
Maximum Output Voltage Swing	Set by BYP pin THD ≤ 5%	3.0			Vpp
Differential Input Resistance	(IN+) - (IN-) = 100 mVpp @ 2.5 MHz		5.0		kΩ
Differential Input Capacitance	(IN+) - (IN-) = 100 mVpp @ 2.5 MHz			10	pF
Common Mode Input	R/$\overline{W}$ = high		1.8		kΩ
Impedance	R/$\overline{W}$ = low		250		Ω
Input Noise Voltage	Gain set to maximum			15	nV$\sqrt{Hz}$
Bandwidth	-3 dB bandwidth at maximum gain	32			MHz
OUT+ & OUT- Pin Current	No DC path to AGND		3		mA
CMRR (Input Referred)	(IN+) = (IN-) = 100 mVpp @ 2.5 MHz, gain set to max	40			dB
PSRR (Input Referred)	VPA1, 2 = 100 mVpp @ 2.5 MHz, gain set to max	30			dB

AGC AMPLIFIER (Continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
(DIN+) - (DIN-) Input Swing vs. AGC Input	25 mVpp ≤ (IN+) - (IN-) ≤ 250 mVpp, $\overline{HOLD}$ = high, 0.5 Vpp ≤ (DIN+) - (DIN-) ≤ 1.5 Vpp	0.9	1.0	1.1	Vpp/V
(DIN+) - (DIN-) Input Voltage Swing Variation	25 mVpp ≤ (IN+) - (IN-) ≤ 250 mVpp			6.0	%
AGC Voltage	AGC open	0.8	1.0	1.2	V
AGC Pin Input Impedance		4.4	5.5	6.6	kΩ
Slow AGC Discharge Current	(DIN+) - (DIN-) = 0V	4	4.5	6	µA
Fast AGC Discharge Current	Starts at 0.9 µs after R/$\overline{W}$ goes high, stops at 1.8 µs after R/$\overline{W}$ goes high	100	120	140	µA
AGC Leakage Current	$\overline{HOLD}$ = low	-0.2	0	+0.2	µA
Slow AGC Charge Current	(DIN+) - (DIN-) = 0.8 VDC, vary AGC until slow charge begins	-0.12	-0.18	-0.24	mA
Fast AGC Charge Current	(DIN+) - (DIN-) = 0.8 VDC, V_{AGC} = 3.0V	-0.9	-1.3	-1.7	mA
Fast to Slow Attack Switchover Point	$\frac{[(DIN+)-(DIN-)]}{[(DIN+)-(DIN-)]FINAL}$		125		%
Gain Decay Time (Td)	(IN+) - (IN-) = 250 mVpp to 125 mVpp @ 2.5 MHz, (OUT+) - (OUT-) to 90% final value		12		µs
	(IN+) - (IN-) = 50 mVpp to 25 mVpp at 2.5 MHz (OUT+) - (OUT-) to 90% final value		60		µs
Gain Attack Time	R/$\overline{W}$ = low to high (IN+) - (IN-) = 250 mVpp @ 2.5 MHz, (OUT+) - (OUT-) to 110% final value		2		µs

WRITE MODE (R/$\overline{W}$ is low)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Common Mode Input Impedance			250		Ω

HYSTERESIS COMPARATOR

Unless otherwise specified, recommended operating conditions apply. Input (DIN+) - (DIN-) is an AC coupled, 1.0 Vpp, 2.5 MHz sine wave. 0.5 VDC is applied to the HYS pin. R/$\overline{W}$ pin is high.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Input Signal Range		0.6	1.0	1.5	Vpp
Differential Input Resistance	(DIN+) - (DIN-) = 100 mVpp @ 2.5 MHz	12.5	15	17.5	kΩ
Differential Input Capacitance	(DIN+) - (DIN-) = 100 mVpp @ 2.5 MHz			5.0	pF
Common Mode Input Impedance (Both Sides)		3	4	5	kΩ
Level Pin Output Voltage vs. (DIN+) - (DIN-)	0.6 Vpp < (DIN+) - (DIN-) < 1.5 Vpp, 10K between LEVEL and AGND		1		V/Vpp
Level Pin Output Offset Voltage	10 kΩ between level and AGND		TBD		
Level Pin Output Impedance	I_{LEVEL} = 0.2 mA		250		Ω
Level pin Maximum Output Current		1.5			mA
Hysteresis Voltage at DIN± vs. HYS Pin Voltage	0.3 V < HYS < 1.0V		0.36		V/V
HYS Pin Input Current	0.5 V < HYS < 1.5V	0.0		-10	µA
Comparator Offset Voltage	HYS pin at AGND ≤ 1.5 kΩ across DIN±			5.0	mV
DOUT Pin Output Low Voltage	5 kΩ from DOUT to GND		VPA -2.8		V
DOUT Pin Output High Voltage	5 kΩ from DOUT to GND		VPA -2.4		V

ACTIVE DIFFERENTIATOR

Unless otherwise specified, recommended operating conditions apply. Input (CIN+) - (CIN-) is an AC-coupled, 1.0 Vpp, 2.5 MHz sine wave. 100Ω in series with 65 pF are tied from DIF+ to DIF-.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Input Signal Range		0.6	1.0	1.5	Vpp
Differential Input Resistance	(CIN+) - (CIN-) = 100 mVpp @ 2.5 MHz	12.5	15	17.5	kΩ
Differential Input Capacitance	(CIN+) - (CIN-) = 100 mVpp @ 2.5 MHz			5.0	pF
Common Mode Input Impedance	Both sides	3	4	5	kΩ
Voltage Gain From CIN± to DIF±	(DIF+ to DIF-) = 2 kΩ		1		V/V
DIF+ to DIF- PIn Current	Differentiator impedance must be set so as to not clip the signal for this current level	±0.7			mA
Comparator Offset Voltage	DIF+, DIF- are AC-coupled		0	5.0	mV
COUT Pin Output Low Voltage	5 kΩ from COUT to GND		VPA -2.8		V
COUT Pin Output High Voltage	5 kΩ from COUT to GND		VPA -2.4		V
COUT Pin Output Pulse Width			30		ns

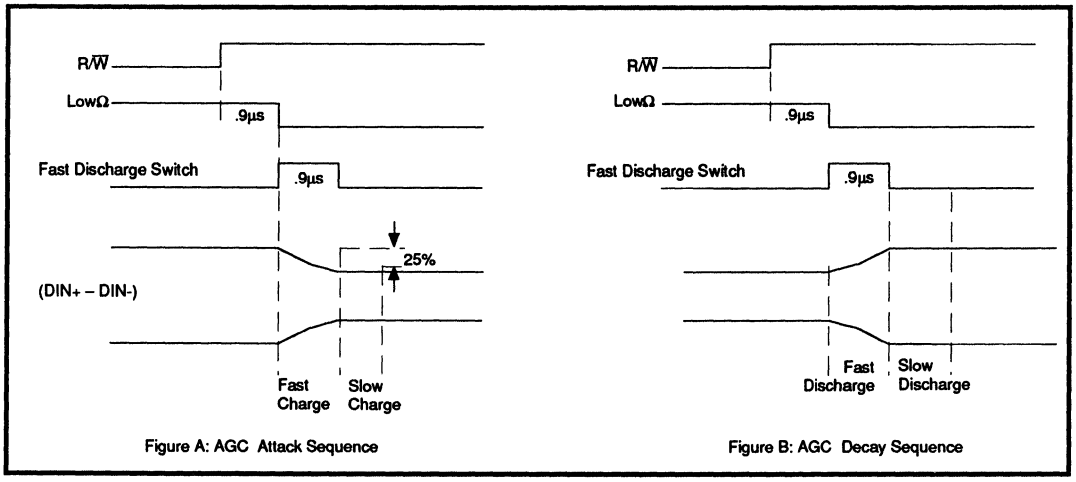


Figure A: AGC Attack Sequence

Figure B: AGC Decay Sequence

FIGURE 7: AGC Timing Diagram

QUALIFIER TIMING

Unless otherwise specified, recommended operating conditions apply. Inputs (CIN+) - (CIN-) and (DIN+) - (DIN-) are in-place as a coupled, 1.0 Vpp, 2.5 MHz sine wave. 100Ω in series with 65 pF are tied from DIF+ to DIF-. 0.5V is applied to the HYS pin. COUT and DOUT each have a 5 kΩ pull-down resistor (for test purposes only.) R/$\overline{W}$ pin is high.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Td1	D Flip-Flop Set Up Time	Minimum allowable time delay from (DIN+) - (DIN-) exceeding hysterisis point to (DIF+) - (DIF-) hitting a peak value.	0			ns
Td3	Propagation Delay	From positive peak to RD0* output pulse		TBD		ns
Td4	Propagation Delay	From negative peak to RD0* output pulse		TBD		ns
Td3-Td4	Pulse Pairing				1.0	ns
Td5	$\overline{RD}$ Output Pulse Width	RDW pin open	24	32	41	ns

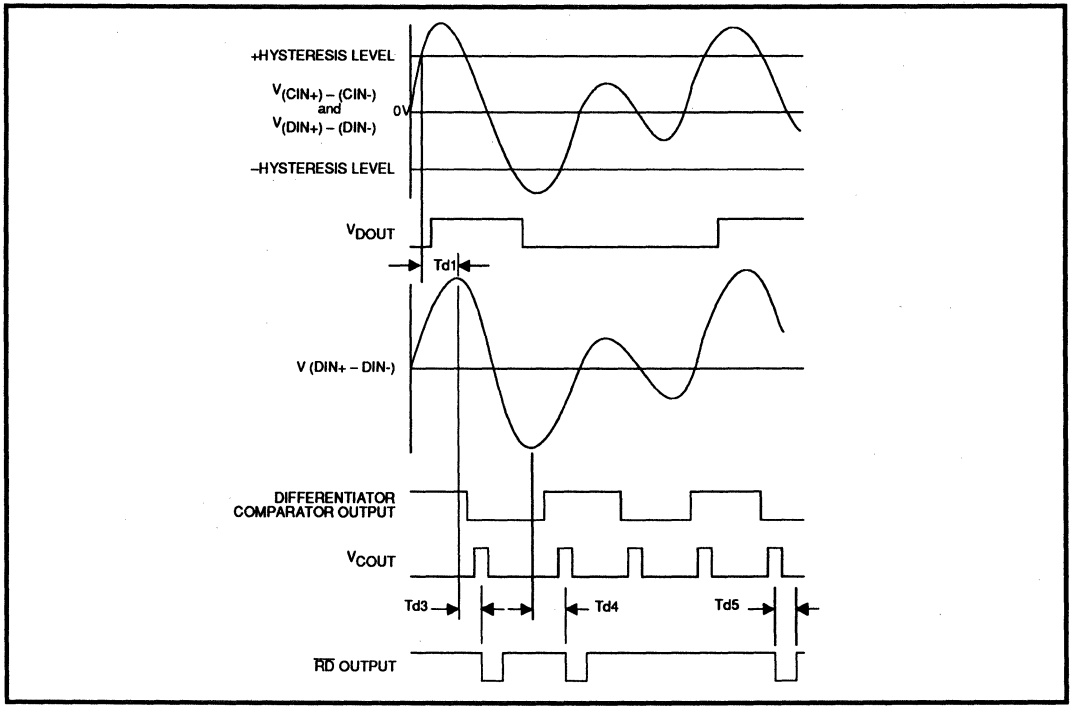
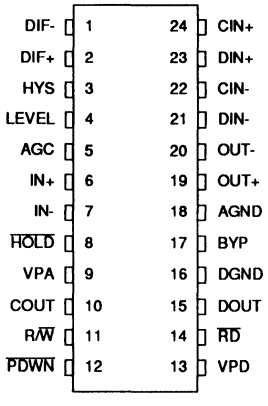


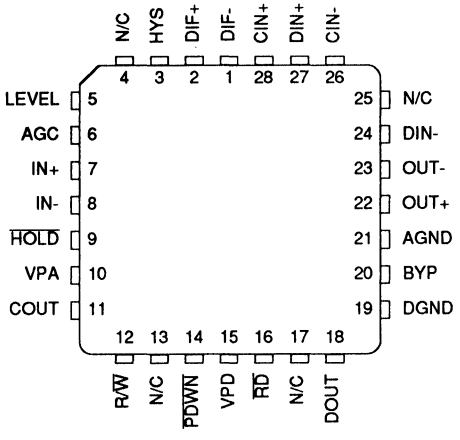
FIGURE 8: Read Mode Digital Section Timing Diagram

PACKAGE PIN DESIGNATIONS

(Top View)



24-Lead PDIP, SOL



28-Lead PLCC

THERMAL CHARACTERISTICS: θja

24-Lead PDIP	115°C/W
24-Lead SOL	80°C/W
28-Lead PLCC	65°C/W

CAUTION: Use handling procedures necessary for a static sensitive component.

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714) 731-7110, FAX: (714) 573-6914

Notes:

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SSI 32P3000
Pulse Detector with Programmable Filter
Preliminary Data

December 1991

2

DESCRIPTION

The SSI 32P3000 is a bipolar integrated circuit that provides all the data processing for detection and qualification of encoded read signals from a head preamplifier. This device can handle a NRZ data rate of 48 Mbit/s.

The SSI 32P3000 includes an AGC amplifier with AGC charge pump, a programmable 7-pole Bessel low pass filter, and a pulse qualification circuit. The device features a complete differential circuit architecture in the signal path, for high immunity to noise and power supply ripples.

For fast write-to-read recovery, the SSI 32P3000 allows the user to control the low input state and AGC fast recovery mode independently. The AGC action can also be disabled for embedded servo decoding or other processing needs.

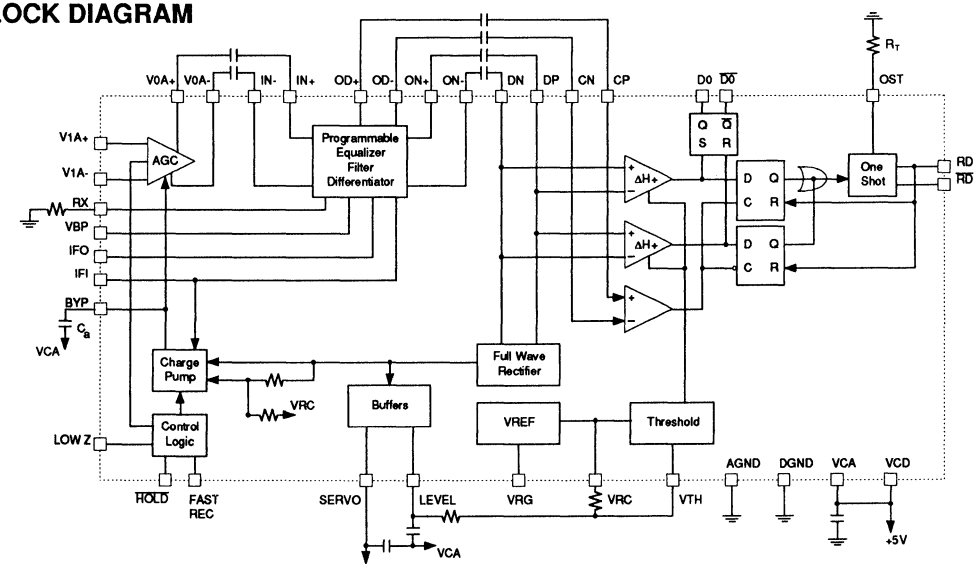
Ideal for constant density recording applications, the SSI 32P3000 low pass filter has a programmable 9 - 27 MHz bandwidth and 0 - 13 dB boost for pulse slimming. A time derivative of the read signal is also provided by the filter for time qualification in peak detection.

The SSI 32P3000 requires only a +5V power supply and is available in a 36-pin SOM package.

FEATURES

- Compatible with 48 Mbit/s data rate operation
- Fast attack/decay modes for rapid AGC recovery
- Low Drift AGC hold, fast AGC recovery, and low AGC input impedance control signals
- Includes programmable pulse slimming equalization and programmable channel filter and differentiator with no external filter components
- ±0.5 ns filter group delay variation from 0.3 FC to FC = 27 MHz
- Independent positive and negative threshold qualification to suppress error propagation
- 0.5 ns max pulse pairing
- +5V only operation
- 36-pin SOM package

BLOCK DIAGRAM



SSI 32P3000
Pulse Detector with Programmable Filter

FUNCTIONAL DESCRIPTION

The SSI 32P3000 Pulse Detector is designed to support a 48 Mbit/s NRZ data rate. The signal processing circuits include a wide band variable gain amplifier, a dual-rate AGC charge pump, a programmable electronic filter, and a pulse qualifier.

AGC Amplifier

The wide band AGC amplifier is to amplify the read signal from the read/write pre-amp to a signal level acceptable at the pulse qualifier. The AGC amplifier gain is an exponential function of the BYP voltage when referenced to VCA.

$$Av = Ao \exp[(\frac{V@BYP - Vr}{K})] \text{ (see note 1)}$$

AGC Actions

The AGC loop is to maintain a constant DP/DN signal at the nominal level, ~1Vppd. The AGC actions are current charging and discharging the external BYP integrating capacitor. These AGC actions can be classified into the following categories:

Automatic

Slow Decay

When the DP/DN signal is below the nominal level, a slow decay current, Id, charges the BYP capacitor. The AGC amplifier gain is increased slowly. This slow decay current tracks with the bandwidth of the filter. Id = 0.008 x IFI. At T = 27°C, the maximum Id is 4.5 µA when the filter cutoff frequency is 27 MHz.

Slow Attack

When the DP/DN signal exceeds the nominal level but is below 125% of the nominal level, a slow attack current, Ich, discharges the BYP capacitor. The AGC amplifier gain is decreased. The slow attack current is 40 times that of the slow decay current. Thus, for a given BYP capacitor, the slow attack response time is quicker than the slow decay response.

Note 1: In a closed AGC loop, the sensitivity of Ao, Vr and K to typical process variations is irrelevant. The typical values of Ao, Vr and K are provided for references only, and not tested in production. Ao = 11, Vr = 3.6 and K = 0.22

Fast Attack

When the DP/DN signal exceeds 125% of the nominal level, the device enters a fast attack mode. A fast attack current, Ichf, discharges the BYP capacitor. The AGC amplifier gain is quickly lowered. The fast attack current is seven times that of the slow attack current.

User Control

FAST REC

When FAST REC = 1, the SSI 32P3000 enters the fast recovery mode. Independent of the DP/DN signal level, a fast recovery current, Idf, charges the BYP capacitor. This fast recovery current magnitude is 20 times that of the slow decay current. The AGC amplifier gain is quickly raised. Meanwhile, all the above automatic AGC actions remain active.

$\overline{\text{HOLD}}$

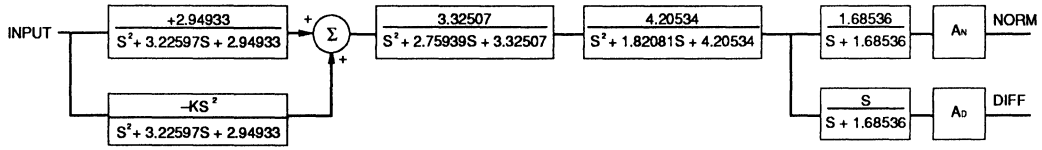
When HOLD = 0, all the automatic AGC actions and the fast recovery action are suspended. The BYP capacitor voltage remains constant, except for leakage effects.

Programmable Filter

The SSI 32P3000 includes a programmable low pass filter following the AGC amplifier for (1) 2X voltage gain from filter input to filter outputs, (2) noise limiting, (3) pulse slimming, and (4) provision of a time differentiated signal. The low pass filter is of a 7-pole 2-zero Bessel type. The filter's un-boosted -3 dB bandwidth, defined as the cutoff frequency, is programmable from 9 - 27 MHz; the high frequency equalization is programmable from 0 - 13 dB at the cutoff frequency.

The filter input is ac-coupled from the AGC amplifier output. The filter's normal low pass output is ac-coupled to the data channel of the pulse qualifier. The differentiated low pass output is ac-coupled to the time channel of the pulse qualifier.

The normalized 7-pole 2-zero Bessel filter transfer function is given as:



The cutoff frequency, fc, is programmable with 3 pins: RX, IFO and IFI. At the RX pin, an external resistor to ground establishes a reference current, IFO = 0.75 / Rx, at T = 27°C. IFI should be made proportional to IFO for fc temperature stability. The cutoff frequency is related to the RX resistor, IFO and IFI currents at the following:

$$fc(\text{MHz}) = 27 \cdot \frac{\text{IFI}}{\text{IFO}} \cdot \frac{1.25}{\text{RX}(k\Omega)}$$

For a fixed cutoff frequency setting, IFO and IFI can be tied together. The cutoff frequency equation then reduces to:

$$fc(\text{MHz}) = 27 \cdot \frac{1.25}{\text{RX}(k\Omega)}$$

For programmable cutoff frequency, an external current DAC can be used. IFO should be the reference current into the DAC. The DAC output current drives IFI, which is then proportional to IFO. The DACF in the SSI 32D4661 Time Base Generator is designed to control fc of the Silicon Systems programmable filters. When the DACF, which has a 4X current gain from its reference to fullscale output, is used, 5 kΩ RX is used. The fc is then given by:

$$fc(\text{MHz}) = 27 \cdot \frac{\text{F\_Code}}{127}$$

where F_Code is a decimal code equivalent to the 7-bit input into the DACF.

The high frequency equalization is programmable with two pins: VRG and VBP. The VRG is a bandgap reference voltage, 2.2 V typically. The voltage at the VBP pin determines the amount of high frequency boost at the cutoff frequency. The boost function is as the following:

$$\text{Boost(dB)} = 20\log_{10}\left[\left(3.47 \cdot \frac{\text{VBP}}{\text{VRG}}\right) + 1\right]$$

For a fixed boost setting, a resistor divider between VRG and ground can be used with the divided voltage at the VBP pin. For programmable equalization, an external voltage DAC can be used. VRG should be the reference voltage to the DAC. The DAC output voltage is then proportional to VRG. The DACS in the SSI 32D4661 is designed to control the magnitude equalization of Silicon Systems' programmable filters. When DACS is used, the boost relation then reduces to:

$$\text{Boost(dB)} = 20\log_{10}\left[\left(\frac{3.47 \cdot \text{S\_Code}}{127}\right) + 1\right]$$

Pulse Qualification

The SSI 32P3000 validates each DP/DN peak by combination of level qualification and time qualification. In level qualification, a dual-comparator threshold detection eliminates errors due to low level additive noise. In time qualification, the filter's differentiated output is used to locate signal peaks.

Level Qualification

The dual-comparator architecture allows independent detection for positive and negative peaks. One comparator detects a positive peak by comparing the data signal with a positive threshold. The other comparator detects a negative peak by comparing the data signal with a negative threshold. Each comparator has a small hysteresis, 20% of the set threshold, to avoid false triggering by noise around the set threshold.

The SSI 32P3000 allows two ways of setting the thresholds: fixed threshold or DP/DN tracking threshold. Fixed threshold can be simply set by a DC voltage at the VTH pin, such as from a resistor divider from VCA to VRC (see note 2). The threshold at each comparator can be computed as: Hysteresis Gain • (VTH - VRC). The thresholds at the two comparators are of the same magnitude, but of opposite polarity. For high performance system application, however, fixed threshold is not recommended.

Note 2: VCA is the +5V supply. VRC is the bandgap voltage referenced from VCA, i.e., VRC = VCA - VRG.

DP/DN tracking threshold has the advantages of shorter write-to-read recovery time and lower probability of error with input amplitude drop out. The threshold is designed as a percentage of the DP/DN peak voltage. This technique can be implemented by feeding the LEVEL output, through a resistor divider network, to the VTH pin. The LEVEL output, amplified peak capture of DP/DN signal, can be computed as: Level Gain • DP/DN ppd + VRC. With the resistor divider, a fraction of the LEVEL output is presented at the VTH pin. The threshold, as a function of DP/DN, can be summarized as Level Gain • Resistor Dividing Ratio • Hysteresis Gain • DP/DN ppd. For a typical case of 1 Vppd DIN signal, assume equal value resistors in the divider network, the threshold is 0.75 • 0.5 • 0.445 • 1.0 = 0.17 V. This represents 34% threshold on a 1 Vppd signal. While both the Level Gain and Hysteresis Gain bear a moderate tolerance due to typical process variation, they inversely track each other to yield a much tighter threshold accuracy in a closed loop.

While the external resistor divider ratio determines the qualification setting, the total resistance and the peak capture capacitor should be optimized for the system data rate. The RC time constant must be small enough to allow good response to changing DP/DN peak, but large enough to provide a constant threshold after a long duration of input absence.

The Pulse Qualifier output is the pseudo-ECL differential output, RD and $\overline{RD}$. Corresponding to each validated peak of the DP/DN signal, a one-shot pulse occurs at the RD/$\overline{RD}$ output. The pulse width of the one-shot pulse is determined by an external resistor from the OST pin to ground.

$$\text{Pulse Width(sec)} = 0.174 \cdot (R_{OST} - 340) \cdot (22\text{pF} + C_s)$$

$$R_{OST} = 3\text{k}\Omega \text{ to } 10\text{k}\Omega, C_s = \text{stray capacitance}$$

DO and $\overline{DO}$ form the differential output as test points to examine the output of the two comparators. Each is an open-emitter output requiring an 5 kΩ external resistor pull-down to ground.

PIN DESCRIPTION

INPUT PINS

NAME	TYPE	DESCRIPTION
VIA+, VIA-	I	AGC Amplifier input pins.
IN+, IN-	I	Equalizer/filter input pins.
DP, DN	I	Data inputs to data comparators and fullwave rectifier.
CP, CN	I	Differentiated data inputs to the clock comparator.
VTH	I	Threshold level setting input for the data comparators.
FAST REC	I	TTL compatible input when high puts the charge pump in the fast decay mode.
LOW Z	I	TTL compatible input when high reduces the AGC amplifier input resistance.
$\overline{HOLD}$	I	TTL compatible input when low disables the AGC action by turning off the charge pump.

PIN DESCRIPTION (continued)

OUTPUT PINS

NAME	TYPE	DESCRIPTION
VOA+, VOA-	O	AGC amplifier output pins.
ON+, ON-	O	Equalizer/filter normal output pins.
OD+, OD-	O	Equalizer/filter differentiated output pins.
DO+, DO-	O	ECL compatible data comparator latch output pins.
RD+, RD-	O	ECL compatible read data output pins.
LEVEL	O	Open NPN emitter output that provides a fullwave rectified signal for the VTH input. The signal is referenced to VRC.
SERVO	O	Open NPN emitter output that provides a fullwave rectified servo signal. The signal is referenced to VRC.
ANALOG PINS		
OST	-	Pin for R_T network to set RD output pulse width. An internal 22 pF capacitor has been included.
VRC	-	Reference voltage pin for SERVO and LEVEL. VRC is referenced to VCA.
VRG	-	Reference voltage pin for the programmable filter. VRG is referenced to ground.
VBP	-	The equalizer high frequency boost is set by an external voltage applied to this pin. VBP must be proportional to VRG. Programmable boost is implemented by using a DAC that uses VRG as its reference. A fixed amount of boost can be set by an external resistor divide network connected from VBP to VRG and GND.
RX	-	Pin to set filter reference current. External resistor Rx from this pin to ground sets the filter reference current IFO.
IFO	-	Reference current output pin. The reference current is normally supplied as the reference current to a current DAC which generates the programmable input current for the IFI pin.
IFI	-	Programmable filter input current pin. The filter cutoff frequency is proportional to the current into this pin. The current must be proportional to the reference current out of IFO. A fixed filter cutoff frequency is generated by connecting IFO to IFI and selecting Rx to set the desired frequency.
AGC	-	Optional reference voltage input for the AGC. The reference voltage is normally set by an internal resistor divider for VCC to VRC. (Not available in 36 pin SO package).
BYP	-	The AGC integrating capacitor C_A is connected between BYP and VCA.
VCA, VCD	-	Analog and Digital +5V.
AGND1, DGND	-	Analog and Digital grounds.

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, 4.5<VCC<5.5, 0°C<Ta<70°C

ABSOLUTE MAXIMUM RATINGS (Operation above maximum ratings may damage the device.)

PARAMETER	VALUE
Storage Temperature	-65 to +150°C
Junction Operating Temperature,Tj	+130°C
Supply Voltage, VCA, VCD	-0.3 to 7V
Voltage Applied to Inputs	-0.3 to VCA, VCD + 0.3V

RECOMMENDED OPERATING CONDITIONS

PARAMETER		RATING	UNIT
Supply Voltage	VCA = VCD = VCC	4.5 < VCC < 5.5	V
Ambient Temperature, Ta		0<Ta<70	°C

POWER SUPPLY

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
ISS	Supply Current			82		mA
PD	Power Dissipation			410	TBD	mW

LOGIC SIGNALS

VIL	TTL Input Low Voltage		-0.3		0.8	V
VIH	TTL Input High Voltage		2.0		VCC +0.3	V
IIL	TTL Input Low Current	VIL = 0.4V			-0.4	mA
IIH	TTL Input High Current	VIH = 2.7V			0.1	mA
VOHE	EECL Output High Voltage	VCC = 5V	VCC -1.02			V
VES	ECL Differential Output Swing |VRD - $\overline{VRD}$|	VCC = 5V	0.6			V
TRF	ECL Output Rise and Fall Time	CL = 10 pF			3.5	ns
TCS	Control Input Switching Times				0.1	µs

AGC AMPLIFIER

The input signals are AC coupled to VIA+ and VIA-. VOA+ and VOA- are AC coupled to IN+ and IN-. ON+ and ON- are AC coupled to DP and DN. Ca 1000 pF. Fin = 4 MHz. Unless otherwise specified, the output is measured differentially at VOA+ and VOA-.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VIR	Input Range	Filter boost at Fc = 0 dB	24		240	mVppd
		Filter boost at Fc = 11 dB	20		100	mVppd
VD	DP-DN voltage	VIA± = 0.1 Vppd			1.05	Vppd
VDV	DP-DN Voltage Variation	24 mV < VIA± < 240 mV			8.0	%
AV	Gain Range		1.9		22	V/V
AVPV	Gain Sensitivity			38		dB/V
DR	VOA± Dynamic Range	THD = 1% max	.75			Vpp
RINDA	Differential Input Impedance	LOW Z = low	3.7		7.4	kΩ
RINSA	Single Ended Input Impedance	LOW Z = low		1.4		kΩ
		LOW Z = high		175		Ω
VOS	Output Offset Voltage Variation	from min gain to max gain	-200		+200	mV
VIN	Input Referred Noise Voltage	gain = max, Rs = 0Ω filter not connected to VOA+, VOA-			20	$nV\sqrt{Hz}$
BW	Bandwidth	No AGC action	55			MHz
CMRR	Common Mode Rejection Ratio	gain = max, f = 5 MHz	40			dB
PSRR	Power Supply Rejection Ratio	gain = max, f = 5 MHz	45			dB
GDT	Gain Decay Time	VIA+ VIA- = 240 mV to 120 mV VOA+ VOA- <0.9 Final Value		32		µs
GAT	Gain Attack Time	VIA+ VIA- = 120 mV to 240 mV VOA+ VOA- <1.1 Final Value		2		µs

ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise specified, 4.5<VCC<5.5, 0°C<Ta<70°C

AGC CONTROL

The input signals are AC coupled to DP and DN. Ca = 1000 pF, LEVEL and SERVO load = 100 µA.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VDI	DP-DN Signal Input Range				1.4	Vpp
ID	Discharge Current, Id	FAST REC = low DP - DN = 0		0.008 x IFI		mA
IDF	Fast Discharge Current, Idf	FAST REC = high		20 x Id		mA
ICH	Charge Pump Attack Current, Ich	DP - DN = 0.55V		40 x Id		mA
ICHF	Charge Pump Fast Attack Current, Ichf	DP-DN = 0.675V		7 x Ich		mA
IK	BYP Pin Leakage Current	$\overline{HOLD}$ = low, VBYP = 3.5V	-0.1		0.1	µA
VRG	Reference Voltage	I source = 0 to 1 mA	2.2		2.45	V
VRC	Reference Voltage			VCC-VRG		V
IVRC	VRC Output Drive		-0.75		0.75	mA

EQUALIZER/FILTER The input signals are AC coupled to IN+ and IN-.

FC	Filter Cutoff Frequency	RX = 5kΩ fc = 27 x IFI/(4 x IFO) MHz 4 ≥ IFI/IFO ≥ 4/3	9		27	MHz
IFO	IFO Reference Current Range	IFO = 0.75/RX; Tj = 27°C 5kΩ > RX > 1.25 kΩ	0.15		0.6	mA
IFI	IFI Program Current Range	Tj = 27°C, 27 MHz > fc > 9 MHz	0.2		0.6	mA
FCA	FCA Filter FC Accuracy	fc nominal = 27 MHz	-10		10	%
RX	RX Range		1.25		5	kΩ
AO	Normal Low Pass Gain AO = (ON ±) / (IN±)	Fin = 0.67fc	1.4		2.2	V/V
AD	Differentiated Low Pass Gain AD = (ON ±) / (IN±)	Fin = 0.67fc	0.8AO		1.2AO	V/V
FB	Frequency Boost at fc	FB = 20log [3.47 (VBP/VR) + 1]	0		13	dB
FBA	Frequency Boost Accuracy	FB nominal = 13 dB	-1.5		+1.5	dB
TGD1	Group Delay Variation	fc = 27 MHz, FB = 0 to 9 dB fc > Fin > 0.3fc	-0.5		+0.5	ns

EQUALIZER/FILTER (continued)

The input signals are AC coupled to IN+ and IN-.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TGD2		*fc* = 9 to 27 MHz *fc* > Fin > 0.3 *fc*	-2.5		+2.5	%
VOSF	Output Offset Voltage				200	mV
DRF	VOF Filter Output Dynamic Range	THD = 1.5% max Fin = 0.67 *fc*	1.2			Vpp
RINF	Filter Input Resistance		3.0			kΩ
CINF	Filter Input Capacitance				7	pF
ROF	Filter Output Resistance	IO = 1 mA			60	Ω
VNN	Eout Output Noise Voltage; ON+, ON-	BW = 100 MHz, RS = 50Ω VBP = 0, *fc* = 27 MHz		2.7		mVRms
		BW = 100 MHz, RS = 50Ω VBP = VRG, *fc* = 27 MHz		5.7		mVRms
VND	Eout Output Noise Voltage; OD+, OD-	BW = 100 MHz, RS = 50Ω VBP = 0, *fc* = 27 MHz		5.7		mVRms
		BW = 100 MHz, RS = 50Ω VBP = VRG, *fc* = 27 MHz		13.0		mVRms

DATA COMPARATOR

The input signals are AC coupled to DP and DN.

VID	DP-DN Signal Range				1.5	Vpp
RIND	Differential Input Resistance		8		14	kΩ
CIND	Differential Input Capacitance				5	pF
VOSD	Comparator Offset Voltage (Note 1)				4	mV
LG	Level (Servo) Output Gain	DP-DN = .5 to 1 Vpp	.712		.788	V/Vpp
LBW	Level (Servo) Output Bandwidth	1 dB	20			MHz
VLOS	Level Offset Voltage	Output-VRC, IL = 50 µA			±30	mV
VSOS	Servo Offset Voltage	Output - VRC, IL = 100 µA			±30	mV
GHYS	Threshold Voltage Gain, Kth	0.3 < VTH-VRC < 0.9	.41	0.445	.48	V/V
VSH	Threshold Voltage Hysteresis			.20 x GHYS x (VTH - VRC)		V/V

Note 1: Not directly measurable

DATA COMPARATOR (continued)

The input signals are AC coupled to DP and DN.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VHM	Minimum Threshold Voltage	VTH-VRC ≤ 0.11V		.05		V
TPDD	Propagation Delay	From DP/DN to DO, $\overline{DO}$		6		ns
IVTH	Input Bias Current				2	µA

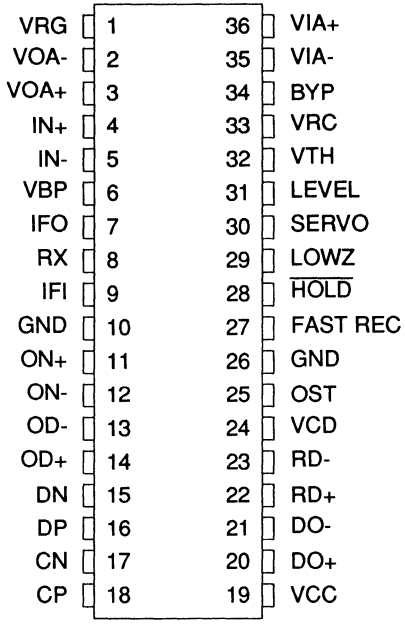
CLOCKING

The input signals are AC coupled to CP and CN.

VC	CP-CN Signal Range				1.5	Vpp
VOSC	Comparator Offset Voltage				4	mV
RINC	Differential Input Resistance		8		14	kΩ
CINC	Differential Input Capacitance				5	pF
TDS	D F/F Set Up Time	DP-DN threshold to CP-CN zero cross	0			ns
PP	Pulse Pairing	Vs = 1Vpp, F = 18 MHz			0.5	ns
TPDC	Propagation Delay to RD	Vs = 20 mVpp sq wave		9		ns
PWRD	RD Output Pulse Width	Tpd =.174 (Rt-340)(22pf + Cs) Rt = 3K to 10K, Cs = stray	.82x Tpd		1.18x Tpd	ns
RT	Resistor Range		3		10	kΩ

PIN DIAGRAM

(Top View)



32P3000-CM
36-Pin SOM

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32P3000 36-Pin Small Outline (31.6 mil. pitch)	32P3000-CM	32P3000-CM

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 731-7110, FAX (714) 573-6914

Notes:

silicon systems®
A TDK Group Company

SSI 32P3010
Pulse Detector with Programmable Filter
Advance Information

December 1991

2

DESCRIPTION

The SSI 32P3010 is a bipolar integrated circuit that provides all the data processing for pulse detection and four-burst servo capture from encoded read signals. This device can handle a NRZ data rate of 48 Mbit/s.

The SSI 32P3010 includes an AGC amplifier with AGC charge pump, a programmable 7-pole Bessel low pass filter, a pulse qualification circuit, and a 4-burst servo capture circuit. Automatic AGC control maintains a constant signal level into the pulse qualifier, and achieves fast write-to-read recovery. A time differentiator is included in the servo signal path, if so needed.

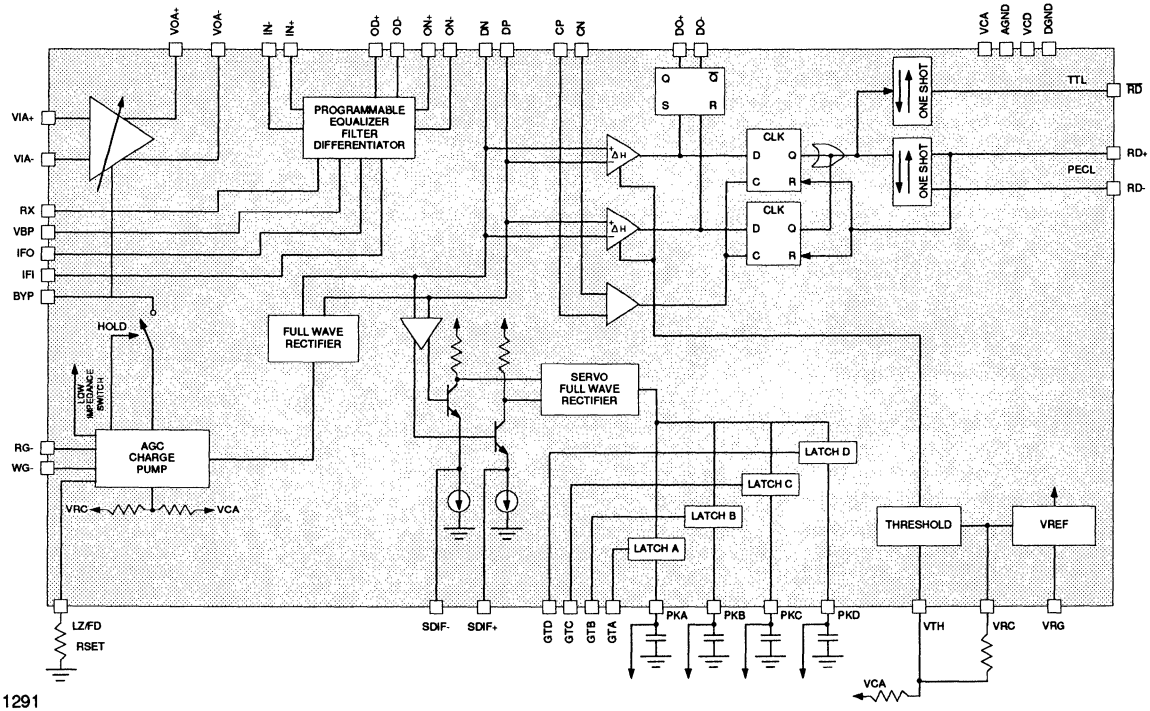
Ideal for constant density recording applications, the SSI 32P3010 low pass filter has a programmable 9-27 MHz bandwidth and 0-13 dB boost for pulse slimming. A time derivative of the read signal is also provided by the filter for time qualification in peak detection.

The SSI 32P3010 requires only a +5V power supply and is available in a 44-pin SOM package.

FEATURES

- Compatible with 48 Mbit/s data rate operation
- Fast attack/decay modes for rapid AGC recovery
- Automatic AGC actions: Low Drift AGC hold, fast AGC recovery, and low AGC input impedance control signals
- Includes programmable pulse slimming equalization and programmable channel filter and differentiator with no external filter components
- ±0.5 ns filter group delay variation from 0.3FC to FC = 27 MHz
- Independent positive and negative threshold qualification to suppress error propagation
- 0.5 ns max pulse pairing
- Servo differentiator and 4-burst servo capture
- +5V only operation
- 44-pin SOM package

BLOCK DIAGRAM



SSI 32P3010
Pulse Detector with Programmable Filter

FUNCTIONAL DESCRIPTION

The SSI 32P3010 Pulse Detector/Filter with 4-Burst Servo Capture is designed to support a 48 Mbit/s NRZ data rate. The signal processing circuits include a wide band variable gain amplifier, a sophisticated dual-rate AGC charge pump, a programmable electronic filter, a pulse qualifier, a servo differentiator and a 4-burst servo capture circuit.

Modes of Operation

The SSI 32P3010 can operate in one of three modes as controlled by $\overline{RG}$ and $\overline{WG}$.

Normal Read Mode $\overline{RG}$ = 0, $\overline{WG}$ = 1

In the normal Read Mode, the AGC actions are active. The AGC amplifier processes the input signal pulses; one-shot pulses are generated at the RD and $\overline{RD}$ outputs for each qualified signal peak. The $\overline{RDO}$ output buffer, which is a TTL buffer of the RD/$\overline{RD}$, is disabled and its output is pulled up high to reduce jitter and noise.

Servo Read Mode $\overline{RG}$ = 1, $\overline{WG}$ = 1

In the servo Read Mode, the AGC actions remain active (See note 1). The servo signal is amplified, fullwave rectified, differentiated and gated to the proper peak capture capacitor. The pulse qualifier remains active, and the $\overline{RDO}$ output is active to aid in servo decode.

Write Mode $\overline{RG}$ = X, $\overline{WG}$ = 0

In the Write Mode, the AGC actions are suspended. The AGC amplifier input impedance is clamped low to facilitate fast recovery. The $\overline{RDO}$ output is disabled and pulled up high to reduce jitter and noise.

AGC Amplifier

The wide band AGC amplifier amplifies the read signal from the read/write pre-amp to a signal level acceptable at the pulse qualifier. The AGC amplifier gain is an exponential function of the BYP voltage when referenced to VR.

$$Av = Ao \exp[\frac{(V_{BYP} - VR)}{K}] \quad \text{(See note 2)}$$

AGC Actions

The AGC loop maintains a constant DP/DN signal level at a nominal level, ~1Vppd. The AGC actions are current charging and discharging to/from the external BYP integrating capacitor, and are classified into the following modes:

Normal Read and Servo Read Mode ($\overline{RG}$ = X, $\overline{WG}$ = 1)

Slow Decay: When the DP/DN signal is below 1Vppd, a slow decay current, Id, charges the BYP capacitor. The AGC amplifier gain is increased slowly. This slow decay current tracks with the bandwidth of the filter. Id = 0.008 x IFI. At T = 27°C, the maximum Id is 4.5 µA when the filter cutoff frequency is 27 MHz.

Slow Attack: When the DP/DN signal exceeds 1Vppd, but is below 1.25 Vppd, a slow attack current, Ich, discharges the BYP capacitor. The AGC amplifier gain is decreased. The slow attack current is 20 times that of the slow decay current. Thus, for a given BYP capacitor, the slow attack response time is quicker than the slow decay response.

Fast Attack: When the DP/DN signal exceeds 1.25 Vppd, the device enters a fast attack mode. A fast attack current, Ichf, discharges the BYP capacitor. The AGC amplifier gain is quickly lowered. The fast attack current is seven times that of the slow attack current.

In servo Read Mode, constant AGC amplifier gain is generally desirable. Without an external AGC hold control, the servo data amplitude should be made lower than that of the data signal prior to the servo read mode. The SSI 32P3010 then enters the slow decay mode, which has a very slow effect on the AGC amplifier gain.

Write Mode ($\overline{RG}$ = X, $\overline{WG}$ = 0)

In the write mode, the AGC charge pump is disabled. This holds the AGC amplifier gain at its previous value.

Notes:

1. The servo signal should have a lower amplitude than the data signal prior to the servo read mode. Servo read should be completed before and significant change in AGC amplifier gain is resulted from the slow decay AGC mode.

2. In a closed AGC loop, the sensitivity of Ao and K to typical process variations is irrelevant. The typical values of Ao and K are provided for reference only, and not tested in production. Ao = 11, K = 0.22, VR = 3.6.

Write-to-Read Transition
($\overline{RG}$ = X, $\overline{WG}$ = 0-to-1)

When the SSI 32P3010 switches from the write to read mode, i.e., $\overline{WG}$ 0-to-1 transition, the device remains in the low input impedance state for a preset time period. For the next time period, the device then enters either the fast decay or attack mode depending on the signal level at the DP/DN pins. The time period, τ, is determined by an external resistor, RT, from the LZ/FD pin to ground.

$$\tau(\mu s) = \frac{RT(k\Omega)}{42}$$

For example, with RT = 38 kΩ, each time period is 0.9 μs.

Programmable Filter

The SSI 32P3010 includes a programmable low pass filter following the AGC amplifier for (1) 2X voltage gain from the AGC amplifier output to the pulse qualifier input, (2) noise limiting, (3) pulse slimming, and (4) provision of a time differentiated signal. The low pass filter is of a 7-pole 2-zero Bessel type. The filter's unboosted -3 dB bandwidth, defined as the cutoff frequency, is programmable from 9-27 MHz; the high frequency equalization is programmable from 0-13 dB at the cutoff frequency.

The filter input is ac-coupled from the AGC amplifier output. The filter's normal low pass output is ac-coupled to the data channel of the pulse qualifier. The differentiated low pass output is ac-coupled to the time channel of the pulse qualifier.

The normalized 7-pole 2-zero Bessel filter transfer function is given in Figure 1.

The cutoff frequency, fc, is programmable with 3 pins: RX, IFO and IFI. At the RX pin, an external resistor to ground establishes a reference current:

$$IFO = \frac{0.75}{Rx}, \text{at } T = 27°C$$

IFI should be made proportional to IFO for fc temperature stability. The cutoff frequency is related to the RX resistor, IFO and IFI currents as the following:

$$fc(MHz) = 27 \bullet \frac{IFI}{IFO} \bullet \frac{1.25}{Rx(k\Omega)}$$

For a fixed cutoff frequency setting, IFO and IFI can be tied together. The cutoff frequency equation then reduces to:

$$fc(MHz) = 27 \bullet \frac{1.25}{Rx(k\Omega)}$$

For programmable cutoff frequency, an external current DAC can be used. IFO should be the reference current into the DAC. The DAC output current drives IFI, which is then proportional to the IFO. The DACF in the SSI 32D4661 Time Base Generator is designed to control fc of the Silicon Systems programmable filters. When the DACF, which has a 4X current gain from its reference to fullscale output, is used, 5 kΩ RX is used. The fc is then given by:

$$fc(MHz) = 27 \bullet \frac{F\_Code}{127}$$

where F_Code is the decimal code equivalent to the 7-bit input into the DACF.

The high frequency equalization is programmable with two pins: VRG and VBP. The VRG is a bandgap reference voltage, 2.2V typically. The voltage at the VBP pin determines the amount of high frequency boost at the cutoff frequency. The boost function is as follows:

$$Boost(dB) = 20\log_{10}\left[\left(\frac{3.47 \bullet VBP}{VRG}\right) + 1\right]$$

For a fixed boost setting, a resistor divider between VRG to ground can be used with the divided voltage at the VBP pin. For programmable equalization, an external voltage DAC can be used. VRG should be the reference voltage to the DAC. The DAC output voltage is then proportional to the VRG. The DAC in the SSI 32D4661 is designed to control the magnitude equalization of Silicon Systems programmable filters.

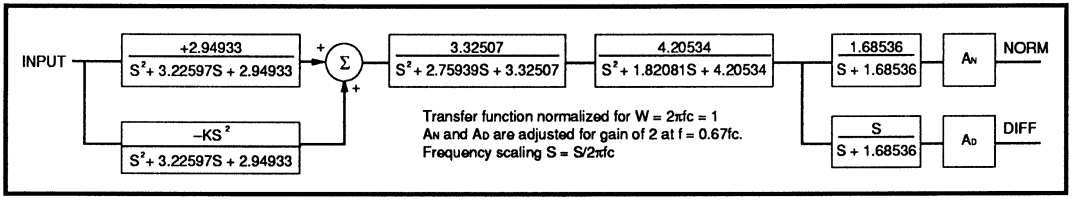


FIGURE 1: Bessel Filter Transfer Function

When DACs are used, the boost relation then reduces to:

$$\text{Boost(dB)} = 20\log_{10}[(3.47 \bullet \frac{\text{S\_Code}}{127}) + 1]$$

Pulse Qualification

The SSI 32P3010 validates each DP/DN peak by a combination of level qualification and time qualification. In level qualification, a dual-comparator threshold detection eliminates errors due to low level additive noise. In time qualification, the filter's differentiated output is used to locate signal peaks.

Level Qualification

The dual-comparator architecture allows independent detection for positive and negative peaks. One comparator detects a positive peak by comparing the data signal with a positive threshold. The other comparator detects a negative peak by comparing the data signal with a negative threshold. Each comparator has a small hysteresis, 20% of the set threshold, to help qualify signals which just clear the set threshold.

The SSI 32P3010 comparator thresholds are set by a DC voltage at the VTH pin, such as from a resistor divider from VCA to VRC (see note 3). The threshold at each comparator can be computed as: Hysteresis Gain x (VTH - VRC). The thresholds at the two comparators are of the same magnitude, but of opposite polarity.

The SSI 32P3010 has three sets of pulse detector outputs: RD/$\overline{\text{RD}}$, $\overline{\text{RDO}}$, and DO/$\overline{\text{DO}}$. RD/$\overline{\text{RD}}$ output is the pseudo-ECL differential output. Corresponding to each validated peak of the DP/DN signal, a one-shot pulse occurs at the RD/$\overline{\text{RD}}$ output. The pulse width of the one-shot pulse is determined by an internal timing circuit, and specified in the electrical specification.

$\overline{\text{RDO}}$ is the TTL output of the pulse detector, logically equivalent to RD/$\overline{\text{RD}}$. Again, a one-shot pulse occurs at the $\overline{\text{RDO}}$ output for each validated peak of the DP/DN signal. The pulse width of this one-shot pulse is also specified in the electrical specification. DO/$\overline{\text{DO}}$ outputs are differential test points used to monitor the outputs of the internal comparators. Each is an open-emitter output requiring a 5 kΩ external resistor pull-down to ground.

Four-Burst Servo Differentiator and Capture

The SSI 32P3010 supports advanced embedded 4-burst servo technique. The signal at the DP/DN input can be time differentiated, fullwave rectified, and gated onto the selected peak capture output. A peak capture output is selected by pulling its corresponding $\overline{\text{GT}}$ x to logic '0.'

The transfer function from the DP/DN to the servo fullwave rectifier input is:

$$\text{Av} = \frac{2380\,\text{Cs}}{\text{LCs}^2 + (\text{R} + 48.1)\text{Cs} + 1}$$

where: R, L, and C are external passive components across SDIF±

$$15\ \text{pF} < \text{C} < 125\ \text{pF}$$
$$\text{s} = \text{jw}$$

When the time differentiation function is not desired, a 2 kΩ resistor should be used across the SDIF± pins.

The transfer function from the servo fullwave rectifier input to the peak capture output is set so that a 1 Vppd DP/DN signal produces 0.95 Vpeak output. With no signal input, the outputs are set close to ground, with a finite offset common to all four channels.

Note 3: VCA is the +5V supply. VRC is the bandgap voltage referenced from VCA, i.e., VRC = VCA - VRG.

PIN DESCRIPTION

INPUT PINS

NAME	TYPE	DESCRIPTION
VIA+, VIA-	I	AGC Amplifier input pins.
IN+, IN-	I	Equalizer/filter input pins.
DP, DN	I	Data inputs to data comparators and fullwave rectifier.
CP, CN	I	Differentiated data inputs to the clock comparator.
VTH	I	Threshold level setting input for the data comparators.
$\overline{\text{WG}}$	I	TTL compatible input. When low the device is in Write Mode.

PIN DESCRIPTION

INPUT PINS (continued)

NAME	TYPE	DESCRIPTION
$\overline{RG}$	I	TTL compatible input. When low, the device is In normal Read Mode.
$\overline{WG}$	I	TTL compatible input. When low, the device is in Write Mode. When both $\overline{RG}$ and $\overline{WG}$ are low, the device is in Servo Mode.
$\overline{GTA}$, $\overline{GTB}$, $\overline{GTC}$, $\overline{GTD}$	I	TTL compatible input. When low the corresponding servo gate channel is enabled.
OUTPUT PINS		
VOA+, VOA-	O	AGC amplifier output pins.
ON+, ON-	O	Equalizer/filter normal output pins.
OD+, OD-	O	Equalizer/filter differentiated output pins.
DO, $\overline{DO}$	O	ECL compatible data comparator latch output pins.
RD, $\overline{RD}$	O	ECL compatible read data output pins.
$\overline{RDO}$	O	TTL compatible read data output.
SDIF+, SDIF-	-	Pins for external differentiating network for servo data.
PKA, PKB PKC, PKD	O	Open npn emitter outputs that provide a fullwave rectified signal from the servo differentiator. These outputs are referenced to AGND. These outputs are high impedance when not enabled by $\overline{GTX}$
ANALOG PINS		
VRC	-	Reference voltage pin for SERVO and LEVEL. VRC is referenced to VCA.
VRG	-	Reference voltage pin for the programmable filter. VRG is referenced to ground.
VBP	-	The equalizer high frequency boost is set by an external voltage applied to this pin. VBP must be proportional to VRG. Programmable boost is implemented by using a DAC that uses VRG as its reference. A fixed amount of boost can be set by an external resistor divide network connected from VBP to VRG and GND.
RX	-	Pin to set filter reference current. External resistor Rx from this pin to ground sets the filter reference current IFO.
IFO	-	Reference current output pin. The reference current is normally supplied as the reference current to a current DAC which generates the programmable input current for the IFI pin.
IFI	-	Programmable filter input current pin. The filter cutoff frequency is proportional to the current into this pin. The current must be proportional to the reference current out of IFO. A fixed filter cutoff frequency is generated by connecting IFO to IFI and selecting Rx to set the desired frequency.
LZ/FD	-	Pin for external resistor to set timing for both Low-Z input and fast decay modes.
BYP	-	The AGC integrating capacitor C_A is connected between BYP and VCA.
VCA, VCD	-	Analog and Digital +5 volts.
AGND1, DGND	-	Analog and Digital grounds.

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, 4.5 to 5.5, 0°C<Ta<70°C

ABSOLUTE MAXIMUM RATINGS (Operation above maximum ratings may damage the device.)

PARAMETER	VALUE	UNIT
Storage Temperature	-65 to +150	°C
Junction Operating Temperature,Tj	+130	°C
Supply Voltage, VCA, VCD	-0.7 to 7	V
Voltage Applied to Inputs	-0.7 to VCA, VCD	V

RECOMMENDED OPERATING CONDITIONS

PARAMETER		RATING	UNIT
Supply Voltage	VCA = VCD = VCC	4.5 < VCC < 5.5	V
Ambient Temperature, Ta		0<Ta<70	°C

POWER SUPPLY

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
PD	Power Dissipation	Outputs unloaded 4.5V < VCA, VCD < 5.5V		490	540	mW

LOGIC SIGNALS

VIL	TTL Input Low Voltage		-0.3		0.8	V
VIH	TTL Input High Voltage		2.0		VCC +0.3	V
IIL	TTL Input Low Current	VIL = 0.4V	-0.4			mA
IIH	TTL Input High Current	VIH = 2.7V			0.1	mA
VOL	ECL Output High Voltage	VCC = 5V		VCC -1.02		V
VOE	ECL Differential Output Swing	VCC = 5V	0.6			Vpp
TRF	EC1 Output Rise and Fall Time	CL = 10 pF			3.5	ns
TS	Control Input Switching Times				0.1	µs
VOLT	TTL Output Low Voltage	IOL = 4mA	0.5			V
VOHT	TTL Output High Voltage	IOH = -400 mA			2.7	V

AGC AMPLIFIER

The input signals are AC coupled to VIA+ and VIA-. VOA+ and VOA- are AC coupled to IN+ and IN-. ON+ and ON- are AC coupled to DP and DN. Ca 1000 pF. Fin = 4 MHz. Unless otherwise specified, the output is measured differentially at VOA+ and VOA-.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VIB	Input Range	Filter boost at fc = 0 dB	24		240	mVppd
		Filter boost at fc = 11 dB	20		100	mVppd
VD	DP-DN Voltage	VIAppd = 0.1 Vppd	0.90		1.10	Vppd
VDV	DP-DN Voltage Variation	24 mV < VIAppd < 240 mV			8.0	%
AV	Gain Range		1.9		22	V/V
AVPV	Gain Sensitivity w.r.t. BYP Voltage			28		dB/V
DR	VOA+ VOA- Dynamic Range	THD = 1% max	.75			Vppd
RINDA	Differential Input Impedance	$\overline{WG}$ = 1	4.7		8.4	kΩ
		$\overline{WG}$ =0		1		
RINSA	Single Ended Input Impedance	$\overline{WG}$ = 1		3		kΩ
		$\overline{WG}$ = 0		0.5		kΩ
VOS	Differential Output Offset Variation	from min. gain to max. gain	-200		+200	mV
VIN	Input Referred Noise Voltage	gain = max, Rs = 0Ω filter not connected to VOA+ and VOA-			15	$nV\sqrt{Hz}$
BW	Bandwidth	No AGC action, Gain = 22	55			MHz
CMRR	Common Mode Rejection Ratio	gain = 22, f = 5 MHz	40			dB
PSRR	Power Supply Rejection Ratio	gain = 22, f = 5 MHz	45			dB
TGD	Gain Decay Time	VIAppd = 240 mV to 120 mV VOAppd < 0.9 Final Value		TBD		µs
TGA	Gain Attack Time	VIAppd = 120 mV to 240 mV VOAppd < 1.1 Final Value		TBD		µs

ELECTRICAL SPECIFICATIONS (continued)

Unless otherwise specified, 4.65<VCC<5.25, 0°C<Ta<70°C

AGC CONTROL

The input signals are AC coupled to DP and DN. Ca = 1000 pF.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VDI	DP-DN Signal Input Range				1.5	Vpp
ID	Discharge Current	$\overline{WG}$ = 1, DP - DN = 0V		0.008 x IFI		A
IDF	Fast Discharge Current			20 x Id		A
ICH	Charge Pump Attack Current	$\overline{WG}$ = 1, DP - DN = 0.55V		40 x Id		A
ICHF	Charge Pump Fast Attack Current, Ichf	$\overline{WG}$ = 1, DP - DN = 0.675V		7 x Ich		A
IK	BYP Pin Leakage Current	$\overline{WG}$ = 0	-0.1		+0.1	µA
VRC	VRC Reference Voltage			VCA -VRG		V
IVRC	VRC Output Drive		-0.75		+0.75	mA
VRG	VRG Reference Voltage		2.2		2.45	V
IVRG	VRG Source Current		1			mA
TLZ	Low-Z and Fast Decay Timing Accuracy	T = RT/42	-30		+30	%

EQUALIZER/FILTER

The input signals are AC coupled to IN+ and IN-.

fc	Filter Cutoff Frequency	RX = 5kΩ *fc* = 27 x IFI/(4 x IFO) MHz 4 ≥ IFO/IFI ≥ 4/3	9		27	MHz
IFO	IFO Reference Current	IFO = 0.75/RX; Tj = 27°C 5kΩ > RX > 1.25 kΩ	0.15		0.6	mA
IFI	IFI Program Current Range	Tj = 27°C, 27 MHz > *fc* > 9 MHz	0.2		0.6	mA
FCA	FCA Filter FC Accuracy	*fc* = 27 MHz	-10		10	%
RX	RX Range		1.25		5	kΩ
AO	Normal Low Pass Gain AO = (ON ±) / (IN±)	Fin = 0.67*fc*	1.6		2.4	V/V
AD	Differentiated Low Pass Gain AD = (ON ±) / (IN±)	Fin = 0.67*fc*	0.8AO		1.2AO	V/V
FB	Frequency Boost at *fc*	FB = 20log [3.47 (VBP/VR) + 1]	0		13	dB
FBA	Frequency Boost Accuracy	FB = 13 dB	-1		+1	dB

EQUALIZER/FILTER (continued)

The input signals are AC coupled to IN+ and IN-.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TGD1	Group Delay Variation	*fc* = 27 MHz, FB = 0 to 9 dB *fc* > Fin > 0.3 *fc*	-0.5		+0.5	ns
TGD2		*fc* = 9 to 27 MHz *fc* > Fin > 0.3 *fc*	-2.5		+2.5	%
VOSF	Output Offset Voltage				200	mV
DRF	VOF Filter Output Dynamic Range	THD = 1.5% max Fin = 0.67 *fc*	1.5			Vpp
RINF	Filter Input Resistance		3.0			kΩ
CINF	Filter Input Capacitance				7	pF
ROF	Filter Output Resistance	IO = 0.5 mA			60	Ω
VNN	Eout Output Noise Voltage; ON+, ON-	BW = 100 MHz, RS = 50Ω VBP = 0, *fc* = 27 MHz		2.7		mVRms
		BW = 100 MHz, RS = 50Ω VBP = VRG, *fc* = 27 MHz		5.7		mVRms
VND	Eout Output Noise Voltage; OD+, OD-	BW = 100 MHz, RS = 50Ω VBP = 0, *fc* = 27 MHz		5.5		mVRms
		BW = 100 MHz, RS = 50Ω VBP = VRG, *fc* = 27 MHz		13.0		mVRms

DATA COMPARATOR

The input signals are AC coupled to DP and DN.

VID	DP-DN Signal Range				1.5	Vpp
RIND	Differential Input Resistance		8		14	kΩ
CIND	Differential Input Capacitance				5	pF
VOSD	Comparator Offset Voltage				4	mV
HYS	Threshold Voltage Gain	0.3 < VTH-VRC < 0.9	0.41		0.48	V/V
VSH	Threshold Voltage Hysteresis			.20 x GHYS x (VTH -VRC)		V/V
TPDD	Propagation Delay	To DO, $\overline{DO}$		6		ns
IVTH	VTH Input Bias Current				2	µA

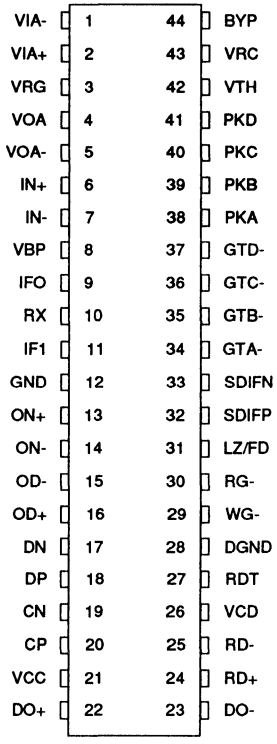
CLOCKING
The input signals are AC coupled to CP and CN.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VIC	CP-CN Signal Range				1.5	Vppd
VOSC	Comparator Offset Voltage				4	mV
RINC	Differential Input Resistance		8		14	kΩ
CINC	Differential Input Capacitance				5	pF
TDS	D Flip-Flop Set Up Time	DP-DN threshold to CP-CN zero cross, CP-CN = 1Vppd at 18 MHz	0			ns
PP	Pulse Pairing	CP-CN = 20 mVppd square wave			0.5	ns
TPDC	Propagation Delay from CP-CN zero crossing to RD			9		ns
PWRD	RD Output Pulse Width		8		14	ns
PWRT	$\overline{RDO}$, TTL Output Pulse Width		20		40	ns

SERVO DIFFERENTIATOR/FULL-WAVE RECTIFIER
An external series network is connected between SDIF and $\overline{SDIF}$ to determine the servo differentiator transfer function. The input signals are AC coupled to DP and DN. Fin = 6.7 MHz at 1.0 Vppd.

ISDIF	SDIF to $\overline{SDIF}$ pin current	Differentiator impedance must be set so as not to dip the signal for this level	0.7	1.0	1.3	mA
RDIF	Internal differentiator pull-up resistors	Cannot be directly tested	1.0	1.2	1.4	kΩ
FWR	Input voltage range to maintain FWR voltage gain	Cannot be directly tested	0.1		2.0	Vppd
RERR	Rectification Error				5	%
AFWR	FWR Voltage Gain from FWR Input to PKA-D Outputs		TBD	0.97	TBD	Vpp/Vppd
ISL	Servo Output Leakage Current	Channel diabled			10	µA
VCOS	PKA-D Channel to Channel Offset	1Vppd input to servo FWR	-5		5	mV
VAOS	PKA-D Absolute Offset	1Vppd input to servo FWR	TBD		TBD	mV

PACKAGE PIN DESIGNATIONS
(Top View)



32P3010
44-Pin SOM

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 731-7110, FAX (714) 573-6914

Notes:

silicon systems®
A TDK Group Company

SSI 32P3030
Pulse Detector and Servo Demodulator

November 1991

2

DESCRIPTION

The SSI 32P3030 is a low power pulse detector and servo demodulator designed for use in low power applications requiring +5V only power supplies. This device has a fully integrated bipolar circuit that detects and validates amplitude peaks in the output from a disk drive read amplifier, as well as detecting embedded servo information to provide position error signals used for read head positioning.

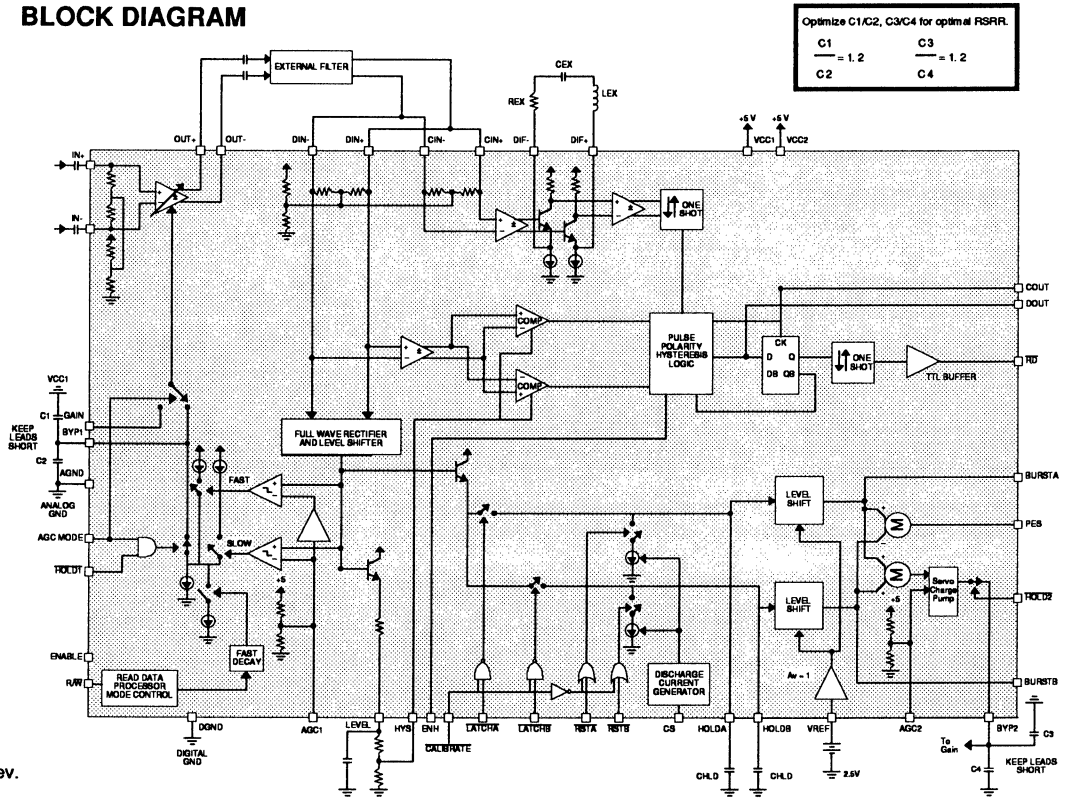
Time and amplitude qualification are used to provide a TTL compatible output that accurately duplicates the time position of input signal peaks. An AGC control loop, using a dual rate charge pump, provides a constant input amplitude for the level qualifier. Level qualification with or without hysteresis can be implemented as a fixed threshold or a constant percentage that tracks signal amplitude that enhances qualification during AGC loop transients.

(Continued)

FEATURES

- **+5V only power supplies**
- **Wide bandwidth AGC input amplifier**
- **Fast and slow AGC attack and decay regions for fast transient recovery**
- **Embedded servo channel provides servo burst capture and difference circuits**
- **Local sampled servo AGC provided based on servo burst output amplitude sum**
- **Write to Read transient suppression**
- **Dual mode pulse qualification with/without pulse polarity hysteresis for read/servo data retrieval.**
- **16 Mbit/s operation**

BLOCK DIAGRAM



DESCRIPTION (Continued)

The Servo Demodulator consists of two peak detector channels that capture rectified servo data peaks. Buffered individual channel outputs are provided along with a difference output. Servo channel gain can be controlled by a sampled AGC signal based on maintaining the amplitude of the sum of both channels.

CIRCUIT OPERATION

READ MODE (R/$\overline{W}$ pin high or open)

In Read Mode the SSI 32P3030 is used to process either data or servo signals. In the Data Read Mode the input signal is amplified and qualified using an AGC amplifier and pulse level qualification of the detected signal peaks. In the Servo Read Mode the input signal is amplified and rectified and an error signal based on amplitude comparison is made available. Two servo burst channels are available that provide A & B burst levels.

DATA READ MODE (AGCMODE pin high or open)

An amplified head output signal is AC coupled to the IN+ and IN- pins of the AGC amplifier. Gain control is accomplished by full wave rectifying and amplifying the [(DIN+) - (DIN-)] voltage level and comparing it to a reference voltage level at the AGC1 pin.

The SSI 32P3030 contains a dual rate attack charge pump. The value of the attack current is dependent on the instantaneous level at DIN±. For signal levels above 125% of the desired level a fast attack mode is invoked that supplies a 1.4 mA charge current to the network on the BYP1 pin. Between 125% and 100% of the desired level the circuit enters a slow attack mode and supplies 0.18 mA of charge current to the BYP1 pin. This allows the AGC to rapidly recover during a write to read transition but reduces distortion once the AGC amplifier is within range.

Two decay modes are available and are automatically controlled within the device.

Upon a switch to write mode (R/$\overline{W}$ pin low), the device will hold the gain at its previous value, and the AGC input stage is switched into a low impedance state. When the device is then switched back to read mode the AGC holds the gain and stays in the low impedance state for 0.9 µs. It then switches into a fast/slow attack mode if the new gain required is less than the previously held gain or a fast decay mode if the gain required is more than its previous value. The fast decay current is 0.12 mA and stays on 0.9 µs. After the 0.9 µs time period the device stays in a steady state slow attack, slow decay mode. The slow decay discharge current is 4.5 µA.

The AGC1 pin is internally biased so that the target differential voltage input at DIN± is 1.0 Vpp at nominal conditions. The voltage on this pin can be modified by tying a resistor between AGC and AGND or VCC1. A resistor to AGND decreases the voltage level, while a resistor to VCC1 increases it. The resulting AGC voltage level is shown in Figure 1;

Where:

V = Voltage at AGC1 with pin open (2.3V, nom.)

Rint = AGC1 pin input impedance (6.5 kΩ, typ.)

Rx = External resistor.

The new DIN± input target level is nominally
(V_{AGC1} - 0.75) • 0.64 Vpp

The maximum AGC amplifier output swing is 2.6 Vpp at OUT± which allows for up to 6 dB loss in any external filter between OUT± and DIN±.

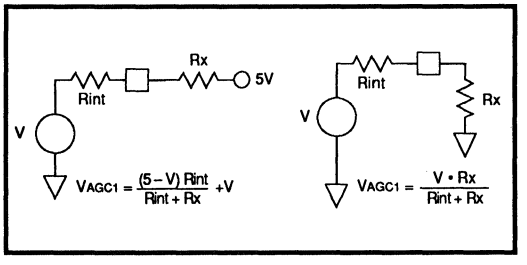


FIGURE 1: AGC Voltage

AGC gain is a linear function of the BYP1/Gain-pin voltage (VBYP1) as shown in Figure 2.

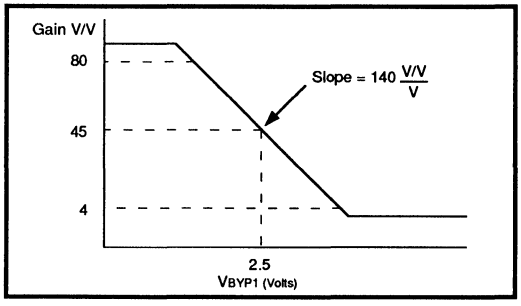


FIGURE 2: AGC Gain

The AGC amplifier has emitter follower outputs and can sink 4.0 mA.

One filter for both amplitude (DIN± input) and time (CIN± input) channels, or a separate filter for each may be used. If two filters are used, attention must be paid to time delays so that each channel is timed properly. A multi-pole Bessel filter is typically used for its linear phase or constant group delay characteristics.

In the amplitude channel the signal is sent to a hysteresis comparator. The hysteresis threshold level is set so that it will be tripped only by valid signal pulses and not by baseband noise. It can be a fixed level or a fraction of the DIN± voltage level.

The latter approach is accomplished by using an external filter/network between the LEVEL and HYS pins. This allows setting the AGC slow attack and decay times slow enough to minimize time channel distortion and setting a shorter time constant for the hysteresis level. The LEVEL pin output is a rectified and amplified version of DIN±, 1.0 Vpp at DIN± results in 1.0 Vop nominally, at the LEVEL pin. A voltage divider is used from LEVEL to ground to set the Hysteresis threshold at a percentage of the peak DIN± voltage. For example, if DIN± is 1.0 Vpp, then using an equal valued resistor divider will result in 0.5 Vop at the HYS pin. This will result in a nominal ±0.18V threshold or a 36% threshold of a ±0.5V DIN± input. The capacitor, from the LEVEL pin to GND, is chosen to set an appropriate time constant. This "feed forward" technique speeds up transient recovery by allowing qualification of the input pulses while the AGC is still settling. This helps in the two critical areas of write to read and head change recovery. Some care in the selection of the hysteresis level time constant must be exercised so as to not miss pattern (resolution) induced lower amplitude signals. Note that there is a built in 50mV threshold (ie., 10% of ±0.5V DIN± input) for level qualification even when the HYS pin is grounded. This is to prevent false triggering by baseband noise during a DC erase gap, (e.g., address mark). The output of the hysteresis comparator is the "D" input of a D-type flip-flop. The DOUT pin is a comparator output signal for testing purposes only. When testing, it requires an external 3-6 kΩ pull-down resistor to ground. If no testing is necessary, the DOUT pin can be pulled up to Vcc (+5V) to save power.

In the time channel the signal is differentiated to transform signal peaks to zero crossings which are detected and used to trigger a bi-directional one-shot. The one-shot output pulses are used as the clock input of the D flip-flop. The COUT pin provides the one-shot output for test purposes. It also requires an external 3-6 kΩ pull down resistor for testing.

The differentiator function is accomplished by an external network between the DIF+ and DIF- pins. The transfer function from CIN± to the comparator input (not DIF±) is:

$$Av = \frac{-2000Cs}{LCs^2 + C(R+92)s + 1}$$

Where: C, L, R are external passive components

$20\ pF < C < 150\ pF$

$s = j\omega = j2\pi f$

During normal operation, the time channel clocks the D flip-flop on every positive and negative peak of the CIN± input. Two qualification modes exist to determine peaks. The first mode, qualification with pulse polarity hysteresis, (ENH = High), is exactly the same as the qualification on the SSI 32P541. In this mode, the D input to the flip-flop only changes state when the DIN± input exceeds the hysteresis comparator threshold opposite in polarity to the previous threshold exceeding peak. In the second mode, qualification without pulse polarity hysteresis, (ENH = Low), the polarity of the peaks is ignored. In this mode, the D input to the flip-flop changes state whenever the DIN± input exceeds the threshold regardless of polarity. This is accomplished, (see figure 3), by clocking the toggle flip-flop whenever the threshold is exceeded in either direction at the same time that the comparator detects a zero

crossing. It may be advantageous to use this mode of pulse qualification for retrieving certain kinds of servo patterns.

The time channel, then, determines signal peak timing and the amplitude channel determines validity by blocking signal peaks that do not exceed the hysteresis comparator threshold. The delays in each of these channels to the D flip-flop inputs are well matched. The D flip-flop output triggers a one-shot that sets the $\overline{RD}$ output pulse width.

SERVO READ MODE

A position error signal (PES) is generated based on the relative amplitude of two servo signals, A and B. Rectified servo signal peaks are captured on hold capacitors at the HOLDA/B pins. This is accomplished by pulling $\overline{LATCHA}$ or $\overline{LATCHB}$ low for a sample period. Additionally, a default hold capacitor discharge current of 1.5 mA can be turned on by pulling $\overline{RSTA}$ or $\overline{RSTB}$ low. This default 1.5 mA discharge current can be modified by tying a resistor between CS and GND or VCC1. A resistor to GND increases the discharge current, while a resistor to VCC1 decreases it. The equation for increasing the discharge current is:

$$Ics = 22.5V \bullet \left(\frac{15k + Rcs}{15k \bullet Rcs}\right), \quad Rcs \geq 15\ k\Omega$$

For decreasing the discharge current, the equation is:

$$Ics = 22.5V \bullet \left(\frac{Rcs - 22.5k}{15k \bullet Rcs}\right), \quad Rcs \geq 22.5\ k\Omega$$

Outputs BURSTA/B & PES are referenced to an external reference applied to the VREF pin.

In servo read mode (see Figure 4) the BYP2 pin is connected to the GAIN pin and the servo channel gain is determined by the read channel gain as controlled by the sum of the A and B amplitudes. In this case a current is sourced/sinked to/from the capacitor on the GAIN/BYP2 pin whenever the $\overline{HOLD2}$ pin is pulled high. The current magnitude and direction is determined by:

$Ic = K_4[(K_5 \bullet V_{AGC2}) - Va(DIN)pp - Vb(DIN)pp]$

Where:

V_{AGC2} = AGC2 pin voltage = 2.3V with pin open.

K_4 = 640 µA/Vpp

K_5 = 0.50 V/V

Va/b(DIN)pp = peak to peak A or B servo pattern signal voltages at DIN±

WRITE MODE

In Write Mode the SSI 32P3030 Pulse Detector section is disabled and preset for the following Read Mode. The digital circuitry is disabled, the input AGC amplifier gain is held at its previous value and the AGC amplifier input impedance is reduced to about 250Ω.

Holding the AGC amplifier gain and reducing input impedance shortens system Write to Read recovery times.

The lowered input impedance improves settling time by reducing the time constant of the network between the SSI 32P3030 and a head preamplifier such as the SSI 32R1200R. Write to read timing is controlled to maintain the reduced impedance for 0.9 µs before the AGC circuitry is activated. Coupling capacitors should be chosen with as low a value as possible consistent with adequate bandwidth to allow more rapid settling.

MODE CONTROL

The device circuit mode is controlled by the ENABLE, R/$\overline{W}$, AGCMODE, $\overline{HOLD1}$ and $\overline{HOLD2}$ pins a shown in Table 1.

DATA READ MODE

AGC active and controlled by data, Digital section active.

DATA READ MODE, HOLD

AGC gain held constant, Digital section active. Gain will drift higher or lower at a rate determined by C_{BYP1} and Hold mode leakage current.

SERVO READ MODE I (See Figures 4 & 5)

The BYP2 and GAIN pins are tied together. Read amplifier AGC control voltage developed from sum of Servo signal levels. $\overline{HOLD2}$ is toggled to update the control voltage after each Servo frame.

CALIBRATE MODE

A low level on $\overline{CALIBRATE}$ shall force $\overline{LATCHA}$ and $\overline{LATCHB}$ low and $\overline{RSTA}$ and $\overline{RSTB}$ high to measure the offset of the entire servo BURSTA, BURSTB, and PES channel.

WRITE

Read amplifier input impedance reduced. AGC gain held constant, $\overline{RD}$ stays high.

POWER DOWN

Circuit switched to a low current disabled mode.

Note: When AGCMODE is switched to a low state the voltage at the BYP1 pin will be held constant subject to Hold mode leakage current induced drift. So, when returning to Data Read Mode, the channel gain will be the same as it was prior to AGCMODE switching or slightly higher/lower.

TABLE 1: SSI 32P3030 Circuit Mode Control

ENABLE	R/$\overline{W}$	AGC MODE	$\overline{HOLD1}$	$\overline{HOLD2}$	READ PATH MODES
1	1	1	1	X	Data Read Mode
1	1	1	0	X	Data Read Mode Hold
1	1	0	X	1	Servo Read Mode - Sample
1	1	0	X	0	Servo Read Mode - Hold
1	0	X	X	X	Write
0	X	X	X	X	Power Down

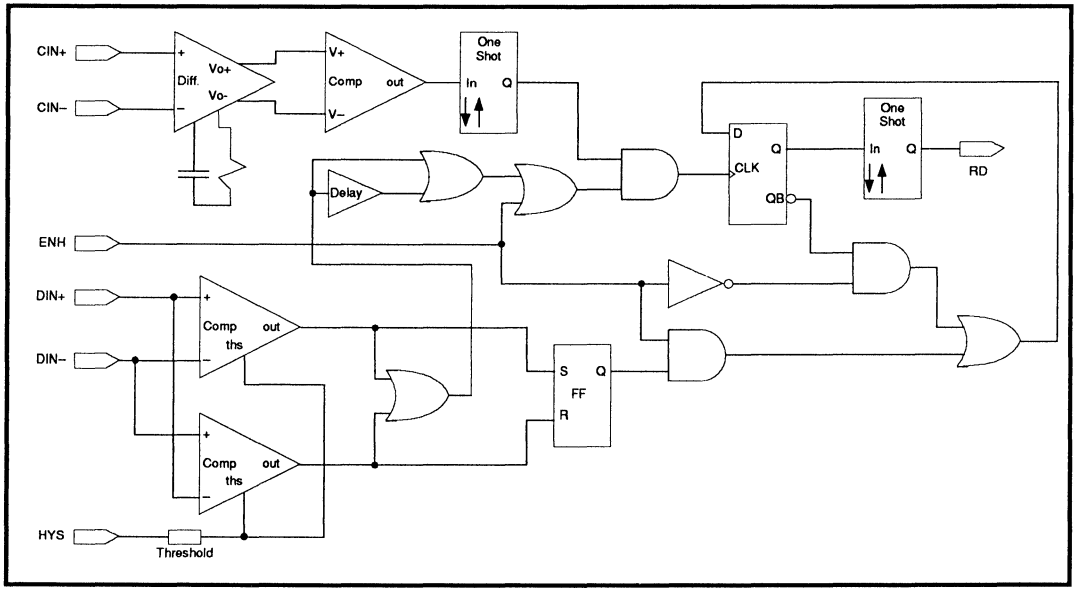


FIGURE 3: ENH Provides Two Pulse Qualification Modes.

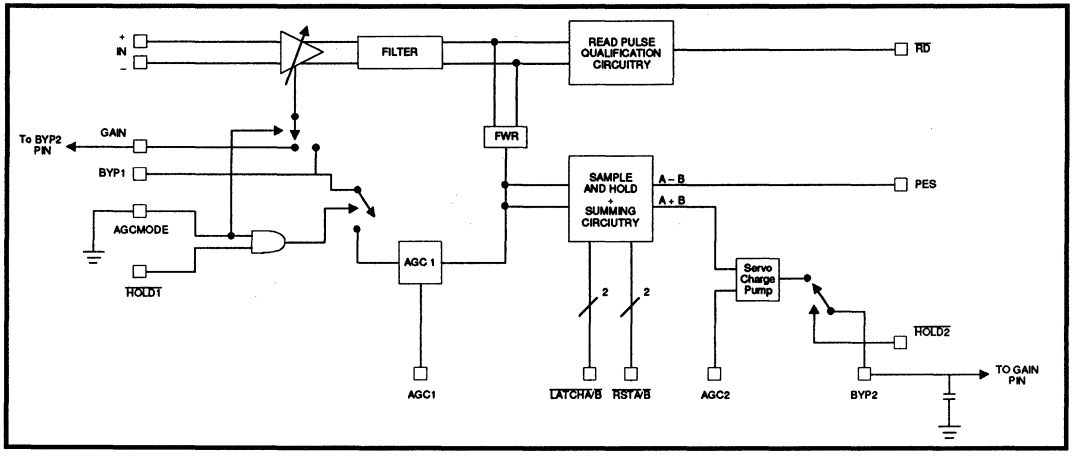


FIGURE 4: Servo Read Mode

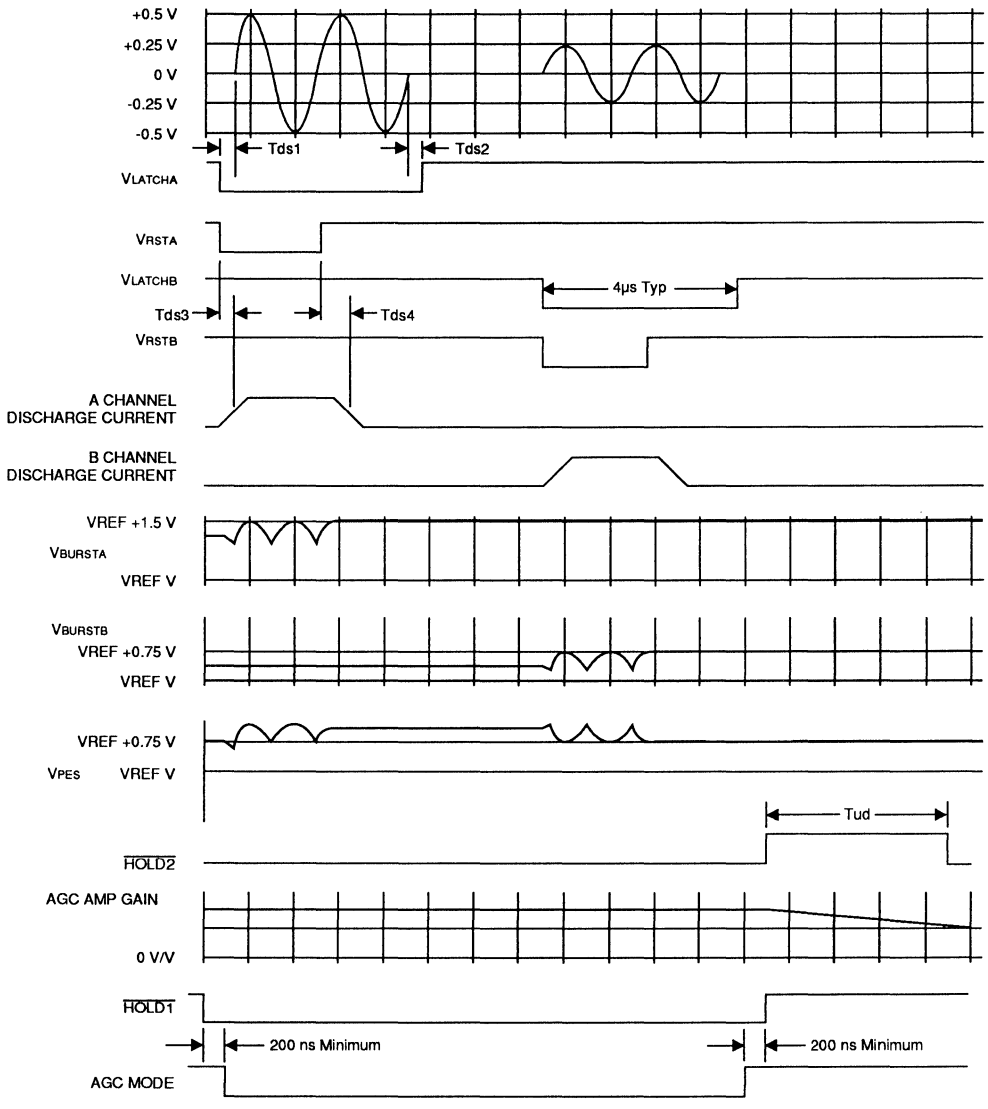


FIGURE 5: Servo Read Mode 1

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
VCC1	I	Analog (+5V) power supply for pulse detector.
AGND	I	Analog ground pin for pulse detector block.
VCC2	I	Digital (+5V) supply pin for data synchronizer block.
DGND	I	Digital ground pin.
IN+, IN–	I	Analog signal input pins.
OUT+, OUT–	O	Read path AGC Amplifier output pins.
DIN+, DIN–	I	Analog input to the amplitude channel.
CIN+, CIN–	I	Analog input to the time channel.
DIF+, DIF–	I/O	Pins for external differentiating network.
COUT	O	Test point for monitoring the flip-flop clock input, pull-down resistor required.
DOUT	O	Test point for monitoring the flip-flop D-input, pull-down resistor required.
BYP1, BYP2	I/O	An AGC timing capacitor or network is tied between each pin and GND. BYP1 is for read data. BYP2 is for servo data.
AGC1, AGC2	I	Reference input voltage for the read data AGC loop. (AGC1) and sampled servo AGC loop (AGC2).
LEVEL	O	Output from fullwave rectifier that may be used for input to the hysteresis comparator.
HYS	I	Hysteresis level setting input to the hysteresis comparator.
$\overline{\text{HOLD1}}$, $\overline{\text{HOLD2}}$	I	TTL compatible pin that holds the AGC gain when pulled low.
$\overline{\text{LATCHA}}$, $\overline{\text{LATCHB}}$	I	TTL compatible inputs that switch channel A or B into peak acquisition mode when low.
$\overline{\text{RSTA}}$, $\overline{\text{RSTB}}$	I	TTL compatible input that enables the discharge of channels A & B hold capacitors when held low.
CS	I	Hold capacitor discharge current magnitude is controlled by a resistor from this pin to GND or VCC1. If left open the default current is 1.5 mA.
HOLDA, HOLDB	I/O	Peak holding capacitors are tied from each of these pins to AGND.
VREF	O	Reference voltage for Servo outputs.
BURSTA, BURSTB	O	Buffered hold capacitor voltage outputs.
PES	O	Position error signal, A minus B output.
R/$\overline{\text{W}}$	I	TTL compatible Read/Write control pin. A low input selects write mode.
Enable	I	TTL compatible power up control. A low input selects a low power state.
AGCMODE	I	TTL compatible pin that selects the AGC loop control input. A high selects BYP1, a low selects GAIN.
Gain	I	A voltage at the pin may be used to control AGC gain.
$\overline{\text{RD}}$	O	TTL compatible read output, a falling edge corresponds to a detected peak.
$\overline{\text{CALIBRATE}}$	I	Used to measure servo offset.
ENH	I	TTL compatible pulse qualification control pin. A low input selects modes which ignore polarity of peaks.

ELECTRICAL SPECIFICATIONS

Recommended conditions apply unless otherwise specified.

ABSOLUTE MAXIMUM RATINGS

Operation outside these rating limits may cause permanent damage to this device.

PARAMETER	RATING	UNIT
5V Supply Voltage, VCC1, VCC2	6.5	V
Pin Voltage (Analog pins)	.3 to VCC1 + .3	V
Pin Voltage (Digital pins)	.3 to VCC2 + .3 or +12 mA	V
Storage Temperature	-65 to 150	°C
Lead Temperature (Soldering 10 sec.)	260	°C

RECOMMENDED OPERATING CONDITIONS

Currents flowing into the chip are positive.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Supply Voltage (VCC1, VCC2)		4.5	5.0	5.5	V
Tj Junction Temperature		-		135	°C
Ambient Temperature	ENABLE = High or Low	0		80	°C

POWER SUPPLY

IVCC1,2 Supply Current	Outputs unloaded; ENABLE = high or open		76	110	mA
Pd Power dissipation	Ta = 25°C, outputs unloaded		380	570	mW
	ENABLE = Low		140	210	mW

LOGIC SIGNALS

VIL	Input Low Voltage		-0.3		0.8	V
VIH	Input High Voltage		2.0		VCC+0.3	V
IIL	Input Low Current	VIL = 0.4V	0.0		-0.4	mA
IIH	Input High Current	VIH = 2.4V			100	µA
VOL	Output Low Voltage	IOL = 4.0 mA			0.5	V
VOH	Output High Voltage	IOH = -400 µA	2.4			V

MODE CONTROL

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Enable to/from Disable Transition Time	Settling time of external capacitors not included, ENABLE pin high to/from low			20	µs
Read to Write Transition Time	R/$\overline{W}$ pin high to low			1.0	µs
Write to Read Transition Time	R/W pin low to high AGC setting not included	0.4	0.9	1.6	µs
AGC on to/from AGC off transition time	AGC mode pin high to/from low			2.0	µs
$\overline{HOLD1}$ ON to/from $\overline{HOLD1}$ OFF transition time	$\overline{HOLD1}$ pin high to/from low			1.0	µs
$\overline{HOLD2}$ ON to/from $\overline{HOLD2}$ OFF	$\overline{HOLD2}$ pin high to/from low			1.0	µs

READ MODE (R/$\overline{W}$ is High)

AGC AMPLIFIER

Unless otherwise specified, recommended operating conditions apply. Input signals are AC coupled to IN±. OUT± are loaded differentially with 800Ω, and each side is loaded with < 10 pF to AGND, and AC coupled to DIN±. A 900 pF capacitor is connected between BYP1/BYP2 and AGND. An 1100 pF capacitor is connected between BYP1/BYP2 and VCC1. AGC1/AGC2 pin is open.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Minimum Gain Range	1.0 Vp-p ≤ (OUT+) - (OUT-) ≤ 2.6 Vp-p	4		80	V/V
AGC Input Range		25		250	mVpp
Output Offset Voltage Variation	Over entire gain range	-500		+500	mV
Maximum Output Voltage Swing	Set by BYP1 pin	2.6			Vpp
Differential Input Resistance	(IN+) - (IN-) = 100 mVp-p @ 2.5 MHz	4	5.4	7.5	kΩ
Differential Input Capacitance	(IN+) - (IN-) = 100 mVp-p @ 2.5 MHz		4	10	pF
Single-Ended Input	R/$\overline{W}$ = high, IN+ or IN-	2	2.7	3.8	kΩ
Impedance	R/$\overline{W}$ = low, IN+ or IN-		160	250	Ω
Input Noise Voltage	Gain set to maximum		5	15	nV/$\sqrt{Hz}$
Bandwidth	-3 dB bandwidth at maximum gain	30			MHz
OUT+ & OUT- Pin Current	No DC path to AGND	±2.5	±4.0		mA
CMRR (Input Referred)	(IN+) = (IN-) = 100 mVp-p @ 5 MHz, gain set to max	40			dB

AGC AMPLIFIER (continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
PSRR (Input Referred)	VCC1, 2 = 100 mVp-p @ 5 MHz, gain set to max	30			dB
(DIN+) - (DIN-) Input Swing vs. AGC1 Input (DIN+) - (DIN-) = (V_{AGC1}-K1) • K2 K2	25 mVp-p ≤ (IN+) - (IN-) ≤ 250 mVp-p, $\overline{HOLD}$ = high, 0.5 Vp-p ≤ (DIN+) - (DIN-) ≤ 1.5 Vp-p	.54	.64	.74	Vp-p/V
K1		0.5	0.75	1.0	V
(DIN+) - (DIN-) Input Voltage Swing Variation	25 mVp-p ≤ (IN+) - (IN-) ≤ 250 mVp-p			5.0	%
AGC1 Voltage	AGC1 open	1.8	2.2	2.7	V
AGC1 Pin Input Impedance		4.8	6.5	9.5	kΩ
Slow AGC Discharge Current	(DIN+) - (DIN-) = 0V	2.8	4.5	6.5	µA
Fast AGC Discharge Current	Starts at 0.9 µs after R/$\overline{W}$ goes high, stops at 1.8 µs	0.07	0.12	0.18	mA
BYP1 Leakage Current	$\overline{HOLD1}$ = low, 10 ≤ Gain ≤ 80	-0.2		+0.2	µA
Gain Pin Leakage Current	$\overline{HOLD2}$ = low, 10 ≤ Gain ≤ 80	-0.2		+0.2	µA
Slow AGC Charge Current	(DIN+) - (DIN-) = .563 VDC, V_{AGC1} = 2.3 V	-0.11	-0.18	-0.27	mA
Fast AGC Charge Current	(DIN+) - (DIN-) = 0.8 VDC, V_{AGC1} = 2.3 V	-0.9	-1.4	-2.1	mA
Fast to Slow Attack Switchover Point	$\frac{[(DIN+)-(DIN-)]}{[(DIN+)-(DIN-)]FINAL}$	110		140	%
Gain Decay Time (Td)	(IN+) - (IN-) = 250 mVp-p to 125 mVp-p @ 2.5 MHz, (OUT+) - (OUT-) to 90% final value	12	20	36	µs
	(IN+) - (IN-) = 50 mVp-p to 25 mVp-p at 2.5 MHz (OUT+) - (OUT-) to 90% final value	38	60	110	µs
Gain Attack Time	R/$\overline{W}$ low to high (IN+) - (IN-) = 250 mVp-p @ 2.5 MHz, (OUT+) - (OUT-) to 110% final value	.8	2	3.6	µs

HYSTERESIS COMPARATOR

Unless otherwise specified, recommended operating conditions apply. Input (DIN+) - (DIN-) is an AC coupled, 1.0 Vp-p, 2.5 MHz sine wave. 0.5 VDC is applied to the HYS pin. R/$\overline{W}$ pin is high.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Input Signal Range				1.5	Vp-p
Differential Input Resistance	(DIN+) - (DIN-) = 100 mVp-p @ 2.5 MHz	8	10	14	kΩ
Differential Input Capacitance	(DIN+) - (DIN-) = 100 mVp-p @ 2.5 MHz		3.0	5.0	pF
Single-Ended Input Impedance	DIN+ or DIN-	4	5	7	kΩ
Slope of Level Gain	Calculated from 0.6 < DIN± < 1.5 Vppd	.85	1	1.2	V/Vp-p
Intercept of Level Gain	DIN± = 0 Vppd	0	0.13	0.26	V
Level Gain		Slope + (Intercept / DIN ppd)			
Level Pin Output Impedance	I_{LEVEL} = 0.2 mA	100	200	300	Ω
Level pin Maximum Output Current		1.5			mA
Slope of Hysteresis Gain	Calculated from 0.3V < HYS < 1.0V	0.32	0.36	0.44	V/V
Intercept of Hysteresis Gain	HYS = 0	-0.04	-0.025	0	V
Hysteresis Gain		Slope + (Intercept / HYS Voltage)			
HYS Pin Current	0.3V < HYS < 1.0V	0.0		-5	µA
Tracking Hysteresis Threshold Tolerance		-15		+15	%
DOUT Pin Output Low Voltage	5 kΩ from DOUT to GND	VCC -2.5	VCC -2.0	VCC -1.35	V
DOUT Pin Output High Voltage	5 kΩ from DOUT to GND	VCC -2.0	VCC -1.6	VCC -1.1	V

ACTIVE DIFFERENTIATOR

Unless otherwise specified, recommended operating conditions apply. Input (CIN+) - (CIN-) is an AC-coupled, 1.0 Vp-p, 2.5 MHz sine wave. 100Ω in series with 65 pF are tied from DIF+ to DIF-.

Input Signal Range				1.5	Vp-p
Differential Input Resistance	(CIN+) - (CIN-) = 100 mVp-p @ 2.5 MHz	8	10	14	kΩ
Differential Input Capacitance	(CIN+) - (CIN-) = 100 mVp-p @ 2.5 MHz		3.0	5.0	pF
Single-Ended Input Impedance	CIN+ or CIN-	4	5	7	kΩ
Voltage Gain From CIN± to DIF±	(DIF+ to DIF-) = 2 kΩ		1		V/V
DIF+ to DIF- Pin Current	Differentiator impedance must be set so as to not clip the signal for this current level	±0.7			mA

ACTIVE DIFFERENTIATOR (Continued)

Unless otherwise specified, recommended operating conditions apply. Input (CIN+) - (CIN-) is an AC-coupled, 1.0 Vp-p, 2.5 MHz sine wave. 100Ω in series with 65 pF are tied from DIF+ to DIF-.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
COUT Pin Output Low Voltage	5 kΩ from COUT to GND	VCC -2.5	VCC -2.0	VCC -1.35	V
COUT Pin Output High Voltage	5 kΩ from COUT to GND	VCC -2.0	VCC -1.6	VCC -1.1	V
COUT Pin Output Pulse Width		22	35	52	ns

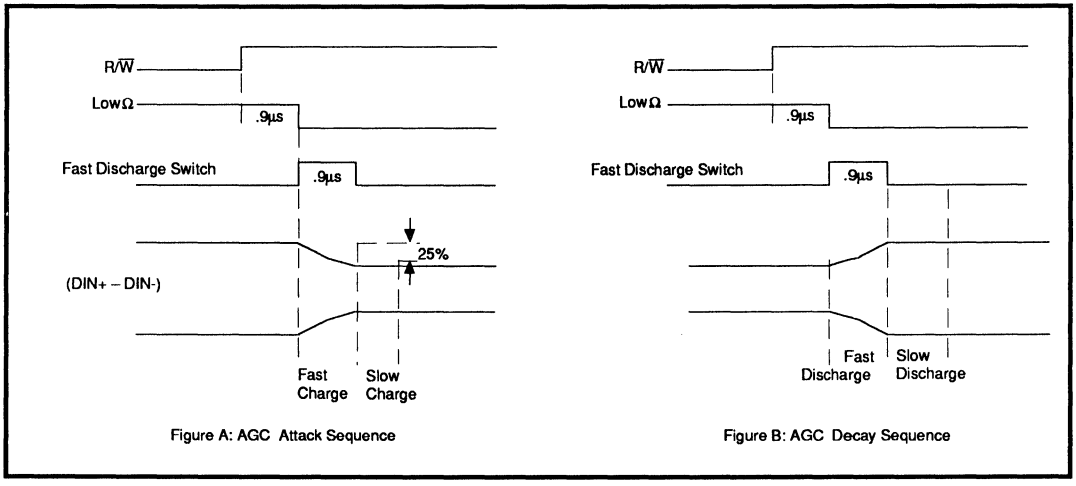


Figure A: AGC Attack Sequence

Figure B: AGC Decay Sequence

FIGURE 6: AGC Timing Diagram

OUTPUT DATA CHARACTERISTICS (See Figure 7)

Unless otherwise specified, recommended operating conditions apply. Inputs (CIN+) - (CIN-) and (DIN+) - (DIN-) are in-place as an AC coupled, 1.0 Vp-p, 2.5 MHz sine wave. 100Ω in series with 65 pF are tied from DIF+ to DIF-. 0.5V is applied to the HYS pin. $\overline{RD}$ is loaded with a 4 kΩ resistor to VCC and a 10 pF capacitor to DGND. ENABLE and R/$\overline{W}$ pins are high.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Td1	D Flip-Flop Set Up Time	Minimum allowable time delay from (DIN+) - (DIN-) exceeding hysteresis point to (DIF+) - (DIF-) hitting a peak value.	0			ns
Td3	Propagation Delay			15	40	ns
|Td3-Td4|	Pulse Pairing	2.5 MHz sine wave input			1.5	ns
|Td3-Td4|	Pulse Pairing	4 MHz sine wave input			1.0	ns
Td5	Output Pulse Width		22	35	52	ns

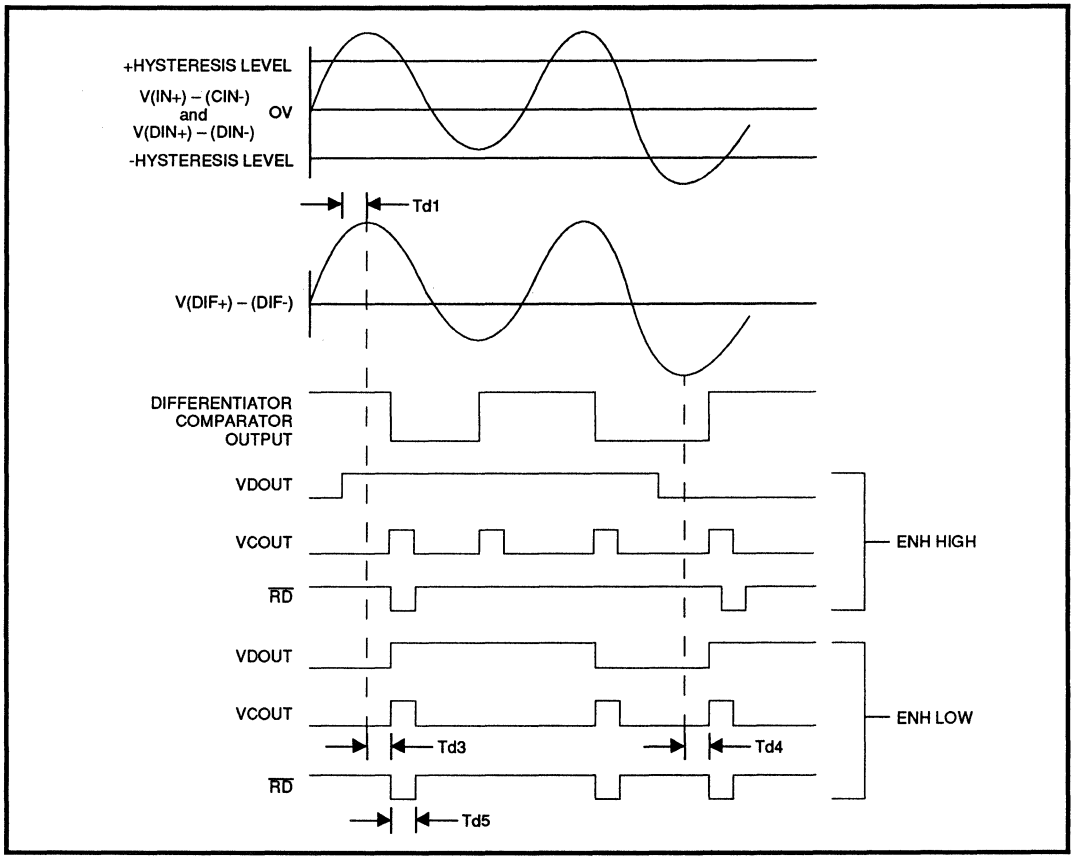


FIGURE 7: Read Mode Digital Section Timing Diagram

SERVO SECTION (Unless otherwise specified, recommended operating conditions apply.), LATCH A/B = Low, RST A/B = High, CS Pin Open

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VREF Voltage Range		2.25	2.5	2.75	V
VREF Pin Input Impedance		30			kΩ
AGC2 Pin Voltage	AGC2 Pin Open,	1.8	2.3	2.7	V
AGC2 Pin Input Impedance		4.8	6.5	9.5	kΩ
BURSTA/B pin Output Voltage vs (DIN+) – (DIN-)	$\overline{LATCHA/B}$ = Low $\frac{V_{BURSTA/B} - VREF}{(DIN+)-(DIN-)} = 1.5\,V/Vp\text{-}p$	-20		+10	%

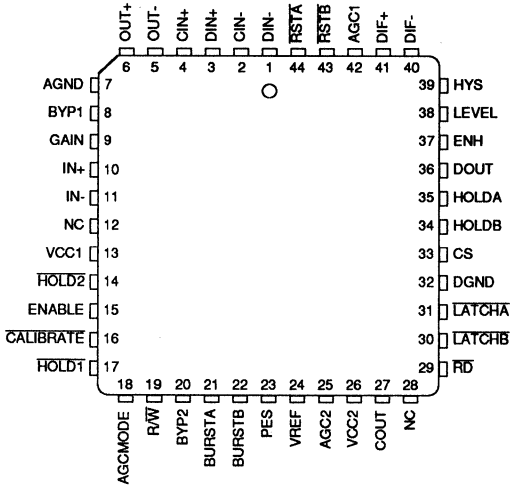
SERVO SECTION (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
BURSTA/B Output Offset Voltage V_{BURST} - VREF	I(HOLDA) = I(HOLDB) =-20 µA, $\overline{LATCHA}$, $\overline{B}$ = Low CS pin open (DIN+) = (DIN-)	-150		+150	mV
BURSTA - BURSTB Output Offset Match	$\overline{LATCHA/B}$ = low (DIN+) = (DIN-)	-15		+15	mV
Maximum PES Pin Output Voltage	Controlled by AGC2			VCC1-1.5	Vpp
PES Pin Output Offset Voltage	V_{PES} - VREF, (DIN+) = (DIN-) $\overline{LATCHA/B}$ = Low	-15		+15	mV
Output Resistance, BURSTA/B & PES pins	I_{LOAD} ± 500 µA			50	Ω
Hold A/B Charge Current	$\overline{LATCHA/B}$ = Low	8			mA
HOLDA/B Discharge Current Tolerance	$\overline{RSTA/B}$ = Low, CS pin open	0.8	1.5	2.2	mA
	$\overline{RSTA/B}$ = High, $\overline{LATCHA/B}$ = High	-0.2		+0.2	µA
Load Resistance BURSTA/B, PES pins	Resistors to GND	10.0			kΩ
Load Capacitance BURSTA/B, PES pins				20	pF
$\overline{LATCHA/B}$ pin set up time	(Tds1 in Figure 5)	150			ns
$\overline{LATCHA/B}$ pin Hold Time	(Tds2 in Figure 5)	150			ns
Channel A/B Discharge Current Turn On time	(Tds3 in Figure 5)			150	ns
Channel A/B discharge Current Turn Off time	(Tds4 in Figure 5)			150	ns
BYP2 Pin Leakage Current	$\overline{HOLD2}$ = Low	-0.2		+0.2	µA
BYP2 Pin Charge/Discharge Current $I_C = K_4[(K_5 \cdot V_{AGC2}) - V_{A(DIN)pp} - V_{B(DIN)pp}]$	K_4, $\overline{HOLD2}$ = High	400	640	880	µA/Vpp
	K_5, $\overline{HOLD2}$ = High	0.4	0.5	0.7	V/V
Maximum BYP2 pin charge/discharge current		190	300	450	µA
V_{PES} pp vs. V_{AGC2}	V_{PES} pp/V_{AGC2}	1.18	1.33	1.5	Vpp/V
	V_{PES} pp Swing AGC2 = Open	2.4	3	3.6	Vpp

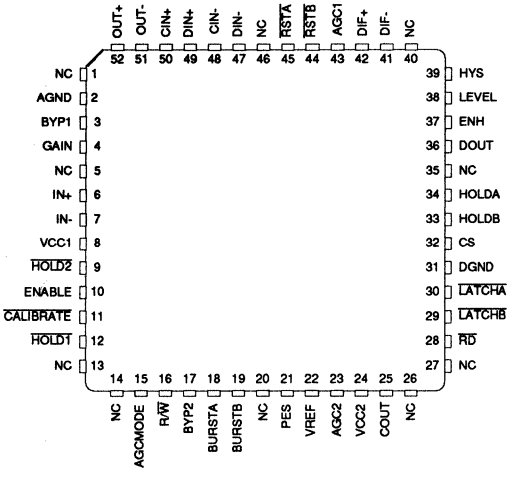
SSI 32P3030
Pulse Detector
and Servo Demodulator

PACKAGE PIN DESIGNATION
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



44-Pin PLCC



52-Pin QFP

THERMAL CHARACTERISTICS: θja

44-Pin PLCC	60° C/W
52-Pin QFP	75° C/W

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32P3030 44-Pin PLCC	32P3030-CH	32P3030-CH
SSI 32P3030 52-Pin QFP	32P3030-CG	32P3030-CG

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 731-7110, FAX (714) 573-6914

silicon systems®
A TDK Group Company

SSI 32P3040
Pulse Detector with Programmable Filter
Preliminary Data

November 1991

2

DESCRIPTION

The SSI 32P3040 is a bipolar integrated circuit that provides all data processing necessary for detection and qualification of encoded read signals. The circuit will handle a data rate of 24 Mbit/s.

In read mode the SSI 32P3040 provides amplification and qualification of head preamplifier outputs. Pulse qualification is accomplished using level qualification of differentiated input zero crossings. An AGC amplifier is used to compensate for variations in head preamp output levels, presenting a constant input level to the pulse qualification circuitry. The AGC loop can be disabled so that a constant gain can be used for embedded servo decoding or other processing needs.

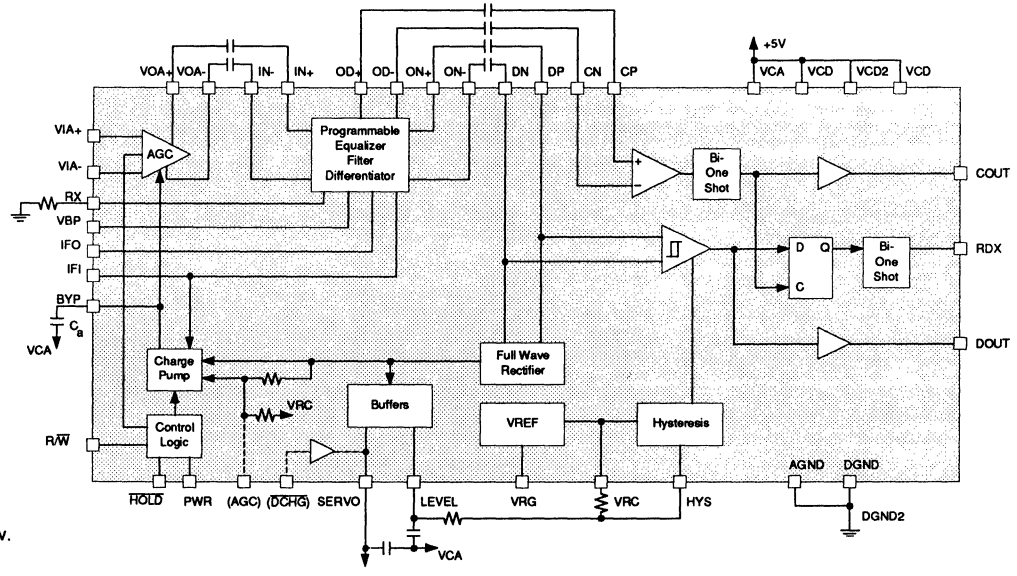
Write to read transient recovery is enhanced by providing AGC input impedance switching and a selectable Fast Recovery mode that provides a higher decay current.

Additionally, the SSI 32P3040 contains an integrated programmable electronic filter with cutoff frequencies between 2.5 and 13 MHz. High frequency boost (for pulse slimming) of up to +9db is also provided. The SSI 32P3040 requires only a +5V power supply and is available in a 36-pin SOM package.

FEATURES

- **Compatible with 24 Mbit/s data rate operation**
- **Fast attack/decay modes for rapid AGC recovery**
- **Dual rate charge pump for fast transient recovery charge pump currents track programmable channel bandwidth**
- **Low drift AGC hold, fast AGC recovery, and low AGC input impedance control signals. Circuitry supports programmable gain non-AGC operation**
- **Temperature compensated, exponential control AGC**
- **Precision wide bandwidth fullwave rectifier**
- **Supports programmable pulse slimming equalization and programmable channel filter and differentiator with no external filter components**
- **±2% Filter group delay variation from .3FC to FC**
- **Servo burst output available**
- **Differential hysteresis qualifier comparator to ease clock channel timing**
- **Accurate feed forward or fixed threshold set**

BLOCK DIAGRAM



SSI 32P3040
Pulse Detector with Programmable Filter

FEATURES (continued)

- 1 ns max pulse pairing with sine wave input
- 5 mW low power idle mode
- TTL read data output
- +5V only operation
- 36-pin SOM package

FUNCTIONAL DESCRIPTION

The SSI 32P3040 Pulse Detector is designed to support a 24 Mbit/s data rate. The signal processing circuits include a wide band variable gain amplifier, a programmable electronic filter, differentiator and pulse slimming equalizer, a precision wide bandwidth fullwave rectifier, and a dual rate charge pump. A fully differential filter, differentiator, equalizer, and fullwave rectifier are provided to minimize external noise pickup. To optimize recovery for constant density recording, the AGC charge pump current tracks the programmable filter current IFI. The differentiator zero tracks the programmable filter cutoff frequency. Thus in constant density recording applications, an approximately constant differentiated signal amplitude is maintained. The desired filter response and equalization are easily programmed with the SSI 32D4661, Time Base Generator DACs. A dual rate attack charge pump and a Fast Decay mode are included for fast transient recovery. At maximum IFI current, the normal AGC attack current is .18 mA. When the signal exceeds 125% of the nominal signal level, the attack current is increased by a factor of 7. The nominal decay current at max IFI is 4 µA. The decay current is increased 20 times when in the fast decay mode. In this mode, transients that produce low gain will recover more rapidly with the fast decay current, while transients that produce high gain will put the circuit in the fast attack recovery mode. The decay modes are automatically controlled within the device. When R/$\overline{W}$ is low, the AGC is in its hold mode and its input impedance is switched low. When R/$\overline{W}$ is switched high, the AGC remains in the hold and low input impedance state for .7 µs and then switches to the fast decay mode for .7µs. The AGC amplifier input impedance is reduced to allow quick recovery of the AGC amplifier input AC coupling capacitors. When the $\overline{HOLD}$ input is low, the AGC action is stopped and the AGC amplifier gain is set by the voltage at the BYP pin. In most applications, the BYP pin voltage is stored on an external capacitor when $\overline{HOLD}$ goes low. In applications where AGC action is not desired, the BYP voltage can be set by a resistor divider network connected from VCC to VRC. If a programmable gain is desired, the resistor network could be driven by a current DAC. The precision fullwave rectifier produces an accurate Level and Servo output signal. These outputs are referenced to the reference voltage VRC. SERVO and LEVEL are buffered open emitter outputs with 100 ohm series current limiting resistors. These outputs could be further filtered with external capacitors.

LEVEL has an internal 50 µA discharge current source. An optional Servo output capacitor discharge circuit can be included. An external resistor connected to the RX pin sets the electronic filter reference current which is the source from pin IFO. If a programmable frequency response is desired, a portion of the current from IFO, which is proportional to absolute temperature, must be injected into pin IFI. This could be accomplished by a current DAC. Some frequency response programming may be accomplished by connecting IFO to IFI and switching different resistors to pin RX. Frequency boost is accomplished by varying the voltage at VBP. VBP has a nominal 100 mV built-in offset so that the circuit has 0 dB boost for VBP below 100 mV. The voltage at VBP should be proportional to the reference voltage at pin VRG.

A differential comparator with floating hysteresis threshold allows differential signal qualification for noise rejection. An accurate feed forward qualification level is generated by comparing the difference between LEVEL and VRC. VRC is referenced to VCA. Thus with the VTH resistor network connected from VCA to VRC, an accurate fixed threshold can be established. The threshold is clamped to a minimum value of 50 mV. Thus a qualified signal must exceed this minimum level even when the VTH_VRC voltage is zero. A qualified signal zero crossing triggers the output one shot. The one shot period is set internally. Low level differential outputs are provided for high speed operation and to minimize noise generation.

PIN DESCRIPTION

INPUT PINS

NAME	TYPE	DESCRIPTION
VIA+, VIA-	I	AGC Amplifier input pins.
IN+, IN-	I	Equalizer/filter input pins.
DP, DN	I	Data inputs to data comparators and fullwave rectifier.
CP, CN	I	Differentiated data inputs to the clock comparator.
HYS	I	Threshold level setting input for the data comparators.
R/$\overline{W}$	I	TTL compatible input when high puts the charge pump in the normal mode.
PWR	I	TTL compatible input when high puts the circuit in its normal operating mode.
$\overline{HOLD}$	I	TTL compatible input when low disables the AGC action by turning off the charge pump.
$\overline{DCHG}$	I	Optional TTL compatible input pin when low produces a discharge current at the SERVO pin. Not available in 36 pin SO package.
OUTPUT PINS		
VOA+, VOA-	O	AGC amplifier output pins.
ON+, ON-	O	Equalizer/filter normal output pins.
OD+, OD-	O	Equalizer/filter differentiated output pins.
DOUT	O	Test point for monitoring the data F/F D-input. Usage requires an external 2.4K resistor from DOUT to GND.
COUT	O	Test points for monitoring the data F/F clock inputs. Usage requires an external 2.4K resistor from DOUT to GND.
$\overline{RD}$	O	TTL compatible read data output pins.
LEVEL	O	Open NPN emitter output that provides a fullwave rectified signal for the VTH input. The signal is referenced to VRC.
SERVO	O	Open NPN emitter output that provides a fullwave rectified servo signal. The signal is referenced to VRC.
ANALOG PINS		
VRC	-	Reference voltage pin for SERVO and LEVEL. VRC is referenced to VCA.
VRG	-	Reference voltage pin for the programmable filter. VRG is referenced to ground.
VBP	-	The equalizer high frequency boost is set by an external voltage applied to this pin. VBP must be proportional to VRG. Programmable boost is implemented by using a DAC that uses VRG as its reference. A fixed amount of boost can be set by an external resistor divide network connected from VBP to VRG and GND.
RX	-	Pin to set filter reference current. External resistor Rx from this pin to ground sets the filter reference current IFO.
IFO		Reference current output pin. The reference current is normally supplied as the reference current to a current DAC which generates the programmable input current for the IFI pin.

PIN DESCRIPTION (Continued)

ANALOG PINS (Continued)

NAME	TYPE	DESCRIPTION
IFI		Programmable filter input current pin. The filter cutoff frequency is proportional to the current into this pin. The current must be proportional to the reference current out of IFO. A fixed filter cutoff frequency is generated by connecting IFO to IFI and selecting Rx to set the desired frequency.
AGC		Optional reference voltage input for the AGC. The reference voltage is normally set by an internal resistor divider for VCC to VRC. (Not available in 36 pin SO package).
BYP		The AGC integrating capacitor C_A is connected between BYP and VCA.
VCA, VCD,VCD2		Analog and Digital +5 volts.
AGND1, DGND1, DGND2		Analog and Digital grounds.

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, 4.65<VCC<5.25, 0°C<Ta<70°C

ABSOLUTE MAXIMUM RATINGS (Operation above maximum ratings may damage the device.)

PARAMETER	VALUE	UNIT
Storage Temperature	-65 to +150	°C
Junction Operating Temperature,Tj	+130	°C
Supply Voltage, VCA, VCD	-0.7 to 7	V
Voltage Applied to Inputs	-0.5 to VCA, VCD +0.5	V

POWER SUPPLY

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
ISS	Supply Voltage Current	Active mode		80		mA
		Low-Power mode		1		mA
PD	Power Dissipation	Active mode		400		mW
		Low-Power mode		5		mW

RECOMMENDED OPERATING CONDITIONS

PARAMETER		RATING	UNIT
Supply Voltage	VCA = VCD = VCC	4.65<VCC<5.25	V
Ambient Temperature, Ta		0<Ta<70	°C

LOGIC SIGNALS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VIL	TTL Input Low Voltage		-0.3		0.8	V
VIH	TTL Input High Voltage		2.0		VCC +0.3	V
IIL	TTL Input Low Current	VIL = 0.4V			-0.4	mA
IIH	TTL Input High Current	VIH = 2.7V			0.1	mA
VOH	TTL Output High Voltage	IOH = -400µA	2.4			V
VOL	TTL Output Low Voltage	IOL = 3 mA			0.5	Vpp
TRDRF	Output Rise and Fall Time	CL = 15 pF			7	ns
TH	Hold Input Switching Times				0.3	µs
TWR	Write to Read Input Short Time	R/$\overline{W}$ pin low to high	0.5		1.4	µs

AGC AMPLIFIER

The input signals are AC coupled to VIA+ and VIA-. VOA+ and VOA- are AC coupled to IN+ and IN-. ON+ and ON- are AC coupled to DP and DN. Ca 1000 pF. Fin = 4 MHz. Unless otherwise specified, the output is measured differentially at VOA+ and VOA-, Fin = 4 MHz and filter boost at Fc = 0dB.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VIR	Input Range	Filter boost at FC = 0 dB	24		240	mVppd
		Filter boost at FC = 9 dB	20		120	mVppd
VDPN	DP-DN voltage	(VIA+) - (VIA-) = 0.1 Vpp	.90		1.10	Vppd
VDPNV	DP-DN Voltage Variation	24 mV < (VIA+) - (VIA-) < 240 mV			8.0	%
AV	Gain Range		1.9		22	V/V
AVPV	Gain Sensitivity			28		dB/V
VOADR	VOA+, VOA- Dynamic Range	THD = 1% max	.75			Vpp
ZIN	Input Impedance	R/$\overline{W}$= high	4.0		8.4	kΩ
ZCMIN	Common Mode	R/$\overline{W}$ = high		1.8		kΩ
	Input Impedance	R/$\overline{W}$ = low		250		Ω
VOS	Output Offset Voltage Variation	Over gain range	-200		+200	mV
VINO	Input Noise Voltage	gain = max, filter not connected to VOA+, VOA-, Rs = 0Ω			15	nV$\sqrt{Hz}$
BW	Bandwidth	No AGC action	45			MHz
CMRR	Common-mode Rejection Ratio	gain = max, f = 5 MHz	40			dB
PSRR	Power Supply Rejection Ratio	gain = max, f = 5 MHz	45			dB
TGD	Gain Decay Time	VIA+ VIA- = 240 mV to 120 mV VOA+ VOA- >0.9 Final Value BYP ≥, 1000 pF		31		µs
TGA	Gain Attack Time	VIA+ VIA- = 120 mV to 240 mV VOA+ VOA- <1.1 Final Value BYP ≥, 1000 pF		2		µs

ELECTRICAL SPECIFICATIONS (continued)

Unless otherwise specified, 4.65<VCC<5.25, 0°C<Ta<70°C

AGC CONTROL

The input signals are AC coupled to DP and DN. Ca = 1000 pF, LEVEL load = 50 µA, SERVO load = 100 µA.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VDI	DP-DN Signal Input Range				1.4	Vpp
ALO	Level (Servo) Output Gain	DP-DN = .5 to 1 Vpp	.712		.788	V/Vpp
BWL	Level (Servo) Output Bandwidth	1 dB	15			MHz
VLO	Level Offset Voltage	Output-VRC, IL = 50 µA			30	mV
VSO	Servo Offset Voltage	Output - VRC, IL = 100 µA			30	mV
ZLS	Level (Servo) Output Impedance	IL = 100 µA		400		Ω
ID	Discharge Current			0.008 x IFI		mA
IDF	Fast Discharge Current	0.7 to 1.4 µs after R/$\overline{W}$ goes high		20 x Id		mA
ICH	Charge Pump Attack Current			40 x Id		mA
ICHF	Charge Pump Fast Attack Current	DP-DN = 1.35 Vpp		7 x Ich		mA
IBYP	Pin Leakage Current	$\overline{HOLD}$ = low	-0.1		0.1	µA
VRC	Reference Voltage		VCC-2.47		VCC-2.2	V
IVRC	Output Drive		-.75		.75	mA
VRG	Reference		2.2		2.45	V
IVRG	Source Current		1			mA
VAGC	Pin Voltage			VRC+1.0		V

EQUALIZER/FILTER The input signals are AC coupled to IN+ and IN-.

fc	Filter Cutoff Frequency	$fc = \frac{22.5\text{MHz}}{\text{mA}}(\text{IFI})$ IFI = 0.11 to .6 mA, TA = 25°C	2.5		13.5	MHz
V_{RX}	PTAT Reference Current Set Output Voltage	TA = 25°C I_{RX} = 0 - 0.6 mA Rx > 1.25 kΩ		750		mV
IFOR	PTAT Reference Current Output Current Range	TA = 25°C 1.25 kΩ < Rx < 6.8 kΩ IFO = V_{RX}/Rx V_{RX} = 750 mV	0.11		0.6	mA

EQUALIZER/FILTER (continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
IFIR	PTAT Programming Current Range	TA = 25°C, VRX = 750 mV	0.11		0.6	mA
VBPR	Input Voltage Range		0		VRG	V
IBP	Input Bias Current				3	µA
FCA	Filter FC Accuracy	FC = 5 to 13.5 MHz	-10		+10	%
AO	[(ON+)-(ON-)]/[(IN+)-(IN-)] Normal Gain	F = 0.67 FC	1.6		2.4	V/V
AD	[(OD+)-(OD-)]/[(IN+)-(IN-)] Diff Gain	F = 0.67 FC	0.9AO		1.1AO	V/V
FB	Frequency Boost at FC	FB = 20 log [1.884(VBP-.1) /VR+1] VBP -0.1>0	0		9	dB
FBA	Frequency Boost Accuracy	FB = 9 dB	-1		+1	dB
TGD	Group Delay Variation	0.3 FC to FC = 13.5 MHz FB = 0 to 9 dB	-2		+2	%
VOO	Output Offset Voltage	Variation over entire gain range	-200		+200	mV
VOF	Filter Output Dynamic Range	THD = 1.5% max F = 0.67 FC	1.5			Vpp
RINF	Filter Input Resistance		3.0			kΩ
CINF	Filter Input Capacitance				7	pF
RO	Filter Output Resistance	IO = 0.5 mA		70	85	Ω
IFOD	Filter Output Drive Current		-1		+1	mA
VNN	Eout Output Noise Voltage ON+ ON-	BW = 100 MHz, Rs = 50Ω IFI = 0.8 mA, VBP = 0		2.2		mVRMS
		BW = 100 MHz, Rs = 50Ω IFI = 0.8 mA, VBP = VRG		3.4		mVRMS
VND	Eout Output Noise Voltage OD+ OD-	BW = 100 MHz, Rs = 50Ω IFI = 0.8 mA, VBP = 0		5.4		mVRMS
		BW = 100 MHz, Rs = 50Ω IFI = 0.8 mA, VBP = VRG		9		mVRMS

DATA COMPARATOR

The input signals are AC coupled to DP and DN.

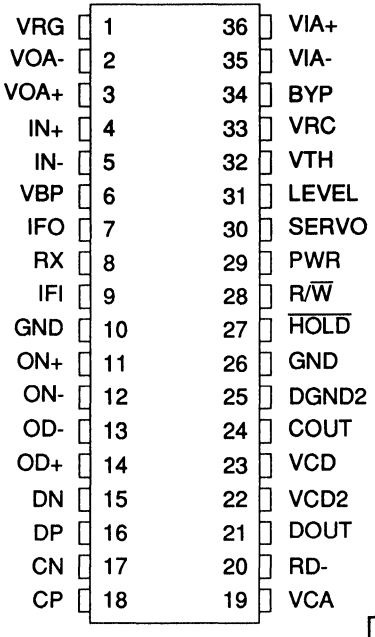
DR	DP-DN Signal Range				1.5	Vpp
RINDC	Differential Input Resistnace		8		14	kΩ
CINDC	Differential Input Capacitance				5	pF
ATH	Threshold Voltage Gain, Kth	0.3 < VTH-VRC < .75	0.41		0.48	V/V
VIAMIN	Minimum Threshold Voltage	VTH-VRC ≤ 0.11V		.05		V
TPDDC	Propagation Delay	To DO+, DO-		10		ns
ITH	VTH Input Bias Current				2	µA
DOUTSS	DOUT Signal Swing	2.4K from DOUT to GND		0.5		V

CLOCKING

The input signals are AC coupled to CP and CN.

CR	CP-CN Signal Range				1.5	Vpp
RINCL	Differential Input Resistance		8		14	kΩ
CINCL	Differential Input Capacitance				5	pF
TDS	D F/F Set Up Time	DP-DN threshold to CP-CN zero cross	0			ns
TPP	Pulse Pairing	Vs = 1Vpp, F = 2.5 MHz			1	ns
TPDCL	Propagation Delay to RD	Vs = 20 mVpp sq wave		14		ns
RDPW	Output Pulse Width	Measured at 1.4V level	10		33	ns
COUTS	Signal Swing	2.4K from COUT to GND		0.5		V

PACKAGE PIN DESIGNATIONS
(Top View)



36-Pin SOM

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32P3040 36-Pin Small Outline	32P3040-CM	32P3040-CM

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 731-7110, FAX (714) 573-6914

Notes:

Section

PROGRAMMABLE ELECTRONIC FILTERS

3

silicon systems®
A TDK Group Company

SSI 32F8000
Low-Power Programmable Electronic Filter

Advance Information

November 1991

3

DESCRIPTION

The SSI 32F8000 Programmable Electronic Filter provides an electronically controlled low–pass filter with a separate differentiated low–pass output. A seven–pole, low–pass filter is provided along with a single-pole, single-zero differentiator. Both outputs have matched delays. The delay matching is unaffected by any amount of programmed equalization or bandwidth. This programability combined with low group delay variation makes the SSI 32F8000 ideal for use in constant density recording applications. Pulse slimming equalization is accomplished by a two–pole, low–pass with a two–pole, high–pass feed forward section to provide complimentary real axis zeros. A variable attenuator is used to program the zero locations.

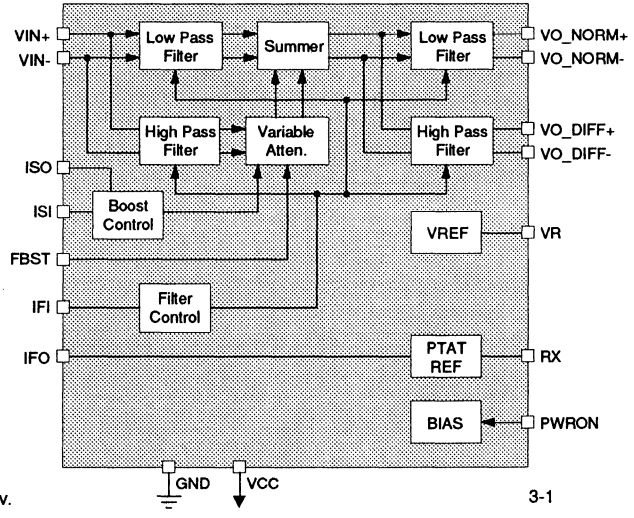
The SSI 32F8000 programmable equalization and bandwidth characteristics can be controlled by external DACs. Fixed characteristics are easily accomplished with three external resistors, in addition equalization can be switched in or out by a logic signal.

The SSI 32F8000 requires only a +5V supply and is available in 16-pin DIP, SON, and SOL packages.

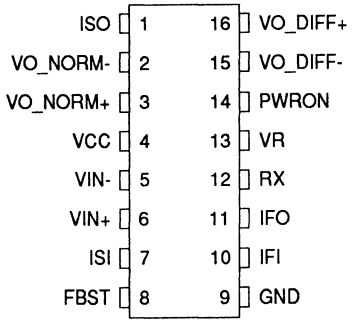
FEATURES

- **Ideal for multi-rate systems applications**
- **Programmable filter cutoff frequency (fc = 9 to 27 MHz)**
- **Programmable pulse slimming equalization (0 to 13 dB boost at the filter cutoff frequency)**
- **Matched normal and differentiated low-pass outputs**
- **Differential filter input and outputs**
- **±10% cutoff frequency accuracy**
- **±2% maximum group delay variation from 9 - 27 MHz**
- **Total harmonic distortion less than 1.5%**
- **No external filter components required**
- **+5V only operation**
- **16-pin DIP, SON, and SOL package**

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

SSI 32F8000
Low-Power Programmable Electronic Filter

FUNCTIONAL DESCRIPTION

The SSI 32F8000 is a high performance programmable electronic filter. It features a 7-pole 0.05° equiripple linear phase filter with matched normal and differentiated outputs.

CUTOFF FREQUENCY PROGRAMMING

The cutoff frequency, fc, of the SSI 32F8000 is defined as the -3dB filter bandwidth with no magnitude equalization applied, and is programmable from 9 MHz to 27 MHz.

The cutoff frequency is programmable with 3 pins: RX, IFO and IFI. At the RX pin, an external resistor to ground establishes the IFO reference current,

$$IFO = \frac{0.75}{RX}, \text{ at } T = 27°C.$$

IFI should be made proportional to IFO for temperature stability. The cutoff frequency is related to the RX resistor, IFO and IFI currents as the following:

$$fc(MHz) = 27 \times \frac{IFI}{IFO} \times \frac{1.25}{Rx\ (k\Omega)}$$

The voltage at the RX pin is a proportional to absolute temperature reference voltage, which is ~ 750 mV @ T = 27 °C. The IFO output is a current source output, thus has high output impedance. The IFI input can be modeled as a diode in series with a 1.2 kΩ resistor.

For a fixed cutoff frequency setting, IFO and IFI can be tied together. The cutoff frequency equation then reduces to:

$$fc(MHz) = 27 \times \frac{1.25}{Rx\ (k\Omega)}$$

For programmable cutoff frequency, an external current DAC can be used. IFO should be the reference current into the DAC. The DAC output current drives IFI, which is then proportional to the IFO. The DACF in the SSI 32D4661 Time Base Generator is designed to control fc of the Silicon Systems programmable filters. When the DACF, which has a 4X gain from its reference to fullscale output, is used, a 5 kΩ RX is used. fc is then given as follows:

$$fc(MHz) = 27 \times \frac{F\_Code}{127}$$

where F_Code is the decimal code equivalent to the 7-bit digital input for the DACF.

MAGNITUDE EQUALIZATION PROGRAMMING

The magnitude equalization, measured in dB, is the amount of high frequency peaking at the cutoff frequency relative to the original -3 dB point. For example, when 12 dB boost is applied, the magnitude response peaks up 9 dB above the DC pain.

The magnitude equalization is programmable with two pins: ISO and ISI. ISO is a reference current which is proportional to the absolute temperature and on-chip resistance, 600 µA typicaly at T=27°C. The input at the ISI pin determines the amount of high frequency boost. The boost function is as follows:

$$\text{Boost (dB)} = 20 \log_{10} [3.46\ (\frac{ISI}{ISO}) + 1].$$

The ISO output is a current source output, thus has high output impedance. The ISI input has low input impedance and is biased at the bandgap voltage reference, VR.

For a fixed boost setting, one can set a current divider from ISO to ISI and VR. When two resistors of equal value are connected from ISO to ISI and ISO to VR, the ISO current is then divided equally into ISI and VR. For programmable equalization, an external current DAC can be used. ISO should be the reference current to the DAC. The DAC output current is then proportional to ISO.

For SSI 32F8000, the equalization function can be disabled when FBST is pulled to logic 0.

POWER ON / OFF

The SSI 32F8000 supports a power down mode for minimal idle dissipation. When PWRON is pulled up to logic 1, the device is in normal operation mode. When PWRON is pulled down to logic 0, or left open, the device is in the power down mode.

PIN DESCRIPTIONS

NAME	DESCRIPTION
VIN+, VIN-	DIFFERENTIAL SIGNAL INPUTS. The input signals must be AC coupled to these pins.
VO_NORM+, VO_NORM-	DIFFERENTIAL NORMAL OUTPUTS. The output signals must be AC coupled to the load.
VO_DIFF+ VO_DIFF-	DIFFERENTIAL DIFFERENTIATED OUTPUTS. These outputs should be AC coupled to the load also, to eliminate DC offsets.
RX	PTAT REFERENCE CURRENT SET. PTAT (proportional to absolute temperature) reference current IFO is equivalent to the current set on this pin by a resistor to GND.
IFI	FREQUENCY PROGRAM INPUT. The filter cutoff frequency FC, is set by an external current IFI, injected into this pin. IFI must be proportional to current IFO. This current can be set with an external current generator such as a DAC, referenced to IFO.
IFO	PTAT CURRENT REFERENCE OUTPUT. This pin ouputs a PTAT reference current which is externally scaled for control input into IFI.
ISI	FREQUENCY BOOST PROGRAM INPUT. The slimmer high frequency boost is set by an external current applied to this pin. ISI must be proportional to ISO. A fixed amount of boost can be set by an external resistor divider network connected from ISO to VR and ISI. No boost is applied if the FBST pin is grounded, or at logic low. V_{ISI} = VR
ISO	CURRENT REFERENCE OUTPUT. This pin outputs a reference current which can be scaled by diverting current to pin VR. This current is used to control frequency boost via connection to pin ISI.
FBST	FREQUENCY BOOST. A high logic level or open input enables the frequency boost circuitry.
PWRON	POWER ON. A high logic level circuit enables the chip. A low level or open pin puts the chip in a low power state.
VR	REFERENCE VOLTAGE. Internally generated reference voltage.
VCC	+5 VOLT SUPPLY.
GND	GROUND

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

PARAMETER	RATINGS	UNIT
Storage Temperature	-65 to +150	°C
Junction Operating Temperature, Tj	+130	°C
Supply Voltage, VCC	-0.5 to 7	V
Voltage Applied to Inputs	-0.5 to VCC	V

RECOMMENDED OPERATING CONDITIONS

PARAMETER	RATINGS	UNIT
Supply voltage, VCC	4.50 < VCC < 5.50	V
Ambient Temperature	0 < Ta < 70	°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified recommended operating conditions apply.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Power Supply Characteristics						
ICC	Power Supply Current	PWRON = 0.8V			1	mA
ICC	Power Supply Current	PWRON ≥ 2.2V		50	TBD	mA
PD	Power Dissipation	PWRON ≥ 2.2V, VCC = 5.0V		250	TBD	mW
		PWRON ≥ 2.2V, VCC = 5.5V		280	TBD	mW
DC Characteristics						
VIH	High Level Input Voltage	TTL input	2.0			V
VIL	Low Level Input Voltage				0.8	V
IIH	High Level Input Current	VIH = 2.7V			20	µA
IIL	Low Level Input Current	VIL = 0.4V			−1.5	mA
Filter Characteristics						
*fc	Filter Cutoff Frequency *(f -3dB)	$fc = \frac{45\ \text{MHz}}{\text{mA}}$ (IFI) IFI = 0.2 to 0.6 mA, Ta = 25°C	9.0		27.0	MHz
FCA	Filter fc Accuracy	fc = 18 MHz	−10		+10	%
AO	VO_NORM Diff Gain	F = 0.67 fc, FB = 0 dB	0.8		1.20	V/V
AD	VO_DIFF Diff Gain	F = 0.67 fc, FB = 0 dB	0.90AO		1.1AO	V/V
FB	Frequency Boost at fc	$FB(db) = 20 \log \left[3.46 \left(\frac{ISI}{ISO} \right) + 1 \right]$		13.0		dB
FBA	Frequency Boost Accuracy	ISI/ISO = 0.5255	−1		+1	dB
TGDO	Group Delay Variation Without Boost	fc = 27 MHz, ISI = 0mA F = 0.2 fc to fc	−500		+500	ps
		fc = 9 MHz - 27 MHz F = 0.2 fc to fc, ISI = 0mA	−2		+2	%
		fc = 9 MHz - 27 MHz, ISI = 0mA F = fc to 1.75 fc	-3		+3	%

ELECTRICAL CHARACTERISTICS, (Continued)
Unless otherwise specified recommended operating conditions apply.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Filter Characteristics, continued						
TGDB	Group Delay Variation With Boost	*fc* = 27 MHz, ISI = ISO F = 0.2 *fc* to *fc*	–500		+500	ps
		fc = 9 MHz - 27 MHz F = 0.2 *fc* to *fc*, ISI = ISO	–2		+2	%
		fc = 9 MHz - 27 MHz, ISI = ISO F = *fc* to 1.75 *fc*	-3		+3	%
VIF	Filter Input Dynamic Range	THD = 1% max, F = 0.67 *fc*	1.0			Vpp
		THD = 1.5% max, F = 0.67 *fc*	1.5			Vpp
VOF	Filter Output Dynamic Range	THD = 1% max, F = 0.67 *fc* $R_{LOAD} \geq 1k\Omega$	1.0			Vpp
RIN	Filter Diff Input Resistance		3.0			kΩ
CIN	Filter Input Capacitance				7	pF
EOUT	Output Noise Voltage Differentiated Output	BW = 100 MHz, Rs = 50Ω *fc* = 27 MHz, ISI = 0mA		3.6		mVRms
EOUT	Output Noise Voltage Normal Output	BW = 100 MHz, Rs = 50Ω *fc* = 27 MHz, ISI = 0mA		2.2		mVRms
EOUT	Output Noise Voltage Differentiated Output	BW = 100 MHz, Rs = 50Ω *fc* = 27 MHz, ISI = ISO		5.8		mVRms
EOUT	Output Noise Voltage Normal Output	BW = 100 MHz, Rs = 50Ω *fc* = 27 MHz, ISI = ISO		2.9		mVRms
IO–	Filter Output Sink Current		1.0			mA
IO+	Filter Output Source Current		2.0			mA
RO	Filter Output Resistance (Single ended)	IO+ = 1.0 mA			60	Ω
Filter Control Characteristics						
VR	Reference Voltage		2.2		2.45	V
V_{RX}	PTAT Reference Current Set Output Voltage	TA = 25°C IRX = 0 - 0.6 mA Rx > 1.25 kΩ		750		mV
IFO	PTAT Reference Current, Output Current Range	TA = 25°C 1.25 kΩ < Rx < 5.0 kΩ IFO = VRX/Rx VRX = 750 mV	0.15		0.6	mA
R@IFO	IFO Output Impedance		50			kΩ
V@IFO	IFO Voltage Compliance				Vcc-1	V
IFI	PTAT Programming Current Range	TA = 25°C, VRX = 750 mV	0.2		0.6	mA
R@IFI	IFI Input Impedance	0.2 mA < IFI < 0.6 mA, T = 25°C			2	KΩ

ELECTRICAL CHARACTERISTICS, (Continued)
Unless otherwise specified recommended operating conditions apply.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Filter Control Characteristics, continued						
ISO	Reference Current	TA = 25°C		0.6		mA
R@ISO	ISO Output Impedance		50			kΩ
ISI	Programming Current Range	TA = 25°C	0		0.6	mA
R@ISI	ISI Input Impedance				TBD	Ω
V_{ISI}	Voltage at pin ISI			VR		V
V_{ISO} max	Saturation Voltage at pin ISO	Maximum voltage guaranteed not to saturate current source			Vcc-1	V

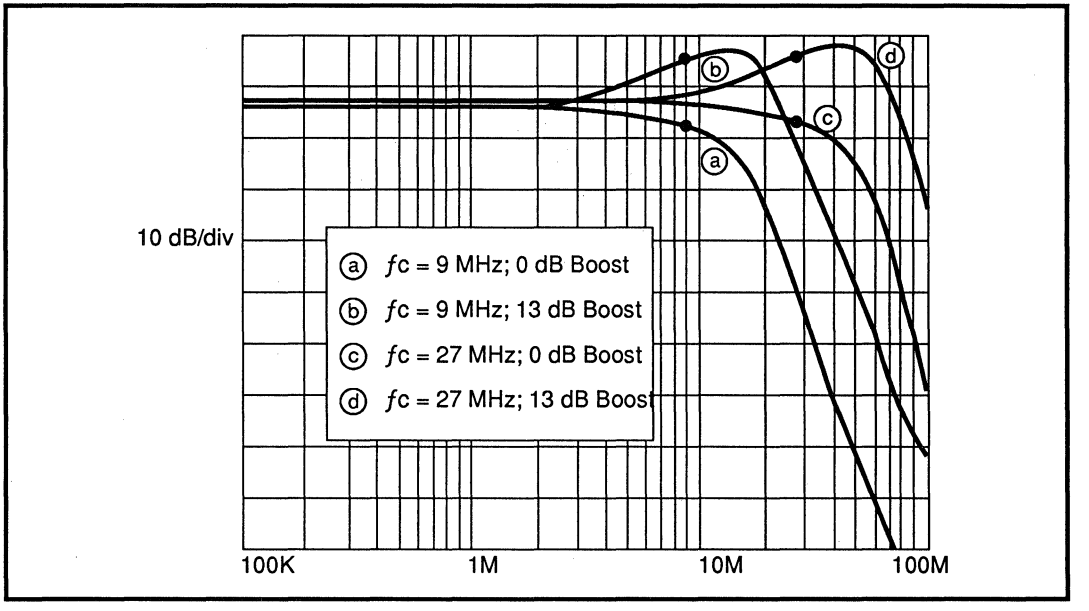


FIGURE 1: 32F8000 Normal Low Pass Response

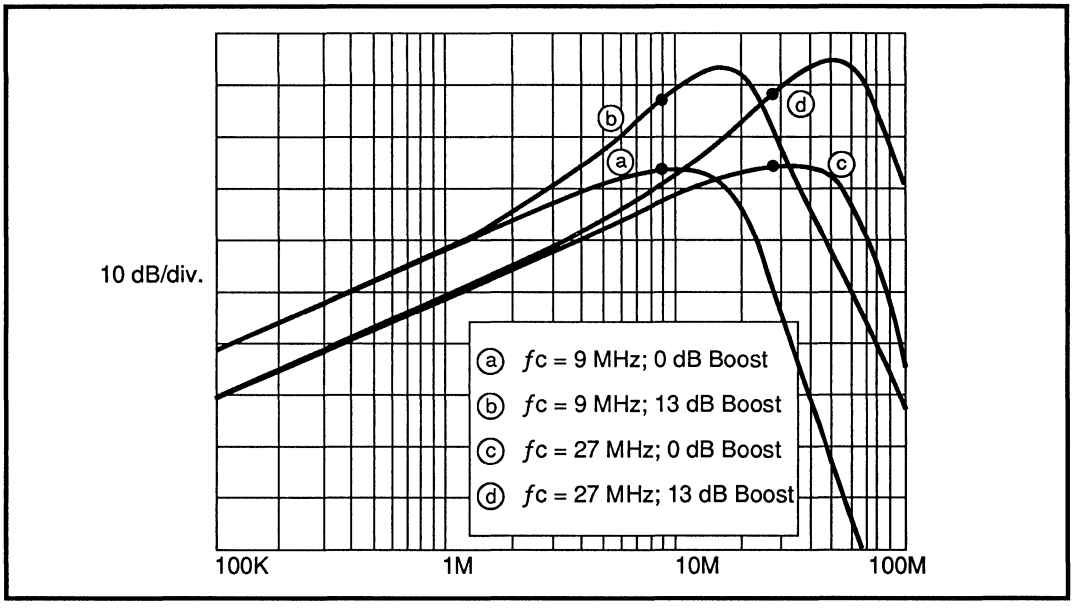


FIGURE 2: 32F8000 Differentiated Low Pass Response

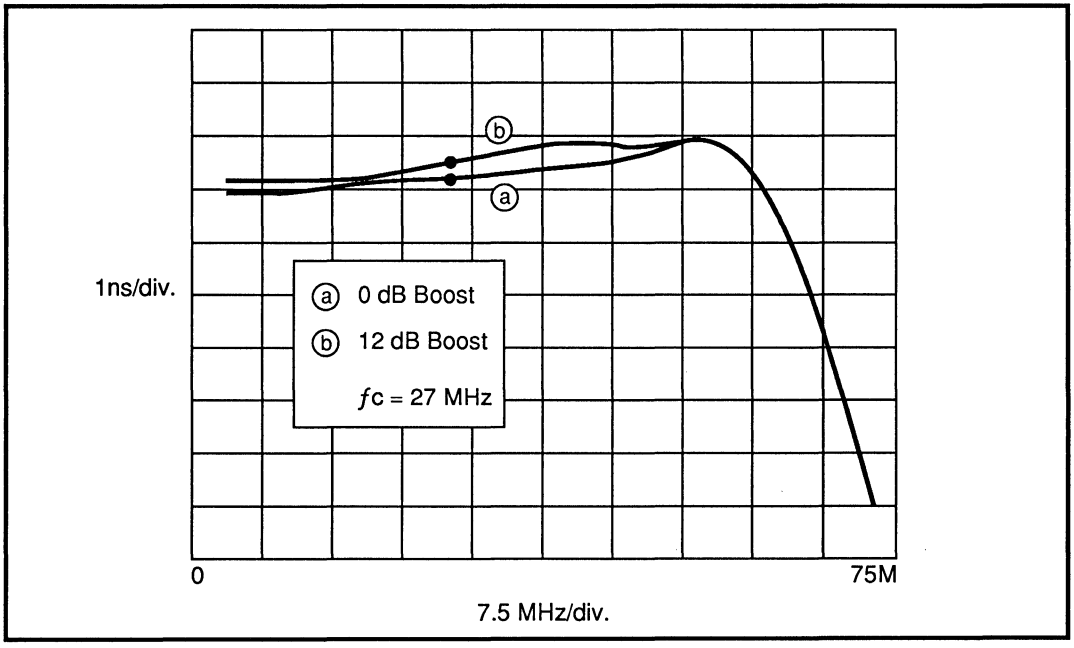
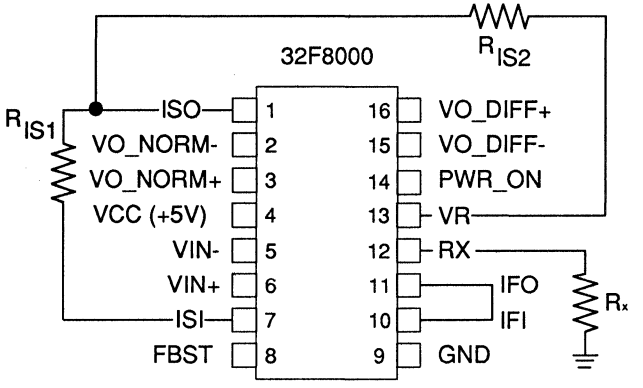


FIGURE 3: 32F8000 Group Delay Response with *fc* = 27 MHz



VR = 2.2V

V_{RX} = 750 mV @25°C

IFO = V_{RX}/Rx

IFI range: 0.2 mA to 0.6 mA @25°C

(9 to 27 MHz no boost)

Fixed frequency programming is accomplished as shown in the drawing above. In this case IFI (programming current) is equivalent to IFO (reference current). Programming current is then set by V_{RX}/Rx.

i.e.: fc = 27 MHz then

IFI = IFO = 0.6 mA @25°C

Rx = 750 mV/0.6 mA = 1.25 kΩ

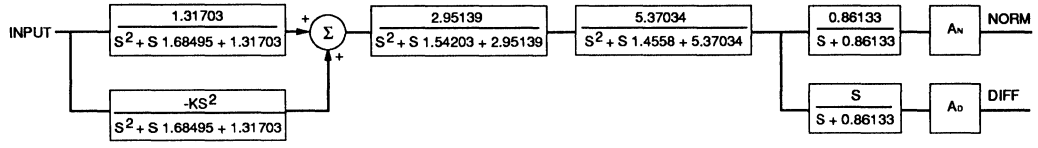
Fixed boost programming is also accomplished as shown above. In this case ISI (programming current) is set by a current divider, where excess current is diverted to pin VR (V_{ISI} = VR).

i.e.: boost = 9 dB then,
ISI/ISO = 0.5255 9 dB = 20 log [3.46 (0.5255) + 1]

$$\frac{R_{IS2}}{R_{IS1}} = \frac{1}{(\frac{ISO}{ISI}) - 1} = 1.107$$

Care should be taken that ($I_{RIS2} \cdot R_{IS2}$) or ($I_{RIS1} \cdot R_{IS1}$) do not exceed (V_{ISO} max - V_{ISI}).

FIGURE 4: 32F8000 Applications Setup



Normalized for $\omega c = (2\pi)\ fc = 1$
AN and AD are adjusted for unity gain (0 dB) at $F = 0.67\ fc$
Denormalize the frequency by substituting $S \rightarrow (S/2\pi fc)$
Eq for fc = 27 MHz, $S = S / [(2\pi)(27 \times 10^6)]$

FIGURE 5: 32F8000 Normalized Block Diagram

TABLE 1: 32F8000 Frequency Boost Calculations

Assuming 13 dB boost for ISO = ISI

$$\frac{ISI}{ISO} \cong \frac{(10^{(FB/20)}) - 1}{3.46}$$

Boost	ISI/ISO	Boost	ISI/ISO
1 dB	0.035	6 dB	0.288
2 dB	0.075	7 dB	0.358
3 dB	0.119	8 dB	0.437
4 dB	0.169	9 dB	0.526
5 dB	0.225	10 dB	0.625
		11 dB	0.737
		12 dB	0.862
		13 dB	1.00

or,

boost in dB $\cong 20 \log[3.46\left(\frac{ISI}{ISO}\right) + 1$

ISI/ISO	Boost	ISI/ISO	Boost
0.1	2.581 dB	0.6	9.760 dB
0.2	4.568 dB	0.7	10.686 dB
0.3	6.184 dB	0.8	11.522 dB
0.4	7.546 dB	0.9	12.285 dB
0.5	8.723 dB	1.0	13 dB

TABLE 2: Calculations

Typical change in f-3 dB point with boost

Boost at fc	f-3 dB/fc	Boost at fc	f-3 dB/fc
0 dB	1.0	5 dB	2.13
1	1.22	6	2.28
2	1.47	7	2.41
3	1.74	8	2.53
4	1.95	9	2.65
		10	2.73
		11	2.81
		12	2.88
		13	2.96

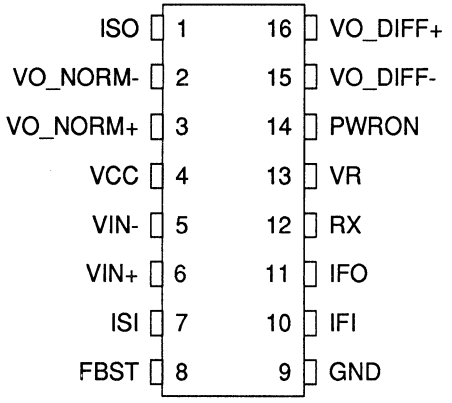
Notes: 1. fc is the original programmed cutoff frequency with no boost
2. f-3 dB is the new -3 dB value with boost implemented

i.e., fc = 9 MHz when boost = 0 dB
if boost is programmed to 5 dB then f-3 dB = 19.17 MHz

SSI 32F8000
Low-Power Programmable Electronic Filter

PACKAGE PIN DESIGNATION

(Top View)



32F8000
16-pin DIP, SON, SOL

THERMAL CHARACTERISTICS: θja

16-lead SON (150 mil)	105°C/W
16-lead SOL (300 mil)	100°C/W
16-lead PDIP	170°C/W

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 731-7110, FAX (714) 573-6914

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SSI 32F8011/8012
Programmable Electronic Filter

November 1991

3

DESCRIPTION

The SSI 32F8011/8012 Programmable Electronic Filter provides an electronically controlled low–pass filter with a separate differentiated low–pass output. A seven–pole, Bessel–type, low–pass filter is provided along with a single-pole, single-zero differentiator. Both outputs have matched delays. The delay matching is unaffected by any amount of programmed high frequency peaking (boost) or bandwidth. This programmability, combined with low group delay variation makes the SSI 32F8011/8012 ideal for use in many applications. Double differentiation high frequency boost is accomplished by a two–pole, low–pass with a two–pole, high–pass feed forward section to provide complementary real axis zeros. A variable attenuator is used to program the zero locations, which controls the amount of boost.

The SSI 32F8011/8012 programmable boost and bandwidth characteristics can be controlled by external DACs or DACs provided in the SSI 32D4661 Time Base Generator. Fixed characteristics are easily accomplished with three external resistors, in addition boost can be switched in or out by a logic signal.

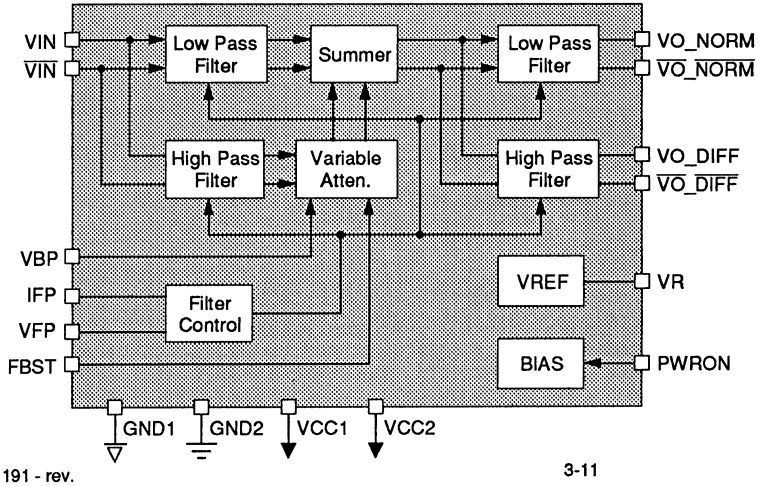
The SSI 32F8011/8012 requires only a +5V supply and is available in 16-pin DIP, SON, and SOL packages.

Note: SSI 32F8011 is in full production; SSI 32F8012 is in preliminary status. Samples of both are available.

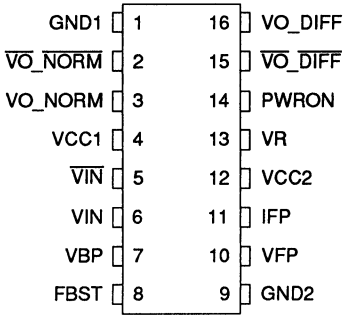
FEATURES

- **Ideal for:**
  - **constant density recording applications**
  - **cellular telephone applications**
  - **radio**
  - **data acquisition**
  - **LAN**
- **Programmable filter cutoff frequency (SSI 32F8011 fc = 5 to 13 MHz) (SSI 32F8012 fc = 6 to 15 MHz)**
- **Programmable high frequency peaking (0 to 9 dB boost at the filter cutoff frequency)**
- **Matched normal and differentiated low-pass outputs**
- **Differential filter input and outputs**
- **±0.75 ns group delay variation from 0.2 fc to fc = 13 MHz**
- **Total harmonic distortion less than 1%**
- **+5V only operation**
- **16-pin DIP, SON, and SOL package**

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION

The SSI 32F8011/8012, a high performance programmable electronic filter, provides a low pass Bessel-type seven pole filter with matched normal and differentiated outputs. The device has been optimized for usage with several Silicon Systems products, including the SSI 32D4661 Time Base Generator, the SSI 32P54x family of Pulse Detectors, and the SSI 32P4622 Combo chip (Data Separator and Pulse Detector).

CUTOFF FREQUENCY PROGRAMMING

The programmable electronic filter can be set to a filter cutoff frequency from 5 to 13 MHz (with no boost) for SSI 32F8011 and 6 to 15 MHz for SSI 32F8012.

Cutoff frequency programming can be established using either a current source fed into pin IFP whose output current is proportional to the SSI 32F8011/8012 output reference voltage VR, or by means of an external resistor tied from the output voltage reference pin VR to pin VFP. The former method is optimized using the SSI 32D4661 Time Base Generator, since the current source into pin IFP is available at the DAC F output of the 32D4661. Furthermore, the voltage reference input is supplied to pin VR3 of the 32D4661 by the reference voltage VR from the VR pin of the 32F8011/8012. This reference voltage is an internally generated bandgap reference, which typically varies less than 1% over supply voltage and temperature variation.

The cutoff frequency, determined by the -3dB point relative to a very low frequency value (< 10 kHz), is related to the current IVFP injected into pin IFP by the following formulas.

SSI 32F8011
Fc (ideal, in MHz) = 16.25•IFP = 16.25•IVFP•2.2/VR

SSI 32F8012
Fc (ideal, in MHz) = 18.75•IFP = 18.75•IVFP•2.2/VR
where IFP and IVFP are in mA, 0.31<IFP<0.8 mA, and VR is in volts.

If a current source is used to inject current into pin IFP, pin VFP should be left open.

If the 32F8011/8012 cutoff frequency is set using voltage VR to bias up a resistor tied to pin VFP, the cutoff frequency is related to the resistor value by the following formulas.

SSI 32F8011
Fc (ideal, in MHz) = 16.25•IFP = 16.25•2.2/(3•Rx)

SSI 32F8012
Fc (ideal, in MHz) = 18.75•IFP = 18.75•2.2/(3•Rx)
where Rx is in ohms, 0.917<Rx<2.366 kΩ.

If pin VFP is used to program cutoff frequency, pin IFP should be left open.

SLIMMER HIGH FREQUENCY BOOST PROGRAMMING

The amplitude of the input signal at frequencies near the cutoff frequency can be increased using this feature. Applying an external voltage to pin VBP which is proportional to reference output voltage VR (provided by the VR pin) will set the amount of boost. A fixed amount of boost can be set by an external resistor divider network connected from pin VBP to pins VR and GND. No boost is applied if pin FBST, frequency boost enable, is at a low logic level.

The amount of boost FB at the cutoff frequency Fc is related to the voltage VBP by the formula

FB (ideal, in dB) = 20 $\log_{10}$[1.884(VBP/VR)+1], where 0<VBP<VR.

PIN DESCRIPTION

NAME	DESCRIPTION
VIN, $\overline{\text{VIN}}$	DIFFERENTIAL SIGNAL INPUTS. The input signals must be AC coupled to these pins.
VO_NORM, $\overline{\text{VO\_NORM}}$	DIFFERENTIAL NORMAL OUTPUTS. The output signals must be AC coupled.
VO_DIFF, $\overline{\text{VO\_DIFF}}$	DIFFERENTIAL DIFFERENTIATED OUTPUTS. For minimum time skew, these outputs should be AC coupled to the pulse detector.
IFP	FREQUENCY PROGRAM INPUT. The filter cutoff frequency FC, is set by an external current IFP, injected into this pin. IFP must be proportional to voltage VR. This current can be set with an external current generator such as a DAC. VFP should be left open when using this pin.
VFP	FREQUENCY PROGRAM INPUT. The filter cutoff frequency can be set by programming a current through a resistor from VR to this pin. IFP should be left open when using this pin.
VBP	FREQUENCY BOOST PROGRAM INPUT. The high frequency boost is set by an external voltage applied to this pin. VBP must be proportional to voltage VR. A fixed amount of boost can be set by an external resistor divider network connected from VBP to VR and GND. No boost is applied if the FBST pin is grounded, or at logic low.
FBST	FREQUENCY BOOST. A high logic level or open input enables the frequency boost circuitry.
PWRON	POWER ON. A high logic level or open circuit enables the chip. A low level puts the chip in a low power state.
VR	REFERENCE VOLTAGE. Internally generated reference voltage.
VCC1, VCC2	+5 VOLT SUPPLY.
GND1, GND2	GROUND

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

PARAMETER	RATINGS	UNIT
Storage Temperature	-65 to +150	°C
Junction Operating Temperature, Tj	+130	°C
Supply Voltage, VCC1, VCC2	-0.5 to 7	V
Voltage Applied to Inputs	-0.5 to VCC + 0.5	V
IFP, VFP Inputs Maximum Current*	≤1.2	mA

* Exceeding this current may cause frequency programming lockup.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	RATINGS	UNIT
Supply voltage, VCC1, VCC2	4.5 < VCC1,2 < 5.50	V
Ambient Temperature	0 < Ta < 70	°C

ELECTRICAL CHARACTERISTICS

Power Supply Characteristics (Unless otherwise specified, recommended operating conditions apply.)

PARAMETER		CONDITIONS		MIN	NOM	MAX	UNITS
ICC	Power Supply Current	PWRON ≤ 0.8V	VBP = VR		14	17	mA
			VBP = 0V		12	15	mA
ICC	Power Supply Current	PWRON ≥ 2.0V			67	80	mA

DC Characteristics

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
VIH	High Level Input Voltage	TTL input	2.0		VCC+0.3	V
VIL	Low Level Input Voltage		-0.3		0.8	V
IIH	High Level Input Current	VIH = 2.7V			20	μA
IIL	Low Level Input Current	VIL = 0.4V			–1.5	mA

Filter Characteristics

PARAMETER		CONDITIONS		MIN	NOM	MAX	UNITS
FCA	Filter *fc* Accuracy	using VFP pin	32F8011	11.7		14.3	MHz
		Rx = 0.917 kΩ	32F8012	13.5		16.5	MHz
AO	VO_NORM Diff Gain	F = 0.67 *fc*, FB = 0 dB		0.8		1.20	V/V
AD	VO_DIFF Diff Gain	F = 0.67 *fc*, FB = 0 dB		0.8AO		1.0AO	V/V
FBA	Frequency Boost Accuracy	VBP = VR @ *fc* = 5 MHz		8.5	9.5	10.5	dB
TGD0	Group Delay Variation Without Boost*	*fc* = Max *fc*, VBP = 0V F = 0.2 *fc* to *fc*		–0.75		+0.75	ns
TGDB	Group Delay Variation With Boost*	*fc* = Max *fc*, VBP = VR F = 0.2 *fc* to *fc*		–0.75		+0.75	ns
VIF	Filter Input Dynamic Range	THD = 1% max, F = 0.67 *fc* (no boost)		1.5			Vpp
VOF	Filter Output Dynamic Range	THD = 1% max, F = 0.67 *fc*		1.5			Vpp
RIN	Filter Diff Input Resistance			3.0			kΩ
CIN	Filter Diff Input Capacitance*					7	pF
EOUT	Output Noise Voltage* Differentiated Output	BW = 100 MHz, Rs = 50Ω, I*fp* = 0.8 mA, VBP = 0.0V			5.5	6.8	mVRms
EOUT	Output Noise Voltage* Normal Output	BW = 100 MHz, Rs = 50Ω I*fp* = 0.8 mA, VBP = 0.0V			2.5	3.6	mVRms
EOUT	Output Noise Voltage* Differentiated Output	BW = 100 MHz, Rs = 50Ω I*fp* = 0.8 mA, VBP = VR			6.0	8.1	mVRms
EOUT	Output Noise Voltage* Normal Output	BW = 100 MHz, Rs = 50Ω I*fp* = 0.8 mA, VBP = VR			3.25	4.4	mVRms

* Not directly testable in production, design characteristic.

ELECTRICAL CHARACTERISTICS (continued)

Filter Characteristics (continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
IO–	Filter Output Sink Current		1.0			mA
IO+	Filter Output Source Current		2.0			mA
RO	Filter Output Resistance Single ended	Source Current (IO+) = 1 mA			60	Ω

Filter Control Characteristics

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
VR	Reference Voltage Output		2.0		2.40	V
I_{VR}	Reference Output Source Current				2.0	mA

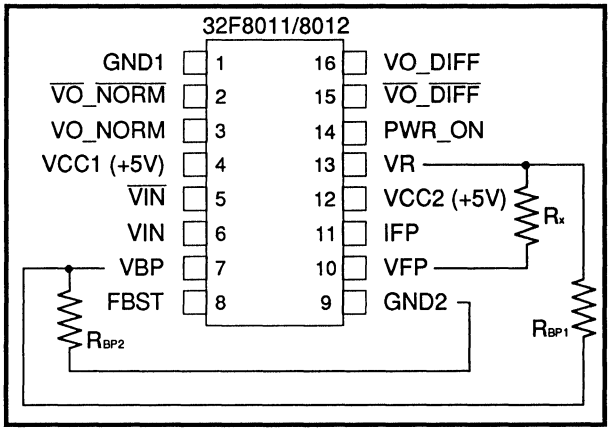


FIGURE 1: 32F8011/8012 Applications Setup, 16-Pin SO or DIP

VR = 2.2V

VFP = 0.667 VR

IVfp = 0.33VR/Rx

IVfp range: 0.31 mA to 0.8 mA
(5 MHz to 13 MHz for SSI 32F8011)
(6 MHz to 15 MHz for SSI 32F8012)

VFP is used when programming current is set with a resistor from VR. When VFP is used IFP must be left open.

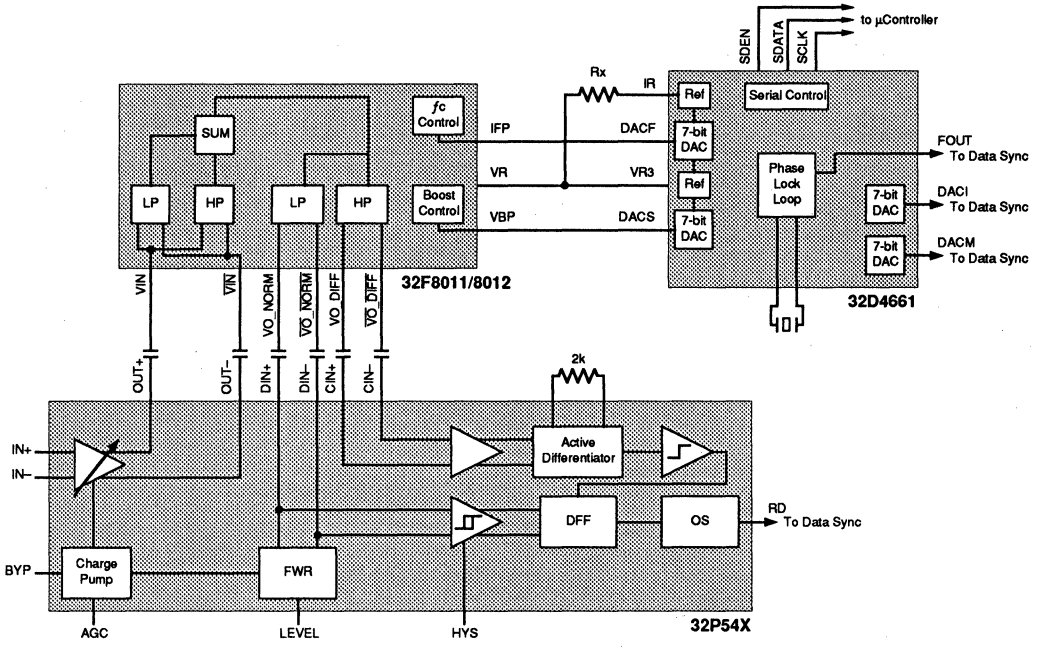


FIGURE 2: Applications Setup, Constant Density Recording
32F8011/8012, 32P54X, 32D4661

IOF = DACF output current

IOF = (0.98F•VR)/127Rx

Rx = (0.98F•VR)/127IOF

Rx = current reference setting resistor

VR = Voltage Reference = 2.2V

F = DAC setting: 0-127

Full scale, F = 127

For range of Max fc then IFP = 0.8 mA

Therefore, for Max programming current range to 0.8 mA:

Rx = (0.98)(2.2/0.8) = 2.7 kΩ

Please note that in setups such as this where IFP is used for cutoff frequency programming VFP must be left open.

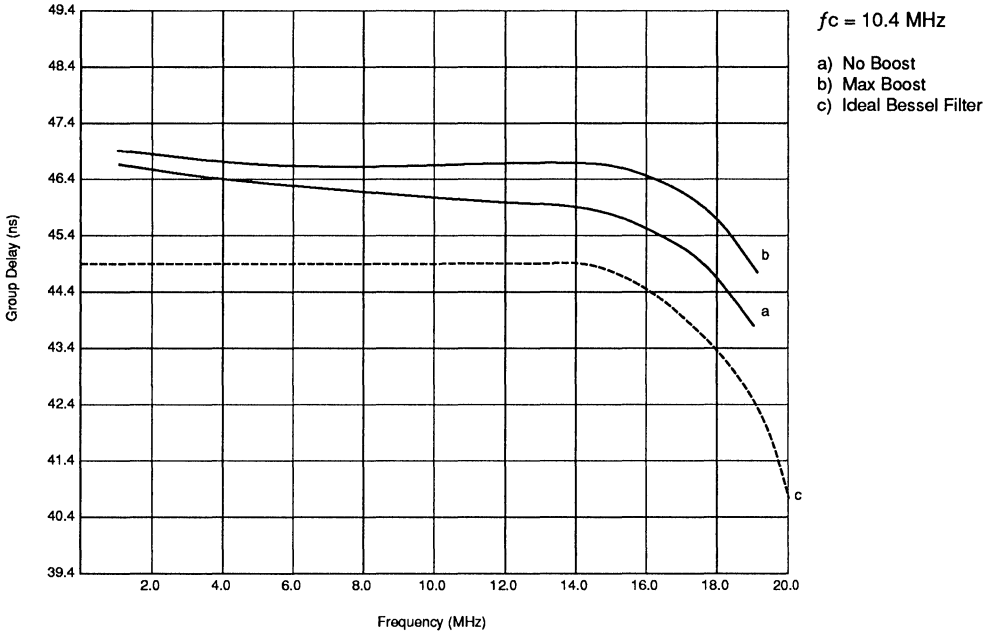


FIGURE 3: 32F8011/8012 Typical Group Delay Variation (Differentiated Output)

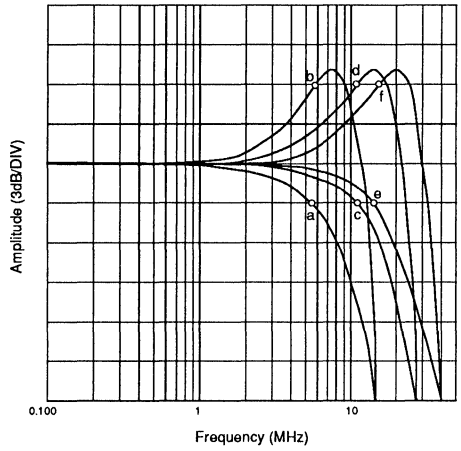


FIGURE 4: 32F8011/8012 Normal Low Pass Output Response (VO_NORM)

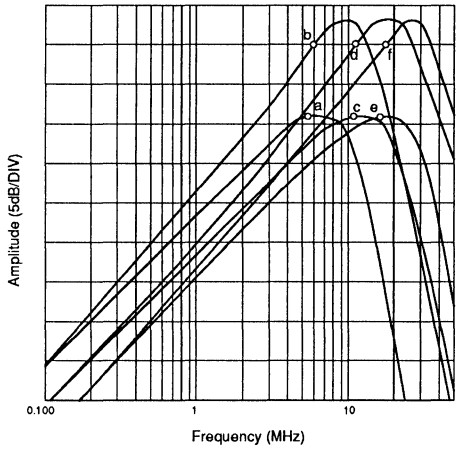
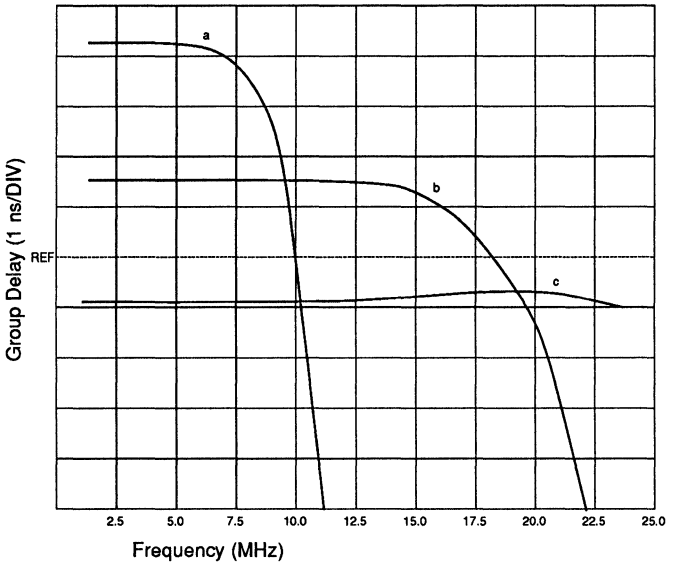


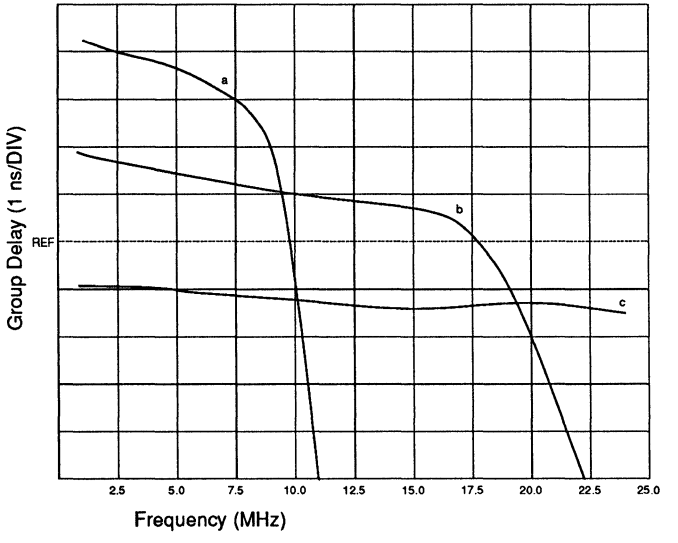
FIGURE 5: 32F8011/8012 Differented Low Pass Output Response (VO_DIFF)

a) fc = 5 MHz No Boost
b) fc = 5 MHz Max Boost
c) fc = 10 MHz No Boost
d) fc = 10 MHz Max Boost
e) fc = 15 MHz No Boost
f) fc = 15 MHz Max Boost



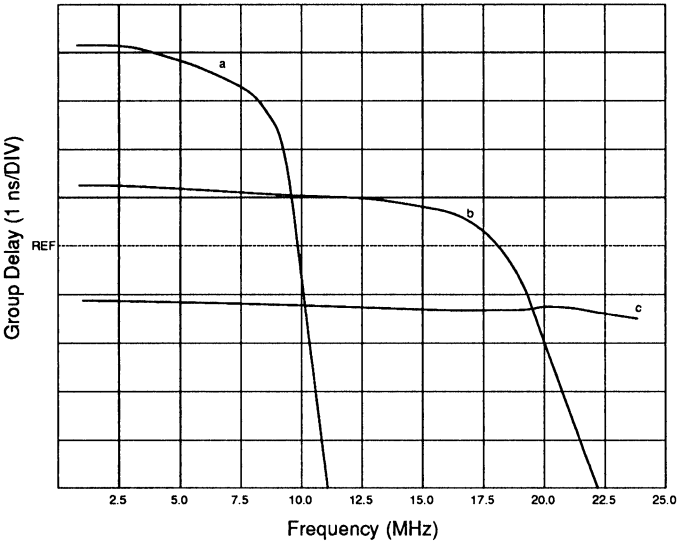
a) fc = 5 MHz (Ref = 80 ns)
b) fc = 10 MHz (Ref = 45 ns)
c) fc = 15 MHz (Ref = 35 ns)

FIGURE 6: 32F8011/8012 Typical Group Delay Variation (Differentiated Output) Maximum Boost



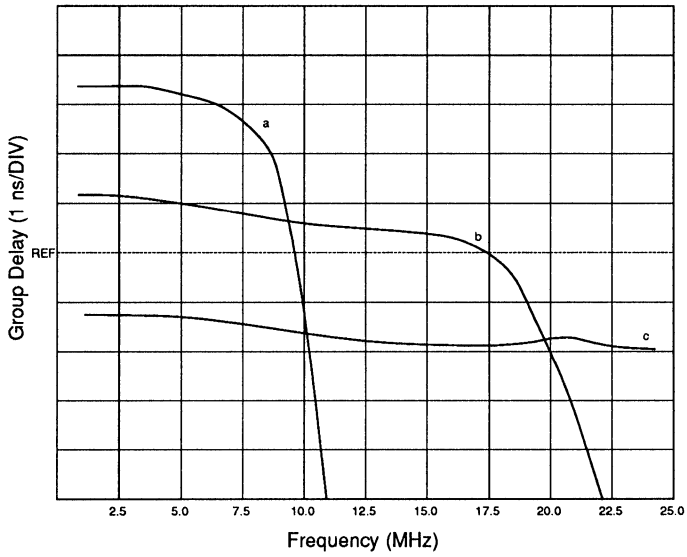
a) fc = 5 MHz (Ref = 80 ns)
b) fc = 10 MHz (Ref = 45 ns)
c) fc = 15 MHz (Ref = 35 ns)

FIGURE 7: 32F8011/8012 Typical Group Delay Variation (Differentiated Output) No Boost



a) fc = 5 MHz (Ref = 80 ns)
b) fc = 10 MHz (Ref = 45 ns)
c) fc = 15 MHz (Ref = 35 ns)

FIGURE 8: 32F8011/8012 Typical Group Delay Variation (Normal Low Pass Output) Maximum Boost



a) fc = 5 MHz (Ref = 80 ns)
b) fc = 10 MHz (Ref = 45 ns)
c) fc = 15 MHz (Ref = 35 ns)

FIGURE 9: 32F8011/8012 Typical Group Delay Variation (Normal Low Pass Output) No Boost

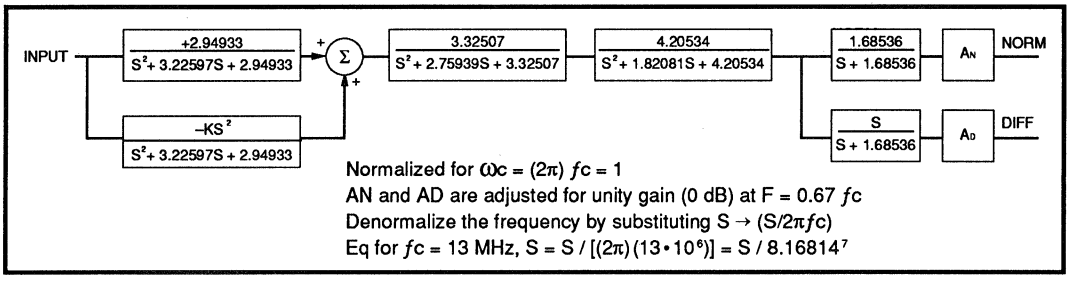


FIGURE 12: 32F8011/8012 Normalized Block Diagram

TABLE 1: 32F8011/8012 Frequency Boost Calculations

Assuming 9.2 dB boost for VBP = VR

$$\frac{VBP}{VR} \cong \frac{\left(10^{(FB/20)}\right)-1}{1.884}$$

Boost	VBP/VR	Boost	VBP/VR
1 dB	0.065	6 dB	0.528
2 dB	0.137	7 dB	0.658
3 dB	0.219	8 dB	0.802
4 dB	0.310	9 dB	0.965
5 dB	0.413		

or,

boost in dB ≅ 20 log $\left[1.884\left(\frac{VBP}{VR}\right)+1\right]$

VBP/VR	Boost	VBP/VR	Boost
0.1	1.499 dB	0.6	6.569 dB
0.2	2.777 dB	0.7	7.305 dB
0.3	3.891 dB	0.8	7.984 dB
0.4	4.879 dB	0.9	8.613 dB
0.5	5.765 dB	1.0	9.200 dB

TABLE 2: Calculations

Typical change in *f*-3 dB point with boost

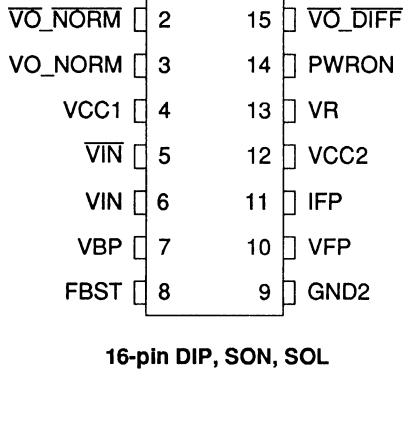
Boost at *fc*	*f*-3 dB/*fc*	Boost at *fc*	*f*-3 dB/*fc*
0 dB	1.0	5 dB	2.13
1	1.2	6	2.28
2	1.47	7	2.41
3	1.74	8	2.53
4	1.95	9	2.65

Notes: 1. *fc* is the original programmed cutoff frequency with no boost
2. *f*-3 dB is the new -3 dB value with boost implemented

i.e., *fc* = 5 MHz when boost = 0 dB
if boost is programmed to 5 dB then f-3 dB = 10.65 MHz

PIN DIAGRAM

(Top View)



16-pin DIP, SON, SOL

Thermal Characteristics: θjA

16-lead SON (150 mil)	105° C/W
16-lead SOL (300 mil)	100° C/W
16-lead PDIP	170° C/W

3

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32F8011		
16-lead SON (150 mil)	32F8011-CN	32F8011-CN
16-lead SOL (300 mil)	32F8011-CL	32F8011-CL
16-pin PDIP	32F8011-CP	32F8011-CP
SSI 32F8012		
16-lead SON (150 mil)	32F8012-CN	32F8012-CN
16-lead SOL (300 mil)	32F8012-CL	32F8012-CL
16-pin PDIP	32F8012-CP	32F8012-CP

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 731-7110, FAX (714) 573-6914

Notes:

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A TDK Group Company

SSI 32F8020/8022
Low-Power Programmable Electronic Filter

December 1991

3

DESCRIPTION

The SSI 32F8020/8022 Programmable Electronic Filter provides an electronically controlled low–pass filter with a separate differentiated low–pass output. A seven–pole, .05° Equiripple-type linear phase, low–pass filter is provided along with a single-pole, single-zero differentiator. Both outputs have matched delays. The delay matching is unaffected by any amount of programmed equalization or bandwidth. This programability combined with low group delay variation makes the SSI 32F8020/8022 ideal for use in constant density recording applications. Double differentiation pulse slimming equalization is accomplished by a two–pole, low–pass with a two–pole, high–pass feed forward section to provide complimentary real axis zeros. A variable attenuator is used to program the zero locations.

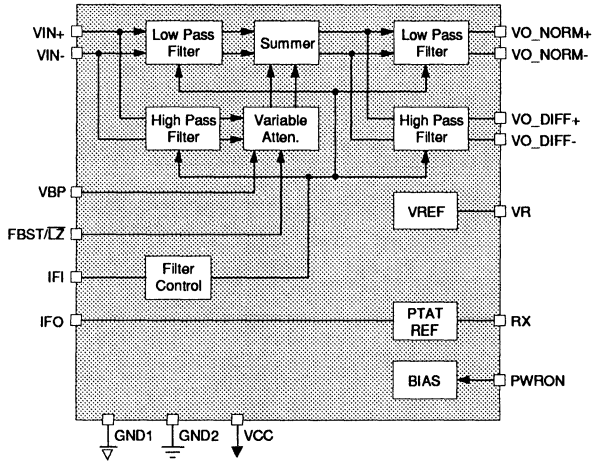
The SSI 32F8020/8022 programmable equalization and bandwidth characteristics can be controlled by external DACs or DACs provided in the SSI 32D4661 time base generator. Fixed characteristics are easily accomplished with three external resistors. For the SSI 32F8020, equalization can be switched in or out by a logic signal. The input impedance of the SSI 32F8022 can be clamped low for fast recovery from input overload.

The SSI 32F8020/8022 requires only a +5V supply and is available in 16-pin DIP, SON, and SOL packages.

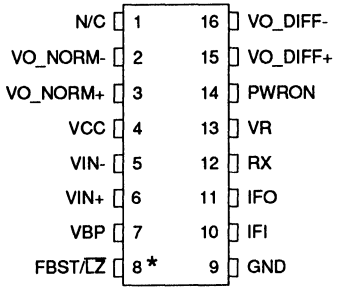
FEATURES

- **Ideal for constant density recording applications**
- **Programmable filter cutoff frequency (fc = 1.5 to 8 MHz)**
- **Programmable pulse slimming equalization (0 to 9 dB boost at the filter cutoff frequency)**
- **Matched normal and differentiated low-pass outputs**
- **Differential filter input and outputs**
- **±10% cutoff frequency accuracy**
- **±2% maximum group delay variation from 1.5 - 8 MHz**
- **Total harmonic distortion less than 1%**
- **No external filter components required**
- **+5V only operation**
- **16-pin DIP, SON, and SOL package**

BLOCK DIAGRAM



PIN DIAGRAM



* Pin 8 = FBST - SSI 32F8020
LZ - SSI 32F8022

CAUTION: Use handling procedures necessary for a static sensitive component.

SSI 32F8020/8022
Low-Power Programmable Electronic Filter

FUNCTIONAL DESCRIPTION

The SSI 32F8020/8022 is a high performance programmable electronic filter. It features a 7-pole 0.05° phase equiripple filter with matched normal and differentiated outputs. The device has been optimized for usage with several Silicon Systems products, including the SSI 32D4661 Time Base Generator, the SSI 32P54X family pulse detectors, and the SSI 32P4622 combo chip (Data Separator and Pulse Detector).

CUTOFF FREQUENCY PROGRAMMING

The cutoff frequency, fc, of the SSI 32F8020/8022 is defined as the -3dB filter bandwidth with no magnitude equalization applied, and is programmable from 1.5 MHz to 8 MHz.

The cutoff frequency is programmable with 3 pins: RX, IFO and IFI. At the RX pin, an external resistor to ground establishes a reference current:

$$IFO = \frac{0.75}{RX} \text{ at } T = 27°C$$

IFI should be made proportional to IFO for temperature stability. The cutoff frequency is related to the RX resistor, IFO and IFI currents as follows:

$$fc(MHz) = 8x\frac{IFI}{IFO}x\frac{1.25}{Rx(k\Omega)}$$

For a fixed cutoff frequency setting, IFO and IFI can be tied together. The cutoff frequency equation then reduces to: $fc(MHz) = 8x\frac{1.25}{Rx(k\Omega)}$

For programmable cutoff frequency, an external current DAC can be used. The IFO should be the reference current into the DAC. The DAC output current drives IFI, which is then proportional to IFO. The DACF in the SSI 32D4661 Time Base Generator is designed to control fc of the Silicon Systems programmable filters. When the DACF, which has a 4X current from its reference to full scale output is used, a 5-kΩ RX is used. The fc is then given as follows:

$$fc(MHz) = 8x\frac{F\_Code}{127}$$

where F_Code is the decimal code equivalent to the 7-bit digital input for the DACF.

MAGNITUDE EQUALIZATION PROGRAMMING

The magnitude equalization, measured in dB, is the amount of high frequency peaking at the cutoff frequency relative to the original -3 dB point. For example, when 9 dB boost is applied, the magnitude response peaks up 6 dB above the DC gain.

The magnitude equalization is programmable with two pins: VR and VBP. The VR is a bandgap reference voltage, 2.2 V typically. The voltage at the VBP pin determines the amount of high frequency boost. The boost function is as follows:

$$Boost(dB) = 20\log_{10}[1.884(\frac{VBP}{VR}) + 1]$$

For a fixed boost setting, a resistor divider between VR to ground can be used with the divided voltage at the VBP pin. For programmable equalization, an external voltage DAC can be used. VR should be the reference voltage to the DAC. The DAC output voltage is then proportional to VR. The DACS in the SSI 32D4661 is designed to control the magnitude equalization of Silicon Systems programmable filters. When DACS is used, the boost relation then reduces to:

$$Boost(dB) = 20\log_{10}[1.884(\frac{S\_Code}{127}) + 1]$$

where S_Code is the decimal code equivalent to the 7-bit digital input for the DACS.

For the SSI 32F8020, the equalization function can be disabled when FBST is pulled to logic 0. For the SSI 32F8022, the VBP pin should be grounded to achieve 0 dB boost.

LOW INPUT IMPEDANCE (SSI 32F8022 only)

When the $\overline{LZ}$ is at logic 1 or left open, the SSI 32F8022 input is at high impedance state. When the $\overline{LZ}$ is pulled to logic 0, the SSI 32F8022 input is clamped to a low impedance state, 200 Ω typical.

POWER ON/OFF

The SSI 32F8020/8022 supports a power down mode for minimal idle dissipation. When PWRON is pulled up to logic 1, the device is in normal operation mode. When PWRON is pulled down to logic 0, or left open, the device is in the power down mode.

PIN DESCRIPTION

NAME	DESCRIPTION
VIN+, VIN-	DIFFERENTIAL SIGNAL INPUTS. The input signals must be AC coupled to these pins.
VO_NORM+, VO_NORM-	DIFFERENTIAL NORMAL OUTPUTS. The output signals must be AC coupled to load.
VO_DIFF+ VO_DIFF-	DIFFERENTIAL DIFFERENTIATED OUTPUTS. These outputs should be AC coupled to load.
RX	PTAT REFERENCE CURRENT SET. PTAT (proportional to absolute temperature) reference current IFO is equivalent to the current set on this pin.
IFO	PTAT CURRENT REFERENCE OUTPUT. This pin ouputs a PTAT reference current which is externally scaled for control input into IFI.
IFI	FREQUENCY PROGRAM INPUT. The filter cutoff frequency fc, is set by an external current IFI, injected into this pin. IFI must be proportional to current IFO. This current can be set with an external current generator such as a DAC, referenced to IFO.
VBP	FREQUENCY BOOST PROGRAM INPUT. The slimmer high frequency boost is set by an external voltage applied to this pin. VBP must be proportional to voltage VR. A fixed amount of boost can be set by an external resistor divider network connected from VBP to VR and GND. No boost is applied if the FBST pin is grounded, or at logic low.
FBST (32F8020 only)	FREQUENCY BOOST. A high logic level or open input enables the frequency boost circuitry. No boost is applied if the FBST pin is grounded, or at logic low.
$\overline{LZ}$ (32F8022 only)	LOW IMPEDANCE MODE. With a low logic level, the analog input impedance is switched low for fast recovery from input overload. With a high logic level or left open, the input is at high impedance state.
PWRON	POWER ON. A high logic level circuit enables the chip. A low level puts the chip in a low power state. A low or open circuit disables the chip.
VR	REFERENCE VOLTAGE. Internally generated reference voltage.
VCC	+5 VOLT SUPPLY.
GND	GROUND

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

PARAMETER	RATINGS	UNIT
Storage Temperature	-65 to +150	°C
Junction Operating Temperature, Tj	+130	°C
Supply Voltage, VCC	-0.5 to 7	V
Voltage Applied to Inputs	-0.5 to VCC	V
Maximum Power Dissipation, fc = 8 MHz, Vcc = 5.5V	226	mW

RECOMMENDED OPERATING CONDITIONS

PARAMETER	RATINGS	UNIT
Supply voltage, VCC	4.50 < VCC < 5.50	V
Ambient Temperature	0 < Ta < 70	°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified recommended operating conditions apply.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Power Supply Characteristics						
ICC	Power Supply Current	PWRON = 0.8V			3	mA
ICC	Power Supply Current	PWRON ≥ 2.2V		35	41	mA
PD	Power Dissipation	PWRON ≥ 2.2V, VCC = 5.0V		175	205	mW
		PWRON ≥ 2.2V, VCC = 5.5V		193	226	mW
DC Characteristics						
VIH	High Level Input Voltage	TTL input	2.0			V
VIL	Low Level Input Voltage				0.8	V
IIH	High Level Input Current	VIH = 2.7V			20	µA
IIL	Low Level Input Current	VIL = 0.4V			−1.5	mA
Filter Characteristics						
fc	Filter Cutoff Frequency	Rx = 5kΩ $fc = (\text{ideal})\,8\text{MHz} \cdot \frac{\text{IFI}}{4\text{IFO}}$	1.5		8.0	MHz
FCA	Filter fc Accuracy	fc (nominal) = 8 MHz	−10		+10	%
AO	VO_NORM Diff Gain	F = 0.67 fc, FB = 0 dB	0.8	0.9	1.0	V/V
AD	VO_DIFF Diff Gain	F = 0.67 fc, FB = 0 dB	0.8AO		1.2AO	V/V
FB	Frequency Boost at fc	$\text{FB(db)} = 20 \log \left[1.884 \left(\frac{\text{VBP}}{\text{VR}} \right) + 1 \right]$ VBP = VR		9.2		dB
FBA	Frequency Boost Accuracy	FB (ideal) = 9.0 dB	−1		+1	dB
TGD0	Group Delay Variation Without Boost	fc = 8 MHz, VBP = 0V F = 0.2 fc to fc	−1.3		+1.3	ns
		fc = 1.5 MHz - 8 MHz F = 0.2 fc to fc, VBP = 0V	−2		+2	%
TGDB	Group Delay Variation With Boost	fc = 8 MHz, VBP = VR F = 0.2 fc to fc	−1.3		+1.3	ns
		fc = 1.5 MHz - 8 MHz F = 0.2 fc to fc, VBP = VR	−2		+2	%

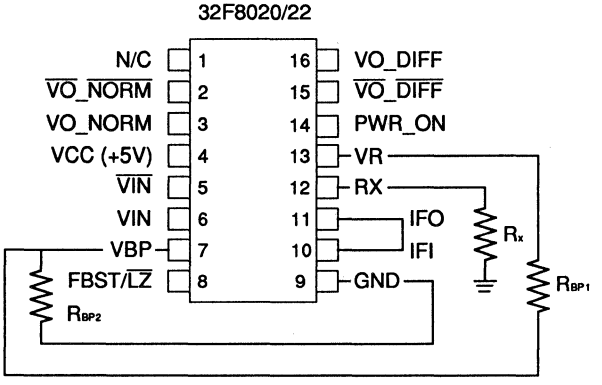
ELECTRICAL CHARACTERISTICS (Continued)
Unless otherwise specified recommended operating conditions apply.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Filter Characteristics, continued						
VIF	Filter Input Dynamic Range	THD = 1% max, F = 0.67 *fc*	1.0			Vpp
VOF	Filter Output Dynamic Range	THD = 1% max, F = 0.67 *fc*	1.0			Vpp
VIF	Filter Input Dynamic Range	THD = 3% max, F = 0.67 *fc*	2.0			Vpp
VOF	Filter Output Dynamic Range	THD = 3% max, F = 0.67 *fc*	2.0			Vpp
RIN	Filter Diff Input Resistance	32F8020 32F8022 $\overline{LZ}$ = 1	3.0			kΩ
		32F8022 $\overline{LZ}$ = 0		200		Ω
CIN	Filter Input Capacitance				7	pF
EOUT	Output Noise Voltage Differentiated Output	BW = 100 MHz, Rs = 50Ω *fc* = 8 MHz, VBP = 0.0V		6.3	7.5	mVRms
EOUT	Output Noise Voltage Normal Output	BW = 100 MHz, Rs = 50Ω *fc* = 8 MHz, VBP = 0.0V		2.7	4.0	mVRms
EOUT	Output Noise Voltage Differentiated Output	BW = 100 MHz, Rs = 50Ω *fc* = 8 MHz, VBP = VR		9.4	11.0	mVRms
EOUT	Output Noise Voltage Normal Output	BW = 100 MHz, Rs = 50Ω *fc* = 8 MHz, VBP = VR		3.7	4.5	mVRms
IO–	Filter Output Sink Current		1.0			mA
IO+	Filter Output Source Current		2.0			mA
RO	Filter Output Resistance (Single ended)	IO+ = 1.0 mA			60	Ω
Filter Control Characteristics						
VR	Reference Voltage		2.0		2.40	V
VBP	Frequency Boost Control Voltage Range	VR = 2.2V FBOOST = 0 to 9.2 dB	0		2.2	V
VRX	PTAT Reference Current Set Output Voltage	TA = 25°C IRX = 0 - 0.6 mA Rx > 1.25 kΩ		750		mV
IFO	PTAT Reference Current, Output Current Range	TA = 25°C 1.25 kΩ < Rx < 6.8 kΩ IFO = VRX/Rx VRX = 750 mV	0.11		0.6	mA
RIFO	IFO Output Impedance		50			kΩ
VIFO	IFO Voltage Compliance		0		Vcc -1	V

ELECTRICAL CHARACTERISTICS, (Continued)

Unless otherwise specified recommended operating conditions apply.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Filter Control Characteristics (continued)						
IFI	PTAT Programming Current Range	TA = 25°C, VRX = 750 mV	0.11		0.6	mA
RIFI	IFI Input Impedance		1.0		2.5	kΩ
VIFI	IFI Voltage Compliance		0.5		2.5	V



VR = 2.2V

VRX = 750 mV @25°C

IFO = VRX/Rx

IFI range: 0.11 mA to 0.60 mA @25°C

(1.5 to 8 MHz NO BOOST)

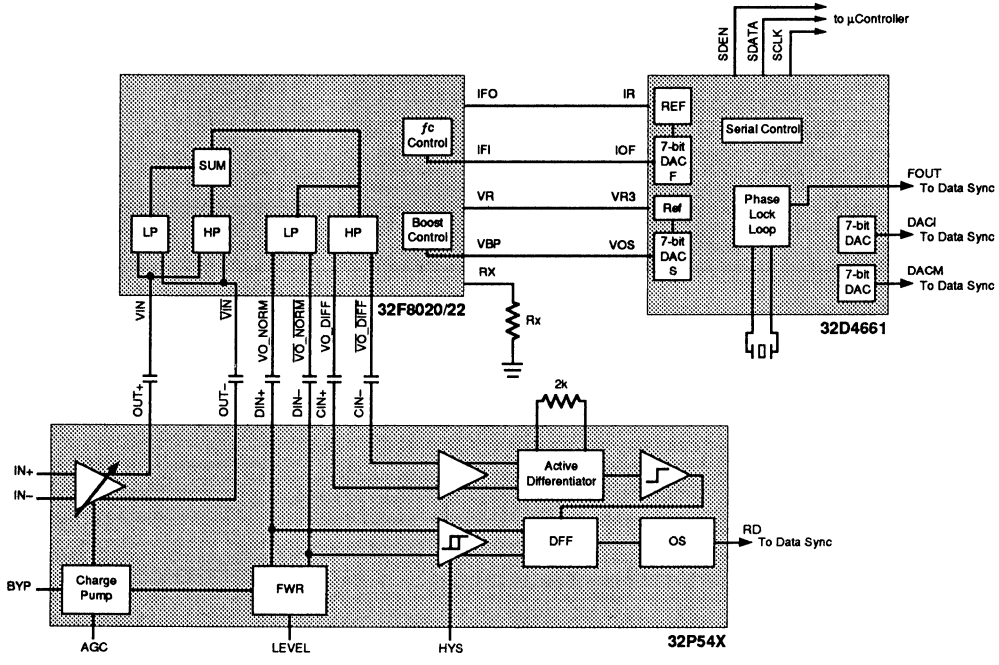
Fixed frequency programming is accomplished as shown in the drawing above. In this case IFI (programming current) is equivalent to IFO (reference current). Programming current is then set by VRX/Rx.

where: fc = 8.0 MHz then

IFI = IFO = 0.60 mA @25°C

Rx = 750 mV/0.60 mA = 1.25 kΩ

FIGURE 1: 32F8020/8022 Applications Setup



VR = 2.2V

VRX = 750 mV @25°C

IFO = VRX/Rx

IFI range: 0.11 mA to 0.60 mA @25°C

(1.5 to 8 MHz NO BOOST)

In this case the IFI (programming current) is scaled from IFO (reference current) through DACF on the 32D4661. DACF has a current gain of 4; therefore, the reference current should be set to 25% of the maximum desired IFI (programming current).

where: fc (max) = 8.0 MHZ then

IFI (max) = 0.60 mA @25°C

IFO (max) = 0.15 mA

therefore Rx = 750 mV/0.15 mA = 5 kΩ

FIGURE 2: Applications Setup, Constant Density Recording 32F8020/8022, 32P54X, 32D4661

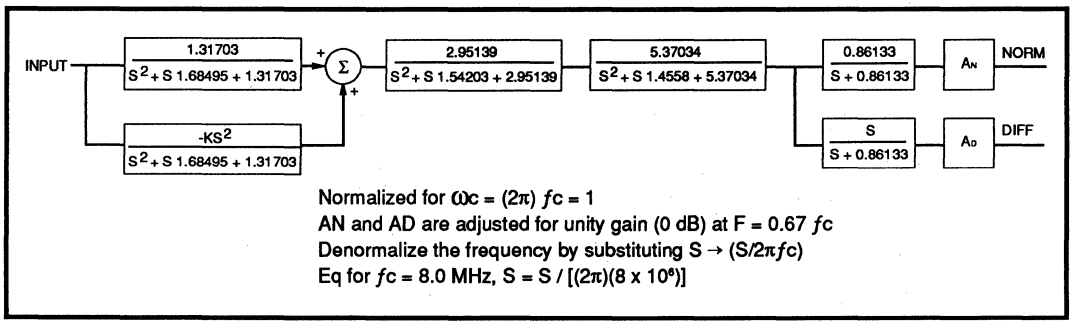


FIGURE 3: 32F8020/8022 Normalized Block Diagram

TABLE 1: 32F8020/8022 Frequency Boost Calculations

Assuming 9.2 dB boost for **VBP = VR**

$$\frac{VBP}{VR} \cong \frac{\left(10^{(FB/20)}\right)-1}{1.884}$$

Boost	VBP/VR
1 dB	0.065
2 dB	0.137
3 dB	0.219
4 dB	0.310
5 dB	0.413
6 dB	0.528
7 dB	0.658
8 dB	0.802
9 dB	0.965

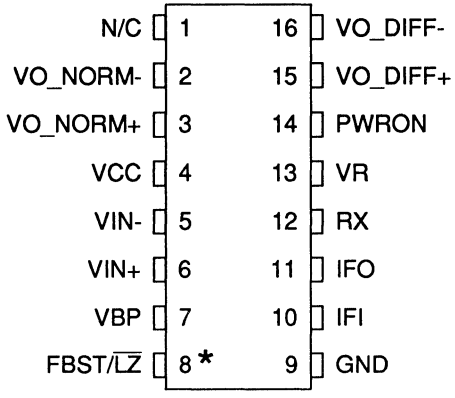
or,

$$\text{boost in dB} \cong 20 \log\left[1.884\left(\frac{VBP}{VR}\right)+1\right]$$

VBP/VR	Boost
0.1	1.499 dB
0.2	2.777 dB
0.3	3.891 dB
0.4	4.879 dB
0.5	5.765 dB
0.6	6.569 dB
0.7	7.305 dB
0.8	7.984 dB
0.9	8.613 dB
1.0	9.200 dB

PACKAGE PIN DESIGNATIONS

(Top View)



* Pin 8 = FBST - SSI 32F8020
$\overline{LZ}$ - SSI 32F8022

32F8020/8022
16-pin DIP, SON, SOL

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32F8020		
Standard Width 16-Pin Plastic Dip	32F8020-CP	32F8020-CP
Narrow Width (150 Mil.) Small Outline	32F8020-CN	32F8020-CN
Large Width (300 Mil.) Small Outline	32F8020-CL	32F8020-CL
SSI 32F8022		
Standard Width 16-Pin Plastic Dip	32F8022-CP	32F8022-CP
Narrow Width (150 Mil.) Small Outline	32F8022-CN	32F8022-CN
Large Width (300 Mil.) Small Outline	32F8022-CL	32F8022-CL

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Notes:

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SSI 32F8021/8023
Low-Power Programmable Electronic Filter
Preliminary Data

November 1991

3

DESCRIPTION

The SSI 32F8021/8023 Programmable Electronic Filter provides an electronically controlled low–pass filter. A seven–pole, .05° Equiripple-type linear phase, low–pass filter is provided. This programability combined with low group delay variation makes the SSI 32F8021/8023 ideal for use in constant density recording applications. Double differentiation pulse slimming equalization is accomplished by a two–pole, low–pass with a two–pole, high–pass feed forward section to provide complimentary real axis zeros. A variable attenuator is used to program the zero locations.

The SSI 32F8021/8023 programmable equalization and bandwidth characteristics are controlled by external DACs. The circuit is optimized to be used with the SSI 32P4620 and 54x series pulse detectors.

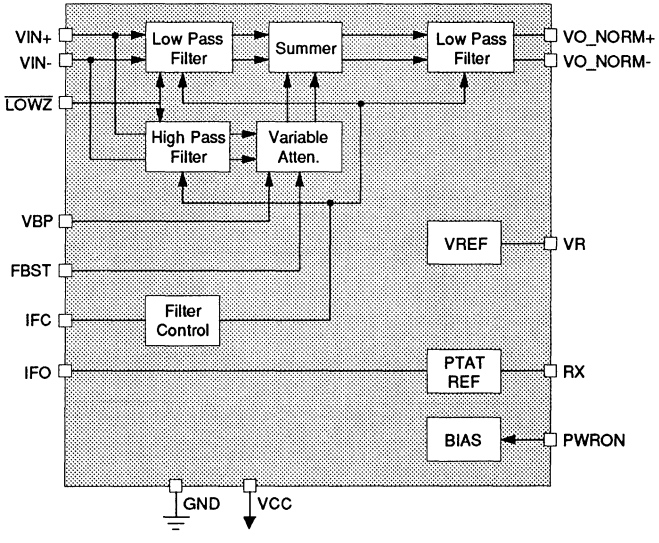
The 32F8023 is the same as the 8021, but with a low impedance switch instead of the frequency boost enable pin.

The SSI 32F8021/8023 requires only a +5V supply and is available in 16-pin DIP, SON, and SOL packages.

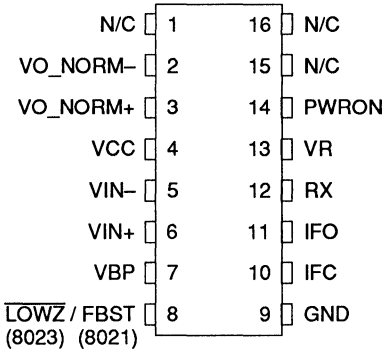
FEATURES

- **Ideal for constant density recording applications**
- **Programmable filter cutoff frequency (fc = 1.5 to 8 MHz)**
- **Programmable pulse slimming equalization (0 to 9 dB boost at the filter cutoff frequency)**
- **Differential filter input and outputs**
- **±10% cutoff frequency accuracy**
- **±2% maximum group delay variation from 1.5 - 8 MHz**
- **Total harmonic distortion less than 1%**
- **No external filter components required**
- **+5V only operation**
- **16-pin DIP, SON, and SOL package**

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

PIN DESCRIPTIONS

NAME	DESCRIPTION
VIN+, VIN-	DIFFERENTIAL SIGNAL INPUTS. The input signals must be AC coupled to these pins.
VO_NORM+, VO_NORM-	DIFFERENTIAL NORMAL OUTPUTS. The output signals must be AC coupled to the pulse detector.
IFC	FREQUENCY PROGRAM CONTROL. The filter cutoff frequency FC, is set by an external current sink, from this pin. IFC must be proportional to current IFO. This current can be set with an external current generator such as a DAC, referenced to IFO.
IFO	PTAT CURRENT REFERENCE OUTPUT. This pin ouputs a PTAT reference current which is externally scaled for control input into IFC. IFO is proportional to absolute temperature (PTAT).
RX	PTAT REFERENCE CURRENT SET. PTAT (proportional to absolute temperature) reference current IFO is equivalent to the current set on this pen.
VBP	FREQUENCY BOOST PROGRAM INPUT. The slimmer high frequency boost is set by an external voltage applied to this pin. VBP must be proportional to voltage VR. A fixed amount of boost can be set by an external resistor divider network connected from VBP to VR and GND. No boost is applied if the FBST pin is grounded, or at logic low.
FBST	FREQUENCY BOOST. A high logic level or open input enables the frequency boost circuitry (32F8021 only).
$\overline{\text{LOWZ}}$	A high logic level or open input selects the high-impedance mode, at VIN±, a low-logic level selects the low impedance input state (32F8023 only).
PWRON	POWER ON. A high logic level enables the chip. A low level puts the chip in a low power state. A low or open circuit disables the chip.
VR	REFERENCE VOLTAGE. Internally generated reference voltage.
VCC	+5 VOLT SUPPLY.
GND	GROUND

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

PARAMETER	RATINGS	UNIT
Storage Temperature	-65 to +150	°C
Junction Operating Temperature, Tj	+130	°C
Supply Voltage, VCC	-0.5 to 7	V
Voltage Applied to Inputs	-0.5 to VCC	V
Maximum Power Dissipation, fc = 8 MHz, Vcc = 5.5V	198	mW

RECOMMENDED OPERATING CONDITIONS

PARAMETER	RATINGS	UNIT
Supply voltage, VCC	4.5 < VCC < 5.50	V
Ambient Temperature Range	0 < Ta < 70	°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified recommended operating conditions apply.

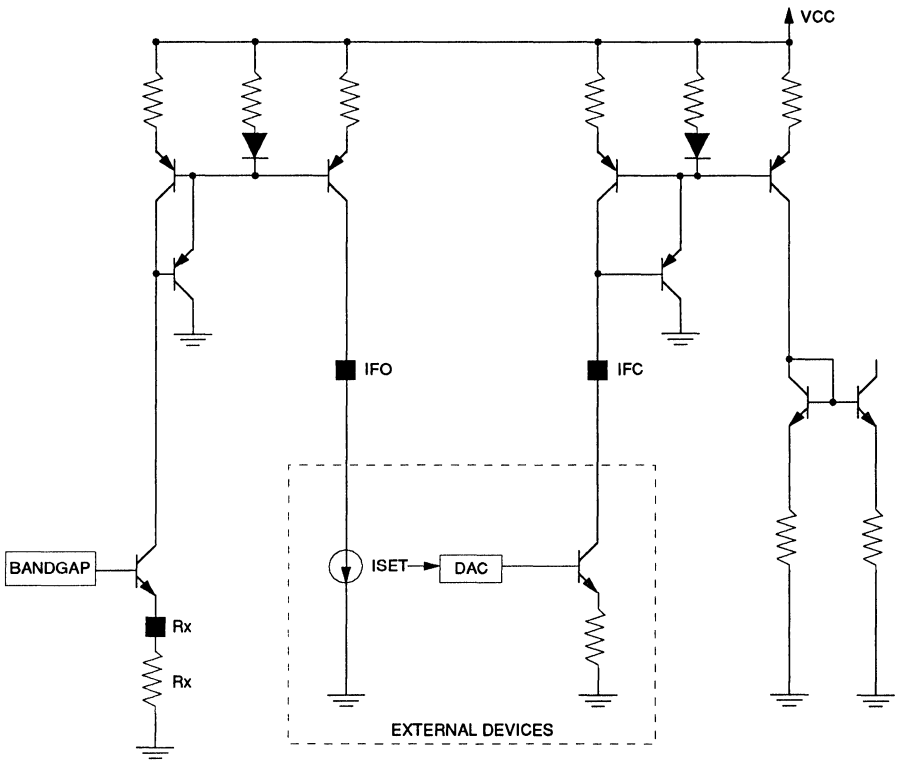
PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Power Supply Characteristics						
ICC, Power Supply Current		PWRON = 0.8V			0.5	mA
ICC, Power Supply Current		PWRON ≥ 2.2V		26	32	mA
PD	Power Dissipation	PWRON ≥ 2.2V, VCC = 5.0V		130	160	mW
		PWRON ≥ 2.2V, VCC = 5.5V		143	176	mW
DC Characteristics						
VIH	High Level Input Voltage	TTL input	2.0			V
VIL	Low Level Input Voltage				0.8	V
IIH	High Level Input Current	VIH = 2.7V			20	µA
IIL	Low Level Input Current	VIL = 0.4V			−1.5	mA
Filter Characteristics						
fc	Filter Cutoff Frequency	Rx = 5 kΩ $fc = 8.0\ \text{MHz} \times \frac{IFC}{4\ IFO}$	1.5		8.0	MHz
FCA	Filter *fc* Accuracy	*fc* = 8 MHz	−10		+10	%
AO	VO_NORM Diff Gain	F = 0.67 *fc*, FB = 0 dB	0.8		1.2	V/V
FB	Frequency Boost at *fc*	$FB(dB) = 20\ \log\left[1.884\left(\frac{VBP}{VR}\right)+1\right]$ VBP = VR		9.2		dB
FBA	Frequency Boost Accuracy	FB = 9.0 dB	−1		+1	dB
TGD0	Group Delay Variation Without Boost	*fc* = 8 MHz, VBP = 0V F = 0.2 *fc* to *fc*	−1.3		+1.3	ns
		fc = 1.5 MHz - 8 MHz F = 0.2 *fc* to *fc*, VBP=0V	−2		+2	%

ELECTRICAL CHARACTERISTICS, (Continued)
Unless otherwise specified recommended operating conditions apply.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Filter Characteristics, continued						
TGDB	Group Delay Variation With Boost	fc = 8 MHz, VBP = VR F = 0.2 fc to fc	–1.3		+1.3	ns
		fc = 1.5 MHz - 8 MHz F = 0.2 fc to fc, VBP=VR	–2		+2	%
VIF	Filter Input Dynamic Range	THD = 1% max, F = 0.67 fc	1.0			Vpp
VOF	Filter Output Dynamic Range	THD = 1% max, F = 0.67 fc	1.0			Vpp
VIF	Filter Input Dynamic Range	THD = 3% max, F = 0.67 fc	2.0			Vpp
VOF	Filter Output Dynamic Range	THD = 3% max, F = 0.67 fc	2.0			Vpp
RIN	Filter Diff Input Resistance	LOWZ = high or open	3.0	4.0		kΩ
		LOWZ = low		150	300	Ω
CIN	Filter Input Capacitance				7	pF
EOUT	Output Noise Voltage Normal Output	BW = 100 MHz, Rs = 50Ω IFC = 0.6 mA, VBP = VR		4.1		mVRms
EOUT	Output Noise Voltage Normal Output	BW = 100 MHz, Rs = 50Ω IFC = 0.6 mA, VBP = 0.0V		2.7		mVRms
IO–	Filter Output Sink Current		1.0			mA
IO+	Filter Output Source Current		2.0			mA
RO	Filter Output Resistance (Single ended)	IO+ = 1.0 mA			60	Ω
Filter Control Characteristics						
VR	Reference Voltage		2.0		2.40	V
VBP	Frequency Boost Control Voltage Range	VR = 2.2V FBOOST = 0 to 9.2 dB	0		2.2	V
VRX	PTAT Reference Current Set Output Voltage	TA = 25°C IRX = 0 - 0.6 mA Rx > 1.25 kΩ		750		mV
IFO	PTAT Reference Current, Output Current Range	TA = 25°C 1.25 kΩ < Rx < 6.8 kΩ IFO = VRX/Rx VRX = 750 mV	0.11		0.6	mA
IFC	PTAT Programming Current Range	TA = 25°C, VRX = 750 mV	0.11		0.6	mA

TIMING CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Transition to/from $\overline{\text{LOWZ}}$ (8023)			TBD		ns
Transition to Idle Mode	PWRON switches from high to low		TBD		ns
Transition from Idle Mode	PWRON switches from low to high		TBD		µs



VRX = 750 mV @25°C

IRX = IFO

IFC programming range: 0.11 mA to 0.60 mA @25°C
(1.5 to 8.0 MHz: No Boost)

The IFC (programming current) is scaled from IFO (reference current) by the set-up shown above. Assuming the DAC current gain = 8.0, then programming is accomplished as follows:

MAX programming current required: IFC = 0.6 mA (fc = 8.0 MHz) @25°C

IFO = IFC/8 = 0.075 mA (MAX) @25°C

IRX = IFO

IRX = 750mV/Rx @25°C

Rx = 10 kΩ

FIGURE 1: 32F8021/8023 Frequency Programming

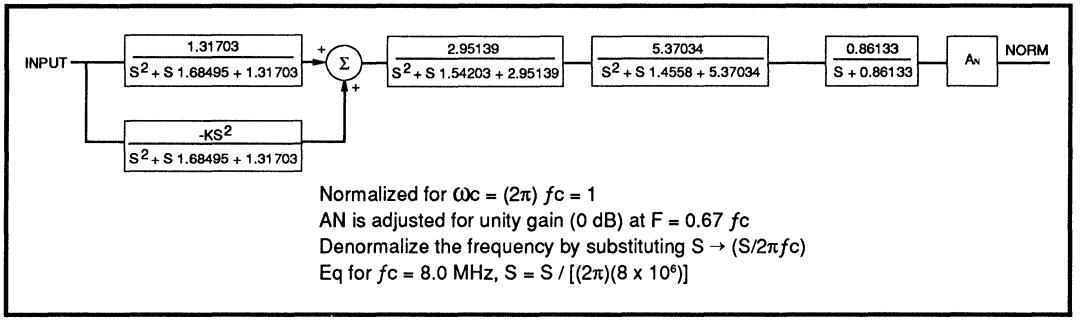


FIGURE 2: 32F8021/8023 Normalized Block Diagram

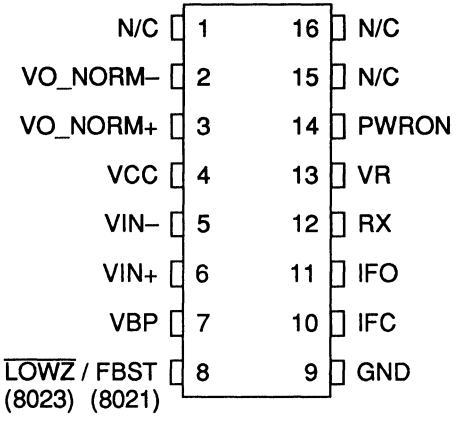
TABLE 1: 32F8011 Frequency Boost Calculations

Assuming 9.2 dB boost for **VBP = VR**	**Boost**	**VBP/VR**
	1 dB	0.065
	2 dB	0.137
	3 dB	0.219
	4 dB	0.310
	5 dB	0.413
$\frac{VBP}{VR} \cong \frac{(10^{(FB/20)})-1}{1.884}$	6 dB	0.528
	7 dB	0.658
	8 dB	0.802
	9 dB	0.965

or,	**VBP/VR**	**Boost**
	0.1	1.499 dB
	0.2	2.777 dB
	0.3	3.891 dB
	0.4	4.879 dB
$\text{boost in dB} \cong 20\log\left[1.884\left(\frac{VBP}{VR}\right)+1\right]$	0.5	5.765 dB
	0.6	6.569 dB
	0.7	7.305 dB
	0.8	7.984 dB
	0.9	8.613 dB
	1.0	9.200 dB

PIN DIAGRAM

(Top View)



32F8021/8023
16-pin DIP, SON, SOL

ORDERING INFORMATION

PART DESCRIPTION	ORDERING NUMBER	PACKAGE MARK
SSI 32F8021 Low-Power Programmable Electronic Filter		
16-Lead SON (150 mil)	32F8021-CN	32F8021
16-Lead SOL (300 mil)	32F8021-CL	32F8021
16-Lead PDIP	32F8021-CP	32F8021-CP
SSI 32F8023 Low-Power Programmable Electronic Filter		
16-Lead SON (150 mil)	32F8023-CN	32F8023
16-Lead SOL (300 mil)	32F8023-CL	32F8023
16-Lead PDIP	32F8023-CP	32F8023-CP

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 731-7110, FAX (714) 573-6914

Notes:

silicon systems®
A TDK Group Company

SSI 32F8030
Programmable Electronic Filter
Advance Information

November 1991

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DESCRIPTION

The SSI 32F8030 Programmable Electronic Filter provides an electronically controlled low–pass filter with a separate differentiated low–pass output. A seven–pole, 0.05° Equiripple-type linear phase, low–pass filter is provided along with a single-pole, single-zero differentiator. Both outputs have matched delays. The delay matching is unaffected by any amount of programmed high frequency peaking (boost) or bandwidth. This programability, combined with low group delay variation makes the SSI 32F8030 ideal for use in many applications. Double differentiation high frequency boost is accomplished by a two–pole, low–pass with a two–pole, high–pass feed forward section to provide complementary real axis zeros. A variable attenuator is used to program the zero locations, which controls the amount of boost.

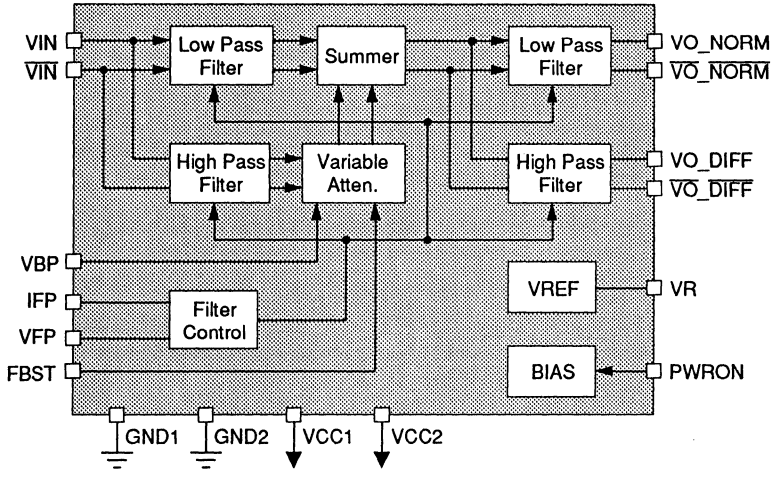
The SSI 32F8030 programmable boost and bandwidth characteristics can be controlled by external DACs or DACs provided in the SSI 32D4661 Time Base Generator. Fixed characteristics are easily accomplished with three external resistors, in addition boost can be switched in or out by a logic signal.

The SSI 32F8030 requires only a +5V supply and is available in 16-pin DIP, SON, and SOL packages.

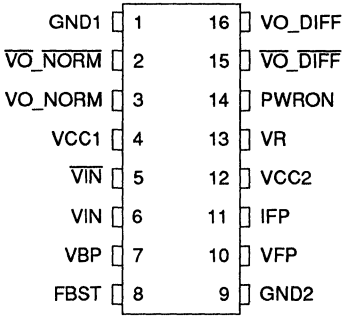
FEATURES

- **Ideal for:**
  - **constant density recording applications**
  - **magnetic tape recording**
- **Programmable filter cutoff frequency (fc = 250 kHz to 2.5 MHz)**
- **Programmable high frequency peaking (0 to 9 dB boost at the filter cutoff frequency)**
- **Matched normal and differentiated low-pass outputs**
- **Differential filter input and outputs**
- **±3.0% group delay variation from 0.2 fc to fc = 2.5 MHz**
- **Total harmonic distortion less than 1%**
- **+5V only operation**
- **16-pin DIP, SON, and SOL packages**
- **5 mW idle mode**

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION

The SSI 32F8030, a high performance programmable electronic filter, provides a low pass 0.05° Equiripple-type linear phase seven pole filter with matched normal and differentiated outputs. The device has been optimized for usage with several Silicon Systems products, including the SSI 32D4661 Time Base Generator, the SSI 32P54x family of Pulse Detectors, and the SSI 32P4622 and 32P4720 Combo chips (Data Separator and Pulse Detector).

CUTOFF FREQUENCY PROGRAMMING

The SSI 32F8030 programmable electronic filter can be set to a filter cutoff frequency from 250 kHz to 2.5 MHz (with no boost).

Cutoff frequency programming can be established using either a current source fed into the IFP pin, whose output current is proportional to the SSI 32F8030 output reference voltage VR, or by means of an external resistor tied from the output voltage reference pin VR to pin VFP. The former method is optimized using the SSI 32D4661 Time Base Generator, since the current source into pin IFP is available at the DAC F output of the 32D4661. Furthermore, the voltage reference input is supplied to pin VR3 of the 32D4661 by the reference voltage VR from the VR pin of the 32F8030. This reference voltage is an internally generated bandgap reference, which typically varies less than 1 % over voltage supply and temperature variation. (For the calculations below IVFP = current into IFP or VFP pins).

The cutoff frequency, determined by the -3dB point relative to a very low frequency value (< 10kHz), is related to the current IVFP injected into pin IFP by the formula

Fc (ideal, in MHz) = 3.125•IFP = 3.125•IVFP•2.2/VR, where IFP and IVFP are in mA, 0.08<IFP<0.8 mA, and VR is in volts.

If a current source is used to inject current into pin IFP, pin VFP should be left open.

If the 32F8030 cutoff frequency is set using voltage VR to bias up a resistor tied to pin VFP, the cutoff frequency is related to the resistor value by the formula

Fc (ideal, in MHz) = 3.125•IFP = 3.125•2.2/(3•Rx) where Rx is in ohms, & 0.917 kΩ <Rx<9.17 kΩ.

If pin VFP is used to program cutoff frequency, pin IFP should be left open.

SLIMMER HIGH FREQUENCY BOOST PROGRAMMING

The amplitude of the input signal at frequencies near the cutoff frequency can be increased using this feature. Applying an external voltage to pin VBP which is proportional to reference output voltage VR (provided by the VR pin) will set the amount of boost. A fixed amount of boost can be set by an external resistor divider network connected from pin VBP to pins VR and GND. No boost is applied if pin FBST, frequency boost enable, is at a low logic level.

The amount of boost FB at the cutoff frequency Fc is related to the voltage VBP by the formula

FB (ideal, in dB) = $20 \log_{10}[1.884(VBP/VR)+1]$, where 0<VBP<VR.

PIN DESCRIPTION

NAME	DESCRIPTION
VIN, $\overline{\text{VIN}}$	DIFFERENTIAL SIGNAL INPUTS. The input signals must be AC coupled to these pins.
VO_NORM, $\overline{\text{VO\_NORM}}$	DIFFERENTIAL NORMAL OUTPUTS. The output signals must be AC coupled.
VO_DIFF, $\overline{\text{VO\_DIFF}}$	DIFFERENTIAL DIFFERENTIATED OUTPUTS. For minimum time skew, these outputs should be AC coupled to the pulse detector.
IFP	FREQUENCY PROGRAM INPUT. The filter cutoff frequency FC, is set by an external current IFP, injected into this pin. IFP must be proportional to voltage VR. This current can be set with an external current generator such as a DAC. VFP should be left open when using this pin.
VFP	FREQUENCY PROGRAM INPUT. The filter cutoff frequency can be set by programming a current through a resistor from VR to this pin. IFP should be left open when using this pin.
VBP	FREQUENCY BOOST PROGRAM INPUT. The high frequency boost is set by an external voltage applied to this pin. VBP must be proportional to voltage VR. A fixed amount of boost can be set by an external resistor divider network connected from VBP to VR and GND. No boost is applied if the FBST pin is grounded, or at logic low.
FBST	FREQUENCY BOOST. A high logic level or open input enables the frequency boost circuitry.
PWRON	POWER ON. A high logic level enables the chip. A low level puts the chip in a low power state.
VR	REFERENCE VOLTAGE. Internally generated reference voltage.
VCC1, VCC2	+5 VOLT SUPPLY.
GND1, GND2	GROUND

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

PARAMETER	RATINGS	UNIT
Storage Temperature	-65 to +150	°C
Junction Operating Temperature, Tj	+130	°C
Supply Voltage, VCC1, VCC2	-0.5 to 7	V
Voltage Applied to Inputs	-0.5 to VCC + 0.5	V
IFP, VFP Inputs Maximum Current	≤1.2	mA

RECOMMENDED OPERATING CONDITIONS

PARAMETER	RATINGS	UNIT
Supply voltage, VCC1, VCC2	4.5 < VCC1,2 < 5.50	V
Ambient Temperature	0 < Ta < 70	°C

ELECTRICAL CHARACTERISTICS

Power Supply Characteristics (Unless otherwise specified, recommended operating conditions apply.)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
ICC	Power Supply Current	PWRON ≤ 0.8V			1	mA
ICC	Power Supply Current	PWRON ≥ 2.0V		35	42	mA

DC Characteristics

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
VIH	High Level Input Voltage	TTL input	2.0		VCC+0.3	V
VIL	Low Level Input Voltage		-0.3		0.8	V
IIH	High Level Input Current	VIH = 2.7V			20	µA
IIL	Low Level Input Current	VIL = 0.4V			–1.5	mA

Filter Characteristics (Fc = 1.25 MHz unless otherwise stated)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
FCA	Filter *fc* Accuracy	using IFP pin: IFP = 0.4 mA or using VFP pin: Rx = 1.84 kΩ	1.125		1.375	MHz
AO	VO_NORM Diff Gain	F = 0.67 *fc*, FB = 0 dB	0.8		1.20	V/V
AD	VO_DIFF Diff Gain	F = 0.67 *fc*, FB = 0 dB	0.8AO		1.0AO	V/V
FBA	Frequency Boost Accuracy	VBP = VR	8.0	9.2	10.4	dB
TGD0	Group Delay Variation Without Boost*	*fc* = 0.25 MHz, VBP = 0V F = 0.2 *fc* to *fc*	–40 –2		+40 +2	ns %
TGDB	Group Delay Variation With Boost*	*fc* = 0.25 MHz, VBP = VR F = 0.2 *fc* to *fc*	–40 –2		+40 +2	ns %
TGD0	Group Delay Variation Without Boost*	*fc* = 0.25 MHz, VBP = 0V F = 0.2 *fc* to 1.75 *fc*	–40 –2		+40 +2	ns %
TGDB	Group Delay Variation With Boost*	*fc* = 0.25 MHz, VBP = VR F = 0.2 *fc* to 1.75 *fc*	–40 –2		+40 +2	ns %
TGD0	Group Delay Variation Without Boost*	*fc* = 2.5 MHz, VBP = 0V F = 0.2 *fc* to *fc*	–6 –3		+6 +3	ns %
TGDB	Group Delay Variation With Boost*	*fc* = 2.5 MHz, VBP = VR F = 0.2 *fc* to *fc*	–6 –3		+6 +3	ns %
TGD0	Group Delay Variation Without Boost*	*fc* = 2.5 MHz, VBP = 0V F = 0.2 *fc* to 1.75 *fc*	–6 –3		+6 +3	ns %
TGDB	Group Delay Variation With Boost*	*fc* = 2.5 MHz, VBP = VR F = 0.2 *fc* to 1.75 *fc*	–6 –3		+6 +3	ns %
VIF	Filter Input Dynamic Range	THD = 1% max, F = 0.67 *fc* (no boost)	1.0			Vpp
VOF	Filter Normal Output Dynamic Range	THD = 1% max, F = 0.67 *fc* VBP = 0	1.0			Vpp

ELECTRICAL CHARACTERISTICS (continued)

Filter Characteristics (continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
VOF	Filter Normal Output Dynamic Range	THD = 1% max, F = 0.67 *fc* VBP = VR	1.0			Vpp
VOF	Filter Differentiated Output Dynamic Range	THD = 1% max, F = 0.67 *fc* VBP = 0	1.0			Vpp
VOF	Filter Differentiated Output Dynamic Range	THD = 1% max, F = 0.67 *fc* VBP = VR	1.0			Vpp
RIN	Filter Diff Input Resistance		3.0	4.0		kΩ
CIN	Filter Diff Input Capacitance*			3.0		pF
EOUT	Output Noise Voltage* Differentiated Output	BW = 100 MHz, Rs = 50Ω, I*fp* = 0.8 mA, VBP = 0.0V		3.0	3.2	mVRms
EOUT	Output Noise Voltage* Normal Output	BW = 100 MHz, Rs = 50Ω I*fp* = 0.8 mA, VBP = 0.0V		1.8	2.0	mVRms
EOUT	Output Noise Voltage* Differentiated Output	BW = 100 MHz, Rs = 50Ω I*fp* = 0.8 mA, VBP = VR		3.5	3.8	mVRms
EOUT	Output Noise Voltage* Normal Output	BW = 100 MHz, Rs = 50Ω I*fp* = 0.8 mA, VBP = VR		2.0	2.2	mVRms
EOUT	Output Noise Voltage* Differentiated Output	BW = 10 MHz, Rs = 50Ω, I*fp* = 0.08 mA, VBP = 0.0V		1.7	1.8	mVRms
EOUT	Output Noise Voltage* Normal Output	BW = 10 MHz, Rs = 50Ω I*fp* = 0.08 mA, VBP = 0.0V		1.0	1.2	mVRms
EOUT	Output Noise Voltage* Differentiated Output	BW = 10 MHz, Rs = 50Ω I*fp* = 0.08 mA, VBP = VR		1.9	2.2	mVRms
EOUT	Output Noise Voltage* Normal Output	BW = 10 MHz, Rs = 50Ω I*fp* = 0.08 mA, VBP = VR		1.1	1.2	mVRms
IO–	Filter Output Sink Current		1.0			mA
IO+	Filter Output Source Current		2.0			mA
RO	Filter Output Resistance**				60	Ω

* Not directly testable in production, design characteristic.

** Single ended

Filter Control Characteristics

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
VR	Reference Voltage Output		2.0		2.40	V
I_{VR}	Reference Output Source Current				2.0	mA

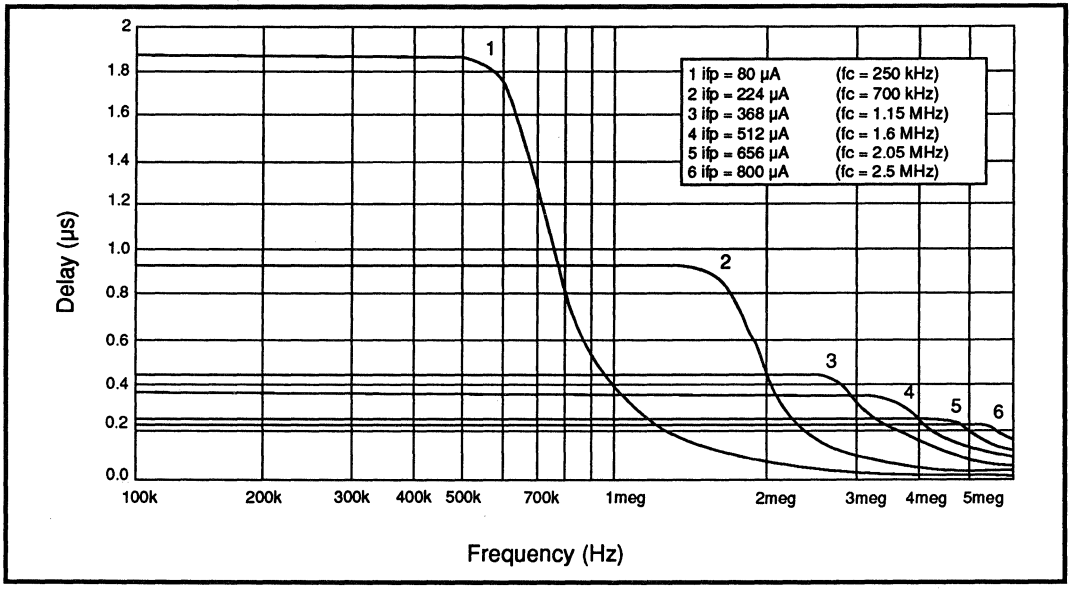


FIGURE 1: Typical Normal/Differentiated Output Group Delay Response

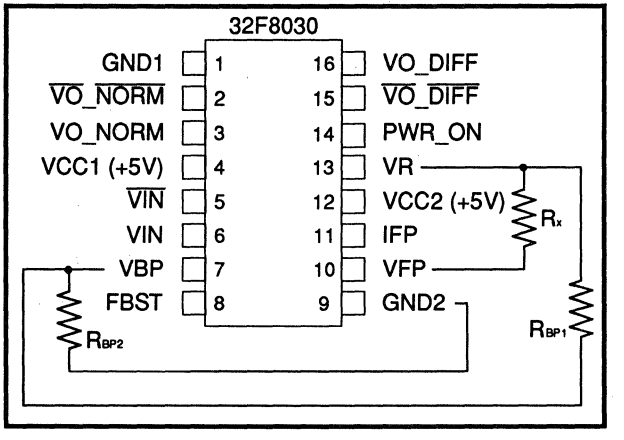


FIGURE 1: 32F8030 Applications Setup, 16-Pin SO or DIP

VR = 2.2V	IVfp = .33VR/Rx
VFP = .667 VR	IVfp range: 0.08 mA to 0.8 mA (0.25 MHz to 2.5 MHz)

VFP is used when programming current is set with a resistor from VR. When VFP is used IFP must be left open.

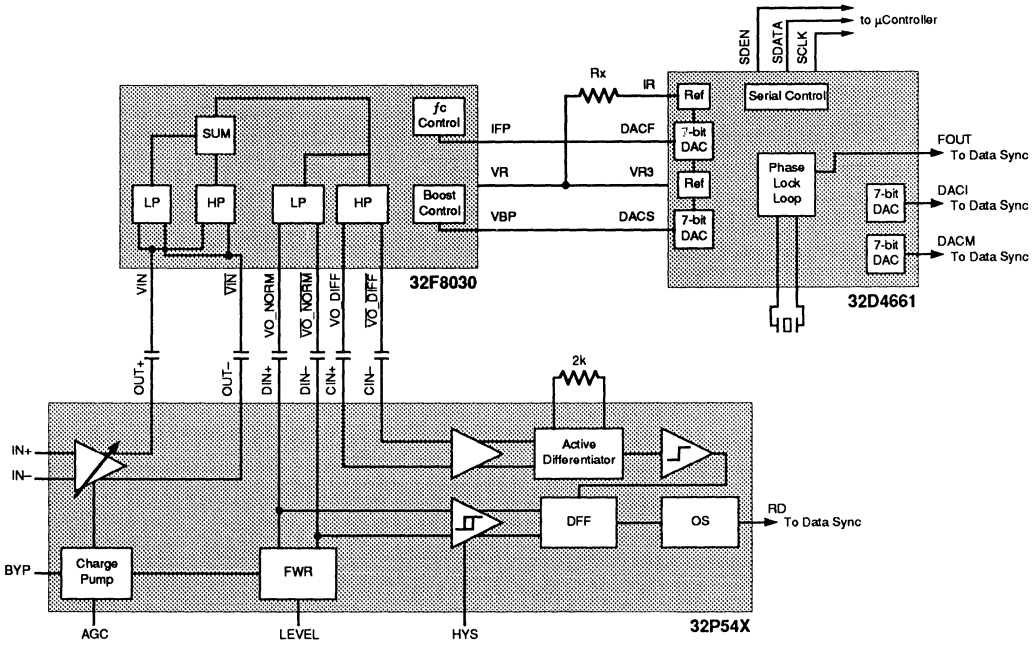


FIGURE 2: Applications Setup, Constant Density Recording
32F8030, 32P54X, 32D4661

IOF = DACF output current

IOF = (0.98F•VR)/127Rx

Rx = (0.98F•VR)/127IOF

Rx = current reference setting resistor

VR = Voltage Reference = 2.2V

F = DAC setting: 0-127

Full scale, F = 127

For range of Max fc = 2.5 MHz then IFP = 0.8 mA

Therefore, for Max programming current range to 0.8 mA:

Rx = (0.98)(2.2/0.8) = 2.7 kΩ

Please note that in setups such as this where IFP is used for cutoff frequency programming VFP must be left open.

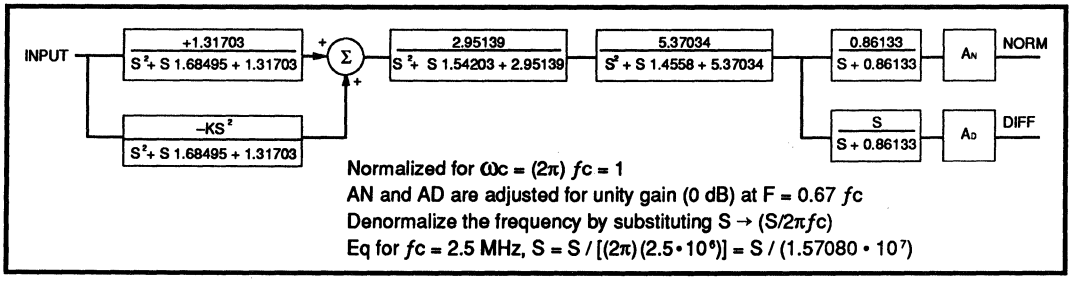


FIGURE 3: 32F8030 Normalized Block Diagram

TABLE 1: 32F8030 Frequency Boost Calculations

Assuming 9.2 dB boost for VBP = VR

$$\frac{VBP}{VR} \cong \frac{\left(10^{(FB/20)}\right)-1}{1.884}$$

Boost	VBP/VR	Boost	VBP/VR
1 dB	0.065	6 dB	0.528
2 dB	0.137	7 dB	0.658
3 dB	0.219	8 dB	0.802
4 dB	0.310	9 dB	0.965
5 dB	0.413		

or,

boost in dB ≅ 20 log $\left[1.884\left(\frac{VBP}{VR}\right)+1\right]$

VBP/VR	Boost	VBP/VR	Boost
0.1	1.499 dB	0.6	6.569 dB
0.2	2.777 dB	0.7	7.305 dB
0.3	3.891 dB	0.8	7.984 dB
0.4	4.879 dB	0.9	8.613 dB
0.5	5.765 dB	1.0	9.200 dB

TABLE 2: Calculations

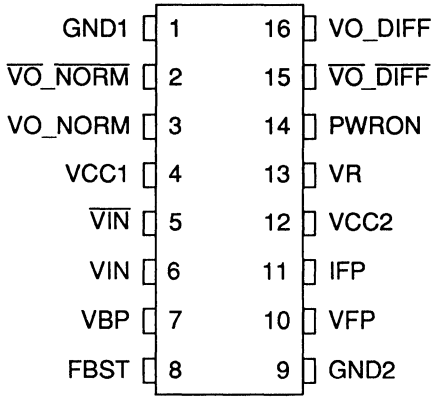
Typical change in *f*-3 dB point with boost

Boost at *fc*	*f*-3 dB/*fc*	Boost at *fc*	*f*-3 dB/*fc*
0 dB	1.0	5 dB	2.13
1	1.2	6	2.28
2	1.47	7	2.41
3	1.74	8	2.53
4	1.95	9	2.65

Notes: 1. *fc* is the original programmed cutoff frequency with no boost
2. *f*-3 dB is the new -3 dB value with boost implemented

i.e., *fc* = 2.5 MHz when boost = 0 dB
if boost is programmed to 5 dB then f-3 dB = 5.32 MHz

PIN DIAGRAM (Top View)



16-pin DIP, SON, SOL

Thermal Characteristics: ØjA

16-lead SON (150 mil)	105° C/W
16-lead SOL (300 mil)	100° C/W
16-lead PDIP	170° C/W

3

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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Notes:

silicon systems®
A TDK Group Company

SSI 32F8120
Low-Power Programmable Electronic Filter
Advance Information

November 1991

3

DESCRIPTION

The SSI 32F8120 is a continuous time low pass filter with programmable bandwidth and high frequency boost. The low pass filter is of a 2 zero / 7 pole 0.05° phase equiripple type, featuring excellent group delay characteristics. It features 1.5 - 8 MHz programmable bandwidth and 0 - 9.5 dB programmable boost. Both functions are controlled by 7-bit command words, which are input via a 3-line serial interface.

FUNCTIONAL DESCRIPTION

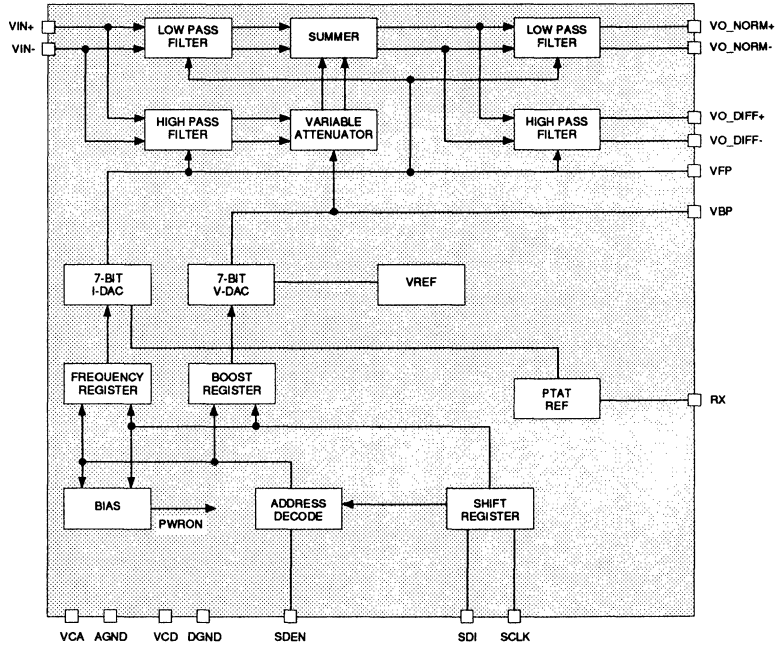
The SSI 32F8120, a high performance programmable electronic filter, provides a low pass equiripple type seven pole filter with matched normal and differentiated outputs.

(continued)

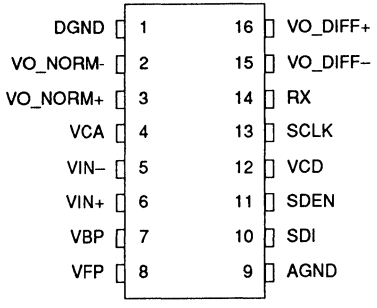
FEATURES

- **Programmable filter cutoff frequency (FC=1.5 to 8 MHz) with no external components**
- **Programmable pulse slimming equalization (0 to 9.5 dB boost at the filter cutoff frequency)**
- **± 10% cutoff frequency accuracy**
- **Matched normal and differentiated low-pass outputs**
- **Differential filter inputs and outputs**
- **Device idle mode**
- **+5V only operation**
- **No external filter components required**
- **Supports constant density recording**

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION (continued)

CUTOFF FREQUENCY PROGRAMMING

The SSI 32F8120 programmable electronic filter can be set to a filter cutoff frequency from 1.5 to 8 MHz. The cutoff frequency can be set by using the serial port through pins SDI, SDEN, and SCLK. SDI is the serial data input for an 8-bit control shift register, SDEN is the control register enable, and SCLK is the control register clock. The data packet is transmitted MSB (D7) first. The first four bits are the register address, the last four are the data bits. Registers larger than four bits must be loaded with two 8-bit data packets. These packets should be loaded sequentially and in less than 10 microseconds. See Table 1.

The cutoff frequency is determined by the equation:

$$Fc = 8 \times \frac{F\_Code}{127} (MHz)$$

$$1.5\ MHz \leq Fc \leq 8\ MHz$$

SLIMMER HIGH FREQUENCY BOOST PROGRAMMING

The amplitude of the input signal at frequencies near the cutoff frequency can be increased using this feature. By controlling the V-DAC output, the boost can be determined. The amount of boost at the cutoff frequency is related to the V-DAC output by the following formula:

$$[Ouput\ of\ V-DAC = VBP = VREF \times \frac{S\_Code}{127}]$$

$$BOOST\ (dB) = 20*\log\ [0.01563\ (S\_Code) + 1].$$

TABLE 1:

ADDRESS BITS				USAGE	DATA BITS			
D7	D6	D5	D4		D3	D2	D1	D0
X	0	0	0	S-MSB REGISTER	X	S6	S5	S4
X	0	0	1	S-LSB REGISTER	S3	S2	S1	S0
X	0	1	0	F-MSB REGISTER	X	F6	F5	F4
X	0	1	1	F-LSB REGISTER	F3	F2	F1	F0
X	1	1	1	P REGISTER	X	X	X	P0

X = Don't Care
S = 7-bit Boost (Slimming) Control
F = 7-bit Frequency (Bandwidth) Control
P = Power Down Control; PO = 1 for power up; PO = 0 for power down

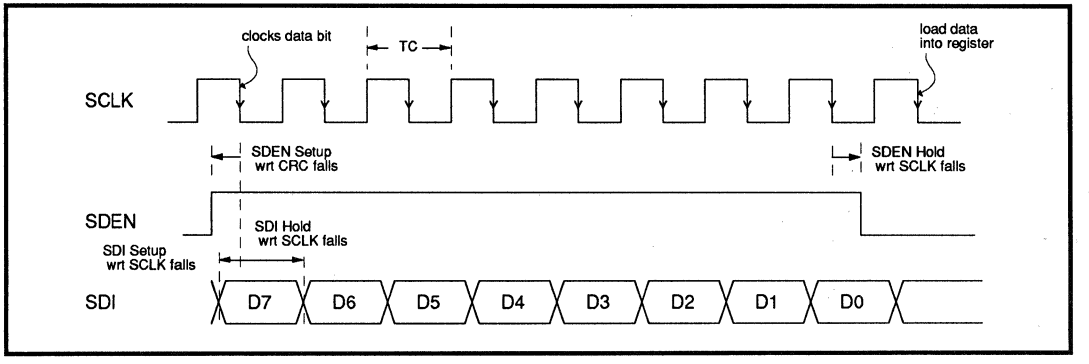


FIGURE 1: Serial Port Timing Diagram

PIN DESCRIPTIONS

NAME	DESCRIPTION
VIN+, VIN–	DIFFERENTIAL FILTER INPUTS. The input signals must be AC coupled to these pins.
VO_NORM+, VO_NORM–	DIFFERENTIAL NORMAL OUTPUTS. The output signals must be AC coupled to the pulse detector.
VO_DIFF+ VO_DIFF–	DIFFERENTIAL DIFFERENTIATED OUTPUTS. For minimum pulse pairing, these outputs should be AC coupled to the pulse detector.
SDEN	SERIAL DATA ENABLE. A logic HIGH level allows SERIAL CLOCK to clock data into the control register via the SERIAL DATA input. A logic LOW level latches the register data and issues the information to the appropriate circuitry.
SCLK	SERIAL CLOCK. Negative edge triggered clock input for serial register.
SDI	SERIAL DATA INPUT.
RX	REFERENCE CURRENT SET. With an external resistor (Rx = 5KΩ ±1%) to ground, this pin gives a voltage proportional to the absolute temperature, setting the range for VFP.
VCC1	ANALOG +5 VOLT SUPPLY.
VCC2	DIGITAL +5 VOLT SUPPLY.
GND1	ANALOG GROUND.
GND2	DIGITAL GROUND.
VBP	BOOST PROGRAMMING VOLTAGE. Output of V-DAC which programs the boost.
VFP	CUTOFF FREQUENCY PROGRAMMING VOLTAGE. Output of I-DAC which programs the cutoff frequency.*

*A minimum load resistance of 150kΩ should be used so as not to affect the total minimum on-chip resistance of 1.35kΩ.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

PARAMETER	RATINGS	UNIT
Storage Temperature	-65 to +150	°C
Junction Operating Temperature, Tj	+130	°C
Supply Voltage, VCC	-0.5 to 7	V
Voltage Applied to Inputs*	-0.5 to VCC	V
Maximum Power Dissipation, fc = 8 MHz, Vcc = 5.5V	.5	W
T1 Lead Temperature (1/16" from case for 10 seconds)	260	°C

* Analog input signals of this magnitude shall not cause any change or degradation in filter performance after signal has returned to normal operating range.

ELECTRICAL SPECIFICATIONS (continued)

RECOMMENDED OPERATING CONDITIONS

PARAMETER	RATINGS	UNIT
Supply voltage, VCC	4.5 < VCC < 5.50	V
Ambient Temperature	0 < Ta < 70	°C
Tj Junction Temperature	0 < Tj < 130	°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified recommended operating conditions apply.

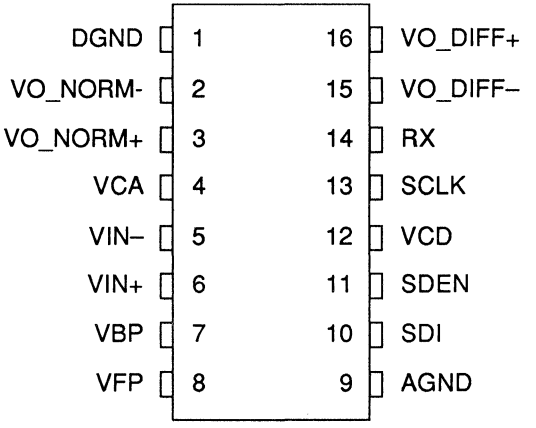
PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Isupply		VCC = 5.50V, outputs unloaded			75	mA
Idle Mode Current				11	15	mA
Idle to Active Mode Recovery Time					50	µs
Serial port program to output response time					50	µs
DC Characteristics						
VIH	High Level Input Voltage	TTL input	2.0			V
VIL	Low Level Input Voltage				0.8	V
IIH	High Level Input Current	VIH = 2.7V			20	µA
IIL	Low Level Input Current	VIL = 0.4V			–1.5	mA
Filter Characteristics						
fc	Filter Cutoff Frequency	*fc* = VFP, 24 ≤ F_Code ≤ 127	1.5		8	MHz
FCA	Filter *fc* Accuracy	*fc* = VFP, 24 ≤ F_Code ≤ 127	-10		+10	%
	Cutoff Resolution	1.5 to 8 MHz	100			kHz
AO	VO_NORM Diff Gain	F = 0.67 *fc*	0.8		1.2	V/V
AD	VO_DIFF Diff Gain	F = 0.67 *fc*	0.90 AO		1.1 AO	V/V
FB	Frequency Boost at *fc*	FB(dB) = 20 log [.01563 (S_Code) +1]	0		9.5	dB
FBA	Frequency Boost Accuracy	0 to 9.5 dB	–1		+1	dB
TGD0	Group Delay Variation Without Boost	0.2 *fc* - *fc*	–2% gdm		+2% gdm	ns
	fc = 1.5 - 8 MHz gdm = group delay magnitude	*fc* - 1.75 *fc*	–3% gdm		+3% gdm	ns

ELECTRICAL CHARACTERISTICS (continued)
Unless otherwise specified recommended operating conditions apply.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Filter Characteristics, continued					
TGDB Group Delay Variation With Boost	0.2 *fc* - *fc*	–2% gdm		+2% gdm	ns
fc = 1.5 - 8 MHz	*fc* - 1.75 *fc*	–3% gdm		+3% gdm	ns
Boost Resolution	1.5 to 8 MHz	.25			dB
VIF Filter Input Dynamic Range	THD = 1.5 % max, VBP = 0	1.5			Vppd
VOF Filter Output Dynamic Range	THD = 1.5 % max, VBP = 0	1.5			Vppd
RIN Filter Diff Input Resistance		3.0			kΩ
CIN Filter Input Capacitance				7	pF
EOUT Output Noise Voltage (VO_NORM)	BW = 100 MHz, 0 dB Boost, 50Ω input		2.2	3	mVRms
	fc = 8 MHz 9.5 dB Boost		3.2	4	mVRms
EOUT Output Noise Voltage (VO_DIFF)	BW = 100 MHz, 0 dB Boost, 50Ω input		4.7	6	mVRms
	fc = 8 MHz 9.5 dB Boost		7.5	9	mVRms
IO– Filter Output Sink Current		1.0			mA
IO+ Filter Output Source Current		3.0			mA
RO Filter Output Resistance (Single ended)	Output source current, IO+ = 1 mA			60	Ω
TC Period, SCLK		100			ns
T1 SDEN Setup to SCLK		0		TC/4	ns
T2 SDEN Hold to SCLK		0		TC/4	ns
T3 SDI Setup to SCLK		25			ns
T4 SDI Hold to SCLK		25			ns
Power Supply Rejection Ratio		TBD	TBD		dB
Common Mode Rejection Ratio		TBD	TBD		dB
Bias: Vin+, Vin-		2.5	2.9	3.3	
VVO_NORM+, VO_NORM–	VCC = 5V	2.8	3.2	3.6	V
VO_DIFF+, VO_DIFF-		2.8	3.2	3.6	V
Normal Output Offset	VDAC switched from 0-127	TBD	TBD	TBD	V
Differentiated output offset	VDAC switched from 0-127	TBD	TBD	TBD	V

SSI 32F8120
Low-Power Programmable Electronic Filter

PACKAGE PIN DESIGNATIONS
(Top View)



16-pin SOL

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only.

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A TDK Group Company

SSI 32F8130/8131
Low-Power Programmable Electronic Filter
Advance Information

November 1991

3

DESCRIPTION

The SSI 32F8130/8131 Programmable Electronic Filter is a digitally controlled low pass filter with a normal low pass output and a time differentiated low pass output. The low pass filter is of a 7-pole / 2-zero 0.05° phase equiripple type, with flat group delay response beyond the passband.

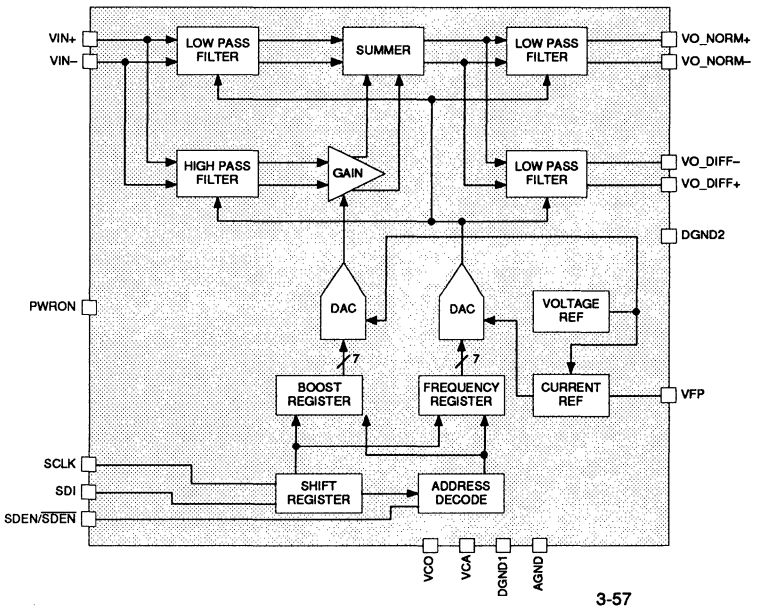
The SSI 32F8130/8131 bandwidth and boost are controlled by two on-chip 7-bit DACs, which are programmed via a 3-line serial interface. The SSI 32F8130 filter bandwidth is programmable from 250 kHz to 2.5 MHz. The SSI 32F8131 is programmable from 150 kHz to 1.5 MHz. The boost is programmable from 0 to 10 dB. Because the boost function is implemented as two zeros on the real axis with opposite sign, the flat group delay characteristic is not affected by the boost programming.

The SSI 32F8130/8131 is ideal for multi-rate, equalization applications. It requires only a +5V supply and has a power down mode for minimal idle dissipation. The SSI 32F8130/8131 is available in 16-pin PDIP and SOL packages.

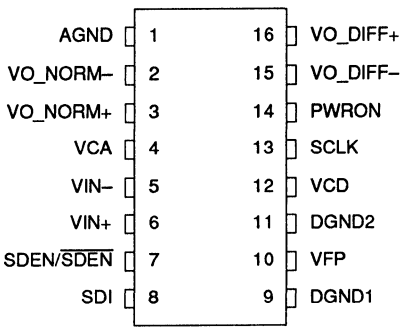
FEATURES

- **Programmable filter cutoff frequency (SSI 32F8130 FC=0.25 to 2.5 MHz, SSI 32F8131: FC = 0.15 to 1.5 MHz) with no external components, serial data connections to minimze pin count**
- **Power down mode (<5 mW)**
- **Programmable pulse slimming equalization (0 to 10 dB boost at the filter cutoff frequency)**
- **Matched normal and differentiated low-pass outputs**
- **Differential filter inputs and outputs**
- **Programming via internal 7-bit DACs**
- **No external filter components required**
- **+5V only operation**
- **Supports constant density recording**

BLOCK DIAGRAM



PIN DIAGRAM



SSI 32F8130: Pin 7 = SDEN
SSI 32F8131: Pin 7 = $\overline{\text{SDEN}}$

CAUTION: Use handling procedures necessary for a static sensitive component.

SSI 32F8130/8131
Low-Power Programmable Electronic Filter

FUNCTIONAL DESCRIPTION

The SSI 32F8130/8131, a high performance programmable electronic filter, provides a 7-pole / 2-zero 0.05° equiripple linear phase low pass function with matched normal and time differentiated outputs. The device includes multiple biquads and first-order sections to accomplish the filter function, two 7-bit DACs for bandwidth and boost controls, a 3-line serial interface, and complete bias reference circuits. Only one external precision 8.25 kΩ resistor should be connected from the VFP pin to ground for operation. See Figure 1.

SERIAL INTERFACE

The SSI 32F8130/8131 allows easy digital controls of filter bandwidth and magnitude equalization via a 3-line serial interface. The three pins are SDI, SDEN and SCLK. SDI is the serial data input to an internal 8-bit shift register. SDEN is the shift register enable. SCLK is the shift register clock. Besides the 8-bit shift register which accepts data from the SDI input, there are four 4-bit registers which hold the filter bandwidth and boost controls. Two 4-bit registers are assigned to each control function, because a 7-bit binary control is required for each function.

The S-MSB register, whose address code is X000, holds the 3 MSBs of the boost control. The S-LSB register, whose address code is X001, holds the 4 LSBs of the boost control. The F-MSB register, whose address code is X010, holds the 4 MSBs of the cutoff frequency control. The F-LSB register, whose address code is X011, holds the 4 LSBs of the cutoff frequency control.

The serial interface consists of data packets, which are structured as 4-bit address decode followed by 4-bit data. Figure 2 shows the serial interface timing to successfully program the SSI 32F8130/8131.

CUTOFF FREQUENCY PROGRAMMING

The cutoff frequency, fc, is defined as the -3dB bandwidth with no magnitude equalization applied, and is programmable from 250 kHz to 2.5 MHz for SSI 32F8130, and 150 kHz to 1.5 MHz for SSI 32F8131. While the fc is controlled by an on-chip 7-bit DAC, the cutoff frequency resolution is better than 20-kHz step.

Let F_Code be the decimal equivalent of the 7-bit control. The cutoff frequency can be determined by the equation:

SSI 32F8130: fc (MHz) = 2.5 x F_Code / 127.

SSI 32F8131: fc (MHz) = 1.5 x F_Code / 127.

where 12 < F_Code < 127.

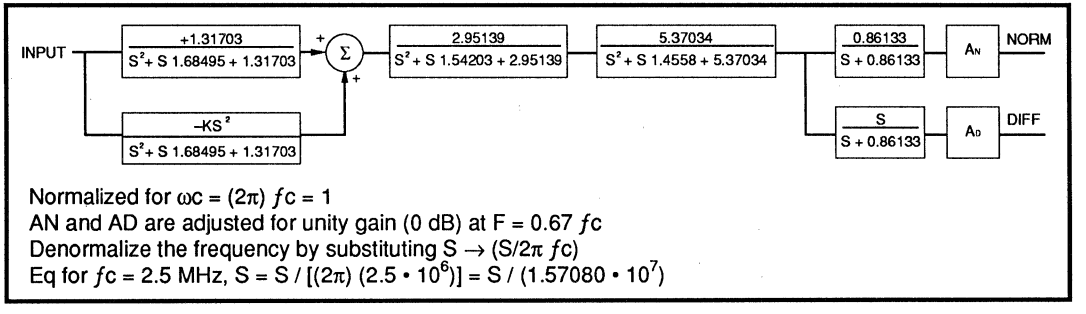
MAGNITUDE EQUALIZATION PROGRAMMING

The magnitude equalization, measured in dB, is the amount of high frequency peaking at the cutoff frequency relative to the original -3 dB point. For example, when 10 dB boost is applied, the magnitude response peaks up 7 dB above the DC gain. This equalization function is also controlled by an on-chip 7-bit DAC.

Let S_Code be the decimal equivalent of the 7-bit control. The magnitude equalization can be determined by the equation:

Boost (dB) = 20 x $\log_{10}$ [0.01703 x S_Code + 1]

where 0 < S_Code < 127.



Normalized for $\omega c = (2\pi)\ fc = 1$
AN and AD are adjusted for unity gain (0 dB) at F = 0.67 fc
Denormalize the frequency by substituting $S \rightarrow (S/2\pi\ fc)$
Eq for fc = 2.5 MHz, $S = S / [(2\pi)\ (2.5 \cdot 10^6)] = S / (1.57080 \cdot 10^7)$

FIGURE 1: Normalized Transfer Function of the SSI 32F8130/8131

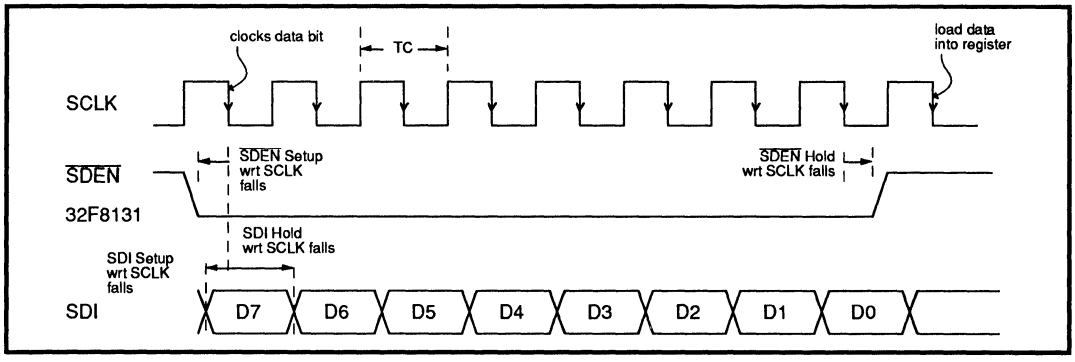


FIGURE 2: Serial Port Timing Relationship

Note:
The serial data enable function of the SSI 32F8130 and that of the SSI 32F8131 are of opposite polarity.

TABLE 1: Data Packet Fields

ADDRESS BITS				USAGE	DATA BITS			
D7	D6	D5	D4		D3	D2	D1	D0
X	0	0	0	S - MSB REGISTER	X	S6	S5	S4
X	0	0	1	S - LSB REGISTER	S3	S2	S1	S0
X	0	1	0	F - MSB REGISTER	X	F6	F5	F4
X	0	1	1	F - LSB REGISTER	F3	F2	F1	F0

X = Don't care bit.

PIN DESCRIPTION

NAME	DESCRIPTION
VIN+, VIN–	DIFFERENTIAL FILTER INPUTS. The input signals must be AC coupled to these pins.
VO_NORM+, VO_NORM–	DIFFERENTIAL NORMAL OUTPUTS. The output signals must be AC coupled to the load.
VO_DIFF+ VO_DIFF–	DIFFERENTIAL DIFFERENTIATED OUTPUTS. These outputs should be AC coupled to the load.
PWR_ON	POWER ON. A TTL high logic level enables the chip. A low level or open circuit puts the chip into a low power state.
$\overline{\text{SDEN}}$ (8130) SDEN (8131)	SERIAL DATA ENABLE. An active level allows SCLK to clock data into the shift register via the SDI input. An inactive level latches the register data and issues the information to the appropriate circuitry. Active level for SSI 32F8130 is HIGH, for SSI 32F8131 is LOW.
SCLK	SERIAL CLOCK. Negative edge triggered clock input for serial register.
SDI	SERIAL DATA INPUT.
VCA	ANALOG +5 VOLT SUPPLY.
VCD	DIGITAL +5 VOLT SUPPLY.
AGND	ANALOG GROUND.
DGND1 DGND2	DIGITAL GROUND.
VFP	CUTOFF FREQUENCY PROGRAMMING REFERENCE. A resistor of 8.25 kΩ should be connected between this pin and AGND.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may permanently damage the device.

PARAMETER	RATINGS	UNIT
Storage Temperature	-65 to +150	°C
Junction Operating Temperature, Tj	+130	°C
Supply Voltage, VCC	-0.5 to 7	V
Voltage Applied to Inputs*	-0.5 to VCC	V
T1 Lead Temperature (1/16" from case for 10 seconds)	260	°C

* Analog input signals of this magnitude shall not cause any change or degradation in filter performance after signal has returned to normal operating range.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	RATINGS	UNIT
Supply voltage, VCC	4.50 < VCC < 5.50	V
Ambient Temperature	0 < Ta < 70	°C
Tj Junction Temperature	0 < Tj < 130	°C

ELECTRICAL SPECIFICATIONS (continued)

ELECTRICAL CHARACTERISTICS

Unless otherwise specified recommended operating conditions apply.

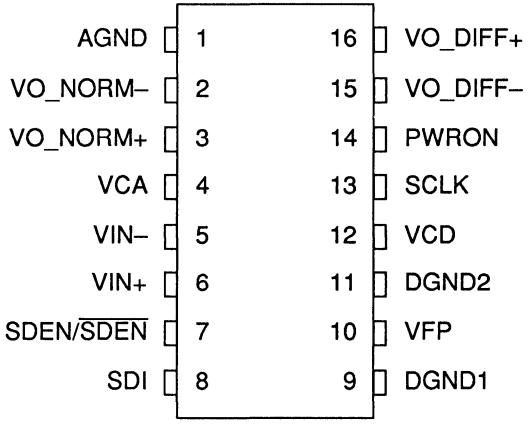
PARAMETER		CONDITIONS		MIN	NOM	MAX	UNIT
Idle Mode Current						1	mA
Idle to Active Mode Recovery Time						50	µs
Serial port program to output response time						50	µs
Isupply					60		mA
DC Characteristics							
VIH	High Level Input Voltage	TTL input		2.0			V
VIL	Low Level Input Voltage					0.8	V
IIH	High Level Input Current	VIH = 2.7V				20	µA
IIL	Low Level Input Current	VIL = 0.4V				−1.5	mA
Filter Characteristics							
fc	Filter Cutoff Frequency	12 < F_Code < 127					
		SSI 32F8130		0.25		2.5	MHz
		SSI 32F8131		0.15		1.5	MHz
FCA	Filter *fc* Accuracy	over *fc* range		-10		+10	%
Cutoff Resolution		$\text{Resolution} = \frac{\text{Max fc}}{127}$	F8130		20		kHz
			F8131		12		kHz
AO	VO_NORM Diff Gain	F = 0.67 *fc*		0.8		1.2	V/V
AD	VO_DIFF Diff Gain	F = 0.67 *fc*		0.9 AO		1.1 AO	V/V
FB	Frequency Boost at *fc*	FB(dB) = 20 log [.01703 (S_Code) + 1] 0 ≤ S_Code ≤ 127		0		10	dB
FBA	Frequency Boost Accuracy	10 dB nominal		-1		+1	dB
TGD0	Group Delay Variation Without Boost	0.2 *fc* - *fc*		-2% gdm		+2% gdm	ns
	fc = 0.25 - 2.5 MHz	*fc* - 1.75 *fc*		-3% gdm		+3% gdm	ns
gdm = group delay magnitude							
TGDB	Group Delay Variation With Boost	0.2 *fc* - *fc*		-2% gdm		+2% gdm	ns
		fc - 1.75 *fc*		-3% gdm		+3% gdm	ns
Boost Resolution				.25			dB
VOF_N	Filter Output Dynamic Range	THD = 1% max, Normal Output		1			Vpp

ELECTRICAL CHARACTERISTICS (continued)
Unless otherwise specified recommended operating conditions apply.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Filter Characteristics, continued					
VOF_D Filter Output Dynamic Range	THD = 1% max, Differentiated Output	1			Vpp
RIN Filter Diff Input Resistance		3.0	4.0		kΩ
CIN Filter Input Capacitance			3.0		pF
EOUT Output Noise Voltage (VO_NORM)	BW = 100 MHz, 50Ω input, 0 dB Boost		1.8		mVRms
	fc = Max fc, 10 dB Boost		2.0		mVRms
EOUT Output Noise Voltage (VO_DIFF)	BW = 100 MHz, 50Ω input, 0 dB Boost		3.0		mVRms
	fc = Max fc, 10 dB Boost		3.5		mVRms
IO– Filter Output Sink Current		1.0			mA
IO+ Filter Output Source Current		3.0			mA
RO Filter Output Resistance (Single ended)	Output source current, IO+ = 1 mA			60	Ω
SDEN Set-up WRT SCLK		0		TC/4	ns
SDEN Hold WRT SCLK		0		TC/4	ns
SDI Set-up WRT SCLK		25			ns
SDI Hold WRT SCLK		25			ns
SCLK Period, TC		100			ns
Power Supply Rejection Ratio		TBD			dB
Common Mode Rejection Ratio		TBD			dB
Bias: VO_NORM±	VCC = 5V		2.75		V
Vin±			2.35		V
VO_DIFF±			2.75		V
Normal Output Offset	S_Code switched from 0-127			TBD	mV
Differentiated output offset	S_Code switched from 0-127			TBD	mV

PACKAGE PIN DESIGNATIONS

(Top View)



16-pin SOL

SSI 32F8130: Pin 7 = SDEN
SSI 32F8131: Pin 7 = $\overline{\text{SDEN}}$

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 731-7110, FAX (714) 573-6914

Notes:

Section

HDD DATA RECOVERY

3

silicon systems®
A TDK Group Company

SSI 32D5321
Data Synchronizer/ 2, 7 RLL ENDEC

November 1991

4

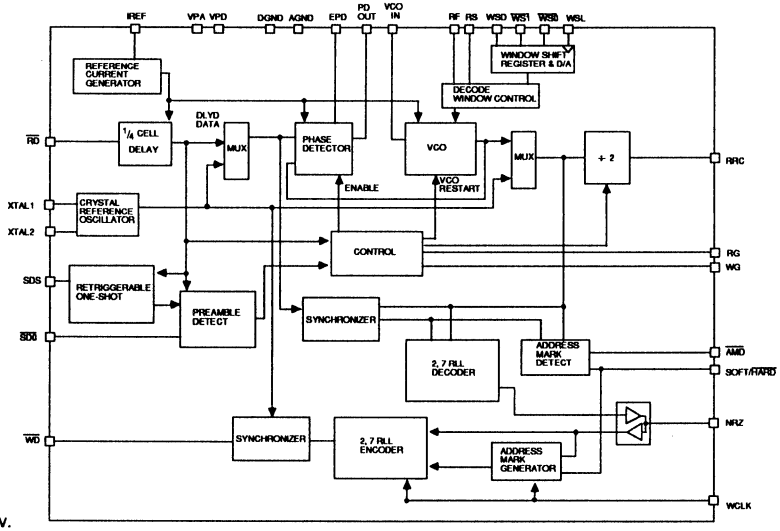
DESCRIPTION

The SSI 32D5321 Data Synchronizer / 2, 7 RLL ENDEC provides data recovery and data encoding for storage systems which employ a 2, 7 RLL encoding format. Data synchronization is performed with a fully integrated high performance PLL. A zero phase restart technique is used to minimize PLL acquisition time. The SSI 32D5321 has been optimized for operation as a companion device to the SSI 32C452A and the AIC 010 controllers. The VCO frequency setting elements are incorporated within the SSI 32D5321 for enhanced performance and reduced board space. Data rate is established with a single external programming resistor. The SSI 32D5321 utilizes an advanced bipolar process technology which affords precise decode window control without the requirement of an accurate 1/4 cell delay or external devices. To enhance disk drive testability, decode window symmetry control is available through a digital µP port and/or two analog pins. This feature can facilitate defect mapping, automatic calibration, systematic error cancellation, window margin testing and error recovery. The SSI 32D5321 requires a single +5V power supply and is available in a 28-pin PLCC package.

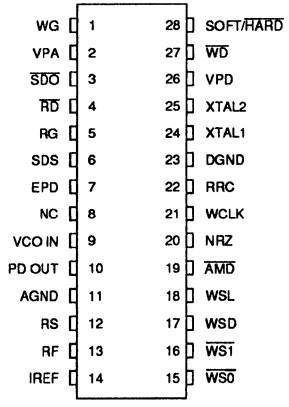
FEATURES

- **Data Synchronizer and 2, 7 RLL ENDEC**
- **7.5 to 10 Mbit/s Operation Programmed with a Single External Resistor or Current Source**
- **Optimized for Operation with the SSI 32C452 and AIC 010 Controllers**
- **Programmable Decode Window Symmetry via a µP Port and/or Analog Pins**
- **Fast Acquisition Phase Locked Loop**
  - **Zero Phase Restart Technique**
- **Fully Integrated Data Separator**
  - **No External Delay Lines or Active Devices Required**
- **Crystal Controlled Reference Oscillator**
- **Hard/Soft Sector Operation**
- **+5V Operation**
- **28-pin PLCC Package**

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

SSI 32D5321
Data Synchronizer/
2, 7 RLL ENDEC

FUNCTIONAL DESCRIPTION

The SSI 32D5322 is designed to perform data recovery and data encoding in rotating memory systems which utilize a 2, 7 RLL encoding format. In the Read Mode the SSI 32D5322 performs Data Synchronization, Sync Field Search and Detect, Address Mark Detect and Data Decoding. In the Write Mode, the SSI 32D5322 converts NRZ data into the 2,7 RLL format described in Table 1, it generates the Preamble Field, and inserts Address Marks as requested. The interface electronics and architecture of the SSI 32D5322 have been optimized for use as a companion device to the SSI 32C452 or AIC 010 controllers.

The SSI 32D5322 can operate with data rates ranging from 7.5 to 10 Mbit/s. This data rate is established by a single 1% external resistor, RR, connected from pin IREF to VPA. This resistor establishes a reference current which sets the VCO center frequency, the phase detector gain, and the 1/4 cell delay. The value of this resistor is given by:

$$RR = \frac{40.67}{DR} - 0.5\ (k\Omega)$$

where: DR = Data Rate in Mbit/s

An internal crystal reference oscillator, operating at twice the data rate, generates the standby reference for the PLL. A series resonant crystal between XTAL1 and XTAL2 should be selected at twice the Data Rate. If a crystal oscillator is not desired, then an external TTL compatible reference may be applied to XTAL1, leaving XTAL2 open.

The SSI 32D5322 employs a Dual Mode Phase Detector; Harmonic in the Read Mode and Non-Harmonic in Write and Idle Modes. In the Read Mode the Harmonic Phase Detector updates the PLL with each occurrence of a DLYD DATA pulse. In the Write and Idle Modes the Non-Harmonic Phase Detector is continuously enabled, thus maintaining both phase and frequency lock. By acquiring both phase and frequency lock to the crystal reference oscillator and utilizing a zero phase restart technique, false lock to DLYD DATA is eliminated.

The phase detector incorporates a charge pump in order to drive the loop filter directly. The polarity and width of the output current pulses correspond to the direction and magnitude of the phase error. Figure 1 depicts the average output current as a function of the input phase error (relative to the VCO period).

The READ GATE (RG), and WRITE GATE (WG), inputs control the device mode as described in Table 2. RG is an asynchronous input and may be initiated or terminated at any position on the disk. WG is also an asynchronous input, but should not be terminated prior to the last output Write Data pulse.

READ OPERATION

The Data Synchronizer utilizes a fully integrated fast acquisition PLL to accurately develop the decode window. Read Gate, RG, initiates the PLL locking sequence and selects the PLL reference input; a high level (Read Mode) selects the $\overline{RD}$ input and a low level selects the crystal reference oscillator.

In the Read Mode the rising edge of DLYD DATA enables the Phase Detector while the falling edge is phase compared to the rising edge of the VCO. As depicted in Figure 2, DLYD DATA is a 1/4 cell wide (TVCO/2) pulse whose leading edge is defined by the leading edge of $\overline{RD}$. An accurate and symmetrical decode window is developed from the VCO clock. The decode window is generated from the falling edges of the VCO clock. By utilizing a fully integrated symmetrical VCO running at twice the data rate, the decode window is insured to be accurate and centered symmetrically about the falling edges of DLYD DATA. The accuracy of the 1/4 cell delay only affects the retrace angle of the phase detector and does not influence the accuracy of the decode window.

Shifting the symmetry of the VCO clock effectively shifts the relative position of the DLYD DATA pulse within the decode window. This powerful capability easily facilitates defect mapping, automatic calibration, window margin testing, error recovery, and systematic error cancellation. For enhanced disk drive testability and error recovery, decode window control is provided via a µP port (WSL, WSD, $\overline{WS0}$, $\overline{WS1}$) as

described in Table 3. In applications not utilizing this feature, WSL should be connected to ground, while WSD, $\overline{WS0}$, and $\overline{WS1}$ can be left open.

Window shifts in the range of ±1.5% to ±7.5% of TORC are easily programmed by latching the appropriate control word into the Window Shift Register with the WSL pin. Shifts in the positive or negative directions result in early or late decode windows respectively, as depicted in Figure 3. Additionally, for small systematic error cancellation, a resistor, R, connected from either RS (Early) or RF (Late) to ground will provide analog control over the decode window. The magnitude of this shift, TSA is determined by:

$$TSA = 0.125\ TORC\left(1 - \frac{680 + R}{1180 + R}\right)$$

where: R is in ohms

Pins RF and RS are intended to be used as a trim and should be restricted to ±1.5% window shifts. They can be used in conjunction with the digital control port.

In Non-Read Modes, the PLL is locked to the crystal reference oscillator. This forces the VCO to run at a frequency which is very close to that required for tracking actual data and thus minimizes the associated frequency step during acquisition. When the reference input to the PLL is switched, the VCO is stopped momentarily, then restarted in an accurate phase alignment with the next PLL reference input pulse, and the VCO clock divider is reset. By minimizing the phase alignment in this manner (phase error ≤ 0.5 rads), the acquisition time is substantially reduced.

The SSI 32D5322 provides two sync modes for controlling the PLL locking sequence; Soft Sector and Hard Sector.

SOFT SECTOR MODE

The Soft Sector Mode activates the Preamble Search and Address Mark detection circuitry. As depicted in Figure 4, when RG transitions high, the counter is reset and the SSI 32D5322 requires 10 high to low transitions (Preamble '1' bits) before switching the reference input to the PLL, 48 high to low transitions before switching the Read Reference Clock to the VCO clock divided by two and activating the Address Mark Detect circuitry; then it must detect the Address Mark prior to 80 high to low transitions in order to enter the Read Mode. This sequence repeats after 95 input '1' bits until the read mode is successfully entered or until RG is cancelled.

When RG transitions high, the following PLL locking sequence begins:

a) PREAMBLE SEARCH:

The 3T detect circuitry initiates the PLL locking sequence once it has detected 10 consecutive '100' bit groups from the 3T preamble field. The 3T detect timing is set by the sum of the 1/4 cell delay and the retriggerable one-shot delay. The 1/4 cell timing capacitor is included on-chip and its timing is externally set by resistor RR. The retriggerable one-shot timing is externally set by resistor Rd and capacitor Cd. The sum of their delays is set to 3.5 bit cell times. Therefore, a continuous stream of input pulses with a 3T bit cell time pulse rate keeps the one-shot reset, and a 4T or longer bit cell time input period allows the one-shot to time out producing a 4T detect pulse. The 4T detect pulse resets the Input Counter and the search is started over.

b) PLL ACQUISITION:

Once 10 consecutive '100' bit groups are detected, the reference input to the PLL is switched from the crystal reference oscillator to the DLYD DATA, the VCO is phase reset to the next DLYD DATA pulse, and PLL acquisition begins. When an additional 38 '100' bit groups are detected, the Read Reference Clock output (RRC) is switched to the VCO clock divided by 2, the 4T Detect circuitry is inhibited, and the Address Mark Detection circuitry is enabled. If a 4T detect pulse occurs before 48 Preamble '1' bits are detected, then the PLL is locked back to the crystal reference oscillator, the RRC output is switched to the crystal reference oscillator divided by 2, the Input Counter reset, and the sequence is restarted. No short duration glitches will occur at the RRC output during this switching.

c) **ADDRESS MARK DETECTION:**

The circuit searches for the occurrence of the $5EAx_{16}$ Address Mark. If an Address Mark is detected prior to the Input Counter reaching count 80, the correct phase of the RRC is ensured by resetting the n/2 divider, the $\overline{AMD}$ output is latched low, the PLL training sequence is terminated, and the Read Mode is entered allowing the data field to be read. If the Input Counter reaches count 80 before the Address Mark is detected, the PLL is locked back to the crystal reference oscillator, the RRC output is switched to the crystal reference oscillator divided by 2, and the PLL training sequence is restarted when the Input Counter reaches count 96. Figure 5 depicts the Address Mark detection sequence.

HARD SECTOR MODE

In the Hard Sector mode (SOFT/$\overline{HARD}$ = 0) the SSI 32D5321 utilizes a 4T (1000) Preamble Field and disables the Preamble Search and Address Mark detection circuitry. It allows the PLL to be controlled directly by RG for Hard Sector format operation. With the absence of an Address Mark, the 4T Preamble Field is utilized to properly set the bit cell alignment boundaries for proper decoding.

When RG transitions high, as depicted in Figure 6, reference input to the PLL is switched from the crystal reference oscillator to DLYD DATA, the VCO is phase reset to the next DLYD DATA pulse, and the PLL acquisition begins. When 32 '1' Preamble bits are detected, the RRC output is switched to the VCO clock divided by 2, and the Read Mode is entered allowing the data field to be read.

In the Hard Sector mode, the NRZ output is inverted and will remain low until the data field is read, as shown in Figure 7. Since the Preamble Search circuitry is not utilized, the external one-shot timing components (Cd, Rd) are not required and the SDS pin can be left open.

WRITE OPERATION

In the Write Mode the SSI 32D5321 converts NRZ data from the controller into 2, 7 RLL formatted data for storage onto the disk. The SSI 32D5321 can operate with a soft or hard sectored disk drive. In the Soft Sector Mode, (SOFT/$\overline{HARD}$ = 1) the device generates a 3T Preamble Field and can insert a N7V Address Mark. The N7V Address Mark is a valid 2, 7 RLL pattern which is not contained in the code set. In the Hard Sector Mode, (SOFT/$\overline{HARD}$ = 0) the device generates a 4T Preamble Field and no Address Mark. Serial NRZ data is clocked into the SSI 32D5321 and latched on defined cell boundaries. The NRZ input data must be synchronous with the rising edges of the WCLK input. In a SCSI or ST506 operation, WCLK is connected directly to the RRC output.

SOFT SECTOR MODE

In the Soft Sector Mode, when WRITE GATE (WG), transitions high and the NRZ input is held low, the SSI 32D5321 automatically generates the 3T (100) Preamble Field at the WRITE DATA ($\overline{WD}$), output. The 3T Preamble Field will continue to be generated until the first low to high transition on the NRZ line. As shown in Figure 8, the first low to high transition occurs with the second bit '1' of the 5_{16} (0101) in the $5EAx_{16}$ Address Mark generation pattern. To generate the Address Mark, the SSI 32D5321 automatically changes the '1' in the eleventh position (see note 3) of the 2, 7 RLL encoded sequence, to a '0'. This generates a pattern of seven zero's followed by two zero's. This unique pattern satisfies the 2, 7 RLL constraints, but will never occur during a normal encoding sequence. The x_{16} of the $5EAx_{16}$ Address Mark generation pattern can be selected, a 'C_{16}' (1100) was utilized in this example.

HARD SECTOR MODE

In the Hard Sector Mode, when WG goes high and the NRZ input is held low, the SSI 32D5321 automatically generates the 4T (1000) Preamble Field at the WRITE DATA, $\overline{WD}$, output. Note that in the Hard Sector mode, the NRZ input is inverted, therefore a constant low is equivalent to an '11...' input which generates the 4T '1000...' Preamble Field. The 4T Preamble Field will be generated between the time WG goes high and the first low to high transition on the NRZ line. The 32D5321 requires a minimum of 32 4T (1000) bit groups prior to the data field.

PIN DESCRIPTION

INPUT PINS

NAME	TYPE	DESCRIPTION
$\overline{RD}$	I	READ DATA: Encoded Read Data from the disk drive read channel, active low.
RG	I	READ GATE: Selects the PLL reference input and initiates the PLL synchronization sequence. A high level selects the $\overline{RD}$ input and enables the Read Mode/ Address Mark Detection sequences. A low level selects the crystal reference oscillator. Pin RG has an internal resistor pull-up.
WG	I	WRITE GATE: Enables the write mode. Pin WG has an internal resistor pull-up.
WSL	I	WINDOW SYMMETRY LATCH: Used to latch the input window symmetry control bits WSD, $\overline{WS0}$ and $\overline{WS1}$ into the internal DAC. An active high level latches the input bits. Pin WSL has an internal resistor pull-up.
WSD	I	WINDOW SYMMETRY DIRECTION: Controls the direction of the optional window symmetry shift. Pin WSD has an internal resistor pull-up.
$\overline{WS0}$	I	WINDOW SYMMETRY CONTROL BIT: A low level introduces a window shift of 1.5% TORC (Read Reference Clock Period) in the direction established by WSD. Pin $\overline{WS0}$ has an internal resistor pull-up.
$\overline{WS1}$	I	WINDOW SYMMETRY CONTROL BIT: A low level introduces a window shift of 6% TORC (Read Reference Clock Period) in the direction established by WSD. A low level at both $\overline{WS0}$ and $\overline{WS1}$ will produce the sum of the two window shifts. Pin $\overline{WS1}$ has an internal resistor pull-up.
SOFT/$\overline{HARD}$	I	SOFT/$\overline{HARD}$ SECTOR: Selects the address mark and the Preamble field patterns. A high level (Soft Sector) selects a 3T Preamble Field pattern and a non-violating 2, 7 address mark, N7V. A low level (Hard Sector) selects a 4T Preamble Field pattern and disables the address mark circuitry. Pin SOFT/$\overline{HARD}$ has an internal resistor pull-up.
WCLK	I	WRITE CLOCK: Write Clock input. Must be synchronous with the Write Data input on the NRZ Data Port. For small cable delays, WCLK may be connected directly to pin RRC (Read/Reference Clock).
EPD	I	ENABLE PHASE DETECTOR: A low level (Coast Mode) disables the phase detector and allows the VCO to coast. Pin EPD has an internal resistor pull up.

BIDIRECTIONAL PINS

NRZ	I/O	NRZ DATA PORT: Read Data output when RG is high and Write Data input when WG is high. In the idle mode NRZ is in a high impedance state.

PIN DESCRIPTION (Cont.)

OUTPUT PINS

NAME	TYPE	DESCRIPTION
$\overline{WD}$	O	WRITE DATA: Encoded write data output, active low.
RRC	O	READ/REFERENCE CLOCK: A multiplexed clock source used by the controller. In the read mode, this clock is the VCO frequency divided by two (1/TORC) and in the write mode it is the crystal reference frequency divided by two (1/TORO). No short clock pulses are generated during a mode change.
$\overline{AMD}$	O	ADDRESS MARK DETECT: In the soft sector Read Mode, a latched low level output indicates that an address mark has been detected. In non-Read modes $\overline{AMD}$ is configured as a high impedance output.
$\overline{SDO}$	O	SYNC DETECT OUTPUT: An active low output that indicates successful detection of the 3T Preamble sync field. THE $\overline{SDO}$ pin is not a TTL level signal.

ANALOG PINS

IREF	I	TIMING PROGRAM PIN: The VCO center frequency and the 1/4 Cell Delay are a function of the current source into pin IREF. The current is set by an external resistor, RR, connected from IREF to VPA.
XTAL1, XTAL2	I	CRYSTAL OSCILLATOR CONNECTIONS: If a crystal oscillator is not desired, XTAL1 maybe driven by a TTL source with XTAL2 open. The frequency must be at twice the data rate.
PD OUT	O	PHASE DETECTOR OUTPUT: Drives the Loop Filter input.
VCO IN	I	VCO CONTROL INPUT: Driven by the Loop Filter output.
SDS	I	SYNC DETECT SET: Used to program the sync detect retriggerable one-shot timing with an external R-C network. Connect the capacitor, Cd, to VPA and the resistor, Rd, to AGND.
RF, RS	I	WINDOW SYMMETRY ADJUST PINS: Provides analog control over the decode window symmetry; typically used to null out any window symmetry offset. A resistor connected from either RF or RS to AGND will provide magnitude and direction control. They can be used in conjunction with the digital control port WSD, $\overline{WS0}$, $\overline{WS1}$.

POWER

DGND, AGND	I	DIGITAL AND ANALOG GROUND
VPA	I	ANALOG +5V
VPD	I	DIGITAL +5V

NRZ	2, 7 RLL
10	0100
11	1000
000	000100
010	100100
011	001000
0010	00100100
0011	00001000

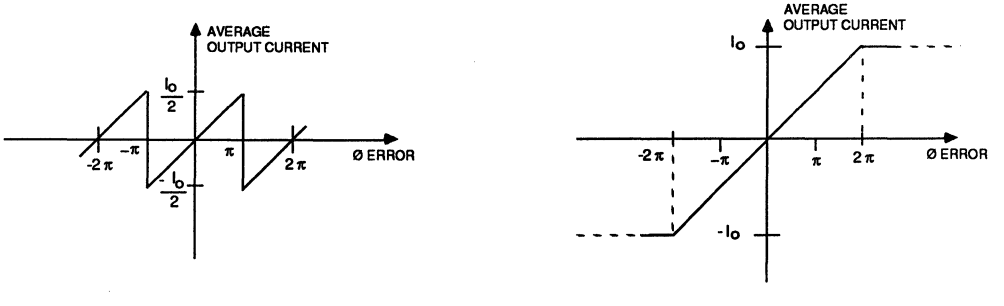
TABLE 1: 2, 7 RLL Code Set

WG	RG	MODE
0	0	IDLE
0	1	READ
1	0	WRITE
1	1	ILLEGAL

TABLE 2: Mode Control

Ts, NOMINAL WINDOW SHIFT	WSD	$\overline{WS1}$	$\overline{WS0}$
+TS3	0	0	0
+TS2	0	0	1
+TS1	0	1	0
0	0	1	1
-TS3	1	0	0
-TS2	1	0	1
-TS1	1	1	0
0	1	1	1

TABLE 3 : Decode Window Symmetry Control



a) HARMONIC MODE

b) NON-HARMONIC MODE

Note 1) Io is the magnitude of the charge pump current.
2) Phase error is relative to the VCO period

FIGURE 1: Phase Detector Transfer Function

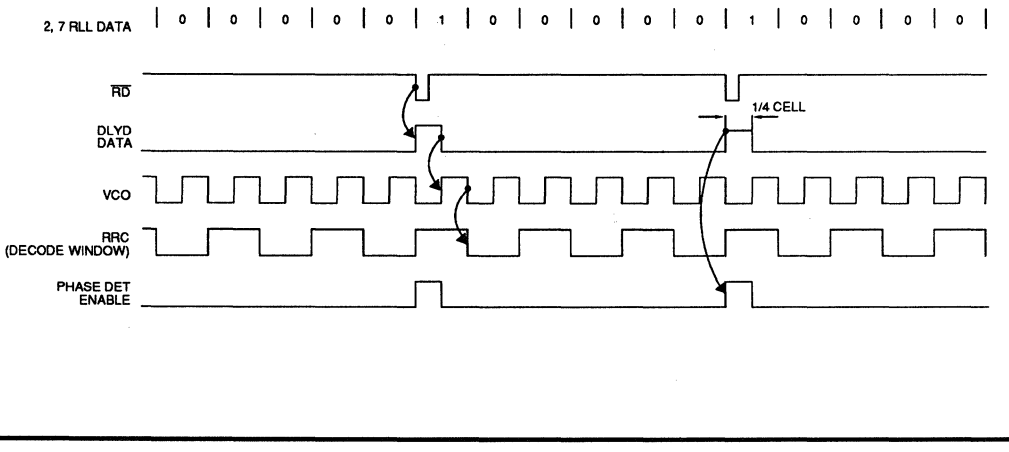


FIGURE 2: Data Synchronization Waveform Diagram

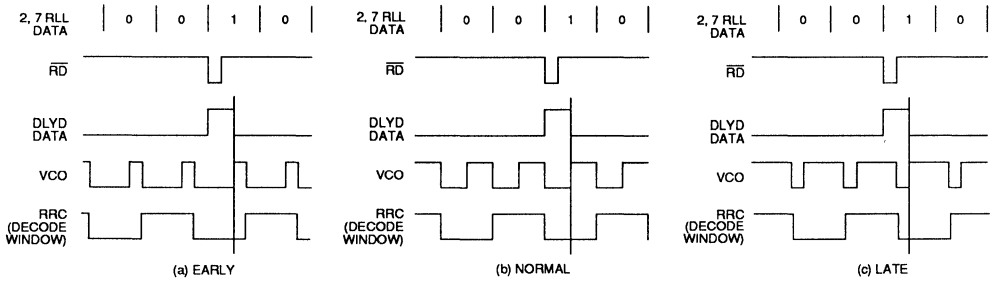
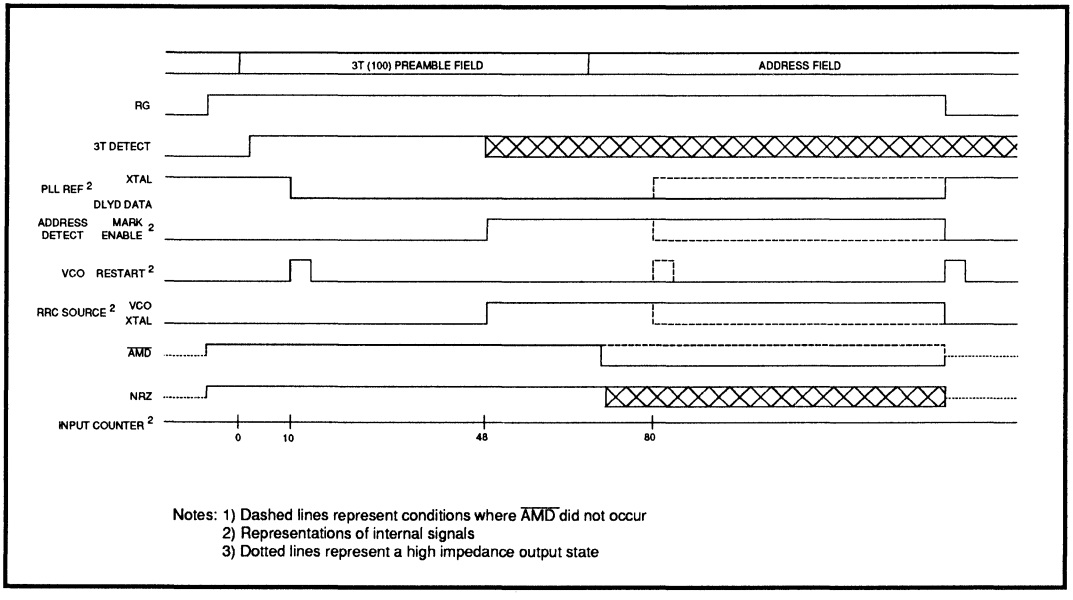


FIGURE 3: Decode Window



Notes: 1) Dashed lines represent conditions where $\overline{AMD}$ did not occur
2) Representations of internal signals
3) Dotted lines represent a high impedance output state

FIGURE 4: Soft Sector Mode Timing Diagram

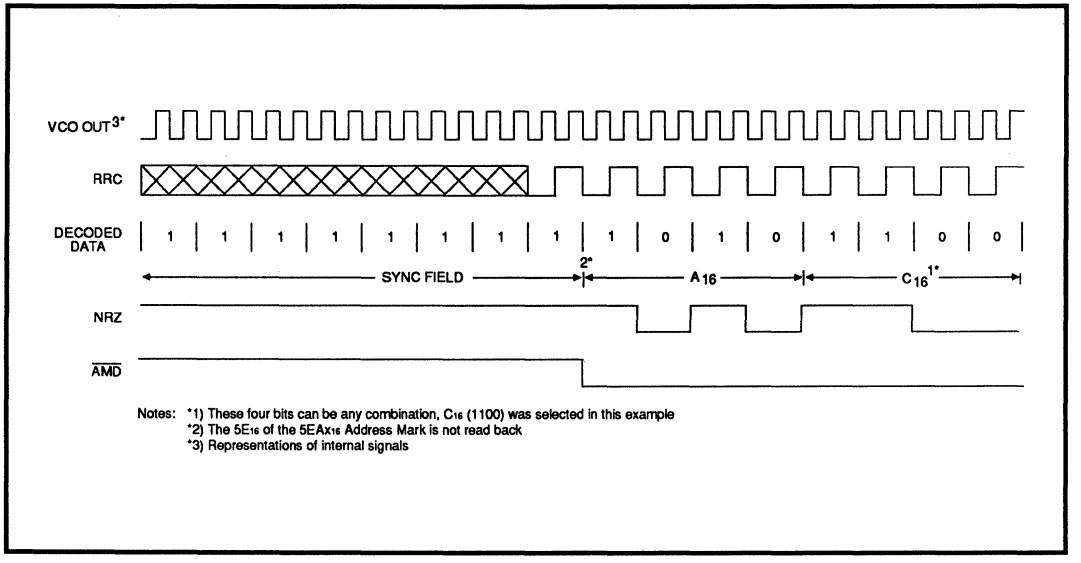


FIGURE 5: Address Mark Detection and NRZ Output Waveform

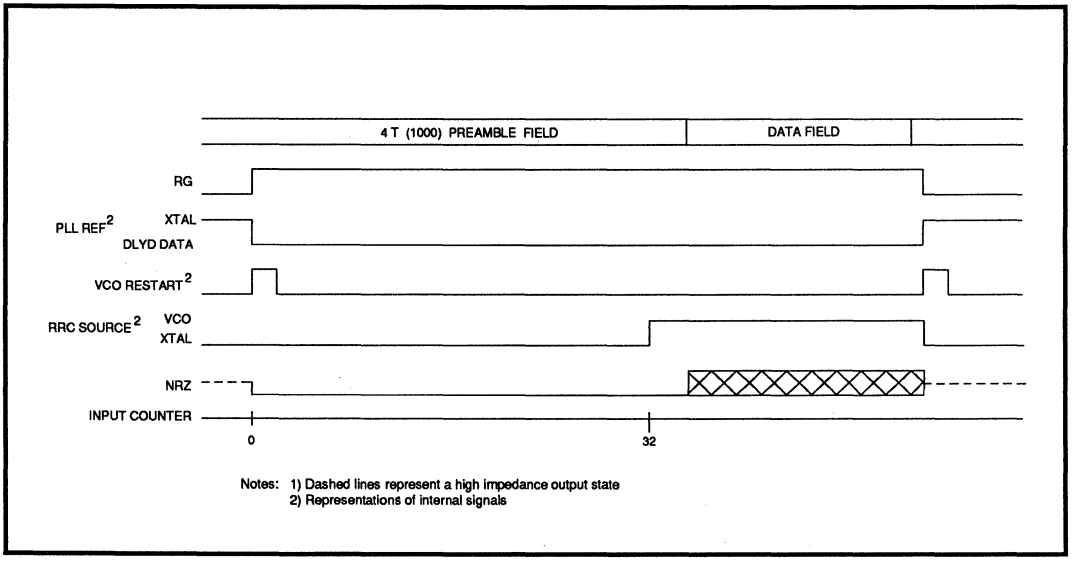


FIGURE 6: Hard Sector Mode Timing Diagram

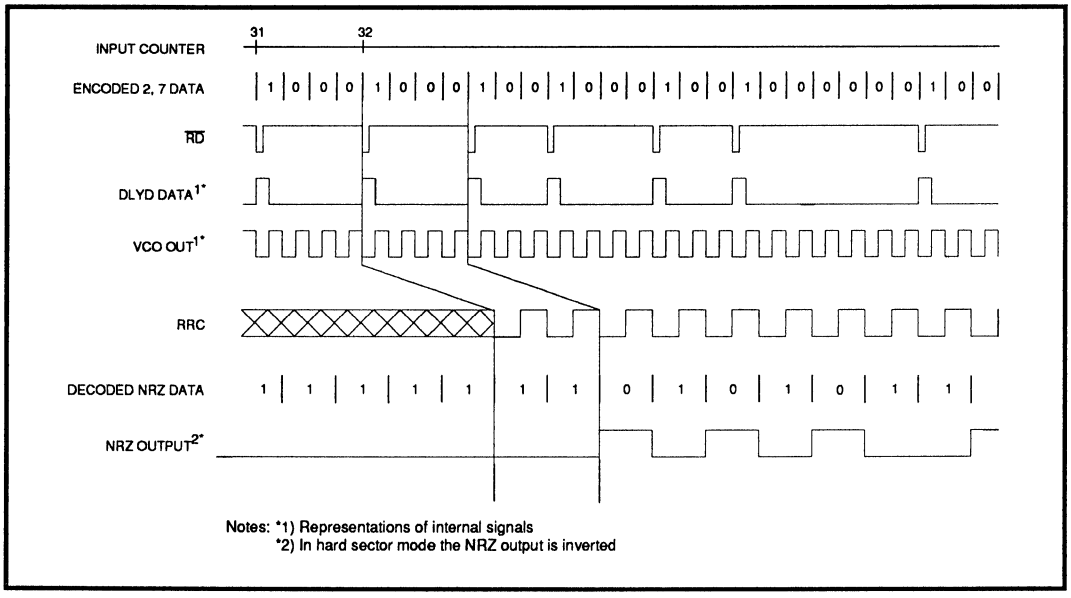


FIGURE 7: Hard Sector Mode Decode Timing

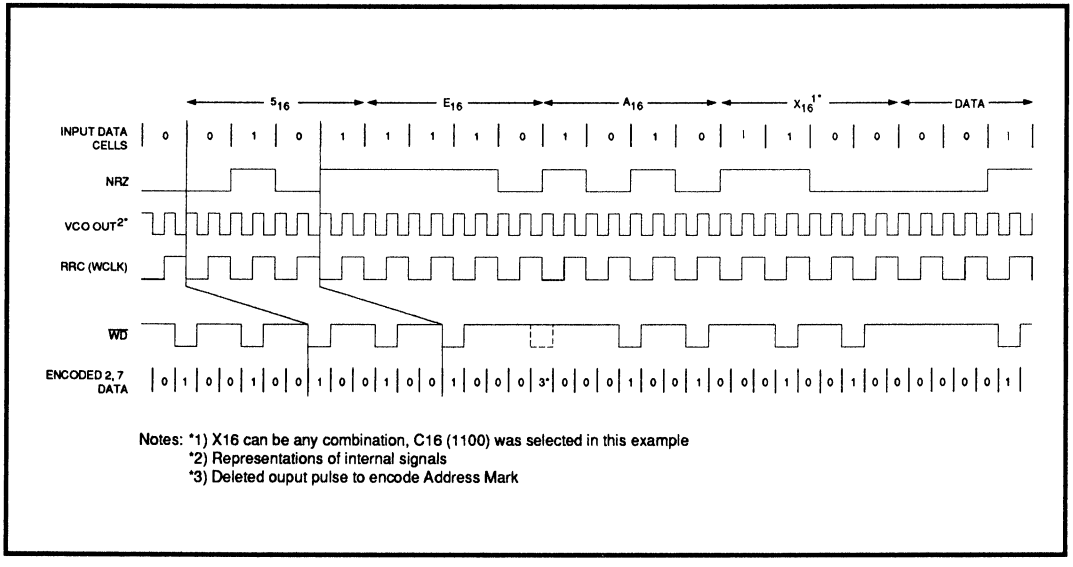


FIGURE 8: Write Address Mark Generation

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATINGS	UNIT
Storage Temperature	-65 to +150	°C
Ambient Operating Temperature, Ta	0 to +70	°C
Junction Operating Temperature	0 to +130	°C
Supply Voltage, VCC	-0.5 to 7	Vdc
Voltage Applied to Logic inputs	-0.5 to VCC +0.5	Vdc
Maximum Power Dissipation	950	mW

DC ELECTRICAL CHARACTERISTICS - unless otherwise specified, 4.75V < VCC < 5.25V, Ta = 0°C to 70°C, 7.5 MHz < 1/TORC < 10 MHz, 15 MHz < 1/TVCO < 20 MHz

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VIH, High Level Input Voltage		2.0			V
VIL, Low Level Input Voltage				0.8	V
IIH, High Level Input Current	VIH = 2.7V			20	µA
IIL, Low Level Input Current	VIL = 0.4V			-0.36	mA
VOH, High Level Output Voltage	IOH = -400 µA	2.7			V
VOL, Low Level Output Voltage	IOL = 4 mA			0.5	V
ICC, Power Supply Current	All outputs open			165	mA

DYNAMIC CHARACTERISTICS AND TIMING

READ MODE (See Figure 9)

TRD, Read Data Pulse Width		20		TORC-40	ns
TFRD, Read Data Fall Time	2.0V to 0.8V, CL ≤ 15 pF			15	ns
TRRC, Read Clock Rise Time	0.8V to 2.0V, CL ≤ 15 pF			8	ns
TFRC, Read Clock Fall Time	2.0V to 0.8V, CL ≤ 15 pF			5	ns
TPNRZ, NRZ (out) Propagation Delay		-15		15	ns
TPAMD, $\overline{AMD}$ Propagation Delay		-15		15	ns

READ MODE (Cont.)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Decode Window Centering Accuracy				± (0.01 TORC + 2)	ns
Decode Window		(TORC/2) -2			ns

WRITE MODE (See Figure 10)

TWD, Write Data Pulse Width	CL ≤15 pF	(TORO/2) -12		(TORO/2) +12	ns
TFWD, Write Data Fall Time	2.0V to 0.8V, CL ≤ 15 pF			8	ns
TOWC Write Data Clock Repetition Period		TORO -12		TORO +12	ns
TRWC Write Data Clock Rise Time	0.8V to 2.0V			10	ns
TFWC Write Data Clock Fall Time	2.0V to 0.8V			8	ns
TSNRZ, NRZ (in) Set Up Time		20			ns
THNRZ, NRZ (in) Hold Time		7			ns

DATA SYNCHRONIZATION (VCC = 5.0V)

TVCO	VCO Center Frequency Period	VCO_IN = 2.7V TO = 1.23E - 11 (RR +0.5) $\overline{WS0}$ = $\overline{WS1}$ = 1	0.83 TO		1.17 TO	sec
	VCO Frequency Dynamic Range	1.0V ≤ VCO_IN ≤ VCC -0.6V $\overline{WS0}$ = $\overline{WS1}$ = 1	±24		±40	%
KVCO	VCO Control Gain	ωo = 2π / TVCO; $\overline{WS0}$ = $\overline{WS1}$ = 1	0.14 ωo		0.235 ωo	rad/s V
		1.0V ≤ VCO_IN ≤ VCC -0.6V; $\overline{WS0}$ = $\overline{WS1}$ ≠ 1	0.104 ωo		0.235 ωo	rad/s V
KD	Phase Detector Gain	KD = 309 / (RR + 0.5) RR (kΩ); KD (μA/rad)	0.83KD		1.17 KD	A/rad
	KVCO x KD Product Accuracy		-28		+28	%
	VCO Phase Restart Error		-0.5		+0.5	rad
1/4 Cell + Retriggerable One-Shot Detect Stability			-4		+4	%
1/4 Cell + Retriggerable One-Shot Delay*		TD 6.14(RR +0.5) + 0.172 Rd (Cd +11.5) RR (kΩ) Rd (kΩ) Cd = 68 pF to 100 pF	0.89 TD		1.11 TD	ns
Note: * = Excludes External Capacitor and Resistor Tolerances						

DATA SYNCHRONIZATION (Cont.)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TS1	Decode Window Time Shift Magnitude	TS1 = 0.015 TORC	0.85 TS1		1.15 TS1	sec
TS2	Decode Window Time Shift Magnitude	TS2 = 0.06 TORC	0.90 TS2		1.1 TS2	sec
TS3	Decode Window Time Shift Magnitude	TS3 = 0.075 TORC	0.90 TS3		1.1 TS3	sec
TSA	Decode Window Time Shift Magnitude	$TSA = 0.125\ TORC\left(1 - \frac{680 + R}{1180 + R}\right)$ with: R in ohms	0.65 TSA		1.35 TSA	sec

CONTROL CHARACTERISTICS (See Figure 11)

TSWS, $\overline{WS0}$, $\overline{WS1}$, WSD Set Up Time		50			ns
THWS, $\overline{WS0}$, $\overline{WS1}$, WSD Hold Time		0			ns
RG, WG, SOFT/$\overline{HARD}$ Time Delay				100	ns

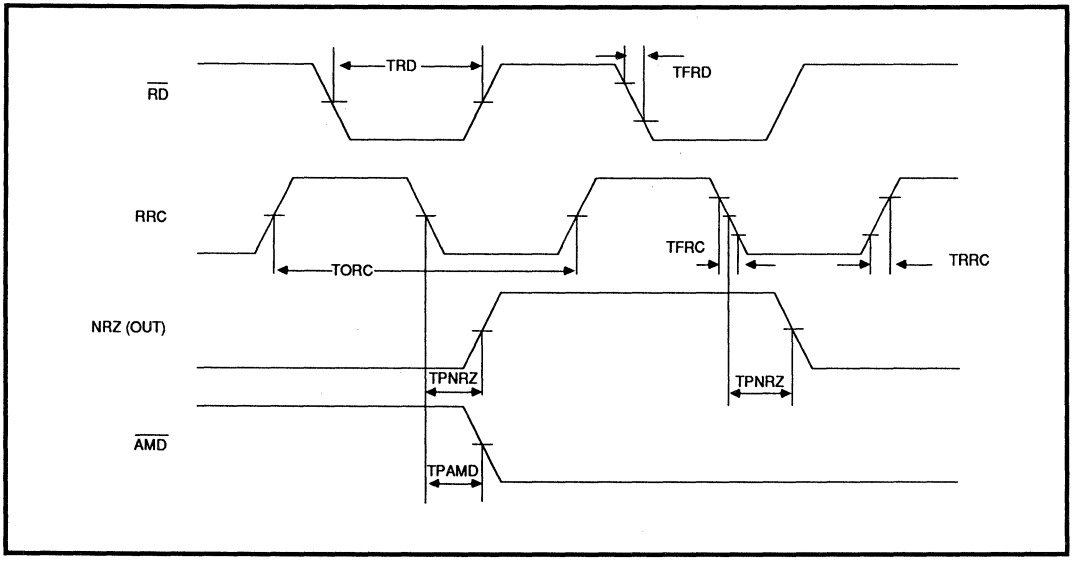


FIGURE 9: Read Timing

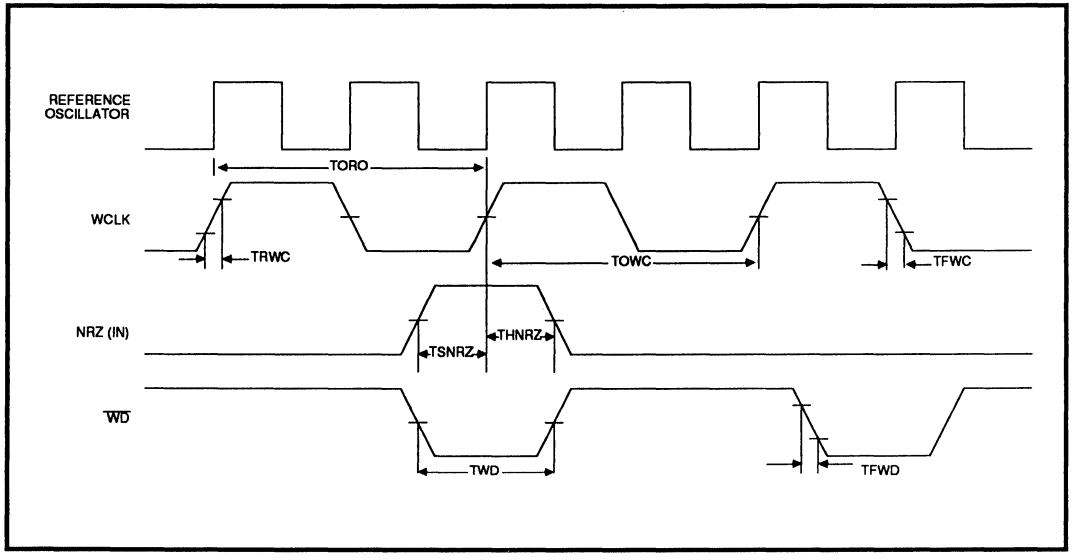


FIGURE 10: Write Timing

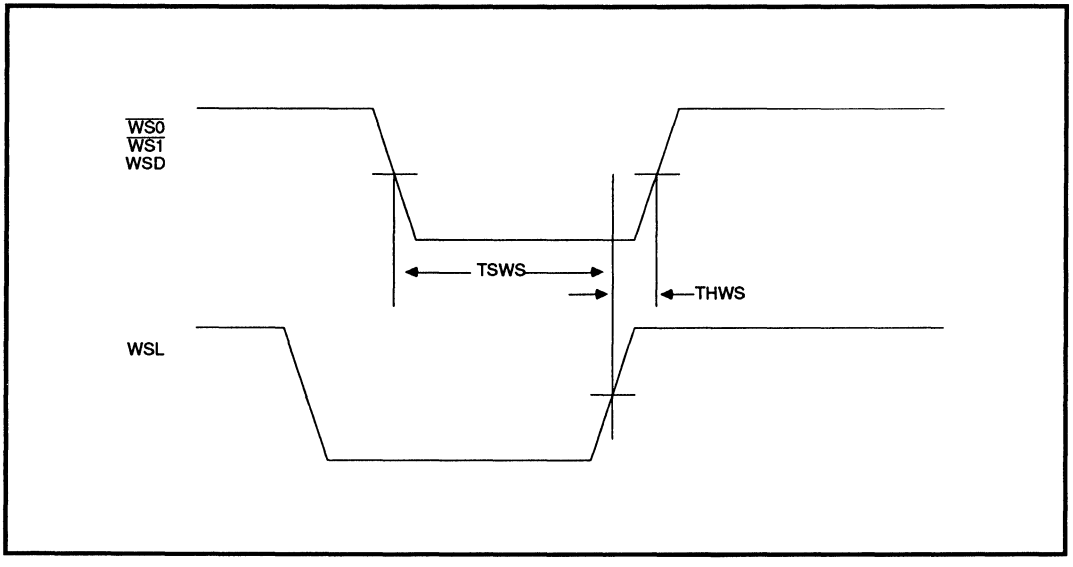
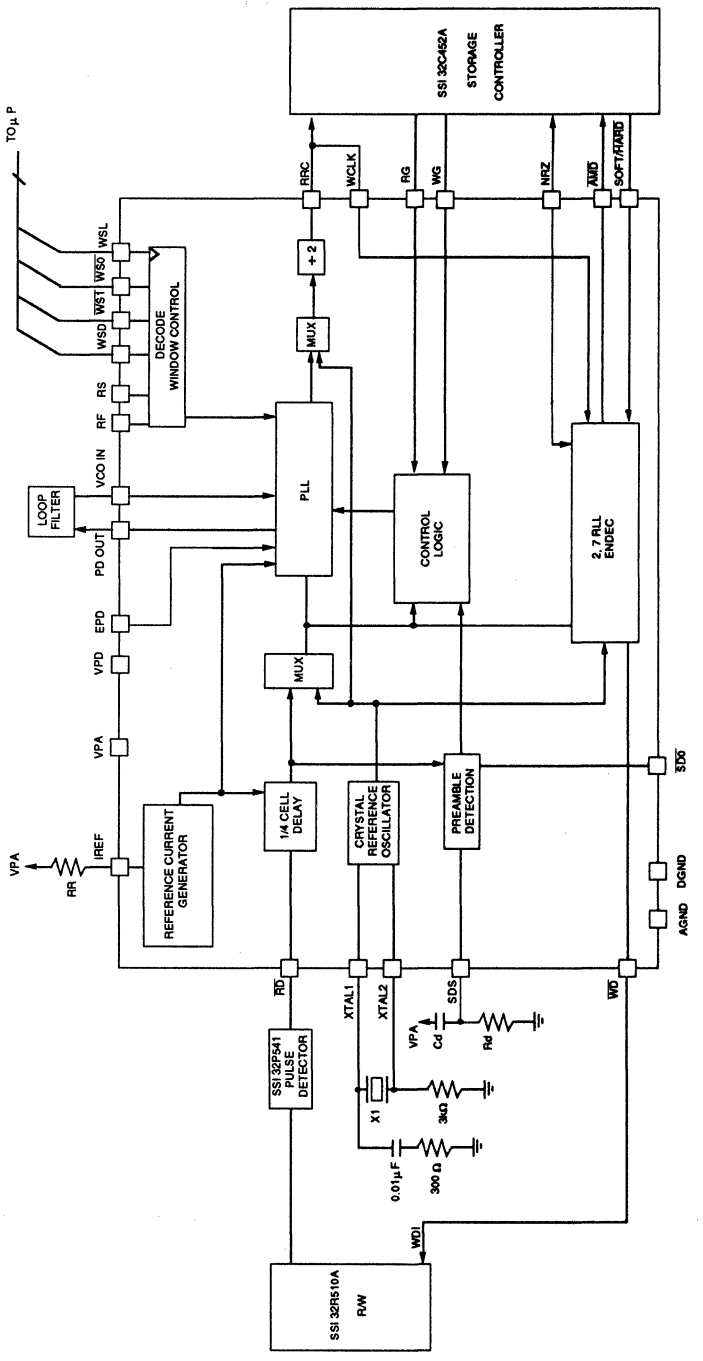


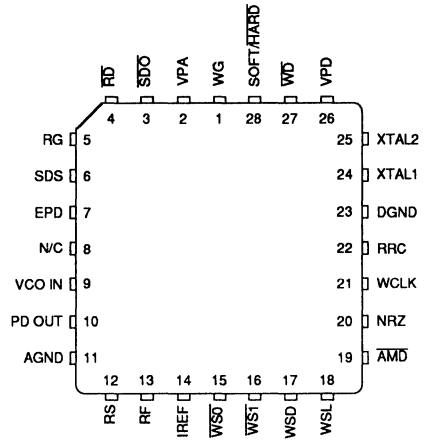
FIGURE 11: Control Timing



TYPICAL SSI 532 APPLICATION

PACKAGE PIN DESIGNATIONS

(Top View)



28-Pin PLCC

4

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32D5321 28-Pin PLCC	32D5321 - CH	32D5321 - CH

Silicon Systems, Inc. 14351 Myford Road, Tustin, CA 92680, (714) 731-7110, FAX (714) 573-6914

Notes:

silicon systems®
A TDK Group Company

SSI 32D5322
Data Synchronizer/ 2, 7 RLL ENDEC

Preliminary Data

November 1991

DESCRIPTION

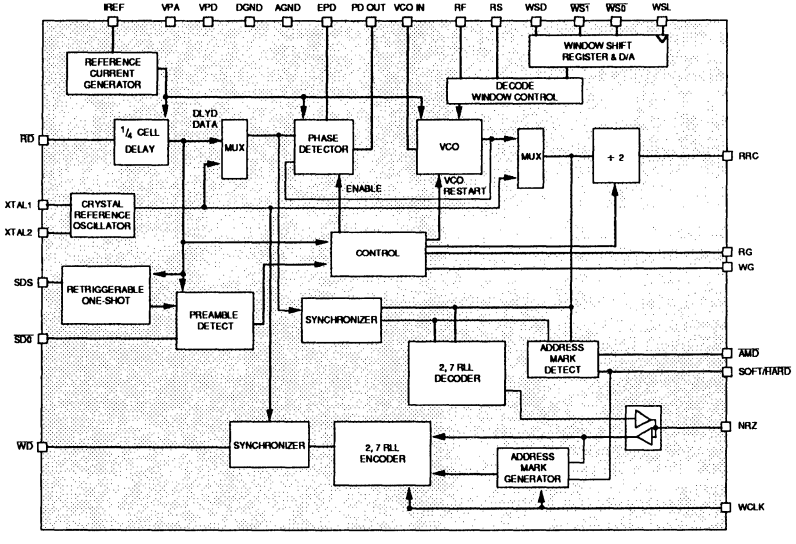
The SSI 32D5322 Data Synchronizer/2, 7 RLL ENDEC provides data recovery and data encoding for storage systems which employ a 2, 7 RLL encoding format. Data synchronization is performed with a fully integrated high performance PLL. A zero phase restart technique is used to minimize PLL acquisition time. The SSI 32D5322 has been optimized for operation as a companion device to the SSI 32C452 and the AIC 010 controllers. The VCO frequency setting elements are incorporated within the SSI 32D5322 for enhanced performance and reduced board space. Data rate is established with a single external programming resistor. The SSI 32D5322 utilizes an advanced bipolar process technology which affords precise decode window control without the requirement of an accurate 1/ 4 cell delay or external devices. To enhance disk drive testability, decode window symmetry control is available through a digital µP port and/or two analog pins. This feature can facilitate defect mapping, automatic calibration, systematic error cancellation, window margin testing and error recovery. The SSI 32D5322 requires a single +5V power supply and is available in a 28-pin PLCC package.

FEATURES

- **Data Synchronizer and 2, 7 RLL ENDEC**
- **7.5 to 15 Mbit/s Operation Programmed with a Single External Resistor or Current Source**
- **Optimized for Operation with the SSI 32C452 and AIC 010 Controllers**
- **Programmable Decode Window Symmetry via a µP Port and/or Analog Pins**
- **Fast Acquisition Phase Locked Loop**
  - **Zero Phase Restart Technique**
- **Fully Integrated Data Separator**
  - **No External Delay Lines or Active Devices Required**
- **Crystal Controlled Reference Oscillator**
- **Hard/Soft Sector Operation**
- **+5V Operation**
- **28-Pin PLCC Package**
- **ESDI (Hard Sector) Compatible**

4

BLOCK DIAGRAM



OPERATION

The SSI 32D5322 is designed to perform data recovery and data encoding in rotating memory systems which utilize a 2, 7 RLL encoding format. In the Read Mode the SSI 32D5322 performs Data Synchronization, Sync Field Search and Detect, Address Mark Detect and Data Decoding. In the Write Mode, the SSI 32D5322 converts NRZ data into the 2,7 RLL format described in Table 1, it generates the Preamble Field, and inserts Address Marks as requested. The interface electronics and architecture of the SSI 32D5322 have been optimized for use as a companion device to the SSI 32C452 or AIC 010 controllers.

The SSI 32D5322 can operate with data rates ranging from 7.5 to 15 Mbit/s. This data rate is established by a single 1% external resistor, RR, connected from pin IREF to VPA. This resistor establishes a reference current which sets the VCO center frequency, the phase detector gain, and the 1/4 cell delay. The value of this resistor is given by:

$$RR = \frac{43.86}{DR} - 1.2(k\Omega)$$

where: DR = Data Rate in Mbit/s.
[* Note: This equation differs from 32D5321 RR equation]

An internal crystal reference oscillator, operating at twice the data rate, generates the standby reference for the PLL. A series resonant crystal between XTAL1 and XTAL2 should be selected at twice the Data Rate. If a crystal oscillator is not desired, then an external TTL compatible reference may be applied to XTAL1, leaving XTAL2 open.

The SSI 32D5322 employs a Dual Mode Phase Detector; Harmonic in the Read Mode and Non-Harmonic in Write and Idle Modes. In the Read Mode the Harmonic Phase Detector updates the PLL with each occurrence of a DLYD DATA pulse. In the Write and Idle Modes the Non-Harmonic Phase Detector is continuously enabled, thus maintaining both phase and frequency lock. By acquiring both phase and frequency lock to the crystal reference oscillator and utilizing a zero phase restart technique, false lock to DLYD DATA is eliminated.

The phase detector incorporates a charge pump in order to drive the loop filter directly. The polarity and width of the output current pulses correspond to the direction and magnitude of the phase error. Figure 1 depicts the average output current as a function of the input phase error (relative to the VCO period).

The READ GATE (RG), and WRITE GATE (WG), inputs control the device mode as described in Table 2. RG is an asynchronous input and may be initiated or terminated at any position on the disk. WG is also an asynchronous input, but should not be terminated prior to the last output Write Data pulse.

READ OPERATION

The Data Synchronizer utilizes a fully integrated fast acquisition PLL to accurately develop the decode window. Read Gate, RG, initiates the PLL locking sequence and selects the PLL reference input; a high level (Read Mode) selects the $\overline{RD}$ input and a low level selects the crystal reference oscillator.

In the Read Mode the rising edge of DLYD DATA enables the Phase Detector while the falling edge is phase compared to the rising edge of the VCO. As depicted in Figure 2, DLYD DATA is a 1/4 cell wide (TVCO/2) pulse whose leading edge is defined by the leading edge of $\overline{RD}$. An accurate and symmetrical decode window is developed from the VCO clock. The decode window is generated from the falling edges of the VCO clock. By utilizing a fully integrated symmetrical VCO running at twice the data rate, the decode window is insured to be accurate and centered symmetrically about the falling edges of DLYD DATA. The accuracy of the 1/4 cell delay only affects the retrace angle of the phase detector and does not influence the accuracy of the decode window.

Shifting the symmetry of the VCO clock effectively shifts the relative position of the DLYD DATA pulse within the decode window. This powerful capability easily facilitates defect mapping, automatic calibration, window margin testing, error recovery, and systematic error cancellation. For enhanced disk drive testability and error recovery, decode window control is provided via a µP port (WSL, WSD, $\overline{WS0}$, $\overline{WS1}$) as described in Table 3. In applications not utilizing this feature, WSL should be connected to ground, while WSD, $\overline{WS0}$, and $\overline{WS1}$ can be left open.

Window shifts in the range of ±1.5% to ±7.5% of TORC are easily programmed by latching the appropriate control word into the Window Shift Register with the WSL pin. Shifts in the positive or negative directions result in early or late decode windows respectively, as depicted in Figure 3. Additionally, for small systematic error cancellation, a resistor, R, connected from either RS (Early) or RF (Late) to ground will provide analog control over the decode window. The magnitude of this shift, TSA is determined by:

$$TSA = 0.125\ TORC\left(1 - \frac{680 + R}{1180 + R}\right)$$

where: R is in ohms

Pins RF and RS are intended to be used as a trim and should be restricted to ±1.5% window shifts. They can be used in conjunction with the digital control port.

In Non-Read Modes, the PLL is locked to the crystal reference oscillator. This forces the VCO to run at a frequency which is very close to that required for tracking actual data and thus minimizes the associated frequency step during acquisition. When the reference input to the PLL is switched, the VCO is stopped momentarily, then restarted in an accurate phase alignment with the next PLL reference input pulse, and the VCO clock divider is reset. By minimizing the phase alignment in this manner (phase error ≤ 0.5 rads), the acquisition time is substantially reduced.

The SSI 32D5322 provides two sync modes for controlling the PLL locking sequence; Soft Sector and Hard Sector.

SOFT SECTOR MODE

The Soft Sector Mode activates the Preamble Search and Address Mark detection circuitry. As depicted in Figure 4, when RG transitions high, the counter is reset and the SSI 32D5322 requires 10 high to low transitions (Preamble '1' bits) before switching the reference input to the PLL, 48 high to low transitions before switching the Read Reference Clock to the VCO clock divided by two and activating the Address Mark Detect circuitry; then it must detect the Address Mark prior to 80 high to low transitions in order to enter the Read Mode. This sequence repeats after 95 input '1' bits until the read mode is successfully entered or until RG is cancelled.

When RG transitions high, the following PLL locking sequence begins:

a) PREAMBLE SEARCH:

The 3T detect circuitry initiates the PLL locking sequence once it has detected 10 consecutive '100' bit groups from the 3T preamble field. The 3T detect timing is set by the sum of the 1/4 cell delay and the retriggerable one-shot delay. The 1/4 cell timing capacitor is included on-chip and its timing is externally set by resistor RR. The retriggerable one-shot timing is externally set by resistor Rd and capacitor Cd. The sum of their delays is set to 3.5 bit cell times. Therefore, a continuous stream of input pulses with a 3T bit cell time pulse rate keeps the one-shot reset, and a 4T or longer bit cell time input period allows the one-shot to time out producing a 4T detect pulse. The 4T detect pulse resets the Input Counter and the search is started over.

b) PLL ACQUISITION:

Once 10 consecutive '100' bit groups are detected, the reference input to the PLL is switched from the crystal reference oscillator to the DLYD DATA, the VCO is phase reset to the next DLYD DATA pulse, and PLL acquisition begins. When an additional 38 '100' bit groups are detected, the Read Reference Clock output (RRC) is switched to the VCO clock divided by 2, the 4T Detect circuitry is inhibited, and the Address Mark Detection circuitry is enabled. If a 4T detect pulse occurs before 48 Preamble '1' bits are detected, then the PLL is locked back to the crystal reference oscillator, the RRC output is switched to the crystal reference oscillator divided by 2, the Input Counter reset, and the sequence is restarted. No short duration glitches will occur at the RRC output during this switching.

c) ADDRESS MARK DETECTION:

The circuit searches for the occurrence of the $5EA_{X16}$ Address Mark. The 4T detect circuitry remains active, so that, during the search, once a 4T or longer bit cell time input period is detected, the address mark must be found within the next five counts of the read input pulses. If an Address Mark is detected prior to

c) **ADDRESS MARK DETECTION** (Continued)

the Input Counter reaching count 80, the correct phase of the RRC is ensured by resetting the n/2 divider, the $\overline{AMD}$ output is latched low, the PLL training sequence is terminated, and the Read Mode is entered allowing the data field to be read. If the Input Counter reaches count 80 before the Address Mark is detected, the PLL is locked back to the crystal reference oscillator, the RRC output is switched to the crystal reference oscillator divided by 2, and the PLL training sequence is restarted when the Input Counter reaches count 96. Figure 5 depicts the Address Mark detection sequence.

HARD SECTOR MODE

In the Hard Sector mode (SOFT/$\overline{HARD}$ = 0) the SSI 32D5322 utilizes a 4T (1000) Preamble Field and disables the Preamble Search and Address Mark detection circuitry. It allows the PLL to be controlled directly by RG for Hard Sector format operation. With the absence of an Address Mark, the 4T Preamble Field is utilized to properly set the bit cell alignment boundaries for proper decoding.

When RG transitions high, as depicted in Figure 6, reference input to the PLL is switched from the crystal reference oscillator to DLYD DATA, the VCO is phase reset to the next DLYD DATA pulse, and the PLL acquisition begins. When 32 '1' Preamble bits are detected, the RRC output is switched to the VCO clock divided by 2, and the Read Mode is entered allowing the data field to be read.

In the Hard Sector mode, the NRZ output is inverted and will remain low until the data field is read, as shown in Figure 7. Since the Preamble Search circuitry is not utilized, the external one-shot timing components (Cd, Rd) are not required and the SDS pin can be left open.

WRITE OPERATION

In the Write Mode the SSI 32D5322 converts NRZ data from the controller into 2, 7 RLL formatted data for storage onto the disk. The SSI 32D5322 can operate with a soft or hard sectored disk drive. In the Soft Sector Mode, (SOFT/$\overline{HARD}$ = 1) the device generates a 3T Preamble Field and can insert a N7V Address Mark. The N7V Address Mark is a valid 2, 7 RLL pattern which is not contained in the code set. In the Hard Sector Mode, (SOFT/$\overline{HARD}$ = 0) the device generates a 4T Preamble Field and no Address Mark. Serial NRZ data is clocked into the SSI 32D5322 and latched on defined cell boundaries. The NRZ input data must be synchronous with the rising edges of the WCLK input. In a SCSI or ST506 operation, WCLK is connected directly to the RRC output.

SOFT SECTOR MODE

In the Soft Sector Mode, when WRITE GATE (WG), transitions high and the NRZ input is held low, the SSI 32D5322 automatically generates the 3T (100) Preamble Field at the WRITE DATA ($\overline{WD}$), output. The 3T Preamble Field will continue to be generated until the first low to high transition on the NRZ line. As shown in Figure 8, the first low to high transition occurs with the second bit '1' of the 5_{16} (0101) in the $5EAx_{16}$ Address Mark generation pattern. To generate the Address Mark, the SSI 32D5322 automatically changes the '1' in the eleventh position (see note 3) of the 2, 7 RLL encoded sequence, to a '0'. This generates a pattern of seven zero's followed by two zero's. This unique pattern satisfies the 2, 7 RLL constraints, but will never occur during a normal encoding sequence. The x_{16} of the $5EAx_{16}$ Address Mark generation pattern can be selected, a 'C_{16}' (1100) was utilized in this example.

HARD SECTOR MODE

In the Hard Sector Mode, when WG goes high and the NRZ input is held low, the SSI 32D5322 automatically generates the 4T (1000) Preamble Field at the WRITE DATA, $\overline{WD}$, output. Note that in the Hard Sector mode, the NRZ input is inverted, therefore a constant low is equivalent to an '11 . . . ' input which generates the 4T '1000 . . . ' Preamble Field. The 4T Preamble Field will be generated between the time WG goes high and the first low to high transition on the NRZ line. The SSI 32D5322 requires a minimum of 32 4T (1000) bit groups prior to the data field.

PIN DESCRIPTIONS

INPUT PINS

NAME	TYPE	DESCRIPTION
$\overline{RD}$	I	READ DATA: Encoded Read Data from the disk drive read channel, active low.
RG	I	READ GATE: Selects the PLL reference input and initiates the PLL synchronization sequence. A high level selects the $\overline{RD}$ input and enables the Read Mode/Address Mark Detection sequences. A low level selects the crystal reference oscillator. Pin RG has an internal resistor pull-up.
WG	I	WRITE GATE: Enables the write mode. Pin WG has an internal resistor pull-up.
WSL	I	WINDOW SYMMETRY LATCH: Used to latch the input window symmetry control bits WSD, $\overline{WS0}$ and $\overline{WS1}$ into the internal DAC. An active high level latches the input bits. Pin WSL has an internal resistor pull-up. If unused, connect this pin to ground.
WSD	I	WINDOW SYMMETRY DIRECTION: Controls the direction of the optional window symmetry shift. Pin WSD has an internal resistor pull-up. If unused, this pin can be left open.
$\overline{WS0}$	I	WINDOW SYMMETRY CONTROL BIT: A low level introduces a window shift of 1.5% TORC (Read Reference Clock Period) in the direction established by WSD. Pin $\overline{WS0}$ has an internal resistor pull-up. If unused, this pin can be left open.
$\overline{WS1}$	I	WINDOW SYMMETRY CONTROL BIT: A low level introduces a window shift of 6% TORC (Read Reference Clock Period) in the direction established by WSD. A low level at both $\overline{WS0}$ and $\overline{WS1}$ will produce the sum of the two window shifts. Pin $\overline{WS1}$ has an internal resistor pull-up. If unused, this pin can be left open.
SOFT/$\overline{HARD}$	I	SOFT/$\overline{HARD}$ SECTOR: Selects the address mark and the Preamble field patterns. A high level (Soft Sector) selects a 3T Preamble Field pattern and a non-violating 2, 7 address mark, N7V. A low level (Hard Sector) selects a 4T Preamble Field pattern and disables the address mark circuitry. Pin SOFT/$\overline{HARD}$ has an internal resistor pull-up.
WCLK	I	WRITE CLOCK: Write Clock input. Must be synchronous with the Write Data input on the NRZ Data Port. For small cable delays, WCLK may be connected directly to pin RRC (Read/Reference Clock).
EPD	I	ENABLE PHASE DETECTOR: A low level (Coast Mode) disables the phase detector and allows the VCO to coast. Pin EPD has an internal resistor pull up.

BIDIRECTIONAL PINS

NRZ	I/O	NRZ DATA PORT: Read Data output when RG is high and Write Data input when WG is high. In the idle mode NRZ is in a high impedance state.

PIN DESCRIPTIONS (Cont.)

OUTPUT PINS

NAME	TYPE	DESCRIPTION
$\overline{WD}$	O	WRITE DATA: Encoded write data output, active low.
RRC	O	READ/REFERENCE CLOCK: A multiplexed clock source used by the controller. In the read mode, this clock is the VCO frequency divided by two (1/TORC) and in the write mode it is the crystal reference frequency divided by two (1/TORO). No short clock pulses are generated during a mode change.
$\overline{AMD}$	O	ADDRESS MARK DETECT: In the soft sector Read Mode, a latched low level output indicates that an address mark has been detected. In non-Read modes $\overline{AMD}$ is configured as a high impedance output.
$\overline{SDO}$	O	SYNC DETECT OUTPUT: An active low output that indicates successful detection of the 3T Preamble sync field. THE $\overline{SDO}$ pin is not a TTL level signal.

ANALOG PINS

IREF	I	TIMING PROGRAM PIN: The VCO center frequency and the 1/4 Cell Delay are a function of the current source into pin IREF. The current is set by an external resistor, RR, connected from IREF to VPA.
XTAL1, XTAL2	I	CRYSTAL OSCILLATOR CONNECTIONS: If a crystal oscillator is not desired, XTAL1 maybe driven by a TTL source with XTAL2 open. The frequency must be at twice the data rate.
PD OUT	O	PHASE DETECTOR OUTPUT: Drives the Loop Filter input.
VCO IN	I	VCO CONTROL INPUT: Driven by the Loop Filter output.
SDS	I	SYNC DETECT SET: Used to program the sync detect retriggerable one-shot timing with an external R-C network. Connect the capacitor, Cd, to VPA and the resistor, Rd, to AGND.
RF, RS	I	WINDOW SYMMETRY ADJUST PINS: Provides analog control over the decode window symmetry; typically used to null out any window symmetry offset. A resistor connected from either RF or RS to AGND will provide magnitude and direction control. They can be used in conjunction with the digital control port WSD, $\overline{WS0}$, $\overline{WS1}$.

POWER

DGND,AGND	I	DIGITAL AND ANALOG GROUND
VPA	I	ANALOG +5V
VPD	I	DIGITAL +5V

NRZ	2, 7 RLL
10	0100
11	1000
000	000100
010	100100
011	001000
0010	00100100
0011	00001000

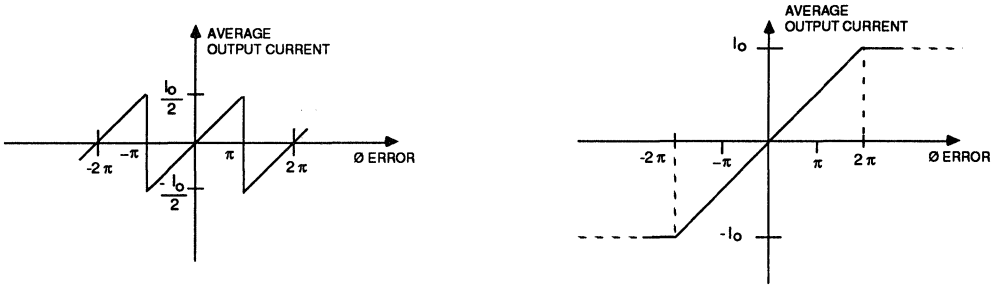
TABLE 1: 2, 7 RLL Code Set

WG	RG	MODE
0	0	IDLE
0	1	READ
1	0	WRITE
1	1	ILLEGAL

TABLE 2: Mode Control

Ts, NOMINAL WINDOW SHIFT	WSD	$\overline{WS1}$	$\overline{WS0}$
+TS3	0	0	0
+TS2	0	0	1
+TS1	0	1	0
0	0	1	1
-TS3	1	0	0
-TS2	1	0	1
-TS1	1	1	0
0	1	1	1

TABLE 3: Decode Window Symmetry Control



a) HARMONIC MODE

b) NON-HARMONIC MODE

Note 1) Io is the magnitude of the charge pump current.
2) Phase error is relative to the VCO period

FIGURE 1: Phase Detector Transfer Function

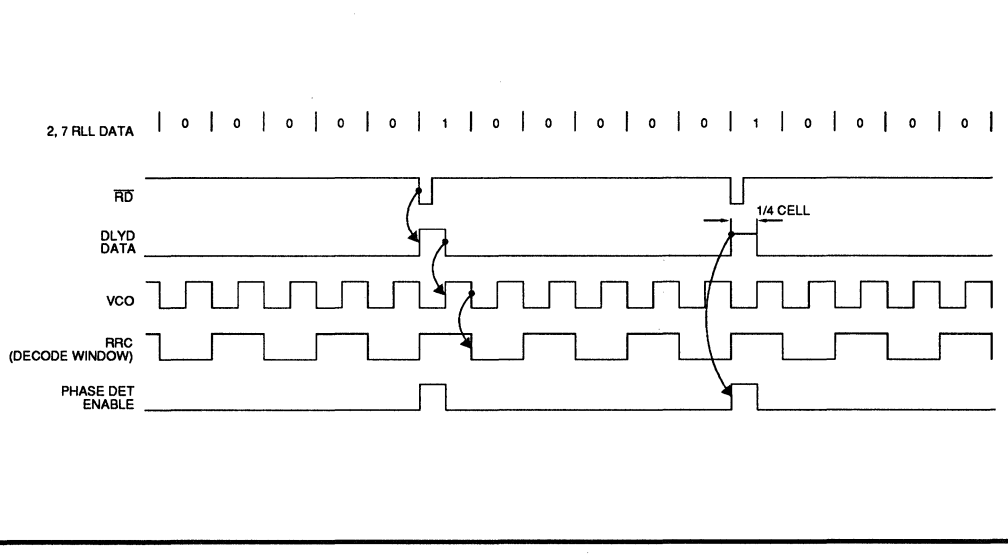


FIGURE 2: Data Synchronization Waveform Diagram

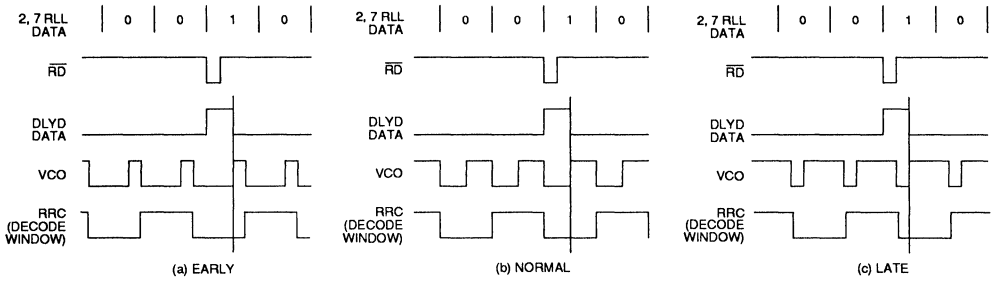
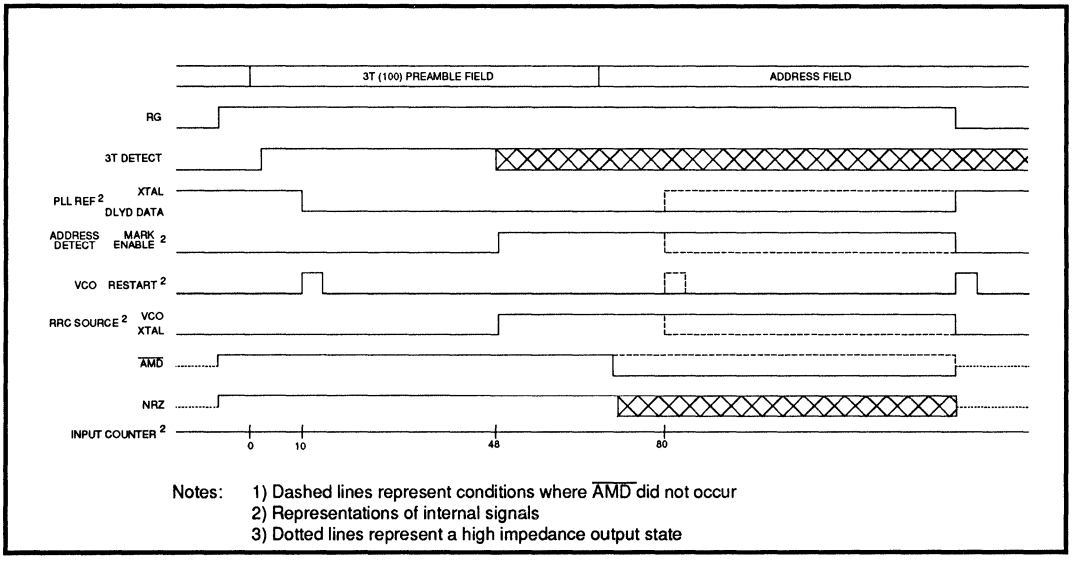
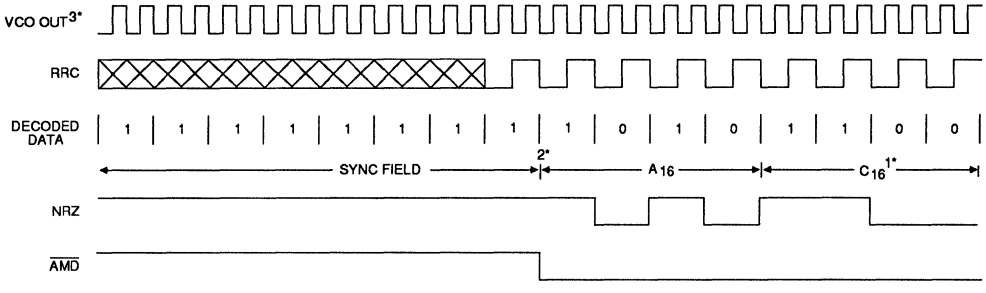


FIGURE 3: Decode Window



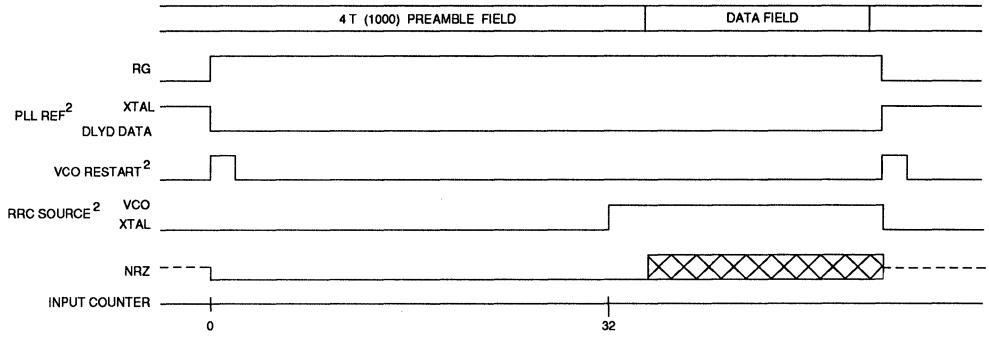
Notes: 1) Dashed lines represent conditions where $\overline{AMD}$ did not occur
2) Representations of internal signals
3) Dotted lines represent a high impedance output state

FIGURE 4: Soft Sector Mode Timing Diagram



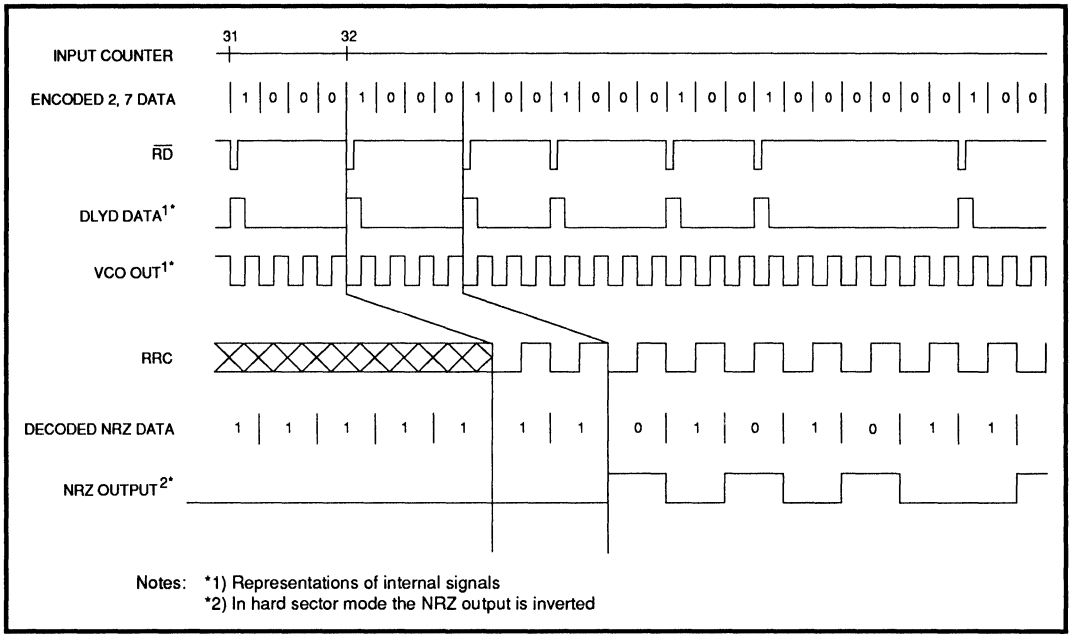
Notes: *1) These four bits can be any combination, C16 (1100) was selected in this example
*2) The 5E16 of the 5EAx16 Address Mark is not read back
*3) Representations of internal signals

FIGURE 5: Address Mark Detection and NRZ Output Waveform



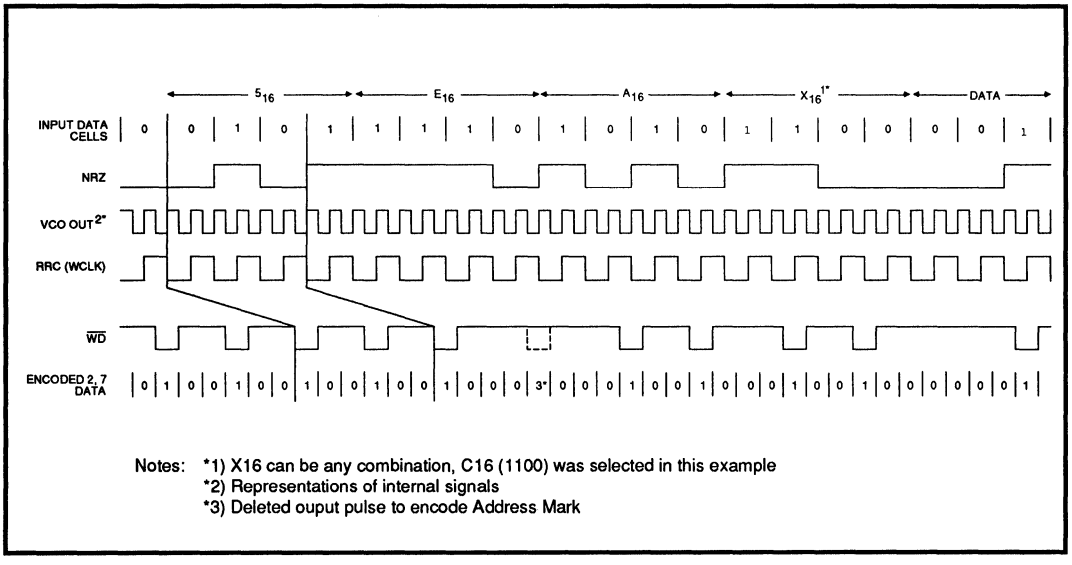
Notes: 1) Dashed lines represent a high impedance output state
2) Representations of internal signals

FIGURE 6: Hard Sector Mode Timing Diagram



Notes: *1) Representations of internal signals
*2) In hard sector mode the NRZ output is inverted

FIGURE 7: Hard Sector Mode Decode Timing



Notes: *1) X16 can be any combination, C16 (1100) was selected in this example
*2) Representations of internal signals
*3) Deleted ouput pulse to encode Address Mark

FIGURE 8: Write Address Mark Generation

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATINGS	UNIT
Storage Temperature	-65 to +150	°C
Ambient Operating Temperature, TA	0 to +70	°C
Junction Operating Temperature	0 to +130	°C
Supply Voltage, VCC	-0.5 to 7	Vdc
Voltage Applied to Logic inputs	-0.5 to VCC +0.5	Vdc
Maximum Power Dissipation	950	mW

DC ELECTRICAL CHARACTERISTICS - unless otherwise specified, 4.75V < VCC < 5.25V, TA = 0°C to 70°C, 7.5 MHz < 1/TORC < 15 MHz , 15 MHz < 1/TVCO < 30 MHz

PARAMETER	CONDITIONS	MIN	MAX	UNIT
VIH, High Level Input Voltage		2.0		V
VIL, Low Level Input Voltage			0.8	V
IIH, High Level Input Current	VIH = 2.7V		20	µA
IIL, Low Level Input Current	VIL = 0.4V		-0.36	mA
VOH, High Level Output Voltage	IOH = -400 µA	2.4		V
VOL, Low Level Output Voltage	IOL = 4 mA		0.5	V
ICC, Power Supply Current	All outputs open		165	mA

DYNAMIC CHARACTERISTICS AND TIMING

READ MODE (See Figure 9)

TRD, Read Data Pulse Width		20	TORC-40	ns
TFRD, Read Data Fall Time	2.0V to 0.8V, CL ≤ 15 pF		15	ns
TRRC, Read Clock Rise Time	0.8V to 2.0V, CL ≤ 15 pF		8	ns
TFRC, Read Clock Fall Time	2.0V to 0.8V, CL ≤ 15 pF		5	ns
TPNRZ, NRZ (out) Propagation Delay		-15	15	ns
TPAMD, $\overline{AMD}$ Propagation Delay		-15	15	ns
1/4 Cell + Retriggerable One-Shot Detect Stability		-4	+4	%
1/4 Cell + Retriggerable One-Shot Delay (see note)	TD=10.5(RR+0.5)+0.12Rd(Cd+Cs) Cs=Stray capacitance, RR = kΩ Rd = kΩ, Cd = 68 pF to 100 pF	0.89 TD	1.11 TD	ns
Note: Excludes External Capacitor and Resistor Tolerances				

WRITE MODE (See figure 10)

PARAMETER		CONDITIONS	MIN	MAX	UNIT
TWD	Write Data Pulse Width	CL ≤15 pF	(TORO/2) -12	(TORO/2) +12	ns
TFWD	Write Data Fall Time	2.0V to 0.8V, CL ≤ 15 pF		8	ns
TOWC	Write Data Clock Repetition Period		TORO -12	TORO +12	ns
TRWC	Write Data Clock Rise Time	0.8V to 2.0V		10	ns
TFWC	Write Data Clock Fall Time	2.0V to 0.8V		8	ns
TSNRZ	NRZ (in) Set Up Time		20		ns
THNRZ	NRZ (in) Hold Time		7		ns

DATA SYNCHRONIZATION

PARAMETER		CONDITIONS	MIN	MAX	UNIT
TVCO	VCO Center Frequency Period	VCO IN = 2.7V TO = 1.14 E-11 (RR + 1200) VCC = 5.0V	0.8 TO	1.2 TO	sec
	VCO Frequency Dynamic Range	1.0V ≤ VCO IN ≤ VCC -0.6V VCC = 5.0V	±24	±40	%
KVCO	VCO Control Gain	ωo = 2π / TO 1.0V ≤ VCO IN ≤ VCC -0.6V	0.14 ωo	0.20 ωo	rad/s V
KD	Phase Detector Gain	KD = 0.309 / (RR + 500) VCC = 5.0V	0.83 KD	1.17 KD	A/rad
	KVCO x KD Product Accuracy		-28	+28	%
	VCO Phase Restart Error		-0.5	+0.5	rad
	Decode Window Centering Accuracy			± (0.01 TORC+2)	ns
	Decode Window		(TORC/2)-2		ns
TS1	Decode Window Time Shift Magnitude	TS1 = 0.015 TORC	0.85 TS1	1.15 TS1	sec
TS2	Decode Window Time Shift Magnitude	TS2 = 0.06 TORC	0.90 TS2	1.1 TS2	sec

DATA SYNCHRONIZATION (Continued)

PARAMETER		CONDITIONS	MIN	MAX	UNIT
TS3	Decode Window Time Shift Magnitude	TS3 = 0.075 TORC	0.90 TS3	1.1 TS3	sec
TSA	Decode Window Time Shift Magnitude	$TSA = 0.125\ TORC\left(1 - \frac{680+R}{1180+R}\right)$ with: R in ohms	0.65 TSA	1.35 TSA	sec

CONTROL CHARACTERISTICS (See figure 11)

PARAMETER	CONDITIONS	MIN	MAX	UNIT
TSWS, $\overline{WS0}$, $\overline{WS1}$, WSD Set Up Time		50		ns
THWS, $\overline{WS0}$, $\overline{WS1}$, WSD Hold Time		0		ns
RG, WG, SOFT/$\overline{HARD}$ Time Delay			100	ns

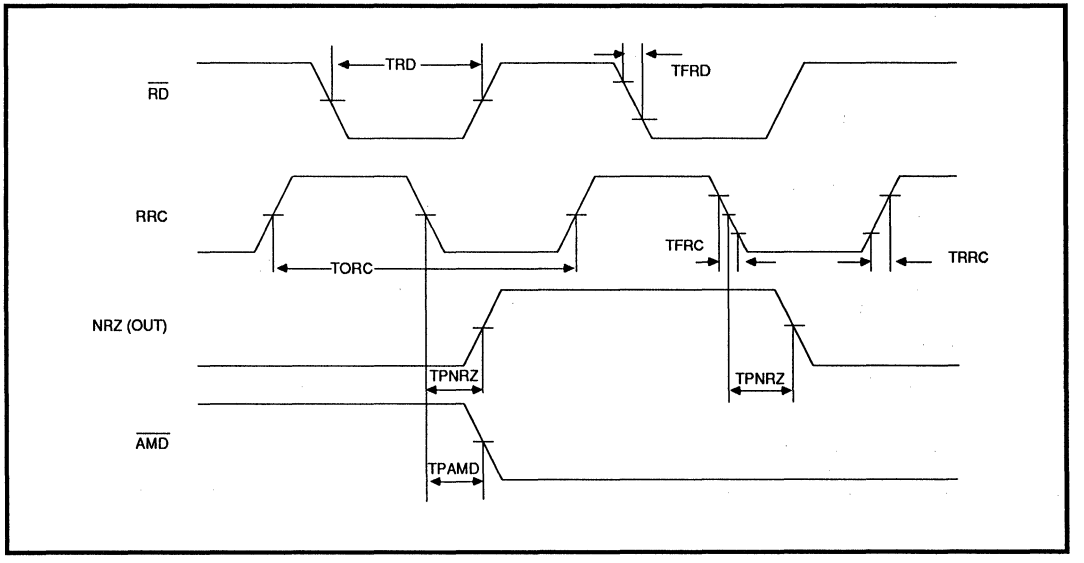


FIGURE 9: Read Timing

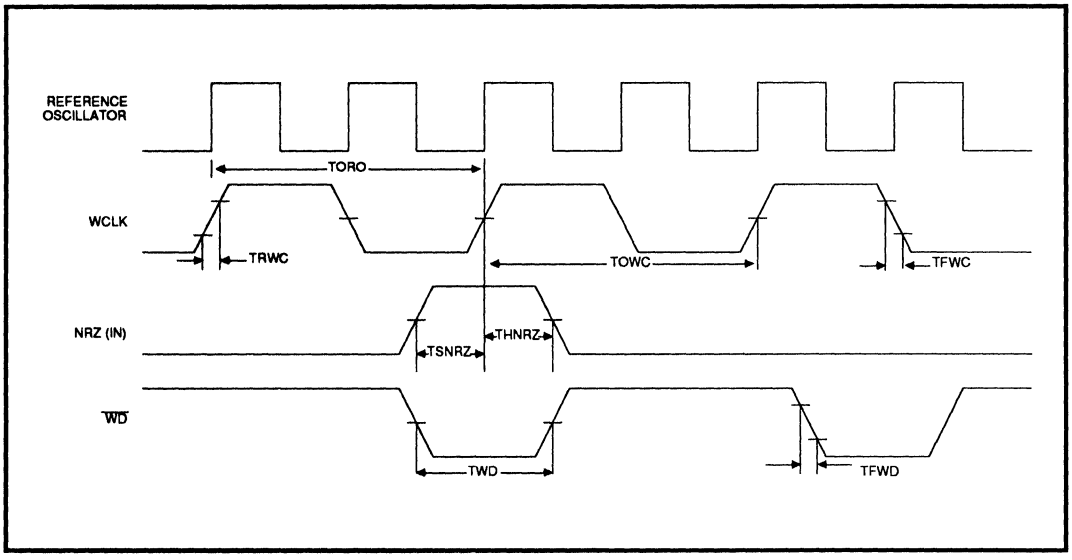


FIGURE 10: Write Timing

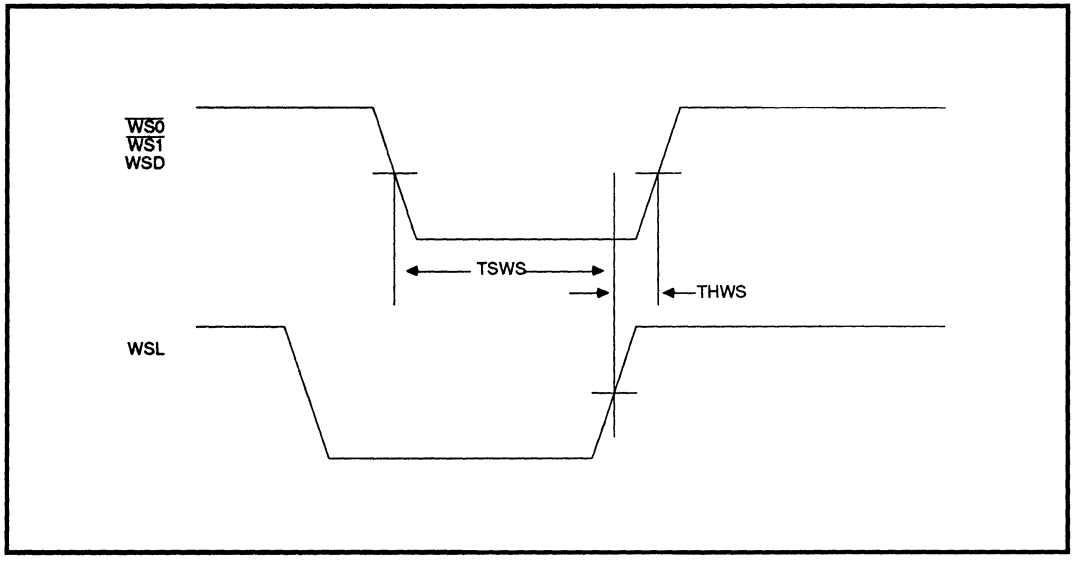


FIGURE 11: Control Timing

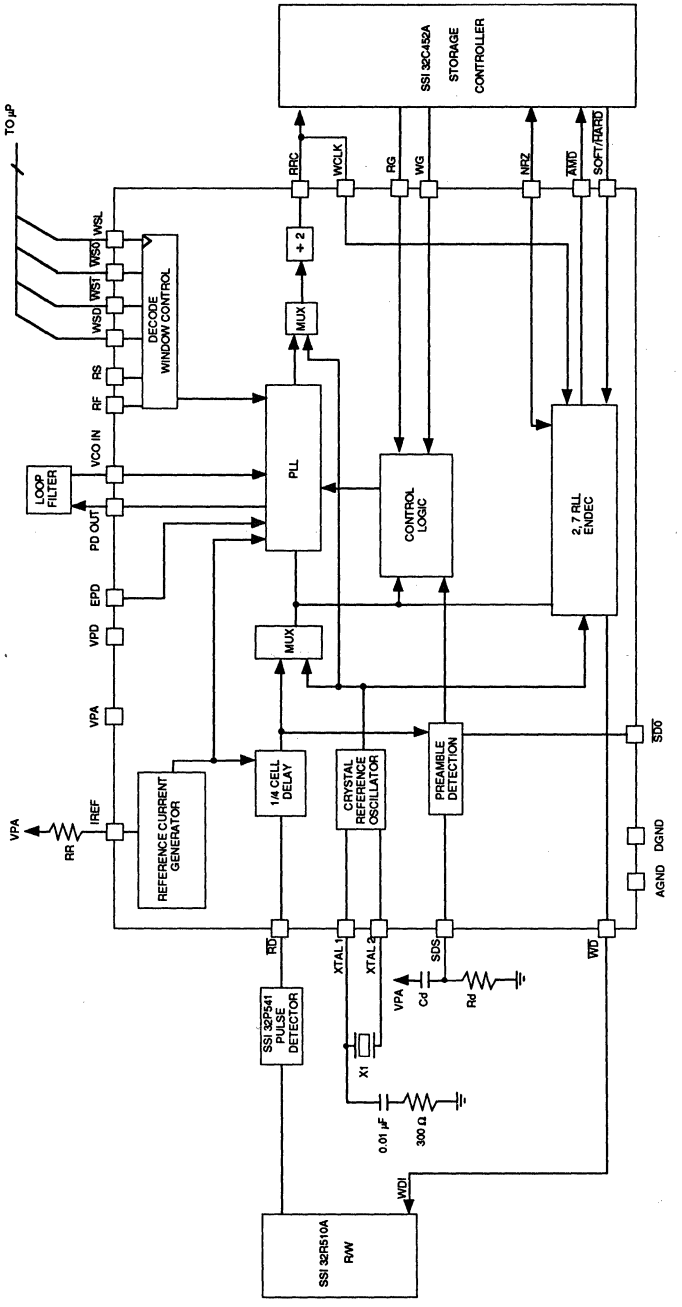
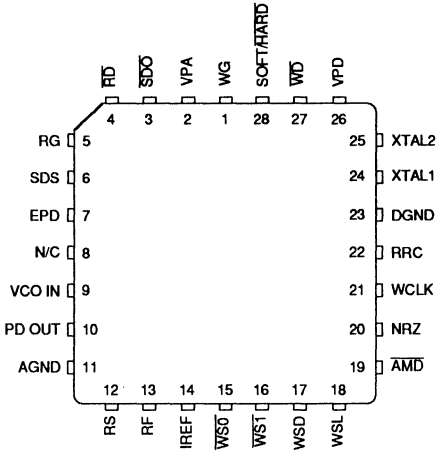


FIGURE 12: SSI 32D5322 Typical Application

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



28-pin PLCC

4

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32D5322 28-pin PLCC	32D5322-CH	32D5322-CH

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc. 14351 Myford Road, Tustin, CA 92680, (714) 731-7110, FAX (714) 573-6914

Notes:

silicon systems®
A TDK Group Company

SSI 32D535
Data Synchronizer/ 2, 7 RLL ENDEC with Write Precompensation

November 1991

4

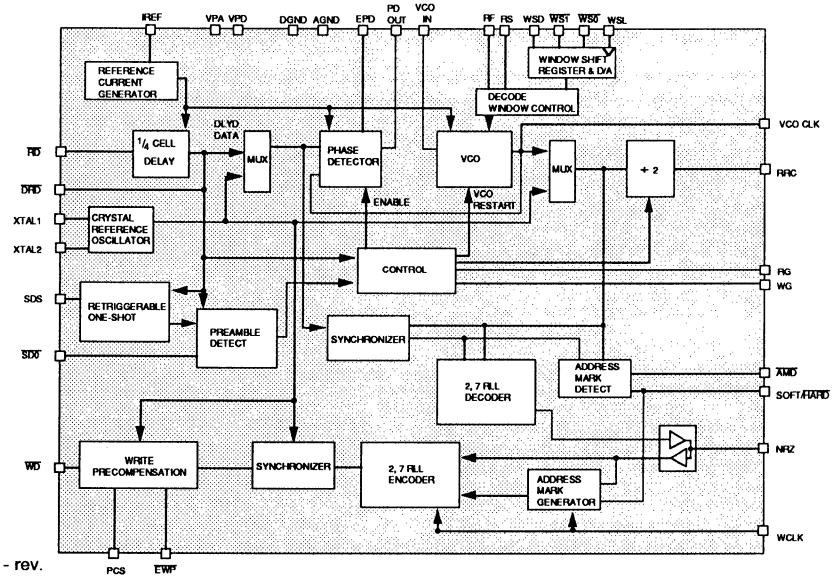
DESCRIPTION

The SSI 32D535 Data Separator provides data recovery, data encoding, and write precompensation for storage systems which employ a 2, 7 RLL encoding format. Data synchronization is performed with a fully integrated high performance PLL. A zero phase restart technique is used to minimize PLL acquisition time. The SSI 32D535 has been optimized for operation at a single data rate between 7.5 to 10 Mbit/s operation utilizing a crystal reference oscillator. The VCO frequency setting elements are incorporated within the SSI 32D535 for enhanced performance and reduced board space. Data rate is established with a single external programming resistor. The SSI 32D535 utilizes an advanced bipolar process technology which affords precise decode window control without requiring an accurate 1/4 cell delay or external devices. To enhance disk drive testability, decode window symmetry control is available through a digital µP port and/or two analog pins. This feature can facilitate defect mapping, automatic calibration, systematic error cancellation, window margin testing, and error recovery. The SSI 32D535 requires a single +5V power supply and is available in a 32-pin SOW, DIP & 28-pin PLCC package.

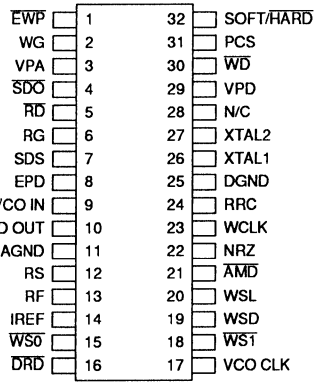
FEATURES

- **Data Synchronizer and 2, 7 RLL ENDEC**
- **Write Precompensation**
- **7.5 to 10 Mbit/s Programmed with a Single External Resistor or Current Source**
- **Optimized for Operation with the SSI 32C452A and AIC 010 Controllers**
- **ESDI compatible**
- **Programmable Decode Window Symmetry via a µP Port and/or Analog Pins**
- **Fast Acquisition Phase Locked Loop**
  - **Zero Phase Restart Technique**
- **Input Clock Circuitry Optimized for use with Crystal Controlled Reference Oscillator**
- **Hard/Soft Sector Operation**
- **+5V Operation**
- **32-Pin SOW & 28-Pin PLCC**

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

PIN DESCRIPTION

INPUT PINS

NAME	TYPE	DESCRIPTION
$\overline{RD}$	I	READ DATA: Encoded Read Data from the disk drive read channel, active low.
RG	I	READ GATE: Selects the PLL reference input and initiates the PLL synchronization sequence. A high level selects the $\overline{RD}$ input and enables the Read Mode/Address Mark Detection sequences. A low level selects the crystal reference oscillator. Pin RG has an internal resistor pull-up.
WG	I	WRITE GATE: Enables the write mode. Pin WG has an internal resistor pull-up. If unused, tie pin low.
WSL	I	WINDOW SYMMETRY LATCH: Used to latch the input window symmetry control bits WSD, $\overline{WS0}$ and $\overline{WS1}$ into the internal DAC. An active high level latches the input bits. Pin WSL has an internal resistor pull-up. If unused, tie pin low.
WSD	I	WINDOW SYMMETRY DIRECTION: Controls the direction of the optional window symmetry shift. Pin WSD has an internal resistor pull-up.
$\overline{WS0}$	I	WINDOW SYMMETRY CONTROL BIT: A low level introduces a window shift of 1.5% TORC (Read Reference Clock Period) in the direction established by WSD. Pin $\overline{WS0}$ has an internal resistor pull-up. If unused, leave open or tie high.
$\overline{WS1}$	I	WINDOW SYMMETRY CONTROL BIT: A low level introduces a window shift of 6% TORC (Read Reference Clock Period) in the direction established by WSD. A low level at both $\overline{WS0}$ and $\overline{WS1}$ will produce the sum of the two window shifts. Pin $\overline{WS1}$ has an internal resistor pull-up. If unused, leave open or tie high.
SOFT/$\overline{HARD}$	I	SOFT/$\overline{HARD}$ SECTOR: Selects the address mark and the Preamble field patterns. A high level (Soft Sector) selects a 3T Preamble Field pattern and a non-violating 2, 7 address mark, N7V. A low level (Hard Sector) selects a 4T Preamble Field pattern and disables the address mark circuitry. Pin SOFT/$\overline{HARD}$ has an internal resistor pull-up.
WCLK	I	WRITE CLOCK: Write Clock input. Must be synchronous with the Write Data input on the NRZ Data Port. For small cable delays, WCLK may be connected directly to pin RRC (Read/Reference Clock).
EPD	I	ENABLE PHASE DETECTOR: A low level (Coast Mode) disables the phase detector and allows the VCO to coast. Pin EPD has an internal resistor pull up.
$\overline{EWP}$	I	ENABLE WRITE PRECOMPENSATION: A low level enables Write Precompensation. Pin $\overline{EWP}$ has an internal resistor pull-up.

PIN DESCRIPTION (Continued)

OUTPUT PINS

NAME	TYPE	DESCRIPTION
$\overline{WD}$	O	WRITE DATA: Encoded write data output, active low.
RRC	O	READ/REFERENCE CLOCK: A multiplexed clock source used by the controller. In the read mode, this clock is the VCO frequency divided by two (1/TORC) and in the write mode it is the crystal reference frequency divided by two (1/TORO). No short clock pulses are generated during a mode change.
$\overline{AMD}$	O	ADDRESS MARK DETECT: In the soft sector Read Mode, a latched low level output indicates that an address mark has been detected. In non-Read modes $\overline{AMD}$ is configured as a high impedance output.
$\overline{SDO}$	O	SYNC DETECT OUTPUT: An active low output that indicates successful detection of the 3T Preamble sync field. THE $\overline{SDO}$ pin is not a TTL level signal.
VCO CLK	O	VCO CLK: An open emitter VCO clock test point. Two external resistors are required to utilize this output, they can be removed during normal operaton for reduced power dissipation.
$\overline{DRD}$	O	DELAYED READ DATA: Test point. The positive edges of this open emitter output signal indicate the data bit position. The positive edges of the $\overline{DRD}$ and the VCO CLK signals can be used to estimate window centering. The time jitter of $\overline{DRD}$'s positive edge is an indication of media bit shift. Two external resistors are required to perform this test, they can be removed during normal operation for reduced power dissipation.

BIDIRECTIONAL PINS

NRZ	I/O	NRZ DATA PORT: Read Data output when RG is high and Write Data input when WG is high. In the idle mode NRZ is in a high impedance state.

ANALOG PINS

IREF	I	TIMING PROGRAM PIN: The VCO center frequency and the 1/4 Cell Delay are a function of the current sourced into pin IREF. The current is set by an external resistor, RR, connected from IREF to VPA.
PCS	I	PRECOMP SET: Used to set the magnitude of the Write Precompensation time shift via an external capacitor, Cp to VPA and an external resistor, Rp to AGND.
XTAL1, XTAL2	I	CRYSTAL OSCILLATOR CONNECTIONS: The frequency must be at twice the data rate.
PD OUT	O	PHASE DETECTOR OUTPUT: Drives the Loop Filter input.
VCO IN	I	VCO CONTROL INPUT: Driven by the Loop Filter output.

PIN DESCRIPTION (Continued)

OUTPUT PINS (Continued)

NAME	TYPE	DESCRIPTION
SDS	I	SYNC DETECT SET: Used to program the sync detect retriggerable one-shot timing with an external R-C network. Connect the capacitor, Cd, to VPA and the resistor, Rd, to AGND.
RF, RS	I	WINDOW SYMMETRY ADJUST PINS: Provides analog control over the decode window symmetry; typically used to null out any window symmetry offset. A resistor connected from either RF or RS to AGND will provide magnitude and direction control. They can be used in conjunction with the digital control port WSD, $\overline{WS0}$, $\overline{WS1}$.

POWER

DGND, AGND	I	DIGITAL AND ANALOG GROUND
VPA	I	ANALOG +5V
VPD	I	DIGITAL +5V

OPERATION

The SSI 32D535 is designed to perform data recovery and data encoding in rotating memory systems which utilize a 2, 7 RLL encoding format. In the Read Mode the SSI 32D535 performs Data Synchronization, Sync Field Search and Detect, Address Mark Detect and Data Decoding. In the Write Mode, the SSI 32D535 converts NRZ data into the 2,7 RLL format described in Table 1, performs write precompensation, generates the Preamble Field, and inserts Address Marks as requested. The interface electronics and architecture of the SSI 32D535 have been optimized for use as a companion device to the SSI 32C452 or AIC 010 controllers.

The SSI 32D535 can operate with data rates ranging from 7.5 to 10 Mbit/s operation. This data rate is established by a single 1% external resistor, RR, connected from pin IREF to VPA. This resistor establishes a reference current which sets the VCO center frequency, the phase detector gain, and the 1/4 cell delay. The value of this resistor is given by:

$$RR = \frac{40.67}{DR} - 0.5\ (k\Omega)$$

where: DR = Data Rate in Mbit/s.

An internal crystal reference oscillator, operating at twice the data rate, generates the standby reference for the PLL. A series resonant crystal between XTAL1 and XTAL2 should be selected at twice the Data Rate.

The SSI 32D535 employs a Dual Mode Phase Detector; Harmonic in the Read Mode and Non-Harmonic in Write and Idle Modes. In the Read Mode the Harmonic Phase Detector updates the PLL with each occurrence of a DLYD DATA pulse. In the Write and Idle Modes the Non-Harmonic Phase Detector is continuously enabled, thus maintaining both phase and frequency lock. By acquiring both phase and frequency lock to the crystal reference oscillator and utilizing a zero phase restart technique, false lock to DLYD DATA is eliminated.

The phase detector incorporates a charge pump in order to drive the loop filter directly. The polarity and width of the output current pulses correspond to the direction and magnitude of the phase error. Figure 1 depicts the average output current as a function of the input phase error (relative to the VCO period).

The READ GATE (RG), and WRITE GATE (WG), inputs control the device mode as described in Table 2. RG is an asynchronous input and may be initiated or terminated at any position on the disk. WG is also an asynchronous input, but should not be terminated prior to the last output Write Data pulse.

READ OPERATION

The Data Synchronizer utilizes a fully integrated fast acquisition PLL to accurately develop the decode window. Read Gate, RG, initiates the PLL locking sequence and selects the PLL reference input; a high level (Read Mode) selects the $\overline{RD}$ input and a low level selects the crystal reference oscillator.

In the Read Mode the rising edge of DLYD DATA enables the Phase Detector while the falling edge is phase compared to the rising edge of the VCO. As depicted in Figure 2, DLYD DATA is a 1/4 cell wide (TVCO/2) pulse whose leading edge is defined by the leading edge of $\overline{RD}$. An accurate and symmetrical decode window is developed from the VCO clock. The decode window is generated from the falling edges of the VCO clock. By utilizing a fully integrated symmetrical VCO running at twice the data rate, the decode window is insured to be accurate and centered symmetrically about the falling edges of DLYD DATA. The accuracy of the 1/4 cell delay only affects the retrace angle of the phase detector and does not influence the accuracy of the decode window.

Shifting the symmetry of the VCO clock effectively shifts the relative position of the DLYD DATA pulse within the decode window. This powerful capability easily facilitates defect mappings, automatic calibration, window margin testing, error recovery, and systematic error cancellation. For enhanced disk drive testability and error recovery, decode window control is provided via a µP port (WSL, WSD, $\overline{WS0}$, $\overline{WS1}$) as described in Table 3. In applications not utilizing this feature, WSL must be connected to ground, while WSD, $\overline{WS0}$, and $\overline{WS1}$ must be left open.

Window shifts in the range of ±1.5% to ±7.5% of TORC are easily programmed by latching the appropriate control word into the Window Shift Register with the WSL pin. Shifts in the positive or negative directions result in early or late decode windows respectively, as depicted in Figure 3. Additionally, for small systematic error cancellation, a resistor, R, connected from either RS (Early) or RF (Late) to ground will provide analog control over the decode window. The magnitude of this shift, TSA is determined by:

$$TSA = 0.125\ TORC\left(1 - \frac{680 + R}{1180 + R}\right)$$

where: R is in ohms

Pins RF and RS are intended to be used as a trim and should be restricted to ±1.5% window shifts. They can be used in conjunction with the digital control port.

The VCO CLK and $\overline{DRD}$ outputs can be used to estimate window centering and data bit shift. The rising edges of VCO CLK indicate the data detection window edges. The rising edge of $\overline{DRD}$ indicates the data bit position relative to the decode window. Two external resistors are required during such testing. A pull-up resistor of 130Ω should be connected to VPD, while a pull-down resistor of 200Ω should be connected to DGND. The resistors can be removed during normal operation to reduce power dissipation.

In Non-Read Modes, the PLL is locked to the crystal reference oscillator. This forces the VCO to run at a frequency which is very close to that required for tracking actual data and thus minimizes the associated frequency step during acquisition. When the reference input to the PLL is switched, the VCO is stopped momentarily, then restarted in an accurate phase alignment with the next PLL reference input pulse, and the VCO clock divider is reset. By minimizing the phase alignment in this manner (phase error ≤ 0.5 rads), the acquisition time is substantially reduced.

The SSI 32D535 provides two sync modes for controlling the PLL locking sequence; Soft Sector and Hard Sector.

SOFT SECTOR MODE

The Soft Sector Mode activates the Preamble Search and Address Mark detection circuitry. As depicted in Figure 4, when RG transitions high, the counter is reset and the SSI 32D535 requires 10 high to low transitions (Preamble '1' bits) before switching the reference input to the PLL, 48 high to low transitions before switching the Read Reference Clock to the VCO clock divided by two and activating the Address Mark Detect circuitry; then it must detect the Address Mark prior to 80 high to low transitions in order to enter the Read Mode. This sequence repeats after 95 input '1' bits until the read mode is successfully entered or until RG is cancelled.

When RG transitions high, the following PLL locking sequence begins:

a) PREAMBLE SEARCH:

The 3T detect circuitry initiates the PLL locking sequence once it has detected 10 consecutive '100' bit groups from the 3T preamble field. The 3T detect timing is set by the sum of the 1/4 cell delay and the retriggerable one-shot delay. The 1/4 cell timing capacitor is included on-chip and its timing is externally set by resistor RR. The retriggerable one-shot timing is externally set by resistor Rd and capacitor Cd. The sum of their delays is set to 3.5 bit cell times. Therefore, a continuous stream of input pulses with a 3T bit cell time pulse rate keeps the one-shot reset, and a 4T or longer bit cell time input period allows the one-shot to time out producing a 4T detect pulse. The 4T detect pulse resets the Input Counter and the search is started over.

b) PLL ACQUISITION:

Once 10 consecutive '100' bit groups are detected, the reference input to the PLL is switched from the crystal reference oscillator to the DLYD DATA, the VCO is phase reset to the next DLYD DATA pulse, and PLL acquistion begins. When an additional 38 '100' bit groups are detected, the Read Reference Clock output (RRC) is switched to the VCO clock divided by 2, the 4T Detect circuitry is inhibited, and the Address Mark Detection circuitry is enabled. If a 4T detect pulse occurs before 48 Preamble '1' bits are detected, then the PLL is locked back to the crystal reference oscillator, the RRC output is switched to the crystal reference oscillator divided by 2, the

Input Counter reset, and the sequence is restarted. No short duration glitches will occur at the RRC output during this switching.

c) **ADDRESS MARK DETECTION:**

The circuit searches for the occurrence of the $5EAx_{16}$ Address Mark. If an Address Mark is detected prior to the Input Counter reaching count 80, the correct phase of the RRC is ensured by resetting the n/2 divider, the $\overline{AMD}$ output is latched low, the PLL training sequence is terminated, and the Read Mode is entered allowing the data field to be read. If the Input Counter reaches count 80 before the Address Mark is detected, the PLL is locked back to the crystal reference oscillator, the RRC output is switched to the crystal reference oscillator divided by 2, and the PLL training sequence is restarted when the Input Counter reaches count 96. Figure 5 depicts the Address Mark detection sequence.

HARD SECTOR MODE

In the Hard Sector mode (SOFT/$\overline{HARD}$ = 0) the SSI 32D535 utilizes a 4T (1000) Preamble Field and disables the Preamble Search and Address Mark detection circuitry. It allows the PLL to be controlled directly by RG for Hard Sector format operation. With the absence of an Address Mark, the 4T Preamble Field is utilized to properly set the bit cell alignment boundaries for proper decoding.

When RG transitions high, as depicted in Figure 6, reference input to the PLL is switched from the crystal reference oscillator to DLYD DATA, the VCO is phase reset to the next DLYD DATA pulse, and the PLL acquisition begins. When 32 '1' Preamble bits are detected, the RRC output is switched to the VCO clock divided by 2, and the Read Mode is entered allowing the data field to be read.

In the Hard Sector mode, the NRZ output is inverted and will remain low until the data field is read, as shown in Figure 7. Since the Preamble Search circuitry is not utilized, the external one-shot timing components (Cd, Rd) are not required and the SDS pin can be left open.

WRITE OPERATION

In the Write Mode the SSI 32D535 converts NRZ data from the controller into 2, 7 RLL formatted data for storage onto the disk. The SSI 32D535 can operate with a soft or hard sectored disk drive. In the Soft Sector Mode, (SOFT/$\overline{HARD}$ = 1) the device generates a 3T Preamble Field and can insert a N7V Address Mark. The N7V Address Mark is a valid 2, 7 RLL pattern which is not contained in the code set. In the Hard Sector Mode, (SOFT/$\overline{HARD}$ = 0) the device generates a 4T Preamble Field and no Address Mark. Serial NRZ data is clocked into the SSI 32D535 and latched on defined cell boundaries. The NRZ input data must be synchronous with the rising edges of the WCLK input. The WCLK input is a feature provided for operation in an ESDI application to compensate for large cable delays. In a SCSI or ST506 operation, WCLK is connected directly to the RRC output.

Write precompensation circuitry is provided to compensate for media bit shift caused by intersymbol interference. The SSI 32D535 recognizes specific write data patterns and can add or subtract delays in the time position of write data bits to counteract the read back bit shift. The magnitude of the time shift, TC, is determined by an external R-C network on the PCS pin given by:

$$TC = 0.15\ (Rp)(Cp + Cs)$$

with $RP \geq 2.0\ k\Omega$, Cs = stray capacitance

When the ENABLE WRITE PRECOMP, $\overline{EWP}$, input is low the SSI 32D535 performs write precompensation according to the algorithm outlined in Table 4.

SOFT SECTOR MODE

In the Soft Sector Mode, when WRITE GATE (WG), transitions high and the NRZ input is held low, the SSI 32D535 automatically generates the 3T (100) Preamble Field at the WRITE DATA ($\overline{WD}$), output. The 3T Preamble Field will continue to be generated until the first low to high transition on the NRZ line. As shown in Figure 8, the first low to high transition occurs with the second bit '1' of the 5_{16} (0101) in the $5EAx_{16}$ Address Mark generation pattern. To generate the Address Mark, the SSI 32D535 automatically changes the '1' in the eleventh position (see note 3) of the 2, 7 RLL encoded sequence, to a '0'. This generates a pattern of seven zeros followed by two zeros. This unique pattern satisfies the 2, 7 RLL constraints, but will never occur during a normal encoding sequence. The x_{16} of the $5EAx_{16}$ Address Mark generation pattern can be selected, a 'C_{16}' (1100) was utilized in this example.

HARD SECTOR MODE

In the Hard Sector Mode, when WG goes high and the NRZ input is held low, the SSI 32D535 automatically generates the 4T (1000) Preamble Field at the WRITE DATA, $\overline{WD}$, output. Note that in the Hard Sector mode, the NRZ input is inverted, therefore a constant low is equivalent to an '11 . . .' input which generates the 4T '1000 . . . ' Preamble Field. The 4T Preamble Field will be generated between the time WG goes high and the first low to high transition on the NRZ line. The 32D535 requires a minimum of 32 4T (1000) bit groups prior to the data field.

NRZ	2, 7 RLL
10	0100
11	1000
000	000100
010	100100
011	001000
0010	00100100
0011	00001000

TABLE 1: 2, 7 RLL Code Set

WG	RG	MODE
0	0	IDLE
0	1	READ
1	0	WRITE
1	1	ILLEGAL

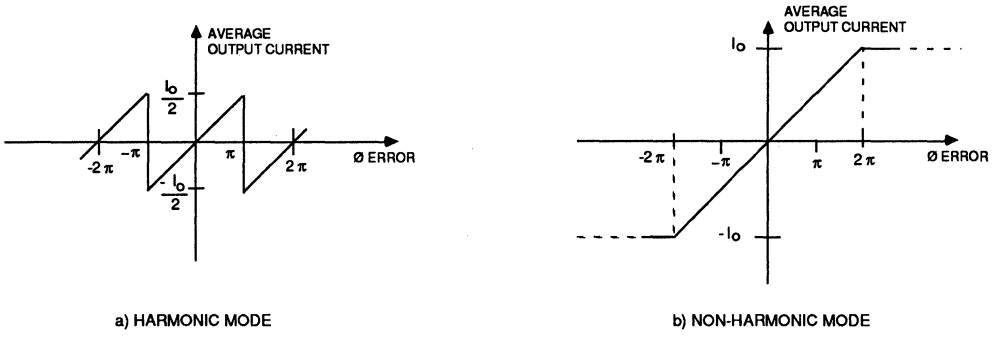
TABLE 2: Mode Control

Ts, NOMINAL WINDOW SHIFT	WSD	$\overline{WS1}$	$\overline{WS0}$
+TS3	0	0	0
+TS2	0	0	1
+TS1	0	1	0
0	0	1	1
-TS3	1	0	0
-TS2	1	0	1
-TS1	1	1	0
0	1	1	1

TABLE 3 : Decode Window Symmetry Control

ENCODED 2, 7 RLL DATA PATTERN							
BIT n - 3	BIT n - 2	BIT n - 1	BIT n	BIT n + 1	BIT n + 2	BIT n + 3	COMPENSATION BIT n
0	0	0	1	0	0	0	none
1	0	0	1	0	0	1	none
1	0	0	1	0	0	0	early
0	0	0	1	0	0	1	late

TABLE 4 : Write Precompensation Algorithm



a) HARMONIC MODE

b) NON-HARMONIC MODE

Notes: 1) Io is the magnitude of the charge pump current
2) Phase error is relative to the VCO period

FIGURE 1: Phase Detector Transfer Function

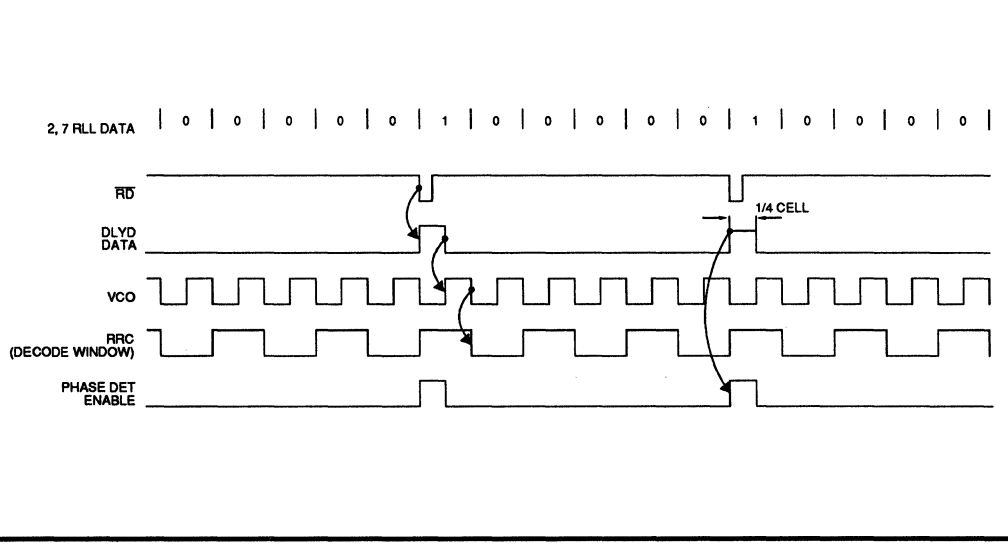


FIGURE 2: Data Synchronization Waveform Diagram

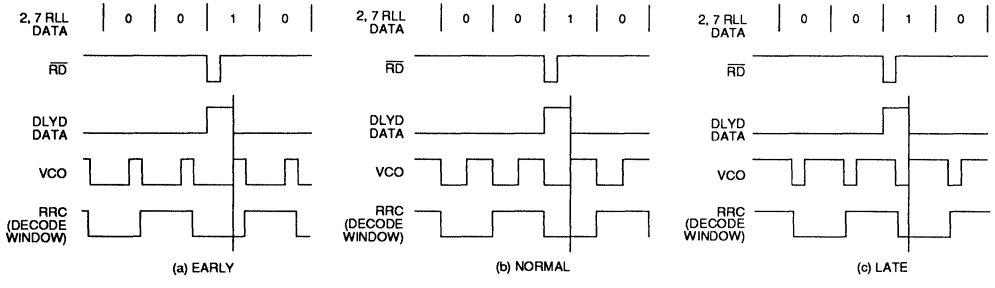
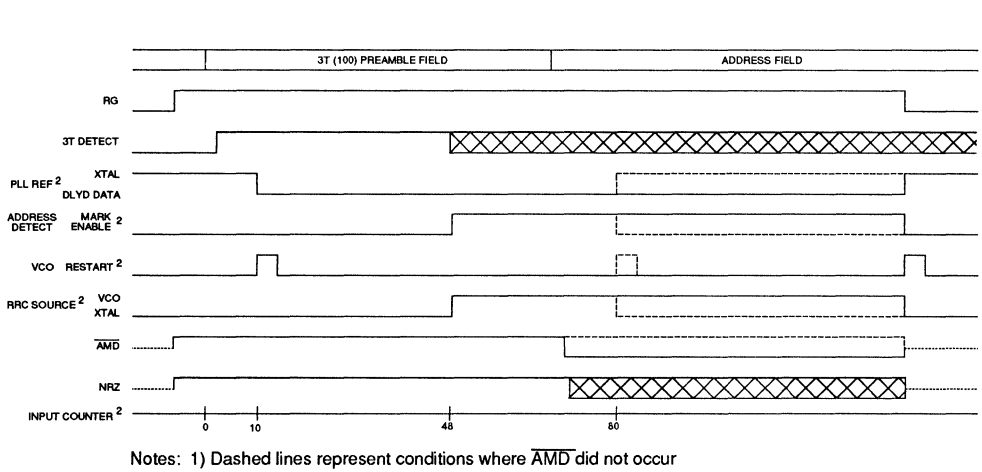


FIGURE 3: Decode Window



Notes: 1) Dashed lines represent conditions where $\overline{AMD}$ did not occur
2) Representations of internal signals
3) Dotted lines represent a high impedance output state

FIGURE 4: Soft Sector Mode Timing Diagram

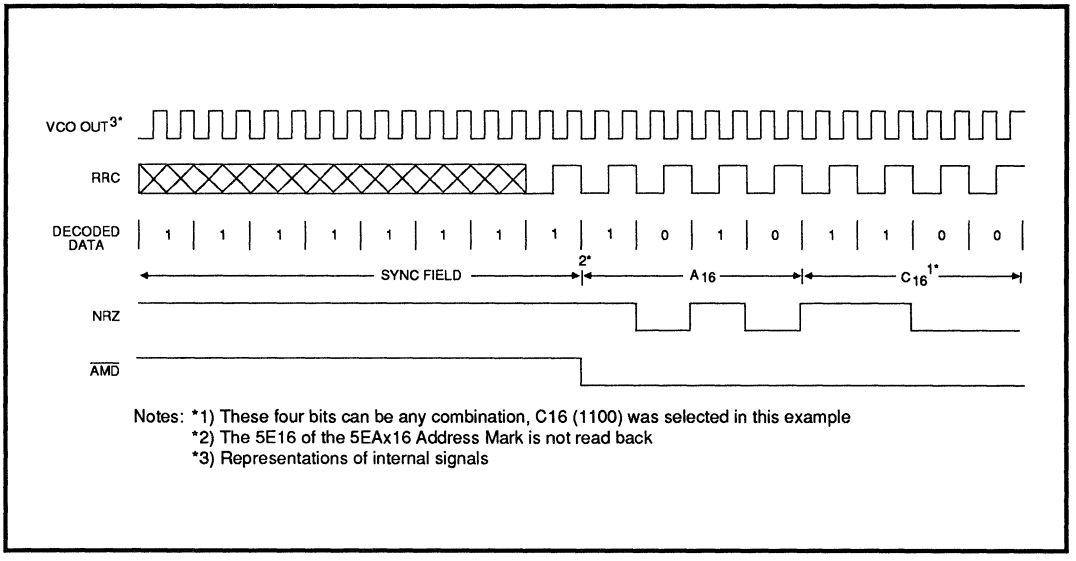


FIGURE 5: Address Mark Detection and NRZ Output Waveform

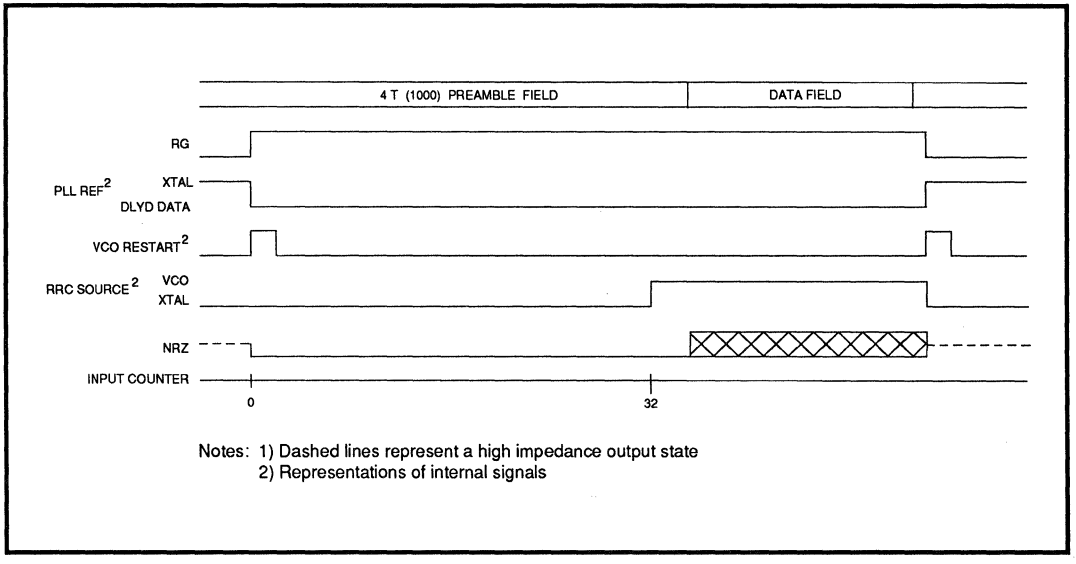


FIGURE 6: Hard Sector Mode Timing Diagram

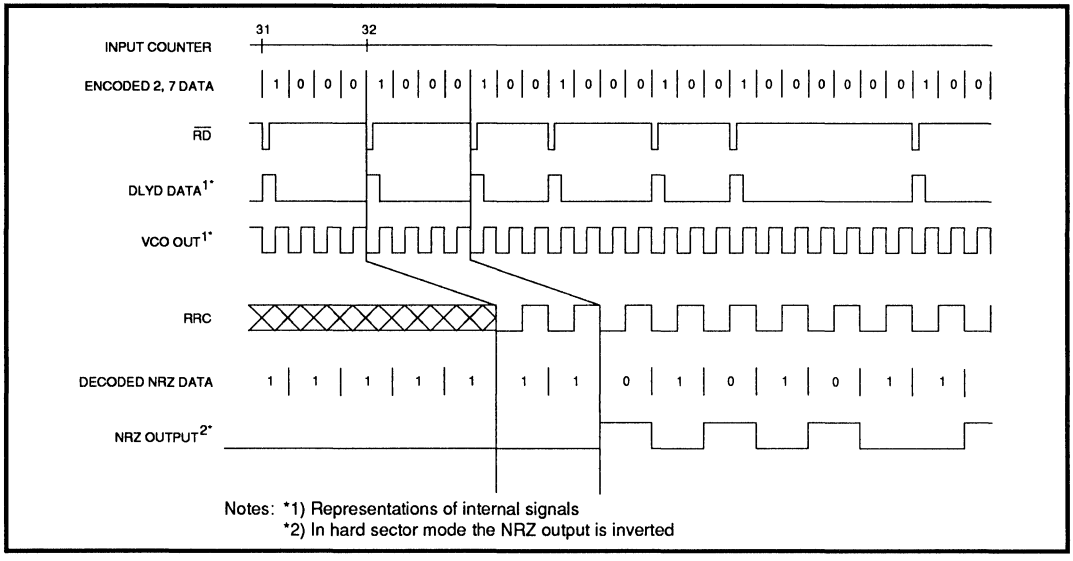


FIGURE 7: Hard Sector Mode Decode Timing

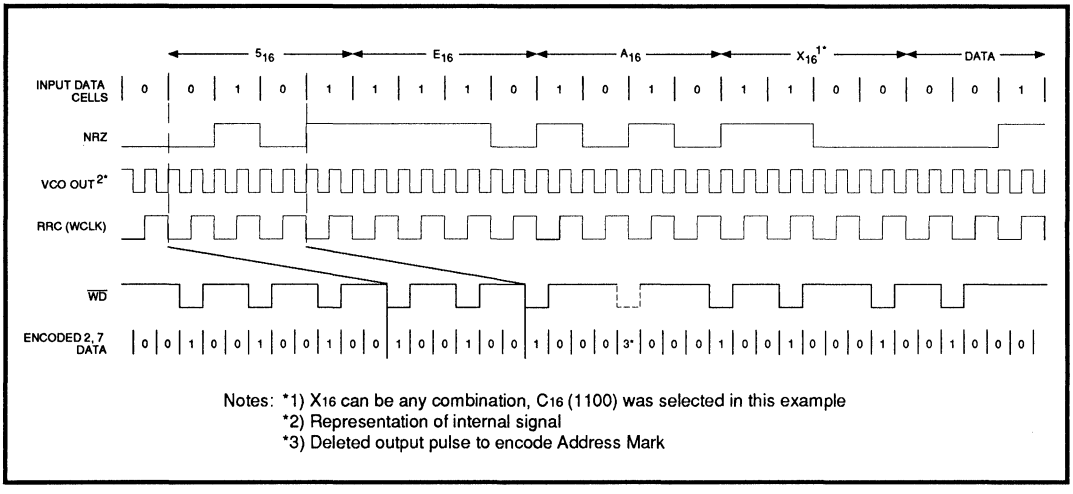


FIGURE 8: Write Address Mark Generation

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may permanently damage the device.

PARAMETER	RATINGS	UNIT
Storage Temperature	-65 to +150	° C
Ambient Operating Temperature, Ta	0 to +70	° C
Junction Operating Temperature, Tj	0 to +130	° C
Supply Voltage, VCC	-0.5 to 7	Vdc
Voltage Applied to Logic inputs	-0.5 to VCC +0.5	Vdc
Maximum Power Dissipation	950	mW

DC ELECTRICAL CHARACTERISTICS - unless otherwise specified, 4.75V < VCC < 5.25V, Ta = 0°C to 70°C, 7.5 MHz < 1/TORC < 10 MHz, 15 MHz < 1/TVCO < 20 MHz

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
TTL Inputs:					
VIH, High Level Input Voltage		2.0			V
VIL, Low Level Input Voltage				0.8	V
IIH, High Level Input Current	VIH = 2.7V			20	µA
IIL, Low Level Input Current	VIL = 0.4V			-0.36	mA
TTL Outputs:					
VOH, High Level Output Voltage	IOH = -400 µA	2.4			V
VOL, Low Level Output Voltage	IOL = 4 mA			0.5	V
Test Point Outputs: $\overline{DRD}$, VCO CLK (See Figure 12)					
VOH, High Level Ouput Voltage	RL= 130Ω to VPD, 200Ω to DGND		VPD-1.0		V
VOL, Low Level Output Voltage	RL= 130Ω to VPD, 200Ω to DGND		VPD-1.75		V
ICC, Power Supply Current	All outputs open			180	mA

DYNAMIC CHARACTERISTICS AND TIMING

READ MODE (See Figure 9)

TRD, Read Data Pulse Width		20		TORC-40	ns
TFRD, Read Data Fall Time	2.0V to 0.8V, CL ≤ 15 pF			15	ns
TRRC, Read Clock Rise Time	0.8V to 2.0V, CL ≤ 15 pF			8	ns
TFRC, Read Clock Fall Time	2.0V to 0.8V, CL ≤ 15 pF			5	ns

READ MODE (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
TPNRZ, NRZ (out) Propagation Delay		-15		15	ns
TPAMD, $\overline{AMD}$ Propagation Delay		-15		15	ns
1/4 Cell + Retriggerable One-Shot Delay Stability	4.5V < VCC < 5.5V	-4		+4	%
1/4 Cell + Retriggerable One-Shot Delay*	TD = 6.14(RR +0.5) + 0.172 Rd (Cd +Cs)** RR = kΩ Rd = kΩ Cd = 68 pF to 100 pF	0.89 TD		1.11 TD	ns

* Excludes External Capacitor and Resistor Tolerances **Cs = Stray Capacitance

WRITE MODE (See Figure 10)

PARAMETER	CONDITIONS	MIN	MAX	UNIT
TWD, Write Data Pulse Width	CL ≤15 pF	(TOWC/2)-12-1.4TC	(TOWC/2) +12	ns
TFWD, Write Data Fall Time	2.0V to 0.8V, CL ≤ 15 pF		8	ns
TRWC Write Data Clock Rise Time	0.8V to 2.0V		10	ns
TFWC Write Data Clock Fall Time	2.0V to 0.8V		8	ns
TSNRZ, NRZ (in) Set Up Time		20		ns
THNRZ, NRZ (in) Hold Time		7		ns
TWDC Compensated Write Data Pulse Width	CL ≤ 15 pF	(TOWC/2)-2.4TC-12		ns
TE, TL Write Data Compensation Accuracy	TC = 0.15(Rp)(Cp + Cs) 2 kΩ ≤ Rp ≤ 3 kΩ, Cs = Stray Capacitance Cp = 15 pF to 36 pF	0.8 TC	1.2 TC	ns

DATA SYNCHRONIZATION

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
TVCO VCO Center Frequency Period	VCO IN = 2.7V TO = 1.23E - 11(RR +500) VCC = 5.0V	0.8 TO		1.2 TO	sec

DATA SYNCHRONIZATION (Cont.)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VCO Frequency	Dynamic Range	1.0V ≤ VCO IN ≤ VCC -0.6V VCC = 5.0V	±24		±40	%
KVCO	VCO Control Gain	ωo = 2π / TO 1.0V ≤ VCO IN ≤ VCC -0.6V	0.14 ωo		0.20 ωo	rad/s-V
KD	Phase Detector Gain	KD = 0.309 / (RR + 500) VCC = 5.0V	0.83 KD		1.17 KD	A/rad
*	KVCO x KD Product Accuracy		-28		+28	%
*	VCO Phase Restart Error			6		ns
	Decode Window Centering Accuracy				± (0.01 TORC + 2)	ns
	Decode Window		(TORC/2) -2			ns
TS1	Decode Window Time Shift Magnitude	TS1 = 0.015 TORC		TS1		sec
TS2	Decode Window Time Shift Magnitude	TS2 = 0.06 TORC		TS2		sec
TS3	Decode Window Time Shift Magnitude	TS3 = 0.075 TORC		TS3		sec
TSA	Decode Window Time Shift Magnitude	$TSA = 0.125\ TORC\left(1 - \frac{680 + R}{1180 + R}\right)$ with: R in ohms		TSA		sec

* Not directlly testable – Design Characteristics

CONTROL CHARACTERISTICS (See figure 11)

TSWS, $\overline{WS0}$, $\overline{WS1}$, WSD Set Up Time		50			ns
THWS, $\overline{WS0}$, $\overline{WS1}$, WSD Hold Time		0			ns
RG, WG, SOFT/$\overline{HARD}$ Time Delay				100	ns

REFERENCE CLOCK CHARACTERISTICS

TXPW, Crystal Input Pulse Width	Min. Negative Pulse Width	19.23			ns
(Reference Oscillator See Figure 10)	Min. Positive Pulse Width	16			ns

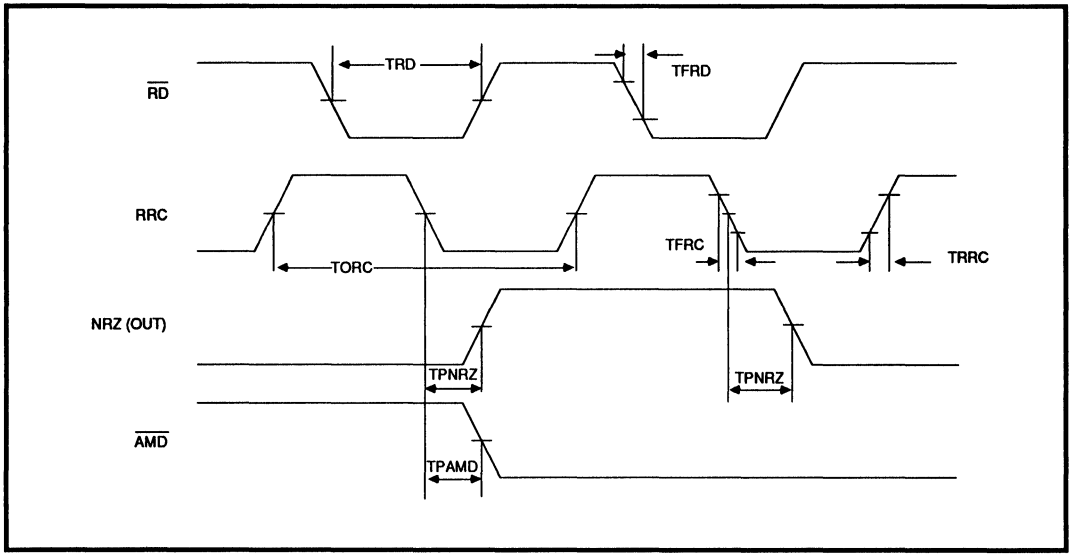


FIGURE 9: Read Timing

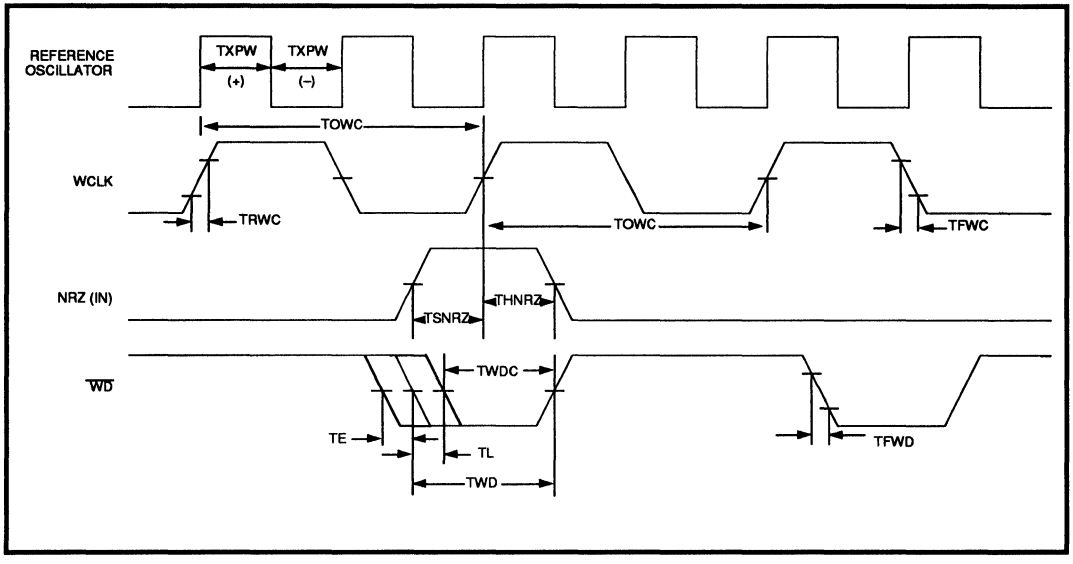


FIGURE 10: Write Timing

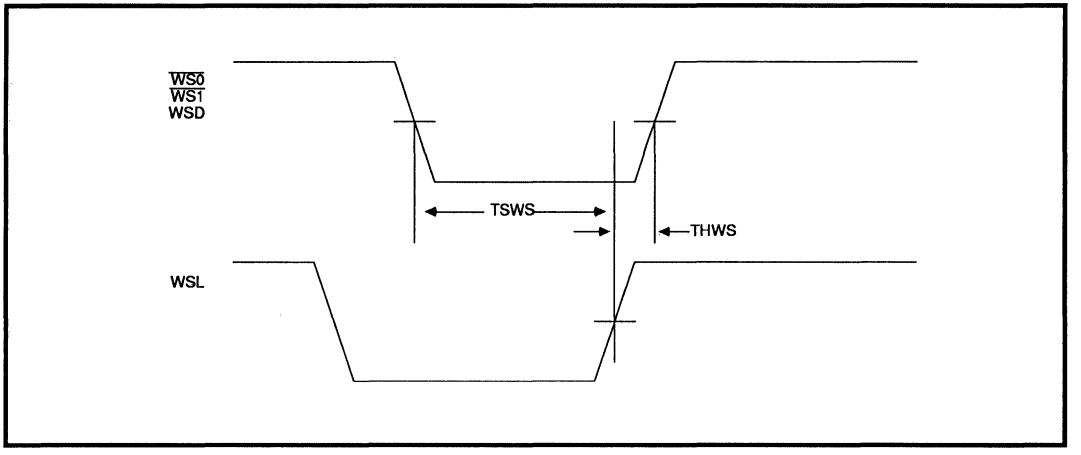


FIGURE 11: Control Timing

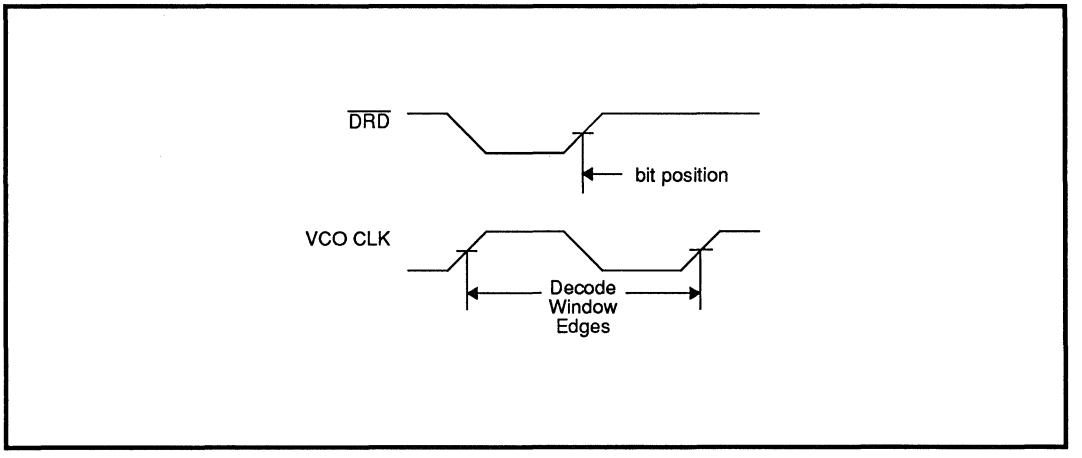


FIGURE 12: Test Point Timing

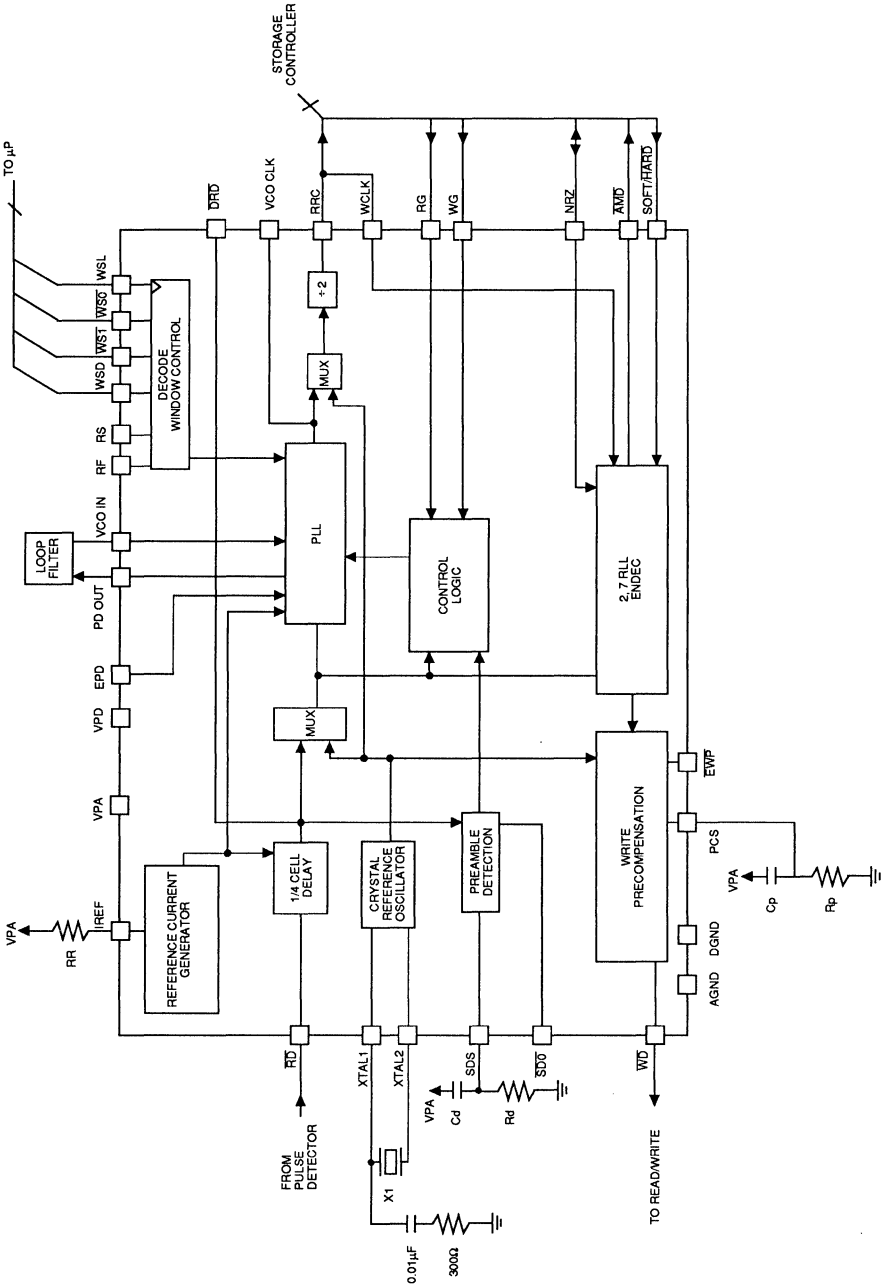
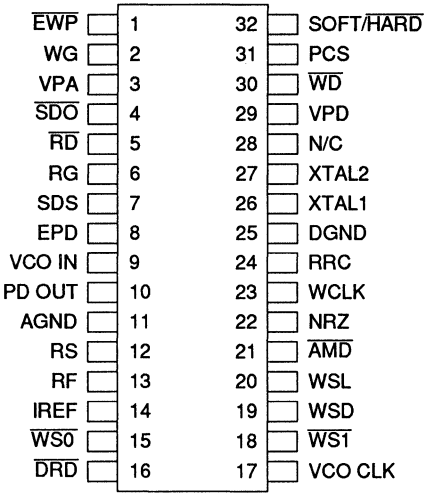


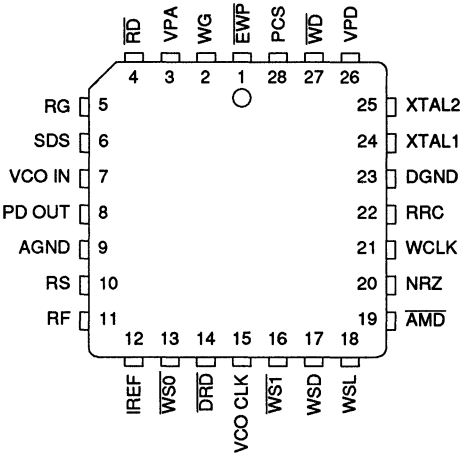
FIGURE 13: Typical SSI 32D535 Application

SSI 32D535
Data Synchronizer/ 2, 7 RLL ENDEC with Write Precompensation

PACKAGE PIN DESIGNATIONS
(Top View)



32-Lead SOW



28-Pin PLCC

Note: This package is bonded out for soft sector applications only. (SOFT/$\overline{\text{HARD}}$) pin internally pulled up). $\overline{\text{SDO}}$ and EPD are not available in this package.

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32D535 32-Pin Small Outline - Wide	32D535 - CW	32D535 - CW
SSI 32D535 28-Pin PLCC	32D535 - CH	32D535 - CH

Silicon Systems, Inc. 14351 Myford Road, Tustin, CA 92680, (714) 731-7110, FAX (714) 573-6914

silicon systems®
A TDK Group Company

SSI 32D5351A

Data Synchronizer/2, 7 RLL ENDEC w/ Write Precompensation

Preliminary Data

November 1991

DESCRIPTION

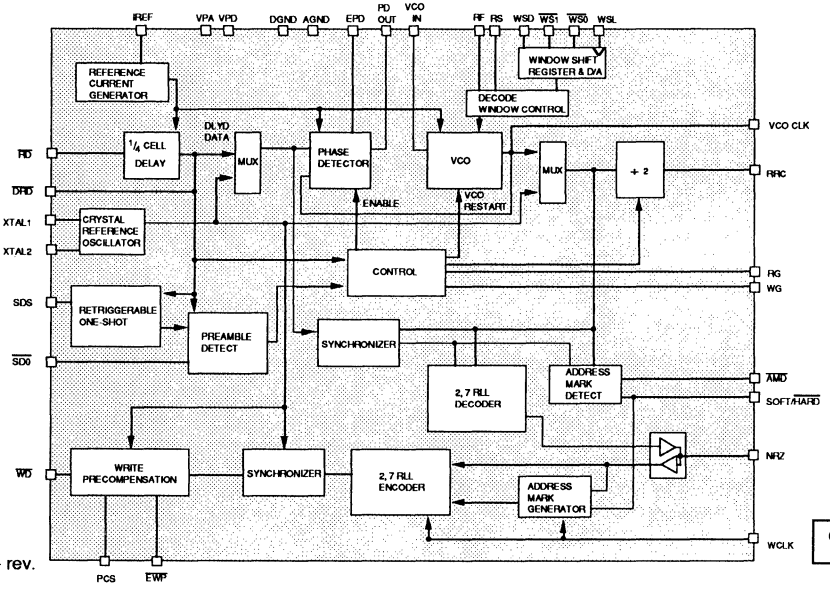
The SSI 32D5351A Data Separator provides data recovery, data encoding, and write precompensation for storage systems which employ a 2, 7 RLL encoding format. Data synchronization is performed with a fully integrated high performance PLL. An improved zero phase restart technique is used to minimize PLL acquisition time. The SSI 32D5351A has been optimized for operation at multiple data rates between 8 to 16 Mbit/s with multiple TTL clock schemes or the 32D4661 Time Base Generator. The VCO frequency setting elements are incorporated within the SSI 32D5351A for enhanced performance and reduced board space. Data rate is established with a single external programming resistor. The SSI 32D5351A utilizes an advanced bipolar process technology which affords precise decode window control without the requirement of an accurate 1/4 cell delay or external devices. To enhance disk drive testability, decode window symmetry control is available through a digital µP port and/or two analog pins. This feature can facilitate defect mapping, automatic calibration, systematic error cancellation, window margin testing, and error recovery. The SSI 32D5351A requires a single +5V power supply and is available in 32-pin SOW and 28-Pin PLCC packages.

FEATURES

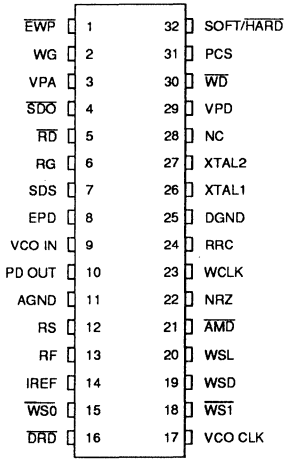
- **Data Synchronizer and 2, 7 RLL ENDEC**
- **Fast Acquisition Phase Locked Loop**
  - **Improved Zero Phase Restart Technique**
- **Write Precompensation**
- **8 - 13 Mbit/s Operation Programmed with a Single External Resistor**
- **Input Reference Clock Circuitry Optimized for use with Constant Density Recording Applications**
- **ESDI compatible (Hard Sector)**
- **Programmable Decode Window Symmetry via a µP Port and/or Analog Pins**
- **Fully Integrated Data Separator**
  - **No External Delay Lines or Active Devices Required**
- **Crystal Controlled Reference Oscillator**
- **Hard/Soft Sector Operation**
- **+5V Operation**
- **32-Pin SOW, 28-Pin PLCC Packages**

4

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

PIN DESCRIPTIONS

INPUT PINS

NAME	TYPE	DESCRIPTION
$\overline{RD}$	I	READ DATA: Encoded Read Data from the disk drive read channel, active low.
RG	I	READ GATE: Selects the PLL reference input and initiates the PLL synchronization sequence. A high level selects the $\overline{RD}$ input and enables the Read Mode/Address Mark Detection sequences. A low level selects the crystal reference oscillator. Pin RG has an internal resistor pull-up.
WG	I	WRITE GATE: Enables the write mode. Pin WG has an internal resistor pull-up.
WSL	I	WINDOW SYMMETRY LATCH: Used to latch the input window symmetry control bits WSD, $\overline{WS0}$ and $\overline{WS1}$ into the internal DAC. An active high level latches the input bits. Pin WSL has an internal resistor pull-up. If unused, connect this pin to ground.
WSD	I	WINDOW SYMMETRY DIRECTION: Controls the direction of the optional window symmetry shift. Pin WSD has an internal resistor pull-up. If unused, this pin can be left open.
$\overline{WS0}$	I	WINDOW SYMMETRY CONTROL BIT: A low level introduces a window shift of 1.5 % TORC (Read Reference Clock Period) in the direction established by WSD. Pin $\overline{WS0}$ has an internal resistor pull-up. If unused, this pin can be left open.
$\overline{WS1}$	I	WINDOW SYMMETRY CONTROL BIT: A low level introduces a window shift of 6% TORC (Read Reference Clock Period) in the direction established by WSD. A low level at both $\overline{WS0}$ and $\overline{WS1}$ will produce the sum of the two window shifts. Pin WS1 has an internal resistor pull-up. If unused, this pin can be left open.
SOFT/$\overline{HARD}$	I	SOFT/$\overline{HARD}$ SECTOR: Selects the address mark and the Preamble field patterns. A high level (Soft Sector) selects a 3T Preamble Field pattern and a non-violating 2, 7 address mark, N7V. A low level (Hard Sector) selects a 4T Preamble Field pattern and disables the address mark circuitry. Pin SOFT/$\overline{HARD}$ has an internal resistor pull-up.
WCLK	I	WRITE CLOCK: Write Clock input. Must be synchronous with the Write Data input on the NRZ Data Port. For small cable delays, WCLK may be connected directly to pin RRC (Read/Reference Clock).
EPD	I	ENABLE PHASE DETECTOR: A low level (Coast Mode) disables the phase detector and allows the VCO to coast. Pin EPD has an internal resistor pull up.
$\overline{EWP}$	I	ENABLE WRITE PRECOMPENSATION: A low level enables Write Precompensation. Pin $\overline{EWP}$ has an internal resistor pull-up.

PIN DESCRIPTIONS (Cont.)

OUTPUT PINS

NAME	TYPE	DESCRIPTION
$\overline{WD}$	O	WRITE DATA: Encoded write data output, active low.
RRC	O	READ/REFERENCE CLOCK: A multiplexed clock source used by the controller. In the read mode, this clock is the VCO frequency divided by two (1/TORC) and in the write mode it is the crystal reference frequency divided by two (1/TORO). No short clock pulses are generated during a mode change.
$\overline{AMD}$	O	ADDRESS MARK DETECT: In the soft sector Read Mode, a latched low level output indicates that an address mark has been detected. In non-Read modes $\overline{AMD}$ is configured as a high impedance output.
$\overline{SDO}$	O	SYNC DETECT OUTPUT: An active low output that indicates successful detection of the 3T Preamble sync field. THE SD0 pin is not a TTL level signal.
VCO CLK	O	VCO CLK: An open emitter VCO clock test point. Two external resistors are required to utilize this output, they can be removed during normal operaton for reduced power dissipation.
$\overline{DRD}$	O	DELAYED READ DATA: Test point. The positive edges of this open emitter output signal indicate the data bit position. The positive edges of the $\overline{DRD}$ and the VCO CLK signals can be used to estimate window centering. The time jitter of $\overline{DRD}$'s positive edge is an indication of media bit shift. Two external resistors are required to perform this test, they can be removed during normal operation for reduced power dissipation.

BIDIRECTIONAL PINS

NRZ	I/O	NRZ DATA PORT: Read Data output when RG is high and Write Data input when WG is high. In the idle mode NRZ is in a high impedance state.

ANALOG PINS

IREF	I	TIMING PROGRAM PIN: The VCO center frequency and the 1/4 Cell Delay are a function of the current sourced into pin IREF. The current is set by an external resistor, RR, connected from IREF to VPA.
PCS	I	PRECOMP SET: Used to set the magnitude of the Write Precompensation time shift via an external capacitor, Cp to VPA and an external resistor, Rp to AGND.
XTAL1, XTAL2	I	CRYSTAL OSCILLATOR CONNECTIONS: If a crystal oscillator is not desired, XTAL1 maybe driven by a TTL source* with XTAL2 open. The frequency must be at twice the data rate.
PD OUT	O	PHASE DETECTOR OUTPUT: Drives the Loop Filter input.
VCO IN	I	VCO CONTROL INPUT: Driven by the Loop Filter output.

* See Clock Characteristics

4

PIN DESCRIPTIONS (Cont.)

ANALOG PINS (Cont.)

NAME	TYPE	DESCRIPTION
SDS	I	SYNC DETECT SET: Used to program the sync detect retriggerable one-shot timing with an external R-C network. Connect the capacitor, Cd, to VPA and the resistor, Rd, to AGND.
RF, RS	I	WINDOW SYMMETRY ADJUST PINS: Provides analog control over the decode window symmetry; typically used to null out any window symmetry offset. A resistor connected from either RF or RS to AGND will provide magnitude and direction control. They can be used in conjunction with the digital control port WSD, $\overline{WS0}$, $\overline{WS1}$.

POWER

DGND, AGND	I	DIGITAL AND ANALOG GROUND
VPA	I	ANALOG +5V
VPD	I	DIGITAL +5V

OPERATION

The SSI 32D5351A is designed to perform data recovery and data encoding in rotating memory systems which utilize a 2, 7 RLL encoding format. In the Read Mode the SSI 32D5351A performs Data Synchronization, Sync Field Search and Detect, Address Mark Detect and Data Decoding. In the Write Mode, the SSI 32D5351A converts NRZ data into the 2,7 RLL format described in Table 1, performs write precompensation, generates the Preamble Field, and inserts Address Marks as requested. The interface electronics and architecture of the SSI 32D5351A have been optimized for use as a companion device to the SSI 32C452A or AIC 010 controllers.

The SSI 32D5351A can operate with data rates ranging from 8 to 16 Mbit/s. This data rate is established by a single 1% external resistor, RR, connected from pin IREF to VPA. This resistor establishes a reference current which sets the VCO center frequency, the phase detector gain, and the 1/4 cell delay. The value of this resistor is given by:

$$RR = \frac{76}{DR} - 1.75\ (k\Omega)$$

where: DR = Data Rate in Mbit/s.
$4.1\ k\Omega < RR < 7.75\ k\Omega$

An internal crystal reference oscillator, operating at twice the data rate, generates the standby reference for the PLL. A series resonant crystal between XTAL1 and XTAL2 should be selected at twice the Data Rate. If a crystal oscillator is not desired, then an external TTL compatible reference may be applied to XTAL1, leaving XTAL2 open.

The SSI 32D5351A employs a Dual Mode Phase Detector; Harmonic in the Read Mode and Non-Harmonic in Write and Idle Modes. In the Read Mode the Harmonic Phase Detector updates the PLL with each occurrence of a DLYD DATA pulse. In the Write and Idle Modes the Non-Harmonic Phase Detector is continuously enabled, thus maintaining both phase and frequency lock. By acquiring both phase and frequency lock to the crystal reference oscillator and utilizing an improved zero phase restart technique, false lock to DLYD DATA is eliminated.

The phase detector incorporates a charge pump in order to drive the loop filter directly. The polarity and width of the output current pulses correspond to the direction and magnitude of the phase error. Figure 1 depicts the average output current as a function of the input phase error (relative to the VCO period).

The READ GATE (RG), and WRITE GATE (WG), inputs control the device mode as described in Table 2. RG is an asynchronous input and may be initiated or terminated at any position on the disk. WG is also an asynchronous input, but should not be terminated prior to the last output Write Data pulse.

4

READ OPERATION

The Data Synchronizer utilizes a fully integrated fast acquisition PLL to accurately develop the decode window. Read Gate, RG, initiates the PLL locking sequence and selects the PLL reference input; a high level (Read Mode) selects the $\overline{RD}$ input and a low level selects the crystal reference oscillator.

In the Read Mode the rising edge of DLYD DATA enables the Phase Detector while the falling edge is phase compared to the rising edge of the VCO. As depicted in Figure 2, DLYD DATA is a 1/4 cell wide (TVCO/2) pulse whose leading edge is defined by the leading edge of $\overline{RD}$. An accurate and symmetrical decode window is developed from the VCO clock. The decode window is generated from the falling edges of the VCO clock. By utilizing a fully integrated symmetrical VCO running at twice the data rate, the decode window is insured to be accurate and centered symmetrically about the falling edges of DLYD DATA. The accuracy of the 1/4 cell delay only affects the retrace angle of the phase detector and does not influence the accuracy of the decode window.

Shifting the symmetry of the VCO clock effectively shifts the relative position of the DLYD DATA pulse within the decode window. This powerful capability easily facilitates defect mappings, automatic calibration, window margin testing, error recovery, and systematic error cancellation. For enhanced disk drive testability and error recovery, decode window control is provided via a µP port (WSL, WSD, $\overline{WS0}$, $\overline{WS1}$) as described in Table 3. In applications not utilizing this feature, WSL should be connected to ground, while WSD, $\overline{WS0}$, and $\overline{WS1}$ can be left open.

Window shifts in the range of ±1.5% to ±7.5% of TORC are easily programmed by latching the appropriate control word into the Window Shift Register with the WSL pin. Shifts in the positive or negative directions result in early or late decode windows respectively, as depicted in Figure 3. Additionally, for small systematic error cancellation, a resistor, R, connected from either RS (Early) or RF (Late) to ground will provide analog control over the decode window. The magnitude of this shift, TSA is determined by:

$$TSA = 0.125\ TORC\left(1 - \frac{680 + R}{1180 + R}\right)$$

where: R is in ohms

Pins RF and RS are intended to be used as a trim and should be restricted to ±1.5% window shifts. They can be used in conjunction with the digital control port.

The VCO CLK and $\overline{DRD}$ outputs can be used to estimate window centering and data bit shift. The rising edges of VCO CLK indicate the data detection window edges. The rising edge of $\overline{DRD}$ indicates the data bit position relative to the decode window. Two external resistors are required during such testing. A pull-up resistor of 130Ω should be connected to VPD, while a pull-down resistor of 200Ω should be connected to DGND. The resistors can be removed during normal operation to reduce power dissipation.

In Non-Read Modes, the PLL is locked to the crystal reference oscillator. This forces the VCO to run at a frequency which is very close to that required for tracking actual data and thus minimizes the associated frequency step during acquisition. When the reference input to the PLL is switched, the VCO is stopped momentarily, then restarted in an accurate phase alignment with the next PLL reference input pulse, and the VCO clock divider is reset. By minimizing the phase alignment in this manner (phase error ≤ 0.5 rads), the acquisition time is substantially reduced.

The SSI 32D5351A provides two sync modes for controlling the PLL locking sequence; Soft Sector and Hard Sector.

SOFT SECTOR MODE

The Soft Sector Mode activates the Preamble Search and Address Mark detection circuitry. As depicted in Figure 4, when RG transitions high, the counter is reset and the SSI 32D5351A requires 10 high to low transitions (Preamble '1' bits) before switching the reference input to the PLL, 48 high to low transitions before switching the Read Reference Clock to the VCO clock divided by two and activating the Address Mark Detect circuitry; then it must detect the Address Mark prior to 80 high to low transitions in order to enter the Read Mode. This sequence repeats after 95 input '1' bits until the read mode is successfully entered or until RG is cancelled.

When RG transitions high, the following PLL locking sequence begins:

a) **PREAMBLE SEARCH:**

The 3T detect circuitry initiates the PLL locking sequence once it has detected 10 consecutive '100' bit groups from the 3T preamble field. The 3T detect timing is set by the sum of the 1/4 cell delay and the retriggerable one-shot delay. The 1/4 cell timing capacitor is included on-chip and its timing is externally set by resistor RR. The retriggerable one-shot timing is externally set by resistor Rd and capacitor Cd. The sum of their delays is set to 3.5 bit cell times. Therefore, a continuous stream of input pulses with a 3T bit cell time pulse rate keeps the one-shot reset, and a 4T or longer bit cell time input period allows the one-shot to time out producing a 4T detect pulse. The 4T detect pulse resets the Input Counter and the search is started over.

b) **PLL ACQUISITION:**

Once 10 consecutive '100' bit groups are detected, the reference input to the PLL is switched from the crystal reference oscillator to the DLYD DATA, the VCO is phase reset to the next DLYD DATA pulse, and PLL acquisition begins. When an additional 38 '100' bit groups are detected, the Read Reference Clock output (RRC) is switched to the VCO clock divided by 2, the 4T Detect circuitry is inhibited, and the Address Mark Detection

circuitry is enabled. If a 4T detect pulse occurs before 48 Preamble '1' bits are detected, then the PLL is locked back to the crystal reference oscillator, the RRC output is switched to the crystal reference oscillator divided by 2, the Input Counter reset, and the sequence is re-started. No short duration glitches will occur at the RRC output during this switching.

c) **ADDRESS MARK DETECTION:**

The circuit searches for the occurrence of the $5EAx_{16}$ Address Mark. If an Address Mark is detected prior to the Input Counter reaching count 80, the correct phase of the RRC is ensured by resetting the n/2 divider, the $\overline{AMD}$ output is latched low, the PLL training sequence is terminated, and the Read Mode is entered allowing the data field to be read. If the Input Counter reaches count 80 before the Address Mark is detected, the PLL is locked back to the crystal reference oscillator, the RRC output is switched to the crystal reference oscillator divided by 2, and the PLL training sequence is restarted when the Input Counter reaches count 96. Figure 5 depicts the Address Mark detection sequence.

HARD SECTOR MODE

In the Hard Sector mode (SOFT/$\overline{HARD}$ = 0) the SSI 32D5351A utilizes a 4T (1000) Preamble Field and disables the Preamble Search and Address Mark detection circuitry. It allows the PLL to be controlled directly by RG for Hard Sector format operation. With the absence of an Address Mark, the 4T Preamble Field is utilized to properly set the bit cell alignment boundaries for proper decoding.

When RG transitions high, as depicted in Figure 6, reference input to the PLL is switched from the crystal reference oscillator to DLYD DATA, the VCO is phase reset to the next DLYD DATA pulse, and the PLL acquisition begins. When 32 '1' Preamble bits are detected, the RRC output is switched to the VCO clock divided by 2, and the Read Mode is entered allowing the data field to be read.

In the Hard Sector mode, the NRZ output is inverted and will remain low until the data field is read, as shown in Figure 7. Since the Preamble Search circuitry is not utilized, the external one-shot timing components (Cd, Rd) are not required and the SDS pin can be left open.

WRITE OPERATION

In the Write Mode the SSI 32D5351A converts NRZ data from the controller into 2, 7 RLL formatted data for storage onto the disk. The SSI 32D5351A can operate with a soft or hard sectored disk drive. In the Soft Sector Mode, (SOFT/$\overline{HARD}$ = 1) the device generates a 3T Preamble Field and can insert a N7V Address Mark. The N7V Address Mark is a valid 2, 7 RLL pattern which is not contained in the code set. In the Hard Sector Mode, (SOFT/$\overline{HARD}$ = 0) the device generates a 4T Preamble Field and no Address Mark. Serial NRZ data is clocked into the SSI 32D5351A and latched on defined cell boundaries. The NRZ input data must be synchronous with the rising edges of the WCLK input. The WCLK input is a feature provided for operation in an ESDI application to compensate for large cable delays. In a SCSI or ST506 operation, WCLK is connected directly to the RRC output.

Write precompensation circuitry is provided to compensate for media bit shift caused by intersymbol interference. The SSI 32D5351A recognizes specific write data patterns and can add or subtract delays in the time position of write data bits to counteract the read back bit shift. The magnitude of the time shift, TPC, is determined by an external R-C network on the PCS pin given by:

$$TPC = 0.15\ (Rp)(Cp + Cs)$$
$$Cp = 15 \text{ to } 36\ pF$$
$$Rp = 1k \text{ to } 3\ k\Omega$$
$$Cs = \text{stray capacitance}$$

When the ENABLE WRITE PRECOMP, $\overline{EWP}$, input is low the SSI 32D5351A performs write precompensation according to the algorithm outlined in Table 4.

SOFT SECTOR MODE

In the Soft Sector Mode, when WRITE GATE (WG), transitions high and the NRZ input is held low, the SSI 32D5351A automatically generates the 3T (100) Preamble Field at the WRITE DATA ($\overline{WD}$), output. The 3T Preamble Field will continue to be generated until the first low to high transition on the NRZ line. As shown in Figure 8, the first low to high transition occurs with the second bit '1' of the 5_{16} (0101) in the $5EAx_{16}$ Address Mark generation pattern. To generate the Address Mark, the SSI 32D5351A automatically changes the '1' in the eleventh position (see note 3) of the 2, 7 RLL encoded sequence, to a '0'. This generates a pattern of seven zero's followed by two zero's. This unique pattern satisfies the 2, 7 RLL constraints, but will never occur during a normal encoding sequence. The x_{16} of the $5EAx_{16}$ Address Mark generation pattern can be selected, a 'C_{16}' (1100) was utilized in this example.

HARD SECTOR MODE

In the Hard Sector Mode, when WG goes high and the NRZ input is held low, the SSI 32D5351A automatically generates the 4T (1000) Preamble Field at the WRITE DATA, $\overline{WD}$, output. Note that in the Hard Sector mode, the NRZ input is inverted, therefore a constant low is equivalent to an '11 . . .' input which generates the 4T '1000 . . . ' Preamble Field. The 4T Preamble Field will be generated between the time WG goes high and the first low to high transition on the NRZ line. The 32D5351A requires a minimum of 32 4T (1000) bit groups prior to the data field.

NRZ	2, 7 RLL
10	0100
11	1000
000	000100
010	100100
011	001000
0010	00100100
0011	00001000

TABLE 1: 2, 7 RLL Code Set

WG	RG	MODE
0	0	IDLE
0	1	READ
1	0	WRITE
1	1	ILLEGAL

TABLE 2: Mode Control

Ts, NOMINAL WINDOW SHIFT	WSD	$\overline{WS1}$	$\overline{WS0}$
+TS3	0	0	0
+TS2	0	0	1
+TS1	0	1	0
0	0	1	1
-TS3	1	0	0
-TS2	1	0	1
-TS1	1	1	0
0	1	1	1

TABLE 3 : Decode Window Symmetry Control

ENCODED 2, 7 RLL DATA PATTERN							
BIT n - 3	BIT n - 2	BIT n - 1	BIT n	BIT n + 1	BIT n + 2	BIT n + 3	COMPENSATION BIT n
0	0	0	1	0	0	0	none
1	0	0	1	0	0	1	none
1	0	0	1	0	0	0	early
0	0	0	1	0	0	1	late

TABLE 4 : Write Precompensatiom Algorithm

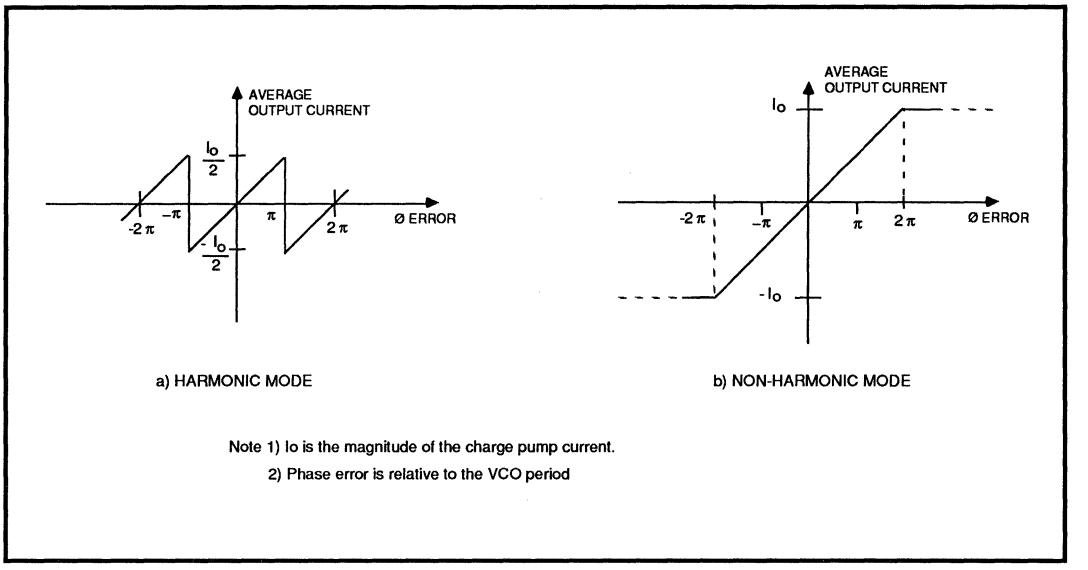


FIGURE 1: Phase Detector Transfer Funtion

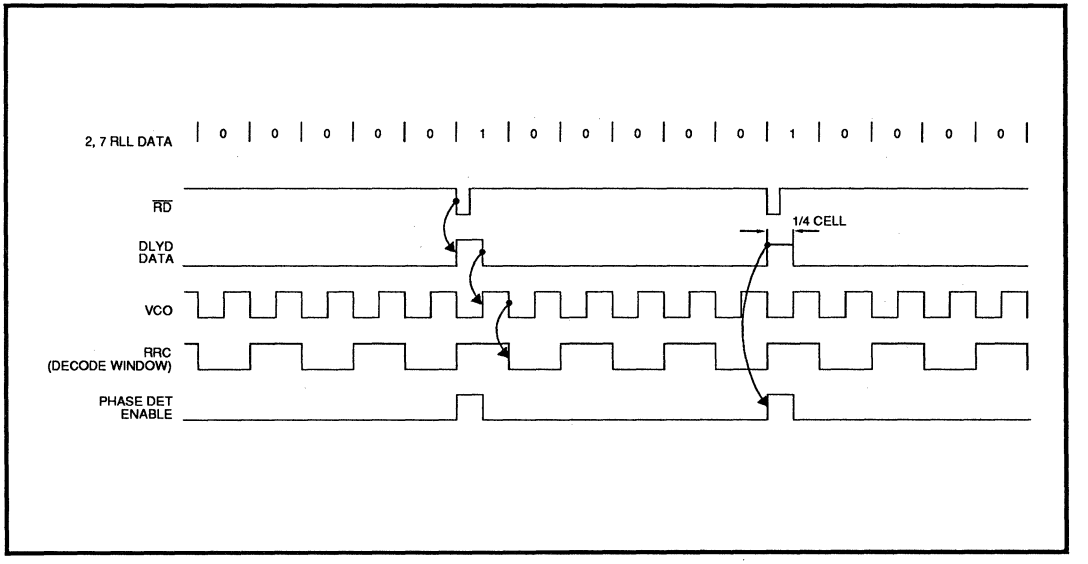


FIGURE 2: Data Synchronization Waveform Diagram

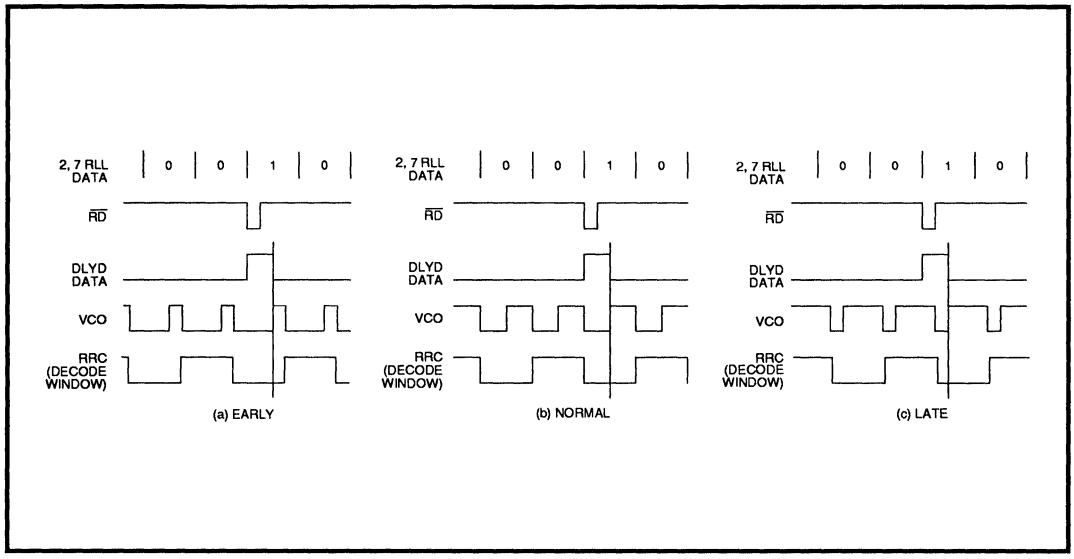


FIGURE 3: Decode Window

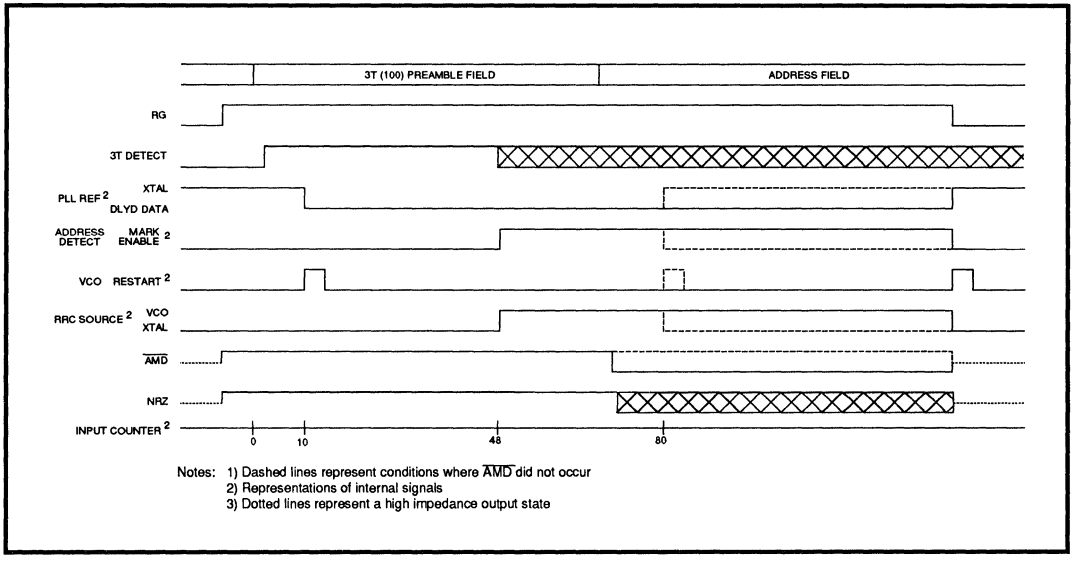


FIGURE 4: Soft Sector Mode Timing Diagram

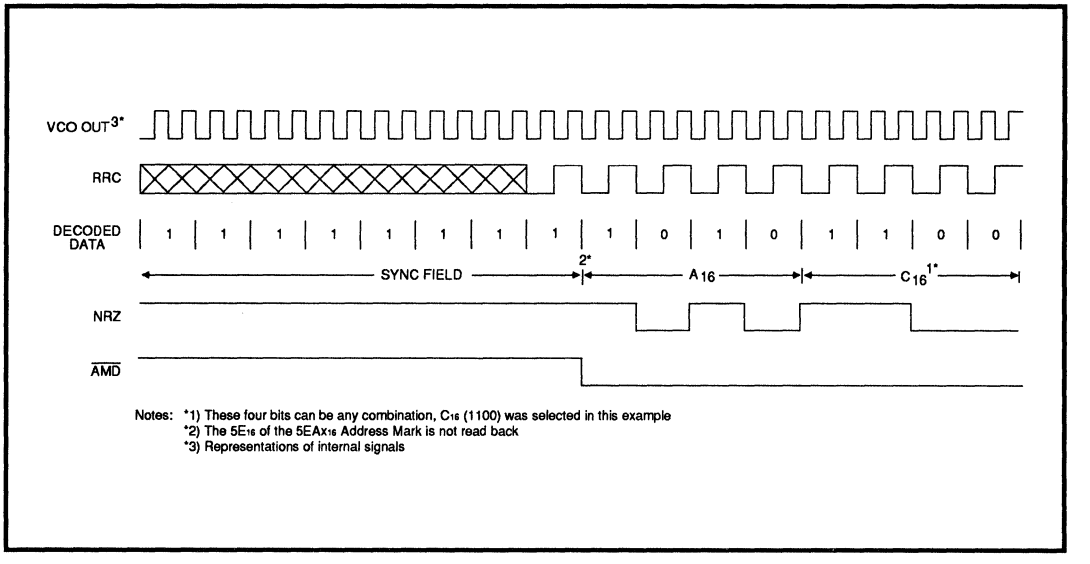


FIGURE 5: Address Mark Detection and NRZ Output Waveform

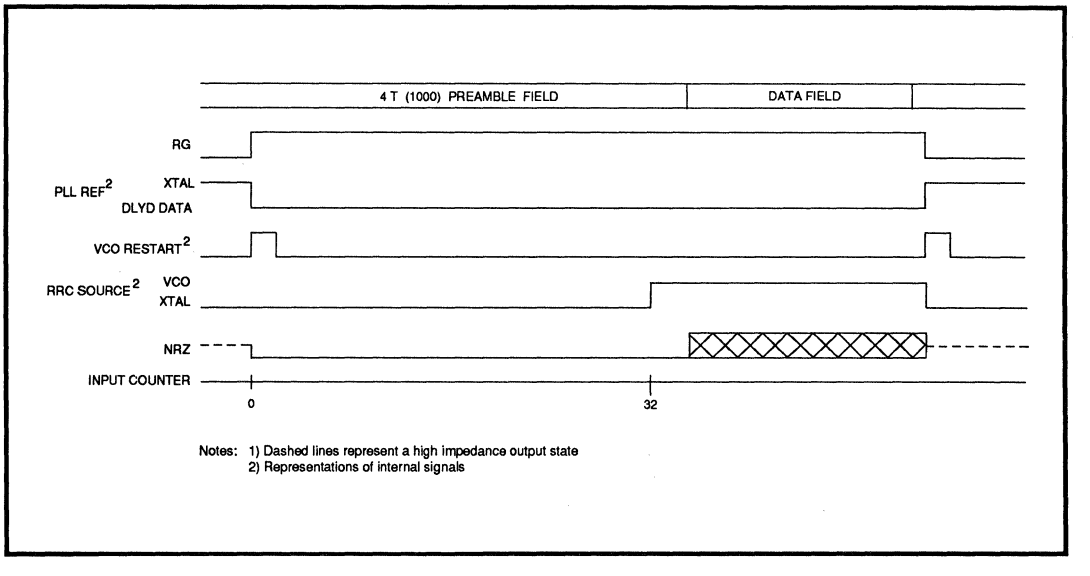


FIGURE 6: Hard Sector Mode Timing Diagram

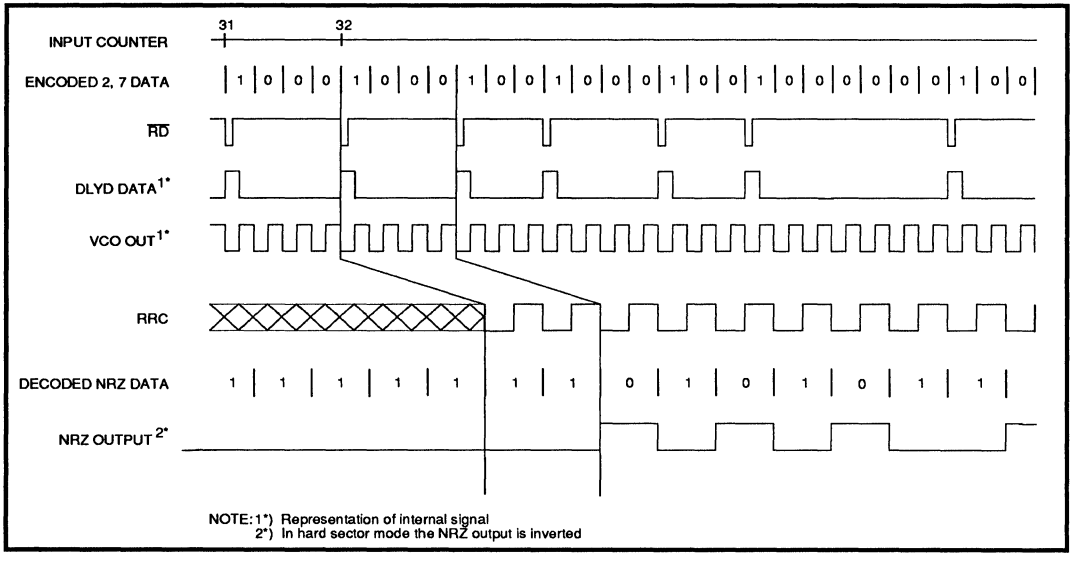


FIGURE 7: Hard Sector Mode Decode Timing

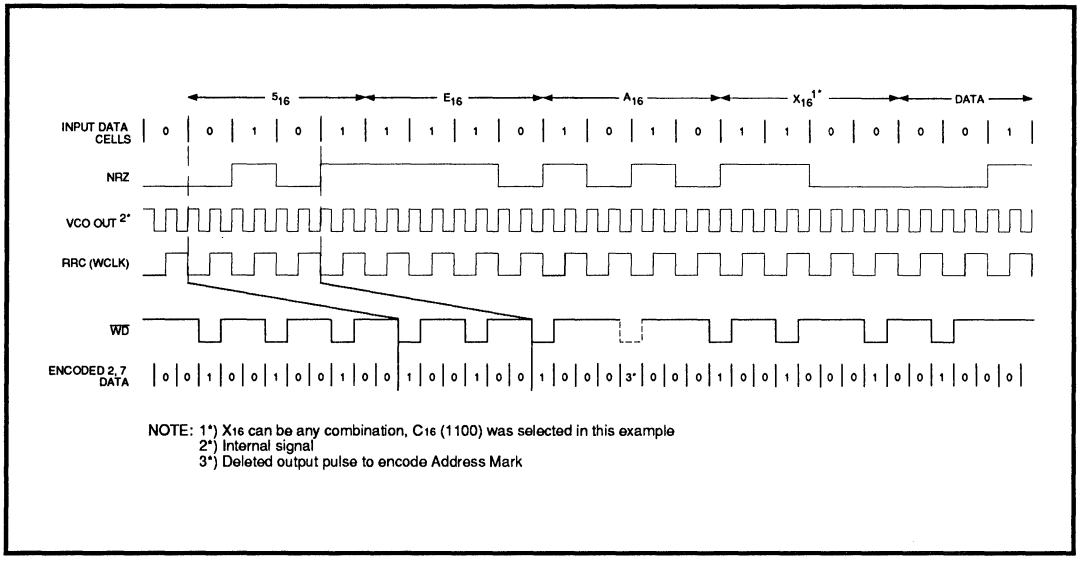


FIGURE 8: Write Address Mark Generation

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATINGS	UNIT
Storage Temperature	-65 to +150	° C
Ambient Operating Temperature, Ta	0 to +70	° C
Junction Operating Temperature, Tj	0 to +130	° C
Supply Voltage, VCC	-0.5 to 7	Vdc
Voltage Applied to Logic inputs	-0.5 to VCC +0.5	Vdc
Maximum Power Dissipation	950	mW

DC ELECTRICAL CHARACTERISTICS - unless otherwise specified, 4.75V < VCC < 5.25V, Ta = 0°C to 70°C, 8 MHz < 1/TORC < 16 MHz, 16 MHz < 1/TVCO < 32 MHz

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
TTL Inputs:					
VIH, High Level Input Voltage		2.0			V
VIHX, XTAL1 High Level Input Voltage	External Reference Clock	2.4			V
VIL, Low Level Input Voltage				0.8	V
IIH, High Level Input Current	VIH = 2.7V			20	µA
IIL, Low Level Input Current	VIL = 0.4V			-0.36	mA
TTL Outputs:					
VOH, High Level Output Voltage	IOH = -400 µA	2.4			V
VOL, Low Level Output Voltage	IOL = 4 mA			0.5	V
Test Point Outputs: $\overline{DRD}$, VCO CLK (See Figure 12)					
VOH, High Level Ouput Voltage	RL= 130Ω to VPD, 200Ω to DGND		VPD-1.00		V
VOL, Low Level Output Voltage	RL= 130Ω to VPD, 200Ω to DGND		VPD-1.75		V
ICC, Power Supply Current	All outputs open			180	mA

DYNAMIC CHARACTERISTICS AND TIMING

READ MODE (See Figure 9)

TRD, Read Data Pulse Width*		20		TORC-40	ns
TFRD, Read Data Fall Time*	2.0V to 0.8V, CL ≤ 15 pF			15	ns
TRRC, Read Clock Rise Time	0.8V to 2.0V, CL ≤ 15 pF			8	ns
TFRC, Read Clock Fall Time	2.0V to 0.8V, CL ≤ 15 pF			5	ns
TRNRZ, Read Data Output Rise Time	0.8V to 2.0V, CL ≤ 15 pF			8	ns
TFNRZ, Read Data Output Fall Time	2.0V to 0.8V, CL ≤ 15 pF			5	ns
TFNRZ, NRZ (out) Propagation Delay		-15		15	ns

* Input requirements for pulse detector

READ MODE (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
TPAMD, $\overline{AMD}$ Propagation Delay		-15		15	ns
1/4 Cell + Retriggerable One-Shot Delay Stability	4.75V < VCC < 5.25V	-4		+4	%
1/4 Cell + Retriggerable One-Shot Delay*	TD = 4.37 (RR +0.80) + 0.155 (Cd +Cs)** RR = kΩ Rd = kΩ Cd = 68 pF to 100 pF	0.89 TD		1.11 TD	ns
*Excludes External Capacitor and Resistor Tolerances, Tested Indirectly. ** Cs = Stray Capacitance [minimized]					

WRITE MODE (See Figure 10)

PARAMETER	CONDITIONS	MIN	MAX	UNIT
TWD, Write Data Pulse Width	CL ≤ 15 pF	(TOWC/2) -1.4 TPC - 12	(TOWC/2) +12	ns
TFWD, Write Data Fall Time	2.0V to 0.8V, CL ≤ 15 pF		8	ns
TRWC, Write Data* Clock Rise Time	0.8V to 2.0V		10	ns
TFWC Write Data* Clock Fall Time	2.0V to 0.8V		8	ns
TSNRZ, NRZ (in) Set Up Time		20		ns
THNRZ, NRZ (in) Hold Time		7		ns
TWDC, Compensated Write Data Pulse Width	CL ≤ 15 pF	(TOWC/2) -2.4 TPC-12		ns
TE, TL, Write Data Compensation Accuracy	TPC = 0.15(Rp)(Cp + Cs) Cp = 15 pF to 36 pF Cs = Stray Capacitance Rp = 1k to 3 kΩ	0.8T PC	1.2T PC	ns

DATA SYNCHRONIZATION

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
TVCO VCO Center Frequency Period	VCO IN = 2.7V TO = 6.59 (RR + 0.53) + 8 VCC = 5.0V; RR (kΩ)	0.83 TO		1.17 TO	ns
VCO Frequency Dynamic Range	1.0V ≤ VCO IN ≤ VCC -0.6V VCC = 5.0V	±24		±40	%

* Input requirements for write clock

DATA SYNCHRONIZATION (Continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
KVCO	VCO Control Gain	$\omega o = 2\pi$ / TVCO 1.0V ≤ VCO IN ≤ VCC -0.6V	0.14 ωo		0.235 ωo	rad/s V
KD	Phase Detector Gain	KD = 0.34 / (RR + 900) VCC = 5.0V	0.83 KD	1.0 KD	1.17 KD	A/rad
	*KVCO x KD Product Accuracy		-32		+32	%
	VCO Phase Restart Error			2		ns
	Decode Window Centering Accuracy				± (0.01 TORC + 2)	ns
	Decode Window Size		(TORC/2) -2			ns
TS1	Decode Window Time Shift Magnitude			0.015 TORC		ns
TS2	Decode Window Time Shift Magnitude			0.06 TORC		ns
TS3	Decode Window Time Shift Magnitude			0.075 TORC		ns
TSA	Decode Window Time Shift Magnitude	$TSA = 0.125\ TORC\left(1 - \frac{680+R}{1180+R}\right)$ with: R in ohms				ns

CONTROL CHARACTERISTICS (See Figure 11)

TSWS	$\overline{WS0}$, $\overline{WS1}$, WSD Set Up Time	50			ns
THWS	$\overline{WS0}$, $\overline{WS1}$, WSD Hold Time	0			ns
RG, WG, SOFT/$\overline{HARD}$ Time Delay				100	ns

REFERENCE CLOCK CHARACTERISTICS

TXPW, Reference Oscillator Pulse Width	Positive pulse width**	12			ns
	Negative pulse width**	12			ns

*not directly testable – design characteristics
**measured at 50% point

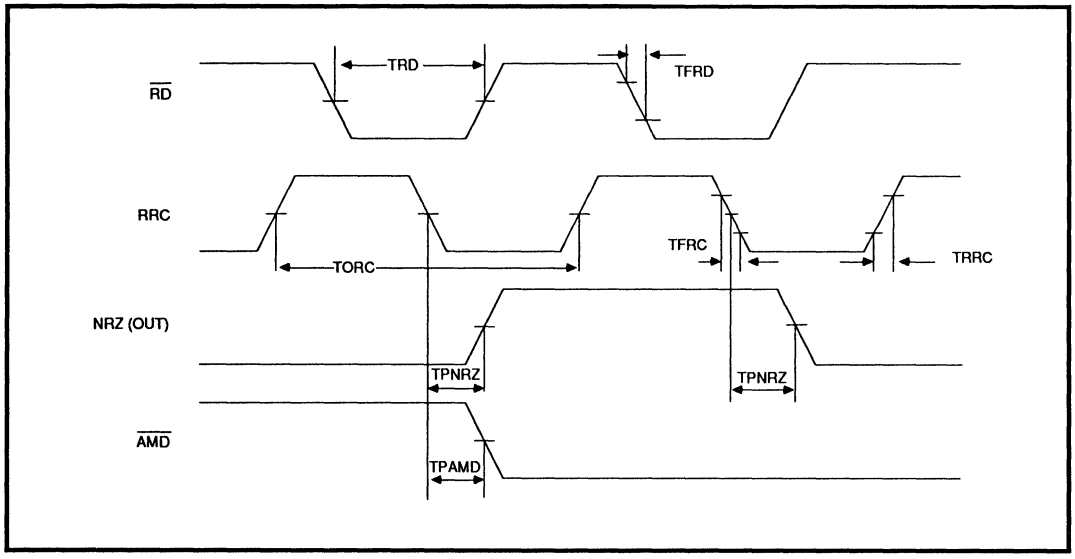


FIGURE 9: Read Timing

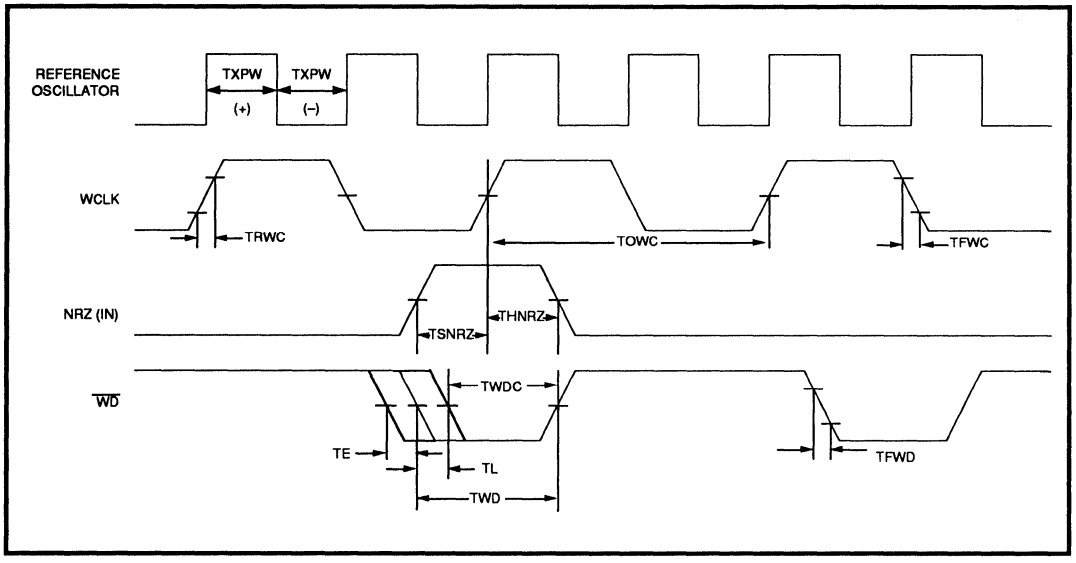


FIGURE 10: Write Timing

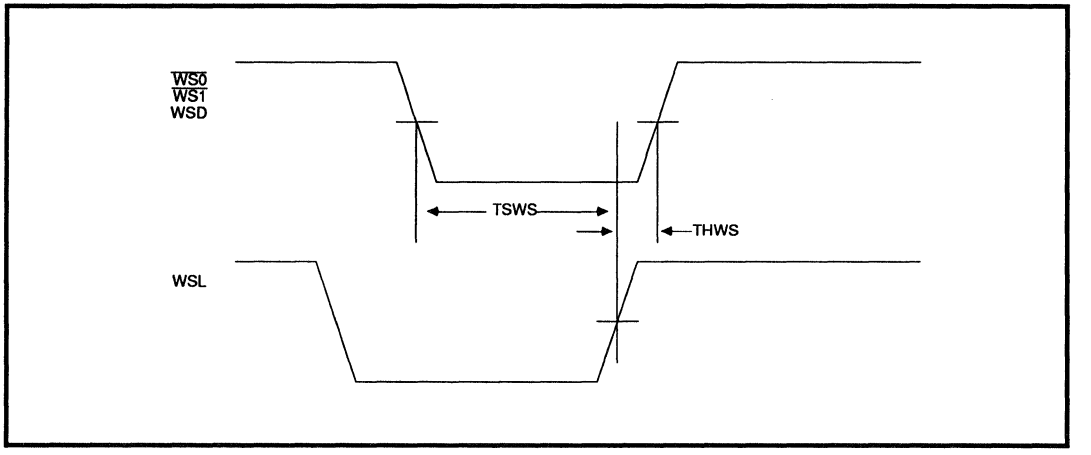


FIGURE 11: Control Timing

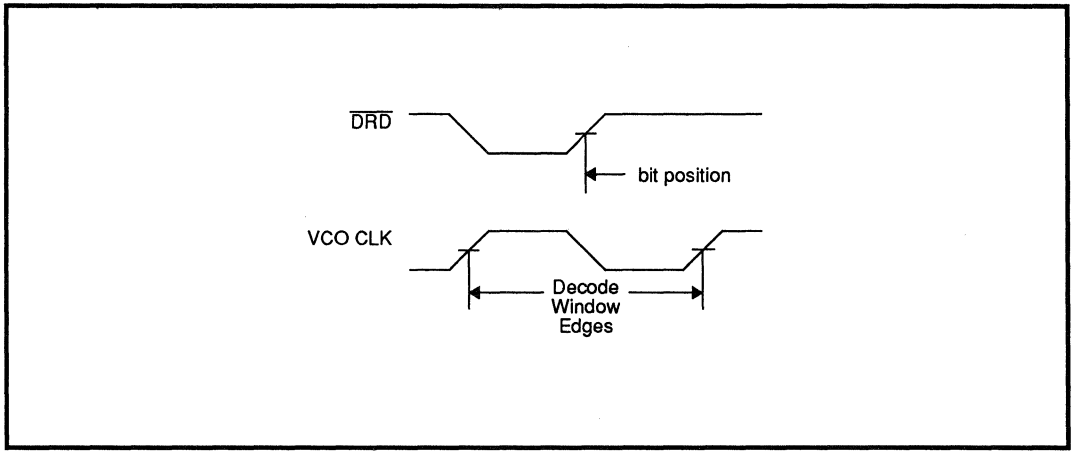


FIGURE 12: Test Point Timing

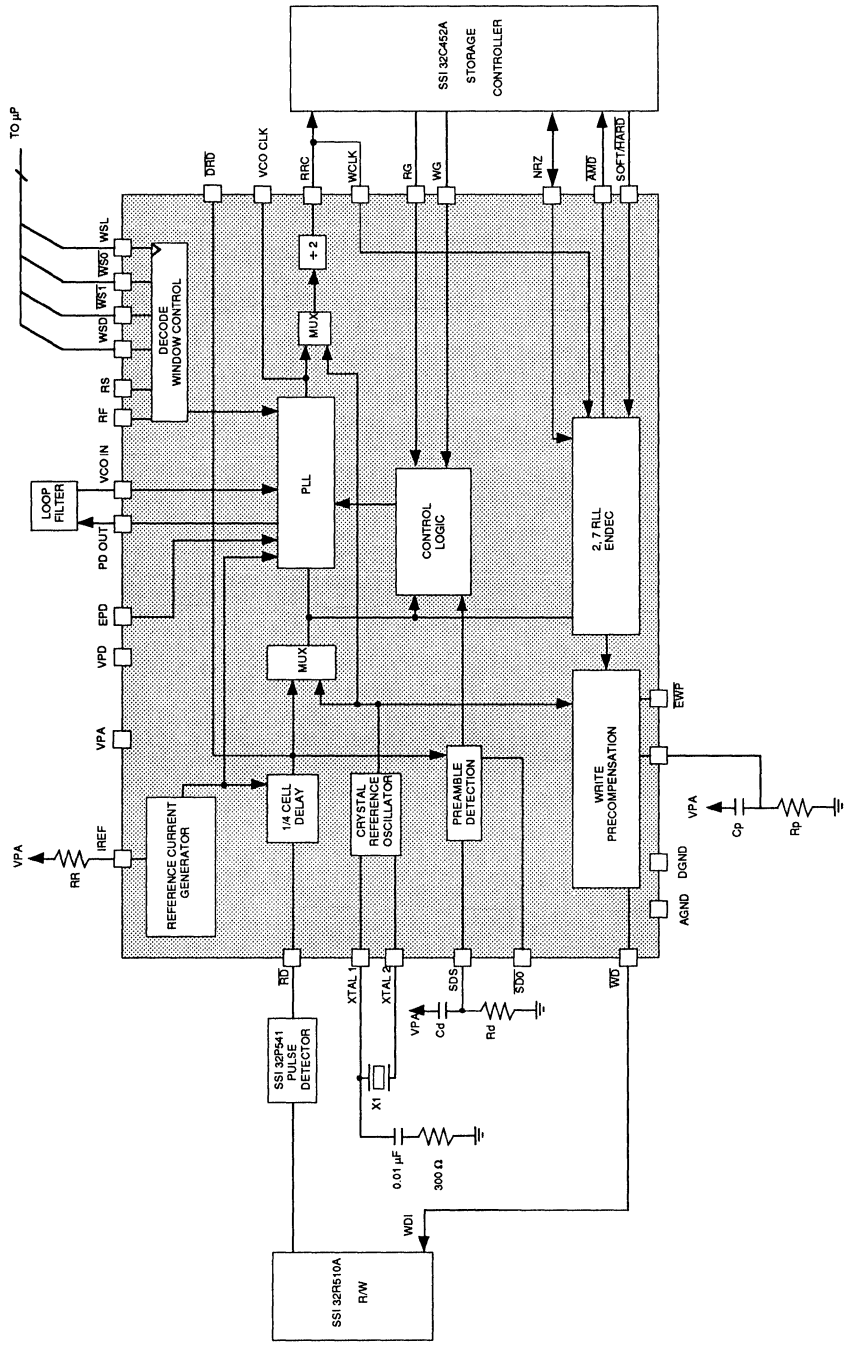
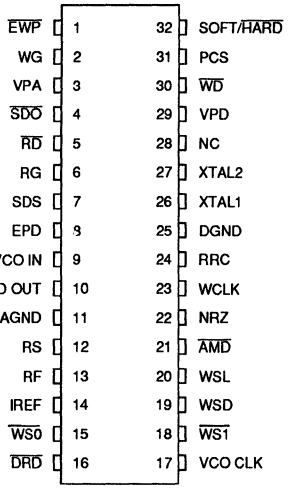


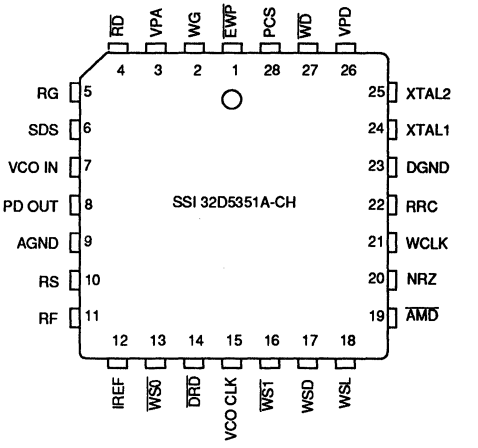
FIGURE 13: Typical SSI 32D5351A Application

SSI 32D5351A
Data Synchronizer/ 2, 7 RLL ENDEC with Write Precompensation

PACKAGE PIN DESIGNATIONS
(Top View)



32-Lead SOW



28-Pin PLCC

NOTE: Does not include the following pins which are available on the 32-Pin Packages
- SDO
- EPD
- SOFT/HARD (internally pulled up high)

So must be used in soft sector applications only.

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32D5351A 32-Pin Small Outline - Wide	32D5351A - CW	32D5351A - CW
SSI 32D5351A 28-Pin Plastic - Quad	32D5351A - CH	32D5351A - CH

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 731-7110, FAX (714) 573-6914

silicon systems®
A TDK Group Company

SSI 32D5362A
Data Synchronization/1, 7 RLL ENDEC with Write Precompensation

November 1991

4

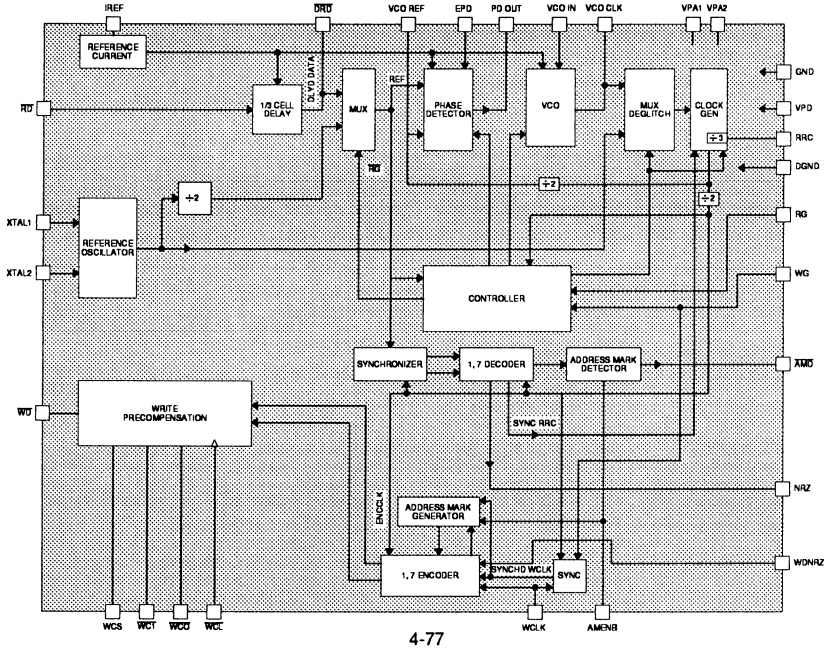
DESCRIPTION

The SSI 32D5362A Data Synchronizer/1, 7 RLL ENDEC provides data recovery and data encoding for storage systems which employ a 1, 7 RLL encoding format. Data synchronization is performed with a fully integrated high performance PLL. A zero phase restart technique is used to minimize PLL acquisition time. The SSI 32D5362A has been optimized for operation as a companion device to the SSI 32C9000 controller. The VCO frequency setting elements are incorporated within the SSI 32D5362A for enhanced performance and reduced board space. Data rate is established with a single external programming resistor. The SSI 32D5362A utilizes an advanced bipolar process technology which affords precise decode window control without the requirement of an accurate 1/3 cell delay or external devices. The SSI 32D5362A requires a single +5V supply.

FEATURES

- **Data Synchronizer and 1, 7 RLL ENDEC**
- **10 to 20 Mbit/s operation**
  - **Data Rate programmed with a single external resistor or current source**
- **Optimized for operation with the SSI 32C9000 controller.**
- **Fast acquisition phase lock loop**
  - **Zero phase restart technique**
- **Fully integrated data separator**
  - **No external delay lines or active devices required**
- **Programmable write precompensation**
- **Hard and soft sector operation**
- **Crystal controlled reference oscillator**
- **+5V operation**
- **28-pin PLCC package**
- **Test outputs - Allow drive margin testing with available test chip**

BLOCK DIAGRAM



SSI 32D5362A
Data Synchronization/1, 7 RLL ENDEC with Write Precompensation

OPERATION

The SSI 32D5362A is designed to perform data recovery and data encoding in rotating memory systems which utilize a 1,7 RLL encoding format. In the Read Mode the SSI32D5362A performs Data Synchronization, Sync Field Search and Detect, Address Mark Detect, and Data Decoding. In the Write Mode, the SSI 32D5362A converts NRZ data into the 1,7 RLL format described in Table 1, performs Write Precompensation, and inserts Address Marks as requested. The interface electronics and architecture of the SSI 32D5362A have been optimized for use as a companion device to the SSI 32C9000 controller.

The SSI 32D5362A can operate with data rates ranging from 10 to 20 Mbit/s. This data rate is established by a single 1% external resistor, RR, connected from pin IREF to VPA. This resistor establishes a reference current which sets the VCO center frequency, the phase detector gain, and the 1/3 cell delay. The value of this resistor is given by:

$$RR = \frac{92.6}{DR} - 2.3 (k\Omega)$$

where: DR = Data Rate in Mbit/s.

An internal crystal reference oscillator, operating at three times the data rate, generates the standby reference for the PLL. A series resonant crystal between XTAL1 and XTAL2 should be selected at three times the Data Rate. If a crystal oscillator is not desired, then an AC coupled ECL source may be applied to XTAL1, leaving XTAL2 open. A TTL compatible reference may also be used if suitably attenuated and AC coupled.

The SSI 32D5362A employs a Dual Mode Phase Detector; Harmonic in the Read Mode and Non Harmonic in Write and Idle Modes. In the Read Mode the Harmonic Phase Detector updates the PLL with each occurrence of a DYLD DATA pulse. In the Write and Idle modes the Non-Harmonic Phase Detector is continuously enabled, thus maintaining both phase and frequency lock. By acquiring both phase and frequency lock to the crystal reference oscillator and utilizing a zero phase restart technique, false lock to DLYD DATA is eliminated.

The phase detector incorporates a charge pump in order to drive the loop filter directly. The polarity and width of the output current pulses correspond to the direction and magnitude of the phase error.

The READ GATE (RG), and WRITE GATE (WG) inputs control the device mode.

RG is an asynchronous input and may be initiated or terminated at any position on the disk. WG is also an asynchronous input, but should not be terminated prior to the last output Write Data pulse.

READ OPERATION

The Data Synchronizer utilizes a fully integrated fast acquisition PLL to accurately develop the decode window. Read Gate, RG, initiates the PLL locking sequence and selects the PLL reference input; a high level (Read Mode) selects the $\overline{RD}$ input and a low level selects the crystal reference oscillator.

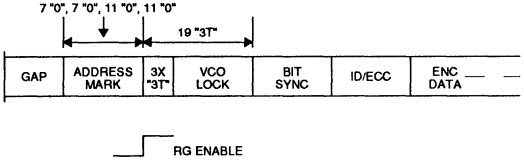
In the Read Mode the falling edge of $\overline{DRD}$ enables the Phase Detector while the rising edge is phase compared to the rising edge of the VCO/2. As depicted in Figure 1, $\overline{DRD}$ is a 1/3 cell wide (TVCO) pulse whose leading edge is defined by the leading edge of $\overline{RD}$. An accurate and symmetrical decode window is developed from the VCO/2 clock. By utilizing a fully integrated symmetrical VCO running at three times the data rate, the decode window is insured to be accurate and centered symmetrically about the rising edges of $\overline{DRD}$. The accuracy of the 1/3 cell delay only affects the retrace angle of the phase detector and does not influence the accuracy of the decode window.

In Non-Read Modes, the PLL is locked to the crystal reference oscillator. This forces the VCO to run at a frequency which is very close to that required for tracking actual data and thus minimizes the associated frequency step during acquisition. When the reference input to the PLL is switched, the VCO is stopped momentarily, then restarted in an accurate phase alignment with the next PLL reference input pulse, and the VCO clock divider is reset. By minimizing the phase alignment in this manner the acquisition time is substantially reduced.

After Read Mode is terminated (RG low), the VCO and RRC sources switch from $\overline{RD}$ and VCO/3, respectively, to the reference crystal. After a delay of one NRZ bit time (minimum) from when RG is low, write gate (WG) may be enabled (see figure 7 for timing diagram). NRZ is a tri-statable pin controlled by RG. NRZ will change states within one NRZ bit time. The NRZ pin can be connected to WDNRZ to form a bi-directional port.

SOFT SECTOR OPERATION

Disk Operation Lock Sequence in Read Mode Soft Sector Operation



ADDRESS MARK DETECT

In Soft Sector Read Operation the SSI 32D5362A must first detect an address mark to be able to initiate the rest of the read lock sequence. An address mark for the SSI 32D5362A consists of two (2) 7 "0" patterns followed by two 11 "0" patterns. To begin the read lock sequence the Address Mark Enable (AMENB) is asserted high by the controller. The SSI 32D5362A Address Mark Detect ($\overline{AMD}$) circuitry then initiates a search of the read data ($\overline{RD}$) for an address mark. First the $\overline{AMD}$ looks for a set of 6 "0's" within the 7 "0" patterns. Having detected a 6 "0" the $\overline{AMD}$ then looks for a 9 "0" set within the 11 "0's." If $\overline{AMD}$ does not detect 9 "0's" within 5 $\overline{RD}$ bits after detecting 6 "0's" it will restart the Address Mark Detect sequence and look for 6 "0's." When the $\overline{AMD}$ has acquired a 6 "0," 9 "0" sequence the $\overline{AMD}$ transitions low disabling AMENB input. When AMENB is released, $\overline{AMD}$ will be released and reset by the SSI 32D5362A. The AMENB should be released prior to entering Read Mode.

PREAMBLE SEARCH

After the Address Mark (AM) has been detected, Read Gate (RG) can be asserted initiating the remainder of the read lock sequence. When RG is asserted an internal counter counts negative transitions of the incoming Read Data ($\overline{RD}$) looking for (3) consecutive 3T preamble. Once the counter reaches count 3 (finds (3) consecutive negative transistors) the internal read gate switches the phase detector input from the reference oscillator to the Delayed Read Data ($\overline{DRD}$); at the same time a zero phase (internal) restart signal restarts the VCO in phase with the Delayed Read Data. This prepares the VCO to be synchronized to data when the bit sync circuitry is enabled after VCO lock is established.

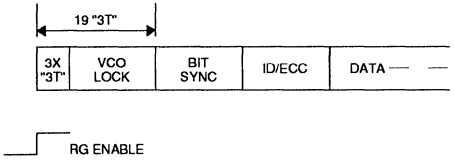
VCO LOCK & BIT SYNC ENABLE

When the internal counter counts 16 more negative transitions or a total of 19 "3T's" from RG enable, an internal VCO lock signal enables. The VCO lock signal activates the decoder bit synchronization circuitry to define the proper decode boundaries. Also, at the count of 19, the RRC source switches from the reference oscillator to VCO clock signal which is phase locked to $\overline{DRD}$. The VCO is assumed locked at this point. The bit sync circuitry searches for a '1001001' pattern to align the proper decode boundaries. During this time, an RRC pulse may be stretched a maximum of 2 RRC time periods during the alignment process to prevent any glitches.

HARD SECTOR OPERATION

Disk Operation Lock Sequence in Read Mode Hard Sector Operation

In hard sector operation a low AMENB disables the SSI 32D5362A's Address Mark Detection circuitry and



$\overline{AMD}$ remains inactive. A hard sector read operation does not require an address mark search but starts with a preamble search as with soft sector and sequences identically. In all respects, with the exception of the address mark search sequence, hard sector read operation is the same as soft sector read.

WRITE MODE

In the write mode the SSI 32D5362A converts NRZ data from the controller into 1,7 RLL formatted data for storage on the disk. The SSI 32D5362A can operate with a soft or hard sector hard drive.

Serial NRZ data is clocked into the SSI 32D5362A and latched on defined cell boundaries. The NRZ input data must be synchronous with the rising edges of the WCLK input. The WCLK input is a feature provided for operation in an ESDI application to compensate for large cable delays. In SCSI or IDE operation, WCLK is connected directly to the RRC output.

Write precompensation circuitry is provided to compensate for intersymbol interference caused by media bit shift. The SSI 32D5362A recognizes specific write data patterns and can add or subtract delays in the time position of write data bits to counteract the read back bit shift. The magnitude of the time shift, TPC, is determined by an external RC network on the WCS pin where the capacitor is connected from WCS to VPA1 and the resistor is connected from WCS to AGND. The equations is:

$$TPC = 0.053(Rc)(Cc + Cs)$$

When the write precompensation control latch, $\overline{WCL}$ is low, the SSI 32D5362A performs write precompensation according to the algorithm outlined in Table 4.

SOFT SECTOR

In soft sector operation, when Write Gate (WG) is asserted, the NRZ input (WDNRZ) must be kept low. To generate an Address Mark (consisting of 7 "0's", 7 "0's", 11 "0's", 11 "0's") the Address Mark Enable (AMENB) is toggled high for a minimum of 1 NRZ bit time. The toggling of AMENB must occur at least 1 NRZ bit time after WG is asserted. After the address mark is generated, WDNRZ must be kept low for an additional 44 NRZ bits to properly generate 19 x '3T' for the preamble plus three '3T' for the bit sync field. Data can then be written on the WDNRZ line with the encode data appearing on $\overline{WD}$ 5 NRZ bit times later. After writing is complete, WG should be held high for an additional 5 NRZ bit times to ensure that the encoder is flushed. See figure 9 for timing diagram.

HARD SECTOR

After WG is asserted, WDNRZ must be kept low for a minimum of 44 NRZ bit times to ensure a preamble field of at least 19 x "3T" plus 3 x "3T" for the bit sync field. Data can then be written as in the soft sector operation.

TEST POINTS

The SSI 32D5362A provides three (3) test points which can be utilized to evaluate window margin characteristics.

(a) $\overline{DRD}$, delayed read data – the positive edges represent the data bit position

(b) VCO REF, the VCO reference which represents the input to the Phase Detector, synchronizer, and 1,7 decoder

(c) VCO CLK, the VCO clock output which represents the output of the VCO

The following figure describes the relationship between the various test points:

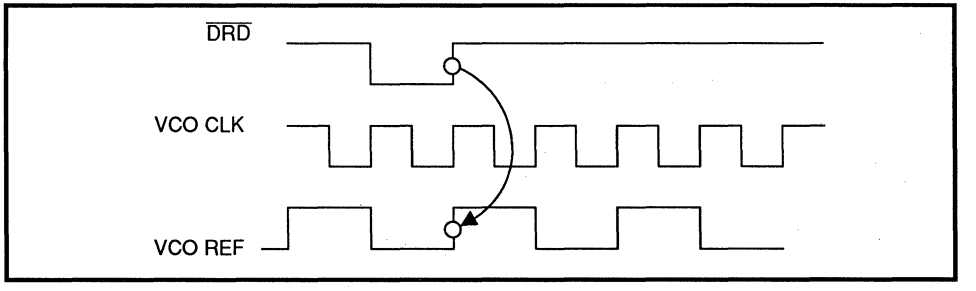


FIGURE 1: Test Point Relationships

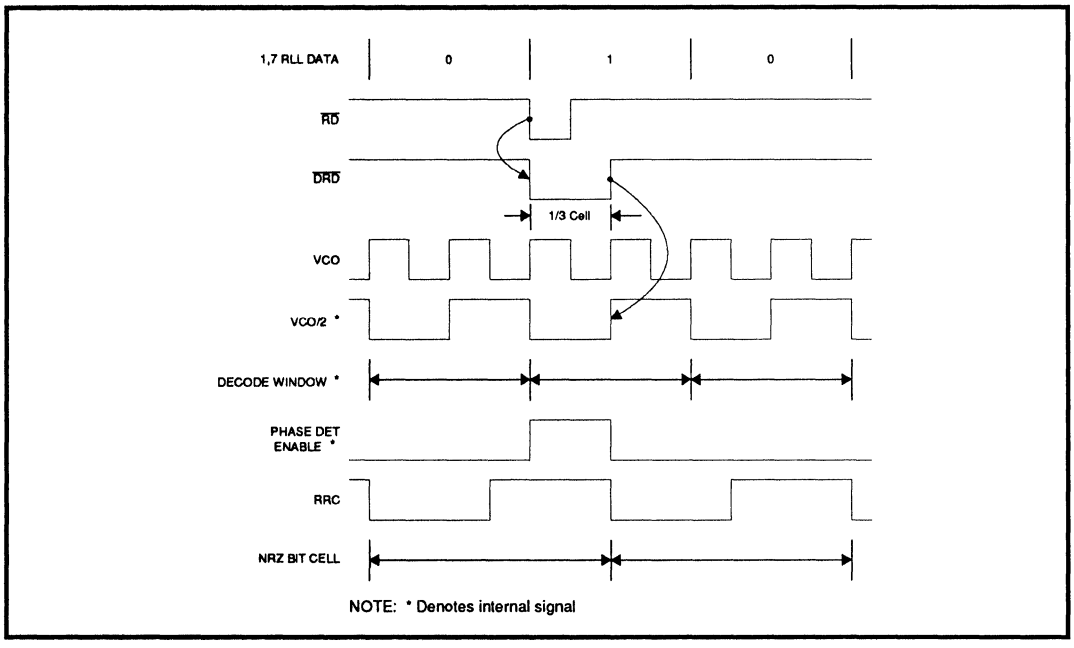


FIGURE 2: Data Synchronization Waveform

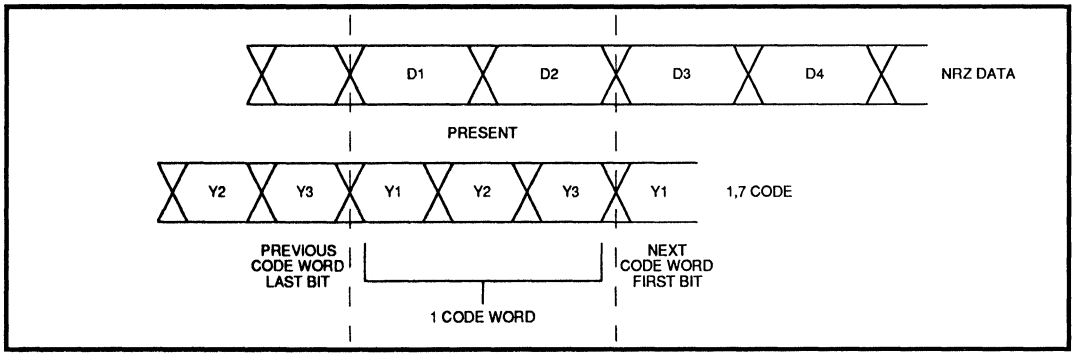


FIGURE 3: NRZ Data Word Comparision to 1, 7 Code Word (See Tables 1, and 2 for Decode Scheme)

TABLE 1: Decode Table for (1, 7) RLL Code Set

ENCODED READ DATA			DECODED DATA	
Previous	Present	Next		
Y Y	Y Y Y	Y Y Y	D D	
2' 3'	1 2 3	1 2 3	1 2	
0 0	0 0 0	X X X	0 1	
1 0	0 0 0	X X X	0 0	
0 1	0 0 0	X X X	0 1	
X X	1 0 0	X X X	1 1	
X 0	0 1 0	0 0	1 1	
X 0	0 1 0	1 0	1 0	
X 0	0 1 0	0 1	1 0	
X 1	0 1 0	0 0	0 1	
X 1	0 1 0	1 0	0 0	
X 1	0 1 0	0 1	0 0	
0 0	0 0 1	X X	0 1	
1 0	0 0 1	X X	0 0	
0 1	0 0 1	X X	0 0	(Preamble)
X X	1 0 1	X X	1 0	

TABLE 2: Encode Table for (1, 7) RLL Code Set

NRZ DATA				ENCODED WRITE DATA			
Present		Next		Previous	Present		
D	D	D	D	Y	Y	Y	Y
1	2	3	4	3	1	2	3
0	0	0	X	X	0	0	1
0	0	1	X	0	0	0	0
0	0	1	X	1	0	1	0
1	0	0	X	0	1	0	1
1	0	1	X	0	0	1	0
0	1	0	0	0	0	0	1
0	1	0	0	1	0	1	0
0	1	1	0	0	0	0	0
0	1	1	0	1	0	0	0
0	1	0	1	0	0	0	1
0	1	0	1	1	0	0	0
0	1	1	1	0	0	0	0
0	1	1	1	1	0	0	0
1	1	0	0	0	0	1	0
1	1	1	0	0	1	0	0
1	1	0	1	0	1	0	0
1	1	1	1	0	1	0	0

NOTE: X = Don't Care

TABLE 3: Clock Frequency

WG	RG	VCO REF	RRC	DECCLK	ENCCLK	MODE
0	0	XTAL/2	XTAL/3	XTAL/2	XTAL/2	IDLE
0	1	$\overline{RD}$	VCO/3	VCO/2	XTAL/2	READ
1	0	XTAL/2	XTAL/3	XTAL/2	XTAL/2	WRITE
1	1	XTAL/2	XTAL/3	XTAL/2	XTAL/2	ILLEGAL

Note 1: Until the VCO locks to the new source, the VCO/2 entries will be XTAL/2.

2: Until the VCO locks to the new source, the VCO/3 entries will be XTAL/3.

TABLE 4: Write Precompensation Algorithm

BIT	BIT	BIT	BIT	BIT	COMPENSATION
n-2	n-1	n	n+1	n+2	BIT n
1	0	1	0	1	NONE
0	0	1	0	0	NONE
1	0	1	0	0	EARLY
0	0	1	0	1	LATE

LATE: Bit n is time shifted (delayed) from its nominal time position towards the bit n+1 time position.

EARLY: Bit n is time shifted (advanced) from its nominal time position towards the bit n-1 time position.

TABLE 5: Write Precompensation Magnitude

$\overline{WCI}$	$\overline{WCO}$	MAGNITUDE.WP
0	0	3
0	1	2
1	0	1
1	1	0

The nominal magnitude,
(TPC = WP x 0.053 (Rc) (Cc+Cs), is externally set with an R-C network on pin WCS.

PIN DESCRIPTION

INPUT PINS

NAME	TYPE	DESCRIPTION
$\overline{RD}$	I	READ DATA: Encoded Read Data from the disk drive read channel, active low.
RG	I	READ GATE: Selects the PLL reference input (REF), see Table 1. A change in state on RG initiates the PLL synchronization sequence.
WG	I	WRITE GATE: Enables the write mode, see Table 2.
WCLK	I	WRITE CLOCK: Write Clock input. Must be synchronous with the NRZ Write Data input. For small cable delays, WCLK may be connected directly to pin RRC.
EPD	I	ENABLE PHASE DETECTOR: A low level (Coast Mode) disables the phase detector. This opens the PLL and the VCO will run at the frequency commanded by the voltage on pin VCO IN. Pin EPD has an internal resistor pull up.
AMENB	I	ADDRESS MARK ENABLE: Used to enable the address mark detection and address mark generation circuitry, active high.
$\overline{WC0}$, $\overline{WC1}$	I	WRITE PRECOMPENSATION CONTROL BITS: Pins $\overline{WC1}$, and $\overline{WC0}$ control the magnitude of the write precompensation, see Table 4. Internal resistor pull ups are provided.
$\overline{WCL}$	I	WRITE PRECOMPENSATION CONTROL LATCH: Used to latch the write precompensation control bits $\overline{WC1}$ and $\overline{WC0}$ into the internal DAC. An active low level latches the input bits. Pin $\overline{WCL}$ has an internal resistor pull up.
WDNRZ	I	NRZ WRITE DATA INPUT PIN: This pin can be connected to the NRZ pin to form a bidirectional data port.

OUTPUT PINS

NAME	TYPE	DESCRIPTION
$\overline{WD}$	O	WRITE DATA: Encoded write data output, active low. The data is automatically resynchronized (independent of the delay between RRC and WCLK) to one edge of the XTAL 1 input clock.
RRC	O	READ/REFERENCE CLOCK: A multiplexed clock source used by the controller, see Table 2. During a mode change, no glitches are generated and no more than two lost clock pulses will occur. When RG goes high, RRC is synchronized to the NRZ Read Data after 19 read data pulses.
$\overline{AMD}$	O	ADDRESS MARK DETECT: Tristate output pin that is in its high impedance state when WG is high or AMENB is low. A latched low level output indicates that an address mark has been detected. A low level on pin AMENB resets pin $\overline{AMD}$.

OUTPUT PINS (Continued)

NAME	TYPE	DESCRIPTION
VCO REF	O	VCO REFERENCE: An open emitter ECL output test point. The VCO reference input to the phase detector, the negative edges are phase locked to DLYD DATA. The positive edges of this open emitter output signal indicate the edges of the decode window. Two external resistors are required to perform this test, they should be removed during normal operation for reduced power dissipation.
VCO CLK	O	VCO CLOCK: An open emitter ECL output test point. Two external resistors are required to perform this test. They should be removed during normal operation for reduced power dissipation.
$\overline{\text{DRD}}$	O	DELAYED READ DATA: An open emitter ECL output test point. The positive edges of this open emitter output signal indicates the data bit position. The positive edges of the $\overline{\text{DRD}}$ and the VCO REF signals can be used to estimate window centering. The time jitter of DRD's positive edge is an indication of media bit shift. Two external resistors are required to perform this test. They should be removed during normal operation for reduced power dissipation.
NRZ	O	NRZ READ DATA OUTPUT: Tristate output pin that is enabled when read gate is high. This pin can be connected to the WDNRZ pin to form a bidirectional data port.

ANALOG PINS

NAME	TYPE	DESCRIPTION
IREF	I	TIMING PROGRAM PIN: The VCO center frequency and the 1/3 cell delay are a function of the current sourced into pin IREF.
XTAL1, 2	I	CRYSTAL OSCILLATOR CONNECTIONS: The pin frequency is at three times the data rate. If the crystal oscillator is used, an AC coupled parallel LC circuit must be connected from XTAL1 to ground. If the crystal oscillator is not desired, XTAL1 may be driven by a TTL source with XTAL2 open. The source duty cycle should be close to 50% as possible since its duty cycle will affect the RRC clock duty cycle when XTAL is its source. The additional RRC duty cycle error will be one third the source duty cycle error.
PD OUT	O	PHASE DETECTOR OUTPUT: Drives the loop filter input.
VCO IN	I	VCO CONTROL INPUT: Driven by the loop filter output.
WCS	I	WRITE PRECOMPENSATION SET: Pin for RC network to program write precompensation magnitude value. C_P to VPA1, R_P to AGND.
DGND, AGND	I	Digital and Analog Ground
VPA1, VPA2	I	Analog +5V Supplies
VPD	I	Digital +5V Supply

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

PARAMETER	RATING	UNIT
Storage Temperature	-65 to + 150	°C
Junction Operating Temperature, Tj	0 to +130	°C
Supply Voltage, VPA1, VPA2, VPD	-0.5 to 7	V
Voltage Applied to Logic Inputs	-0.5 to VPD + 0.5	V
Maximum Power Dissipation	1.1	W

RECOMMENDED OPERATING CONDITIONS

PARAMETER	RATING	UNIT
Supply Voltage, VPA1 = VPA2 = VPD = VCC	4.75 < VCC < 5.25	V
Ambient Operating Temperature, TA	0 < TA < +70	°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, 4.75V< VCC <5.25V, 10 MHz< 1/TORC <20 MHz, 30 MHz< 1/TVCO <60 MHz, TA = 0°C to 70°C

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VIH	High Level Input Voltage		2.0			V
VIL	Low Level Input Voltage				0.8	V
IIH	High Level Input Current	VIH = 2.7V			2.0	µA
IIL	Low Level Input Current	VIL = 0.4V			-1.5	mA
VOH	High Level Output Voltage	IOH = 400 µA	2.4			V
VOL	Low Level Output Voltage	IOL = 4 mA			0.5	V
ICC	Power Supply Current	All outputs open,*		170	190	mA
PWR	Power Dissipation	Test point* pins open		0.85	1.0	W

* WG, RG ***CANNOT*** both be high

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VOHT*	Test Point Output High Level $\overline{DRD}$, VCO CLK, VCO REF	262Ω to VPD 402Ω to GND VPD = 5.0V VOHT - VPD		-0.85		V
VOLT*	Test Point Output Low Level $\overline{DRD}$, VCO CLK, VCO REF	262Ω to VPD 402Ω to GND VPD = 5.0V VOLT - VPD		-1.75		V

* Monitor points only - Not tested

DYNAMIC CHARACTERISTICS AND TIMING

READ MODE (See Figure 3)

TRD	Read Data Pulse Width	Measured at 1.5V	15		TORC-20	ns
RRC	Duty Cycle	Measured at 1.5V, 15 Mbit/s	43		57	%
TFRD	Read Data Fall Time	2.0V to 0.8V, $C_L \leq 15$ pF			15	ns
TRRC	Read Clock Rise Time	0.8V to 2.0V, $C_L \leq 15$ pF			8	ns
TFNRZ	NRZ Fall Time	0.8V to 2.0V, $C_L \leq 15$ pF			8	ns
TRNRZ	NRZ Rise Time	2.0V to 0.8V, $C_L \leq 15$ pF			5	ns
TFRC	Read Clock Fall Time	2.0V to 0.8V, $C_L \leq 15$ pF			5	ns
TPNRZ	NRZ (out) Set Up/Hold Time		0.31 TORC			ns
Decode Window Centering Accuracy					±1.5	ns
Decode Window			(2TORC/3) - 3			ns

WRITE MODE (See Figure 4)

TWD	Write Data Pulse Width	$C_L \leq 15$ pF	See Note 1		See Note 2	ns
TFWD	Write Data Fall Time	2.0V to 0.8V, $C_L \leq 15$ pF			8	ns
TRWC**	Write Data Clock Rise Time	0.8V to 2.0V			10	ns
TFWC**	Write Data Clock Fall Time	2.0V to 0.8V			8	ns
TSNRZ	WDNRZ Set up Time		5			ns
THNRZ	WDNRZ Hold Time		5			ns

Note 1: $\frac{2}{3}TOWC - 5 - 4.76TPCO - TPC$ Note 2: $\frac{2}{3}TOWC + 10 - 4.76TPCO - TPC$

** **INPUT** requirement - Not tested

WRITE MODE (Continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TPC	Precompensation Time Shift Magnitude Accuracy	TPCO=0.053 (Cc+Cs) (Rc) Rc=1k to 2k; Cc + Cs = 25pF to 40 pF; Cs=stray capacity				
		$\overline{WC0}$ = 1 $\overline{WC1}$ = 1		0		ns
		$\overline{WC0}$ = 0 $\overline{WC1}$ = 1		TPCO		ns
		$\overline{WC0}$ = 1 $\overline{WC1}$ = 0		(2)TPCO		ns
		$\overline{WC0}$ = 0 $\overline{WC1}$ = 0		(3)TPCO		ns

DATA SYNCHRONIZATION

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TVCO	VCO Center Frequency Period	VCC = 5.0V, VCO_IN = 2.7V TO = 3.6 (RR + 2.3) TO (ns); RR (kΩ) RR = 2.3k to 7.0k	0.85 TO		1.15 TO	ns
	VCO Frequency Dynamic Range	1V ≤ VCO_IN ≤ VCC-0.6V	±20		±40	%
KVCO	VCO Control Gain	ωo = 2π/TVCO 1V ≤ VCO IN ≤ VCC 0.6V	0.12 ωo		0.24 ωo	rad/s-V
KD*	Phase Detector Gain	KD = 570/ (RR + 0.53) KD(μA/rad), RR (kΩ), PLL REF = $\overline{RD}$, 1T pattern	0.83 KD		1.17 KD	μA/rad
*KVCO •	KD Product Accuracy		-28		-28	%
TD	1/3 Cell Delay	TD0 = 5.05 (RR + 0.530) RR = kΩ	0.8TD0		1.2TD0	ns
*VCO	Phase Restart Error			6		ns

CONTROL CHARACTERISTICS (See Figure 5)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TSWS	$\overline{WC0}$, $\overline{WC1}$ SET UP TIME		50			ns
THWS	$\overline{WC0}$, $\overline{WC1}$ HOLD TIME		0			ns

* Indirectly tested

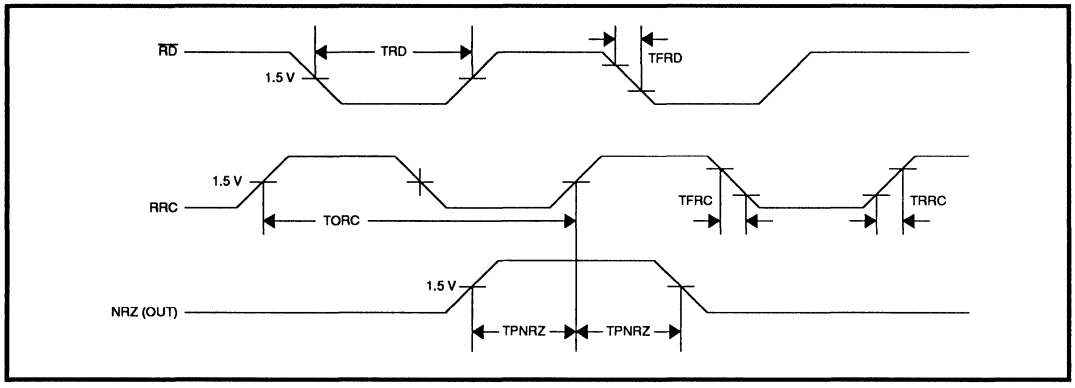


FIGURE 3: Read Timing

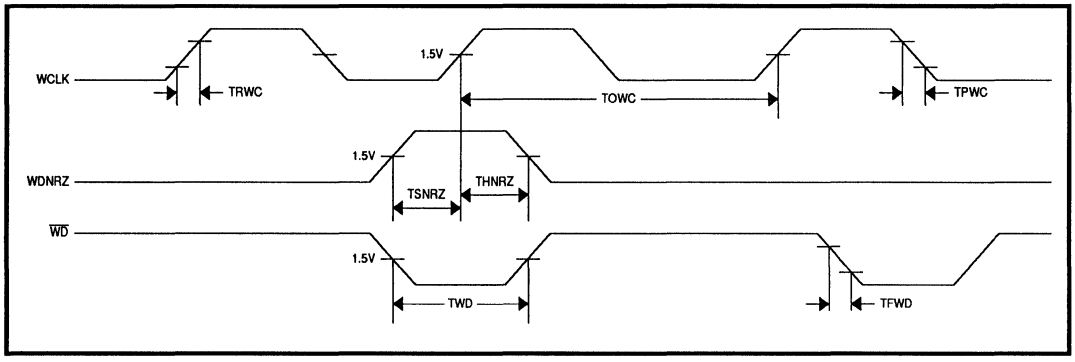


FIGURE 4: Write Timing

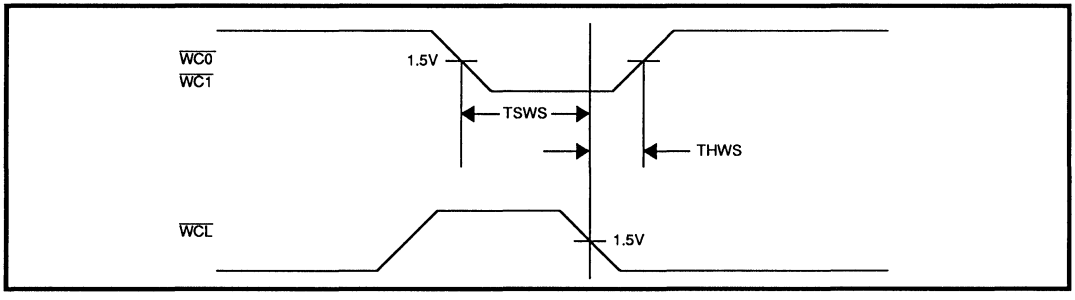


FIGURE 5: Control Timing

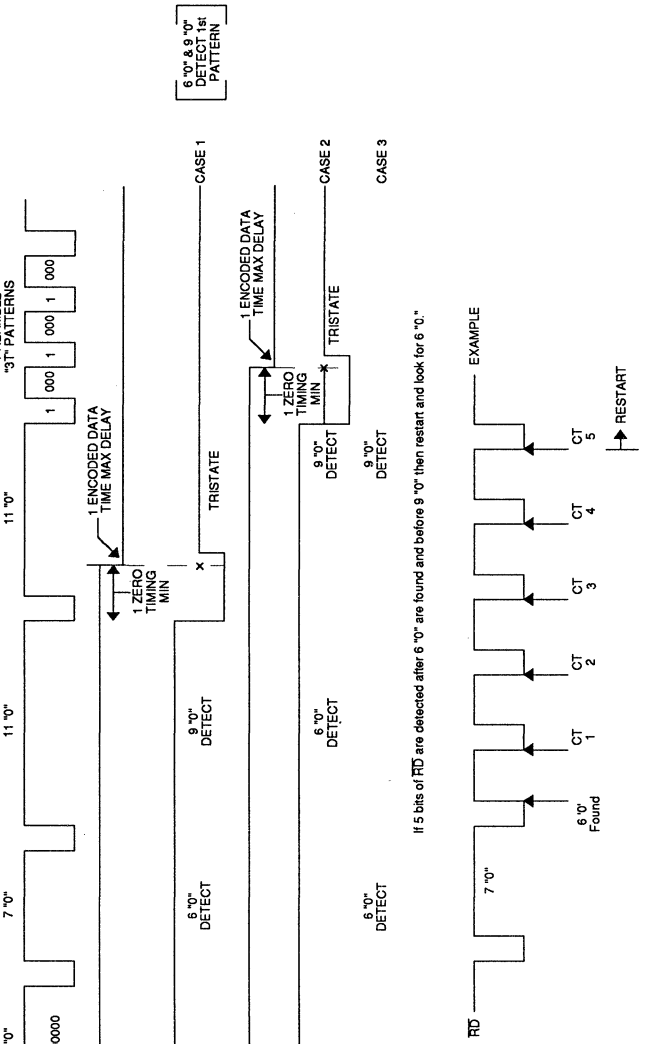


FIGURE 6: Address Mark Search

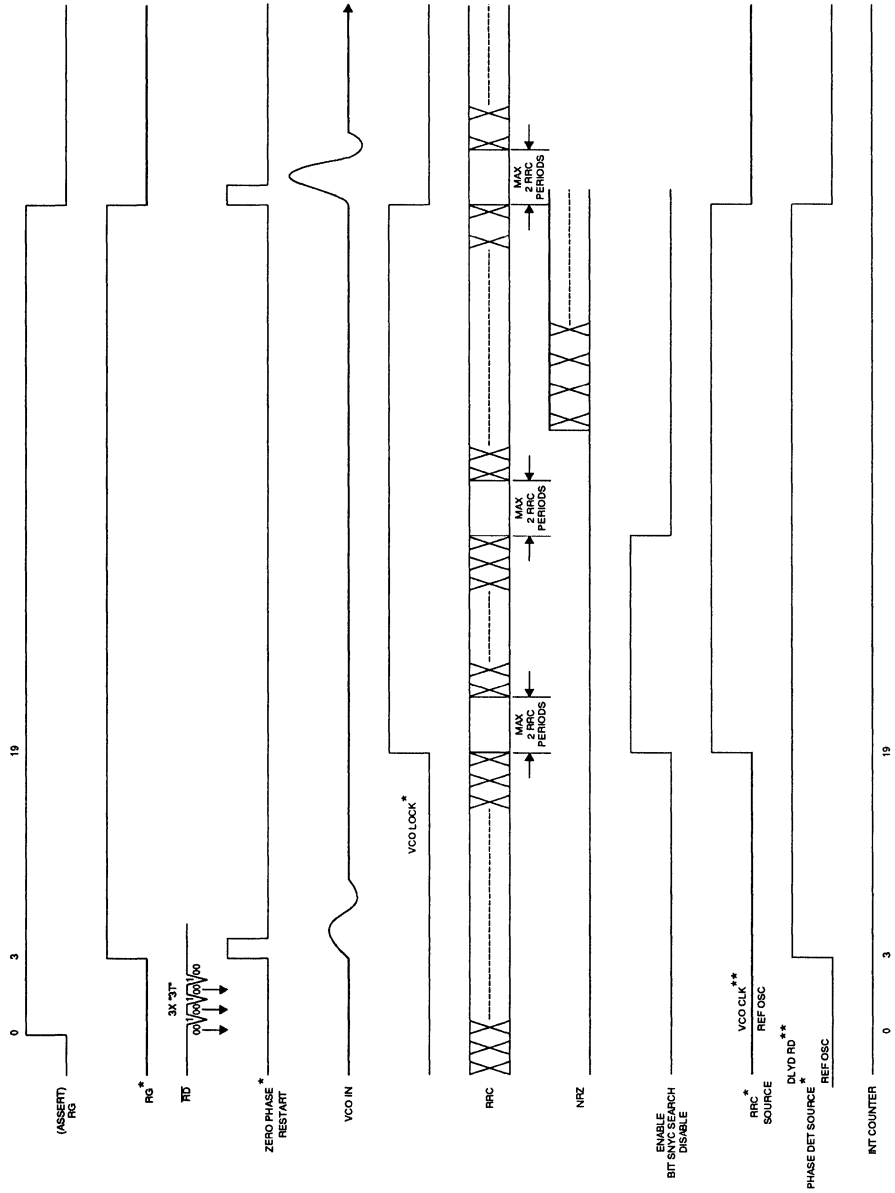


FIGURE 7: Read Mode Locking Sequence (Soft and Hard Sector)

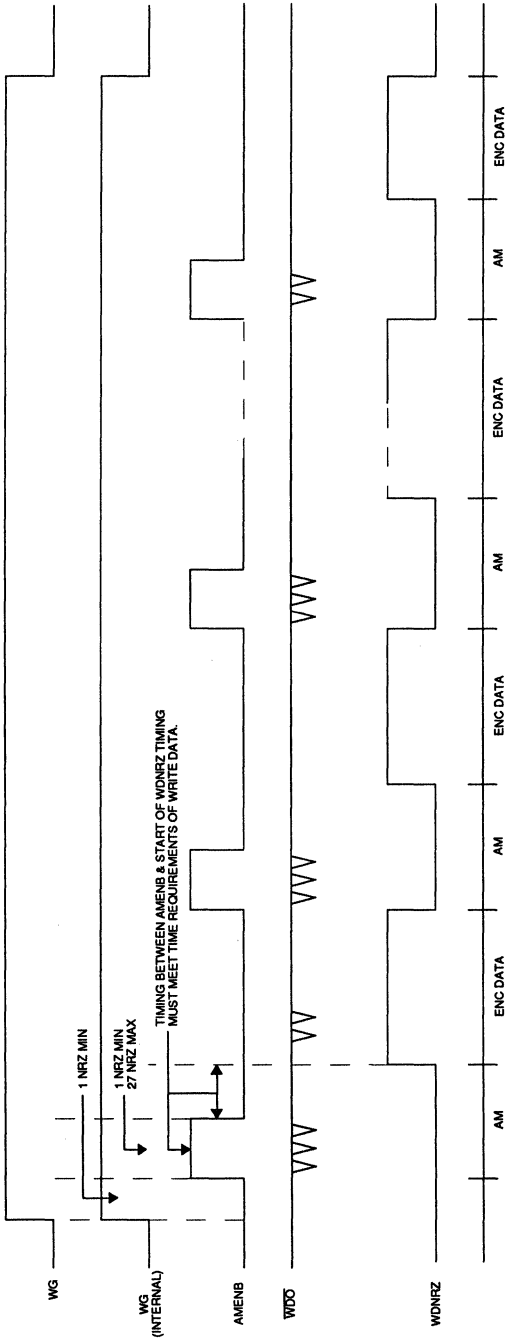


FIGURE 8: Multiple Address Mark Write

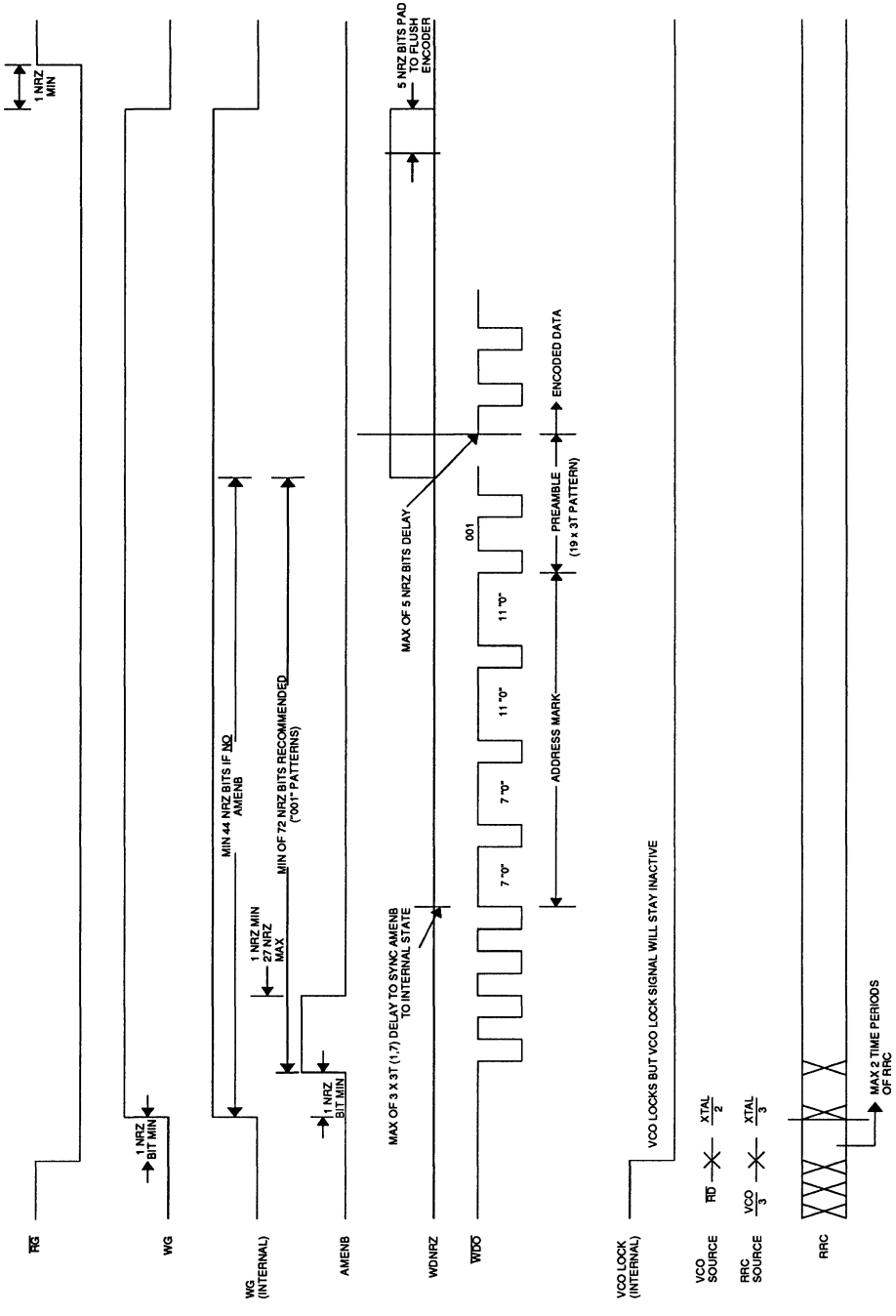
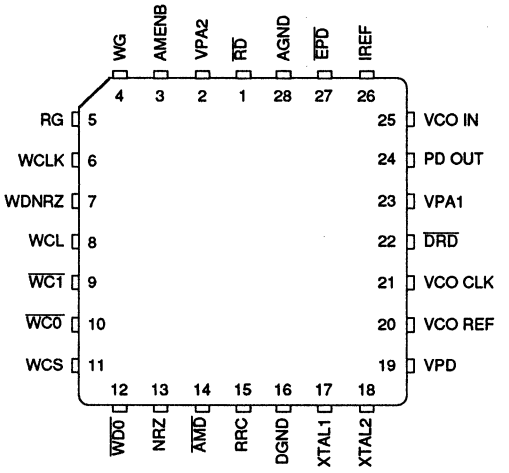


FIGURE 9: Write Data

SSI 32D5362A
Data Synchronization/1, 7 RLL ENDEC with Write Precompensation

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



28-Pin PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDERING NUMBER	PACKAGE MARK
SSI 32D5362A		
28-Pin PLCC	32D5362A-CH	32D5362A-CH

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 731-7110, FAX (714) 573-6914

silicon systems®
A TDK Group Company

SSI 32D5371/2/3/4

Data Synchronization/1, 7 RLL ENDEC with Write Precompensation

Preliminary Data

November 1991

DESCRIPTION

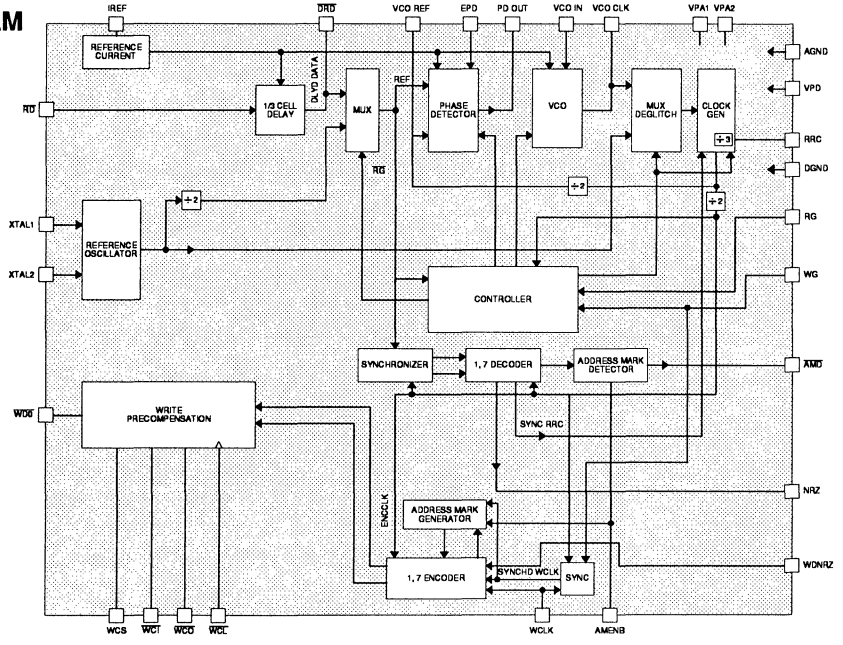
The SSI 32D537 Data Synchronizer/1, 7 RLL ENDEC family provides data recovery and data encoding for storage systems which employ a 1, 7 RLL encoding format. Data synchronization is performed with a fully integrated high performance PLL. A zero phase restart technique is used to minimize PLL acquisition time. The SSI 32D537 family has been optimized for operation as a companion device to the SSI 32C4650 controller. The VCO frequency setting elements are incorporated within the SSI 32D537 family for enhanced performance and reduced board space. Data rate is established with a single external programming resistor. The SSI 32D5371 family utilizes an advanced bipolar process technology which affords precise decode window control without the requirement of an accurate 1/3 cell delay or external devices. The SSI 32D537 family requires a single +5V supply.

FEATURES

- **32D5371 – ECL RD Input Option, 10 to 24 Mbit/s**
- **32D5372 – TTL $\overline{RD}$ Input Option, 10 to 24 Mbit/s**
- **32D5373 – TTL $\overline{RD}$ Input Option, 15 to 32 Mbit/s**
- **32D5374 – ECL RD Input Option, 15 to 32 Mbit/s**
- **Data Synchronizer and 1, 7 RLL ENDEC**
- **Data Rate programmed with a single external resistor or current source**
- **Optimized for operation with the SSI 32C4650 controller.**
- **Fast acquisition phase lock loop**
  - **Zero phase restart technique**
- **Fully integrated data separator**
  - **No external delay lines or active devices required**
- **Programmable write precompensation**
- **Hard and soft sector operation**
- **Crystal controlled reference oscillator**
- **+5V operation**
- **28-Pin PLCC & 28-Pin SOL packages**
- **Test outputs - Allow drive margin testing**

4

BLOCK DIAGRAM



OPERATION

The SSI 32D5371, 32D5372, 32D5373, 32D5374 product family, hereafter designated as the 32D537X, are designed to perform data recovery and data encoding in rotating memory systems which utilize a 1,7 RLL encoding format. In the Read Mode the SSI 32D5367X performs Data Synchronization, Sync Field Search and Detect, Address Mark Detect, and Data Decoding. In the Write Mode, the SSI 32D537X converts NRZ data into the 1,7 RLL format described in Table 1, performs Write Precompensation, and inserts Address Marks as requested. The interface electronics and architecture of the SSI 32D537X have been optimized for use as a companion device to the SSI 32C9000 controller.

The SSI 32D537X can operate with data rates ranging from 10 to 20 Mbit/s. This data rate is established by a single 1% external resistor, RR, connected from pin IREF to VPA. This resistor establishes a reference current which sets the VCO center frequency, the phase detector gain, and the 1/3 cell delay. The value of this resistor is given by:

$$32D5371/5372:\ RR=\frac{92.6}{DR}-1.7\,(k\Omega)$$

$$32D5373/5374:\ RR=\frac{139}{DR}-1.7\,(k\Omega)$$

where: DR = Data Rate in Mbit/s.

An internal crystal reference oscillator, operating at three times the data rate, generates the standby reference for the PLL. A series resonant crystal between XTAL1 and XTAL2 should be selected at three times the Data Rate. If a crystal oscillator is not desired, then an AC coupled ECL source may be applied to XTAL1, leaving XTAL2 open. A TTL compatible reference may also be used if suitably attenuated and AC coupled.

The SSI 32D537X employs a Dual Mode Phase Detector; Harmonic in the Read Mode and Non Harmonic in Write and Idle Modes. In the Read Mode the Harmonic Phase Detector updates the PLL with each occurrence of a DYLD DATA pulse. In the Write and Idle modes the Non-Harmonic Phase Detector is continuously enabled, thus maintaining both phase and frequency lock. By acquiring both phase and frequency lock to the crystal reference oscillator and utilizing a zero phase restart technique, false lock to DLYD DATA is eliminated.

The phase detector incorporates a charge pump in order to drive the loop filter directly. The polarity and width of the output current pulses correspond to the direction and magnitude of the phase error.

The READ GATE (RG), and WRITE GATE (WG) inputs control the device mode.

RG is an asynchronous input and may be initiated or terminated at any position on the disk. WG is also an asynchronous input, but should not be terminated prior to the last output Write Data pulse.

READ OPERATION

The Data Synchronizer utilizes a fully integrated fast acquisition PLL to accurately develop the decode window. Read Gate, RG, initiates the PLL locking sequence and selects the PLL reference input; a high level (Read Mode) selects the $\overline{RD}$ input and a low level selects the crystal reference oscillator.

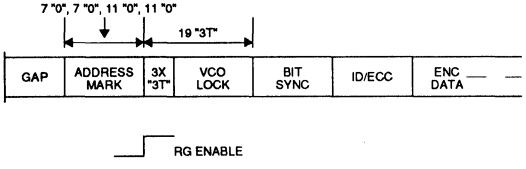
In the Read Mode the falling edge of $\overline{DRD}$ enables the Phase Detector while the rising edge is phase compared to the rising edge of the VCO/2. As depicted in Figure 1, $\overline{DRD}$ is a 1/3 cell wide (TVCO) pulse whose leading edge is defined by the leading edge of $\overline{RD}$. An accurate and symmetrical decode window is developed from the VCO/2 clock. By utilizing a fully integrated symmetrical VCO running at three times the data rate, the decode window is insured to be accurate and centered symmetrically about the rising edges of $\overline{DRD}$. The accuracy of the 1/3 cell delay only affects the retrace angle of the phase detector and does not influence the accuracy of the decode window.

In Non-Read Modes, the PLL is locked to the crystal reference oscillator. This forces the VCO to run at a frequency which is very close to that required for tracking actual data and thus minimizes the associated frequency step during acquisition. When the reference input to the PLL is switched, the VCO is stopped momentarily, then restarted in an accurate phase alignment with the next PLL reference input pulse, and the VCO clock divider is reset. By minimizing the phase alignment in this manner the acquisition time is substantially reduced.

After Read Mode is terminated (RG low), the VCO and RRC sources switch from $\overline{RD}$ and VCO/3, respectively, to the reference crystal. After a delay of one NRZ bit time (minimum) from when RG is low, write gate (WG) may be enabled (see figure 7 for timing diagram). NRZ is a tri-statable pin controlled by RG. NRZ will change states within one NRZ bit time. The NRZ pin can be connected to WDNRZ to form a bi-directional port.

SOFT SECTOR OPERATION

Disk Operation Lock Sequence in Read Mode Soft Sector Operation



ADDRESS MARK DETECT

In Soft Sector Read Operation the SSI 32D537X must first detect an address mark to be able to initiate the rest of the read lock sequence. An address mark for the SSI 32D537X consists of two (2) 7 "0" patterns followed by two 11 "0" patterns. To begin the read lock sequence the Address Mark Enable (AMENB) is asserted high by the controller. The SSI 32D537X Address Mark Detect ($\overline{AMD}$) circuitry then initiates a search of the read data ($\overline{RD}$) for an address mark. First the $\overline{AMD}$ looks for a set of 6 "0's" within the 7 "0" patterns. Having detected a 6 "0" the $\overline{AMD}$ then looks for a 9 "0" set within the 11 "0's." If $\overline{AMD}$ does not detect 9 "0's" within 5 $\overline{RD}$ bits after detecting 6 "0's" it will restart the Address Mark Detect sequence and look for 6 "0's." When the $\overline{AMD}$ has acquired a 6 "0," 9 "0" sequence the $\overline{AMD}$ transitions low disabling AMENB input. When AMENB is released, $\overline{AMD}$ will be released and reset by the SSI 32D537X. The AMENB should be released prior to entering Read Mode.

PREAMBLE SEARCH

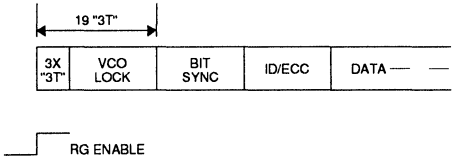
After the Address Mark (AM) has been detected, Read Gate (RG) can be asserted initiating the remainder of the read lock sequence. When RG is asserted an internal counter counts negative transitions of the incoming Read Data ($\overline{RD}$) looking for (3) consecutive negative transitions. Once the counter reaches count 3 (finds (3) consecutive negative transistors) the internal read gate switches the phase detector input from the reference oscillator to the Delayed Read Data ($\overline{DRD}$); at the same time a zero phase (internal) restart signal restarts the VCO in phase with the Delayed Read Data. This prepares the VCO to be synchronized to data when the bit sync circuitry is enabled after VCO lock is established.

VCO LOCK & BIT SYNC ENABLE

When the internal counter counts 16 more negative transitions or a total of 19 "3T's" from RG enable, an internal VCO lock signal enables. The VCO lock signal activates the decoder bit synchronization circuitry to define the proper decode boundaries. Also, at the count of 19, the RRC source switches from the reference oscillator to VCO clock signal which is phase locked to $\overline{DRD}$. The VCO is assumed locked at this point. The bit sync circuitry searches for a '1001001' pattern to align the proper decode boundaries. During this time, an RRC pulse may be stretched a maximum of 2 RRC time periods during the alignment process to prevent any glitches.

HARD SECTOR OPERATION

Disk Operation Lock Sequence in Read Mode Hard Sector Operation



In hard sector operation a low AMENB disables the SSI 32D537X's Address Mark Detection circuitry and $\overline{AMD}$ remains inactive. A hard sector read operation does not require an address mark search but starts with a preamble search as with soft sector and sequences identically. In all respects, with the exception of the address mark search sequence, hard sector read operation is the same as soft sector read.

WRITE MODE

In the write mode the SSI 32D537X converts NRZ data from the controller into 1,7 RLL formatted data for storage on the disk. The SSI 32D537X can operate with a soft or hard sector hard drive.

Serial NRZ data is clocked into the SSI 32D537X and latched on defined cell boundaries. The NRZ input data must be synchronous with the rising edges of the WCLK input. The WCLK input is a feature provided for operation in an ESDI application to compensate for large cable delays. In SCSI or IDE operation, WCLK is connected directly to the RRC output.

Write precompensation circuitry is provided to compensate for intersymbol interference caused by media bit shift. The SSI 32D537X recognizes specific write data patterns and can add or subtract delays in the time position of write data bits to counteract the read back bit shift. The magnitude of the time shift, TPC, is determined by an external register on the WCS pin where the register is connected from WCS to VPA1.

When the write precompensation control latch, $\overline{WCL}$ is low, the SSI 32D537X performs write precompensation according to the algorithm outlined in Table 4.

SOFT SECTOR

In soft sector operation, when Write Gate (WG) is asserted, the NRZ input (WDNRZ) must be kept low. To generate an Address Mark (consisting of 7 "0's", 7 "0's", 11 "0's", 11 "0's") the Address Mark Enable (AMENB) is toggled high for a minimum of 1 NRZ bit time. The toggling of AMENB must occur at least 1 NRZ bit time after WG is asserted. After the address mark is generated, WDNRZ must be kept low for an additional 44 NRZ bits to properly generate 19 x '3T' for the preamble plus three '3T' for the bit sync field. Data can then be written on the WDNRZ line with the encode data appearing on $\overline{WD}$ 5 NRZ bit times later. After writing is complete, WG should be held high for an additional 5 NRZ bit times to ensure that the encoder is flushed. See Figure 9 for timing diagram.

HARD SECTOR

After WG is asserted, WDNRZ must be kept low for a minimum of 44 NRZ bit times to ensure a preamble field of at least 19 x "3T" plus 3 x "3T" for the bit sync field. Data can then be written as in the soft sector operation.

TEST POINTS

The SSI 32D537X provides three (3) test points which can be utilized to evaluate window margin characteristics.

(a) $\overline{DRD}$, delayed read data – the positive edges represent the data bit position

(b) VCO REF, the VCO reference which represents the input to the Phase Detector, synchronizer, and 1,7 decoder

(c) VCO CLK, the VCO clock output which represents the output of the VCO

The following figure describes the relationship between the various test points:

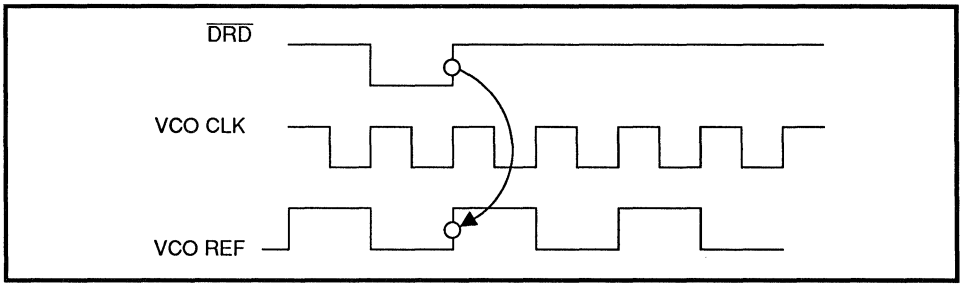


FIGURE 1: Test Point Relationships

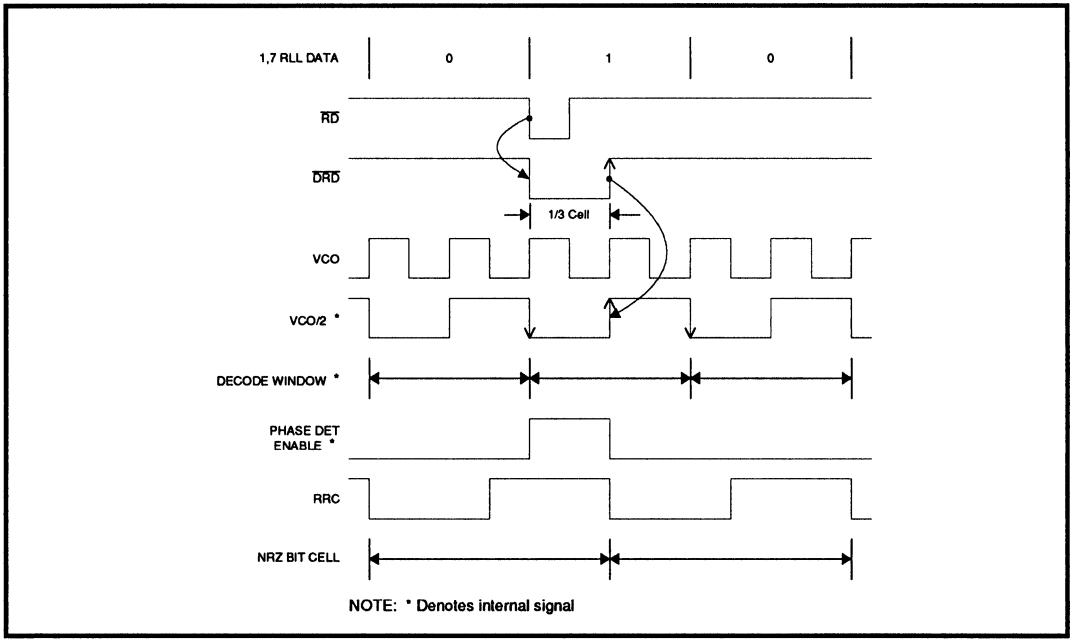


FIGURE 2: Data Synchronization Waveform

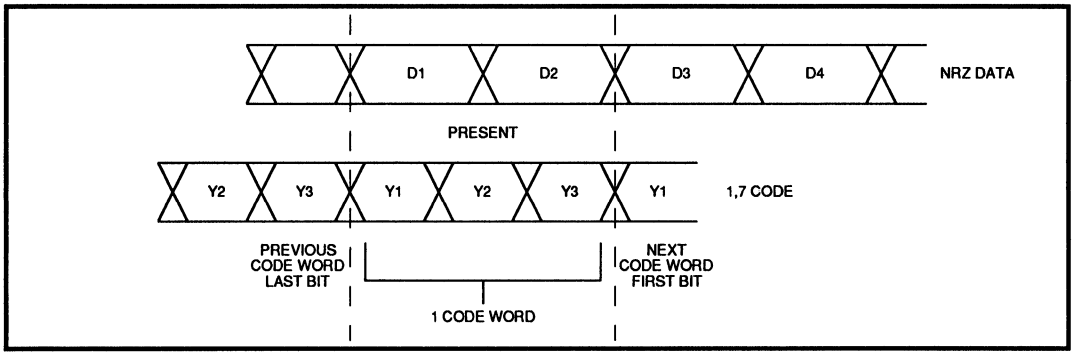


FIGURE 3: NRZ Data Word Comparision to 1, 7 Code Word (See Tables 1, and 2 for Decode Scheme)

TABLE 1: Decode Table for (1, 7) RLL Code Set

ENCODED READ DATA			DECODED DATA	
Previous	Present	Next		
Y Y	Y Y Y	Y Y	D D	
2' 3'	1 2 3	1 2	1 2	
0 0	0 0 0	X X	0 1	
1 0	0 0 0	X X	0 0	
0 1	0 0 0	X X	0 1	
X X	1 0 0	X X	1 1	
X 0	0 1 0	0 0	1 1	
X 0	0 1 0	1 0	1 0	
X 0	0 1 0	0 1	1 0	
X 1	0 1 0	0 0	0 1	
X 1	0 1 0	1 0	0 0	
X 1	0 1 0	0 1	0 0	
0 0	0 0 1	X X	0 1	
1 0	0 0 1	X X	0 0	
0 1	0 0 1	X X	0 0	(Preamble)
X X	1 0 1	X X	1 0	

TABLE 2: Encode Table for (1, 7) RLL Code Set

NRZ DATA				ENCODED WRITE DATA			
Present		Next		Previous	Present		
D	D	D	D	Y	Y	Y	Y
1	2	3	4	3	1	2	3
0	0	0	X	X	0	0	1
0	0	1	X	0	0	0	0
0	0	1	X	1	0	1	0
1	0	0	X	0	1	0	1
1	0	1	X	0	0	1	0
0	1	0	0	0	0	0	1
0	1	0	0	1	0	1	0
0	1	1	0	0	0	0	0
0	1	1	0	1	0	0	0
0	1	0	1	0	0	0	1
0	1	0	1	1	0	0	0
0	1	1	1	0	0	0	0
0	1	1	1	1	0	0	0
1	1	0	0	0	0	1	0
1	1	1	0	0	1	0	0
1	1	0	1	0	1	0	0
1	1	1	1	0	1	0	0

NOTE: X = Don't Care

TABLE 3: Clock Frequency

WG	RG	VCO REF	RRC	DECCLK	ENCCLK	MODE
0	0	XTAL/2	XTAL/3	XTAL/2	XTAL/2	IDLE
0	1	$\overline{RD}$	VCO/3	VCO/2	XTAL/2	READ
1	0	XTAL/2	XTAL/3	XTAL/2	XTAL/2	WRITE
1	1	XTAL/2	XTAL/3	XTAL/2	XTAL/2	IDLE

Note 1: Until the VCO locks to the new source, the VCO/2 entries will be XTAL/2.

2: Until the VCO locks to the new source, the VCO/3 entries will be XTAL/3.

TABLE 4: Write Precompensation Algorithm

BIT	BIT	BIT	BIT	BIT	COMPENSATION
n-2	n-1	n	n+1	n+2	BIT n
1	0	1	0	1	NONE
0	0	1	0	0	NONE
1	0	1	0	0	EARLY
0	0	1	0	1	LATE

LATE: Bit n is time shifted (delayed) from its nominal time position towards the bit n+1 time position.

EARLY: Bit n is time shifted (advanced) from its nominal time position towards the bit n-1 time position.

TABLE 5: Write Precompensation Magnitude

$\overline{WCI}$	$\overline{WCO}$	MAGNITUDE (WP)
0	0	3
0	1	2
1	0	1
1	1	0

The nominal magnitude,
TPC = WP x TPC0 is externally set with resistors on pins WCS and IREF.

PIN DESCRIPTION

INPUT PINS

NAME	TYPE	DESCRIPTION
$\overline{RD}$ (TTL) RD (ECL)	I	READ DATA: Encoded Read Data from the disk drive read channel. The TTL input version (5372/5373) is an active low signal. The ECL input version (5371/5374) is an active high signal.
RG	I	READ GATE: Selects the PLL reference input (REF), see Table 2. A change in state on RG initiates the PLL synchronization sequence. Pin RG has an internal resistor pullup.
WG	I	WRITE GATE: Enables the write mode, see Table 2. Pin WG has an internal resistor pullup.
WCLK	I	WRITE CLOCK: Write Clock input. Must be synchronous with the NRZ Write Data input. For small cable delays, WCLK may be connected directly to pin RRC.
EPD	I	ENABLE PHASE DETECTOR: A low level (Coast Mode) disables the phase detector and enables the test mode. This opens the PLL and the VCO will run at the frequency commanded by the voltage on pin VCO IN. In the test mode, functions normally driven by the VCO are switched to XTAL. Pin EPD has an internal resistor pull up.
AMENB	I	ADDRESS MARK ENABLE: Used to enable the address mark detection and address mark generation circuitry, active high. Pin AMENB has an internal resistor pullup.
$\overline{WC0}$, $\overline{WC1}$	I	WRITE PRECOMPENSATION CONTROL BITS: Pins $\overline{WC1}$, and $\overline{WC0}$ control the magnitude of the write precompensation, see Table 4. Internal resistor pull ups are provided. If unused, leave pins open or tie high.
$\overline{WCL}$	I	WRITE PRECOMPENSATION CONTROL LATCH: Used to latch the write precompensation control bits $\overline{WC1}$ and $\overline{WC0}$ into the internal DAC. An active low level latches the input bits. Pin $\overline{WCL}$ has an internal resistor pull up. If unused, leave pin open or tie high.
WDNRZ	I	NRZ WRITE DATA INPUT PIN: This pin can be connected to the NRZ pin to form a bidirectional data port.

OUTPUT PINS

$\overline{WD0}$	O	WRITE DATA: Encoded write data output, active low. The data is automatically resynchronized (independent of the delay between RRC and WCLK) to one edge of the XTAL1 input clock.
RRC	O	READ/REFERENCE CLOCK: A multiplexed clock source used by the controller, see Table 2. During a mode change, no glitches are generated and no more than two lost clock pulses will occur. When RG goes high, RRC is synchronized to the NRZ Read Data after 19 read data pulses.
$\overline{AMD}$	O	ADDRESS MARK DETECT: Tristate output pin that is in its high impedance state when WG is high or AMENB is low. A latched low level output indicates that an address mark has been detected. A low level on pin AMENB resets pin $\overline{AMD}$.

OUTPUT PINS (Continued)

NAME	TYPE	DESCRIPTION
VCO REF	O	VCO REFERENCE: An open emitter ECL output test point. The VCO reference input to the phase detector, the positive edges are phase locked to DLYD DATA. The negative edges of this open emitter output signal indicate the edges of the decode window. Two external resistors are required to perform this test, they should be removed during normal operation for reduced power dissipation.
VCO CLK	O	VCO CLOCK: An open emitter ECL output test point. Two external resistors are required to perform this test. They should be removed during normal operation for reduced power dissipation.
$\overline{\text{DRD}}$	O	DELAYED READ DATA: An open emitter ECL output test point. The positive edges of this open emitter output signal indicates the data bit position. The positive edges of the $\overline{\text{DRD}}$ and the VCO REF signals can be used to estimate window centering. The time jitter of DRD's positive edge is an indication of media bit shift. Two external resistors are required to perform this test. They should be removed during normal operation for reduced power dissipation.
NRZ	O	NRZ READ DATA OUTPUT: Tristate output pin that is enabled when read gate is high. This pin can be connected to the WDNRZ pin to form a bidirectional data port.

ANALOG PINS

IREF	I	TIMING PROGRAM PIN: The VCO center frequency and the 1/3 cell delay are a function of the current sourced into pin IREF. The current is set by an external resistor, RR, connected between pin IREF and VPA2.
XTAL1, 2	I	CRYSTAL OSCILLATOR CONNECTIONS: The pin frequency is at three times the data rate. If the crystal oscillator is used, an AC coupled parallel LC circuit must be connected from XTAL1 to ground. If the crystal oscillator is not desired, XTAL1 may be driven either by an AC coupled suitably attenuated TTL source or by an AC coupled ECL source, with XTAL2 open. The source duty cycle should be as close to 50% as possible, since its duty cycle will affect the RRC clock duty cycle when XTAL is its source. The additional RRC duty cycle error will be one third the source duty cycle error.
PD OUT	O	PHASE DETECTOR OUTPUT: Drives the loop filter input.
VCO IN	I	VCO CONTROL INPUT: Driven by the loop filter output.
WCS	I	WRITE PRECOMPENSATION SET: Pin for a resistor to program the write precompensation magnitude value. The resistor, RC, is connected between pin WCS and VPA2. If this pin is left open, write precompensation is disabled.
DGND, AGND	I	Digital and Analog Ground
VPA1, VPA2	I	Analog +5V Supplies
VPD	I	Digital +5V Supply

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

PARAMETER	RATING	UNIT
Storage Temperature	-65 to + 150	°C
Junction Operating Temperature, Tj	+150	°C
Supply Voltage, VPA1, VPA2, VPD	-0.5 to 7	V
Voltage Applied to Logic Inputs	-0.5 to VPD + 0.5	V
Maximum Power Dissipation	0.9	W

RECOMMENDED OPERATING CONDITIONS

Supply Voltage, VPA1 = VPA2 = VPD = VCC	4.75 < VCC < 5.25	V
Junction Temperature, Tj	0 < Tj < 135	°C
Ambient Temperature, Ta	0 < Ta < 70°	°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, 4.75V < VCC < 5.25V, 10 MHz < 1/TORC < 24 MHz, 30 MHz < 1/TVCO < 72 MHz (32D5371/5372), 15 MHz < 1/TORC < 32 MHz, 45 MHz < 1/TVCO < 96 MHz (32D5373/5374), 0 °C < Ta < 70 °C.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VIH	High Level Input Voltage		2.0			V
VIL	Low Level Input Voltage				0.8	V
IIH	High Level Input Current	VIH = 2.7V			20	µA
IIL	Low Level Input Current	VIL = 0.4V			-0.36	mA
VOH	High Level Output Voltage	IOH = 400 µA	2.4			V
VOL	Low Level Output Voltage	IOL = 4 mA			0.5	V
VIHP	Pseudo ECL High Level Input Voltage; RD	Ta = 25°C	VCC-1.0			V
VILP	Pseudo ECL Low Level Input Voltage; RD	Ta = 25°C			VCC-1.5	V
IIHP	Pseudo ECL High Level Input Current; RD	VIH = VCC -0.8V			2.0	mA
IILP	Pseudo ECL Low Level Input Current; RD	VIL = VCC -1.5V			1.6	mA
ICC	Power Supply Current	All outputs & test point pins open			160	mA
PWR	Power Dissipation	All outputs & test point pins open			0.84	W

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VOHT	Test Point Output High Level $\overline{DRD}$, VCO CLK, VCO REF	262Ω to VPD 402Ω to DGND VPD = 5.0V VOHT - VPD		-0.85		V
VOLT	Test Point Output Low Level $\overline{DRD}$, VCO CLK, VCO REF	262Ω to VPD 402Ω to DGND VPD = 5.0V VOLT - VPD		-1.75		V

4

DYNAMIC CHARACTERISTICS AND TIMING

READ MODE (See Figure 3)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TRD	Read Data Pulse Width		12		4/3TORC-20	ns
TFRD	Read Data Fall Time	2.0V to 0.8V, $C_L \leq 15$ pF			9	ns
TRRC	Read Clock Rise Time	0.8V to 2.0V, $C_L \leq 15$ pF			8	ns
TFRC	Read Clock Fall Time	2.0V to 0.8V, $C_L \leq 15$ pF			5	ns
RRC	Duty Cycle	10 - 20 Mbit/s	43	50	57	%
		>20 - 32 Mbit/s	40.8	50	59.2	%
TPNRZ	NRZ (out) Set Up/ Hold Time	10 - 20 Mbit/s	15.5			ns
		>20 - 24 Mbit/s	13			ns
		>24 - 32 Mbit/s	10			ns
KD	Decode Window Centering Accuracy			±1.5	ns	
	Decode Window		(2TORC/3) - 1.5		ns	

WRITE MODE (See Figure 4)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TWD	Write Data Pulse Width	$C_L \leq 15$ pF	2TOWC/3 -TPC -5		2TOWC/3 +TPC +5	ns
TFWD	Write Data Fall Time	2.0V to 0.8V, $C_L \leq 15$ pF			5	ns
TRWC	Write Data Clock Rise Time	0.8V to 2.0V			10	ns
TFWC	Write Data Clock Fall Time	2.0V to 0.8V			8	ns
TSNRZ	WDNRZ Set up Time		5			ns
THNRZ	WDNRZ Hold Time		5			ns

WRITE MODE (Continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TPC	Precompensation Time Shift Magnitude Accuracy	TPCO = 1.12T x A / (B + 3A) T = XTAL Period A = 0.19 / (Rc + 0.51) + 5.8E-3 B = 0.42 / (RR + 0.53) + 1.08E-2 $RC = \frac{0.19(1-2.7S)}{S[\frac{0.38}{RR+0.53)} + 0.025] - 0.006} - 0.51$ S = TPCO/T; RR, RC (kΩ) (Rc tied between WCS and +5V)				
		$\overline{WC0}$ = 1, $\overline{WC1}$ = 1	0	0		ns
		$\overline{WC0}$ = 0, $\overline{WC1}$ = 1		TPCO		ns
		$\overline{WC0}$ = 1, $\overline{WC1}$ = 0		2TPCO		ns
		$\overline{WC0}$ = 0, $\overline{WC1}$ = 0		3TPCO		ns

DATA SYNCHRONIZATION VCC = 5.0V; 32D5371/2: 2.15k ≤ RR ≤ 7.6k; 32D5373/4: 2.60k ≤ RR ≤ 7.6k

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TVCO	VCO Center Frequency Period	VCO_IN = 2.7V 32D5371/5372 TO = 3.6 (RR + 1.7) 32D5373/5374 TO = 2.4 (RR + 1.7)	0.8 TO		1.2 TO	ns
VCO	Frequency Dynamic Range	1V ≤ VCO_IN ≤ VCC-0.6V	±25		±45	%
KVCO	VCO Control Gain	ωo = 2π/TVCO 1V ≤ VCO_IN ≤ VCC 0.6V	0.14 ωo		0.26 ωo	rad/s-V
KD	Phase Detector Gain*	KD= 0.66/(RR+530) Read Mode = 0.33/(RR+530) Non-Read Mode Indirectly tested	0.83 KD		1.17 KD	μA/rad
	KVCO x KD Product Accuracy*	Indirectly tested	-28		-28	%
	VCO Phase Restart Error*	Referred to RRC Indirectly tested	-1		1	rad
TPAMD	$\overline{AMD}$ Propogation Delay	10 - 24 Mbit/s >24 - 32 Mbit/s	13 10			ns ns
	1/3 Cell Delay	TD = 3.6 (RR+1.7): 32D5371/2 TD = 2.4 (RR+1.7): 32D5373/4	0.8TD		1.2TD	ns

CONTROL CHARACTERISTICS (See Figure 5)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TSWS	$\overline{WC0}$, $\overline{WC1}$ SET UP TIME		7			ns
THWS	$\overline{WC0}$, $\overline{WC1}$ HOLD TIME		7			ns

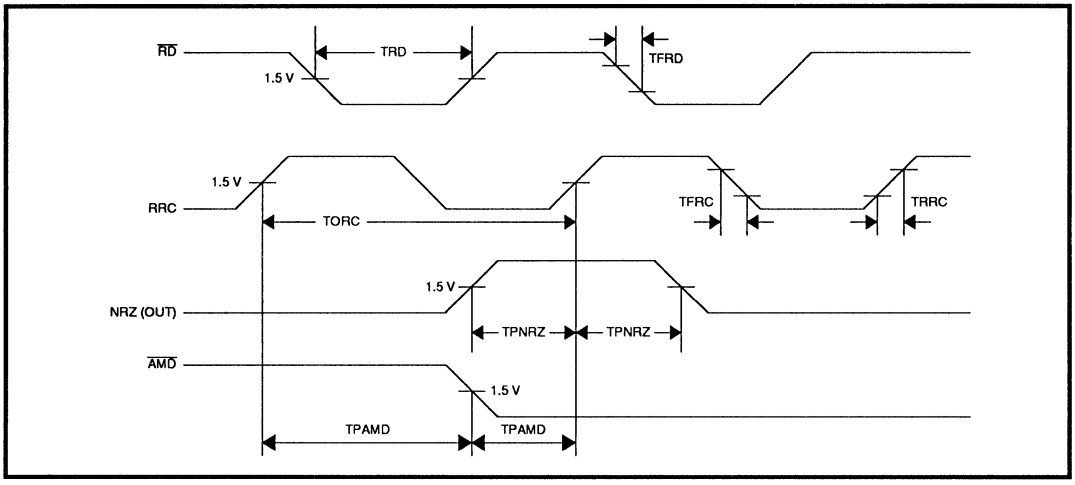


FIGURE 3: Read Timing

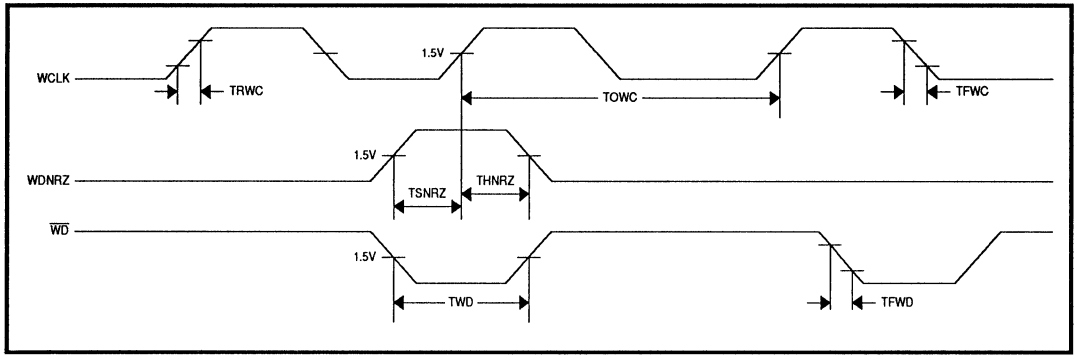


FIGURE 4: Write Timing

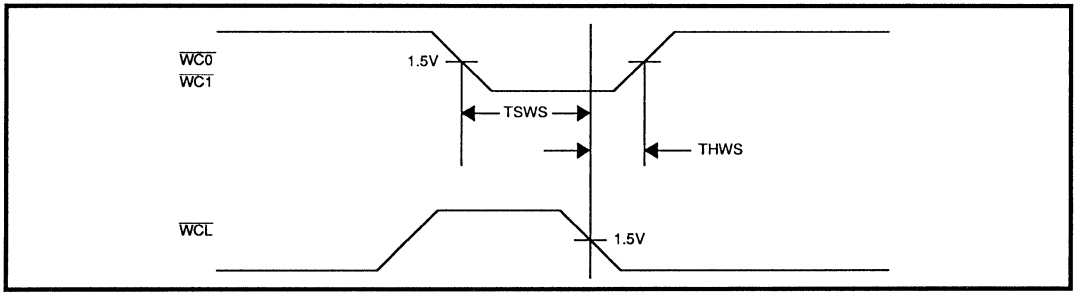


FIGURE 5: Control Timing

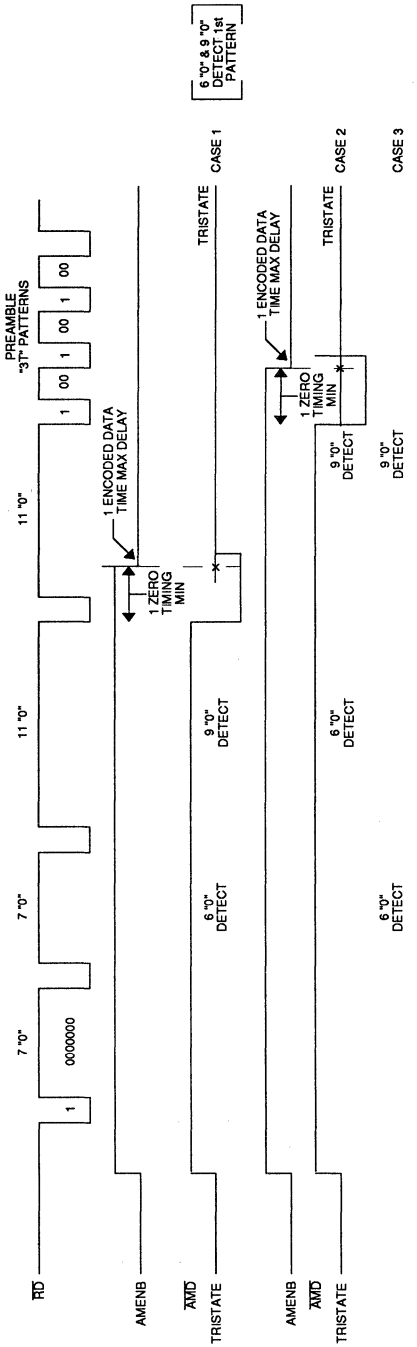


FIGURE 6: Address Mark Search

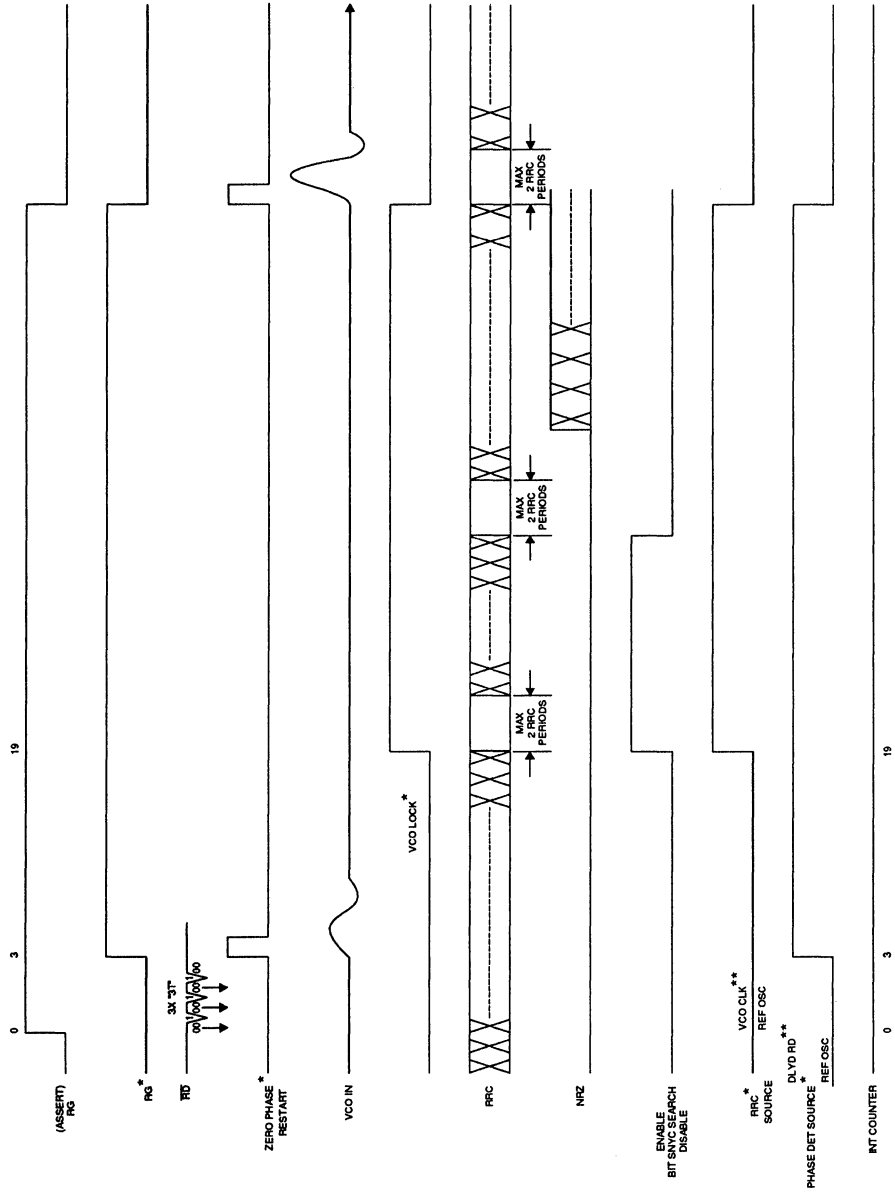


FIGURE 7: Read Mode Locking Sequence (Soft and Hard Sector)

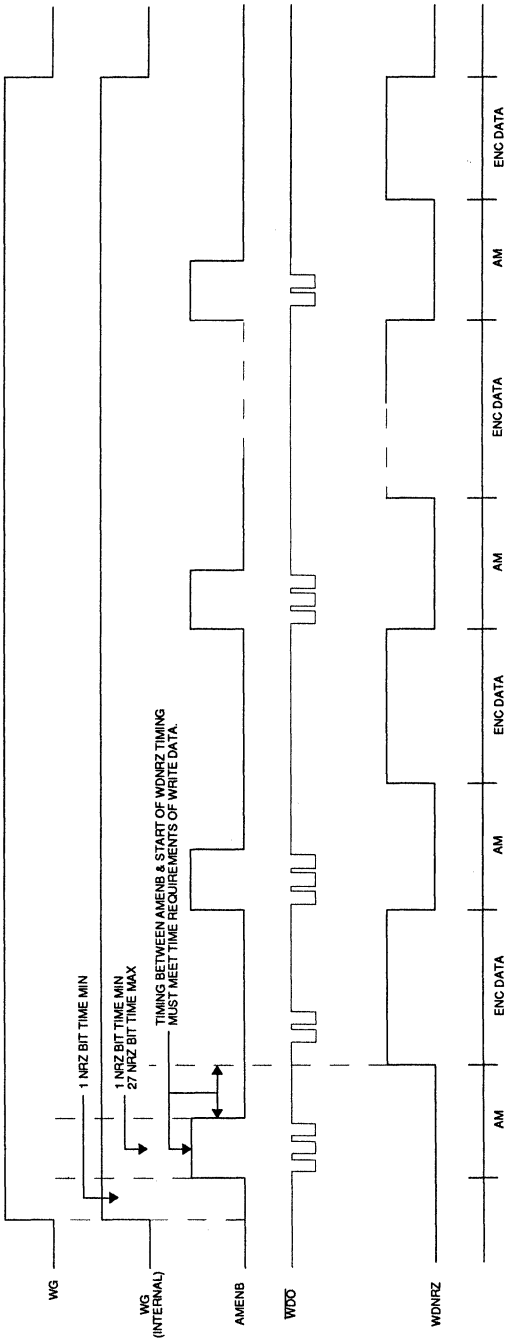


FIGURE 8: Multiple Address Mark Write

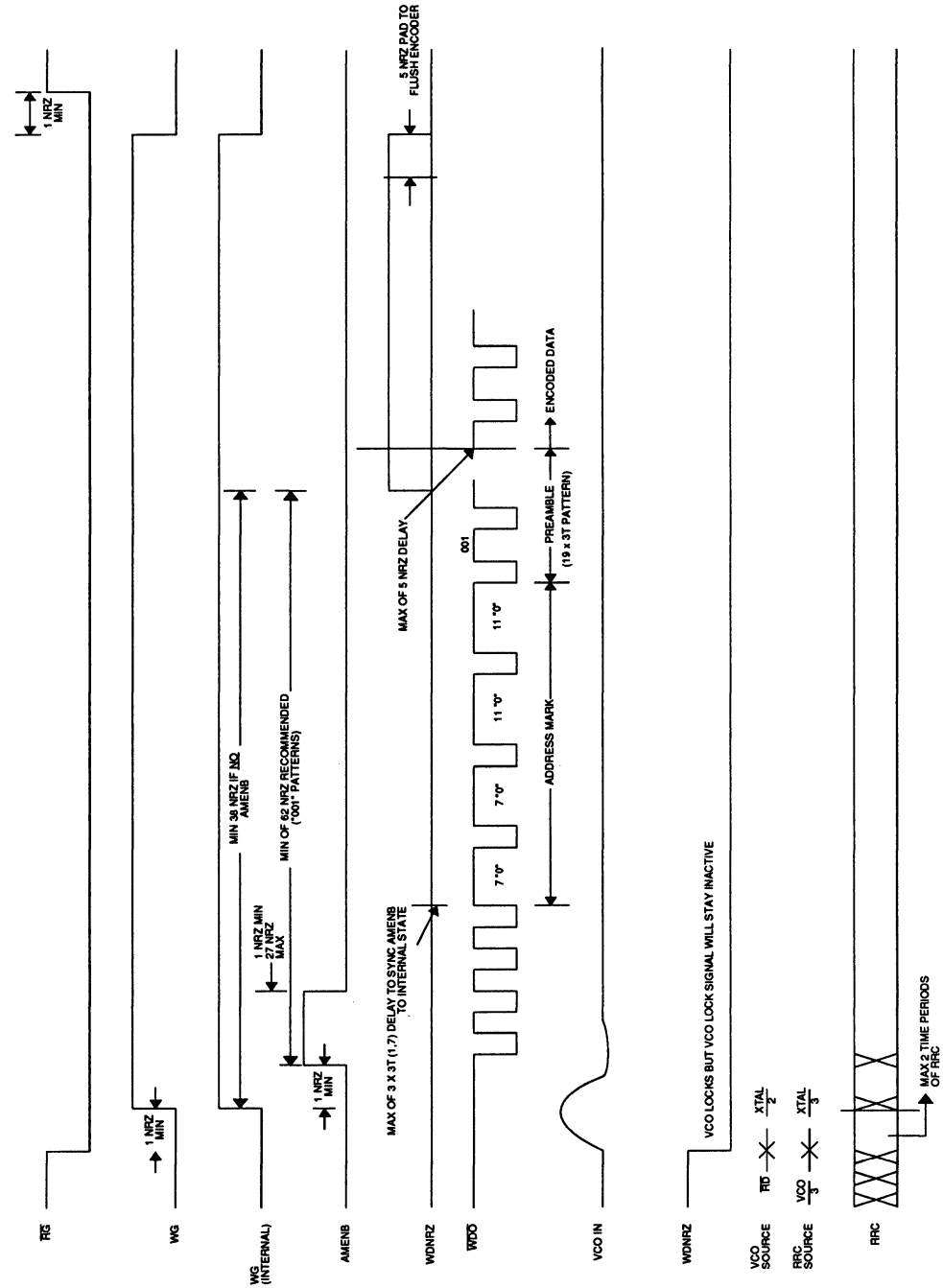
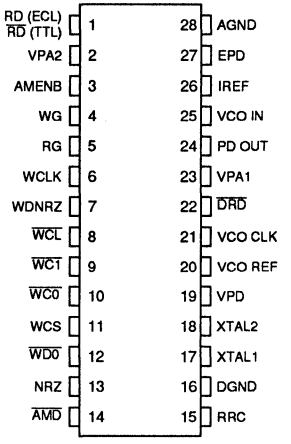


FIGURE 9: Write Data

SSI 32D5371/2/3/4
Data Synchronization/1, 7 RLL ENDEC with Write Precompensation

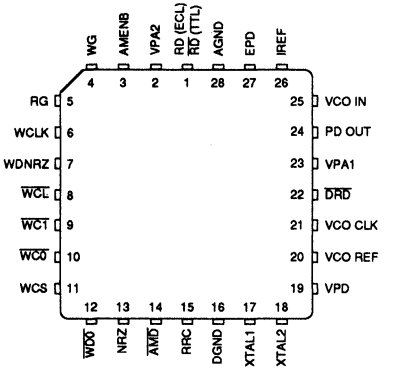
PACKAGE PIN DESIGNATIONS

(Top View)



28-Pin SOL

CAUTION: Use handling procedures necessary for a static sensitive component.



28-Pin PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDERING NUMBER	PACKAGE MARK
SSI 32D5371 Data Synchronization/1, 7 RLL ENDEC with Write Precompensation		
28-Pin SOL	32D5371-CL	32D5371-CL
28-PIN PLCC	32D5371-CH	32D5371-CH
SSI 32D5372 Data Synchronization/1, 7 RLL ENDEC with Write Precompensation		
28-Pin SOL	32D5372-CL	32D5372-CL
28-PIN PLCC	32D5372-CH	32D5372-CH
SSI 32D5373 Data Synchronization/1, 7 RLL ENDEC with Write Precompensation		
28-Pin SOL	32D5373-CL	32D5373-CL
28-PIN PLCC	32D5373-CH	32D5373-CH
SSI 32D5374 Data Synchronization/1, 7 RLL ENDEC with Write Precompensation		
28-Pin SOL	32D5374-CL	32D5374-CL
28-PIN PLCC	32D5374-CH	32D5374-CH

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 731-7110, FAX (714) 573-6914

silicon systems®
A TDK Group Company

SSI 32D539
Data Synchronizer & 1, 7 RLL ENDEC

Preliminary Data

December 1991

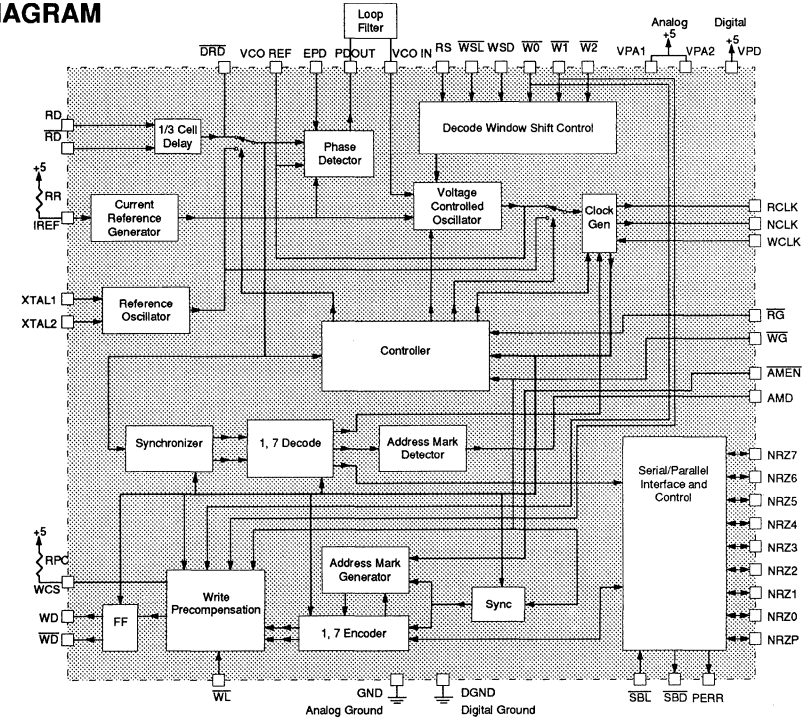
DESCRIPTION

The circuit is intended to be used as a data/clock recovery circuit for 1, 7 RLL code in hard disk drive systems with a +5V supply.

FEATURES

- **Data synchronizer and 1, 7 RLL ENDEC**
- **9-bit bi-directional data bus interface**
  - **8 data bits plus 1 parity bit**
  - **Parity generation during read operation**
  - **Parity checking during write operation**
- **Up to 48 Mbit/s operation**
  - **Data rate programmed with a single external resistor or current source**
- **Programmable Sync-Byte pattern detection**
- **Fast acquisition phase locked loop with zero phase restart technique**
- **Fully integrated data separator**
  - **No external delay lines or active devices required**
- **Programmable decode window symmetry control**
  - **Includes delayed read data and VCO clock monitor points**
- **Programmable write precompensation**
- **Hard and soft sector operation**
- **Uses standard 5V ± 5% supply**
- **44-pin PLCC package**

BLOCK DIAGRAM



OPERATION

DATA/CLOCK RECOVERY CIRCUIT

The circuit is designed to perform data recovery and data encoding in rotating memory systems which utilize a 1, 7 RLL encoding format. In the read mode the circuit performs data synchronization, sync field search and detect, address mark detect, and data decoding. In the write mode, the circuit converts NRZ data into the 1, 7 RLL format described in Table 1, performs write precompensation, generates the preamble field and inserts address marks as requested.

This data rate is established by a single 1% external resistor, RR, connected from the IREF pin to VPA. This resistor establishes a reference current which sets the VCO center frequency, the phase detector gain, and the 1/3 cell delay. The value of this resistor is given by:

$$RR = \frac{185}{DR} - 1.7k\Omega$$

Where: DR = data rate in Mbit/s

Alternately, the IREF pin can be driven from the SSI 32D4660 in a constant density recording application.

The circuit employs a dual mode phase detector; harmonic in the read mode and non-harmonic in the write and idle modes. In the read mode, the harmonic phase detector updates the PLL with each occurrence of a DLYD DATA pulse. In the write and idle modes, the non-harmonic phase detector is continuously enabled, thus maintaining both phase and frequency lock. By acquiring both phase and frequency lock to the input reference frequency and utilizing a zero phase restart technique, false lock to DLYD DATA is eliminated.

The phase detector incorporates a charge pump in order to drive the loop filter directly. The polarity and width of the output current pulses correspond to the direction and magnitude of the phase error.

The READ GATE ($\overline{RG}$) and WRITE GATE ($\overline{WG}$) inputs control the mode of the data/clock recovery section of the chip.

$\overline{RG}$ is an asynchronous input and may be initiated or terminated at any position on the disk. $\overline{WG}$ is also an asynchronous input, but should not be terminated prior to the last output write data pulse.

READ OPERATION

The data synchronizer utilizes a fully integrated fast acquisition PLL to accurately develop the decode window. Read gate, $\overline{RG}$, initiates the PLL locking sequence and selects the PLL reference input; a low level (read mode) selects the $\overline{RD}$ input and a high level selects the external reference clock.

In the read mode the falling edge of $\overline{DRD}$ enables the phase detector while the rising edge is phase compared to the rising edge of VCO. As depicted in Figure 1, $\overline{DRD}$ is a 1/3 cell wide (TVCO/2) pulse whose leading edge is defined by the leading edge of $\overline{RD}$. A decode window is developed from the VCO clock.

Shifting the symmetry of the VCO clock effectively shifts the relative position of the DRD pulse within the decode window. Decode window control is provided via the WS controls.

In the non-read modes, the PLL is locked to the external reference clock. When the reference input to the PLL is switched, the VCO is stopped momentarily, then restarted in an accurate phase alignment with the next PLL reference input pulse, and the VCO clock divider is reset.

ADDRESS MARK DETECT

In soft sector read operation the circuit must first detect an address mark to be able to initiate the rest of the read lock sequence. An address mark consists of two sets

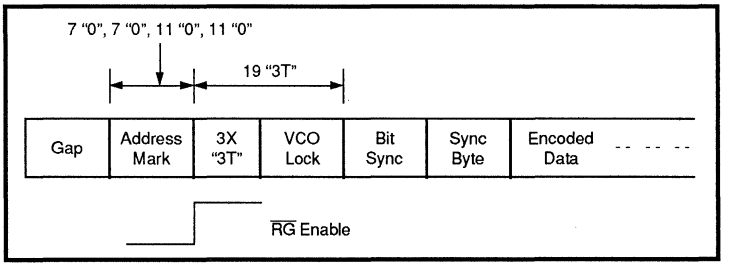


FIGURE 1: Disk Operation Lock Sequence in Read Mode Soft Sector Operation

of 7 "0" patterns followed by two sets of 11 "0" patterns. To begin the read lock sequence the Address Mark Enable ($\overline{AMEN}$) is asserted low by the controller. The address mark detect ($\overline{AMD}$) circuit then initiates a search of the read data ($\overline{RD}$) for an address mark. First the $\overline{AMD}$ looks for a set of 6 "0"s within the 7 "0" patterns. Having detected a 6 "0" the $\overline{AMD}$ then looks for a 9 "0" set within the 11 "0"s. If $\overline{AMD}$ does not detect 9 "0"s within 5 $\overline{RD}$ bits after detecting 6 "0"s it will restart the address mark detect sequence and look for 6 "0"s. When the $\overline{AMD}$ has acquired a 6 "0," 9 "0" sequence, the $\overline{AMD}$ transitions low.

PREAMBLE SEARCH

After the Address Mark (AM) has been detected, a Read Gate ($\overline{RG}$) can be asserted low, initiating the remainder of the read lock sequence. When $\overline{RG}$ is asserted, an internal counter counts negative transitions of the incoming read data ($\overline{RD}$) looking for 3 consecutive 3T preambles. Once the counter reaches count 3 (finds 3 consecutive 3T preambles) the internal read gate enables, switching the phase detector from the external reference clock to the delayed read data input ($\overline{DRD}$); at the same time a zero phase (internal) restart signal restarts the VCO in phase with the read reference clock. This prepares the VCO to be synchronized to data when the bit sync circuitry is enabled after VCO lock is established.

VCO LOCK AND BIT SYNC ENABLE

When the internal counter counts 16 more "3T" or a total of 19 negative transitions from RG enable, an internal VCO lock signal enables. The VCO lock signal activates the decoder bit synchronization circuitry to define the proper decode boundaries. Also, at count 19, the RRC source switches from the external reference clock to VCO clock signal which is phase locked to $\overline{DRD}$. The VCO is assumed locked at this point. A maximum of 2 RRC time periods may occur for the RRC transition, however, no short duration glitches will occur. After the bit sync circuitry sets the proper decode window (VCO in sync with RRC and RRC in sync with the data) NRZ is enabled and data is toggled in to be decoded for the duration of the read gate.

BYTE SYNC AND NRZ OUT

As the data is decoded, it is compared to a Sync Byte that was loaded prior to the read operation. When a match is found, RCLK and NCLK are resynchronized to the correct byte boundary. NRZ data then appears at the byte output beginning with the sync byte. The $\overline{SBD}$ output is also set low at this time. It remains low until the end of the read operation. A parity bit (NRZP) is also generated for each output byte (even parity).

HARD SECTOR OPERATION

In hard sector operation AMD remains inactive. A hard sector read operation does not require an address mark search but starts with a preamble search as with soft sector and sequences identically. In all respects, with exception to the address mark search sequence, hard sector read operation is the same as soft sector read.

WRITE MODE

In the write mode the circuit converts NRZ data from the controller into 1, 7 RLL formatted data for storage on the disk. The circuit can operate with a soft or hard sector hard drive.

In soft sector operation the circuit generates a "7, 7, 11, 11" address mark and a preamble pattern. In hard sector operation the circuit generates a 19 x "3T" preamble pattern but no preceding address mark.

NRZ data is clocked into the circuit, serialized and latched on defined cell boundaries. The NRZ input data must be synchronous with the rising edges of the WCLK.

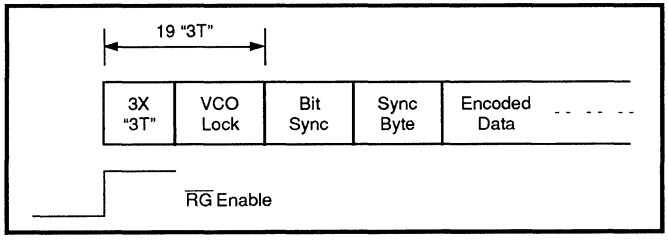


FIGURE 2: Disk Operation Lock Sequence in Read Mode Hard Sector Operation

WRITE MODE (Continued)

Write precompensation circuitry is provided to compensate for media bit shift caused by intersymbol interference. The circuit recognizes specific write data patterns and can add or subtract delays in the time position of write data bits to counteract the read back bit shift. The magnitude of the time shift, TPC, is determined by an external resistor on the WCS pin.

The circuit performs write precompensation according to the algorithm outlined in Table 3.

SOFT SECTOR

In soft sector operation, when read gate ($\overline{RG}$) transitions high, VCO source and RRC source switch from $\overline{RD}$ and 2VCO/3, respectively, to the external reference clock. At the same time the VCO (internal) lock goes inactive but the VCO is locked to the external reference clock. After delay of 1 NRZ time period (min) from $\overline{RG}$ high, the write gate ($\overline{WG}$) can be enabled low while NRZ is maintained (NRZ write data) low. The address mark enable ($\overline{AMEN}$) is made active (low) a minimum of 1 NRZ time period later. The address mark (consisting of 7 "0"s, 7 "0"s, 11 "0"s, 11 "0"s) and the 19 x "3T" preamble is then written by WD. While the preamble is being written, WCLK is clocking in an all "0" NRZ byte. The first non-zero NRZ byte input is assumed to be the sync byte. After a delay of 5 NRZ time periods, non-preamble data begins to toggle out WD. Finally, at the end of the write cycle, 2 bytes of blank NRZ time passes to insure the encoder is flushed of data; $\overline{WG}$ then goes high. WD stops toggling a maximum of 2 NRZ time periods after $\overline{WG}$ goes high.

As each NRZ byte is input for encoding, its parity is checked against the parity bit (NRZP). If a parity error is detected the PERR output flag is set high. It remains high until WG goes high.

HARD SECTOR

In hard sector operation, when read gate ($\overline{RG}$) transitions high, VCO source and RRC switch references and VCO lock (internal) goes inactive as with soft sector but the $\overline{AMEN}$ (address mark enable) is kept high.

The circuit then sequences from $\overline{RG}$ disable to $\overline{WG}$ enable and NRZ active as in soft sector operation.

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
VPA1, VPA2	I	5 volt analog power supply pins
VPD	I	5 volt digital power supply pin
AGND	O	Analog ground pin
DGND	O	Digital ground pin
$\overline{AMEN}$	I	ADDRESS MARK ENABLE: Used to enable the address mark detection and address mark generation circuitry. Active low TTL input levels.
EPD	I	ENABLE PHASE DETECTOR: A low level (coast mode) disables the phase detector and enables the Test Mode. This opens the PLL and the VCO will run at the frequency commanded by the voltage on the VCO IN pin. (In the Test Mode, functions normally driven by the VCO are switched to XTAL.) Pin EPD has an internal pull-up resistor. TTL input levels.
RD, $\overline{RD}$	I	READ DATA: Encoded Read Data from the disk drive read channel. Differential +5 volts offset ECL (PECL) input levels.
$\overline{RG}$	I	READ GATE: Selects the PLL reference input and initiates the PLL synchronization sequence. A low level selects the RD input and enables the read mode/address detect sequences. A high level selects the XTAL input. See Table 2, TTL input levels.
$\overline{SBL}$	I	SYNC BYTE LATCH CONTROL: Used to latch the Sync Byte reference value into the internal Sync Byte comparator. During idle mode, the Sync Byte latch is transparent while $\overline{SBL}$ is high. An active low level latches the input Sync Byte. The Sync Byte latch is kept in a hold state during non-idle modes, independent of the state of the $\overline{SBL}$ control. Pin $\overline{SBL}$ has an internal pull-up resistor. TTL input levels.

PIN DESCRIPTION (Continued)

NAME	TYPE	DESCRIPTION
$\overline{W0}$, $\overline{W1}$, $\overline{W2}$	I	WRITE/WINDOW CONTROL BITS: In Write Mode, pins $\overline{W0}$ and $\overline{W1}$ control the magnitude of the write precompensation (see Table 4). In Read Mode, pins $\overline{W0}$ and $\overline{W1}$, $\overline{W2}$ control the magnitude of the decode window shift. Each pin has an internal pull-up resistor. TTL input levels.
$\overline{WL}$	I	WRITE PRECOMPENSATION LATCH CONTROL: Used to latch the write precompensation control bits $\overline{W0}$ and $\overline{W1}$ into the internal DAC. The latch is transparent while $\overline{WL}$ is high. An active low level latches the input control bits. Pin $\overline{WL}$ has an internal pull-up resistor. TTL input levels.
WCLK	I	WRITE CLOCK: Write mode byte clock. Must be synchronous with the Write Data NRZ input. For short cable delays, WCLK may be connected directly to pin RCLK. For long cable delays, WCLK should be connected to an RCLK return line matched to the NRZ data bus line delay. TTL input levels.
$\overline{WG}$	I	WRITE GATE: Enables the write mode. See Table 2. Active low TTL input levels.
WSD	I	WINDOW SYMMETRY DIRECTION CONTROL: Controls the direction of the decode window shift. Each pin has an internal pull-up resistor. TTL input levels.
$\overline{WSL}$	I	WINDOW SYMMETRY LATCH CONTROL: Used to latch the window symmetry control bits $\overline{W0}$, $\overline{W1}$, $\overline{W2}$ and WSD into the internal DAC. The latch is transparent while $\overline{WSL}$ is high. An active low level latches the input control bits. Pin $\overline{WSL}$ has an internal pull-up resistor. TTL input levels.
$\overline{AMD}$	O	ADDRESS MARK DETECT: Tristate output pin that is in its high impedance state when WG is low or $\overline{AMEN}$ is high. When $\overline{AMEN}$ is low, this output indicates address mark search status. A latched low level output appears when an address mark has been detected. A high level on pin $\overline{AMEN}$ resets pin $\overline{AMD}$. TTL output levels.
$\overline{DRD}$	O	DELAYED READ DATA: An open emitter ECL output test point. The positive edges of this signal indicate the data bit position. The positive edges of the $\overline{DRD}$ and VCO_REF outputs can be used to estimate window centering. The time jitter of $\overline{DRD}$'s positive edge is an indication of media bit jitter. Two external resistors are required to use this pin. They should be removed during normal operation to reduce power dissipation.
NCLK	O	NIBBLE CLOCK: A half-byte clock synchronized to RCLK. It runs at twice the RCLK frequency. TTL output levels.
PERR	O	PARITY ERROR FLAG: Active during write mode and during Sync Byte loading. When $\overline{WG}$ is low, the contents of the NRZ write data input register is examined and compared with the NRZP write data parity bit. Even parity is assumed. For example, PERR becomes active when NRZ7-0 and NRZP are all high. Parity checking is performed after each WCLK load operation. If the input data contains a parity error, or if the WCLK timing causes the input register to contain a parity error, an internal write parity error flag is set. If a parity error occurs during a write operation, the Write Data encoding will continue to function normally. This error flag is reset low when $\overline{WG}$ goes high. Independent of $\overline{WG}$, a separate circuit monitors the Sync Byte. Each time $\overline{SBL}$ transitions from high to low, the contents of the Sync Byte latch is compared with the NRZP data parity bit. If a parity error exists, an internal Sync Byte parity error flag is set. This flag is reset low when $\overline{SBL}$ goes high. The PERR output displays the write parity flag condition when $\overline{WG}$ is low. When $\overline{WG}$ is high, PERR outputs the state of the Sync Byte parity error flag. TTL output levels.

PIN DESCRIPTION (Continued)

NAME	TYPE	DESCRIPTION
RCLK	O	READ CLOCK: A multiplexed byte clock source used by the controller, see Table 2. During a mode change, no glitches are generated and no more than one lost clock pulse will occur. When $\overline{RG}$ goes low, RCLK initially remains synchronized to XTAL/12. When the Sync Byte is detected, RCLK is synchronized to the Read Data. When $\overline{RG}$ goes high, RCLK is synchronized back to the XTAL/12. TTL output levels.
$\overline{SBD}$	O	SYNC BYTE DETECT: A TTL output that transitions low upon detecting a Sync Byte. This transition is synchronized to the first NRZ byte out following the sync byte. Once it transitions, $\overline{SBD}$ remains low until $\overline{RG}$ is raised, when it is returned to a high state.
VCO REF	O	VCO REFERENCE: An open emitter ECL output test point. This is the VCO reference input to the phase detector. The positive edges are phase locked to Delayed Read Data. The negative edges of this open emitter output signal indicate the edges of the decode window. Two external resistors are required to use this pin. They should be removed during normal operation to reduce power dissipation.
WD, $\overline{WD}$	O	WRITE DATA: Encoded write data flip-flop output. The data is automatically resynchronized (independent of the delay between RCLK and WCLK) to the XTAL reference clock. Differential +5 volts offset ECL (PECL) output levels.
NRZ0-7	I/O	NRZ DATA PORT: Read data output when $\overline{RG}$ is low, write data input when $\overline{WG}$ is low, and Sync Byte input when both $\overline{RG}$ and $\overline{WG}$ are high. TTL input and output levels.
NRZP	I/O	NRZ DATA PARITY BIT: Generated read data parity bit output when $\overline{RG}$ is low, write data parity bit input when $\overline{WG}$ is low, and Sync Byte parity bit input when both $\overline{RG}$ and $\overline{WG}$ are high. In read mode, even parity is generated. For example, when NRZ7-0 are all high, NRZP will be set low. TTL input and output levels.

ANALOG PINS

IREF	I	CURRENT REFERENCE INPUT: The VCO center frequency, the 1/3 cell delay, and the phase detector gain are a function of the current sourced into this pin.
PD OUT	I/O	PHASE DETECTOR OUTPUT: Drives the loop filter input.
RS	I	WINDOW SYMMETRY ADJUST PIN: This pin allows analog adjustment of the decode window shift magnitude. Used in conjunction with the digital controls $\overline{W0}$ and $\overline{W1}$, $\overline{W2}$ this pin can be used to scale the magnitude of the preset window shift. Connect resistor to VPA.
VCO IN	I/O	VCO CONTROL INPUT: Driven by the loop filter output.
WCS	I	WRITE PRECOMPENSATION SET: Pin for the reference current to set the write precompensation magnitude value.
XTAL1, 2	I	REFERENCE FREQUENCY INPUT: The pin frequency is at one and one-half times the data rate. If a crystal oscillator is used, an AC coupled parallel LC circuit must be connected from XTAL1 to ground. The crystal is connected between XTAL1 and XTAL2. If a crystal oscillator is not desired, XTAL1 may be driven either by a direct coupled TTL signal or by an AC coupled ECL signal, with XTAL2 open.

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, 4.75V < VPA/VPD < 5.25V, 0 °C < T(ambient) < 70 °C, 25 °C < T(junction) < 135 °C. Currents flowing into the chip are positive. Current maximums are currents with the highest absolute value.

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device

PARAMETER	RATING	UNIT
Supply Voltage, VPA1, VPA2, VPD	-0.3 to 6	V
Storage Temperature	-65 to 150	°C
Lead Temperature (Soldering 10 sec.)	260	°C
NRZ0 - NRZ7, RCLK, NCLK, WDT, $\overline{WDT}$, AMFND, SBFND, VCOREF, DRD Pins	-0.3 to (VPA/VPD+0.3), or +12	V mA
All other pins	-0.3 to (VPA/VPD+0.3)	V

POWER SUPPLY CURRENTS AND POWER

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
ICC (VPA, VPD) Supply Current	Outputs and test point pins open, Ta = 70 °C		200	230	mA
PWR Power Dissipation	Outputs and test point pins open, Ta = 70 °C		1.0	1.2	W

DIGITAL INPUTS AND OUTPUTS

TTL Compatible Inputs: $\overline{AMENB}$, EPD, NRZ0-NRZ7 (bid.), NRZP (bid.), $\overline{RG}$, $\overline{SBL}$, $\overline{W0}$, $\overline{W1}$, $\overline{W2}$, $\overline{WL}$, WCLK, $\overline{WG}$, WSD, $\overline{WSL}$ Pins

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Input Low Voltage (VIL)		-0.3		0.8	V
Input High Voltage (VIH)		2.0		VPD+0.3	V
Input Low Current	VIL = 0.4 V	0.0		-0.4	mA
Input High Current	VIH = 2.4 V			100	µA

Note: "bid." means bi-directional

TTL Compatible Outputs $\overline{AMD}$, NCLK, NRZ0-NRZ7 (bid.), NRZP (bid.), PERR, RCLK, $\overline{SBD}$ Pins

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Output Low Voltage	Iol = 4.0 mA			0.5	V
Output High Voltage	Ioh = -400 µA	2.4			V

Digital Differential Inputs: RD, $\overline{RD}$ Pins

Input Low Voltage (VIL)		VPA-2.2		VIH-0.5	V
Input High Voltage (VIH)		VIL+0.5		VPA-0.5	V
Differential Voltage	$\lvert V_{RD} - V_{\overline{RD}} \rvert$	0.5			V
Input Low Current	VIL = Min	-100			µA
Input High Current	VIH = Max			+100	µA

Digital Differential Outputs: WD, $\overline{WD}$ Pins

Output Low Voltage	Iol = TBD	VPD-2.1			V
Output High Voltage	Ioh = TBD			VPD-0.7	V
Differential Voltage	$\lvert V_{WD} - V_{\overline{WD}} \rvert$	0.5			V

Test Point Output Levels

Test Point Output High Level $\overline{DRD}$, VCO REF	262Ω to VPA, 402Ω to GND VPA = 5V		VPA -0.85		V
Test Point Output Low Level $\overline{DRD}$, VCO REF	262Ω to VPA, 402Ω to GND VPA = 5V		VPA -1.75		V

DYNAMIC CHARACTERISTICS AND TIMING

READ MODE

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Read Data Pulse Width (TPRD)		10		(2)TVCO -10	ns
Read Data Rise Time (TRRD)	20% to 80%, CL ≤ 10 pF			5	ns
Read Data Fall Time (TFRD)	80% to 20%, CL ≤ 10 pF			5	ns
Read Clock Rise Time (TRRC)	0.8V to 2.0V, CL ≤ 15 pF			10	ns
Read Clock Fall Time (TFRC)	2.0V to 0.8V, CL ≤ 15 pF			8	ns
NCLK Rise Time (TRNC)	0.8V to 2.0V, CL ≤ 15 pF			10	ns
NCLK Fall Time (TFNC)	2.0V to 0.8V, CL ≤ 15 pF			8	ns
NRZ (out) Set Up & Hold Time (TDS, TDH)		30			ns
$\overline{SBD}$ Set up & Hold Time (TSBS, TSBH)		30			ns

READ MODE (Continued)

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
RCLK Pulse Width (TRD)	VCO re-sync	0.4 TORC		1.25 TORC	ns
	BYTE re-sync	0.4 TORC		1.6 TORC	ns
RCLK Duty Cycle		40		60**	%
NCLK Pulse Width (TQD)	Except during re-sync	(TORC/4)-5		(TORC/4)+5	ns
NCLK Pulse Width (TQD)	During re-sync	TORC/4-5		3TORC/4+5	ns
NCLK Skew (TQS)		-20		20	ns
RCLK Resync Period (Tdc2)		TORC		(2)TORC	ns
NCLK Resync Period (Tdc1)		TORC/2		TORC	ns
Decode Window Centering Accuracy				±0.75	ns
Decode Window		TVCO -0.75			ns

** Except during re-sync

WRITE MODE

Write Data Rise Time (TRWD)	20% to 80% Points 110Ω to VPD, 160Ω to DGND			5	ns
Write Data Fall Time (TFWD)	80% to 20% Points 110Ω to VPD, 160Ω to DGND			5	ns
Write Data Clock Rise Time (TRWC)	0.8V to 2.0V, CL ≤ 15 pF			10	ns
Write Data Clock Fall Time (TFWC)	2.0V to 0.8V, CL ≤ 15 pF			8	ns
NRZ Set Up Time (TSNRZ)		20			ns
NRZ Hold Time (THNRZ)		20			ns
Precompensation Time Shift Magnitude Accuracy (TPC)	TPCO = 0.22 (Rc + 0.53) Rc min=1 KΩ, Rc max=0.3TXTAL				
	$\overline{W0}$=1 $\overline{W1}$=1	-0.5		0.5	ns
	$\overline{W0}$=0 $\overline{W1}$=1	0.8 TPCO		1.2 TPCO	ns
	$\overline{W0}$=1 $\overline{W1}$=0	2 (0.8 TPCO)		2 (1.2 TPCO)	ns
	$\overline{W0}$=0 $\overline{W1}$=0	3 (0.8 TPCO)		3 (1.2 TPCO)	ns

DATA SYNCHRONIZATION

VCO Center Frequency Period (TVCO)	VCO IN=2.7V, VPA=VPD=5V TO=3.6 (RR+1.7), RR=(185/DR)-1.7K	0.8TO		1.2TO	ns
VCO Frequency Dynamic Range	1.0 V ≤ VCO IN ≤ VPA - 0.6V VPA=VPD = 5 V	± 25		± 45	%
VCO Control Gain (KVCO)	ωo = 2π/TVCO 1.0 V ≤ VCO IN ≤ VPA - 0.6V	0.14 ωo		0.26 ωo	rad/s V

DATA SYNCHRONIZATION (Continued)

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Phase Detector Gain (KD)	VPA=VPD=5V Read: KD=750/(RR + 0.53) Non-Read: KD=375/(RR + 0.53)	0.83KD		1.17KD	µA/rad
KVCO x KD Product Accuracy		-28		+28	%
VCO Phase Restart Error	Referred to RRC	-1		+1	rad
1/3 Cell Delay	VCC = 5.0V TD=1.8 (RR + 1.7); RR = kΩ	0.8TD		1.2TD	ns

CONTROL TIMING

$\overline{W0}$, $\overline{W1}$, WSD Set Up and Hold Time (TSWC, THWC)		20			ns
$\overline{WL}$, $\overline{WSL}$ Pulse Width (TWL)		50			ns
Sync Byte NRZ Set Up and Hold Time (TSSB, THSB)		20			ns
$\overline{SBL}$ Pulse Width (TSB)		50			ns
Sync Byte Parity Error Output Delay (TDSE)		0		50	ns
Sync Byte Parity Error Reset Delay (TSER)		0		50	ns

MODE CONTROL

$\overline{WG}$	$\overline{RG}$	$\overline{AMENB}$	$\overline{SBL}$	Modes	
1	1	1	1	Idle (SB Enable)	Idle mode. VCO locked to external XTAL reference. Byte clock and 4-bit clock synchronized to XTAL. NRZ0-NRZ7 tri-stated. $\overline{AMD}$ high. SB latch transparent.
1	1	1	0	SB Load	SB latch in a hold state. Other conditions same as idle mode.
1	1	0	X	AM Search	Read mode Address Mark search. VCO locked to external XTAL reference. Byte clock and 4-bit clock synchronized to XTAL. NRZ0-NRZ7 tri-stated. $\overline{AMD}$ active.
1	0	1	X	Read Data	Read mode preamble search and data acquisition. VCO switched from XTAL to RD after preamble lock. Byte clock and 4-bit clock synchronized to RD after Sync Byte found. NRZ0-NRZ7 active. $\overline{SBD}$ active.
1	0	0	X	Undefined	Illegal state.
0	1	0	X	Write AM	Write mode Address Mark insertion. VCO locked to external XTAL reference. Byte clock and 4-bit clock synchronized to XTAL. WD, $\overline{WD}$ active. NRZ0-NRZ7 tri-stated. $\overline{AMD}$ high.
0	1	1	X	Write Data	Write mode preamble insertion and data write. VCO locked to external XTAL reference. Byte clock and 4-bit clock synchronized to XTAL. WD, $\overline{WD}$ active. NRZ0-NRZ7 tri-stated. $\overline{AMD}$ high.
0	0	1	X	Undefined	Illegal state.
0	0	0	X	Undefined	Illegal state.

WRITE PRECOMP CONTROL

$\overline{WL}$ - Write precomp latch control	$\overline{W1}$, $\overline{W0}$ - Write precomp magnitude control bits
0 → Write precomp control latches in hold state 1 → Write precomp control latches in transparent state	00 → 3x (maximum) shift 01 → 2x shift 10 → 1x shift 11 → No shift

WINDOW SHIFT CONTROL

$\overline{WSL}$ - Window shift latch control

0 → Window shift control latches in hold state

1 → Window shift control latches in transparent state

WSD - Window shift direction control

0 → Early window (+TS)

1 → Late window (-TS)

WINDOW SHIFT MAGNITUDE CONTROL BITS

$\overline{W2}$	$\overline{W1}$	$\overline{W0}$	TS0 (decode window %)
1	1	1	No shift
1	1	0	4% Minimum shift
1	0	1	8%
1	0	0	12%
0	1	1	15%
0	1	0	18%
0	0	1	20%
0	0	0	22% Maximum shift

Window shift with RRS used:	($2K\Omega \leq RRS \leq 16\ K\Omega$)
$TS = TSO\left(\frac{RRS}{RRS + 0.8}\right)$	TSO = Window shift set by $\overline{W0}$ - $\overline{W1}$ with no RRS

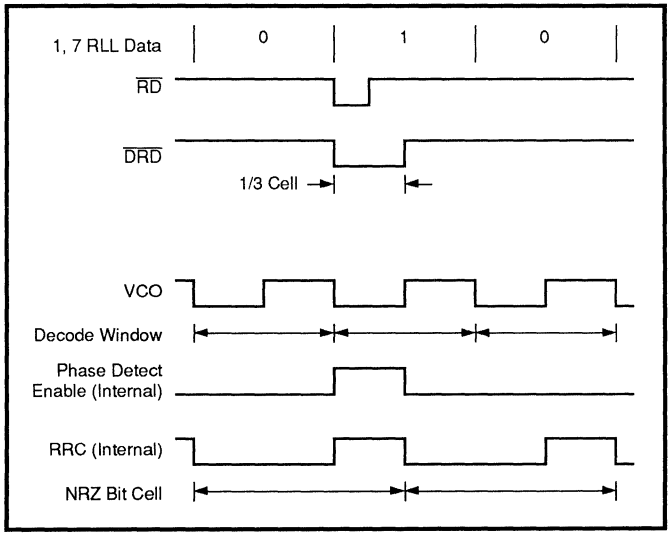


FIGURE 3: Data Synchronization Waveforms

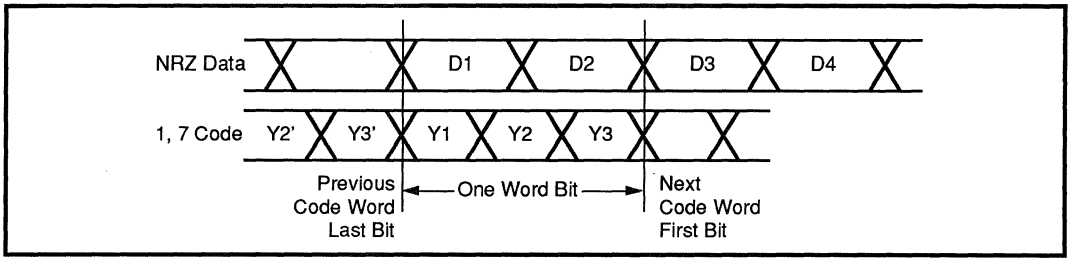


FIGURE 4: NRZ Data Word Comparison to 1, 7 Code Word Bit
(See Table 1 for Decode Scheme)

TABLE 1: 1, 7 RLL Code Set

Previous Code Word Last Bits		Data Bits Present			Next	Code Bits		
X	0	1	0	0	X	1	0	1
X	0	1	0	1	X	0	1	0
X	0	1	1	0	0	0	1	0
X	0	1	1	✶	✶	1	0	0
1	0	0	0	0	X	0	0	1
1	0	0	0	1	X	0	0	0
0	0	0	1	0	X	0	0	1
0	0	0	1	1	X	0	0	0
X	1	0	0	0	X	0	0	1
X	1	0	0	1	X	0	1	0
X	1	0	1	0	0	0	1	0
X	1	0	1	✶	✶	0	0	0
Y2'	Y3	D1	D2	D3	D4	Y1	Y2	Y3

X = Don't Care;
✶ = Not All Zeros

TABLE 2: Clock Frequency

$\overline{WG}$	$\overline{RG}$	VCO REF	RCLK	DECCLK	ENCCLK	MODE
1	1	XTAL	XTAL/12	XTAL	XTAL	IDLE
1	0	RD	VCO/12	VCO	XTAL	READ
0	1	XTAL	XTAL/12	XTAL	XTAL	WRITE

Notes 1: Until the VCO locks to the new source, the VCO entries will be XTAL.
2: Until the VCO locks to the new source, the VCO/12 entries will be XTAL/12.
3: $\overline{WG}$ = $\overline{RG}$ = 0 is undefined.

TABLE 3: Write Precompensation Algorithm

Bit n-2	Bit n-1	Bit n	Bit n+1	Bit n+2	Compensation Bit n
1	0	1	0	1	None
0	0	1	0	0	None
1	0	1	0	0	Early
0	0	1	0	1	Late

Notes Late: Bit n is time shifted (delayed) from its normal time position towards the Bit n+1 time position.
Early: Bit n is time shifted (advanced) from its normal time position towards the Bit n-1 time position.

TABLE 4: Write Precompensation Magnitude

$\overline{WC1}$	$\overline{WC0}$	Magnitude, TPC
0	0	3 (TPC0)
0	1	2 (TPC0)
1	0	TPC0
1	1	0

The normal magnitude TPC0 is externally set with a resistor on pin WCS.

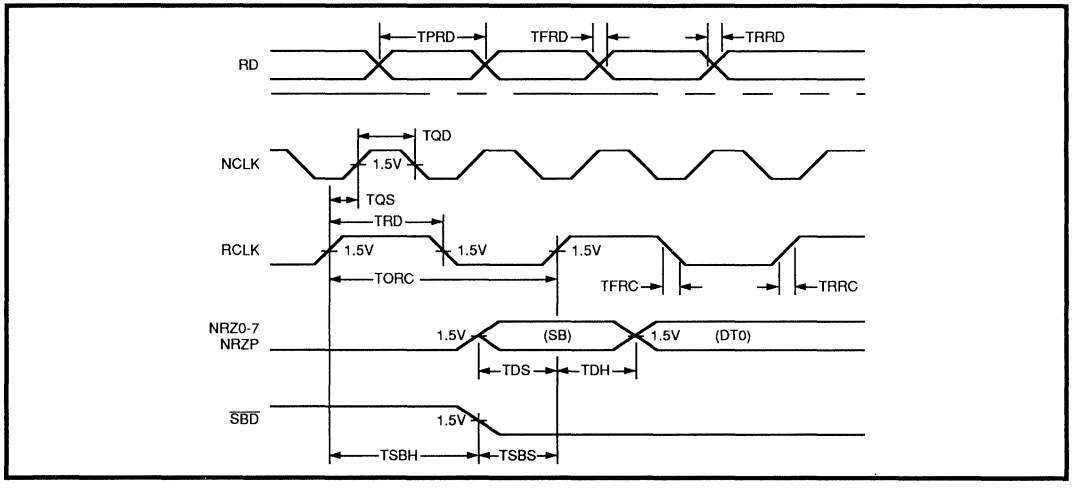


FIGURE 5: Read Timing

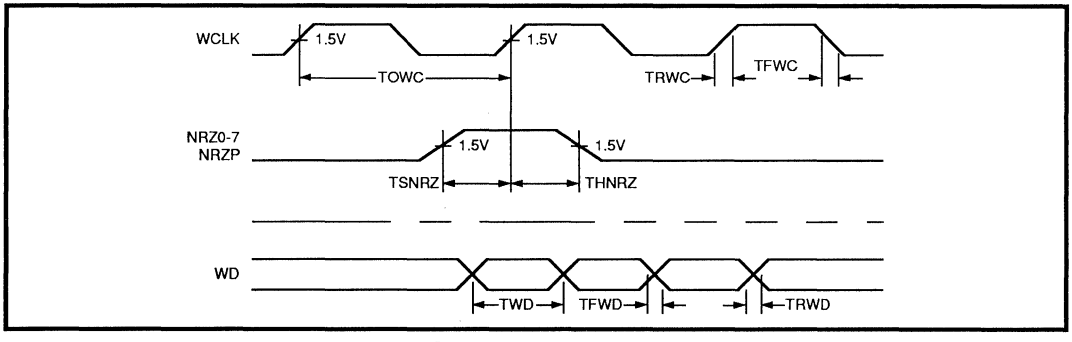


FIGURE 6: Write Timing

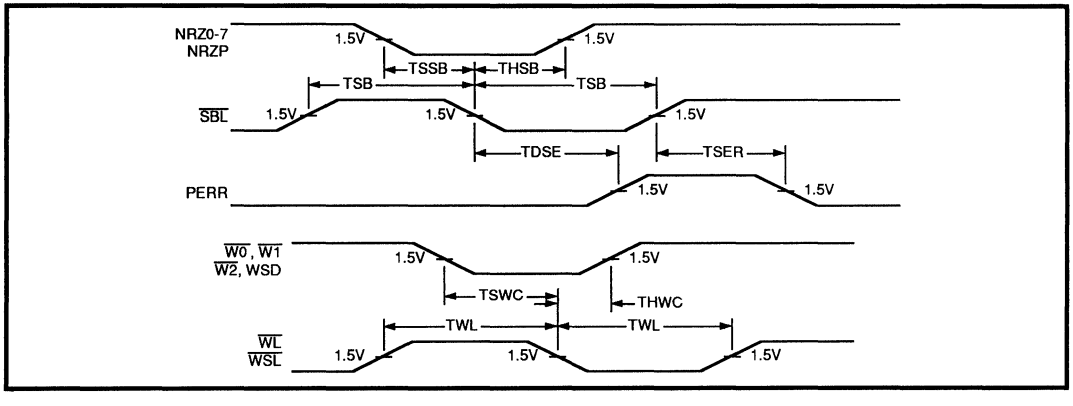


FIGURE 7: Control Timing

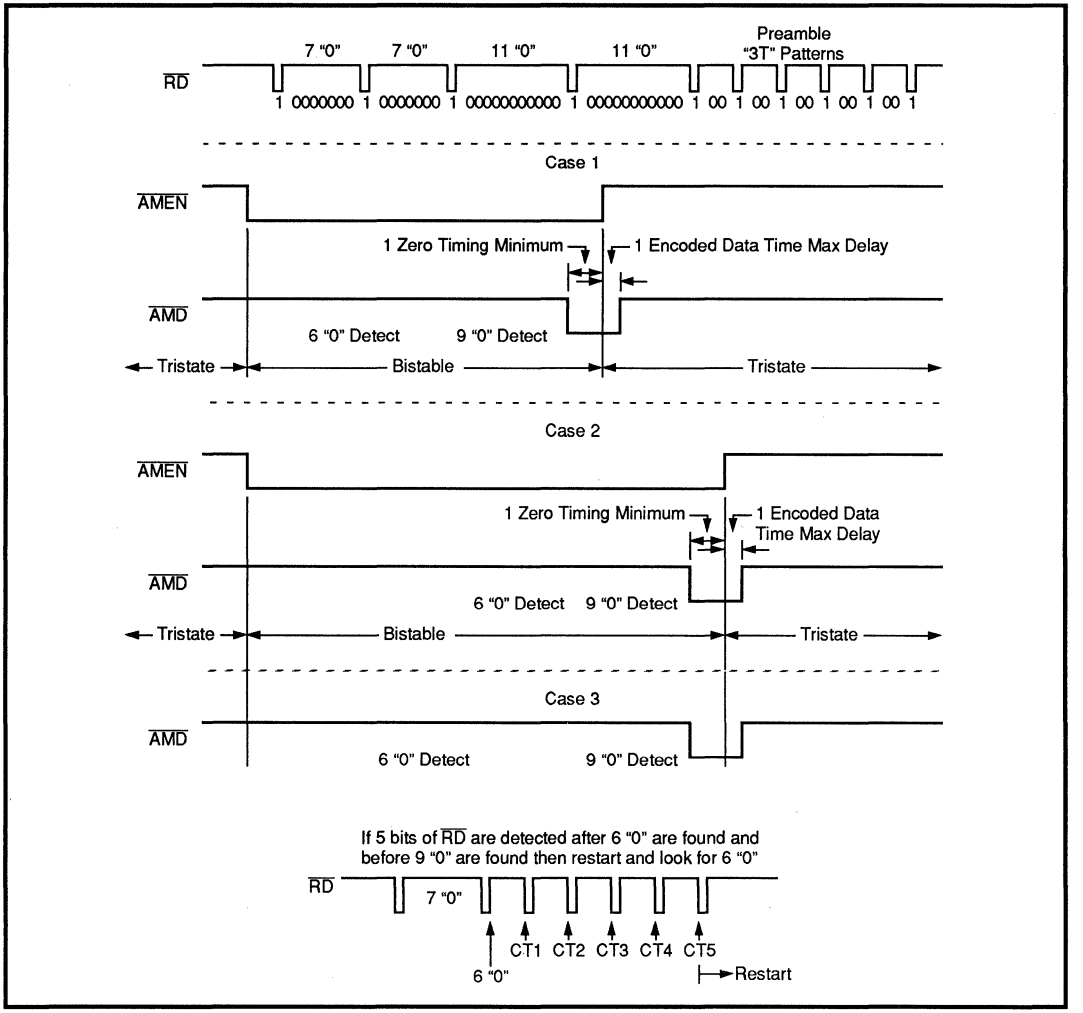


FIGURE 8: Address Mark Search

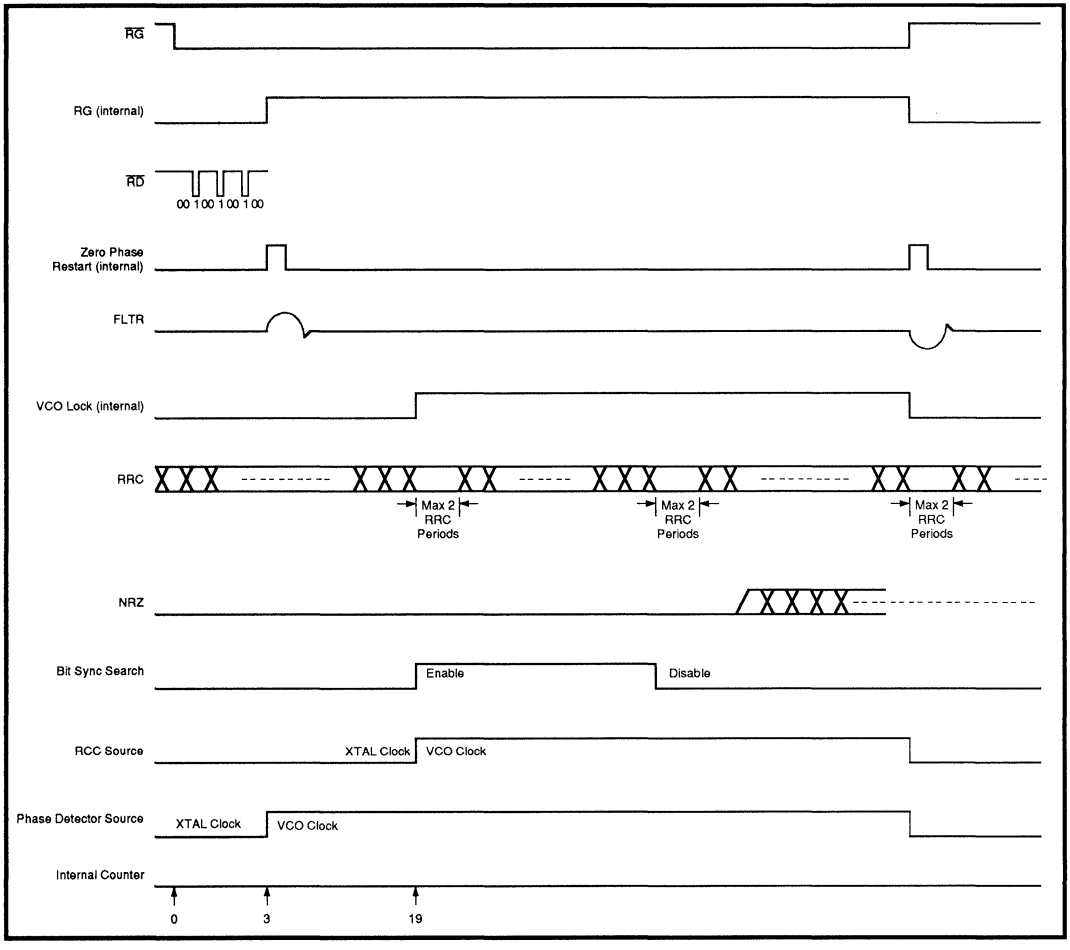


FIGURE 9: Read Mode Locking Sequence (Soft and Hard Sector)

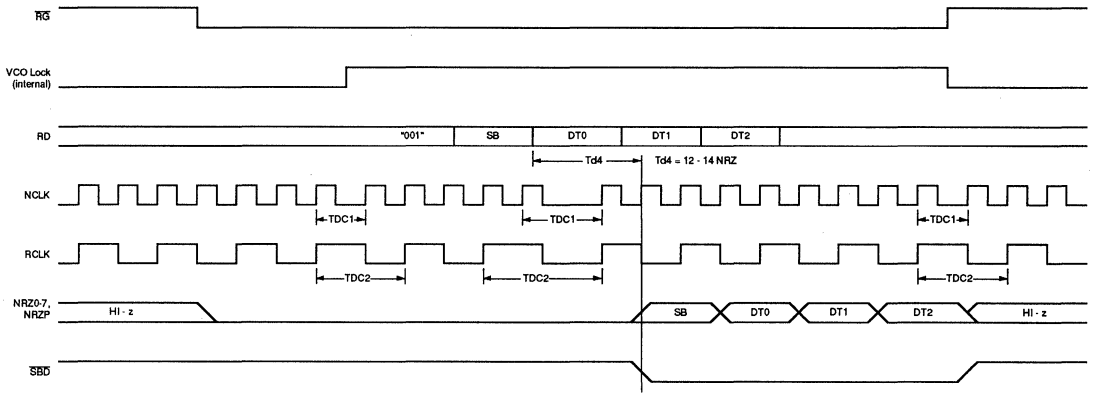


FIGURE 10: Read Mode NRZ Data Timing

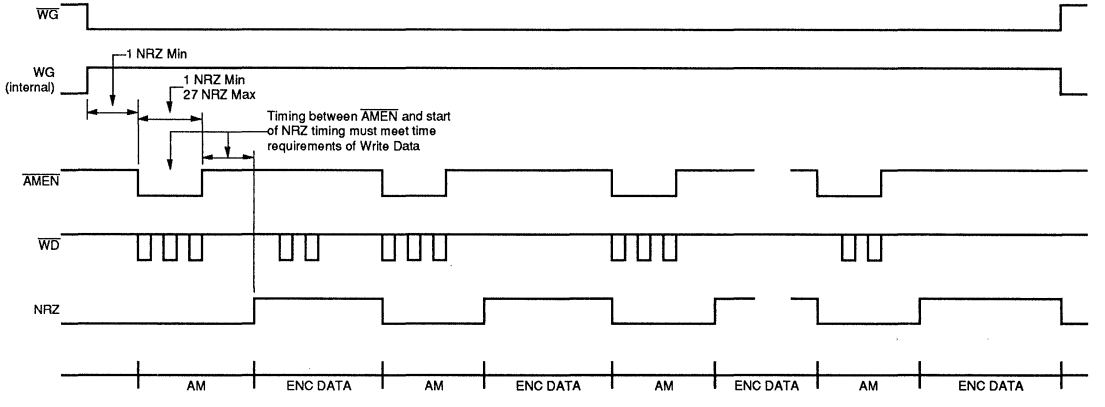


FIGURE 11: Multiple Address Mark Write

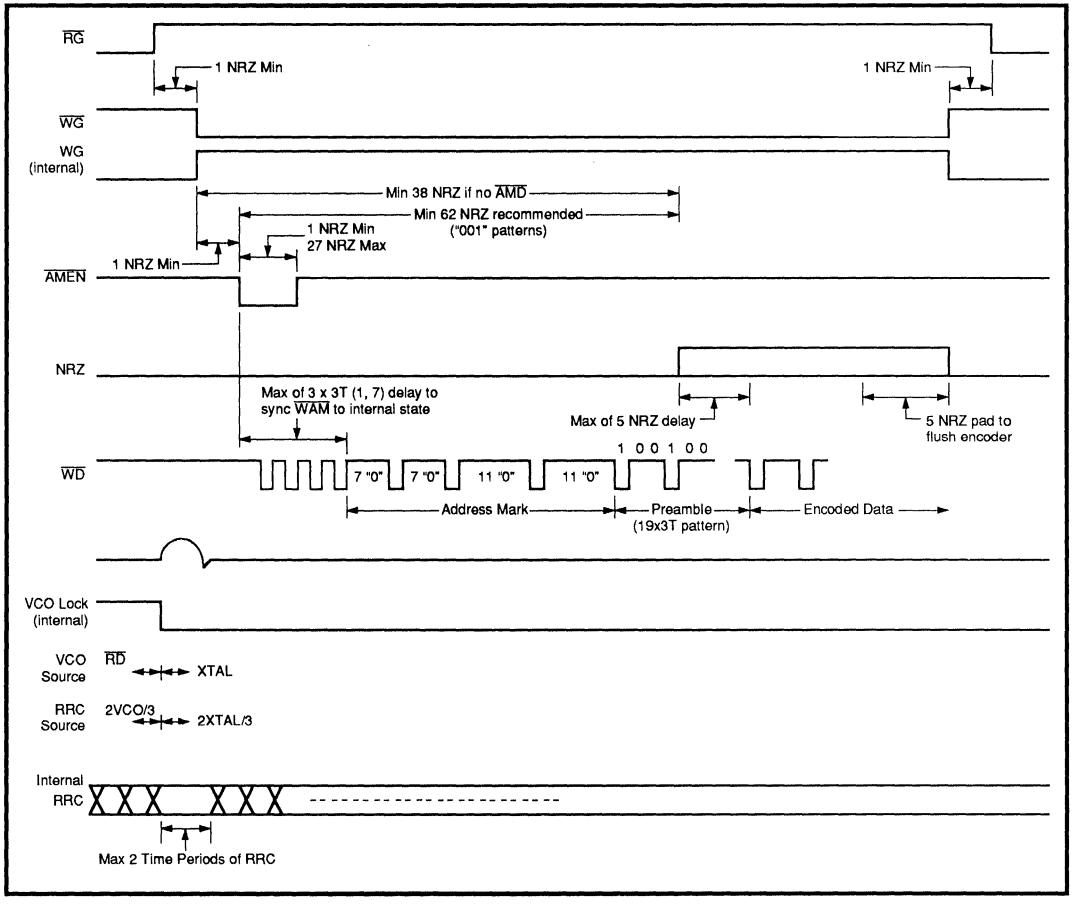


FIGURE 12: Write Data

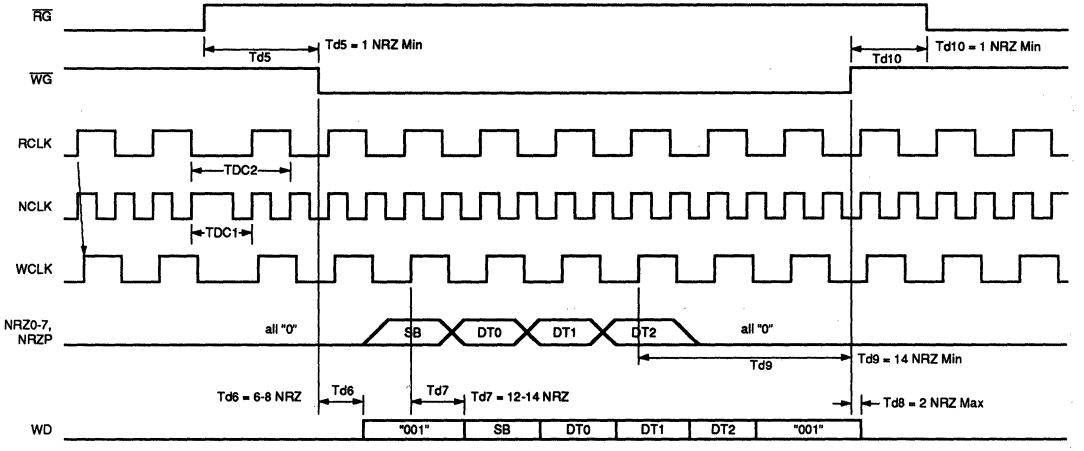


FIGURE 13: Write Mode NRZ Timing

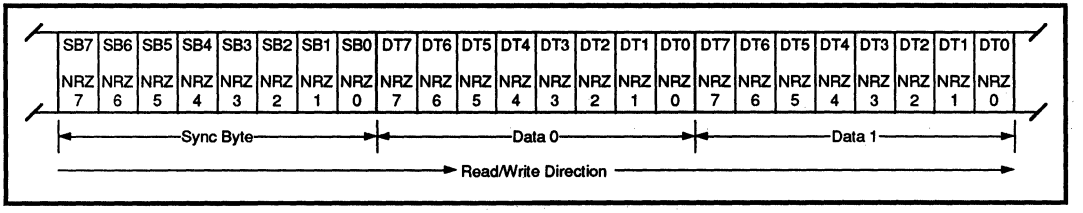
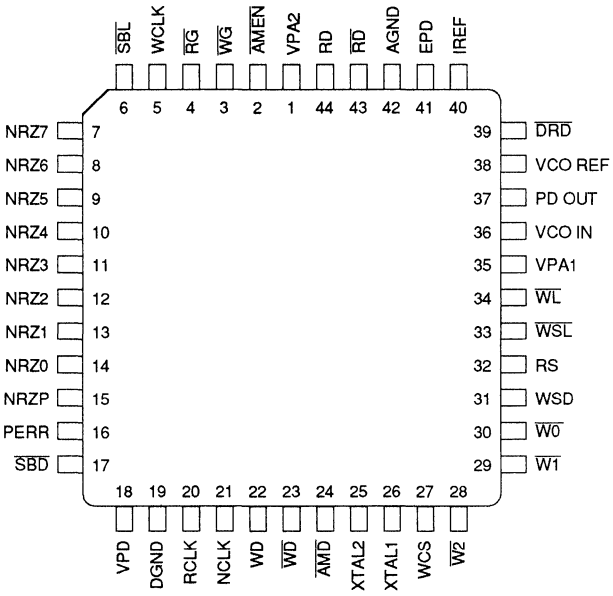


FIGURE 14: Parallel/Serial Conversion Format

PACKAGE PIN DESIGNATIONS

(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



4

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32D539		
44-Pin PLCC	32D539-CH	32D539-CH

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714) 731-7110, FAX: (714) 573-6914

Notes:

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SSI 32D5391
Data Synchronizer & 1, 7 RLL ENDEC

Advance Information

December 1991

DESCRIPTION

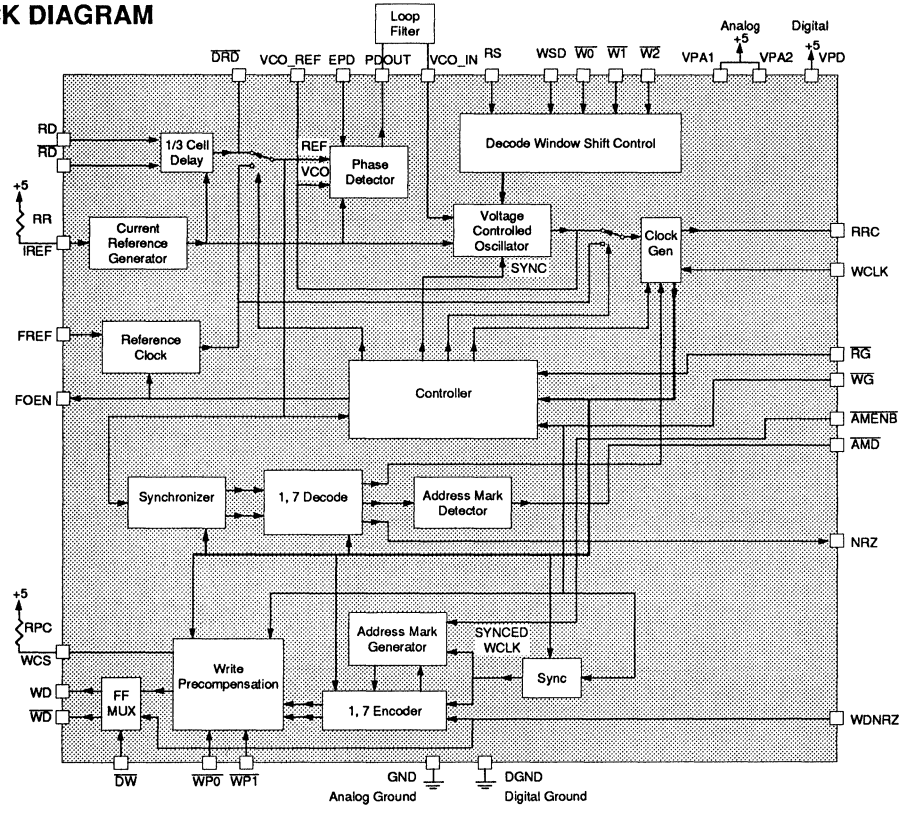
The SSI 32D5391 is intended to be used as a data/clock recovery circuit for 1, 7 RLL code in high performance hard disk drive systems with a +5V supply.

FEATURES

- **Data synchronizer and 1, 7 RLL ENDEC**
- **Up to 40 Mbit/s operation**
  - **Data rate programmed with a single external resistor or current source**
- **Direct write capability**
- **Fast acquisition phase locked loop with zero phase restart technique**
- **Fully integrated data separator**
  - **No external delay lines or active devices required**
- **Programmable decode window symmetry control**
  - **Includes delayed read data and VCO clock monitor points**
- **Programmable write precompensation**
- **Hard and soft sector operation**
- **Uses standard 5V ± 5% supply**
- **44-pin PLCC package**

4

BLOCK DIAGRAM



PIN DEFINITION

INPUT PINS

NAME	TYPE	DESCRIPTION
VPA1, VPA2	I	5 volt analog power supply pins.
VPD	I	5 volt digital power supply pin.
$\overline{\text{AMEN}}$	I	ADDRESS MARK ENABLE: Used to enable the address mark detection and address mark generation circuitry. Active low TTL input levels.
$\overline{\text{DW}}$	I	DIRECT WRITE ENABLE: Use to enable the direct write mode. A high level allows normal write operation. A low level enables the encoder bypass mode. In this bypass mode, each falling edge of WDNRZ will directly clock the WD flip-flop when $\overline{\text{WG}}$ is low. Pin $\overline{\text{DW}}$ has an internal pull up resistor. TTL input levels.
EPD	I	ENABLE PHASE DETECTOR: A low level (coast mode) disables the phase detector and enables the Test Mode. This opens the PLL and the VCO will run at the frequency commanded by the voltage on the VCO_IN pin. (In the Test Mode, functions normally driven by the VCO are switched to XTAL.) Pin EPD has an internal pull-up resistor. TTL input levels.
FREF	I	REFERENCE FREQUENCY INPUT: The pin frequency is at one and one-half times the data rate. FREF may be driven either by an AC coupled suitably attenuated TTL signal or by an AC coupled ECL signal.
RD, $\overline{\text{RD}}$	I	READ DATA: Encoded Read Data from the disk drive read channel. Differential pseudo ECL (PECL) input levels.
$\overline{\text{RG}}$	I	READ GATE: Selects the PLL reference input and initiates the PLL synchronization sequence. A low level selects the RD input and enables the read mode/address detect sequences. A high level selects the XTAL input. See Table 2, TTL input levels.
$\overline{\text{W0}}$, $\overline{\text{W1}}$, $\overline{\text{W2}}$	I	WINDOW SHIFT CONTROL BITS: In Read Mode, pins $\overline{\text{W}}$, $\overline{\text{W1}}$ and $\overline{\text{W2}}$ control the magnitude of the decode window shift. Each pin has an internal pull-up resistor. TTL input levels.
WSD	I	WINDOW SYMMETRY DIRECTION CONTROL: Controls the direction of the decode window shift. The pin has an internal pull-up resistor. TTL input levels.
WCLK	I	WRITE CLOCK: Write mode clock. Must be synchronous with the WDNRZ input. For short cable delays, WCLK may be connected directly to pin RRC. For long cable delays, WCLK should be connected to an RRC return line matched to the WDNRZ data line delay. TTL input levels.
WDNRZ	I	NRZ WRITE DATA INPUT PIN: This pin can be connected to the NRZ pin to form a bidirectional data port. Pin WDNRZ has an internal pull up resistor. TTL input levels.
$\overline{\text{WP0}}$, $\overline{\text{WP1}}$	I	WRITE PRECOMPENSATION CONTROL BITS: In Write Mode, pins $\overline{\text{WP0}}$ and $\overline{\text{WP1}}$ control the magnitude of the write precompensation. Each pin has an internal pull up resistor. TTL input levels.
$\overline{\text{WG}}$	I	WRITE GATE: Enables the write mode. Active low TTL input levels.

PIN DEFINITION (continued)

OUTPUT PINS

NAME	TYPE	DESCRIPTION
AGND	O	Analog ground pin
DGND	O	Digital ground pin
$\overline{AMD}$	O	ADDRESS MARK DETECT: Tristate output pin that is in its high impedance state when $\overline{WG}$ is low or $\overline{AMENB}$ is high. When $\overline{AMENB}$ is low, this output indicates address mark search status. A latched low level output appears when an address mark has been detected. A high level on pin $\overline{AMENB}$ resets pin $\overline{AMD}$. TTL output levels.
$\overline{DRD}$	O	DELAYED READ DATA: An open emitter ECL output test point. The positive edges of this signal indicate the data bit position. The positive edges of the $\overline{DRD}$ and VCO_REF outputs can be used to estimate window centering. The time jitter of DRD's positive edge is an indication of media bit jitter. Two external resistors are required to use this pin. They should be removed during normal operation to reduce power dissipation.
FOEN	O	REFERENCE CLOCK ENABLE: When this output is high, the FREF clock is controlling the internal timing. When this output is low, the FREF clock is internally disabled. The output from pin FOEN can be used to disable the clock applied to the FREF pin to reduce VCO jitter during read modes. TTL output levels.
NRZ	O	NRZ READ DATA OUTPUT: Tristate output pin that is enabled when read gate is active. This pin can be connected to the WDNRZ pin to form a bidirectional data port. TTL output levels.
RRC	O	READ CLOCK: A multiplexed bit clock source used by the controller, see Table 2. During a mode change, no glitches are generated and no more than one lost clock pulse will occur. When $\overline{RG}$ goes low, RRC initially remains synchronized to 2FREF/3. After 19 read data pulses, RRC is synchronized to the Read Data. When $\overline{RG}$ goes high, RRC is synchronized back to 2FREF/3. TTL output levels.
VCO REF	O	VCO REFERENCE: An open emitter ECL output test point. This is the VCO reference input to the phase detector. The positive edges are phase locked to Delayed Read Data. The negative edges of this open emitter output signal indicate the edges of the decode window. Two external resistors are required to use this pin. They should be removed during normal operation to reduce power dissipation.
WD, $\overline{WD}$	O	WRITE DATA: Encoded write data flip-flop output. The data is automatically resynchronized (independent of the delay between RRC and WCLK) to the FREF reference clock. Differential ECL output levels.

PIN DEFINITION (Continued)

ANALOG PINS

NAME	TYPE	DESCRIPTION
IREF	I	CURRENT REFERENCE INPUT: The VCO center frequency, the 1/3 cell delay, and the phase detector gain are a function of the current sourced into this pin.
PD OUT	I/O	PHASE DETECTOR OUTPUT: Drives the loop filter input.
RS	I	WINDOW SYMMETRY ADJUST PIN: A resistor connected between this pin and VPA allows analog adjustment of the decode window shift magnitude. Used in conjunction with the digital controls $\overline{W0}$, $\overline{W1}$ and $\overline{W2}$, this pin can be used to scale the magnitude of the preset window shift. Connect resistor to VPA.
VCO IN	I/O	VCO CONTROL INPUT: Driven by the loop filter output.
WCS	I	WRITE PRECOMPENSATION SET: Pin for the reference current to set the write precompensation magnitude value.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

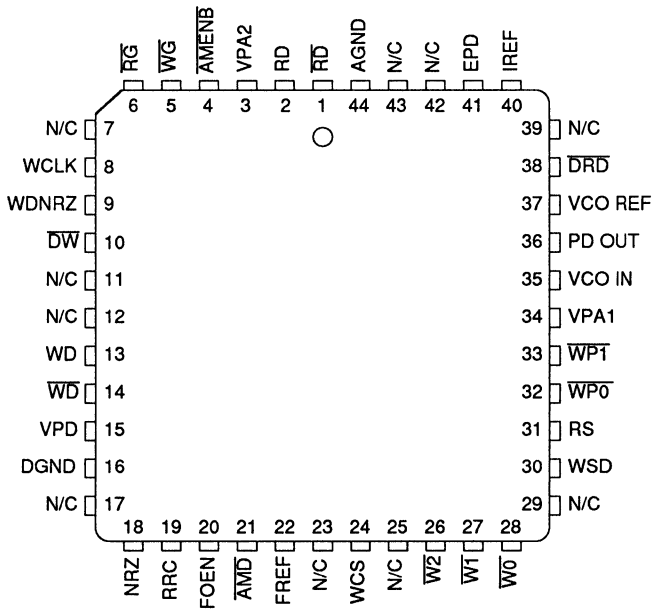
Operation above maximum ratings may damage the device

PARAMETER	RATING
Positive 5.0V Supply Voltage, VPA1, VPA2, VPD	6V
Storage Temperature	-65 to 150°C
Lead Temperature (Soldering 10 sec.)	260°C
FOEN, NRZ, RRC, WD, $\overline{WD}$, $\overline{AMD}$, VCOREF, $\overline{DRD}$ Pins	0.3V to VPA/VPD+0.3 or +12 mA
All other pins	-0.3V to VPA/VPD+0.3

PACKAGE PIN DESIGNATIONS

(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



44-Pin PLCC

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Advance Infromation: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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Notes:

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SSI 32D5392
Data Synchronizer & 1, 7 RLL ENDEC

Advance Information

December 1991

DESCRIPTION

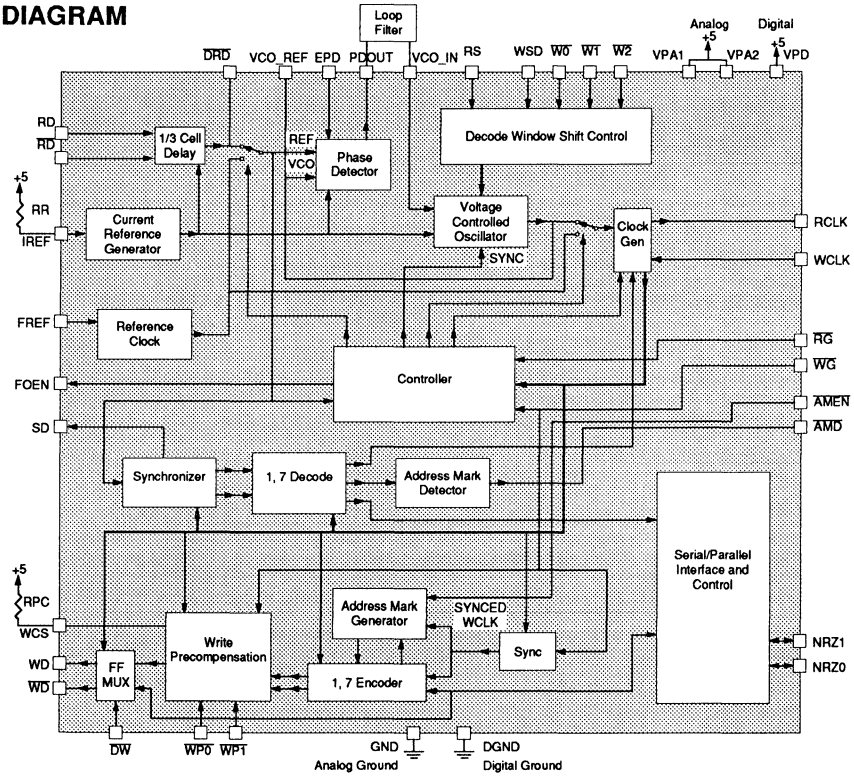
The SSI 32D5392 is intended to be used as a data/clock recovery circuit for 1, 7 RLL code in high performance hard disk drive systems with a +5V supply.

FEATURES

- **Data synchronizer and 1, 7 RLL ENDEC**
- **Dual bit bi-directional data bus interface**
- **Up to 48 Mbit/s operation**
  - **Data rate programmed with a single external resistor or current source**
- **Direct write capability**
- **Fast acquisition phase locked loop with zero phase restart technique**
- **Fully integrated data separator**
  - **No external delay lines or active devices required**
- **Programmable decode window symmetry control**
  - **Includes delayed read data and VCO clock monitor points**
- **Programmable write precompensation**
- **Hard and soft sector operation**
- **Uses standard 5V ± 5% supply**
- **36-pin SOM package**

4

BLOCK DIAGRAM



PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
VPA1, VPA2	I	5V analog power supply pins.
VPD	I	5 V digital power supply pin.
AGND	O	Analog ground pin.
DGND	O	Digital ground pin.
$\overline{\text{AMEN}}$	I	ADDRESS MARK ENABLE: Used to enable the address mark detection and address mark generation circuitry. Active low TTL input levels.
EPD	I	ENABLE PHASE DETECTOR: A low level (coast mode) disables the phase detector and enables the Test Mode. This opens the PLL and the VCO will run at the frequency commanded by the voltage on the VCO IN pin. (In the Test Mode, functions normally driven by the VCO are switched to FREF.) Pin EPD has an internal pull-up resistor. TTL input levels.
RD, $\overline{\text{RD}}$	I	READ DATA: Encoded Read Data from the disk drive read channel. Differential +5 volts offset ECL (PECL) input levels.
$\overline{\text{RG}}$	I	READ GATE: Selects the PLL reference input and initiates the PLL synchronization sequence. A low level selects the RD input and enables the read mode/address detect sequences. A high level selects the FREF input. TTL input levels.
$\overline{\text{W0}}$, $\overline{\text{W1}}$, $\overline{\text{W2}}$	I	WINDOW CONTROL BITS: In Read Mode, pins $\overline{\text{W0}}$ and $\overline{\text{W1}}$, $\overline{\text{W2}}$ control the magnitude of the decode window shift. Each pin has an internal pull-up resistor. TTL input levels.
WSD	I	WINDOW SYMMETRY DIRECTION CONTROL: Controls the direction of the decode window shift. The pin has an internal pull-up resistor. TTL input levels.
WCLK	I	WRITE CLOCK: Write mode dual bit clock. Must be synchronous with the Write Data NRZ input. For short cable delays, WCLK may be connected directly to pin RCLK. For long cable delays, WCLK should be connected to an RCLK return line matched to the NRZ data bus line delay. TTL input levels.
$\overline{\text{WG}}$	I	WRITE GATE: Enables the write mode. Active low TTL input levels.
$\overline{\text{AMD}}$	O	ADDRESS MARK DETECT: Tristate output pin that is in its high impedance state when $\overline{\text{WG}}$ is low or $\overline{\text{AMEN}}$ is high. When $\overline{\text{AMEN}}$ is low, this output indicates address mark search status. A latched low level output appears when an address mark has been detected. A high level on pin $\overline{\text{AMEN}}$ resets pin $\overline{\text{AMD}}$. TTL output levels.
$\overline{\text{DRD}}$	O	DELAYED READ DATA: An open emitter ECL output test point. The positive edges of this signal indicate the data bit position. The positive edges of the $\overline{\text{DRD}}$ and VCO_REF outputs can be used to estimate window centering. The time jitter of $\overline{\text{DRD}}$'s positive edge is an indication of media bit jitter. Two external resistors are required to use this pin. They should be removed during normal operation to reduce power dissipation.
$\overline{\text{DW}}$	I	DIRECT WRITE ENABLE: Used to enable the direct write mode. A high level allows normal write operation. A low level enables the encoder bypass mode. In this bypass mode, the falling edge of NRZ0 will directly clock the write data flip flop when $\overline{\text{WG}}$ is low. Pin $\overline{\text{DW}}$ has an internal pull up resistor. TTL input levels.
FOEN	O	REFERENCE CLOCK ENABLE: When this output is high, the FREF clock is controlling the internal timing. When this output is low, the FREF clock is internally disabled. The output from pin FOEN can be used to disable the clock applied to the FREF pin to reduce VCO jitter during read modes. TTL output levels.

PIN DESCRIPTION (Continued)

NAME	TYPE	DESCRIPTION
RCLK	O	READ CLOCK: A multiplexed dual bit clock source used by the controller. During a mode change, no glitches are generated and no more than one lost clock pulse will occur. When $\overline{RG}$ goes low, RCLK initially remains synchronized to 2FREF/3. After 19 read data pulses, RCLK is synchronized to the Read Data. When $\overline{RG}$ goes high, RCLK is synchronized back to the 2FREF/3. TTL output levels.
$\overline{WP0}$, $\overline{WP1}$	I	WRITE PRECOMPENSATION CONTROL BITS: In Write Mode, pins $\overline{WP0}$ and $\overline{WP1}$ control the magnitude of the write precompensation. Each pin has an internal pull-up resistor. TTL input levels.
VCO REF	O	VCO REFERENCE: An open emitter ECL output test point. This is the VCO reference input to the phase detector. The positive edges are phase locked to Delayed Read Data. The negative edges of this open emitter output signal indicate the edges of the decode window. Two external resistors are required to use this pin. They should be removed during normal operation to reduce power dissipation.
WD, $\overline{WD}$	O	WRITE DATA: Encoded write data flip-flop output. The data is automatically resynchronized (independent of the delay between RCLK and WCLK) to the FREF reference clock. Differential +5 volts offset ECL (PECL) output levels.
NRZ0-1	I/O	NRZ DATA PORT: Read data output when $\overline{RG}$ is low, write data input when $\overline{WG}$ is low. TTL input and output levels.

ANALOG PINS

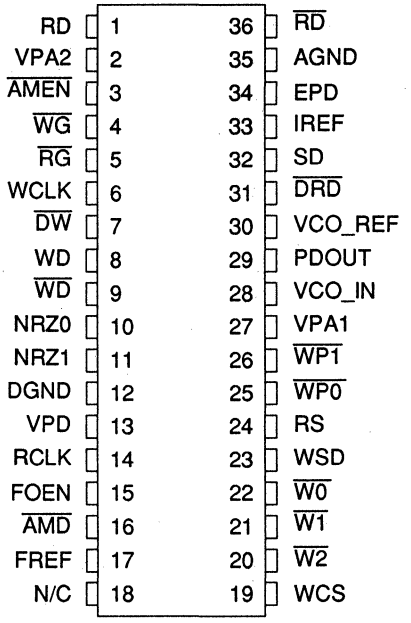
IREF	I	CURRENT REFERENCE INPUT: The VCO center frequency, the 1/3 cell delay, and the phase detector gain are a function of the current sourced into this pin.
PD OUT	O	PHASE DETECTOR OUTPUT: Drives the loop filter input.
RS	I	WINDOW SYMMETRY ADJUST PIN: This pin allows analog adjustment of the decode window shift magnitude. Used in conjunction with the digital controls $\overline{W0}$ and $\overline{W1}$, $\overline{W2}$ this pin can be used to scale the magnitude of the preset window shift. Connect resistor to VPA.
VCO IN	I	VCO CONTROL INPUT: Driven by the loop filter output.
WCS	I	WRITE PRECOMPENSATION SET: Pin for the reference current to set the write precompensation magnitude value.
FREF	I	REFERENCE FREQUENCY INPUT: The pin frequency is at one and one-half times the data rate. FREF may be driven either by an AC coupled suitably attenuated TTL signal or by an AC coupled ECL signal.

SSI 32D5392
Data Synchronizer
& 1, 7 RLL ENDEC

PACKAGE PIN DESIGNATIONS

(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



36-Lead SOM

Advance Infromation: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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SSI 32D4010

Data Synchronization/1, 7 RLL ENDEC with Write Precompensation

Advance Information

May 1991

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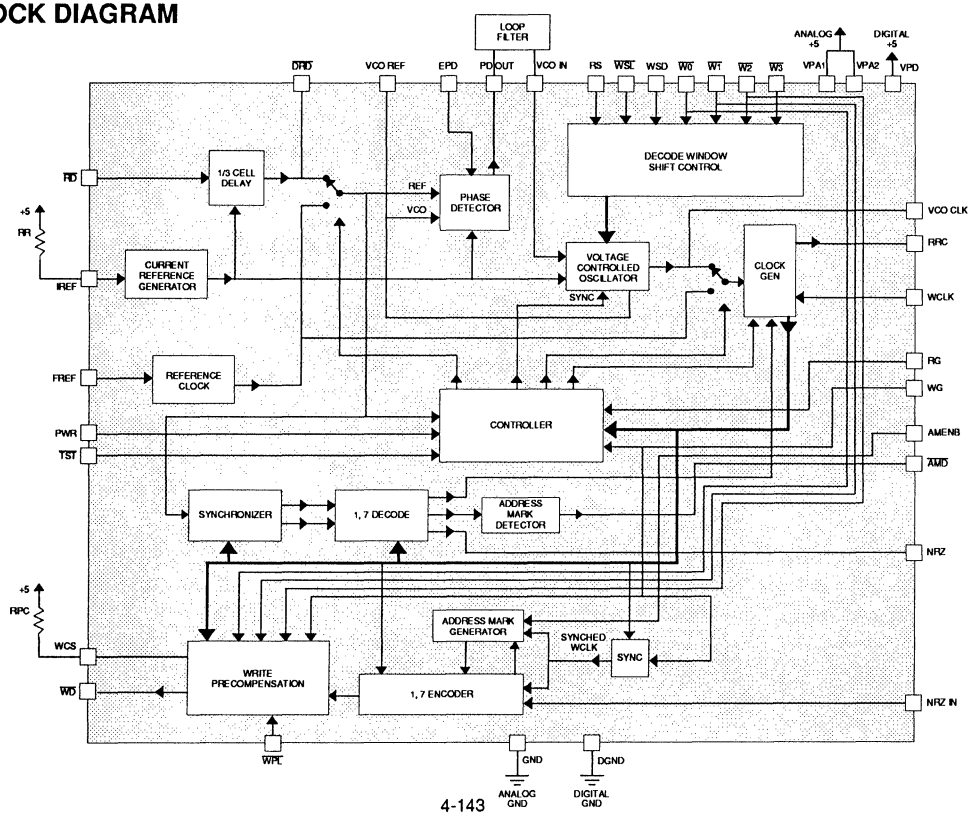
DESCRIPTION

The SSI 32D4010 Data Synchronizer/1, 7 RLL ENDEC provides data recovery and data encoding for storage systems which employ a 1, 7 RLL encoding format. Data synchronization is performed with a fully integrated high performance PLL. A zero phase restart technique is used to minimize PLL acquisition time. The VCO frequency setting elements are incorporated within the SSI 32D4010 for enhanced performance and reduced board space. Data rate is established with a single external programming resistor. The SSI 32D4010 utilizes an advanced bipolar process technology which affords precise decode window control without the requirement of an accurate 1/3 cell delay or external devices. The SSI 32D4010 requires a single +5V supply.

FEATURES

- **Data Synchronizer and 1, 7 RLL ENDEC**
- **12 to 24 Mbit/s operation - Data Rate programmed with a single external resistor**
- **Fast acquisition phase lock loop**
  - **Zero phase restart technique**
- **Fully integrated data separator**
  - **No external delay lines or active devices required**
- **Power-down mode (<1 mW)**
- **Programmable decode window symmetry control**
- **Programmable write precompensation**
- **Hard and soft sector operation**
- **+5V operation**
- **36-Pin SO package**
- **Test outputs - Allow drive margin testing**

BLOCK DIAGRAM



SSI 32D4010
Data Synchronization/1, 7 RLL ENDEC with Write Precompensation

OPERATION

The SSI 32D4010 is designed to perform data recovery and data encoding in rotating memory systems which utilize a 1,7 RLL encoding format. In the Read Mode the SSI 32D4010 performs Data Synchronization, Sync Field Search and Detect, Address Mark Detect, and Data Decoding. In the Write Mode, the SSI 32D4010 converts NRZ data into the 1,7 RLL format described in Table 1, performs Write Precompensation, generates the Preamble Field, and inserts Address Marks as requested.

The SSI 32D4010 can operate with data rates ranging from 12 to 24 Mbit/s. This data rate is established by a single 1% external resistor, RR, connected from pin IREF to VPA2. This resistor establishes a reference current which sets the VCO center frequency, the phase detector gain, and the 1/3 cell delay. The value of this resistor is given by:

$$RR = \frac{93}{DR} - 1.7\ (k\Omega)$$

where: DR = Data Rate in Mbit/s.

A reference clock, operating at 3x the data rate, generates the standby reference for the PLL. Either an attenuated external TTL compatible reference or an AC coupled ECL source may be applied to FREF.

The SSI 32D4010 employs a Dual Mode Phase Detector; Harmonic in the Read Mode and Non Harmonic in Write and Idle Modes. In the Read Mode the Harmonic Phase Detector updates the PLL with each occurrence of a DYLD DATA pulse. In the Write and Idle modes the Non-Harmonic Phase Detector is continuously enabled, thus maintaining both phase and frequency lock. By acquiring both phase and frequency lock to the crystal reference oscillator and utilizing a zero phase restart technique, false lock to delayed data is eliminated.

The phase detector incorporates a charge pump in order to drive the loop filter directly. The polarity and width of the output current pulses correspond to the direction and magnitude of the phase error.

The READ GATE (RG), and WRITE GATE (WG) inputs control the device mode.

RG is an asynchronous input and may be initiated or terminated at any position on the disk. WG is also an asynchronous input, but should not be terminated prior to the last output Write Data pulse.

READ OPERATION

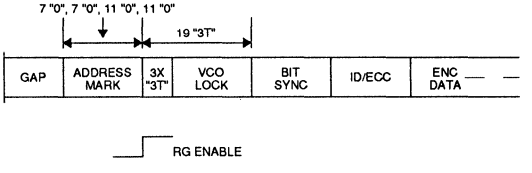
The Data Synchronizer utilizes a fully integrated fast acquisition PLL to accurately develop the decode window. Read Gate, RG, initiates the PLL locking sequence and selects the PLL reference input; a high level (Read Mode) selects the RD input and a low level selects the crystal reference oscillator.

In the Read Mode the falling edge of $\overline{DRD}$ enables the Phase Detector while the rising edge is phase compared to the rising edge of the VCO. As depicted in Figure 6, $\overline{DRD}$ is a 1/3 cell wide (TVCO) pulse whose leading edge is defined by the leading edge of $\overline{RD}$. A decode window is developed from the VCO clock. Shifting the phase of the VCO clock effectively shifts the relative position of the DRD pulse within the decode window. Decode window control is provided via the WS controls.

In Non-Read Modes, the PLL is locked to the external reference clock. This forces the VCO to run at a frequency which is very close to that required for tracking actual data and thus minimizes the associated frequency step during acquisition. When the reference input to the PLL is switched, the VCO is stopped momentarily, then restarted in an accurate phase alignment with the next PLL reference input pulse, and the VCO clock divider is reset.

SOFT SECTOR OPERATION

Disk Operation Lock Sequence in Read Mode Soft Sector Operation



ADDRESS MARK DETECT

In Soft Sector Read Operation the SSI 32D4010 must first detect an address mark to be able to initiate the rest of the read lock sequence. An address mark for the SSI 32D4010 consists of two (2) 7 "0" patterns followed by two 11 "0" patterns. To begin the read lock sequence the Address Mark Enable (AMENB) is asserted high by the controller. The SSI 32D4010 Address Mark Detect ($\overline{AMD}$) circuitry then initiates a search of the read data ($\overline{RD}$) for an address mark. First the $\overline{AMD}$ looks for a set of 6 "0's" within the 7 "0" patterns. Having detected a 6 "0" the $\overline{AMD}$ then looks for a 9 "0" set within the 11 "0's". If $\overline{AMD}$ does not detect 9 "0's" within 5 $\overline{RD}$ bits after detecting 6 "0's" it will restart the Address Mark Detect sequence and look for 6 "0's." When the $\overline{AMD}$ has acquired a 6 "0," 9 "0" sequence the $\overline{AMD}$ transitions low. $\overline{AMD}$ will remain low for the duration of AMENB. When AMENB is released, $\overline{AMD}$ will be released by the SSI 32D4010.

PREAMBLE SEARCH

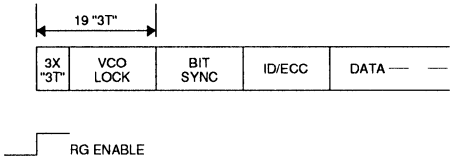
After the Address Mark (AM) has been detected a Read Gate (RG) can be asserted initiating the remainder of the read lock sequence. When RG is asserted an internal counter counts transitions of the incoming Read Data, ($\overline{RD}$ looking for 3 consecutive '3T's). Once the counter reaches count 3 (finds (3) consecutive 3T preamble) the internal read gate enables switching the phase detector from the reference oscillator to the delayed Read Data input ($\overline{DRD}$); at the same time a zero phase (internal) restart signal restarts the VCO in phase with the $\overline{DRD}$. This prepares the VCO to be synchronized to data when the bit sync circuitry is enabled after VCO lock is established.

VCO LOCK & BIT SYNC ENABLE

When the internal counter counts 16 more "3T" or a total of 19 positive transitions from RG enable, an internal VCO lock signal enables. The VCO lock signal activates the decoder bit synchronization circuitry to define the proper decode boundaries. Also, at count 19, the RRC source switches from the external reference clock to the VCO clock signal which is phase locked to $\overline{DRD}$. The VCO is assumed locked at this point. A maximum of 2 RRC time periods may occur for the RRC transition, however, no short duration glitches will occur. After the bit sync circuitry sets the proper decode window (VCO in sync with RRC and RRC in sync with data) NRZ is enabled and data is toggled in to be decoded for the duration of the read gate.

HARD SECTOR OPERATION

READ MODE



In hard sector operation a low AMENB disables the SSI 32D4010's Address Mark Detection circuitry and $\overline{AMD}$ remains inactive. A hard sector read operation does not require an address mark search but starts with a preamble search as with soft sector and sequences identically. In all respects, with exception to the address mark search sequence, hard sector read operation is the same as soft sector read.

WRITE MODE

In the write mode the SSI 32D4010 converts NRZ data from the controller into 1,7 RLL formatted data for storage on the disk. The SSI 32D4010 can operate with a soft or hard sector hard drive.

In soft sector operation the device generates a "7, 7, 11, 11" Address Mark, and a preamble pattern.

In the hard sector operation the device generates a 19 x "3T" preamble pattern but no preceding Address Mark. The NRZIN pin must be kept low for the duration of the preamble pattern. The NRZ input data is clocked on the rising edges of WCLK.

Write precompensation circuitry is provided to compensate for media bit shift caused by intersymbol interference. The SSI 32D4010 recognizes specific write data patterns and can add or subtract delays in the time position of write data bits to counteract the read back bit shift. The magnitude of the time shift, TPC, is determined by an external resistor on the WCS pin.

The SSI 32D4010 performs write precompensation according to the algorithm outlined in Table 3.

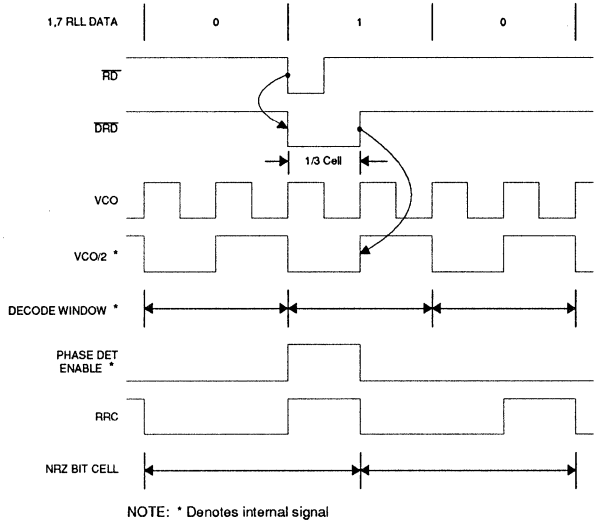
SOFT SECTOR

In soft sector operation, when Read Gate (RG) transitions low, VCO source and RRC source switch from $\overline{RD}$ and VCO/3, respectively, to the external reference clock. At the same time the VCO (internal) lock goes inactive but the VCO is locked to the external reference clock. After a delay of 1 NRZ time period (min) from RG low, the Write Gate (WG) can be enabled while NRZIN is maintained (NRZ write data) low. The Address Mark Enable (AMENB) is made active (high) a minimum of 1 NRZ time period later. The Address Mark (consisting of 7 "0's," 7 "0's," 11 "0's, "11 "0's") and the 19 x "3T" Preamble is then written by $\overline{WD}$. While the preamble is being written, the encoder is active. Therefore, WCLK must be clocking in an all "0" NRZIN pattern. The first non-zero NRZIN input bit indicates the end of the preamble pattern. After a delay of 10-12 NRZIN bit time periods, non preamble data begins to toggle out $\overline{WD}$. Finally, at the end of the write cycle, 16 bits of blank NRZ time passes to ensure the encoder is flushed of data; WA goes low. $\overline{WD}$ stops toggling a maximum of 2 NRZ time periods after WG goes low.

HARD SECTOR

In hard sector operation, when read gate (RG) transitions low, VCO source and RRC switch references and VCO lock (internal) goes inactive as with soft sector but the AMENB (address mark enable) is kept low.

The SSI 32D4010 then sequences from RG disable to WG enable and NRZIN active as in soft sector operation.



NOTE: * Denotes internal signal

FIGURE 1: Data Synchronization Waveform

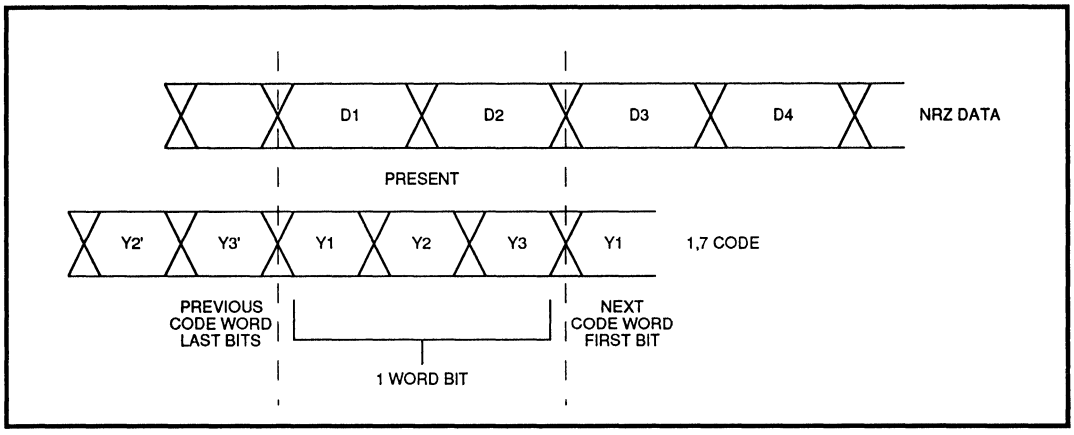


FIGURE 2: NRZ Data Word Comparision to 1, 7 Code Word Bit (See Table 1, for Decode Scheme)

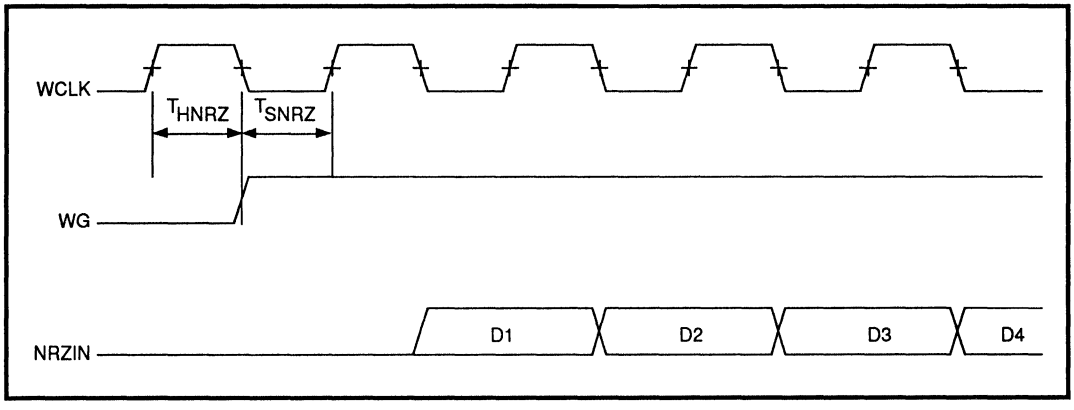


FIGURE 3: WG Timing Requirement for Predictable Write Encoding

A decodable write pattern will always be generated, regardless of the phasing of WG. However, a repeatable write pattern will be generated only if WG satisfies the same WCLK setup and hold requirements as the NRZIN data.

TABLE 1: Decode Table

ENCODED READ DATA			DECODED DATA	
Previous	Present	Next		
Y Y	Y Y Y	Y Y Y	D D	
2' 3'	1 2 3	1 2 3	1 2	
0 0	0 0 0	X X X	0 1	
1 0	0 0 0	X X X	0 0	
0 1	0 0 0	X X X	0 1	
X X	1 0 0	X X X	1 1	
X 0	0 1 0	0 0	1 1	
X 0	0 1 0	1 0	1 0	
X 0	0 1 0	0 1	1 0	
X 1	0 1 0	0 0	0 1	
X 1	0 1 0	1 0	0 0	
X 1	0 1 0	0 1	0 0	
0 0	0 0 1	X X	0 1	
1 0	0 0 1	X X	0 0	
0 1	0 0 1	X X	0 0	(Preamble)
X X	1 0 1	X X	1 0	

TABLE 2: Encode Table

NRZ DATA				ENCODED WRITE DATA			
Present		Next		Previous	Present		
D	D	D	D	Y	Y	Y	Y
1	2	3	4	3	1	2	3
0	0	0	X	0	0	0	1
0	0	1	X	0	0	0	0
0	0	1	X	1	0	1	0
1	0	0	X	0	1	0	1
1	0	1	X	0	0	1	0
0	1	0	0	0	0	0	1
0	1	0	0	1	0	1	0
0	1	1	0	0	0	0	0
0	1	1	0	1	0	0	0
0	1	0	1	0	0	0	1
0	1	0	1	1	0	0	0
0	1	1	1	0	0	0	0
0	1	1	1	1	0	0	0
1	1	0	0	0	0	1	0
1	1	1	0	0	1	0	0
1	1	0	1	0	1	0	0
1	1	1	1	0	1	0	0

NOTE: X = Don't Care

TABLE 3: Clock Frequency

WG	RG	VCO REF	RRC	DECCLK	ENCCLK	MODE
0	0	FREF/2	FREF/3	FREF/2	FREF/2	IDLE
0	1	$\overline{RD}$	VCO/3	VCO/2	FREF/2	READ
1	0	FREF/2	FREF/3	FREF/2	FREF/2	WRITE
1	1	FREF/2	FREF/3	FREF/2	FREF/2	UNDEFINED

Note 1: Until the VCO locks to the new source, the VCO/2 entries will be FREF/2.
2: Until the VCO locks to the new source, the VCO/3 entries will be FREF/3.

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TABLE 4: Write Precompensation Algorithm

BIT	BIT	BIT	BIT	BIT	COMPENSATION
n-2	n-1	n	n+1	n+2	BIT n
1	0	1	0	1	NONE
0	0	1	0	0	NONE
1	0	1	0	0	EARLY
0	0	1	0	1	LATE

LATE: Bit n is time shifted (delayed) from its nominal time position towards the bit n+1 time position.

EARLY: Bit n is time shifted (advanced) from its nominal time position towards the bit n-1 time position.

PIN DESCRIPTION

INPUT PINS

NAME	TYPE	DESCRIPTION
FREF	I	REFERENCE FREQUENCY INPUT: The pin frequency is at 3 times the data rate. FREF may be driven by a direct coupled TTL signal or by an AC coupled ECL signal. Pin FREF has an internal pull-down resistor.
$\overline{RD}$	I	READ DATA: Encoded Read Data from the disk drive read channel. Timing is referenced to the falling edge of this signal. Pin $\overline{RD}$ has an internal pullup resistor. TTL input levels.
RG	I	READ GATE: Selects the PLL reference input (REF)and initiates the PLL synchronization sequence. Pin RG has an internal resistor pullup. A high level selects the RD input and enables the Read Mode. A low level selects the FREF input. See Table 3.
WG	I	WRITE GATE: Enables the write mode, see Table 3. Pin WG has an internal resistor pullup. Active high TTL input levels.
WCLK	I	WRITE CLOCK: Write Mode Clock. Must be synchronous with the NRZ Write Data input. For short cable delays, WCLK may be connected directly to pin RRC. TTL input levels.
EPD	I	ENABLE PHASE DETECTOR: A low level (Coast Mode) disables the phase detector. Pin EPD has an internal resistor pullup. TTL input levels.
AMENB	I	ADDRESS MARK ENABLE: Used to enable the address mark detection and address mark generation circuitry. Active high TTL input levels. Pin AMENB has an internal resistor pull up.
$\overline{W0}$ - $\overline{W3}$	I	WRITE/WINDOW CONTROL BITS: In Write Mode, pins $\overline{W0}$, $\overline{W1}$, $\overline{W2}$ control the magnitude of the write precompensation. In Read Mode pins $\overline{W0}$ - $\overline{W3}$ control the magnitude of the decode window shift. Each pin has an internal pullup resistor. TTL input levels.
$\overline{WL}$	I	WRITE PRECOMPENSATION CONTROL LATCH: Used to latch the write precompensation control bits $\overline{W0}$ - $\overline{W2}$ into the internal DAC. The latch is transparent while $\overline{WL}$ is high. An active low level latches the input bits. Pin $\overline{WL}$ has an internal resistor pullup. If unused, leave pin open or tie high. TTL input levels.
NRZIN	I	NRZ WRITE DATA INPUT PIN: This pin can be connected to the NRZ pin to form a bidirectional data port. Pin NRZIN has an internal pullup resistor. TTL input levels.
PWR	I	POWER ENABLE: A high level enables the device. A low level shuts off power to all the functions. TTL input levels. If unused, this pin must be tied high.
$\overline{TST}$	I	TEST MODE CONTROL: A low level enables test mode. In the test mode the $\overline{W0}$ - $\overline{W3}$ and WSD pins are used to control various test functions. Pin $\overline{TST}$ has an internal pullup resistor. TTL input levels.
WSD	I	WINDOW SYMMETRY DIRECTION CONTROL: Controls the direction of the decode window shift. Pin WSD has an internal pullup resistor. TTL input levels.
$\overline{WSL}$	I	WINDOW SYMMETRY LATCH CONTROL: Used to latch the window symmetry control bits $\overline{W0}$ - $\overline{W3}$ and WSD into the internal DAC. The latch is transparent while $\overline{WSL}$ is high. An active low level latches the input control bits. Pin $\overline{WSL}$ has an internal pullup resistor. TTL input levels.

OUTPUT PINS

NAME	TYPE	DESCRIPTION
$\overline{WD}$	O	WRITE DATA: Encoded write data output, active low. Timing is referenced to the falling edge of this signal. The data is automatically resynchronized (independent of the delay between RRC and WCLK) to the FREF reference clock. TLL output levels.
RRC	O	READ/REFERENCE CLOCK: A multiplexed clock source used by the controller, see Table 2. During a mode change, no glitches are generated and no more than two lost clock pulses will occur. When RG goes high, RRC initially remains synchronized to FREF/3. When the sync bits are detected RRD is synchronized to the Read Data. When RG goes low, RCLK is synchronized back to FREF/3. TTL output levels.
$\overline{AMD}$	O	ADDRESS MARK DETECT: Tristate output pin that is in its high impedance state when WG is high or AMENB is low. When AMENB is high, this output indicates address mark search status. A latched low level output indicates that an address mark has been detected. A low level on pin AMENB resets pin $\overline{AMD}$. TTL output levels.
VCO REF	O	VCO REFERENCE: An open emitter ECL output test point. This is the VCO reference input to the phase detector. The positive edges are phase locked to DLYD DATA. The negative edges of this open emitter output signal indicate the edges of the decode window. Two external resistors are required to perform this test. They should be removed during normal operation for reduced power dissipation.
VCO CLK	O	VCO CLOCK: An open emitter ECL output test point. Two external resistors are required to perform this test. They should be removed during normal operation for reduced power dissipation.
$\overline{DRD}$	O	DELAYED READ DATA: An open emitter ECL output test point. The positive edges of this open emitter output signal indicates the data bit position. The positive edges of the $\overline{DRD}$ and the VCO REF signals can be used to estimate window centering. The time jitter of DRD's positive edge is an indication of media bit shift. Two external resistors are required to perform this test. They should be removed during normal operation for reduced power dissipation.
NRZ	O	NRZ READ DATA OUTPUT: Tristate output pin that is in its high impedance state when read gate is low. Read Data output when RG is high. TTL ouput levels.

ANALOG PINS

IREF	I	CURRENT REFERENCE INPUT: The VCO center frequency, the phase detector gain, and the 1/3 cell delay are a function of the current sourced into pin IREF. The current is set by an external resistor, RR, connected between pin IREF and VPA2.
PD OUT	O	PHASE DETECTOR OUTPUT: Drives the loop filter input.
VCO IN	I	VCO CONTROL INPUT: Driven by the loop filter output.
WCS	I	WRITE PRECOMPENSATION SET: Pin for the reference current to set the write precompensation magnitude value. If this pin is left open, write precompensation is disabled.

ANALOG PINS (continued)

NAME	TYPE	DESCRIPTION
RS	I	WINDOW SYMMETRY ADJUST PIN: A resistor connected between this pin and VPA allows analog adjustment of the decode window shift magnitude. Used in conjunction with the digital controls $\overline{W0}$, $\overline{W1}$, $\overline{W2}$ this pin can be used to set the magnitude of the window shift. If this pin is left unconnected, the window shift function is disabled.
DGND, AGND	I	Digital and Analog Ground
VPA1, VPA2	I	Analog +5V Supplies
VPD	I	Digital +5V Supply

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

PARAMETER	RATING	UNIT
Storage Temperature	-65 to + 150	°C
Junction Operating Temperature, Tj	+150	°C
Supply Voltage, VPA1, VPA2, VPD	-0.5 to 7	V
Voltage Applied to Logic Inputs	-0.5 to VPD + 0.5	V
Maximum Power Dissipation	TBD	W

RECOMMENDED OPERATING CONDITIONS

Supply Voltage, VPA1 = VPA2 = VPD = VCC	4.75 < VCC < 5.25	V
Junction Temperature, Tj	0 < Tj < 135	°C
Ambient Temperature, Ta	0 < Ta < 70°	°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, 4.75V< VCC <5.25V, 12 MHz< 1/TORC <24 MHz, 30 MHz< 1/TVCO <72 MHz, 0 °C< Ta <70 °C.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VIH	High Level Input Voltage		2.0		VPD + 0.3	V
VIL	Low Level Input Voltage		-0.3		0.8	V
IIH	High Level Input Current	VIH = 2.4V			100	µA
IIL	Low Level Input Current	VIL = 0.4V			-0.4	mA
VOH	High Level Output Voltage	IOH = 400 µA	2.4			V
VOL	Low Level Output Voltage	IOL = 4 mA			0.5	V
FREF	Input Low Current	VIL = 0.4V		TBD		mA
FREF	Input High	VIH = 2.4V		TBD		mA

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
ICC	Power Supply Current	All outputs & test point pins open Ta = 70°C		100		mA
ICC	(Power Down)	All outputs & test point pins open Ta = 70°C PWR = 0		0.1		mA
VOHT	Test Point Output High Level $\overline{DRD}$, VCO REF, VCO CLK	262Ω to VPD 402Ω to DGND VPD = 5.0V		VPA - 0.85		V
VOLT	Test Point Output Low Level $\overline{DRD}$, VCO REF, VCO CLK	262Ω to VPD 402Ω to DGND VPD = 5.0V		VPA - 1.75		V

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DYNAMIC CHARACTERISTICS AND TIMING

READ MODE (See Figure 4)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TRRC	Read Clock Rise Time	0.8V to 2.0V, $C_L \leq 15$ pF			8	ns
TFRC	Read Clock Fall Time	2.0V to 0.8V, $C_L \leq 15$ pF			5	ns
RRC	Duty Cycle	12 - 20 Mbit/s	43	50	57	%
		>20 - 24 Mbit/s	40.8	50	59.2	%
TNS,TNH	NRZ (out) Set Up/	12 - 20 Mbit/s	15.5			ns
	Hold Time	>20 - 24 Mbit/s	13			ns
TPNRZ	NRZ (out) Propogation Delay			TBD		ns
TPAMD	$\overline{AMD}$ Propogation Delay			TBD		ns
AMD	Set Up and Hold Time (TAS, TAH)		13			ns
1/3 Cell Delay		TD = 3.6 (RR+1.7) 2.1 KΩ ≤ RR ≤ 6.1 KΩ	0.8TD		1.2TD	ns

WRITE MODE (Design Targets) (See Figure 5)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TWD	Write Data Pulse Width	$C_L \leq 15$ pF TC = 3.52 (RC + 0.53) RC = kΩ	2TOWC/3 -TC -5		2TOWC/3	ns
TRWD	Write Data Rise Time	0.8V to 2.0V, $C_L \leq 15$ pF			9	ns
TFWD	Write Data Fall Time	2.0V to 0.8V, $C_L \leq 15$ pF			5	ns
TSNRZ	NRZIN Set up Time		5			ns
THNRZ	NRZIN Hold Time		5			ns

WRITE MODE (Continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TPWD	Write Data Position Accuracy	$C_L \leq 15$ pF; TPC = 0		±1		ns
TPC	Precompensation Time Shift Magnitude Accuracy	TP = 0.22M (RC + 0.53) RC (MIN) = TBD RC (MAX) = TBD, M = (See Table)	TBD	TP	TBD	ns

INPUT REQUIREMENTS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TRD	Read Data Pulse Width		12		(4) TVCO-20	ns
TFRD	Read Data Fall Time	2.0V to 0.8V, $C_L \leq 15$ pF			9	ns
TRWC	Write Data Clock Rise Time	0.8V to 2.0V $C_L \leq 15$ pF			10	ns
TFWC	Write Data Clock Fall Time	2.0V to 0.8V $C_L \leq 15$ pF			8	ns

REFERENCE CLOCK CHARACTERISTICS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TXPW	Reference Clock Pulse Width		TBD		TBD	ns
	Reference Clock P-P Amplitude	AC coupled	TBD		TBD	ns

DATA SYNCHRONIZATION (Design Targets)

PARAMETER		CONDITIONS	MIN	MAX	UNIT
TVCO	VCO Center Frequency Period	VCO IN = 2.7V TO = 3.6 (RR + 1.7) 2.1 kΩ ≤ RR ≤ 6.1 kΩ VCC = 5.0V RR = (93/DR) –1.7(kΩ)	0.8TO	1.2TO	ns
VCO	Frequency Dynamic Range	1V ≤ VCO IN ≤ VCC-0.6V VCC = 5.0	±25	±45	%
KVCO	VCO Control Gain	$\omega o = 2\pi/TO$ 1V ≤ VCO IN ≤ VCC 0.6V	0.12ωo	0.26ωo	rad/s-V
KD	Phase Detector Gain	KD= 0.22/(RR+530) Read Mode = 0.11/(RR+530) Non-Read Mode VCC= 5V, PLL REF = $\overline{RD}$ 3T ('100') Pattern	0.83KD	1.17KD	A/rad
	Decode Window Centering Accuracy	RS = N/C		±1.5	ns
	Decode Window	RS = N/C	(2TORC/3) - 1.5		ns

CONTROL CHARACTERISTICS (See Figure 6)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TSWC THWC	$\overline{W0}$ - $\overline{W3}$ SET UP TIME		7			ns
TWL	$\overline{WL}$, $\overline{WSL}$ Pulse Width		20			ns

DESIGN CHARACTERISTICS (Not Tested)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
KVCO x KD Product Accuracy			±28		%
VCO Phase Restart Error	Referred to RRC	TBD	TBD	TBD	rad

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Mode Control

WG	RG	AMENB	$\overline{TST}$	Modes	
0	0	0	1	Idle	Idle mode. VCO locked to external FREF. RRC sychronized to FREF. NRZ tri-stated. $\overline{AMD}$ high.
0	0	1	1	AM Search	Read mode Address Mark search. VCO locked to external FREF. RRC synchronized to FREF. NRZ tri-stated. $\overline{AMD}$ active.
0	1	0	1	Read Data	Read mode preamble search and data acquisition. VCO switched from FREF to $\overline{RD}$ after preamble lock. RRC synchronized to $\overline{RD}$ after sync bits found. NRZ active.
0	1	1	1	Undefined	Illegal state.
1	0	1	1	Write AM	Write mode Address Mark insertion. VCO locked to external FREF. $\overline{WD}$ active. NRZ tri-stated. $\overline{AMD}$ high.
1	0	0	1	Write data	Write mode preamble insertion and data write. VCO locked to external FREF. $\overline{WD}$ active. NRZ tri-stated. $\overline{AMD}$ high.
1	1	0	1	Undefined	Illegal state.
1	1	1	1	Undefined	Illegal state.

Write Precomp Control

$\overline{WL}$ - Write precomp latch control
0 = > Write precomp control latches in hold state
1 = > Write precomp control latches in transparent state

$\overline{W2}$, $\overline{W1}$, $\overline{W0}$ - Write precomp magnitude control bits

$\overline{W2}$	$\overline{W1}$	$\overline{W0}$	Precomp	Magnitude	M
1	1	1		None	0
1	1	0	1X	Minimum	1
1	0	1	2X		2
1	0	0	3X		3
0	1	1	4X		4
0	1	0	5X		5
0	0	1	6X		6
0	0	0	7X	Maximum	7

Window Shift Control

$\overline{WSL}$ - Window Shift latch control
0 = > Window Shift control latches in hold state
1 = > Window shift control latches in transparent state

WSD - Window Shift direction control
0 = > Early window (+TS)
1 = > Late window (-TS)

Window Shift magnitude control bits:

$\overline{W3}$	$\overline{W2}$	$\overline{W1}$	$\overline{W0}$	Shift	Magnitude
1	1	1	1		No shift
1	1	1	0	1X	Minimum shift
1	1	0	1	2X	
1	1	0	0	3X	
1	0	1	1	4X	
1	0	1	0	5X	
1	0	0	1	6X	
1	0	0	0	7X	
0	1	1	1	8X	
0	1	1	0	9X	
0	1	0	1	10X	
0	1	0	0	11X	
0	0	1	1	12X	
0	0	1	0	13X	
0	0	0	1	14X	
0	0	0	0	15X	Maximum shift

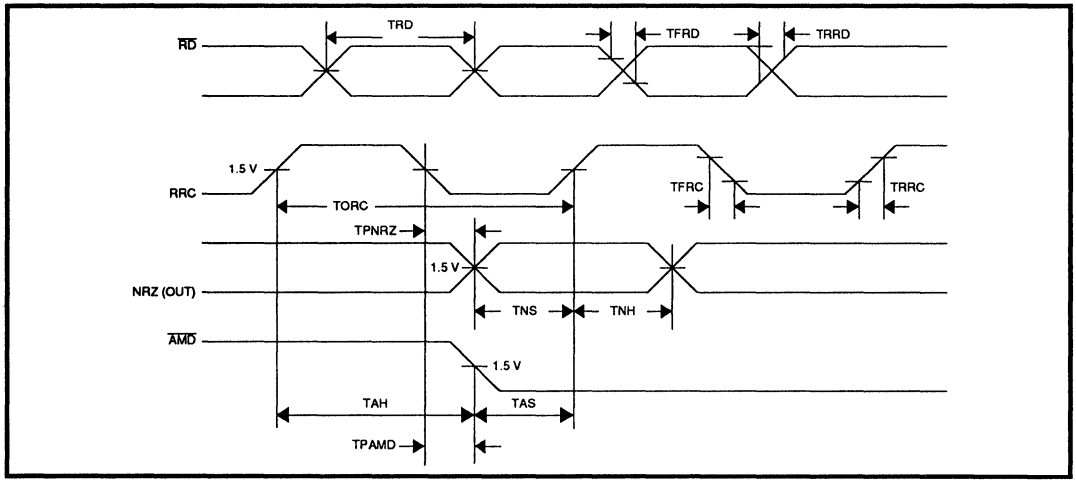


FIGURE 4: Read Timing

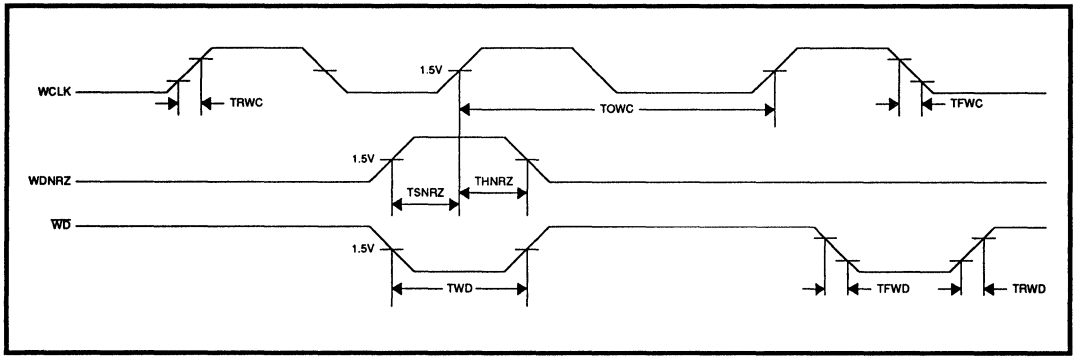


FIGURE 5: Write Timing

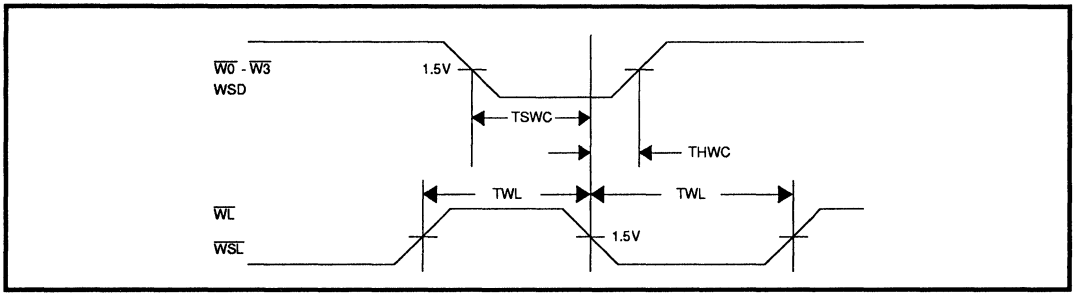
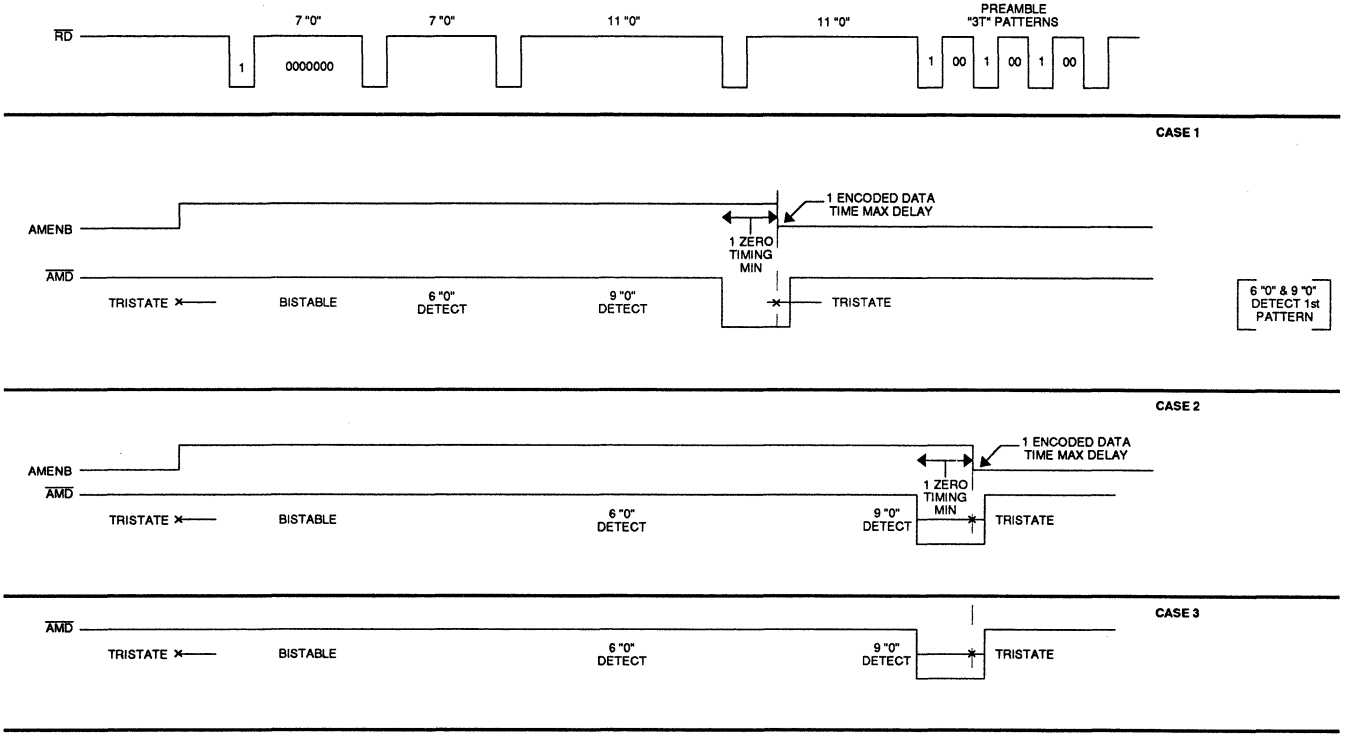


FIGURE 6: Control Timing



If 5 bits of RD are detected after 6 "0" are found and before 9 "0" then restart and look for 6 "0."

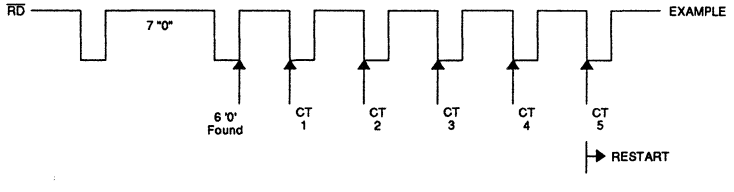


FIGURE 7: Address Mark Search

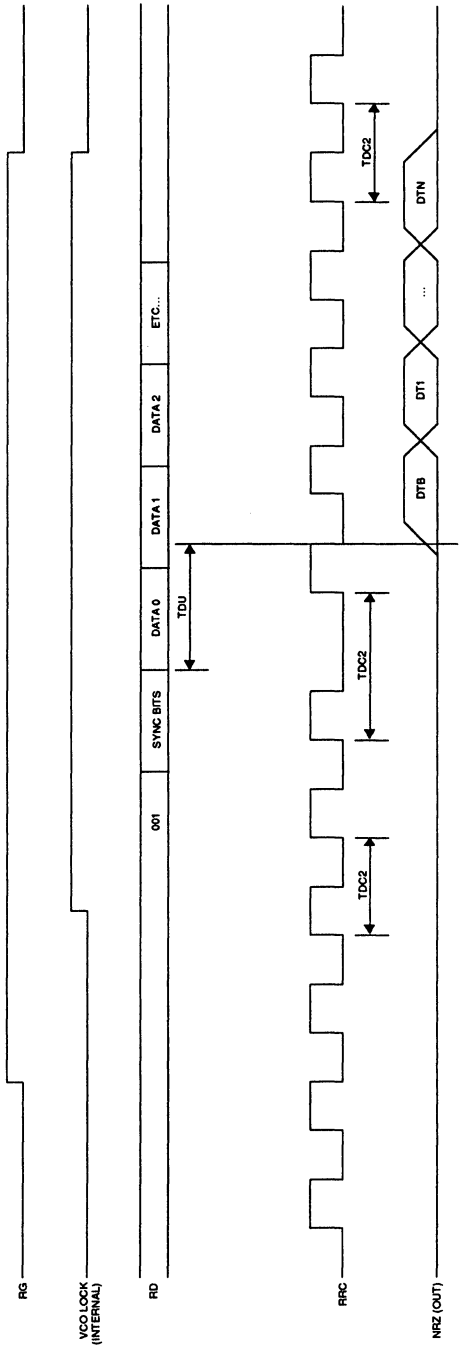


FIGURE 8: Read Mode NRZ and RRC Timing

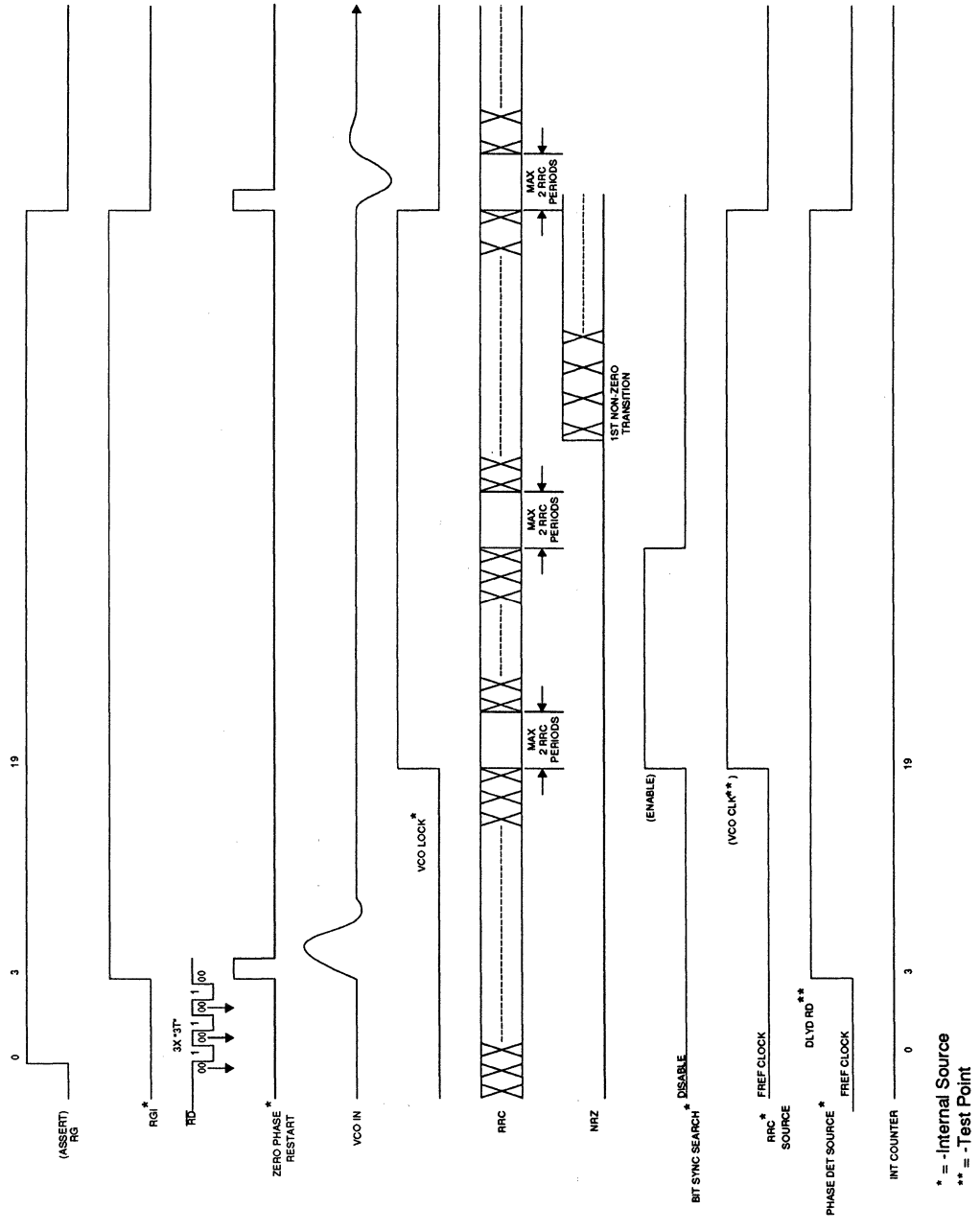


FIGURE 9: Read Mode Locking Sequence (Soft and Hard Sector)

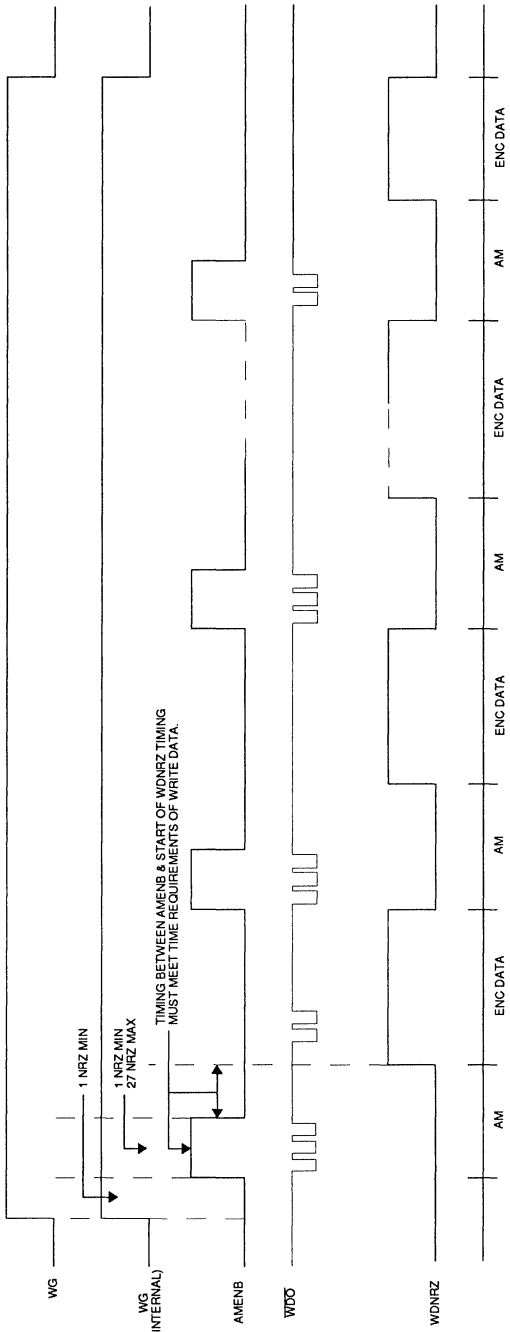


FIGURE 10: Multiple Address Mark Write

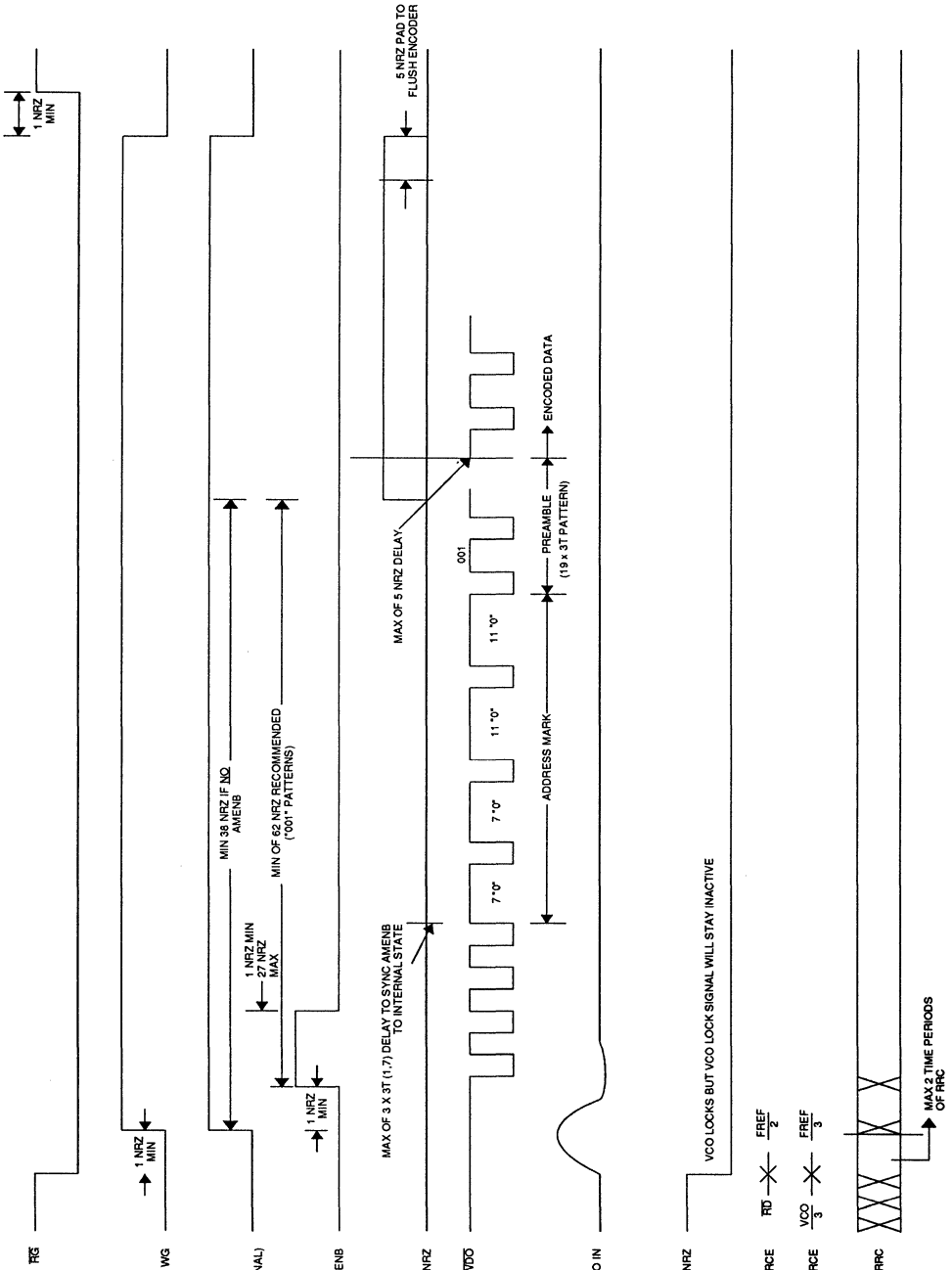


FIGURE 11: Write Data

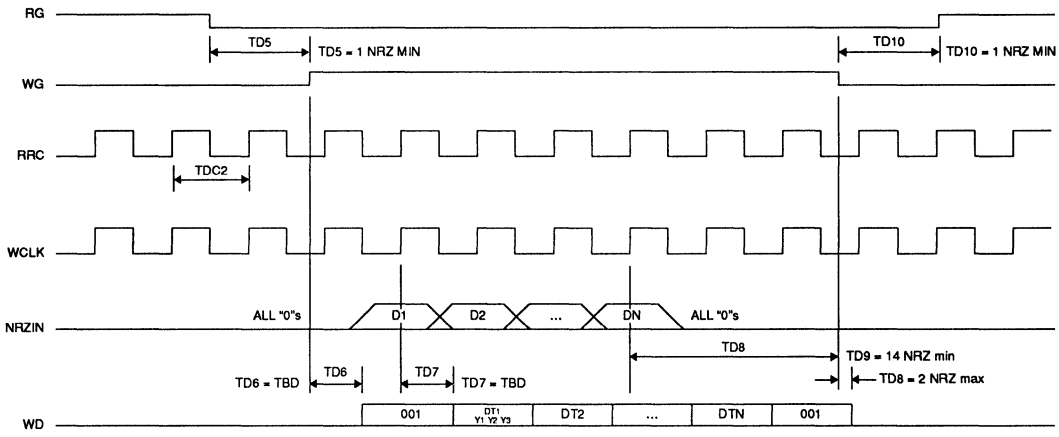


FIGURE 12: Write Mode NRZ Data Timing

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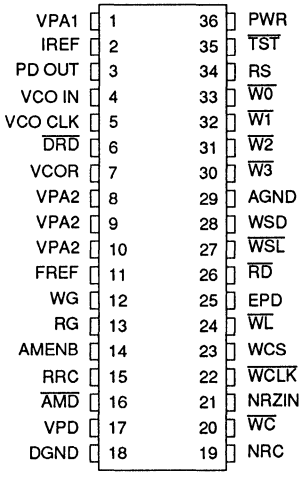
PACKAGE PIN DESIGNATIONS



36-Pin SOM

CAUTION: Use handling procedures necessary for a static sensitive component.

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

Silicon Systems, Inc. 14351 Myford Road, Tustin, CA 92680, (714) 731-7110, FAX (714) 573-6914

Notes:

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SSI 32D4420
Programmable Filter and Frequency Reference

Advance Information

November 1991

DESCRIPTION

The SSI 32D4420 is a low power, high performance bipolar device that provides a programmable filter and programmable frequency reference to support hard disk drive applications that use zoned recording techniques. The 7-pole equiripple filter section includes a programmable cutoff range of 1.5 to 8 MHz and programmable pulse slimming of 0 to 9 dB. The frequency reference can be programmed up to 72 MHz with 1% resolution. In addition, a 7-bit current output DAC is included to control the data rate of an external data separator device. Control of the programmable features is provided through a simple, easy to use serial interface. The 32D4420 functions as a companion device to the 32P4720 Pulse Detector/Data Separator device to form a complete two-chip read channel. The combination of these features along with a power-down mode, small footprint, and +5V only operation make the 32D4420 suitable for a wide variety of hard disk drive applications.

FEATURES

FILTER:

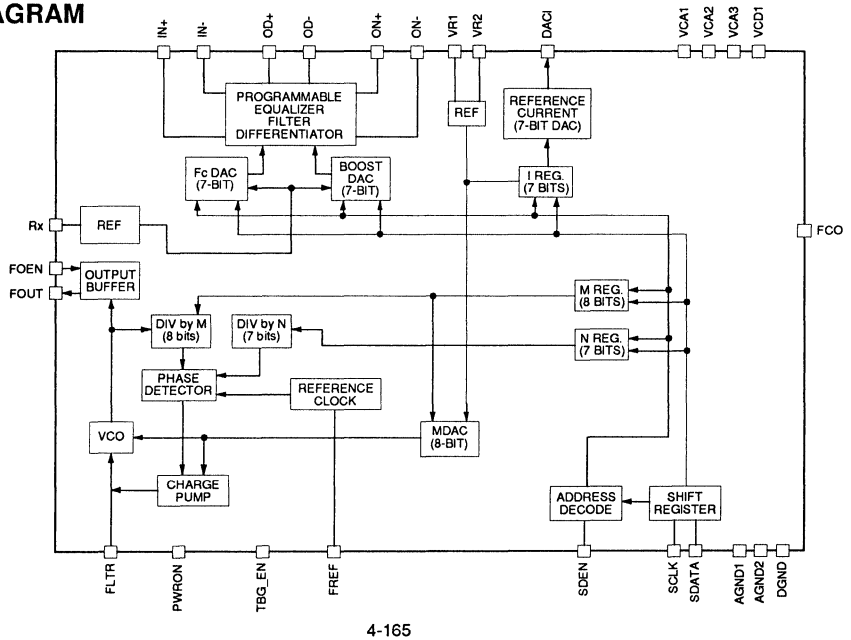
- **Cutoff frequency range of 1.5 to 8 MHz (7-bit DAC control)**
- **Programmable pulse slimming equalization of 0 to 9 dB (7-bit DAC control)**
- **Matched normal and differentiated low pass outputs**
- **±2% group delay variation from 1.5 to 8 MHz**
- **<1% total harmonic distortion**

FREQUENCY REFERENCE:

- **Programmable frequency output up to 72 MHz**
- **1% frequency resolution**
- **TTL compatible reference input**
- **Internal 7-bit DAC for data separator control**
- **Low power (<5 mW), 5V only operation**
- **Power down mode (<5 mW)**
- **Available in small footprint 32-pin QFP packages**

4

BLOCK DIAGRAM



SSI 32D4420
Programmable Filter and Frequency Reference

FUNCTIONAL DESCRIPTION

FILTER SECTION

The 32D4420 includes a 7-pole, .05° equiripple-type linear phase low pass filter along with a single-pole, single zero differentiator. Both outputs have well matched group delays. In addition, the delay matching is unaffected by the amount of equalization programmed or the bandwidth that is selected. Programmable pulse slimming and cutoff are provided to support filtering requirements in a zoned recording application.

The 3 dB cutoff frequency, F(3 dB), can be varied over a range of 1.5 - 8 MHz using an internal 7-bit DAC. This cutoff frequency is the unboosted F(3 dB) the filter. It is important to note that the F(3 dB) will move out when boost is increased. With maximum boost programmed the cutoff range of the filter will increase from 1.5 - 8 MHz to 4 - 21 MHz. Table 1 provides the scaling factors for F(3 dB) versus the amount of programmed boost.

TABLE 1: 3 dB frequency change versus boost value

Boost Value	Actual 3 dB Frequency
0 dB	F(3 dB) x 1.00
1 dB	F(3 dB) x 1.20
2 dB	F(3 dB) x 1.47
3 dB	F(3 dB) x 1.74
4 dB	F(3 dB) x 1.95
5 dB	F(3 dB) x 2.13
6 dB	F(3 dB) x 2.28
7 dB	F(3 dB) x 2.41
8 dB	F(3 dB) x 2.53
9 dB	F(3 dB) x 2.65

PULSE SLIMMING

Double differentiation pulse slimming is accomplished by a two-pole, low pass with a two-pole high pass feed-forward section that provides complimentary real axis zeros. The zero locations are controlled by a variable attenuator that is set using an internal 7-bit DAC. A range of 0 to 9 dB is available.

FREQUENCY REFERENCE

The 32D4420 programmable frequency reference accepts a TTL compatible clock source or an AC-coupled ECL clock source and generates an ECL compatible reference output. The output frequency of the reference is controlled by programming internal M and N counters to set up internal divide-by ratios. The 7-bit N register sets the divide-by factor for the input clock source. The value of this register is set based upon the frequency of the input clock according to the following equation:

$$N = (FIN \times 256)/72\ MHz$$

The N register can be varied by ±TBD bits for a given input clock frequency. The 8-bit M register sets the divide-by term for the VCO reference clock. The value set in the M register is independent of the input clock frequency. When the N and M registers are set, the resulting frequency output will be:

$$FOUT = [(M+1)/(N+1)] \times FIN$$

POWER DOWN MODES

The 32D4420 includes a power saving mode to support power management. When the PWRON pin is brought low, the device goes into a complete power down mode. In this mode power consumption is reduced to less than 5 mW. During this mode, the serial port registers are powered down. As a result, programming data must be rewritten to the 32D4420 registers upon coming out of the power down mode.

SERIAL PORT OPERATION

The 32D4420 provides a simple serial port interface that allows programming of the device's internal registers. The write-only serial port is a three-line interface that requires an enable signal (SDEN) along with clock (SCLK) and data (SDATA) signals to program the internal registers of the 32D4420. Data is shifted into the registers in 8-bit bytes that are divided into four bits of address and four bits of data. To load data into the device, the enable pin (SDEN) is asserted for eight clock cycles during which data can be presented on the SDATA input pin. Data on the SDATA pin is clocked into the device on the falling edges of the clock signal provided on the SCLK pin. The falling edge of SDEN latches the data internally and initiates the function selected. To save power the serial port circuitry is powered down when the SDEN line is low. Because of this, there is a minimum set-up and hold time for the SDEN signal (refer to specifications.) Table 2 provides the address-to-function mapping for the internal registers.

PIN DESCRIPTION (PRELIMINARY)

INPUT PINS

NAME	TYPE	DESCRIPTION
AGND1	I	Analog ground pin for the filter.
AGND2	I	Analog ground pin for the frequency reference.
DGND	I	Digital ground.
DACI	I	Current DAC output. This output is controlled by the 7-bit DACI register and the resistor connected between VR1 and VR2.
FLTR	I	PLL loop filter pin. An RC filter is connected to this pin to control the VCO voltage.
FOEN	I	This is a TTL compatible input that disables the output buffer of the FOUT pin. This function is used to reduce jitter when the reference output is not required.
FOUT	I	ECL compatible frequency reference output. This output should be AC coupled into the reference input of the data separator device.
FREF	I	Reference clock input for the internal PLL.
IN+/-	I	Differential inputs for the programmable filter. A differential input signal should be AC-coupled into these pins.
OD+/-	I	Differentiated output of the programmable filter. These differential outputs should be AC-coupled into the receiving device.
ON+/-	I	Normal low pass outputs of the programmable filter. These differential outputs should be AC-coupled into the receiving device.
PWRON	I	Active high TTL input signal that enables the device. When this pin is brought low it puts the device into a complete power down mode.
Rx	I	Current input for filter control DACs. An external 1% resistor is connected from Rx to ground to set internal currents for the filter control DACs.
SCLK	I	Serial port clock input used for clocking in data on the SDATA pin. The clock source for this pin should be externally gated with the SDEN signal.
SDATA	I	Serial port input data.
SDEN	I	Serial port enable input.
VR1/VR2	I	Current setting resistor pins. A resistor is connected between these pins to set the current reference for DACI.
VPA1	I	+5V analog power input for the filter.
VPA2	I	+5V analog power input for the frequency reference.
VPA3	I	+5V analog power input for the frequency reference.
VPD	I	+5V digital power input.
TBG_EN	I	Time Base Generator Enable. Active high enables the time base generator portion of the device. A low level disables the TBG portion and reduces power.
FC0	O	Filter Control 0. TTL output used to control an external filter multiplexer.

TABLE 2: Serial Port Register Mapping

ADDRESS BITS				USAGE	DATA BITS			
D7	D6	D5	D4		D3	D2	D1	D0
0	1	1	0	DACI	X	I6	I5	I4
0	1	1	1	DACI	I3	I2	I1	I0
1	0	0	0	PULSE SLIMMING	X	S6	S5	S4
1	0	0	1	PULSE SLIMMING	S3	S2	S1	S0
1	0	1	0	3 dB FREQUENCY	X	F6	F5	F4
1	0	1	1	3 dB FREQUENCY	F3	F2	F1	F0
1	1	0	0	M REGISTER	M7	M6	M5	M4
1	1	0	1	M REGISTER	M3	M2	M1	M0
1	1	1	0	N REGISTER	X	N6	N5	N4
1	1	1	1	N REGISTER	N1	N2	N1	N0

X = Don't care bit.

ELECTRICAL SPECIFICATIONS

Unless otherwise specified recommended operating conditions apply.

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

PARAMETER	RATINGS	UNIT
Storage Temperature	-65 to +150	°C
Junction Operating Temperature, Tj	+130	°C
Supply Voltage, VCC	-0.5 to 7	V
Voltage Applied to Inputs	-0.5 to VCC	V

RECOMMENDED OPERATING CONDITIONS

Supply voltage, VCC	4.65 < VCC < 5.50	V
Ambient Temperature	0 < Ta < 70	°C

POWER SUPPLY CHARACTERISTICS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
ICC	Power Supply Current	PWRON = 0.8V			5	mA
ICC	Power Supply Current	PWRON ≥ 2.2V		35	41	mA
PD	Power Dissipation	PWRON ≥ 2.2V, VCC = 5.0V		175	205	mW
		PWRON ≥ 2.2V, VCC = 5.5V		500		mW

ELECTRICAL SPECIFICATIONS (continued)

DC CHARACTERISTICS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
VIH	High Level Input Voltage	TTL input	2.0			V
VIL	Low Level Input Voltage				0.8	V
IIH	High Level Input Current	VIH = 2.7V			20	µA
IIL	Low Level Input Current	VIL = 0.4V			–1.5	mA

FILTER CHARACTERISTICS

fc	Filter Cutoff Frequency	$fc = \frac{13.33\ \text{MHz}}{\text{mA}}$ (IFI) IFI = 0.11 to .6 mA, TA = 25°C	1.5		8.0	MHz
FCA*	Filter *fc* Accuracy	*fc* = 8 MHz	–10		+10	%
AO	VO_NORM Diff Gain	F = 0.67 *fc*, FB = 0 dB	0.9		1.10	V/V
AD	VO_DIFF Diff Gain	F = 0.67 *fc*, FB = 0 dB	0.90AO		1.1AO	V/V
FB	Frequency Boost at *fc*	$FB(db) = 20\ \log\left[1.884\left(\frac{F}{127}\right)+1\right]$ VBP = MAX		9.2		dB
FBA	Frequency Boost Accuracy	FB = 15 dB	–1		+1	dB
TGD0	Group Delay Variation Without Boost	*fc* = 8 MHz, VBP = 0V F = 0.2 *fc* to *fc*	–1.3		+1.3	ns
		fc = 1.5 MHz - 8 MHz F = 0.2 *fc* to *fc*, VBP = 0V	–2		+2	%
TGDB	Group Delay Variation With Boost	*fc* = 8 MHz, VBP = VR F = 0.2 *fc* to *fc*	–1.3		+1.3	ns
		fc = 1.5 MHz - 8 MHz F = 0.2 *fc* to *fc*, VBP = VR	–2		+2	%
VIF	Filter Input Dynamic Range	THD = 1% max, F = 0.67 *fc*	1.0			Vpp
VOF	Filter Output Dynamic Range	THD = 1% max, F = 0.67 *fc*	1.0			Vpp
VIF	Filter Input Dynamic Range	THD = 3% max, F = 0.67 *fc*	2.0			Vpp
VOF	Filter Output Dynamic Range	THD = 3% max, F = 0.67 *fc*	2.0			Vpp
RIN	Filter Diff Input Resistance		3.0			kΩ
CIN	Filter Input Capacitance				7	pF
EOUT	Output Noise Voltage Differentiated Output	BW = 100 MHz, Rs = 50Ω IFI = 0.6 mA, VBP = 0.0V		6.3		mVRms
EOUT	Output Noise Voltage Normal Output	BW = 100 MHz, Rs = 50Ω IFI = 0.6 mA, VBP = 0.0V		2.7		mVRms
EOUT	Output Noise Voltage Differentiated Output	BW = 100 MHz, Rs = 50Ω IFI = 0.6 mA, VBP = VR		10.3		mVRms
EOUT	Output Noise Voltage Normal Output	BW = 100 MHz, Rs = 50Ω IFI = 0.6 mA, VBP = VR		4.1		mVRms
IO–	Filter Output Sink Current		1.0			mA
IO+	Filter Output Source Current		2.0			mA
RO	Filter Output Resistance (Single ended)				60	Ω

FREQUENCY REFERENCE CHARACTERISTICS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VOH	FOUT ECL High Level	VCD = 5V, VOH-VCD	-1.02			V
VOL	FOUT ECL Low Level	VCD = 5V, VOL-VCD			-1.45	V
IO	FOUT Output Current			±4		mA
VO	FOUT Output Swing		0.6			V

INPUT/OUTPUT CHARACTERISTICS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
FIN	FIN Frequency		8		20	MHz
FO	FOUT Frequency				75	MHz
JFO	FOUT Jitter	TO = 1/FO; FCLK active			±400	ps(pk)
DFO	FOUT Duty Cycle	50% Amplitude FOUT = 72 MHz	42		58	%
M	M Divide Number		80		255	-
N,F	N,F Divide Number		25		127	-
I	I Register Number		30		127	-
RR	External Resistor		4.50		5.25	kΩ
TVCO	VCO Center Frequency Period	TO=(6.17 E-10)(RR/M)+2.4 ns VCC = 5V, RR = 4.75 kΩ FLTR = 2.7V FIN = 20 MHz, M = 100	0.77TO	TVCO	1.23TO	ns
	VCO Frequency Dynamic Range	1V < FLTR < VCC – 0.5V, VCC = 5V, FOUT = 31.5 MHz	±25		±45	%
KVCO	VCO Control Gain	ωi = 2π/TVCO	0.14ωi		0.26ωi	rad/s V
KD	Phase Detector	KD = (4.16 E-3)/RR		KD		A/rad
IOI	DACI Current	IO = (7.41 E-2)I/RR VCC = 5V, TA = 25°C, RR = 4.75kΩ	0.95IO –3/4LSB		1.05IO +3/4LSB	A
Rx			2.5		3.0	kΩ
I	DAC Current Tolerance	RR = 4.75 kΩ 0°C <Ta< 70°C 4.75V < Vcc < 5.25V	.81 IO		1.17 IO	A
I	Differential Linearity (Monotonicity)	0°C Ta<70°C 4.75V < Vcc < 5.25V	-1LSB			-

INPUT/OUTPUT CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
SCLK Data Clock Period, TC		100			ns
TDD Data Set Up/Hold Time		25			ns
TDE Data Enable Delay Time	Delay from data clock rising edge	– TC		TC/4	ns

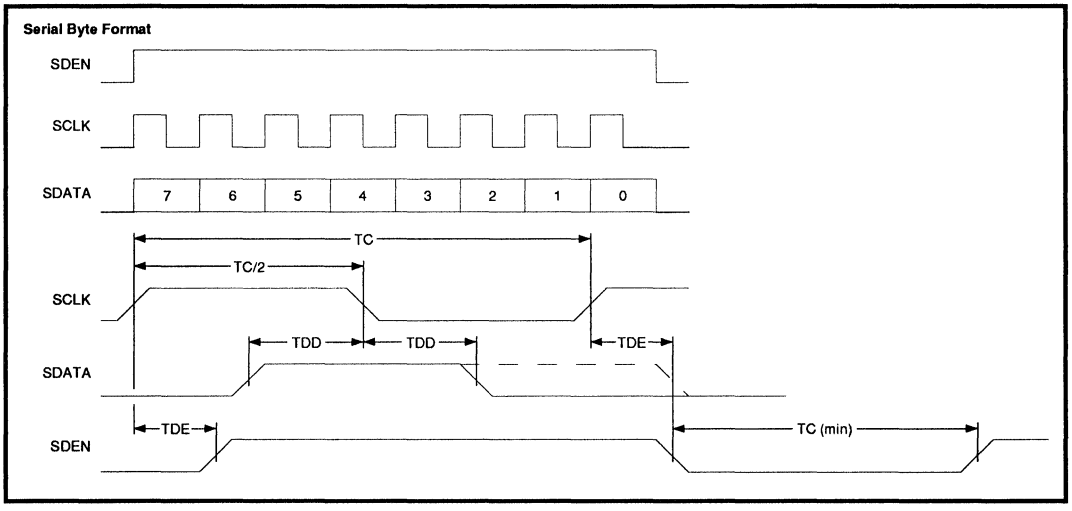


FIGURE 1: Serial Port Timing

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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Notes:

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SSI 32D4660
Time Base Generator
Preliminary Data

December 1991

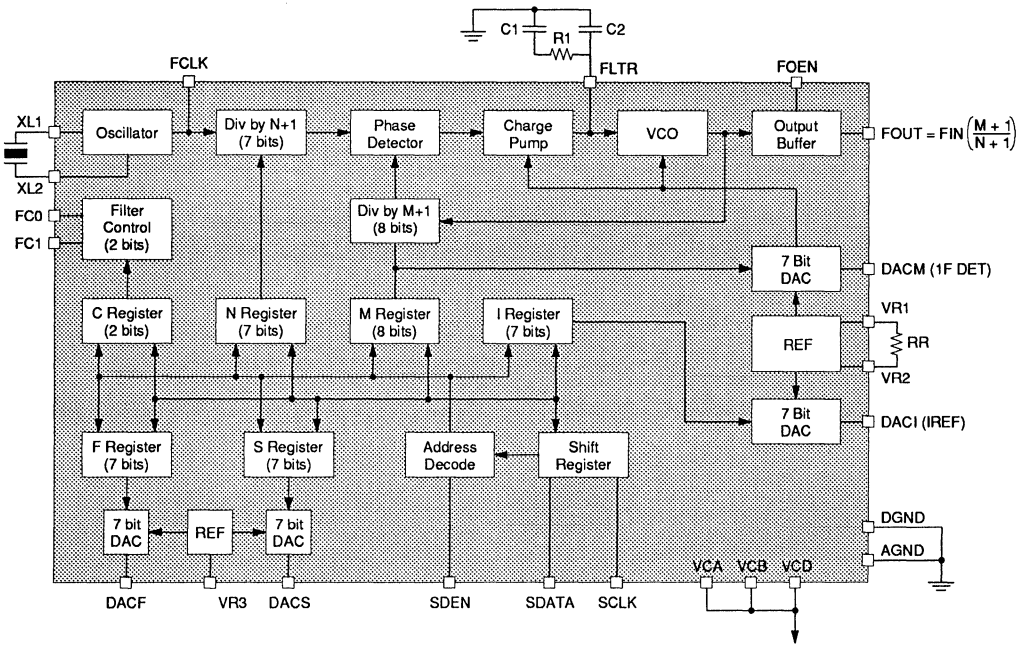
DESCRIPTION

The SSI 32D4660 Time Base Generator provides a programmable reference generator, channel filter control and data rate control for constant density recording applications. It is optimized to operate with the SSI 32P4620 pulse detector data separator combo device. The SSI 32D4660 contains a high performance programmable PLL for 1% reference frequency control. A 7-bit DAC is provided to program the IREF current which sets the data separator PLL operating center frequency. A 7-bit DAC is provided to program the 1FDET current which sets the timing for the data separator synch field detect. Two additional 7-bit DAC's are provided for programmable electronic filter (slimmer) control. Two latched TTL outputs are provided to control filter multiplexers. A serial microprocessor interface reduces pin count and provides convenient access to the internal program storage registers. The 32D4660 only requires a +5V supply and will be available in 24-pin SO packages.

FEATURES

- **For constant density recording applications when utilized with SSI 32P4620**
- **Reference frequency control**
- **Internal DAC available to program data separator data rate**
- **Internal DAC available to program data separator sync field detect timing**
- **Up to 75 MHz operation**
- **1% frequency resolution**
- **No external active components required**
- **+5V only operation**
- **Low power mode**
- **24-pin SOL package**

BLOCK DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

PIN DESCRIPTIONS

INPUT PINS

NAME	DESCRIPTION
SDATA	Serial Data. Data input for an 8-bit control shift register. The data packet is transmitted MSB (D7) first. The first four bits are the register address and the last four are its data bits. Registers larger than 4-bits must be loaded with two 8-bit data packets. These packets should be loaded sequentially in less than 10 µs since the loading operation will cause output transients. With proper loop filter design, the output transients will recover within 1 ms. The data packet fields are given in Table 1.
SCLK	Serial Data Clock. Negative edge triggered clock input for the serial data.
SDEN	Serial Data Enable. A high level input enables data loading. The data is latched when the input is low.
FOEN	Frequency Output Enable. A high level input enables the FOUT output. A low level disables the output and minimizes the driven data separator jitter.

OUTPUT PINS

FOUT	Frequency Output. An ECL output with internal current source. The low voltage swing which minimizes data separator jitter must be AC coupled to the data separator XLT1 input. FOUT = [(M +1)/(N +1)]FIN where M = M Register number and N must be set to approximately [(FIN) (256) / 72MHz] - 1
DAC M	DAC Output. 7-bit DAC current sink output used to program timing current to the data separator sync field detect SDS pin. The current magnitude is controlled by the 7 MSB's of the M Register and is compensated to minimize the sensitivity to power supply and temperature variations. If this output isn't required, the pin must be connected to VCC.
DAC I	DAC Output. 7-bit DAC current source output used to program timing current for the data separator VCO center frequency. The current magnitude is controlled by the I Register and is compensated to minimize the sensitivity to power supply and temperature variations.
DAC F	DAC Output. 7-bit DAC voltage output used for electronic filter control. The output voltage is set by the voltage at VR3 and the F Register number.
DAC S	DAC Output. Similar to DAC F except controlled by the S Register number.
FC0	Filter Control 1. TTL output used to control an external filter multiplexer. C0 = H sets FC0 = H.
FC1	Filter Control 2. TTL output used to control an external filter multiplexer. C1 = H sets FC1 = H.

OUTPUT PINS (Continued)

NAME	DESCRIPTION
FCLK	Clock Output. Optional TTL output that may be used for a system clock. The output frequency is the same as the oscillator output frequency. For minimum FOUT jitter, parts with FCLK disabled should be used. FCLK remains active when PWR ON is low.

ANALOG PINS

XTL1, XTL2	Crystal Oscillator Connections. The circuit is designed to be used with an 8 MHz to 20 MHz crystal. If a crystal is not desired, XTL1 may be driven by a TTL source with XTL2 left open.
VR1, VR2	Current Setting Resistor Connections. An external resistor RR connected between VR1 and VR2 sets the DACM and DACI currents.
VR3	Reference Voltage Input. An external 2.2V supply sets the reference for the DACF and DACS currents.
FLTR	PLL Loop Filter Connection. Connection for loop filter components R1, C1 and C2.
DGND, AGND	Digital and Analog Ground
VCA, VCB	Analog +5V Supplies
VCD	Digital +5V Supply

TABLE 1: Data Packet Fields

ADDRESS BITS				USAGE	DATA BITS			
D7	D6	D5	D4		D3	D2	D1	D0
0	1	1	0	I REGISTER	X	I6	I5	I4
0	1	1	1	I REGISTER	I3	I2	I1	I0
1	0	0	0	F, C, REGISTER	C1	F6	F5	F4
1	0	0	1	F REGISTER	F3	F2	F1	F0
1	0	1	0	S, C, REGISTER	C0	S6	S5	S4
1	0	1	1	S REGISTER	S3	S2	S1	S0
1	1	0	0	M REGISTER	M7	M6	M5	M4
1	1	0	1	M REGISTER	M3	M2	M1	M0
1	1	1	0	N REGISTER	X	N6	N5	N4
1	1	1	1	N REGISTER	N1	N2	N1	N0

X = Don't care bit.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

PARAMETER	RATING
Storage Temperature	–65 to +150°C
Junction Operating Temperature, Tj	+150°C
Supply Voltage, VCA, VCB, VCD	–0.5 to 7V
Voltage Applied to Logic Inputs	–0.5 to 5.5V
Maximum Power Dissipation	540 mW

RECOMMENDED OPERATING CONDITIONS

PARAMETER	RATING	UNITS
Supply voltage, VCA = VCB = VCD	4.65<VCC<5.25	V
Junction Temperature, Tj	0<Tj<135	°C
Ambient Temperature, Ta	0<Ta<70	°C

ELECTRICAL CHARACTERISTICS

Unless Otherwise Specified: 4.65V<VCC<5.25, 0°C<Ta<70°C

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VIH	High Level Input Voltage		2.0			V
VIL	Low Level Input Voltage				0.8	V
IIH	High Level Input Current	VIH = 2.7V			20	µA
IIL	Low Level Input Current	VIL = 0.4V			–1.5	mA
VOH	High Level Output Voltage	IOH = -400 µA	2.4			V
VOL	Low Level Output Voltage	IOL = 2 mA			0.5	V
VOH	FOUT ECL High Level	VCD = 5V, VOH-VCD	–1.02			V
VOL	FOUT ECL Low Level	VCD = 5V, VOL-VCD			–1.45	V
ICC	Power Supply Current			77	103	mA
IO	FOUT Output Current			±4		mA
VO	FOUT Output Swing		0.6			V

INPUT/OUTPUT CHARACTERISTICS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
FIN	FIN Frequency		8		20	MHz
FO	FOUT Frequency				75	MHz
JFO	FOUT Jitter	TO = 1/FO; FCLK active			±400	ps(pk)
DFO	FOUT Duty Cycle	50% Amplitude FOUT = 72 MHz	42		58	%
F	F Register Number		0		127	-
S	S Register Number		0		127	-
M	M Divide Number		80		255	-
N	N Divide Number		25		127	-
I	I Register Number		30		127	-
RR	External Resistor		4.50		5.25	kΩ
TVCO	VCO Center Frequency Period	TO=(6.17 E-10)(RR/M)+2.4 ns VCC = 5V, RR = 4.75 kΩ FLTR = 2.7V M = 100; FIN = 20 MHz	0.77TO	TVCO	1.23TO	ns
	VCO Frequency Dynamic Range	1V < FLTR < VCC – 0.5V, VCC = 5V, Fout = 31.5 MHz	±25		±45	%
KVCO	VCO Control Gain	ωi = 2π/TVCO	0.14ωi		0.26ωi	rad/s V
KD	Phase Detector	KD = (4.16E – 3)/RR		KD		A/rad
IOM	DACM Current	IO = (1.641 E-2) M/RR VCC = 5V, TA = 25°C, RR = 4.75kΩ	0.97IO –1LSB		1.03IO +1LSB	A
IOI	DACI Current	IO = (7.41 E-2)I/RR VCC = 5V, TA = 25°C, RR = 4.75kΩ	0.95IO –3/4LSB		1.05IO +3/4LSB	A
VOF	DACF Voltage	VOF = 0.98 F*VR3/127, VCC = 5V	0.97VOF –3/4LSB +15 mV		1.03VOF +3/4LSB +60 mV	V
VOS	DACS Voltage	VOS = 0.98 S*VR3/127 VCC = 5V	0.97VOS –3/4LSB +15 mV		1.03VOS +3/4LSB +60 mV	V
VR3	DAC Reference		2.0		2.4	V
IVR3	VR3 Input Current	VR3 = 2.2V			1.0	mA
I, M	DAC Current Tolerance	RR = 4.75 kΩ 0°C <Ta< 70°C 4.75V < Vcc < 5.25V	.81 IO		1.17 IO	A

INPUT/OUTPUT CHARACTERISTICS (Continued)

PARAMETER		CONDITIONS	MIN	MAX	UNITS
I, F, M, S	Differential Linearity (Monotonicity)	0°C Ta<70°C 4.75V < Vcc < 5.25V	-1LSB		-
VODH	DACM Output Voltage		2.5	VCC	V
VODL	DACI Output Voltage			2	V
VOFL	DACF, DACS Output Voltage		0.1	2.4	V
ROUT	DACF, DACS Output Resistance			3.7	kΩ
SCLK	Data Clock Period, TC		100		ns
TDD	Data Set Up/Hold Time		25		ns
TDE	Data Enable Delay Time	Delay from data clock rising edge	– TC	TC/4	ns

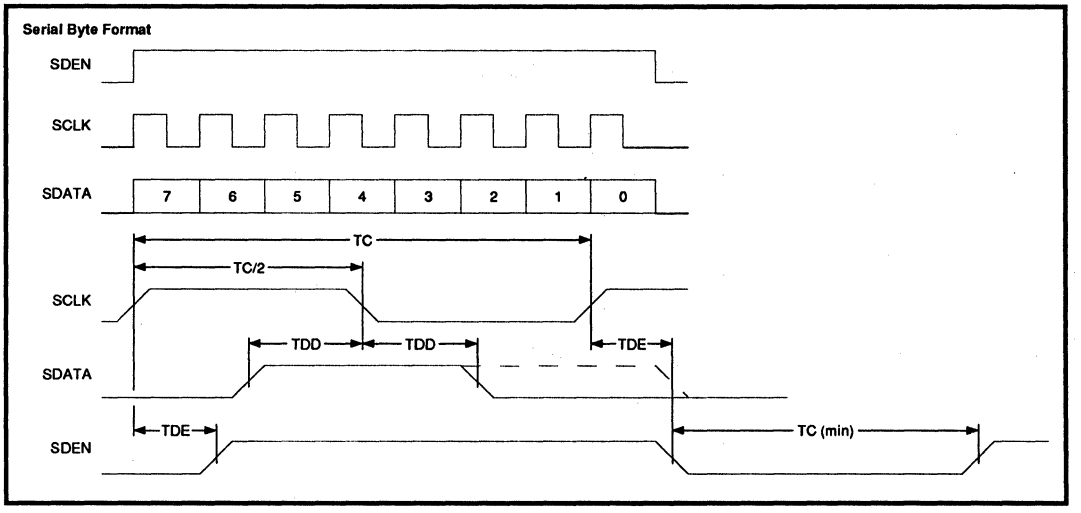


FIGURE 1: Serial Port Timing

APPLICATIONS INFORMATION

The serial port allows the user to program the internal registers of the 32D4660 device. This port has been designed to operate with the serial port on most microcontrollers such as the 8051. Silicon Systems also provides a serial port board that can be used to operate the serial interface. The serial port consists of three lines: enable (SDEN or SERMODE), data (SDATA), and clock (SCLK). During a serial data transfer, eight bits of data should be transferred to the selected device. The first four bits of data contain register address information while the last four bits contain the programming data. The timing considerations for the serial port are fairly straight forward (see Figure 2). The enable line is driven high to initiate the data transfer. While the enable line is high, the transmitting device should output eight clock pulses along with eight bits of synchronous programming data. The data is shifted internally on the falling edge of the clock pulses. To prevent false data from being latched in, only eight (8) clock pulses should be provided while the enable line is active. The falling edge of the enable input will latch the data into the internal registers and initiate the selected function.

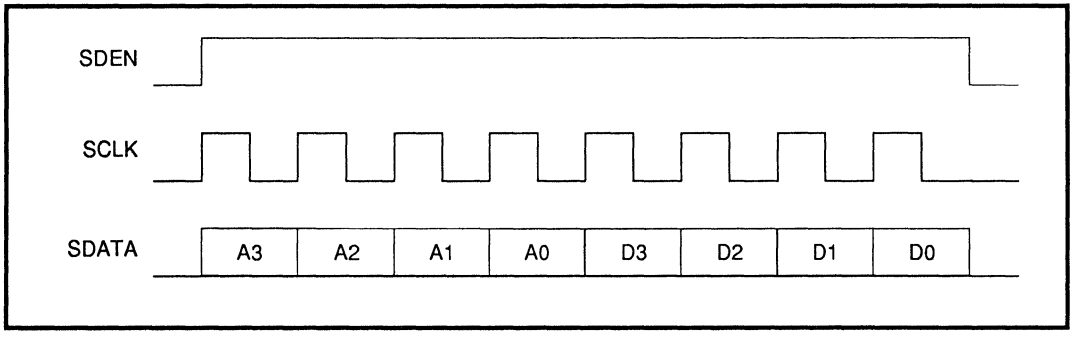


FIGURE 2: Serial Port Timing

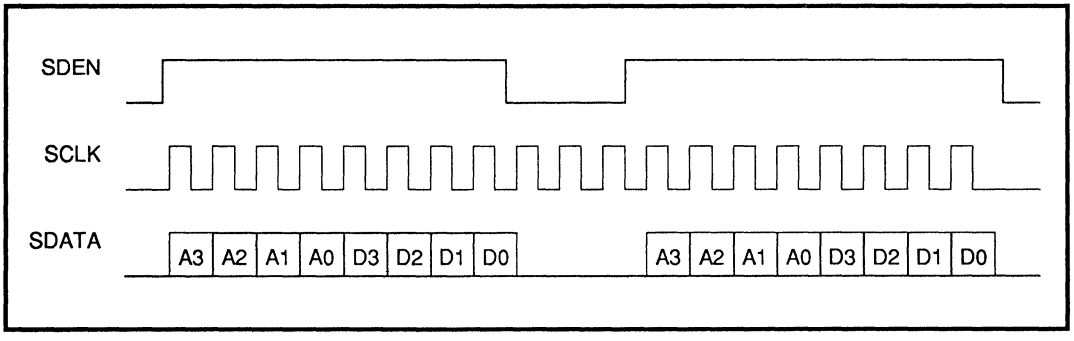


FIGURE 3: Serial Port Timing, Multiple Transfers

APPLICATIONS INFORMATION (continued)

REFERENCE FREQUENCY OUTPUT:

The 32D4660 provides the reference frequency for the phase-locked loop (PLL) of a data separator. The required frequency is programmed using the **M** and **N** registers of the 4660. The value of the **N** register is determined by the oscillator that drives the 32D4660 according to the following equation:

$$N=\frac{(Fin \cdot 256)}{(72\ MHz)}-1$$

For this application, using a 12 MHz oscillator (Fin) would yield an **N** value of 41.7. Although the value of **N** should be fixed according to the equation shown above, there is a tolerance of ± 1 integer so **N** can be set from 41 to 43. (This is necessary as the phase detector frequency is fixed by Fin & **N**) Substituting **N** into the following equation and knowing the reference frequency required for each data rate allows for the determination of the **M** register value:

$$Fout=\frac{(M+1)}{(N+1)} \cdot Fin$$

Since **M** must be an integer value, it may be necessary to change **N** values for each data rate to obtain the required output frequency. For example (for 3x reference clock), at 12 Mbit/s the required reference frequency is 36 MHz and using a value of **N** = 41, yields an **M** value of 125. At 13 Mbit/s using the **N** value of 41 would require an **M** value of 135.5 to produce an output frequency of 39 MHz. Using **M** = 135 would give an output frequency of 38.86 MHz while using an **M** value of 136 the output frequency would be 39.14 MHz. If **N** is changed to 43 then a value of 143 for **M** would produce the required output frequency of 39 MHz. The required **M** and **N** values for some sample data rates are provided in the table that follows.

TABLE 1: M and N Register Programming Example

DR (Mbit/s)	Fout	M	N
12 Mb/s	36 MHz	125	41
13 Mb/s	39 MHz	142	43
14 Mb/s	42 MHz	146	41
15 Mb/s	45 MHz	164	43

The **N** register is at address "1110" for the MSBs and address "1111" for the LSBs. The table that follows gives the required register programming information for the values of **N**.

TABLE 2: Frequency Programming Information, N Register

ADDRESS BITS				DATA BITS				FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
1	1	1	0	X	0	1	0	N Register MSBs for N = 41
1	1	1	1	1	0	0	1	N Register LSBs for N = 41
1	1	1	0	X	0	1	0	N Register MSBs for N = 43
1	1	1	1	1	0	1	1	N Resgister LSBs for N = 43

The **M** register is at address "1100" for the MSB's and at address "1101" for the LSB's. The table that follows gives the required register programming information for the values of **M** based on the equation given above for Fout.

TABLE 3: Frequency Programming Information, M Register

ADDRESS BITS				DATA BITS				FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
1	1	0	0	0	1	1	1	M Register = 125,
1	1	0	1	1	1	0	1	Fout = 36 MHz
1	1	0	0	1	0	0	0	M Register = 142,
1	1	0	1	1	1	1	0	Fout = 39 MHz
1	1	0	0	1	0	0	1	M Register = 146,
1	1	0	1	0	0	1	0	Fout = 42 MHz
1	1	0	0	1	0	1	0	M Register = 164,
1	1	0	1	0	1	0	0	Fout = 45 MHz

4

LOOP FILTER FOR THE 32D4660:

The 32D4660 requires a loop filter to control the PLL locking characteristics. While there are several types of filters that can be used to perform this function, a simple integrating filter has proven to be very effective (see Figure 4). To select the components for the loop filter, two considerations should be made. First, the acquisition time of the loop must be less than the minimum track-to-track seek time and second, the capacitor C1 should be low leakage (C1 < 1.0 μF). The acquisition time of the loop is set-up to accommodate a zero phase restart and allow for 1% maximum phase error after phase acquisition. This yields a settling time of: $t_s = 5/\omega_n$.

From the data sheet,

KVCO = $(0.21)(2\pi)(F_{out})$ rad/s V (typ.), at 72MHz KVCO = 9.5×10^7

KD = (4.14 E-3)/RR A/rad @ RR = 4.75KΩ, KD = 8.76×10^{-7}

For a second order system,

R1 = $(2 \times \zeta \times \omega_n)/(KVCO \times KD)$ where ζ is the damping factor.

C1 = $(KVCO \times KD)/(\omega_n^2)$ and C1/10 > C2 > C1/20

A damping factor of 0.7 to 1.0 is suggested to prevent locking to harmonics while maintaining an acceptable lock time. At the maximum frequency selected, the damping factor of 1.0 should be considered thereby allowing the damping factor to drop as the frequency drops.

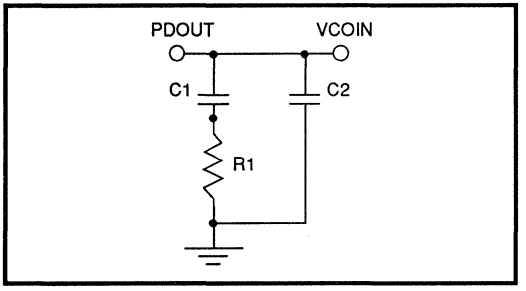
If we start with $\omega_n = 2 \times 10^4$, C1 can be calculated as 0.21 μF and C2 can be calculated as 0.01 to 0.02 μF. As mentioned above, the damping factor at the maximum frequency of 72 MHz should be 1.0, so R1 is calculated as:

R1 = (2 x 1.0 x 2E4)/(9.5E7 x 8.76E-7) = 480 ohms

These values will produce a loop settling time t_s of $5/2 \times 10^4$ = 250 μsecs.

The values calculated here are sample values that have been used in the lab and should be considered starting values. The values of R1, C1, and C2 can be further optimized to meet specific needs.

SSI 32D4660
Time Base Generator

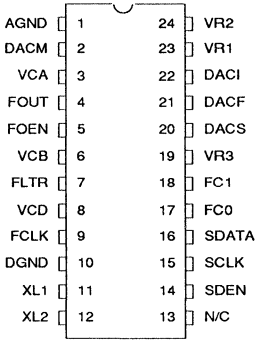


2 Single Rate

FIGURE 4: Integrating Filter for the Phase Locked Loop.

NOTE: For further information on the loop filter consult the Data Synchronizer Family Application Notes in chapter 4 of the Silicon Systems Storage Products data book.

PIN DIAGRAM
(Top View)



24 Pin SOL

ORDERING INFORMATION

PART DESCRIPTION	ORDERING NUMBER	PACKAGE MARK
SI 32D4660, Time Base Generator		
24-Pin SOL	32D4660-CL	32D4660-CL

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 731-7110, FAX (714) 573-6914

silicon systems®
A TDK Group Company

SSI 32D4661/4662
Time Base Generator

Preliminary Data

December 1991

4

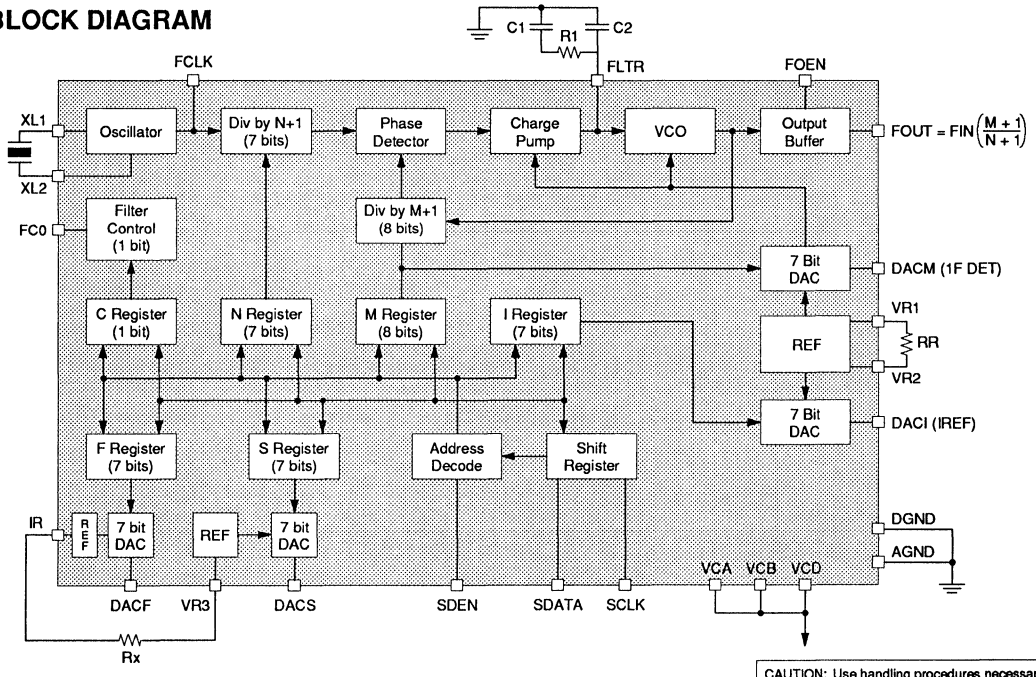
DESCRIPTION

The SSI 32D4661/4662 Time Base Generator provides a programmable reference generator, channel filter control and data rate control for constant density recording applications. It is optimized to operate with the 32D53xx series data separators and contains a high performance programmable PLL for 1% reference frequency control. A 7–bit DAC, DACI is provided to program the IREF current which sets the data separator PLL operating center frequency. A 7–bit DAC, DACM is provided to program the 1FDET current which sets the timing for the data separator synch field detect. Two additional 7–bit DACs are provided for programmable electronic filter (slimmer) control. DACS controls the boost while DACF controls the cutoff frequency of the electronic filter. A latched TTL output is provided to control filter multiplexer. A serial microprocessor interface reduces pin count and provides convenient access to the internal program storage registers. The 32D4661/4662 only requires a +5V supply and is available in 24-pin SO packages.

FEATURES

- **Not plug compatible with SSI 32D4660**
- **For constant density recording applications**
- **Reference frequency control**
- **Channel filter control**
- **Internal DAC available to program data separator data rate**
- **Internal DAC available to program data separator sync field detect timing**
- **Up to 72 MHz operation for the 32D4661**
- **Up to 108 MHz operation for the 32D4662**
- **1% frequency resolution**
- **No external active components required**
- **+5V only operation**
- **Low power mode**
- **24-pin SOL/SSOP package**

BLOCK DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

PIN DESCRIPTION

INPUT PINS

NAME	DESCRIPTION
SDATA	Serial Data. Data input for an 8-bit control shift register. The data packet is transmitted MSB (D7) first. The first four bits are the register address and the last four are its data bits. Registers larger than 4-bits must be loaded with two 8-bit data packets. These packets should be loaded sequentially in less than 10 µs since the loading operation will cause output transients. With proper loop filter design, the output transients will recover within 1 ms. The data packet fields are given in Table 1.
SCLK	Serial Data Clock. Negative edge triggered clock input for the serial data.
SDEN	Serial Data Enable. A high level input enables data loading. The data is latched when the input is low.
FOEN	Frequency Output Enable. A high level input enables the FOUT output. A low level disables the output and minimizes the driven data separator jitter.

OUTPUT PINS

FOUT	Frequency Output. An ECL output with internal current source. The low voltage swing which minimizes data separator jitter must be AC coupled to the data separator XTL1 input. FOUT = [(M +1)/(N +1)]FIN where M = M Register number and N must be set to approximately 32D4661: [(FIN) (256) / 72 MHz] - 1; 32D4662: [(FIN) (256) / 108 MHz] - 1
DACM	DAC Output. 7-bit DAC current sink output used to program timing current to the data separator sync field detect SDS pin. The current magnitude is controlled by the 7 MSB's of the M Register and is compensated to minimize the sensitivity to power supply and temperature variations. If this output isn't required, the pin must be connected to VCC.
DACI	DAC Output. 7-bit DAC current source output used to program timing current for the data separator VCO center frequency. The current magnitude is controlled by the I Register and is compensated to minimize the sensitivity to power supply and temperature variations.
DACF	DAC Output. 7-bit DAC current output used for electronic filter control. The output current is set by the voltage at VR3, and the F Register number and an external resistor Rx.
DACS	DAC Output. 7-bit DAC voltage output used for electronic filter control. The output voltage is set by the voltage at VR3 and the S Register number.
FC0	Filter Control 0. TTL output used to control an external filter multiplexer. C0 = H sets FC0 = H.

OUTPUT PINS (Continued)

NAME	DESCRIPTION
FCLK	Clock Output. Optional TTL output that may be used for a system clock. The output frequency is the same as the oscillator output frequency. For minimum FOUT jitter, this pin should be a no connect. FCLK remains active when PWR ON is low.

ANALOG PINS

XTL1, XTL2	Crystal Oscillator Connections. The circuit is designed to be used with an 8 MHz to 20 MHz crystal. If a crystal is not desired, XTL1 may be driven by a TTL source with XTL2 left open.
VR1, VR2	Current Setting Resistor Connections. An external resistor RR connected between VR1 and VR2 sets the DACM and DACI currents.
VR3	Reference Voltage Input. An external 2.2V supply sets the reference for the DACS voltage.
IR	Reference Current Input. An external resistor Rx, connected from IR to VR3 reference voltage sets the reference current for the DACF current.
FLTR	PLL Loop Filter Connection. Connection for loop filter components R1, C1 and C2.
DGND, AGND	Digital and Analog Ground
VCA, VCB	Analog +5V Supplies
VCD	Digital +5V Supply

TABLE 1: Data Packet Fields

ADDRESS BITS				USAGE	DATA BITS			
D7	D6	D5	D4		D3	D2	D1	D0
0	1	1	0	I REGISTER	X	I6	I5	I4
0	1	1	1	I REGISTER	I3	I2	I1	I0
1	0	0	0	S REGISTER	X	S6	S5	S4
1	0	0	1	S REGISTER	S3	S2	S1	S0
1	0	1	0	F, C REGISTER	C0	F6	F5	F4
1	0	1	1	F REGISTER	F3	F2	F1	F0
1	1	0	0	M REGISTER	M7	M6	M5	M4
1	1	0	1	M REGISTER	M3	M2	M1	M0
1	1	1	0	N REGISTER	X	N6	N5	N4
1	1	1	1	N REGISTER	N1	N2	N1	N0

X = Don't care bit.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

PARAMETER	RATING
Storage Temperature	–65 to +150°C
Junction Operating Temperature, Tj	+150°C
Supply Voltage, VCA, VCB, VCD	–0.5 to 7V
Voltage Applied to Logic Inputs	–0.5 to 5.5V
Maximum Power Dissipation	540 mW

RECOMMENDED OPERATING CONDITIONS

PARAMETER	RATING	UNITS
Supply voltage, VCA = VCB = VCD	4.65 to 5.25	V
Junction Temperature, Tj	0<Tj<135	°C
Ambient Temperature, Ta	0<Ta<70	°C

ELECTRICAL CHARACTERISTICS

Unless Otherwise Specified: Recommended operating conditions apply

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VIH	High Level Input Voltage		2.0			V
VIL	Low Level Input Voltage				0.8	V
IIH	High Level Input Current	VIH = 2.7V			20	µA
IIL	Low Level Input Current	VIL = 0.4V			-1.5	mA
VOH	High Level Output Voltage	IOH = -400 µA	2.4			V
VOL	Low Level Output Voltage	IOL = 2 mA			0.5	V
VOH	FOUT ECL High Level	VCD = 5V, VOH-VCD	-1.02			V
VOL	FOUT ECL Low Level	VCD = 5V, VOL-VCD			-1.45	V
ICC	Power Supply Current			77	103	mA
IO	FOUT Output Current			±4		mA
VO	FOUT Output Swing		0.6			V

INPUT/OUTPUT CHARACTERISTICS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
FIN	FIN Frequency		8		20	MHz
FO	FOUT Frequency	32D4661			72	MHz
		32D4662			108	MHz
JFO	FOUT Jitter	TO = 1/FO; FCLK active			±400	ps(pk)
DFO	FOUT Duty Cycle	50% Amplitude 32D4661: FOUT = 72 MHz 32D4662: FOUT = 108 MHz	42		58	%
F	F Register Number		0		127	-
S	S Register Number		0		127	-
M	M Divide Number		80		255	-
N	N Divide Number		25		127	-
I	I Register Number		30		127	-
RR	External Resistor		4.50		5.25	kΩ
TVCO	VCO Center Frequency Period	32D4661: TO=(6.17)(RR/M)+2.4 ns 32D4662: TO=(4.08)(RR/M)+2.4 ns VCC = 5V, RR = 4.75 kΩ FLTR = 2.7V M = 100	0.77TO	TVCO	1.23TO	ns
	VCO Frequency Dynamic Range	1V < FLTR < VCC – 0.5V, VCC = 5V, M = 100	±25		±45	%
KVCO	VCO Control Gain	ωi = 2π/TVCO	0.14ωi		0.26ωi	rad/s V
KD	Phase Detector	KD = (4.16E – 3)/RR		KD		A/rad
IOM	DACM Current	IO = (1.641E-2) M/RR VCC = 5V, TA = 25°C, RR = 4.75kΩ	0.97IO –1LSB		1.03IO +1LSB	A
IOI	DACI Current	IO = (7.41E-2)I/RR VCC = 5V, TA = 25°C, RR = 4.75kΩ	0.97IO –3/4LSB		1.05IO +3/4LSB	A
IOF	DACF Current	IOF = 0.98 F*4/128 • IR VCC = 5V, Rx = 2.74 kΩ Where IR = VR3/(4*Rx) or an external current source	0.97IOF –3/4LSB		1.03IOF +3/4LSB	V
VOS	DACS Voltage	VOS = 0.98 S*VR3/127 VCC = 5V	0.97VOS –3/4LSB +15 mV		1.03VOS +3/4LSB +60 mV	V
VR3	DAC Reference		2.0		2.4	V
IVR3	VR3 Input Current	VR3 = 2.2V			1.0	mA

INPUT/OUTPUT CHARACTERISTICS (Continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Rx			2.5		3.0	kΩ
I, M	DAC Current Tolerance	RR = 4.75 kΩ 0°C < Ta < 70°C 4.75V < Vcc < 5.25V	.81 IO		1.17 IO	A
I, F, M, S	Differential Linearity (Monotonicity)	0°C<Ta<70°C 4.75V < Vcc < 5.25V	-1LSB			-
VODH	DACM Output Voltage		2.5		VCC	V
VODL	DACI Output Voltage				2	V
VOFL	DACF, DACS Output Voltage		0.1		2.4	V
ROUT	DACF, DACS Output Resistance				3.7	kΩ
SCLK	Data Clock Period, TC		100			ns
TDD	Data Set Up/Hold Time		25			ns
TDE	Data Enable Delay Time	Delay from data clock rising edge	– TC		TC/4	ns

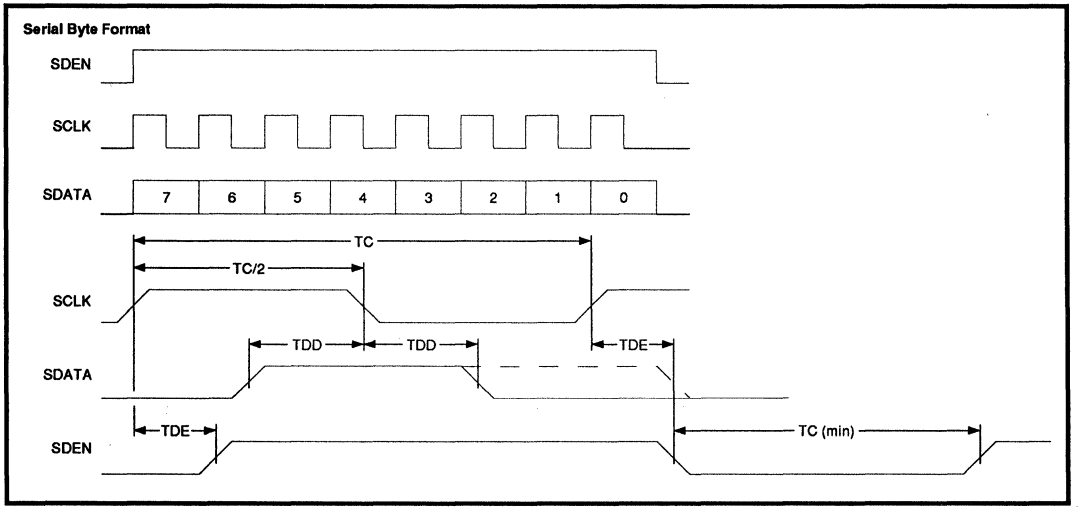


FIGURE 1: Serial Port Timing

APPLICATIONS INFORMATION

The serial port allows the user to program the internal registers of the 32D4661/4662 device. This port has been designed to operate with the serial port on most microcontrollers such as the 8051. Silicon Systems also provides a serial port board that can be used to operate the serial interface. The serial port consists of three lines: enable (SDEN or SERMODE), data (SDATA), and clock (SCLK). During a serial data transfer, eight bits of data should be transferred to the selected device. The first four bits of data contain register address information while the last four bits contain the programming data. The timing considerations for the serial port are fairly straight forward (see Figure 2). The enable line is driven high to initiate the data transfer. While the enable line is high, the transmitting device should output eight clock pulses along with eight bits of synchronous programming data, four address bits followed by four data bits. The data is shifted internally on the falling edge of the clock pulses. To prevent false data from being latched in, only eight (8) clock pulses should be provided while the enable line is active. The falling edge of the enable input will latch the data into the internal registers and initiate the selected function.

Note: it takes two transfers to load a single register.

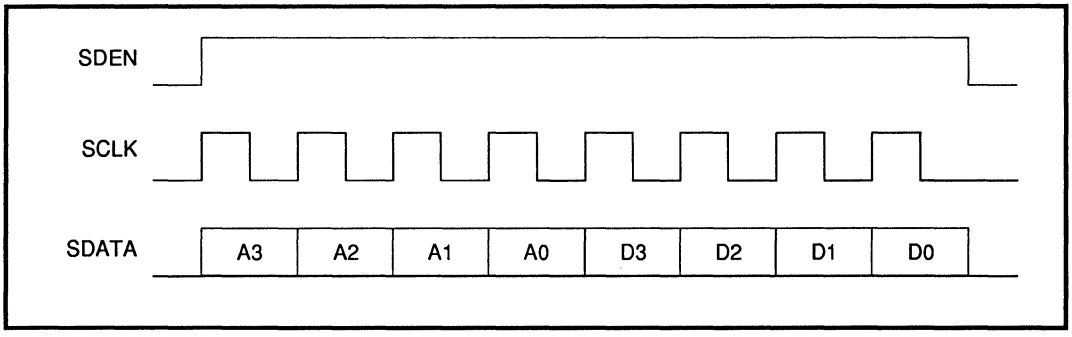


FIGURE 2: Serial Port Timing

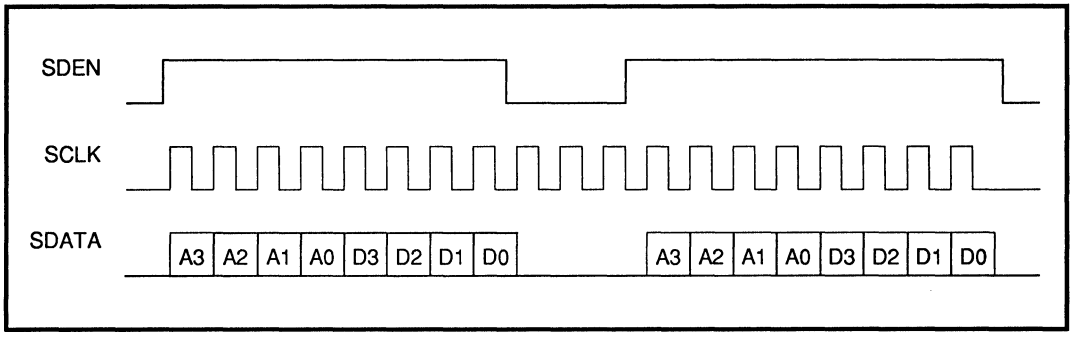


FIGURE 3: Serial Port Timing, Multiple Transfers

APPLICATIONS INFORMATION (continued)

REFERENCE FREQUENCY OUTPUT:

The 32D4661/4662 provides the reference frequency for the phase-locked loop (PLL) of a data separator. The required frequency is programmed using the **M** and **N** registers of the 4661/4662.

32D4661:
The value of the **N** register is determined by the oscillator that drives the 32D4661 according to the following equation:

$$N=\frac{(Fin \cdot 256)}{(72\ MHz)}-1$$

For this application, using a 12 MHz oscillator (Fin) would yield an **N** integer value of 42. Although the value of **N** should be fixed according to the equation shown above, there is a tolerance of ± 1 integer so **N** can be set from 41 to 43. (This is necessary as the phase detector frequency is fixed by Fin & **N**) Substituting **N** into the following equation and knowing the reference frequency required for each data rate allows for the determination of the **M** register value:

$$Fout=\frac{(M+1)}{(N+1)} \cdot Fin$$

Since **M** must be an integer value, it may be necessary to change **N** values for each data rate to obtain the required output frequency. For example (for 3x reference clock), at 12 Mbit/s the required reference frequency is 36 MHz and using a value of **N** = 41, yields an **M** value of 125. At 13 Mbit/s using the **N** value of 41 would require an **M** value of 135.5 to produce an output frequency of 39 MHz. Using **M** = 135 would give an output frequency of 38.86 MHz while using an **M** value of 136 the output frequency would be 39.14 MHz. If **N** is changed to 43 then a value of 143 for **M** would produce the required output frequency of 39 MHz. The required **M** and **N** values for some sample data rates are provided in the table that follows.

TABLE 1: M and N Register Programming Example

DR (Mbit/s)	Fout	M	N
12 Mb/s	36 MHz	125	41
13 Mb/s	39 MHz	142	43
14 Mb/s	42 MHz	146	41
15 Mb/s	45 MHz	164	43

The **N** register is at address "1110" for the MSBs and address "1111" for the LSBs. The table that follows gives the required register programming information for the values of **N**.

TABLE 2: Frequency Programming Information, N Register

ADDRESS BITS				DATA BITS				FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
1	1	1	0	X	0	1	0	N Register MSBs for N = 41
1	1	1	1	1	0	0	1	N Register LSBs for N = 41
1	1	1	0	X	0	1	0	N Register MSBs for N = 43
1	1	1	1	1	0	1	1	N Resgister LSBs for N = 43

APPLICATIONS INFORMATION (continued)

The **M** register is at address "1100" for the MSB's and at address "1101" for the LSB's. The table that follows gives the required register programming information for the values of **M** based on the equation given above for Fout.

TABLE 3: Frequency Programming Information, M Register

ADDRESS BITS				DATA BITS				FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
1	1	0	0	0	1	1	1	M Register = 125,
1	1	0	1	1	1	0	1	Fout = 36 MHz
1	1	0	0	1	0	0	0	M Register = 142,
1	1	0	1	1	1	1	0	Fout = 39 MHz
1	1	0	0	1	0	0	1	M Register = 146,
1	1	0	1	0	0	1	0	Fout = 42 MHz
1	1	0	0	1	0	1	0	M Register = 164,
1	1	0	1	0	1	0	0	Fout = 45 MHz

32D4662:
The value of the **N** register is determined by the oscillator that drives the 32D4662 according to the following equation:

$$N=\frac{(Fin \cdot 256)}{(108\ MHz)}-1$$

For this application, using a 20 MHz oscillator (Fin) would yield an **N** value of 46.4. Although the value of **N** should be fixed according to the equation shown above, there is a tolerance of ± 1 integer so **N** can be set from 45 to 47. (This is necessary as the phase detector frequency is fixed by Fin & **N**) Substituting **N** into the following equation and knowing the reference frequency required for each data rate allows for the determination of the **M** register value:

$$Fout=\frac{(M+1)}{(N+1)} \cdot Fin$$

Since **M** must be an integer value, it may be necessary to change **N** values for each data rate to obtain the required output frequency. For example (for 3x reference clock), at 26 Mbit/s the required reference frequency is 78 MHz and using a value of **N** = 47, yields an **M** value of 186. At 28 Mbit/s using the **N** value of 49 would require an **M** value of 209 to produce an output frequency of 84MHz. **M** and **N** values for some sample data rates are provided in the table that follows. Note: the values for Fout are approximate.

TABLE 4: M and N Register Programming Example

DR (Mbit/s)	Fout	M	N
26 Mb/s	78 MHz	186	47
28 Mb/s	84 MHz	192	45
30 Mb/s	90 MHz	206	45
32 Mb/s	96 MHz	220	45

APPLICATIONS INFORMATION (continued)

REFERENCE FREQUENCY OUTPUT (32D4662) (continued):

The **N** register is at address "1110" for the MSBs and address "1111" for the LSBs. The table that follows gives the required register programming information for the values of **N**.

TABLE 5: Frequency Programming Information, N Register

ADDRESS BITS				DATA BITS				FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
1	1	1	0	X	0	1	0	N Register MSBs for N = 47
1	1	1	1	1	1	1	1	N Register LSBs for N = 47

The **M** register is at address "1100" for the MSBs and at address "1101" for the LSBs. The table that follows gives the required register programming information for the values of **M** based on the equation given above for Fout.

TABLE 6: Frequency Programming Information, M Register

ADDRESS BITS				DATA BITS				FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
1	1	0	0	1	0	1	1	M Register = 186,
1	1	0	1	1	0	1	0	Fout = 78 MHz
1	1	0	0	1	1	0	0	M Register = 192,
1	1	0	1	0	0	0	0	Fout = 84 MHz
1	1	0	0	1	1	0	0	M Register = 206,
1	1	0	1	1	1	1	0	Fout = 90 MHz
1	1	0	0	1	1	0	1	M Register = 220,
1	1	0	1	1	1	0	0	Fout = 96 MHz

LOOP FILTER FOR THE 32D4661/32D4662:

The 32D4661/4662 requires a loop filter to control the PLL locking characteristics. While there are several types of filters that can be used to perform this function, a simple integrating filter has proven to be very effective (see Figure 4). To select the components for the loop filter, two considerations should be made. First, the acquisition time of the loop must be less than the minimum track-to-track seek time and second, the capacitor C1 should be low leakage (C1 < 1.0 μF). The acquisition time of the loop is set-up to accommodate a zero phase restart and allow for 1% maximum phase error after phase acquisition. This yields a settling time of: $t_s = 5/\omega_n$.

32D4661:

KVCO = (0.21)(2π)(F_{out}) rad/s V (typ.), at 72MHz KVCO = 9.5×10^7

KD = (4.14 E-3)/RR A/rad @ RR = 4.75KΩ, KD = 8.76×10^{-7}

For a second order system,

R1 = (2 x ζ x ω_n)/(KVCO x KD) where ζ is the damping factor.

C1 = (KVCO x KD)/(ω_n^2) and C1/10 > C2 > C1/20

A damping factor of 0.7 to 1.0 is suggested to prevent locking to harmonics while maintaining an acceptable lock time. At the maximum frequency selected, the damping factor of 1.0 should be considered thereby allowing the damping factor to drop as the frequency drops.

If we start with ω_n = 2 x 10^4, C1 can be calculated as 0.21 µF and C2 can be calculated as 0.01 to 0.02 µF. As mentioned above, the damping factor at the maximum frequency of 72 MHz should be 1.0, so R1 is calculated as:

R1 = (2 x 1.0 x 2E4)/(9.5E7 x 8.76E-7) = 480 ohms

These values will produce a loop settling time t_s of 5/2 x 10^4 = 250 µsecs.

The values calculated here are sample values that have been used in the lab and should be considered starting values. The values of R1, C1, and C2 can be further optimized to meet specific needs.

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32D4662:

KVCO = (0.21)(2π)(F_{out}) rad/s V (typ.), at 100MHz KVCO = 13.2 x 10^7

KD = (4.14 E-3)/RR A/rad @ RR = 4.75KΩ, KD = 8.76 x 10^{-7}

For a second order system,

R1 = (2 x ζ x ω_n)/(KVCO x KD) where ζ is the damping factor.

C1 = (KVCO x KD)/(ω_n^2) and C1/10 > C2 > C1/20

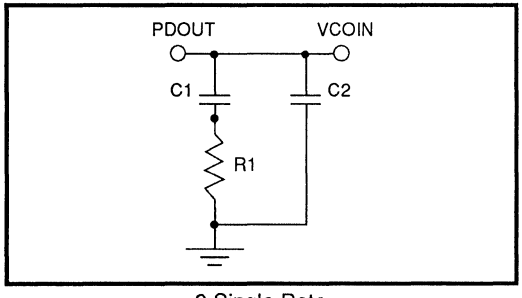
A damping factor of 0.7 to 1.0 is suggested to prevent locking to harmonics while maintaining an acceptable lock time. At the maximum frequency selected, the damping factor of 1.0 should be considered thereby allowing the damping factor to drop as the frequency drops.

If we start with ω_n = 2 x 10^4, C1 can be calculated as 0.21 µF and C2 can be calculated as 0.01 to 0.02 µF. As mentioned above, the damping factor at the maximum frequency of 100 MHz should be 1.0, so R1 is calculated as:

R1 = (2 x 1.0 x 2E4)/(13.2E7 x 8.76E-7) = 354 ohms

These values will produce a loop settling time t_s of 5/2 x 10^4 = 250 µsecs.

The values calculated here are sample values that have been used in the lab and should be considered starting values. The values of R1, C1, and C2 can be further optimized to meet specific needs.



2 Single Rate

FIGURE 4: Integrating Filter for the Phase Locked Loop

NOTE: For further information on the loop filter, consult the Data Synchronizer Family Application Notes in Section 4 of the Silicon Systems Storage Products data book.

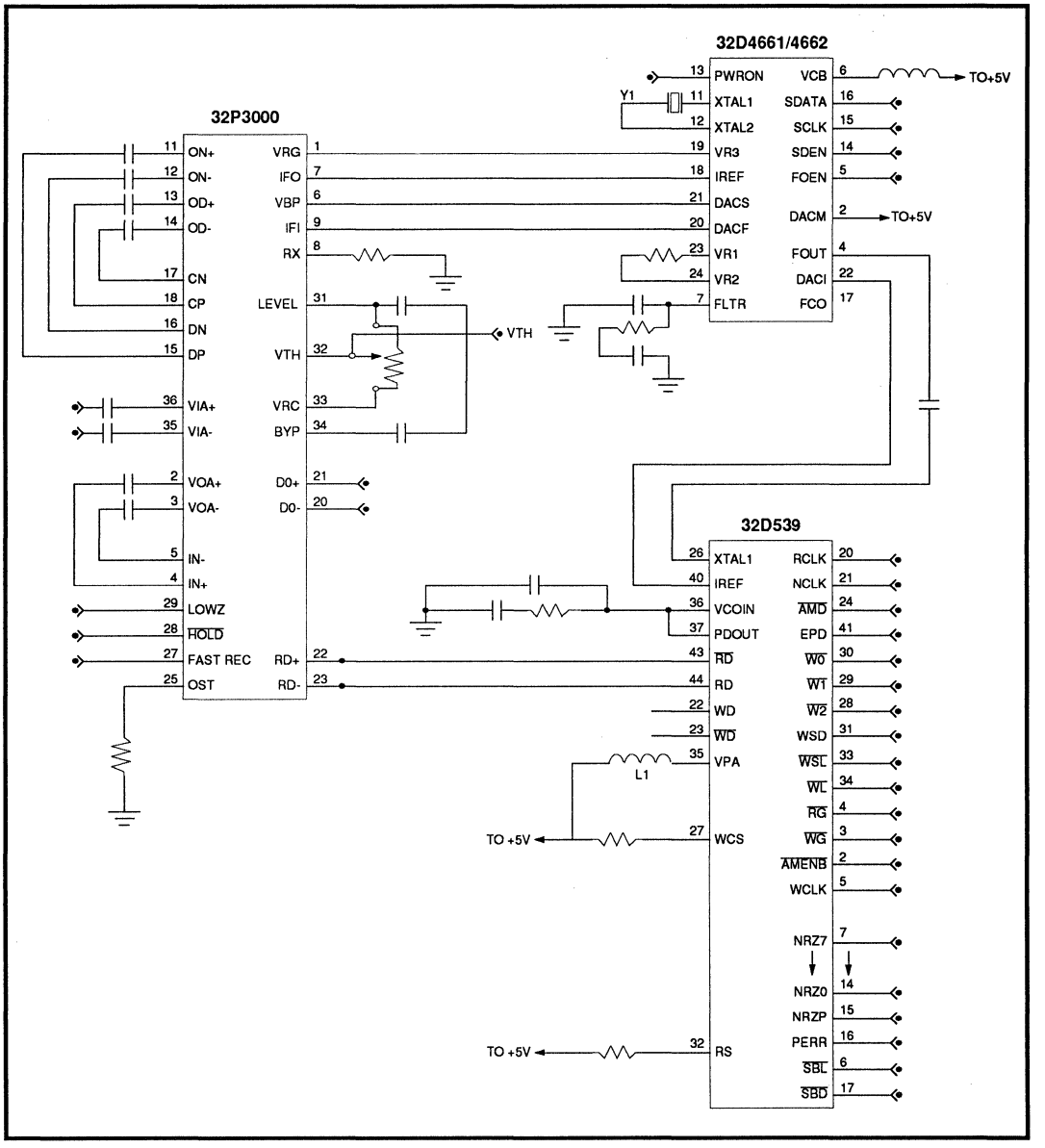
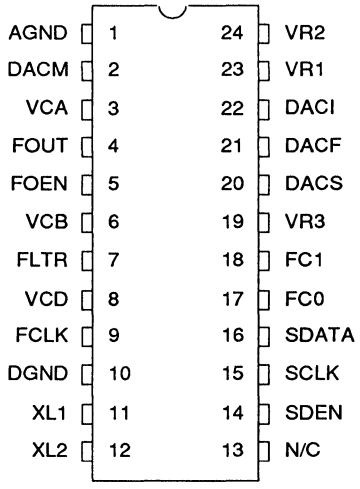


FIGURE 5: Typical 32D4661/4662 Application

PIN DIAGRAM
(Top View)



24 Pin SOL/SSOP

ORDERING INFORMATION

PART DESCRIPTION	ORDERING NUMBER	PACKAGE MARK
SI 32D4661 Time Base Generator		
24-Pin SOL	32D4661-CL	32D4661-CL
24-Pin SSOP	32D4661-CMS	32D4661-CMS
SI 32D4662 Time Base Generator		
24-Pin SOL	32D4662-CL	32D4662-CL
24-Pin SSOP	32D4662-CMS	32D4662-CMS

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 731-7110, FAX (714) 573-6914

Notes:

silicon systems®
A TDK Group Company

SSI 32D4665
Time Base Generator

Advance Information

December 1991

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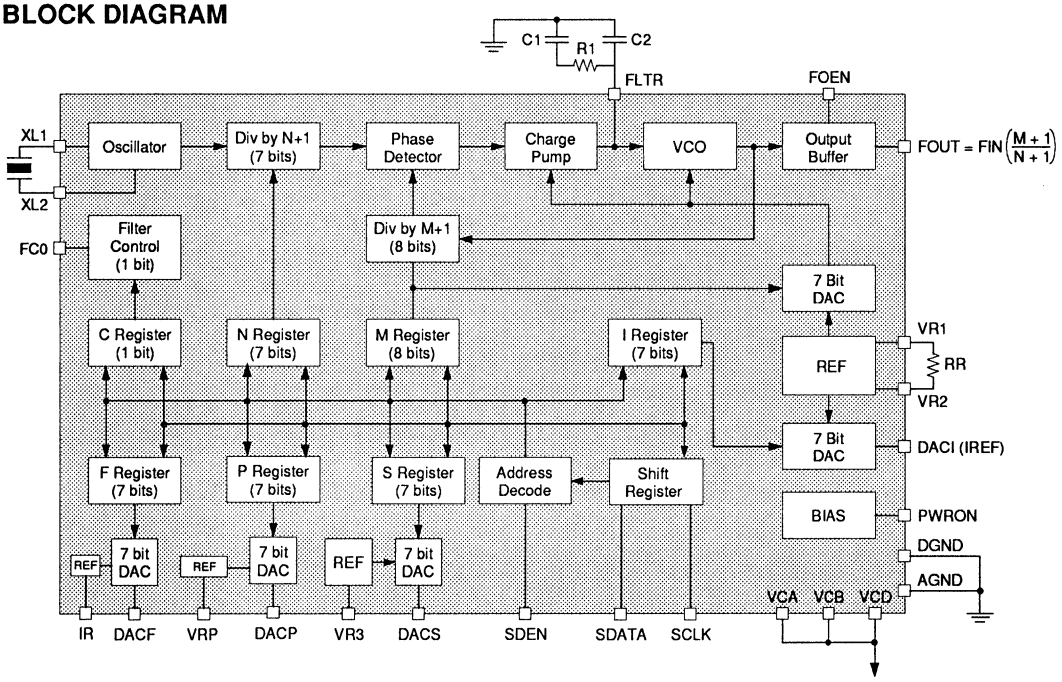
DESCRIPTION

The SSI 32D4665 Time Base Generator provides a programmable reference generator, channel filter control and data rate control for constant density recording applications. It is optimized to operate with the 32D53xx series data separators and contains a high performance programmable PLL for 1% reference frequency control. A 7–bit DAC is provided to program the IREF current which sets the data separator PLL operating center frequency. A 7–bit DAC is provided to program the hysteresis level in the SSI 32P3000 series pulse detectors. Two additional 7–bit DACs are provided for programmable electronic filter (slimmer) control. A single latched TTL output is provided to control filter multiplexers. A serial microprocessor interface reduces pin count and provides convenient access to the internal program storage registers. The 32D4665 only requires a +5V supply and will be available in 24-pin SO packages.

FEATURES

- **For constant density recording applications**
- **Reference frequency control**
- **Channel filter control**
- **Internal DAC available to program data separator data rate**
- **Internal DAC available to program pulse detector hysteresis (DACP)**
- **Up to 75 MHz operation**
- **1% frequency resolution**
- **No external active components required**
- **+5V only operation**
- **Low power mode**
- **24-pin SOL package**

BLOCK DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

PIN DESCRIPTION

INPUT PINS

NAME	DESCRIPTION
SDATA	Serial Data. Data input for an 8-bit control shift register. The data packet is transmitted MSB (D7) first. The first four bits are the register address and the last four are its data bits. Registers larger than 4-bits must be loaded with two 8-bit data packets. These packets should be loaded sequentially in less than 10 µs since the loading operation will cause output transients. With proper loop filter design, the output transients will recover within 1 ms. The data packet fields are given in Table 1.
SCLK	Serial Data Clock. Negative edge triggered clock input for the serial data.
SDEN	Serial Data Enable. A high level input enables data loading. The data is latched when the input is low.
PWRON	Power On. A high level input enables the chip. A low level puts the chip in a low power idle state.
FOEN	Frequency Output Enable. A high level input enables the FOUT output. A low level disables the output and minimizes the driven data separator jitter.

OUTPUT PINS

FOUT	Frequency Output. An ECL output with internal current source. The low voltage swing which minimizes data separator jitter must be AC coupled to the data separator XTL1 input. FOUT = [(M +1)/(N +1)]FIN where M = M Register number and N must be set to approximately [(FIN) (256) / 72 MHz] - 1.
DACI	DAC Output. 7-bit DAC current source output used to program timing current for the data separator VCO center frequency. The current magnitude is controlled by the I Register and is compensated to minimize the sensitivity to power supply and temperature variations.
DACP	DAC Output. 7-bit DAC voltage output used to program hysterysis levels to the pulse detector. The output voltage is set by tyhe difference between the VRP input voltage and the value of (Vcc - VR3). The voltage at the output is: (Vcc - VR3) + (2.0 • P/127) • (VRP - (Vcc - VR3).
DACF	DAC Output. 7-bit DAC current source output used for electronic filter control. The output current is set by the F Register number and the current entering the IR pin. This can be generated by an external resistor (Rx) between VR3 and IR or an external current source.
DACS	DAC Output. 7-bit DAC voltage output used for electronic filter control. The output voltage is set by the voltage at VR3 and the S Register number.
FC0	Filter Control 1. TTL output used to control an external filter multiplexer. C0 = H sets FC0 = H.

ANALOG PINS

XTL1, XTL2	Crystal Oscillator Connections. The circuit is designed to be used with an 8 MHz to 20 MHz crystal. If a crystal is not desired, XTL1 may be driven by a TTL source with XTL2 left open.
VR1, VR2	Current Setting Resistor Connections. An external resistor RR connected between VR1 and VR2 sets the voltage controlled oscillator center frequency and the DACI currents.
VR3	Reference Voltage Input. An external 2.2V supply sets the reference for the DACS voltage.
FLTR	PLL Loop Filter Connection. Connection for loop filter components R1, C1 and C2.
DGND, AGND	Digital and Analog Ground
VCA, VCB	Analog +5V Supplies
VCD	Digital +5V Supply
IR	Reference Current Input. An external resistor Rx, connected from IR to VR3 reference voltage or an external current source sets the reference current for the DACF current.
VRP	Reference Voltage Input. The output level for DACP is set by the difference between (Vcc - VR3) and VRP.

TABLE 1: Data Packet Fields

ADDRESS BITS				USAGE	DATA BITS			
D7	D6	D5	D4		D3	D2	D1	D0
0	1	0	0	P REGISTER	X	P6	P5	P4
0	1	0	1	P REGISTER	P3	P2	P1	P0
0	1	1	0	I REGISTER	X	I6	I5	I4
0	1	1	1	I REGISTER	I3	I2	I1	I0
1	0	0	0	S REGISTER	X	S6	S5	S4
1	0	0	1	S REGISTER	S3	S2	S1	S0
1	0	1	0	F, C REGISTER	C0	F6	F5	F4
1	0	1	1	F REGISTER	F3	F2	F1	F0
1	1	0	0	M REGISTER	M7	M6	M5	M4
1	1	0	1	M REGISTER	M3	M2	M1	M0
1	1	1	0	N REGISTER	X	N6	N5	N4
1	1	1	1	N REGISTER	N1	N2	N1	N0

X = Don't care bit.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

PARAMETER	RATING	UNITS
Storage Temperature	–65 to +150	°C
Junction Operating Temperature, Tj	+150	°C
Supply Voltage, VCA, VCB, VCD	–0.5 to 7	V
Voltage Applied to Logic Inputs	–0.5 to 5.5	V
Maximum Power Dissipation	540	mW

RECOMMENDED OPERATING CONDITIONS

PARAMETER	RATING	UNITS
Supply voltage, VCA = VCB = VCD	4.65 to 5.25	V
Junction Temperature, Tj	0<Tj<135	°C
Ambient Temperature, Ta	0<Ta<70	°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified: recommended operating conditions apply.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VIH	High Level Input Voltage		2.0			V
VIL	Low Level Input Voltage				0.8	V
IIH	High Level Input Current	VIH = 2.7V			20	µA
IIL	Low Level Input Current	VIL = 0.4V			-1.5	mA
VOH	High Level Output Voltage	IOH = -400 µA	2.4			V
VOL	Low Level Output Voltage	IOL = 2 mA			0.5	V
VOH	FOUT ECL High Level	VCD = 5V, VOH-VCD	-1.02			V
VOL	FOUT ECL Low Level	VCD = 5V, VOL-VCD			-1.45	V
ICC	Power Supply Current	PWRON = 2.0V		77	103	mA
		PWRON = 0.8V		25		mA
IO	FOUT Output Current			±4		mA
VO	FOUT Output Swing		0.6			V

INPUT/OUTPUT CHARACTERISTICS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
FIN	FIN Frequency		8		20	MHz
FO	FOUT Frequency				72	MHz
JFO	FOUT Jitter	TO = 1/FO; FCLK active			±400	ps(pk)
DFO	FOUT Duty Cycle	50% Amplitude FOUT = 72 MHz	42		58	%
M	M Divide Number		80		255	-
N, F	N, F Divide Number		25		127	-
P	P Register Number		10		127	-
I	I Register Number		30		127	-
RR	External Resistor		4.50		5.25	kΩ
TVCO	VCO Center Frequency Period	TO=(6.17 E-10)(RR/M)+2.4 ns VCC = 5V, RR = 4.75 kΩ FLTR = 2.7V FIN = 20 MHZ, M = 100	0.77TO	TVCO	1.23TO	ns
	VCO Frequency Dynamic Range	1V < FLTR < VCC – 0.5V, VCC = 5V, FOUT = 31.5 MHz	±25		±45	%
KVCO	VCO Control Gain	ωi = 2π/TVCO	0.14ωi		0.26ωi	rad/s V
KD	Phase Detector	KD = (4.16 E – 3)/RR		KD		A/rad
IOI	DACI Current	IO = (7.41 E-2)I/RR VCC = 5V, TA = 25°C, RR = 4.75 kΩ	0.95IO –3/4LSB		1.05IO +3/4LSB	A
IOF	DACF Current	IOF = F • 4/128 • IR VCC = 5V, Rx = 2.74 kΩ Where IR = VR3/(4 • R) or an external current source	0.97IOF –3/4LSB		1.03IOF +3/4LSB	V
VOP	DACP Voltage	VOP = 2.0 • P • (VRP-(Vcc-VR3))/128 VCC = 5V, VR3 = 2.2V, VRP = 3.6V	0.97VOP +(Vcc-VR3) -3/4LSB -25mV		1.04VOP +(Vcc-VR3) +3/4LSB +25mV	A
VOS	DACS Voltage	VOS = S • VR3/128 VCC = 5V	0.97VOS –3/4LSB +15 mV		1.03VOS +3/4LSB +60 mV	V
VR3	DAC Reference		2.0		2.4	V
IVR3	VR3 Input Current	VR3 = 2.2V			1.0	mA

INPUT/OUTPUT CHARACTERISTICS (Continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Rx			2.5		3.0	kΩ
VRP	DAC P Reference		(Vcc-VR3) +0.2		Vcc-1.0	V
IVRP	VRP Input Current	2.0V ≤ VRP ≤ Vcc			20	µA
I	DAC Current Tolerance	RR = 4.75 kΩ 0°C < Ta < 70°C 4.75V < Vcc < 5.25V	.81 IO		1.17 IO	A
I, F, P, S	Differential Linearity (Monotonicity)	0°C < Ta < 70°C 4.75V < Vcc < 5.25V	-1LSB			-
VODL	DACI, DACF Output Voltage				2	V
VOSL	DACS Output Voltage		0.1		2.4	V
VOPL	DACP Output Voltage		Vcc-VR3		Vcc-0.9	V
ROUT	DACF, DACS Output Resistance				3.7	kΩ
SCLK	Data Clock Period, TC		100			ns
TDD	Data Set Up/Hold Time		25			ns
TDE	Data Enable Delay Time	Delay from data clock rising edge	-TC		TC/4	ns
ROUTP	DACP Output Resistance		50		200	Ω

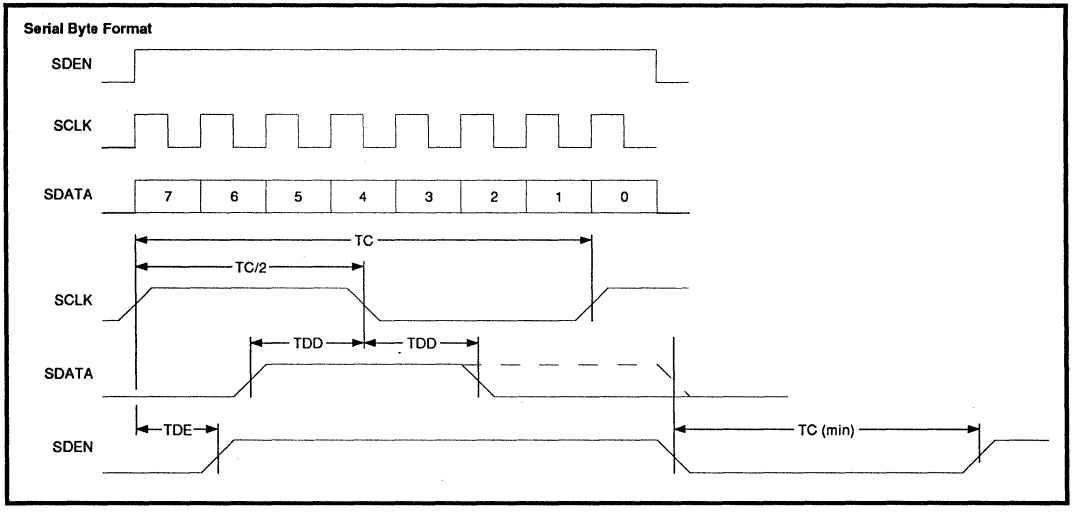


FIGURE 1: Serial Port Timing

APPLICATIONS INFORMATION

REFERENCE FREQUENCY OUTPUT:

The 32D4665 provides the reference frequency for the phase-locked loop (PLL) of a data separator. The required frequency is programmed using the **M** and **N** registers of the 4661. The value of the **N** register is determined by the oscillator that drives the 32D4665 according to the following equation:

$$N=\frac{(Fin \cdot 256)}{(72\ MHz)}-1$$

For this application, using a 12 MHz oscillator (Fin) would yield an **N** value of 41.7. Although the value of **N** should be fixed according to the equation shown above, there is a tolerance of ± 1 integer so **N** can be set from 41 to 43. (This is necessary as the phase detector frequency is fixed by Fin & **N**) Substituting **N** into the following equation and knowing the reference frequency required for each data rate allows for the determination of the **M** register value:

$$Fout=\frac{(M+1)}{(N+1)} \cdot Fin$$

Since **M** must be an integer value, it may be necessary to change **N** values for each data rate to obtain the required output frequency. For example (for 1.5x reference clock), at 24 Mbit/s the required reference frequency is 36 MHz and using a value of **N** = 41, yields an **M** value of 125. At 30 Mbit/s using the **N** value of 41 would require an **M** value of 156.5 to produce an output frequency of 45 MHz. Using **M** = 156 would give an output frequency of 44.86 MHz while using an **M** value of 157 the output frequency would be 45.14 MHz. If **N** is changed to 43 then a value of 146 for **M** would produce the required output frequency of 45 MHz. The required **M** and **N** values for some sample data rates are provided in the table that follows.

TABLE 2: M and N Register Programming Example

DR (Mbit/s)	Fout	M	N
24 Mbit/s	36 MHz	125	41
30 Mbit/s	45 MHz	164	43
36 Mbit/s	54 MHz	188	41
40 Mbit/s	60 MHz	209	41

The **N** register is at address "1110" for the MSBs and address "1111" for the LSBs. The table that follows gives the required register programming information for the values of **N**.

TABLE 3: Frequency Programming Information, N Register

ADDRESS BITS				DATA BITS				FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
1	1	1	0	X	0	1	0	N Register MSBs for N = 41
1	1	1	1	1	0	0	1	N Register LSBs for N = 41
1	1	1	0	X	0	1	0	N Register MSBs for N = 43
1	1	1	1	1	0	1	1	N Register LSBs for N = 43

The **M** register is at address "1100" for the MSBs and at address "1101" for the LSBs. The table that follows gives the required register programming information for the values of **M** based on the equation given above for Fout.

APPLICATIONS INFORMATION (continued)

TABLE 4: Frequency Programming Information, M Register

ADDRESS BITS				DATA BITS				FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
1	1	0	0	0	1	1	1	M Register = 125,
1	1	0	1	1	1	0	1	Fout = 36 MHz
1	1	0	0	1	0	1	0	M Register = 164,
1	1	0	1	0	1	0	0	Fout = 45 MHz
1	1	0	0	1	0	1	1	M Register = 188,
1	1	0	1	1	1	0	0	Fout = 54 MHz
1	1	0	0	1	1	0	1	M Register = 209,
1	1	0	1	0	0	0	1	Fout = 60 MHz

Loop Filter for the SSI 32D4665

The SSI 32D4665 requires a loop filter to control the PLL locking characteristics. While there are several types of filters that can be used to perform this function, a simple integrating filter has proven to be very effective (see Figure 2). To select the components for the loop filter, two considerations should be made. First, the acquisition time of the loop must be less than the minimum track-to-track seek time and second, the capacitor C1 should be low leakage (C1 < 1.0 µF). The acquisition time of the loop is set-up to accommodate a zero phase restart and allow for 1% maximum phase error after phase acquisition. This yields a settling time of: $t_s = 5/\omega_n$.

From the data sheet,

KVCO = $(0.21)(2\pi)(F_{out})$ rad/s V (typ.), at 72 MHz $\underline{KVCO = 9.5 \times 10^7}$

KD = (4.14 E-3)/RR A/rad @ RR = 4.75 kΩ, $\underline{KD = 8.76 \times 10^{-7}}$

For a second order system,

R1 = $(2 \times \zeta \times \omega_n)/(KVCO \times KD)$ where ζ is the damping factor.

C1 = $(KVCO \times KD)/(\omega_n^2)$ and C1/10 > C2 > C1/20

A damping factor of 0.7 to 1.0 is suggested to prevent locking to harmonics while maintaining an acceptable lock time. At the maximum frequency selected, the damping factor of 1.0 should be considered thereby allowing the damping factor to drop as the frequency drops.

If we start with $\omega_n = 2 \times 10^4$, C1 can be calculated as 0.21 µF and C2 can be calculated as 0.01 to 0.02 µF. As mentioned above, the damping factor at the maximum frequency of 72 MHz should be 1.0, so R1 is calculated as:

R1 = (2 x 1.0 x 2E4)/(9.5E7 x 8.76E-7) = 480 Ω

These values will produce a loop settling time t_s of $5/2 \times 10^4$ = 250 µsecs.

The values calculated here are sample values that have been used in the lab and should be considered starting values. The values of R1, C1, and C2 can be further optimized to meet specific needs.

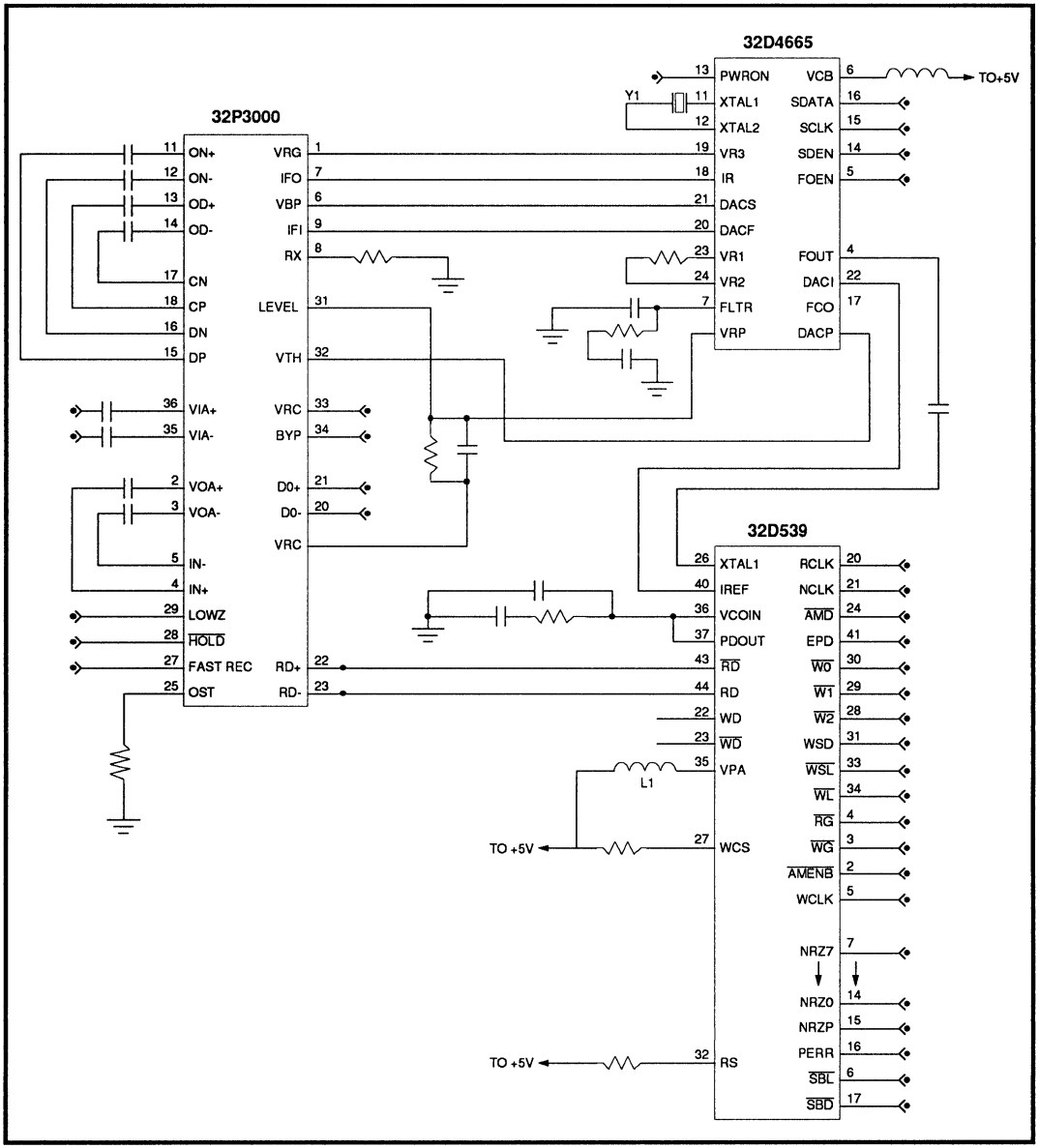
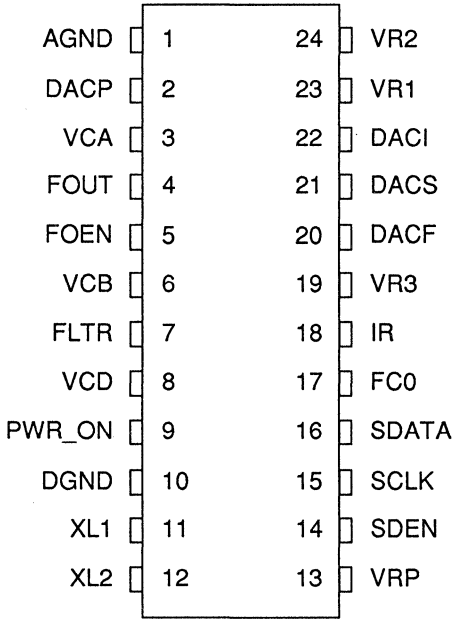


FIGURE 2: Typical 32D4665 Application

PACKAGE PIN DESIGNATIONS
(Top View)



24 Pin SOL

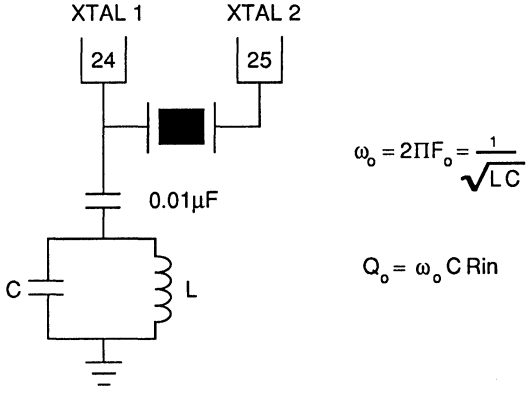
Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 731-7110, FAX (714) 573-6914

December 1991

REFERENCE OSCILLATOR

An internal reference oscillator generates the standby reference for the PLL. A series resonant crystal should be used between XTAL1 and XTAL2. If a crystal oscillator is not desired, then an external AC coupled ECL source may be applied to XTAL1, leaving XTAL2 open. A TTL compatible reference may also be used if suitably attenuated.

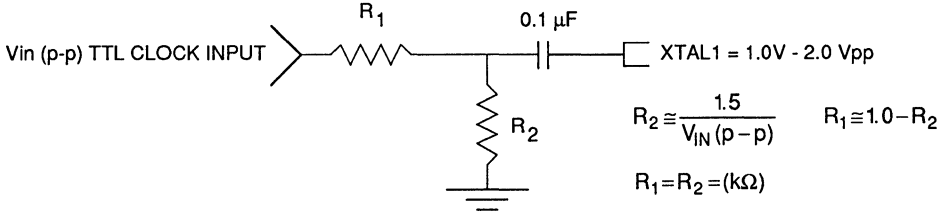
If it is desired to operate a crystal at a non-fundamental or harmonic frequency, then the following network is suggested:



The typical input impedance looking into XTAL1 is approximately Rin = 250Ω. It is recommended to design the value of Q_o at approximately 10 to 15. Therefore, a resonant frequency of F_o = 20 MHz would result in L ≅ 0.16 μH and C ≅ 380 pF.

ATTENUATOR CIRCUIT

If a crystal oscillator is not desired, then an external TTL Compatible reference may be applied to XTAL1 leaving XTAL2 open. It is required, however that the TTL signal be attenuated then A.C. coupled into XTAL1 using the following network:



The signal amplitude into XTAL1 should be attenuated to approximately 1.0 to 2.0 Vp-p; this will insure that the transients associated with TTL switching characteristics won't couple into the data synchronizer and degrade performance.

LOOP FILTER

The performance of the data synchronizer is directly related to the selection of the loop filter. The loop filter characteristics should be optimized for:

(A) Fast Acquisition

The ability of the loop to quickly obtain lock when the input signal to the Phase Detector is switched between the reference oscillator (crystal) and the Read Data ($\overline{RD}$). Fast acquisition implies a large loop bandwidth so that it can quickly respond to changes at the input.

(B) Data Margin

The ability of the loop to ignore bit shifts (jitter) and maintain a well centered window about the data pulse train. In general, it is not desirable to allow the loop to respond to a single shifted bit as this would cause the subsequent bit to be poorly centered within its window and possibly cause an error. This requirement implies a small loop bandwidth reducing the sensitivity to high frequency jitter.

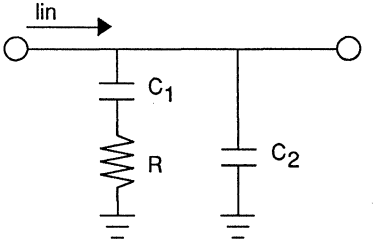
(C) Data Tracking

The ability to respond to instantaneous changes in phase and frequency of the data. This can be a result of such phenomena as disk rotational speed variations which cause changes in the characteristics of the incoming data stream. In general, this requirement is consistent with that of fast acquisition, however, this depends upon the application.

Although the loop performance characteristics place conflicting requirements on the loop bandwidth, the architecture of the Silicon Systems data synchbronizer family significantly simplifies the design by minimizing the "step in phase" and "step in frequency" encountered when switching the Phase Detector input reference signal. A zero phase restart technique is employed to minimize the initial phase error while the standby reference oscillator keeps the VCO at the center frequency during non-read modes.

One approach in determining the initial loop filter selection is to consider the requirements imposed during acquisition. This includes both acquiring lock to the crystal reference in non-read modes, as well as locking to the preamble field prior to decoding data. The format of the sector will dictate which of these two criteria imposes the tightest restriction on acquisition.

The requirements for acquiring lock to the crystal oscillator are application specific and usually depend upon the length of the Write Splice gap. Therefore, the design approach employed in this analysis will be based upon the requirements during acquisition to the preamble field. The length (in time) of the preamble field is set by the data synchronizer's locking sequence. Knowing this length in time, and that our initial phase error is less than 0.5 radians, we can determine an acceptable loop bandwidth (ωn) and damping factor (ζ).
One possible loop filter configuration is as follows:



The role of C1 is as an integrating element. The larger this capacitance, the longer the acquisition time; the smaller the capacitance, the greater the ability to track high frequency jitter. The resistor R reduces the phase shift induced by C1. The capacitor C2 will suppress high frequency transients and will have minimal effect on the loop response if it is small relative to C1 (typically C2 = C1/10)

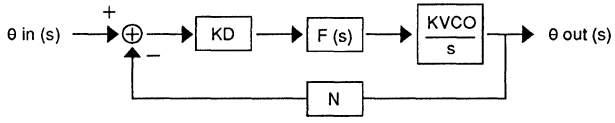
The loop filter transfer function is:

$$F(s) = \frac{Vout}{Iin} = \frac{1 + sRC_1}{sC_1\left(1 + sC_2R + C_2/C_1\right)}$$

If C2 << C1, then:

$$F(s) = \frac{Vout}{Iin} = \frac{1 + sRC_1}{sC_1}$$

The overall block diagram for the phaselock loop can be described as:



Where:

KD = Phase Detector gain [A/rad]

F(s) = Loop filter impedance [V/A]

KVCO/s = VCO control gain [rad/s V]

N = The ratio of the reference input frequency to the VCO output frequency

The closed loop transfer function is:

$$T(s) = \frac{\theta out(s)}{\theta in(s)} = \frac{G(s)}{1 + GH(s)} = \frac{KD \cdot KVCO[(1 + sRC_1)/C_1]}{s^2 + s[N \cdot KD \cdot KVCO \cdot R] + \frac{N \cdot KD \cdot KVCO}{C_1}}$$

by putting the characteristic equation (denominator) in the form of:

$$s^2 + 2s\zeta\omega n + \omega n^2$$

we can solve for ωn and ζ to get:

$$\omega n^2 = \frac{N \cdot KD \cdot KVCO}{C1} \qquad \zeta = \frac{N \cdot KD \cdot KVCO \cdot R}{2\omega n}$$

Now we can solve for R, C1 and C2:

$$C1 = \frac{N \cdot KD \cdot KVCO}{\omega n^2} \qquad R = \frac{2\zeta\omega n}{N \cdot KD \cdot KVCO} \qquad C_2 = \frac{C_1}{10}$$

where: ωn = loop bandwidth and, ζ = loop damping factor

Because of the nature of Run Length Limited (RLL) codes, the Phase Detector will only be enabled during a data pulse. This technique allows the VCO to run at a center frequency with period, TVCO, equal to one encoded data bit cell time.

Figure 1 represents the relationship between the VCO output when locked to various Phase Detector input signals.

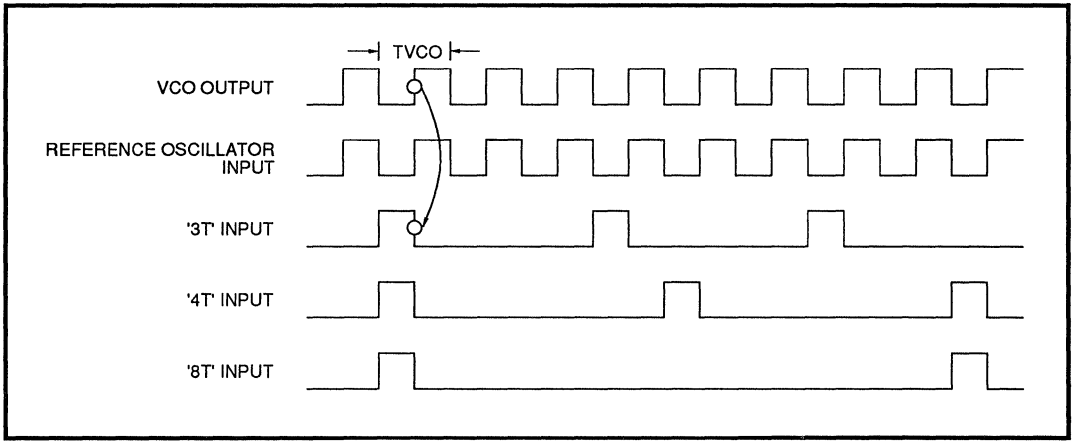


FIGURE 1: Relationship of VCO Output to Phase Detector Input

The average amplitude of the Phase Detector gain depends upon the Phase Detector input signal. When the PLL is locked to the reference oscillator, the Phase Detector is continuously enabled and the gain is at its maximum. When the PLL is tracking data and the input is an "8T" pattern, then the Phase Detector gain is at its minimum. The following indicates the value of "N" for various input conditions:

N = 1.0 for θin = reference oscillator
N = 0.33 for θin = 3T (100) preamble field
N = 0.25 for θin = 4T (1000)
N = 0.125 for θin = 8T

Throughout this analysis the PLL has been considered as a continuous time system. In actuality the characteristics of the Phase Detector result in a sampled data system. By utilizing an integrating loop filter to average and smooth the Phase Detector charge pump output pulses, this analogy should be reasonable.

Determining an acceptable amount of phase error after locking to the preamble field depends upon the system requirements. In addition, it may be necessary to consider the effects of frequency steps in applications where motor speed control tolerances are significant. Generally, an acceptable amount of error is defined to be that amount which when added to all other timing error contributors, results in the data being within its timing window by the required margin.

In general, it is desirable to have the loop damping factor "ζ" between 0.5 and 1.0 during acquisition. For a high gain, second-order loop this results in minimal noise bandwidth.

Figure 2 represents the phase error's response in time to a transient step in phase as a function of the loop bandwidth and damping factor. Figure 3 indicates the response of the VCO control voltage to compensate for this step in phase.

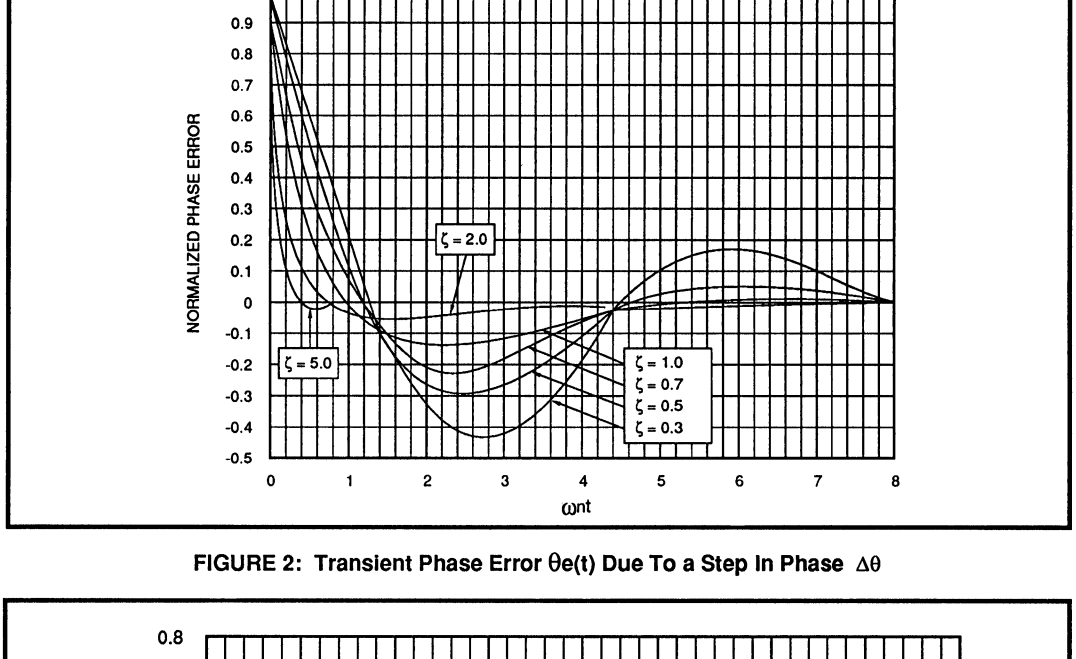


FIGURE 2: Transient Phase Error θe(t) Due To a Step In Phase Δθ

FIGURE 3: Transient Phase Error θe(t) Due to a Step In Frequency Δω

Data Synchronizer Family Application Notes

DATA RECOVERY APPLICATIONS

DETERMINING LOOP FILTER COMPONENTS

What follows is a method to calculate loop filter components based on the acceptable phase error when the VCO switches from the reference frequency to read data.

To determine the maximum time the VCO has to lock from the reference frequency to read data, the equation is:
Tmax = Ln • 'xT'/(DR•M)

DR is the data rate and Tmax is the amount of time the Phase Lock Loop (PLL) has to settle to within an acceptable amount of error before tracking and decoding data. Ln, 'xT' and M are variables that are device dependent and are defined tin Table 'A'. It is important to note it follows from the above equation that the locking time from the reference frequency (crystal oscillator) to read data is fixed and is not dependent on the length of the preamble field. Although, any additional preamble field will allow more time for the PLL to settle out before starting to decode data.

Table A

DEVICE	MODE	PREAMBLE ('xT')	Ln	M
5321	HS	4	32	2.0
5321	SS	3	38	2.0
5322	HS	4	32	2.0
5322	SS	3	38	2.0
535X	HS	4	32	2.0
535X	SS	3	38	2.0
5362A	--	3	16	1.5
537X	--	3	16	1.5
539X	--	3	16	1.5

DEVICE: An 'X' implies a family of devices, for instance 537X includes the 5371, 5372, 5373 and 5374

MODE: This is 'SS' for soft sector and 'HS' for hard sector application. '--' implies that there is no difference between hard sector or soft sector applications.

PREAMBLE ('xT'): Depending on the mode, the preamble could be a '3T' (xT = 3) or '4T' (xT = 4).

Ln: This is the number of read data transitions that the device counts within the preamble to allow for VCO lock. The transitions are assumed to be part of a uniform preamble field.

M: This factor times the Data Rate determines the frequency of read data. It is also the code rate. For instance, for the 537X, if the data rate is 20Mbit/s then the read data frequency would be 20 • M = 20 • 1.5 = 30 Mbit/s.

Example;

Assuming a SSI 32D5372 running at a data rate of 20Mbit/s,

tmax = 16 • 3/(20E6 • 1.5) = 1.6 µs

Therefore, the PLL has 1.6 µs to settle within an acceptable amount of error before tracking and decoding data.

To determine the components of the loop filter, the next step is to calculate the typical phase detector gain (Kd) and VCO control gain (KVCO) of the specific data synchronizer device.

In Table B is the typical Kd and KVCO equations of the current data synchronizer family, check the latest product data sheet to ensure that the equations have not changed during the product characterization cycle.

Table B

DEVICE	Kd (μA/rad)	KVCO
5321	309/(RR + 0.53)	0.19 • 2 • π/To
5322	309/(RR + 0.53)	0.17 • 2 • π/To
535	309/(RR + 0.53)	0.17 • 2 • π/To
5351/1A	340/(RR + 0.90)	0.17 • 2 • π/To
5362A	570/(RR + 0.53)	0.20 • 2 • π/(2To)**
5371/2	660/(RR + 0.53)*	0.20 • 2 • π/(2To)**
5373/4	660/(RR + 0.53)*	0.20 • 2 • π/(2To)
539	750/(RR + 0.42)*	0.20 • 2 • π/To

Where: To: is the VCO Center frequency period
RR: is the reference resistor connected to the IR pin
KD: is normalized for a 1F read data pattern

*Note: This device switches the phase detector gain between read and non-read modes to optimize locking between the reference frequency and read data (and back again.) The equation give in the table is for read mode.

**Note: The VCO frequency in this device is divided by two before entering the phase detector. The additional '2' in the denominator normalizes KVCO for the following loop filter equations.

In general, it is desirable to have the loop damping factor "ζ" between 0.5 and 1.0 during acquisition. For a high gain, second-order loop this results in minimal noise bandwidth.

To determine the bandwidth ω_n, one must decide what the acceptable phase error will be when the PLL switches from the reference frequency to read data after the locking time, Tmax, is complete. As shown in figure 2, with $\zeta = 0.7$, choosing $\omega_n T = 2.3$ the phase error will be at most 22% of the initial phase error, 7.5% at $\omega_n T = 4.0$, etc. The bandwidth is then $\omega_n = (\omega_n T)/Tmax$; where Tmax is the settling time of the PLL calculated above.

We now have enough information to calculate the loop filter components:

$C1 = N \cdot Kd \cdot KVCO/(\omega_n)^2$ $\quad R = 2 \cdot "\zeta" \cdot \omega_n/(N \cdot KD \cdot KVCO)$ $C2 = C1/10$

where:

Kd = Phase Detector gain (μA/rad)
KVCO = VCO control gain (rad/s V)
N = The ratio of the reference input frequency to the VCO output frequency.
(For a '3T' preamble
N = 0.33, '4T' preamble N = 0.25)
ω_n = Acceptable loop bandwidth
"ζ" = Acceptable loop damping factor

Example:

SSI 32D5362A running at 15 Mbit/s.

From Table A

xT = 3; Ln = 16; M = 1.5

Tmax = Ln • 'xT'/(DR • M) = 16 • 3/(15E6 • 1.5) = 2.1 μs

For this example, we want the acceptable phase error when the VCO is switched from the reference frequency to read data to be less than 15% of the initial phase error. This results, from figure 2 and "ζ" = 0.7, in a wn(Tmax) between 3 and 4. To simplify the results let ω_n(Tmax) = 3.2. Since the data synchronizer family employs a zero phase restart technique to reduce the initial phase error (a design goal of ± one rad is typical for the family.) The initial phase error has been characterized to be typically 6ns for the SSI 32D5362A. Thus the acceptable phase error will be 0.15 • 6 = 0.9 ns when the VCO is switched.

ω_n(Tmax) = 3.2 ω_n = 3.2/2.1E-6 = 1.5 Mrad/s

RR = 92.6/DR-2.3 = 92.6/15 - 2.3 = 3.87k

From Table B

KD = 570/(RR + 0.53) = 130 μA/rad

KVCO = 0.2 • 2 • π/(2To) = 0.2 • 2 • π/(2 • 22.2E-9) = 28.3 Mrad/sV

C1 = N • KVCO • KD/(ω_n)2 = 0.33 • 28.3 • 130/1.5E62 = 540pF

C2 = 540pF/10 = 54pF

R = 2 • "ζ" • ω_n/(N • KD • KVCO) = 2 • 0.7 • 1.5E6/(0.33 • 130 • 28.3) = 1729

LAYOUT CONSIDERATIONS

As with other high frequency analog devices the SSI 32D5321/22 requires care in layout. The designer should keep analog signal lines as short as possible and well balanced. Use of a ground plane is recommended, along with supply bypassing to separate the SSI 32D5321/22, and associated circuitry, from other circuits on the PCB.

32D5321

DATA RATE (Mbit/s)	DAMPING FACTOR,ζ	LOCK TIME t_{max} (μs)	$\omega_n t$	BANDWIDTH $\omega_n \left(\frac{rad}{sec}\right)$	EXTERNAL COMPONENT VALUES					
					RR(kΩ)	Cd(pF)	Rd(kΩ)	R(kΩ)	C_1 (pF)	C_2 (pF)
7.5	0.7	7.5	5.0	6.67×10^5	4.92	100	11.0	3.1	680	68
10.0	0.7	5.7	5.7	1.0×10^6	3.57	82	10.0	2.7	510	51

32D5322

DATA RATE (Mbit/s)	DAMPING FACTOR,ζ	LOCK TIME t_{max} (μs)	$\omega_n t$	BANDWIDTH $\omega_n \left(\frac{rad}{sec}\right)$	EXTERNAL COMPONENT VALUES					
					RR(kΩ)	Cd(pF)	Rd(kΩ)	R(kΩ)	C_1 (pF)	C_2 (pF)
7.5	0.7	7.5	5.0	6.67×10^5	4.64	100	13.0	2.94	710	71
10.0	0.7	5.7	5.7	1.0×10^6	3.19	100	10.0	2.37	590	59
15.0	0.7	3.8	5.7	1.5×10^6	1.72	100	6.49	1.43	654	65

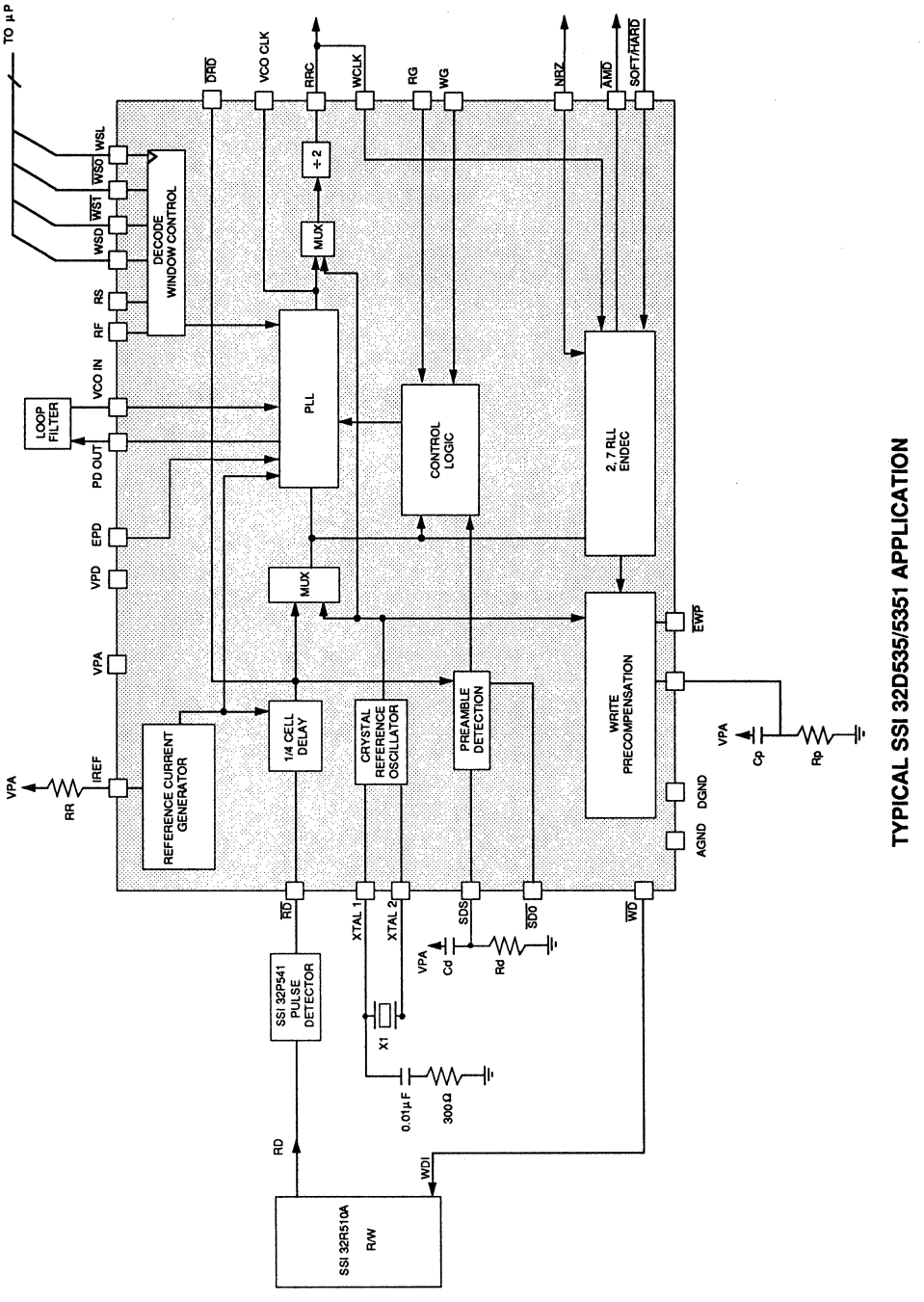
These loop filter configurations and component values should be considered a starting point. The final value of ωn depends upon the system requirements and can certainly be optimized for a specific application. In the table below, we have listed some suggested external component values for several common data rates.

32D535

DATA RATE (Mbit/s)	DAMPING FACTOR,ζ	LOCK TIME t_{max} (μs)	$\omega_n t$	BANDWIDTH $\omega_n \left(\frac{rad}{sec}\right)$	EXTERNAL COMPONENT VALUES					
					RR(kΩ)	Cd(pF)	Rd(kΩ)	R(kΩ)	C_1 (pF)	C_2 (pF)
7.5	0.7	7.5	5.0	6.67×10^5	4.92	100	11.0	3.0	687	69
10.0	0.7	5.7	5.7	1.0×10^6	3.57	82	10.0	2.7	510	51

32D5351

DATA RATE (Mbit/s)	DAMPING FACTOR,ζ	LOCK TIME t_{max} (μs)	$\omega_n t$	BANDWIDTH $\omega_n \left(\frac{rad}{sec}\right)$	EXTERNAL COMPONENT VALUES					
					RR(kΩ)	Cd(pF)	Rd(kΩ)	R(kΩ)	C_1 (pF)	C_2 (pF)
10.0	0.7	5.7	5.7	1.0×10^6	5.85	100	10.0	3.94	356	36
15.0	0.7	3.8	5.7	1.5×10^6	3.32	100	6.49	2.46	379	38



TYPICAL SSI 32D535/5351 APPLICATION

These loop filter configurations and component values should be considered a starting point. The final value of ωn depends on the system requirements and can certainly be optimized for a specific application. In the following table we have listed some suggested external component values for two common data rates:

32D5362A

DATA RATE (Mbit/s)	DAMPING FACTOR, ζ	LOCK TIME tmax (μs)	$\omega_n t$	BANDWIDTH $\omega_n \left(\frac{rad}{sec}\right)$	EXTERNAL COMPONENT VALUES			
					RR(kΩ)	R(Ω)	C_1(pF)	C_2(pF)
10	0.7	3.2	3.2	1.0×10^6	6.96	2957	470	47
15	0.7	2.1	3.2	1.5×10^6	3.87	1729	540	54

4

The following is a list of recommended component values based on the above calculations. It is important to note that these values should be considered a starting point in designing a loop filter for a specific drive application, the optimal bandwidth and requirements for re-locking back to the reference frequency after read mode has been terminated have not been considered.

32D5371/5372

DATA RATE (Mbit/s)	DAMPING FACTOR,ζ	LOCK TIME tmax (μs)	$\omega_n t$	BANDWIDTH $\omega_n \left(\frac{rad}{sec}\right)$	KD $\left(\frac{\mu A}{rad}\right)$	KVCO $\left(\frac{\mu A}{s\text{-}V}\right)$	EXTERNAL COMPONENT VALUES			
							RR(kΩ)	R(kΩ)	C_1 (pF)	C_2 (pF)
10	0.7	3.2	3.2	1.0×10^6	81.18	18.85	7.6	2.8	500	50
17	0.7	1.9	3.2	1.7×10^6	152.4	32.04	3.8	1.5	550	55
24	0.7	1.3	3.2	2.5×10^6	241.8	45.24	2.2	1.0	570	57

32D5373/5374

DATA RATE (Mbit/s)	DAMPING FACTOR,ζ	LOCK TIME tmax (μs)	$\omega_n t$	BANDWIDTH $\omega_n \left(\frac{rad}{sec}\right)$	KD $\left(\frac{\mu A}{rad}\right)$	KVCO $\left(\frac{\mu A}{s\text{-}V}\right)$	EXTERNAL COMPONENT VALUES			
							RR(kΩ)	R(kΩ)	C_1 (pF)	C_2 (pF)
15	0.7	2.1	3.2	1.5×10^6	81.18	28.27	7.6	1.85	330	33
23	0.7	1.4	3.2	2.3×10^6	133.9	43.35	4.4	1.62	360	36
32	0.7	1.0	3.6	3.6×10^6	479.0	60.32	2.6	0.53	735	75

32D539

DATA RATE (Mbit/s)	DAMPING FACTOR,ζ	LOCK TIME tmax (μs)	$\omega_n t$	BANDWIDTH $\omega_n \left(\frac{rad}{sec}\right)$	KD $\left(\frac{\mu A}{rad}\right)$	KVCO $\left(\frac{\mu A}{s\text{-}V}\right)$	EXTERNAL COMPONENT VALUES			
							RR(kΩ)	R(kΩ)	C_1 (pF)	C_2 (pF)
24	0.7	1.30	3.2	2.5×10^6	105.3	45.24	6.7	3.0	250	25
36	0.7	0.89	3.2	3.6×10^6	196.3	67.86	3.4	1.1	340	33
48	0.7	0.67	3.2	4.8×10^6	297.6	90.48	2.1	0.75	385	38

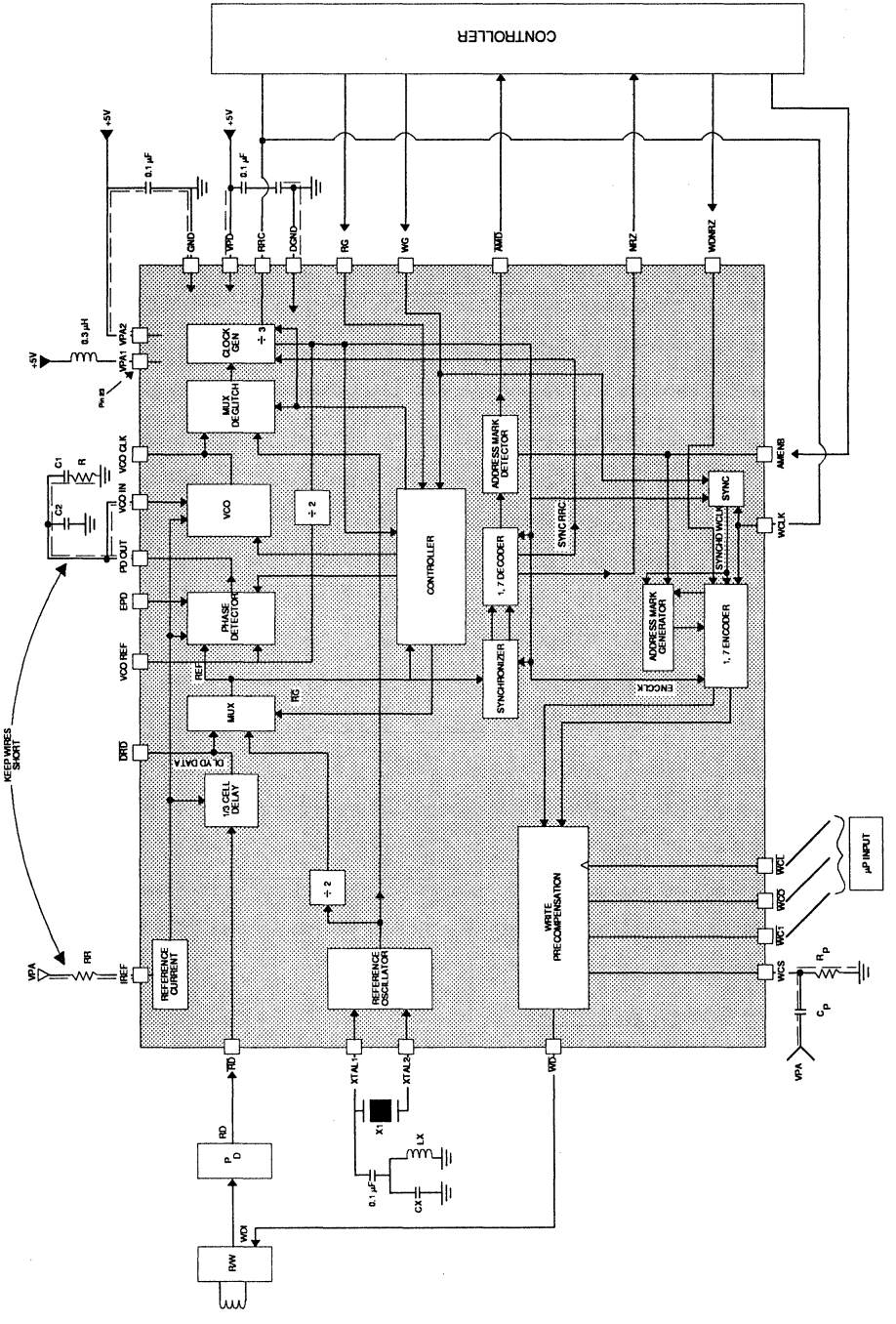


FIGURE 5: Typical Application

LAYOUT CONSIDERATIONS

As with other high frequency devices the data synchronizer family requires care in layout. The designer should keep analog signal lines as short as possible and well balanced. Use of a ground plane is recommended, along with supply bypassing, to separate the data synchronizer device and associated circuitry from other circuits on the PCB. It is also recommended that an inductor (~0.3µH) be placed in series with the analog supply which supports the VCO circuitry on the higher data rate (1,7) RLL products. This is generally VPA1, but check the application diagram in the specific product data sheet for more information. This additional filtering has been shown to be effective in reducing VCO jitter, which can degrade window margin performance.

TEST POINTS

The SSI 32D5362A, 5371/5372/5373/5374, 539 provide three (3) test points which can be utilized to evaluate window margin characteristics.

(a) $\overline{DRD}$, delayed read data – the positive edges represent the data bit position

(b) VCO REF, the VCO reference which represents the input to the Phase Detector, synchronizer, and 1,7 decoder

(c) VCO CLK, the VCO clock output which represents the output of the VCO

The following figure describes the relationship between the various test points:

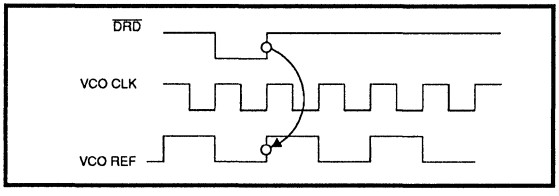


FIGURE 6: Test Point Relationships

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714) 731-7110, FAX: (714) 573-6914

Notes:

Section

READ CHANNEL COMBINATION DEVICES

silicon systems®
A TDK Group Company

SSI 32P548
Pulse Detector & Data Synchronizer

Advance Information

July, 1990

DESCRIPTION

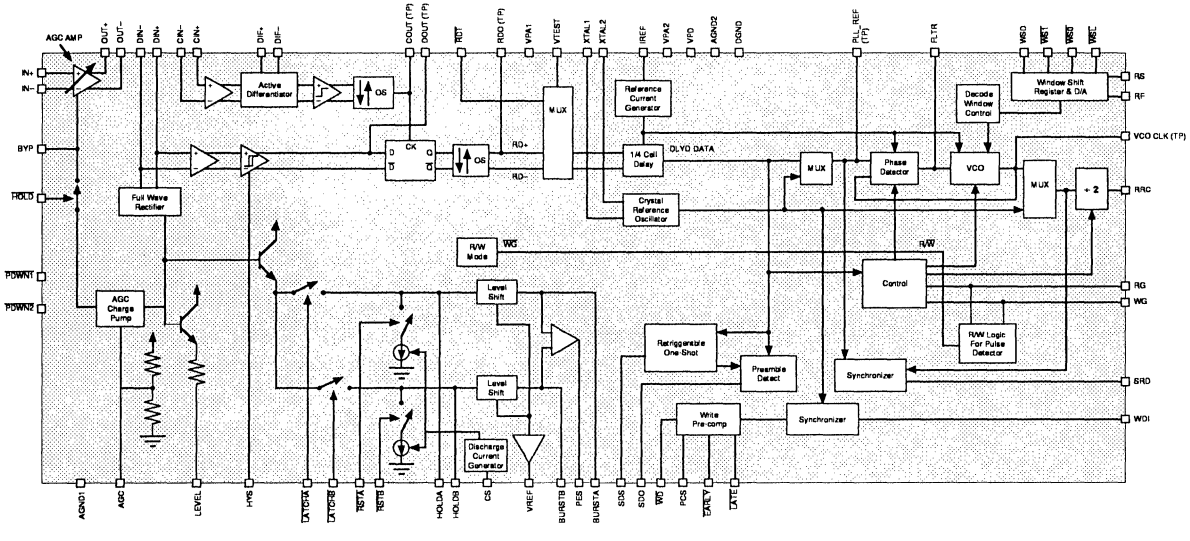
The SSI 32P548 is a low power, high performance Pulse Detection, Data Synchronization combination device. This device is designed for use in low power applications requiring +5V only power supplies. The pulse detection portion of this device detects and validates amplitude peaks in the output from a disk drive read amplifier, as well as detecting embedded servo information to provide position signals used for read head positioning. The data synchronization portion is a 2, 7 data synchronizer with window shift and write pre-compensation capability. The SSI 32P548 achieves low system operating power three ways, with a low operating power (+5V only design) and with two independent power down modes. Mode 1 is a complete shutdown or sleep mode. Mode 2 is a low power mode for use while acquiring servo, where all circuitry not associated with obtaining servo information is powered down. The SSI 32P548 is available in a 52-pin fine pitch QFP, and 68-pin PLCC.

FEATURES

- **Highly Integrated Pulse Detector and Data Synchronizer**
- **+5V only Power Supplies**
- **Low Power <750 mW (max)**
- **Dual Power Down Modes**
- **Dual Servo Burst Channels with Position Error Signal**
- **Low Pulse Pairing (≤ ±1 ns)**
- **5-12 Mbit/s operation**

5

BLOCK DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

CIRCUIT OPERATION

PULSE DETECTOR SECTION

READ MODE

In read mode the SSI 32P548 is used to process either data or servo signals. In the Data Read Mode the input signal is amplified and qualified using an AGC amplifier and pulse level qualification of the detected signal peaks. In the servo read mode the input signal is amplified and rectified. Two servo burst channels are available that provide A and B burst levels.

DATA READ MODE

An amplified head output signal is AC coupled to the IN+ and IN- pins of the AGC amplifier. Gain control is accomplished by full wave rectifying and amplifying the [(DIN+)-(DIN-)] voltage level and comparing it to a reference voltage level at the AGC pin.

The SSI 32P548 contains a dual rate attack charge pump. The value of the attack current is dependent on the instantaneous level at DIN±. For signal levels above 125% of the desired level a fast attack mode is invoked that supplies a 1.3 mA charge current to the network on the BYP pin. Between 125% and 100% of the desired level the circuit enters a slow attack mode and supplies 0.18 mA of charge current to the BYP pin.

Two decay modes are available and are automatically controlled within the device.

Upon a switch to write mode, the device will hold the gain at its previous value. When the device is then switched back to read mode the AGC holds the gain and stays in a low impedance state for 0.9 µs. It then switches into a fast/slow attack mode if the new gain required is less than the previously held gain or a fast decay mode if the gain required is more than its previous value. The fast decay current is 0.12 mA and stays on 0.9 µs. After the 0.9 µs time period the device stays in a steady state slow attack, slow decay mode. The slow decay discharge current is 4.5 µA.

The AGC pin is internally biased so that the target differential voltage input at DIN± is 1.0 Vp-p under nominal conditions. The voltage on this pin can be modified by tying a resistor between AGC and GND or VPA. A resistor to GND decreases the voltage level, while a resistor to VPA increases it. The resulting AGC

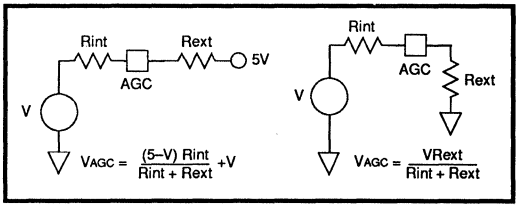


FIGURE 1: AGC Voltage

voltage level is shown in Figure 1; where:

V = Voltage at AGC w/pin open (2.3V, nom)

Rint = AGC pin input impedance (2.5 kΩ, typ)

Rext = External resistor

The new DIN ± input target level is nominally 0.45 Vp-p/ V_{AGC}.

The maximum AGC amplifier output swing is 3.0 Vp-p at OUT±, which allows for up to 6dB loss in any external filter between OUT± and DIN±.

AGC gain is a linear function of the BYP-pin voltage (VBYP) as shown in Figure 2.

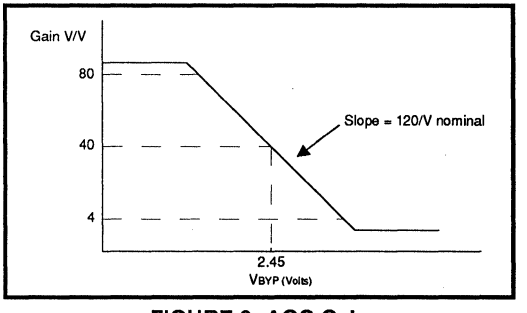


FIGURE 2: AGC Gain

The AGC amplifier has an open collector output and can sink 4.0 mA. For correct operation to the gain range the outputs should be pulled up to VPA through a 340Ω resistor as shown in Figure 3.

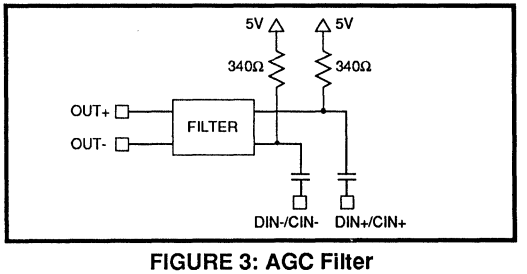


FIGURE 3: AGC Filter

In the 52-pin package configuration CIN+ and DIN+ will be bonded together, likewise CIN- and DIN- will be bonded together. In this situation one filter must be used for both time and amplitude channels. A multipole Bessel filter is typically used for its linear phase or constant group delay characteristics.

In the amplitude channel the signal is sent to a hysteresis comparator. The hysteresis threshold level is set so that it will be tripped only by valid signal pulses and not by baseband noise. It can be fixed level or a fraction of the DIN± voltage level.

The latter approach is accomplished by using an external filter/network between the LEVEL and HYS pins. This allows setting the AGC slow attack and decay times slow enough to minimize time channel distortion and setting a shorter time constant for the hysteresis level. The LEVEL pin output is a rectified and amplified version of DIN±, 1.0 p-p at DIN± results in 1.0 Vo-p nominally, at the LEVEL pin. A voltage divider is used from LEVEL to ground to set the Hysteresis threshold at a percentage of the peak DIN± voltage. For example, if DIN± is 1.0 Vp-p, then using an equal valued resistor divider will result in 0.5 Vpk at the HYS pin. This will result in a nominal ±0.18V threshold or a 36% threshold of a ±0.500V DIN± input. The capacitor is chosen to set an appropriate time constant. This "feed forward" technique speeds up transient recovery by allowing qualification of the input pulses while the AGC is still settling. This helps in the two critical areas of write to read and head change recovery. Some care in the selection of the hysteresis level time constant must be exercised so as to not miss pattern (resolution) induced lower amplitude signals. The output of the hysteresis comparator is the "D" input of a D-type flip-flop. The DOUT pin is a comparator output signal for testing purposes only.

In the time channel the signal is differentiated to transform signal peaks to zero crossings which are detected and used to trigger a bi-directional one-shot. The one-shot output pulses are used as the clock input of the D flip-flop. The COUT pin provides the one-shot output for test purposes.

The differentiator function is accomplished by an external network between the DIF+ and DIF- pins. The transfer function from CIN± to the comparator input (not DIF±) is:

$$Av = \frac{-2000Cs}{LCs^2 + C(R+92)s + 1}$$

where: C, L, R are external passive components
$20\ pF < C < 150\ pF$
$s = j\omega = j2\pi f$

During normal operation, the time channel clocks the D flip-flop on every positive and negative peak of the CIN± input. The D input to the flip-flop only changes state when the DIN± input exceeds the hysteresis comparator threshold opposite in polarity to the previous threshold exceeding peak.

The time channel, then, determines signal peak timing and the amplitude channel determines validity by blocking signal peaks that do not exceed the hysteresis comparator threshold. The delays in each of these channels to the D flip-flop inputs are well matched.

SERVO READ MODE

A position error signal (PES) is generated based on the relative amplitude of two servo signals, BURST A and BURST B.

Rectified servo signal peaks are captured on hold capacitors at the HOLDA/B pins. This is accomplished by pulling $\overline{\text{LATCHA}}$ or $\overline{\text{LATCHB}}$ low for a sample period. Additionally, a hold capacitor discharge current of up to 1.5 mA can be turned on by pulling $\overline{\text{RSTA}}/\overline{\text{RSTB}}$ low.

Outputs BURSTA/B and PES are referenced to an internal reference supplied by the VREF pin.

WRITE MODE

In Write Mode the SSI 32P548 Pulse Detector section is disabled and preset for the following Read Mode. The digital circuitry is disabled, the input AGC amplifier gain is held at its previous value and the AGC amplifier input impedance is reduced.

Holding the AGC amplifier gain and reducing input impedance shortens system Write to Read recovery times.

The lowered input impedance improves settling time by reducing the time constant of the network between the SSI 32P548 and a head preamplifier such as the SSI 32R1200R. Write to read timing is controlled to maintain the reduced impedance for 0.9 µs before the AGC circuitry is activated. Coupling capacitors should be chosen with as low a value as possible consistent with adequate bandwidth to allow more rapid settling.

DATA SYNCHRONIZER SECTION

The SSI 32P548 is designed to perform data synchronization and write precompensation in rotating memory systems which utilize a 2, 7 RLL and MFM encoding format. In the Read Mode the SSI 32P548 performs Data Synchronization, and Preamble Detect. In the Write Mode, the SSI 32P548 performs write precompensation. The interface electronics and architecture of the SSI 32P548 have been optimized for use as a companion device to the WD 42C22 controllers.

The SSI 32P548 can operate with data rates ranging from 5 to 12 Mbit/s. This data rate is established by a single 1% external resistor, RR, connected from pin IREF to VPA2. This resistor establishes a reference current which sets the VCO center frequency, the phase detector gain, and the 1/4 cell delay. The value of this resistor is given by:

$$RR = 50/DR - 1.7\ (k\Omega)$$

Where: DR = Data Rate in Mbit/s

An internal crystal reference oscillator, operating at twice the data rate, generates the standby reference for the PLL. A series resonant crystal between XTAL1 and XTAL2 should be selected at twice the Data Rate. If a crystal oscillator is not desired, then an external TTL compatible reference may be applied to XTAL1, leaving XTAL2 open.

The SSI 32P548 employs a Dual Mode Phase Detector; Harmonic in the Read Mode and Non-Harmonic in Write and Idle Modes. In the Read Mode the Harmonic Phase Detector updates the PLL with each occurrence of a DLYD DATA pulse. In the Write and Idle Modes the Non-Harmonic Phase Detector is continuously enabled, thus maintaining both phase and frequency lock. By acquiring both phase and frequency lock to the crystal reference oscillator and utilizing a zero phase restart technique, false lock to DLYD DATA is eliminated.

The phase detector incorporates a charge pump in order to drive the loop filter directly. The polarity and width of the output current pulses correspond to the direction and magnitude of the phase error. Figure 4 depicts the average output current as function of the input phase error (relative to the VCO period.)

The READ GATE (RG), and WRITE GATE (WG), inputs control the device mode as described in Table 1. RG is an asynchrouous input and may be initiated or terminated at any position on the disk. WG is also an asynchronous input, but should not be terminated prior to the last output Write Data pulse.

READ OPERATION

The Data Synchronizer utilizes a fully integrated fast acquisition PLL to accurately develp the decode window. Read Gate, RG, initiates the PLL locking sequence and selects the PLL reference input; a high level (Read Mode) selects the Read Data input and low level selects the crystal reference oscillator.

In the Read Mode the rising edge of DLYD DATA enables the Phase Detector while the falling edge is phase compared to the rising edge of the VCO. As depicted in Figure 2, DLYD DATA is a 1/4 cell wide (TVCO/2) pulse whose leading edge is defined by the leading edge of Read Data. RRC is generated from the rising edges of the VCO clock. By utilizing a fully integrated symmetrical VCO running at twice the data rate, RRC is insured to be accurate and centered symmetrically about the falling edges of DLYD DATA. The accuracy of the 1/4 cell delay only affects the retrace angle of the phase detector and does not influence the accuracy of RRC.

Shifting the symmetry of the VCO clock effectively shifts the relative position of the DLYD DATA pulse within the decode window. This powerful capability easily facilitates defect mappings, automatic calibration, window margin testing, error recovery, and systematic error cancellation. For enhanced disk drive testability and error recovery, decode window control is provided via a µP port ($\overline{WSL}$, WSD, $\overline{WS0}$, $\overline{WS1}$) as described in Table 2. In application not utilizing this feature, $\overline{WSL}$ should be left open or connected to VPA2, while WSD, $\overline{WS0}$, and $\overline{WS1}$ can be left open.

Window shifts in the range of ±1.5% to ±7.5% of TORC are easily programmed by latching the appropriate control word into the Window Shift Register with the WSL pin. Shifts in the positive or negative directions result in early or late decode windows respectively, as depicted in Figure 6. Additionally, for small systematic error cancellation, a resistor, R, connected from either RS (Early) or RF (Late) to ground will provide analog control over the decode window. The magnitude of this shift, TSA is determined by:

$$TSA = 0.125\,TORC\left(1 - \frac{790+R}{1450+R}\right)$$

Where: R is in Ω

Pins RF and RS are intended to be used as a trim and should be restricted to ±1.5% window shifts. They can be used in conjunction with the digital control port.

In Non-Read Modes, the PLL is locked to the crystal reference oscillator. This forces the VCO to run at a frequency which is very close to that required for tracking actual data and thus minimizes the associated frequency step during acquisition. When RG transitions, the VCO is stopped momentarily, then restared in an accurate phase alignment with the next PLL reference input pulse. By minimizing the phase alignment in this manner (phase error ≤ 0.5 rads), the acquisition time is substantially reduced.

PREAMBLE DETECTION

Preamble detection timing is set by the sum of the 1/4 cell delay and the retriggerable one-shot delay. The 1/4 cell timing capacitor is included on-chip and its timing is externally set by resistor RR. The retriggerable one-shot timing is externally set by resistor Rd and capacitor Cd. The sum of their delays is set to exceed the preamble bit spacing. Therefore, a continuous stream of input pulses at the preamble pulse rate keeps the SDO high, and a longer bit cell time input period allows the one-shot to time out producing a low at SDO.

WRITE OPERATION

Write precompensation circuitry is provided to compensate for media bit shift caused by intersymbol interference. The magnitude of the time shift, TC, is determinded by an external R-C network on the PCS pin given by:

TC = 0.155 Rp Cp

Direction of the time shift is determined by the state of the $\overline{\text{EARLY}}$ and $\overline{\text{LATE}}$ inputs.

POWER DOWN MODE

Two power down modes are provided to reduce power usage during the idle periods. Taking $\overline{\text{PDWN1}}$ low causes the device to go into complete shutdown, and taking the $\overline{\text{PDWN2}}$ pin low shuts down all functions not required for servo aquisition.

MODE CONTROL

The SSI 32P548 circuit mode is controlled by the $\overline{\text{PDWN1}}$, $\overline{\text{PDWN2}}$, $\overline{\text{HOLD}}$, RG, and WG pins as shown in Table 1.

TABLE 1: Mode Control

WG	RG	$\overline{\text{HOLD}}$	$\overline{\text{PDWN1}}$	$\overline{\text{PDWN2}}$	
0	0	1	1	1	Read Mode VCO Locked to XTAL
0	1	1	1	1	Read Mode VCO Locked to Read Data
0	X	0	1	1	Read Mode AGC gain held constant*
1	0	X	1	1	Write Mode AGC gain held constant* Input impedance reduced
X	X	X	0	X	Power Down 1 - Power shutdown mode
X	X	X	1	0	Power Down 2 - Servo mode

* AGC gain will drift at a rate determined by BYP and Hold mode discharge current.

Ts, NOMINAL WINDOW SHIFT	WSD	$\overline{WS1}$	$\overline{WS0}$
+TS3	0	0	0
+TS2	0	0	1
+TS1	0	1	0
0	0	1	1
-TS3	1	0	0
-TS2	1	0	1
-TS1	1	1	0
0	1	1	1

TABLE 2: Decode Window Symmetry Control

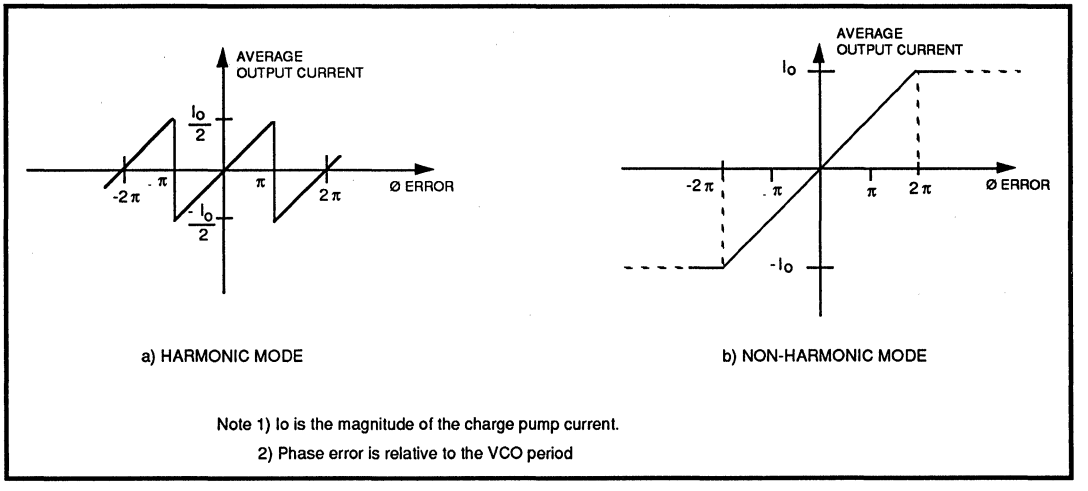


FIGURE 4: Phase Detector Transfer Function

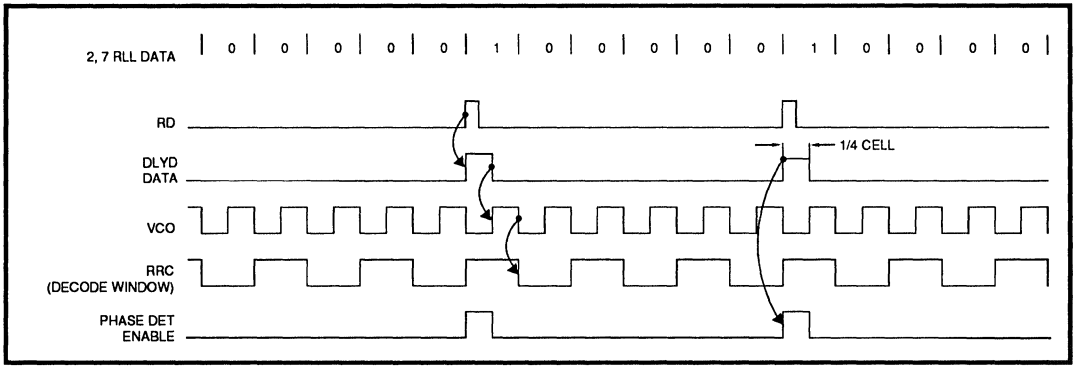


FIGURE 5: Data Synchronization Waveform Diagram

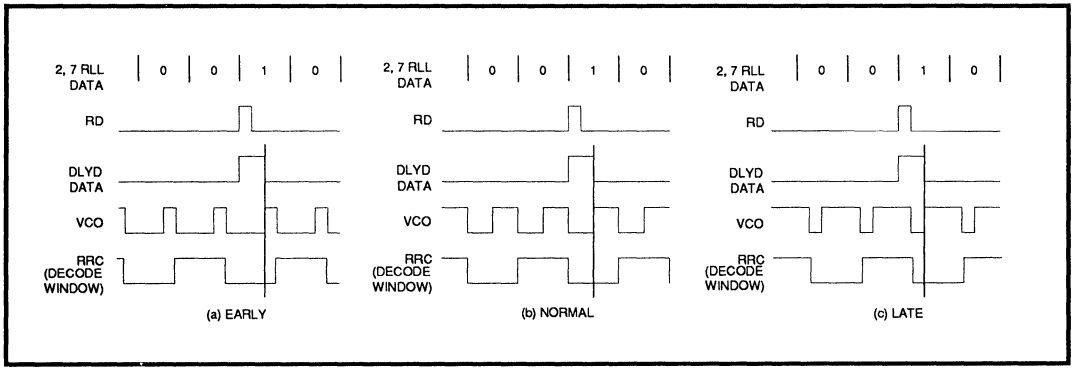


FIGURE 6: Decode Window

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
VPA1	I	Analog (+5V) power supply for pulse detector.
AGND1	I	Analog ground pin for pulse detector block.
VPA2	I	Analog (+5V) supply pin for data synchronizer block.
AGND2	I	Analog ground pin for data synchronizer block.
VPD	I	Digital (+5V) power supply pin.
DGND	I	Digital ground pin.
IN+, IN–	I	Analog signal input pins.
OUT+, OUT–	O	Read path AGC Amplifier output pins.
DIN+, DIN– *	I	Analog input to the hysteresis comparator.
CIN+, CIN– *	I	Analog input to the differentiator.
DIF+, DIF–	I/O	Pins for external differentiating network.
COUT	O	Test point for monitoring the flip-flop clock input.
DOUT	O	Test point for monitoring the flip-flop D-input.
RDO	O	Test point for ECL like read data prior to input to the data synchronizer.
BYP	I/O	An AGC timing capacitor or network is tied between this pin and AGND1.
AGC	I	Reference input voltage for the read data AGC loop.
LEVEL	O	Output from fullwave rectifier that may be used for input to the hysteresis comparator.
HYS	I	Hysteresis level setting input to the hysteresis comparator.
$\overline{\text{HOLD}}$	I	TTL compatible pin that holds the AGC gain when pulled low.
$\overline{\text{LATCHA}}$, $\overline{\text{LATCHB}}$	I	TTL compatible inputs that switch channel A or B into peak acquistion mode when low.
$\overline{\text{RST}}$, $\overline{\text{RSTA}}$, $\overline{\text{RSTB}}$ **	I	TTL compatible input that enables the discharge of channels A & B hold capacitors when held low.
CS***	I	Hold capacitor discharge current magnitude is controlled by a resistor from this pin to VPA or GND. If left open the default current is 1.5 mA.
HOLDA, HOLDB	I/O	Peak holding capacitors are tied from each of these pins to AGND1.
VREF	O	Reference voltage for Servo outputs.
BURSTA, BURSTB	O	Buffered hold capacitor voltage outputs.
PES	O	Position error signal, A minus B output.
$\overline{\text{PDWN1}}$	I	Low state on this pin puts the device in a low power "off" state.
$\overline{\text{PDWN2}}$	I	Low state on this pin disables all circuitry not required for use during Servo mode.
XTAL1, XTAL2	I	Crystal oscillator connections: if a crystal oscillator is not desired, XTAL1 may be driven by a TTL source with XTAL2 open.

*In 52-pin package CIN+ will be internally bonded to DIN+, CIN- will be internally bonded to DIN-.
**$\overline{\text{RSTA}}$ and $\overline{\text{RSTB}}$ will be internally bonded to $\overline{\text{RST}}$ in 52-pin package, and separately bonded out in 68-pin package.
***Not available in 52-pin package.

PIN DESCRIPTION (Continued)

NAME	TYPE	DESCRIPTION
IREF	I	Timing program pin: the VCO center frequency, Phase Detector Gain and the 1/4 cell delay are a function of the current source into pin IREF. The current is set by an external resistor, RR connected from IREF to VPA2.
FLTR	I/O	Filter pin: the phase detector output and VCO input node. The loop filter is connected to this pin.
SRD	O	Synchronized Read Data: read data that has been re-synchronized to read clock.
WSD	I	Window Symmetry Direction: controls the directions of the optional window symmetry shift. Pin WSD has an internal resistor pull-up.
$\overline{WS0}$	I	Window symmetry control bit: a low level introduces a window shift of 1.5% TORC (read reference clock period) in the direction established by WSD pin. $\overline{WS0}$ has an internal resistor pull-up.
$\overline{WS1}$	I	Window Symmetry Control bit: a low level introduces a window shift of 6% TORC (read reference clock period) in the direction established by WSD. A low level at both $\overline{WS0}$ and $\overline{WS1}$ will produce the sum of the two window shifts. Pin $\overline{WS1}$ has an internal resistor pull-up.
$\overline{WSL}$	I	Window Symmetry Latch: used to latch the input window symmetry control bits WSD, $\overline{WS0}$, $\overline{WS1}$ into the internal DAC. An active low level latches the input bits.
RF, RS*	I	WINDOW SYMMETRY ADJUST PINS: Provides analog control over the decode window symmetry; typically used to null out any window symmetry offset. A resistor connected from either RF or RS to AGND will provide magnitude and direction control. They can be used in conjunction with the digital control port WSD, $\overline{WS0}$, $\overline{WS1}$.
RRC	O	Read/Reference Clock: a multiplexed clock source used by the controller. In the read mode, this clock is the VCO frequency divided by two (1/TORC) and in the write mode it is the crystal reference frequency divided by two (1/TORO). No short clock pulses are generated during a mode change.
SDS	I	Sync Detect Set: used to program the preamble detect timing with an external RC Network. Connect the capacitor, Cd to VPA2 and the resistor, Rd, to AGND2.
RG	I	Read gate: selects the PLL reference input and initiates the PLL synchronization sequence. A high level selects the internal RD± inputs. A low level selects the crystal reference oscillator, Pin RG has an internal resistor pull-up.
WG	I	Write Gate: enables the write mode. Pin WG has an internal resistor pull-up.
SDO	O	Sync Detect Output: an active high output that indicates successful detection of the preamble sync field.
WDI	I	Write Data Input, active high.
$\overline{WD}$	O	Write Data: encoded write data output, active low.
PCS	I	Precomp Set: used to set the magnitude of the write pre-compensation time shift via an external capacitor, Cp to VPA2 and an external resistor, Rp to AGND2.
$\overline{EARLY}$	I	Early pin: shifts Write Data pulses earlier in their relative position; $\overline{EARLY}$ and $\overline{LATE}$ cannot be active simultaneously.

*Not available in 52-pin package.

PIN DESCRIPTION (Continued)

NAME	TYPE	DESCRIPTION
$\overline{\text{LATE}}$	I	Late Pin: shifts Write Data pulses later in their relative position $\overline{\text{LATE}}$ and $\overline{\text{EARLY}}$ cannot be active simultaneously.
PLL_REF	O	An open emitter ECL output test point. The positive edges of this output signal are phase locked with the positive edges of the VCO CLK signal. These two edges may be used to estimate window centering. The time jitter of the negative edge of the PLL_REF is an indication of media bit shift. Two external resistors are required to use this pin. They should be removed during normal operation for reduced power dissipation.
VCO CLK*	O	VCO CLK: An open emitter ECL output test point. Two external resistors are required to perform this test. They should be removed during normal operation for reduced power dissipation.
$\overline{\text{RDT}}$, VTEST*	I	Input test pins for testing the Data Synchronizer section only. To test the Data Synchronizer, connect VTEST pin to VPA2 and feed the TTL level test signal to $\overline{\text{RDT}}$ pin.

* Not available on 52-pin package

ELECTRICAL SPECIFICATIONS

Recommended conditions apply unless otherwise specified.

ABSOLUTE MAXIMUM RATINGS

Operation outside these rating limits may cause permanent damage to this device.

PARAMETER	RATING	UNIT
5V Supply Voltage, VPA1, VPA2, VPD	6.0	V
Pin Voltage (Analog pins)	-0.3 to VPA1, 2 + 0.3	V
Pin Voltage (All others)	-0.3 to VPD + 0.3 or +12 mA	V
Storage Temperature	65 to 150	°C
Lead Temperature (Soldering 10 sec.)	260	°C

RECOMMENDED OPERATING CONDITIONS

Currents flowing into the chip are positive.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Supply Voltage (VPA1, 2 & VPD)		4.75	5.0	5.25	V
Tj Junction Temperature		25		135	°C

POWER SUPPLY

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
IVPA1, 2 Supply Current IVPD	Outputs unloaded; $\overline{PDWN1}$, $\overline{PDWN2}$ = high or open			160	mA
Pd Power dissipation	Ta = 25°C, outputs unloaded		650	750	mW
	$\overline{PDWN1}$ = low, Outputs unloaded		300	380	mW
	$\overline{PDWN2}$ = low, $\overline{PDWN1}$ = high		450	550	mW

LOGIC SIGNALS

VIL	Input Low Voltage		-0.3		0.8	V
VIH	Input High Voltage		2.0		VCC+0.3	V
IIL	Input Low Current	VIL = 0.4V	0.0		-0.4	mA
IIL	WG Input Low Current	VIL = 0.4V	0.0		-0.8	mA
IIH	Input High Current	VIH = 2.7V			100	µA
VOL	Output Low Voltage	IOL = 4.0 mA			0.5	V
VOH	Output High Voltage	IOH = -400 µA	2.7			V
VIHX	XTAL1 Input High Voltage		2.6			V

* Output load is a 4K resistor to 5V and a 10 pF capacitor to DGND.

MODE CONTROL

Enable to/from $\overline{PDWN1}$, $\overline{PDWN2}$ Transition Time	Settling time of external capacitors not included, pin high to/from low			20	µs
Read to Write Transition Time	WG pin low to high			1.0	µs
Write to Read Transition Time	WG pin high to low AGC setting not included	0.5	0.9	1.3	µs
$\overline{HOLD}$ On to/from $\overline{HOLD}$ Off Transition Time	$\overline{HOLD}$ pin high to/from low			1.0	µs
RG Time Delay				100	ns

READ MODE WG is low

AGC AMPLIFIER

Unless otherwise specified, recommended operating conditions apply. Input signals are AC coupled to IN±. OUT± are loaded differentially with >340Ω x 2, and each side is loaded with < 10 pF to AGND, and AC coupled to DIN±. A 2000 pF capacitor is connected between BYP and AGND. AGC pin is open.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Gain Range	1.0 Vp-p ≤ (OUT+) - (OUT-) ≤ 3.0 Vp-p	4		80	V/V
Output Offset Voltage	Over entire gain range	-400		+400	mV
Maximum Output Voltage Swing	Set by BYP pin	3.0			Vp-p
Differential Input Resistance	(IN+) - (IN-) = 100 mVp-p @ 2.5 MHz		5.0		kΩ
Differential Input Capacitance	(IN+) - (IN-) = 100 mVp-p @ 2.5 MHz			10	pF
Common Mode Input	WG = low, IN+ or IN-		2.7		kΩ
Impedance	WG = high, IN+ or IN-			250	Ω
Input Noise Voltage	Gain set to maximum			15	nV/√Hz
Bandwidth	-3 dB bandwidth at maximum gain	16			MHz
OUT+ & OUT- Pin Current	No DC path to AGND		-4.0		mA
CMRR (Input Referred)	(IN+) = (IN-) = 100 mVp-p @ 5 MHz, gain set to max	40			dB
PSRR (Input Referred)	VPA1, 2 = 100 mVp-p @ 5 MHz, gain set to max	30			dB
(DIN+) - (DIN-) Input Swing vs. AGC Input	25 mVp-p ≤ (IN+) - (IN-) ≤ 250 mVp-p, $\overline{HOLD}$ = high, 0.5 Vp-p ≤ (DIN+) - (DIN-) ≤ 1.5 Vp-p	0.37	0.45	0.56	Vp-p/V
(DIN+) - (DIN-) Input Voltage Swing Variation	25 mVp-p ≤ (IN+) - (IN-) ≤ 250 mVp-p			8.0	%
AGC Voltage	AGC open		2.3		V
AGC Pin Input Impedance			2.5		kΩ
Slow AGC Discharge Current	(DIN+) - (DIN-) = 0V		4.5		µA
Fast AGC Discharge Current	Starts at 0.9 µs after WG goes low, stops at 1.8 µs after WG goes low	0.12			mA
AGC Leakage Current	$\overline{HOLD}$ = low	-0.2		+0.2	µA
Slow AGC Charge Current	(DIN+) - (DIN-) = 0.8 VDC, vary AGC until slow charge begins	-0.12	-0.18	-0.24	mA

AGC AMPLIFIER (Continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Fast AGC Charge Current	(DIN+) - (DIN-) = 0.8 VDC, V_{AGC} = 3.0V	-0.9	-1.3	-1.7	mA
Fast to Slow Attack Switchover Point	$\frac{[(DIN+)-(DIN-)]}{[(DIN+)-(DIN-)]FINAL}$		125		%
Gain Decay Time (Td)	(IN+) - (IN-) = 250 mVp-p to 125 mVp-p @ 2.5 MHz, (OUT+) - (OUT-) to 90% final value		12		µs
	(IN+) - (IN-) = 50 mVp-p to 25 mVp-p at 2.5 MHz (OUT+) - (OUT-) to 90% final value		60		µs
Gain Attack Time	WG = high to low (IN+) - (IN-) = 250 mVp-p @ 2.5 MHz, (OUT+) - (OUT-) to 110% final value		2		µs

WRITE MODE WG is high

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Common Mode Input Impedance			250		Ω

HYSTERESIS COMPARATOR

Unless otherwise specified, recommended operating conditions apply. Input (DIN+) - (DIN-) is an AC coupled, 1.0 Vp-p, 2.5 MHz sine wave. 0.5 VDC is applied to the HYS pin. WG pin is low.

Input Signal Range				1.5	Vp-p
Differential Input Resistance	(DIN+) - (DIN-) = 100 mVp-p @ 2.5 MHz	8	10	14	kΩ
Differential Input Capacitance	(DIN+) - (DIN-) = 100 mVp-p @ 2.5 MHz			5.0	pF
Common Mode Input Impedance (Both Sides)		2	2.5	3.5	kΩ
Level Pin Output Voltage vs. (DIN+) - (DIN-)	0.6 Vp-p < (DIN+) - (DIN-) < 1.5 Vp-p, 10K between LEVEL and AGND		1		V/Vp-p
Level Pin Output Impedance	I_{LEVEL} = 0.2 mA		250		Ω
Level pin Maximum Output Current		1.5			mA
Hysteresis Voltage at DIN± vs. HYS Pin Voltage	0.3 V < HYS < 1.0V		0.36		V/V

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HYSTERESIS COMPARATOR (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
HYS Pin Current	0.5 V < HYS < 1.5V	0.0		-10	µA
Comparator Offset Voltage	HYS pin at AGND ≤ 1.5 kΩ across DIN±			5.0	mV
DOUT Pin Output Low Voltage	5 kΩ from DOUT to GND		VPA2 -2		V
DOUT Pin Output High Voltage	5 kΩ from DOUT to GND		VPA2 -1.6		V

ACTIVE DIFFERENTIATOR

Unless otherwise specified, recommended operating conditions apply. Input (CIN+) - (CIN-) is an AC-coupled, 1.0 Vp-p, 2.5 MHz sine wave. 100Ω in series with 65 pF are tied from DIF+ to DIF-.

Input Signal Range				1.5	Vp-p
Differential Input Resistance	(CIN+) - (CIN-) = 100 mVp-p @ 2.5 MHz	8	10	14	kΩ
Differential Input Capacitance	(CIN+) - (CIN-) = 100 mVp-p @ 2.5 MHz			5.0	pF
Common Mode Input Impedance	Both sides	2.0	2.5	3.5	kΩ
Voltage Gain From CIN± to DIF±	(DIF+ to DIF-) = 2 kΩ		1		V/V
DIF+ to DIF- Pin Current	Differentiator impedance must be set so as to not clip the signal for this current level	±0.7			mA
Comparator Offset Voltage	DIF+, DIF- are AC-coupled			5.0	mV
COUT Pin Output Low Voltage	5 kΩ from COUT to GND		VPA2 -2		V
COUT Pin Output High Voltage	5 kΩ from COUT to GND		VPA2 -1.6		V
COUT Pin Output Pulse Width			30		ns

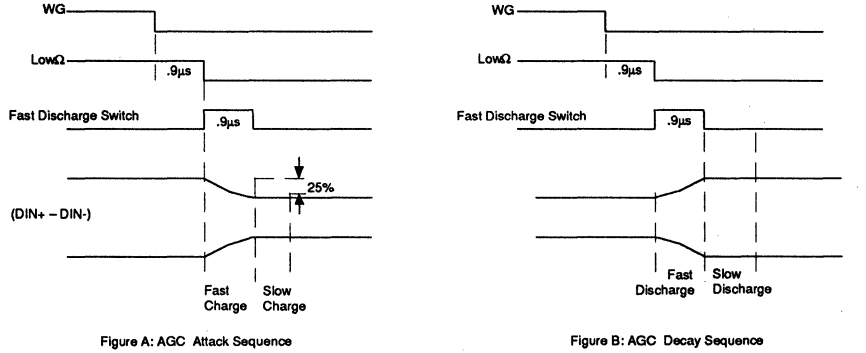

Figure A: AGC Attack Sequence

Figure B: AGC Decay Sequence

FIGURE 7: AGC Timing Diagram

QUALIFIER TIMING (See Figure 8)

Unless otherwise specified, recommended operating conditions apply. Inputs (CIN+) - (CIN-) and (DIN+) - (DIN-) are in-place as a coupled, 1.0 Vp-p, 2.5 MHz sine wave. 100Ω in series with 65 pF are tied from DIF+ to DIF-. 0.5V is applied to the HYS pin. COUT, DOUT and RD has a 5 kΩ pull-down resistor (for test purposes only.) WG pin is low.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Td1	D Flip-Flop Set Up Time	Minimum allowable time delay from (DIN+) - (DIN-) exceeding hysteresis point to (DIF+) - (DIF-) hitting a peak value.	0			ns
Td3	Propagation Delay			15		ns
|Td3-Td4|	Pulse Pairing				1.0	ns

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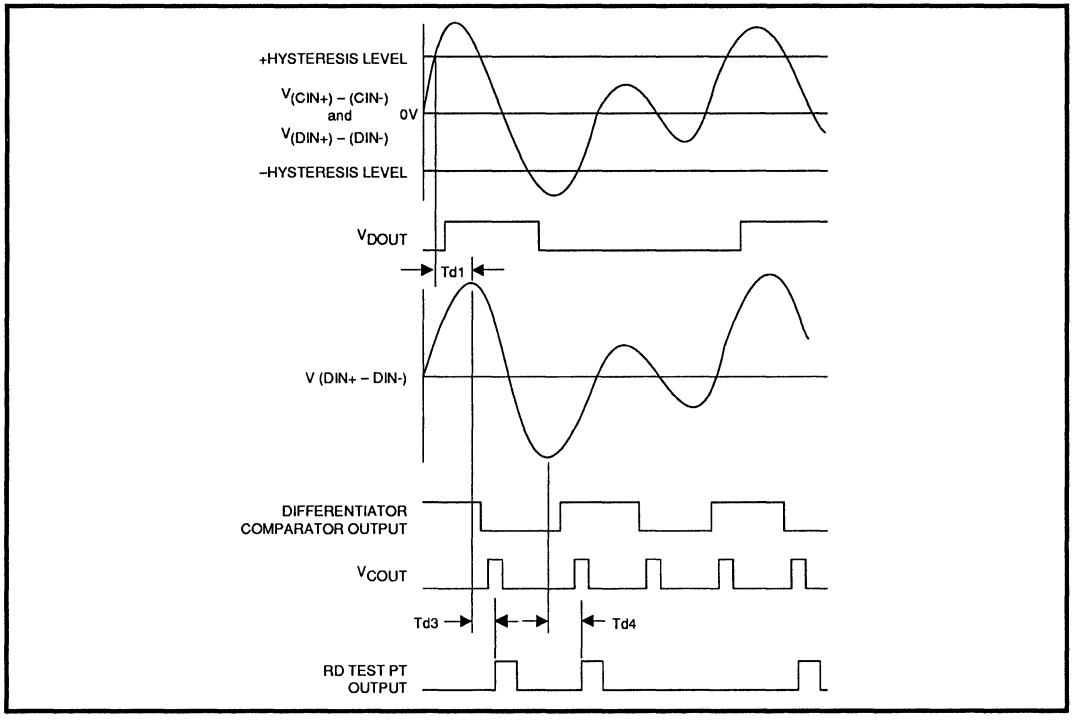

FIGURE 8: Read Mode Digital Section Timing Diagram

SERVO SECTION (Unless otherwise specified, recommended operating conditions apply.)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VREF Voltage Range Output			2.0		V
BURSTA/B Pin Output Voltage vs (DIN+) - (DIN-)	$\overline{LATCHA/B}$ = Low $\frac{V_{BURSTA/B} - VREF}{(DIN+) - (DIN-)}$		1.0		V/Vp-p
BURSTA/B Output Offset Voltage, V_{BURST} - VREF	$\overline{LATCHA/B}$ = Low, (DIN+) = (DIN-)	-50		+50	mV
BURSTA - BURSTB Output Offset Match	$\overline{LATCHA/B}$ = low (DIN+) = (DIN-)	-10		+10	mV
Output Resistance, BURSTA/B, PES				20	Ω
PES Pin Output Offset Voltage	V_{BURSTA} - V_{BURSTB} +VREF (DIN+) = (DIN-), $\overline{LATCHA/B}$ =Low	-10		+10	mV
HOLDA/B Discharge Current	$\overline{RST}$ = low,		1.5		mA
HOLDA/B Leakage Current	$\overline{RST}$ = high, $\overline{LATCHA/B}$ = high	-0.5		+0.5	µA
Load Resistance, BURSTA/B, PES	Resistors to VREF	10.0	20.0		kΩ
Load Capacitance, BURSTA/B, PES				20	pF
$\overline{LATCHA/B}$ pin set up time	TDS1, Figure 14	150			ns
$\overline{LATCHA/B}$ pin Hold Time	TDS2, Figure 14	150			ns
Channel A/B Discharge Current Turn On time	$\overline{RST}$ high → low			150	ns
Channel A/B Discharge Current Turn Off time	$\overline{RST}$ low → high			150	ns

SYNCHRONIZER SECTION

WRITE MODE (See Figure 9)

PARAMETER	CONDITIONS	MIN	MAX	UNIT
TWD, Write Data Pulse Width	CL ≤ 15 pF	(TORC/2)-12 -1.65 TPCO -TPC -12	(TORC/2)+12 -1.65 TPCO -TPC +12	ns
TFWD, Write Data Fall Time	2.0V to 0.8V, CL ≤ 15 pF		8	ns
TSWD, Write Data Input Setup Time	Either edge of WDI to either edge of RRC	15		ns

WRITE MODE (continued)

PARAMETER	CONDITIONS	MIN	MAX	UNIT
THWD, Write Data Input Hold Time	Either edge of RRC to either edge of WDI	3		ns
TSP, Early*/Late* Input Setup Time	Falling edge of Early*/Late* to either edge of RRC	15		ns
THP, Early*/Late* Input Hold Time	Rising edge of Early*/Late* to either edge of RRC	10		ns
TPC, Precompensation Time Shift Magnitude Accuracy	TPCO = 0.155 Rp Cp Rp = 1K to 2K	0.8TPC0	1.2TPC0	ns

READ MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
TRRC, Read Clock Rise Time	0.8V to 2.0V, CL ≤ 15 pF			8	ns
TFRC, Read Clock Fall Time	2.0V to 0.8V, CL ≤ 15 pF			5	ns
TSRD, Read Data Pulse Width		(TORC/2)-12		(TORC/2)+12	ns
TRSRD, Read Data Rise Time	0.8V to 2.0V, CL ≤ 15 pF			10	ns
TFSRD, Read Data Fall Time	2.0V to 0.8V, CL ≤ 15 pF			8	ns
TPSRD, SRD Output Setup/HoldTime		-15		15	ns
1/4 Cell + Retriggerable One-Shot Delay*	TD = 5.0 (RR +1.2) + 0.154 Rd (Cd +Cs)** ns RR in kΩ, Rd in kΩ, Cd in pF Cd = 68 pF to 100 pF	0.89TD		1.11TD	ns
1/4 Cell + Retriggerable One-Shot Detect Stability	4.5V < VPA2 < 5.5V	-4		+4	%

*Excludes External Capacitor and Resistor Tolerances. ** Cs = Stray Capacitance

WINDOW SYMMETRY CONTROL CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
TWSS $\overline{WS0}$, $\overline{WS1}$, WSD Set Up Time		50			ns
TWSH $\overline{WS0}$, $\overline{WS1}$, WSD Hold Time		0			ns

DATA SYNCHRONIZATION

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TVCO	VCO Center Frequency Period	VCO IN = 2.7V TO = TBD VPA2 = 5.0V	0.8TO		1.2TO	sec
	VCO Frequency Dynamic Range	1.0V ≤ VCO IN ≤ VPA2-0.6V VPA2 = 5.0V	±27		±40	%
KVCO	VCO Control Gain	ωo = 2π / TO 1.0V ≤ VCO IN ≤ VPA2-0.6V	0.14 ωo		0.20 ωo	rad/s V
KD	Phase Detector Gain	KD = 0.62 / (RR+500) VPA2 = 5.0V, Input = 3T Sync Field	0.83 KD		1.17 KD	A/rad
*	KVCO x KD Product Accuracy		-28		+28	%
*	VCO Phase Restart Error			6		ns
	Decode Window Centering Accuracy				± (0.01 TORC + 2)	ns
	Decode Window		(TORC/2) -2			ns
TS1	Decode Window Time Shift Magnitude	TS1 = 0.015 TORC $\overline{WSO}$ = 0; $\overline{WSI}$ = 1	0.8 TS1 -0.5		1.2 TS1 +0.5	ns
TS2	Decode Window Time Shift Magnitude	TS2 = 0.06 TORC $\overline{WSO}$ = 1; $\overline{WSI}$ = 0	0.8 TS2		1.2 TS2	ns
TS3	Decode Window Time Shift Magnitude	TS3 = 0.075 TORC $\overline{WSO}$ = 0; $\overline{WSI}$ = 0	0.8 TS3		1.2 TS3	ns
TSA	Decode Window Time Shift Magnitude	$TSA = 0.135\ TORC \cdot \left(1 - \frac{780 + R}{1450 + R}\right)$	0.65 TSA		1.35 TSA	ns

* Not directly testable; design characteristics

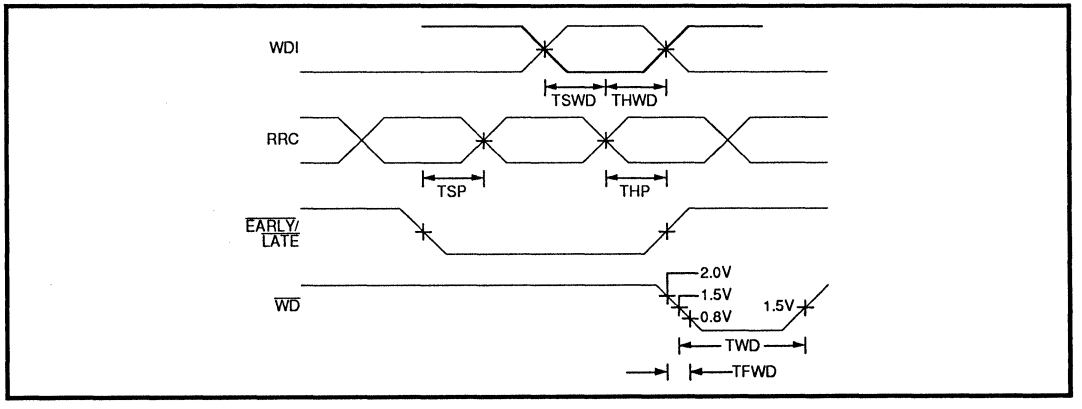

FIGURE 9: Write Mode Timing

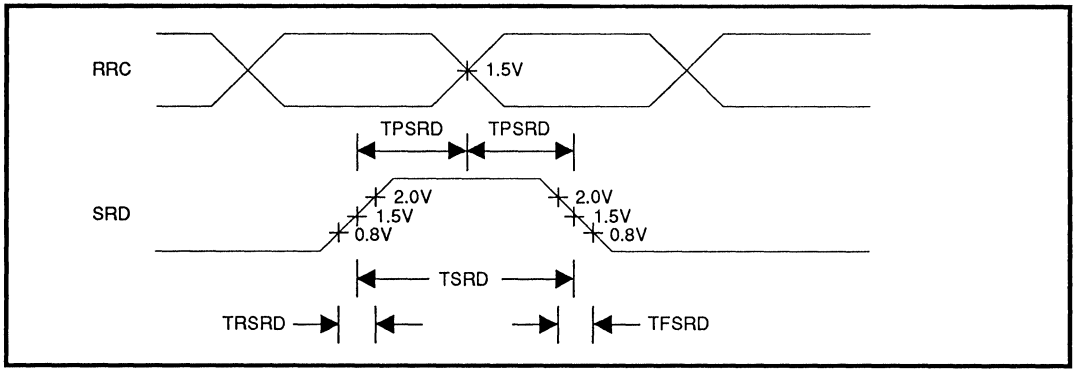

FIGURE 10: Read Mode Timing

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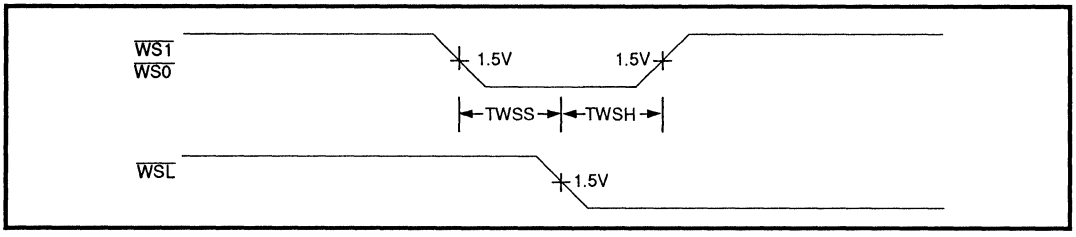


FIGURE 11: Window Symmetry Control Timing

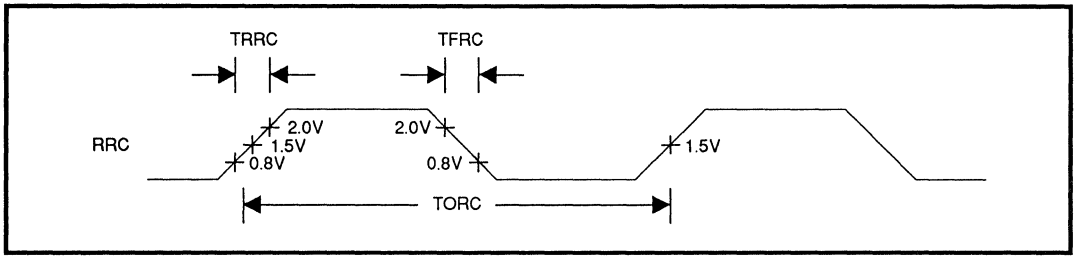


FIGURE 12: RRC Timing

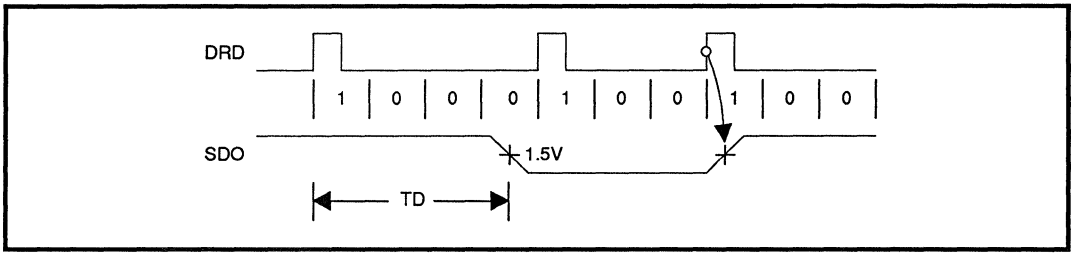


FIGURE 13: SDO Timing

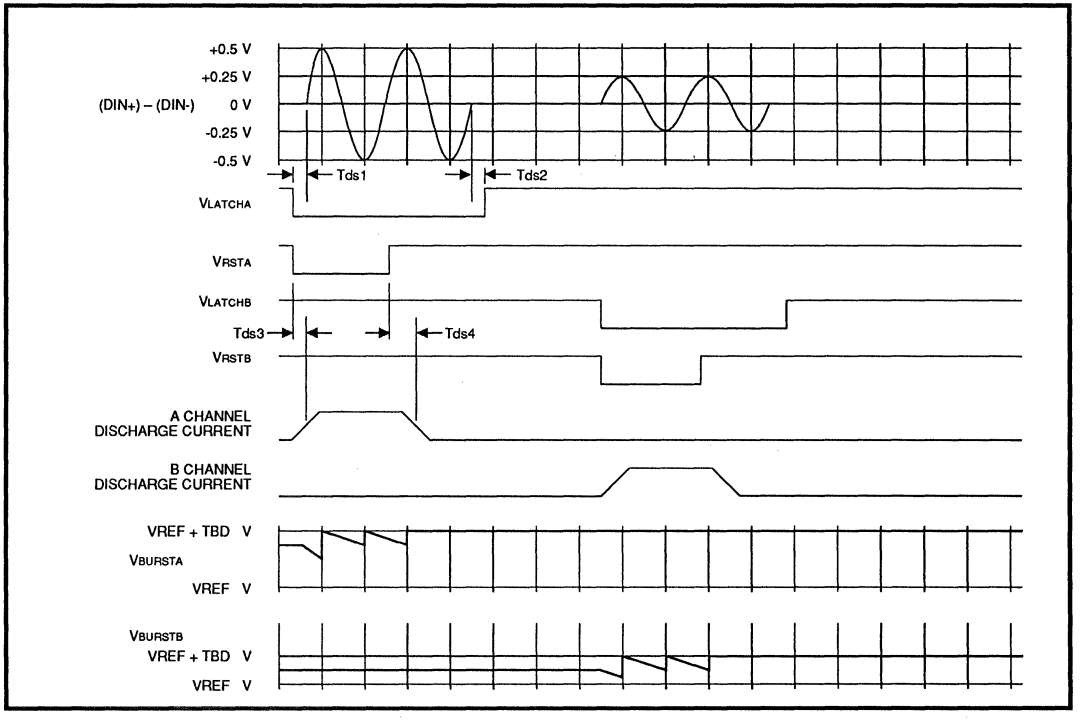


FIGURE 14: Servo Read Mode Timing

APPLICATIONS INFORMATION

The SSI 32P548 PLL uses a new architecture which incorporates an accurate quarter cell delay circuit. The standard architecture of a data synchronizer PLL is shown in Figure17A. In read mode, the rising edge of the quarter cell delay enables the phase detector, and the falling edge is locked to the VCO. Ideally, the quarter cell delay enables the phase detector one half of an encoded bit cell time before the phase comparison takes place. A data bit could then shift early or late by one half of an encoded bit cell time before a phase detector output error would occur. If the quarter cell delay is not exactly one half of an encoded bit cell time, a phase detector error will occur when the read data shifts by an amount that is smaller than one half of and encoded bit cell time when shifting in one direction and an amount larger than one half of an encoded bit cell time in the other direction. In addition, when an error occurs, the resulting charge pump output goes from maximum output one way to maximum output the other way. This can cause loss of lock to occur. The timing is shown in Figure 18.

The 32P548 achieves an accurate quarter cell delay time by using the VCO control voltage to compensate the quarter cell delay one-shot circuit for process, temperature and power supply induced timing variations. The modified architecture of the 32P548 data synchronizer is shown in Figure 19B. Because the quarter cell delay timing is adjusted by the VCO control voltage, there is an effect on the PLL transfer function due to the new quarter cell delay circuit.

The quarter cell delay circuit produces a time delay output in response to a voltage input. In order to include this function in a phase-locked loop, the time delay function must be converted into a phase function. This is straightforward, since a time delay is equivalent to a phase angle. The equivalent phase representation of the quarter cell delay is derived below.

For the VCO:

$$K_o = \frac{d\omega_o}{dV} \qquad (1a)$$

$$\frac{dT_o}{dV} = \frac{d}{dV}\left(\frac{1}{f_o}\right) = -\frac{1}{f_o^2}\frac{df_o}{dV} = -T_o^2\frac{df_o}{dV} = -\frac{T_o^2}{2\pi}\frac{dw_o}{dV} \qquad (1b)$$

where:

K_0 = VCO gain
ω_0 = VCO center frequency (rad/s)
f_0 = VCO center frequency (Hz)
T_0 = VCO center frequency (sec)

For the quarter cell delay,

$$K_T = \frac{dq_o}{dV} = \frac{2\pi}{T_o}a\frac{dT_o}{dV} = -\alpha T_o\frac{dw_o}{dV} = -\alpha T_o K_o$$

where:

θ_0 = Phase due to quarter cell delay circuit
T_0 = VCO center frequency period
T_Q = Quarter cell delay time
$\alpha = T_Q/T_0 = 0.5$ for the 32P548

The gain of the quarter cell delay block is constant in the 32P548, regardless of the values of other components.

For the 32P548, the nominal value of K_T is 0.17π.

PLL TRANSFER FUNCTION

There are two modes of operation of the PLL, and two transfer functions. In write and idle modes, the PLL is locked to the reference oscillator, and the quarter cell delay does not enter into the transfer function. In read, mode, the PLL is locked to read data, and the quarter cell delay is included in the transfer function. In addition, the effective loop gain of the PLL increases in idle mode due to the phase detector. This will be explained later in more detail.

The transfer functions for read and idle modes are given in (3) and (4), respectively.

$$\frac{\theta_o(s)}{\theta_r(s)} = \frac{\frac{nK_oK_dF(s)}{S}}{1+nK_TK_dF(s)+\frac{nK_oK_dF(s)}{S}} \qquad (3)$$

$$\frac{\theta_o(s)}{\theta_r(s)} = \frac{\frac{nK_oK_dF(s)}{S}}{1+\frac{nK_oK_dF(s)}{S}} \qquad (4)$$

where:

K_T = Quarter cell delay one-shot gain
K_o = VCO gain
K_d = Phase detector gain
F(s) = Loop filter transfer function
n = Ratio of input freq. to reference freq.

In (3) the K term in the denominator is a result of the quarter cell delay. Substituting $K_T = \alpha K_O T_O$ into (3),

$$\frac{\theta_o(s)}{\theta_r(s)} = \frac{\frac{nK_oK_dF(s)}{S}}{1+(1-s\alpha T_o)\frac{nK_oK_dF(s)}{S}}$$

The additional $-s\alpha T_O$ term in the denominator due to the quarter cell delay introduces positive feedback. However, the gain of the positive feedback is always less than one, so there is no instability. The additional term is not always negligible, and must be taken into account in the loop analysis and design.

Two loop filter configurations, shown in Figure 15, will be considered. Both filters result in a second order type 2 loop transfer function, with only minor differences in the loop equation.

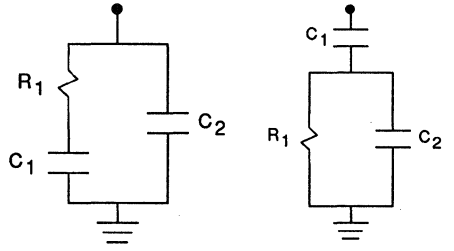


FIGURE 15: Loop Filter

The transfer function of the loop filter for a charge-pump PLL is the transimpedance, $V_o/I_i(s)$, where $V_o(s)$ is the output voltage, and $I_i(s)$ is the input current. The transfer functions of (a) and (b) are given by:

$$F_a(s) = \frac{sR_1C_1+1}{s(C_1+C_2)\left(sR_1\frac{C_1C_2}{C_1+C_2}+1\right)} \quad (6)$$

$$F_b(s) = \frac{sR_1(C_1+C_2)+1}{sC\left(sR_1C2+1\right)} \quad (7)$$

For loop filter (a), C is normally chosen to be much smaller than C so that it does not affect the loop transfer function significantly. Assuming the C » C and sRC « 1 at the frequencies of interest, (6) reduces to:

$$F_a(s) = \frac{sR_1C_1+1}{sC_1} \quad (8)$$

For loop filter (b), C is normallly chosen to be much smaller than C, so that it does not affect the loop transfer function significantly. Assuming the C » C and that sRC « 1 at the frequencies of interest, (7) reduces to:

$$F_b(s) = \frac{sR_1C_1+1}{sC_1} \quad (9)$$

Equations (8) and (9) are the same, and either loop filter may be used. Substituting (8) into (3) gives:

$$\frac{\theta_o(s)}{\theta_r(s)} = \frac{\frac{nK_oK_d}{C_1(1-\alpha T_onK_oK_dR_1)}(sR_1C_1+1)}{s^2+s\frac{nK_oK_d}{1-\alpha T_onK_oK_dR_1}\left(R_1-\frac{\alpha T_o}{C_1}\right)+\frac{nK_oK_d}{C_1(1-\alpha T_onK_oK_dR_1)}} \quad (10)$$

This is in the form of a standard second order transfer fucntion. The denominator has the form:

$$D(s) = s^2 + 2\zeta\omega_n s + \omega_n^2 \quad (11)$$

where: ζ = damping factor
ω_n = natural frequency

The damping factor and natural frequency of (10) can be extracted:

$$\omega_n = \sqrt{\frac{nK_oK_d}{C_1(1-\alpha T_onK_oK_dR_1)}} \quad (12)$$

$$\zeta = \frac{R_1-\frac{\alpha T_o}{C_1}}{2}\sqrt{\frac{nK_oK_dC_1}{1-\alpha T_onK_oK_dR_1}} \quad (13)$$

Substituting (8) into (4) gives the transfer function for idle mode:

$$\frac{\theta_o(s)}{\theta_r(s)} = \frac{\frac{nK_oK_d}{C_1}(sR_1C_1+1)}{s^2+s(nK_oK_dR_1)+\frac{nK_oK_d}{C_1}} \quad (14)$$

Again, this is in the form of a second order transfer function. The damping factor and natural frequency are found to be:

$$\omega_n = \sqrt{\frac{nK_0K_d}{C_1}} \quad (15)$$

$$\zeta = \frac{R_1}{2}\sqrt{nK_0K_dC_1} \quad (16)$$

To design the loop for proper read mode operation using (12) and (13), R, and C, must be found in terms of the damping factor and natural frequency.

To do this, first find ζ/ω_n, then solve for R_1C_1.

$$R_1C_1 = \frac{2\zeta}{\omega_n} + \alpha T_0 \quad (17)$$

Substitute this value for R_1C_1 into the equation for ω_n and solve for C_1.

$$C_1 = \frac{nK_0K_d}{\omega_n^2} + \alpha T_0 nK_0K_d\left(\frac{2\zeta}{\omega_n} + \alpha T_0\right) \quad (18)$$

Now that C_1 is known, R_1 can be found by dividing (17) through by C_1.

$$R_1 = \left(\frac{2\zeta}{\omega_n} + \alpha T_0\right)\frac{1}{C_1} \quad (19)$$

EXAMPLE 1

Assume that the data rate is 10 Mbit/s, a 3T preamble pattern is used, and that $\omega_n = 10^6$ and $\zeta = 0.707$ are desired.

For the SSI 32P548:

$R_R = 50/DR - 1.7\ k\Omega$
$K_0 = 0.17\omega_0 = 21.4 \cdot 10^6$
$K_d = 0.62/(R_R+500) = 160 \cdot 10^6$
$K_T = 0.17\pi = 0.534$

Due to the 3T preamble pattern, the input frequency is one third the VCO frequency, so n = 1/3.

$\omega_0 = 2\pi(2 \cdot 10^7)$, $\alpha = 0.5$, and $T_0 = 1/(20 \cdot 10^6) = 50$ ns
$C_1 = 1160\ pF + 41.9\ pF = 1.21\ nF$
$R_1 = 1.20\ k\Omega$

The resulting loop filter is shown in Figure 16.

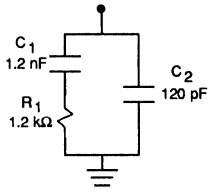


FIGURE 16

The value of $C_2 = C_1/10$ is chosen to damp out transients on the FILT pin and meet the requirement $C_2 \ll C_1$.

When the loop locks to the reference oscillator in idle mode, the loop transfer function is given by (14), and ω_n and ζ are given by (15) and (16). R_1 and C_1 from Example 1 can be substituted into these equations to find the resulting natural frequency and damping factor in idle mode.

EXAMPLE 2

When locking onto the reference oscillator, the input frequency is the same as the VCO frequency, so n = 1. Using the values of R_1 and C_1 found in Example 1, the values of ω_n and ζ when locking to the reference oscillator are found to be:

$\omega_n = 1.7 \cdot 10^6$ rad/s
$\zeta = 1.23$

5

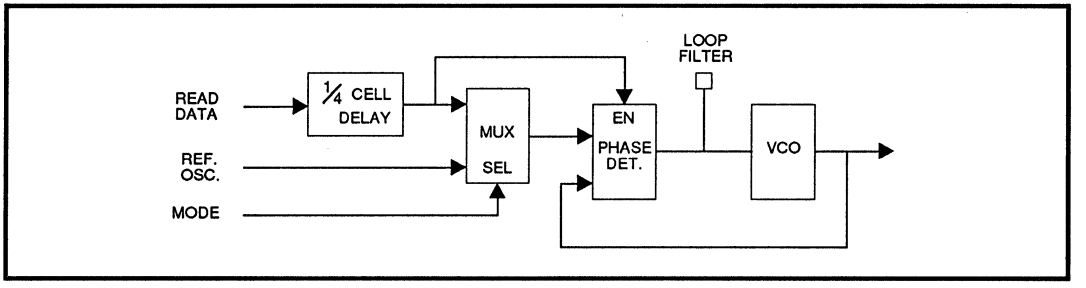


FIGURE 17A: Standard Configuration of a Data Synchronizer Phase-Locked Loop

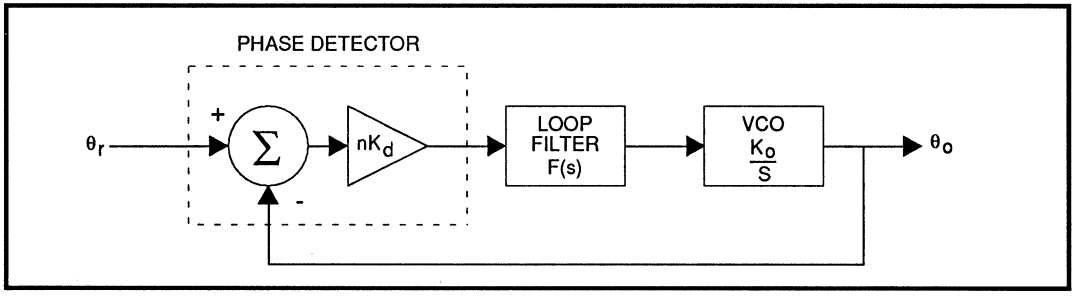


FIGURE 17B: Phase-Lock Loop System Representation

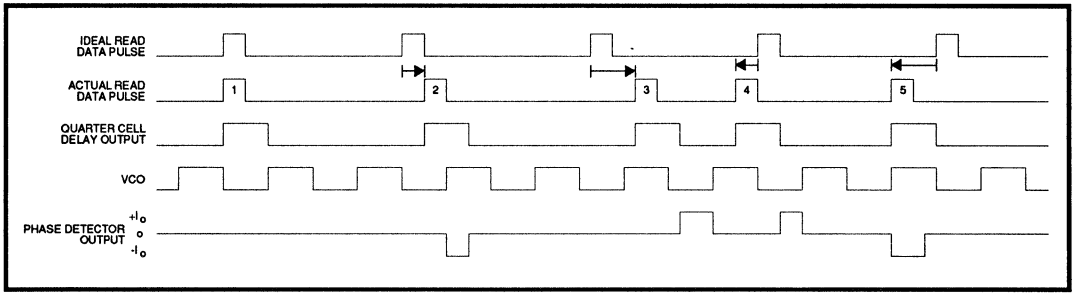


FIGURE 18A: Phase Detector Timing with Ideal Quarter Cell Delay. For an ideal pulse (1), there is no phase detector output. When a pulse is shifted late (2) or early (4) by less than the quarter cell delay time, the phase detector output is negative or positive, respectively. When the read data is shifted late (3) or early (5) by more than the quarter cell delay time, a phase detector output polarity error occurs. In this case, the output polarity becomes positive for a late shifted pulse and negative for an early shifted pulse.

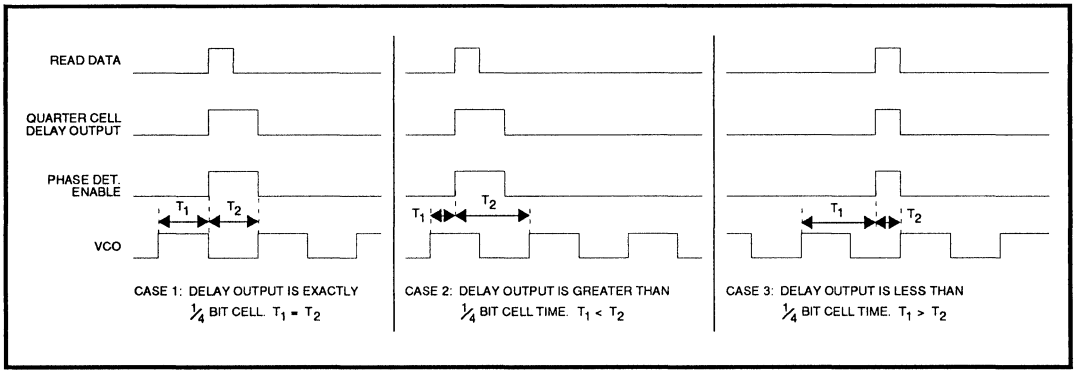


FIGURE 18B: Timing of Phase Detector Enable Logic. The read data input pulse can shift to the left by T1 and to the right by T2 before an error occurs in the phase detector output polarity, If the quarter cell delay output is not exactly 1/4 bit cell wide, then T1 ≠ T2, as shown in cases 2 and 3.

5

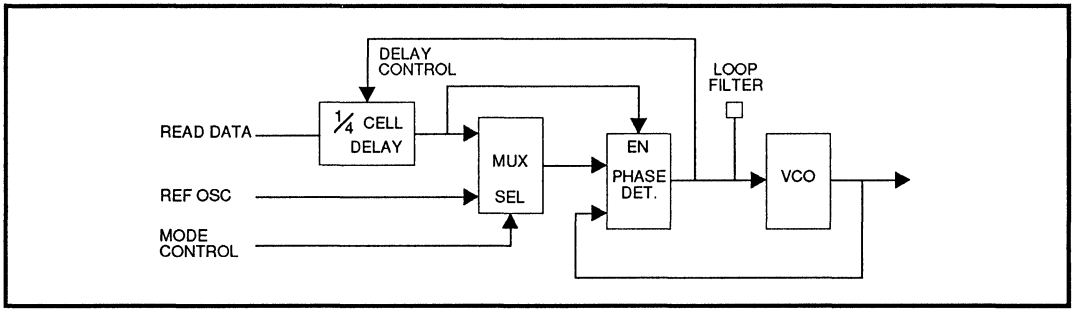


FIGURE 19A: Modified Data Synchronizer Phase-Locked-Loop with Quarter Cell Delay Control

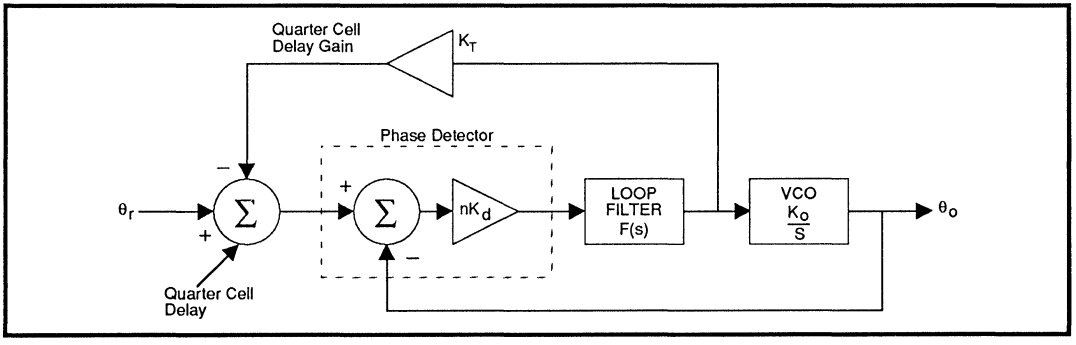
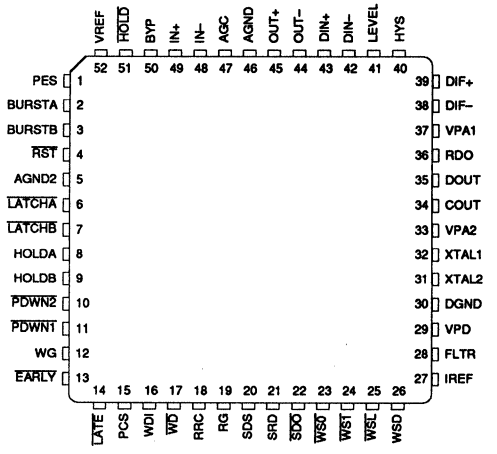


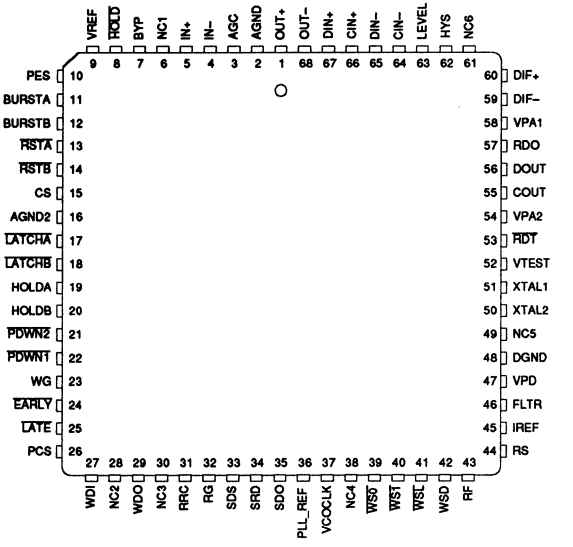
FIGURE 19B: Modified Data Synchronizer System Representation

SSI 32P548
Pulse Detector & Data Synchronizer

PACKAGE PIN DESIGNATIONS
(Top View)



52-Pin QFP



68-Pin PLCC

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only.

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SSI 32P5481/5482
Pulse Detector & Data Synchronizer
Advance Information

November 1991

DESCRIPTION

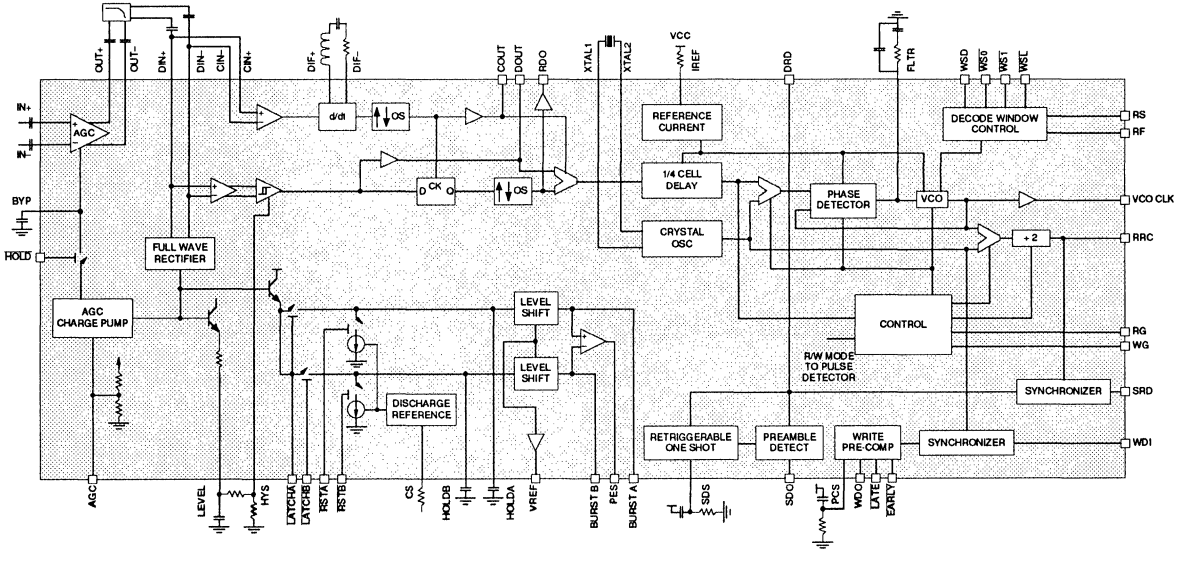
The SSI 32P5481/5482 is a low power, high performance Pulse Detection, Data Synchronization combination device. This device is designed for use in low power applications requiring +5V only power supplies. The pulse detection portion of this device detects and validates amplitude peaks in the output from a disk drive read amplifier, as well as detecting embedded servo information to provide position signals used for read head positioning. The data synchronization portion is a 2, 7 data synchronizer with window shift. The SSI 32P5481/5482 also provides write precompensation function. The SSI 32P5481/5482 achieves low system operating power three ways, with a low operating power (+5V only design) and with two independent power down modes. Mode 1 is a complete shutdown or sleep mode. Mode 2 is a low power mode for use while acquiring servo, where all circuitry not associated with obtaining servo information is powered down. The SSI 32P5481/5482 is available in a 52-pin fine pitch QFP, and 68-pin PLCC.

FEATURES

- **Highly Integrated Pulse Detector and Data Synchronizer**
- **+5V only Power Supplies**
- **Low Power <500 mW (max)**
- **Dual Power Down Modes**
- **Dual Servo Burst Channels with Position Error Signal**
- **Low Pulse Pairing (≤ ±1 ns)**
- **8-16 Mbit/s operation**

5

BLOCK DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

CIRCUIT OPERATION

PULSE DETECTOR SECTION

READ MODE

In read mode the SSI 32P5481/5482 is used to process either data or servo signals. In the Data Read Mode the input signal is amplified and qualified using an AGC amplifier and pulse level qualification of the detected signal peaks. In the servo read mode the input signal is amplified and rectified. Two servo burst channels are available that provide A and B burst levels.

DATA READ MODE

An amplified head output signal is AC coupled to the IN+ and IN- pins of the AGC amplifier. Gain control is accomplished by full wave rectifying and amplifying the [(DIN+)-(DIN-)] voltage level and comparing it to a reference voltage level at the AGC pin.

The SSI 32P5481/5482 contains a dual rate attack charge pump. The value of the attack current is dependent on the instantaneous level at DIN±. For signal levels above 125% of the desired level a fast attack mode is invoked that supplies a 1.3 mA charge current to the network on the BYP pin. Between 125% and 100% of the desired level the circuit enters a slow attack mode and supplies 0.18 mA of charge current to the BYP pin.

Two decay modes are available and are automatically controlled within the device.

Upon a switch to write mode, the device will hold the gain at its previous value. When the device is then switched back to read mode the AGC holds the gain and stays in a low impedance state for 0.9 µs. It then switches into a fast/slow attack mode if the new gain required is less than the previously held gain or a fast decay mode if the gain required is more than its previous value. The fast decay current is 0.12 mA and stays on 0.9 µs. After the 0.9 µs time period the device stays in a steady state slow attack, slow decay mode. The slow decay discharge current is 4.5 µA.

The AGC pin is internally biased so that the target differential voltage input at DIN± is 1.0 Vp-p under nominal conditions. The voltage on this pin can be modified by tying a resistor between AGC and GND or VPA. A resistor to GND decreases the voltage level, while a resistor to VPA increases it. The resulting AGC

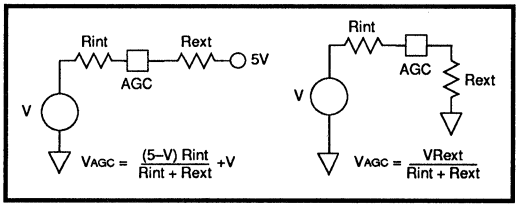


FIGURE 1: AGC Voltage

voltage level is shown in Figure 1; where:

V = Voltage at AGC w/pin open (1.0V, nom)

Rint = AGC pin input impedance (3.91 kΩ, typ)

Rext = External resistor

The new DIN ± input target level is nominally 1.0 Vp-p/ V_{AGC}.

The maximum AGC amplifier output swing is 3.0 Vp-p at OUT±, which allows for up to 8dB loss in any external filter between OUT± and DIN±.

AGC gain is a linear function of the BYP-pin voltage (VBYP) as shown in Figure 2.

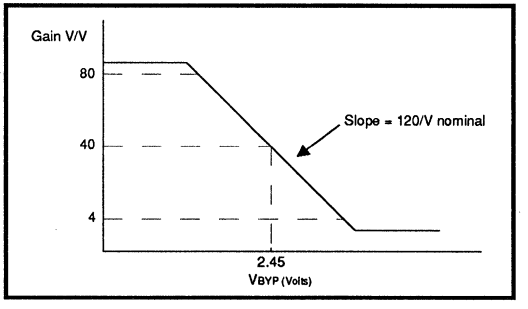


FIGURE 2: AGC Gain

The AGC amplifier has an open collector output and can sink 6.0 mA. For correct operation to the gain range the outputs should be pulled up to VPA through a 340Ω resistor as shown in Figure 3.

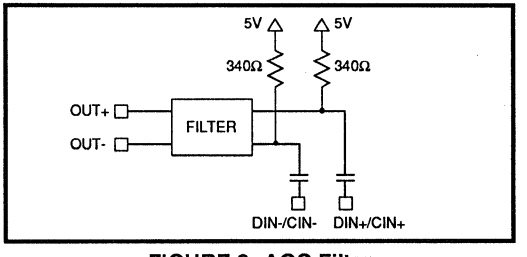


FIGURE 3: AGC Filter

In the 52-pin package configuration CIN+ and DIN+ will be bonded together, likewise CIN- and DIN- will be bonded together. In this situation one filter must be used for both time and amplitude channels. A multipole Bessel filter is typically used for its linear phase or constant group delay characteristics.

In the amplitude channel the signal is sent to a hysteresis comparator. The hysteresis threshold level is set so that it will be tripped only by valid signal pulses and not by baseband noise. It can be fixed level or a fraction of the DIN± voltage level.

The latter approach is accomplished by using an external filter/network between the LEVEL and HYS pins. This allows setting the AGC slow attack and decay times slow enough to minimize time channel distortion and setting a shorter time constant for the hysteresis level. The LEVEL pin output is a rectified and amplified version of DIN±, 1.0 p-p at DIN± results in 1.0 Vo-p nominally, at the LEVEL pin. A voltage divider is used from LEVEL to ground to set the Hysteresis threshold at a percentage of the peak DIN± voltage. For example, if DIN± is 1.0 Vp-p, then using an equal valued resistor divider will result in 0.5 Vpk at the HYS pin. This will result in a nominal ±0.18V threshold or a 36% threshold of a ±0.500V DIN± input. The capacitor is chosen to set an appropriate time constant. This "feed forward" technique speeds up transient recovery by allowing qualification of the input pulses while the AGC is still settling. This helps in the two critical areas of write to read and head change recovery. Some care in the selection of the hysteresis level time constant must be exercised so as to not miss pattern (resolution) induced lower amplitude signals. The output of the hysteresis comparator is the "D" input of a D-type flip-flop. The DOUT pin is a comparator output signal for testing purposes only.

In the time channel the signal is differentiated to transform signal peaks to zero crossings which are detected and used to trigger a bi-directional one-shot. The one-shot output pulses are used as the clock input of the D flip-flop. The COUT pin provides the one-shot output for test purposes.

The differentiator function is accomplished by an external network between the DIF+ and DIF- pins. The transfer function from CIN± to the comparator input (not DIF±) is:

$$Av = \frac{Cs}{LCs^2 + C(R+92)s + 1}$$

where: C, L, R are external passive components
$15\ pF < C < 125\ pF$
$s = j\omega = j2\pi f$

During normal operation, the time channel clocks the D flip-flop on every positive and negative peak of the CIN± input. The D input to the flip-flop only changes state when the DIN± input exceeds the hysteresis comparator threshold opposite in polarity to the previous threshold exceeding peak.

The time channel, then, determines signal peak timing and the amplitude channel determines validity by blocking signal peaks that do not exceed the hysteresis comparator threshold. The delays in each of these channels to the D flip-flop inputs are well matched.

SERVO READ MODE

A position error signal (PES) is generated based on the relative amplitude of two servo signals, BURST A and BURST B.

Rectified servo signal peaks are captured on hold capacitors at the HOLDA/B pins. This is accomplished by pulling $\overline{\text{LATCHA}}$ or $\overline{\text{LATCHB}}$ low for a sample period. Additionally, a hold capacitor discharge current of up to 1.5 mA can be turned on by pulling $\overline{\text{RSTA}}/\overline{\text{RSTB}}$ low.

Outputs BURSTA/B and PES are referenced to an internal reference supplied by the VREF pin.

WRITE MODE

In Write Mode the SSI 32P5481/5482 Pulse Detector section is disabled and preset for the following Read Mode. The digital circuitry is disabled, the input AGC amplifier gain is held at its previous value and the AGC amplifier input impedance is reduced.

Holding the AGC amplifier gain and reducing input impedance shortens system Write to Read recovery times.

The lowered input impedance improves settling time by reducing the time constant of the network between the SSI 32P5481/5482 and a head preamplifier such as the SSI 32R1200R. Write to read timing is controlled to maintain the reduced impedance for 0.9 µs before the AGC circuitry is activated. Coupling capacitors should be chosen with as low a value as possible consistent with adequate bandwidth to allow more rapid settling.

5

DATA SYNCHRONIZER SECTION

The SSI 32P5481/5482 is designed to perform data synchronization in rotating memory systems which utilize a 2, 7 RLL and MFM encoding format. In the Read Mode the SSI 32P5481/5482 performs Data Synchronization, and Preamble Detect. In the Write Mode, the SSI 32P5481 performs write precompensation. The interface electronics and architecture of the SSI 32P5481/5482 have been optimized for use as a companion device to the WD 42C22 controllers.

The SSI 32P5481/5482 can operate with data rates ranging from 8 to 16 Mbit/s. This data rate is established by a single 1% external resistor, RR, connected from pin IREF to VPA2. This resistor establishes a reference current which sets the VCO center frequency, the phase detector gain, and the 1/4 cell delay. The value of this resistor is given by:

$$RR = 75.5/DR - 2\ (k\Omega)$$

Where: DR = Data Rate in Mbit/s

An internal crystal reference oscillator, operating at twice the data rate, generates the standby reference for the PLL. A series resonant crystal between XTAL1 and XTAL2 should be selected at twice the Data Rate. If a crystal oscillator is not desired, then an external TTL compatible reference may be applied to XTAL1, leaving XTAL2 open.

The SSI 32P5481/5482 employs a Dual Mode Phase Detector; Harmonic in the Read Mode and Non-Harmonic in Write and Idle Modes. In the Read Mode the Harmonic Phase Detector updates the PLL with each occurrence of a DLYD DATA pulse. In the Write and Idle Modes the Non-Harmonic Phase Detector is continuously enabled, thus maintaining both phase and frequency lock. By acquiring both phase and frequency lock to the crystal reference oscillator and utilizing a zero phase restart technique, false lock to DLYD DATA is eliminated.

The phase detector incorporates a charge pump in order to drive the loop filter directly. The polarity and width of the output current pulses correspond to the direction and magnitude of the phase error. Figure 4 depicts the average output current as function of the input phase error (relative to the VCO period.)

The READ GATE (RG), and WRITE GATE (WG), inputs control the device mode as described in Table 1. RG is an asynchrouous input and may be initiated or terminated at any position on the disk. WG is also an asynchronous input, but should not be terminated prior to the last output Write Data pulse.

READ OPERATION

The Data Synchronizer utilizes a fully integrated fast acquisition PLL to accurately develp the decode window. Read Gate, RG, initiates the PLL locking sequence and selects the PLL reference input; a high level (Read Mode) selects the Read Data input and low level selects the crystal reference oscillator.

In the Read Mode the rising edge of DLYD DATA enables the Phase Detector while the falling edge is phase compared to the rising edge of the VCO. As depicted in Figure 2, DLYD DATA is a 1/4 cell wide (TVCO/2) pulse whose leading edge is defined by the leading edge of Read Data. RRC is generated from the rising edges of the VCO clock. By utilizing a fully integrated symmetrical VCO running at twice the data rate, RRC is insured to be accurate and centered symmetrically about the falling edges of DLYD DATA. The accuracy of the 1/4 cell delay only affects the retrace angle of the phase detector and does not influence the accuracy of RRC.

Shifting the symmetry of the VCO clock effectively shifts the relative position of the DLYD DATA pulse within the decode window. This powerful capability easily facilitates defect mappings, automatic calibration, window margin testing, error recovery, and systematic error cancellation. For enhanced disk drive testability and error recovery, decode window control is provided via a µP port ($\overline{WSL}$, WSD, $\overline{WS0}$, $\overline{WS1}$) as described in Table 2. In application not utilizing this feature, $\overline{WSL}$ should be left open or connected to VPA2, while WSD, $\overline{WS0}$, and $\overline{WS1}$ can be left open.

Window shifts in the range of ±1.5% to ±7.5% of TORC are easily programmed by latching the appropriate control word into the Window Shift Register with the WSL pin. Shifts in the positive or negative directions result in early or late decode windows respectively, as depicted in Figure 6. Additionally, for small systematic error cancellation, a resistor, R, connected from either RS (Early) or RF (Late) to ground will provide analog control over the decode window. The magnitude of this shift, TSA is determined by:

$$TSA = 0.125\,TORC\left(1 - \frac{790+R}{1450+R}\right)$$

Where: R is in Ω

Pins RF and RS are intended to be used as a trim and should be restricted to ±1.5% window shifts. They can be used in conjunction with the digital control port.

In Non-Read Modes, the PLL is locked to the crystal reference oscillator. This forces the VCO to run at a frequency which is very close to that required for tracking actual data and thus minimizes the associated frequency step during acquisition. When RG transitions, the VCO is stopped momentarily, then restared in an accurate phase alignment with the next PLL reference input pulse. By minimizing the phase alignment in this manner (phase error ≤ 0.5 rads), the acquisition time is substantially reduced.

PREAMBLE DETECTION

Preamble detection timing is set by the sum of the 1/4 cell delay and the retriggerable one-shot delay. The 1/4 cell timing capacitor is included on-chip and its timing is externally set by resistor RR. The retriggerable one-shot timing is externally set by resistor Rd and capacitor Cd.

TOS = 0.1 • RD • (Cd + Cs) nsec, where Rd is in kΩ, Cd is in pF. Cs = stray capacitance.

The sum of their delays is set to exceed the preamble bit spacing. Therefore, a continuous stream of input pulses at the preamble pulse rate keeps the SDO high, and a longer bit cell time input period allows the one-shot to time out producing a low at SDO.

WRITE OPERATION

Write precompensation circuitry is provided to compensate for media bit shift caused by intersymbol interference. The magnitude of the time shift, TC, is determinded by an external R-C network on the PCS pin given by:

TC = TBD Rp Cp

Direction of the time shift is determined by the state of the $\overline{\text{EARLY}}$ and $\overline{\text{LATE}}$ inputs.

POWER DOWN MODE

Two power down modes are provided to reduce power usage during the idle periods. Taking $\overline{\text{PDWN1}}$ low causes the device to go into complete shutdown, and taking the $\overline{\text{PDWN2}}$ pin low shuts down all functions not required for servo aquisition.

MODE CONTROL

The SSI 32P5481/5482 circuit mode is controlled by the $\overline{\text{SLEEP}}$, $\overline{\text{SERVO}}$, $\overline{\text{HOLD}}$, RG, and WG pins as shown in Table 1.

TABLE 1: Mode Control

WG	RG	$\overline{\text{HOLD}}$	$\overline{\text{PDWN1}}$	$\overline{\text{PDWN2}}$	
0	0	1	1	1	Read Mode VCO Locked to XTAL
0	1	1	1	1	Read Mode VCO Locked to Read Data
0	X	0	1	1	Read Mode AGC gain held constant*
1	0	X	1	1	Write Mode AGC gain held constant* Input impedance reduced
X	X	X	0	X	Power Down 1 - Power shutdown mode
X	X	X	1	0	Power Down 2 - Servo mode

* AGC gain will drift at a rate determined by BYP and Hold mode discharge current.

Ts, NOMINAL WINDOW SHIFT	WSD	$\overline{WS1}$	$\overline{WS0}$
+TS3	0	0	0
+TS2	0	0	1
+TS1	0	1	0
0	0	1	1
-TS3	1	0	0
-TS2	1	0	1
-TS1	1	1	0
0	1	1	1

Note: Positive denotes a late shift, negative denotes an early shift. A late shift in the window increases the late (right) margin and decreases the early (left) margin.

TABLE 2: Decode Window Symmetry Control

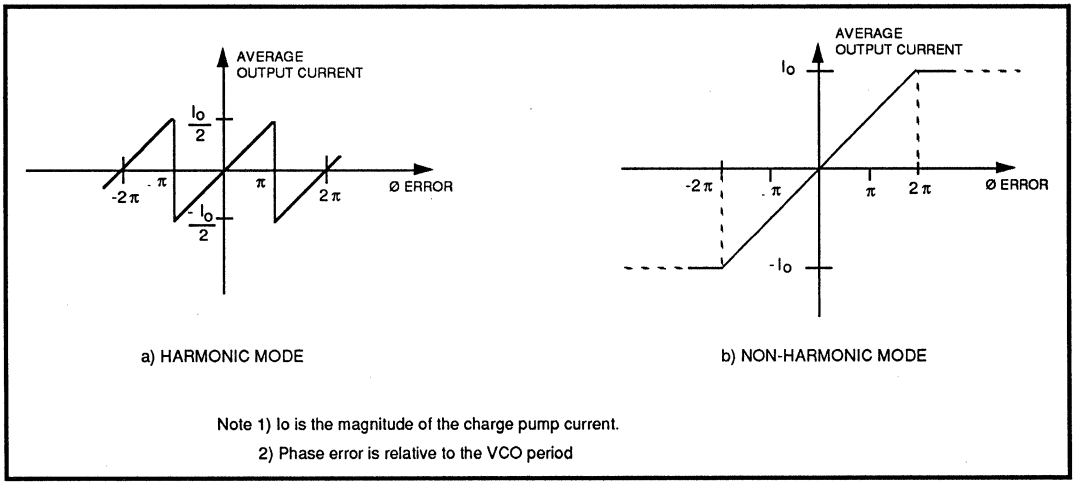


FIGURE 4: Phase Detector Transfer Function

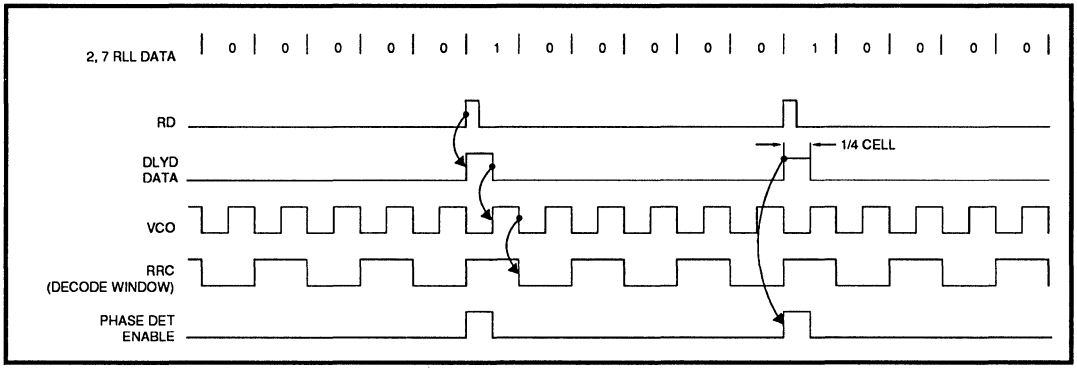


FIGURE 5: Data Synchronization Waveform Diagram

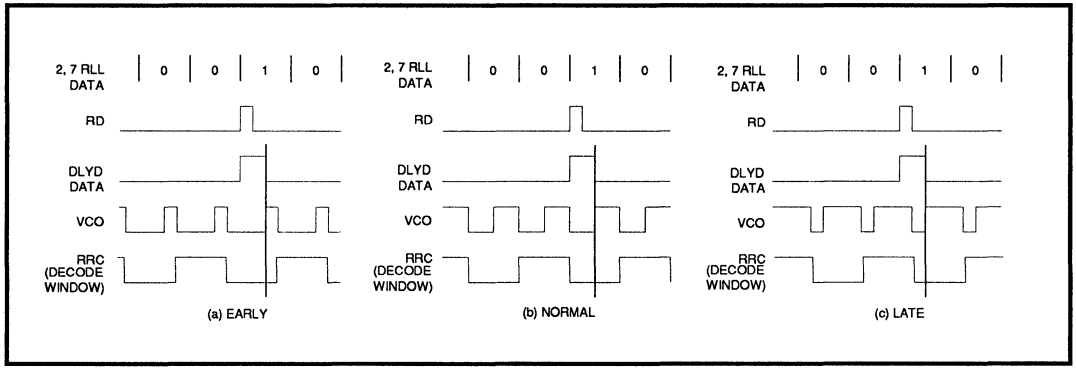


FIGURE 6: Decode Window

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
VPA1		Analog (+5V) power supply for pulse detector.
AGND1		Analog ground pin for pulse detector block.
VPA2		Analog (+5V) supply pin for data synchronizer block.
AGND2		Analog ground pin for data synchronizer block.
VPD		Digital (+5V) power supply pin.
DGND		Digital ground pin.
IN+, IN–		Analog signal input pins.
OUT+, OUT–	O	Read path AGC Amplifier output pins. Open collector output, external pull-up resistors should be added between these pins and VPA1.
DIN+, DIN– *	I	Analog input to the hysteresis comparator.
CIN+, CIN– *	I	Analog input to the differentiator.
DIF+, DIF–	I/O	Pins for external differentiating network.
COUT	O	Test point for monitoring the flip-flop clock input. Forcing this pin above 4.5V activates a test mode in which the DOUT pin becomes the input to the data synchronizer.
DOUT	O	Test point for monitoring the flip-flop D-input. In the special test mode which is controlled by COUT, this pin is the input to the data synchronizer.
$\overline{\text{RDO}}$	O	Test point for ECL like read data prior to input to the data synchronizer. This is a TTL level signal which is active during SERVO, READ, and IDLE modes.
BYP	I/O	An AGC timing capacitor or network is tied between this pin and AGND1.
AGC	I	AGC Reference: the voltage on this pin determines the reference voltage for the read data AGC loop.
LEVEL	O	Open emitter output from fullwave rectifier that may be used for input to the hysteresis comparator.
HYS	I	Hysteresis level setting input to the hysteresis comparator.
$\overline{\text{HOLD}}$	I	TTL compatible pin that holds the AGC gain when pulled low.
$\overline{\text{LATCHA}}$, $\overline{\text{LATCHB}}$	I	TTL compatible inputs that switch channel A or B into peak acquistion mode when low.
$\overline{\text{RST}}$, $\overline{\text{RSTA}}$, $\overline{\text{RSTB}}$ **	I	TTL compatible input that enables the discharge of channels A & B hold capacitors when held low.
CS***	I	Hold capacitor discharge current magnitude is controlled by a resistor from this pin to VPA1 or GND1. If left open the default current is 1.5 mA.
HOLDA, HOLDB	O	Peak holding capacitors are tied from each of these pins to AGND1.
VREF	O	Reference voltage for Servo outputs.
BURSTA, BURSTB	O	Buffered hold capacitor voltage outputs.

*In 52-pin package CIN+ will be internally bonded to DIN+, CIN- will be internally bonded to DIN-.
**$\overline{\text{RSTA}}$ and $\overline{\text{RSTB}}$ will be internally bonded to $\overline{\text{RST}}$ in 52-pin package, and separately bonded out in 68-pin package.
***Not available in 52-pin package.

PIN DESCRIPTION (Continued)

NAME	TYPE	DESCRIPTION
PES	O	Position error signal, A minus B output, offseted by VREF.
$\overline{\text{SLEEP}}$	I	Low state on this pin puts the device in a low power "off" state.
$\overline{\text{SERVO}}$	I	Low state on this pin disables all circuitry not required for use during Servo mode.
XTAL1, XTAL2	I	Crystal oscillator connections: if a crystal oscillator is not desired, XTAL1 may be driven by a TTL source with XTAL2 open.
IREF	I	Timing program pin: the VCO center frequency, Phase Detector Gain and the 1/4 cell delay are a function of the current source into pin IREF. The current is set by an external resistor, RR connected from IREF to VPA2.
FLTR	I/O	Filter pin: the phase detector output and VCO input node. The loop filter is connected to this pin.
SRD	O	Synchronized Read Data: TTL read data that has been re-synchronized to read clock.
WSD	I	Window Symmetry Direction: TTL compatible input controls the directions of the optional window symmetry shift. Pin WSD has an internal resistor pull-up.
$\overline{\text{WS0}}$	I	Window symmetry control bit: TTL compatible input, a low level introduces a window shift of 1.5% TORC (read reference clock period) in the direction established by WSD pin.
$\overline{\text{WS1}}$	I	Window Symmetry Control bit: TTL compatible input, a low level introduces a window shift of 6% TORC (read reference clock period) in the direction established by WSD. A low level at both $\overline{\text{WS0}}$ and $\overline{\text{WS1}}$ will produce the sum of the two window shifts.
$\overline{\text{WSL}}$	I	Window Symmetry Latch: used to latch the input window symmetry control bits WSD, $\overline{\text{WS0}}$, $\overline{\text{WS1}}$ into the internal DAC. An active low level latches the input bits.
RF, RS*	I	WINDOW SYMMETRY ADJUST PINS: Provides analog control over the decode window symmetry; typically used to null out any window symmetry offset. A resistor connected from either RF or RS to AGND will provide magnitude and direction control. They can be used in conjunction with the digital control port WSD, $\overline{\text{WS0}}$, $\overline{\text{WS1}}$.
RRC	O	Read/Reference Clock: a multiplexed clock source used by the controller. In the read mode, this clock is the VCO frequency divided by two (1/TORC) and in the write mode it is the crystal reference frequency divided by two (1/TORO). No short clock pulses are generated during a mode change.
SDS	I	Sync Detect Set: used to program the preamble detect timing with an external RC Network. Connect the capacitor, Cd to VPA2 and the resistor, Rd, to AGND2.
RG	I	Read gate: TTL compatible input selects the PLL reference input and initiates the PLL synchronization sequence. A high level selects the internal RD± inputs. A low level selects the crystal reference oscillator, Pin RG has an internal resistor pull-up.
WG	I	Write Gate: TTL compatible input enables the write mode. Pin WG has an internal resistor pull-up.
SDO	O	Sync Detect Output: an active high output that indicates successful detection of the preamble sync field.

*Not available in 52-pin package.

PIN DESCRIPTION (Continued)

NAME	TYPE	DESCRIPTION
WDI	I	Write Data Input, active high TTL compatible input.
$\overline{WD}$	O	Write Data: encoded write data output, active low.
PCS	I	Precomp Set: used to set the magnitude of the write pre-compensation time shift via an external capacitor, Cp to VPA2 and an external resistor, Rp to AGND2.
$\overline{EARLY}$	I	Early pin: TTL compatible input shifts Write Data pulses earlier in their relative position; $\overline{EARLY}$ and $\overline{LATE}$ cannot be active simultaneously.
$\overline{LATE}$	I	Late Pin: TTL compatible input shifts Write Data pulses later in their relative position. $\overline{LATE}$ and $\overline{EARLY}$ cannot be active simultaneously.
$\overline{DRD}$	O	DELAYED READ DATA/PLL REFERENCE: An open emitter ECL output test point. The positive edges of this signal indicate the data bit position. The positive edges of DRD and VCO CLK can be used to estimate window centering. The time jitter of DRDs positive edge is an indication of media bit shift. Two external resistors are required to observe this signal. They should be removed during normal operation for reduced power dissipation. This pin is multiplexed so that when RG is high, DRD is output and when RG is low, the PLL reference oscillator is output.
VCO CLK*	O	VCO CLK: An open emitter ECL output test point. Two external resistors are required to perform this test. They should be removed during normal operation for reduced power dissipation.

* Not available on 52-pin package

ELECTRICAL SPECIFICATIONS

Recommended conditions apply unless otherwise specified.

ABSOLUTE MAXIMUM RATINGS

Operation outside these rating limits may cause permanent damage to this device.

PARAMETER	RATING	UNIT
5V Supply Voltage, VPA1, VPA2, VPD	6.0	V
Pin Voltage (Analog pins)	-0.3 to VPA1, 2 + 0.3	V
Pin Voltage (All others)	-0.3 to VPD + 0.3 or +12 mA	V
Storage Temperature	65 to 150	°C
Lead Temperature (Soldering 10 sec.)	260	°C

RECOMMENDED OPERATING CONDITIONS

Currents flowing into the chip are positive.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Supply Voltage (VPA1, 2 & VPD)		4.75	5.0	5.25	V
Tj Junction Temperature		25		135	°C

POWER SUPPLY

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
IVPA1, 2 IVPD	Supply Current	Outputs unloaded; $\overline{SLEEP}$, $\overline{SERVO}$ = high or open			80	mA
Pd	Power dissipation	Ta = 25°C, outputs unloaded		400	500	mW
		$\overline{SLEEP}$ = low, Outputs unloaded		3	5	mW
		$\overline{SERVO}$ = low, $\overline{SLEEP}$ = high Outputs unloaded		200	250	mW

LOGIC SIGNALS

* Output load is a 4K resistor to 5V and a 10 pF capacitor to DGND.

VIL	Input Low Voltage		-0.3		0.8	V
VIH	Input High Voltage		2.0		VCC+0.3	V
IIL	Input Low Current	VIL = 0.4V	0.0		-0.4	mA
IIL	WG Input Low Current	VIL = 0.4V	0.0		-0.8	mA
IIH	Input High Current	VIH = 2.7V			100	µA
VOL	Output Low Voltage	IOL = 4.0 mA			0.5	V
VOH	Output High Voltage	IOH = -400 µA	2.7			V
VIHX	XTAL1 Input High Voltage		2.6			V
VILX	XTAL1 Input Low Voltage				1.4	V
VOHT	Test Poin Output High Voltage for DRD and VCO CLK	261Ω to VPD, 420Ω to DGND		4.2		V
VOLT	Test Point Output Low Voltage for DRD and VCO CLK			3.6		V
VTIH	Input High Level Input Voltage at COUT pin.	Activates sync test mode. VPA2 = 5.02V	4.8			V
VTIL	Input Low Level Input Voltage at COUT pin.	De-activates sync test mode. VPA2 = 5.0V			4.2	V
RDIH	Input High Level Input Voltage at DOUT pin.	Drives data synchronizer in in sync test mode. VPA2 = 5.0V	4.8			V
RDIL	Input Low Level Input Voltage at DOUT pin.				4.2	V

MODE CONTROL

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
TDRW	Read to Write Transition Time	WG pin low to high			1.0	µs
TDWR	Write to Read Transition Time	WG pin high to low AGC setting not included	0.5	0.9	1.3	µs
TDH	$\overline{\text{HOLD}}$ On to/from $\overline{\text{HOLD}}$ Off Transition Time	$\overline{\text{HOLD}}$ pin high to/from low			1.0	µs
TDRG	RG Time Delay				100	ns
TDSL	Power Shutdown Mode to/from Read/Write delay time.	Settling time of external capacitors not included. XTAL1 driven by external TTL source.		50		µs
TDOFF	Read/Write Mode to power shutdown mode delay time.	Settling time of external capacitors not included		2000		µs
TDSLX	Power shutdown mode to/from Read/Write delay time.	Including XTAL oscillator turn on/off settling time		500		mS
TDSE	Servo mode to/from Read/Write delay time.	Settling time of external capacitors not included			20	µs
PWIMS	Low Input Impedance Pulse Width	WG pin high to low. Not directly testable.		0.9		µs
PWFDC	Fast Discharge Pulse Width	Follows the end of the IMS pulse. Not directly testable.		0.9		µs

READ MODE WG is low

AGC AMPLIFIER

Unless otherwise specified, recommended operating conditions apply. Input signals, 100 mVppd at 2.5 MHz, are AC coupled to IN±. OUT± are loaded differentially with >340Ω x 2, and each side is loaded with < 10 pF to AGND, and AC coupled to DIN±. A 2000 pF capacitor is connected between BYP and AGND. AGC pin is open.

GR	Gain Range	1.0 Vp-p ≤ (OUT+) - (OUT-) ≤ 3.0 Vp-p	4		80	V/V
VOS	Output Offset Voltage Variation	Over entire gain range	-200	0	+200	mV
VOMX	Maximum Output Voltage Swing	Set by BYP pin	3.0			Vp-p
RIN	Differential Input Resistance	(IN+) - (IN-) = 100 mVp-p @ 2.5 MHz		5.0		kΩ
CIN	Differential Input Capacitance	(IN+) - (IN-) = 100 mVp-p @ 2.5 MHz			10	pF

AGC AMPLIFIER (Continued)

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
ZCMH	Single Ended Input	WG = low, IN+ or IN-		1.8		kΩ
	Impedance	WG = high, IN+ or IN-			250	Ω
VN	Input Noise Voltage	Gain set to maximum			15	$nV/\sqrt{Hz}$
BW	Bandwidth	Gain set to maximum referenced to 2.5 MHz	32			MHz
IOUT	OUT+ & OUT- Pin Current	No DC path to AGND	2			mA
CMRR	Input Referred Common Mode Rejection Ratio	(IN+) = (IN-) = 100 mVp-p @ 2..5 MHz, gain set to max	40			dB
PSRR	Input Referred Power Supply Rejection Ratio	VPA1, 2 = 100 mVp-p @ 2.5 MHz, gain set to max	30			dB
KAGC	(DIN+) - (DIN-) Input Swing vs. AGC Input	25 mVp-p ≤ (IN+) - (IN-) ≤ 250 mVp-p, $\overline{HOLD}$ = high, 0.5 Vp-p ≤ (DIN+) - (DIN-) ≤ 1.5 Vp-p	0.9	1.0	1.1	Vp-p/V
ΔDIN	(DIN+) - (DIN-) Input Voltage Swing Variation	25 mVp-p ≤ (IN+) - (IN-) ≤ 250 mVp-p			6.0	%
VAGC	AGC Voltage	AGC open	0.8	1.0	1.2	V
RAGC	AGC Pin Input Impedance		4.4	5.5	6.6	kΩ
ISD	Slow AGC Discharge Current	(DIN+) - (DIN-) = 0V	4	4.5	6	μA
IFD	Fast AGC Discharge Current	Starts at 0.9 μs after WG goes low, stops at 1.8 μs after WG goes low	0.10	0.12	0.14	mA
ILK	AGC Leakage Current	$\overline{HOLD}$ = low	-0.2	0	+0.2	μA
ISC	Slow AGC Charge Current	(DIN+) - (DIN-) = 0.8 VDC, vary AGC until slow charge begins	-0.12	-0.18	-0.24	mA
IFC	Fast AGC Charge Current	(DIN+) - (DIN-) = 0.8 VDC, V_{AGC} = 3.0V	-0.9	-1.3	-1.7	mA
FSSP	Fast to Slow Attack Switchover Point	$\frac{[(DIN+)-(DIN-)]}{[(DIN+)-(DIN-)]FINAL}$		125		%

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AGC AMPLIFIER (Continued)

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
TGD	Gain Decay Time (Td)	(IN+) - (IN-) = 250 mVp-p to 125 mVp-p @ 2.5 MHz, (OUT+) - (OUT-) to 90% final value		12		µs
		(IN+) - (IN-) = 50 mVp-p to 25 mVp-p at 2.5 MHz (OUT+) - (OUT-) to 90% final value		60		µs
TGA	Gain Attack Time	WG = high to low (IN+) - (IN-) = 250 mVp-p @ 2.5 MHz, (OUT+) - (OUT-) to 110% final value		2		µs

WRITE MODE WG is high

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
ZCML	Common Mode Input Impedance			250		Ω

HYSTERESIS COMPARATOR

Unless otherwise specified, recommended operating conditions apply. Input (DIN+) - (DIN-) is an AC coupled, 1.0 Vp-p, 2.5 MHz sine wave. 0.5 VDC is applied to the HYS pin. WG pin is low.

IRHC	Input Signal Range				1.5	Vp-p
RHCD	Differential Input Resistance	(DIN+) - (DIN-) = 100 mVp-p @ 5 MHz	12.5	15	17.5	kΩ
CHCD	Differential Input Capacitance	(DIN+) - (DIN-) = 100 mVp-p @ 5 MHz			5.0	pF
RHCC	Single Ended Input Impedance (Both Sides)		3	4	5	kΩ
KLD	Level Pin Output Voltage vs. (DIN+) - (DIN-)	0.6 Vp-p < (DIN+) - (DIN-) < 1.5 Vp-p, 10kΩ between LEVEL and AGND1	0.75	1	1.25	V/Vp-p
VLOS	Level Pin Output Offset Voltage	10kΩ between LEVEL and AGND1		TBD		mV
ZLV	Level Pin Output Impedance	I_{LEVEL} = 0.2 mA		250		Ω
ILMX	Level pin Maximum Output Current		1.5			mA
KHYS	Hysteresis Voltage at DIN± vs. HYS Pin Voltage	0.3 V < HYS < 1.0V		0.36		V/V

HYSTERESIS COMPARATOR (Continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
IHYS	HYS Pin Current	0.5 V < HYS < 1.5V	0.0		-10	µA
VHCOS	Comparator Offset Voltage	HYS pin at AGND ≤ 1.5 kΩ across DIN±			5.0	mV
VDOL	DOUT Pin Output Low Voltage	5 kΩ from DOUT to GND		VPA2 -2.8		V
VDOH	DOUT Pin Output High Voltage	5 kΩ from DOUT to GND		VPA2 -2.4		V

ACTIVE DIFFERENTIATOR

Unless otherwise specified, recommended operating conditions apply. Input (CIN+) - (CIN-) is an AC-coupled, 1.0 Vp-p, 2.5 MHz sine wave. 100Ω in series with 65 pF are tied from DIF+ to DIF-.

IRAD	Input Signal Range				1.5	Vp-p
RADD	Differential Input Resistance	(CIN+) - (CIN-) = 100 mVp-p @ 5 MHz	12.5	15.0	17.5	kΩ
CADD	Differential Input Capacitance	(CIN+) - (CIN-) = 100 mVp-p @ 5 MHz			5.0	pF
RADC	Single Ended Input Impedance	Both sides	3.0	4.0	5.0	kΩ
KAD	Voltage Gain from CIN± to DIF±	3.5kΩ from DIF+ to DIF-		1		V/V
IDIF	DIF+ to DIF- Pin Current	Differentiator impedance must be set so as not to clip the signal for this current level	±0.7			mA
VADOS	Comparator Offset Voltage	DIF+, DIF- are AC-coupled		0	5.0	mV
VCOL	COUT Pin Output Low Voltage	5 kΩ from COUT to GND		VPA2 -2.8		V
VCOH	COUT Pin Output High Voltage	5 kΩ from COUT to GND		VPA2 -2.4		V
PWC	COUT Pin Output Pulse Width			30		ns

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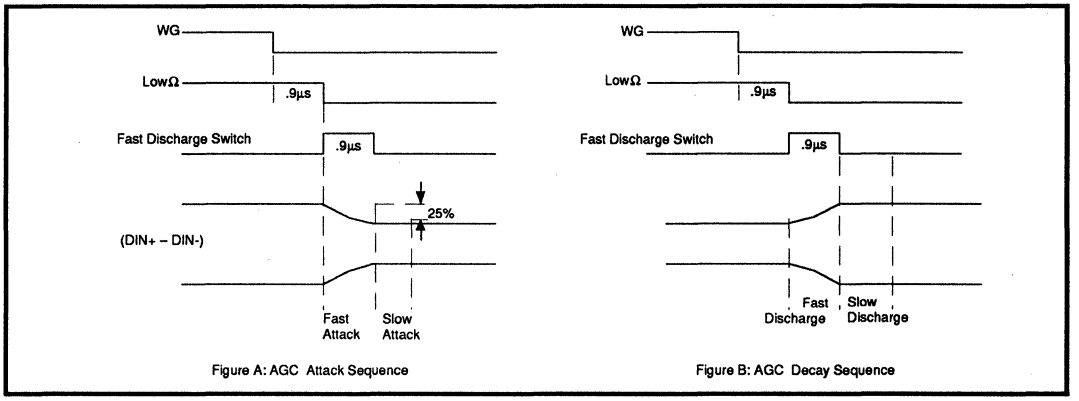

FIGURE 7: AGC Timing Diagram

QUALIFIER TIMING (See Figure 8)

Unless otherwise specified, recommended operating conditions apply. Inputs (CIN+) - (CIN-) and (DIN+) - (DIN-) are in-place as a coupled, 1.0 Vp-p, 2.5 MHz sine wave. 100Ω in series with 65 pF are tied from DIF+ to DIF-. 0.5V is applied to the HYS pin. COUT, DOUT and RD has a 5 kΩ pull-down resistor (for test purposes only.) WG pin is low.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TD1	D Flip-Flop Set Up Time	Minimum allowable time delay from (DIN+) - (DIN-) exceeding hysteresis point to (DIF+) - (DIF-) hitting a peak value.	0			ns
TD3	Propagation Delay from Positive Peak to $\overline{RDO}$ Pulse			15		ns
TD4	Propagation Delay from Negative Peak to $\overline{RDO}$ Output Pulse			15		ns
PP	|TD3-TD4| Pulse Pairing				1.0	ns
TRD0	$\overline{RDO}$ Pulse Width		24	32	41	ns

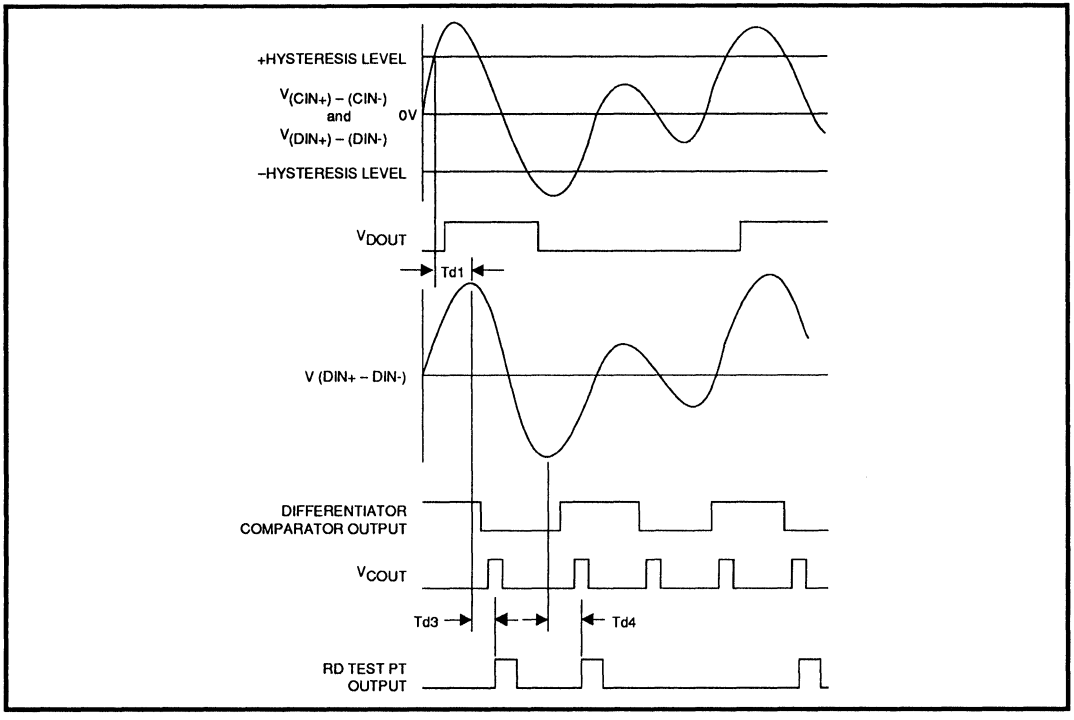

FIGURE 8: Read Mode Digital Section Timing Diagram

SERVO SECTION (Unless otherwise specified, recommended operating conditions apply.)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VREF	Reference Voltage Range Output			2.0		V
KBD	BURSTA/B Pin Output Voltage vs (DIN+) - (DIN-)	$\overline{LATCHA/B}$ = Low $\frac{V_{BURSTA/B} - VREF}{(DIN+) - (DIN-)}$		1.0		V/Vp-p
BVOS	BURSTA/B Output Offset Voltage, V_{BURST} - VREF	$\overline{LATCHA/B}$ = Low, (DIN+) = (DIN-)	-50		+50	mV
BVM	BURSTA - BURSTB Output Offset Match	$\overline{LATCHA/B}$ = low (DIN+) = (DIN-)	-10		+10	mV
RO	Output Resistance, BURSTA/B, PES				20	Ω

SERVO SECTION (Continued)
(Unless otherwise specified, recommended operating conditions apply.)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VOPE	PES Pin Output Offset Voltage	V_{BURSTA} - V_{BURSTB} +VREF (DIN+) = (DIN-), $\overline{LATCHA/B}$ =Low	-10		+10	mV
IDC	HOLDA/B Discharge Current	$\overline{RST}$ = low,		1.5		mA
ILC	HOLDA/B Leakage Current	$\overline{RST}$ = high, $\overline{LATCHA/B}$ = high	-0.5		+0.5	µA
RL	Load Resistance, BURSTA/B, PES	Resistors to VREF	10.0	20.0		kΩ
CL	Load Capacitance, BURSTA/B, PES				20	pF
STSU	$\overline{LATCHA/B}$ Pin Set Up Time	TDS1, Figure 14	150			ns
STH	$\overline{LATCHA/B}$ pin Hold Time	TDS2, Figure 14	150			ns
TDON	Channel A/B Discharge Current Turn On Time	$\overline{RST}$ high → low			150	ns
TDOFF	Channel A/B Discharge Current Turn Off Time	$\overline{RST}$ low → high			150	ns

SYNCHRONIZER SECTION

WRITE MODE (See Figure 9)

PARAMETER		CONDITIONS	MIN	MAX	UNIT
TWD	Write Data Pulse Width	CL ≤ 15 pF	(TORC/2)-12 -1.65 TPCO -TPC -12	(TORC/2)+12 -1.65 TPCO -TPC +12	ns
TFWD	Write Data Fall Time	2.0V to 0.8V, CL ≤ 15 pF		8	ns
TSWD	Write Data Input Setup Time	Either edge of WDI to either edge of RRC	15		ns
THWD	Write Data Input Hold Time	Either edge of RRC to either edge of WDI	3		ns
TSP	$\overline{EARLY/LATE}$ Input Setup Time	Falling edge of $\overline{EARLY}$/ $\overline{LATE}$ to either edge of RRC	15		ns
THP	$\overline{EARLY/LATE}$ Input Hold Time	Rising edge of $\overline{EARLY}$/ $\overline{LATE}$ to either edge of RRC	10		ns
TPC	Precompensation Time Shift Magnitude Accuracy	TPCO = 0.155 Rp Cp Rp = 1K to 2K	0.8TPC0	1.2TPC0	ns

READ MODE

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TRRC	Read Clock Rise Time	0.8V to 2.0V, CL ≤ 15 pF			8	ns
TFRC	Read Clock Fall Time	2.0V to 0.8V, CL ≤ 15 pF			5	ns
TSRD	Read Data Pulse Width		(TORC/2)-2	TORC/2	(TORC/2)+2	ns
TRSRD	Read Data Rise Time	0.8V to 2.0V, CL ≤ 15 pF			10	ns
TFSRD	Read Data Fall Time	2.0V to 0.8V, CL ≤ 15 pF			8	ns
TPSRD	SRD Output Setup/HoldTime		-15		15	ns
TD	1/4 Cell + 1F Detect Delay, Excluding External Capacitor and Resistor Tolerances	TD = 3.31 (RR + Z) + 0.1 • Rd (Cd + Cs) RR = 2.7k to 8k Rd = 10k to 20k Cd = 62pF to 100 pF Cs = stray capacitances	0.89 TD	TD	1.11 TD	ns
TDS	1/4 Cell + 1F Detect	Stability over temperature and supply	-4		+4	%

WINDOW SYMMETRY CONTROL CHARACTERISTICS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TWSS	$\overline{WS0}$, $\overline{WS1}$, WSD Set Up Time		50			ns
TWSH	$\overline{WS0}$, $\overline{WS1}$, WSD Hold Time		0			ns

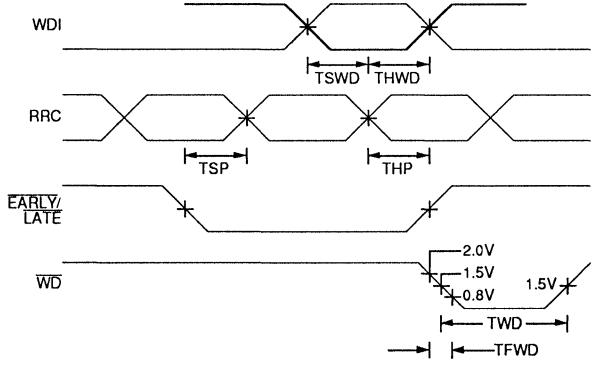

FIGURE 9: Write Mode Timing

DATA SYNCHRONIZATION

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TVCO	VCO Center Frequency Period	VCO IN = 2.7V TO = 6.621 (RR + 2) VPA2 = 5.0V TO (ns) RR (kzΩ) 2.7kΩ < RR < 8kΩ	0.8TO	TO	1.2TO	sec
VDR	VCO Frequency Dynamic Range	1.0V ≤ VCO IN ≤ VPA2-0.6V VPA2 = 5.0V	±27	±34	±40	%
KVCO	VCO Control Gain	ωo = 2π / TO VCO In = 2.7V	0.14 ωo	±0.17 ωo	0.20 ωo	rad/s V
KD	Phase Detector Gain	KD = 0.62 / (RR+527) VPA2 = 5.0V, 2.7kΩ < RR < 8kΩ	0.83 KD	KD	1.17 KD	A/rad
*KPA	KVCO x KD Product Accuracy		-28	0	+28	%
*PRE	VCO Phase Restart Error			4		ns
DWCA	Decode Window Centering Accuracy		-0.01 TORC -2		0.01 TORC + 2	ns
DW	Decode Window		(TORC/2) -2			ns
TS1	Decode Window Time Shift Magnitude	TS1 = 0.015 TORC $\overline{WSO}$ = 0; $\overline{WSI}$ = 1		TWS1		ns
TS2	Decode Window Time Shift Magnitude	TS2 = 0.06 TORC $\overline{WSO}$ = 1; $\overline{WSI}$ = 0		TWS2		ns
TS3	Decode Window Time Shift Magnitude	TS3 = 0.075 TORC $\overline{WSO}$ = 0; $\overline{WSI}$ = 0		TWS3		ns
TSA	Decode Window Time Shift Magnitude	$TWSA = 0.12 \text{ TORC} \cdot \left(1 - \frac{2RR+5}{1440+8}\right)$		TWSA		ns

* Not directly testable; design characteristics

MISCELLANEOUS TIMNG

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
RWTD	RG, WG Time Delay				100	ns

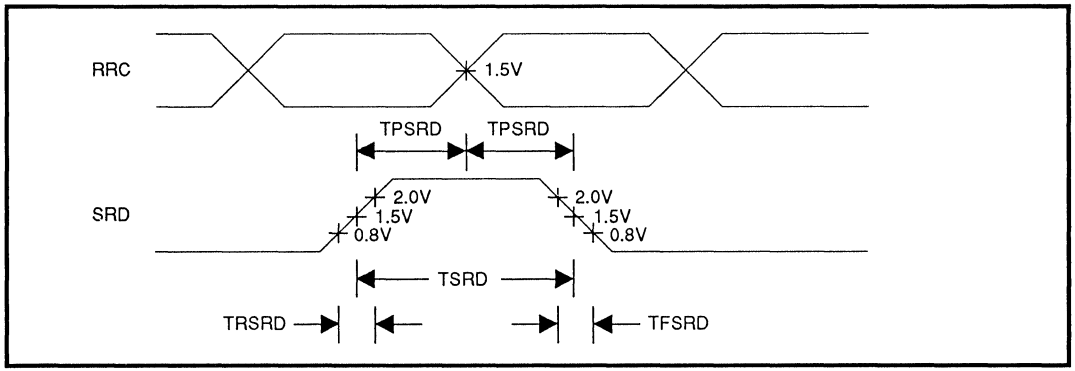

FIGURE 10: Read Mode Timing

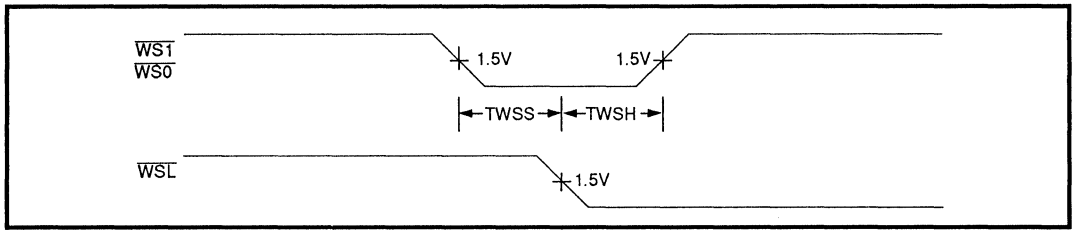

FIGURE 11: Window Symmetry Control Timing

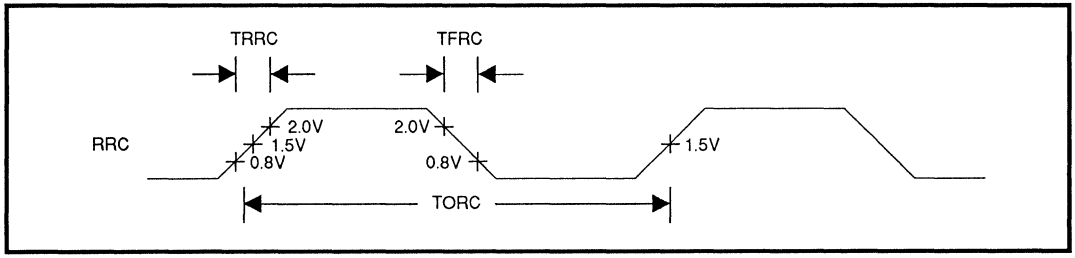

FIGURE 12: RRC Timing

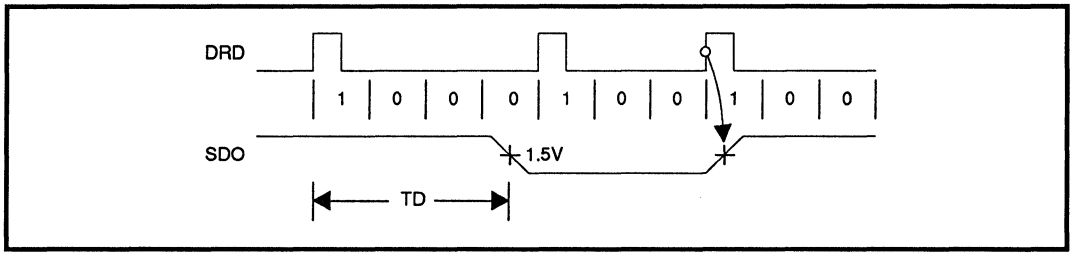

FIGURE 13: SDO Timing

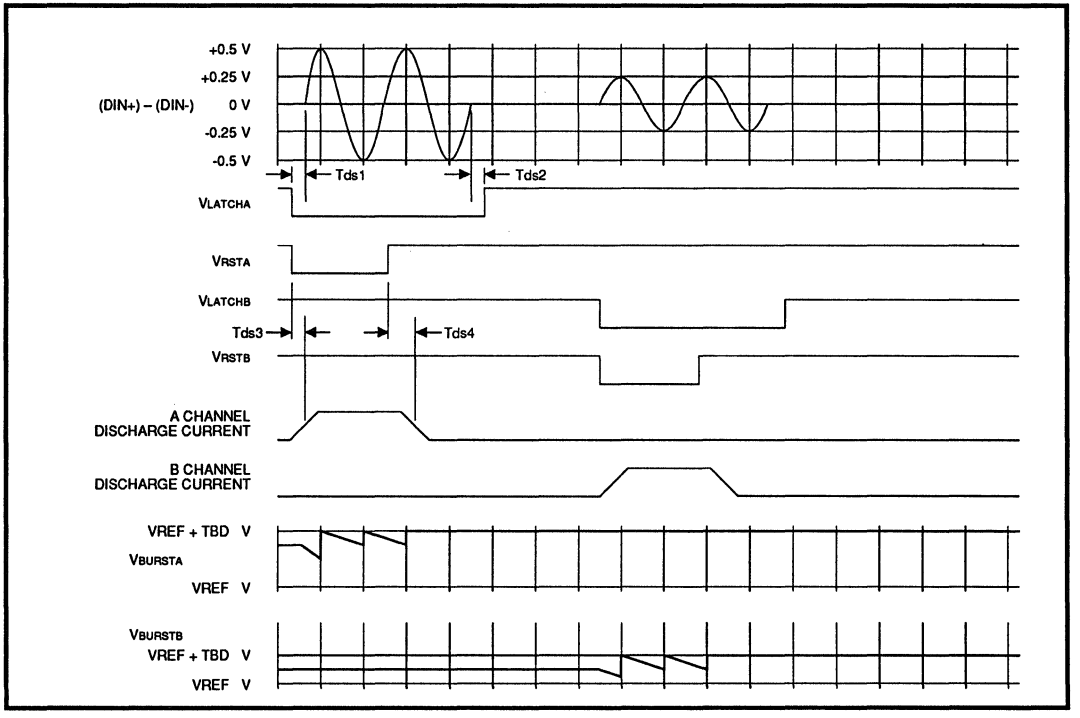

FIGURE 14: Servo Read Mode Timing

APPLICATIONS INFORMATION

The SSI 32P5481/5482 PLL uses a new architecture which incorporates an accurate quarter cell delay circuit. The standard architecture of a data synchronizer PLL is shown in Figure17A. In read mode, the rising edge of the quarter cell delay enables the phase detector, and the falling edge is locked to the VCO. Ideally, the quarter cell delay enables the phase detector one half of an encoded bit cell time before the phase comparison takes place. A data bit could then shift early or late by one half of an encoded bit cell time before a phase detector output error would occur. If the quarter cell delay is not exactly one half of an encoded bit cell time, a phase detector error will occur when the read data shifts by an amount that is smaller than one half of and encoded bit cell time when shifting in one direction and an amount larger than one half of an encoded bit cell time in the other direction. In addition, when an error occurs, the resulting charge pump output goes from maximum output one way to maximum output the other way. This can cause loss of lock to occur. The timing is shown in Figure 18.

The 32P5481/5482 achieves an accurate quarter cell delay time by using the VCO control voltage to compensate the quarter cell delay one-shot circuit for process, temperature and power supply induced timing variations. The modified architecture of the 32P5481/5482 data synchronizer is shown in Figure 19B. Because the quarter cell delay timing is adjusted by the VCO control voltage, there is an effect on the PLL transfer function due to the new quarter cell delay circuit.

The quarter cell delay circuit produces a time delay output in response to a voltage input. In order to include this function in a phase-locked loop, the time delay function must be converted into a phase function. This is straightforward, since a time delay is equivalent to a phase angle. The equivalent phase representation of the quarter cell delay is derived below.

For the VCO:

$$K_o = \frac{d\omega_o}{dV} \qquad (1a)$$

$$\frac{dT_o}{dV} = \frac{d}{dV}\left(\frac{1}{f_o}\right) = -\frac{1}{f_o^2}\frac{df_o}{dV} = -T_o^2\frac{df_o}{dV} = -\frac{T_o^2}{2\pi}\frac{dw_o}{dV} \qquad (1b)$$

where:

K_0 = VCO gain
ω_0 = VCO center frequency (rad/s)
f_0 = VCO center frequency (Hz)
T_0 = VCO center frequency (sec)

For the quarter cell delay,

$$K_T = \frac{dq_o}{dV} = \frac{2\pi}{T_o}a\frac{dT_o}{dV} = -\alpha T_o\frac{dw_o}{dV} = -\alpha T_o K_o$$

where:

θ_0 = Phase due to quarter cell delay circuit
T_0 = VCO center frequency period
T_Q = Quarter cell delay time
$\alpha = T_Q/T_0 = 0.5$ for the 32P5481/5482

The gain of the quarter cell delay block is constant in the 32P5481/5482, regardless of the values of other components.

For the 32P5481/5482, the nominal value of K_T is 0.17π.

PLL TRANSFER FUNCTION

There are two modes of operation of the PLL, and two transfer functions. In write and idle modes, the PLL is locked to the reference oscillator, and the quarter cell delay does not enter into the transfer function. In read, mode, the PLL is locked to read data, and the quarter cell delay is included in the transfer function. In addition, the effective loop gain of the PLL increases in idle mode due to the phase detector. This will be explained later in more detail.

The transfer functions for read and idle modes are given in (3) and (4), respectively.

$$\frac{\theta_0(s)}{\theta_r(s)} = \frac{\frac{nK_0K_dF(s)}{S}}{1+nK_TK_dF(s)+\frac{nK_0K_dF(s)}{S}} \qquad (3)$$

$$\frac{\theta_0(s)}{\theta_r(s)} = \frac{\frac{nK_0K_dF(s)}{S}}{1+\frac{nK_0K_dF(s)}{S}} \qquad (4)$$

where:

K_T = Quarter cell delay one-shot gain
K_o = VCO gain
K_d = Phase detector gain
F(s) = Loop filter transfer function
n = Ratio of input freq. to reference freq.

In (3) the K term in the denominator is a result of the quarter cell delay. Substituting $K_T = \alpha K_o T_o$ into (3),

$$\frac{\theta_o(s)}{\theta_r(s)} = \frac{\frac{nK_oK_dF(s)}{S}}{1+(1-s\alpha T_o)\frac{nK_oK_dF(s)}{S}}$$

The additional $-s\alpha T_o$ term in the denominator due to the quarter cell delay introduces positive feedback. However, the gain of the positive feedback is always less than one, so there is no instability. The additional term is not always negligible, and must be taken into account in the loop analysis and design.

Two loop filter configurations, shown in Figure 15, will be considered. Both filters result in a second order type 2 loop transfer function, with only minor differences in the loop equation.

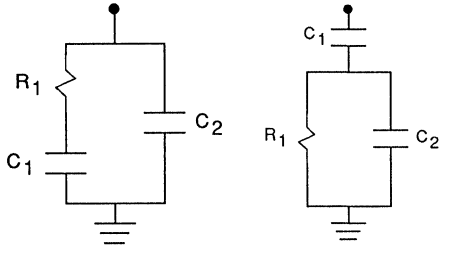

FIGURE 15: Loop Filter

The transfer function of the loop filter for a charge-pump PLL is the transimpedance, $V_o/I_i(s)$, where $V_o(s)$ is the output voltage, and $I_i(s)$ is the input current. The transfer functions of (a) and (b) are given by:

$$F_a(s) = \frac{sR_1C_1+1}{s(C_1+C_2)\left(sR_1\frac{C_1C_2}{C_1+C_2}+1\right)} \quad (6)$$

$$F_b(s) = \frac{sR_1(C_1+C_2)+1}{sC\left(sR_1C2+1\right)} \quad (7)$$

For loop filter (a), C is normally chosen to be much smaller than C so that it does not affect the loop transfer function significantly. Assuming the C » C and sRC « 1 at the frequencies of interest, (6) reduces to:

$$F_a(s) = \frac{sR_1C_1+1}{sC_1} \quad (8)$$

For loop filter (b), C is normallly chosen to be much smaller than C, so that it does not affect the loop transfer function significantly. Assuming the C » C and that sRC « 1 at the frequencies of interest, (7) reduces to:

$$F_b(s) = \frac{sR_1C_1+1}{sC_1} \quad (9)$$

Equations (8) and (9) are the same, and either loop filter may be used. Substituting (8) into (3) gives:

$$\frac{\theta_o(s)}{\theta_r(s)} = \frac{\frac{nK_oK_d}{C_1(1-\alpha T_onK_oK_dR_1)}(sR_1C_1+1)}{s^2+s\frac{nK_oK_d}{1-\alpha T_onK_oK_dR_1}\left(R_1-\frac{\alpha T_o}{C_1}\right)+\frac{nK_oK_d}{C_1(1-\alpha T_onK_oK_dR_1)}} \quad (10)$$

This is in the form of a standard second order transfer fucntion. The denominator has the form:

$$D(s) = s^2 + 2\zeta\omega_n s + \omega_n^2 \quad (11)$$

where: ζ = damping factor
ω_n = natural frequency

The damping factor and natural frequency of (10) can be extracted:

$$\omega_n = \sqrt{\frac{nK_oK_d}{C_1(1-\alpha T_onK_oK_dR_1)}} \quad (12)$$

$$\zeta = \frac{R_1-\frac{\alpha T_o}{C_1}}{2}\sqrt{\frac{nK_oK_dC_1}{1-\alpha T_onK_oK_dR_1}} \quad (13)$$

Substituting (8) into (4) gives the transfer function for idle mode:

$$\frac{\theta_o(s)}{\theta_r(s)} = \frac{\frac{nK_oK_d}{C_1}(sR_1C_1+1)}{s^2+s(nK_oK_dR_1)+\frac{nK_oK_d}{C_1}} \quad (14)$$

Again, this is in the form of a second order transfer function. The damping factor and natural frequency are found to be:

$$\omega_n = \sqrt{\frac{nK_oK_d}{C_1}} \quad (15)$$

$$\zeta = \frac{R_1}{2}\sqrt{nK_oK_dC_1} \quad (16)$$

To design the loop for proper read mode operation using (12) and (13), R, and C, must be found in terms of the damping factor and natural frequency.

To do this, first find ζ/ω_n, then solve for R_1C_1.

$$R_1C_1 = \frac{2\zeta}{\omega_n} + \alpha T_o \quad (17)$$

Substitute this value for R_1C_1 into the equation for ω_n and solve for C_1.

$$C_1 = \frac{nK_oK_d}{\omega_n^2} + \alpha T_o nK_oK_d\left(\frac{2\zeta}{\omega_n} + \alpha T_o\right) \quad (18)$$

Now that C_1 is known, R_1 can be found by dividing (17) through by C_1.

$$R_1 = \left(\frac{2\zeta}{\omega_n} + \alpha T_o\right)\frac{1}{C_1} \quad (19)$$

EXAMPLE 1

Assume that the data rate is 10 Mbit/s, a 3T preamble pattern is used, and that $\omega_n = 10^6$ and $\zeta = 0.707$ are desired.

For the SSI 32P5481/5482:

$R_R = 50/DR - 1.7\ k\Omega$
$K_o = 0.17\omega_o = 21.4 \cdot 10^6$
$K_d = 0.62/(R_R+500) = 160 \cdot 10^6$
$K_T = 0.17\pi = 0.534$

Due to the 3T preamble pattern, the input frequency is one third the VCO frequency, so n = 1/3.

$\omega_o = 2\pi(2 \cdot 10^7)$, $\alpha = 0.5$, and $T_o = 1/(20 \cdot 10^6) = 50$ ns
$C_1 = 1160\ pF + 41.9\ pF = 1.21\ nF$
$R_1 = 1.20\ k\Omega$

The resulting loop filter is shown in Figure 16.

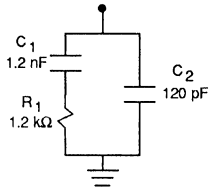

FIGURE 16

The value of $C_2 = C_1/10$ is chosen to damp out transients on the FILT pin and meet the requirement $C_2 \ll C_1$.

When the loop locks to the reference oscillator in idle mode, the loop transfer function is given by (14), and ω_n and ζ are given by (15) and (16). R_1 and C_1 from Example 1 can be substituted into these equations to find the resulting natural frequency and damping factor in idle mode.

EXAMPLE 2

When locking onto the reference oscillator, the input frequency is the same as the VCO frequency, so n = 1. Using the values of R_1 and C_1 found in Example 1, the values of ω_n and ζ when locking to the reference oscillator are found to be:

$\omega_n = 1.7 \cdot 10^6$ rad/s
$\zeta = 1.23$

5

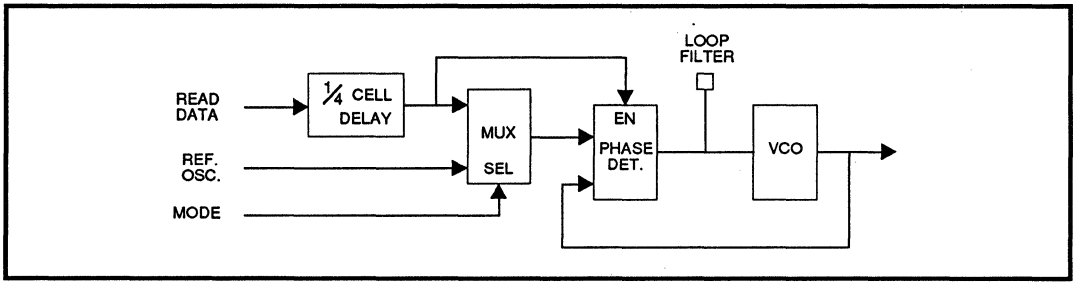

FIGURE 17A: Standard Configuration of a Data Synchronizer Phase-Locked Loop

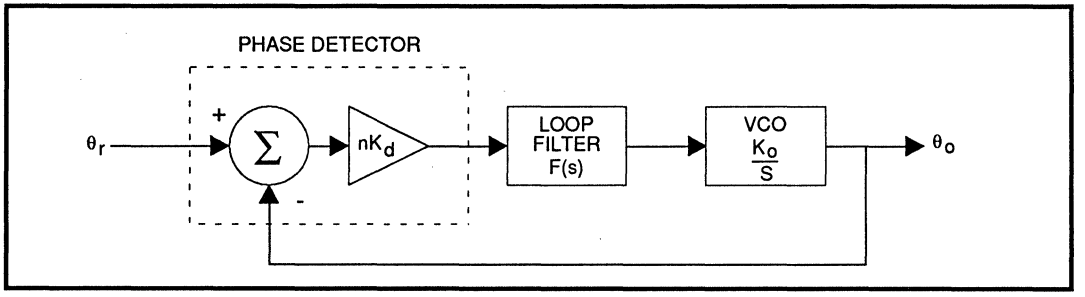

FIGURE 17B: Phase-Lock Loop System Representation

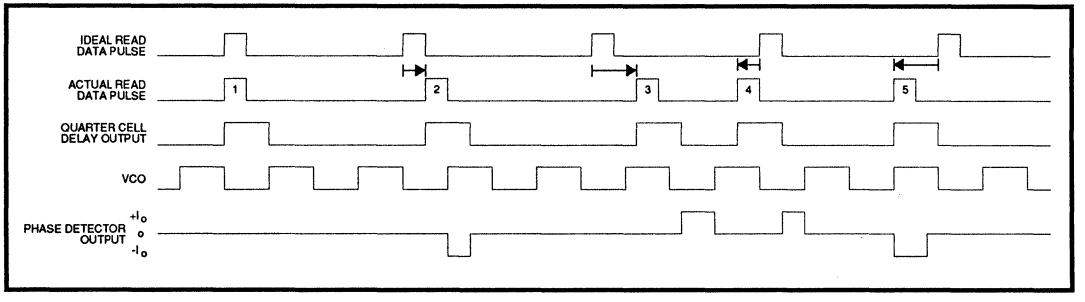

FIGURE 18A: Phase Detector Timing with Ideal Quarter Cell Delay. For an ideal pulse (1), there is no phase detector output. When a pulse is shifted late (2) or early (4) by less than the quarter cell delay time, the phase detector output is negative or positive, respectively. When the read data is shifted late (3) or early (5) by more than the quarter cell delay time, a phase detector output polarity error occurs. In this case, the output polarity becomes positive for a late shifted pulse and negative for an early shifted pulse.

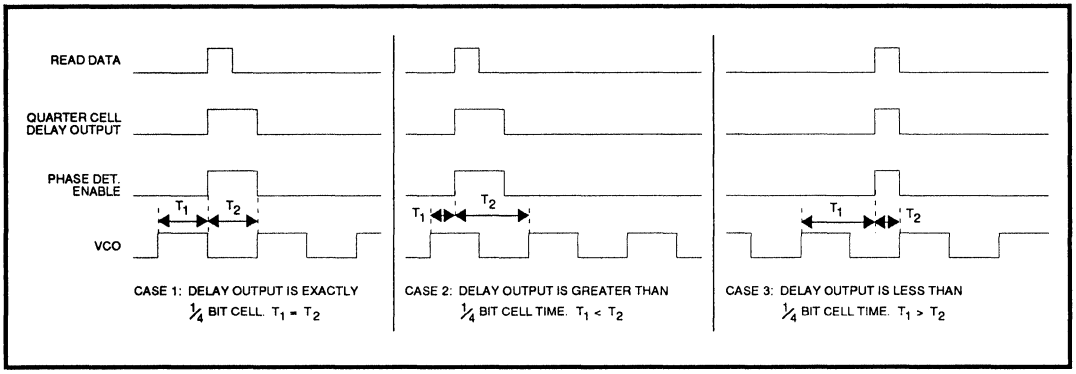

FIGURE 18B: Timing of Phase Detector Enable Logic. The read data input pulse can shift to the left by T1 and to the right by T2 before an error occurs in the phase detector output polarity, If the quarter cell delay output is not exactly 1/4 bit cell wide, then T1 ≠ T2, as shown in cases 2 and 3.

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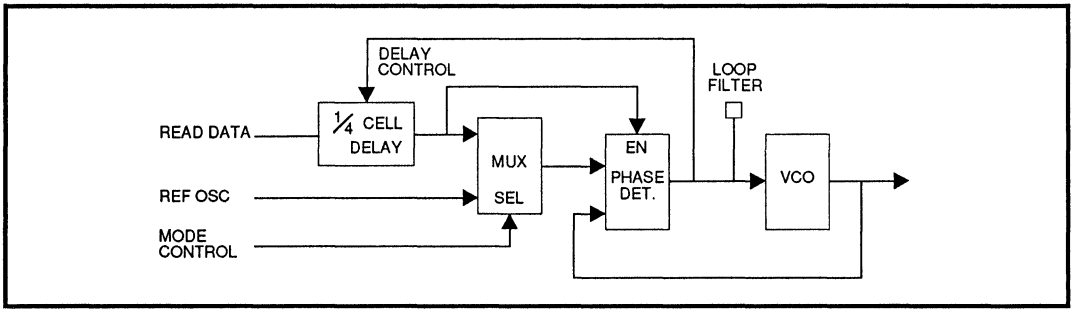


FIGURE 19A: Modified Data Synchronizer Phase-Locked-Loop with Quarter Cell Delay Control

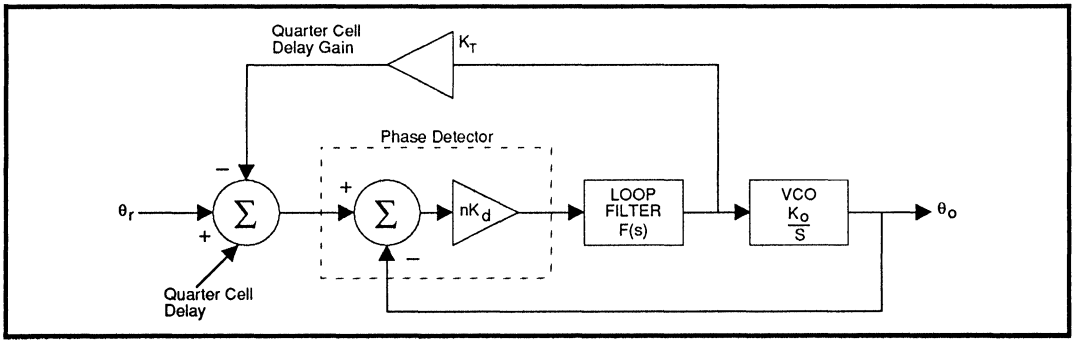
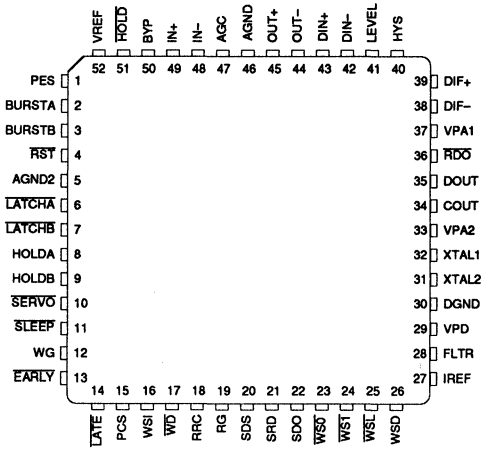


FIGURE 19B: Modified Data Synchronizer System Representation

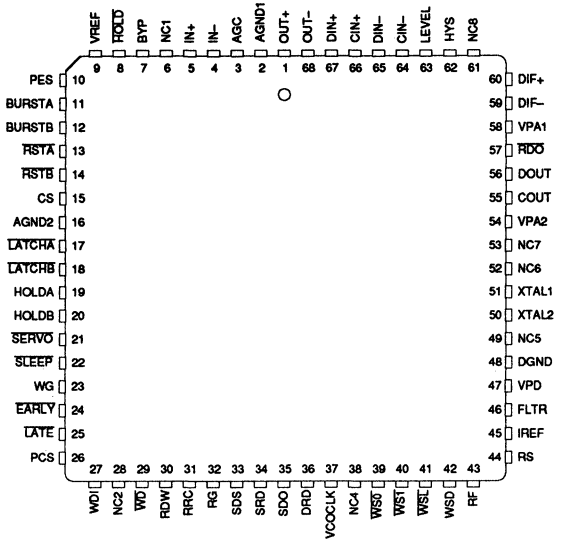
SSI 32P5481/5482
Pulse Detector & Data Synchronizer

PACKAGE PIN DESIGNATIONS

(Top View)



52-Pin QFP



68-Pin PLCC

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only.

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SSI 32P4622
Pulse Detector & Data Separator
Advance Information

December 1991

DESCRIPTION

The SSI 32P4622 combines pulse detection and data synchronization electronics into a single high-performance bipolar integrated circuit. It provides advanced features like programmable data rate, and write precompensation control. Data synchronization is performed with a fully integrated high-performance PLL. The VCO frequency setting elements are incorporated into the SSI 32P4622 for enhanced performance and reduced board space. Data rate is programmed by a single external resistor or a DAC in constant-density recording applications. The SSI 32P4622 has been optimized for use with the SSI 32F8011 programmable filter. The SSI 32P4622 operates from a single +5V power supply and is available in 52-pin QFP, PLCC packages.

FEATURES

- **10-24 Mbit/s date rates**
- **High performance pulse detector**
  - **Wide bandwidth AGC**
  - **Dual Rate charge pump**
  - **Amplitude pulse qualification**
- **High performance data synchronizer**
  - **Fast aquisition PLL, using zero phase restart**
  - **Programmable write precompensation**
  - **1, 7 ENDEC**
- **Supports Constant-Density Recording applications**
  - **Programmable data rate**
- **Servo burst output available**
- **Supports external read channel margin testing**
- **Low power, +5 volt only operation**
- **Available in a 52-pin QFP, and a 52-pin PLCC package**

CIRCUIT DESCRIPTION

The circuit is intended to be used as a read pulse detector and data/clock recovery circuit for 1, 7 RLL code in hard disk drive systems with a +5V supply. A circuit block diagram is shown in Figure 5.

MODE CONTROL

The function of the SSI 32P4622 is controlled by the CHIP_EN, SERVO_EN, WG, RG, $\overline{\text{HOLD}}$, AND SHORT pins. Additionally, the chip can be configured through the PULSE DETECTOR MODE CONTROL register and the DATA/CLOCK RECOVERY MODE CONTROL register, both of which are loaded through the serial digital interface.

When reading or writing data the CHIP_EN pin should be high or open circuited. When the CHIP_EN pin is pulled low and the SERVO_EN pin is pulled high the chip data/clock recovery section is disabled. This mode is intended for monitoring servo data in a low power mode when data is not being read or written. When the CHIP_EN and SERVO_EN pins are pulled low the chip goes into a low power state.

The input AGC amplifier, pulse detector and write driver sections of the circuit are controlled by the WG pin and are placed in the read mode when the WG pin is low and in write mode when the WG pin is high or open. The write driver is active during write and inactive during read.

The RG pin controls what signal the data/clock recovery PLL locks to. When RG is high the PLL locks to the signal from the pulse detector input. Normally this is the signal from the pulse detector but the signal can be externally supplied from the $\overline{\text{RD}}$ pin for testing by setting the appropriate control register bit. When RG is low the PLL locks to an external reference supplied at the FREF pin.

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CAUTION: Use handling procedures necessary for a static sensitive component.

CIRCUIT DESCRIPTION (Continued)

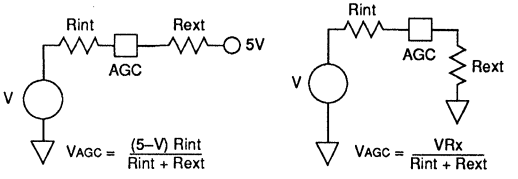
AUTOMATIC GAIN CONTROL CIRCUIT

An amplified head output signal, such as the output of the SSI 32R117, 501, 510 or 32R4610 read/write circuits, is AC coupled to the IN1+ and IN1– inputs. When WG is high or when SHORT is high the pulse detect digital circuitry is disabled and the input impedance of the input AGC stage is reduced to allow more rapid settling of the input coupling capacitors from the read/write circuit upon transition to the read mode. Transition timing to read is controlled to allow settling of the coupling capacitors between the read/write circuit and the SSI 32P4622 before the AGC circuitry is activated when going to the read mode. Coupling capacitors should be chosen with as low a value as possible consistent with adequate bandwidth to allow more rapid settling. Also, when SHORT is high the AGC circuit enters the read mode in a maximum gain state and can rapidly attack to the desired level.

The $\overline{\text{HOLD}}$ pin controls the input AGC stage automatic gain circuit. When CHIP_EN or SERVO_EN is high, $\overline{\text{HOLD}}$ is high and WG and SHORT are low the input AGC amplifier is controlled to keep a constant read data peak level. When the $\overline{\text{HOLD}}$ pin is pulled low the gain of the analog circuit is held at the level determined when the $\overline{\text{HOLD}}$ pin was high (the gain will slowly drift due to leakage).

In the read mode the level at the input to the DIN+, DIN- pins is controlled by full wave rectifying the level at these pins and comparing it to a reference level supplied at the AGC pin. When the input level at the DIN+, DIN- input is greater than about 125% the desired level as set by the AGC pin the circuit is in a fast attack mode and will supply about 1.7 mA of discharge current at the GAIN pin. When the circuit is not in fast attack and the input level is above 100% of the desired level the circuit enters a slower attack mode and will supply about 0.18mA of discharge current. This allows the AGC amplifier to rapidly recover when going from write to read but reduces zero crossing distortion once the AGC amplifier is in range. There is an on-chip fixed slow decay current source. When the slow attack threshold has not been reached for a specified amount of time the circuit assumes the signal is too low and goes into a fast decay mode. The fast attack and fast decay modes can be disabled with the fast attack/decay control bit in the PULSE DETECTOR MODE CONTROL register.

The AGC pin is internally biased so that the target differential voltage input at the DIN+/– pins is 1.0 Vp-p at nominal conditions. The AGC voltage can be modified by tying a resistor between AGC and ground or VPA. A resistor to ground decreases the voltage level while a resistor to VPA increases it. The resultant AGC voltage level is:



where:

V=Voltage at AGC with pin open(2.19V, nom.)
Rint = AGC pin input impedance (6.7 kΩ, typ.)
Rx = External resistor

The new DIN+/– input target level is nominally 0.48 Vp-p/V_{AGC}.

Gain of the AGC amplifier is nominally:

Av = Gain of the AGC stage
= K1 x exp[K2 x V(GAIN)]

where:

Av = Gain of AGC stage
V(GAIN) = Voltage on the gain pin

READ MODE DIGITIZING SECTION

In the data path the signal is sent to a hysteresis comparator. The comparator hysteresis level can be set at a fixed level or, with the addition of an external filter network, can be set as a fraction of the signal level as shown in the circuit block diagram. The latter approach allows setting the AGC circuit decay and slow attack times slow enough to minimize distortion of the signal going into the clocking path and setting a shorter time constant for the hysteresis level. Thus when switching to a head with a different output level or when switching from write to read the circuit is properly decoding data before the AGC circuit gain has settled to its final steady state level. In addition, the hysteresis threshold level can be set from the serial data port. The output of the hysteresis comparator is sent to the "D" input of a D flip-flop. The DOUT pin provides the TTL compatible comparator output digital signal for testing purposes and, if required, for use in the servo circuit.

In the clocking path the signal is sent to a differentiator circuit whose characteristics are set by external components. The output of the differentiator circuit is sent to an edge trigger circuit which creates an output pulse on every zero crossing of the output of the differentiator. The output of the edge trigger is the clock input of the D flip flop. The COUT pin provides the edge trigger output signal for testing purposes.

During normal system operation the differentiator circuit clocks the D flip-flop on every positive and negative peak of the signal input to DIN+,DIN-. The data path D input to the flip-flop only changes state when the signal applied to the DIN+, DIN- inputs exceeds the hysteresis comparator threshold in a polarity opposite the polarity of the peak which last exceeded the threshold. Therefore, the clocking path determines signal timing and the data path blocks spurious peaks if they do not exceed the hysteresis comparator threshold. Figure 7 shows circuit operation of the digital section. The two digital signal path delays between the DIN+, DIN- inputs to the flip-flop CK input and the DIN+, DIN- inputs to flip-flop D input are well matched.

SERVO BURST CAPTURE SECTION

The circuit provides a full wave rectified output of the signal appearing at the DIN+/- inputs at the SER_OUT pin and a servo reference level at the SER_REF pin for use in embedded servo recovery.

DATA/CLOCK RECOVERY CIRCUIT

The circuit is designed to perform data recovery and data encoding in rotating memory systems which utilize a 1,7 RLL encoding format. In the read mode the circuit performs data synchronization, sync field search and detect, address mark detect, and data decoding. In the write mode, the circuit converts NRZ data into the 1,7 RLL format described in Table 3, performs write precompensation, generates the preamble field and inserts address marks as requested. The interface electronics and architecture of the circuit have been optimized for use as a companion device to the SSI 32C452, SSI 32C4640 or AIC 010 controllers.

The data rate is established by a single 1% external resistor, RR, connected from the IREF pin to VPA. This resistor establishes a reference current which sets the VCO center frequency, the phase detector gain, and the 1/3 cell delay. The value of this resistor is given by:

$$\frac{92.6}{DR} - 1.7\ (K\Omega)$$

where: DR = data rate in Mbit/s

In a constant density recording application the IREF pin can be driven by a DAC such as contained in the SSI 32D4661.

An internal crystal reference oscillator, operating at three times the data rate, generates the standby reference for the PLL. An attenuated external TTL compatible reference or an AC coupled ECL source at three times the data rate should be applied to the 'FREF' pin.

The device employs a Dual Mode Phase Detector; Harmonic in the Read Mode and Non Harmonic in Write and Idle Modes. In the Read Mode the Harmonic Phase Detector updates the PLL with each occurrence of a DYLD DATA pulse. In the Write and Idle modes the Non-Harmonic Phase Detector is continuously enabled, thus maintaining both phase and frequency lock. By acquiring both phase and frequency lock to the crystal reference oscillator and utilizing a zero phase restart technique, false lock to DLYD DATA is eliminated.

The phase detector incorporates a charge pump in order to drive the loop filter directly. The polarity and width of the output current pulses correspond to the direction and magnitude of the phase error.

The READ GATE (RG), and WRITE GATE (WG) inputs control the device mode.

RG is an asynchronous input and may be initiated or terminated at any position on the disk. WG is also an asynchronous input, but should not be terminated prior to the last output Write Data pulse.

READ OPERATION

The Data Synchronizer utilizes a fully integrated fast acquisition PLL to accurately develop the decode window. Read Gate, RG, initiates the PLL locking sequence and selects the PLL reference input; a high level (Read Mode) selects the internal RD input and a low level selects the crystal reference oscillator.

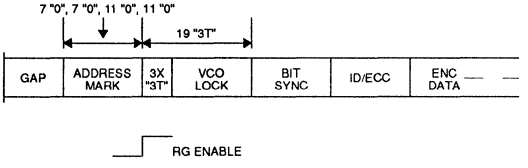
In the Read Mode the falling edge of $\overline{DRD}$ enables the Phase Detector while the rising edge is phase compared to the rising edge of the VCO/2. As depicted in Figure 1, $\overline{DRD}$ is a 1/3 cell wide (TVCO) pulse whose leading edge is defined by the leading edge of RD. An accurate and symmetrical decode window is developed from the VCO/2 clock. By utilizing a fully integrated symmetrical VCO running at three times the data rate, the decode window is insured to be accurate and centered symmetrically about the rising edges of

$\overline{DRD}$. The accuracy of the 1/3 cell delay only affects the retrace angle of the phase detector and does not influence the accuracy of the decode window.

In Non-Read Modes, the PLL is locked to the crystal reference oscillator. This forces the VCO to run at a frequency which is very close to that required for tracking actual data and thus minimizes the associated frequency step during acquisition. When the reference input to the PLL is switched, the VCO is stopped momentarily, then restarted in an accurate phase alignment with the next PLL reference input pulse, and the VCO clock divider is reset. By minimizing the phase alignment in this manner (phase error ≤ 1 rads), the acquisition time is substantially reduced.

SOFT SECTOR OPERATION

Disk Operation Lock Sequence in Read Mode Soft Sector Operation



ADDRESS MARK DETECT

In Soft Sector Read Operation the SSI 32P4622 must first detect an address mark to be able to initiate the rest of the read lock sequence. An address mark consists of two (2) 7 "0" patterns followed by two 11 "0" patterns. To begin the read lock sequence the "Hard/Soft" bit in the data recovery mode control register is set to "0." The Address Mark Detect ($\overline{AMD}$) circuitry then initiates a search of the read data ($\overline{RD}$) for an address mark. First the $\overline{AMD}$ looks for a set of 6 "0's" within the 7 "0" patterns. Having detected a 6 "0" the $\overline{AMD}$ then looks for a 9 "0" set within the 11 "0's". If $\overline{AMD}$ does not detect 9 "0's" within 5 $\overline{RD}$ bits after detecting 6 "0's" it will restart the Address Mark Detect sequence and look for 6 "0's." When the $\overline{AMD}$ has acquired a 6 "0," 9 "0" sequence the $\overline{AMD}$ transitions low.

PREAMBLE SEARCH

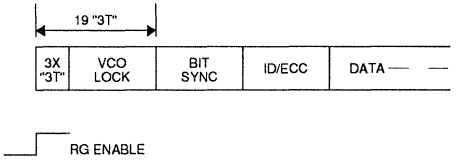
After the Address Mark (AM) has been detected a Read Gate (RG) can be asserted initiating the remainder of the read lock sequence. When RG is asserted an internal counter counts transitions of the incoming Read Data, (positive transitions for RD ECL, negative transitions for $\overline{RD}$ TTL). Once the counter reaches count 3 (finds (3) consecutive 3T preamble) the internal read gate enables switching the phase detector from the reference oscillator to the delayed Read Data input ($\overline{DRD}$); at the same time a zero phase (internal) restart signal restarts the VCO in phase with the $\overline{DRD}$. This prepares the VCO to be synchronized to data when the bit sync circuitry is enabled after VCO lock is established.

VCO LOCK & BIT SYNC ENABLE

When the internal counter counts 16 more "3T" or a total of 19 read data transitions from RG enable, an internal VCO lock signal enables. The VCO lock signal activates the decoder bit synchronization circuitry to define the proper decode boundaries. Also, at count 19, the RRC source switches from the reference oscillator to the VCO clock signal which is phase locked to $\overline{DRD}$. The VCO is assumed locked at this point. A maximum of 2 RRC time periods may occur for the RRC transition, however, no short duration glitches will occur. After the bit sync circuitry sets the proper decode window (VCO in sync with RRC and RRC in sync with data) NRZ is enabled and data is toggled in to be decoded for the duration of the read gate.

HARD SECTOR OPERATION

READ MODE



In hard sector operation $\overline{AMD}$ remains inactive. A hard sector read operation does not require an address mark search but starts with a preamble search as with soft sector and sequences identically. In all respects, with exception to the address mark search sequence, hard sector read operation is the same as soft sector read.

WRITE MODE

In the write mode the SSI 32P4622 converts NRZ data from the controller into 1,7 RLL formatted data for storage on the disk. The SSI 32P4622 can operate with a soft or hard sector hard drive.

In soft sector operation the device generates a "7, 7, 11, 11" Address Mark, and a preamble pattern.

In the hard sector operation the device generates a 19 x "3T" preamble pattern but no preceding Address Mark. Serial NRZ data is clocked into the SSI 32P4622 and latched on defined cell boundaries. The NRZ input data must be synchronous with the rising edges of the WCLK input. The WCLK input is a feature provided for operation in an ESDI application to compensate for large cable delays. In SCSI or ST506 operation, WCLK is connected directly to the RRC output.

Write precompensation circuitry is provided to compensate for media bit shift caused by intersymbol interference. The SSI 32P4622 recognizes specific write data patterns and can add or subtract delays in the time position of write data bits to counteract the read back bit shift. The magnitude of the time shift, TPC, is determined by a combination of the RR value and of an external resistor on the WCS pin.

The SSI 32P4622 performs write precompensation according to the algorithm outlined in Table 3.

SOFT SECTOR

In soft sector operation, when Read Gate (RG) transitions low, VCO source and RRC source switch from $\overline{RD}$ and VCO/3, respectively, to the reference crystal. At the same time the VCO (internal) lock goes inactive but the VCO is locked to the reference crystal. After a delay of 1 NRZ time period (min) from RG low, the Write Gate (WG) can be enabled while NRZ2 is maintained (NRZ write data) low. The Write Address Mark ($\overline{WAM}$) is made active (low) a minimum of 1 NRZ time period later. The Address Mark (consisting of 7 "0's," 7 "0's," 11 "0's, "11 "0's") and the 19 x "3T" Preamble is then written by $\overline{WDO}$. WDNRZ goes active at this point and after a delay of 5 NRZ time periods begins to toggle out $\overline{WDO}$ encoded data. Finally, at the end of the write cycle, 5 NRZ of blank encoded time passes to insure the encoder is flushed of data; WG then goes low.

HARD SECTOR

In hard sector operation, when read gate (RG) transitions low, VCO source and RRC switch references and VCO lock (internal) goes inactive as with soft sector but the AMENB (address mark enable) is kept low.

The SSI 32P4622 then sequences from RG disable to WG enable and WDNRZ active as in soft sector operation.

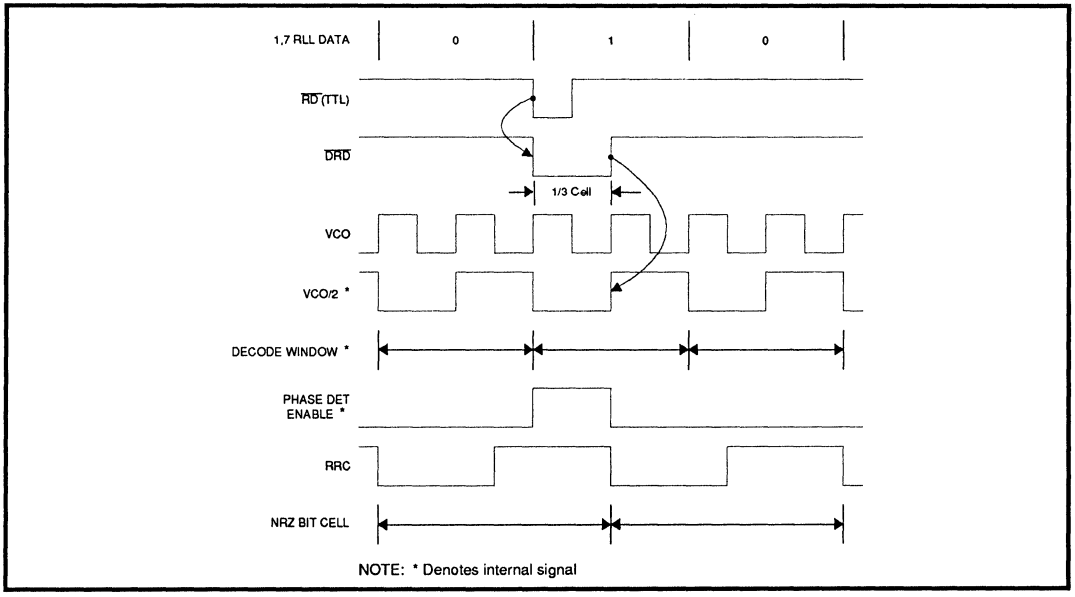


FIGURE 1: Data Synchronization Waveform

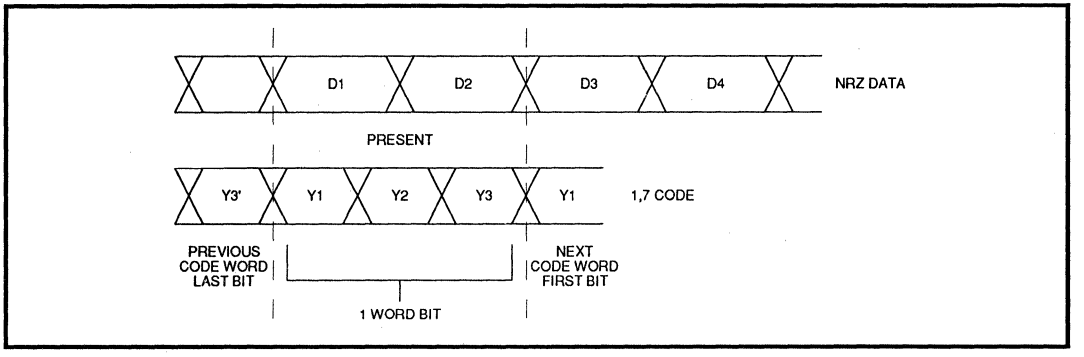


FIGURE 2: NRZ Data Word Comparision to 1, 7 Code Word Bit (See Table 1, for Decode Scheme)

TABLE 1: 1, 7 RLL Code Set

PREVIOUS CODE WORD LAST BITS		DATA BITS PRESENT		NEXT		CODE BITS		
X	0	1	0	0	X	1	0	1
X	0	1	0	1	X	0	1	0
X	0	1	1	0	0	0	1	0
X	0	1	1	*	*	1	0	0
1	0	0	0	0	X	0	0	1
1	0	0	0	1	X	0	0	0
0	0	0	1	0	X	0	0	1
0	0	0	1	1	X	0	0	0
X	1	0	0	0	X	0	0	1
X	1	0	0	1	X	0	1	0
X	1	0	1	0	0	0	1	0
X	1	0	1	*	*	0	0	0
Y2'	Y3'	D1	D2	D3	D4	Y1	Y2	Y3

X = Don't care

* = Not all zeros

TABLE 2: Clock Frequency

WG	RG	VCO REF	RRC	DECCLK	ENCCLK	MODE
0	0	XTAL/2	XTAL/3	XTAL/2	XTAL/2	IDLE
0	1	$\overline{RD}$	VCO/3	VCO/2	XTAL/2	READ
1	0	XTAL/2	XTAL/3	XTAL/2	XTAL/2	WRITE
1	1	XTAL/2	XTAL/3	XTAL/2	XTAL/2	IDLE

Note 1: Until the VCO locks to the new source, the VCO/2 entries will be XTAL/2.

2: Until the VCO locks to the new source, the VCO/3 entries will be XTAL/3.

TABLE 3: Write Precompensation Algorithm

BIT	BIT	BIT	BIT	BIT	COMPENSATION
n-2	n-1	n	n+1	n+2	BIT n
1	0	1	0	1	NONE
0	0	1	0	0	NONE
1	0	1	0	0	EARLY
0	0	1	0	1	LATE

LATE: Bit n is time shifted (delayed) from its nominal time position towards the bit n+1 time position.

EARLY: Bit n is time shifted (advanced) from its nominal time position towards the bit n-1 time position.

SERIAL PORT OPERATION

Programming of the 32P4622 internal registers is achieved through a three-line serial interface port. The interface requires an enable line, data line, and clock line. Data is transferred into the serial port in eight bit bytes. The first four bits contain the address information and the remaining four bits contain the programming data (reference Figure 3). The timing considerations for the serial port are fairly straight forward. The enable line is driven high by the external controller to initiate data transfer. While the enable line is high, the controller must output eight clock pulses along with eight bits of synchronous programming data. The 32P4622 will internally latch the data on the falling edge of the clock pulses. To prevent false data from being latched in, only eight clock pulses should be provided. The following tables provide register information.

TABLE 4: Serial Port Register Addresses

A0	A1	A2	A3	DESTINATION
0	0	0	0	Pulse detector mode control
1	0	0	0	Data/clock recovery control register
0	1	0	0	Reserved

SERIAL PORT (Continued)

TABLE 5: Pulse Detector Mode Control Register Bit Definition

BITS		DESCRIPTION
D0		Fast attack/decay current control
0		Fast attack/decay enabled
1		Fast attack/decay disabled
D1	D2	Hysteresis level control
0	0	Level always controlled by HYS pin level
0	1	Level fixed at maximum percent of input level
1	0	Level fixed at nominal percent of input level
1	1	Level fixed at minimum percent of input level
D3		Test Mode
0		Normal mode: Read mode can be monitored on $\overline{RD}$ pin.
1		Test mode: Read data can be sent to the data/clock recovery section by driving the $\overline{RD}$ pin.

TABLE 6: Data/Clock Recovery Mode Control Register Bit Definition

BITS		DESCRIPTION
D0		Phase detector enable control bit
0		Normal mode
1		Disables the phase detector and allows the VCO to coast (test mode only)
D1		Hard/soft sector control bit
1		Hard sector
0		Soft sector activates the 7 "0," 7 "0," 11"0," 11 "0" pattern soft sector address mark circuitry
D2	D3	Write precompensation magnitude control bits
1	1	Maximum shift
0	1	Second highest shift
1	0	Minimum shift
0	0	No shift

SERIAL PORT (continued)

TABLE 7: Serial Port Timing Specifications

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
TSLAT	Setup time: see Figure 3	1.5			µs
THLAT	Hold time: see Figure 3	1.0			µs
TSSDAT	Data setup time: see Figure 3	45			ns
THSDAT	Data hold time: see Figure 3	45			ns
TC	Clock period	100			ns

DIGITAL INPUTS AND OUTPUTS

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$\overline{WAM}$, WG, CHIP_EN, SERVO_EN, DATA_EN, SDATA, RG, FREF, SHORT, $\overline{HOLD}$, WDNRZ, WCLK, (These are TTL inputs)

$\overline{AMD}$, $\overline{VCOE}$, R/$\overline{W}$, $\overline{WD}$, DOUT, NRZ1, RRC (These are TTL outputs)
$\overline{RD}$ is a bidirectional pin with TTL input and ECL-like output

TABLE 8: TTL COMPATIBLE INPUTS

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Input Low Voltage	(VIL)	-0.3		0.8	V
Input High Voltage	(VIH)	2.0		VPD+0.3	V
Input Low Current	VIL = 0.4 V	0.0		0.4	mA
Input High Current	VIH = 2.4 V			100	µA

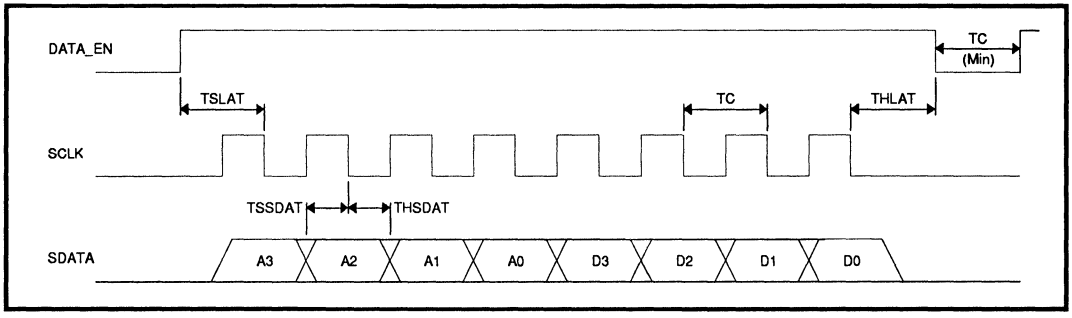

FIGURE 3: Serial Data Interface Timing

PIN DESCRIPTIONS

POWER SUPPLY

NAME	TYPE	DESCRIPTION
VPA1, VPA2, VPA3	I	5 volt analog power supply pins.
VPD1, VPD2	I	5 volt digital power supply pins.
AGND1, AGND3	I	Analog ground pins.
DGND1, DGND2	I	Digital ground pins.

CHIP MODE CONTROL

CHIP_EN	I	CHIP ENABLE: TTL compatible input which enables the chip during normal drive operation.
SERVO_EN	I	SERVO ENABLE: TTL compatible input which enables only the portions of the chip needed to read the servo burst.
WG	I	WRITE GATE: TTL compatible read/write control pin.
SDATA	I	SERIAL DATA: Serial data input.
SCLK	I	SERIAL CLOCK: Serial data clock.
SDEN	I	SERIAL DATA ENABLE: Serial data enable pin.
R/$\overline{W}$	O	READ/WRITE: TTL compatible output pin which is the negative of WG and which is intended to drive the R/$\overline{W}$ input of the read write chip.

AGC GAIN STAGE

IN1+, IN1-	I	INPUT1+/-: AGC amplifier signal input pins.
DCPL1, DCPL2	O	A decoupling capacitor is connected across these pins to remove DC offset in the gain buffer.
OUT1+, OUT1-	O	OUTPUT1+/-: AGC amplifier signal output pins.
$\overline{HOLD}$	I	HOLD: TTL compatible control pin which, when pulled low, holds the input AGC amplifier gain.
SHORT	I	SHORT: TTL compatible control pin which, when pulled high shorts the AGC input pins.
AGC	I	AUTOMATIC GAIN CONTROL REFERENCE: Reference input voltage level for the AGC circuit.
GAIN	I	GAIN CONTROL VOLTAGE: The AGC timing capacitor is tied between this pin and AGND. Also gain of the AGC amplifier can be controlled by a DC voltage on this pin.

PULSE DIGITIZING STAGE

NAME	TYPE	DESCRIPTION
DIN+, DIN-	I	DATA IN+/-: Signal input pins to the hysteresis level detect comparator.
HYS	I	HYSTERESIS: Hysteresis level setting input to the hysteresis level detect comparator.
LEVEL	O	LEVEL: Provides rectified level setting level for input into the hysteresis circuit.
DOUT	O	DATA OUT: D input into D flip-flop provided as output for testing or servo use.
CIN+, CIN-	I	CLOCK INPUT+/-: Differential signal input pins to the clocking channel.
COUT	O	CLOCK OUTPUT: Clock input into D flip-flop provided for testing.
$\overline{RD}$	I/O	READ DATA: Bidirectional test pin which provides ECL like read output from the pulse detector section when WG is low and allows a TTL compatible external read data pattern to be sent to the data/clock recovery when WG is high.

SERVO OUTPUT

SERV_OUT	O	SERVO OUTPUT: Servo output signal
SERV_REF	O	SERVO REFERENCE: Servo reference level

DATA/CLOCK RECOVERY SECTION

RG	I	READ GATE: Selects the PLL reference input and initiates the PLL synchronization sequence. A high level selects the RD input and enables the read mode/address detect sequences. A low level selects the FREF input.
FREF	I	REFERENCE FREQUENCY: The input can be driven by a direct coupled attenuated TTL signal or an AC coupled ECL signal. For minimizing pulse jitter during read, FREF should be stopped by gating it externally with $\overline{VCOE}$.
NRZ	O	NRZ OUTPUT PORT: When in read mode NRZ is a single ended TTL output for NRZ read data. When in write or idle mode NRZ is tristated.
WDNRZ	I	NRZ INPUT PORT: WDNRZ is a single ended TTL input for NRZ write data. Data must be synchronous with the write clock (WCLK) signal.
$\overline{WAM}$	I	WRITE ADDRESS MARK: The pin is the write address mark input when WG is high. In soft sector mode, a one bit wide low level pulse will write a 7"0," 7"0," 11"0," 11"0" address mark.
WCLK	I	WRITE CLOCK: TTL clock input that is used to shift in the data presented on the WDNRZ input.

DATA/CLOCK RECOVERY SECTION (continued)

NAME	TYPE	DESCRIPTION
$\overline{AMD}$	O	ADDRESS MARK DETECT: The pin is the low level address mark detect output when RG is high. In hard sector mode, the pin is in a high impedance state.
$\overline{WD}$	O	WRITE DATA: Encoded write data output, active low. The data is automatically re sychronized to one edge of the FREF input clock.
RRC	O	READ/REFERENCE CLOCK: RRC is a single ended TTL output. Clock synchronous with NRZ output data.
$\overline{VCOE}$	O	VCO ENABLE: This active low TTL output is used to disable the external clock applied to the FREF pin.
VCO_CLK	O	VCO CLOCK: An open emitter ECL output test point. Two external resistors are required to use this pin. They should be removed during normal operation to reduce power dissipation.
$\overline{DRD}$	O	DELAYED READ DATA: An open emitter ECL output test point. The positive edges of this signal indicate the data bit position. Two external resistors are required to use this pin. They should be removed during normal operation to reduce power dissipation.

ANALOG PINS

IREF	I	CURRENT REFERENCE INPUT: The VCO center frequency, the 1/3 cell delay, and the phase gain are a function of the current sourced into this pin.
FLTR	I	LOOP FILTER INPUT: Input for passive PLL filter.
WCS	I	WRITE PRECOMPENSATION SET: Pin for RC network to program the write precompensation magnitude value.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	MIN	NOM	MAX	UNIT
+5V supply voltage - VPA1,VPA2,VPA3,VPD1,VPD2			6	V
Storage Temperature	65		150	°C
Package Temp. PLCC, QFP (20 sec reflow solder)			215	°C
Pin Voltages: DOUT, $\overline{DOUT}$, RD, $\overline{WD}$, NRZ1, NRZ2, $\overline{WAM}$/$\overline{AMD}$, $\overline{VCOE}$, RRC, $\overline{RRC}$, VCO_CLK, $\overline{DRD}$	–0.3		VPA/VPD+0.3 or +12	V mA
All other pins	–0.3		VPA/VPD+0.3	V

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified: 4.65 ≤ VPA ≤ 5.25, 4.65 ≤ VPD ≤ 5.25, TBD ≤ Tj ≤ TBD.)

POWER SUPPLY

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
+5 V (VPA/VPD) Supply current	Outputs unloaded, CHIP_EN, SERVO_EN=High		175	TBD	mA
Power Dissipation	Outputs unloaded, Tj=145 °C, CHIP_EN,SERVO_EN=High		0.875	TBD	W
	CHIP_EN=High, SERVO_EN=Low		TBD	TBD	mW
	CHIP_EN,SERVO_EN=Low		TBD	TBD	mW

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MODE CONTROL

Power Down Modes

CHIP_EN	SERVO_EN	MODE	DESCRIPTION
1	-	Enable	The entire chip is enabled.
0	1	Servo	Only the parts of the chip necessary to generate the SERV_OUT and DOUT/$\overline{\text{DOUT}}$ outputs are active.
0	0	Disable	The entire chip is in a power down mode.

Pulse Detector Mode Control

(CHIP_EN or SERVO_EN = 1)

WG	$\overline{\text{HOLD}}$	SHORT	MODE	DESCRIPTION
0	1	0	Read	Read amp on, AGC active and controlled by data.
0	0	0	Read/Hold	Read amp on, AGC level held at previous active level
1	-	0	Write	(Read amp gain set to zero) AGC level held at previous active level, AGC inputs shorted by low impedance.
-	-	1	Reset AGC	(Read amp gain set to zero) GAIN pin set for AGC maximum AGC gain, AGC inputs shorted by low impedance

Data/Clock Recovery Mode Control
(CHIP_EN = 1)

WG	RG	MODES	DESCRIPTION
0	1	RD lock	Data/clock recovery PLL locked to read data, $\overline{WD}$ is high.
0	0	FREF lock	Data/clock recovery PLL locked to external FREF reference, $\overline{WD}$ high.
1	0	Write	Data/clock recovery PLL locked to external FREF reference, $\overline{WD}$ active.
1	1	-	Undefined state.

PULSE DETECTOR TRANSITION TIMES

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Enable <–> Disable Transition time	Settling time of external capacitors not included			20.0	µs
Read –> Write Transition Time	WG pin Low –> High			1.0	µs
Write –> Read Transition Time	WG pin High –>Low AGC settling not included	1.2		3.0	µs
Read –> Short Transition Time	SHORT pin Low –> High			1.0	µs
Short –> Read Transition Time	SHORT pin High –> Low AGC settling not included	1.2		3.0	µs
Hold On <–> Hold Off Transition time	$\overline{HOLD}$ pin High <–> Low			1.0	µs

TTL COMPATIBLE OUTPUTS
Note: Outputs are loaded with a 4 kΩ resistor to 5V and 15 pF total capacitance (including stray capacitance) to GND for rise/fall time measurements.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Output Low voltage	Iol = 4.0 mA			0.4	V
Output High Voltage	Ioh = –400 µA	2.4			V
Output Rise Time	Voh = 2.4 V			9.0	ns
Output Fall Time	Vol = 0.4 V			9.0	ns

DIFFERENTIAL OUTPUTS
Outputs are loaded with a 10 kΩ resistor and 5 pF total capacitance (including stray capacitance) to GND for rise/fall time measurements.

PARAMETER	CONDITION		MIN	MAX	UNIT
Output Low Voltage	−0.5 mA < Iol < 0.5 mA	Tj=25°C	VPD−2.7	VPD−2.5	V
		Tj=145°C	VPD−2.2	VPD−2.0	V
Output High Voltage	−0.5 mA < Ioh < 0.5mA	Tj=25°C	VPD−1.8	VPD−1.7	V
		Tj=145°C	VPD−1.3	VPD−1.2	V
Output Rise Time	Voh = 90% final			6.0	ns
Output Fall time	Vol = 10% final			6.0	ns

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ANALOG GAIN SECTION
The circuit is intended to interface with the filter structure shown in Figure 5.
The following measurements are made with the following conditions unless otherwise stated: 1. The circuit is in the read mode (CHIP_EN or SERVO_EN, and $\overline{\text{HOLD}}$ PINS high, WG and SHORT pins low) 2. The circuit is connected as in Figure 5.

Automatic Gain Control Section
The AGC circuit maintains the AC voltage level monitored across the DIN+/- pins at a level defined by the voltage on the AGC pin.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Stage Gain Settings					
K1	K1 = 75 V/V			±17	%
K2	K2 = −2.5 V/V			±5	%
Minimum Gain Range		0.75		50	V/V
AGC Loop Level Settings					
DIN+ - DIN- Input Voltage Swing vs. V(AGC)	20mVpp≤V(IN1+−IN1-)≤240mVpp, 0.5Vpp≤V(DIN+ − DIN-)≤1.4Vpp	0.37		0.56	Vpp/V
DIN+ - DIN- Input Voltage Swing When AGC Pin is Open	20 mVpp ≤ V(IN1+ − IN1-) ≤ 240mVpp	0.85	1.0	1.12	%
DIN+ - DIN- Input Voltage Swing Variation	20 mVpp ≤ V(IN1+ − IN1-) ≤ 240mVpp			8.0	%
AGC Pin Input Impedance		4.4		10.8	kΩ
AGC Pin Voltage	V(AGC) = 2.19V, AGC pin open			±11	%
Allowable DIN+ - DIN- Input signal range				1.4	Vpp

AGC Loop Time Constants

Slow AGC Decay Capacitor Charge Current	V(DIN+ - DIN-)=0.0		4.5		µA
Fast AGC Decay Capacitor Charge Current	V(DIN+ - DIN-)=0.0		1.2		mA
Fast Decay Hold Off Time	Slow attack threshold not reached	0.7		0.3	µs
AGC Capacitor Leakage Current	Read/Hold Mode	-0.2		0.2	µA
Slow AGC Attack Capacitor Discharge Current	V(DIN+ - DIN-)=0.8Vdc Vary V(AGC) until slow charge begins.	0.14		0.22	mA
Fast AGC Attack Capacitor Discharge Current	V(DIN+ - DIN-)=0.8Vdc V(AGC)= 3.0V	-1.3		-2.0	mA
Fast –> Slow Attack Switchover Point	V(DIN+ - DIN-) - V(DIN+ - DIN-)Final		0.25		V
Gain Decay Time (Td) (see Figure 6)	Vin = 240 mVpp –> 120 mVpp @ 2.5 Mhz, Vout to 90% of final value		TBD		µs
Gain Attack Time (Ta) (see Figure 6)	WG = high –> low, Vin = 240 mV @ 2.5 Mhz Vout to 110% final value		4		µs

General Amplifier Characteristics

PARAMETER	CONDITION	MIN	NOM	MAX	UNITS
Input Voltage Range		20		240	mVpp
Differential Input Resistance	V(IN1+ - IN1-) = 100 mVpp @ 2.5 Mhz		5.0		kΩ
Differential Input Capacitance	V(IN1+ - IN1-)=100 mVpp			10.0	pF
Common Mode Input	SHORT pin = low		1.8		kΩ
Impedance (both sides)	SHORT pin = high		250		Ω
Input Noise	Gain set to Maximum			30	$nV/\sqrt{Hz}$
Differential Output Resistance OUT1+/-		16		60	Ω
OUT1+ to OUT1- Pin current	No DC path from OUT+/- to GND	±1.1			mA
Bandwidth	Gain set to maximum, ±3 dB bandwidth	30			MHz

General Amplifier Characteristics (Continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNITS
Common ModeRejection Ratio (Input Referred)	V(IN1+)=V(IN1-)=100 mVpp, 5 Mhz, Gain set to maximum	40			dB
Power Supply Rejection Ratio (Input Referred)	V(VPA/VPD) = 100 mVpp 5 MHz, Gain set to maximum	30			dB

Gain Buffer to Differentiator and Matdched Delay Section

Differential Output Resistance OUT4+/-		10		32	Ω
Maximum Output Voltage Swing	Z(load diff.) = 350 Ω	1.4			Vpp
OUT4+ to OUT4- Pin current	No DC path from OUT+/- to GND	±2.3			mA
Output Offset Voltage				±50	mV
Bandwidth	Gain set to maximum,	30			MHz
Common Mode Rejection Ratio (Input referred)	V(IN4+) = V(IN4-)=100 mVpp, 5 Mhz, Gain set to maximum	40			dB
Power Supply Rejection Ratio (Input referred)	V(VPA/VPD) = 100 mVpp, 5 Mhz, Gain set to maximum	30			dB

READ MODE DIGITIZING SECTION

All of the measurements in the read digital section are made with the following conditions unless otherwise stated:

1. In the read mode, (CHIP_EN high, WG & SHORT pins low)
2. The clock and data input (CIN+ - CIN) and (DIN+ - DIN-), receive AC coupled 2.5 MHz, 1.0 Vpp sine-wave input signals with the DIN+/- input leading CIN+/- by 90 degrees.
3. A 1.8V DC voltage is applied to HYS pin.
4. The $\overline{RD}$ and DOUT pins are loaded with a 10 kΩ resistor and 5 pF total capacitance to GND.

Hysteresis Comparator Circuit

Input Signal Range				1.4	Vpp
Differential Input Resistance	V(DIN+ - DIN-) = 100 mVpp, 2.5 Mhz	10		16.5	kΩ
Differential Input Capacitance	V(DIN+ - DIN-) = 100 mVpp, 2.5 Mhz			4.0	pF

Hysteresis Comparator Circuit (Continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNITS
Common Mode Input Impedance	Both sides	2.5		4.0	kΩ
LEVEL Pin Output Voltage vs DIN+ - DIN- Input voltage	0.6 < V(DIN+ - DIN-)<1.4 Vpp 10 kΩ between LEVEL & GND	1.3		2.2	V/Vpp
LEVEL Pin Output Impedance	I(LEVEL) = 0.5 mA		140		Ω
LEVEL Pin Maximum Output Current		3.0			mA
Comparator Offset Voltage	HYS pin at GND, ≤1.5 kΩ across DIN+, DIN-			±10	mV
Hysteresis Trip Voltage (at DIN+, DIN-) vs. HYS pin voltage	1V < V(HYS) < 2V	0.44	0.5	0.64	Vpp/V
Hysteresis Threshold Margin as a % of V(DIN+ - DIN-) Peak	V(HYS) = some % of V(AGC)* or V(LEVEL), 1V < V(HYS) < 3V See Figures 17 & 18	-15		+15	% Peak
HYS Pin Input Current	1V < V(HYS) < 3V	0.0		-20	µA

*In an open loop configuration where reference is V(AGC) tolerance may be slightly higher

TABLE 1: Frequency Template of Hysteresis Trip Point as Percent of Peak Input Voltage Across DIN+/– Pins

Frequency	Hysteresis			
	External	High	Medium	Low
0 to TBD MHz	TBD to TBD %	TBD to TBD %	TBD to TBD %	TBD to TBD %
TBD MHz	TBD to TBD %	TBD to TBD %	TBD to TBD %	TBD to TBD %

Note 1: Pulse detector mode control register bits D1, 2 set as follows:

00 = External hysteresis

10 = About 65% hysteresis

01 = About 50% hysteresis

11 = About 35% hysteresis

Note 2: For external hysteresis, LEVEL/HYS pin network is set up with external component values as shown in Figure 5a.

Clocking Circuit

PARAMETER	CONDITION	MIN	NOM	MAX	UNITS
Input Signal Range				1.4	Vpp
Differential Input Resistance	V(CIN+ - CIN-) = 100 mVp-p, 2.5 Mhz	10		16.5	kΩ
Differential Input Capacitance	V(CIN+ - CIN-) = 100 mVp-p, 2.5 Mhz			4.0	pF
Common Mode Input Impedance	Both sides	2.7		3.8	kΩ
Input Offset Voltage				6.0	mV
COUT Pin Output Low Voltage	TIE 2 kΩ from COUT to GND		VPA-3.0		V
COUT Pin Output Pulse Voltage V(high) - V(low)	TIE 2 kΩ from COUT to GND		+0.8		V
COUT Pin Output Pulse Width	TIE 2 kΩ from COUT to GND		12		ns

Read Mode Digital Section as System

PARAMETER	CONDITION	MIN	NOM	MAX	UNITS
Required DFF Set up Time, (Td1 in Figure 7)	Minimum allowable time delay from V(DIN+, DIN) exceeding hysteresis point to V(CIN+,CIN) crossing zero	0			ns
Propagation Delay Td3 in Figure 7				60	ns
Pulse Pairing	|Td3-Td4| in Figure 7			1.0	ns
RD Pin Output Pulse Width	0.0 < Ioh < 0.5 mA		10		ns
RD Pin Output Low Voltage	0.0 < Iol < 0.5 mA		VPA-2.1		V
RD Pin Output Pulse Voltage V(high)-V(low)	0.0 < Ioh < 0.5 mA		+0.8		V

Servo Burst Capture Circuit
All of the measurements for the servo are made with the following conditions unless otherwise stated. The circuit is connected as shown in Figure 5.

PARAMETER	CONDITION	MIN	NOM	MAX	UNITS
SERV_REF Pin Level		VPA-2.8		VPA-2.1	V
SERV_OUT to SERV_REF Offset	DIN+ shorted to DIN-			±20	mV
SERV_OUT Level vs AGC Pin Voltage	$\frac{V(SERV\_OUT)}{V(AGC)} = 0.2$ Vp/V			±TBD	%
Servo Frame vs. V(DIN+/-)	$\frac{V(SERV\_OUT - SERV\_REF)}{V(DIN+/-)}$ = 0.39 Vp/Vpp			TBD	Vp/Vpp
Allowable Load Impedance SERV_OUT or SERV_REF to GND	Equivalent parallel resistance	10			kΩ
	Equivalent parallel capacitance			5	pF

CLOCK/DATA RECOVERY SECTION:
See applications section for loop filter development.

DC Output levels

PARAMETER	CONDITION	MIN	NOM	MAX	UNITS
Test Point Output High Level (VOHT) $\overline{DRD}$, VCO_CLK, VCO_REF	262Ω to VPD,402Ω to GND VPA = VPD	VPD-1.02			V
Test Point Output Low Level (VOLT) $\overline{DRD}$, VCO_CLK, VCO_REF	262Ω to VPD,402Ω to GND VPA = VPD			VPD-1.625	V

Read Mode

PARAMETER	CONDITION	MIN	NOM	MAX	UNITS
Read Clock Rise Time (TRRC)	0.8V to 2.0V, C1 ≤ 15 pF			8	ns
Read Clock Fall Time (TFRC)	2.0V to 0.8V, C1 ≤ 15 pF			5	ns
NRZ (out) Set Up and Hold Time (TPNRZ)		.31 TORC			ns
$\overline{AMD}$ Propagation Delay (TPAMD)		10			ns
1/3 Cell Delay	TD=3.6E-12(RR+1700)	0.8TD		1.2TD	ns

Write Mode

PARAMETER	CONDITION	MIN	MAX	UNIT
Write Data Pulse Width (TWDC)	C1 < 15 pF	$\frac{2TOWC}{3}$ - 2TPC - 5	$\frac{2TOWC}{3}$ +5	ns
Write Data Fall Time (TFWD)	2.0V to 0.8V, C1 ≤ 15 pF		8	ns
Write Data Clock Rise Time (TWRC)	0.8V to 2.0V, C1 < 15 pF		10	ns
Write Data Clock Fall Time (TWFC)	2.0 to 0.8V C1 < 15 pF		8	ns
NRZ Set Up Time (TSNRZ)		5		ns
NRZ Hold Time (THNRZ)		5		ns
Precompensation Time Shift Magnitude Accuracy (TPC)	TPCO = 1.12T x A/(B+3A) See note			
	D2 bit=0, D3 bit=0	0	0	ns
	D2 bit=1, D3 bit=0	0.8TPC-0.2	1.2TPC+0.2	ns
	D2 bit=0, D3 bit=1	2(0.8TPC)	2(1.2TPC)	ns
	D2 bit=1, D3 bit=1	3(0.8TPC)	3(1.2TPC)	ns

Note: T = FREF period, A=0.19/(Rpc+0.51)+0.0058, B=0.42/(RR+0.53)+0.0108, Rpc & RR in kΩ

Data Synchronization

PARAMETER	CONDITION	MIN	MAX	UNIT
VCO Center Frequency Period (TVCO)	VCO IN = 2.7V, TO = 3.6E(RR+1700), VPA, VPD = 5.0V, RR = $\frac{92.6}{DR}$ - 1.7(KΩ)	0.8TO	1.2TO	ns
VCO Frequency Dynamic Range	1.0V≤VCO IN≤VPA-0.6V VPA, VPD = 5.0V	±25	±45	%
VCO Control Gain (KVCO)	ωo = 2 x π/TO, 1.0V≤VCO IN≤VPA-0.6V	0.14ωo	0.26ωo	$\frac{rad}{VxS}$
Phase Detector Gain (KD)	For PLL REF=FREF, KD=0.22/(RR+530) For PLL REF=RD, KD=0.11/(RR+530) VPA, VPD = 5.0V	0.83KD	1.17KD	A/rad
KVCOxKD Product Accuracy		-28	+28	%
VCO Phase Restart Error	Referred to RRC	-1	+1	rad
Decode Window Centering Accuracy			±1.0	ns
Decode Window		(2TORC/3) -1.5		ns

5

APPLICATIONS INFORMATION

LOOP FILTER

The low pass filter attenuates high frequency components fo the phase error signal from the phase detector and modifies the dynamics of the PLL. In lock mode, the PLL can be approximated by the linear model shown in Figure 4. The transfer functions of the blocks are as follows:

KD = conversion factor for phase detector in µA/radian
KVCO = VCO gain factor in radians/volt-second
F(s) = low pass filter transfer function

Thus the closed loop transfer function is:

$$H(s) = \frac{\frac{KD \cdot Kvco \cdot F(s)}{N}}{s + \frac{KD \cdot Kvco \cdot F(s)}{N}}$$

where: N = ratio between TBD and FIN
N = 1.0 for preamble
N= 0.5 for external clock

For the low pass filter example:

$$F(s) = \frac{1 + sC1R}{sC1\left(1 + \frac{C2}{C1} + sC2R\right)}$$

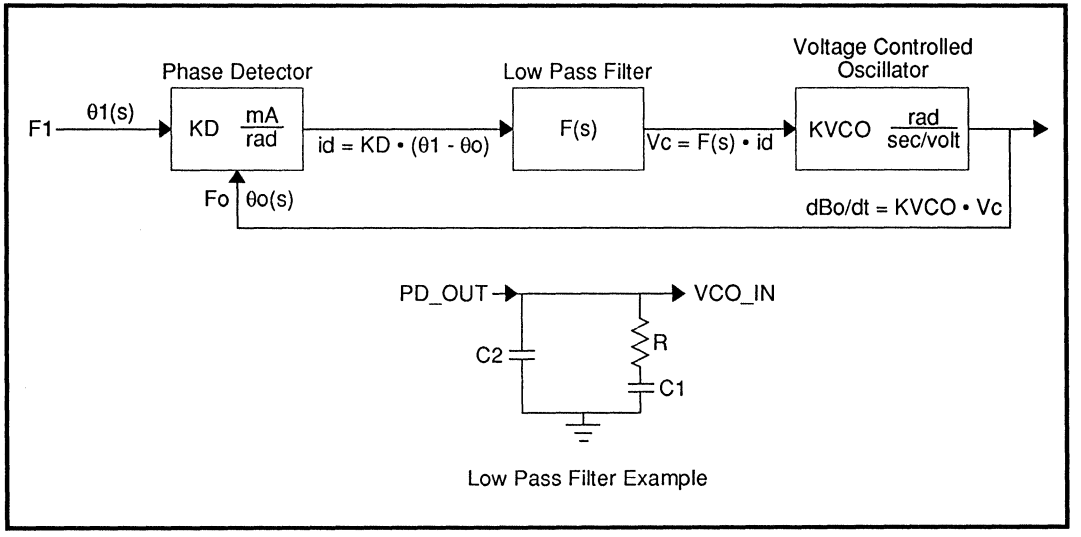


FIGURE 4: Phase Locked Loop

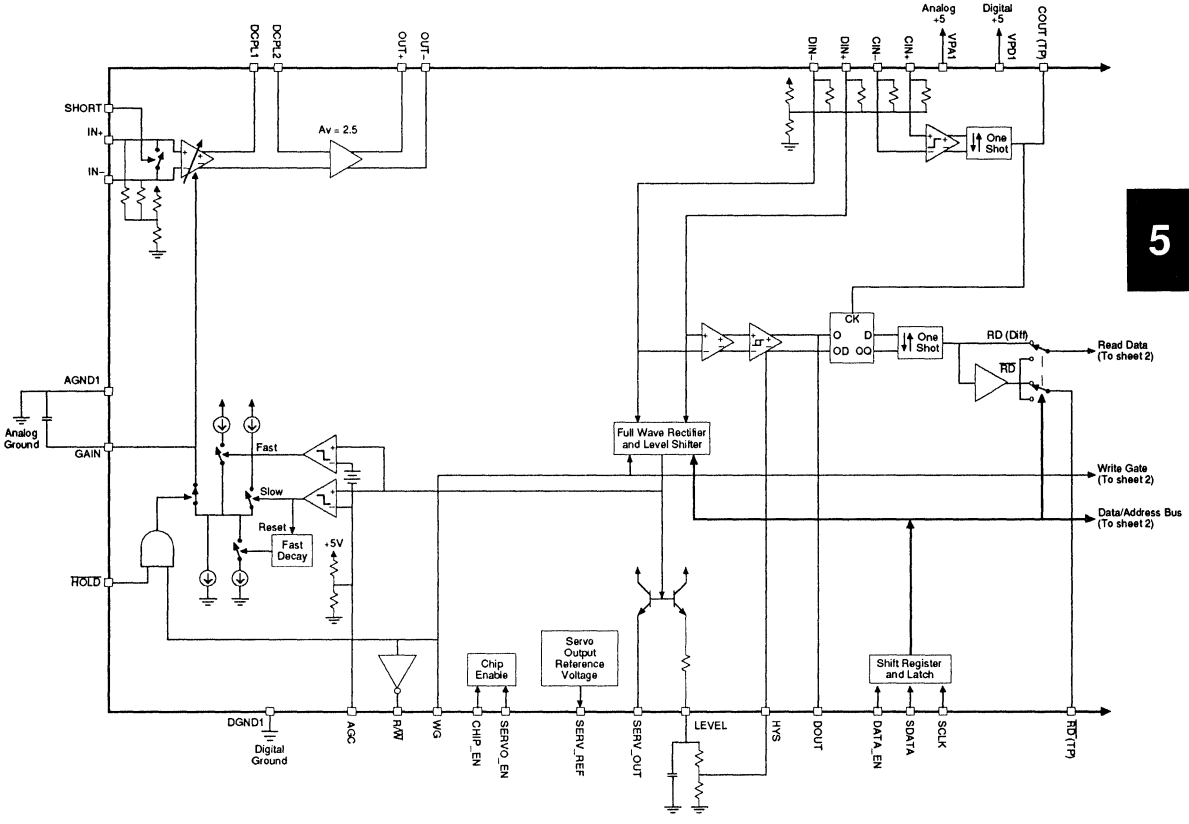


FIGURE 5a: SSI 32P4622 Circuit Block Diagram (Sheet 1)

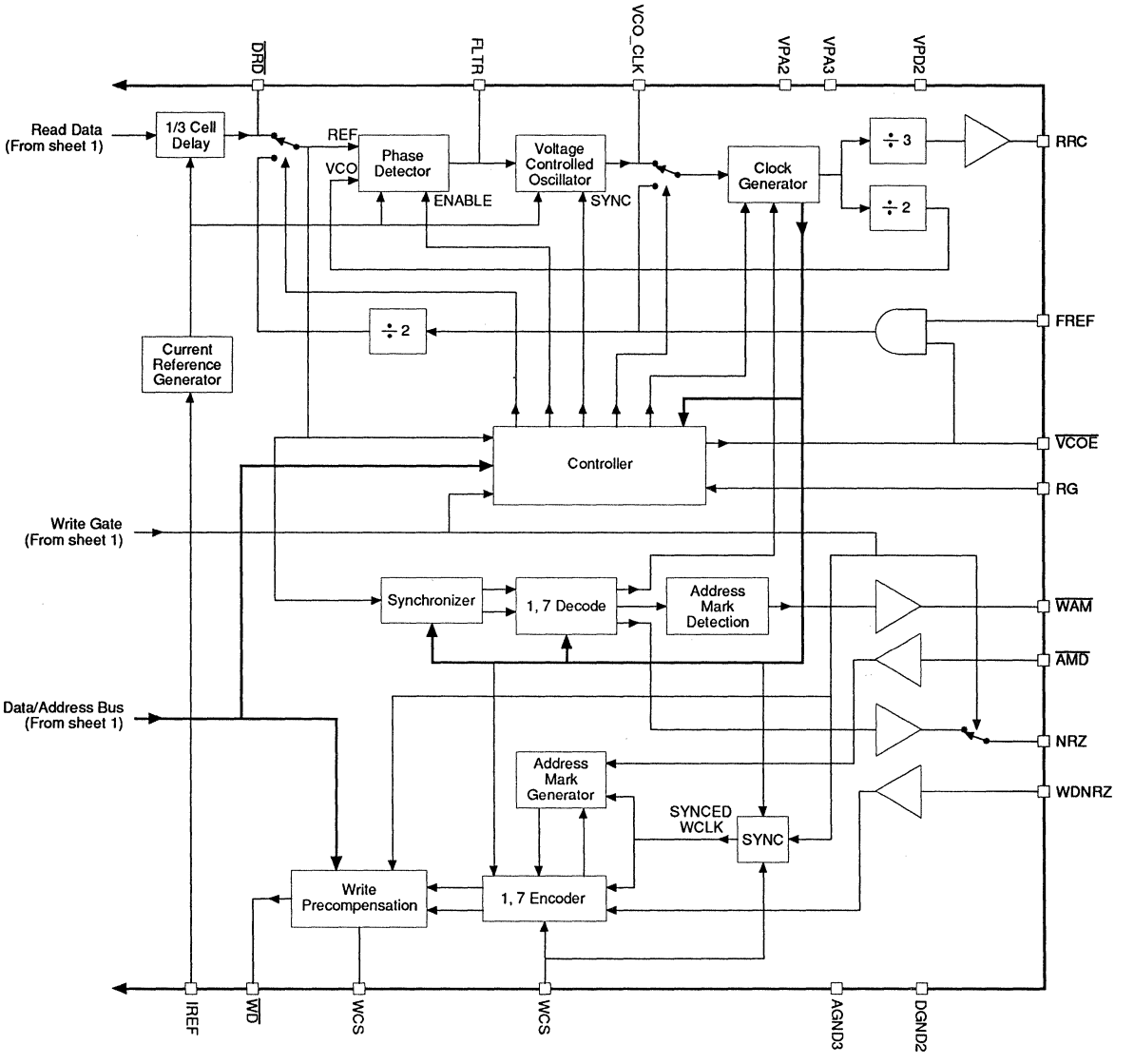


FIGURE 5b: SSI 32P4622 Circuit Block Diagram (Sheet 2)

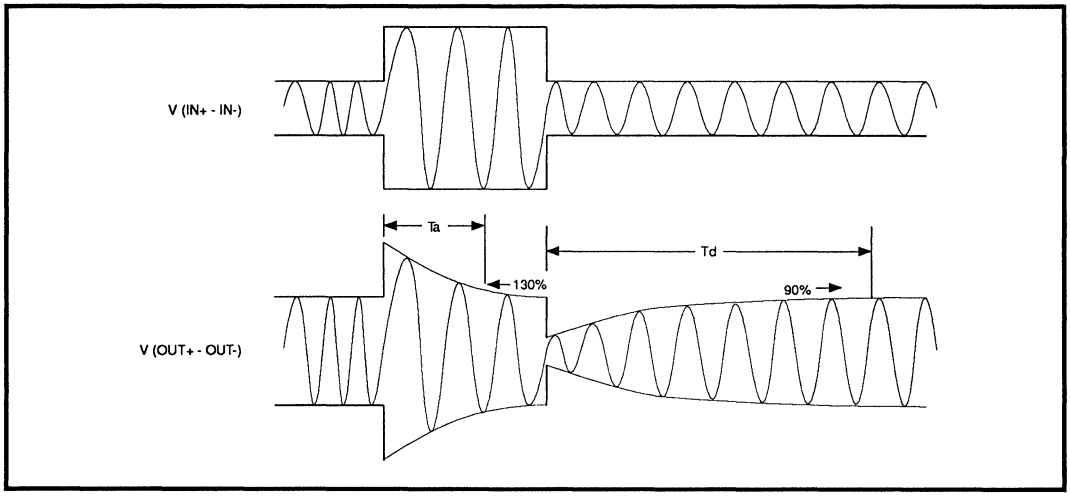


FIGURE 6: AGC Timing Diagram

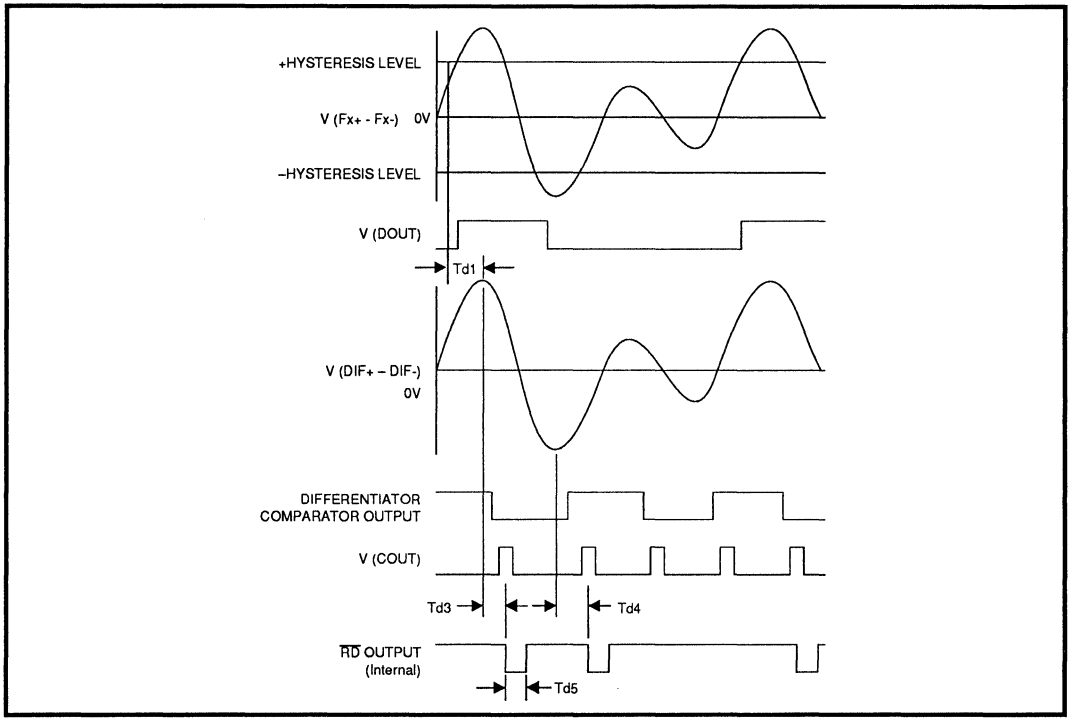


FIGURE 7: Read Mode Digital Section Timing Diagram

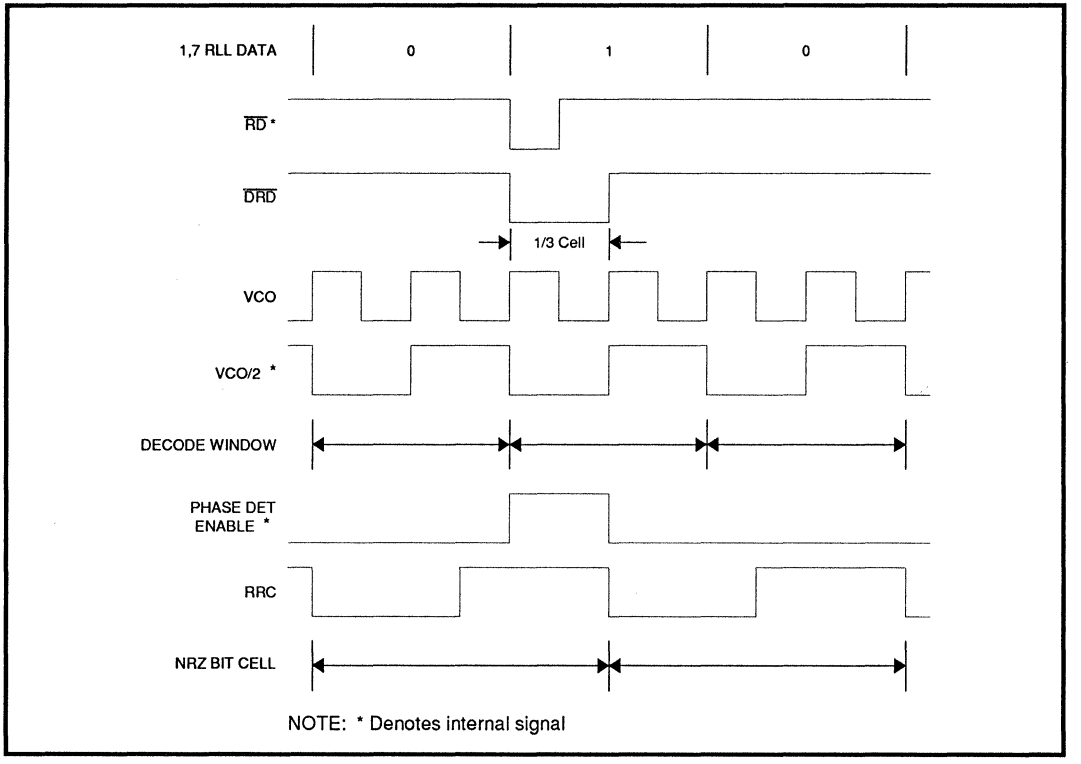


FIGURE 8: Data Synchronization Waveform

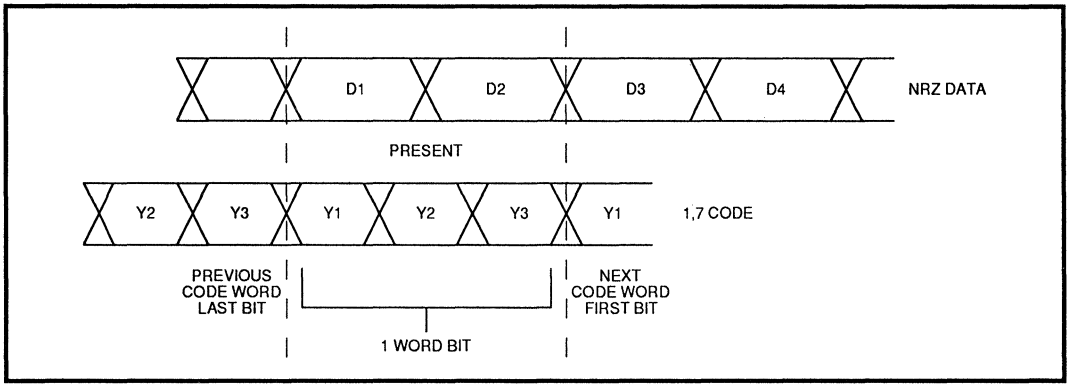


FIGURE 9: NRZ Data Word Comparison to 1, 7 Code Word Bit
(See Table 1 for decode scheme)

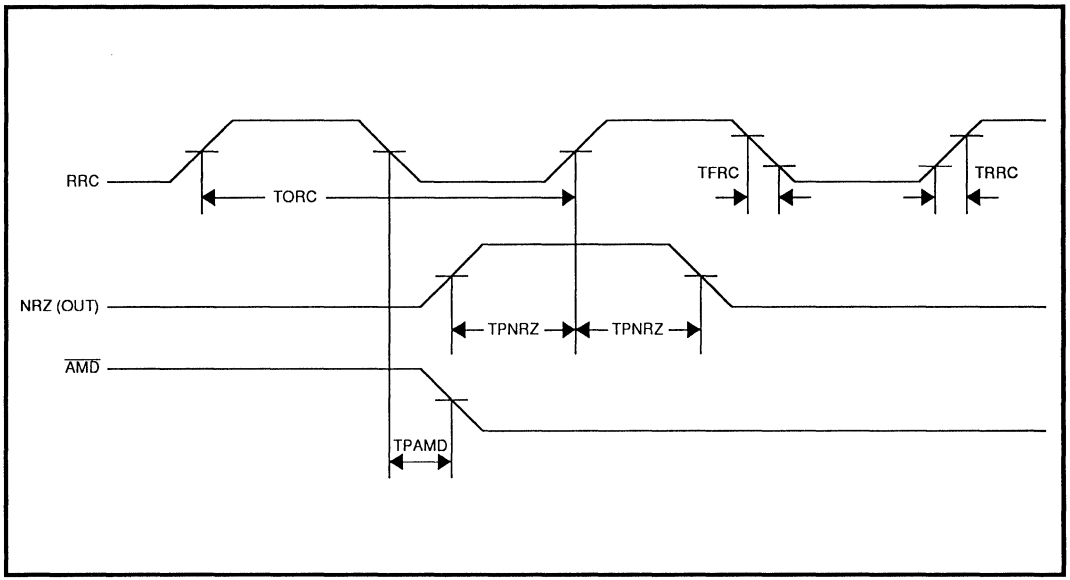


FIGURE 10: Read Timing

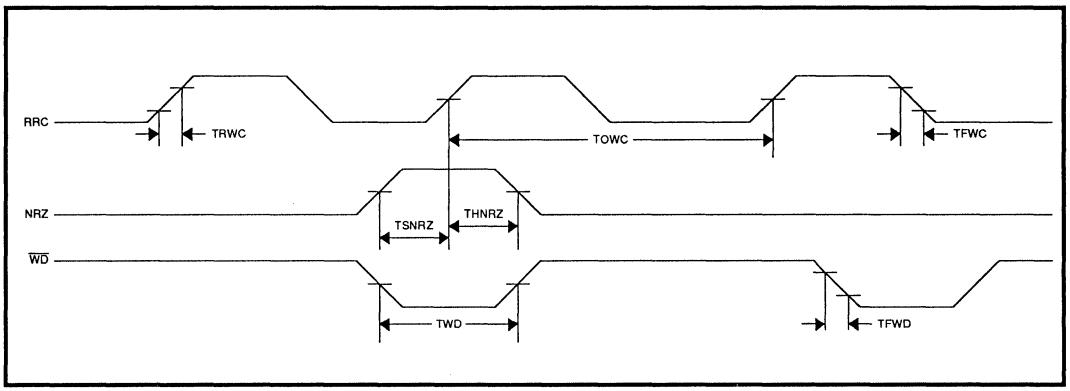
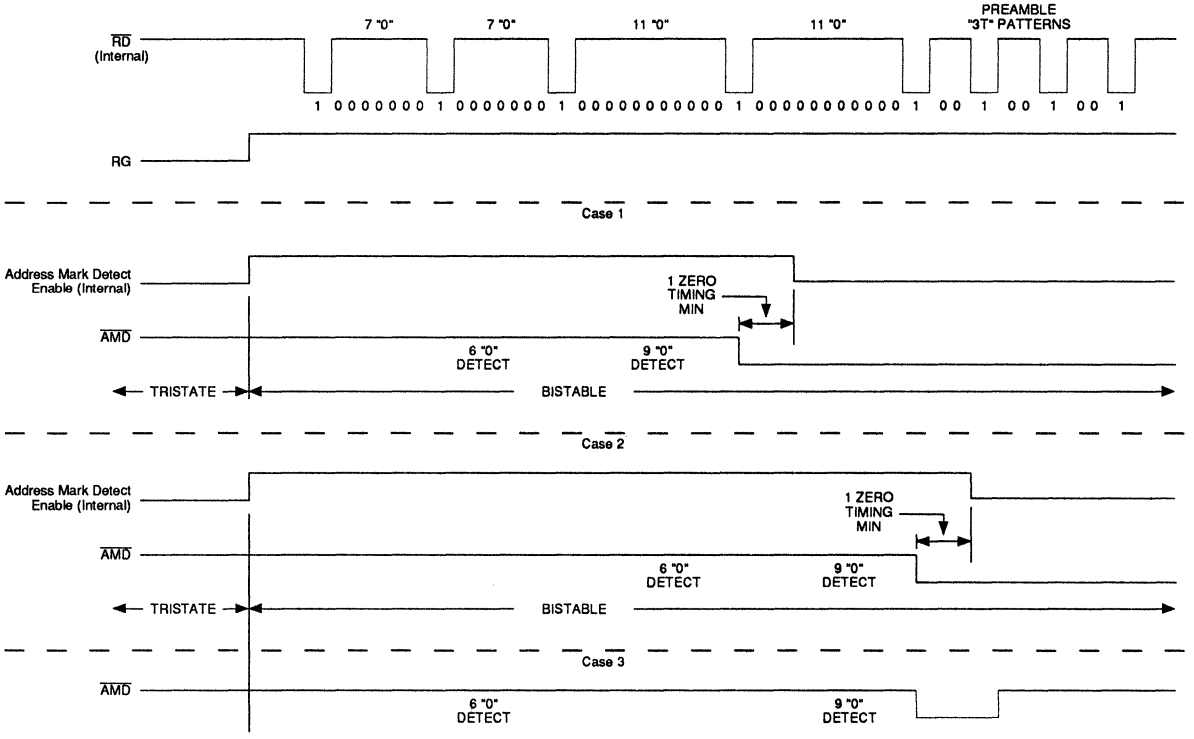


FIGURE 11: Write Timing



If 5 bits of RD are detected after 6 "0" and before 9 "0" are found, then restart and look for 6 "0."

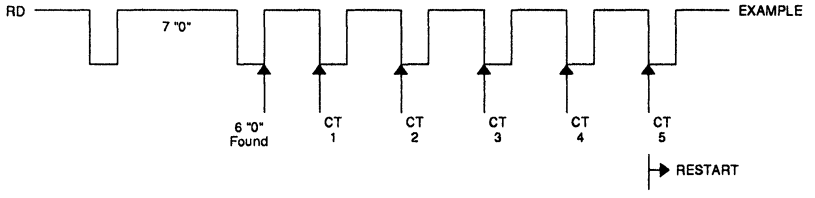
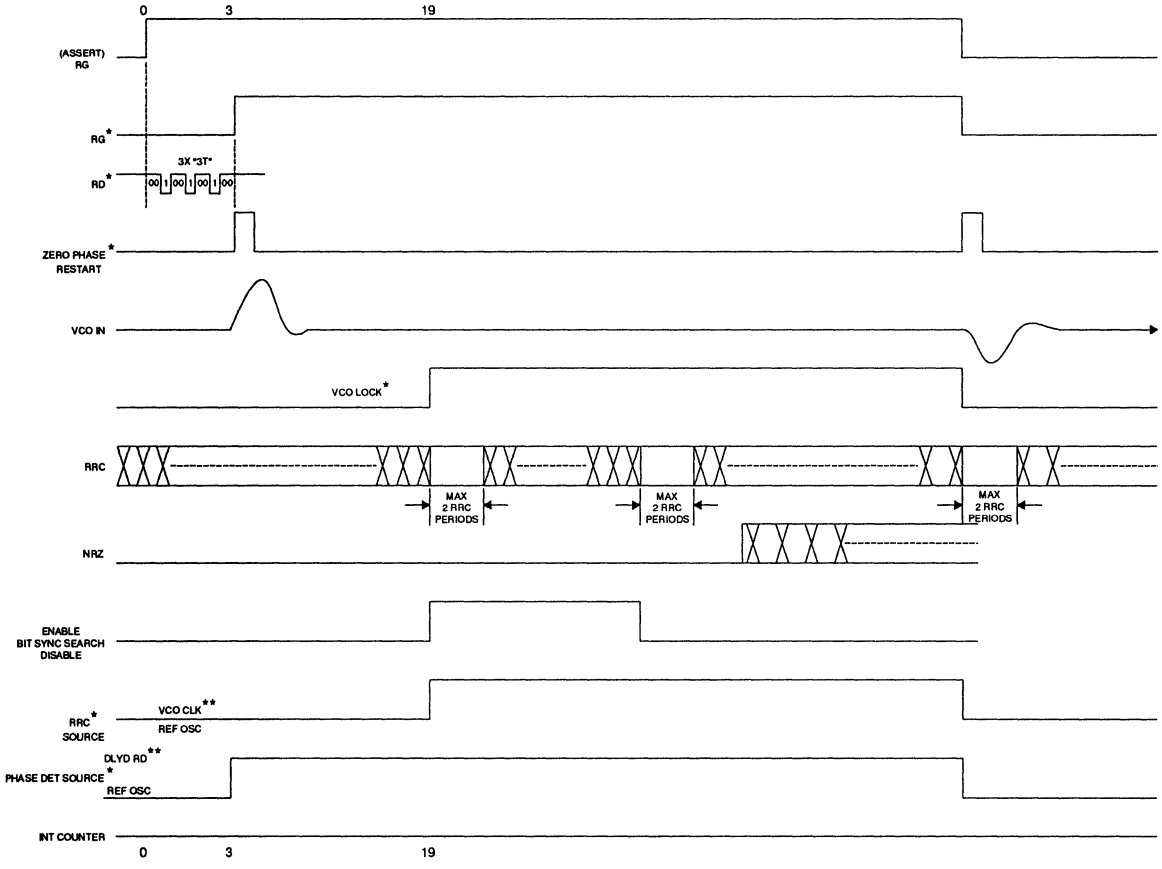


FIGURE 12: Address Mark Search



*= – Internal Source

** = – Test Point

FIGURE 13: Read Mode Locking Sequence (Soft and Hard Sector)

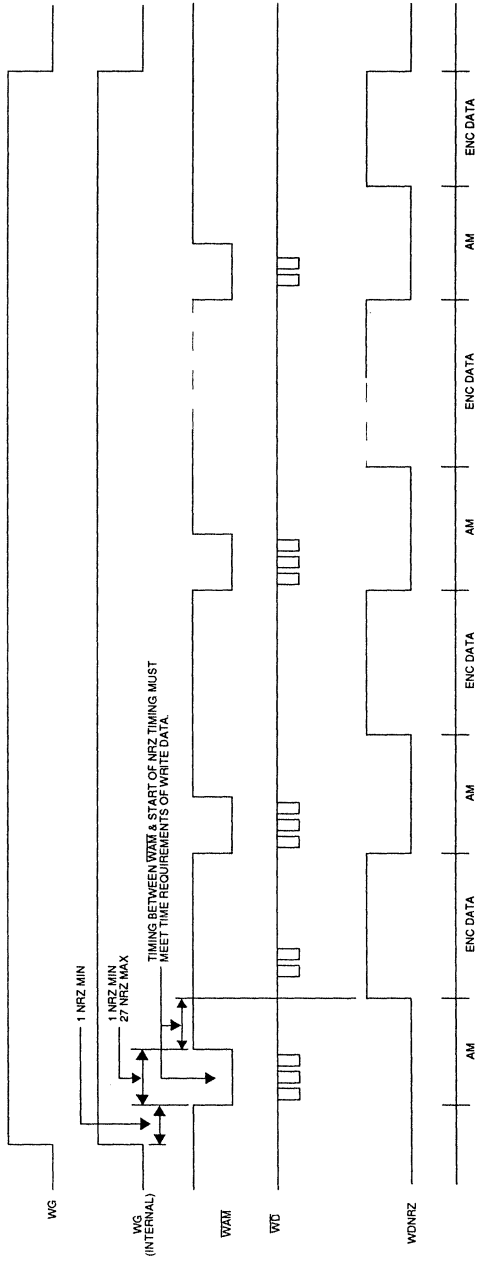


FIGURE 14: Multiple Address Mark Write

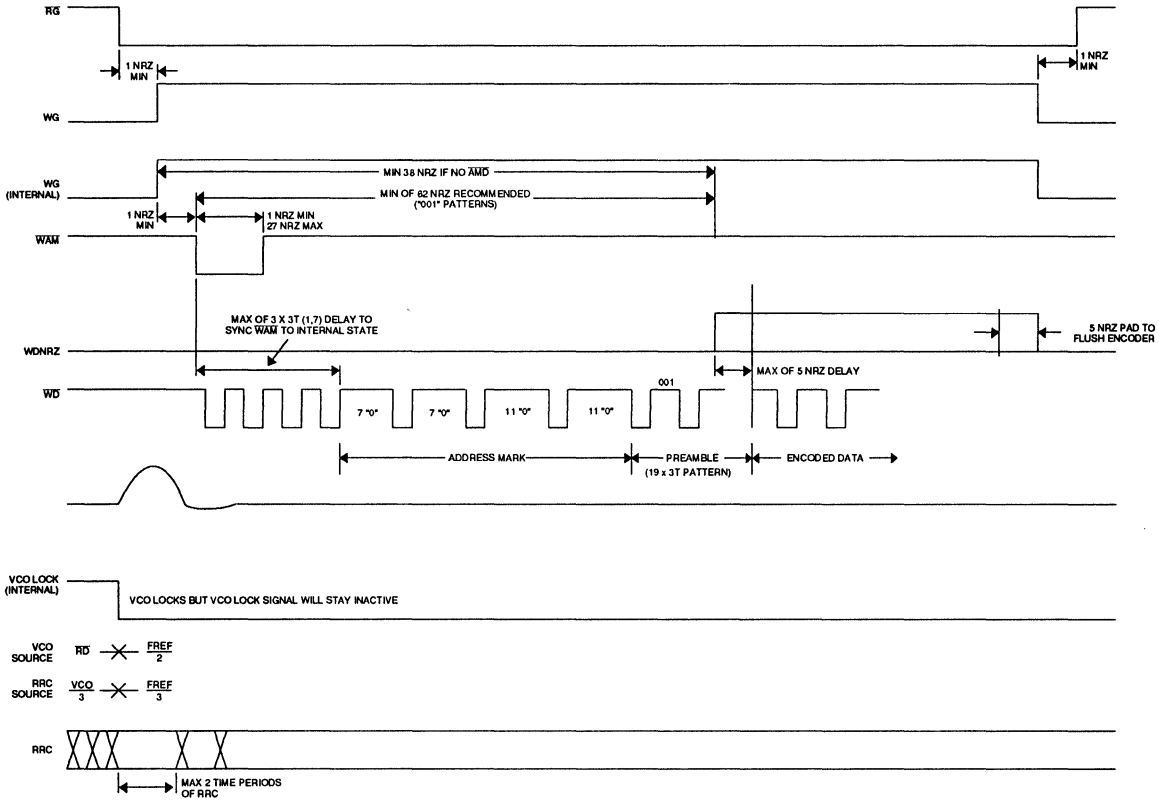


FIGURE 15: Write Data

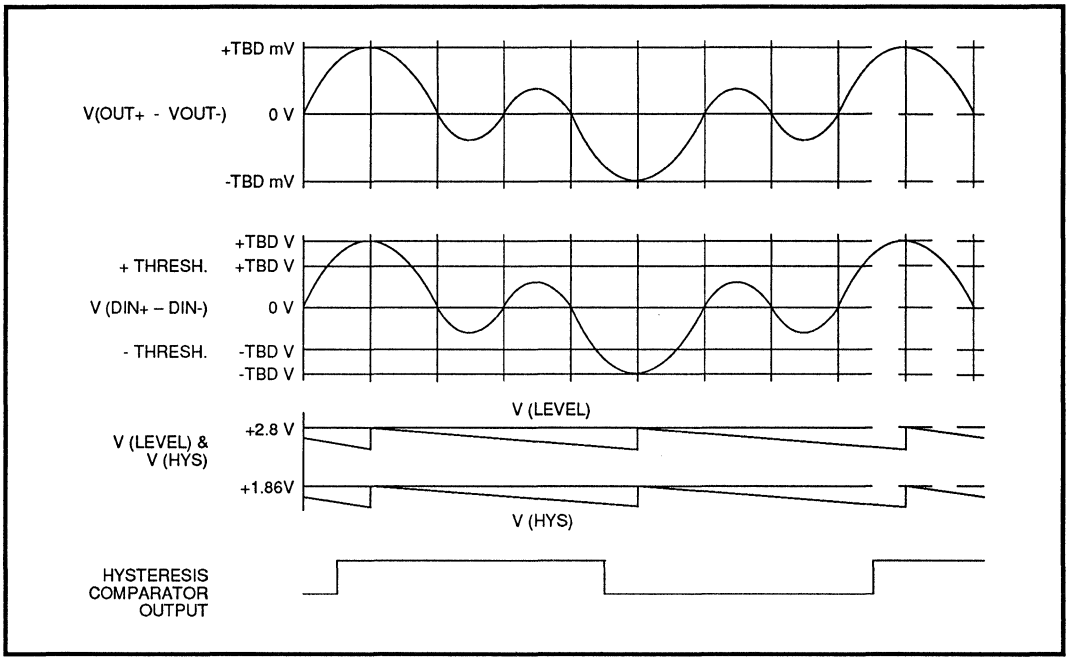


FIGURE 16: Expected Nominal Voltage Levels

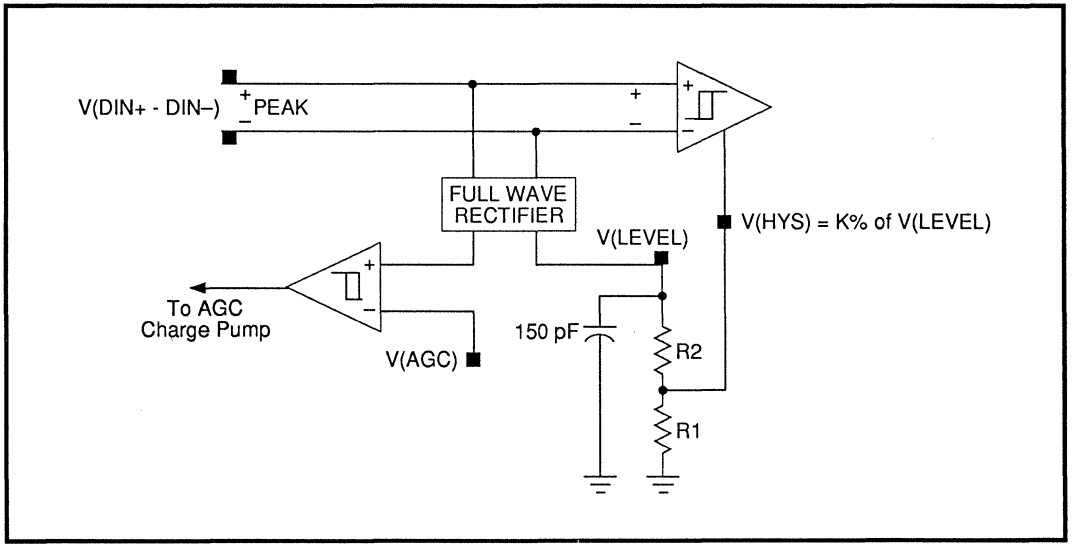


FIGURE 17: Feed Forward Mode

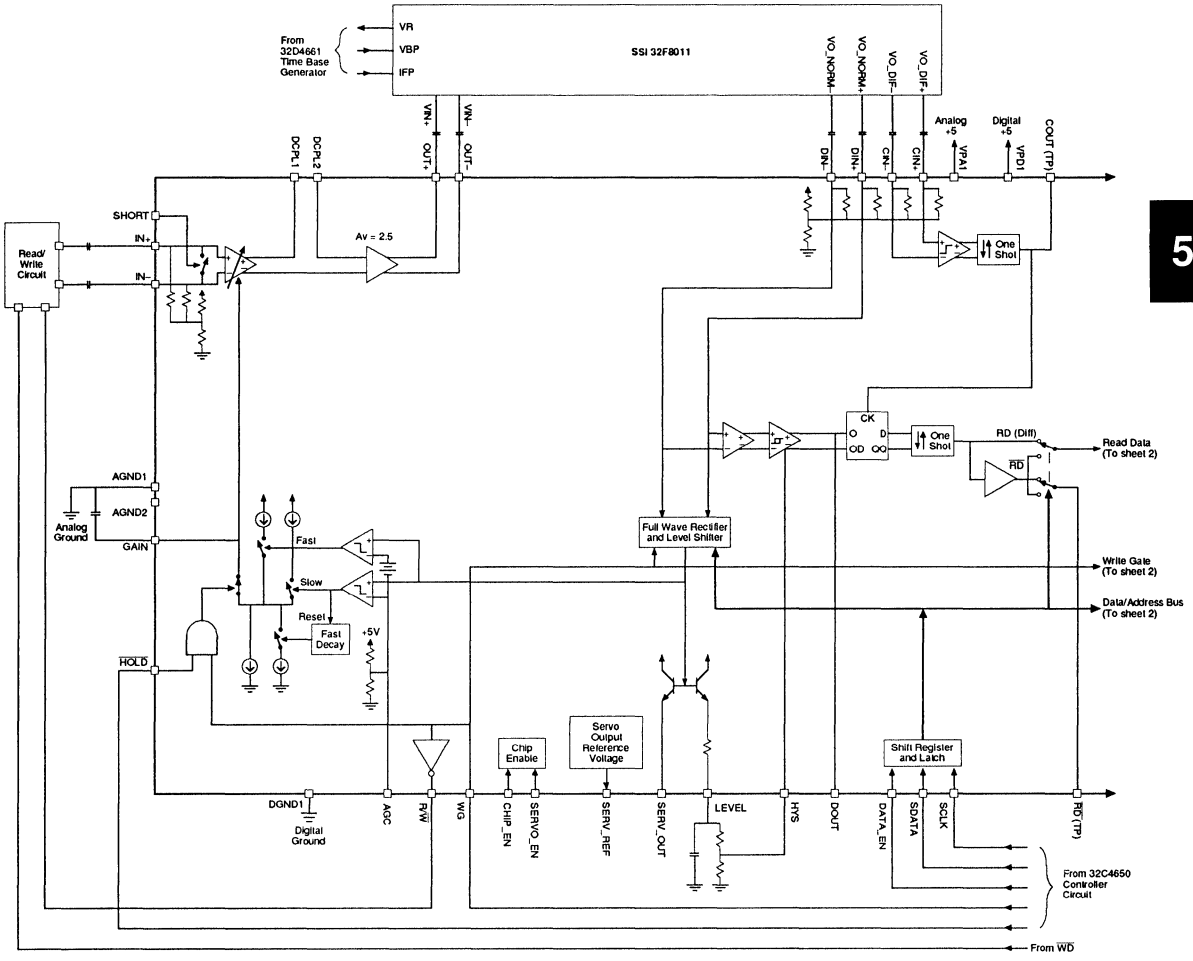


FIGURE 17a: SSI 32P4622 System Configuration (Sheet 1)

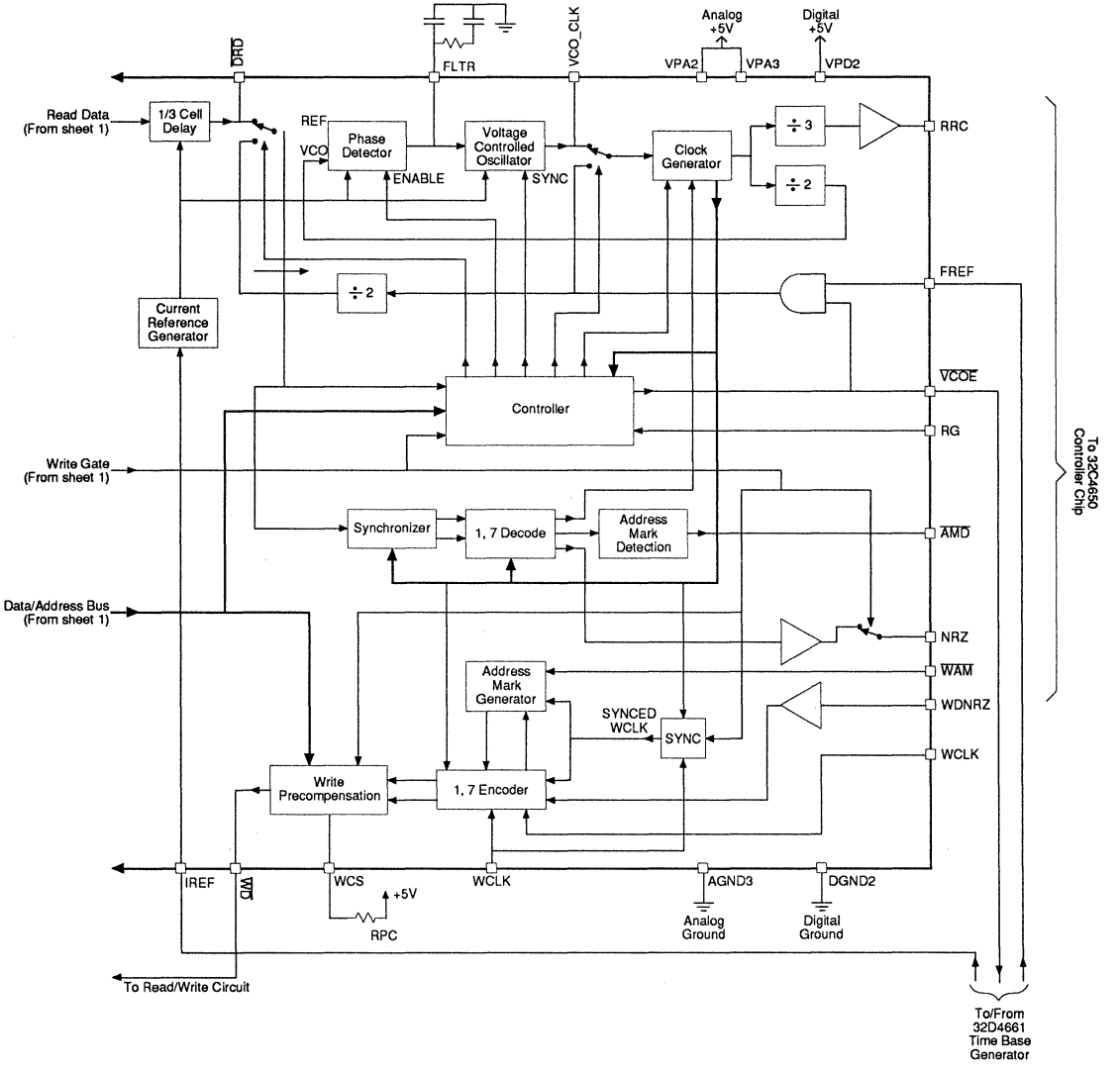


FIGURE 17b: SSI 32P4622 System Configuration (Sheet 2)

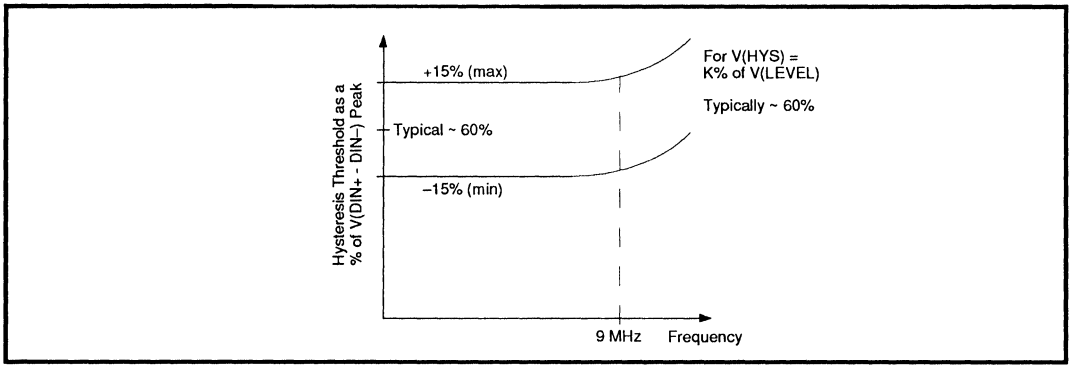
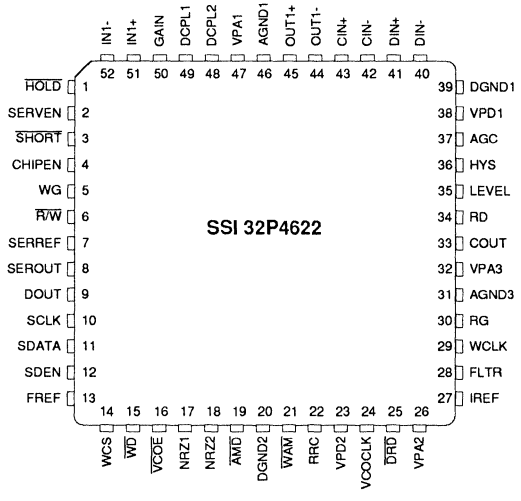


FIGURE 18: Percentage Threshold vs. Frequency

5

PACKAGE PIN DESIGNATIONS
(Top View)



52-pin QFP, PLCC

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 731-7110, FAX (714) 573-6914

Notes:

silicon systems®
A TDK Group Company

SSI 32P4720/4721
Pulse Detector & Data Separator

Advance Information

November 1991

DESCRIPTION

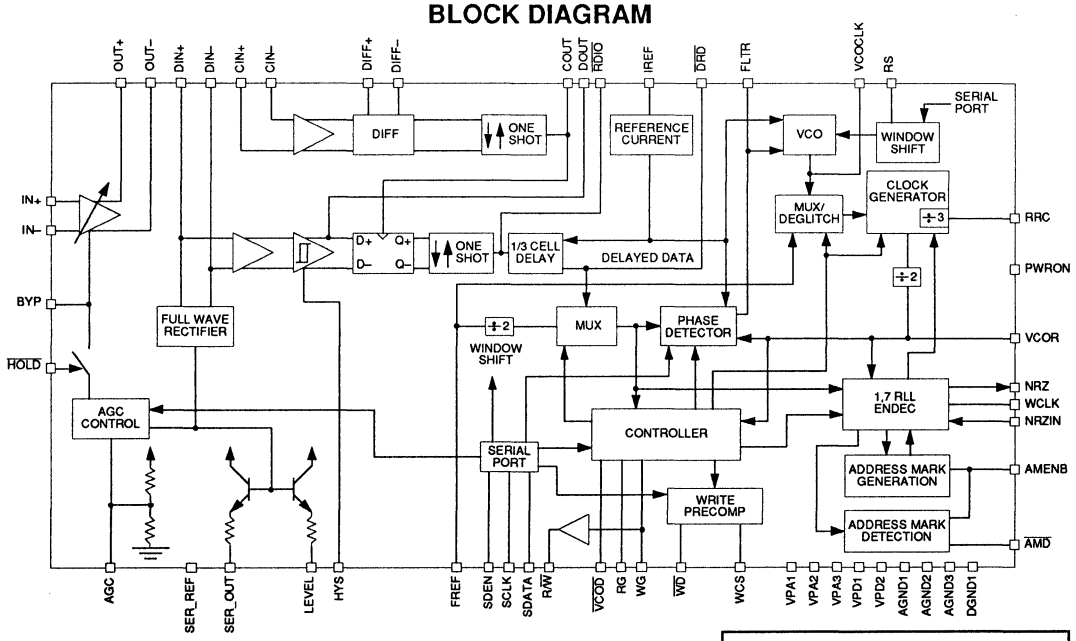
The SSI 32P4720/4721 is a low power, high performance bipolar device that provides pulse detection, data synchronization, and ENDEC electronics on a single integrated circuit. It supports RLL 1,7 data recording at rates programmable up to 24 Mbit/s and includes advanced features such as window shift and write precompensation control. The device reduces board layout space by including a fully integrated high-performance PLL with the VCO frequency setting elements incorporated on-chip. Data rate is programmed using an external resistor or, for constant density recording applications, an external current DAC. Control of the programmable features is provided through a simple, easy to use serial interface. The combination of these features along with a power-down mode, small footprint, and +5V only operation make the SSI 32P4720/4721 suitable for a wide variety of hard disk drive applications.

FEATURES

- **High performance pulse detector with:**
  - **Wide bandwidth AGC**
  - **Dual rate charge pump**
  - **Amplitude pulse qualification**
- **High performance data synchronizer with:**
  - **Fast acquisition PLL**
  - **Programmable write precompensation**
  - **Programmable window shift**
  - **1,7 RLL ENDEC**
- **Programmable data rate from 8 to 18 Mbit/s (4720) and 12 to 24 Mbit/s (4721)**
- **Servo burst and reference outputs**
- **Low power (<750 mW), 5V only operation**
- **Two power down modes (<15 mW power down mode)**
- **Available in 52-pin QFP & 52-pin PLCC packages**

5

BLOCK DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION

The SSI 32P4720/4721 is designed for use as a read pulse detector, data/clock recovery circuit, and write data encoder for RLL 1,7 code hard disk drive systems. In addition, it provides a servo burst output mode to support embedded servo applications.

PULSE DETECTOR CIRCUIT

The SSI 32P4720/4721 includes a complete pulse detection circuit that provides amplitude qualification of the incoming data signals during read mode operation. The pulse detector circuitry is optimized to operate with the SSI 32F8011 and SSI 32F8020 programmable filters as well as discrete filter implementations.

READ MODE OPERATION

AGC Amplifier

The initial stage of the pulse detector circuitry is a wide bandwidth AGC amplifier circuit that is capable of producing an output swing of 3 Vp-p maximum. This allows for operation with external filters that have up to 8 dB of loss. The gain of the AGC amplifier is a linear function of the voltage present on the BYP pin of the device (Figure 1.) The AGC is internally biased to maintain an input voltage of 1 Vp-p differential at the DIN+/- pins of the device. An external resistor can be connected to the AGC pin to adjust the AGC voltage either up (resistor to VPA3) or down (resistor to AGND3.) as shown in Figure 2. The desired AGC voltage level can be set using the following equations:

VAGC = [((5-V) x RINT) / (RINT + REXT)] + V (Fig. 2a)
or, VAGC = (V x REXT) / (RINT + REXT) (Fig. 2b)

where: V = 1.0 V (nominal)
RINT = 3.91 kΩ (typical)

When an external resistance is applied to the AGC pin, the signal level at DIN+/- will be:

$$DIN+/- = 1.0 \times V_{AGC}\ Vppd$$

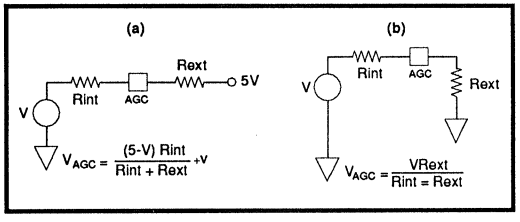


FIGURE 2: AGC Voltage

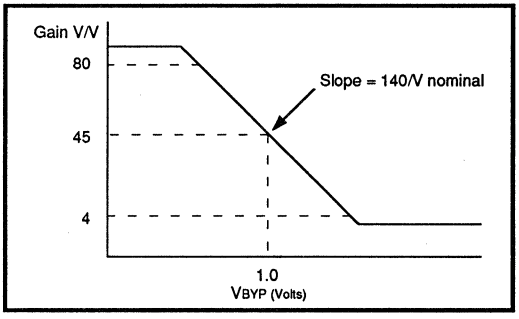


FIGURE 1: AGC Gain

An internal full-wave rectifier accepts the DIN+/- input signal and provides a rectified signal to the AGC circuit. Dual charge pumps in the AGC circuit provide both fast and slow attack modes to support rapid recovery during write to read transitions. When the DIN+/- signal level is greater than 125% of the desired level, the fast attack mode is entered and 1.3 mA of charge current is supplied to the BYP pin. When the DIN+/- input signal is between 100% and 125% of the desired level, the AGC switches to slow attack mode and 0.18 mA of charge current is supplied to the BYP pin.

The SSI 32P4720/4721 also provides two decay modes that are automatically controlled within the device. During write mode, the gain of the AGC circuit is automatically held to its previous value and the inputs to the AGC amplifier are placed into a low impedance state. When the device is switched from write mode to read mode the AGC circuit will maintain the low impedance state and hold the previous gain for 0.9 µs. After 0.9 µs, the AGC will go into either attack mode or decay mode depending upon the signal level at the DIN+/- pins. If the DIN+/- signal requires less gain, the AGC will go into attack mode. If the DIN+/- signal requires more gain, the AGC will go into the fast decay mode. In fast decay mode a discharge current of 120 µA is turned-on for a period of 0.9 µs or until the correct level is reached at the DIN+/- inputs. After the 0.9 µs period the device will remain in the slow decay mode with a discharge current of 4.5 µA.

DATA PATH (LEVEL QUALIFICATION)

In the data path of the SSI 32P4720/4721, the signal at the DIN+/- inputs is applied to an internal hysteresis comparator that provides level qualification of the incoming signal. The output of the hysteresis comparator serves as the input to a D flip-flop and is also provided

as an external pin (DOUT) for testing. The hysteresis level is determined by the voltage applied to the HYS pin. The voltage applied to the HYS pin can be either a fixed voltage or a percentage of the voltage at the DIN+/- inputs.

HYSTERESIS LEVEL CONTROL

In level qualification, hysteresis comparator eliminates errors due to low level additive noise. 32P4720/4721 allows two implementations of hysteresis: fixed hysteresis threshold or DIN tracking hysteresis threshold. Fixed hysteresis threshold can be simply done by a setting a DC voltage at HYS pin, such as from a resistor divider from VCC to GND. The hysteresis threshold at the comparator can be computed as: Hysteresis Gain x V_{HYS}. For high performance system application, however, fixed hysteresis threshold is not recommended.

DIN tracking hysteresis has the advantages of shorter write-to-read recovery time and lower probability of error with input amplitude drop out. The hysteresis threshold is designed as a percentage of the DIN peak voltage. This technique can be implemented by feeding the LEVEL output, through a resistor divider network, to the HYS pin. The LEVEL output, amplified peak capture of DIN voltage, can be computed as: Level Gain x V (DIN ± DIN-). With the resistor divider, a fraction of the LEVEL output is presented at the HYS pin. The hysteresis threshold, as a function of DIN, can be summarized as: Level Gain x Resistor Dividing Ratio x Hysteresis Gain x V(DIN ± DIN-). For a typical case of 1 Vpp differential at DIN± input, assume equal value resistors in the divider network, the hysteresis threshold is 1.0 x 0.50 x 0.36 x 1V = 0.18V. This represents 36% hysteresis on a 1 Vpp signal. While both the Level Gain and Hysteresis threshold vs HYS bear a moderate tolerance due to typical process variations, they inversely track each other to yield a much tighter hysteresis threshold in a closed loop. In designing the hysteresis threshold, the nominal Level Gain and Hysteresis Gain values should be used. The tolerance on DIN tracking hysteresis threshold is specified as the Tracking Hysteresis Tolerance in the specification.

While the external resistor divider ratio determines the hysteresis threshold, the total resistance and the peak capture capacitor should be optimized for the system data rate. The RC time constant must be small enough to allow good response to changing DIN ± peak-to-peak, but large enough to provide a constant hysteresis threshold in each level qualification.

CLOCK PATH (TIME QUALIFICATION)

The input signal at the CIN+/- pins goes through a differentiator circuit that converts signal peaks to zero crossings. The zero crossings are used to trigger a bi-directional one-shot that serves as the clocking input for the D flip-flop in the data path. The COUT pin is provided as a test point for monitoring the output of the one-shot. The differentiator function is provided by external components connected between the DIF+ and DIF- pins of the device. The transfer function from CIN+/- to the comparator input is:

$AV = (-3536 \times CS) / (LCS^2 + C(R + 52)S + 1)$,
where C, L, and R are external components
$15pF < C < 125pF$, and $S = jw = j2\pi f$

During normal operation, the time channel clocks the D flip-flop on every positive and negative peak of the CIN+/- input.

When the SSI 32P4720/4721 is used with an external filter that provides differentiated outputs (such as those of the SSI 32F8011 or SSI 32F8020), the differentiated outputs of the filter can be AC coupled to the CIN+/- inputs of the SSI 32P4720/4721. The differentiator components on the DIF+/- pins can then be replaced by a 2 KΩ external resistor.

WRITE MODE OPERATION

In the Write Mode, the SSI 32P4720/4721 pulse detector circuitry is disabled and preset for the Read Mode. The digital circuitry is shut-down to conserve power. The AGC amplifier gain is held at the previous value and the AGC input impedance is reduced. This reduces the write-to-read recovery time of the device and allows for improved settling of the coupling capacitors between the SSI 32P4720/4721 and the read/write preamplifier (such as the SSI 32R1200R.) The coupling capacitors should be as small as possible to allow for rapid settling while providing adequate bandwidth.

SERVO BURST CAPTURE

The SSI 32P4720/4721 provides a servo signal and an associated servo reference voltage. The SER_OUT pin is a rectified version of the DIN+/- input signal that can be used by an external servo demodulator circuit (such as the SSI 32H4631.) The SER_REF pin provides a reference voltage for the SER_OUT signal. The magnitude of the servo signal is the difference between the signal at the SER_OUT pin and the reference voltage at the SER_REF pin.

Additional servo support is provided by the SSI 32P4720/4721 through the RDIO pin. In the Servo Mode of operation, this pin provides a TTL output of the pulse detector read data.

DATA SEPARATOR

The SSI 32P4720/4721 is designed to perform data recovery and data encoding in rotating memory systems which utilize a 1,7 RLL encoding format. In the Read Mode the SSI 32P4720/4721 performs Data Synchronization, Sync Field Search and Detect, Address Mark Detect, and Data Decoding. In the Write Mode, the SSI 32P4720/4721 converts NRZ data into the 1,7 RLL format described in Table 2, performs Write Precompensation, generates the Preamble Field, and inserts Address Marks as requested.

The SSI 32P4720/4721 can operate with data rates ranging from 8 to 24 Mbit/s. This data rate is established by a single 1% external resistor, RR, connected from pin IREF to VPA2. This resistor establishes a reference current which sets the VCO center frequency, the phase detector gain, and the 1/3 cell delay. The value of this resistor is given by:

$$RR = \frac{77.4}{DR} - 2.1(k\Omega) \quad (32P4720)$$

$$RR = \frac{93}{DR} - 1.7(k\Omega) \quad (32P4721)$$

where: DR = Data Rate in Mbit/s.

For zoned recording applications an external current DAC (such as that provided in the SSI 32D4661) can be directly connected to the IREF pin. The current required to set a given data rate would be determined by:

$$I_{IN} = 4.3/\,[(77.4/DR) - 1.57]\ (mA)\ (32P4720)$$

$$I_{IN} = 4.3/\,[(93/DR) - 1.17]\ (mA)\ (32P4721)$$

A reference clock, operating at 3x the data rate, generates the standby reference for the PLL. Either an attenuated external TTL compatible reference or an AC coupled ECL source may be applied to FREF.

The SSI 32P4720/4721 employs a Dual Mode Phase Detector; Harmonic in the Read Mode and Non Harmonic in Write and Idle Modes. In the Read Mode the Harmonic Phase Detector updates the PLL with each occurrence of a DYLD DATA pulse. In the Write and Idle modes the Non-Harmonic Phase Detector is continuously enabled, thus maintaining both phase and frequency lock. By acquiring both phase and frequency lock to the crystal reference oscillator and utilizing a zero phase restart technique, false lock to delayed data is eliminated.

The phase detector incorporates a charge pump in order to drive the loop filter directly. The polarity and width of the output current pulses correspond to the direction and magnitude of the phase error.

The READ GATE (RG), and WRITE GATE (WG) inputs control the device mode.

RG is an asynchronous input and may be initiated or terminated at any position on the disk. WG is also an asynchronous input, but should not be terminated prior to the last output Write Data pulse.

READ OPERATION

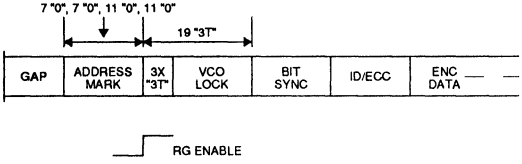
The Data Synchronizer utilizes a fully integrated fast acquisition PLL to accurately develop the decode window. Read Gate, RG, initiates the PLL locking sequence and selects the PLL reference input; a high level (Read Mode) selects the RD input and a low level selects the crystal reference oscillator.

In the Read Mode the falling edge of DRD enables the Phase Detector while the rising edge is phase compared to the rising edge of the VCO. As depicted in Figure 3, DRD is a 1/3 cell wide (TVCO) pulse whose leading edge is defined by the leading edge of RD. A decode window is developed from the VCO clock. Shifting the phase of the VCO clock effectively shifts the relative position of the DRD pulse within the decode window. Decode window control is provided via the WS controls.

In Non-Read Modes, the PLL is locked to the external reference clock. This forces the VCO to run at a frequency which is very close to that required for tracking actual data and thus minimizes the associated frequency step during acquisition. When the reference input to the PLL is switched, the VCO is stopped momentarily, then restarted in an accurate phase alignment with the next PLL reference input pulse, and the VCO clock divider is reset.

SOFT SECTOR

The disk operation lock sequence in Read Mode for Soft Sector Operation is shown below.



ADDRESS MARK DETECT

In Soft Sector Read Operation the SSI 32P4720/4721 must first detect an address mark to be able to initiate the rest of the read lock sequence. An address mark for the SSI 32P4720/4721 consists of two (2) 7 "0" patterns followed by two 11 "0" patterns. To begin the read lock sequence the Address Mark Enable (AMENB) is asserted high by the controller. The SSI 32P4720/4721 Address Mark Detect (AMD) circuitry then initiates a search of the read data (RD) for an address mark. First the AMD looks for a set of 6 "0's" within the 7 "0" patterns. Having detected a 6 "0" the AMD then looks for a 9 "0" set within the 11 "0's." If AMD does not detect 9 "0's" within 5 RD bits after detecting 6 "0's" it will restart the Address Mark Detect sequence and look for 6 "0's." When the AMD has acquired a 6 "0," 9 "0" sequence the $\overline{AMD}$ transitions low. $\overline{AMD}$ will remain low for the duration of AMENB. When AMENB is released, $\overline{AMD}$ will be released by the SSI 32P4720/4721.

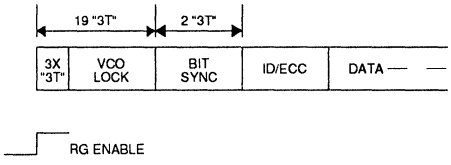
PREAMBLE SEARCH

After the Address Mark (AM) has been detected a Read Gate (RG) can be asserted initiating the remainder of the read lock sequence. When RG is asserted an internal counter counts transitions of the incoming Read Data, (RD looking for 3 consecutive '3T's). Once the counter reaches count 3 (finds (3) consecutive 3T preamble) the internal read gate enables switching the phase detector from the reference oscillator to the delayed Read Data input (DRD); at the same time a zero phase (internal) restart signal restarts the VCO in phase with the DRD. This prepares the VCO to be synchronized to data when the bit sync circuitry is enabled after VCO lock is established.

VCO LOCK & BIT SYNC ENABLE

When the internal counter counts 16 more "3T" or a total of 19 positive transitions from RG enable, an internal VCO lock signal enables. The VCO lock signal activates the decoder bit synchronization circuitry to define the proper decode boundaries. Also, at count 19, the RRC source switches from the external reference clock to the VCO clock signal which is phase locked to DRD. The VCO is assumed locked at this point. A maximum of 2 RRC time periods may occur for the RRC transition, however, no short duration glitches will occur. Also at this time, the $\overline{VCOD}$ line is brought low to disable the external reference clock and reduce jitter. Two additional "3T" are required for internal bit sync. After the bit sync circuitry sets the proper decode window (VCO in sync with RRC and RRC in sync with data) NRZ is enabled and data is toggled in to be decoded for the duration of the read gate.

HARD SECTOR



In hard sector operation a low AMENB disables the SSI 32P4720/4721's Address Mark Detection circuitry and AMD remains inactive. A hard sector read operation does not require an address mark search but starts with a preamble search as with soft sector and sequences identically. In all respects, with exception to the address mark search sequence, hard sector read operation is the same as soft sector read.

WRITE MODE

In the Write Mode the SSI 32P4720/4721 converts NRZ data from the controller into 1,7 RLL formatted data for storage on the disk. The SSI 32P4720/4721 can operate with a soft or hard sector hard drive.

In soft sector operation the device generates a "7, 7, 11, 11" Address Mark, and a preamble pattern.

In the hard sector operation the device generates a 19 x "3T" preamble pattern but no preceding Address Mark. The NRZIN pin must be kept low for the duration of the preamble pattern. The NRZ input data is clocked on the rising edges of WCLK.

Write precompensation circuitry is provided to compensate for media bit shift caused by intersymbol interference. The SSI 32P4720/4721 recognizes specific write data patterns and can add or subtract delays in the time position of write data bits to

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counteract the read back bit shift. The magnitude of the time shift, TPC, is determined by an external resistor on the WCS pin and by value of write precomp register.

The SSI 32P4720/4721 performs write precompensation according to the algorithm outlined in Table 4.

SOFT SECTOR

In soft sector operation, when Read Gate (RG) transitions low, VCO source and RRC source switch from RD and VCO/3, respectively, to the external reference clock. At the same time the VCO (internal) lock goes inactive but the VCO is locked to the external reference clock. After a delay of 1 NRZ time period (min) from RG low, the Write Gate (WG) can be enabled while NRZIN is maintained (NRZ write data) low. The Address Mark Enable (AMENB) is made active (high) a minimum of 1 NRZ time period later. The Address Mark (consisting of 7 "0's," 7 "0's," 11 "0's,"11 "0's") and the 19 x "3T" Preamble is then written by WD. While the preamble is being written, the encoder is active. Therefore, WCLK must be clocking in an all "0" NRZIN pattern. The first non-zero NRZIN input bit indicates the end of the preamble pattern. After a delay of 10-12 NRZIN bit time periods, non preamble data begins to toggle out WD. Finally, at the end of the write cycle, 16 bits of blank NRZ time passes to ensure the encoder is flushed of data; WG goes low. WD stops toggling a maximum of 2 NRZ time periods after WG goes low.

HARD SECTOR

In hard sector operation, when read gate (RG) transitions low, the write sequence is the same as the soft sector operation except the AMENB (address mark enable) is kept low.

The SSI 32P4720/4721 then sequences from RG disable to WG enable and NRZIN input is active as in soft sector operation.

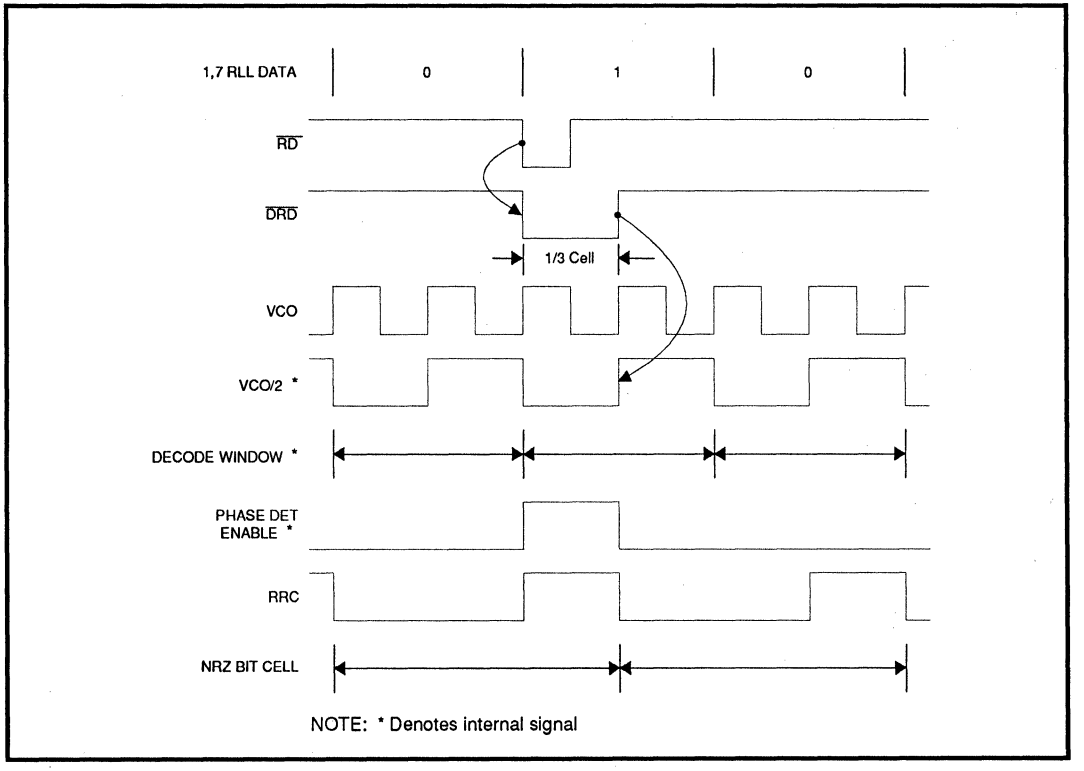

FIGURE 3: Data Synchronization Waveform

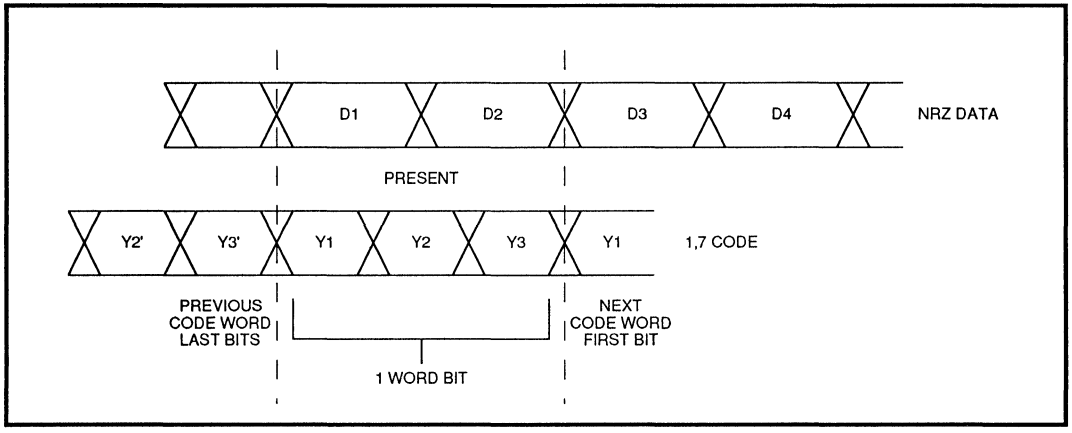

FIGURE 4: NRZ Data Word Comparision to 1, 7 Code Word Bit (See Table 1, for Decode Scheme)

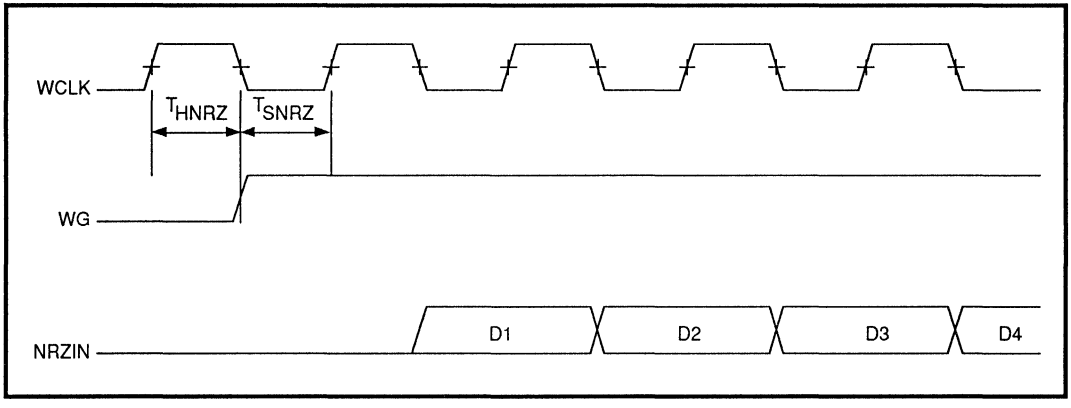

FIGURE 5: WG Timing Requirement for Predictable Write Encoding

A decodable write pattern will always be generated, regardless of the phasing of WG. However, a repeatable write pattern will be generated only if WG satisfies the same WCLK setup and hold requirements as the NRZIN data.

TABLE 1: Decode Table

ENCODED READ DATA			DECODED DATA	
Previous	Present	Next		
Y Y	Y Y Y	Y Y Y	D D	
2' 3'	1 2 3	1 2 3	1 2	
0 0	0 0 0	X X X	0 1	
1 0	0 0 0	X X X	0 0	
0 1	0 0 0	X X X	0 1	
X X	1 0 0	X X X	1 1	
X 0	0 1 0	0 0	1 1	
X 0	0 1 0	1 0	1 0	
X 0	0 1 0	0 1	1 0	
X 1	0 1 0	0 0	0 1	
X 1	0 1 0	1 0	0 0	
X 1	0 1 0	0 1	0 0	
0 0	0 0 1	X X	0 1	
1 0	0 0 1	X X	0 0	
0 1	0 0 1	X X	0 0	(Preamble)
X X	1 0 1	X X	1 0	

TABLE 2: Encode Table

NRZ DATA				ENCODED WRITE DATA			
Present		Next		Previous	Present		
D	D	D	D	Y	Y	Y	Y
1	2	3	4	3	1	2	3
0	0	0	X	0	0	0	1
0	0	1	X	0	0	0	0
0	0	1	X	1	0	1	0
1	0	0	X	0	1	0	1
1	0	1	X	0	0	1	0
0	1	0	0	0	0	0	1
0	1	0	0	1	0	1	0
0	1	1	0	0	0	0	0
0	1	1	0	1	0	0	0
0	1	0	1	0	0	0	1
0	1	0	1	1	0	0	0
0	1	1	1	0	0	0	0
0	1	1	1	1	0	0	0
1	1	0	0	0	0	1	0
1	1	1	0	0	1	0	0
1	1	0	1	0	1	0	0
1	1	1	1	0	1	0	0

NOTE: X = Don't Care

TABLE 3: Clock Frequency

WG	RG	VCO REF	RRC	DECCLK	ENCCLK	MODE
0	0	FREF/2	FREF/3	FREF/2	FREF/2	IDLE
0	1	$\overline{RD}$	VCO/3	VCO/2	FREF/2	READ
1	0	FREF/2	FREF/3	FREF/2	FREF/2	WRITE
1	1	FREF/2	FREF/3	FREF/2	FREF/2	UNDEFINED

Note 1: Until the VCO locks to the new source, the VCO/2 entries will be FREF/2.
2: Until the VCO locks to the new source, the VCO/3 entries will be FREF/3.

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TABLE 4: Write Precompensation Algorithm

BIT	BIT	BIT	BIT	BIT	COMPENSATION
n-2	n-1	n	n+1	n+2	BIT n
1	0	1	0	1	NONE
0	0	1	0	0	NONE
1	0	1	0	0	EARLY
0	0	1	0	1	LATE

LATE: Bit n is time shifted (delayed) from its nominal time position towards the bit n+1 time position.

EARLY: Bit n is time shifted (advanced) from its nominal time position towards the bit n-1 time position.

MODE CONTROL

The operating modes of the SSI 32P4720/4721 are controlled with the RG, WG, AMENB, and PWRON pins and by bits in the test mode control register and power mode control register. The SSI 32P4720/4721 has three operating modes: Read Mode, Write Mode and Servo Mode. In addition, there are the Idle Mode and Sleep Mode for reduced power consumption.

WG	RG	AMENB	TEST BIT	SERVO BIT	SLEEP BIT	PWRON	MODE
X	X	X	X	X	X	0	Power Down. All functions of the device are powered down. The serial port must be reprogrammed when returning from this mode.
X	X	X	X	X	1	1	Sleep Mode. All functions of the device are powered down except the serial port registers. Data is retained in the registers.
0	0	X	0	1	0	1	Servo Mode. The AGC is active, the data separator is powered down, and rectified AGC data is available at the SER_OUT pin. The $\overline{\text{RDIO}}$ output buffer can be made active to monitor servo timing data.
0	0	X	1	0	0	1	Test Mode. The $\overline{\text{RDIO}}$ pin is set as an input buffer. TTL read data can be driven into the $\overline{\text{RDIO}}$ pin to test the data separator. AMENB pin determines hard/soft sector mode.
0	0	0	0	0	0	1	Idle Mode. AGC is active, VCO is locked to the external reference clock.
0	0	1	0	1	0	1	Address mark search mode. The $\overline{\text{AMD}}$ pin is driven high, the AGC is active, the VCO is locked to the external reference, NRZ is Hi-Z, and the data separator searches for the address mark pattern.
0	1	0	1	0	0	1	Read Mode. The AGC is active, the VCO switches from external reference to internal $\overline{\text{DRD}}$ after detection of 3 x 3T patterns. After 19 x 3T the RRC switches from the external reference to the internal $\overline{\text{DRD}}$ and the NRZ output is made active.
0	1	1	1	0	0	1	Illegal state. RG should not be made active until after the AMENB pin is released.

MODE CONTROL (continued)

WG	RG	AMENB	TEST BIT	SERVO BIT	SLEEP BIT	$\overline{PWR}$ $\overline{DWN}$	MODE
1	0	0	0	0	0	1	Write Mode. The AGC gain is held and the input impedance is reduced, NRZ pin is Hi-Z, and the VCO is locked to the external reference. A preamble pattern is generated, $\overline{WD}$ is active, NRZIN data is encoded.
1	0	1	0	0	0	1	Write Address Mark. The AGC gain is held and the input impedance is reduced, NRZ pin is Hi-Z, and the VCO is locked to the external reference. An address mark and preamble pattern are generated, $\overline{WD}$ is active, NRZIN data is encoded.
1	1	X	0	0	0	1	Illegal state. RG and WG should not be made active at the same time.

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POWER DOWN MODES

The SSI 32P4720/4721 provides three power saving modes to support servo only and shut-down operations. In the Servo Mode, the pulse detector and servo circuitry is operational while the data separator circuitry is placed into power down mode. Operating power in this mode is 235 mW. In the Sleep Mode, the registers in the serial port remain powered-up so that programming information is retained. Operating power in this mode is 40 mA. For complete shut-down, a power down mode is provided that removes power from all circuits in the device. During this mode, the serial port registers are powered down and programming data must be rewritten to the device upon coming out of Power Down Mode. Power dissipation in Power Down Mode is less than 15 mW.

SERIAL PORT OPERATION

The SSI 32P4720/4721 provides a simple serial port interface that allows programming of the device's internal registers. The write-only serial port is a three-line interface that requires an enable signal (SDEN) along with clock (SCLK) and data (SDATA) signals to program the internal registers of the SSI 32P4720/4721. Data is shifted into the registers in 8-bit bytes that are divided into four bits of address and four bits of data. To load data into the device, the enable pin (SDEN) is asserted for eight clock cycles during which data can be presented on the SDATA input pin. Data on the SDATA pin is clocked into the device on the falling edges of the clock signal provided on the SCLK pin. The falling edge of SDEN latches the data internally and intitiates the function selected. To save power the serial port circuitry is powered down when the SDEN line is low. Because of this, there is a minimum set-up and hold time for the SDEN signal (refer to specifications.) Address mapping for the serial port is as follows:

SERIAL PORT ADDRESS MAP

Address	Register Function
0 0 0 0	Test Mode Control Register
0 0 0 1	Write Precomp Control Register
0 0 1 0	Window Shift Control Register
0 0 1 1	Power Mode Control Register

Note: At Power-Up, all register bits are reset to "0."

TEST MODE CONTROL REGISTER MAPPING

REGISTER BIT	FUNCTION
X X X 0	Selects the signal source for the VCOR, VCO_CLK, and $\overline{DRD}$ test pins. "0" VCOR pin = VCOR DRD* pin = DRD* VCO_CLK pin = VCO_CLK "1" VCOR pin = phase detector pump-down DRD* pin = phase detector pump-up VCO_CLK pin = Disable detector
X X 0 X	Controls the test buffers on VCOR, VCO_CLK, and $\overline{DRD}$ test pins. "0" = test buffers disabled "1" = test buffers enabled
X 0 X X	Selects the data separator input source. "0" = Pulse detector data input to the data separator "1" = RDIO input data to the data separator
0 X X X	Selects the source of the test point signals for VCOR, VCO_CLK, and DRD. "0" = VCO signals are available "1" = FREF signals are available

WRITE PRECOMP CONTROL REGISTER MAPPING

X 0 0 0	No write precompensation selected
X 0 0 1	Minimum precompensation (1X)
"	
X 1 1 1	Maximum precompensation (7X)
0 X X X	Controls the phase detector. "0" = Normal phase detector operation "1" = Phase detector disabled (coast mode)

WINDOW SHIFT CONTROL REGISTER MAPPING

0 0 0 0	No window shift selected
0 0 0 1	Minimum window shift selected (1X)
"	
1 1 1 1	Maximum window shift selected (16X)

POWER MODE CONTROL REGISTER MAPPING

X X X 0	Selects the window shift direction "0" = Early window shift "1" = Late window shift
X X 0 X	Controls the RDIO TTL output buffer (subordinate to the Test Mode Control Register bit X0XX.) "0" = RDIO buffer disabled (Hi-Z) "1" = RDIO buffer enabled
X 0 X X	Controls the "Servo" power down mode. "0" = Selects normal operation "1" = Selects Servo Mode. The data separator is powered down.
0 X X X	Controls the chip "Sleep" power down mode. "0" = Selects normal operation "1" = Selects Sleep Mode. Only the serial port registers are powered up.

PIN DEFINITION (PRELIMINARY)

NAME	TYPE	DESCRIPTION
AGC	I	AGC Reference. Voltage level input for setting the signal level for the read data AGC loop.
AGND	I	Analog ground pin for the data separator section.
AGND3	I	Analog ground pin for the pulse detector section.
AGND4	I	Digital ground pin for the pulse detector section.
AMENB	I	Address Mark Enable. Active High level TTL input that enables the address mark detect and generation circuitry. This pin has an internal pull-up resistor.
BYP	I	Bypass. An AGC timing capacitor is connected between this pin and AGND1 to set the AGC gain control.
CIN+, CIN-	I	Clock Inputs. Analog input signals to the differentiator in the pulse detector clock circuit.
DGND	I	Digital ground for TTL output buffers.
DIN+, DIN-	I	Data Inputs. Analog input signals to the hysteresis comparator and full-wave rectifier circuits of the pulse detector.
FREF	I	Frequency reference input for the internal PLL.
$\overline{\text{HOLD}}$	I	Active low TTL compatible input that holds the present AGC gain value.
HYS	I	Hysteresis Level. Voltage level input that sets the trip level for the hysteresis comparator.
IN+, IN-	I	Analog input data from the read/write preamplifier.
IREF	I	Current input for programming the VCO center frequency, phase detector gain, and the 1/3 cell delay. Current can be set with an external resistor to VPA2 or by an external current DAC.
WCS	I	Write Precompensation Set. Pin for reference current to set the write precompensation magnitude value. A resistor is connected from WCS to VPA.
$\overline{\text{RDIO}}$	I/O	Read Data Test Point. Bidirectional test pin that is a TTL compatible read data output during servo mode and a read data input during the test mode. In test mode, a read data signal applied to this pin goes into the data separator, bypassing the pulse detector circuit.
RS	I	Analog input for adjusting the window symmetry. An external resistor connected between this pin and VPA3 provides magnitude control of the window shift symmetry.
RG	I	Read Gate. A high TTL level selects read mode and enables the PLL to lock to the incoming read data. A low level allows the PLL to lock to the external reference signal at FREF.
SCLK	I	TTL compatible. Serial port clock input used for clocking in data on the SDATA pin. The clock source for this pin should be externally gated with the SDEN signal.
SDATA	I	TTL compatible. Serial port input data.
SDEN	I	TTL compatible. Serial port enable input.
PWRON	I	Active high TTL input signal that enables the device. When this pin is brought low it puts the device into a complete power down mode.
VPA1	I	+5V analog power input.

PIN DEFINITION (PRELIMINARY) (Continued)

NAME	TYPE	DESCRIPTION
VPA1	-	+5V analog power supply for data separator.
VPA2	-	+5V digital power supply for data separator.
VPA3	-	+5V power supply for pulse detector.
VPA4	-	+5V digital power supply for pulse detector.
VPD	-	+5V digital power for TTL output buffers.
NRZIN	I	NRZ Input Data. TTL compatible NRZ write data input.
WCLK	I	Write Clock. TTL level clock that is synchronous with the data on NRZIN pin.
WG	I	Write Gate. Active high TTL compatible input that enables the write mode.
$\overline{\text{AMD}}$	O	Address Mark Detect. Active low level TTL compatible signal that indicates successful detection of an address mark during read mode. High impedance when in write mode.
COUT	O	Test point signal for monitoring the output of the pulse detector clock flip-flop. An external pull-down resistor is required to use this pin (5kΩ)
DIFF+, DIFF-	O	Pins for implementing the external differentiator network for the pulse detector clocking circuit.
DOUT	O	Test point signal for monitoring the output of the pulse detector data flip-flop. An external pull-down resistor is required to use this pin (5kΩ)
$\overline{\text{DRD}}$	O	A multiplexed open emitter test signal. When RG is high the output is the DRD signal from the 1/3 cell delay. When RG is low the output is the PLL reference clock. External pull-up and pull-down resistors are required to use this pin. They should be disconnected during operation to reduce power consumption.
FLTR	O	This is the output of the phase detector to which the loop filter must be connected.
LEVEL	O	Open emitter output from the full-wave rectifier that can be used for the HYS pin input voltage.
NRZ	O	TTL compatible NRZ output data that is synchronous to the read reference clock.
OUT+, OUT-	O	Differential outputs of the AGC amplifier.
SER_OUT	O	Full-wave rectified output of the signal appearing at the DIN± inputs.
RRC	O	Read Reference Clock. TTL compatible clock that is synchronous to NRZ out data during read mode. During write mode the RRC is the FREF divided by three.
R/$\overline{\text{W}}$	O	READ/$\overline{\text{WRITE}}$. TTL level output that is an inverted version of the WG input pin. This output can be used to control the external read/write amplifier.
VCO_CLK	O	Open emitter test point output of the VCO clock. External pull-up and pull-down resistors are required to use this pin. They should be disconnected during operation to reduce power consumption.
$\overline{\text{VCOD}}$	O	VCO Disable. Active Low TTL compatible output signal that is used to disable the external reference signal at FREF during the read mode. The signal is asserted in read mode after the PLL has locked to incoming read data.
SER_REF	O	Reference voltage output for the servo signals.
$\overline{\text{WD}}$	O	TTL compatible encoded write data output for the read/write preamplifier.
VCOR	O	Open emitter test point output of the VCO reference signal. External pull-up and pull-down resistors are required to use this pin. They should be disconnected during operation to reduce power consumption.

ELECTRICAL SPECIFICATIONS

Recommended operating conditions apply unless otherwise specified.

ABSOLUTE MAXIMUM RATINGS

Operation outside these rating limits may cause permanent damage to this device.

PARAMETER	RATING	UNIT
5V Supply Voltage, VPA, VPD	6.0	V
Pin Voltage (Analog pins)	-0.3 to VPA, + 0.3	V
Pin Voltage (All others)	-0.3 to VPD + 0.3 or +12 mA	V
Storage Temperature	-65 to 150	°C
Lead Temperature (Soldering 10 sec.)	260	°C

RECOMMENDED OPERATING CONDITIONS

Currents flowing into the chip are positive.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Supply Voltage (VPA & VPD)		4.75	5.0	5.25	V
Junction Temperature, Tj		25		135	°C
Ambient Temperature, Ta		0		70	°C

POWER SUPPLY

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
IVPA IVPD	Supply Current	Outputs unloaded; PWRON = high or open		146		mA
Pd	Power dissipation	Ta = 25°C, outputs unloaded		730		mW
		SERVO Bit = 1		235		mW
		SERVO Bit = 1		40		mW
		PWRON = low, Outputs unloaded		15		mW

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, 4.75V< VCC <5.25V, 12 MHz< 1/TORC <24 MHz, 30 MHz< 1/TVCO <72 MHz, 0 °C< Ta <70 °C.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VIH	High Level Input Voltage		2.0		VPD + 0.3	V
VIL	Low Level Input Voltage		-0.3		0.8	V
IIH	High Level Input Current	VIH = 2.4V			100	µA
IIL	Low Level Input Current	VIL = 0.4V			-0.4	mA

ELECTRICAL CHARACTERISTICS (continued)
Unless otherwise specified, 4.75V< VCC <5.25V, 12 MHz< 1/TORC <24 MHz, 30 MHz< 1/TVCO <72 MHz, 0 °C< Ta <70 °C.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VOH	High Level Output Voltage	IOH = 400 µA	2.4			V
VOL	Low Level Output Voltage	IOL = 4 mA			0.5	V
FREF	Input Low Current	VIL = 0.4V		TBD		mA
FREF	Input High	VIH = 2.4V		TBD		mA
VOHT	Test Point Output High Level $\overline{DRD}$, VCO REF, VCO CLK	262Ω to VPD 402Ω to DGND VPD = 5.0V		VPA - 0.85		V
VOLT	Test Point Output Low Level $\overline{DRD}$, VCO REF, VCO CLK	262Ω to VPD 402Ω to DGND VPD = 5.0V		VPA - 1.75		V

PULSE DETECTOR SPECIFICATIONS

READ MODE (R/G is high)

AGC Amplifier
Unless otherwise specified, recommended operating conditions apply. Input signals are AC coupled to IN± and amplitude is between 25 mVpp & 250 mVpp differential. OUT± are loaded differentially with >600Ω, and each side is loaded with < 10 pF to AGND, and AC coupled to DIN±. A 2000 pF capacitor is connected between BYP and AGND. AGC pin is open.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Gain Range	1.0 Vpp ≤ (OUT+) - (OUT-) ≤ 3.0 Vpp	4		80	V/V
Output Offset Voltage Variation	Over entire gain range	-200	0	+200	mV
Maximum Output Voltage Swing	Set by BYP pin THD ≤ 5%	3.0			Vpp
Differential Input Resistance	(IN+) - (IN-) = 100 mVpp @ 2.5 MHz		5.0		kΩ
Differential Input Capacitance	(IN+) - (IN-) = 100 mVpp @ 2.5 MHz			10	pF
Common Mode Input Impedance	R/$\overline{W}$ = high		1.8		kΩ
	R/$\overline{W}$ = low		250		Ω
Input Noise Voltage	Gain set to maximum			15	$nV\sqrt{Hz}$
Bandwidth	-3 dB bandwidth at maximum gain	32			MHz
OUT+ & OUT- Pin Current	No DC path to AGND		3		mA

AGC Amplifier (Continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
CMRR (Input Referred)	(IN+) = (IN-) = 100 mVpp @ 2.5 MHz, gain set to max	40			dB
PSRR (Input Referred)	VPA1, 2 = 100 mVpp @ 2.5 MHz, gain set to max	30			dB
(DIN+) - (DIN-) Input Swing vs. AGC Input	25 mVpp ≤ (IN+) - (IN-) ≤ 250 mVpp, $\overline{HOLD}$ = high, 0.5 Vpp ≤ (DIN+) - (DIN-) ≤ 1.5 Vpp	0.9	1.0	1.1	Vpp/V
(DIN+) - (DIN-) Input Voltage Swing Variation	25 mVpp ≤ (IN+) - (IN-) ≤ 250 mVpp			6.0	%
AGC Voltage	AGC open	0.8	1.0	1.2	V
AGC Pin Input Impedance		4.4	5.5	6.6	kΩ
Slow AGC Discharge Current	(DIN+) - (DIN-) = 0V	4	4.5	6	µA
Fast AGC Discharge Current	Starts at 0.9 µs after R/$\overline{W}$ goes high, stops at 1.8 µs after R/$\overline{W}$ goes high	100	120	140	µA
AGC Leakage Current	$\overline{HOLD}$ = low	-0.2	0	+0.2	µA
Slow AGC Charge Current	(DIN+) - (DIN-) = 0.8 VDC, vary AGC until slow charge begins	-0.12	-0.18	-0.24	mA
Fast AGC Charge Current	(DIN+) - (DIN-) = 0.8 VDC, V_{AGC} = 3.0V	-0.9	-1.3	-1.7	mA
Fast to Slow Attack Switchover Point	$\frac{[(DIN+)-(DIN-)]}{[(DIN+)-(DIN-)]FINAL}$		125		%
Gain Decay Time (Td)	(IN+) - (IN-) = 250 mVpp to 125 mVpp @ 2.5 MHz, (OUT+) - (OUT-) to 90% final value		12		µs
	(IN+) - (IN-) = 50 mVpp to 25 mVpp at 2.5 MHz (OUT+) - (OUT-) to 90% final value		60		µs
Gain Attack Time	R/$\overline{W}$ = low to high (IN+) - (IN-) = 250 mVpp @ 2.5 MHz, (OUT+) - (OUT-) to 110% final value		2		µs

WRITE MODE (WG is high)

Common Mode Input Impedance			250		Ω

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HYSTERESIS COMPARATOR

Unless otherwise specified, recommended operating conditions apply. Input (DIN+) - (DIN-) is an AC coupled, 1.0 Vpp, 2.5 MHz sine wave. 0.5 VDC is applied to the HYS pin. R/$\overline{W}$ pin is high.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Input Signal Range		0.6	1.0	1.5	Vppd
Differential Input Resistance	(DIN+) - (DIN-) = 100 mVpp @ 2.5 MHz	12.5	15	17.5	kΩ
Differential Input Capacitance	(DIN+) - (DIN-) = 100 mVpp @ 2.5 MHz			5.0	pF
Common Mode Input Impedance (Both Sides)		3	4	5	kΩ
Level Gain Level Pin Output Voltage vs. (DIN+) - (DIN-)	0.6 Vpp < (DIN+) - (DIN-) < 1.5 Vpp, 10K between LEVEL and AGND		1		V/Vpp
Level Pin Output Offset Voltage	10 kΩ between level and AGND		TBD		
Level Pin Output Impedance	I_{LEVEL} = 0.2 mA		250		Ω
Level pin Maximum Output Current		1.5			mA
Tracking Threshold Tolerance		-15		+15	%
Hysteresis Gain	0.3 V < HYS < 1.0V		0.36		V/V
HYS Pin Input Current	0.5 V < HYS < 1.5V	0.0		-10	µA
Comparator Offset Voltage	HYS pin at AGND ≤ 1.5 kΩ across DIN±			5.0	mV
DOUT Pin Output Low Voltage	5 kΩ from DOUT to GND		VPA -2.8		V
DOUT Pin Output High Voltage	5 kΩ from DOUT to GND		VPA -2.4		V

ACTIVE DIFFERENTIATOR

Unless otherwise specified, recommended operating conditions apply. Input (CIN+) - (CIN-) is an AC-coupled, 1.0 Vpp, 2.5 MHz sine wave. 100Ω in series with 65 pF are tied from DIF+ to DIF-.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Input Signal Range		0.6	1.0	1.5	Vppd
Differential Input Resistance	(CIN+) - (CIN-) = 100 mVpp @ 2.5 MHz	12.5	15	17.5	kΩ
Differential Input Capacitance	(CIN+) - (CIN-) = 100 mVpp @ 2.5 MHz			5.0	pF
Common Mode Input Impedance	Both sides	3	4	5	kΩ
Voltage Gain From CIN± to DIF±	(DIF+ to DIF-) = 2 kΩ		1		V/V

ACTIVE DIFFERENTIATOR (continued)

Unless otherwise specified, recommended operating conditions apply. Input (CIN+) - (CIN-) is an AC-coupled, 1.0 Vpp, 2.5 MHz sine wave. 100Ω in series with 65 pF are tied from DIF+ to DIF-.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
DIF+ to DIF- PIn Current	Differentiator impedance must be set so as to not clip the signal for this current level	±0.7			mA
Comparator Offset Voltage	DIF+, DIF- are AC-coupled		0	5.0	mV
COUT Pin Output Low Voltage	5 kΩ from COUT to GND		VPA -2.8		V
COUT Pin Output High Voltage	5 kΩ from COUT to GND		VPA -2.4		V
COUT Pin Output Pulse Width			30		ns

SERVO BURST CAPTURE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
SERV_REF DC Pin Level		1.0		1.3	V
SERV_OUT to SERV_REF Offset	DIN+ shorted to DIN-			±40	mV
SERV_OUT Level vs. AGC Pin Voltage	V(SERV OUT - SERV REF) / V(AGC) = 1.0 Vp/V			±TBD	%
SERV_OUT Level vs. DIN+ - DIN- Pin Voltage	V(SERV OUT - SERV REF) / V(DIN+ - DIN-) = 1.0 Vp/Vpp			±TBD	%
Allowable Load Impedance SERV_OUT or SERV_REF to GND	Equivalent parallel resistance and capacitance	10		5	kΩ pF

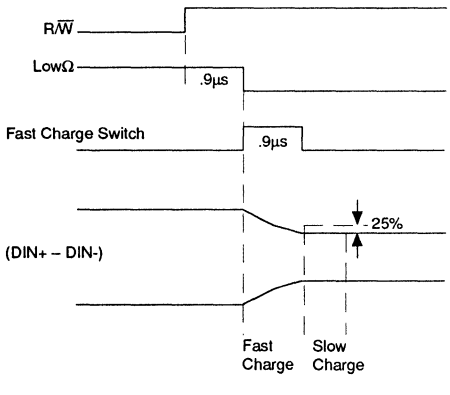

Figure A: AGC Attack Sequence

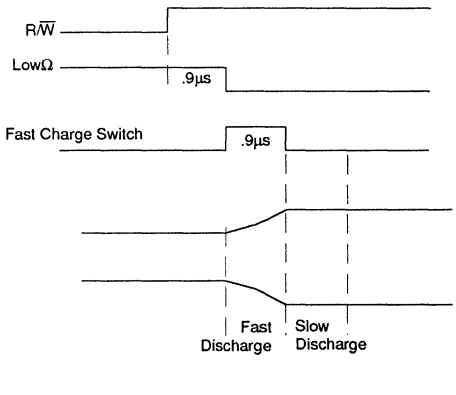

Figure B: AGC Decay Sequence

FIGURE 7: AGC Timing Diagram

QUALIFIER TIMING

Unless otherwise specified, recommended operating conditions apply. Inputs (CIN+) - (CIN-) and (DIN+) - (DIN-) are in-place as a coupled, 1.0 Vpp, 2.5 MHz sine wave. 100Ω in series with 65 pF are tied from DIF+ to DIF-. 0.5V is applied to the HYS pin. COUT and DOUT each have a 5 kΩ pull-down resistor (for test purposes only.) R/$\overline{W}$ pin is high.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Td1	D Flip-Flop Set Up Time	Minimum allowable time delay from (DIN+) - (DIN-) exceeding hysterisis point to (DIF+) - (DIF-) hitting a peak value.	0			ns
Td3	Propagation Delay	From positive peak to RD0* output pulse		TBD		ns
Td4	Propagation Delay	From negative peak to RD0* output pulse		TBD		ns
Td3-Td4	Pulse Pairing				1.0	ns
Td5	$\overline{RD}$ Output Pulse Width	RDW pin open	24	32	41	ns

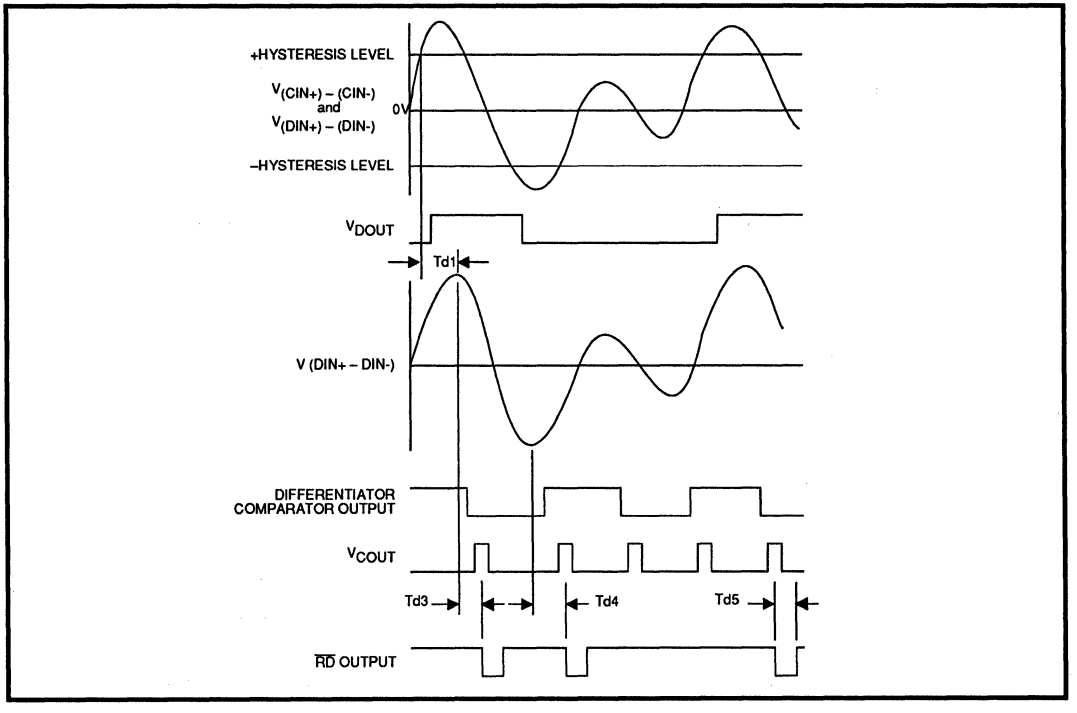

FIGURE 8: Read Mode Digital Section Timing Diagram

DATA SEPARATOR SPECIFICATIONS

DYNAMIC CHARACTERISTICS AND TIMING

READ MODE (See Figure 9)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TRRC	Read Clock Rise Time	0.8V to 2.0V, $C_L \leq 15$ pF			8	ns
TFRC	Read Clock Fall Time	2.0V to 0.8V, $C_L \leq 15$ pF			5	ns
RRC	Duty Cycle	12 - 20 Mbit/s	43	50	57	%
		>20 - 24 Mbit/s	40.8	50	59.2	%
TNS,TNH	NRZ (out) Set Up/	12 - 20 Mbit/s	15.5			ns
	Hold Time	>20 - 24 Mbit/s	13			ns
TPNRZ	NRZ (out) Propogation Delay			TBD		ns
TPAMD	$\overline{AMD}$ Propogation Delay			TBD		ns
AMD	Set Up and Hold Time (TAS, TAH)		13			ns
1/3 Cell Delay		TD = 3.6 (RR+1.7) 2.1 kΩ ≤ RR ≤ 6.1 kΩ	0.8TD		1.2TD	ns

WRITE MODE (Design Targets) (See Figure 10)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TWD	Write Data Pulse Width	$C_L \leq 15$ pF TC = 3.52 (RC + 0.53) RC = kΩ	2TOWC/3 -TPC -5		2TOWC/3 +TPC +5	ns
TRWD	Write Data Rise Time	0.8V to 2.0V, $C_L \leq 15$ pF			9	ns
TFWD	Write Data Fall Time	2.0V to 0.8V, $C_L \leq 15$ pF			5	ns
TSNRZ	NRZIN Set up Time		5			ns
THNRZ	NRZIN Hold Time		5			ns
TPWD	Write Data Position Accuracy	$C_L \leq 15$ pF; TPC = 0		±1	ns	
TPC	Precompensation Time Shift	TP= 0.22M (RC + 0.53)	TBD	TP	TBD	ns
	Magnitude	RC (MIN) = TBD				
	Accuracy	RC (MAX) = TBD, M = Value programmed in write precomp control register				

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INPUT REQUIREMENTS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TRD	Read Data Pulse Width		12		(4/3) TVCO-20	ns
TFRD	Read Data Fall Time	2.0V to 0.8V, $C_L \leq 15$ pF			9	ns
TRWC	Write Data Clock Rise Time	0.8V to 2.0V $C_L \leq 15$ pF			10	ns
TFWC	Write Data Clock Fall Time	2.0V to 0.8V $C_L \leq 15$ pF			8	ns

REFERENCE CLOCK CHARACTERISTICS

TXPW	Reference Clock Pulse Width		TBD		TBD	ns
	Reference Clock P-P Amplitude	AC coupled	TBD		TBD	ns

DATA SYNCHRONIZATION (Design Targets)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TVCO	VCO Center Frequency Period	VCO IN = 2.7V VCC = 5.0V TO = 3.6 (RR + 1.7) 2.1 kΩ ≤ RR ≤ 6.1 kΩ RR = (93/DR) −1.7 kΩ (4721)) RRz $\frac{77.4}{DR}$ − 2.1 kΩ (4720)	0.8TO		1.2TO	ns
VCO	Frequency Dynamic Range	1V ≤ VCO IN ≤ VCC-0.6V VCC = 5.0	±25		±45	%
KVCO	VCO Control Gain	ωo = 2π/TO 1V ≤ VCO IN ≤ VCC 0.6V	0.12ωo		0.26ωo	rad/s-V
KD	Phase Detector Gain	KD= 0.22/(RR+530) Read Mode = 0.11/(RR+530) Non-Read Mode VCC= 5V, PLL REF = $\overline{RD}$ 3T ('100') Pattern	0.83KD		1.17KD	A/rad
	Decode Window Centering Accuracy	RS = N/C			±1.5	ns
	Decode Window	RS = N/C	(2TORC/3) - 1.5			ns

DESIGN CHARACTERISTICS (Design Information Only)

KVCO x KD Product Accuracy			±28		%
VCO Phase Restart Error	Referred to RRC	TBD	TBD	TBD	rad

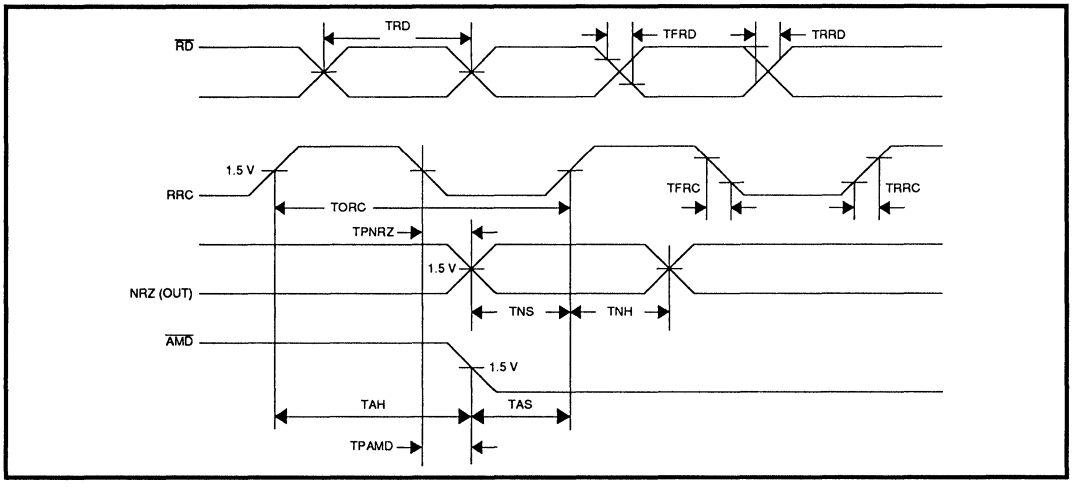


FIGURE 9: Read Timing

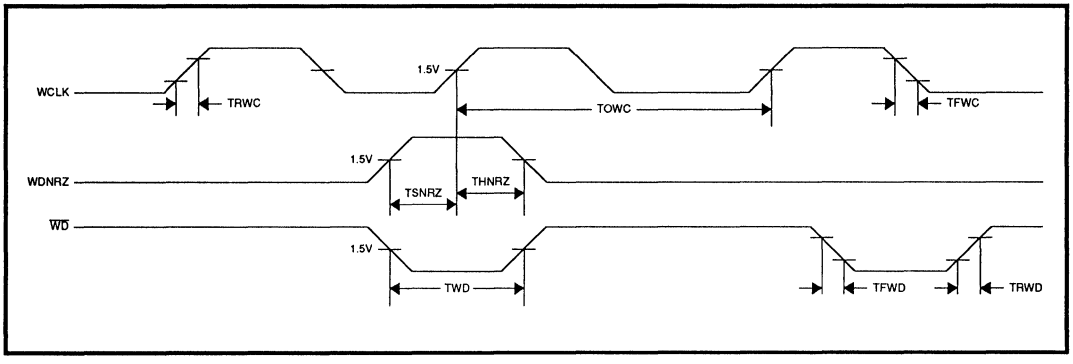
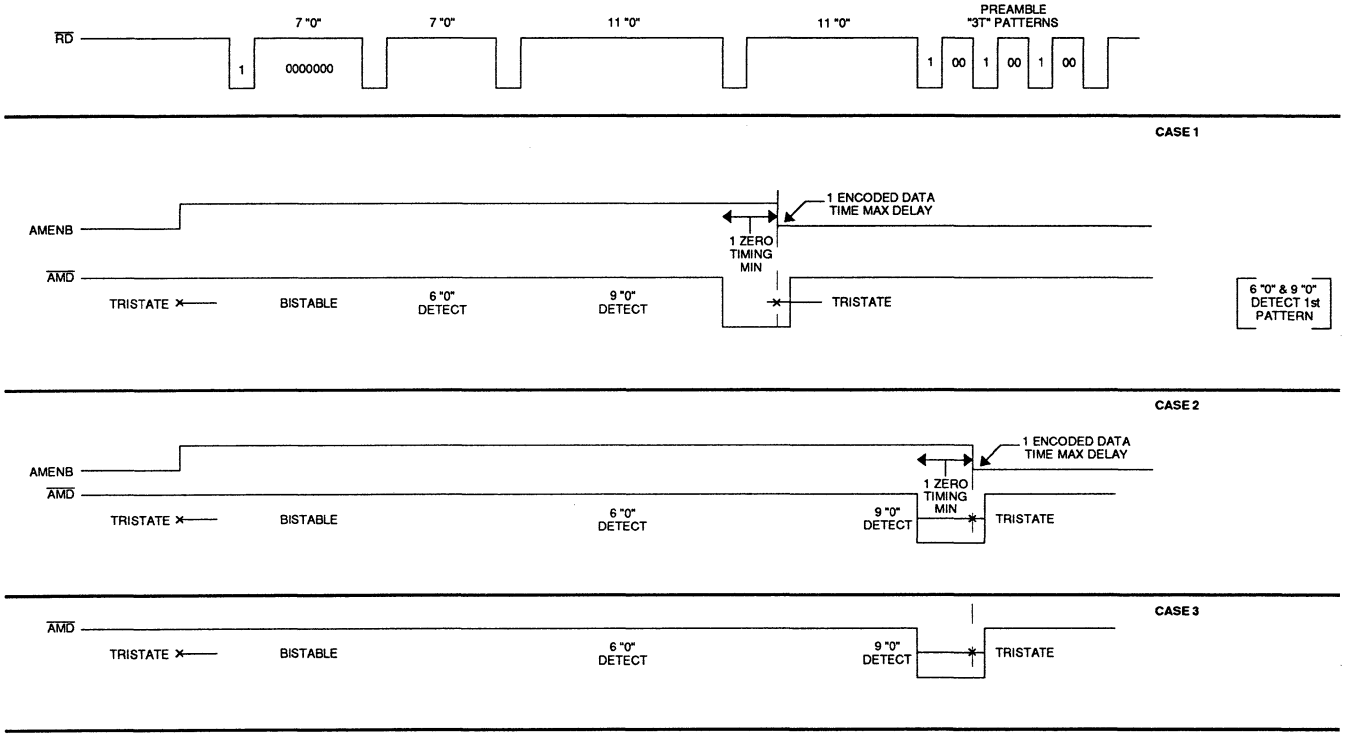


FIGURE 10: Write Timing



If 5 bits of RD are detected after 6 "0" are found and before 9 "0" then restart and look for 6 "0."

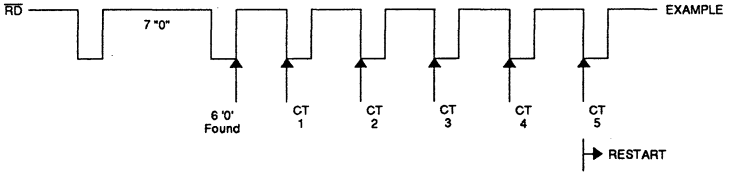


FIGURE 11: Address Mark Search

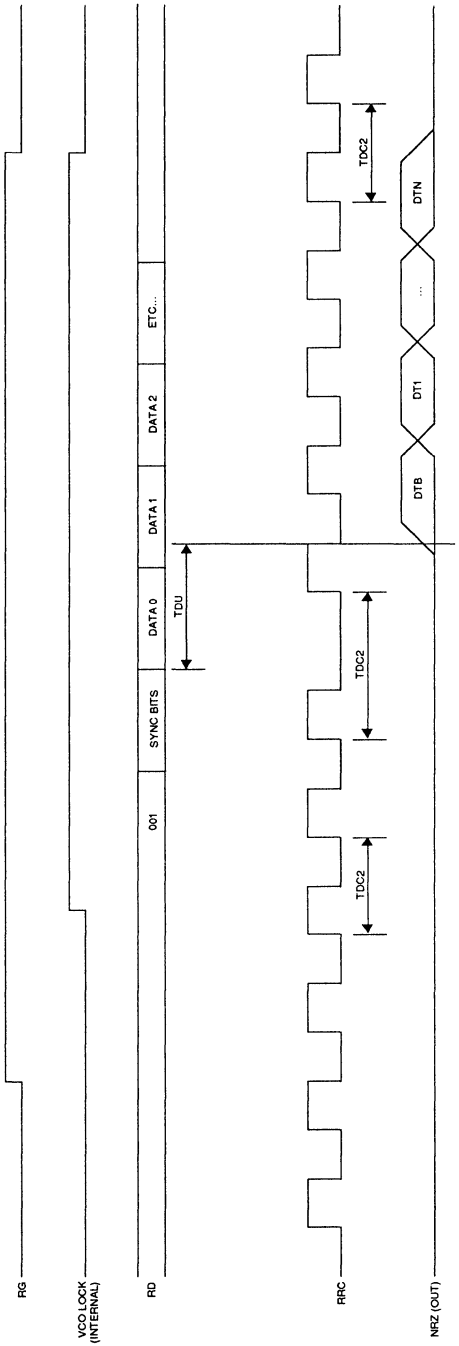


FIGURE 12: Read Mode NRZ and RRC Timing

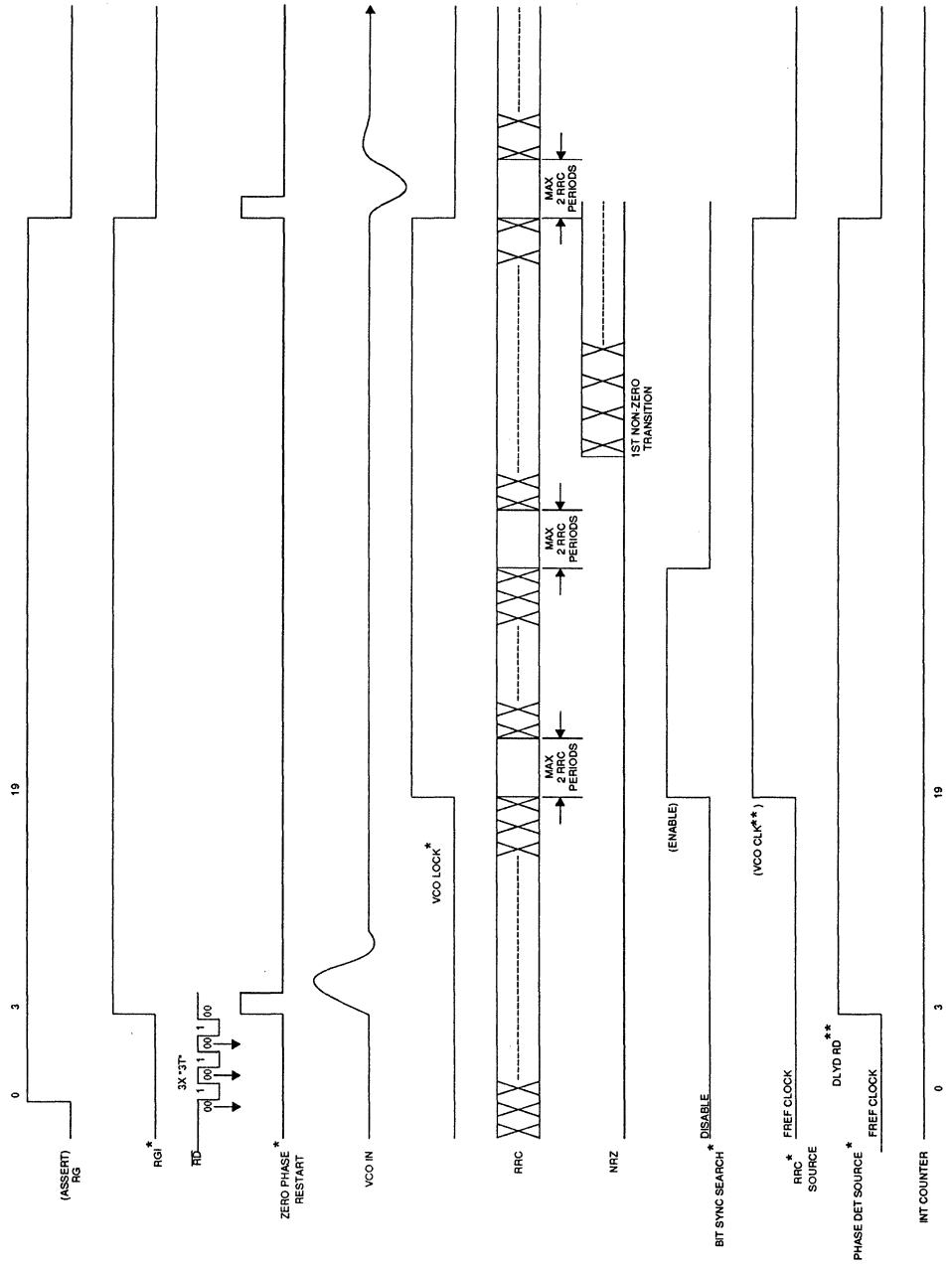


FIGURE 13: Read Mode Locking Sequence (Soft and Hard Sector)

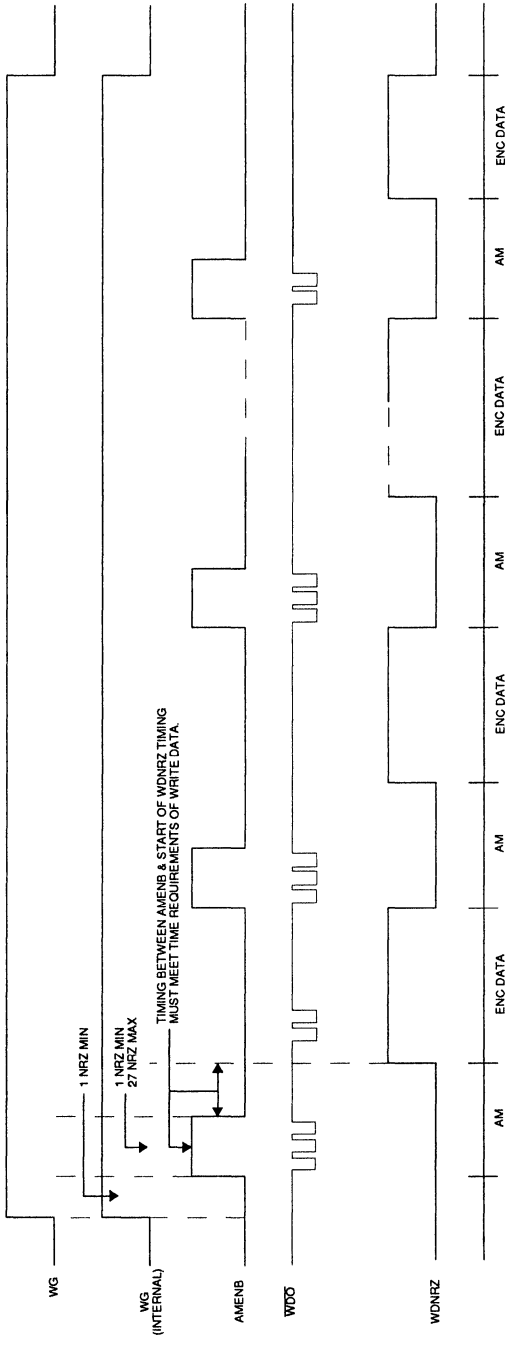


FIGURE 14: Multiple Address Mark Write

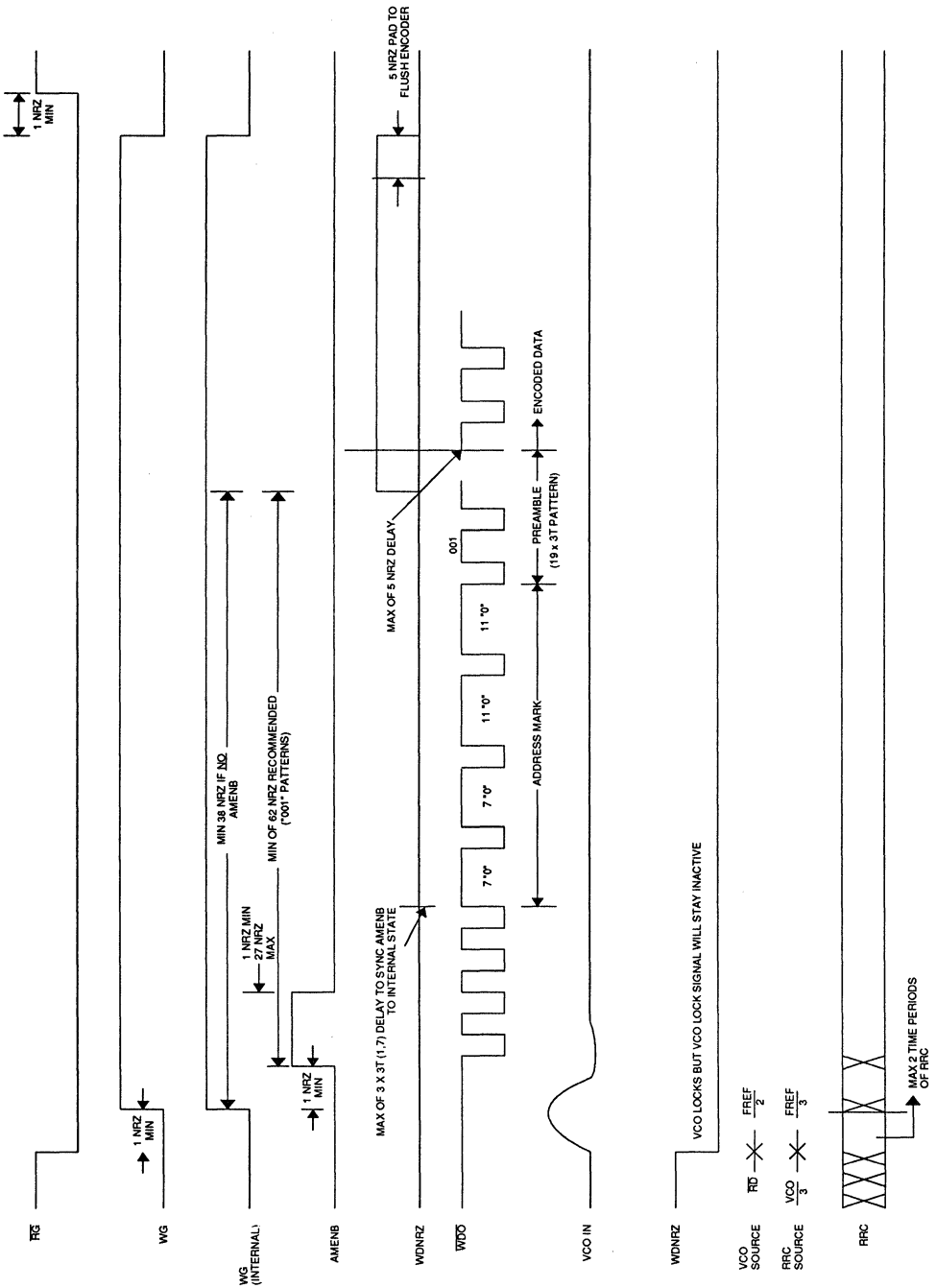


FIGURE 15: Write Data

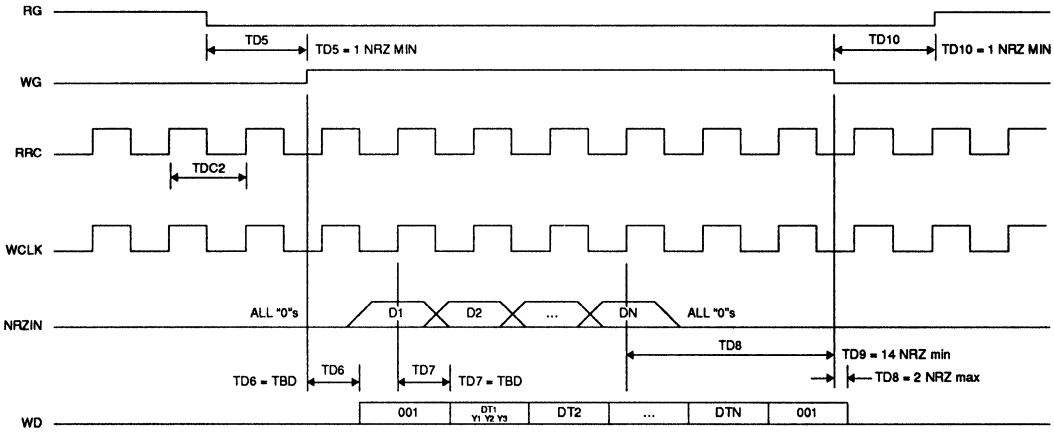


FIGURE 16: Write Mode NRZ Data Timing

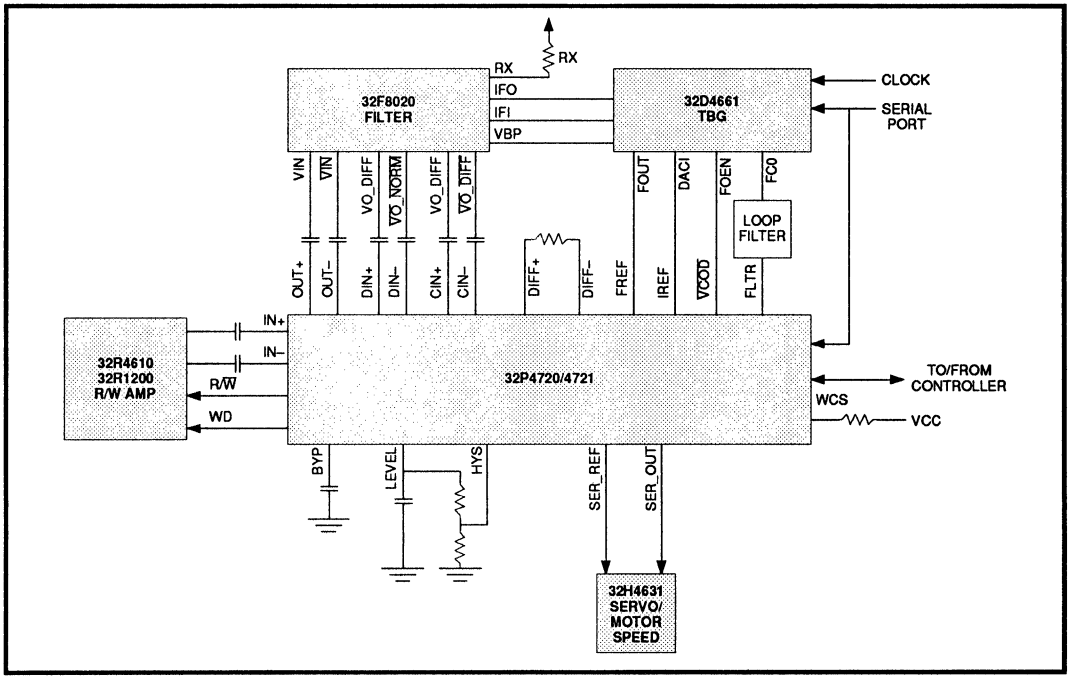
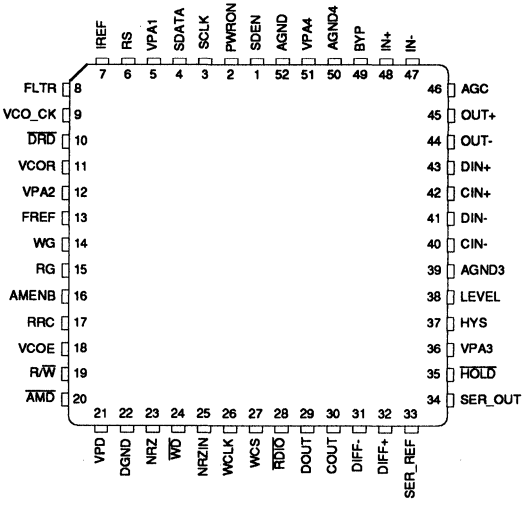


FIGURE 17: Typical Setup for Zoned Recording Application

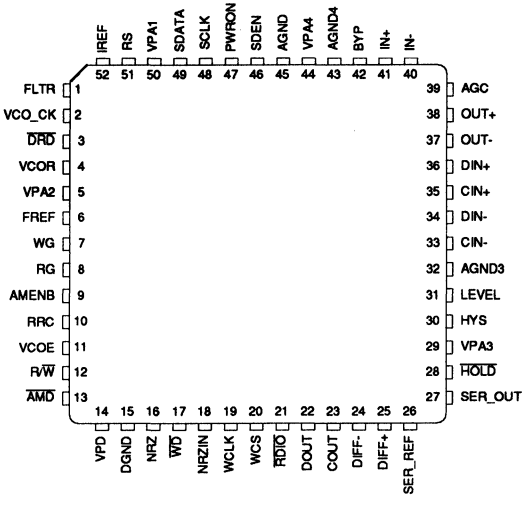
SSI 32P4720/4721
Pulse Detector & Data Separator

PACKAGE PIN DESIGNATIONS

(Top View)



52-Pin PLCC



52-Pin QFP

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only.

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SSI 32P4730
Single Chip Read Channel
Advance Information

December 1991

DESCRIPTION

The SSI 32P4730 device is a high performance BiCMOS single chip read channel IC that contains all the functions needed to implement a complete zoned recording read channel for hard disk drive systems. Functional blocks include the pulse detector, programmable filter, 4-burst servo capture, time base generator, and data separator with 1,7 RLL ENDEC. Data rates from 8 to 24 Mbit/s can be programmed using an internal DAC whose reference current is set by a single external resistor.

Programmable functions of the SSI 32P4730 device are controlled through a bi-directional serial port and banks of internal registers. This allows zoned recording applications to be supported without changing external component values from zone to zone.

The SSI 32P4730 utilizes an advanced BiCMOS process technology along with advanced circuit design techniques which result in a high performance device with low power consumption.

FEATURES

GENERAL:

- 8-24 Mbit/s data rate (controlled by internal DAC)
- Complete zoned recording application support
- Low power operation (<400 mW typical @ 5V)
- Bi-directional serial port for register access
- Register programmable power management
  - Sleep mode <5 mW (Design goal:≤ 1 mW)
- Power supply range (4.3 to 5.5 volts)
- Small footprint 64-pin TQFP package

PULSE DETECTOR:

- Fast attack/decay modes for rapid AGC recovery
- Dual rate charge pump for fast transient recovery
- Low Drift AGC hold circuitry supports programmable gain, non-AGC operation
- Temperature compensated, exponential control AGC
- Wide bandwidth, high precision full-wave rectifier
- Dual mode pulse qualification circuitry (user selectable)
- TTL $\overline{RDIO}$ signal output for servo timing support
- Timing for LOW-Z and fast decay functions set internally
- 0.5 ns max. pulse pairing with sine wave input
- 4-burst servo capture
- Provision for on-chip switching of the hysteresis threshold time constant

PROGRAMMABLE FILTER:

- Programmable cutoff frequency of 3 to 9 MHz
- Programmable boost/equalization of 0 to 13 dB
- Matched normal and differentiated outputs
- ± 10% Fc accuracy
- ± 2% maximum group delay variation
- Less than 1.5% total harmonic distortion
- Low-Z input switch
- No external filter components required

TIME BASE GENERATOR:

- Better than 1% frequency resolution
- Independent M and N divide-by registers
- VCO center frequency matched to data synchronizer VCO

DATA SEPARATOR:

- Fast acquisition phase lock loop with zero phase restart technique
- Integrated 1,7 RLL Encoder/Decoder
- Fully integrated data separator
  - No external delay lines or active devices required
  - No external active PLL components required
- Programmable decode window symmetry control via serial port
  - Window shift control ± 30%
  - Includes delayed read data and VCO clock monitor points
- Hard and soft sector operation

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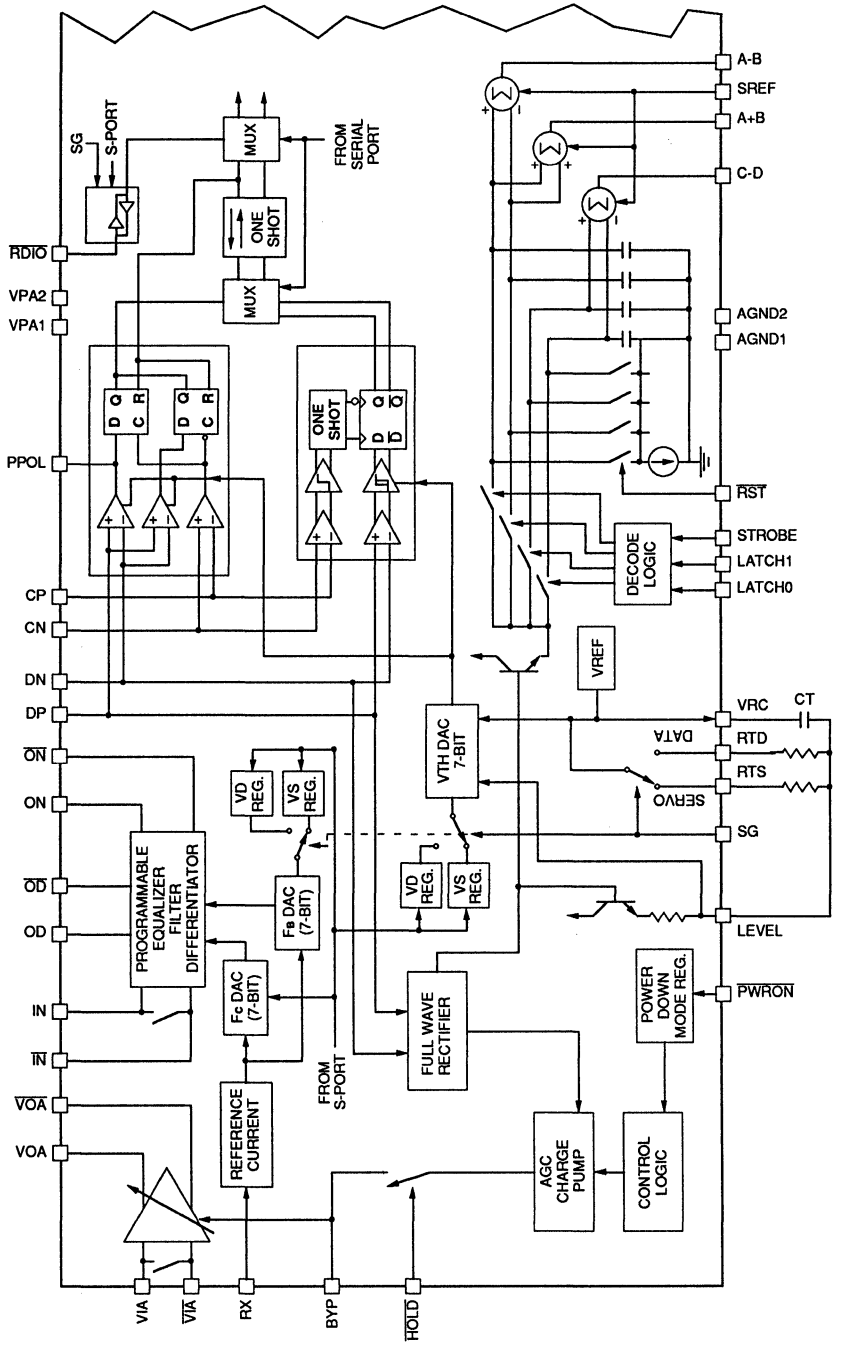

FIGURE 1(A): SSI 32P4730 Combo Device Part 1

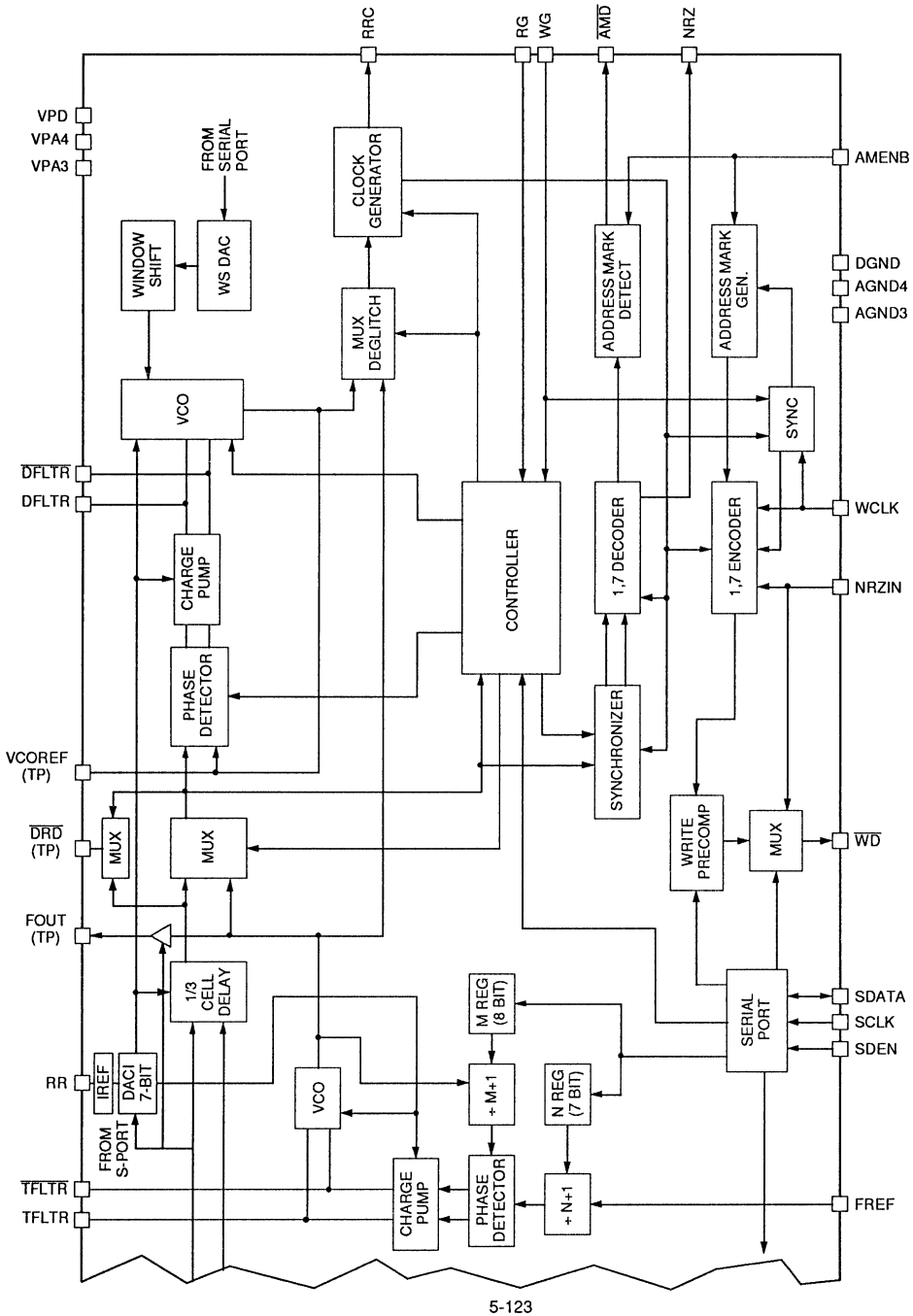

FIGURE 1(B): SSI 32P4730 Combo Device Part 2

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SSI 32P4730
Single Chip
Read Channel

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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SSI 32P4740
Single Chip Read Channel

Advance Information

December 1991

DESCRIPTION

The SSI 32P4740 device is a 5-volt single chip read channel IC that contains all the functions needed to implement a high performance read channel. Functional blocks include the pulse detector, programmable filter, 4-burst servo capture, time base generator, and data separator with 1, 7 RLL ENDEC. Data rates from 16 to 48 Mbit/s can be programmed using an internal DAC whose reference current is set by a single external resistor.

Programmable functions of the SSI 32P4740 device are controlled through a bi-directional serial port and banks of internal registers. This allows zoned recording applications to be supported without changing external component values from zone to zone.

The SSI 32P4740 utilizes an advanced BiCMOS process technology along with advanced circuit design techniques which result in a high performance device with low power consumption.

FEATURES

GENERAL:

- 16-48 Mbit/s data rate (controlled by internal DAC)
- Complete zoned recording application support
- Low power operation (600 mW typical @ 5V)
- Bi-directional serial port for register access
- 9 bit bi-directional NRZ bus
  - 8 data bits plus 1 parity bit
- Register programmable power management
  - Sleep mode < 5 mW (Design goal: ≤ 1 mW)
- Power supply range (4.3 to 5.5 volts)
- Small footprint 100-pin TQFP package

PULSE DETECTOR:

- Fast attack/decay modes for rapid AGC recovery
- Dual rate charge pump for fast transient recovery
- Low Drift AGC hold circuitry supports programmable gain, non-AGC operation
- Temperature compensated, exponential control AGC
- Wide bandwidth, high precision full-wave rectifier
- TTL $\overline{\text{RDIO}}$ signal output for servo timing support
- Timing for LOW-Z and fast decay functions set internally
- 0.5 ns max. pulse pairing with sine wave input
- 4-burst servo capture
- Provision for on-chip switching of the hysteresis threshold time constant

PROGRAMMABLE FILTER:

- Programmable cutoff frequency of 5 to 18 MHz
- Programmable boost/equalization of 0 to 13 dB
- Matched normal and differentiated outputs
- ± 10% Fc accuracy
- ± 2 % maximum group delay variation
- Less than 1% total harmonic distortion
- Low-Z input switch
- No external filter components required

TIME BASE GENERATOR:

- Greater than 1% frequency resolution
- Independent M and N divide-by registers
- VCO center frequency matched to data synchronizer VCO

DATA SEPARATOR:

- Fast acquisition phase lock loop with zero phase restart technique
- Integrated 1, 7 RLL Encoder/Decoder
- Fully integrated data separator
  - No external delay lines or active devices required
  - No external active PLL components required
- Programmable decode window symmetry control via serial port
  - Window shift control ±30%
  - Includes delayed read data and VCO clock monitor points
- Hard and soft sector operation

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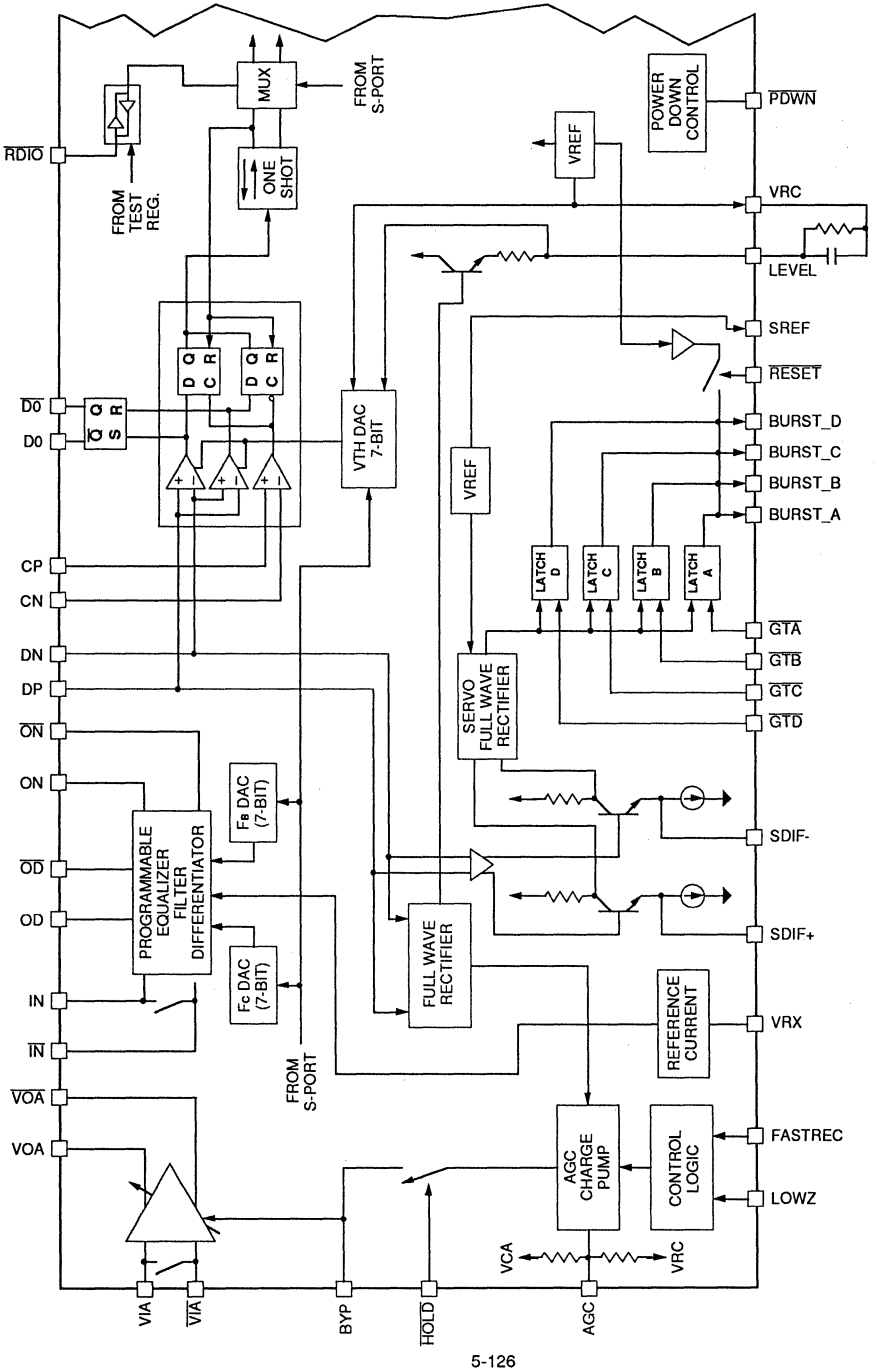

FIGURE 1(A): SSI 32P4740 Combo Device Part 1

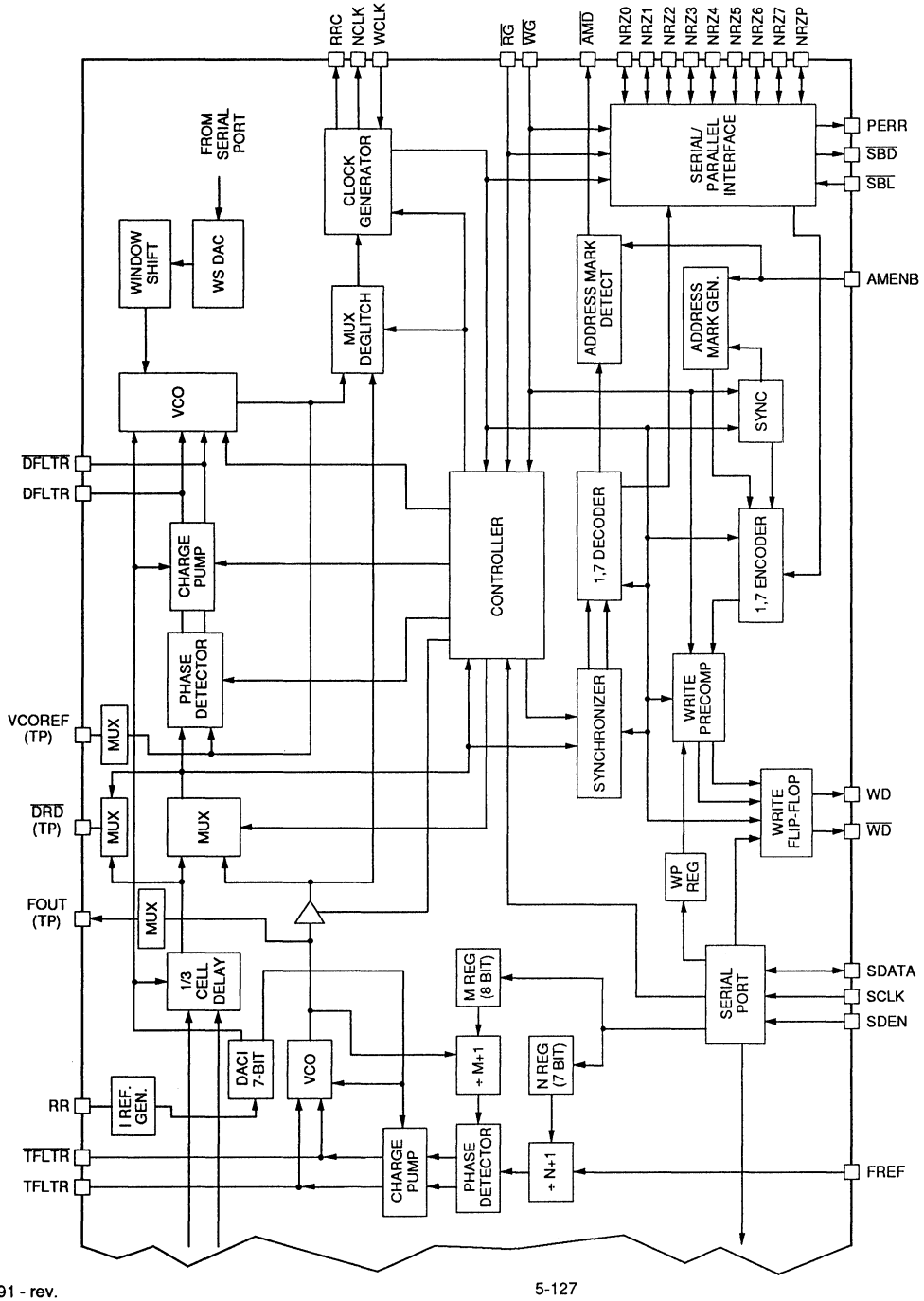

FIGURE 1(B): SSI 32P4740 Combo Device Part 2

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SSI 32P4740
Single Chip
Read Channel

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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Section 6

HDD HEAD POSITIONING

SSI 32H116A
Differential Amplifier

November 1991

DESCRIPTION

The SSI 32H116A is a high performance differential amplifier applicable for use as a preamplifier for the magnetic servo thin film head in Winchester disk drives.

FEATURES

- **Narrow gain range**
- **50 MHz bandwidth**
- **IBM 3370/3380-compatible performance**
- **Operates on either IBM-compatible voltages (8.3V) or OEM-compatible (10V)**
- **Packages include 8-pin Plastic DIP and SON**
- **SSI 32H1162 available to operate with a 12V power supply**

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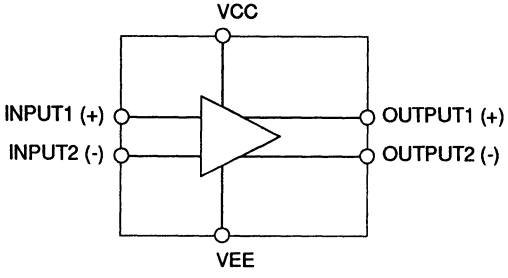
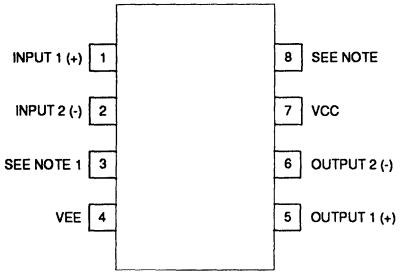
BLOCK DIAGRAM



PIN DIAGRAM



8-Pin PDIP, SON

CAUTION: Use handling procedures necessary for a static sensitive component.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Power Supply Voltage (VCC-VEE)	12	V
SSI 32H1162	14	V
Differential Input Voltage	±1	V
Storage Temperature Range	-65 to 150	°C
Operating Ambient Temperature (T_A)	15 to 60	°C
Operating Junction Temperature (T_J)	15 to 125	°C
Output Voltage	VCC -2.0 to VCC +0.4	V

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Supply Voltage (VCC-VEE)		7.45	8.3	9.15	V
		9.0	10.0	11.0	V
	SSI 32H1162 only	10.8	12.0	13.2	V
Input Signal Vin			1		mVpp
Ambient Temp T_A		+15		+65	°C

ELECTRICAL CHARACTERISTICS

Tj = 15 °C to 125 °C, (VCC-VEE) = 7.9V to 10.5V (to 13.2V for 32H1162)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Gain (Differential)	Vin = 1mVpp, T_A = 25 °C, f = 1 MHz	200	250	310	mV/mV
Bandwidth (3dB)	Vin = 1mVpp, C_L = 15 pF	20	50		MHz
Gain Sensitivity (Supply)				1.0	%/V
Gain Sensitivity (Temp.)	15 °C < T_A < 55 °C		-0.16		%/C
Input Noise Voltage	Input Referred, Rs = 0		0.7	0.94	$nV/\sqrt{Hz}$
Input Capacitance (Differential)	Vin = 0, f = 5 MHz		40	60	pF
Input Resistance (Differential)			200		Ω
Common Mode Rejection Ratio Input Referred	Vin = 100 mVpp, f = 1 MHz	60	70		dB
Power Supply Rejection Ratio Input Referred	VEE + 100 mVpp, f = 1 MHz	46	52		dB

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Input Dynamic Range (Differential)	AC input voltage where gain falls to 90% of its small signal gain value, f = 5MHz	±0.75			mV
Output Offset Voltage (Differential)	Vin = 0	-400		+400	mV
Output Voltage (Common Mode)	Inputs shorted together and Outputs shorted together	VCC-0.45	VCC-0.6	VCC-1.0	V
Single Ended Output Capacitance				10	pF
Power Supply Current	VCC-VEE = 9.15V		28	40	mA
	VCC-VEE = 11V		29	42	mA
	VCC-VEE = 13.2V, 32H1162 only		39	50	mA
Input DC Voltage	Common Mode		VEE +2.6		V
Input Resistance	Common Mode		80		Ω

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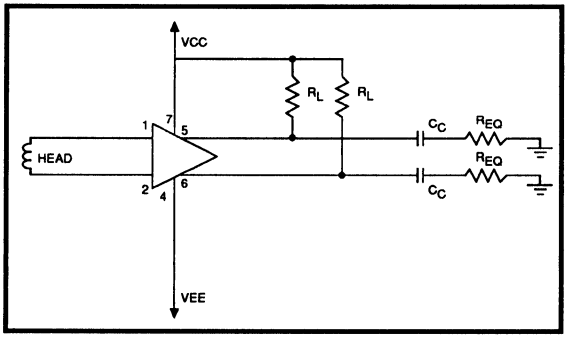
APPLICATIONS INFORMATION

CONNECTION DIAGRAM



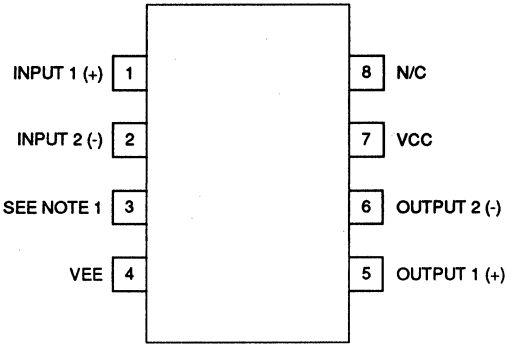
RECOMMENDED LOAD CONDITIONS

1. Input is directly coupled to the head
2. Cc's are AC coupling capacitors
3. RL's are DC bias and termination resistors, 100Ω recommended
4. REQ. represents equivalent load resistance
5. Ceramic capacitors (0.1 µF) are recommended for good power supply noise filtering

SSI 32H116A
Differential Amplifier

PACKAGE PIN DESIGNATIONS

(Top View)



8-Pin PDIP, SON

NOTE : Pin must be left open and not connected to any circuit etch.

ORDERING INFORMATION

PART DESCRIPTION	ORDERING NUMBER	PACKAGE MARK
SSI 32H116A Differential Amplifier		
8-Pin SON	32H116A-CN	H116A
8-Pin PDIP	32H116A-CP	32H116A-CP
SSI 32H1162A		
8-Pin SON	32H1162A-N	H1162A
8-Pin PDIP	32H1162A-CP	32H1162A-CP

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SSI 32H523AR
Thin Film Single Channel Servo Read/Write Device

December 1991

DESCRIPTION

The SSI 32H523AR Read/Write device is a bipolar monolithic integrated circuit designed for use with a two terminal thin film recording head. It provides a low noise read amplifier and write current control. In its servo application, the device will be used in write mode once then switched permanently to read mode. Data protection is provided in both write and read modes to guarantee servo data security. Power supply fault protection is effective in both write and read modes while head short circuit protection is provided in write mode. Further data security can be provided in read mode by removing the write current source voltage. It requires +5V and +12V power supplies and is available in a 14-pin SON surface mount package. Internal 1000Ω damping resistors are provided.

FEATURES

- **High performance:**
  - **Read mode gain = 250 V/V**
  - **Input noise = 1.0 nV/√Hz max.**
  - **Input capacitance = 45 pF max.**
  - **Write current range = 10 mA to 40 mA**
  - **Head voltage swing = 3.4 Vpp min.**
  - **Write current rise time = 13 nsec**
- **Highest level of data security provided**
- **Power supply fault protection**
- **Head to ground short circuit protection**
- **+5V, +12V power supplies**

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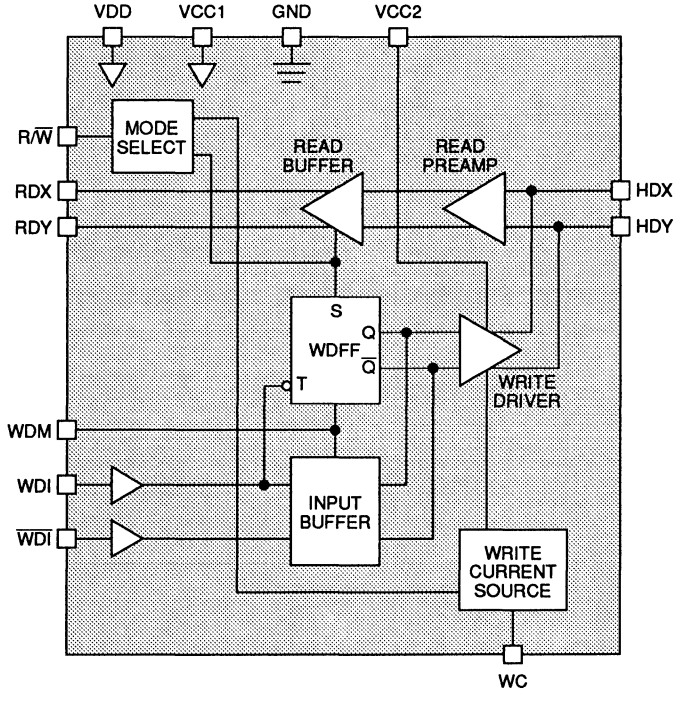
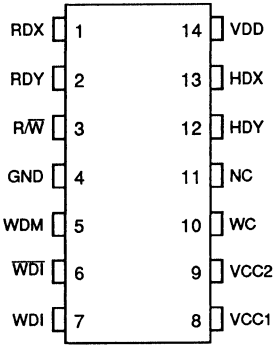
BLOCK DIAGRAM



PIN DIAGRAM



14-PIN SON

CAUTION: Use handling procedures necessary for a static sensitive component.

CIRCUIT OPERATION

The SSI 32H523AR provides write drive or read amplification. Mode control is accomplished with pins WDM, Write Data Mode, and R/$\overline{W}$, as shown in Table 1. An internal resistor pullup on R/$\overline{W}$ will force the device into a non-writing condition if the line is opened accidentally.

WRITE MODE

The write mode configures the SSI 32H523AR as a differential current switch. The WDM pin state determines whether write current transitions are controlled by a single-ended TTL input, WDI, or by differential (ECL-like) inputs, WDI and $\overline{WDI}$. With WDM open, write current is toggled between the X and Y direction of the head on each high to low transition on pin WDI, Write Data Input. A preceding read operation initializes the Write Data Flip-Flop (WDFF) to pass write current in the X-direction of the head.

With WDM grounded the head current direction is controlled by differential inputs WDI and $\overline{WDI}$. For (WDI - $\overline{WDI}$) > 200mV the current is in the X-direction.

The magnitude of the write current (0-pk) given by:

$$Iw = \frac{Vwc}{Rwc}$$

where Vwc (WC pin voltage) = 1.65V ± 5%, is programmed by an external resistor Rwc, connected from pin WC to ground. The actual head current Ix, y is given by:

$$Ix, y = \frac{Iw}{1 + Rh/Rd}$$

where:
Rh = head resistance + external wire resistance, and
Rd = damping resistance.

Power supply fault protection improves data security by disabling the write current generator during a voltage fault or power supply sequencing. In addition a head to ground short circuit protection circuit will shut off the write driver and current to prevent excessive current and power dissipation. Triggering of this feature occurs when the DC voltage at either HDX or HDY is less than 2.0V ± 15% in write mode

READ MODE

The read mode configures the SSI 32H523AR as a low noise differential amplifier and deactivates the write current generator. The RDX and RDY outputs are open collectors.

In read mode, the write data channel is powered down to reduce power consumption. Note that in write mode, the read amplifier is deactivated and will not pull any current from the load resistor.

For maximum data security in read mode VCC2 is left open or grounded. This eliminates the voltage source for write current.

TABLE 1: Mode Select

WDM	R/$\overline{W}$	MODE
GND	0	Write Differential input
OPEN	0	Write Single-ended input
X	1	Read

PIN DESCRIPTIONS

NAME	TYPE	DESCRIPTION
R/$\overline{W}$	I	Read/Write: a high level selects Read mode
WDI, $\overline{WDI}$	I	Write Data In: toggles the direction of the head current
HDX, HDY	I/O	X, Y Head Connections: current in the X-direction flows into the X-port
RDX, RDY	O	X, Y Read Data: differential read data output
WC	-	Write Current: used to set the magnitude of the write current
WDM	I	Write Data Mode: Ground this pin for direct differential input using both WDI and $\overline{WDI}$, leave open to select TTL input using WDI and the internal Write Data Flip-Flop.
VCC1	-	+5V logic circuit supply
VDD	-	+12V supply for read
VCC2	-	+5V power supply for write current drivers (see note)
GND	-	Ground

Note: To ensure maximum data integrity in write-once servo applications, this pin should be left open or shorted to ground after writing servo information.

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ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above absolute maximum ratings may permanently damage the device.

PARAMETER	SYMBOL	VALUE	UNITS
DC Supply Voltage	VDD	-0.3 to +14	VDC
	VCC1, 2	-0.3 to +7	VDC
Write Current	Iw	60	mA
Digital Input Voltage	Vin	-0.3 to VCC1 +0.3	VDC
Head Port Voltage	VH	-0.3 to VCC2 +0.3	VDC
RDX, RDY Output Current	Io	-10	mA
Storage Temperature	Tstg	-65 to +150	°C
Package Temperature (20 sec Reflow)		215	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		SYMBOL	VALUE	UNITS
DC Supply Voltage	Read Mode	VDD	12 ± 10%	VDC
		VCC1	5 ± 10%	VDC
	Write Mode	VDD	12 ± 5%	VDC
		VCC1	5 ± 5%	VDC
		VCC2	5 ± 5%	VDC
Output Pullup Resistors (to VCC1)		RL	100	Ω
Ambient Temperature	Read Mode	TAR	0 - 70	°C
	Write Mode	TAW	20 - 43	°C
Operating Junction Temperature		Tj	0 to +135	°C

DC CHARACTERISTICS (Unless otherwise specified, recommended operating conditions apply.)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
VDD Supply Current		Read Mode	-	-	26	mA
		Write Mode	-	-	12	mA
VCC1 Supply Current		Read Mode	-	-	35	mA
		Write Mode	-	-	30	mA
VCC2 Supply Current		Read Mode, see Note 1	-	-	7	mA
		Write Mode	-	-	19 + Iw	mA
Power Dissipation (Tj = +135°C)		Read Mode, VCC2 = 0	-	-	500	mW
		Write Mode: Iw = 40mA	-	-	500	mW
Input Low Voltage (VIL)		Includes WDI w/WDM = open	-	-	0.8	VDC
Input High Voltage (VIH)		Includes WDI w/WDM = open	2.0	-	-	VDC
Input Low Current (IIL)		VIL = 0.8v	-0.4	-	-	mA
Input High Current (IHL)		VIH = 2.0v	-	-	100	µA
Input Voltage (WDI, $\overline{WDI}$)		WDM = GND	3.0	-	VCC1	VDC
Differential Input Voltage (WDI, $\overline{WDI}$)		WDM = GND	200	-	-	mVDC
VDD Fault Voltage			8. 5	-	10.0	VDC
VCC1 Fault Voltage			3.5	-	4.1	VDC
Head Current (HDX, HDY)	Write Mode	0 ≤ VDD ≤ 8.5V 0 ≤ VCC1 ≤ 3.5V	-200	-	+200	µA
	Write Mode	VCC2 = open or ground	-200	-	+200	µA
	Read Mode	0 ≤ VCC1 ≤ 5.5V 0 ≤ VDD ≤ 13.2V	-200	-	+200	µA

Note 1: If VCC2 is at ground or open this current is zero.

WRITE CHARACTERISTICS
Unless otherwise specified, recommended operating conditions apply, Iw = 15mA, Lh = 1.5µH, Rh = 30Ω f(DATA) = 5MHz, and +20°C < Tj < + 135°C

PARAMETER	CONDITIONS	MIN.	NOM	MAX	UNITS
WC Pin Voltage (Vwc)		-	1.65 ± 5%	-	V
Differential Head Voltage Swing		3.4	-	-	Vpp
Differential Output Capacitance		-	-	25	pF
Differential Output Resistance		800	1000	1400	Ω
Write Current Range		10	-	40	mA

READ CHARACTERISTICS
Unless otherwise specified, recommended operating conditions apply, CL (RDX, RDY) < 20pF

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Differential Voltage Gain		Vin=1mVpp @1MHz, TA = 25°C	200	250	300	V/V
Gain Sensitivity		15°C < TA < 55°C	-	-0.16	-	%/°C
Bandwidth	-1dB	|Zs|<5Ω, Vin = 1mVpp @ 300kHz	10	20	-	MHz
	-3dB	|Zs|<5Ω, Vin = 1mVpp @ 300kHz	20	45	-	MHz
Input Noise Voltage		BW=15MHz, Lh=0 µH, R =0Ω	-	0.7	1.0	nV/√Hz
Differential Input Capacitance		Vin = 1mVpp, f = 5MHz	-	40	45	pF
Differential Input Resistance		Vin = 1mVpp, f = 5MHz	460	750	1.4K	Ω
Dynamic Range		AC input voltage where gain falls to 90% of its small signal gain value, f=5MHz	±2	-	-	mV
Common Mode Rejection Ratio		Vin = 0VDC+100mVpp @ 5MHz	54	-	-	dB
Power Supply Rejection Ratio		100m Vpp @ 5MHz on VDD, 100m Vpp @ 5MHz on VCC1	54	-	-	dB
Output Offset Voltage		Vin = 0V	-600	-	+600	mV
Output Voltage (Common Mode)		Inputs shorted together, and outputs shorted together	**	-	*	VDC

*VCC1 - 0.42
**VCC1 - 1.0

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SWITCHING CHARACTERISTICS (See Figure 1)
Unless otherwise specified, recommended operating conditions apply, Iw = 15mA, Lh = 1.5 µH, Rh = 30Ω, f(DATA) = 5MHz, and +20°C < T_A < +43°C

PARAMETER	CONDITIONS	MIN	MAX	UNITS
R/$\overline{W}$				
R/$\overline{W}$ to Write Mode	Delay to 90% of write current	-	0.6	µs
R/$\overline{W}$ to Read Mode	Delay to 90% of 100mV 10MHz Read signal envelope or to 90% decay of write current	-	0.6	µs
Head Current				
Prop. Delay - TD1	From 50 % points, Lh=0µh, Rh=0Ω	-	32	ns
Asymmetry	Input has 50 % duty cycle and 1ns rise/fall time, Lh=0µh, Rh=0Ω	-	1	ns
Rise/Fall Time	10% - 90% points, Lh=0µh, Rh=0Ω	-	13	ns

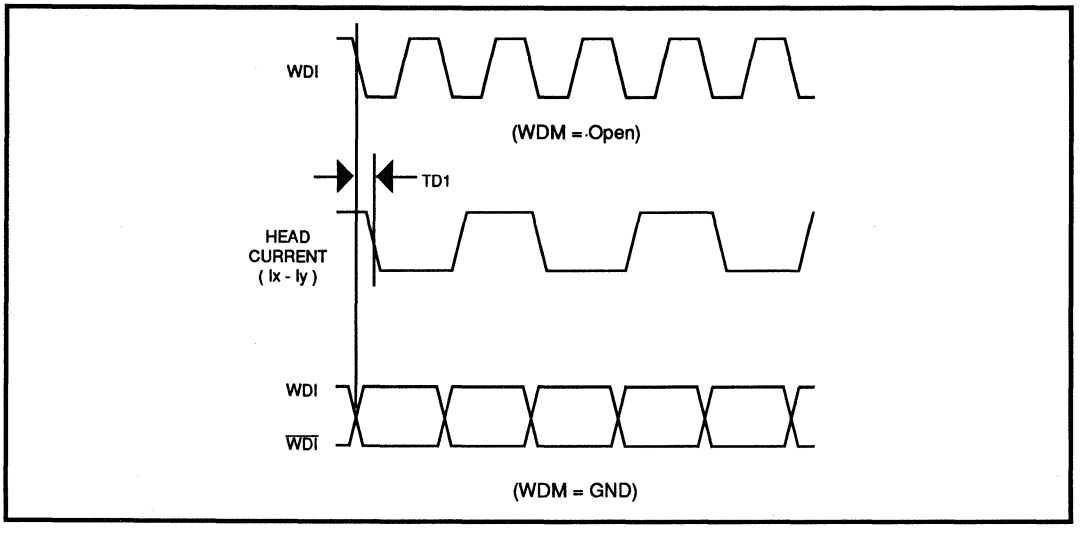

FIGURE 1: Write Mode Timing Diagram

PACKAGE PIN DESIGNATIONS
(TOP VIEW)

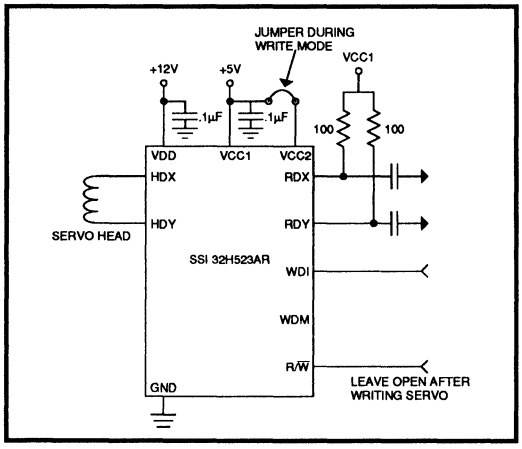

FIGURE 2: Typical Application

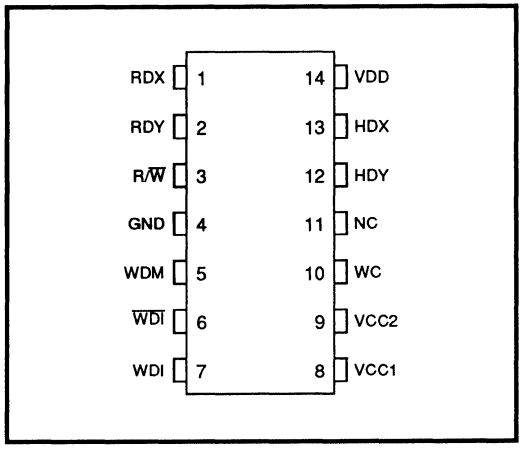

FIGURE 3: 14-Pin SON

6

ORDERING INFORMATION

PART DESCRIPTON	ORDER NO.	PKG. MARK
SSI 32H523AR Servo Read/Write IC	32H523AR-CN	32H523AR-CN

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 731-7110, FAX (714) 573-6914

Notes:

silicon systems®
A TDK Group Company

SSI 32H566R
Ferrite Single-Channel Servo Read/Write Device
Preliminary Data

November 1991

DESCRIPTION

The SSI 32H566R Read/Write device is a bipolar monolithic integrated circuit designed for use with center-tapped ferrite recording heads. It provides a low noise read amplifier, write current control and data protection circuitry for a single channel. The SSI 32H566R provides internal 750Ω damping resistors. Power supply fault protection is provided by disabling the write current generator during power sequencing. System write to read recovery time is significantly improved by controlling the read channel common mode output voltage shift in the write mode.

FEATURES

- **High performance:**
  - **Read mode gain = 150 V/V**
  - **Input noise = 1.5nV/√Hz max.**
  - **Input capacitance = 20 pF max.**
  - **Write current range = 10 mA to 40 mA**
- **Enhanced system write to read recovery time**
- **Power supply fault protection**
- **Designed for center-tapped ferrite heads**
- **Programmable write current source**
- **TTL compatible control signals**
- **+5V, +12V power supplies**
- **Socket compatible with the SSI 32H523R**

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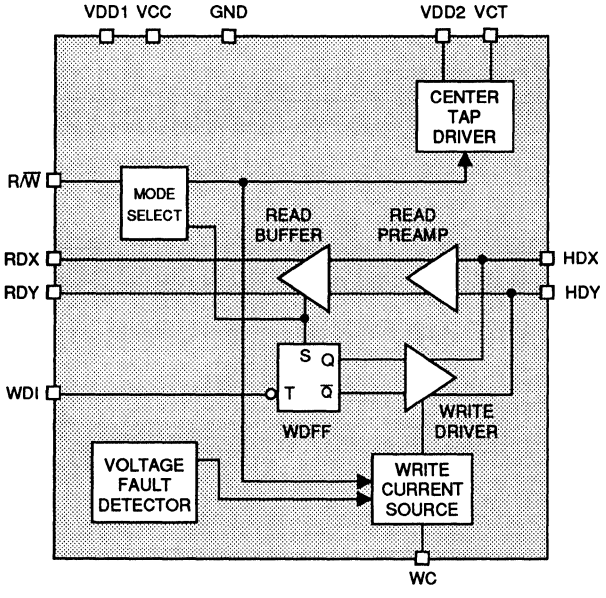
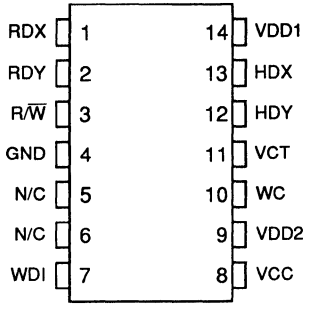
BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

SSI 32H566R
Ferrite Single-Channel
Servo Read/Write Device

CIRCUIT OPERATION

The SSI 32H566R provides center-tapped ferrite head write drive or read amplification. Mode control is accomplished with pin R/$\overline{W}$. Internal resistor pullups, provided on pin R/$\overline{W}$, will force the device into a non-writing condition if a control line is opened accidentally.

WRITE MODE

The write mode configures the SSI 32H566R as a current switch. Write current is toggled between the X and Y side of the selected head on each high to low transition of the Write Data Input (WDI).

The magnitude of the write current (0-pk) is programmed by an external resistor RWC, connected from pin WC to ground and is given by:

$$Iw = \frac{K}{Rwc}$$

where K is the Write Current Constant.

Note that actual head current Ix, y is given by:

$$Ix, y = \frac{Iw}{1 + Rh/Rd}$$

Where: Rh = Head resistance plus external wire resistance
Rd = Damping resistance

Power supply fault protection improves data security by disabling the write current generator during a voltage fault or power supply sequencing.

To reduce internal power dissipation, an optional external resistor, RCT, given by RCT ≤ 130Ω x 40/Iw (Iw in mA), is connected between pins VDD1 and VDD2. Otherwise connect pin VDD1 to VDD2.

To initialize the Write Data Flip Flop (WDFF) to pass current through the X-side of the head, pin WDI must be low when the previous read mode was commanded.

READ MODE

The read mode configures the SSI 32H566R as a low noise differential amplifier and deactivates the write current generator. The RDX and RDY outputs are emitter followers. These outputs should be AC coupled to the load. The RDX, RDY common mode voltage is maintained in the write mode, minimizing the transient between write mode and read mode, substantially reducing the write to read recovery time in the subsequent pulse detection circuitry.

PIN DESCRIPTIONS

NAME	TYPE	DESCRIPTION
R/$\overline{W}$	I	Read/Write - A high level selects Read Mode
WDI	I	WRITE DATA IN - Negative transition toggles direction of head current
HDX, HDY	I/O	X,Y head connections
RDX, RDY	O	X, Y READ DATA - Differential read signal output
WC	I	WRITE CURRENT - Used to set the magnitude of the write current
VCT	O	VOLTAGE CENTER TAP - Voltage source for head center tap
VCC	-	+5V
VDD1	-	+12V
VDD2	-	Positive power supply for the center-tap voltage source
GND	-	GROUND

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

All voltages referenced to GND. Currents into device are positive. Maximum limits indicate when permanent device damage occurs. Continuous operation at these levels is not intended and should be limited to those conditions specified in the DC Operating Characteristics.

PARAMETER		RATING	UNIT
VDD1	DC Supply Voltage	-0.3 to +14	VDC
VDD2	DC Supply Voltage	-0.3 to +14	VDC
VCC	DC Supply Voltage	-0.3 to +7	VDC
V_{IN}	Digital Input Voltage Range	-0.3 to VCC + 0.3	VDC
V_H	Head Port Voltage Range	-0.3 to VDD1 + 0.3	VDC
Iw	Write Current (0-pk)	60	mA
	RDX, RDY (Io) Output Current	-10	mA
	VCT Output Current	-60	mA
Tstg	Storage Temperature Range	-65 to 150	°C
	Lead Temperature PDIP, Flat Pack (10 sec Soldering)	260	°C
	Package Temperature PLCC, SO (20 sec Reflow)	215	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VDD1	DC Supply Voltage		10.8	12.0	13.2	VDC
VCC	DC Supply Voltage		4.5	5.0	5.5	VDC
Lh	Head Inductance				15	µH
RCT*	RCT Resistor	Iw = 40 mA	123	130	137	Ω
Iw	Write Current (0-pk)		10		40	mA
Tj	Junction Temperature Range		+25		+135	°C

*For Iw = 40 mA. At other Iw levels refer to Applications Information that follows this specification.

DC CHARACTERISTICS (Recommended operating conditions apply unless otherwise specified.)

POWER SUPPLY

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VCC Supply Current					
Read	Read Mode			13	mA
Write	Write Mode			25	mA
VDD Supply Current (sum of VDD1 and VDD2)					
Read	Read Mode			33	mA
Write	Write Mode			10+Iw	mA
Power Dissipation (Tj = +135°C)					
Read	Read Mode			500	mW
Write	Write Mode, Iw = 40 mA, RCT = 0Ω			700	mW
	Write Mode, Iw = 40 mA, RCT = 130Ω			500	mW

DIGITAL I/O

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VIL	Input Low Voltage				0.8	VDC
VIH	Input High Voltage		2.0			VDC
IIL	Input Low Current	VIL = 0.8V	-0.4			mA
IIH	Input High Current	VIH = 2.0V			100	µA

WRITE MODE

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VCT	Center Tap Voltage	Write Mode		6.7		VDC
Head Current (per side)		Write Mode, 0 ≤ VCC ≤ 3.7V, 0 ≤ VDD1 ≤ 8.7V	-200		200	µA
Write Current Range			10		40	mA
Write Current Constant "K"			2.375		2.625	V
Iwc to Head Current Gain				0.99		mA/mA
RDX, RDY Output Offset Voltage		Write/Idle Mode	-20		+20	mV

WRITE MODE (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
RDX, RDY Common Mode Output Voltage	Write/Idle Mode		5.3		VDC
RDX, RDY Leakage	RDX, RDY = 6V Write/Idle Mode	-100		100	µA

READ MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VCT Center Tap Voltage	Read Mode		4.0		VDC
Head Current (per side)	Read or Idle Mode 0 ≤ VCC ≤ 5.5V 0 ≤ VDD1 ≤ 13.2V	-200		200	µA
Input Bias Current (per side)				45	µA
Output Offset Voltage	Read Mode	-615		+615	mV
Common Mode Output Voltage	Read Mode	4.5		6.5	VDC

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DYNAMIC CHARACTERISTICS AND TIMING
(Iw = 35 mA, Lh = 10 µH, f(WDI) = 5 MHz, CL(RDX, RDY) ≤ 20 pF. Recommended operating conditions apply unless otherwise specified.)

WRITE MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Differential Head Voltage Swing		7.0			V(pk)
Differential Output Capacitance				15	pF
Differential Output Resistance		600		960	Ω

READ MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Differential Voltage Gain, R_L = 100Ω	Vin = 1 mVpp @ 300 KHz ZL(RDX), ZL(RDY) = 1 KΩ	125		175	V/V
Dynamic Range	AC Input Voltage, Vi, @ 300 KHz Where Gain Falls by 10%.	2			mVpp

READ MODE (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Bandwidth (-3dB)	|Zs| < 5Ω, Vin = 1 mVpp	30			MHz
Input Noise Voltage	BW = 15 MHz, Lh = 0, Rh = 0			1.5	$nV/\sqrt{Hz}$
Differential Input Capacitance	f = 5 MHz			20	pF
Differential Input Resistance	f = 5 MHz	500		1000	Ω
Common Mode Rejection Ratio	Vcm = VCT + 100 mVpp @ 5 MHz	50			dB
Power Supply Rejection Ratio	100 mVpp @ 5 MHz on VDD1, VDD2 or VCC	45			dB
Single Ended Output Resistance	f = 5 MHz			30	Ω
Output Current	AC Coupled Load, RDX to RDY	±2.1			mA

SWITCHING CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
R/$\overline{W}$					
R/$\overline{W}$ To Write Mode	Delay to 90% of Write Current			1.0	µs
R/$\overline{W}$ to Read Mode	Delay to 90% of 100 mV 10 MHz Read Signal Envelope or to 90% decay of Write Current			1.0	µs
Head Current (Lh = 0µH, Rh = 0Ω)					
Prop Delay - TD1	From 50% points, WDI to I(x-y)			25	ns
Asymmetry	WDI has 50% duty cycle and 1 ns Rise/Fall Time			2	ns
Rise/Fall Time	10% - 90% points			20	ns

APPLICATIONS INFORMATION

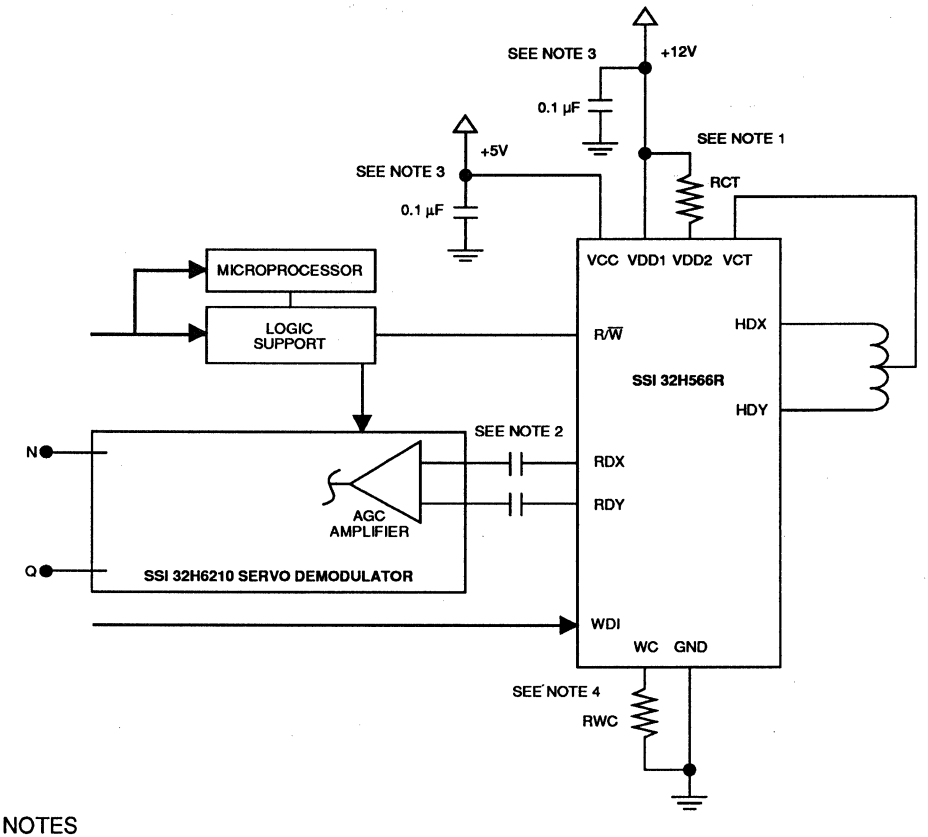
The specifications, provided in the data section, account for the worst case values of each parameter taken individually. In actual operation, the effects of worst case conditions on many parameters correlate. Tables 3 & 4 demonstrate this for several key parameters. Notice that under the conditions of worst case input noise, the higher read back signal resulting from the higher input impedance can compensate for the higher input noise. Accounting for this correlation in your analysis will be more representative of actual performance.

TABLE 3: KEY PARAMETERS UNDER WORST CASE INPUT NOISE CONDITIONS

PARAMETER	Tj=25°C	Tj=125°C	UNIT
Inputs Noise Voltage (max.)	1.1	1.5	$nV/\sqrt{Hz}$
Differential Input Resistance (min.)	850	1000	Ω
Differential Input Capacitance (max.)	11.6	10.8	pF

TABLE 4: KEY PARAMETERS UNDER WORST CASE INPUT IMPEDANCE CONDITIONS

PARAMETER	Tj=25°C	Tj=125°C	UNIT
Inputs Noise Voltage (max.)	0.92	1.2	$nV/\sqrt{Hz}$
Differential Input Resistance (min.)	500	620	Ω
Differential Input Capacitance (max.)	10.1	10.3	pF



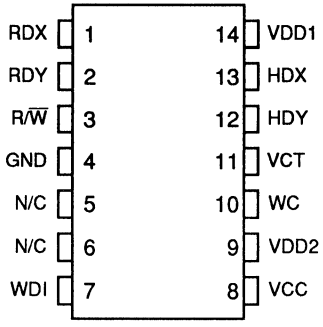
NOTES

1. An external resistor, RCT, given by; RCT ≤ 130 (40/Iw) where Iw is the zero-peak write current in mA, can be used to limit internal power dissipation. Otherwise connect VDD2 to VDD1.
2. Limit DC current from RDX and RDY to 100 µA and load capacitance to 20 pF.
3. The power bypassing capacitor must be located close to the device with its ground returned directly to device ground, with as short a path as possible.
4. To reduce ringing due to stray capacitance this resistor should be located close to the device. Where this is not desirable a series resistor can be used to buffer a long WC line.

FIGURE 2: Typical Application

PACKAGE PIN DESIGNATIONS

(TOP VIEW)



14-Pin SON

THERMAL CHARACTERISTICS: Øja = 130 °C/W

6

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32H566R Servo Ferrite Single Channel Read/Write Device		
14-Pin SON	32H566R-N	32H566R-N

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 731-7110, FAX (714) 573-6914

Notes:

silicon systems®
A TDK Group Company

SSI 32H569
Servo Motor Driver

December 1991

DESCRIPTION

The SSI 32H569 Servo Motor Driver is a bipolar device intended for use in Winchester disk drive head positioning systems employing linear or rotary voice coil motors. When used in conjunction with a position controller, such as the SSI 32H6220 Servo Controller, and a position reference, such as the SSI 32H6210 Servo Demodulator, the device allows the construction of a high performance, dedicated surface head positioning system.

The SSI 32H569 serves as a transconductance amplifier by driving 4 MOSFETs in an H-bridge configuration, performs motor current sensing and limits motor current and velocity. In its linear tracking mode, class B operation is guaranteed by crossover protection circuitry, which ensures that only one MOSFET in each leg of the H-bridge is active. The MOSFET drivers are disabled when motor velocity or current exceed externally programmable limits. In addition, automatic head retraction and spindle braking may be initiated by a low voltage condition or upon external command.

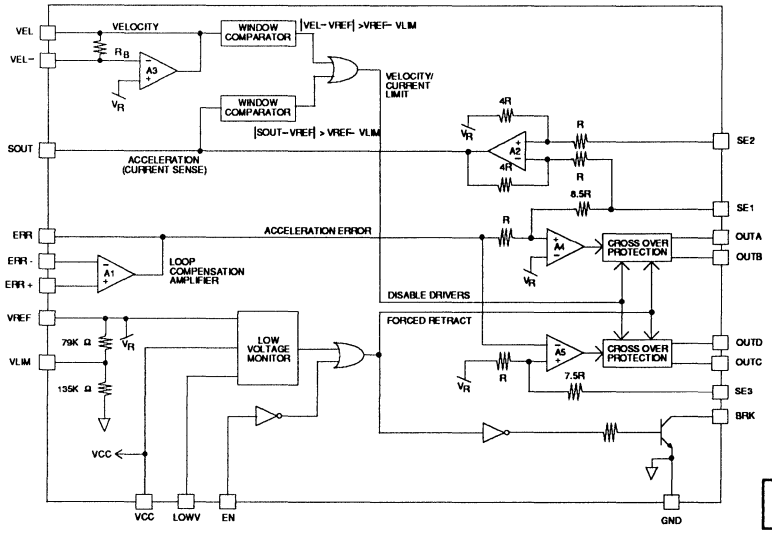
(Continued)

FEATURES

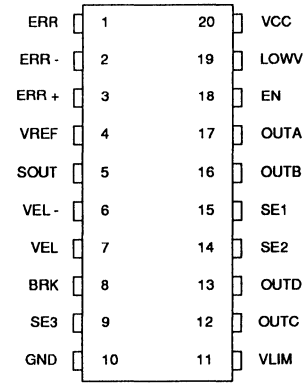
- **Predriver for linear and rotary voice coil motors**
- **Interfaces directly to MOSFET H-Bridge motor driver**
- **Class B linear mode and constant velocity retract mode**
- **Precision differential amplifier for motor current sensing**
- **Motor current and velocity limiting circuitry**
- **Automatic head retract and spindle braking signal on power failure**
- **External digital enable**
- **Servo loop parameters programmed with external components**
- **Advanced bipolar IC requires under 240 mW from 12V supply**
- **Available in 20-pin DIP or SO packaging**

6

BLOCK DIAGRAM



PIN DIAGRAM



20-Pin SO, DIP

CAUTION: Use handling procedures necessary for a static sensitive component.

DESCRIPTION (Continued)

The SSI 32H569 is implemented in an advanced bipolar process and dissipates less than 240 mW from a 12V supply. The IC is available in 20-pin DIP and 20-pin SO packaging.

FUNCTIONAL DESCRIPTION

(Refer to block diagram and typical application Fig.2)

The SSI 32H569 has two modes of operation, linear and retract. The retract mode is activated by a power supply failure or when the control signal EN is false. Otherwise the device operates in linear mode.

During linear operation, an acceleration signal from the servo controller is applied through amplifier A1, whose three connections are all available externally. RC components may be used to provide loop compensation at this stage. The ERR signal drives two precision amplifiers, each with a gain of 8.5. The first of these amplifiers is inverting, and is formed from opamp A4, an on-chip resistor divider and an off-chip complementary MOSFET pair. The second is non-inverting, and is formed in a similar manner from opamp A5. Feedback from the MOSFET drains, on sense inputs SE1 and SE3, allows the amplifiers gains to be established precisely. The voice coil motor and a series current sense resistor are connected between SE1 and SE3.

Crossover protection circuitry between the outputs of A4 and A5, and the external MOSFETs, ensures class B operation by allowing only one MOSFET in each leg of the H-bridge to be in conduction. The crossover separation threshold, illustrated in Figure 5, is the maximum drive on any MOSFET gate when the motor voltage changes sign. The crossover circuitry can also disable all MOSFETS simultaneously (to limit motor current or velocity) or apply a constant voltage across the motor (to retract the heads at a constant velocity).

Motor current is sensed by a small resistor placed in series with the motor. The voltage drop across this resistor is amplified by a differential amplifier with a gain of 4 (A2 and associated resistors), whose inputs are SE1 and SE2. The resulting voltage, SOUT, is proportional to motor current, and hence acceleration. This signal is externally fed back to A1, so that the signal ERR represents the difference between the desired acceleration (from the servo controller) and the actual motor acceleration. If SOUT is integrated, using opamp A3 and an external RC network, the resulting signal, VEL, is proportional to the motor velocity.

Both SOUT and VEL are connected to window comparators, which are used to detect excessive motor current or velocity. The comparator outputs disable the MOSFET drivers until the motor comes within limits again. The VLIM pin may be used to program the voltage limits for the window comparators. The maximum voltage excursion allowed about VREF is (VREF-VLIM). An on-chip resistor divider sets a default value for VLIM and if VLIM is connected to ground, the windowing is effectively disabled.

The SSI 32H569 has low voltage monitor circuitry that will detect a loss of voltage on the VREF, VCC or LOWV pins. The power supply pin, VCC, should be connected to the disk drive's spindle motor so that its stored rotational energy may be used to hold up VCC briefly during a power failure. LOWV is used to detect a system power supply failure. When a low voltage condition is detected, the MOSFET drivers switch from linear operation to retract mode. In this mode a constant voltage is applied across the motor which will cause the heads to move at a constant speed. A mechanical stop must be provided for the heads when they reach a safe location. The current limiting circuitry will disable the MOSFET drivers when motor current increases due to loss of the velocity-induced back EMF. An open collector output, BRK, which is active while the device is in retract mode, is provided for spindle motor braking. An external RC delay may be used to defer braking until the heads are retracted. For proper operation of the SSI 32H569, a pullup resistor on BRK is required even if the BRK output is not used.

An example of an entire servo path implemented with the SSI 32H569 and its companion devices, the SSI 32H6210 and 32H6220, is shown in Figure10.

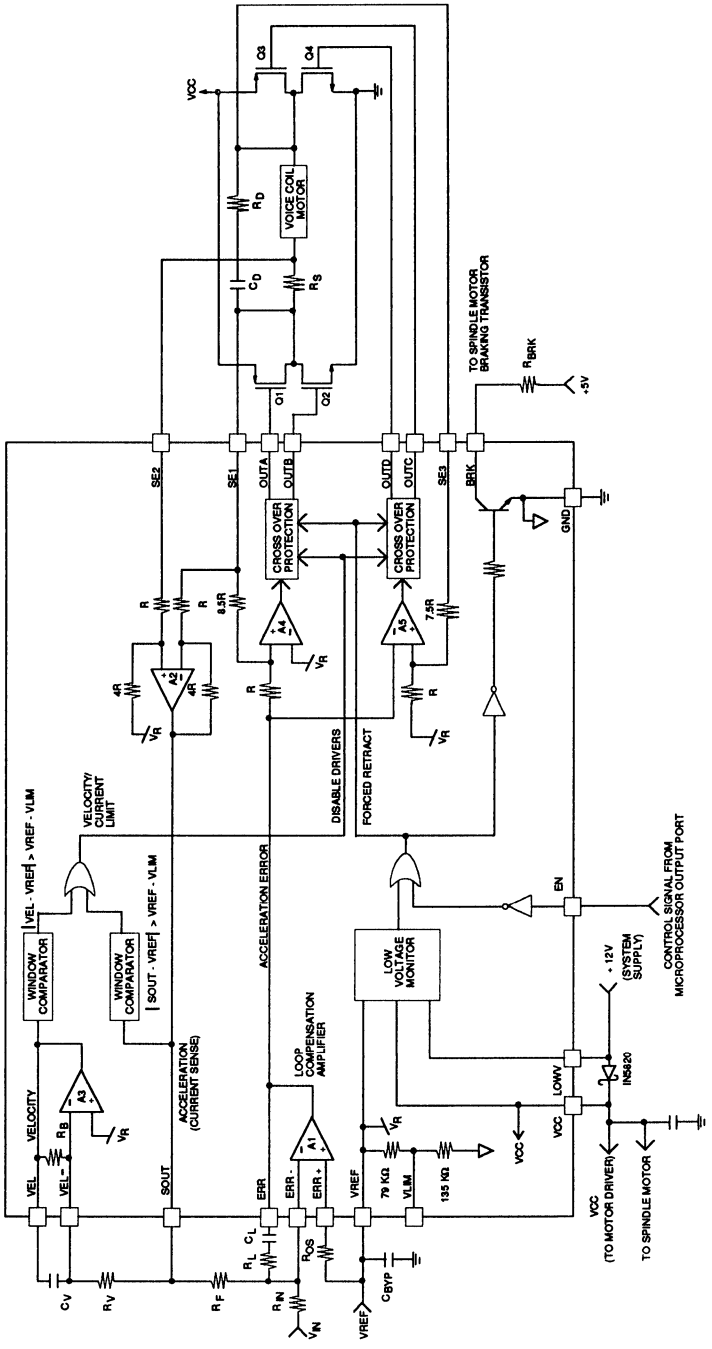


FIGURE 2: Typical Application

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PIN DESCRIPTION

POWER

NAME	PIN	TYPE	DESCRIPTION
VCC	20		POSITIVE SUPPLY - 12V power supply. Usually taken from spindle motor supply. Spindle motor stored energy permits head retraction during power failure. If VCC falls below 9V, a forced head retraction occurs.
LOWV	19	I	LOW VOLTAGE - System 12V supply. If this input falls below 9V, a forced head retraction occurs.
VREF	4	I	REFERENCE VOLTAGE - 5.4V input. All analog signals are referenced to this voltage. If VREF falls below 4.3V, a forced head retraction occurs.
GND	10		GROUND

CONTROL

NAME	PIN	TYPE	DESCRIPTION
ERR	1	O	POSITION ERROR- Loop compensation amplifier output. This signal is amplified by the MOSFET drivers and applied to the motor by an external MOSFET H-bridge, as follows: SE3-SE1 = 17(ERR-VREF)
ERR-	2	I	POSITION ERROR INVERTING INPUT - Inverting input to the loop compensation amplifier.
ERR+	3	I	POSITION ERROR NON-INVERTING INPUT - Non-inverting input to the loop compensation amplifier.
SOUT	5	O	MOTOR CURRENT SENSE OUTPUT - This output provides a voltage proportional to the voltage drop across the external current sense resistor, as follows: SOUT-VREF=4(SE2-SE1)
VEL-	6	I	VELOCITY INVERTING INPUT - Inverting input to the velocity integrating amplifier. The non-inverting input is connected internally to VREF.
VEL	7	O	VELOCITY OUTPUT - Output of the velocity integration amplifier. This signal is internally applied to a window comparator whose output limits motor drive current when the voltage at VEL exceeds a set limit.
BRK	8	O	BRAKE OUTPUT - Active high, open collector output which may be used to enable an external spindle motor braking transistor upon power failure or deassertion of EN.
VLIM	11	I	LIMITING VOLTAGE - The voltage at this pin sets motor current and velocity limits. Limiting occurs when: |SOUT-VREF|>VREF-VLIM or |VEL-VREF|>VREF-VLIM. An internal resistor divider establishes a default value that may be externally adjusted.

CONTROL (Continued)

NAME	PIN	TYPE	DESCRIPTION
SE2	14	I	MOTOR CURRENT SENSE INPUT - Non-inverting input to the current sense differential amplifier. It should be connected to one side of an external current sensing resistor in series with the motor. The inverting input of the differential amplifier is connected internally to SE1.
EN	18	I	ENABLE - Active high TTL compatible input enables linear tracking mode. A low level will initiate a forced head retract.

FET DRIVE

NAME	PIN	TYPE	DESCRIPTION
SE3	9	I	MOTOR VOLTAGE SENSE INPUT - This input provides feedback to the non-inverting MOSFET driver amplifier. It is connected to one side of the motor. The gain to this point is: SE3-VREF = 8.5(ERR-VREF)
OUTC	12	O	P-FET DRIVE (NON-INVERTING) - Drive signal for a P channel MOSFET connected between one side of the motor and VCC. This MOSFET drain is connected to SE3.
OUTD	13	O	N-FET DRIVE (NON-INVERTING) - Drive signal for an N channel MOSFET connected between one side of the motor and GND. This MOSFET drain is connected to SE3. Crossover protection circuitry ensures that the P and N channel devices driven by OUTC and OUTD are never enabled simultaneously.
SE1	15	I	MOTOR VOLTAGE SENSE INPUT - This input provides feedback to the inverting MOSFET driver amplifier. It is connected to the current sensing resistor which is in series with the motor. The gain to this point is: SE1-VREF = -8.5(ERR-VREF) This input is internally connected to the current sense differential amplifier inverting input.
OUTB	16	O	N-FET DRIVE (INVERTING) - Drive signal for an N channel MOSFET connected between the current sense resistor and GND. This MOSFET drain is also connected to SE1.
OUTA	17	O	P-FET DRIVE (INVERTING) - Drive signal for a P channel MOSFET connected between the current sense resistor and VCC. This MOSFET drain is also connected to SE1. Crossover protection circuitry ensures that the P and N channel devices driven by OUTC and OUTD are never enabled simultaneously.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

(Maximum limits indicates where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC operating characteristics.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VCC		0		16	V
VREF		0		10	V
SE1, SE2, SE3		-1.5		15	V
All other pins		0		14	V
Storage temperature		-45		165	°C
Solder temperature	10 sec duration			260	°C

RECOMMENDED OPERATION CONDITIONS (Unless otherwise noted, the following conditions are valid throughout this document.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VCC	Normal Mode	9	12	13.2	V
	Retract Mode	3.5V		14	V
VREF		5		7	V
Operating temperature		0		70	°C

DC CHARACTERISTICS

ICC, VCC current				20	mA
IREF, VREF current				2	mA

A1, LOOP COMPENSATION AMPLIFIER

Input bias current				500	nA
Input offset voltage				3	mV
Voltage swing	About VREF	2			V
Common mode range	About VREF	±1			V
Load resistance	To VREF	4			KΩ
Load capacitance				100	pF
Gain		80			dB
Unity gain bandwidth		1			MHz
CMRR	f<20 kHz	60			dB
PSRR	f<20 kHz	60			dB

A2, CURRENT SENSE AMPLIFIER

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input impedance	SE1 to SE2	3.5	5		KΩ
Input offset voltage				2	mV
Output voltage swing		VREF-4		VCC-1.2	V
Common mode range		0		VCC-0.2	V
Load Resistance	To VREF	4			KΩ
Load Capacitance				100	pF
Output impedance	f<40 KHz			20	Ω
Gain (SOUT-VREF)/(SE1-SE2)		3.9	4	4.1	V/V
Unity gain bandwidth		1			MHz
CMRR	f<20 KHz	52			dB
PSRR	f<20 KHz	60			dB

A3, VELOCITY INTEGRATING AMPLIFIER

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input bias current				250	nA
Input offset voltage				2	mV
Voltage swing		VREF-4		VCC-1.2	V
Common mode range		4.5		6	V
Load resistance	To VREF	10			KΩ
Load capacitance				100	pF
RB, internal feedback resistor		80		150	KΩ

WINDOW COMPARATORS AND LIMITING

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Window comparator threshold (SOUT-VREF or VEL-VREF)		VREF-VLIM			V
Threshold hysteresis		35	50	65	%
VLIM voltage	No external parts	VREF-1.8		VREF-2.2	V
VLIM input resistance		50			KΩ

POWER SUPPLY MONITOR

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VCC fail threshold		8.5	9	9.8	V
LOWV fail threshold	|ILowv| < 0.5 mA	8.5	9	9.8	V
VREF fail threshold		3.9	4.3	4.8	V
Hysteresis (LOWV, VCC)			250		mV
Hysteresis (VREF)			110		mV
EN input low voltage	|IIL| < 0.5 mA	0.8			V
EN input high voltage	|IIH| < 40 uA			2	V
BRK voltage	normal mode, |IOL| < 1 mA			0.4	V
BRK leakage current	retract mode			10	µA
BRK delay (from power fail or EN false to BRK floating)				1	ms

MOSFET DRIVERS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SE3 Input impedance	To VREF	10	25		KΩ
OUTA, OUTC voltage swing |Io|<1 mA		0.7		VCC-1	V
OUTB, OUTD voltage swing |Io|<1 mA		1		VCC-1	V
VTH, Crossover separation threshold				2	V
Slew rate (OUTA, OUTB, OUTC, OUTD)	Cl<1000 pF	1.4			V/µs
Crossover time	300 mV step at ERR			5	µs
Output impedance (OUTA,B,C,D)			50		KΩ
Transconductance I(OUTA,B,C,D)/(ERR-VREF)			8		mA/V
Gain (-(SE1-VREF)/(ERR-VREF) or (SE3-VREF)/(ERR-VREF))		8	8.5	9	V/V
Offset current	R_S = 0.2Ω, R_F = R_{IN}, V_{IN}=VREF			20	mA
Retract motor voltage (SE1-SE3)		0.7	1	1.3	V

APPLICATIONS INFORMATION

A typical SSI 32H569 application is shown in Figure 2. The selection criteria for the external components shown are discussed below. Figure 3 shows the equivalent circuit and equations for the DC motor used in the following derivations. While the nomenclature chosen is for a rotating motor, the results are equally applicable to linear motors.

MOTOR CURRENT SENSE AND LIMITING

The series resistor which senses motor current, Rs, is chosen to be small compared to the resistance of the motor, Rm. A value of Rs = 0.2Ω is typical in disk drive applications. The window comparator threshold, programmed by VLIM, must be chosen to cause limiting when the motor current reaches its maximum permissible value. If iMAX is the maximum motor current in Amps, then this value may be chosen as follows:

$$VLIM = VREF - 4 \cdot R_s \cdot iMAX \ (V)$$

VLIM may be set with a resistor divider whose thevenin resistance is substantially less than the output resistance of the VLIM pin (50 KΩ). The window comparators have hysteresis (typically 50% of their threshold, VREF-VLIM) to prevent multiple triggerings of the driver disable signal.

VELOCITY LIMITING

The values of Rv and Cv in the velocity integrator are chosen to produce a voltage excursion of VREF-VLIM, when the motor speed is at its maximum permissible value. Rv must be large enough to prevent overloading of opamp A2. The following equation ignores the effect of RB, the internal resistor between VEL and VEL- which prevents saturation of A3 due to offsets. For the motor in Figure 3, with maximum velocity ωMAX (rad/s) these components may be chosen as follows:

$$R_V // R_F > 4K\Omega \ (\text{A2 output loading restriction})$$

$$C_V = \frac{4 R_s \cdot J\theta \cdot \omega MAX}{(VREF - VLIM) \cdot R_V \cdot K_m} \ (F)$$

LOOP COMPENSATION

The transfer function of the SSI 32H569 in the application of Figure 2 is shown in figure 4(a). If the zero due to RL and CL in the loop compensation circuit is chosen to cancel the pole due to the motor inductance, Lm, then the transfer function can be simplified as shown in figure 4(b), under the assumption that this pole and the pole due to the motor mechanical response are widely separated. CL may then be chosen to set the desired open loop unity gain bandwidth.

$$C_L = \frac{68 \cdot R_s}{2 \cdot \pi \cdot R_F \cdot (R_m + R_s) \cdot BW}$$

where BW is the unity gain open loop bandwidth

$$R_L = \frac{L_m}{C_L \cdot (R_m + R_s)}$$

The closed loop response of the servo driver and motor combination, using the component values and simplifying assumptions given above, is given by:

$$\frac{i_m}{V_{in}}(s) = -\frac{1}{R_{in}} \cdot \frac{R_F}{4 \cdot R_s} \cdot \frac{1}{(1 + \frac{s}{2 \cdot \pi \cdot BW})}$$

(This analysis neglects the pole due to the output impedance of the MOSFET drivers and the MOSFET gate capacitance, an effect that may be significant in some systems).

RF is chosen to be sufficiently large to avoid overloading A2 ($R_F // R_V > 4K\Omega$). The input resistor, RIN, sets the conversion factor from servo controller output voltage to servo motor current. RIN is chosen such that the servo controller internal voltages are scaled conveniently. The resistor ROS is optional and cancels out the effect of the input bias current of A1.

$$R_{os} = R_{in} // R_F$$

The external components RD and CD have no effect on the motor dynamics, but may be used to improve the stability of the MOSFET drivers. The load represented by the motor, ZM, is given by:

At frequencies above $(R_S+R_M)/(2 \cdot \pi \cdot L_M)$ Hz, this load

$$ZM = (R_s + R_m)(1 + s\frac{L_m}{R_s + R_m})(1 + \frac{K_m^2}{s \cdot J\theta \cdot (R_s + R_m)}) \ (\Omega)$$

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becomes entirely inductive, which is undesireable. RD and CD may be used to add some parallel resistive loading at these frequencies.

H-BRIDGE MOSFETS

The MOSFETs chosen for the H-bridge should have gate capacitances in the range of 500-1000 pF. The MOSFET input capacitance forms part of the compensation for the MOSFET drivers, so values below 500 pF may cause some driver instability. Excessive input capacitance will degrade the slew mode performance of the drivers.

When the motor voltage is changing polarity, the crossover protection circuits at outputs OUTA-OUTD ensure that the maximum MOSFET gate drive is less than 2V (the crossover separation threshold), as illustrated in Figure 5. The thresholds of the MOSFET devices chosen should be as large as possible to minimize conduction in this region. If the device thresholds are significantly less than the crossover separation threshold, the N and P channel devices in each leg of the H-bridge will conduct simultaneously, causing unnecessary power dissipation.

POWER FAILURE OPERATION

The power supply for the SSI 32H569, VCC, should be taken from the system 12V supply through a schottky diode (maximum 0.5V drop at If = 3A) and connected to the disk drive spindle motor. If the system power fails, the IC will continue to operate as the spindle motor becomes a generator. The SSI 32H569 will detect the power failure and cause a forced head retract, continuing to operate with VCC as low as 3.5V. The power fail mode will commence if either VCC or LOWV falls below 9V, or VREF falls below 4.3V, or EN is false. Hysteresis on the low voltage thresholds prevents the device from oscillating between operating modes when the power supply is marginal.

The BRK output, which is pulled low during normal operation, floats during a power failure. This allows an external transistor to be enabled for spindle motor braking. An external RC delay may be added to defer braking until head retraction is complete, since the spindle motor is required to generate the supply voltage during retraction.

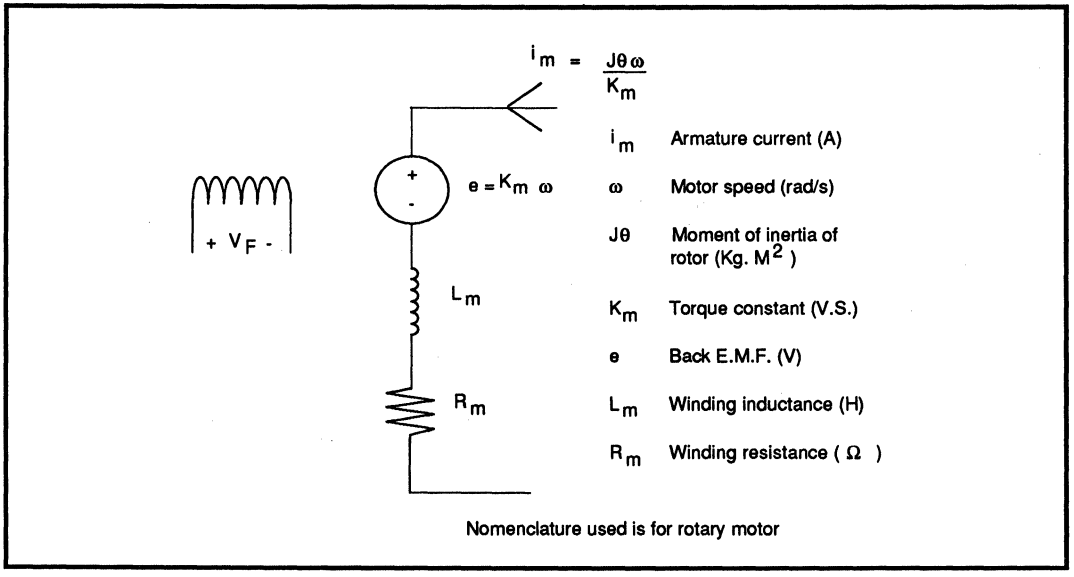

FIGURE 3: Equivelant Circuit For Fixed Field DC Motor

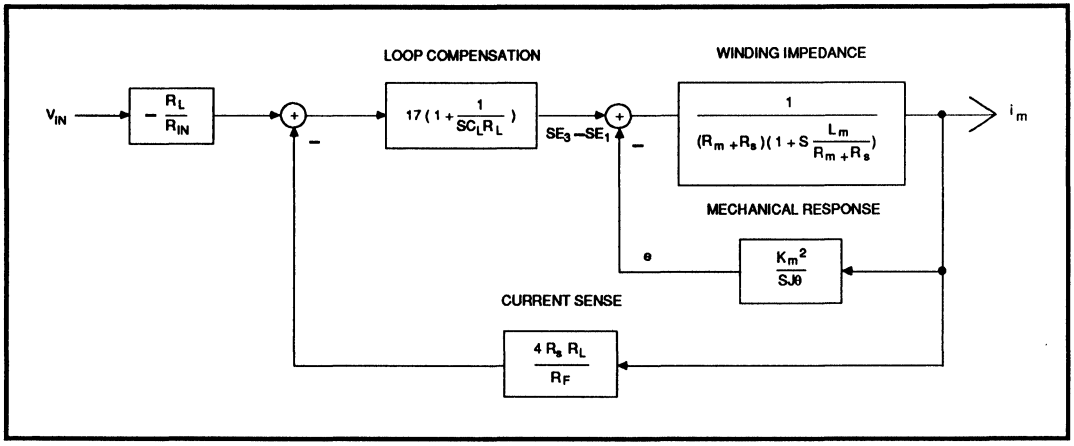

FIGURE 4(A): Transfer Function Of SSI 32H569 In Typical Application With Fixed Field DC Motor

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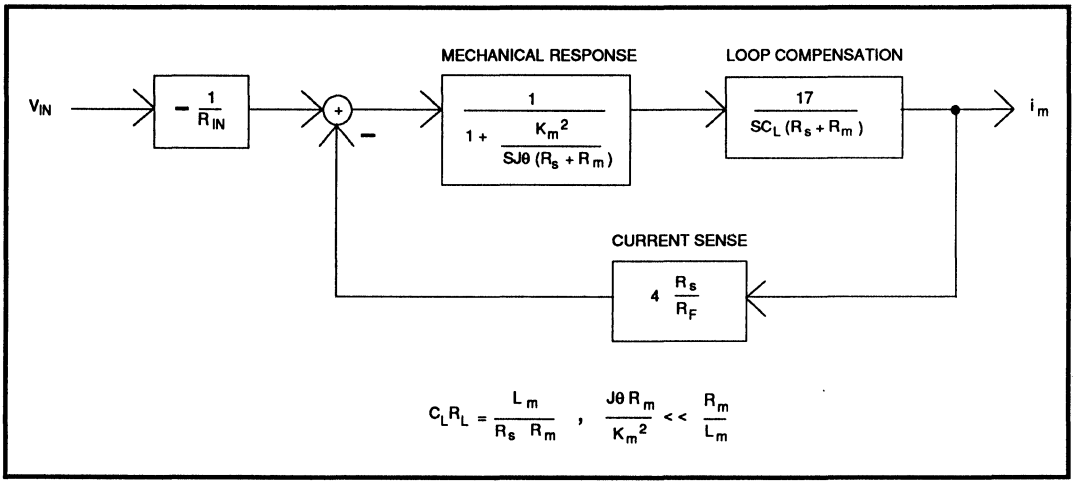


FIGURE 4(B): Simplified Transfer Function Of SSI 32H569 In DC Motor Application

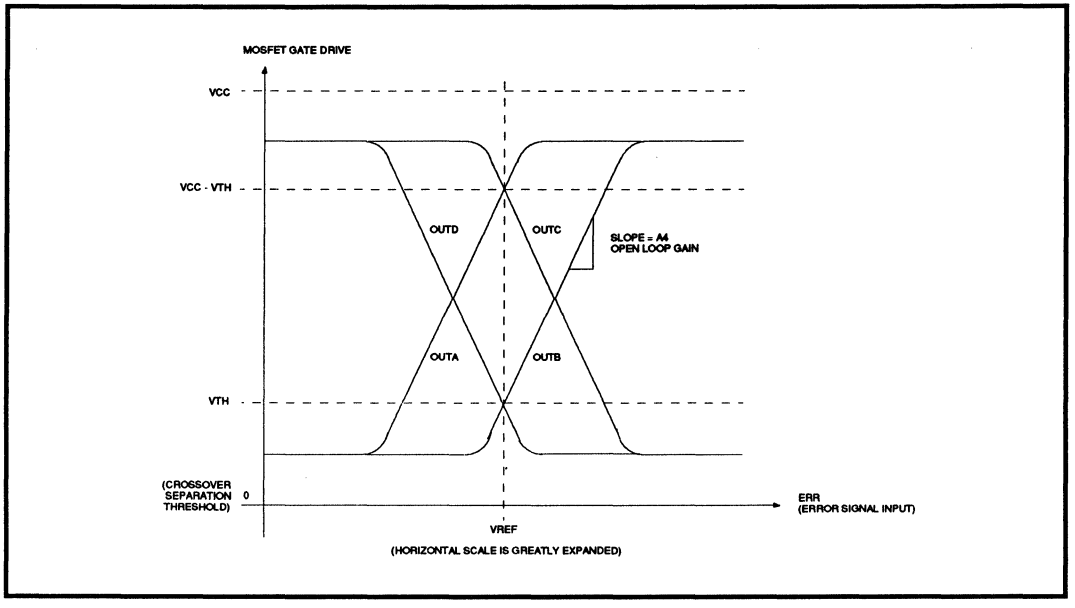


FIGURE 4(B): Simplified Transfer Function Of SSI 32H569 In DC Motor Application

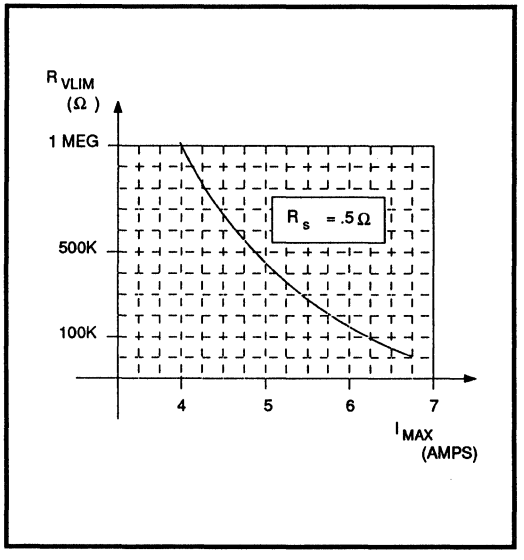


FIGURE 6: RVLIM To Ground Typical Motor Current Limit

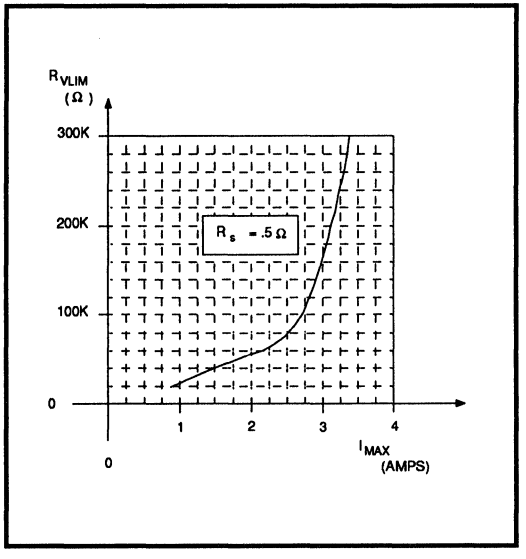


FIGURE 7: RVLIM To VREF Typical Motor Current Limit

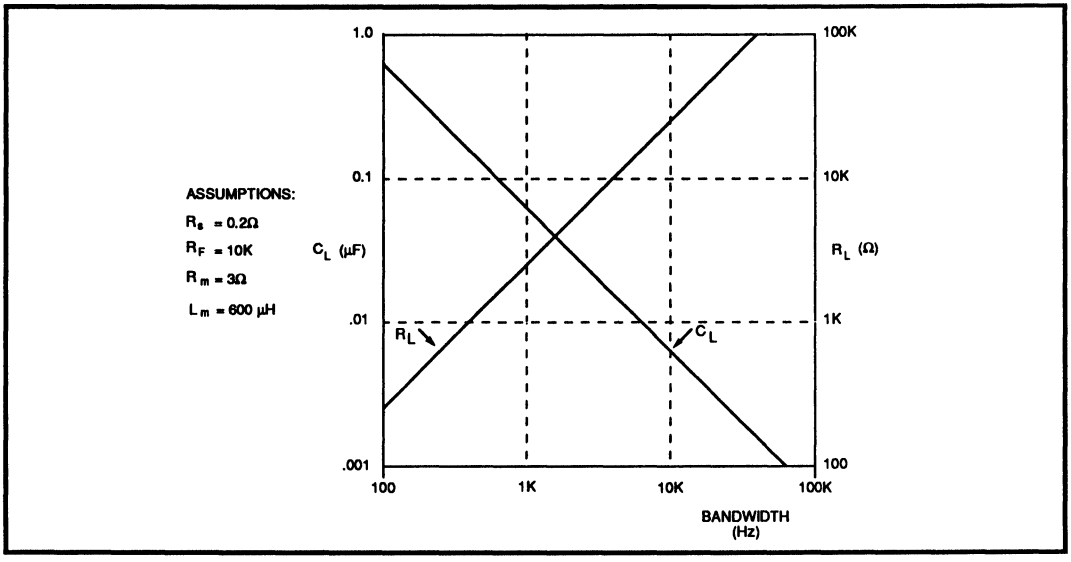


FIGURE 8: Typical Motor Driver Compensation

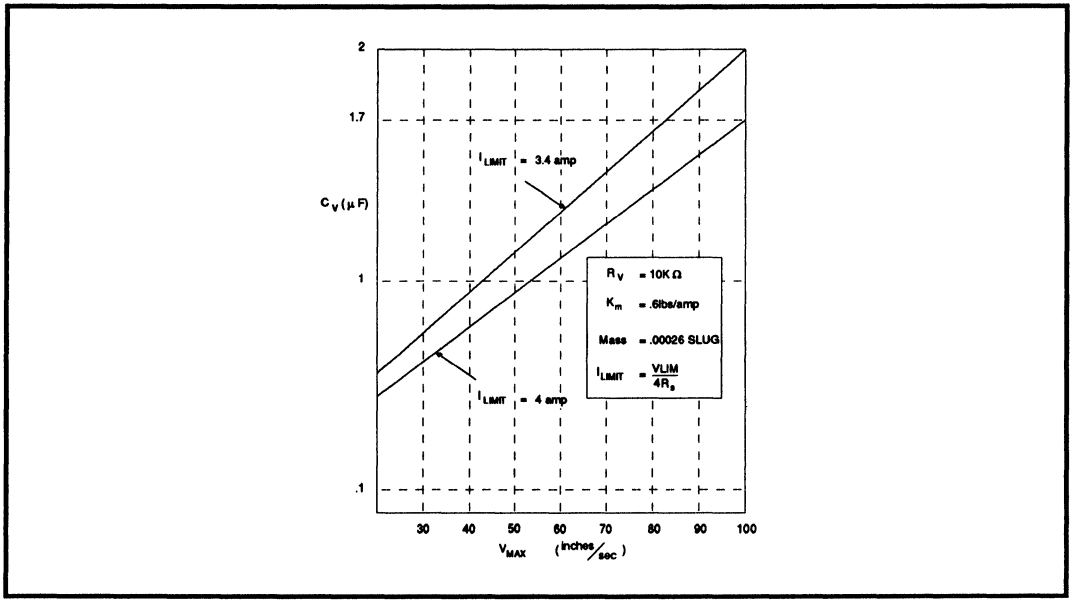


FIGURE 9: Typical Motor Velocity Limit

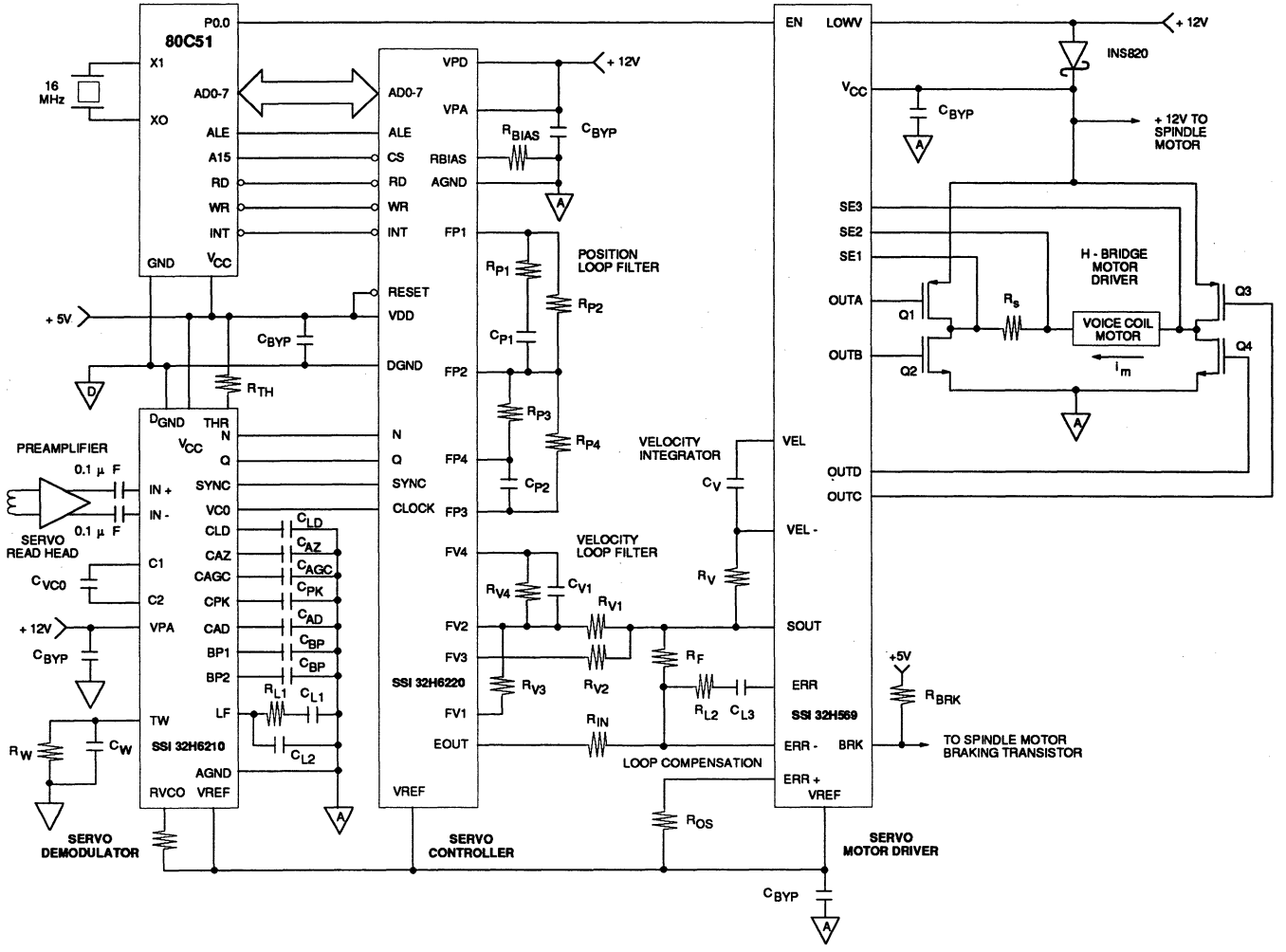
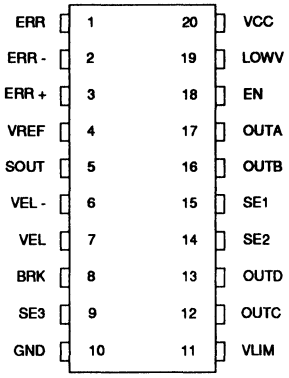


FIGURE 10: Complete Example of Servo Path Electronics Using the SSI 32H6210/ 6220/ 569

PACKAGE PIN DESIGNATIONS

(Top View)



20-Pin SO, DIP

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ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32H569, Servo Motor Driver		
20-Pin DIP	32H569-CP	32H569-CP
20-Pin SOL	32H569-CL	32H569-CL

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 731-7110, FAX (714) 573-6914

Notes:

silicon systems®
A TDK Group Company

SSI 32H4631/4632
Hybrid Servo & Spindle Motor Controller
Advance Information

December 1991

GENERAL DESCRIPTION

The SSI 32H4631/4632 is a CMOS monolithic integrated circuit housed in a 100-pin QFP and operates on a single +5V supply. In addition to supporting Winchester disk drives with embedded servo sectors and dedicated servo surface, it contains all timing and control functions necessary to start, drive, and brake a 3-phase, 4/8/12 pole brushless DC spindle motor without sensors. It also provides an 8-bit A/D converter at a conversion rate up to 250 kHz and a Motorola/Intel compatible bus interface (Motel) to popular microcontrollers such as the 8051 and 68HC11. The features for each functionally different section are summarized in the following:

FEATURES

Servo Head Positioning Control

- Servo control for Winchester disk drives with hybrid servo head positioning systems
- For use in microprocessor-based digital servo applications
- Accepts quadrature position signals N, Q from a dedicated servo demodulator
- 12-bit double-buffered cylinder crossing counter for dedicated seek algorithms
- Timing controller for embedded servo position burst sampling
- Peak detect and sample/hold circuits for up to four embedded servo bursts
- H-bridge MOSFET predriver for linear and rotary voice coil motor
- Class B linear mode and constant voltage retract mode
- Active head retract on power failure

Spindle Motor Speed Control

- 3-phase 4/8/12 pole bipolar/unipolar operation without need for sensors
- Precision speed regulation at 3600 RPM (4631), 5400 RPM (4632) with ± 0.012% speed resolution
- "At speed" indication
- Motor peak current limiting function
- Pulse amplitude modulation (PAM) for bridge MOSFET drivers
- Dynamic braking function on power failure

Data Acquisition and Microprocessor Bus Interface

- Motel bus interface compatible with 8051 and 68HC11
- Ten internal registers and address decoding
- Internal 250 kHz 8-bit A/D and D/A converters

General Functions

- Voltage fault detection for up to two supply voltages
- Write gate guarding
- Low power CMOS design
- 100 pin QFP package

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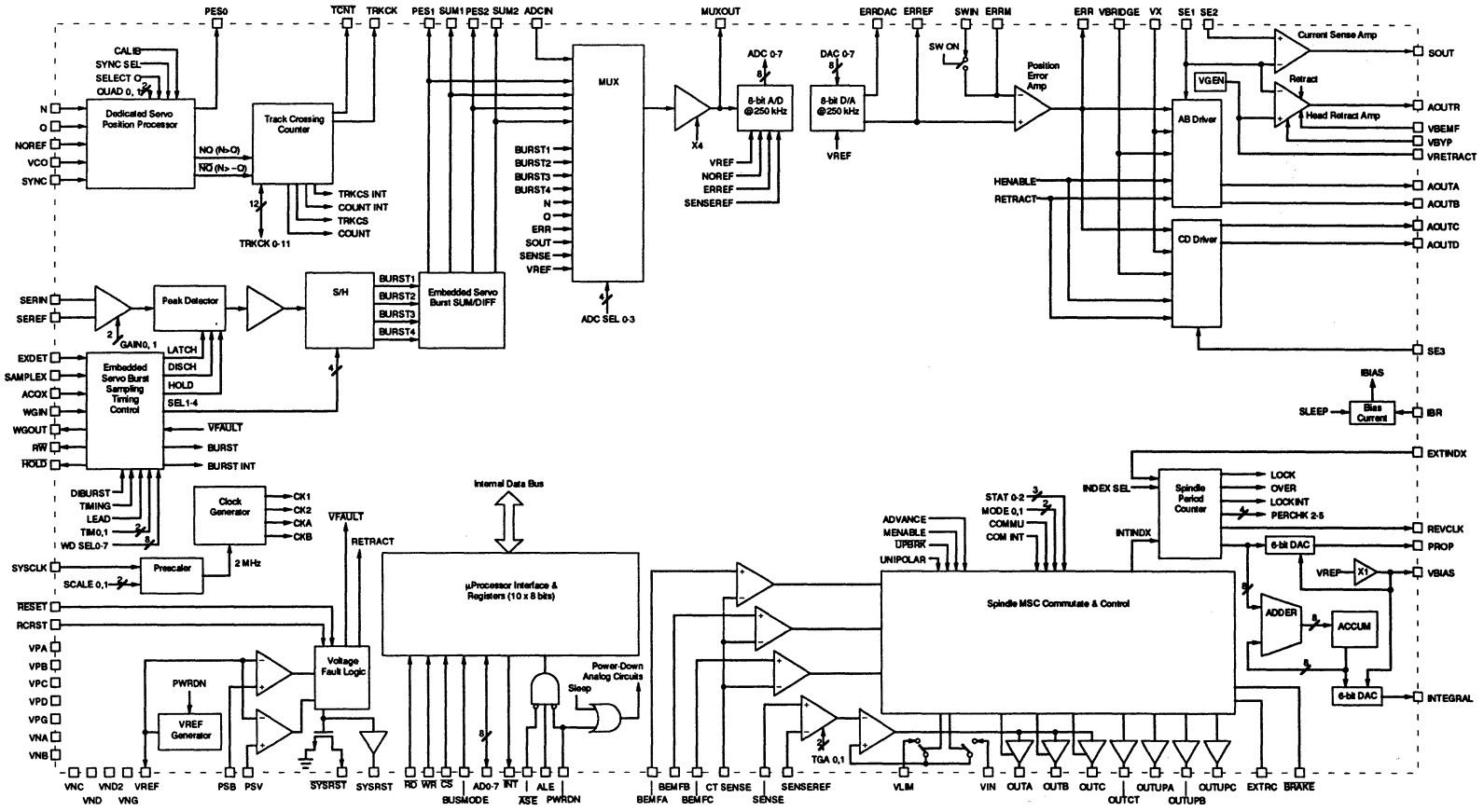

FIGURE 1: SSI 32H4631 Block Diagram

FUNCTIONAL DESCRIPTION

As shown in Figure 1, the SSI 32H4631/4632 can be divided into three major sections: servo head positioning control, spindle motor speed control, data acquisition and microprocessor bus interface.

SERVO HEAD POSITIONING CONTROL

The SSI 32H4631/4632 is intended for a servo head positioner for Winchester disk drives with both embedded servo sectors and a dedicated servo surface. The servo head positioning control section contains the following functions:

1. Dedicated servo position processor
2. Embedded servo burst amplitude processor
3. Embedded servo burst timing controller
4. Servo position error amplifier
5. H-bridge MOSFET predriver
6. Actuator current sense
7. Voltage fault detection and servo head retract

These functions are illustrated in Figure 1.

DEDICATED SERVO POSITION PROCESSOR

The dedicated servo position processor receives quadrature position information from a servo demodulator, such as SSI 32H6210, through analog inputs N, Q and NQREF. The NQREF is applied to establish a DC reference level for N and Q samples. N and Q are sampled at the falling edge of SYNC. The SYNC frequency, which is the servo frame rate on the dedicated servo surface, is generated from the servo demodulator and is no more than 500 kHz. The VCO provides the necessary clock signal to sample N and Q signals. The timing relationship among VCO, SYNC and N, Q is indicated in Figure 2. If it is not necessary to synchronize to N, Q samples, the SYNC input must be grounded and the SYNC SEL bit in the SERVO CONTROL register set HIGH. In this case, the SYSCLK input will be divided down internally to generate the frame rate to sample N and Q signals. The position processor compares N with both Q and -Q to generate digital signals NQ (N>Q) and $N\overline{Q}$ (N>-Q). Since N and Q signals span four tracks per period, NQ and $N\overline{Q}$ provide additional information on which track the head is positioned. In order to produce the position error signal PES0, the position processor selects N, Q, -N or -Q, based upon either the values of bits QUAD0 and QUAD1 when SELECT Q is enable; or the values of the digital signals NQ and $N\overline{Q}$ when SELECT Q is disabled. Note that the analog inputs N and Q to the position processor will switch to the DC reference level, NQREF, when the CALIB bit in the HYBRID SERVO CONTROL register is enabled. This allows calibrating the internal offset of the position error signal, PES0. For digital servo applications, N, Q and PES0 are provided to the internal multiplexed 8-bit A/D converter under µP control.

The SSI 32H4631/4632 supports both hardware and software track counting techniques. The software track counting technique interfaces with bits NQ, $N\overline{Q}$ and TRKCS in the SERVO STATUS register. On each track crossing, either NQ or $N\overline{Q}$ changes state.

An internal timing hysteresis can be provided to prevent multiple state changes on NQ, $N\overline{Q}$ and TRKCS at low head velocities by setting the bit TCHE in the EMBEDDED SERVO GAIN CONTROL register. The TRKCS bit will be reset LOW when the SERVO STATUS REGISTER is read by the µP. The hardware track technique interfaces with TRKCK, an output clock intended to drive a hardware counter such as is available in the Intel 8051 family. TRKCK is normally LOW and pulses HIGH once whenever a track boundary is crossed. A 12-bit double-buffered down counter with programmable loading capability is implemented to aid seek algorithms. The counter is decremented at the LOW-TO-HIGH transition of TRKCK and the register is updated at the HIGH-TO-LOW transition of TRKCK. The 12-bit counter register stops updating after the LSB is read. This ensures consecutive reads provide information that corresponds to a single track. Therefore, one should read the LSB and then the MSB without exception. The counter will produce a LOW level on $\overline{TCNT}$ when the terminal count is reached. $\overline{TCNT}$ remains LOW until the counter is loaded with a new initial value.

EMBEDDED SERVO BURST AMPLITUDE PROCESSOR

The embedded servo burst amplitude processor extracts the fine head position error information from the embedded servo bursts. The circuit acquires up to 4 burst amplitudes BURST1, BURST2, BURST3, and BURST4 from a read data channel, such as the SSI 32P4620, through analog inputs SERIN and SEREF. The SEREF is applied to establish a DC reference level for the full wave-rectified analog signal SERIN.

To accommodate a wide range of servo burst amplitudes, the differential signal between SERIN and SEREF is scaled by a 2-bit programmable gain amplifier under µP control. The gain of the differential amplifier ranges from -6 dB to 3 dB as defined in the EMBEDDED SERVO GAIN CONTROL register. The output of the differential amplifier is then provided to a peak detector which captures the peak voltage within a time interval derived from the internal timing controller or an external timing source through SAMPLEX. The peak voltage is further scaled by a 4-bit programmable gain amplifier under µP control. Thus the gain error introduced by the peak detector can be accurately corrected with this programmable gain amplifier. The gain adjustment ranges from 0 dB to 3 dB in 0.2 dB steps, as defined in the EMBEDDED SERVO GAIN CONTROL register. Each of the following four S/H circuits transfers and holds the scaled peak voltages onto their respective holding capacitors during a time interval defined by the internal timing controller or an external timing source through ACQX. The outputs of S/H circuits, BURST1, BURST2, BURST3, and BURST4, are provided to the 8-bit A/D converter under µP control. Note that the timing windows to acquire the scaled peak voltages can be configurated in any order, as defined in the EMBEDDED SERVO TIMING WINDOW CONTROL register. Therefore, the µP can mix and commutate servo bursts to accommodate for a variety of servo burst formats and maintain the position error signal in a proper polarity. The timing controller also issues a timing signal to discharge the captive voltage for each servo burst.

The captive signals are provided to two difference circuits to extract the differential signals between BURST1, BURST2 and BURST 3, BURST4, respectively. Typically, these differential signals define the distance between the read head and the center of a data track and one of them should be zero while the read head is at the center of a data track. These outputs, available externally on PES1 and PES2, are provided to the 8-bit A/D converter under µP control. Also, two summers add BURST1, BURST2 and BURST3, BURST4, respectively, and their outputs at SUM1 and SUM2 are provided to the 8-bit A/D converter as well.

EMBEDDED SERVO BURST TIMING CONTROLLER

The embedded servo burst timing controller generates all the timing signals to sample the position bursts, as shown in Figures 3 and 4. These timing signals control the discharge, sample, and hold of the peak detector and the four S/H circuits. The EMBEDDED SERVO TIMING WINDOW CONTROL register can be programmed by the µP to select and sample the servo burst pairs in any order. The number of servo position bursts supported are either two or four. The DIBURST bit in the SERVO CONTROL register, when set HIGH, configures the internal timing controller to sample only two servo position bursts. When reset, four servo position bursts are sampled. During position burst sampling, $\overline{HOLD}$ and $\overline{RW}$ will be asserted and WGOUT held LOW.

An external timing controller may be used to provide all the timing signals for the discharge, sample, and hold of the peak detector and the four S/H circuits by setting the TIMING bit HIGH in the SERVO CONTROL register. Usually, in this mode, an external timing controller ASIC will be required to provide the timing signals at SAMPLEX and ACQX for servo position burst sampling while the internal servo timing controller is disabled.

SERVO POSITION ERROR AMPLIFIER

The servo driver has two modes of operation, linear and retract. The retract mode is activated by a power supply failure or when the control signal $\overline{RESET}$ is LOW. Otherwise the driver operates in linear mode. During linear operation, the microcontroller acquires servo burst amplitudes and analyzes them to establish a position error signal. This signal travels through an 8-bit D/A converter and is applied to an amplifier whose three connections, ERRM, ERREF and ERR, are available externally. External RC components may be used to establish the gain and bandwidth of this amplifier. Additional analog input via SWIN may be provided to this amplifier by setting the SW ON bit in the SERVO CONTROL register.

FUNCTIONAL DESCRIPTION (continued)

H-BRIDGE MOSFET PREDRIVER

The error signal ERR generated from the position error amplifier drives two precision differential amplifiers, each with a gain of 15. The differential amplifier outputs, AOUTA, AOUTB, AOUTC and AOUTD drive an external MOSFET bridge powered by VBRIDGE. Feedback from the MOSFET drain terminals via sense inputs SE1 and SE3 allow the differential amplifier gains to be established precisely. The voice coil actuator and a current sense resistor are connected in series between SE1 and SE3. Included in the output control circuitry is a crossover protection function which ensures class B operation by permitting only one MOSFET in each leg of the bridge to be in conduction. The crossover circuit can be adjusted for different MOSFET threshold voltages with a resistor connected to VX. The crossover circuitry can be commanded by the µP to shut down the MOSFET drivers and thus remove current to the external bridge.

MOTOR CURRENT SENSE

Motor current is sensed by a small resistor placed in series with the actuator. The voltage drop across the resistor is level-shifted and amplified by a differential amplifier with a gain of 4. The resulting signal, SOUT, is proportional to actuator current. This signal is externally fed back to the position error amplifier so that the error signal ERR represents the difference between the desired and actual actuator currents.

VOLTAGE FAULT DETECTION AND SERVO HEAD RETRACT

A voltage fault detector which can monitor up to two voltage supplies is included to prevent the actuator from responding to a false error signal during a power failure. Retract mode is started when a power supply failure is sensed by the PSB or PSV comparators or when $\overline{\text{RESET}}$ is pulled LOW externally. During retract, a constant voltage is applied across the actuator in order to cause a constant velocity head retraction. This is accomplished by applying the voltage stored on VBYP to AOUTD and by driving AOUTR with an amplifier that monitors SE1. The amplifier is powered by VBEMF. During retract, VRETRACT is biased by an internal voltage reference and determines the retract voltage. At other times, power is saved by disconnecting VRETRACT from the voltage reference and letting it be pulled to VBEMF by a high value resistor. External components (a diode, for instance) can be connected between VRETRACT and ground to modify the retract voltage.

An open-drain output, $\overline{\text{SYSRST}}$, which is active LOW while the servo driver is in retract mode, is provided for spindle motor braking. An external RC delay may be used to defer braking until the head is retracted. The amount of $\overline{\text{SYSRST}}$ delay is determined by the external capacitor which is connected to the pin, RCRST.

SPINDLE MOTOR SPEED CONTROL

A functional block diagram for the spindle motor control is shown in Figure 1. In conjunction with several external components, the spindle motor speed control provides the starting, accelerating, and precise rotational speed regulation functions. The circuit will control 4, 8, or 12 pole brushless DC motors without the need for Hall sensors. It will operate in either bipolar or unipolar drive mode. Control, configuration, and status monitoring are handled by the µP. The complete speed control loop is contained in the circuit and the µP is only required during start and to monitor status.

SPINDLE MOTOR START-UP

Motor starting is accomplished with the µP utilizing various features contained in the motor speed control circuitry. The µP can write to the commutation counter and set it to a predetermined value with STATE0, STATE1, STATE2 bits. The counter can then be incremented with the ADVANCE bit which also excludes internal commutations when set HIGH. Bits COMMU, PERCHK 2, 3, 4, 5 provide feedback to the µP on motor activity. The µP can enable the drivers with MENABLE and UNIPOLAR bits as required, as well as cause a "soft" brake with $\overline{\text{UPBRK}}$.

Under µP control, initial open-loop commutation sequence is provided to the commutation logic which thereby advances and accelerates the spindle motor. The start-up process settles the motor initially by selecting the bits STATE0, STATE1, STATE2 in the SPINDLE CONTROL register to energize a proper motor winding. Motor current is enabled by setting the MEANABLE bit in the SPINDLE CONTROL register. The commutation state is advanced by providing ADVANCE pulses in the SPINDLE CONTROL register. The period of the ADVANCE pulses will be based upon the motor and load characteristics and decreased

gradually during the acceleration of the motor. The µP may look at the COMMU bit in the SPINDLE STATUS register for feedback indicating whether the motor has achieved a sufficient speed. Once the motor has achieved a sufficient speed, the µP will cease generating ADVANCE pulses and motor starting is thus completed.

SPINDLE MOTOR SPEED REGULATION

Motor speed regulation is accomplished with mixed analog and digital techniques, converting a motor speed error derived from a reference clock and a period counter into a voltage. The voltage translates into a motor current across the current sense resistor regulating the motor speed. The speed regulation loop consists of a period counter, proportional and integral channels, two 6-bit D/A converters and a linear transconductance amplifier.

In operation, the motor speed error is determined by measuring the period of each revolution with a 500 kHz clock signal. Period resolution is therefore 2 microseconds with the desired period being 8333 counts (16.66 ms, or 3600.144 RPM) (4631), and 5555 counts (11.110 ms, 5400.54 RPM) (4632). Motor rotor position is determined by monitoring the coil voltage of the winding that is not presently being driven by the drivers. The back-emf at the coil in conjunction with the state of the output drivers indicates rotor position. The back-emf is compared to a reference at CTSENSE and initiates "commutation events" when the appropriate comparison is made. The commutation is the sequential switching of the drive current to the motor windings. Since the back-emf comparison event occurs prior to the time when optimum commutation should occur, it is thus required to delay actual commutation by a predetermined time after the comparison. The commutation delay is provided by a non-retriggerable one-shot circuit wherein the time delay is a function of external RC timing components connected at EXTRC. Because commutation of the motor windings typically results in large transient voltages which could falsely indicate "commutation events," the one-shot circuit also provides a "noise filter" function which holds off retriggering further and blanks the back-emf comparison events for a period of time (approximately one half the commutation delay) after commutation. The commutation states are defined in the SPINDLE CONTROL register.

The period counter is loaded with a count of 8333 (4631), 5555 (4632) initially, and period measurement results in residual counts (ideally zero) in the period counter as it counts down during the index-to-index time interval. The residual count is fed to the proportional D/A converter (5 bit plus sign) whose output is provided at PROP. No period error will output half of VBIAS at PROP, too short a period will output a value less than half of VBIAS, and too long a period will output a value greater than half of VBIAS depending on the amount of error.

When the residual count is within ± 15 counts of zero, the motor is indicated as "in lock." The lower eight bits of the period counter are fed to an accumulator which adds the present period residue to the previous accumulation thus accomplishing an integrating effect to force the speed error to zero over time. The upper six bits of the accumulator are fed to the integral DAC whose output is INTEGRAL. Gross period errors will cause PROP and INTEGRAL to saturate at the appropriate extreme to achieve the maximum corrective control voltage.

The outputs at PROP and INTERGRAL are connected to VIN with an external resistor network. The resistor values should be selected to set the required loop response based upon motor requirements. The input VIN is the non-inverting input of the linear transconductance amplifier which uses the lower driver transistor that is presently active per the commutation state. An external resistor is used to sense the current flowing through the drive transistor drain (and hence the motor coil current). The voltage across the sense resistor, the difference between SENSE and SENSEREF, is amplified by a programmable gain stage and fed to the inverting input of the transconductance amplifier. The gain of the programmable amplifier is determined by TGAIN0 and TGAIN1 bits.

Motor speed control includes a speed range check circuit, which provides in the SPINDLE STATUS register a LOCK status bit, when the motor is at the target speed within ±0.18% (4631), -27%(4632), along with OVER status bit, when the motor is over or under the target speed. The LOCK and OVER status bits are available to the µP for diagnostics and spindle fault conditions.

Additional low-speed period measurement data is available to the µP as the PERCHK2,3,4,5 bits in the SPINDLE STATUS register.

FUNCTIONAL DESCRIPTION (continued)

MOTOR PEAK CURRENT LIMITING

When the period error exceeds 256 counts too slow, the voltage at VLIM is selected as the control voltage in lieu of VIN. VLIM is to be used to set the motor peak current during start-up and acceleration.

MOTOR BRAKING

Fault conditions on power supplies and internal voltage reference generator will trigger an internal retract condition. The internal retract condition will cause all predriver outputs to the states which will turn the driver transistors off, allowing the motor to coast. $\overline{\text{BRAKE}}$ typically has a capacitor to ground attached and is connected to pin $\overline{\text{SYSRST}}$ via a resistor. $\overline{\text{SYSRST}}$ goes LOW in the retract condition, and thus $\overline{\text{BRAKE}}$ will go LOW after the RC delay. When $\overline{\text{BRAKE}}$ goes LOW, all lower drivers are activated to achieve dynamic braking of the motor. The circuitry for these operations is powered by the back-emf of the spindle motor and will operate without either 5 or 12 volt supply.

Dynamic braking can also be activated under µP control by setting $\overline{\text{UPBRK}}$ to LOW in the SPINDLE CONTROL register. During dynamic braking, the control loop is opened.

Two other motor speed control functions related to other circuit functions in the SSI 32H4631/4632 are SLEEP mode and internal bias current. Two modes of SLEEP are provided for the SSI 32H4631/4632, but the effect on the motor speed control is the same for both modes, i.e., all analog circuitry is de-biased, the clock is disabled, the upper driver outputs become logic HIGH (to turn off all upper drivers including the center tap if used), and the lower driver outputs become logic HIGH. The internal bias currents for analog functions are set by an external resistor connected between IBR and ground. A 22.6 KΩ, ±1% resistor should be used for proper operations.

EXTERNAL INDEX APPLICATION

Normal operation is performed with an internal index signal derived from the commutation counter (scaled via the MODE0 and MODE1 bits based upon the number of motor poles). The period of the index signals is measured and controlled by the circuit to result in a rotational rate of 3600 (4631) 5400 (4632) RPM. Within the range of 3593.5 to 3606.5 RPM for the SSI 32H4631 and 5385.9 to 5415.1 RPM for the SSI 32H4632, the spindle will be "in lock." After the motor is started and accelerated to speed (LOCK bit HIGH), an external index signal may be selected. Applying external index pulses at a rate within the lock range and setting INDEX SEL bit to HIGH will start the following sequence:

The circuit will complete the period measurement of the latest internal index period and then begin to measure the time between the last internal index and the next external index pulse. This will most likely be shorter than the nominal assuming the two events are asynchronous. If the period measured is not within 3% (4631), 4.5% (4632) of the expected value (16.667 (4631), 11.11 (4632) milliseconds), the proportional and integral D/A converters will not be updated with a new correction value but will continue to output the previous value. The LOCK bit will be set to LOW indicating "out of lock." The next period measured will be between the first and second external index pulses and will presumably be within the lock range so that LOCK will be set to HIGH. If the period is within 3% (4631), 4.5% (4632) of the desired value, the proportional and integral D/A converters will be updated. Similarly, during operation with external index, a missing index pulse would look like a gross speed error and no update on proportional and integral D/A converters will take place. The µP must perform the corrective actions in such cases, by examining LOCK bit, the PERCHK2,3,4,5 bits, and the source of the (missing) index pulses. A single missing index should require no action other than checking that LOCK returns to HIGH (in lock) in the next interval.

DATA ACQUISITION AND MICROPROCESSOR BUS INTERFACE

Figure 1 shows data acquisition circuits along with the microprocessor bus interface. To facilitate microprocessor-based servo applications, the SSI 32H4631/4632 contains a high-speed 8-bit A/D converter at a conversion rate up to 250 kHz, an 8-bit D/A converter, and Motel bus interface compatible with commonly used 12 MHz 8051 and 8 MHz 68HC11. The A/D converter can be multiplexed to sixteen different analog inputs by programming the ADC_SEL0, ADC_SEL1, ADC_SEL2 and ADC_SEL3 bits in the ADC ADDRESS register by the µP. The analog inputs can be scaled by a gain of 4 by setting the X4 bit HIGH. The output of the gain stage is available externally at MUXOUT for diagnostics. The A/D converter runs synchronously with the internal 500 kHz clock which is used for various circuits on the SSI 32H4631/4632. Therefore, there

would be a maximum of 2 microseconds of latency between a conversion request and the actual start of the conversion. Conversion is started by reading the A/D output register. The output is coded in 2's complement. Note that different voltage references corresponding to one half of the A/D full scale are used for different analog inputs as defined in the ADC ADDRESS register.

Similarly, the D/A converter runs synchronously with the internal 500 kHz clock and conversion is started by writing to the D/A input register. The output at ERRDAC is referenced to ERREF and is held constant between conversions.

The "Motel" interface to both Motorola and Intel µP's is provided for a direct connection to the SSI 32H4631/4632. Three bus control signals are interpreted differently based upon the type of µP being used. The pin BUSMODE should be tied to HIGH for an Intel bus interface. The table below illustrates how both µPs connect to the SSI 32H4631/4632. The $\overline{ASE}$ pin gates the AL/ASE input and can be used to shut off the ALE/AS to minimize noise on chip when the µP interface is not active. The $\overline{CS}$ pin performs a similar function on the rest of the µP bus inputs. The timing diagrams for Intel and Motorola µP interface are shown in Figures 5 and 6, respectively.

Intel	Motorola	32H4631/ 32H4632
ALE	AS	ALE
$\overline{RD}$	DS;E; or Clock Phase 2	$\overline{RD}$
$\overline{WR}$	R/$\overline{W}$	$\overline{WR}$

REGISTER DESCRIPTIONS

The SSI 32H4631/4632 contains ten 8-bit internal registers which provide control, option select and status monitoring. The registers are addressed with a 4-bit register address which is latched from inputs at AD0, AD1, AD2, and AD3 on the falling edge of ALE. The registers from 0 to 5 are read/write memory, the registers from 6 to 9 are write only. The registers are summarized in Table 1.

TABLE 1: SSI 32H4631/4632 Internal Registers

ADDRESS	TYPE	REGISTER NAME
0	R/W	Interrupt Control/Status
1	R/W	Spindle Control/Status
2	R/W	Servo Control/Status
3	R/W	ADC Address/Data
4	R/W	Track Count LSB
5	R/W	Track Count MSB & Hybrid Servo Control
6	W	Error DAC Data
7	W	Embedded Servo Gain Control
8	W	Transconductance, Prescaler and Mode Control
9	W	Embedded Servo Timing Window Control

INTERRUPT CONTROL/STATUS REGISTER

Address: 0 Access: Read/Write Reset: 00
Register contents when Written to enable or disable interrupt events:

BIT	NAME	DESCRIPTION
0	COMMU INT	When set HIGH, interrupt is enabled on a state change of the back-emf commutation clock COMMU.
1	LOCK INT	When set HIGH, interrupt is enabled on a state change of the spindle speed lock.
2	BURST INT	When set HIGH, interrupt is enabled on the embedded servo position bursts ready.
3	TRKCS INT	When set HIGH, interrupt is enabled on each track crossing.
4	COUNT INT	When set HIGH, interrupt is enabled on the terminal count (000_H) of the track crossing counter.
5,6	-	Undefined.
7	MST INT	When set HIGH, the microprocessor signal $\overline{INT}$ is enabled.

Register contents when Read

BIT	NAME	DESCRIPTION
0	COMMU INT	Active high indicates a state change of the back-emf commutation clock COMMU.
1	LOCK INT	Active high indicates a state change of the spindle speed lock.
2	BURST INT	Active high indicates that the embedded servo position bursts are ready.
3	TRKCS INT	TRKCS INT is asserted when NQ or $N\overline{Q}$ changes state, i.e., on each track crossing.
4	COUNT INT	COUNT INT is asserted when the terminal count (000_H) of the track crossing counter is reached.
5,6	-	Undefined.
7	MST INT	Active high indicates that one or more interrupts are pending.

Each interrupt event status is reset when the µP reads the corresponding status register. Specifically, interrupt events COMMU INT and LOCK INT are reset whenever the SPINDLE STATUS register (ADDRESS=1) is read. Interrupt events TRKCS INT, COUNT INT and BURST INT are reset whenever the SERVO STATUS register (ADDRESS=2) is read. All interrupt events may be read as interrupt status regardless of their corresponding interrupt mask settings. The interrupt control register determines which event will actually cause a latched assertion of the µP signal $\overline{INT}$. Note that the MST INT is a master enable which disables all interrupt events from asserting $\overline{INT}$ when active low. Also, when read, MST INT indicates if any mask enabled interrupt events are still pending for service and reflects the internal state of the µP signal $\overline{INT}$.

SPINDLE CONTROL/STATUS REGISTER

Address: 1 Access: Read/Write Reset: 00
Register contents when Written:

BIT	NAME	DESCRIPTION
0	$\overline{\text{UPBRK}}$	When set LOW, dynamic braking will be initiated where upper drivers are disabled and lower drivers are activated.
1	UNIPOLAR	This bit is set HIGH when unipolar motor is used. For unipolar motors, all upper drivers are disabled and OUTCT is activated.
2	INDEX SEL	When set HIGH, the input signal at EXTINDX, one pulse per revolution, is selected as the spindle speed indicator. Otherwise, the internal revolution clock developed from the back-emf sensing circuit is selected.
3	MENABLE	Driver Enable Control. When set LOW, both upper and lower drivers are turned off to deny power to the motor. This overrides all other output conditions. When set HIGH, drive outputs are activated per the state of the commutation state counter.

Register contents when Written:

BIT	NAME	DESCRIPTION
4	ADVANCE	Each LOW-TO-HIGH transition advances the edge-trigged commutation state counter by one. When set HIGH, the internal clock (derived from the back-emf events) to the commutation state counter is inhibited. When set LOW, normal operation is resumed.
5 6 7	STAT0 STAT1 STAT2	Preset Commutation State. During start-up, the commutation state counter will be preset to the state decoded by these 3 bits per table 2:

TABLE 2:

STAT2	STAT1	STAT0	OUTA	OUTB	OUTC	OUTUPA	OUTUPB	OUTUPC
0	0	0	OFF	ON	OFF	ON	OFF	OFF
0	0	1	OFF	OFF	ON	ON	OFF	OFF
0	1	0	OFF	OFF	ON	OFF	ON	OFF
0	1	1	ON	OFF	OFF	OFF	ON	OFF
1	0	0	ON	OFF	OFF	OFF	OFF	ON
1	0	1	OFF	ON	OFF	OFF	OFF	ON
1	1	0	Normal Operation					
1	1	1	Normal Operation					

SPINDLE CONTROL/STATUS REGISTER (continued)

Register contents when Read:

BIT	NAME	DESCRIPTION
0	LOCK	Active high indicates that the spindle motor is within ±15 counts of the nominal value (8333 (4631), 5555 (4632) counts with the counter clocked at 500 kHz) or ±0.18% (4631), 0.27% (4632). The corresponding interrupt event LOCK INT will be reset whenever this register is read by the µP.
1	OVER	Active high indicates that the spindle speed is faster than the nominal value; active low indicates that the spindle speed is slower than the nominal value.
2	COMMU	Back-emf commutation clock divided by 2. Each state change of COMMU indicates that the commutation state counter has advanced by one. The corresponding interrupt event COMMU INT will be reset whenever this register is read by the µP.
3 4 5 6	PERCHK5 PERCHK4 PERCHK3 PERCHK2	Spindle Speed Check Bits. These bits are used to estimate the spindle speed if it is slower than the nominal value.
7	Undefined	

P2	P3	P4	P5	SPEED,rps (4631)	SPEED,rps (4632)
0	0	0	0	SPEED ≥48	SPEED ≥65
1	0	0	0	40≤ SPEED ≥48	52≤ SPEED ≥65
1	1	0	0	30≤ SPEED ≥40	36≤ SPEED ≥52
1	1	1	0	20≤ SPEED ≥30	23≤ SPEED ≥36
1	1	1	1	SPEED ≥20	SPEED ≥23

SERVO CONTROL/STATUS REGISTER

Address: 2 Access: Read/Write Reset: 00
Register contents when Written:

BIT	NAME	DESCRIPTION
0	HENABLE	H-bridge Driver Enable. When set HIGH, H-bridge MOSFET drivers are enabled.
1	SW ON	When set HIGH, the analog switch between the ERRM and SWIN pins is turned on.
2	-	Undefined
3	TIMING	Timing Controller Disable. When set HIGH, the timing signals required to sample/hold embedded servo position bursts are derived from an external timing source via SAMPLEX and ACQX. Otherwise, the internal timing controller is used.
4	DIBURST	When HIGH, only two servo bursts, BURST1 and BURST2 are sampled. Otherwise, four servo burst amplitudes are sampled.
5	LEAD	Write Gate Guard Lead Enable. When set HIGH, the write gate guard is enabled one burst period prior to the sampling of the first position burst field. Otherwise, the write gate guard is enabled essentially at the same time as the sampling of the first position burst field.
6 7	TIM0 TIM1	Burst Field Length Select. These two bits define the time duration of each embedded servo position burst field per table below:

TIM1	TIM0	Burst Duration, μsec
0	0	5
0	1	6
1	0	8
1	1	10

Register contents when Read:

0	-	Undefined
1	-	Undefined
2	BURST	Active HIGH indicates that the embedded servo position bursts are ready.
3	TRKCS	Active HIGH indicates a track crossing, i.e., NQ or $N\overline{Q}$ changes state.
4	COUNT	Active HIGH indicates that the terminal count (000_H) of the track crossing counter is reached.
5	-	Undefined
6	NQ	Active HIGH when N>Q and reset otherwise.
7	$N\overline{Q}$	Active HIGH when N>-Q and reset otherwise.

The corresponding interrupt events TRKCS INT, COUNT INT and BURST INT will be reset when this register is read by the μP. Also, the TRKCS, COUNT and BURST bits in this register are reset after being read.

ADC ADDRESS/DATA REGISTER

Address: 3 Access: Read/Write Reset: Undefined

Description: When Written, the least significant 4 bits of the register define the analog input to the 8-bit A/D converter. After conversion, the 8-bit digital word of the analog input is stored into the register.

Register contents when Written:

BIT	NAME	DESCRIPTION
0 1 2 3	ADC_SEL0 ADC_SEL1 ADC_SEL2 ADC_SEC3	A/D Converter Input Select. These 4 bits define the analog input to the A/D converter per table below:
4	X4	X4 Enable. When set HIGH, the analog input to the A/D converter will be multiplied by 4 before converted into a digital value.
5,6,7	-	Undefined

BIT3	BIT2	BIT1	BIT0	ADC INPUT	ADC Vref
0	0	0	0	BURST1	VREF
0	0	0	1	BURST2	VREF
0	0	1	0	BURST3	VREF
0	0	1	1	BURST4	VREF
0	1	0	0	PES1	VREF
0	1	0	1	PES2	VREF
0	1	1	0	PES0	VREF
0	1	1	1	N	NQREF
1	0	0	0	Q	NQREF
1	0	0	1	ERR	VREF
1	0	1	0	SOUT	VREF
1	0	1	1	SENSE	SENSEREF
1	1	0	0	ADCIN	VREF
1	1	0	1	VREF	VREF
1	1	1	0	SUM1	VREF
1	1	1	1	SUM2	VREF

Register contents when Read:

BIT	NAME	DESCRIPTION
0..7	ADC0..7	Digital output of the A/D converter in 2's complement format. ADC7 corresponds to the sign bit.

TRACK COUNT AND HYBRID SERVO CONTROL REGISTER

Address: 4 and 5 Access: Read/Write Reset: 00

Description: In a hybrid servo application, the dedicated servo channel is supported by a 12-bit track crossing counter with a 4-bit hybrid control register. The counter is preset by the µP and counts down by one whenever the head crosses a track boundary. The LSB 8 bits of the counter are defined at register 4 as follows:

BIT	NAME	DESCRIPTION
0..7	TRACK0..7	LSB of the track crossing counter 0..7. When written, these bits preset the track counter. When read, they reflect the counter state.

The MSB 4 bits of the counter along with the hybrid control bits are latched when the LSB 8 bits are read. The hybrid control bits, QUAD0, QUAD1, SELECT Q and CALIB are "write only." They are defined at register 5 as follows:

BIT	NAME	DESCRIPTION
0..3	TRACK8..11	MSB of track crossing counter 8..11. When written, these bits preset the track counter. When read, they reflect the counter state.
4 5	QUAD0 QUAD1	Quadrant Select. These 2 bits select the quadrant per table below: **QUAD1 QUAD0 Quadrant Selected** 0 0 -Q 0 1 N 1 0 -N 1 1 Q
6	SELECT Q	Quadrant Select Enable. Select quadrant with QUAD0 and QUAD1 when set HIGH.
7	CALIB	Calibration Enable. When set HIGH, the device is in the calibration mode in which analog inputs N and Q are tied to a DC reference level, NQREF; the analog input SERIN is tied to the DC reference level, SEREF.

ERROR DAC DATA REGISTER

Address: 6 Access: Write Reset: 00

BIT	NAME	DESCRIPTION
0..7	DAC0..7	Digital input to the D/A converter in 2's complement format. DAC7 corresponds to the sign bit.

EMBEDDED SERVO GAIN CONTROL REGISTER

Address: 7 Access: Write Reset: 00

<table>
<tr><th>BIT</th><th>NAME</th><th>DESCRIPTION</th></tr>
<tr><td>1</td><td>GAIN1</td><td>These two bits define the gain setting for the embedded servo differential amplifier per table below:
GAIN1 GAIN0 Gain, dB
0 0 -6
0 1 -3
1 0 0
1 1 3</td></tr>
<tr><td>2
3
4
5</td><td>GAIN2
GAIN3
GAIN4
GAIN5</td><td>Embedded Servo Burst Amplitude Gain Select.
These four bits define the gain setting for the sample/hold amplifier per table below:
GAIN5 GAIN4 GAIN3 GAIN2 Gain, dB
0 0 0 0 0.0
0 0 0 1 0.2
0 0 1 0 0.4
0 0 1 1 0.6
0 1 0 0 0.8
0 1 0 1 1.0
0 1 1 0 1.2
0 1 1 1 1.4
1 0 0 0 1.6
1 0 0 1 1.8
1 0 1 0 2.0
1 0 1 1 2.2
1 1 0 0 2.4
1 1 0 1 2.6
1 1 1 0 2.8
1 1 1 1 3.0</td></tr>
<tr><td>6</td><td>SYNC SEL</td><td>Sync Input Select. When set HIGH, the frame rate to sample dedicated quadrature position signals N and Q is derived internally from SYSCLK. Otherwise, it is provided externally from the servo demodulator through SYNC and VCO inputs.</td></tr>
<tr><td>7</td><td>TCHE</td><td>Track Clock Hysteresis Enable. When set HIGH, an internal timing hysteresis is added for deriving the TRKCK output.</td></tr>
</table>

6

TRANSCONDUCTANCE, PRESCALER & MODE CONTROL REGISTER

Address: 8 Access: Write Reset: Bit 4 and 5 only

Bit	Name	Description
0	TEST	Test Mode Enable. When set HIGH, the device is in the test mode where the testing time for the spindle motor speed control function is shortened.
1	SLEEP	Power-down Mode Enable. When set HIGH, the device is in the power-down mode where all analog circuitry is de-biased, the clock is disabled and the output drivers are pulled to logical HIGH.
2 3	TGAIN0 TGAIN1	Transconductance Select. The transconductance gain of spindle motor lower drivers is defined per table below: **TGAIN1 TGAIN0 Gain** 0 0 2 0 1 4 1 0 8 1 1 16
4 5	SCALE0 SCALE1	SYSCLK Prescaler. To accommodate different system clocks which may be used, the prescaler selects a proper divider to generate a fixed clock at 500 kHz per table below: **SCALE1 SCALE0 SYSCLK(MHz) Divider** 0 0 10 20 0 1 8 16 1 0 6 12 1 1 4 8
6 7	MODE0 MODE1	Spindle Mode Control. These two bits define the number of motor poles per table below: **MODE1 MODE0 POLES COMMU/INDEX** 0 0 4 12 0 1 8 24 1 0 12 36 1 1 N/A N/A

EMBEDDED SERVO TIMING WINDOW CONTROL REGISTER

Address: 9 Access: Write Reset: 00

Description: The embedded servo position burst timing controller generates four timing windows. The sample control register matches these timing windows with four SAMPLE/HOLD circuits. The µP writes into the register a control pattern which will provide a necessary sampling to compare the required bursts in a proper polarity and sequence. In this manner, the µP can mix and commutate the bursts so that the position error signal is always in the same direction.

BIT	NAME	DESCRIPTION
0,1	WD SH1	Define timing window for SAMPLE/HOLD 1. Bit 0 is LSB.
2,3	WD SH2	Define timing window for SAMPLE/HOLD 2. Bit 2 is LSB.
4,5	WD SH3	Define timing window for SAMPLE/HOLD 3. Bit 4 is LSB.
6,7	WD SH4	Define timing window for SAMPLE/HOLD 4. Bit 6 is LSB.

The timing window is selected per table below:

MSB	LSB	S/H Timing Window
0	0	Timing window 1
0	1	Timing window 2
1	0	Timing window 3
1	1	Timing window 4

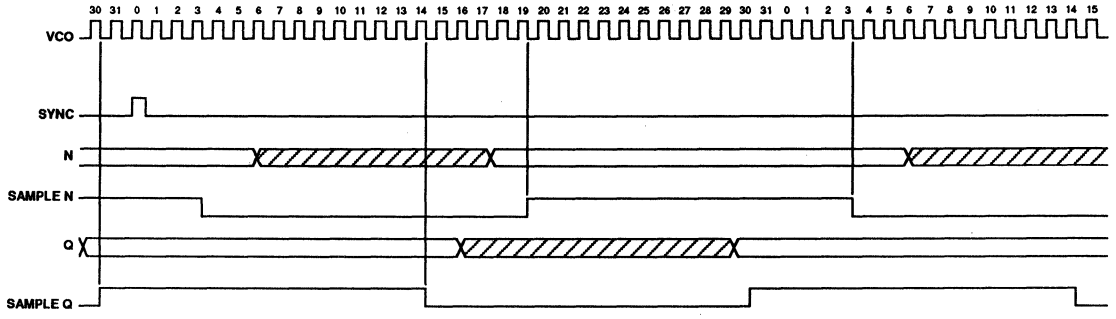

FIGURE 2: Dedicated Servo Timing Diagram

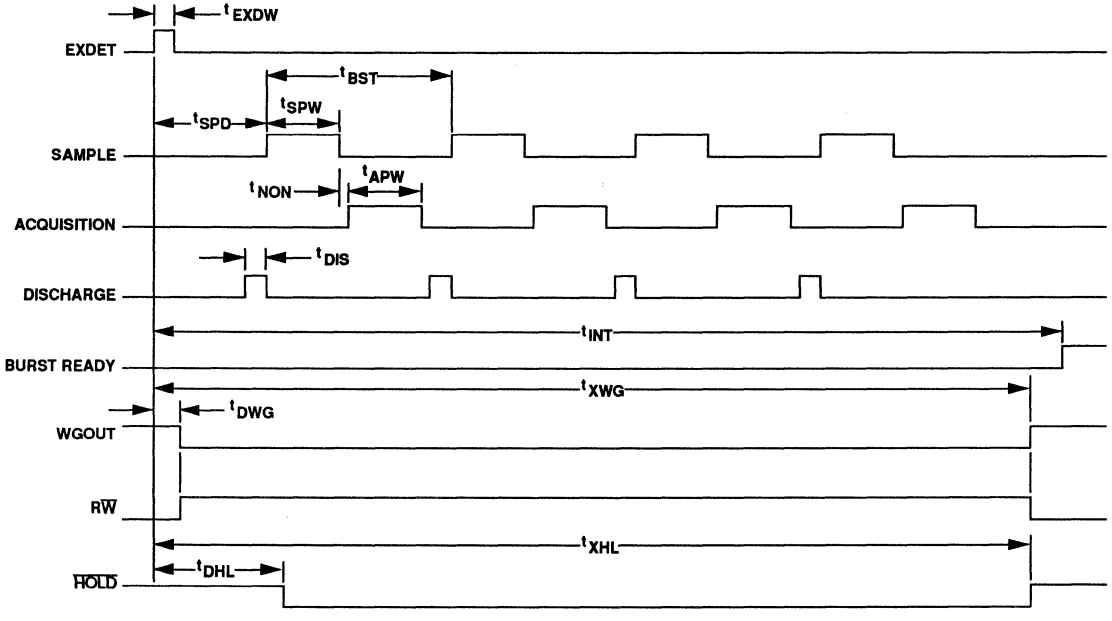

FIGURE 3: Embedded Servo Timing Diagram with Internal Timing Source

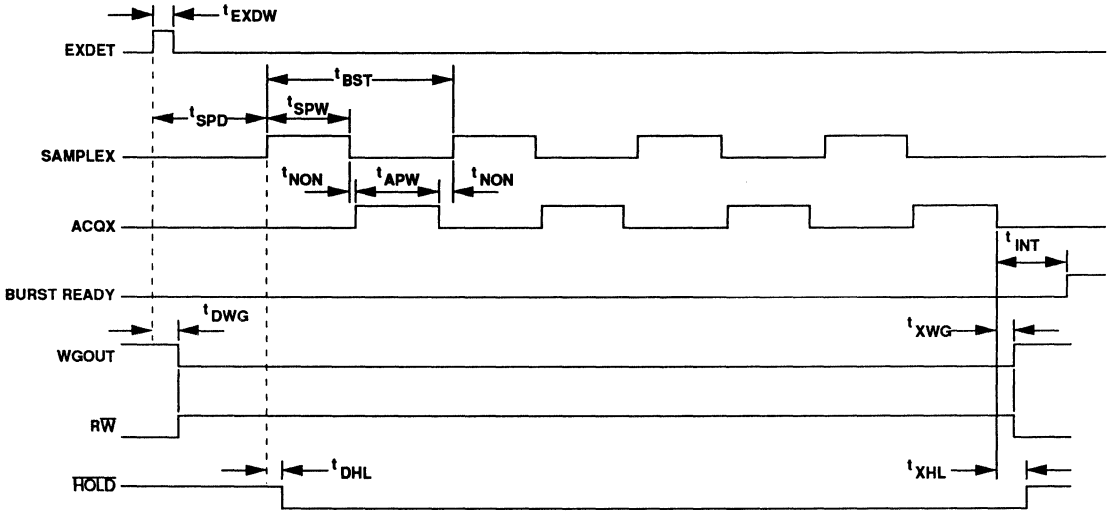

FIGURE 4: Embedded Servo Timing Diagram with External Timing Source

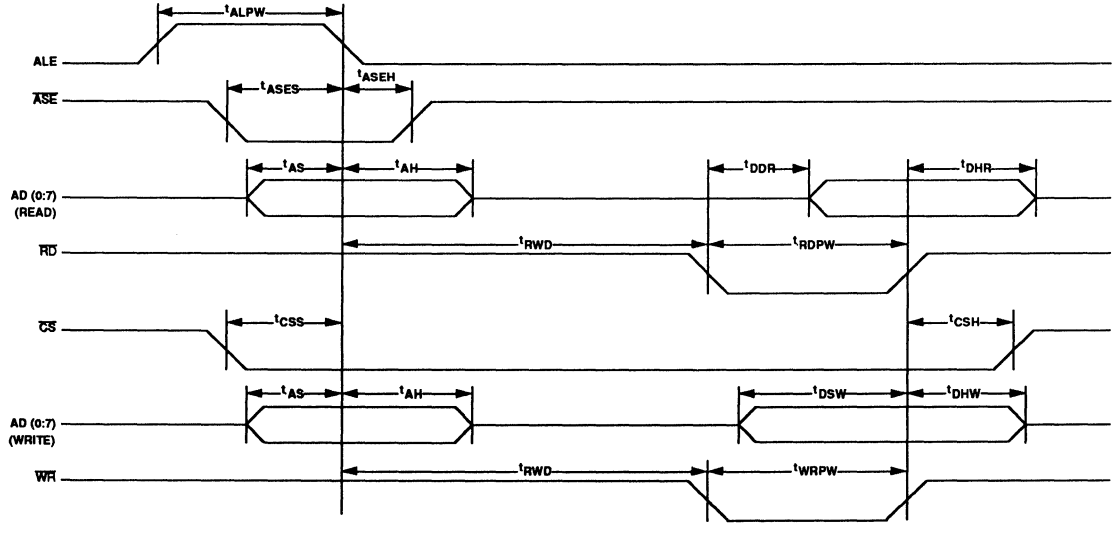

FIGURE 5: Intel Microprocessor Bus Interface Timing Diagram

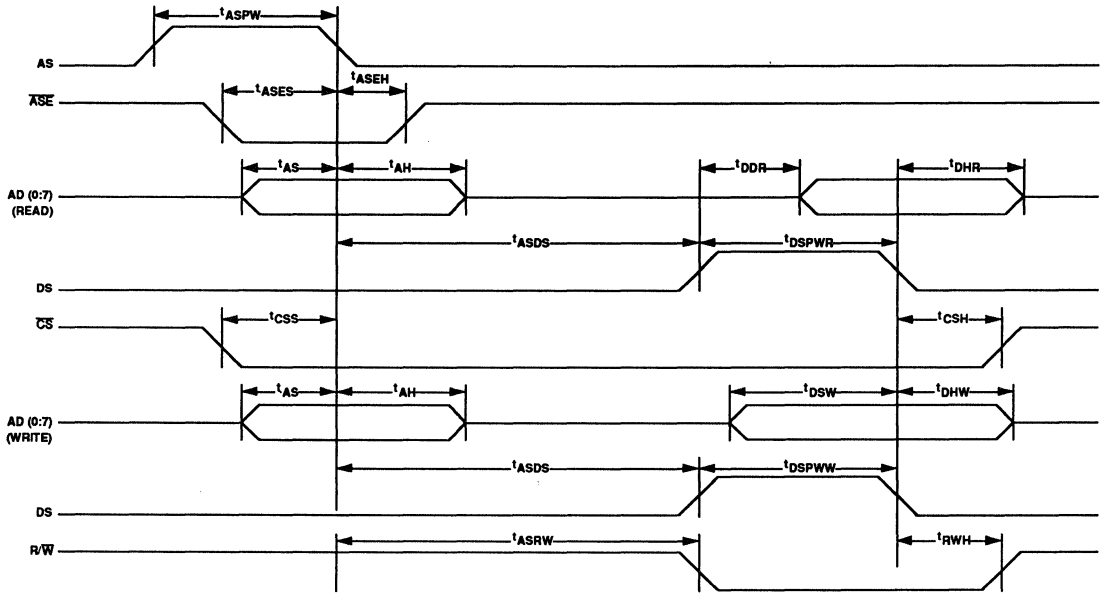

FIGURE 6: Motorola Microprocessor Bus Interface Timing Diagram

PIN DESCRIPTION

This section describes the names of the pins, their symbols, their functions and their active states. The pins are grouped together into function for clarity.

POWER SUPPLIES

NAME	TYPE	DESCRIPTION
VPA, B, C, G	-	Analog +5V supplies. They must be shorted externally.
VPD	-	Digital +5V supply. It must be shorted to analog +5V supplies externally.
VNA, B, C, G	-	Analog grounds. They must be shorted externally.
VND, VND2	-	Digital grounds. They must be shorted to analog grounds externally.

SERVO HEAD POSITION PROCESSOR

N	I	Normal Input - Analog position signal from a dedicated servo demodulator. This input along with quadrature input is used to extract the position information from a dedicated servo surface.
Q	I	Quadrature Input - Analog position signal from a dedicated servo demodulator.
NQREF	I	Dedicated Position Error Reference - DC reference voltage for both normal and quadrature analog inputs.
SYNC	I	Sync Input - A clock signal generated from a dedicated servo demodulator. The falling edge of this clock causes the analog signals N and Q to be sampled.
VCO	I	VCO Input - A clock signal generated from a dedicated servo demodulator. The VCO should be synchronous with N and Q inputs.
TRKCK	O	Track Crossing Clock - This digital output drives external hardware track counter and is compatible with the counter function available in the Intel 8051 family of microcontrollers. It is normally LOW and pulses HIGH once per track crossing.
$\overline{\text{TCNT}}$	O	Terminal Count - The terminal count output is normally HIGH and goes LOW when the 12-bit counter reaches zero.
PES0	O	Position Error Output - Test point for the analog output of the position processor. This signal is proportional to the radial displacement of the head from the center of the current track, based upon the values of bits QUAD0, QUAD1 and SELECT Q.
SERIN	I	Embedded Servo Input - Full-wave rectified analog signal generated from a read data channel. This input is to extract the position information from embedded servo bursts.
SEREF	I	Embedded Servo Burst Reference - A DC reference level for the full-wave rectified analog signal SERIN.
SAMPLEX	I	Servo Burst Sample - This TTL compatible input, when HIGH, activates the peak detector. This input is used only when the TIMING bit in the SERVO CONTROL register is set HIGH for an external timing source.

SERVO HEAD POSITION PROCESSOR (continued)

NAME	TYPE	DESCRIPTION
ACQX	I	Servo Burst Acquisition - This TTL compatible input, when HIGH, activates the transfer of the voltage captured by the peak detector onto holding capacitors. This input is used only when the TIMING bit in the SERVO CONTROL register is set HIGH for an external timing source.
PES1 PES2	O	Position Error Signal - Test point for differential signals which are defined as: PES1 = BURST1-BURST2 PES2 = BURST3-BURST4
SUM1 SUM2	O	Position Sum Signal - Test point for summed signals which are defined as: SUM1 = BURST1+BURST2 SUM2 = BURST3+BURST4

HEAD POSITIONER MOSFET DRIVER AND VOLTAGE FAULT DETECTION

ERRM	I	Actuator Inverting Input - Inverting input to the position error amplifier of the MOSFET predriver.
SWIN	I	This input is shorted to ERRM when the bit SW ON is set HIGH. SWIN floats otherwise.
ERR	O	Acceleration Error - Position error amplifier output. This signal is amplified by the MOSFET drivers and applied to the actuator through an external MOSFET H-bridge as follows: SE3-SE1 = 30 (ERR-VREF)
AOUTA AOUTC	O	PFET Driver - Drive signals for P channel MOSFETs connected between VBRIDGE and the voice coil actuator. Crossover protection circuitry ensures that the P and N channel devices driven by OUTC and OUTD are never enabled simultaneously.
AOUTB AOUTD	O	NFET Driver - Drive signals for N channel MOSFETs connected between the current sense resistor and the voice coil actuator.
VBRIDGE	I	Bridge Voltage Supply - Pin for connection to the voltage supply provided to external power transistors.
VRETRACT	I	Retract Voltage - In head retract mode this voltage is applied across the actuator to force the heads to move at a constant speed.
AOUTR	O	Head Retract Amplifier Output - Voltage output to drive an external head retract circuit.
SE1 SE3	I	Motor Voltage Sense Input - These inputs provide feedback to the internal MOSFET drive amplifier.
SE2	I	Motor Current Sense Input - Non-inverting input to the current sense differential amplifier. It should be connected to an external current sense resistor. The inverting input of the differential amplifier is SE1.
SOUT	O	Motor Current Sense Output - This output provides a voltage proportional to the voltage drop across the external current sense resistor as follows: SOUT-ERREF = 4 (SE2-SE1)

HEAD POSITIONER MOSFET DRIVER AND VOLTAGE FAULT DETECTION (continued)

NAME	TYPE	DESCRIPTION
VX	O	Crossover Protection Voltage - The current source output at VX is converted to a voltage with an external resistor. The value of the resistor should be adjusted so that VX is less than the specified minimum threshold voltage of the MOSFET bridge.
VBYP	I	Bypass Voltage Supply - The VBRIDGE voltage is stored on this node for use during retract.
PSB PSV	I	Fault Voltage Comparator Inputs - Voltage inputs for the low voltage comparators. These two inputs should be connected to separate external resistor dividers. Each resistor divider divides its corresponding supply voltage to a proper value which is comparable with the internal voltage reference at 2.25 volts.
VREF	O	Internal Voltage Reference - A voltage reference at 2.25 volts is generated internally for the DC reference level throughout the device. Due to limited drive capability provided with on-chip voltage reference, this pin shall be used only for connecting an external bypass capacitor of 10 µF.
IBR	O	Bias Current Reference - Pin for connection to an external resistor (from GND) to establish a reference current for bias currents used in analog circuits.
$\overline{\text{RESET}}$	I	Reset Input - When set LOW, all the internal registers are reset and a forced head retraction is activated.
$\overline{\text{SYSRST}}$	O	Reset Output - Active LOW output signal, which is generated by a supply voltage fault or $\overline{\text{RESET}}$ being pulled LOW externally.
SYSRST	O	Reset Output - Active HIGH output signal which is inverted version of $\overline{\text{SYSRST}}$.
RCRST	I	Pin for connection to an external capacitor to extend the active low duration of $\overline{\text{SYSRST}}$.

SPINDLE MOTOR SPEED CONTROL

EXTINDX	I	External Index Input - This TTL compatible input, when selected via the INDEX SEL bit, is used to provide a once-per-revolution indication of angular position and speed to the device. The falling edge of EXTINDX is the reference.
SYSCLK	I	System Clock Input - A TTL compatible input is provided to derive internal timing signals.
EXTRC	I	Pin for connection to a resistor (from VDD) and a capacitor (from GND) to provide the commutation delay. The commutation delay is 0.56 RC. After the commutation delay, the timing block provides a noise rejection interval to reject transients on the motor coils due to commutations. This noise rejection is an additional 0.29 RC. The total time (commutation delay and noise rejection internal) must be less than a commutation cycle time.

SPINDLE MOTOR SPEED CONTROL (continued)

NAME	TYPE	DESCRIPTION
$\overline{\text{BRAKE}}$	I	Spindle Braking Enable - This input, when active LOW, dynamically brakes the spindle motor. A resistor (from $\overline{\text{SYSRST}}$) and a capacitor (from GND) are connected to this pin to provide a delay between the initiation of fault-induced head retraction and motor braking. RC are selected such that 1.2 RC is equal to the maximum time required for head retraction.
VBIAS	O	Buffered Bias Voltage - VBIAS is buffered VREF to be used for VLIM and motor speed setting bias. (In some applications, it is necessary to create an "offset" to the speed control loop to obtain proper speed regulation.)
PROP	O	Proportional Channel D/A Output - The proportional channel output is the least significant 5 bits plus sign of the period measuring counter. The LSB signifies a 2 microsecond period variation.
INTEGRAL	O	Integral Channel D/A Output - The integral channel output is the most significant 6 bits of an 8-bit accumulator. The accumulator adds the least 8 bits of the period measurement counter to the previous value obtained from prior period measurements and accumulations.
VIN	I	Speed Control Voltage Input - The combination of external driver transistors and internal predriver circuits forms a transconductance amplifier which will define the motor current in relation to VIN. In conjunction with the SENSE input and the gain setting for the sense amplifier, the transconductance gain is given by: $g_m=I_m/VIN=1/(R_S \cdot A_V)$ where I_m is the current flowing through the spindle motor coils, R_S the current sense resistor and A_V the transconductance gain defined by TGAIN0 and TGAIN1 bits.
VLIM	I	Current Limit Setting Voltage - The spindle motor current will be limited to a value determined by R_S, VLIM and Av such that Imax=VLIM/($R_S \cdot A_V$). VLIM is used whenever the spindle speed is measured less than 3490 RPM (4631), 5162 RPM (4632).
SENSE	I	Current Sense Amplifier Noninverting Input - The external driver transistor sources are connected to a current sense resistor R_S to monitor motor current. The device will control the voltage across the sense resistor to match either VIN (during normal operation) and VLIM (during acceleration).
SENSEREF	I	Current Sense Amplifier Reference Input - Pin for a Kelvin connection to the ground side of the sense resistor.
OUTA OUTB OUTC	O	Predriver Outputs - These predriver outputs drive the gates of external power NFETs. They are configured as open-drain outputs with internal 10 KΩ pull-up resistors to VBEMF.
OUTUPA OUTUPB OUTUPC	O	Upper Pull-up Outputs - These predriver outputs drive the gates of external power PFETs. They are configured as open-drain outputs with internal 10 KΩ pull-up resistors to VBEMF.
OUTCT	O	Center Tap Predriver - This output drives an external PFET driver which connects the motor center tap to the positive power supply for unipolar drive applications. OUTCT has the same characteristics as OUTUPA,B,C and is enabled via the UNIPOLAR bit.

SPINDLE MOTOR SPEED CONTROL (continued)

NAME	TYPE	DESCRIPTION
VBEMF	I	Back-emf Voltage - A power diode voltage drop from the motor power supply is defined as VBEMF. The external PFET sources are connected to VBEMF as is this pin. During power failure, this voltage is used to provide power for head retraction and motor braking.
BEMFA BEMFB BEMFC CTSENSE	I	Back-emf Inputs - Inputs to be connected to their respective motor coils and the center tap for sensing generated back-emf voltages. The device uses the back-emf voltages to determine the rotor position and effect commutation.
REVCLK	O	Revolution Clock Output - This output generates a once-per-revolution indication of motor activity derived from back-emf events.

DATA ACQUISITION AND MICROPROCESSOR BUS INTERFACE

ALE	I	Address Latch Enable - Falling edge latches the register address from the AD0..AD7 address/data bus.
$\overline{ASE}$	I	Address Strobe Enable - When set LOW, this input enables ALE input to the device.
$\overline{CS}$	I	Chip Select - Active LOW signal enables the device to respond to µP read or write.
$\overline{WR}$	I	Write Strobe - In Intel µP applications, active LOW signal causes the data on the address/data bus to be written to the addressed register if $\overline{CS}$ is also active.
$\overline{RD}$	I	Read Strobe - In Intel µP applications, active LOW signal causes the contents of the addressed register to be placed on the address/data bus if $\overline{CS}$ is also active.
AD0..AD7	I/O	Address/Data Bus - 8-bit bus which carries register address information and bidirectional data. These pins are in the high impedance state when not used.
BUSMODE	I	Mode Select - When active HIGH, Intel bus interface is selected. Otherwise, Motorola bus interface is selected.
$\overline{INT}$	O	Interrupt Strobe - Active LOW output signals the µP to respond to the device. It is released when all the pending interrupts have been serviced by the µP.
PWRDN	I	Power-down Mode Enable - When set HIGH, the device is in the power-down mode where all analog circuitry is de-biased, the clock is disabled and the output drivers are pulled to logical HIGH.
ERRDAC	O	Error DAC Output - An 8-bit D/A output which converts a digital word from the µP into an analog signal. This signal is fed back to the position error amplifier through external RC components.
ERREF	O	Reference voltage for D/A output ERRDAC.
ADCIN	I	External A/D input.
MUXOUT	O	Test point for the X4 amplifier output which is the input to the A/D converter.

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EMBEDDED SERVO TIMING CONTROLLER

NAME	TYPE	DESCRIPTION
EXDET	I	Bit Synchronization Input - The internal servo timing controller is synchronized with this TTL compatible input.
$\overline{HOLD}$	O	AGC Gain Hold - TTL compatible control signal holds the input AGC amplifier gain of a pulse detector, such as 32P4620, when pulled LOW.
WGIN	I	Write Gate Input - TTL compatible input from the storage controller.
WGOUT	O	Write Gate Output - TTL compatible control signal derived from WGIN. This output will be pulled LOW during embedded servo position burst sampling.
$R\overline{W}$	O	Read/Write Control Output - TTL compatible control signal derived from WGIN. This output will be pulled HIGH during embedded servo position burst sampling or when a low voltage fault occurs.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device or affect reliability.

PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNITS
Supply voltage applied at VPA, VPB, VPC, VPD, VPG	VDD		0.1		7.0	V
Signal ground applied at VNA, VNB, VNC, VND, VND2, VNG	GND		0.0		0.0	V
Bridge voltage applied at VBRIDGE	VBRIDGE		0.1		14.0	V
Bypass voltage applied at VBYP	VBYP		0.1		14.0	V
Back-emf voltage applied at VBEMF	VBEMF		0.1		20.0	V
VBEMF current if VBEMF>18V	IBEMF		-		5.0	mA
Digital input voltages	VIND		-0.3		VDD+0.3	V
Analog input voltages	VINA		-0.3		VDD+0.3	V
Storage temperature	Tstg		-65		150	°C
Lead temperature	TI		-		300	°C

OPERATING ENVIRONMENT LIMITATIONS

The recommended operating conditions for the device are indicated in the table below. Performance specifications do not apply where the device is operating outside these limits.

PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Supply voltage applied at VPA,VPB,VPC,VPD,VPG	VDD		4.75	-	5.25	V
Signal ground applied at VNA,VNB,VNC,VND, VND2,VNG	GND		0.0	-	0.0	V
Bridge voltage applied at VBRIDGE	VBRIDGE		4.75	-	13.2	V
Bypass voltage applied at VBYP	VBRIDGE -VBYP		0.0	-	0.8	V
Back-emf voltage applied at VBEMF	VBRIDGE -VBEMF		-5.0	-	0.8	V
Ambient temperature	TA		0.0	-	70.0	°C
System clock (10 MHz, Max)	Fc		-0.01	-	+0.01	%
Capacitive load on digital outputs	CL		-	-	100	pF
Analog input impedance	Rin		100	-	-	kΩ
	Cin		-	-	50	pF
Load on analog outputs	Rout		10	-	-	kΩ
	Cout		-	-	40	pF
Bias resistor (22.6 kΩ, Typ)	RBIAS		-1	-	+1	%

DC CHARACTERISTICS

The following electrical specifications apply to the digital input and output signals over the recommended operating range unless otherwise noted. Positive current is defined as entering the device. Minimum and maximum are based upon the magnitude of the number.

Supply current Normal mode	IDD	VDD=5.25V	-	-	50	mA
Power-down mode	-		-	-	5	mA
Output logic "1" voltage	Voh	Ioh=-0.4 mA VDD=4.75V	2.4	-	-	V
Output logic "0" voltage	Vol	Iol=1.6 mA VDD=4.75V	-	-	0.4	V
Input logic "1" voltage	Vih	VDD=4.75V	2.0	-	-	V
Input logic "0" voltage	Vil	VDD=4.75V	-	-	0.8	V

ELECTRICAL SPECIFICATIONS (continued)

DC CHARACTERISTICS (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Input logic "1" current	Iih	Vih=5.25V VDD=5.25V	-	-	10	µA
Input logic "0" current	Iil	Vil=0.0 VDD=5.25V	-	-	-10	µA
Input capacitance	Cin		-	-	10	pF

FUNCTIONAL CHARACTERISTICS

Dedicated Servo Position Processor

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
N,Q comparator hysteresis		5	-	30	mV
Commutator comparator offset		-	-	30	mV
N,Q input voltage w.r.t GND		0	-	3.7	V
NQREF w.r.t. GND		2.1	-	2.9	V
Channel gain from N,Q to PES0		0.96	1.0	1.04	
PES0 output swing w.r.t. VREF		-	-	±1.1	V
PES0 offset		-50	-	50	mV
PES0 output corner frequency		20	40	80	kHz

Embedded Servo Burst Amplitude Processor

SERIN w.r.t. GND		2.0	-	VDD	V
SEREF w.r.t. GND		2.0	-	3.0	V
SERIN input voltage	Channel gain=-6 dB	0.0	-	2.0	Vp
swing w.r.t. SEREF	Channel gain=0 dB	0.0	-	1.0	Vp
Servo burst frequency		0.5	-	2.0	MHz
Input impedance at		20	-	-	kΩ
SERIN, SEREF		-	-	10	pF
DC offset at PES1,PES2	BURST1=BURST2=0.5V BURST3=BURST4=0.5V	-	-	±20	mV
DC offset at SUM1,SUM2	BURST1=BURST2=0.5V BURST3=BURST4=0.5V	-	-	-200	mV

Embedded Servo Burst Amplitude Processor (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Differential gain error at PES1,PES2,SUM1,SUM2		-	-	±0.05	dB
Integral gain error at PES1,PES2,SUM1,SUM2		-	-	±0.5	dB
PES1,PES2 output swing w.r.t. VREF		-	-	±1.1	V
SUM1,SUM2 output swing w.r.t. VREF		-	-	1.1	V
Allowable load at PES1, PES2,		10	-	-	kΩ
SUM1,SUM2 to VREF		-	-	40	pF

Embedded Servo Timing

The following timing specifications are applied when the internal servo timing block is selected by pulling the TIMING bit to logical LOW. Timing measurements are defined in Figure 3 and made at 50% VDD with 50 pF load capacitances for all pins, unless otherwise noted.

PARAMETER	SYMBOL	MIN	NOM	MAX	UNIT
Burst cell time	t_{BST}				
TIM0='0' TIM1='0'		-	5.0	-	µs
TIM0='1' TIM1='0'		-	6.0	-	µs
TIM0='0' TIM1='1'		-	8.0	-	µs
TIM0='1' TIM1='1'		-	10.0	-	µs
EXDET pulse width	t_{EXDW}	0.5	-	t_{BST}	µs
Internal first sampling time from EXDET rise	t_{SPD}				
LEAD='0'		1.0	-	1.7	µs
LEAD='1'		(t_{BST}+1.0)	-	(t_{BST}+1.7)	µs
Sampling pulse width	t_{SPW}				
TIM0='0' TIM1='0'		-	2.0	-	µs
TIM0='1' TIM1='0'		-	3.0	-	µs
TIM0='0' TIM1='1'		-	5.0	-	µs
TIM0='1' TIM1='1'		-	7.0	-	µs
Acquisition pulse width	t_{APW}	-	2.0	-	µs
Discharge pulse width	t_{DIS}	-	0.75	-	µs
Nonoverlapping time between sampling & acquisition pulses	t_{NON}	-	0.25	-	µs

Embedded Servo Timing (continued)

PARAMETER	SYMBOL	MIN	NOM	MAX	UNIT
Burst ready interrupt from EXDET rise	t_{INT}				
DIBURST='0' LEAD='0'		$(4t_{BST}+5.2)$	-	$(4t_{BST}+5.9)$	µs
DIBURST='1' LEAD='0'		$(2t_{BST}+5.2)$	-	$(2t_{BST}+5.9)$	µs
DIBURST='0' LEAD='1'		$(5t_{BST}+5.2)$	-	$(5t_{BST}+5.9)$	µs
DIBURST='1' LEAD='1'		$(3t_{BST}+5.2)$	-	$(3t_{BST}+5.9)$	µs
WGOUT & $R\overline{W}$ delay time from EXDET rise	t_{DWG}	0.0	-	0.1	µs
WGOUT & $R\overline{W}$ hold time from EXDET rise	t_{XWG}				
DIBURST='0' LEAD='0'		$(4t_{BST}+1.0)$	-	$(4t_{BST}+1.7)$	µs
DIBURST='1' LEAD='0'		$(2t_{BST}+1.0)$	-	$(2t_{BST}+1.7)$	µs
DIBURST='0' LEAD='1'		$(5t_{BST}+1.0)$	-	$(5t_{BST}+1.7)$	µs
DIBURST='1' LEAD='1'		$(3t_{BST}+1.0)$	-	$(3t_{BST}+1.7)$	µs
$\overline{HOLD}$ delay time from EXDET rise	t_{DHL}				
LEAD='0'		0.2	-	0.7	µs
LEAD='1'		$(t_{BST}+0.2)$		$(t_{BST}+0.7)$	µs
$\overline{HOLD}$ hold time from EXDET rise	t_{XHL}				
DIBURST='0'		$(4t_{BST}+1.0)$	-	$(4t_{BST}+1.7)$	µs
DIBURST='1'		$(2t_{BST}+1.0)$	-	$(2t_{BST}+1.7)$	µs

The following timing specifications are applied when the internal servo timing block is selected by pulling the TIMING bit to logical HIGH. Timing measurements are defined in Figure 4 and made at 50% VDD with 50 pF load capacitances for all pins, unless otherwise noted.

EXDET pulse width	t_{EXDW}	0.5	-	5.0	µs
SAMPLEX delay time from EXDET rise	t_{SPD}	0.2	-	-	µs
SAMPLEX pulse width	t_{SPW}	3	-	-	µs
ACQX pulse width	t_{APW}	2	-	-	µs
Nonoverlapping time between SAMPLEX & ACQX pulses	t_{NON}	0.0	-	-	µs
Burst ready interrupt from last ACQX fall	t_{INT}	5.2	-	5.9	µs
WGOUT & $R\overline{W}$ delay time from EXDET rise	t_{DWG}	0.0	-	0.1	µs

Embedded Servo Timing (continued)

PARAMETER	SYMBOL	MIN	NOM	MAX	UNIT
WGOUT & $R\overline{W}$ hold time from last ACQX fall	t_{XWG}	1.0	-	1.7	µs
$\overline{HOLD}$ delay time from first SAMPLEX rise	t_{DHL}	0.2	-	0.7	µs
$\overline{HOLD}$ hold time from last ACQX fall	t_{XHL}	1.0	-	1.7	µs

Head Positioner MOSFET Driver

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VRETRACT voltage	VBEMF = 3V	0.3	-	0.9	V
	VBEMF = 12V	0.4	-	1.2	V
Retract offset VBEMF = 3V	VRETRACT = 0.5V	-50	-	50	mV
VBEMF = 6V	VBYP = 4V to 13V	-70	-	70	mV
VBEMF = 12V	I_{AOUTR}<1mA	-150	-	150	mV
Voh at AOUTR VBEMF = 4V VBYP = 4V	Ioh = 1mA	1.5	-	-	V
VBEMF = 4V VBYP = 3V		1.3	-	-	V
Leakage current at AOUTR	RETRACT = LOW AOUTR = 0V to 14V	-	-	1	µA
Voh at AOUTA, AOUTC	Ioh = -1 mA	VBRIDGE-1.2	-	-	V
	Ioh = -1 µA	VBRIDGE-0.1	-	-	V
Vol at AOUTA, AOUTC	Iol = 10 µA	-	-	1	V
Voh at AOUTB	Ioh = -10 µA	VBRIDGE-0.5	-	-	V
Voh at AOUTD	Ioh = -10 µA	VBYP-0.5	-	-	V
Vol at AOUTB, AOUTD	Iol = 1 mA	-	-	1	V
	Iol = 10 µA	-	-	0.2	V
Input offset at SOUT		-	-	3	mV
SOUT/(SE1-SE2)		3.9	-	4.1	V/V
SE1/ERR, SE3/ERR		14.0	-	15.4	V/V
ERRAMP input offset		-	-	10	mV
ERRAMP gain		1000	-	-	V/V
Output crossover time CL = 600 pF at AOUTA,C CL = 150 pF at AOUTB,D	PFET VTH = -2V NFET VTH = 2V R_X = 50 kΩ	-	-	45	µs
Input impedance at SE1, SE2,SE3		20	-	-	kΩ

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Voltage Reference and Voltage Fault Circuit

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VPB voltage for $\overline{SYSRST}$ & RCRST in operation		-	-	2	V
On resistance at RCRST					
VPB>3.5V VBYP>4V		-	-	800	Ω
VPB>3.5V VBYP>10V		-	-	550	Ω
RCRST input threshold	VBYP=4V	0.2	-	1.2	V
IBR voltage w.r.t. VREF		-80	-	20	mV
VREF voltage	|II|<10μA	2.14	-	2.36	V
VREF trimming steps	relative to				
TRIM0 = '0' TRIM1 = '0'	TRIM0 = '1', TRIM1 = '1'	-	-30	-	mV
TRIM0 = '0' TRIM1 = '1'		-	+70	-	mV
TRIM0 = '1' TRIM1 = '0'		-	-90	-	mV
PSB,PSV comparator offset		-15	-	15	mV

Spindle Motor Speed Control

SYSCLK duty cycle		40	-	60	%
EXTINDX pulse width		200	-	-	ns
Timing resistor at EXTRC		0.01	-	10	MΩ
Timing capacitor at EXTRC		100	-	-	pF
Delay time variation relative to T0*		-5	-	5	%
Vil at $\overline{BRAKE}$	VBEMF = 5V	0	-	0.3	V
Vih at $\overline{BRAKE}$	VBEMF = 5V	1.5	-	-	V
Output voltage swing at PROP & INTEGRAL	I_{out}<0.1mA	0	-	VBIAS±5%	V
DAC step size at PROP & INTEGRAL		32	-	39	mV
Output impedance at PROP & INTEGRAL	0.5V<V_{out}<2.0V, I_{out}=0.1mA	-	-	300	Ω
Kp,proportional gain**	32H4631	0.70	0.77	0.85	V/rad/s
	32H4632	0.31	0.34	0.38	V/rad/s
Ki,integral gain	32H4631	10.48	11.6	12.75	V/rad
	32H4632	6.98	7.75	8.533	V/rad
VBIAS output w.r.t. VREF		-50	-	25	mV
Input voltage at VIN & VLIM		0	-	2.25	V

I*T0 is the commutation delay and is given by the relationship T0 = 0.56RC. Suggested value for C would be 470 to 1000 pF. An external R and C must be provided such that T0 is greater than 10 μs (R=22 kΩ, C=470 pF).

**The motor speed control loop can be described as: $H(s)=K_p+K_i/s$

Spindle Motor Speed Control (continued)

PARAMETER	CONDITIONS		MIN	NOM	MAX	UNIT
Input leakage current at VIN & VLIM			-1	-	1	µA
Output resistance at OUTUPA,B,C & OUTCT	Output in HIGH state, pulled to VBEMF		5	-	20	kΩ
Vol at OUTUPA,B,C & OUTCT	I_{out}<3mA VBEMF=13.2V		-	-	1.0	V
Output resistance at OUTA,B,C	Output in HIGH state, pulled to VBEMF		5	-	20	kΩ
Vol at OUTA,B,C	I_{out}<5mA		-	-	1.0	V
Input voltage at SENSE	A_V=2		0.0	-	1.0	V
Input voltage at SENSEREF			0.0	-	0.05	V
Input leakage current at SENSE	0.0V<V_{in}<1.0V		-10	-	10	µA
Input leakage current at SENSEREF	0.0V<V_{in}<0.05V		-200	-	10	µA
Input capacitance at SENSE & SENSEREF			-	-	20	pF
Gain variation*	A_V=2,4,8,16		-10	-	10	%
Input impedance at	-0.3V<V_{in}<15V		100	-	-	kΩ
BEMFA,B,C,CTSENSE			-	-	10	pF
LOCK indication range			3593.5	-	3606.5	RPM
Speed resolution		32H4631	3593.5	0.012	3606.5	%
		32H4632	5385.9	0.18	5415.1	%

*The transconductance gain from VIN or VLIM to the steady-state current flowing through the motor is given by $G = 1/(R_{SENSE} \cdot A_V)$

DATA ACQUISITION

A/D Converter

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
ADCIN full-scale	X4=LOW	-	±(VREF/2)	-	V
swing w.r.t. VREF	X4-HIGH	-	±(VREF/8)	-	V
Resolution		-	8	-	Bits
Conversion time*		-	-	4.0	µs
LSB voltage	X4=LOW	-	VREF/256	-	mV
	X4=HIGH	-	VREF/1024	-	mV
Differential nonlinearity		-	-	±0.5	LSB

DATA ACQUISITION (continued)

Error D/A Converter

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
ERRDAC full-scale voltage swing w.r.t ERREF		-	±(VREF/2)	-	V
Resolution		-	8	-	Bits
Conversion time*		-	-	4.0	µs
LSB voltage		-	VREF/256	-	mV
Differential nonlinearity		-	-	±0.5	LSB

*A maximum of 2 µs of latency between a conversion request and the actual start of conversion must be added to this conversion time of 4 µs to calculate the total delay time from a conversion request to the completion of conversion.

Intel Microprocessor Interface Timing

The following timing specifications are applied when an Intel bus interface is selected by pulling the BUSMODE pin to logical HIGH. Timing measurements are defined in Figure 5 and made at 50% VDD with 50 pF load capacitances for all pins, unless otherwise noted.

PARAMETER	SYMBOL	MIN	NOM	MAX	UNIT
Pulse width, ALE HIGH	t_{ALPW}	45	-	-	ns
Muxed address valid time to ALE fall	t_{AS}	7.5	-	-	ns
Muxed address hold time from ALE fall	t_{AH}	20	-	-	ns
Read data delay time from $\overline{RD}$ fall	t_{DDR}	-	-	149	ns
Read data hold time from $\overline{RD}$ rise	t_{DHR}	0	-	55	ns
Pulse width, $\overline{RD}$ LOW	t_{RDPW}	200	-	-	ns
Write data set up time to $\overline{WR}$ rise	t_{DSW}	70	-	-	ns
Write data hold time from $\overline{WR}$ rise	t_{DHW}	10	-	-	ns
Pulse width, $\overline{WR}$ LOW	t_{WRPW}	100	-	-	ns
$\overline{RD}$ or $\overline{WR}$ delay time from ALE fall	t_{RWD}	25	-	-	ns
$\overline{CS}$ valid time to ALE fall	t_{CSS}	0	-	-	ns
$\overline{CS}$ hold time from $\overline{RD}$ or $\overline{WR}$ rise	t_{CSH}	0	-	-	ns
$\overline{ASE}$ valid time to ALE fall	t_{ASES}	45	-	-	ns
$\overline{ASE}$ hold time from ALE fall	t_{ASEH}	0	-	-	ns

Motorola Microprocessor Interface Timing

The following timing specifications are applied when a Motorola bus interface is selected by pulling the BUSMODE pin to logical LOW. Timing measurements are defined in Figure 6 and made at 50% VDD with 50 pF load capacitances for all pins, unless otherwise noted.

PARAMETER	SYMBOL	MIN	NOM	MAX	UNIT
Pulse width, AS HIGH	t_{ASPW}	45	-	-	ns
Muxed address valid time to AS fall	t_{AS}	10	-	-	ns
Muxed address hold time from AS fall	t_{AH}	20	-	-	ns
Read data delay time from DS rise	t_{DDR}	-	-	180	ns
Read data hold time from DS fall	t_{DHR}	0	-	80	ns
Pulse width, DS HIGH during READ	t_{DSPWR}	200	-	-	ns
Write data setup time to DS fall	t_{DSW}	70	-	-	ns
Write data hold time from DS fall	t_{DHW}	10	-	-	ns
Pulse width, DS HIGH during WRITE	t_{DSPWW}	100	-	-	ns
DS delay time from AS fall	t_{ASDS}	25	-	-	ns
R/$\overline{W}$ delay time from AS fall during WRITE	t_{ASRW}	25	-	-	ns
R/$\overline{W}$ hold time from DS fall during WRITE	t_{RWH}	0	-	-	ns
$\overline{CS}$ valid time to AS fall	t_{CSS}	0	-	-	ns
$\overline{CS}$ hold time from DS fall	t_{CSH}	0	-	-	ns
$\overline{ASE}$ valid time to AS fall	t_{ASES}	45	-	-	ns
$\overline{ASE}$ hold time from AS fall	t_{ASEH}	0	-	-	ns

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Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 731-7110, FAX (714) 573-6914

Notes:

silicon systems®
A TDK Group Company

SSI 32H6110
Differential Amplifier

November 1991

DESCRIPTION

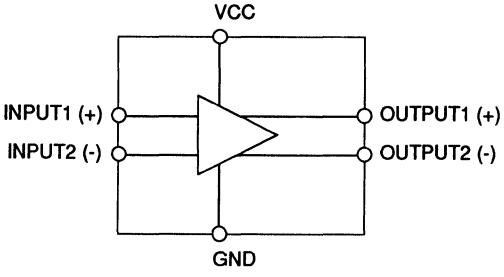
The SSI 32H6110 is a high performance, differential amplifier used as a preamplifier for the magnetic servo thin-film head in Winchester disk drives. The SSI 32H6110 is offered in an 8-pin SON package.

FEATURES

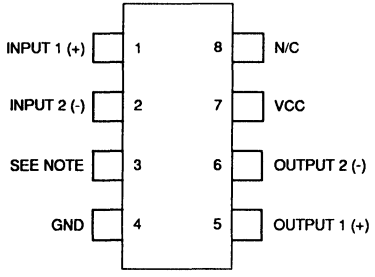
- **High gain (Av=300)**
- **Low noise, 0.85 nV/$\sqrt{Hz}$ maximum**
- **Operates with a +5V power supply**

6

BLOCK DIAGRAM



PIN DIAGRAM



8-Pin SON

CAUTION: Use handling procedures necessary for a static sensitive component.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS – operating above maximum ratings may damage the device

PARAMETER	RATING	UNIT
Power Supply Voltage (VCC)	7	V
Differential Input Voltage	±1	V
Storage Temperature Range	-65 to 150	°C
Operating Ambient Temperature, Ta	10 to 100	°C
Operating Junction Temperature, Tj	10 to 135	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Supply Voltage (VCC)		4.50	5.0	5.50	V
Input Signal (Vin)			1.0		mVpp
Ambient Temperature		+10		+100	°C
Operating Junction Temperature		+10		+135	°C

ELECTRICAL CHARACTERISTICS
Unless otherwise specified, recommended operating conditions apply.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Gain (Differential)	R_L = 120Ω	Vin = 1mVpp, R_L = 120Ω Ta = 25°C, f = 1 MHz	225	300	375	mV/mV
	R_L = 100Ω	Vin = 1mVpp, R_L = 100Ω Ta = 25°C, f = 1 MHz	200	250	300	mV/mV
Bandwidth (3 dB)		Vin = 1mVpp, C_L = 15 pF R_L = 120Ω	10	30		MHz
Gain Sensitivity (Supply)		Ta = 25°C			4.0	%/V
Gain Sensitivity (Temp.)		15°C < Ta < 55°C			–0.16	%/°C
Input Noise Voltage		Input Referred, Rs = 0		0.6	0.85	nV/√Hz
Input Capacitance (Differential)		Vin = 1 mVpp, f = 5 MHz			35	pF
Input Resistance (Differential)				200		Ω
Common Mode Rejection Ratio (Input Referred)		Vin = 100 mVpp, f = 1 MHz	60			dB
Power Supply Rejection Ratio (Input Referred)		Vin = 100 mVpp, f = 1 MHz	54			dB

ELECTRICAL CHARACTERISTICS, (Continued)
Unless otherwise specified, recommended operating conditions apply.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Input Dynamic Range (Differential)	AC input voltage where gain falls to 90% of its small signal value, f = 5MHz, R_L = 120Ω	5.0			mVpp
Output Offset Voltage (Differential)	Inputs shorted	-400	±50	+400	mV
Output Voltage (Common Mode)	Inputs shorted together and Outputs shorted, R_L = 120Ω	VCC-0.56	VCC-0.88	VCC-1.2	V
Single Ended Output Capacitance				10	pF
Power Supply Current	VCC = 5V		23	34	mA
Input DC Voltage	Common Mode		2.0		V

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APPLICATION INFORMATION

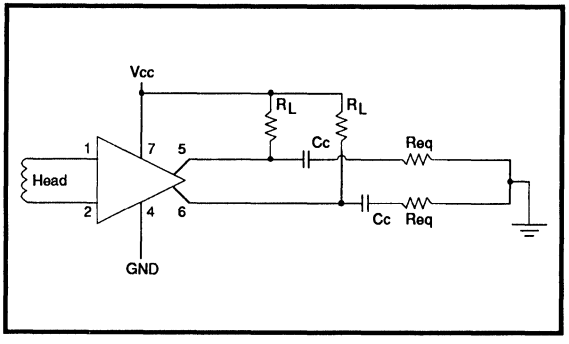


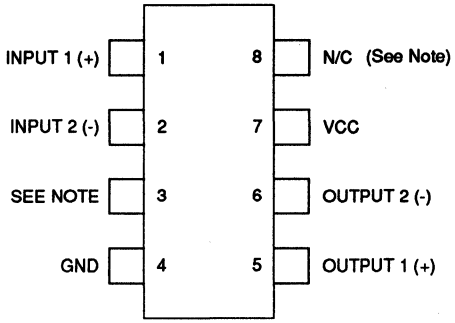
FIGURE 1: Connection Diagram

RECOMMENDED LOAD CONDITIONS

1. Input is directly coupled to the head.
2. Cc's are AC coupling capacitors.
3. RL's are DC bias and termination resistors, 120Ω recommended.
4. REQ. represents equivalent load resistance.
5. Ceramic capacitors (0.1 µF) are recommended for good power supply noise filtering.

SSI 32H6110
Differential Amplifier

PACKAGE PIN DESIGNATIONS
(Top View)



8-Pin SON

NOTE : N/C pin must be left open and not connected to any circuit etch.

ORDERING INFORMATION

PART DESCRIPTION	ORDERING NUMBER	PACKAGE MARK
SSI 32H6110 Differential Amplifier		
8-Pin SON	32H6110-CN	H6110

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 731-7110, FAX (714) 573-6914

silicon systems®
A TDK Group Company

SSI 32H6210
Servo Demodulator

Preliminary Data

December 1991

DESCRIPTION

The SSI 32H6210 Servo Demodulator is a bipolar device intended for use in Winchester disk drives with dedicated surface head positioning systems. It processes a di-bit quadrature pattern read from the servo surface by a preamplifier, such as the SSI 32H101 or SSI 32H116, and generates normal and quadrature (N and Q) position reference signals. These signals provide the servo controller with position error feedback. A complete position control system can be realized with the SSI 32H6210 and its companion devices, the SSI 32H6220 Servo Controller and SSI 32H6230 Servo Motor Driver.

The SSI 32H6210 incorporates an input amplifier with automatic gain control and offset cancellation, a phase locked loop and sync separator to recover timing information, and pulse area detectors to recover the position information. External components are used to set the operating characteristics of the SSI 32H6210, such as AGC response, VCO center frequency, PLL response and sync separator threshold. Its high performance analog/digital circuitry is capable of supporting servo frame rates of up to 400 kHz.

FEATURES

- **Servo signal demodulation for dedicated surface head positioning systems**
- **Supports industry standard di-bit quadrature servo pattern with frame rates up to 400 kHz**
- **N, Q outputs convey track crossing and position error information**
- **PLL for timing recovery and synchronization**
- **Adjustable sync separator threshold**
- **Auto-zeroing AGC input amplifier**
- **AGC reference level adjustment**
- **Precision bandgap voltage reference output**
- **Advanced bipolar process dissipates less than 900 mW (5V, 12V)**
- **Available in 28-pin PLCC, DIP, SO packages**

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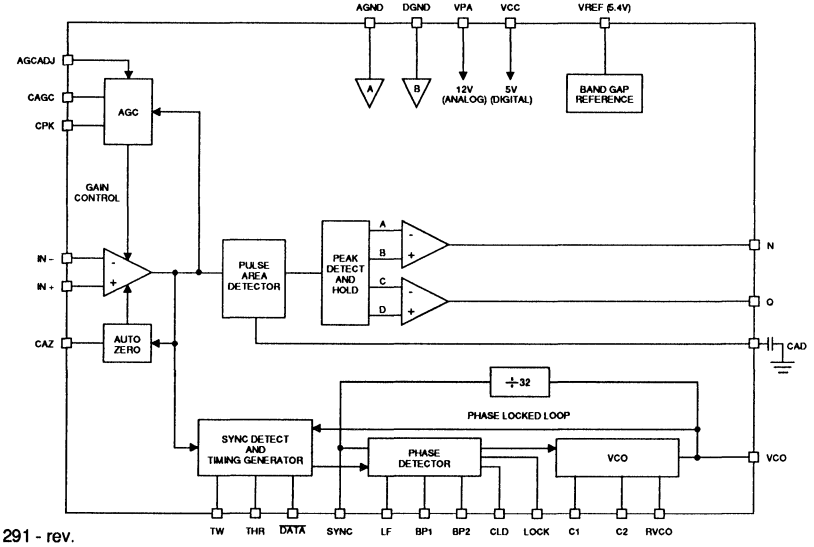
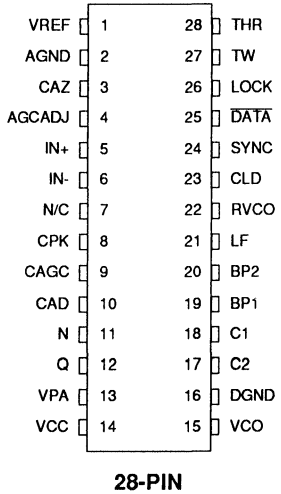
BLOCK DIAGRAM



1291 - rev.

PIN DIAGRAM



28-PIN DIP, SO

FUNCTIONAL DESCRIPTION

(Refer to block diagram, and typical application, Fig.2)

The SSI 32H6210 processes servo position information which is read from a dedicated surface by a pre-amplifier. The servo information must conform to the 'di-bit quadrature' pattern which is illustrated in Figure 4. Servo frames, consisting of data and sync pulses followed by four information pulses (A, B, C, D) are prerecorded along each track of the servo surface. All the servo frames on an individual track are identical, but in the radial direction four different frame types are encountered, with every fourth track being identical. The N signal generated by the SSI 32H6210 is proportional to the difference in sizes of pulses A and B, while the Q signal is proportional to the difference between pulses C and D. When the read head is off track, the read signal is effectively a linear interpolation between the prerecorded information of two adjacent tracks, making it possible to sense the head displacement exactly.

The SSI 32H6210 has a differential input amplifier which incorporates offset voltage cancellation and automatic gain control. An external read preamplifier must provide a differential input signal of 23 to 400 mV peak to peak from the servo read head. This signal is applied to a pulse detector whose output is proportional to the area under the input pulse.

An AGC circuit adjusts the input gain so that the maximum pulse detector output is 2V peak. The AGC circuit incorporates a peak detector which stores the maximum pulse area signal on the external capacitor C_{PK}. This signal is compared to an internal amplitude reference and the input amplifier gain is adjusted until they are equal. The capacitor C_{AGC} determines the response time of the gain control circuit. An offset cancellation circuit , whose response is set with the external capacitor C_{AZ}, ensures that the average level at the differential amplifier output is zero.

An AGC adjust (AGCADJ) pin allows the user to adjust the AGC reference level. AGCADJ can be driven with a potentiometer or a D/A (a simple Pulse Width Modulated signal is usually sufficient.) This pin is left open if no AGC adjustment is required.

All internal analog signals are referenced to a 5.4V bandgap reference voltage. This level is available at the VREF output, which is capable of supplying 10 mA to the rest of the servo path electronics.

In a standard servo frame, the data and sync pulses are more closely spaced than the information pulses (A-D). This allows the sync detect circuit to recover the SYNC pulses. A threshold, which is defined as percentage of the peak signal at the output of the AGC amplifier, is set externally with R_{TH}. Pulses which exceed this threshold are defined as valid pulses. As illustrated in Figure 6, at the end of the positive going half of a valid pulse, a window, whose width is set by Rw and Cw, is opened. If a second valid pulse occurs within this window, it is recognized as a SYNC pulse. This pulse becomes the input signal to a phase locked loop whose VCO clock frequency is 32 times the SYNC frequency (servo frame rate). The $\overline{DATA}$ output rises after a missing data pulse. The example illustrated in Figure 6 includes the case of a missing DATA pulse. The SYNC clock output, which marks the start of a new servo frame, is derived from the VCO output so that the clock continues to run when a data pulse is missing. Absolute positioning information such as track 0 and guardband flags may be encoded on the servo surface by the omission of data pulses.

To generate the servo pattern shown in the timing diagram, Figure 5, the DATA and SYNC pulses must be written to overlap as shown in Figure 7.

The phase detector compares the detected sync pulses with the SYNC output. A current pulse proportional to the phase error is applied to an external loop filter network connected to the LF pin, to generate the VCO control voltage. If improved power supply rejection is required, bypassing may be provided at pins BP1 and BP2. The VCO center frequency is determined by the external components R_{VCO} and C_{VCO}.

A lock detect circuit measures the phase difference between the detected sync pulses and the sync output. When this difference exceeds half of a VCO clock cycle, a pulse of discharge current is applied to CLD. Otherwise a pulse of charging current is applied to CLD.

A clamp circuit limits the swing of the CLD pin and also insures that a small amount of hysteresis is present. When the voltage on CLD falls below the upper clamp level by more than the "lock margin," the open collector LOCK output transistor is turned on. Likewise, when the voltage on CLD rises above the lower clamp level by more than the "unlock margin," the LOCK output transistor is turned off.

FUNCTIONAL DESCRIPTION (Continued)

Internal timing windows are generated from the recovered SYNC pulse and VCO clock. These windows, WA, WB, WC, and WD, in Figure 5, enable the four peak detectors to capture the A, B, C and D information pulses. The N and Q analog outputs are formed by differencing adjacent pulses. These outputs change during a servo frame and only become valid after the D pulse has been detected. N and Q should be sampled by the servo controller on the next falling edge of the SYNC output clock.

An example of an entire servo path implemented with the SSI 32H6210 and its companion devices, the SSI 32H6220 and SSI 32H6230, is shown in Figure 9.

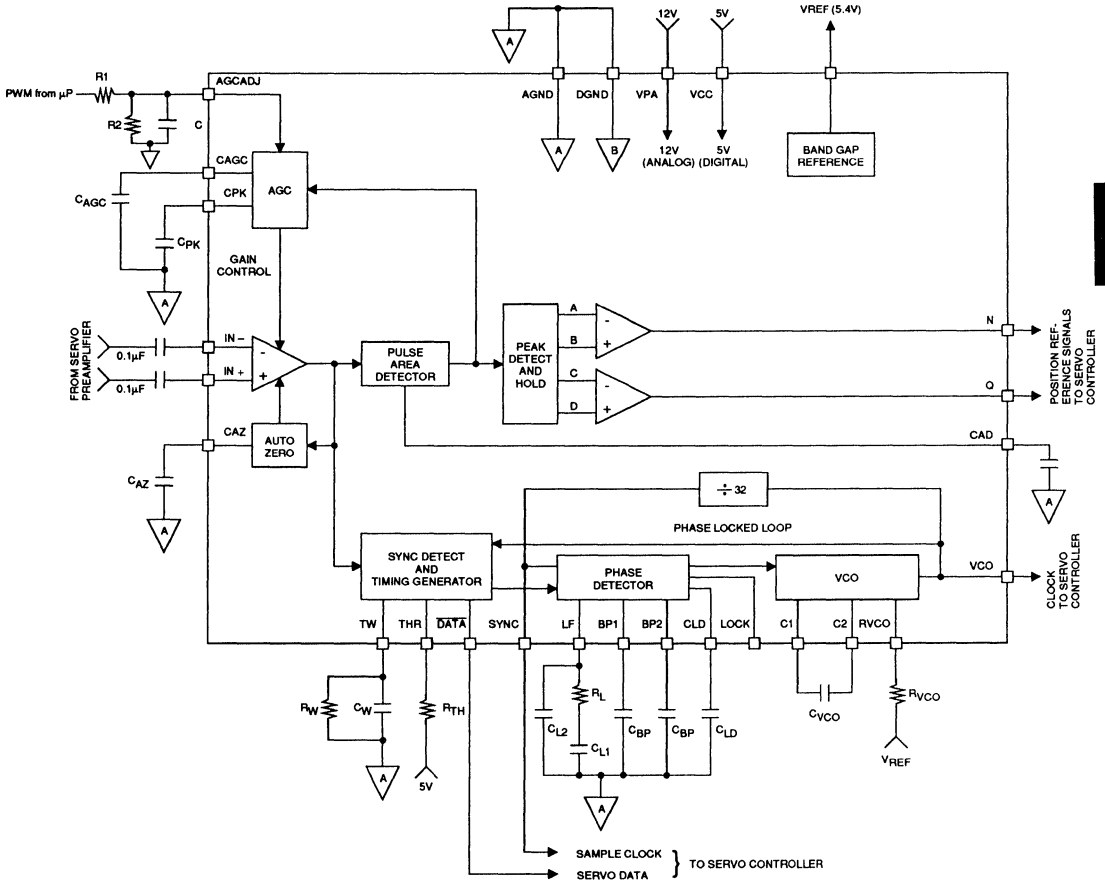


FIGURE 2: Typical Application

PIN DESCRIPTION

POWER

NAME	TYPE	DESCRIPTION
VREF	O	REFERENCE VOLTAGE - 5.4V output. All analog signals are referenced to this voltage.
AGND	-	ANALOG GROUND
VPA	-	ANALOG SUPPLY - 12V power supply.
VCC	-	DIGITAL SUPPLY - 5V power supply.
DGND	-	DIGITAL GROUND

INPUT AMPLIFIER

NAME	TYPE	DESCRIPTION
CAZ	-	AUTOZERO CAPACITOR - A capacitor which sets the response of the input amplifier offset cancellation circuit should be connected between this pin and analog ground.
IN +	I	NON-INVERTING INPUT - AGC input amplifier connection. The non-inverting output of the differential servo pre-amplifier should be AC coupled to this pin.
IN -	I	INVERTING INPUT - AGC input amplifier connection. The inverting output of the differential servo pre-amplifier should be AC coupled to this pin.
CPK	-	PEAK HOLD CAPACITOR - A capacitor which is used by the peak detector of the AGC circuitry must be connected between this pin and analog ground.
CAGC	-	AGC CAPACITOR - A capacitor which sets the AGC attack and decay times must be connected between this pin and analog ground.
AGCADJ	I	AGC Adjust - This pin allows for AGC reference level adjustment. It is driven by a potentiometer or D/A. Normally this pin is left open.

TIMING RECOVERY

NAME	TYPE	DESCRIPTION
VCO	O	VCO OUTPUT - TTL compatible digital clock which is 32 times the sync frequency (servo frame rate).
C2,C1	-	VCO CAPACITOR - Connection points for a capacitor which sets the VCO center frequency in conjunction with an external resistor connected to RVCO.
BP1,BP2	-	PLL BYPASS - Bypass capacitors may be connected between these pins and analog ground to provide additional power supply rejection in the phase locked loop.

TIMING RECOVERY (Continued)

NAME	TYPE	DESCRIPTION
LF	-	PHASE LOCKED LOOP FILTER - An external RC network which sets the PLL loop characteristics must be connected between this pin and analog ground.
RVCO	-	VCO RESISTOR - Connection for a resistor which sets the VCO center frequency, in conjunction with the capacitor between pins C1 and C2. The resistor must be connected between this pin and the VREF output.
SYNC	O	SYNC OUTPUT - TTL compatible digital clock whose falling edge indicates the presence of valid analog signals on the N and Q outputs. There is one SYNC cycle per servo frame.
$\overline{\text{DATA}}$	O	DATA OUTPUT - Active low TTL compatible digital output that indicates the presence of a data pulse in the servo frame. This signal is updated on the falling edge of the SYNC output.
TW	-	TIMING WINDOW - A resistor and capacitor must be connected in parallel between this pin and analog ground to set a timing window which is used in detecting SYNC pulses.
THR	-	PULSE THRESHOLD - A resistor which sets a threshold for SYNC and $\overline{\text{DATA}}$ pulse detection must be connected between this pin and VCC (digital 5V supply).
CLD	-	LOCK DETECT CAPACITOR - The value of this capacitor determines how quickly the LOCK output responds (1000 pF).
LOCK	O	LOCK OUTPUT - An open collector output that indicates the lock status of the PLL.

POSITION INFORMATION

NAME	TYPE	DESCRIPTION
CAD	-	AREA DETECTOR CAPACITOR - A capacitor, which forms an integrator to sense the pulse area of the servo position signals, must be connected between this point and analog ground.
N	O	N OUTPUT - This sampled analog signal is the normal position reference output. N is referenced to VREF and is periodic in radial displacement, with a period of 4 tracks.
Q	O	Q OUTPUT - This sampled analog signal is the quadrature position reference output. Q is referenced to VREF and is periodic in radial displacement, with a period of 4 tracks. It is 90 degrees out of phase with N.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

(Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC operating characteristics.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VCC voltage		0		8	V
VPA voltage		0		16	V
Voltage on PLL inputs		-0.5		VCC+0.5	V
Voltage on other inputs		0		14	V
Storage Temp.		-45		160	°C
Solder Temp.	10 sec. duration			260	°C

RECOMMENDED OPERATION CONDITIONS (Unless otherwise noted, the following conditions are valid throughout this document.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VPA, analog supply		10.8	12	13.2	V
Supply noise	F<1 MHz			0.1	Vpp
VCC, digital supply		4.75	5	5.25	V
Ta, ambient temperature		0		70	°C
VCO operating range				12.8	MHz
Load resistance	To VREF	10			kΩ
Load capacitance				50	pF

DC CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
IPA, VPA current				50	mA
ICC, VCC current				60	mA
VOH, digital output high	|IOH|<40 µA	2.4			V
VOL, digital output low	|IOL|<1.6 mA			0.5	V
IREF, VREF output current capacity		10			mA
VREF output voltage	|IREF|<10 mA	5.1	5.4	5.7	V

ELECTRICAL SPECIFICATIONS (Continued)

AC CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VREF output impedance	IOUT = 0-10 mA 1 µF bypass to AGND Frequency<15MHz			12	Ω
N, Q outputs					
Output impedance	F = 1 MHz			100	Ω
Voltage per track	Referenced to VREF 23-400 mVpp differential AGCADJ open	1.8	2	2.2	V
Offset voltage				20	mV
Output noise	10 Hz<F<1 kHz		-55		dBV
Input amplifier					
Input resistance		5			kΩ
Input resistance mismatch				1	%
Input capacitance				20	pF
PSRR	F<0.5MHz	35			dB
AGC headroom		2			dB
AGC bandwidth	Open loop unity gain C_{AGC}=0.04 µF C_{PK}=1500 pF	5		15	kHz
Autozero pole	C_{AZ} in µF		220/C_{AZ}		Hz
AGCADJ					
Open circuit voltage		0.7	0.76	0.82	V
Gain		-1.6	-1.4	-1.2	V/V
Volts per track adj range		1.0		2.6	V
Input impedance, R_{AGC}	Ta = 25°C	4	5.5	7	kΩ
	Temp. coefficient		2600		ppm/°C
SYNC detector					
Timing window	Rw in Ω, Cw in pF	$0.4(R_W \cdot C_W) + 43 \cdot 10^{-9}$			s
Valid pulse threshold	R_{TH} in kΩ (% of full scale)		0.37/R_{TH}		%

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ELECTRICAL SPECIFICATIONS (Continued)

AC CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LOCK Detector					
CLD up current	RVCO = 11K ± 1%	0.7		3	µA
CLD down current	RVCO = 11K ± 1%	3		10	µA
CLD lock margin		0.5		1.3	V
CLD unlock margin		0.5		1.3	V
CLD hysteresis		75		400	mV
Phase locked loop					
Capture range	Centered on selected f_{NOM}	±5			%
VCO phase shift	Missing DATA pulse			0.005	rad/frame
VCO phase delay	Relative to sync pulse zero crossing			70	ns
VCO gain	f_{VCO} in Hz		10.47 f_{VCO}		rad/s/V
Phase detector gain			32		uA/rad

TIMING CHARACTERISTICS

(Digital output load capacitance Cl<15 pF, VCO frequency f_{VCO} <12.8 MHz, timing measurements for digital signals are measured at 1.3V, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
TDD, data delay				30	ns
TW, sync pulse width		40			ns
TSKW, SYNC to VCO skew		0		40	ns
SYNC fall time				20	ns
TADS, N or Q output settling time				260	ns
TADH, N or Q output hold time		0			ns

APPLICATIONS INFORMATION

A typical SSI 32H6210 application is shown in Figure 2. The selection criteria for the external components shown are discussed below.

INPUT AMPLIFIER

The autozero circuit is effectively a high pass filter, whose pole frequency is given by:

$$f_{AZ} = \frac{220}{C_{AZ}(\mu F)} Hz$$

With a value of 10 µF for C_{AZ}, the autozero circuit's corner frequency will be 22 Hz. This is sufficient for DC offset rejection and it will not interfere with the servo signal.

The AGC response may be characterized in terms of the open loop unity gain bandwidth of its control loop. The nominal value for this loop is set by C_{AGC} as follows:

$$f_{BW} = \frac{390}{C_{AGC}(\mu F)} Hz$$

For a nominal bandwidth of 10 kHz, C_{AGC} should be 0.039 µF. With a 1% capacitor, the variation in actual bandwidth will be +/- 50% due to the tolerance of internal components. The AGC peak detector capacitor should always be set to 1500 pF. This represents a reasonable tradeoff between leakage current tolerance and storage aperture time.

The pulse area detector storage capacitor must be chosen to keep the AGC circuit operating within its linear range. Its value is related to the VCO frequency as follows:

$$C_{AD} = \frac{620}{fvco(MHz)} pF$$, where fvco is the VCO freq.

Larger values for CAD are required with lower VCO frequencies in order to maintain constant signal levels within the device, since the integration time is increased.

$$K = 2\frac{V_{AGCADJ}(typ)}{VCC(min)} \qquad dv = \frac{\Delta V}{AGCADJGain(max)}$$

$$R1 = \frac{R_{AGC}(min)}{K}\left(\frac{V_{AGCADJ}(min)}{dv} - 1\right)$$

$$R2 = \frac{K}{1-K}(R1)$$

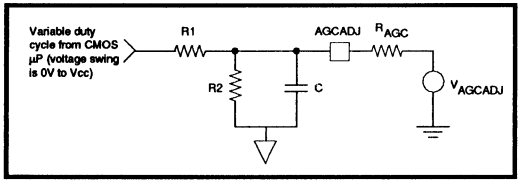

FIGURE 3: AGCADJ Input

for example if: $\Delta V = 0.4V$, $VCC = 5V \pm 5\%$, $Ta = 0\text{-}70°C$
$VREF = 5.4V \pm 6\%$

then: $K = .318$, $dv = 0.26V$, $R1 = 20.4k$,
$R2 = 9.5k$

The amplitude of N & Q signals can be adjusted using the AGCADJ input. If it is desired to adjust the N & Q amplitude by $\pm \Delta V$ volts, the values of R1 and R2 can be calculated from K and dv as shown in figure 3.

When R1 & R2 are calculated, a filter capacitor C is calculated from the replication rate of the µP duty cycle output. The parallel combination of R1, R2, R_{AGC} minimizes the ripple of V_{AGC}, and yet still provides sufficient response time to changes in duty cycle.

SYNC DETECTOR

Two sync detector parameters may be adjusted with external components. The first is the valid pulse threshold. The threshold is expressed as a percentage of a full scale pulse (since the sync detector follows the AGC and input amplitude variations are removed). The threshold is determined with resistor R_{TH} as follows:

$$Threshold = \frac{0.44}{R_{TH}(k\Omega)} \cdot 100(\%)$$

For example, a value of R_{TH} = 1.0 kΩ sets the valid pulse threshold at 44% of full scale. This prevents false triggering on noisy signals, but does not unduly shorten the sync pulse.

A timing window is used to detect sync pulses, since the sync and data pulses are more closely spaced than any other pulses in a valid servo signal. The delay from the zero crossing of the data pulse to the leading edge of the sync pulse is 1.5 cycles of the VCO clock. The next most closely spaced pulses (which must be rejected by the sync detect circuit) are separated by 3

APPLICATIONS INFORMATION (Continued)

SYNC DETECTOR (Continued)

VCO cycles. Thus the timing window should be set for 2 cycles of the VCO clock, to allow reliable detection of the sync pulse while suppressing false syncs. The timing window is determined as follows:

$$0.4\,(R_W \cdot C_W) + 43 \cdot 10^{-9}$$

The resistor Rw should always be set to 5.6 kΩ, which means that for a 2 cycle window, Cw is given by:

$$Cw = \frac{900}{fvco(MHz)} - 19pF$$

For a 12.8 MHz clock, Cw should be chosen as 51 pF.

LOCK DETECTOR

The LOCK detector behavior is controlled by the value of C_{LD}. A value too small will be prone to unlock prematurely and give false warnings to the system. A typical value for C_{LD} is 0.001µF.

PHASE LOCKED LOOP

The VCO center frequency is determined by Rvco and Cvco. Rvco should always be set to 11 kΩ ± 1%. Cvco may then be chosen by:

$$Cvco = \frac{830}{fvco} - 10.6\,pF,$$

where fvco is the desired center frequency in MHz.

For fvco = 12.8 MHz, Cvco = 54 pF and for fvco = 4 MHz, Cvco = 200 pF. If 1% tolerance external components are used, the VCO absolute frequency accuracy will be 15%. The VCO output frequency is related to the control voltage at the loop filter pin, V_{LF}, as follows:

$$fo/fvco = 1 + 1.667(V_{LF} - V_{BPI})$$

This means that the VCO gain, K_0, is given by:

$$K_0 = 2 \cdot \pi \cdot fvco(Hz) \cdot 1.667\ rads/s/V$$

The phase detector is a digitally controlled charge pump, which injects a current into the loop filter whose average value is proportional to the phase error. The detector gain, K_d, is fixed at 32 µA/rad. If a loop filter consisting of a series resistor and capacitor is used, as shown in Figure 2, the phase locked loop becomes a second order system with the following transfer function:

$$\frac{\text{phase error}}{\text{input phase}}(s) = \frac{(s/\omega n)^2}{1 + 2 \cdot \zeta \cdot s/\omega n + (s/\omega n)^2}$$

where:

$$\omega n\,(\text{natural freq.}) = \sqrt{((K_d \cdot K_0/(32 \cdot C_{L1}))}\ rad/s$$

$$\zeta(\text{damping factor}) = 0.5 \cdot R_L \cdot C_{L1} \cdot \omega n$$

As an example, the values for Cvco, R_L and C_L are

$$fvco = 12.8\,MHz,\ \omega n/(2 \cdot \pi) = 4600\,Hz,\ \zeta = 0.68$$

$$Cvco = \frac{830}{fvco} - 10.6 = 54pF$$

$$C_{L1} = \frac{K_d K_0}{32 \cdot \omega n^2} = \frac{(32 \cdot 10e-6)(10.47 \cdot f_{VCO})}{32(2 \cdot \pi \cdot 4600)^2} = .2\mu F$$

$$R_L = \frac{2 \cdot z}{C_{L1} \cdot \omega n} = 470\,\Omega$$

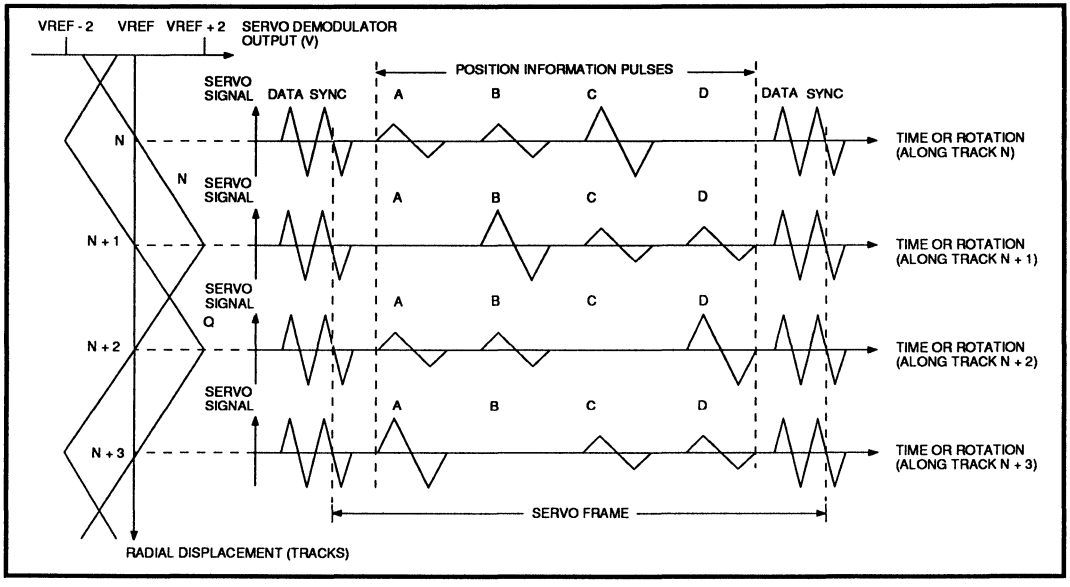

FIGURE 4: Pre-recorded Servo Signal and Servo Demodulator Output vs. Radial Displacement

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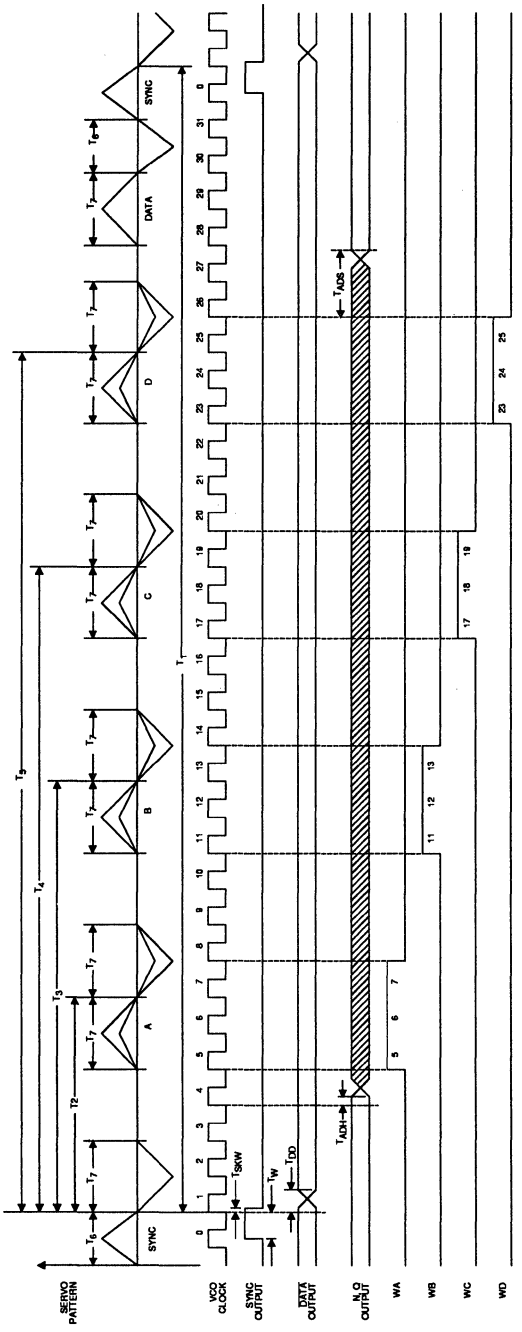

FIGURE 5: Timing Diagram

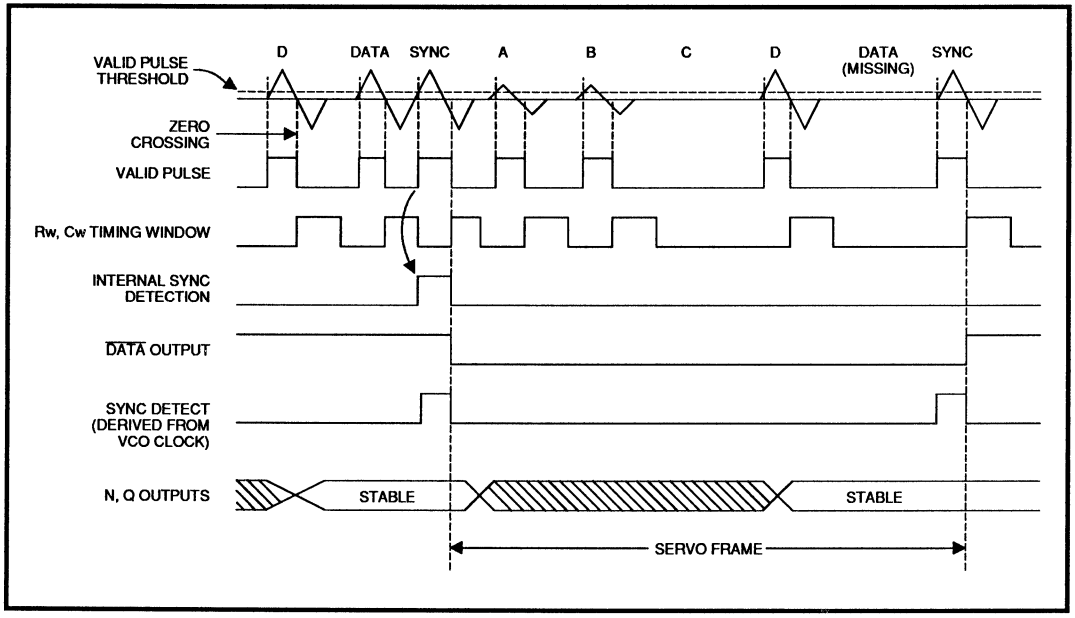

FIGURE 6 : Sync and $\overline{\text{DATA}}$ Pulse Detection

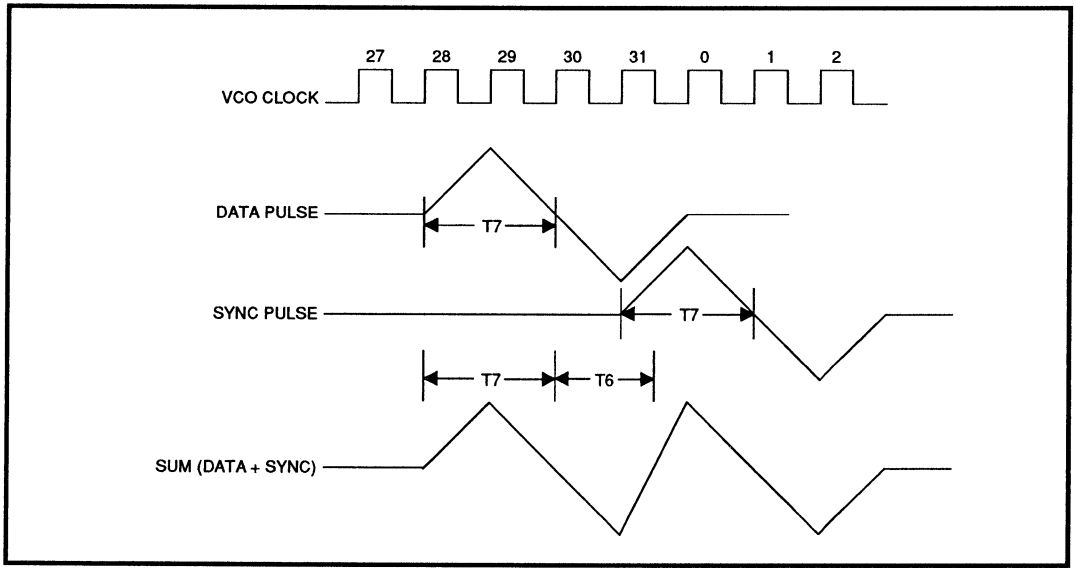

FIGURE 7 : Servo Writer Data-Sync Pulse Generation

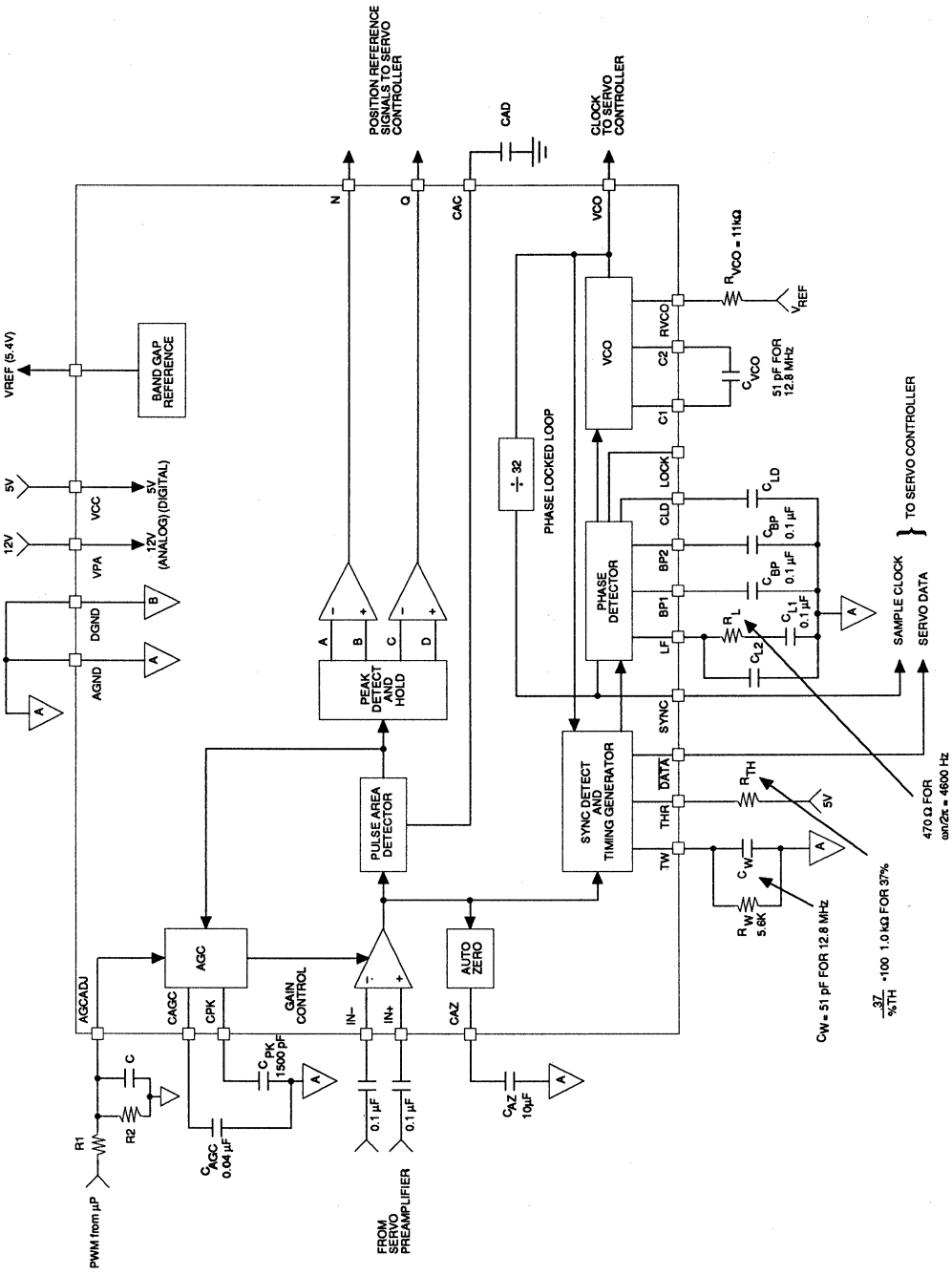

FIGURE 8: Design Example for 400 kHz Frame Rate

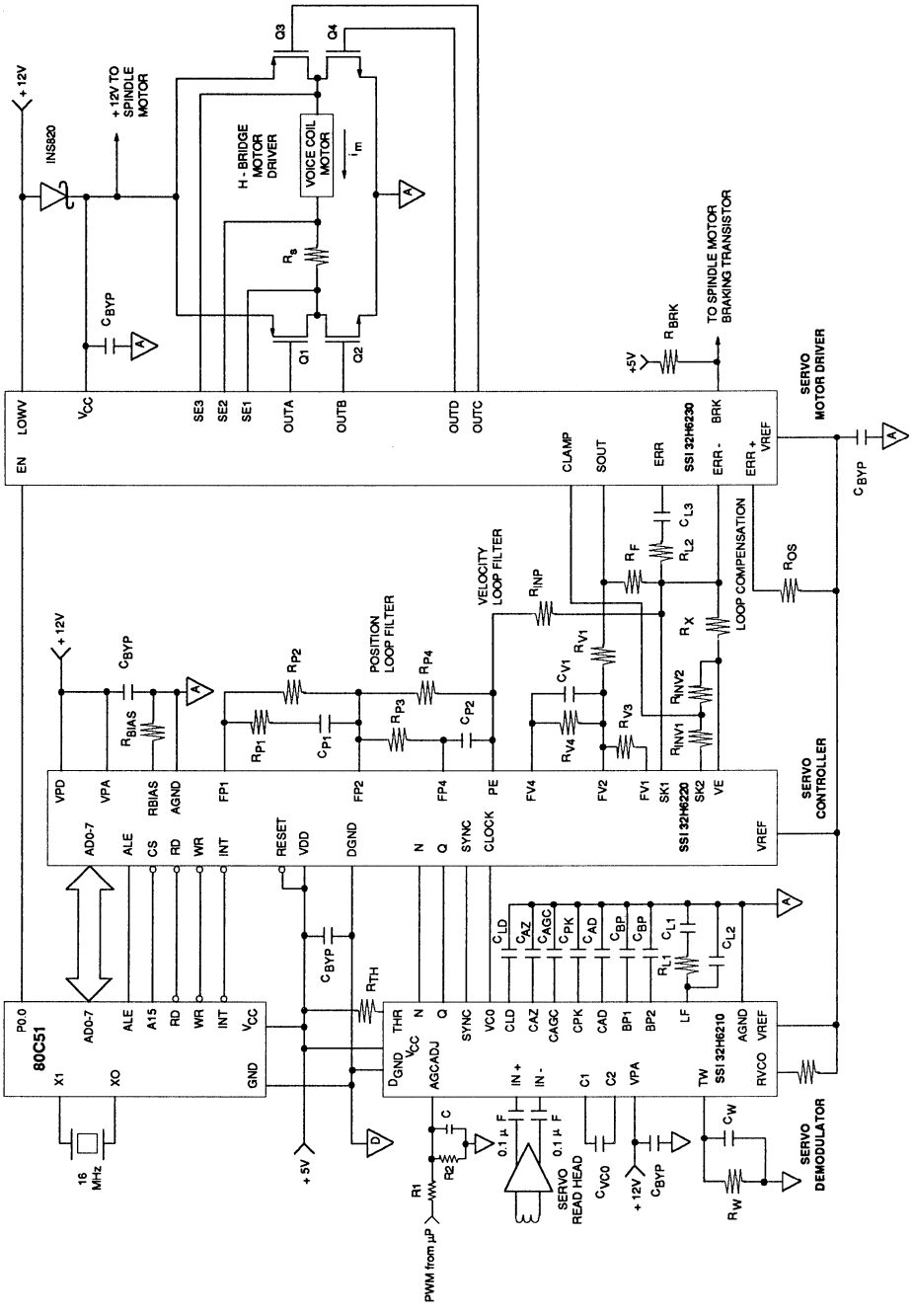

FIGURE 9: Complete Example of Servo Path Electronics Using SSI 32H6210/6220/6230 Chip Set

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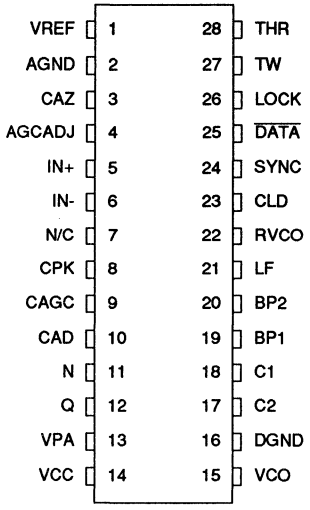
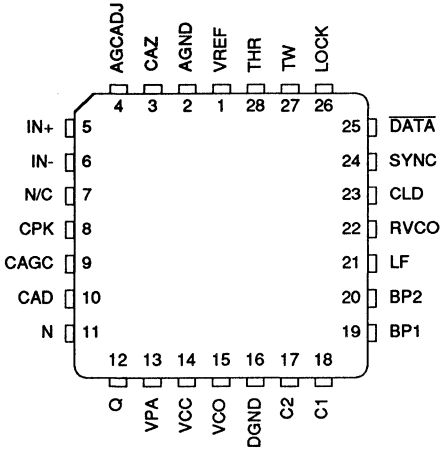
SSI 32H6210
Servo Demodulator

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



28-Pin DIP,SOL



28-Pin PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32H6210		
28-Pin DIP	32H6210-CP	32H6210-CP
28-Lead SOL	32H6210-CL	32H6210-CL
28-Lead PLCC	32H6210-CH	32H6210-CH

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 731-7110, FAX (714) 573-6914

silicon systems®
A TDK Group Company

SSI 32H6220
Servo Controller

Preliminary Data

December 1991

DESCRIPTION

The SSI 32H6220 Servo Controller is a CMOS device intended for use in Winchester disk drive head positioning systems. When used in conjunction with a position reference, such as the SSI 32H567 Servo Demodulator, and a motor driver, such as the SSI 32H569 or the SSI 32H6230 Servo Motor Driver, the device allows the construction of a high performance, dedicated surface, head positioning system which operates under microprocessor control.

The SSI 32H6220 generates position and track crossing information from standard normal and quadrature position signals, derived from a dedicated servo surface. In its seek mode the controller drives the actual head velocity towards a programmed target value, while in its track mode, it keeps the head centered on a track.

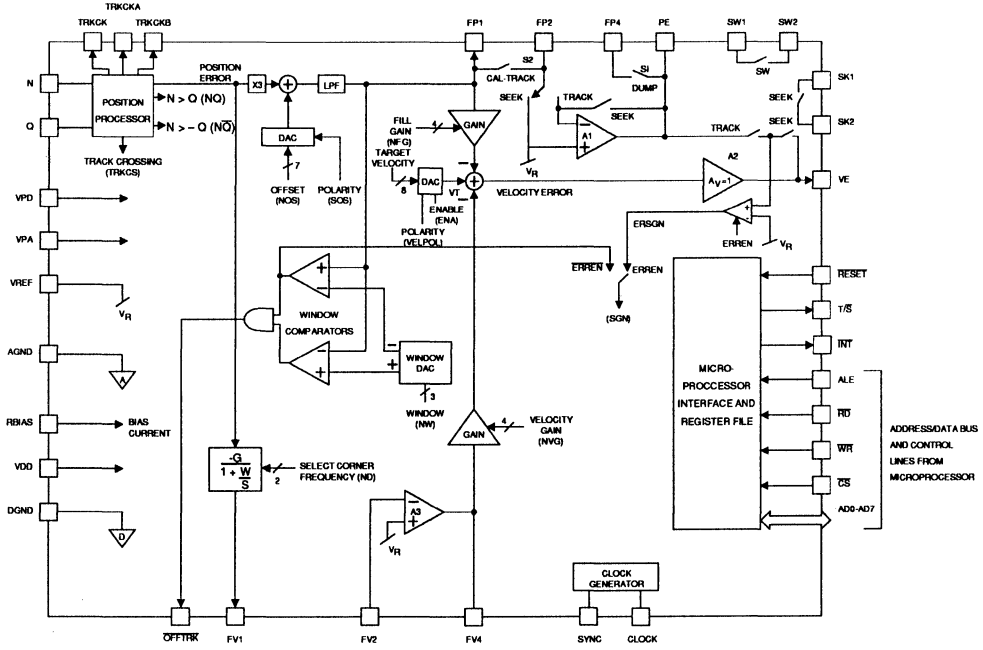
(Continued)

FEATURES

- **Servo control for Winchester disk drives with dedicated surface head positioning systems**
- **Accepts standard normal and quadrature position information**
- **500 kHz maximum servo frame rate**
- **Microprocessor bus interface compatible with 16 MHz 8051**
- **Seek and track modes**
- **Separate position and velocity error outputs**
- **Programmable velocity profile and loop gains**
- **Internal offset cancellation capability**
- **Track crossing output clock**
- **Low power CMOS design**
- **Available in a 44-pin PLCC package**

6

BLOCK DIAGRAM



DESCRIPTION (Continued)

Internal status and control registers allow a microprocessor to select operating modes, monitor track information and establish velocity targets. Digital outputs are available to monitor track crossings and head position accuracy. The microprocessor bus interface is optimized for use with multiplexed address/data bus microprocessors such as Intel's 8051, operating at up to 16 MHz.

The SSI 32H6220 is a low power, CMOS device and is available in a 44-pin PLCC package.

FUNCTIONAL DESCRIPTION

The SSI 32H6220 receives position information from a servo demodulator through the analog inputs N and Q, which are sampled on the falling edge of SYNC. FSYNC, the maximum SYNC frequency (which is the servo frame rate) is 500 kHz. The position processor compares the analog N signal with both Q and –Q, to generate the digital signals NQ and $N\overline{Q}$. Since the N and Q signals have a period of four tracks, NQ and $N\overline{Q}$ provide additional information over which track the head is positioned. Figure 6 shows the behavior of various position signals as radial displacement changes.

The 32H6220 is compatible with both hardware and software track counting techniques. The software track counter interface is bits NQ, $N\overline{Q}$, and TRKCS in the STATUS register. TRKCS can be programmed to pulse on each track crossing or on alternate track crossings. NQ and $N\overline{Q}$ provide information useful to "debounce" the TRKCS bit. Internal timing hysterisis prevents NQ, $N\overline{Q}$, and TRKCS from changing on successive frames. The hardware interface is TRKCK, an output clock intended to drive a hardware counter such as is available in the Intel 8051 family. TRKCK is a single frame pulse that occurs whenever a track boundary is crossed. During seek mode, TRKCK has one full track of hysteresis to prevent false counting. In track mode, hysteresis is removed.

The SSI 32H6220 has two modes of operation, track and seek, which are selected under microprocessor control. In the track mode, the control loop drives the position error signal to zero. In the seek mode, the loop attempts to match the head velocity to a velocity target programmed through the microprocessor interface.

In track mode, the head position error signal is summed with an 8-bit programmable offset signal which may be used to null out circuit offsets or to permit reading of off-track data. This adjusted position error signal is available on pin FP1. A lowpass filter with a corner frequency above 0.1 • FSYNC provides a small amount of smoothing. A position loop filter may be constructed from external RC components and amplifier A1. Switch S1, controlled by the DUMP bit, is used to keep the feedback capacitor in the position loop filter discharged while the controller is in seek mode. The output of A1 is the position error signal (PE) which should be connected to the servo motor driver circuitry. The adjusted position error (FP1) is also applied to a window comparator with programmable limits that provide a digital indication of whether the head is on track or not. In systems employing the SSI 32H569 or the SSI 32H6230, PE should be summed in to the ERR- pin through an input resistor.

In seek mode, the position error is differentiated by a switched capacitor differencer, to produce a velocity estimate. The differencer does not sample the position error immediately after the discontinuity that occurs when a track boundary is crossed. This prevents the discontinuity from disturbing the differentiator output. The velocity estimate is applied to a velocity loop filter consisting of external RC components and amplifier A3. A signal proportional to motor current may also be summed in at A3 to provide a better velocity estimate during rapid acceleration. A velocity error term is computed as the difference between the velocity target and the actual head velocity. The velocity target is generated by a DAC from the digital word stored in the TARGET register. The output of the velocity loop filter (pin FV4) is proportional to the actual head velocity and is scaled by a 4-bit programmable velocity gain before being subtracted from the velocity target. Also, a fill signal which is generated by multiplying the position error by a 4-bit programmable fill gain is subtracted from the velocity error. The fill signal compensates for the 8-bit quantization of the velocity target signal, which becomes a factor as the head velocity approaches zero. As the head nears the destination track at the end of a seek operation, the target velocity is zero, so if a fill term which is proportional to position error is subtracted from the velocity error term, the velocity loop will cause the head to come to rest at the center of the track. Without this additional fill signal, the velocity loop would not necessarily center the head in the destination track. The velocity error signal is buffered by A2

which drives the VE pin. The separate error outputs, PE and VE, allow for independent adjustment of the track and seek loop gains by specifying different values for RINP and RINV.

The actual velocity profile of the head is determined by the values written to the target velocity DAC. Typically, a new velocity target is written at each track crossing. An automatic update feature (enabled when UPDATE=1) causes the next velocity target to be loaded from a holding register when a track crossing occurs, so that the microprocessor does not have to perform this time-critical operation.

The 32H6220 is capable of interactively nulling out offsets at FP1, PE, and VE. The basic technique is to use the low offset ERR comparator (enable with the ERREN bit and visible on the SGN bit) to monitor the offset and then adjust an appropriate DAC value. Offset at FP1 is nulled with the NOS DAC, offset at PE is nulled with the TARGET DAC, and offset at VE is nulled with either NOS or TARGET.

The SSI 32H6220 has 8 registers, described in "Register Description," which are accessed through a microprocessor interface optimized for multiplexed address/data bus processors. A 3-bit register address is latched from the bus on the falling edge of ALE (address latch enable) and a bus cycle occurs if $\overline{CS}$ (chip select) and either $\overline{RD}$ (read strobe) or $\overline{WR}$ (write strobe) are asserted. An open drain interrupt line ($\overline{INT}$) may be used to cause a microprocessor interrupt when a track crossing occurs.

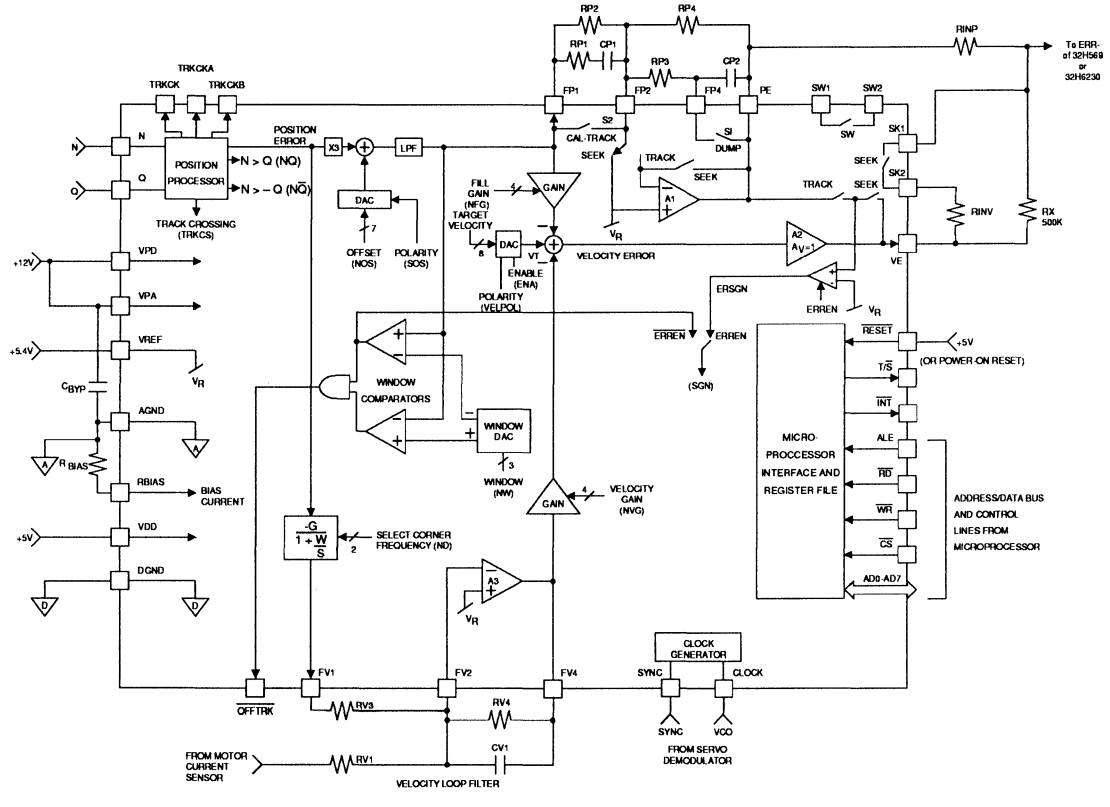


FIGURE 2: SSI 32H6220 Typical Application

PIN DESCRIPTION

POWER

NAME	44-pin PLCC	TYPE	DESCRIPTION
RBIAS	16	I	BIAS INPUT - This input sets the internal opamp bias currents. A 20 kΩ 1% resistor should be connected between RBIAS and AGND.
VREF	17	I	REFERENCE VOLTAGE - 5.4V input which is used as the DC reference level for all analog signals. (This level is available as an output from the SSI 32H567).
AGND	19		ANALOG GROUND
DGND	27		DIGITAL GROUND
VDD	28		DIGITAL 5V SUPPLY - 5 volt supply for the microprocessor interface circuitry.
VPD	43		DIGITAL 12V SUPPLY - 12 volt supply for the switched capacitor filter clocks.
VPA	44		ANALOG 12V SUPPLY - 12 volt supply for all analog circuitry.

POSITION REFERENCE INTERFACE

Q	14	I	QUADRATURE INPUT - Analog position signal from servo demodulator.
N	15	I	NORMAL INPUT - Analog position signal from servo demodulator (90 degrees or 1 track out of phase with Q signal).
SYNC	40	I	SYNC INPUT - The falling edge of this clock causes the analog information on the N, Q inputs to be sampled. There is one SYNC pulse per servo frame and the maximum rate is 500 kHz. This signal is generated by the SSI 32H567. If it is not necessary to synchronize to N and Q samples, and FRFMT is set, SYNC should be grounded. In this case, FSYNC will be internally generated as FCLOCK/32.
CLOCK	41	I	CLOCK INPUT - This clock must be either 32 or 72 times the rate of the SYNC clock (selected by the FRFMT bit in STATUS register). It is usually supplied by the VCO output of the servo demodulator (e.g., SSI 32H567).
TRKCK	33	O	TRACK CROSSING CLOCK - This output drives external hardware track counters and is compatible with the counter function available in the Intel 8251 family of microcontrollers. It is normally low and pulses high one cycle per track.
TRKCKA	20	O	TRACK CROSSING A - This output is derived from TRKCK, it toggles on the rising edges of TRKCK.
TRKCKB	25	O	TRACK CROSSING B - This output is derived from TRKCK, it toggles on the falling edges of TRKCK.

MICROPROCESSOR INTERFACE

$\overline{CS}$	21	I	CHIP SELECT - Active low signal enables device to respond to microprocessor read or write.
ALE	22	I	ADDRESS LATCH ENABLE - Falling edge latches register address from pins AD0-AD2.
$\overline{RD}$	23	I	READ STROBE - Active low signal causes the contents of the addressed register to be placed on the address/data bus (AD0–7) if $\overline{CS}$ is also active.
$\overline{WR}$	24	I	WRITE STROBE - Active low signal causes the data on the address/data bus to be written to the addressed register if $\overline{CS}$ is also active.
$\overline{INT}$	29	O	INTERRUPT - This active low open drain output is asserted when a track crossing is detected. It is released when the internal track crossing status bit (TRKCS) is read by the microprocessor.
T/$\overline{S}$	30	O	TRACK/SEEK - This output reflects the state of the T/$\overline{S}$ bit in the STATUS register. It is high when the device is in track mode and low when it is in seek mode.
AD7 -AD0	31-32 34-39	I/O	ADDRESS/DATA BUS - 8-bit bus which carries register address information and bi-directional data.
$\overline{RESET}$	42	I	RESET - This active low input is used to force all the internal registers to their reset condition.
$\overline{OFFTRK}$	26	O	OFFTRACK - This open drain output is asserted whenever the head position is outside the window specified by NW. It is always asserted in seek mode.

CONTROL LOOP

FV4	1	O	VELOCITY FILTER OUTPUT - This is the output of amplifier A3 which forms part of the velocity loop filter. This signal is internally amplified and compared to the target velocity.
FV2	4	I	VELOCITY FILTER INPUT - Direct connection to the inverting input of amplifier A3.
FV1	7	O	ESTIMATED VELOCITY OUTPUT - Output of the position error differentiating high pass filter.
VE	9	O	VELOCITY ERROR - This signal should be summed in to the servo motor driver circuitry. In systems using the SSI 32H569 or the SSI 32H6230 servo driver, VE is connected to the ERR- pin through a resistor.
SW1, SW2	2	3	UNCOMMITTED SWITCH - This switch can be used to reset a notch filter during seek mode. The switch is controlled by the SW bit in the status word.
SK1, SK2	5	6	UNCOMMITTED SEEK SWITCH - This switch is on during seek operations.

CONTROL LOOP (Continued)

NAME	44-pin PLCC	TYPE	DESCRIPTION
FP4	11	O	POSITION FILTER CAPACITOR - The external position loop filter feedback capacitor should be connected between this pin and PE. When the DUMP bit in register WINDOW is set, an internal switch (S1) shorts PE to FP4. This allows the external capacitor to be kept discharged during seek mode.
PE	10	O	POSITION ERROR OUTPUT - Output of position loop filter amplifier A1.
FP2	12	I	POSITION FILTER INPUT - Inverting input to opamp A1.
FP1	13	O	POSITION ERROR OUTPUT - Offset-corrected output of the position processing circuitry, which is proportional to the radial displacement of the head from the center of the current track.
The actual transfer function from N, Q to FP1 is: $H(z) = \frac{3}{2z-1}\frac{\sin(\omega T/2)}{\omega T/2}$ where: $T = 1/FSYNC$ $z = e^{sT}$			
This transfer function exhibits a high frequency roll off with a 3 dB point at f = 0.11 FSYNC.			
Unused pins on PLCC package: 8, 18			

REGISTER DESCRIPTION

The SSI 32H6220 has 8 internal registers which contain status, control and loop parameter information. A three bit register address is latched from inputs AD0-AD2 on the falling edge of ALE. The corresponding register is accessed if $\overline{CS}$ is then asserted, with the direction of access being determined by $\overline{RD}$ or $\overline{WR}$. The registers are summarized in Figure 3.

REGISTER	ADDRESS	ACCESS	D7	D6	D5	D4	D3	D2	D1	D0
GAIN	0	READ/ WRITE	NFG				NVG			
TARGET	1	READ/ WRITE	TARGET VELOCITY							
NEXT	2	READ/ WRITE	NEXT TARGET VELOCITY							
VELCON	3	READ/ WRITE	UNUSED			ND		UPDATE	ENA	VELPOL
WINDOW	4	READ/ WRITE	CAL	UNUSED	DUMP	T/$\overline{S}$	ERREN	NW		
STATUS	5	AS NOTED	SGN (READ ONLY)	SW (READ/WRITE)	CSMOD (READ/WRITE)	FRFMT (READ/WRITE)	ONTRK (READ ONLY)	NQ (READ ONLY)	$\overline{NQ}$ (READ ONLY)	TRKCS (READ ONLY)
OFFSET	6	READ/ WRITE	SOS	NOS						
RESET	7	WRITE ONLY	RESET (ANY VALUE)							

FIGURE 3: SSI 32H6220 Register Map

REGISTER DESCRIPTION (Continued)

GAIN **Address 0** **Read/Write**

GAIN SETTINGS - Used to set the velocity gain and fill gain. These settings are only significant in the seek mode.

BIT	NAME	DESCRIPTION
3-0	NVG0-3	VELOCITY GAIN - 4-bit quantity which sets the gain applied to the velocity signal at the output of opamp A3.
7-4	NFG0-3	FILL GAIN - 4-bit quantity which sets the gain applied to the position error which is added to the velocity signal.

If NVG and NFG are represented as integers ranging from 0 to 15, then for a zero velocity target, the VE output is given by:

$$VE - VREF = \frac{NVG}{15}(FV4 - VREF) + \frac{NFG}{255}(FP1 - VREF)$$

TARGET **Address 1** **Read/Write**

CURRENT VELOCITY TARGET - This register selects the 8-bit velocity target which is subtracted from the actual velocity to yield velocity error in seek mode. The sign of the velocity target is determined by the VELPOL bit in register VELCON. If TARGET is represented as an integer from 0 to 255, then the voltage at the output of the velocity target DAC, VT, is given by:

$$VT = VREF\left(1 - \frac{TARGET}{340}\right), VELPOL = 0$$

$$VREF\left(1 + \frac{TARGET}{340}\right), VELPOL = 1$$

The SSI 32H6220 has an update feature which allows this register to be loaded automatically with the contents of the next target register when a track crossing occurs. The target register may also be written directly by the microprocessor to cause an immediate change in target velocity.

NEXT **Address 2** **Read/Write**

NEXT TARGET VELOCITY - This register contains an 8-bit value that will be loaded automatically into the velocity target register when a track crossing occurs, if the UPDATE bit in VELCON is set. This register is unused if UPDATE is cleared.

REGISTER DESCRIPTION (Continued)

VELCON Address 3 Read/Write

BIT	NAME	DESCRIPTION
0	VELPOL	VELOCITY TARGET POLARITY - If this bit is set, the velocity target will be positive (with respect to VREF) and if it is reset, the velocity target will be negative.
1	ENA	ENABLE VELOCITY TARGET DAC - If ENA is set, the velocity target DAC will be enabled and if it is cleared the output of the DAC will be clamped to VREF.
2	UPDATE	UPDATE MODE SELECT - When this bit is set, the contents of the NEXT register will be transferred to TARGET automatically when a track crossing occurs. If it is cleared, new velocity targets must be written directly to the TARGET register by the microprocessor.
3-4	ND0-ND1	DIFFERENTIATOR CHARACTERISTIC SELECT - These bits select the characteristic of the differentiator high pass filter as follows: $H(s) = \frac{-G}{1 + \frac{W}{s}}$ $W = \frac{1}{2T}\left(1 + \frac{ND}{1.75}\right)$ rad/s $G = 8.2$ Where T is the period of the SYNC clock input in seconds, s is the complex frequency variable in radians/second and ND is an integer from 0 to 3. For s<<W the high pass filter H(s) acts like a differentiator. For a SYNC rate of 500 kHz, the corner frequency W will be: ND1 | ND0 — W/2π (kHz) 00 — 39.8 01 — 62.5 10 — 85.3 11 — 108
		The actual transfer function from N, Q, to FV1 is: $H(z) = \frac{7G(z-1)}{z[7(z-1)+(3.5+2ND)z]} \frac{\sin(\omega T/2)}{\omega T/2}$ where: $T = 1/FSYNC$ $z = e^{sT}$ This transfer function is approximated throughout this data sheet with the above s domain approximation which is accurate to 0.5 db for f< .05 • FSYNC.
5-7	unused	

REGISTER DESCRIPTION (Continued)

WINDOW Address 4 Read/Write

WINDOW CONTROL - This register is used to program the on-track window comparator and also contains several control bits.

BIT	NAME	DESCRIPTION
0-2	NW0-NW2	WINDOW SELECT BITS - This 3 bit word selects the window comparator threshold voltage. The on track indicator bit will be true as long as: $\|FP1 - VREF\| < VREF[(1 + NW)/32]$ where NW is an integer from 0 to 7.
3	ERREN	ERROR ENABLE - When set, this bit enables the offset comparator and causes SGN to be its output. When reset, SGN is the lower side of the window comparator.
4	T/$\overline{S}$	TRACK/SEEK MODE SELECT - When this bit is set, track mode is selected and when it is reset, seek mode is selected.
5	DUMP	POSITION LOOP FILTER DUMP CONTROL - When this bit is set, pins PE and FP4 are switched together internally by S1. This causes the external position loop filter feedback capacitor to be discharged.
6	unused	
7	CAL	CALIBRATION MODE - When this bit is reset, the N and Q inputs are connected to the position processor and normal operation occurs. When CAL is set, the processor inputs are connected to VREF, causing the FP1 output to reflect the offset voltage errors in the position sensing path.

STATUS Address 5 Read/Write access as noted

STATUS REGISTER - Contains track status information and several control bits.

BIT	NAME	DESCRIPTION
0	TRKCS	TRACK CROSSING INDICATOR - The function of TRKCS is determined by the CSMOD bit in this register. When CSMOD is set, TRKCS will be set every time NQ or N$\overline{Q}$ change state (i.e., on every track crossing). When CSMOD is reset, TRKCS will be set every time NQ changes state (i.e., on alternate track crossings). TRKCS is reset when STATUS is read by the microprocessor. The $\overline{INT}$ interrupt output is the inverse of TRKCS. (TRKCS is read only.)
1	N$\overline{Q}$	TRACK QUADRANT - This bit is set when: N-VREF > VREF-Q and reset otherwise. (N$\overline{Q}$ is read only)
2	NQ	TRACK QUADRANT - This bit is set when: N-VREF > Q-VREF and reset otherwise. (NQ is read only)

REGISTER DESCRIPTION (Continued)

BIT	NAME	DESCRIPTION
3	ONTRK	ON TRACK INDICATOR - This bit is set when the voltage on pin FP1 is within the window selected by the WINDOW register. It is reset otherwise (ONTRK is read only).
4	FRFMT	FRAME FORMAT - Used to indicate the relationship between CLOCK and SYNC. If this bit is set, the VCO clock rate must be 32 times the SYNC clock rate. If it is reset, the VCO clock rate must be 72 times the SYNC clock rate. (FRFMT is read/write).
5	CSMOD	CROSSING INDICATOR MODE - If this bit is reset, TRKCS will be set on alternate track crossings. If it is set, TRKCS will be set on every track crossing. (CSMOD is read/write).
6	SW	SWITCH - This bit controls the SW switch. This uncommitted switch can be used to initialize a notch filter in the servo loop. (SW is read/write).
7	SGN	VOLTAGE SIGN - This bit indicates whether the head position is above or below the lower edge of the track window. If used with the ONTRK bit, it allows the microcontroller to divide a track into three regions and make more informed decisions about overshoot and undershoot. When ERREN is set, SGN is the output of the error comparator. (SGN is read only).

OFFSET **Address 6** **Read/Write**

OFFSET VOLTAGE REGISTER - The 8-bit value in this register drives the offset DAC which adds a correcting voltage to the position error signal.

BIT	NAME	DESCRIPTION
0-6	NOS0-NOS6	OFFSET MAGNITUDE
7	SOS	OFFSET SIGN

The offset correction voltage, VOS, is given by:

$$VOS = -0.89 \left(\frac{NOS}{127}\right) V \text{ , } SOS=0$$

$$0.89 \left(\frac{NOS}{127}\right) V \text{ , } SOS=1$$

RESET **Address 7** **Write only**

RESET REGISTER - When any value is written to this register, all writeable register bits in the SSI 32H6220 are reset.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

(Maximum limits indicate where permanent device damage occurs. Continous operation at these limits is not intended and should be limited to those conditions specified in the DC operating characteristics.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VPA		0		14	V
Voltage on any pin		0		VPA+0.1V	V
Storage Temp.		-45		165	°C
Solder Temp.	10 sec duration			260	°C

RECOMMENDED OPERATION CONDITIONS (Unless otherwise noted, the following conditions are valid throughout this document.)

VPA, VPD		10.8		13.2	V
VDD		4.5		5.5	V
VREF		5.1	5.4	5.7	V
Operating temp.		0		70	°C
RBIAS, bias resistor to AGND		22.3	22.6	22.9	kΩ
Resistive loading (FP1, FV1, PE, FV4, VE)	About VREF	5			kΩ
Capacitive loading (FP1, FV1, PE, FV4, VE)				40	pF

DC CHARACTERISTICS

IVP	Total VPA and VPD current				40	mA
IDD	VDD current				10	mA
IREF	VREF current				3	mA

DIGITAL I/O

Digital Inputs					
VIH	|IIH| < 10µA	2			V
VIL (Except Reset)	|IIL| < 10µA			0.7	V
VIL Reset Pin	|IIL| < 100µA			0.7	V
Digital Outputs (AD0-AD7, T/$\overline{S}$)					
VOH	|IOH| < 40µA	2.4			V
VOL	|IOL| < 1.6mA			0.4	V
Open Drain Digital Outputs ($\overline{INT}$, $\overline{OFFTRK}$)					
VOL	|IOL| < 1.6mA			0.4	V
Off leakage	VOH = VPD			10	µA

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MICROPROCESSOR INTERFACE TIMING (see figure 4(a) and figure 4(b)). (Timing measurements for digital signals are measured at 1.3V, unless otherwise noted.)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
TLHLL	ALE pulse width		45			ns
TAVLL	Address setup time		8			ns
TLLAX	Address hold time		20			ns
TRLVD	$\overline{RD}$ to data valid				145	ns
TRHDX	data hold time after $\overline{RD}$		0		50	ns
TRLRH	$\overline{RD}$ pulse width		200			ns
TLLWL	ALE to $\overline{RD}$ or $\overline{WR}$		25			ns
TRLCL	$\overline{RD}$ or $\overline{WR}$ to $\overline{CS}$ low				20	ns
TRHCH	$\overline{RD}$ or $\overline{WR}$ to $\overline{CS}$ high		10			ns
TWLWH	$\overline{WR}$ pulse width		100			ns
TQVWH	data set up to $\overline{WR}$ high		70			ns
TWHQX	data hold after $\overline{WR}$ high		10			ns

ANALOG I/O

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
N, Q Inputs						
Input resistance			50			kΩ
Input capacitance					25	pF
Offset voltage			-15		15	mV
N, Q Timing (see figure 5)						
fc	VCO input frequency		4		16	MHz
TSYH	SYNC hold time		0			ns
TSYS	SYNC setup time		34			ns
Nc	VCO/SYNC	FRFMT=1	32		32	
	frequency ratio	FRFMT=0	72		72	
TADS	N or Q analog setup time		400			ns
TADH	N or Q analog hold time		180			ns

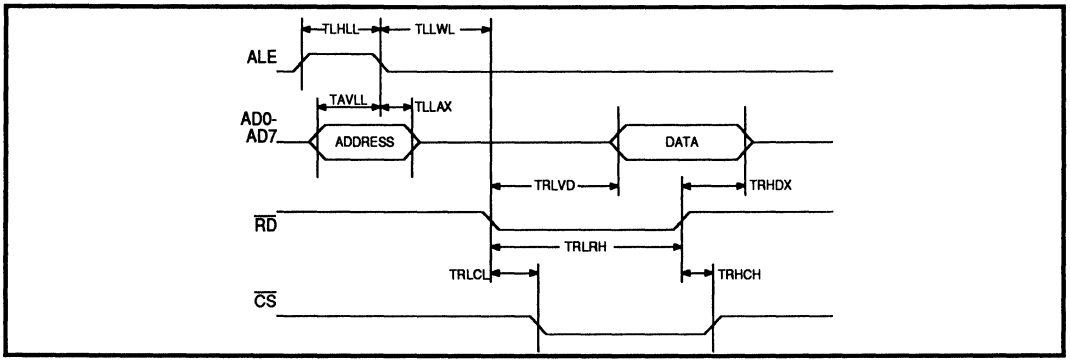

FIGURE 4(a): Read Cycle Timing

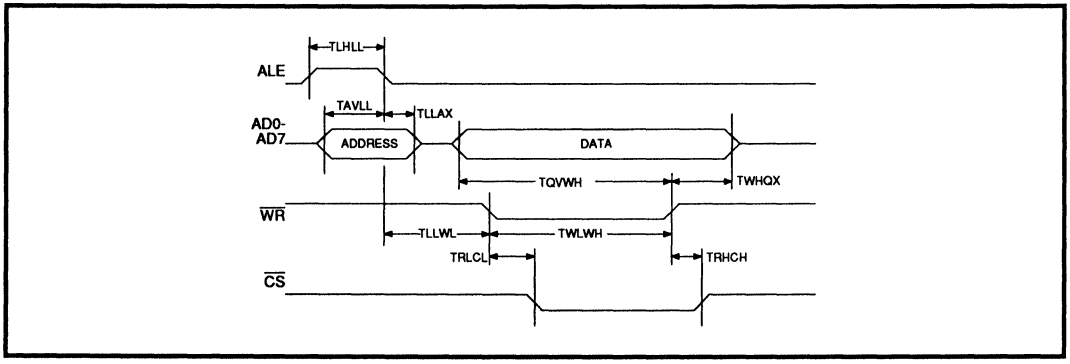

FIGURE 4(b): Write Cycle Timing

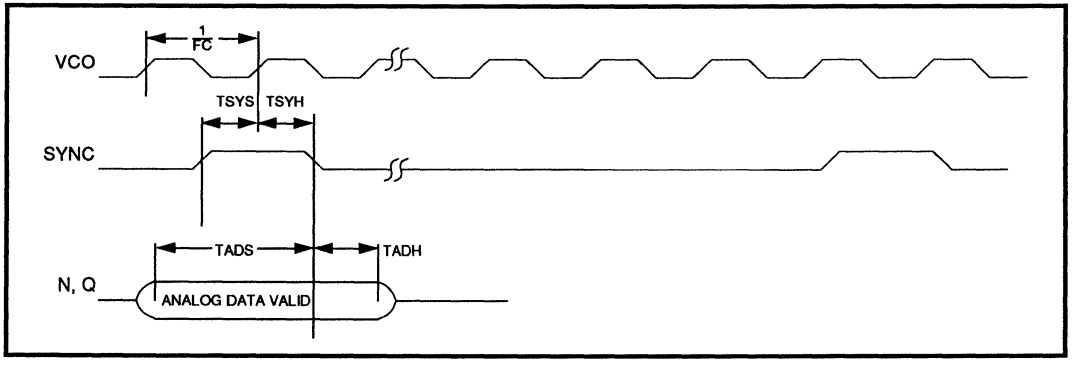

FIGURE 5: Analog Timing

ANALOG I/O (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
FP2, FV2 Inputs					
Input resistance	About VREF	100			kΩ
Input capacitance				20	pF
Offset voltage		-15		15	mV
Analog Outputs					
Output impedance	|Vo-VREF| < 3V			20	Ω
Output swing (FP1, FV1)	About VREF	4			V
Output swing (PE, FV4)	About VREF	3.5			V
Output swing (VE)	About VREF	3.7			V
Gain (FP1 from N or Q)		9.35	9.55	9.75	dB
Gain (Amplifier A1, A3)	Open loop DC gain	60			dB
Gain (Amplifier A2)			0		dB
Unity gain bandwidth (Amplifier A1, A3)	Open loop	1			MHz
Unity gain bandwidth (Amplifier A2)	Open loop		.5		MHz

WINDOW COMPARATOR

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Threshold step size accuracy	Nominal=VREF/32	-30		30	%

FILL GAIN

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum gain	NFG=15	57	58	60	mV/V
Gain step size		3	4	5	mV/V

ANALOG SWITCHES

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
S1	PE ≤ VREF			200	Ω
SW	SW2 ≤ VREF			200	Ω
SK	SK1 ≤ VREF			200	Ω
S2	FP1 ≤ VREF			1500	Ω

VELOCITY GAIN

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum gain	NVG=15	.97	1	1.03	V/V
Gain step size		48	67	82	mV/V

TARGET VELOCITY DAC

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Full scale - VREF	VELPOL=1	72	75	78	%VREF
	VELPOL=0	-72	-75	-78	%VREF
Step size		0.16	0.29	0.50	%VREF
Offset Match (VELPOL=1)- (VELPOL=0)	TARGET=0	0		35	mV

OFFSET CORRECTION DAC

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Full scale - VREF	NOS=127, SOS=1	15	16	18	%VREF
	NOS=127, SOS=0	15	16	18	%VREF
Step size		0.08	0.13	0.18	%VREF

DIFFERENTIATOR

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
High pass gain (N,Q TO FV1)	FIN/FSYNC = 0.02,				
	ND = 0	5.45	5.85	6.25	db
	ND = 1	1.7	2.1	2.5	db
	ND = 2	-.9	-.5	-.1	db
	ND = 3	-2.9	-2.5	-2.1	db

APPLICATIONS INFORMATION

In the examples shown in Figures 7a & 7b, the SSI 32H6220 is used with its companion devices, the SSI 32H567 and SSI 32H569 or SSI 32H6230, as well as a microprocessor and some external components, to implement a complete head positioning system.

Position Reference

The position feedback signal for the servo loop is generated by a servo demodulator from information prerecorded on the disk drive's servo surface. The SSI 32H567 provides quadrature position signals (N and Q), recovered clocks (SYNC and VCO) and an analog reference level (VREF) for the rest of the system. The SSI 32H567 translates the radial displacement of the servo read head to a voltage with a gain of 2 volts/track. The SSI 32H6220 has a front end gain of 3, so the gain from actual position error to the voltage at pin FP1 (the input to the position loop filter) is 6 volts/track.

In order to produce the position error signal illustrated in figure 6, the position processor in the SSI 32H6220 selects either N, Q or an inverted signal, based on the value of the digital signals NQ and $N\overline{Q}$. The resulting error signal is zero (equal to VREF) when the head is perfectly centered on a track. The error signal has a maximum absolute value in the vicinity of a track boundary (i.e., when the head is displaced one half track from a track center) and has a polarity that indicates the direction of the position error.

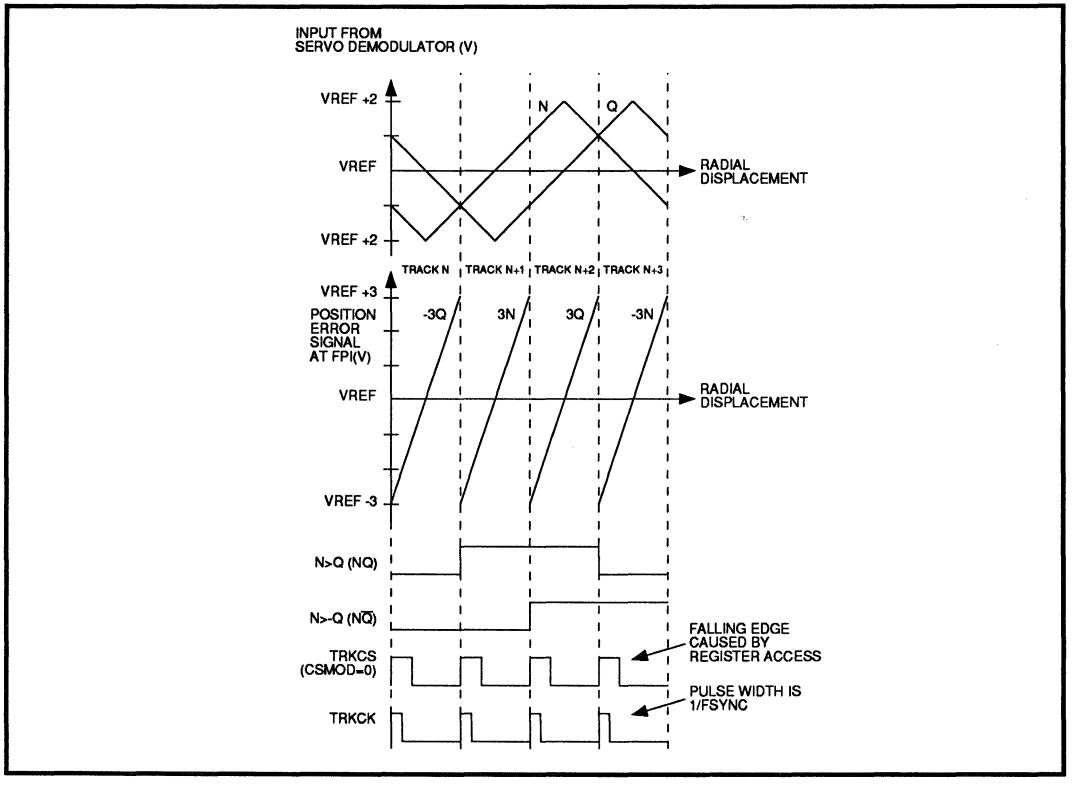

FIGURE 6: Position Signal Waveforms

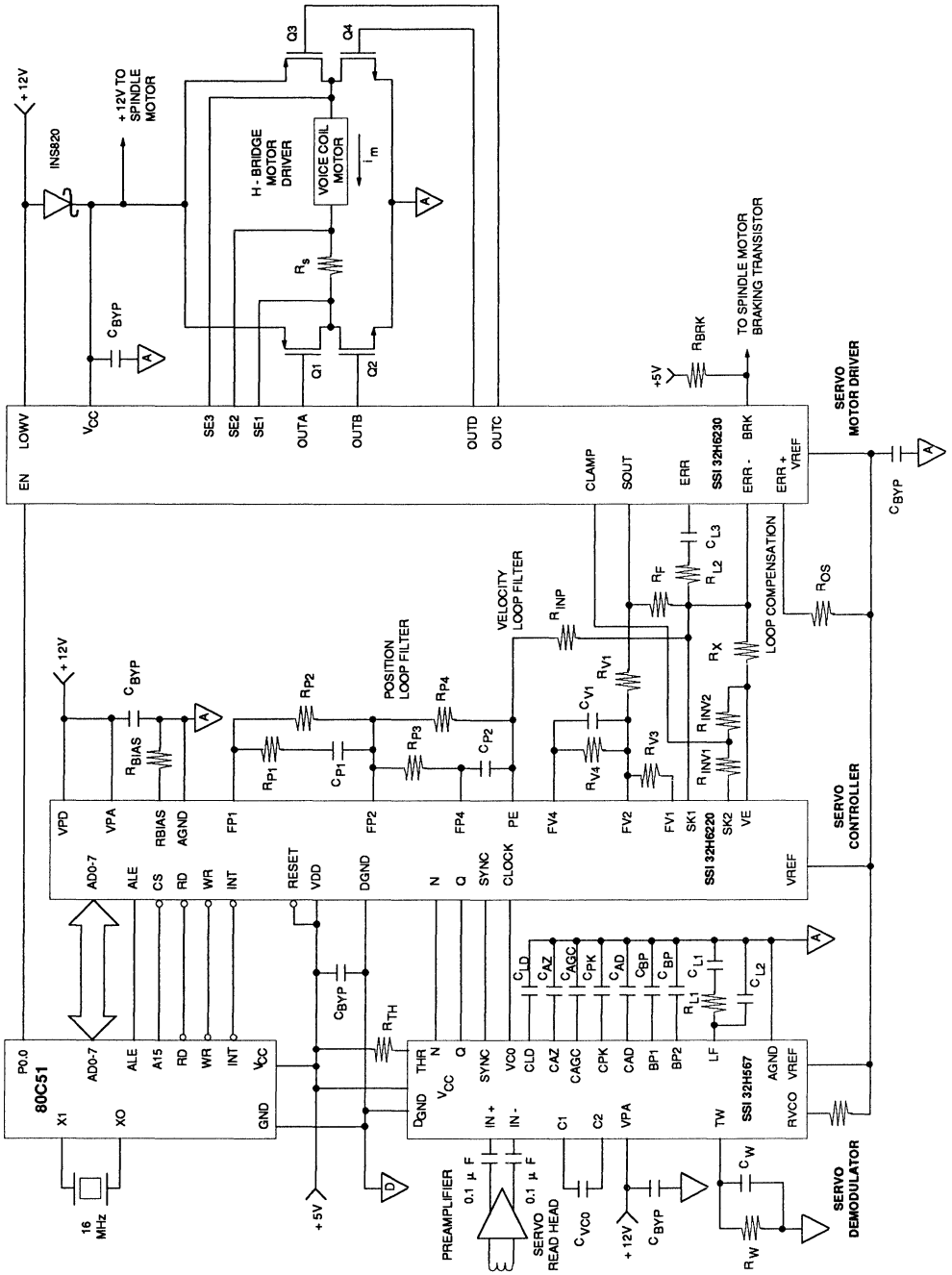

FIGURE 7: Complete Example of Servo Path Electronics Using SSI 32H567/6220/6230 Chip Set

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Servo Motor and Driver

For the purposes of illustration, the following simple model for the servo motor in Figure 7 is assumed.

$$i_m = \frac{J\theta}{K_m} \cdot \frac{d\omega}{dt} \qquad e = K_e \cdot \omega$$

Definition of terms:

im	Armature current (A)
ω	Motor speed (rad/s)
Jθ	Rotor moment of inertia (kg • m²)
Km	Torque constant (Nm/A)
e	Motor back EMF (V)
Lm	Winding inductance (H)
Rm	Winding resistance (Ohm)
Ke	Motor voltage constant (V/rad/s)

Numerically, Ke and Km are equal.

Under the assumption that the electrical and mechanical poles of the motor above are widely separated ($Rm/Lm >> J\theta \cdot Rm/Km^2$), the servo driver loop compensation components, R_{L2} and C_{L3}, may be chosen to cancel the effect of Lm, as follows:

$$C_{L3} = \frac{68\,R_S}{2\pi R_F\,(R_m + R_S)\,BW}, \quad R_{L2} = \frac{L_m}{C_{L3}(R_m + R_S)}$$

where BW is the desired servo driver open loop bandwidth (Hz). This results in the following relationship between motor current (im) and error voltage at the servo controller output (EOUT).

$$\frac{i_m}{EOUT}(s) = \frac{-R_F}{4\,R_{in}\,R_S\left(1 + \frac{s}{2\pi BW}\right)}$$

Where Rin is either Rinp or Rinv depending whether you're in seek or track modes.

This simple first order approximation of the servo motor behaviour neglects effects such as resonance due to the motor inductance, Lm, or the pole due to servo driver transconductance. However, it is sufficient to illustrate the design goals for the velocity and position loop filters that are required with the SSI 32H6220. A more detailed description of the SSI 32H569 may be found in the SSI 32H569 data sheet.

TRACK MODE

Loop Compensation

Track mode is engaged when the head has reached its destination and the current position must be maintained. The control objective is to drive the position error signal at FP1 to zero and minimize excursions of the head due to noise and other perturbations of the system. The transfer function of the complete servo loop in track mode is shown in figure 8(a), using the servo motor model derived above. The gain G1 is the combined effect of the SSI 32H567 and the front end gain of the SSI 32H6220, and has a nominal value of 6 volts/track. The gain G2 is a property of the head transport system, and has units of tracks/radian for rotary servo motors and tracks/meter for linear motors. (The nomenclature chosen for the motor model is that of rotary motors but the results are applicable to linear motors as well, if appropriate units are substituted). To ensure that the control loop has negative feedback, positive motor current (as indicated in Figure 7) must result in negative motor acceleration. This inversion is accomplished in the prerecorded servo pattern and is accounted for in the transfer function by showing G2 to be negative.

Since the servo driver/motor combination has a double pole at the origin and an additional real pole at frequency BW (which is selectable with external components in the SSI 32H569), the position loop filter is essential to ensure a stable system. The effect of the position filter used in this example is to provide lag-lead compensation. Systems of this type are usually designed by trial and error, but a further simplification of the transfer function may be made to obtain an initial solution. If the pole at BW is ignored, RP4 is removed and RP2 made large (RP2 is necessary to provide a DC path for leakage current at pin FP2) then the system illustrated in figure 8(b) is obtained. The compensation has been reduced to lead compensation only. If the following quantities are defined:

$$Gtot = \left(\frac{G_1 G_2 C_{P1}}{C_{P2}}\right)\left(\frac{R_F}{4R_{in}R_S}\right)\left(\frac{K_m}{J\theta}\right)(S^{-2})$$

PM = Desired closed loop phase margin (degrees)

FB = Desired open loop unity gain bandwidth (rad/s)

then appropriate values for the time constants of the

lead compensation circuit (T_1, T_2) may be chosen using the following relationships, assuming $1/T_2 << FB << 1/T_1$:

$$FB = Gtot \cdot T_2 \text{ (rad/s)}$$

$$PM = 90 - \arctan (FB \cdot T_1) \text{ (degrees)}$$

The values for T_1 and T_2 thus chosen form a starting point for the selection of appropriate values for the more complex lag-lead compensator required by the real system.

Position Loop Filter Initialization

Switch S1, which is controlled by the DUMP bit in the WINDOW register, may be used to short out the external feedback capacitor C_{P2}, discharging it. S1 is usually closed during a seek operation, so that when the system is switched to track mode, no sudden transients occur due to charge stored on C_{P2}. Disturbances to the position signal when the system is switching to track mode can greatly extend the disk drive's access time, since the system response is much slower in this mode.

On Track Window

The on track window comparator may be used to monitor the positioning accuracy of the head. The position error voltage at pin FP1 is compared to a signal selected by the bits NW0-2 in the WINDOW register. The ONTRK bit in register STATUS is set if the position error is within the specified limits and cleared if it is outside the limits (in either the positive or the negative direction). The programmable excursion limits (ex-

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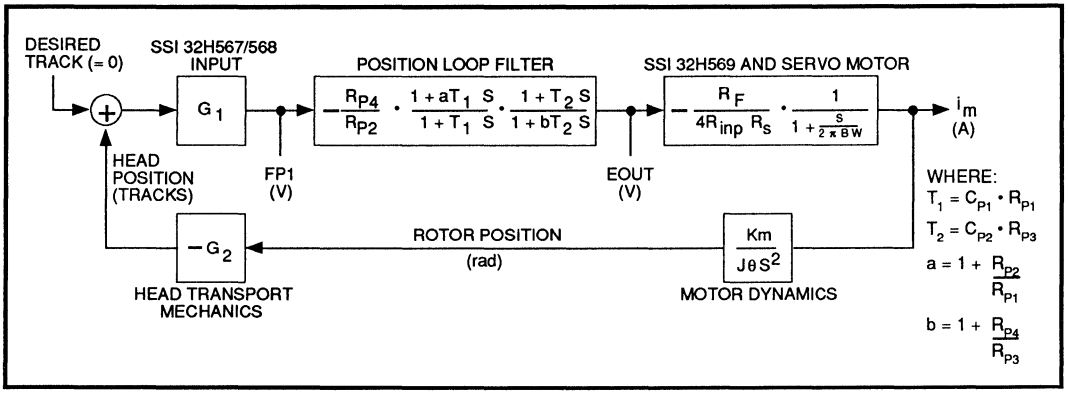


FIGURE 8(a): System Transfer Function in Track Mode

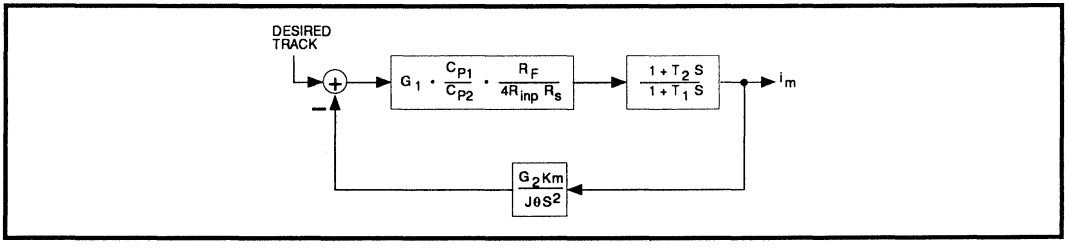


FIGURE 8(b): Simplified Track Mode Transfer Function

pressed as a percentage of a track) range from 2.8% to 22.5% in 8 equal steps. By monitoring the ONTRK bit, the microprocessor can determine when the head has settled sufficiently for read and write operations to commence. The ONTRK bit may also be used to decide when it is appropriate to switch from seek to track mode at the end of a period of deceleration.

SEEK MODE

Velocity Profile

The velocity profile that results in the shortest seek time, subject to motor current and head velocity limitations, is as follows:

1) Maximum acceleration (maximum motor current) until the half-way point or maximum velocity is reached.
2) Constant velocity motion until it is time to commence deceleration (if maximum velocity was reached).
3) Maximum deceleration until head comes to rest over the destination track. The decceleration period is of approximately the same duration as the acceleration period.

The microprocessor computes a velocity profile according to the rules above, based on the current head location and destination track. During the final approach to the destination track, updates to the velocity DAC become more infrequent since the track crossing rate is approaching zero. The fill signal which is derived from the position error can be used to provide a smooth target velocity profile between track crossing updates. Figure 9 shows a set of typical waveforms as the head approaches the destination track. The fill gain is adjusted at each track crossing so that the fill signal interpolates smoothly between target DAC settings. In the destination track, where the target DAC output is zero, the fill signal is especially important, since it becomes zero only when the head is centered on the track. The velocity control loop thus causes the head to come to rest at the center of the destination track.

Loop Compensation

The transfer function for the controller electronics of figure 7 is shown in figure 10(a). This transfer function may be simplified as shown in figure 10(b), under the following conditions:

$$\omega^2 >> \frac{(GG_1G_2)(K_m R_{V1})}{J\theta R_{V3}}$$

$$R_{V4} C_{V1} = \frac{J\theta \omega R_{V3}}{(GG_1G_2)(K_m R_{V1})}$$

The value of ω, the corner frequency of the internal position differentiator, is dependent on the sync rate, but the above condition is generally satisfied by most systems. The condition on RV4 and CV1 sets the position of the zero due to the external components in the velocity loop filter, whose function is described below. The resulting system has two real poles, one of which is at the origin, and is thus unconditionally stable.

The position of the SSI 32H6220 internal differentiator pole is selectable under microprocessor control. It is desireable to select as low a frequency as is consistent with the required seek performance. This pole prevents the differentiator from amplifiying high frequency noise. In order to provide feedback of a velocity signal for frequencies above the differentiator pole, the external velocity loop filter is configured to act as an integrator which integrates the motor current sense output of the SSI 32H569, or the SSI 32H6230, SOUT. Since SOUT is proportional to motor acceleration, this integration produces a signal proportional to velocity. Thus, at low frequencies the velocity feedback is generated by differentiating the position error signal and at high frequencies, the velocity term results from integrating motor current. It is more accurate to estimate velocity from a direct observation of head position, but at higher frequencies it is necessary to provide increased noise immunity. The system described above balances these two considerations.

OFFSET CANCELLATION

The 32H6220 is capable of cancelling position offset, velocity offset, and motor current offset. The following procedures may be used to null out these effects.

A. Position offset

This procedure removes any offset introduced by the position processing circuitry in the SSI 32H6220.

1. Set T/$\overline{S}$. (Enter track mode.)
2. Set CAL and DUMP. (This switches the N and Q inputs to VREF and shorts out CP2).
3. Set ERREN. (This activates the ERR comparator and connects its output to SGN.)
4. Adjust NOS and SOS until a 1LSB change causes SGN to change state. The final values should be stored and used whenever track mode is used.
5. Clear CAL, DUMP, ERREN to resume normal track mode operation.

B. Velocity offset

This procedure removes any offset generated in the velocity path of the SSI 32H6220.

1. Clear T/$\overline{S}$. (Enter seek mode).
2. Set CAL, ERREN, and ENA.
3. Adjust TARGET and VELPOL until 1LSB change causes SGN to change state. This value of TARGET should be stored for use in future seeks as the velocity offset.
4. Clear CAL and ERREN to resume normal seek mode.

Finer offset adjustment can be made by using the OFFSET register, however the calculation must be done for each value of NFG that is planned to be used.

C. Motor Current Offset

Motor current offset (caused, for instance, by cable bias and windage on the head as well as voltage offset in the motor driver) results in an ontrack voltage at PE that is not zero. In some drives, the time from when DUMP is turned off to when the final value of PE is achieved adds appreciably to the loop settling time. The PE voltage can be minimized (and therefore, the settling time) as follows.

1. Enter track mode and wait for the head position to settle. Make sure CAL is reset.
2. Set ERREN.
3. Adjust TARGET until PE is zero (evidenced by SGN toggling equally between 1 and 0. Program target with this value whenever a seek to this area of the disk is performed.

Since this technique compensates for cable bias, care must be taken to interpret the results. Cable bias will be position dependent and can also depend on the previous head positions.

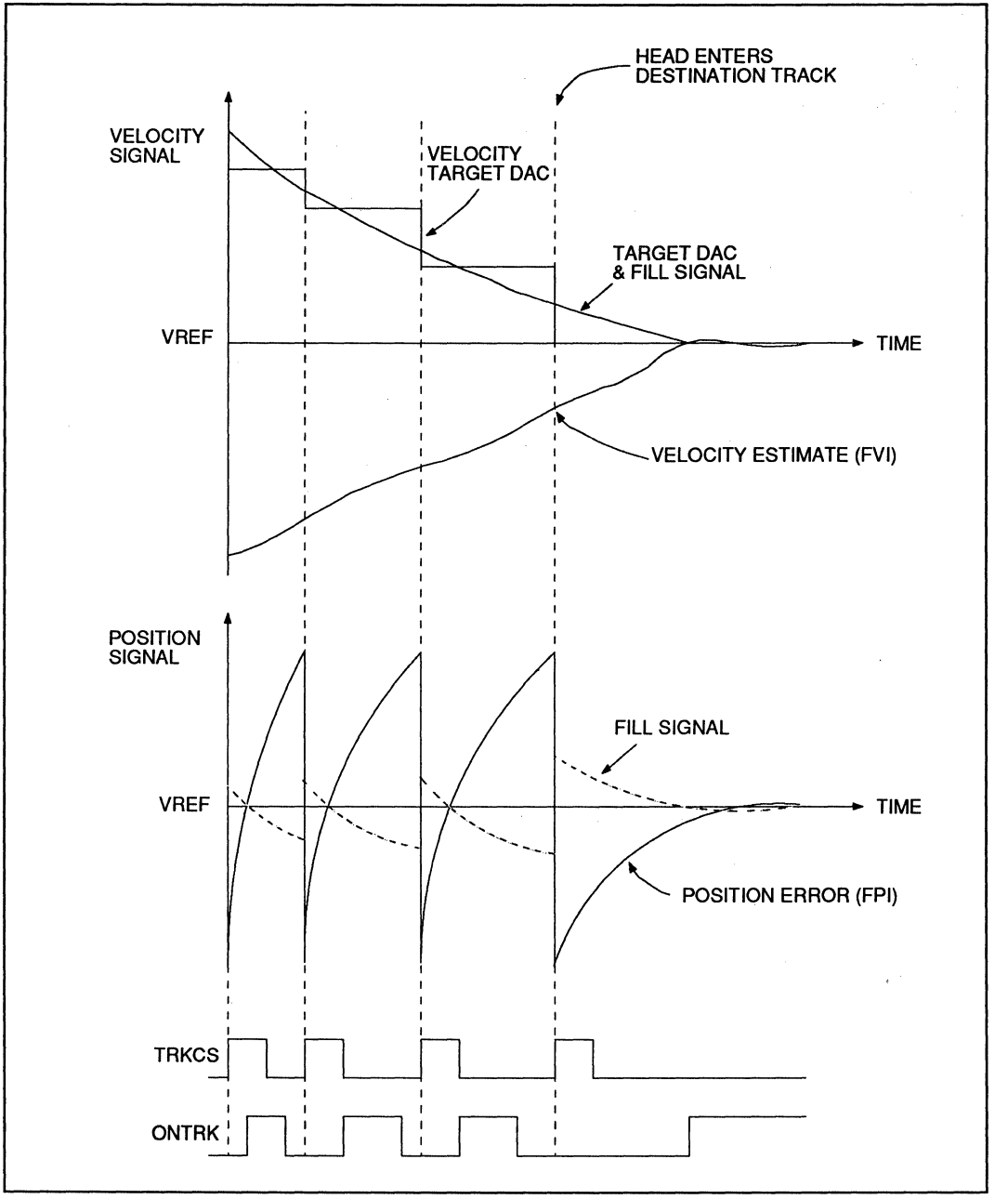


FIGURE 9: Typical Waveforms During Final Deceleration Mode

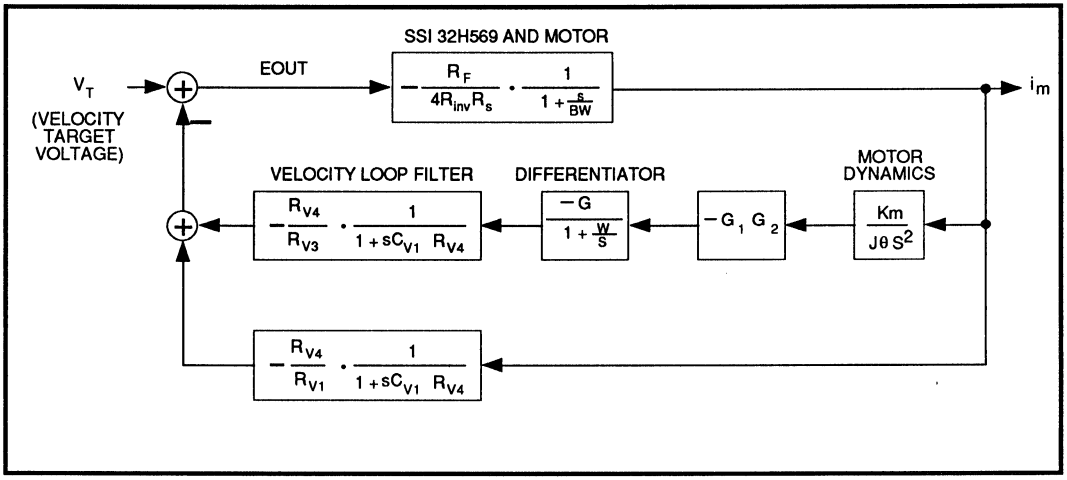


FIGURE 10(a): Transfer Function of SSI 32H6220 in Seek Mode

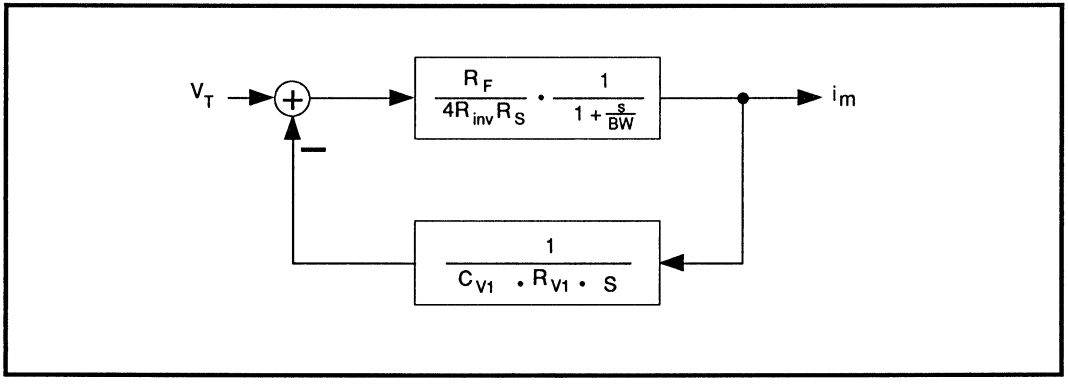


FIGURE 10(b): Simplified Transfer Function of SSI 32H6220 in Seek Mode

$$\omega^2 >> \frac{(GG_1G_2)(K_m R_{V1})}{J\theta R_{V3}}$$

$$R_{V4}C_{V1} = \frac{J\theta\omega R_{V3}}{(GG_1G_2)(K_m R_{V1})}$$

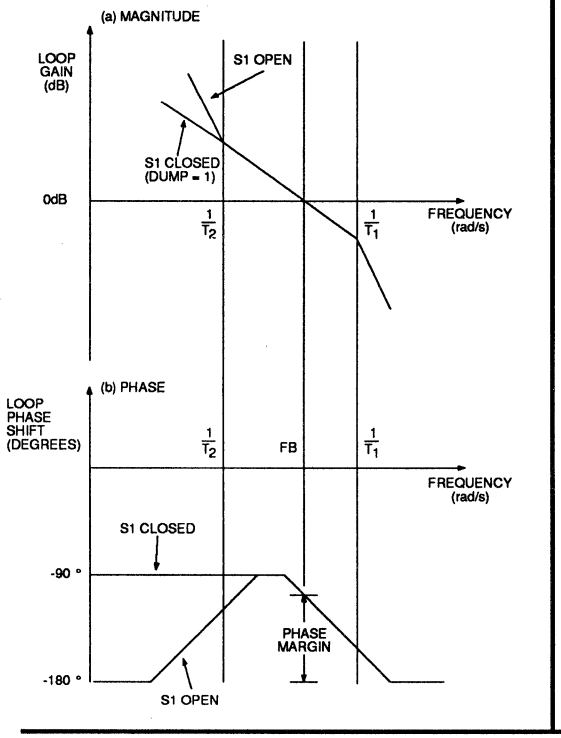


FIGURE 11: Bode Plot of Simplified Track Mode Transfer Function

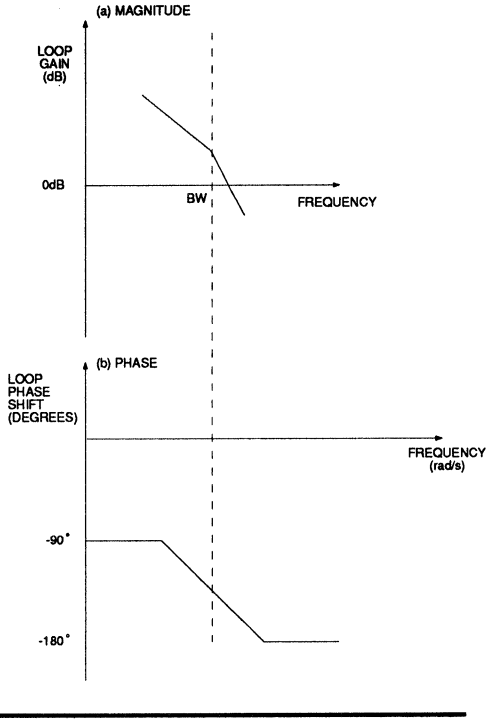
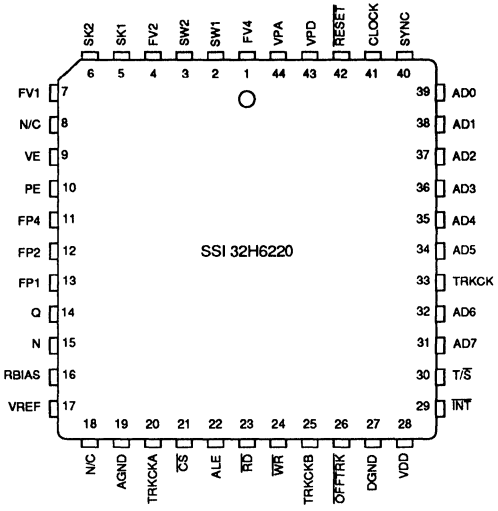


FIGURE 12: Bode Plot of Simplified Seek Mode Transfer Function

PACKAGE PIN DESIGNATIONS

(TOP VIEW)

CAUTION: Use handling procedures necessary for a static sensitive component.



44-Pin PLCC

6

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32H6220, Servo Controller		
44-Pin PLCC	32H6220-CH	32H6220-CH

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 731-7110, FAX (714) 573-6914

Notes:

silicon systems®
A TDK Group Company

SSI 32H6230
Servo Motor Driver

Preliminary Data

December 1991

DESCRIPTION

The SSI 32H6230 Servo Motor Driver is a bipolar device intended for use in Winchester disk drive head positioning systems employing linear or rotary voice coil motors. When used in conjunction with a position controller, such as the SSI 32H568 or the SSI 32H6220 Servo Controllers, and a position reference, such as the SSI 32H567 Servo Demodulator, the device allows the construction of a high performance, dedicated surface head positioning system.

The SSI 32H6230 serves as a transconductance amplifier by driving 4 MOSFETs in an H-bridge configuration, performs motor current sensing and limits motor current. In its linear tracking mode, class B operation is guaranteed by crossover protection circuitry, which ensures that only one MOSFET in each leg of the H-bridge is active. The MOSFET drivers are disabled when motor velocity or current exceed externally programmable limits. In addition, automatic head retraction and spindle braking may be initiated by a low voltage condition or upon external command.

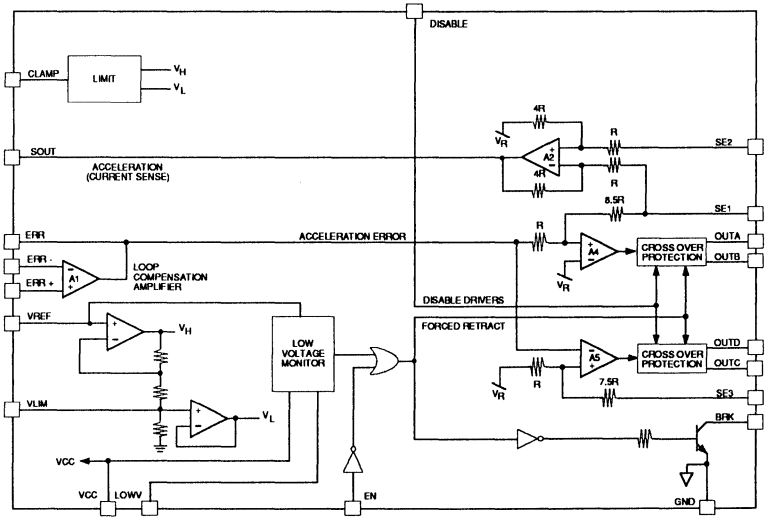
(Continued)

FEATURES

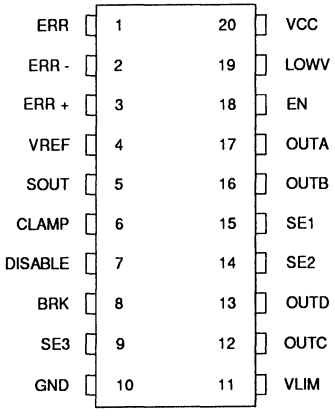
- **Predriver for linear and rotary voice coil motors**
- **Interfaces directly to MOSFET H-Bridge motor driver**
- **Class B linear mode and constant velocity retract mode**
- **FET disable function**
- **Precision differential amplifier for motor current sensing**
- **Clamp for motor current limiting**
- **Automatic head retract and spindle braking signal on power failure**
- **External digital enable**
- **Servo loop parameters programmed with external components**
- **Advanced bipolar IC requires under 240 mW from 12V supply**
- **Available in 20-pin DIP or SO packaging**

6

BLOCK DIAGRAM



PIN DIAGRAM



DESCRIPTION (Continued)

The SSI 32H6230 is implemented in an advanced bipolar process and dissipates less than 240 mW from a 12V supply. The IC is available in 20-pin DIP and 20-pin SO packaging.

FUNCTIONAL DESCRIPTION

(Refer to block diagram and typical application Fig.2)

The SSI 32H6230 has two modes of operation, linear and retract. The retract mode is activated by a power supply failure or when the control signal EN is false. Otherwise the device operates in linear mode.

During linear operation, an acceleration signal from the servo controller is applied through amplifier A1, whose three connections are all available externally. RC components may be used to provide loop compensation at this stage. The ERR signal drives two precision amplifiers, each with a gain of 8.5. The first of these amplifiers is inverting, and is formed from opamp A4, an on-chip resistor divider and an off-chip complementary MOSFET pair. The second is non-inverting, and is formed in a similar manner from opamp A5. Feedback from the MOSFET drains, on sense inputs SE1 and SE3, allows the amplifiers gains to be established precisely. The voice coil motor and a series current sense resistor are connected between SE1 and SE3.

Crossover protection circuitry between the outputs of A4 and A5, and the external MOSFETs, ensures class B operation by allowing only one MOSFET in each leg of the H-bridge to be in conduction. The crossover separation threshold, illustrated in Figure 5, is the maximum drive on any MOSFET gate when the motor voltage changes sign. The crossover circuitry can also disable all MOSFETS simultaneously (to limit motor current or velocity) or apply a constant voltage across the motor (to retract the heads at a constant velocity).

Motor current is sensed by a small resistor placed in series with the motor. The voltage drop across this resistor is amplified by a differential amplifier with a gain of 4 (A2 and associated resistors), whose inputs are SE1 and SE2. The resulting voltage, SOUT, is proportional to motor current, and hence acceleration. This signal is externally fed back to A1, so that the signal ERR represents the difference between the desired acceleration (from the servo controller) and the actual motor acceleration.

An adjustable voltage clamp is provided to prevent over current to the motor. It accomplishes the current limiting by clamping the voltage excursion at the input of A1. The voltage clamp values are programmed by VREF and VLIM. VLIM is the lower clamp value and the upper clamp limit is 2 • VREF - VLIM.

Disable function will cause all 4 bridge FETs to turn off. Note that this function does not override the retract function.

The SSI 32H6230 has low voltage monitor circuitry that will detect a loss of voltage on the VREF, VCC or LOWV pins. The power supply pin, VCC, should be connected to the disk drive's spindle motor so that its stored rotational energy may be used to hold up VCC briefly during a power failure. LOWV is used to detect a system power supply failure. When a low voltage condition is detected, the MOSFET drivers switch from linear operation to retract mode. In this mode a constant voltage is applied across the motor which will cause the heads to move at a constant speed. A mechanical stop must be provided for the heads when they reach a safe location. The current limiting circuitry will disable the MOSFET drivers when motor current increases due to loss of the velocity-induced back EMF. An open collector output, BRK, which is active while the device is in retract mode, is provided for spindle motor braking. An external RC delay may be used to defer braking until the heads are retracted.

Two examples of an entire servo path implemented with the SSI 32H6230 and its companion devices, the SSI 32H567, 32H568, and the SSI 32H567, 32H6220 are shown in Figures 7 and 8.

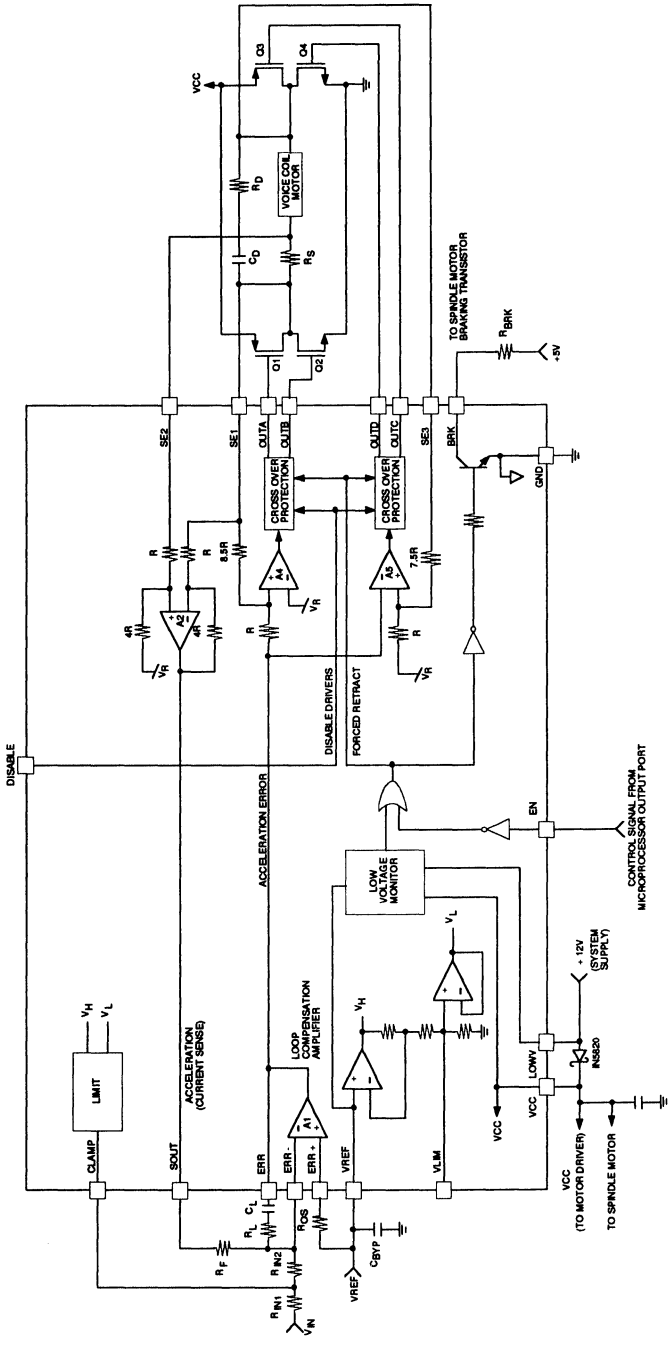


FIGURE 2: Typical Application

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PIN DESCRIPTION

POWER

NAME	PIN	TYPE	DESCRIPTION
VCC	20		POSITIVE SUPPLY - 12V power supply. Usually taken from spindle motor supply. Spindle motor stored energy permits head retraction during power failure. If VCC falls below 9V, a forced head retraction occurs.
LOWV	19	I	LOW VOLTAGE - System 12V supply. If this input falls below 9V, a forced head retraction occurs.
VREF	4	I	REFERENCE VOLTAGE - 5.4V input. All analog signals are referenced to this voltage. If VREF falls below 4.3V, a forced head retraction occurs.
GND	10		GROUND

CONTROL

NAME	PIN	TYPE	DESCRIPTION
ERR	1	O	POSITION ERROR- Loop compensation amplifier output. This signal is amplified by the MOSFET drivers and applied to the motor by an external MOSFET H-bridge, as follows: SE3-SE1 = 17(ERR-VREF)
ERR-	2	I	POSITION ERROR INVERTING INPUT - Inverting input to the loop compensation amplifier.
ERR+	3	I	POSITION ERROR NON-INVERTING INPUT - Non-inverting input to the loop compensation amplifier.
SOUT	5	O	MOTOR CURRENT SENSE OUTPUT - This output provides a voltage proportional to the voltage drop across the external current sense resistor, as follows: SOUT-VREF=4(SE2-SE1)
DISABLE	7	I	DISABLE INPUT – Active High TTL input will cause all 4 bridge FETs to turn off. DISABLE does not override the retract function.
CLAMP	6	I	CLAMP – A clamp pin to limit the input error voltage. The voltage swing at this pin is limited to VREF +- (VREF - VLIM).
BRK	8	O	BRAKE OUTPUT – Active high, open collector output which may be used to enable an external spindle motor braking transistor upon power failure or deassertion of EN.
VLIM	11	I	VOLTAGE LIMIT – The voltage at this pin sets the upper and lower clamp voltage limits in conjunction with the voltage at VREF. Upper Clamp Limit = 2 • VREF - VLIM Lower Clamp Limit = VLIM.
SE2	14	I	MOTOR CURRENT SENSE INPUT - Non-inverting input to the current sense differential amplifier. It should be connected to one side of an external current sensing resistor in series with the motor. The inverting input of the differential amplifier is connected internally to SE1.
EN	18	I	ENABLE - Active high TTL compatible input enables linear tracking mode. A low level will initiate a forced head retract.

FET DRIVE

NAME	PIN	TYPE	DESCRIPTION
SE3	9	I	MOTOR VOLTAGE SENSE INPUT - This input provides feedback to the non-inverting MOSFET driver amplifier. It is connected to one side of the motor. The gain to this point is: SE3-VREF = 8.5(ERR-VREF)
OUTC	12	O	P-FET DRIVE (NON-INVERTING) - Drive signal for a P channel MOSFET connected between one side of the motor and VCC. This MOSFET drain is connected to SE3.
OUTD	13	O	N-FET DRIVE (NON-INVERTING) - Drive signal for an N channel MOSFET connected between one side of the motor and GND. This MOSFET drain is connected to SE3. Crossover protection circuitry ensures that the P and N channel devices driven by OUTC and OUTD are never enabled simultaneously.
SE1	15	I	MOTOR VOLTAGE SENSE INPUT - This input provides feedback to the inverting MOSFET driver amplifier. It is connected to the current sensing resistor which is in series with the motor. The gain to this point is: SE1-VREF = -8.5(ERR-VREF) This input is internally connected to the current sense differential amplifier inverting input.
OUTB	16	O	N-FET DRIVE (INVERTING) - Drive signal for an N channel MOSFET connected between the current sense resistor and GND. This MOSFET drain is also connected to SE1.
OUTA	17	O	P-FET DRIVE (INVERTING) - Drive signal for a P channel MOSFET connected between the current sense resistor and VCC. This MOSFET drain is also connected to SE1. Crossover protection circuitry ensures that the P and N channel devices driven by OUTC and OUTD are never enabled simultaneously.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

(Maximum limits indicates where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC operating characteristics.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VCC		0		16	V
VREF		0		10	V
SE1, SE2, SE3, OUT D		-1.5		15	V
All other pins		-.3		VCC + .3	V
Storage temperature		-45		165	°C
Solder temperature	10 sec duration			260	°C

RECOMMENDED OPERATION CONDITIONS (Unless otherwise noted, the following conditions are valid throughout this document.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VCC	Normal Mode	9	12	13.2	V
	Retract Mode	3.5V		14	V
VREF		5		7	V
Operating temperature		0		70	°C

DC CHARACTERISTICS

ICC, VCC current				20	mA
IREF, VREF current				2	mA

A1, LOOP COMPENSATION AMPLIFIER

Input bias current				500	nA
Input offset voltage				3	mV
Voltage swing	About VREF	2			V
Common mode range	About VREF	±1			V
Load resistance	To VREF	4			kΩ
Load capacitance				100	pF
Gain		80			dB
Unity gain bandwidth		1			MHz
CMRR	f <20 kHz	60			dB
PSRR	f <20 kHz	60			dB

A2, CURRENT SENSE AMPLIFIER

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input impedance	SE1 to SE2	3.5	5		kΩ
Input offset voltage				2	mV
Output voltage swing		VREF-4		VCC-1.2	V
Common mode range		0		VCC-0.2	V
Load Resistance	To VREF	4			kΩ
Load Capacitance				100	pF
Output impedance	f < 40 kHz			20	Ω
Gain (SOUT-VREF)/(SE1-SE2)		3.9	4	4.1	V/V
Unity gain bandwidth		1			MHz
CMRR	f < 20 kHz	52			dB
PSRR	f < 20 kHz	60			dB

VOLTAGE CLAMP

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CLAMP bias current	CLAMP = VREF			0.1	µA
Upper CLAMP limit (VREF + 1/3 VREF)	ICLAMP = 10 µA VLIM open		$\frac{4}{3}$VREF		V
Lower CLAMP limit (VREF - 1/3 VREF)	ICLAMP = -10 µA VLIM open		$\frac{2}{3}$VREF		V
CLAMP accuracy	| ICLAMP | = 10 µA	-3		3	%
CLAMP Impedance	1.0 mA> | ICLAMP | >10 µA			20	Ω
VLIM Voltage			$\frac{2\,VREF}{3}$		V
VLIM Accuracy		-1		+1	%

POWER SUPPLY MONITOR

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VCC fail threshold		8.5	9	9.8	V
LOWV fail threshold	|ILowv| < 0.5 mA	8.5	9	9.8	V
VREF fail threshold		3.9	4.3	4.8	V
Hysteresis (LOWV, VCC)			250		mV
Hysteresis (VREF)			110		mV
EN input low voltage	|IIL| < 0.5 mA	0.8			V

POWER SUPPLY MONITOR (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
EN input high voltage	|IIH| < 40 uA			2	V
BRK voltage	normal mode, |IOL| < 1 mA			0.4	V
BRK leakage current	retract mode			10	µA
BRK delay (from power fail or EN false to BRK floating)				1	ms

MOSFET DRIVERS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SE3 Input impedance	To VREF	10	25		kΩ
OUTA, OUTC voltage swing |Io|<1 mA		0.7		VCC-1	V
OUTB, OUTD voltage swing |Io|<1 mA		1		VCC-1	V
VTH, Crossover separation threshold				2	V
Slew rate (OUTA, OUTB, OUTC, OUTD)	Cl<1000 pF	1.4			V/µs
Crossover time	300 mV step at ERR			5	µs
Output impedance (OUTA,B,C,D)			50		kΩ
Transconductance I(OUTA,B,C,D)/(ERR-VREF)			8		mA/V
Gain (-(SE1-VREF)/(ERR-VREF) or (SE3-VREF)/(ERR-VREF))		8	8.5	9	V/V
Offset current	R_S = 0.2Ω, R_F = R_{IN}, V_{IN}=VREF			20	mA
Retract motor voltage (SE1-SE3)		0.7	1	1.3	V

APPLICATIONS INFORMATION

A typical SSI 32H6230 application is shown in Figure 2. The selection criteria for the external components shown are discussed below. Figure 3 shows the equivalent circuit and equations for the DC motor used in the following derivations. While the nomenclature chosen is for a rotating motor, the results are equally applicable to linear motors.

MOTOR CURRENT SENSE AND LIMITING

The series resistor which senses motor current, Rs, is chosen to be small compared to the resistance of the motor, Rm. A value of Rs = 0.2Ω is typical in disk drive applications.

VLIM, RIN1, and RIN2 must be chosen to keep the motor current below Imax. The voltage clamp values programmed by VREF and VLIM must be chosen to cause limiting when the motor current reaches its maximum permissible current in amps, this value may be chosen as follows:

$$|Imax| = \frac{CLAMP}{RIN2} \cdot \frac{RF}{4 \cdot Rs}$$

Where the upper clamp limit is 2 • VREF - VLIM and the lower clamp limit is VLIM. If VLIM is left open, a value of 0.667 • VREF will appear. The upper clamp limit is then 1.33 • VREF and the lower clamp limit is 0.667 • VREF. The values of RIN1, RIN2 must be chosen to satisfy the maximum swing of Vin before limiting occurs,

$$Vin(max) = CLAMP\left(1 + \frac{RIN1}{RIN2}\right) - \frac{RIN1}{RIN2}(VREF) + VREF$$

and they should also satisfy the maximum current VCLAMP can source or sink

$$\frac{Vin\ (max)\ [Actual] - CLAMP}{RIN1} \leq 1mA$$

LOOP COMPENSATION

The transfer function of the SSI 32H6230 in the application of Figure 2 is shown in Figure 4(a). If the zero due to RL and CL in the loop compensation circuit is chosen to cancel the pole due to the motor inductance, Lm, then the transfer function can be simplified as shown in Figure 4(b), under the assumption that this pole and the pole due to the motor mechanical response are widely separated. CL may then be chosen to set the desired open loop unity gain bandwidth.

$$C_L = \frac{68 \cdot R_s}{2 \cdot \pi \cdot R_F \cdot (R_m + R_s) \cdot BW}$$

where BW is the unity gain open loop bandwidth

$$R_L = \frac{L_m}{C_L \cdot (R_m + R_s)}$$

The closed loop response of the servo driver and motor combination, using the component values and simplifying assumptions given above, is given by:

$$\frac{i_m}{V_{in}}(s) = -\frac{1}{R_{in}} \cdot \frac{R_F}{4 \cdot R_s} \cdot \frac{1}{\left(1 + \frac{s}{2 \cdot \pi \cdot BW}\right)}$$

Where: Rin = RIN1 + RIN2

(This analysis neglects the pole due to the output impedance of the MOSFET drivers and the MOSFET gate capacitance, an effect that may be significant in some systems.)

RF is chosen to be sufficiently large to avoid overloading A2 ($R_F > 4$ kΩ). The input resistor, RIN, sets the conversion factor from servo controller output voltage to servo motor current. RIN is chosen such that the servo controller internal voltages are scaled conveniently. The resistor ROS is optional and cancels out the effect of the input bias current of A1.

$$R_{os} = R_{in} // R_F$$

The external components RD and CD have no effect on the motor dynamics, but may be used to improve the stability of the MOSFET drivers. The load represented by the motor, ZM, is given by:

$$ZM = (R_s + R_m)\left(1 + s\frac{L_m}{R_s + R_m}\right)\left(1 + \frac{K_m^2}{s \cdot J\theta \cdot (R_s + R_m)}\right)(\Omega)$$

At frequencies above $(Rs+Rm)/(2\pi \cdot Lm)$ Hz, this load becomes entirely inductive, which is undesireable. RD and CD may be used to add some parallel resistive loading at these frequencies.

6

H-BRIDGE MOSFETS

The MOSFETs chosen for the H-bridge should have gate capacitances in the range of 500-1000 pF. The MOSFET input capacitance forms part of the compensation for the MOSFET drivers, so values below 500 pF may cause some driver instability. Excessive input capacitance will degrade the slew mode performance of the drivers.

When the motor voltage is changing polarity, the crossover protection circuits at outputs OUTA-OUTD ensure that the maximum MOSFET gate drive is less than 2V (the crossover separation threshold), as illustrated in Figure 5. The thresholds of the MOSFET devices chosen should be as large as possible to minimize conduction in this region. If the device thresholds are significantly less than the crossover separation threshold, the N and P channel devices in each leg of the H-bridge will conduct simultaneously, causing unnecessary power dissipation.

POWER FAILURE OPERATION

The power supply for the SSI 32H6230, VCC, should be taken from the system 12V supply through a schottky diode (maximum 0.5V drop at If = 3A) and connected to the disk drive spindle motor. If the system power fails, the IC will continue to operate as the spindle motor becomes a generator. The SSI 32H6230 will detect the power failure and cause a forced head retract, continuing to operate with VCC as low as 3.5V. The power fail mode will commence if either VCC or LOWV falls below 9V, or VREF falls below 4.3V, or EN is false. Hysteresis on the low voltage thresholds prevents the device from oscillating between operating modes when the power supply is marginal.

The BRK output, which is pulled low during normal operation, floats during a power failure. This allows an external transistor to be enabled for spindle motor braking. An external RC delay may be added to defer braking until head retraction is complete, since the spindle motor is required to generate the supply voltage during retraction.

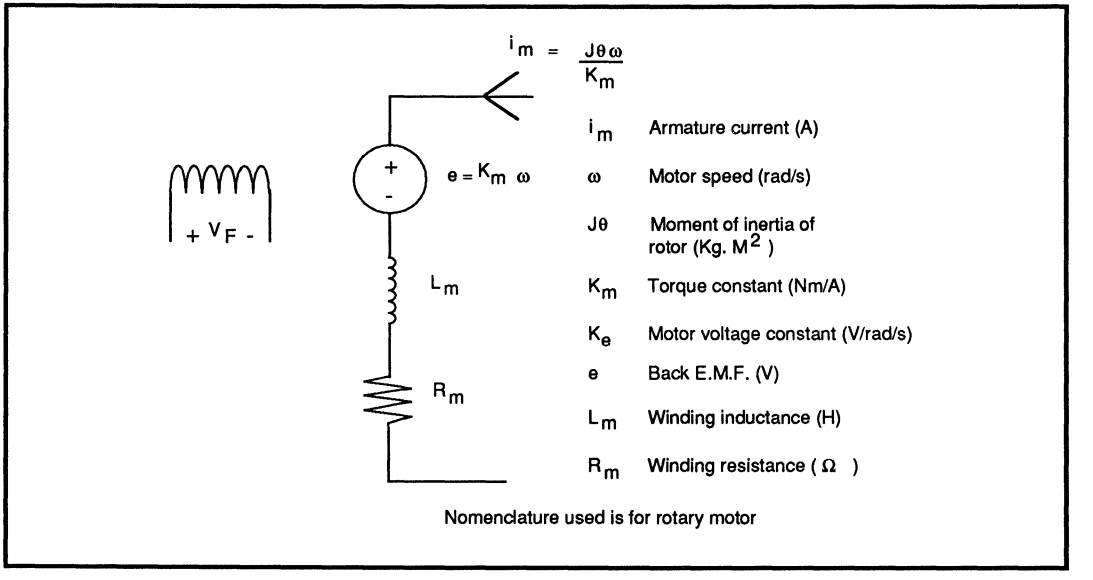

FIGURE 3: Equivalent Circuit for Fixed Field DC Motor

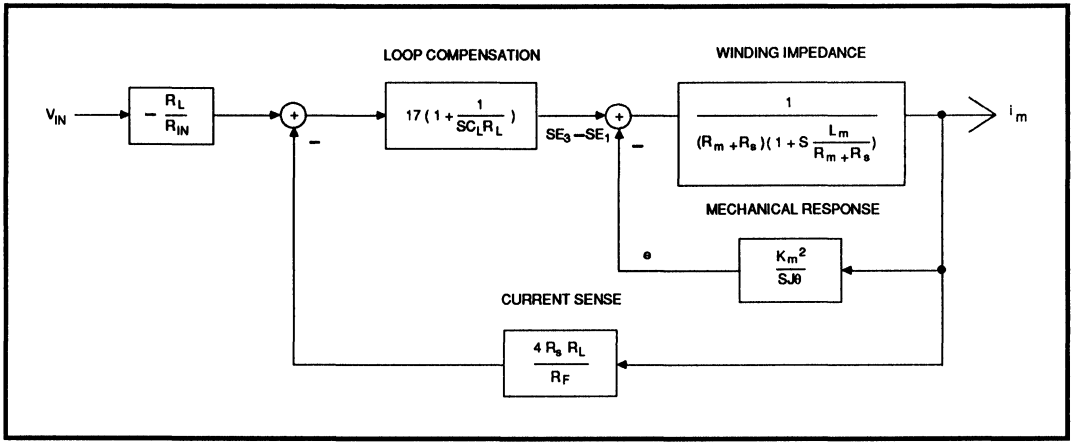

FIGURE 4(A): Transfer Function of SSI 32H6230 In Typical Application with Fixed Field DC Motor

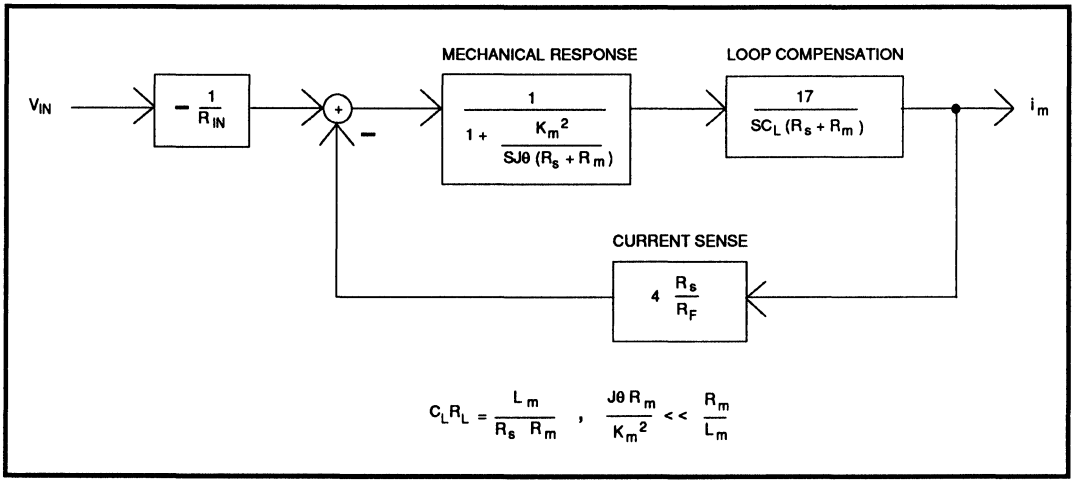

FIGURE 4(B): Simplified Transfer Function of SSI 32H6230 In DC Motor Application

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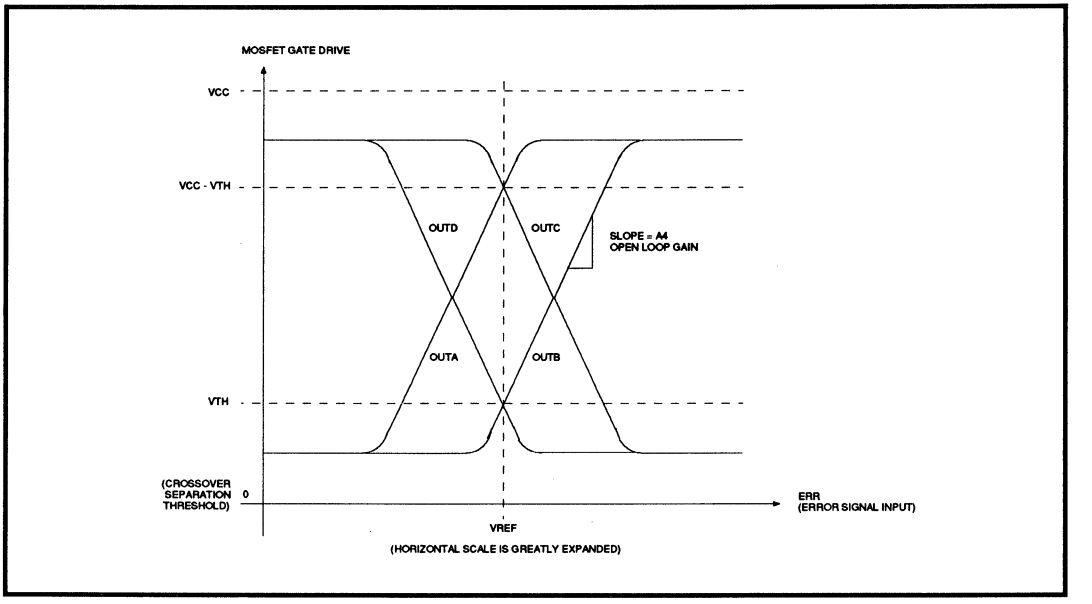

FIGURE 5: Simplified Transfer Function of SSI 32H6230 in DC Motor Application

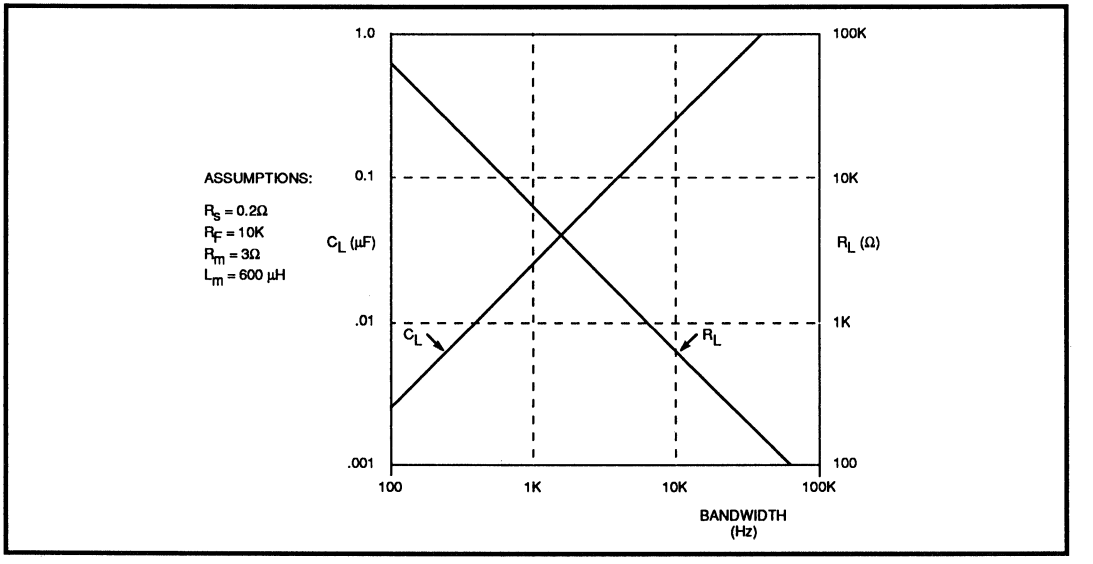

FIGURE 6: Typical Motor Driver Compensation

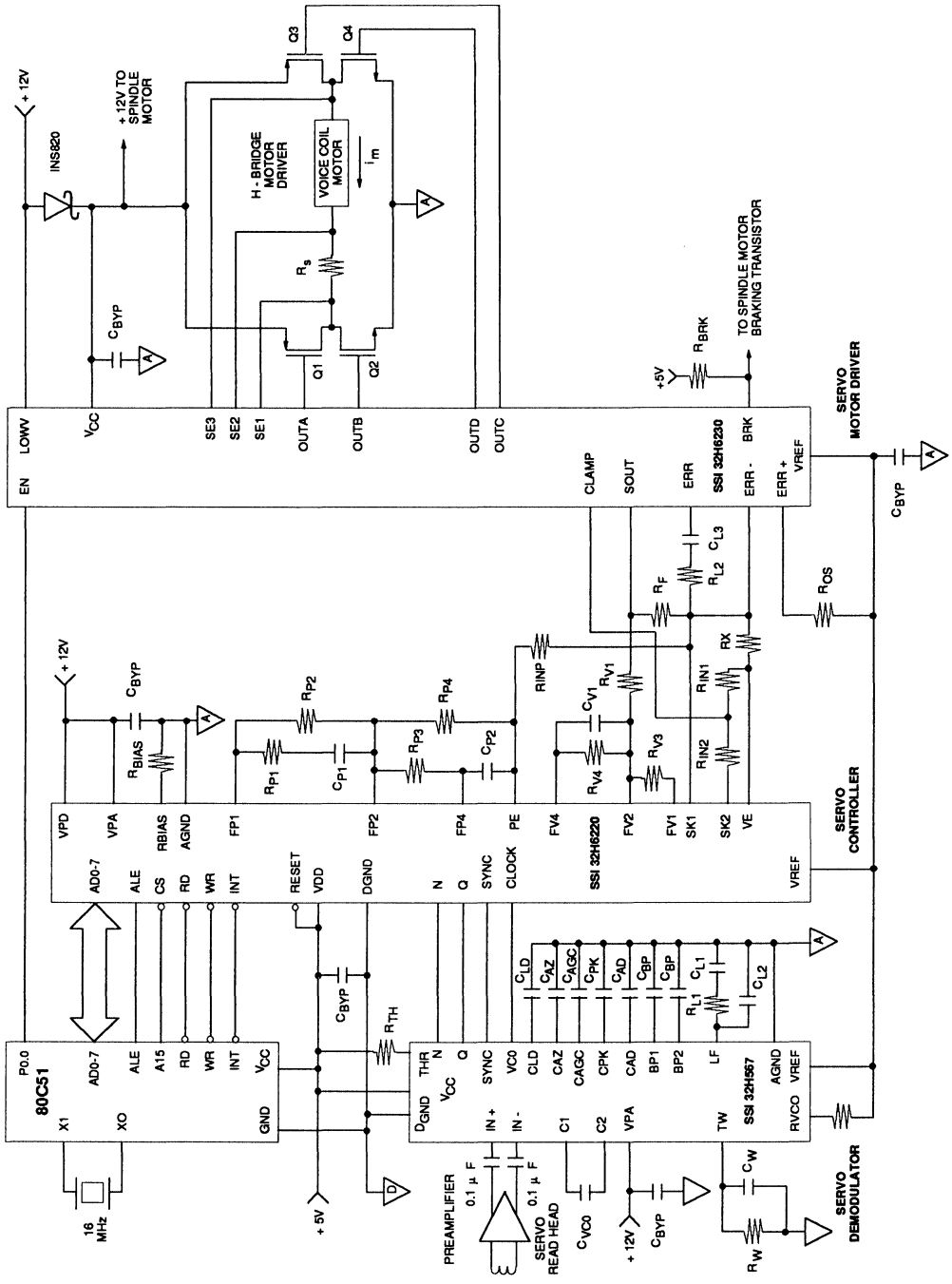

FIGURE 8: Complete Example of Servo Path Electronics Using the SSI 32H567/6220/6230 Chip Set

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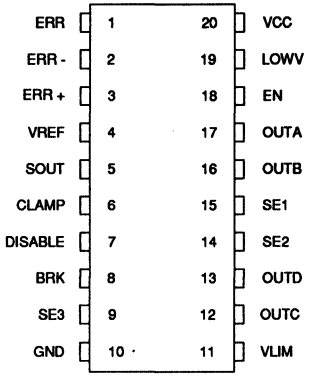
SSI 32H6230
Servo Motor Driver

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



20-Pin SO, DIP

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32H6230, Servo Motor Driver		
20-Pin DIP	32H6230-CP	32H6230-CP
20-Pin SOL	32H6230-CL	32H6230-CL

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 731-7110, FAX (714) 573-6914

SSI 32H6240
Servo Motor Driver

Advance Information

December 1991

DESCRIPTION

The SSI 32H6240 Servo Motor Driver is a bipolar device intended for use in Winchester disk drive head positioning systems employing linear or rotary voice coil motors. When used in conjunction with a position controller, such as the SSI 32H568 or the SSI 32H6220 Servo Controllers, and a position reference, such as the SSI 32H567 Servo Demodulator, the device allows the construction of a high performance, dedicated surface head positioning system.

The SSI 32H6240 serves as a transconductance amplifier by driving 4 bipolar power transistors in an H–bridge configuration and performs motor current sensing by using an on-chip differential amplifier. In its linear tracking mode, class B operation is guaranteed by crossover protection circuitry, which ensures that only one transistor in each leg of the H-bridge is active. Automatic head retraction and spindle braking may be initiated by a low voltage condition or upon external command.

The SSI 32H6240 is implemented in an advanced bipolar process and dissipates less than (240 mW) from a 12V supply. The SSI 32H6240 is available in a 28-pin PLCC.

FEATURES

- **Predriver for linear and rotary voice coil motors**
- **Interfaces directly to Bipolar H-Bridge motor driver**
- **Class B linear mode and constant velocity retract mode**
- **Power transistor disable function**
- **Precision differential amplifier for motor current sensing**
- **On-chip precision power fail detect**
- **Automatic head retract and spindle braking signal on power failure**
- **External digital enable**
- **Servo loop parameters programmed with external components**
- **Advanced bipolar IC requires under (240 mW) from 12V supply**
- **Available in 28-pin PLCC packaging**
- **+5V, +12V operation**

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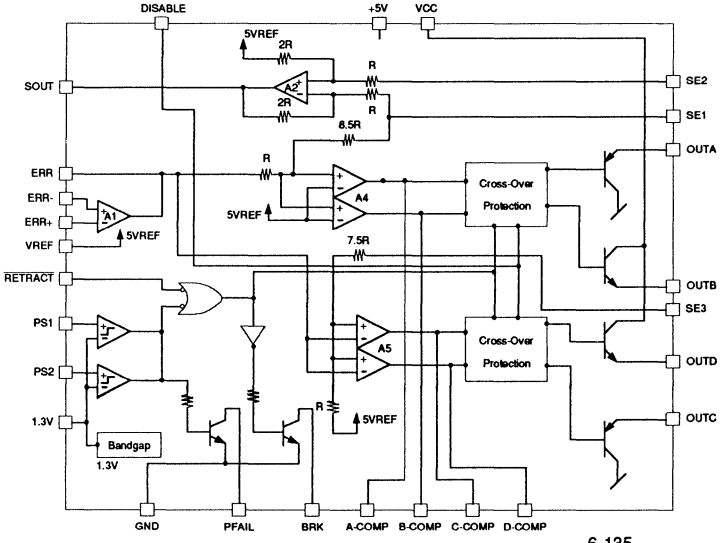
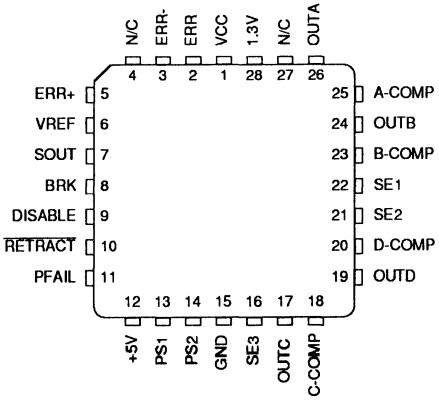
BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION

(Refer to block diagram and typical application Fig.2)

There are three modes of operation of the SSI 32H6240: Disable, Retract, and Linear. The circuit mode is controlled by the DISABLE , $\overline{\text{RETRACT}}$, PS1, and PS2 pins.

DISABLE mode turns off the output drivers. OUTA and OUTC are pulled to VCC through internal 1.5 kΩ resistors. OUTB and OUTD are pulled to GND through internal 1.5 kΩ resistors. Disable mode does not override Retract mode.

RETRACT mode turns off OUTB and OUTC. OUTD is turned on. OUTA is turned on in a special manner to force 1V at SE1. Retract mode does override Disable mode.

POWER FAIL mode occurs when either PS1 or PS2 fall below 1.3V. Power fail overrides Retract and Disable inputs and forces the chip into RETRACT mode.

When the $\overline{\text{RETRACT}}$ pin is pulled low the SSI 32H6240 will go into retract mode. The BRK pin will go high. When the DISABLE pin is pulled high it will cause all 4 bridge power transistors to turn off. PFAIL and BRK will remain low if PS1, PS2, and $\overline{\text{RETRACT}}$ pins do not change.

During linear mode operation an acceleration signal from the servo controller is applied through amplifier A1. Amplifier A1's three connections are available for connection to external loop compensation components. The ERR signal drives two precision amplifiers, each with a gain of 8.5. The first of these amplifiers is inverting, and is formed from opamp A4, an on-chip resistor divider, and an off-chip complementary Bipolar Power Transistor pair. The second amplifier is non-inverting and is formed in a similar manner from opamp A5. Feedback from external transistor's collectors on sense inputs SE1 and SE3 allows the amplifier's gains to be precisely set. The voice coil motor and a series current sense resistor are connected between SE1 and SE3. The output of the amplifiers will provide the base current for the external H-Bridge Bipolar Power Transistors. The chip is designed to work with external transistors with a minimum Beta of 40 and minimum f_T of 40 MHz. The base bias resistors for the external bridge transistors are internal to the IC.

Cross over protection circuitry between the outputs of A4 and A5 and the external power transistors ensure Class B operation by allowing only one transistor in each leg of the H-bridge to be in conduction. The crossover circuitry can also disable all Power Transistors simultaneously (to limit motor current or velocity) or apply a constant voltage across the motor (to retract the heads at a constant velocity.)

Motor current is sensed by a small resistor placed in series with the motor. The voltage drop across this resistor is amplified by a differential amplifier with a gain of 2 (A2 and associated resistors), whose inputs are SE1 and SE2. The resulting output voltage, SOUT, is proportional to motor current, and hence acceleration. This signal is externally fed back to A1 so that the signal ERR represents the difference between the desired acceleration (from the servo controller) and the actual motor acceleration. The total output offset current (Vin = Vref, Rsense = 0.5 Ω) is less than 5.5 mA.

The SSI 32H6240 has low voltage monitor circuitry that will detect a decrease in the voltage at PS1 and PS2 pins. The +5V and +12V power supplies are divided down by external resistors and then compared to an internal 1.25V ±5% reference. The power supply pin, VCC, should be connected to the disk drive's spindle motor so that its stored rotational energy may be used to hold up VCC briefly during a power failure. When a low voltage condition is detected on either the PS1 or PS2 pins the BIPOLAR drivers switch from linear operation to retract mode. In this mode a constant voltage is applied across the motor which will cause the heads to move at a constant speed. A mechanical stop must be provided for the heads when they reach a safe location. External current limiting circuitry is required for both the linear and retract modes of operation. An open collector output, PFAIL, which is low in the linear mode, will go high to indicate a power failure. This signal is gated with the $\overline{\text{RETRACT}}$ input signal to force the chip into the Retract mode during power failure and to signal a BRK spindle. A BRK spindle is signaled by forcing a High level on the BRK open collector output which is normally low in the Linear mode. The BRK pin is provided for spindle motor braking. An external RC delay may be used to defer braking until the heads are retracted.

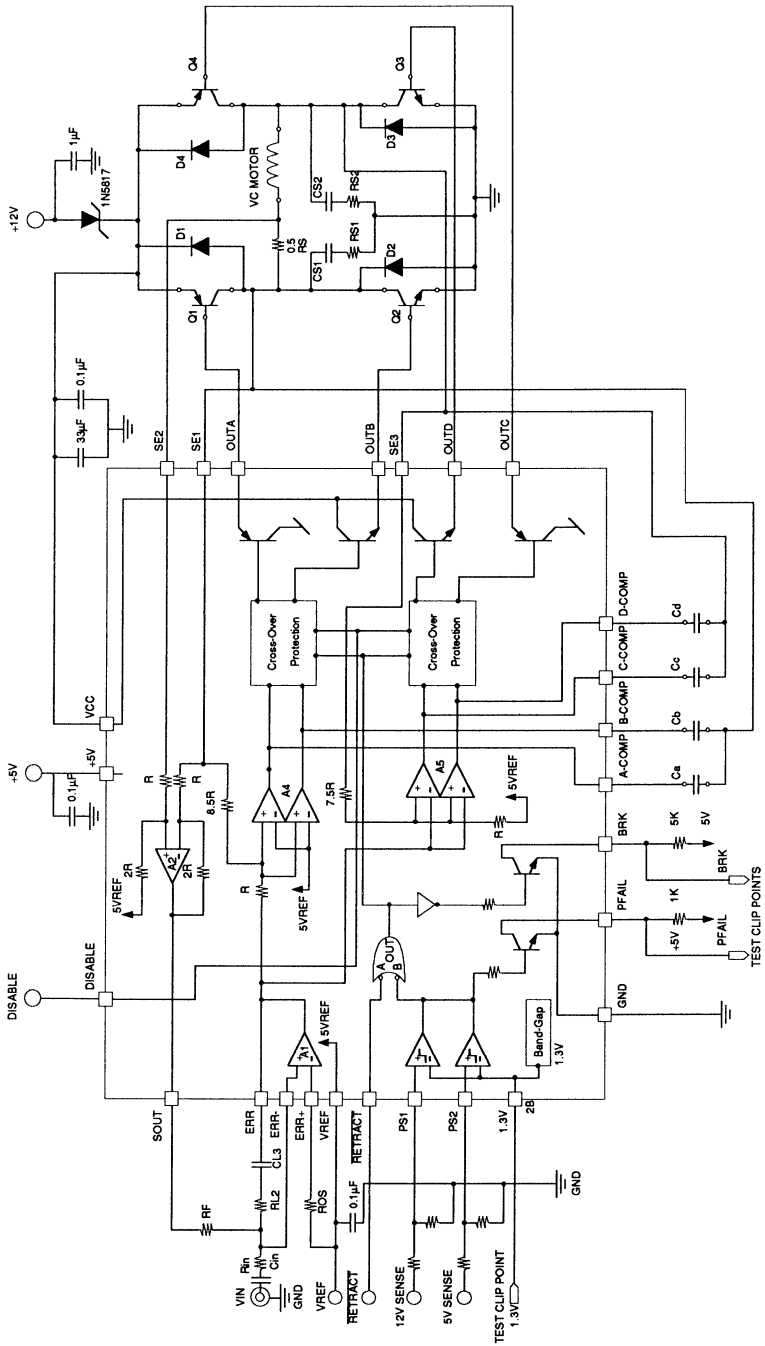


FIGURE 2: SSI 32H6240 Typical Application

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PIN DESCRIPTION

POWER

NAME	TYPE	DESCRIPTION
VCC	-	POSITIVE SUPPLY - Usually taken from spindle motor supply. Spindle motor stored energy permits head retraction during power failure. If either a "Power Failure" or a "Retract" is asserted a forced head retraction occurs. Usually supplied through a power Schottky diode from Spindle Motor Supply.
+5V	I	5-volt power supply
VREF	I	REFERENCE VOLTAGE - 5.0V input. All analog signals are referenced to this input.
GND	-	GROUND

CONTROL

NAME	TYPE	DESCRIPTION
ERR	O	POSITION ERROR- Loop compensation amplifier output. This signal is amplified by the BIPOLAR drivers and applied to the motor by an external BIPOLAR H-bridge, as follows: SE3-SE1 = 17 (ERR-VREF)
ERR-	I	POSITION ERROR INVERTING INPUT - Inverting input to the loop compensation amplifier.
ERR+	I	POSITION ERROR NON-INVERTING INPUT - Non-inverting input to the loop compensation amplifier.
SOUT	O	MOTOR CURRENT SENSE OUTPUT - This output provides a voltage proportional to the voltage drop across the external current sense resistor, as follows: SOUT-VREF=4 (SE2-SE1)
BRK	O	BRAKE OUTPUT - Active high, open collector output which may be used to enable an external spindle motor braking transistor upon power failure. External resistor may be tied to +5 or +12V.
DISABLE	I	DISABLE DRIVERS INPUT – Logic level input. An input high level will cause all 4 bridge BIPOLAR Power Devices to turn off. DISABLE does not override retract.
$\overline{\text{RETRACT}}$	I	$\overline{\text{RETRACT}}$ INPUT – Logic level low will assert a forced head retraction. RETRACT will override DISABLE. $\overline{\text{RETRACT}}$ will continue to work at VCC=3.5V.
PS1	I	POWER SENSE 1 – 12V sense input to power fail comparator.
PS2	I	POWER SENSE 2 – 5V sense input to power fail comparator.
PFAIL	O	POWER FAIL – Power fail indicator open collector output. Floats if either supply goes below threshold.
1.3V	O	INTERNAL REFERENCE MONITOR - Used for testing purposes only.
A-COMP	O	AMPLIFIER A COMPENSATION - Compensation capacitor pin
B-COMP	O	AMPLIFIER B COMPENSATION - Compensation capacitor pin
C-COMP	O	AMPLIFIER C COMPENSATION - Compensation capacitor pin
D-COMP	O	AMPLIFER D COMPENSATION - Compensation capacitor pin

CONTROL (Continued)

NAME	TYPE	DESCRIPTION
SE2	I	MOTOR CURRENT SENSE INPUT - Non-inverting input to the current sense differential amplifier. It should be connected to one side of an external current sensing resistor in series with the motor. The inverting input of the differential amplifier is connected internally to SE1.

BIPOLAR DRIVE

SE3	I	MOTOR VOLTAGE SENSE INPUT - This input provides feedback to the non-inverting BIPOLAR driver amplifier. It is connected to one side of the motor. The gain to this point is: SE3-VREF = 8.5 (ERR-VREF)
SE1	I	MOTOR VOLTAGE SENSE INPUT - This input provides feedback to the inverting BIPOLAR driver amplifier. It is connected to the current sensing resistor which is in series with the motor. The gain to this point is: SE1 - VREF = -8.5 (ERR-VREF)
OUTA	O	PNP DRIVE (INVERTING) - Drive signal for a PNP power transistor connected between the current sense resistor and VCC. The PNP collector is also connected to SE1. Crossover protection circuitry ensures that the PNP and NPN devices driven by OUTA and OUTB are never simultaneously enabled.
OUTB	O	NPN DRIVE (INVERTING) - Drive signal for an NPN power transistor connected between the current sense resistor and GND. This NPN collector is also connected to SE1.
OUTC	O	PNP DRIVE (NON-INVERTING) - Drive signal for a PNP power transistor connected between one side of the motor and VCC. This PNP collector is connected to SE3. Crossover protection circuitry ensures that the PNP and NPN devices driven by OUTC and OUTD are never simultaneously enabled.
OUTD	O	NPN DRIVE (NON-INVERTING) - Drive signal for an NPN power transistor connected between one side of the motor and GND. This NPN collector is connected to SE3. Crossover protection circuitry ensures that the PNP and NPN devices driven by OUTC and OUTD are never simultaneously enabled.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

(Maximum limits indicates where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC operating characteristics.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VCC		0		16	V
VREF		0		10	V
+5V		0		7	V
SE1, SE2, SE3		-1.5		15	V
DISABLE, $\overline{\text{RETRACT}}$		-.3		+5V + .3	V
All other pins		-.3		VCC + .3	V
Storage temperature		-45		165	°C
Solder temperature	10 sec duration			260	°C

RECOMMENDED OPERATION CONDITIONS (Unless otherwise noted, the following conditions are valid throughout this document.)

VCC	Normal Mode	9	12	13.2	V
	Retract Mode	3.5V		13.2	V
+5V		4.5	5	5.5	V
VREF		4.5	5	5.5	V
Operating temperature		0		70	°C

DC CHARACTERISTICS

ICC, VCC current			13	20	mA
I5V, +5V Current			0.6	1	mA
IREF, VREF current			300		µA

A1, LOOP COMPENSATION AMPLIFIER

Input bias current				500	nA
Input offset voltage				3	mV
Voltage swing	About VREF		2		V
Common mode range	About VREF	±1			V
Load resistance	To VREF	4			kΩ
Gain			80		dB
Unity gain bandwidth			1		MHz
CMRR	f<20 kHz		60		dB
PSRR	f<20 kHz		60		dB

A2, CURRENT SENSE AMPLIFIER

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input impedance	SE1 to SE2	7.0	10		kΩ
Input offset voltage	SE1 = SE2 = VREF			2	mV
Output voltage swing		VREF-4		VCC-1.2	V
Common mode range		0		VCC-0.2	V
Load Resistance	To VREF	4			kΩ
Output impedance	f<40 kHz			20	Ω
Gain (SOUT-VREF)/(SE1-SE2)		1.95	2	2.05	V/V
Unity gain bandwidth			1		MHz
CMRR	f<20 kHz		52		dB
PSRR	f<20 kHz		60		dB

POWER SUPPLY MONITOR

1.3V pin voltage	1.3V pin open	1.18	1.25	1.31	V
PS1 threshold			1.25		V
PS2 threshold			1.25		V
PS1, PS2 Hysteresis			20		mV
PS1, PS2 Input Bias Current	PS1, PS2 = 1.3V		1		µA
PFAIL VOL	Linear mode IOC = 1mA			0.4	V
BRK VOL	Linear mode IOC = 1mA			0.4	V
PFAIL IOH	Retract mode VOH = 12V			10	µA
BRK IOH	Retract mode VOH = 12V			10	µA
DISABLE IIL	VIL = 0.8V		2	20	µA
$\overline{\text{RETRACT}}$ IIL	VIL = 0.8V		2	10	µA
DISABLE IIH	VIH = 2.4		1	10	µA
$\overline{\text{RETRACT}}$ IIH	VIH = 2.4		1	10	µA
DISABLE and $\overline{\text{RETRACT}}$ Threshold Voltage			1.4		V

6

BIPOLAR DRIVERS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SE3 Input Impedance	To VREF	10	25		kΩ
A Comp, C Comp Voltage Swing	w/ External Trans.	VCC - 1.4		VCC - .7	V
B comp, D Comp Voltage Swing	w/ External Trans.	0.7		1.4	V
Output Impedance A, B, C, D Comp	Output Off, No External Trans.		75		kΩ
Transconductance I (A, B, C, D Comp)/(ERR-VREF)			6		mA/V
Gain -(SE1-VREF)/(ERR-VREF) or (SE3-VREF)/(ERR-VREF)	Includes External Trans.	8	8.5	9	V/V
Offset Current (A2 Vos)	Rs = 0.5Ω Rf = Rin Vin = Vref		3.5		mA
Retract Motor Voltage (SE1-SE3)		0.7	1.3	1.7	V
Out B, Out D Source Current	Vout = 0.8V	20			mA
Out B, Out D Current Limit	Vcc = 10.8V, Out B, D = 0.8V Vcc = 12.0V, Out B, D = 0.8V	20 23	25 27	30 33	mA mA
Out A, Out C Sink Current	Vout = 11.2V	20			mA
B and D Output NPN Output Transistor Beta	Ic = 20mA Vce = 10V		20		V/V
A and C Output PNP Output Transistor Beta	Ic = 20mA Vce = 10V		10		V/V

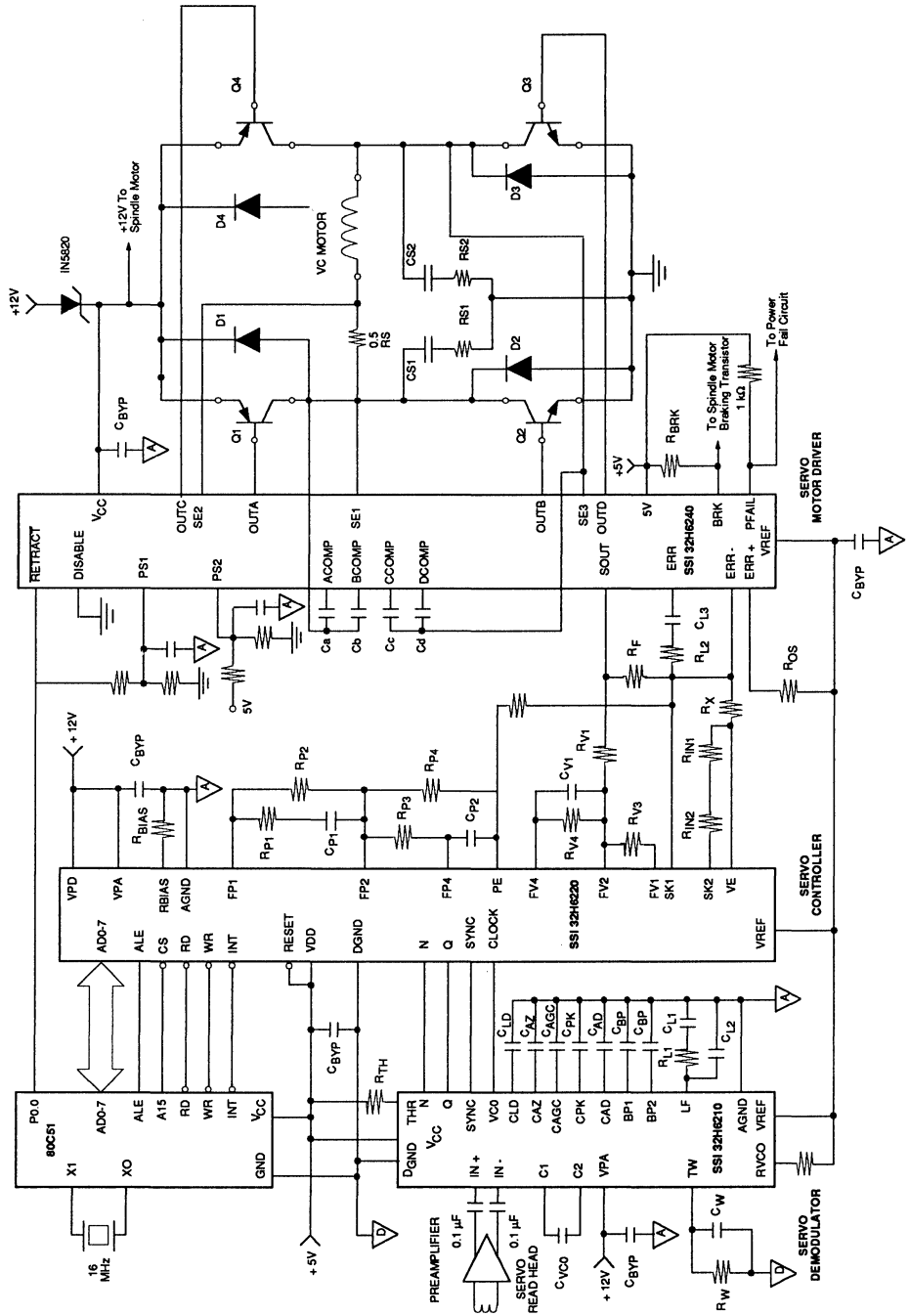
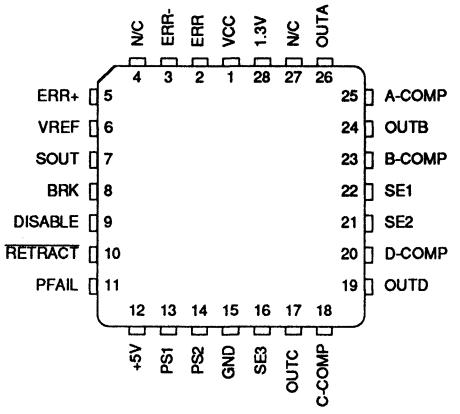


FIGURE 3: Complete Example of Servo Path Electronics using the SSI 32H567/6220/6240 Chip Set

6

PACKAGE PIN DESIGNATIONS
(TOP VIEW)

CAUTION: Use handling procedures necessary for a static sensitive component.



28-Pin PLCC

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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SSI 32H6510
5V Servo Driver

Advance Information

November 1991

DESCRIPTION

The SSI 32H6510 is a fully integrated power amplifier for use in disk drive head positioning systems employing linear or rotary voice coil motors. It is intended for use in 5V systems and is capable of generating ±1 Amp motor currents. The part is internally thermal overload protected.

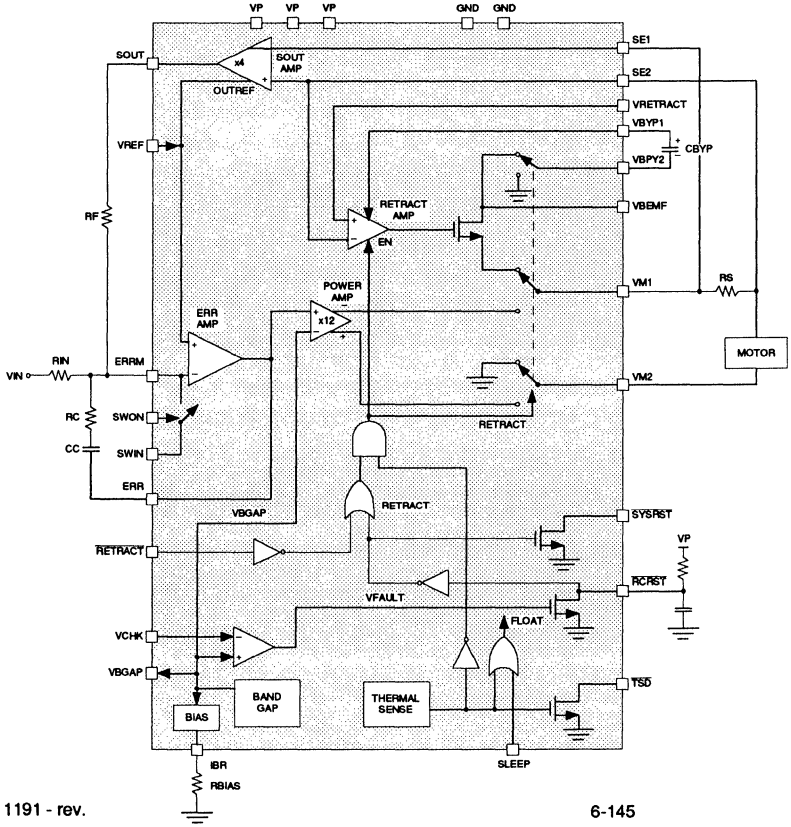
The SSI 32H6510 is a power transconductance amplifier for use in driving voice coil type servo motors (VCMs). The SSI 32H6510 has two primary modes of operation, normal (or linear) and retract. The retract mode is activated by a power supply failure or when $\overline{\text{RETRACT}}$ is asserted. Otherwise the device operates in linear mode.

FEATURES

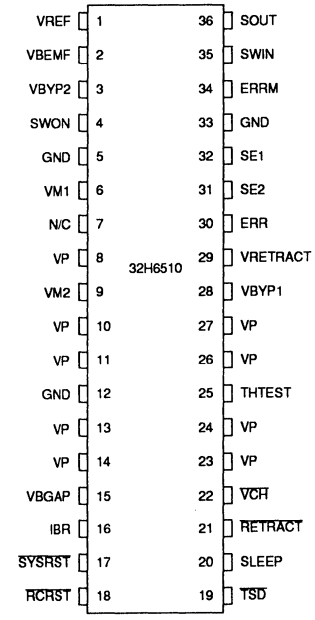
- **36-pin SO package**
- **Internal 1A power devices**
- **NMOS output stage**
- **Total on resistance less than 1.3Ω at 500 mA**
- **Thermal overload protection**
- **No deadband, low distortion, class B output**
- **Low power sleep mode**
- **Gain select switch optimizes performance with 8-bit DACs**
- **Built in retract circuitry**
- **Power fault detection**

6

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

DESCRIPTION (continued)

The SSI 32H6510 consists of five major blocks: SOUT amplifier, ERR amplifier, retract amplifier, power amplifier, and control circuitry. These parts are each described in this section. External components needed for proper operation of the SSI 32H6510 are also described.

SOUT AMPLIFIER

This amplifier generates a voltage at SOUT that is proportional to positioner current. It does this by sensing the voltage across Rs, amplifying it, and referencing the result to VREF. Since the common mode voltage on Rs can range over the full power supply, while the differential voltage is a few millivolts, the SOUT amplifier is designed to have very high input common mode rejection, and very low input offset.

ERR AMPLIFIER

The ERR amplifier is a high gain op amp. Due to the fixed gain of the power amp, ERR is proportional to the VCM voltage. The negative input of this amplifier is the system summing junction--currents proportional to the desired VCM current, the measured VCM current, and the VCM voltage are summed here.

POWER AMPLIFIER

The power amplifier is a fixed gain voltage amplifier with differential inputs and outputs. Its input is the differential voltage between ERR and VBGAP. Its output drives the VCM directly.

RETRACT AMPLIFIER

When a voltage fault is sensed, or when $\overline{\text{RETRACT}}$ is asserted, the SSI 32H6510 enters retract mode. In this mode, it is assumed that no current is available from VP (VP may actually be at GND potential). Thus power for this mode comes from VBEMF, the rectified spindle back EMF voltage, and from VBYP1, a voltage generated from the external storage capacitor CBYP. The retract amplifier is powered by VBYP1. It senses the voltage at VRETRACT and raises VM1 to be equal to VRETRACT. The drain of the source follower is VBEMF.

CONTROL CIRCUITRY

The control circuitry consists of voltage monitoring circuitry, a thermal overload circuit, and control logic. The inputs to the control circuitry are the external signals $\overline{\text{RETRACT}}$, VCHK, and SLEEP, along with internal signal from the thermal overload detector (visible externally on TSD). Table 1 describes the behavior of the part in response to these inputs.

TABLE 1: IC Mode Selection

INPUT				CHIP FUNCTION		
SLEEP	$\overline{\text{RETRACT}}$	VCHK>VBGAP	$\overline{\text{TSD}}$	BRIDGE	RETRACT	$\overline{\text{SYSRST}}$
X	X	0	0	Off	Off	0
X	X	0	1	Off	On	0
X	X	1	0	Off	Off	1
X	0	1	1	Off	On	1
0	1	1	1	On	Off	1
1	1	1	1	Off	Off	1

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
VP	Power	The positive power supply. The VP pins are thermally connected to the die and provide a low thermal resistance path to the circuit board. All VP pins should be shorted together.
GND	Power	The negative power supply. All GND pins should be shorted together.
SWON	Dig In	Turns on the switch between ERRM and SWIN.
SWIN	An In	One side of an analog switch connected to ERRM.
SOUT	An Out	The current sense amplifier output. SOUT is referenced to VREF.
ERR	An Out	The error amplifier output. ERR is used to provide compensation to the transconductance loop. ERR is referenced to VBGAP.
ERRM	An In	The error amplifier negative input.
VREF	An In	The reference voltage for the error amplifier and the current sense amplifier.
$\overline{\text{RETRACT}}$	Dig In	When low, forces a retract.
THTEST	Dig In	Test input.
VCHK	An In	Comparator input for power supply monitoring. When VCHK is below VBGAP, an internal voltage fault is generated.
VBGAP	An Out	An internal voltage reference for use with the power supply monitor comparator.
IBR	An Out	A resistor is tied from this pin to ground to establish the bias current for internal circuitry.
SLEEP	Dig In	Turns off the output drivers. Does not override the retract function when a voltage fault occurs. Powers down all but the voltage monitor and retract circuitry.
$\overline{\text{TSD}}$	O/C Out	Thermal Shut Down. When low, this open collector output indicates that the junction temperature has exceeded the recommended operating range and that the part is in thermal shutdown.
$\overline{\text{RCRST}}$	O/C Out	This pin serves the dual purpose of providing power-on-reset and stretching short VFAULT pulses to a width suitable for the host microcontroller. An external RC network sets the minimum width of any $\overline{\text{SYSRST}}$ pulse.
$\overline{\text{SYSRST}}$	O/C Out	When low, this open collector output indicates that an internal voltage fault has occurred.
VRETRACT	An In	The retract voltage. Supplied externally by a diode reference.
VBYP1	An In	The bypassed power supply. An external capacitor is connected to this node to store charge for use by the retract circuitry.
VBYP2	An In	The other side of the bypass capacitor is connected here.
VBEMF	An In	Rectified spindle back emf voltage. This input provides current to the internal retract power FET.

PIN DESCRIPTION (continued)

NAME	TYPE	DESCRIPTION
VM2	An Out	One side of the voice coil motor.
VM1	An Out	The other side of the voice coil motor and sense resistor combination.
SE1, SE2	An In	The sense voltages around the sense resistor.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation of the part outside these limits may result in degradation or failure of the device.

PARAMETER	RATING	UNITS
Power Supply, VP	7	V
Voltage on any pin		
VBEMF, VBYP1, VBYP2, $\overline{\text{SYSRST}}$, $\overline{\text{RCRST}}$	-0.3 to 16	V
VM1, VM2, SE1, SE2	-0.3 to 12	V
All others	-0.3 to VP+.3	V
Storage Temperature	-45 to 165	°C
Solder Temperature (10 sec duration)	260	°C
Output Current - I(VM1), I(VM2)	2	Amp
Junction Temperature	150	°C

RECOMMENDED OPERATING CONDITIONS

The performance specifications for this part apply only when the operating environment is within this specified range.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Power Supply, VP		4.75		5.25	V
Junction Temperature		0		125	°C
Output Current - I(VM1), I(VM2)				1.0	Amp
VBEMF		1.0		14	V
VREF		0.5		VP-2	V
RF		10			kΩ
RC		10			kΩ
RBIAS		21.5		22.5	kΩ
VBYP1 - Retract Mode		3		14	V

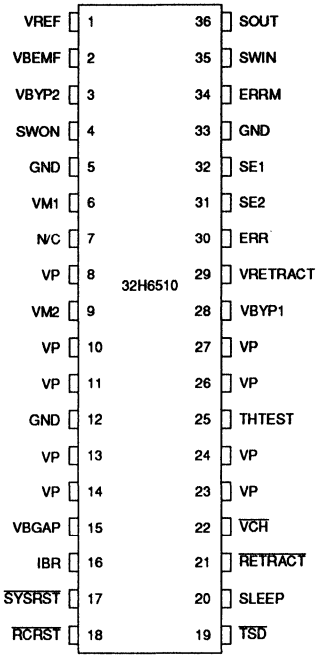
PERFORMANCE SPECIFICATIONS

DESCRIPTION	CONDITIONS	MIN	NOM	MAX	UNITS
VP Supply Current:					
Normal operation, Imotor = 0				15	mA
Sleep mode				2	mA
SOUT gain		3.9		4.1	V/V
SOUT input offset (SOUT = VREF)		-3		3	mV
SOUT output swing		0.15		VP-1	V
ERRM input offset (ERR = ERRM)		-10		10	mV
ERR output swing		1.6		3.25	V
GAIN (VM1-VM2)/(ERR-VBGAP)		11		13	V/V
VBGAP		2.13		2.37	V
VCHK offset		-15		15	mV
Retract offset					
VRETRACT = 0.5V		-50		50	mV
VRETRACT input impedance		500			kΩ
Output voltage drop: VP-|VM1-VM2|					
Imotor = ± 0.5A, Tj = 25°C				0.65	V
Imotor = ± 0.1A, Tj = 25°C				0.15	V
Thermal shutdown temperature		120		140	°C
Thermal shutdown hysteresis		3		7	°C
Crossover time					
Imotor = 10mA p 1000 Hz				45	µs
Crossover distortion					
Imotor = 10mA p 1000 Hz				2	%THD
Digital open collector output, sink current:					
$\overline{\text{SYSRST}}$, $\overline{\text{RC\_RST}}$, $\overline{\text{TSD}}$					
Vol = 0.4V		1.6			mA
SWIN on resistance				250	Ω

6

PACKAGE PIN DESIGNATIONS

(Top View)



36-Lead SOM

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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SSI 32H6520
Embedded Servo Controller

Advance Information

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DESCRIPTION

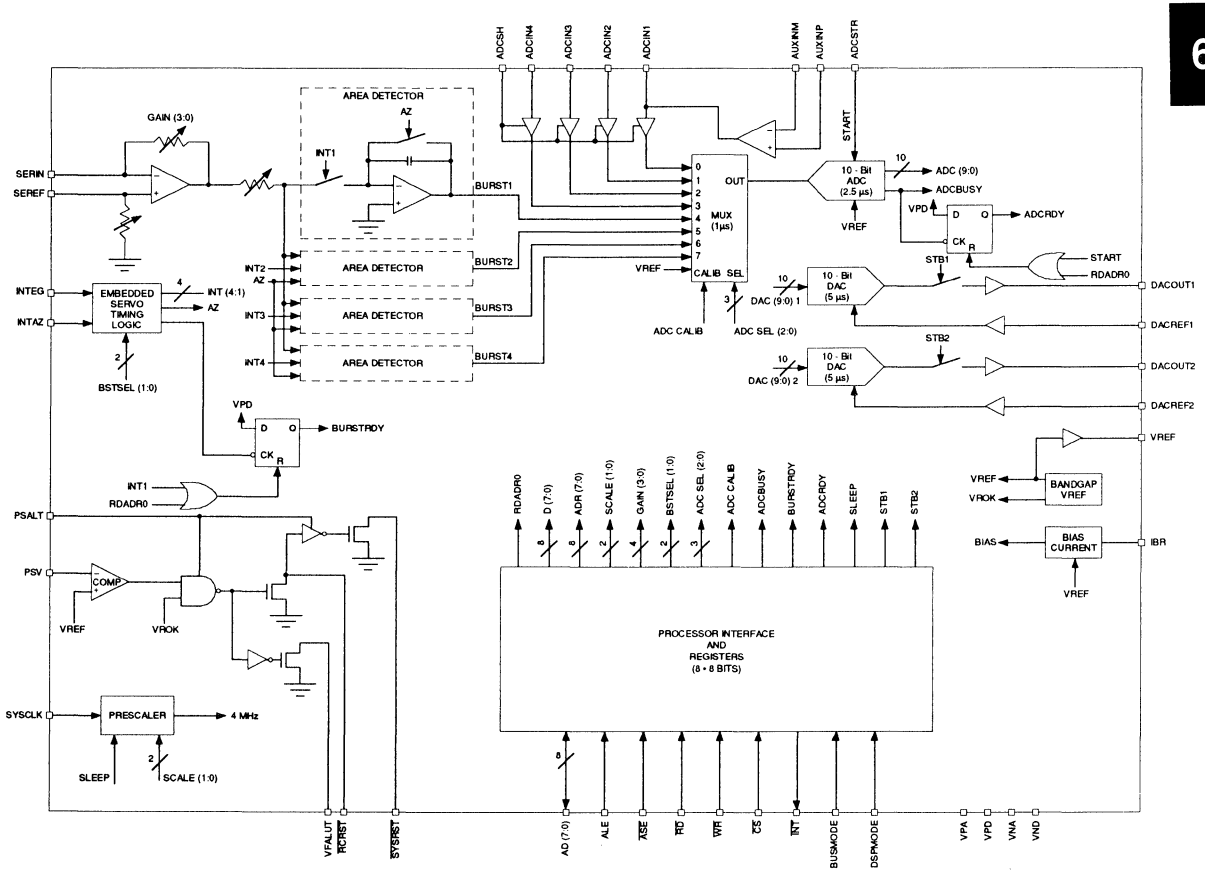
The 32H6520 Embedded Servo Controller is a CMOS monolithic integrated circuit housed in a 44-pin SO and operates on a single +5.0 volt supply. It provides one 10-bit A/D converter with 2.5 µs conversion time, and two 10-bit D/A converters with 5 µs conversion time as well as Motorola/Intel compatible bus interface (Motel) to commonly used microcontrollers such as 80C196 and 68HC11. In addition, it includes bus interface logic to support DSP-based, such as TMS320XX, digital servo applications. The features for each functionally different section are summarized as follows:

Embedded Servo Burst Processor

- Servo control for Winchester disk drives with embedded servo sectors
- For use in µP/DSP-based digital servo applications
- Pulse area detects and S/H circuits for up to four embedded servo bursts
- Programmable gain adjustment from -2.8 dB to 3.2 dB

(continued)

BLOCK DIAGRAM



DESCRIPTION (continued)

Data Acquisition and Microprocessor/DSP Bus Interface

- Motel bus interface compatible with 80C196 and 68HC11
- Bus interface logic to support DSP-based digital servo applications
- Eight internal registers and address decoding
- Two 10-bit D/A converters with 5 µs conversion time
- One 8-channel 10-bit A/D converter with 2.5 µs conversion time

General Functions

- Voltage fault detection
- Low power CMOS design
- 44-pin SO package

FUNCTIONAL DESCRIPTION

The 32H6520 can be divided into four major sections: embedded servo burst processor, voltage fault detector/logic, data acquisition and microprocessor/DSP bus interface.

EMBEDDED SERVO BURST PROCESSOR

The embedded servo burst processor extracts the head position error information from the embedded servo bursts using an area detection technique. The area detection technique provides improved noise immunity over peak detector. The embedded servo burst processor contains a differential/gain amplifier, four pulse area detectors and required timing logic. First, a full wave-rectified analog signal from a read data channel, such as SSI 32P4620, is provided at SERIN through an external resistor equal to Rint and a DC reference level for the full wave-rectified analog signal at SEREF through another external resistor equal to Rint. To accommodate a wide dynamic range of servo burst amplitudes and process variations of the integration capacitor Cint, the differential signal between SERIN and SEREF is scaled under µP control. The gain of the differential amplifier ranges from -2.8 dB to 3.2 dB in a step of 0.4 dB, as defined in the SERVO GAIN CONTROL register. The output of the differential/gain amplifier is then provided to four pulse area detectors whose output are proportional to the area above the DC reference level during time intervals defined by an external timing source through INTEG. Each area detector applies an on-chip capacitor Cint equal to 10 pF to integrate the incoming pulses during the integration interval and then hold the integrated voltage outputs thereafter. Note that the max ±20% tolerance of on-chip capacitors can be calibrated out by adjusting the gain of the preceding amplifier. Finally, the integrated voltage outputs at BURST1, BURST2, BURST3 and BURST4 are provided to a 10–bit A/D converter under µP control and will be discharged during a time interval defined by an external timing source through INTAZ. For proper operatons, the time interval defined by the INTAZ must be no less than 0.5 µs and be applied only once per servo frame preceding the integration pulses defined by the INTEG.

Limited timing logic is included to generate all the timing signals required for the embedded servo burst processor, per figure 1. These timing signals control the integration, sample/hold of the pulse area detectors. The number of embedded servo bursts supported by this circuit are two, three or four. The BSTSEL0 and BSTSEL1 bits in the SERVO CONTROL register configure the internal timing logic to generate a servo burst ready interrupt after the last servo burst is captured.

VOLTAGE FAULT DETECTOR/LOGIC

The voltage fault detector is to monitor the power supply applied at PSV through an external resistor divider, which defines the trigger level for power supply failure. An open-drain output VFAULT is pulled HIGH by an external resistor when a power supply failure is sensed by the PSV comparator. The user-defined trigger level for voltage failure is applied at PSV. Another open-drain output, opposite logic polarity as the pin VFAULT and with an additional RC delay, is provided at $\overline{\text{SYSRST}}$. The amount of $\overline{\text{SYSRST}}$ delay is determined by an external RC connected to the pin, $\overline{\text{RCRST}}$.

DATA ACQUISITION

The A/D converter is multiplexed to eight different analog inputs by programming the ADC SEL0, ADC SEL1, and ADC SEL2 bits in the ADC ADDRESS register by the µP. The eight analog inputs multiplexed to the A/D converter are four embedded servo processor outputs at BURST1, BURST2, BURST3 and BURST4 and four external analog inputs through four T/H amplifiers. These T/H amplifiers sample external

DATA ACQUISITION (continued)

analog inputs during the time interval defined by an external timing source applied at ADCSH. If the sampling of four external analog inputs is not necessarily synchronized, ADCSH must be tied to HIGH. The A/D conversions on these external analog inputs are always referenced to the internal voltage reference at 2.25 volts. An operational amplifier with uncommitted inputs is provided to implement a level shifting function for the external analog input applied to AUXINP. The output of the operational amplifier is tied to ADCIN1.

The A/D converter starts to acquire a new analog input whenever the conversion is completed. A minimum of 1 µs is required to acquire an analog input to the A/D converter. Actual conversion is started by reading the A/D MSB register or by an external timing source applied to ADCSTR. The A/D address lines ADC SEL0, ADC SEL1, and ADC SEL2 will be incremented by one after the A/D conversion is started. The automatic increment of the address lines is employed to eliminate repetitive write operations by the µP to the ADC ADDRESS register required for converting the consecutive analog inputs.

The A/D converter runs synchronously with the internal 4 MHz clock which is used for various circuits on the 32H6520 and divided down from the system clock SYSCLK by a prescaler. Therefore there would be a maximum of 0.25 µs of latency between a conversion request and the actual start of the conversion. The output is coded in 2's complement.

Similarly, the D/A converters run synchronously with the internal 2 MHz clock and the conversion is started by writing to the corresponding D/A input register. The output of the first D/A converter is referenced to an external analog input, DACREF1 and the output of the second D/A converter is referenced to an external analog input, DACREF2. In the "normal" mode when STBEN1 (STBEN2) bit in the ADC ADDRESS register is reset, the D/A output will be automatically applied to DACOUT1 (DACOUT2) during the conversion. In the "strobe" mode, the D/A output will be applied to DACOUT1 (DACOUT2) at the falling edge of $\overline{RD}$ for a read to the corresponding D/A MSB DATA register.

MICROPROCESSOR/DSP BUS INTERFACE

The 32H6520 is provided with Motorola/Intel compatible bus interface for a direct connection to popular microcontrollers such as 80C196 and 68HC11. It also contains logic to interface with TMS320XX for DSP-based servo applications. Bus control signals ALE, $\overline{RD}$, $\overline{WR}$ and BUSMODE are interpreted differently, as described in table 1, based upon the type of processors being used. When the 32H6520 is interfaced with TMS320XX, the pin DSPMODE must be tied to HIGH and the pin BUSMODE is redefined as XFER/$\overline{SEL}$. The pin BUSMODE must be tied to HIGH for an Intel bus interface and LOW for a Motorola bus interface. The $\overline{ASE}$ pin gates the ALE/AS input and can be used to shut off the ALE/AS to minimize noise on the chip when the µP interface is not active. The $\overline{CS}$ pin performs a similar function on the rest of the µP bus inputs. The timing diagrams for different processors are depicted in Figures 2, 3 and 4.

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TABLE 1: Microprocessor/DSP Bus Interface

32H6520	Intel	Motorola	TMS320XX
DSPMODE	LOW	LOW	HIGH
BUSMODE	HIGH	LOW	XFER/$\overline{SEL}$ (PA0)
$\overline{CS}$	$\overline{CS}$	$\overline{CS}$	$\overline{CS}$ (PA1)
ALE	ALE	AS	N/C
$\overline{RD}$	$\overline{RD}$	DS;E; or Clock Phase 2	$\overline{REN}$
$\overline{WR}$	$\overline{WR}$	R/$\overline{W}$	$\overline{WE}$

REGISTER DESCRIPTIONS

The 32H6520 contains eight 8-bit internal registers which provide control, option select and status monitoring. The registers are addressed with a 3-bit register address which is latched from inputs at AD0(LSB), AD1, and AD2(MSB) at the falling edge of ALE. The registers 0, 2, and 3 are read/write memory, and the registers 1, 4, 5, 6, and 7 are write only memory. The registers are summarized in Table 2.

TABLE 2: Register Descriptions

ADDRESS	TYPE	REGISTER NAME
0	R/W	INTERRUPT MASK/STATUS
1	W	SERVO GAIN CONTROL & PRESCALER
2	R/W	ADC LSB DATA
3	R/W	ADC ADDRESS & MSB DATA
4	W	DAC1 LSB DATA
5	W	DAC1 MSB DATA
6	W	DAC2 LSB DATA
7	W	DAC2 MSB DATA

INTERRUPT MASK/STATUS REGISTER

Address: 0
Access: Read/Write
Reset: Bit 0, 1 only

Register contents when Written:

BIT	NAME	DESCRIPTION
0	BURST INT	When set HIGH, interrupt is enabled on the embedded servo position bursts ready.
1	ADC INT	When set HIGH, interrupt is enabled on the completion of the A/D conversion.
2 - 7		Unused.

Register contents when Read:

BIT	NAME	DESCRIPTION
0	BURSTRDY	Active high indicates that the embedded servo bursts are ready.
1	ADCRDY	Active high indicates that the A/D conversion is completed.

Each interrupt event status will be reset after the µP reads this register. The interrupt control register determines if the event will actually cause a latched assertion of the µP signal $\overline{INT}$.

SERVO GAIN CONTROL & PRESCALER REGISTER

Address: 1
Access: Write
Reset: 00

BIT	NAME	DESCRIPTION
0 1	SCALE0 SCALE1	SYSCLK Prescaler. To accommodate different system clocks, the prescaler selects a proper divider to generate a fixed clock at 4 MHz per table below:

SCALE1	SCALE0	SYSCLK(MHz)	Divider
0	0	16	4
0	1	12	3
1	0	8	2
1	1	4	1

BIT	NAME	DESCRIPTION
2 3 4 5	GAIN0 GAIN1 GAIN2 GAIN3	Servo Burst Amplitude Gain Select. These four bits define the gain setting for the differential/gain amplifier per table below:

GAIN3	GAIN4	GAIN3	GAIN0	Gain, dB
0	0	0	0	-2.8
0	0	0	1	-2.4
0	0	1	0	-2.0
0	0	1	1	-1.6
0	1	0	0	-1.2
0	1	0	1	-0.8
0	1	1	0	-0.4
0	1	1	1	+0.0
1	0	0	0	+0.4
1	0	0	1	+0.8
1	0	1	0	+1.2
1	0	1	1	+1.6
1	1	0	0	+2.0
1	1	0	1	+2.4
1	1	1	0	+2.8
1	1	1	1	+3.2

BIT	NAME	DESCRIPTION
6 7	BSTSEL0 BSTSEL1	Burst Number Select. These two bits define the number of embedded servo bursts per sector.

BSTSEL1	BSTSEL0	# of Bursts
0	0	2
0	1	3
1	0	4

ADC LSB DATA REGISTER

Address: 2
Access: Read/Write
Reset: Bit 5, 6, 7 only

Register contents when Written:

BIT	NAME	DESCRIPTION
0 - 4		Unused.
5	SLEEP	Power-down Mode Enable. When set HIGH, the device is in the sleep mode where all analog circuitry are de-biased, the clock is disabled, and the bandgap voltage, reference voltage fault logic and processor interface stay active.
6	STBEN1	When set HIGH, the analog output of the DAC1 is transferred and held onto DACOUT1.
7	STBEN2	When set HIGH, the analog output of the DAC2 is transferred and held onto DACOUT2.

Register contents when Read:

Description: After A/D conversion, the least significant 2 bits of the 10-bit digital word is stored into the register.

0 - 5		Unused. Logic LOW is provided to these bits.
6,7	ADC0, ADC1	The LSB 2 bits of the A/D converter output in 2's complement format.

ADC ADDRESS & MSB DATA REGISTER

Address: 3
Access: Read/Write
Reset: Bits 0, 1, 2, and 3 only

Description: When Written, the least significant 3 bits of the register define the analog input to the 10-bit A/D converter. After conversion, the most significant 8 bits of the 10-bit digital word is stored into the register.

Register contents when Written:

0 1 2	ADC SEL0 ADC SEL1 ADC SEL2	A/D Converter Input Select. These 3 bits define the analog input to the A/D converter per table below:

BIT2	BIT1	BIT0	ADC INPUT
0	0	0	ADCIN1
0	0	1	ADCIN2
0	1	0	ADCIN3
0	1	1	ADCIN4
1	0	0	BURST1
1	0	1	BURST2
1	1	0	BURST3
1	1	1	BURST4

ADC ADDRESS & MSB DATA REGISTER (continued)

BIT	NAME	DESCRIPTION
3	ADC CALIB	When set HIGH, VREF (2.25 volts) is applied to the A/D converter input.
4 - 7		Unused.

Register contents when Read:

0 - 7	ADC2 - 9	The MSB 8 bits of the A/D converter output in 2's complement. ADC9 is the sign bit.

DAC1 LSB DATA REGISTER

Address: 4
Access: Write
Reset: 00

0 - 5		Unused.
6, 7	DAC0, DAC1	The LSB 2 bits to the DAC1 in 2's complement.

DAC1 MSB DATA REGISTER

Address: 5
Access: Write
Reset: 00

0 - 7	DAC2 - 9	The MSB 8 bits to the DAC1 in 2's complement, DAC9 is the sign bit.

DAC2 LSB DATA REGISTER

Address: 6
Access: Write
Reset: 00

0 - 5		Unused.
6 7	DAC0, DAC1	The LSB 2 bits to the DAC2 in 2's complement.

DAC2 MSB DATA REGISTER

Address: 7
Access: Write
Reset: 00

0 - 7	DAC2 - 9	The MSB 8 bits to the DAC2 in 2's complement. DAC9 is the sign bit.

PIN DESCRIPTION

POWER SUPPLIES

NAME	DESCRIPTION
VPA	Analog +5V supply.
VPD	Digital +5V supply. It must be shorted to analog +5V supply externally.
VNA	Analog ground.
VND	Digital ground. It must be shorted to analog ground externally.
PSALT	Alternate Voltage Supply to power the voltage fault logic during a voltage fault. This power supply should be taken from the system +5V supply through a Schottky diode and be connected to a capacitor, which is used to hold up PSALT briefly during a voltage fault.

EMBEDDED SERVO BURST PROCESSOR

NAME	TYPE	DESCRIPTION
SERIN	I	Servo Burst Input - Full-wave rectified analog signal generated from a read data channel. This input is to extract the position information from embedded servo bursts.
SEREF	I	Servo Burst Reference - A DC reference level for the full-wave rectified analog signal SERIN.
INTEG	I	Pulse Area Detector Enable - This TTL compatible input, when HIGH, activates the pulse area detectors.
INTAZ	I	Integrator Capacitor Reset - This TTL compatible input, when HIGH, discharges the holding capacitors, Cint.

VOLTAGE FAULT DETECTION

PSV	I	Fault Voltage Comparator Input - A voltage input for the low voltage comparator. This input should be connected to an external resistor divider. The resistor divider divides its corresponding supply voltage to a proper value which is comparable with the internal voltage reference at 2.25 volts.
VREF	O	VREF Output - A buffered voltage reference at 2.25 volts.
IBR	O	Pin for connection to an external resistor (from GND) to establish a reference current for bias currents required for analog circuits.
VFAULT	O	Voltage Fault Indication - An open-drain output which is pulled HIGH when a supply voltage fault is detected.
$\overline{\text{SYSRST}}$	O	Reset Output - An open-drain output which is pulled LOW with an amount of delay determined by an external RC connected to the pin RCRST when a supply voltage fault is detected.
$\overline{\text{RCRST}}$	O	Pin for connection to an external RC to implement the delay of active LOW $\overline{\text{SYSRST}}$.

MICROPROCESSOR/DSP BUS INTERFACE

NAME	TYPE	DESCRIPTION
ALE	I	Address Latch Enable - Falling edge latches the register address from the AD0 - AD7 address/data bus.
$\overline{ASE}$	I	Address Strobe Enable - When set LOW, this input enables ALE input to the device.
$\overline{CS}$	I	Chip Select - Active LOW signal enables the device to respond to µP read or write.
$\overline{WR}$	I	Write Strobe - In Intel µP applications, active LOW signal causes the data on the address/data bus to be written to the addressed register if $\overline{CS}$ is also active.
$\overline{RD}$	I	Read Strobe - In Intel µP applications, active LOW signal causes the contents of the addressed register to be placed on the address/data bus if $\overline{CS}$ is also active.
AD0 - AD7	I/O	Address/Data Bus - 8-bit bus which carries register address information and bidirectional data. These pins are in the high impedance state when not used.
BUSMODE	I	Mode Select - When active HIGH, Intel bus interface is selected. Otherwise, Motorola bus interface is selected. For DSP interface, when DSPMODE set HIGH, this input is redefined as XFER/$\overline{SEL}$.
$\overline{INT}$	O	Interrupt Strobe - An open-drain output which signals the µP to respond to the device. It is released when all pending interrupts have been serviced by the µP.
DSPMODE	I	DSP Mode Select - When active HIGH, DSP bus interface is selected.
SYSCLK	I	System Clock Input - A TTL compatible input for the system clock which is divided down with a prescaler to generate internal timing signals.

DATA ACQUISITION

DACOUT1	O	DAC1 Output - A 10-bit D/A output which converts a digital word from the µP into an analog signal.
DACREF1	I	DAC1 Output Reference - An external analog input to be provided to DAC1 as a reference voltage for DACOUT1.
DACOUT2	O	DAC2 Output - A 10-bit D/A output which converts a digital word from the µP into an analog signal.
DACREF2	I	DAC2 Output Reference - An external analog input to be provided to DAC2 as a reference voltage for DACOUT2.
ADCIN1 ADCIN2 ADCIN3 ADCIN4	I	External A/D inputs.
ADCSH	I	A/D Analog Sampling Input Strobe - A TTL compatible control signal. During active HIGH, four track/hold amplifiers prior to the A/D converter will sample external A/D analog inputs.

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DATA ACQUISITION (continued)

NAME	TYPE	DESCRIPTION
ADCSTR	I	A/D Conversion Start Strobe - A TTL compatible control signal whose rising edge triggers the start of the A/D conversion.
AUXINP	I	Level Shifter Noninverting Input - Noninverting input to the level-shifting amplifier.
AUXINM	I	Level Shifter Inverting Input - Inverting input to the level-shifting amplifier.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device or affect device reliability.

SYMBOL	PARAMETER	RATING	UNIT
VDD	Supply voltage applied at VPA, VPD	-0.3 to 7.0	V
GND	Signal ground applied at VNA, VND	0.0	V
PSALT	Supply voltage applied at PSALT	-0.3 to 7.0	V
VIND	Digital input voltages	-0.3 to VDD+0.3	V
VINA	Analog input voltages	-0.3 to VDD+0.3	V
Tstg	Storage temperature	-65 to 150	°C
TI	Lead temperature (10 seconds)	300	°C

RECOMMENDED OPERATING CONDITIONS

The recommended operating conditions for the device are indicated in the table below. Performance specifications do not apply where the device is operating outside these limits.

SYMBOL	PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VDD	Supply voltage applied at VPA, VPD		4.75		5.25	V
GND	Signal ground applied at VNA, VND		0.0		0.0	V
PSALT	Supply voltage applied at PSALT		3.0		6.0	V
TA	Ambient temperature		0.0		70.0	°C
Fc	System clock (16MHz, Max)		-0.01		+0.01	%
Tc	System clock duty cycle		40		60	%

RECOMMENDED OPERATING CONDITIONS (continued)

SYMBOL	PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
CLOAD	Capacitive load on digital outputs		-		100	pF
RBIAS	Bias resistor (113 kΩ)		-1		+1	%

DC CHARACTERISTICS

The following electrical specifications apply to the digital input and output signals over the recommended operating range unless otherwise noted. Positive current is defined as entering the device. Minimum and maximum are based upon the magnitude of the number.

IDD	Supply current Normal mode Sleep mode	VDD = 5.25V	 - -		 20 2	 mA mA
Voh	Output logic "1" voltage	Ioh = -0.4mA VDD = 4.75V	2.4		-	V
Vol	Output logic "0" voltage	Iol = 1.6mA VDD = 4.75V	-		0.4	V
Vih	Input logic "1" voltage	VDD = 4.75V	2.0		-	V
Vil	Input logic "0" voltage	VDD = 4.75V	-		0.8	V
Iih	Input logic "1" current	Vih = 5.25V VDD = 5.25V	-		10	µA
Iil	Input logic "0" current	Vil = 0.0 VDD = 5.25V	-		-10	µA
Cin	Input capacitance		-		10	pF

FUNCTIONAL CHARACTERISTICS

EMBEDDED SERVO BURST AMPLITUDE PROCESSOR

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
SERIN with respecet to GND		1.0	-	VDD	V
SEREF with respecet to GND		1.0		3.0	V
SERIN input voltage swing with respect to SEREF	Servo gain = -2.8 dB Servo gain = 0 dB	0.0 0.0	- -	1.5 1.0	Vp Vp
Servo burst frequency		1.0	-	5.0	MHz
Input impedance at		40	-	-	kΩ
SERIN, SEREF		-	-	10	pF
Burst integration period	Integrates to within 1% of final value	1.0			µs

FUNCTIONAL CHARACTERISTICS (conditions)

VOLTAGE REFERENCE AND VOLTAGE FAULT CIRCUIT

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VPA voltage for $\overline{\text{SYSRST}}$ & RCRST in operation		2	-	5.25	V
On resistance at RCRST		-	-	600	Ω
RCRST input threshold	PSALT=4V	0.8	-	1.2	V
IBR voltage with respect to VREF		-20	-	20	mV
VREF voltage	|I| <10µA	2.14	-	2.36	V
VREF trimming steps TRIM1='0' TRIM0='0' TRIM1='0' TRIM0='1' TRIM1='1' TRIM0='0'	relative to TRIM0=TRIM1='1'	 - - -	 -30 +70 -90	 - - -	 mV mV mV
PSV comparator offset		-15	-	15	mV

DATA ACQUISITION

A/D Converter

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
ADCIN full-scale voltage with respect to VREF		-	± (VREF/2)	-	V
Resolution		-	10	-	Bits
Acquisition time		-	-	1.0	µs
Conversion time		-	-	2.5	µs
LSB voltage		-	VREF/1024	-	V
Differential nonlinearity		-	-	±0.5	LSB

D/A Converter

DAC full-scale voltage with respect to DACREF		-	±(VREF/2)	-	V
Resolution		-	10	-	Bits
Conversion time		-	-	5.0	µs
LSB voltage		-	VREF/1024	-	V
Differential nonlinearity		-	-	±0.5	LSB
DACREF1, DACREF2		1.5		2.25	V
DACOUT1, DACOUT2		0.5		3.375	V

Intel Microprocessor Interface Timing

The following timing specifications are applied when an Intel bus interface is selected by pulling the BUSMODE pin to logical HIGH and the DSPMODE pin to logical LOW. Timing measurements are made at 50% VDD with 100 pF load capacitances for all pins, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
t_{ALPW}	Pulse width, ALE HIGH		45		-	ns
t_{AS}	Muxed address valid time to ALE fall		7.5		-	ns
t_{AH}	Muxed address hold time after ALE fall		20		-	ns
t_{DDR}	Read data delay time from $\overline{RD}$ fall		-		60	ns
t_{DHR}	Read data hold time after $\overline{RD}$ rise		0		50	ns
t_{RDPW}	Pulse width, $\overline{RD}$ LOW		75		-	ns
t_{DSW}	Write data setup time to $\overline{WR}$ rise		40			ns
t_{DHW}	Write data hold time after $\overline{WR}$ rise		10		-	ns
t_{WRPW}	Pulse width, $\overline{WR}$ LOW		50		-	ns
t_{RWD}	$\overline{RD}$ or $\overline{WR}$ delay time from ALE fall		25		-	ns
t_{CSS}	$\overline{CS}$ setup time prior to ALE fall		0		-	ns
t_{CSH}	$\overline{CS}$ hold time after $\overline{RD}$ or $\overline{WR}$ rise		0		-	ns
t_{ASES}	$\overline{ASE}$ setup time prior to ALE fall		45		-	ns
t_{ASEH}	$\overline{ASE}$ hold time to ALE fall		0		-	ns

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Motorola Microprocessor Interface Timing

The following timing specifications are applied when a Motorola bus interface is selected by pulling the BUSMODE pin to logical LOW and the DSPMODE pin to logical LOW. Timing measurements are made at 50% VDD with 100 pF load capacitances for all pins, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
t_{ASPW}	Pulse width, AS HIGH		45		-	ns
t_{AS}	Muxed address valid time to AS fall		7.5		-	ns
t_{AH}	Muxed address hold time after AS fall		20		-	ns
t_{DDR}	Read data delay time from DS rise		-		100	ns
t_{DHR}	Read data hold time after DS fall		0		50	ns
t_{DSPWR}	Pulse width, DS HIGH during READ		100		-	ns
t_{DSW}	Write data setup time prior to DS fall		60		-	ns
t_{DHW}	Write data hold time after DS fall		10		-	ns
t_{DSPWW}	Pulse width, DS HIGH during WRITE		100		-	ns
t_{ASDS}	DS delay time from AS fall		25		-	ns
t_{ASRW}	R/$\overline{W}$ delay time from AS fall during WRITE		25		-	ns
t_{RWH}	R/$\overline{W}$ hold time after DS fall during WRITE		0		-	ns
t_{CSS}	$\overline{CS}$ setup time prior to AS fall		0		-	ns
t_{CSH}	$\overline{CS}$ hold time after DS fall		0		-	ns
t_{ASES}	$\overline{ASE}$ setup time prior to AS fall		45		-	ns
t_{ASEH}	$\overline{ASE}$ hold time after AS fall		0		-	ns

DSP Interface Timing

The following timing specifications are applied when a DSP bus interface is selected by pulling the DSPMODE pin to logical HIGH. Timing measurements are made at 50% VDD with 100 pF load capacitances for all pins, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
t_{ALPW}	Pulse width, XFER/$\overline{SEL}$ LOW		75		-	ns
t_{ALHW}	XFER/$\overline{SEL}$ hold time after $\overline{WR}$ rise		0		-	ns
t_{DDR}	Read data delay time from $\overline{REN}$ fall		-		60	ns
t_{DHR}	Read data hold time after $\overline{REN}$ rise		0		50	ns
t_{RDPW}	Pulse width $\overline{REN}$ LOW		75		-	ns
t_{DSW}	Write data setup time prior to $\overline{WR}$ rise		40		-	ns
t_{DHW}	Write data hold time after $\overline{WR}$ rise		10		-	ns
t_{WRPW}	Pulse width, $\overline{WR}$ LOW		50		-	ns
t_{CSSW}	$\overline{CS}$ setup time prior to $\overline{WR}$		25		-	ns
t_{CSSR}	$\overline{CS}$ setup time prior to $\overline{REN}$		0		-	ns
t_{CSH}	$\overline{CS}$ hold time after $\overline{REN}$ or $\overline{WR}$ rise		0		-	ns

6

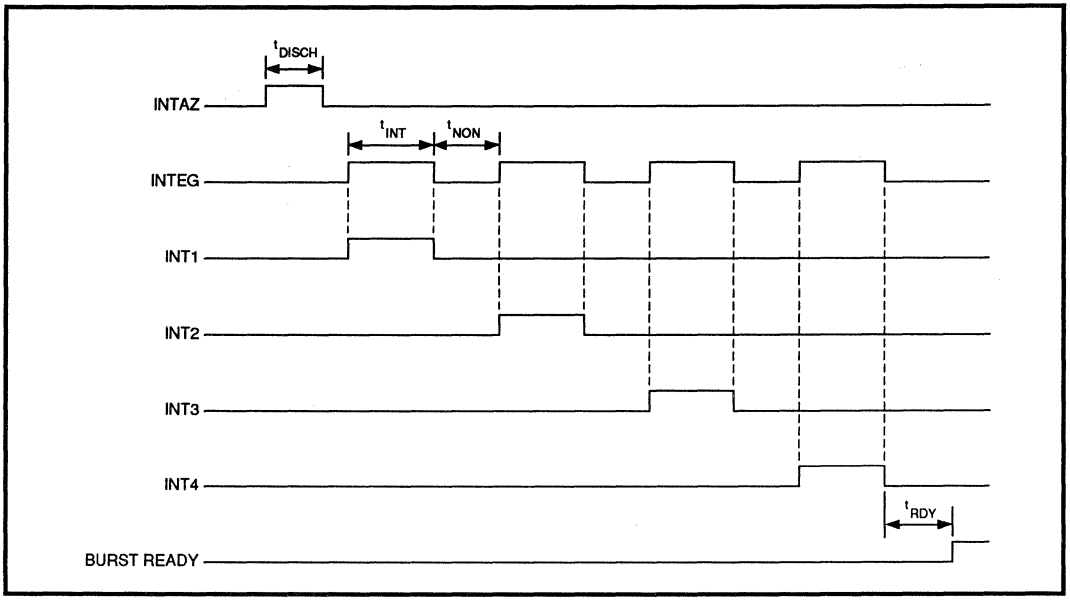


FIGURE 1: Embedded Servo Burst Processor Timing Diagram

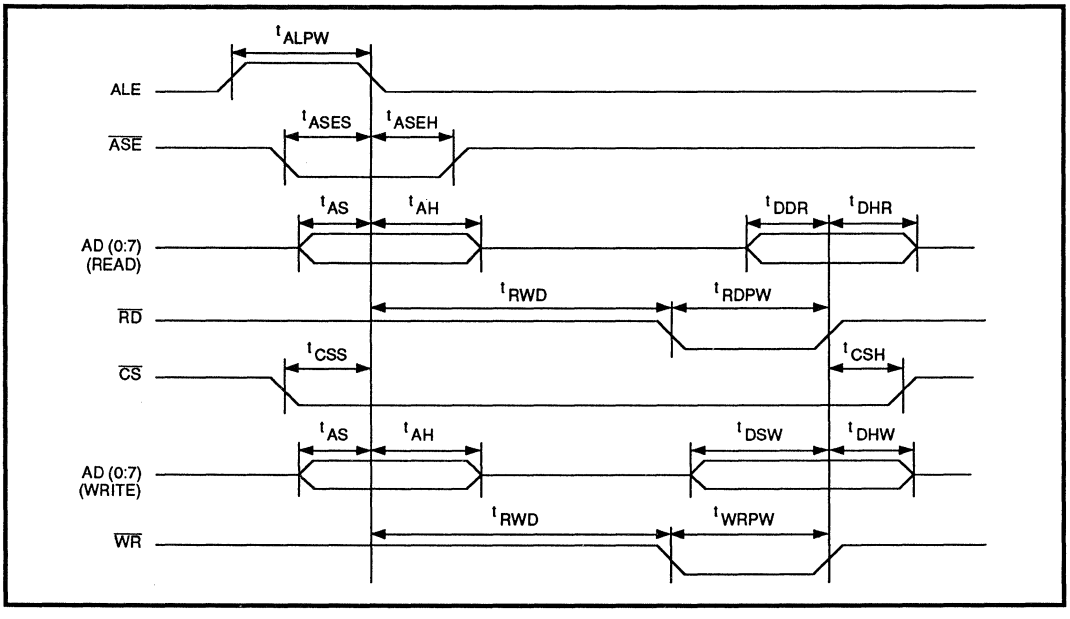


FIGURE 2: Intel Microprocessor Bus Interface Timing Diagram

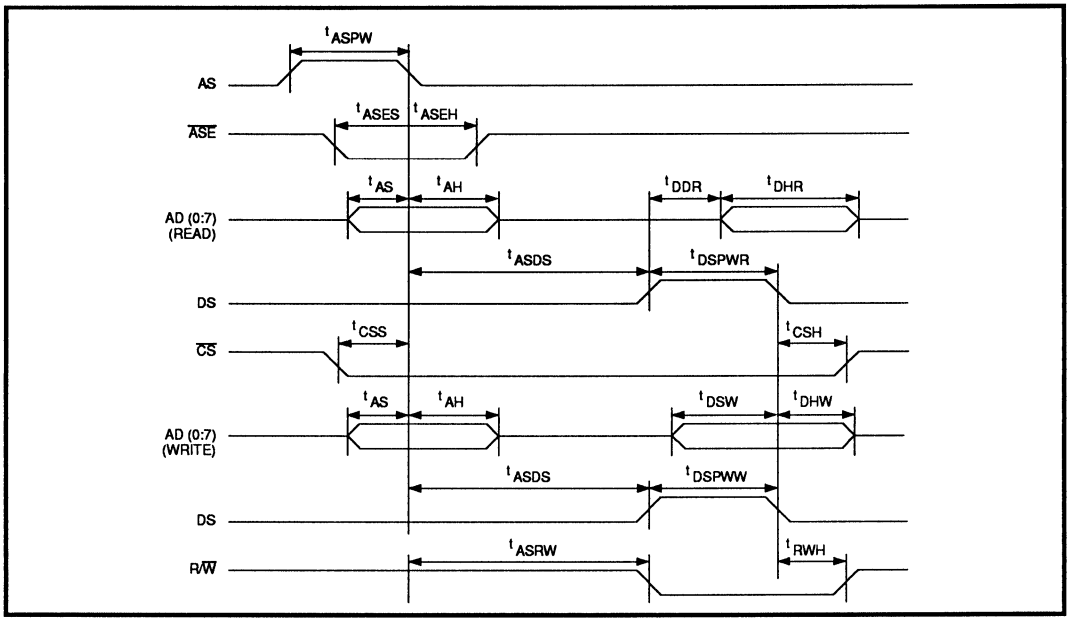


FIGURE 3: Motorola Microprocessor Bus Interface Timing Diagram

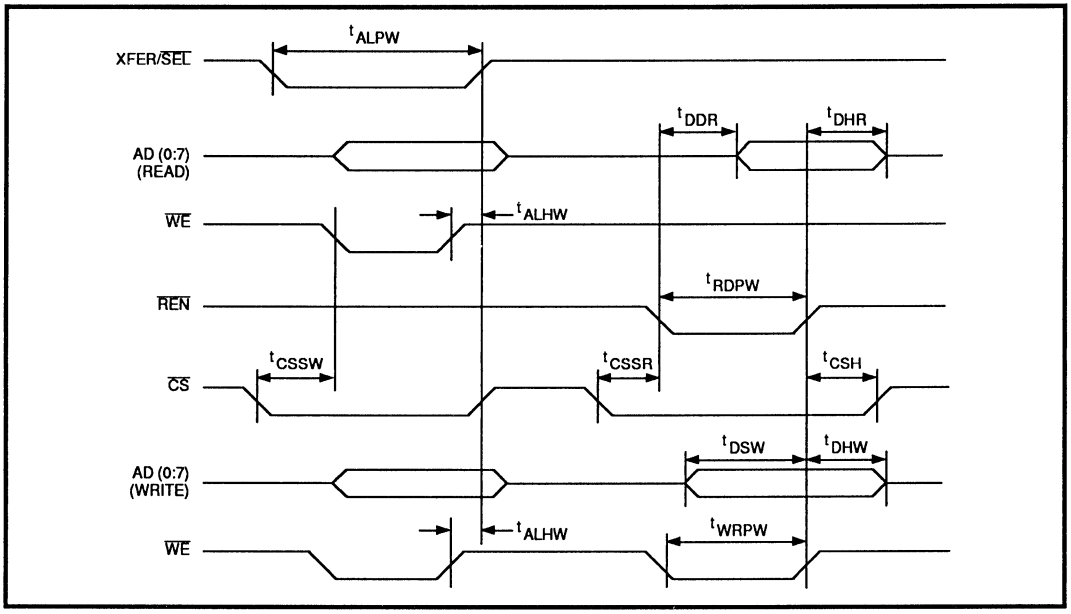
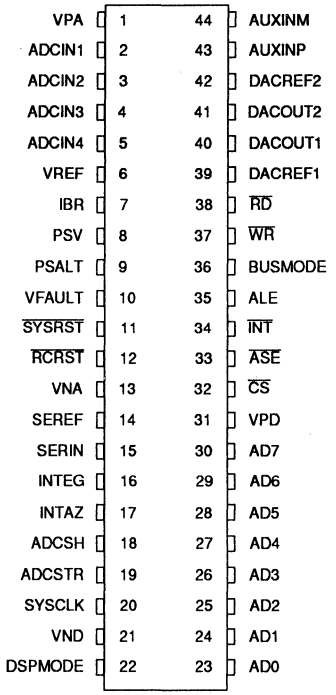


FIGURE 4: TMS320XX Bus Interface Timing Diagram

SSI 32H6520
Embedded Servo Controller

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



44-Pin SOM

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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silicon systems®
A TDK Group Company

SSI 32H6810
5V Servo & Motor Speed Drivers
Advance Information

September 1991

DESCRIPTION

The 32H6810 combines the head positioning and spindle motor electronics with internal power FETs. It also provides voltage fault logic and over-temperature protection.

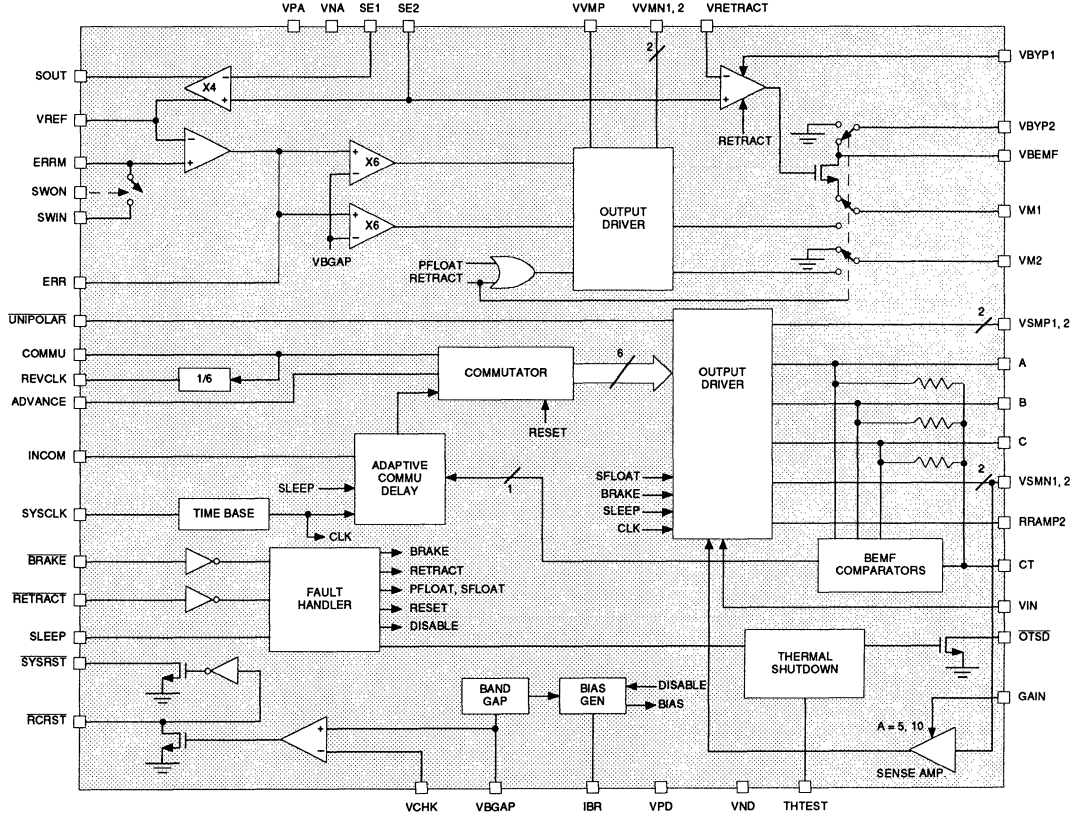
The positioner section serves as a transconductance amplifier by driving 4 internal FETs in an H-bridge configuration and performs motor current sensing. Class B operation is guaranteed by crossover protection circuitry, which ensures that only one FET in each leg of the H-bridge is active. It also offers over-temperature protection by disabling the output FETs. In addition, automatic head retraction may be initiated by a low voltage condition or upon external command.

The (Spindle) Motor Commutator in conjunction with external components, provides the motor driving capability for starting, accelerating, and rotational speed regulation for brushless DC motors without the need for Hall sensors. Control is accomplished via five pins (plus 2 optional pins INCOM & $\overline{\text{UNIPOLAR}}$) and operation is monitored via three pins (plus optional pin REVCLK). The speed regulation control loop is completed with a microprocessor or signal processor external to the SSI 32H6810.

Motor speed control may be accomplished by measuring the period of the output signal COMMU. Motor armature position is determined by monitoring the coil voltage of the winding that is not presently being driven by the drivers. The back-emf from the coil in conjunction with the state of the output drivers, indicates armature position.

6

BLOCK DIAGRAM



DESCRIPTION (continued)

The back emf is compared to a reference (CT) and initiates commutation "events" when the appropriate comparison is made. (Commutation is the sequential switching of drive current to the motor windings.) Because the back-emf comparison event occurs prior to the time when optimum commutation should occur, it is preferred to delay commutation by a predetermined time after the comparison. The commutation delay is provided by circuitry which measures the interval between comparison events and delays commutation by a time equal to 3/7 of the prior measured interval. The circuit is adaptive and will provide the optimum delay for a wide range of motor speeds (-80% to +50% of nominal). Since the commutation of motor coils typically causes transients, the commutation delay circuit also provides a noise blanking function which prevents response to back-emf comparison events for a period of time equal to 4/7 of the interval (between events) after the comparison event. The commutation states are given in Table 1.

Input pin VIN is the non-inverting input of a linear transconductance amplifier which uses the lower driver transistor that is presently active per the commutation state as the power driver element. An external resistor Rsense is used to sense the current in the drive transistor source VSMN (and hence the motor coil current). The voltage across the sense resistor is amplified by a gain stage (Av = 5) and fed to the inverting input of the transconductance output stage.

The output pins A, B, and C are intended to drive motor coils directly. The output drivers operate to reduce switching noise transients by limiting dv/dt during commutation. Each output consists of two n-channel MOSFET drivers, one for pull-up to VSMP and one for pull-down to VSMN. The pull-up looks like a switch (1.5 Ω maximum) with voltage rise and fall times of about 25 microseconds. The pull-down transistor is part of the transconductance amplifier which converts VIN into motor current (Imotor = VIN/(Rsense • 5)). When the pull-down output is commutating to the "off" state, dv/dt is controlled such that dv/dt is approximately 1.5E10/Rramp volts per second.

Motor starting is accomplished by a companion microprocessor utilizing ADVANCE, SLEEP, $\overline{\text{BRAKE}}$ and COMMU. The microprocessor can control SLEEP and $\overline{\text{BRAKE}}$ to initialize the commutation counter and then increment the counter with ADVANCE. Reset with SLEEP = low and $\overline{\text{BRAKE}}$ = low then enable with $\overline{\text{BRAKE}}$ = high (power-up condition and preparation to begin a starting sequence), the commutation state will be state 0 per Table 1, but lower driver output B remains inactive to prevent current flow through the motor (out of A which is "high"). On the first ADVANCE set high, commutation state 1 is selected and the drivers are per Table 1. ADVANCE at logic high excludes internal commutations. COMMU provides feedback to the microprocessor on motor activity.

Seven operating conditions are selected via $\overline{\text{BRAKE}}$, SLEEP and $\overline{\text{RETRACT}}$ (when VPA is present) as indicated by Table 2. If VPA is not present (VCHK < VBGAP), power for the braking circuitry during retract and spin-down is provided by the charge stored on an external capacitor on pin VBYP1, power for the retract circuitry is provided by the back emf voltage and the retract circuitry itself is driven by charge stored on the capacitor between VBYP1 and VBYP2.

TABLE 1: Commutation States

STATE	COMMU	Pull-Downs A	Pull-Downs B	Pull-Downs C	Pull-Ups A	Pull-Ups B	Pull-Ups C
0, (Reset state)	0	off	on (1)	off	on	off	off
1	1	off	off	on	on	off	off
2	0	off	off	on	off	on	off
3	1	on	off	off	off	on	off
4	0	on	off	off	off	off	on
5	1	off	on	off	off	off	on

(1) B is off in reset state, see text.

TABLE 2: Operating Mode Control

VCHK>VBGAP	SLEEP	BRAKE	RETRACT	CONDITION	ANALOG	COUNTERS	POSITIONER	A, B, C
0	X	1	X	Power Fault	Off	Reset	Retract	Float
0	X	0	X	Power Fault	Off	Reset	Retract	Low Z to GND
1	1	1	1	Sleep	Off	Active	Float	Float
1	1	0	1	Sleep/Brake	Off	Active	Float	Low Z to GND
1	1	X	0	Sleep/Retract	Off	Active	Retract	Float
1	0	0	X	Brake/Retract	Off	Reset	Retract	Low Z to GND
1	0	1	0	Retract (Spindle Run)	On	Active	Retract	Active
1	0	1	1	Run	On	Active	Active	Active
X	X	X	X	Thermal Shutdown	Off	Active	Float	Float

NOTES:
1. BRAKE internally linked to force retract.
2. Voltage fault circuit is never turned off.

The circuit also provides an over temperature detection function. If the die temperature exceeds 135°C (approximately), OTSD is asserted low and all output drivers are turned off. The drivers will become operative after the temperature is reduced and ADVANCE is asserted high.

PIN DESCRIPTION

POWER SUPPLIES

NAME	TYPE	DESCRIPTION
VPA	I	Supply: Analog positive power supply.
VNA	I	Ground: Analog ground.
VPD	I	Supply: Digital positive power supply.
VND	I	Ground: Digital ground. VND is circuitry ground and also the low side input to the current SENSE amplifier and thus care should be taken to see that VND and the low side of the external Rsense resistor are at the same potential.
VVMP	I	Supply: Positve supply for voice coil motor.
VVMN1, VVMN2	I	Supply: Negative supply for voice coil motor.

PIN DESCRIPTION

POSITIONER

SWON	I	Turns on the switch between ERRM and SWIN.
SWIN	I	Analog switch, the other side of the switch is connected to ERRM.
SOUT	O	The current sense amplifier output. SOUT is referenced to VREF.
ERR	O	The error amplifier output. ERR is used to provide compensation to the transconductance loop. ERR is referenced to VBGAP.
ERRM	I	The error amplifier negative input.
VREF	I	The reference voltage for the error amplifier and the current sense amplifier.
VRETRACT	I	The retract voltage. If left open, the retract voltage will be the default setting. This value can be over-ridden by biasing VRETRACT externally.
VM1	O	Connection for voice coil motor and sense resistor.
VM2	O	Connection for the other side of voice coil motor.
SE1, SE2	I	Sense voltage on the sense resistor.

MOTOR SPEED CONTROL

SYSCLK	I	System clock (input) pin. SYSCLK is 2.00 MHz and is used to generate internal timing signals assuming a nominal 3600 RPM, 8-pole motor environment.
COMMU	O	Commutation count pin. COMMU is the LSB of the commutation counter.
$\overline{\text{UNIPOLAR}}$	I	Unipolar mode (inverse) select pin. This pin will turn all upper drivers off when low. Pulled high internally to provide the default bipolar mode.
ADVANCE	I	Advance pin. ADVANCE is controlled by microprocessor during start mode to increment the commutation counter. The rising edge of ADVANCE will increment the counter. ADVANCE held high will inhibit internal incrementing of the counter, ADVANCE held low permits the normal operation of commutation from back-emf events.
INCOM	I	Commutation delay control pin. Adaptive commutation delay may be adjusted from its nominal value of one half the commutation interval by inserting or withdrawing current ot this pin. This should only be done via an external control loop which can compensate for the range of internal circuit parameter variations.
VIN	I	Control Voltage input pin. The internal driver transistors and internal predriver circuits form a transconductance amplifier which will set motor current in relation to VIN. In conjunction with Rsense at VSMN input and the gain of the Sense amplifier, transconductance (Gm) will be Gm = Im/VIN = 1/ (Rsense • 5).
A, B, C	O	Motor Drive Outputs. These pins provide drive to the motor coils.

MOTOR SPEED CONTROL (continued)

NAME	TYPE	DESCRIPTION
CT	I	Back EMF input from motor coil center tap. Input connected to the center tap for sensing generated back emf voltages. It is also derived internally from A, B, C through a resistor network (y-connection). The circuit uses the back-emf voltages to determine rotor position and effect commutation.
RRAMP	I	Lower driver turn-off dv/dt setting resistor. External resistor from VPD to this pin sets the dv/dt slope of the motor coil voltage when the lower drivers are commutating to the off state. The dv/dt is given approximately by the relationship dv/dt (volts/second) = 1.5 • 10E10/Rramp. Typical value: RRAMP = 200K.
GAIN	I	Sense amplifier gain control pin. In normal operation, this pin is tied to high to set sense amplifier gain = 5. In low motor current operation, amplifier gain = 10 can be set by tying this input to low.
VSMP	I	Supply: Positive supply for spindle motor.
VSMN1, VSMN2	I	Supply: Negative for spindle motor. Current monitoring sense amplifier (high side) input pin and motor current returns to ground. **All pins must be connected with low resistance circuit board traces.** The lower driver transistor current (hence motor current) comes out of these pins to Rsense resistor to monitor motor current. During normal (at speed) operation, the circuit will control the voltage across this resistor (multiplied by the gain of 5 in the sense amplifier) to match VIN. **VVMP, VVMN, VSMP and VSMN conductors must be sized in accordance with anticipated motor current. The analog and digital supplies should be bypassed separately. VPA and VPD should be shorted externally, VNA and VND should be shorted externally.**

MISCELLANEOUS

VBYP1	I	The bypassed power supply. An external voltage for BRAKE and RETRACT circuitry. An external capacitor is attached to this pin and an internal circuit will charge this pin to VCC. The charge on this capacitor is used by the brake and retract function when VCC is removed (power-off). The capacitor must hold sufficient charge during the period when VCC is lost while retract is taking place (20 to 50 ms) so it will have enough voltage to drive the outputs during braking. Very little current is used during power-off braking so that C can be chosen from the retract conditions: $C \geq Tretract \cdot Ivbyp\ (float\ mode) / .5\ volt$ or approximately: $C \geq 500E\text{-}6 \cdot Tretract$ This pin is normally a diode drop below VPA, rising by VBEMF during retract.
VBYP2	I	The other side of the bypass capacitor connection. This pin is normally at VNA, rising to VBEMF during retract.
VBEMF	I	Rectified spindle back emf voltage. This voltage drives the internal retract FET.

PIN DESCRIPTION

MISCELLANEOUS (continued)

NAME	TYPE	DESCRIPTION
SLEEP	I	Sleep pin. When asserted high, internal counters and registers are cleared. Refer to Table 2. Also forces an internal voltage fault which causes a head retract. Disables all output drivers, powers down all other circuitry except the over-temperature and voltage fault circuitry.
$\overline{\text{RETRACT}}$	I	Retract (inverse) pin. When asserted low, forces a retract. Refer to Table 2.
$\overline{\text{BRAKE}}$	I	Brake (inverse) pin. $\overline{\text{BRAKE}}$ is used to provide a delay between the initiation of fault-induced head retract and motor braking. A capacitor to ground and a resistor to $\overline{\text{SYSRST}}$ are selected such that 1.2 • R • C is equal to the maximum time required for retract. Refer to Table 2.
$\overline{\text{OTSD}}$	O	Over-Temperature Sense Detect. Excessive die temperature will bring this open drain output low. Spindle motor and positioner drivers are disabled whenever $\overline{\text{OTSD}}$ is asserted.
VCHK	I	Comparator input for power supply monitoring.
VBGAP	O	An internal voltage reference for use with the power supply monitor comparator.
IBR	O	A resistor is tied from this pin to ground to establish the bias current for internal circuitry.
$\overline{\text{RCRST}}$	I/O	This pin serves the dual purpose of providing power on reset and stretching short VFAULT pulses to a width suitable for the host microcontroller. An external RC network sets the minimum width of any $\overline{\text{SYSRST}}$ pulse.
$\overline{\text{SYSRST}}$	O	When low, this open drain output indicates that an internal voltage fault has occured or that $\overline{\text{RESET}}$ has been pulled low.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above absolute maximum ratings may permanently damage the device.

PARAMETER	SYMBOL	MIN	MAX	UNIT
Supply Voltage	VPA, VPD, VVMP, VSMP (1, 2)	-0.3 -0.3	7.0 7.0	V V
Output Current	Imax (in or out of A, B, C, VM1, VM2)	0	0.7	Amp
Analog I/O	VIN, RRAMP,	-0.3	VPD + 0.3	V
Voltage on pins	CT, A, B, C, VBEMF, VBYP1, VBYP2	-0.3	12.0	V
	VM1, VM2, SE1, SE2	-0.3	7.0	V
	All other pins	-0.3	VPD + 0.3	V
Storage Temperature	Tstg	-65	150	°C
Lead Temperature (10 sec duration)	Tlead	0	300	°C

OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Supply Voltage	VPA, VPD VVMP, VSMP	4.5 4.5	5.5 5.5	V V
Supply Current	I (VPA + VPD)		26.0	mA
	IVVMP		0.5	A
	IVSMP		0.5	A
	I (VPA + VPD + VVMP + VSMP) Sleep mode		1.0	mA
	IVBYP1, braking		5.0	µA
	IVBYP1, retract		0.25	mA
VBEMF		1.0	10.0	V
VREF		0.5	VPA-2	V
VIN		0	2.5	V
RF		10		kΩ
RC		10		kΩ
RBIAS		112	114	kΩ
Ambient Temperature	Ta	0	70	°C
Capacitive Load Digital I/O	Cl	0	100	pF
Analog Outputs	Cl	0	50	pF
Resistive Load Analog Outputs	Rl	10		kΩ
Power Dissipation	Pd		500	mW

PARAMETRIC REQUIREMENTS

Digital Input/Output

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Fclk, SYSCLK		1.998		2.002	MHz
Twh, Twl, SYSCLK width high or low		40			ns
Input Leakage				10	µA
Vil (SYSCLK, ADVANCE)				0.8	V
Vih (inputs above)		2.0			
Vil ($\overline{\text{RCRST}}$, $\overline{\text{BRAKE}}$, SLEEP, $\overline{\text{RETRACT}}$, $\overline{\text{UNIPOLAR}}$, SWON) VM ≥ 4.5V		0.8			V
Vih ($\overline{\text{RCRST}}$, $\overline{\text{BRAKE}}$, SLEEP, $\overline{\text{RETRACT}}$, $\overline{\text{UNIPOLAR}}$, SWON) VM ≥ 4.5V					

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ELECTRICAL SPECIFICATIONS (continued)

Digital Input/Output (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Output Sink current $\overline{RCRST}$, $\overline{OTSD}$	Vo = 0.4V	1.6			mA
$\overline{SYSRST}$	Vo = 0.4V	4.0			mA

Digital Output COMMU

Voh	Iout = -100 µA	2.4			V
Vol	Iout = 2.0 mA			0.4	V

VIN

Input Current	0 ≤ Vin < 2.5V	-1		+1	µA

Outputs A, B, C

Routup	Output in high state, VPD = 4.75V			1.5	Ω
Routlow	Output driving low, VPD = 4.75V			1.0	Ω

VSMN1, VSMN2

Vin, VSMN1, VSMN2 Iin, VSMN1, VSMN2 Cin	Normal operation 0.0 ≤ Vin < 1.0 volt	0.0 -10		0.50 +10 20	V µA pF
Transconductance gain from VIN to motor current (steady-state) will be given by: G = Imotor/VIN = 1/(Rsense • 5)					

CT, And A, B, C, When Not Driving

Rin	-0.3V ≤ Vin < 10V	30k			Ω
Cin				20	pF

VBYP1

IVBYP1 (run)	VPD = 4.5V			0.25	mA
IVBYP1 (float)	VPD ≤ 0.5V			0.25	mA
IVBYP1 (brake)	VPD ≤ 0.5V			0.25	mA

BEMF

IBEMF				TBD	mA
IBEMF (sleep)				TBD	mA
IBEMF (retract)	I (VM1) = I (VM2) = 0			TBD	mA

SOUT

Gain		3.9		4.1	V/V

SOUT (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Input Offset	SOUT = VREF	-3		3	mV
Output Swing		0.15		VP-1	V

ERR

ERRM Input Offset	ERR = ERRM	-10		10	mV
ERR Output Swing		1.55		VP -1.25	V

POSITIONER

(VM1 - VM2) / (ERR - VBGAP)		11		13	V
Crossover Time	Imotor = 10 mA pp 1kHz			45	µs
Output Distortion	Imotor = 10 mA pp 1kHz			2	%THD

VBGAP

Bandgap Voltage		2.13		2.37	V

VCHK

Offset		-15		15	mV

OUTPUT VM1, VM2

Routup	Output in low state, VM = 4.75V			1.5	Ω
Rout low	Output in high state, VM = 4.75V			1	Ω

SWIN

On Resistance				250	Ω

RETRACT

VRETRACT Input Impedance	Retract mode	25			kΩ
VRETRACT (retract mode) open circuit voltage	VBEMF = 1.0V VBEMF = 1.5V VBEMF = 3.0V VBEMF = 4.5V	0.4 0.4 0.5 0.6		0.9 1.0 1.2	V V V

$\overline{\text{OTSD}}$ (Thermal Shutdown)

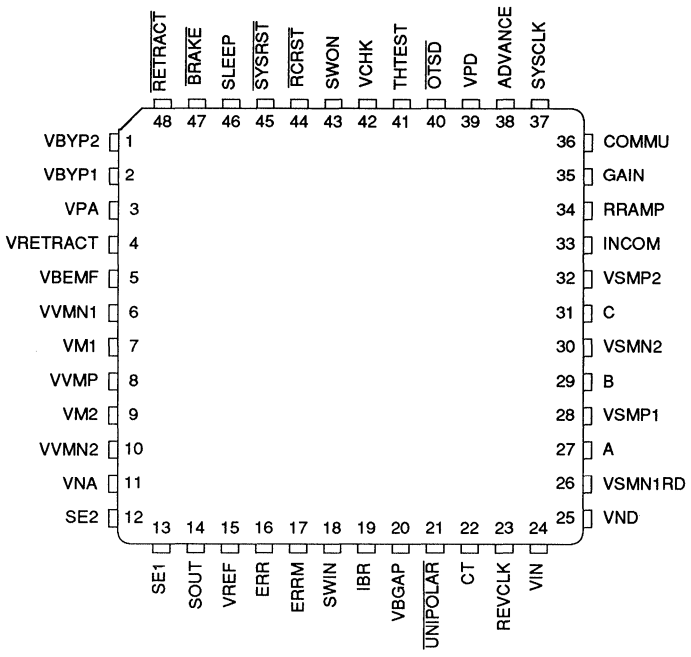
Die temperature		125		145	°C

6

SSI 32H6810
5V Servo &
Motor Speed Drivers

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



48-Lead TQFP

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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December 1991

SERVO DESIGN EXAMPLE

The application of the SSI 32H6220 dedicated servo controller, SSI 32H569/32H6230 H-bridge predriver, and SSI 32H6210 servo demodulator chips require both discrete component determination and microprocessor programmed register values. This section provides as a design example, a systematic method of determining both the discrete components and programmable values required in implementing a fully functional track and seek head positioning servo. This example makes use of an available Silicon Systems' program named SERVO CALC which runs on the PC/XT or PC/AT compatible personal computer. The program provides an interactive enviroment for entering target specifications, systematically proceeding through the design, and automating the calculation of components and programmable values. The program provides various tools for system performance review such as velocity profile plots, open and closed loop Bode plots, step response plot, mechanical resonances and notch filter effects.

SPECIFY SEEK PERFORMANCE REQUIREMENTS

Specifying the average seek time, total number of tracks for a full length seek, and profile characteristics will provide the basis for determining a precise head velocity profile. Profile characteristics specify the relationship between acceleration and deceleration under different conditions. The ratio of deceleration time plus settling time all divided by the acceleration time provides the profile characteristic "R." The number of tracks traveled in "triangular mode" divided by the total number of tracks for a full length seek provides the profile characteristic "BETA." These two profile characteristics may be used along with a modified square root law to determine a velocity profile which will result in satisfying the specified average seek time.

As an example, specify as design goals:

Linear actuator
1400 TPI for a G2 of 55,860 Tracks/Meter
1000 total cylinders
Average access time of 15 ms
30 gram actuator mass
R = 1.2 and BETA = 0.4

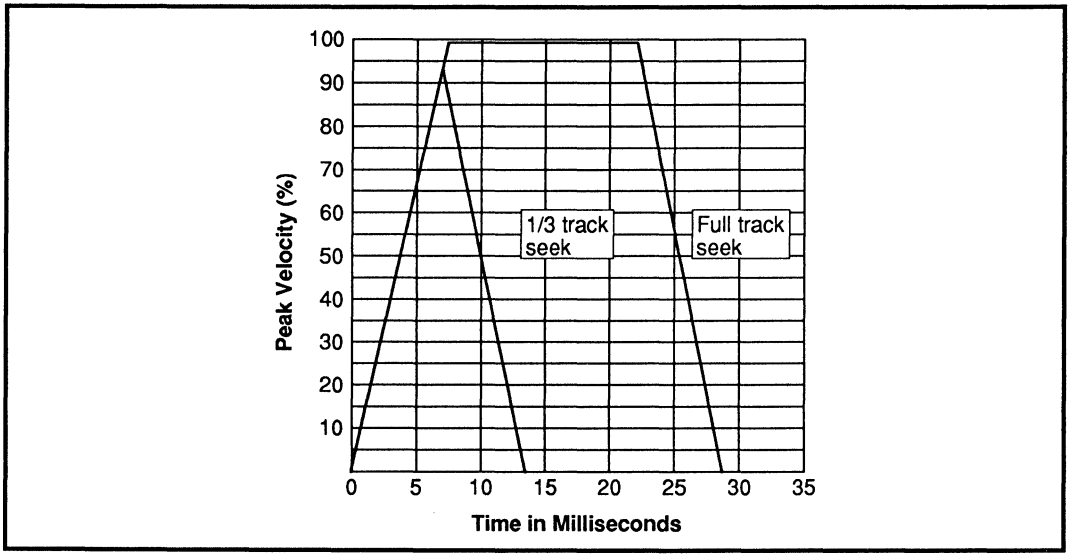


FIGURE 1: Track Seek Profile

REVIEW VELOCITY PROFILES

The deceleration profile may be reviewed and adjusted by modifying the square root law which relates profile head velocity to the number of tracks left to travel. Step-wise increasing the exponent of tracks to go from 1/2 (square root starting point) will "soften" the deceleration approach curve. As the curve softens, the settling time available decreases. The "R" value may be adjusted to match a suitable deceleration curve with the required settling time.

From the profile chosen, the following parameters may be determined for our example design:

Head acceleration of 6,175,115 tracks/sec^2

Peak head velocity of 49,699.5 tracks/sec

200 deceleration tracks required

8.05 ms of acceleration, 12.08 ms coasting, and 9.66ms decelerating full seek

Full seek time 29.8 ms

Both the average and full length seek profiles are shown in Figure 1.

SPECIFY MOTOR AND LOAD PARAMETERS

The motor and load parameters must be estimated and specified so that the power required to meet the velocity profile chosen may be computed and compared against design goals. G1 is preamplifier gain and is not dependent upon motor or load parameters. G1 is fixed at 6 VOLTS/TRACK when using the SSI 32H6210. The motor resistance will introduce both a power loss and a voltage drop which must be considered. The two motor systems, namely linear and rotary, require different units of specification.

Linear Motor Specifications

G2 transport constant in Tracks/Meter

J mass in KG (kilograms)

Km motor constant in N/A (newton/amps)

Rotary Motor Specifications

G2 transport constant in Tracks/Rad

J inertia in KG m^2 (kilograms meter squared)

Km motor constant in (N • m/A)

Optionally, Km may be computed from the head velocity profile based on a specified maximum motor current IPEAK. The two specifications of IPEAK and Km are interrelated.

For our example,

IPEAK is 1 Amp and Km is calculated

Rm = 3.8Ω

Rs = 0.2Ω

REVIEW MOTOR VOLTAGE, POWER AND Km

From the motor and load specifications, the required peak current needed to satisfy the chosen head velocity profile may be calculated. Using the transport constant G2, the back EMF of the motor may be calculated at peak head velocity and added to the the voltage drop across the motor resistance Rm and sense resistor Rs. The total voltage required by the motor may be compared to the available driver voltage. Peak motor power may be computed and compared to design goals. If Km was calculated from a specification of IPEAK, the resulting value of Km may be compared against that actually attainable in the motor design. Adjustment of Km and IPEAK may be made to both satisfy the average seek time specification and general design goals.

For this example:

Km was calculated to be 3.316 N/A

Peak drive voltage required is 6.95V including the voltage across Rs

Peak coil input power is 6.75 Watt

Coil dissipation 3.8 Watt

SPECIFY POWER AMPLIFIER COMPONENTS

The power amplifier is shared by both the track following and seek servo control loops. The determination of DC gain for the power amplifier for seek will also determine some components shared with the track following servo. Referring to the example schematic of the SSI 32H6210/6220/6230, RS, RF and the sum resistance of RINV1 and RINV2 (RINV) may be determined. Choosing RF to be an initial nominal value such as 10,000Ω and choosing RS as some small resistance such as 0.2Ω provides good starting points.

The DC power amplifier gain for the seek servo is calculated from the peak current required to satisfy the peak velociyy of the velocity profile and the full scale target DAC output voltage. A motor current limit may be implemented when using the SSI 32H6230 by connecting the CLAMP pin to ERR- through the RINV1 and RINV2 network as shown on the schematic. The limit voltage is programmable by setting the voltage at the 6230 VLIM pin. It is necessary to choose the limit current higher with tolerance margin above that current required to meet the maximum head velocity from the velocity profile.

In the example,

RINV total should be 5062.5Ω

RF is specified as 10,000Ω

CHOOSE DIFFERENTIATOR AND VELOCITY LOOP GAINS

The differentiator within the SSI 32H568 or 32H6220 provides a programmable corner frequency determined by servo frame rate and the two bit register ND. Having determined the maximum head velocity from the velocity profile and knowing the transport constant and servo frame rate, the maximum output voltage from the differentiator may be calculated.

The output of the differentiator is amplified by the velocity amplifier A3 and the programmable gain stage set by NVG. The velocity loop gain from the output of the differentiator to the feed back summing junction of the target DAC must be set so that the peak differentiator output voltage will result in zero VE voltage (relative to VREF) when the target DAC is at its full range of 255. Choosing a nominal NVG setting of 10 and selecting an ND which does not exceed the amplitude limit of the differentiator itself, will result in the calculation of the necessary gain in A3. The seek velocity feedback may be fine tuned by adjusting the gain of NVG as indicated in drive self-calibration.

For the example, the programmable registers are:

NVG is 10 decimal

ND will be 2 for a frame rate of 250 kHz

Gain of A3 will be 1.96 so that (RV4/RV3) = 1.96; If RV4 = 19.6K, then RV3 = 10K

RV1 and CV1 will not be used in this example

GENERATE TARGET PROFILES

The seek servo velocity loop is closed within the SSI 32H6220. The implementation of the velocity profile is commanded by the supporting microprocessor. The microprocessor commands target velocities by writing to the target DAC. The necessary DAC values may be derived from the velocity profile. The acceleration DAC value is determined from the peak head velocity in the velocity profile. The microprocessor writes the acceleration target velocity to the target DAC and monitors track crossings determining when to begin deceleration. Once the head has moved past the deceleration corner, the microprocessor will write the deceleration target velocities to the target DAC usually track by track thereby following the head velocity down to the transition point into track following. The number of table entries making up the deceleration table can be found from the profile data discussed in the earlier section, Review Velocity Profiles.

A fill table may be generated corresponding to the target velocity table. The fill table is usually only a few entries long. The fill table values are computed from the position error voltage available at FP1 and the step in target DAC voltage for the last few deceleration velocity targets. The fill value programs the gain of the fill amplifier which subtracts from the velocity error a portion of the position error signal. This subtraction of position error from the velocity error has the effect of smoothing the velocity error voltage at VE when the head is moving slowly and tends to insure that the head will move towards the center of the target track prior to switching on track following.

The 20 element fill value table resulting for the example is shown below in Table 1. "t" is the target track.

Target Track Lineup	
t-0: 12	t-10: 2
t-1: 5	t-11: 1
t-2: 4	t-12: 2
t-3: 3	t-13: 1
t-4: 3	t-14: 2
t-5: 3	t-15: 1
t-6: 3	t-16: 1
t-7: 2	t-17: 1
t-8: 2	t-18: 2
t-9: 2	t-19: 1

TABLE 1

The velocity target DAC values for the example are listed below in Table 2, ordered as the number of tracks remaining to go, ie: "t-n":

t-0	t-20	t-40	t-60	t-80	t-100	t-120	t-140	t-160	t-180
0	81	114	140	161	180	198	213	229	243
18	83	115	141	162	181	198	214	229	243
25	85	117	142	163	182	199	215	230	244
31	86	118	143	164	183	200	216	231	245
36	88	120	144	165	184	201	217	232	245
40	90	121	145	166	185	202	218	232	246
44	92	122	146	167	186	202	219	233	247
48	94	124	148	168	187	203	219	234	247
51	95	125	149	169	187	204	220	234	248
54	97	126	150	170	188	205	221	235	249
57	99	127	151	171	189	206	222	236	249
60	100	129	152	172	190	206	222	236	250
62	102	130	153	173	191	207	223	237	250
65	104	131	154	174	192	208	224	238	251
67	105	132	155	175	193	209	224	239	252
70	107	134	156	176	193	209	225	239	252
72	108	135	157	177	194	210	226	240	253
74	110	136	158	178	195	211	227	241	254
76	111	137	159	178	196	212	227	241	254
79	113	138	160	179	197	213	228	242	255

TABLE 2

POWER AMPLIFIER COMPENSATION

Components RL2 and CL3 set the bandwidth of the power amplifier. Specifying motor inductance Lm and power amplifier bandwidth BW while having determined RF, Rm, and Rs from seek requirements provides the means for calculating CL3 and RL2.

For the example,

Power amplifier bandwidth is specified as 10 kHz

Lm is specified as 1 mH

CL3 is calculated to be 0.005 µF

RL2 is calcuated to be 47 kΩ

TRACK FOLLOWING GAIN

Both the track following and seek loops share many of the power amplifier gain setting components. Having determined RINV, RF and Rs from velocity profile requirements, the track following power amplifier gain KP is determined entirely by RINP. The track following power amplifer gain KP is interactively set with the position loop filter gain KF. An initial KP may be chosen as 1 AMP/VOLT and the value of KF may be adjusted as needed to stabilize the track following loop. The value of RINP may be computed from RF, Rs, and KP.

In the example,

Specify KP = 1 Amp/Volt

Calculate RINP = 12.5 kΩ

POSITION LOOP FILTER

The implemented filter will take the form of a LAG-LEAD-LEAD-LAG in ascending frequency breakpoints. Due to the double integration in the motor-load mechanics going from acceleration to position, there is an initial 180 degree position phase lag which must be compensated to prevent instability and oscillation. Phase lag introduced by a pole will add additional phase lag exceeding 180 degrees while phase lead introduced by a zero will reduce phase lag. The objective of the position loop filter is to ensure that there

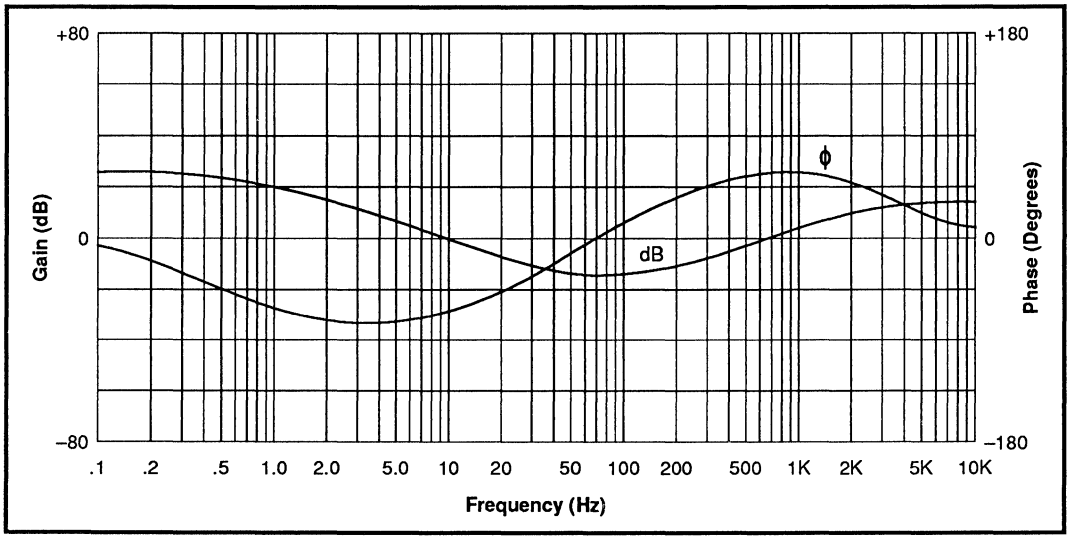


FIGURE 2: Position Loop Filter Bode Plot

is phase margin at the system unity gain crossover frequency while at the same time providing stiffness and long term tracking error cancelation.

The initial position loop filter gain KF may be estimated through a specification for DC stiffness. Specifying a stiffness in units of force per track and knowing G1, Km, and KP will provide a way to solve for KF.

DC stiffness per track is calcuated as:

STIFFNESS = G1 KF KP Km

Specifying 100 N/TRACK stiffness, KF is determined in the example to be 5.

The lowest frequency LAG time constant is referred to as bT2 and is the product CP2(RP3+RP4). This low frequency LAG serves effectively as an integrator with limited DC gain intended to minimize long term tracking error and allowing an increased DC gain improving stiffness which otherwise would not be possible due to mechanical higher frequency resonances. Time constant bT2 generally should be made as large as practically possible. Choosing a value for CP2 such as .47 μF and a pole frequency between 0.1 and 1 HZ will provide a good starting point.

The track following servo is stabilized by providing phase margin at the unity gain crossover frequency. Phase margin is obtained through the use of the two LEAD networks. The first lead breakpoint compensates for the integrator phase lag and the second lead breakpoint provides the required phase margin. Time constant T2 made up of RP3 and CP2 provides the phase lead needed to bring the phase back towards 180 degrees of phase lag. Lead time constant aT1 provides additional phase lead by reducing the phase lag less than 180 degrees at the unity gain crossover frequency. Choosing the time constant aT1 such that its break point frequency is equal to the unity gain crossover bandwidth for the system will provide approximately 45 degrees of phase margin. Time constant T2 needs to be chosen to be at least five times aT1 thereby minimizing the interactive effects of the two leads together. T2 should not be chosen so low in frequency as to cancel out the effects of the integrator lag and the low frequency gain enhancement.

Finally, the high frequency pole T1 determined by RP1 and CP1 provides a high frequency gain limit. The breakpoint frequency associated with the time constant T1 should be placed several times higher than the breakpoint frequency set by aT1. Mechanical resonances may require further adjustment of the T1 breakpoint frequency. Some systems may require additional

POSITION LOOP FILTER (Continued)

notch filters to minimize high frequency mechanical effects.

Having chosen the break point frequencies, the position filter components may all be computed having specified CP2 and KF.

For the example, the break points were initially specified as:

bT2 frequency = 0.6 Hz

T2 frequency = 60 Hz

aT1 frequency = 600 Hz (target system unity gain bandwidth)

T1 frequency = 2000 Hz

TRACK FOLLOWING SYSTEM RESPONSE REVIEW

Bode plots of the open loop response for the LAG-LEAD-LEAD-LAG position loop filter are useful in evaluating the break point frequencies chosen. More useful is the system open loop Bode plot which provides the necessary information needed to properly adjust KF to meet the desired system unity gain bandwidth. Adjusting KF will move the overall response vertically such that unity gain occurs at the desired system bandwidth frequency. The amount of vertical movement indicates how KF should change relative to its intial current value. The phase margin peak may be adjusted horizontally by changing the time constants aT1 and T2. Moving the peak phase lead to correspond to the unity gain frequency is desireable. The system unity bandwidth indicates the stability of the servo system by the amount of phase margin at the unity gain crossover point. Figure 2 shows the open loop position filter Bode plot. Notice the peaking of phase near the target system unity bandwidth frequency of 600 Hz. Figure 3 shows the overall open loop system Bode plot.

After review and adjustment, the final components were standardized as:

RP1 = 8,250Ω

RP2 = 91 kΩ

RP3 = 13 kΩ

RP4 = 680 kΩ

CP1 = 0.0075 μF

CP2 = 0.47 μF

Which resulted in actual break points of:

bT2 frequency = 0.49 Hz

T2 frequency = 26 Hz

aT1 frequency = 213 Hz

T1 frequency = 2572 Hz

And KF = 7.47 for a DC stiffness of 148 N/Track. The resulting phase margin is 51.60 degrees at 630 Hz. The gain margin is 25.2 dB at 4800 Hz.

The closed loop system step response may be obtained and examined to evaluate the overshoot and settling time. The integrator time constant bT2 will tend to control the settling time or "tail." The time constants aT1 and T2 effect the amount of ringing and overshoot. Figure 4 shows the response of the system to a position step.

For the example,

Overshoot is 30%

First zero crossing at 0.4 ms

Settling within 2 ms

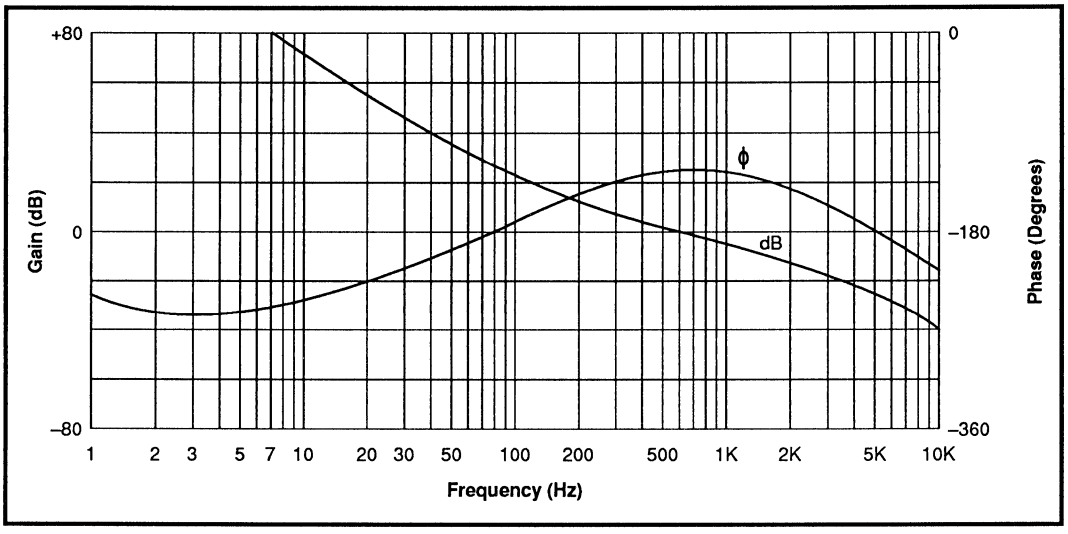


FIGURE 3: Overall Position Open Loop Bode Plot

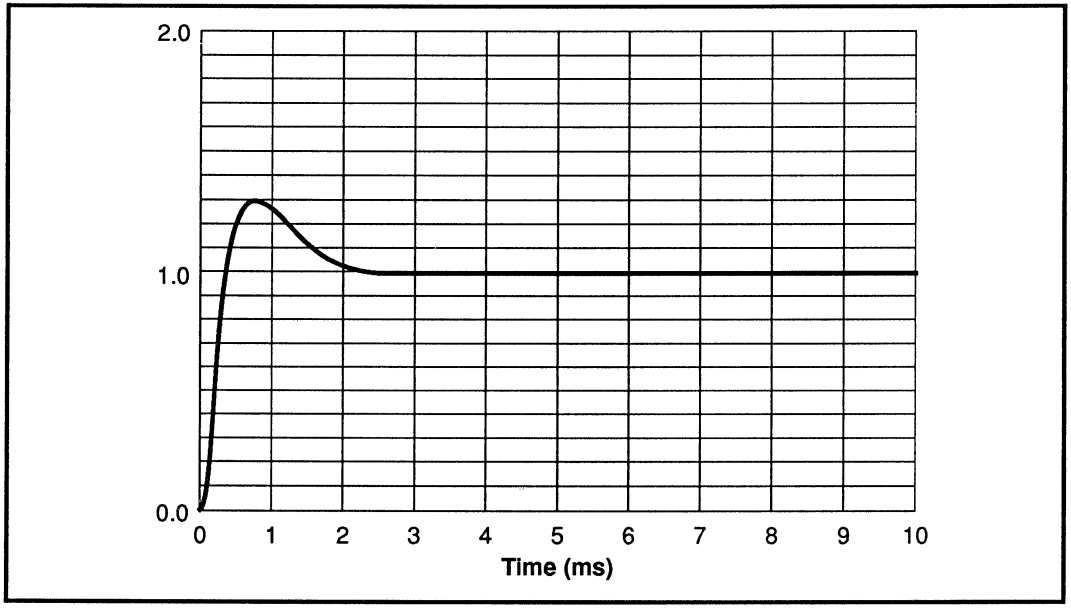


FIGURE 4: Position Closed Loop Step Response

SERVO CALC SOFTWARE

HEAD POSITIONING APPLICATIONS TOOL

DESCRIPTION

This software is an aid to disk drive head position servo design using SSI 32H 6210, 32H6220, 32H569, 32H6230 servo controller and servo motor driver chips. It uses block diagram algebra and transfer function analytical techniques to arrive at first order approximations for the servo design values and parameters. This software offers visual representations of block diagrams, transfer functions, schematics, as well as Bode, seek profile and step response plots. It includes design aids for the design of velocity profiles and tables for evaluation of gain and characteristics settings. It uses simple menus to choose the design screens for power amplifier and position loop filter design and design modules for seek profile/loop parameters and their components. It also has a user definable polynomial transfer function for Bode plot and step response evaluations. The effects of parameter and component changes are specially flagged and quickly displayed.

SERVO CALC PROGRAM FEATURES

- Mathematical modeling
- Polynomial transfer functions displayed/described
- Block diagrams displayed
- Individual design screens displaying design progress
- Stability analysis
- Bode and step response plots
- Mechanical resonance and notch filter effects
- Motor current and power dissipation analysis
- Velocity profile and fill table generation
- Develops design for power amplifier components
- Tabulates and displays design choices in velocity loop
- User-controllable plot and print settings

MINIMUM SYSTEM REQUIREMENTS TO RUN SERVO CALC

An IBM PC/XT/AT or compatible computer with at least 512 Kb of RAM, EGA or EGA-compatible video adapter and monitor, one 5 1/4 inch floppy disk drive. A dot matrix printer for plots and screen printings is optional. A math co-processor and a hard disk is recommended but not required.

For your copy of the SERVO CALC software and other helpful servo tools, please contact your local representative or Silicon Systems, Inc. at (714) 731-7110 ext. 3575.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714) 731-7110, FAX: (714) 573-6914

Section 7

HDD SPINDLE MOTOR CONTROL

silicon systems®
A TDK Group Company

SSI 32M593A
Three-Phase Delta Motor Speed Controller

July 1990

DESCRIPTION

The SSI 32M593A is a motor speed control IC designed to provide all timing and control functions necessary to start, drive, and brake a 3-phase, 4 or 8 pole brushless DC spindle motor. External Darlington power transistors or external power FETs may be used by the SSI 32M593A to drive the spindle motor.

The motor Hall sensors are directly driven and decoded by the device. The controller is optimized for a 3600 rpm motor using a 2 MHz clock. Motor protection features include jammed platter shutdown, supply and clock fault detection, all of which are indicated by a FAULT signal, and coil over-current detection and control. A LOCK signal is provided to indicate that the motor is at speed. The device's linear control loop controls the power drivers using Pulse Amplitude Modulation.

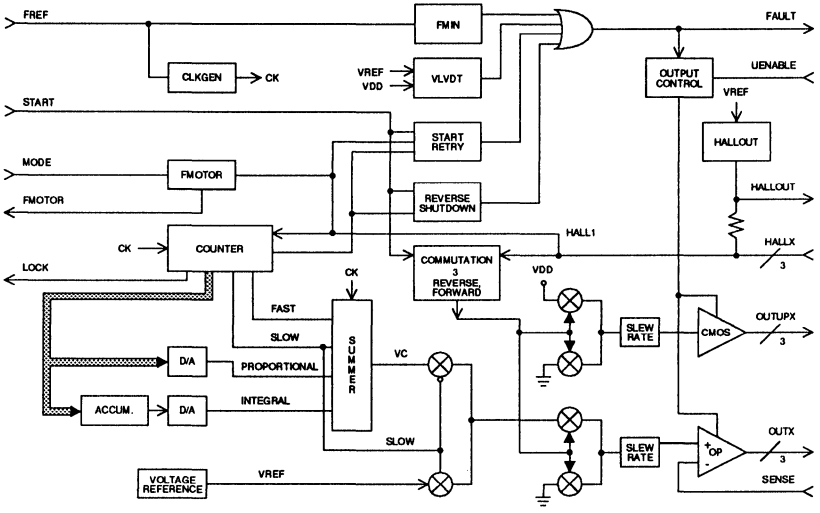
The SSI 32M593A requires a +12V power supply, and is available in 20-pin DIP or SO packages.

FEATURES

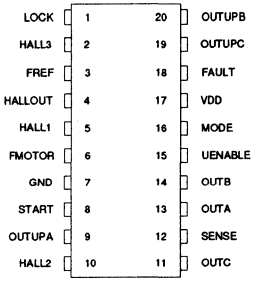
- **3-phase bipolar or unipolar operation**
- **4 or 8-pole operation**
- **3600 rpm speed control using a 2 MHz clock**
- **Highly accurate speed regulation of ±0.037%**
- **At speed indication provided**
- **Active braking function**
- **Output pre-driver for center tap or non-center tap windings**
- **Drives complementary Darlington power transistors or complementary power FETs**
- **Power supply fault protection**
- **Motor over-current protection**
- **Multiple retry on jammed spindle**
- **Single +12 volt power supply**

7

BLOCK DIAGRAM



PIN DIAGRAM



20-PIN DIP or SOL

CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION

The SSI 32M593A uses a mix of analog and digital techniques to accomplish speed control. The control signal is generated by analog conversion of a digital speed error term developed by examining the contents of a count-down counter once per motor revolution. The sign and magnitude of the remainder controls the amplitude of a correction signal applied to the motor. Commutation timing, developed from motor generated HALL signals, applies the correction in the proper phase sequence.

The device uses a Pulse Amplitude Modulation (PAM) scheme rather than Pulse Width Modulation (PWM) to avoid the switching transients and torque ripple inherent in PWM.

In operation, the SSI 32M593A is installed in a closed loop control system that maintains the speed of a 3-Phase Brushless DC motor. By monitoring the HALL signal outputs of the motor, a control voltage is developed using both digital and analog techniques. The analog portion of the control loop uses switched capacitor techniques to eliminate the need for any external passive components required for loop compensation. An operation description of the circuit follows.

CONTROL LOOP

Referring to the block diagram, the major sections of the control loop are a 19-stage Counter, Integral and Proportional channels, D/A's and a Summer.

The speed error is determined by examining the contents of the counter once per revolution. The counter is preset once per revolution by an INDEX signal developed from the HALL1 input, at the same time any remainder resulting from a 500 kHz count-down rate is loaded into a latch.

The lower LSB's of the latch, except for the LSB, are used to drive the Proportional D/A while the entire contents of the latch are accumulated to control the Integral Channel. The MSB's of the accumulator drive the Integral D/A.

If the contents of the counter indicate that the speed is outside the linear regulation range (±0.037%), this is decoded as a "FAST" or "SLOW" condition. Under these conditions the Proportional D/A output is driven to either end of its range, as appropriate. Under a slow condition, a fixed reference voltage is supplied to the output drives.

The Summer then outputs a control voltage (VC) consisting of a bias voltage plus or minus the sum of the two D/A outputs.

The Integral and Proportional channels perform several functions related to the operation of the control loop. One function is to control loop stability by maintaining the loop zero at 1 Hz. In operation this translates to the Integral channel responding to major bias point changes while the Proportional channel takes care of minor perturbations to the loop.

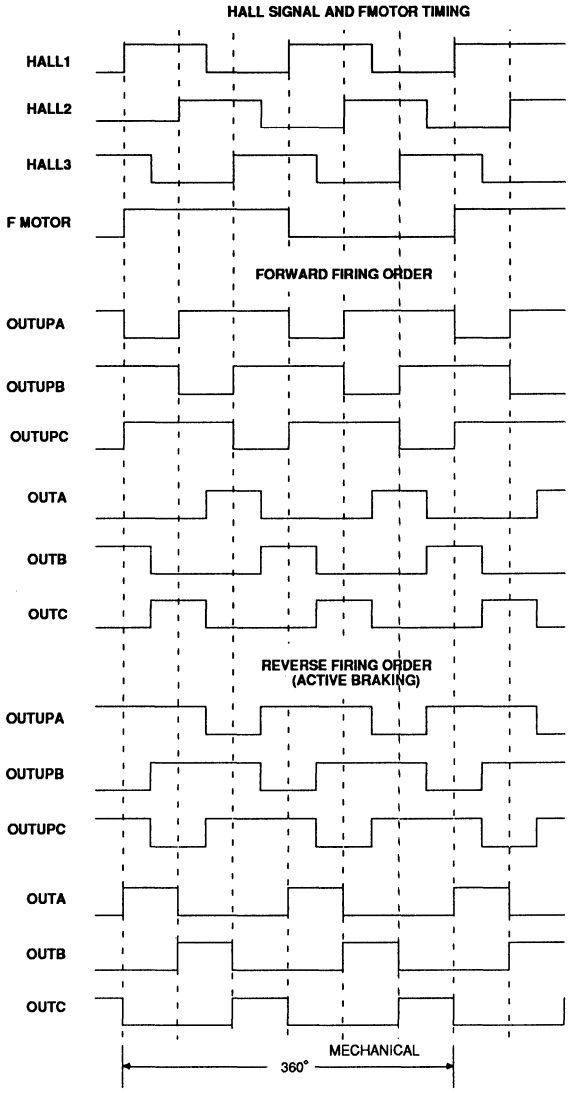
COMMUTATION

The summer output is channeled to the appropriate OUTA, B, C output according to the timing shown in Figure 1. To reduce switching transients, the outputs are slew rate controlled during each transition.

OUTUPA, B, C outputs cycle between approximately VDD in the OFF state and GND in the ON state also according to Figure 1. Again, rise and fall times are controlled during transitions.

MOTOR COIL OVER-CURRENT

Refer to SENSE input description. Sense voltage is generated by current through Re shown in the typical application. The SENSE input threshold limits the maximum coil current.



NOTE: Figure shows commutation of a 4-pole device. 8-pole devices apply same firing order twice per revolution.

FIGURE 1: Commutation Timing Diagram

FUNCTIONAL DESCRIPTION (Continued)

FAULT CONDITIONS

Four conditions cause an active high on the FAULT output pin, also disabling all drivers except as noted :

(1) Low power supply - VDD < Vlvdt

(2) No FREF clock - FREF < Fmin

(3) Stalled motor. If the delay from power onset to a positive HALL index transition or the time interval between successive HALL index transitions is greater than the specified time, the device interprets this delay as a stalled motor, reduces the motor current to zero and performs three retry cycles. If the motor continues to be stalled after three retries, then motor current is reduced to zero until such time as one positive HALL index transition is detected, the START pin is toggled, or power or FREF is removed and re-applied. After the fourth try, FAULT goes high. (See Figure 2.)

(4) Reverse shutdown speed. During active braking (START=0) the HALL sensor's phasing is changed to apply a reverse torque to the motor until the motor speed drops below the reverse shutdown speed at which time the drivers turn off to deny power to the motor and FAULT goes high. If UENABLE is high (non-center tapped motor) the device will perform passive braking after the motor speed drops below the reverse shutdown speed by enabling the lower drivers, OUTX, to dissipate any remaining coil energy. The upper drivers OUTUPX are off. (See Figure 3.)

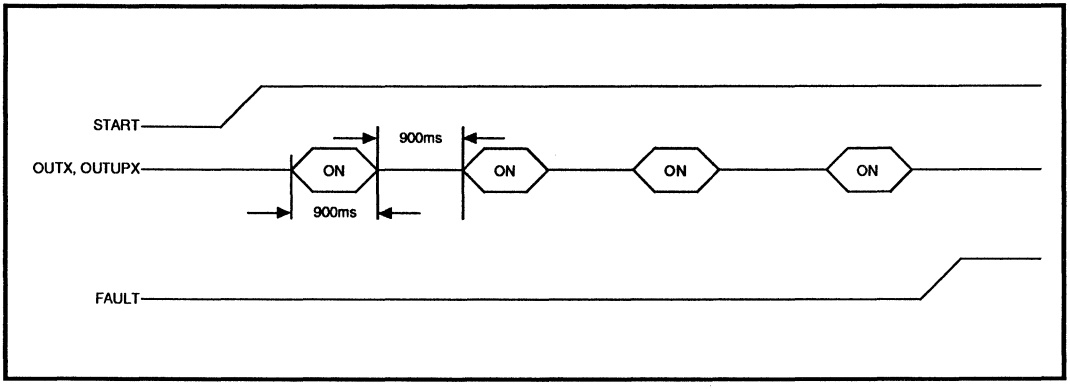


FIGURE 2: Jammed Platter Sequence

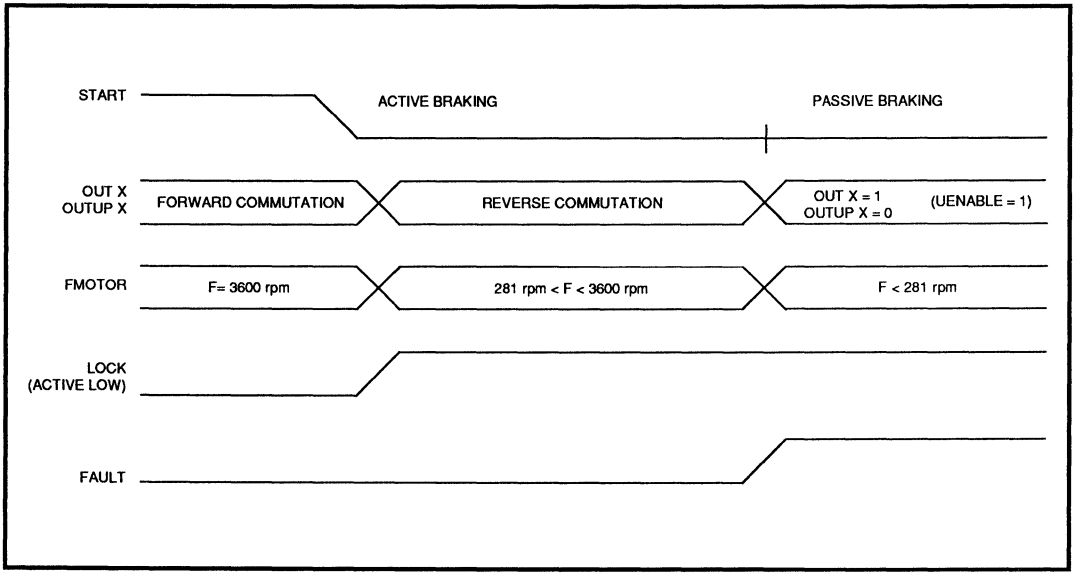


FIGURE 3: Active Braking Sequence

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PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
VDD	I	+12V Power Supply
GND	I	Ground
FREF	I	The reference clock input used to set motor speed and operate circuit blocks.
START	I	A high level on this pin enables the motor. The START input must be low during power-up and should conform to Ts set-up time. Active braking is enabled by applying a logic "zero". During active braking the commutation is changed to apply a reverse torque to the motor until the motor velocity drops below 281 rpm.
MODE	I	Mode Control. When tied high (to VDD) selects 8-pole operation where HALL1 signal is divided by four to generate an index signal. When left open, 4-pole operation is selected and HALL1 is divided by two.
UENABLE	I	Tying UENABLE to GND forces all upper outputs to their off state and disables passive braking. UENABLE must be tied to GND for unipolar center-tapped motors. Tied high or floating, UENABLE = 1 and drives bipolar motors.
FAULT	O	FAULT goes active high indicating low VDD, no FREF, a stalled motor, or motor velocity below the reverse shutdown speed.
LOCK	O	LOCK goes active low when the motor frequency is within a specified lock range.
FMOTOR	O	FMOTOR frequency indicates the motor speed, nominally 3600 rpm. FMOTOR is derived from HALL1.
SENSE	I	Coil Current Sense Input. Senses the coil current and limits the sense voltage to the specified threshold by limiting the voltage from the lower drivers. (OUTX)
HALLOUT	O	Hall Sensor Bias Output. Provides a regulated bias voltage for the hall effect sensors.
HALL1, 2, 3	I	Hall Sensor inputs that determine commutation. The TTL open-collector type motor outputs drive these inputs, which have internal resistor pullups referenced to the HALLOUT bias voltage.
OUTUPA, B, C	O	Upper motor CMOS level outputs that drive either Darlingtons or PFETs.
OUTA, B, C	O	Lower Driver Outputs. These three driver outputs drive external Bipolar or NFET power transistors to control the motor current through the current setting resistor Re. The motor current is V(sense)/Re. During normal operation, the drive voltages are adjusted as necessary to maintain the proper motor speed and drive current.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
VDD Supply Voltage	-0.5 to +14	V
Storage Temperature	-65 to +150	°C
Lead Temperature, PDIP (10 sec. soldering)	260	°C
Package Temperature, SO (20 sec. reflow)	215	°C
Input, Output pins	-0.3 to VDD +0.3	V
Inputs and outputs are protected from static charge using built-in ESD and Latchup protection devices.		

ELECTRICAL CHARACTERISTICS (Unless otherwise specified Vlvdt <Vdd<13.2V.)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VDD supply voltage		10.8	12	13.2	V
IDD supply current	includes output driver current	-	20	38	mA
PDD power dissipation	loutA or B, or C = -10 mA loutupA, or B, or C = 10 mA IHALLOUT = -10 mA	-	240	375	mW
FREF clock frequency		1.998	2	2.002	MHz
TA ambient temperature		0	-	70	°C
TTL Inputs START, FREF, UENABLE					
Vil input low voltage	Iil ≤500 µA	-	-	0.8	V
Vih input high voltage	Iih ≤100 µA	2.0	-	-	V
START set-up time (Ts)	FREF active to START ↑	100			µs
MODE Input					
Vil input low voltage		-	-	0.5	V
Vih input high voltage	Iih ≤500 µA	VDD-.5	-	-	V
HALLX Input					
Vil input low voltage		-	-	0.8	V
Vih input high voltage	External pullup current ≤1.7 mA	3.0	-	-	V
Input Pullup-Pulldown Resistance					
Internal pullup resistance	START, FREF, UENABLE	40	-	-	kΩ
Internal pullup resistance	HALLX inputs	5	-	20	kΩ
Internal pulldown resistance	MODE input	40	-	-	kΩ
Input capacitance	All inputs	-	-	25	pF

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
SENSE Input						
SENSE voltage threshold		if exceeded, driver voltage is limited	0.9	1.0	1.1	V
Input current			-100	-	+100	µA
Open Drain Outputs LOCK, FMOTOR, FAULT						
Vol output low voltage		I_{OL} = 2 mA	-	-	0.5	V
Typical external pullup resistor			-	10	-	kΩ
FAULT Indication						
Vlvdt, low voltage			7.0	-	9.5	V
Fmin, loss of FREF			-	-	100	Hz
Stuck motor, start pulses		drivers on, drivers off	-	0.90	-	sec
Number of start pulses			-	4	-	-
Reverse shutdown speed		START = 0	-	281	-	rpm
LOCK Indication						
Lock range		Measure at FMOTOR, FREF =	3594	3600	3607	rpm
Speed error		2 MHz, 10.8 < V_{DD} < 13.2	-.037		+.037	%
HALL Sensor Interface						
HALLOUT bias voltage		10.8 < VDD < 13.2, Iload = -5 mA	5.0		6.8	V
		10.8 < VDD < 13.2, Iload = -10 mA	5.0			V
Driver Outputs (FHALLX ≥ 100 Hz, V_{lvdt} < VDD ≤ 13.2, CL ≤ 500 pF unless otherwise specified.)						
Slew rate		All driver outputs	150	-	500	V/msec
OUTX	Voh	Iload = -5.0 mA	3.75	-	-	V
	Voh	Iload = -100 µA, 10.8 ≤ V_{DD} ≤ 13.2	8.0	-	-	V
	Vol off state	Iload = 3.4mA, 5.0 ≤ V_{DD} ≤ 13.2	-	-	0.5	V
OUTUPX	Vol	Iload = 10 mA	-	-	3.0	V
	Voh off state	Iload = -5 mA	V_{DD}-0.5	-	-	V
	Voh off state	Iload = -2 mA, 5.0 ≤ VDD ≤ V_{lvdt}	V_{DD}-0.5	-	-	V

APPLICATION INFORMATION

PARAMETER	RECOMMENDED	MIN	NOM	MAX	UNIT
Power Transistors					
Re, Emitter Resistor		.392	.4	.408	Ω
Power Darlington Vbe	Typical device: TIP 125, TIP 120	0.8	-	1.8	V
Power FET Vth	Typical device: IRFT 001	2	-	6	V
Power FET Rds (on)		-	-	0.4	Ω
Power FET BVds		30	-	-	V

Motor Parameters

The SSI 32M593A MSC is optimized for use with a 5 1/4" three-platter Winchester motor. The device will work for a range of motors near this nominal motor. Attempts to use a significantly different motor may require careful choice of a sense resistor for good spin-up and regulation.

KT, Torque Constant Range	(0.015 Nt-m/A nom.)	-10	-	+10	%
J, Inertia Range	(489 x 10^{-6} Nt-m-sec ^{2} nom.)	-33	-	+33	%
KD, Damping Factor Range	(31.8 x 10^{-6} Nt-m/rad/sec nom.)	-33	-	+33	%
Note: $\frac{\text{Motor Frequency (s)}}{\text{Motor Current (s)}} = \frac{KT}{Js + KD}$					

Control Loop Parameters

The motor control loop consists of counter, logic, and digital-to-analog converters that provide loop time constants. The continuous time transfer function of the on-chip control can be modeled as follows:

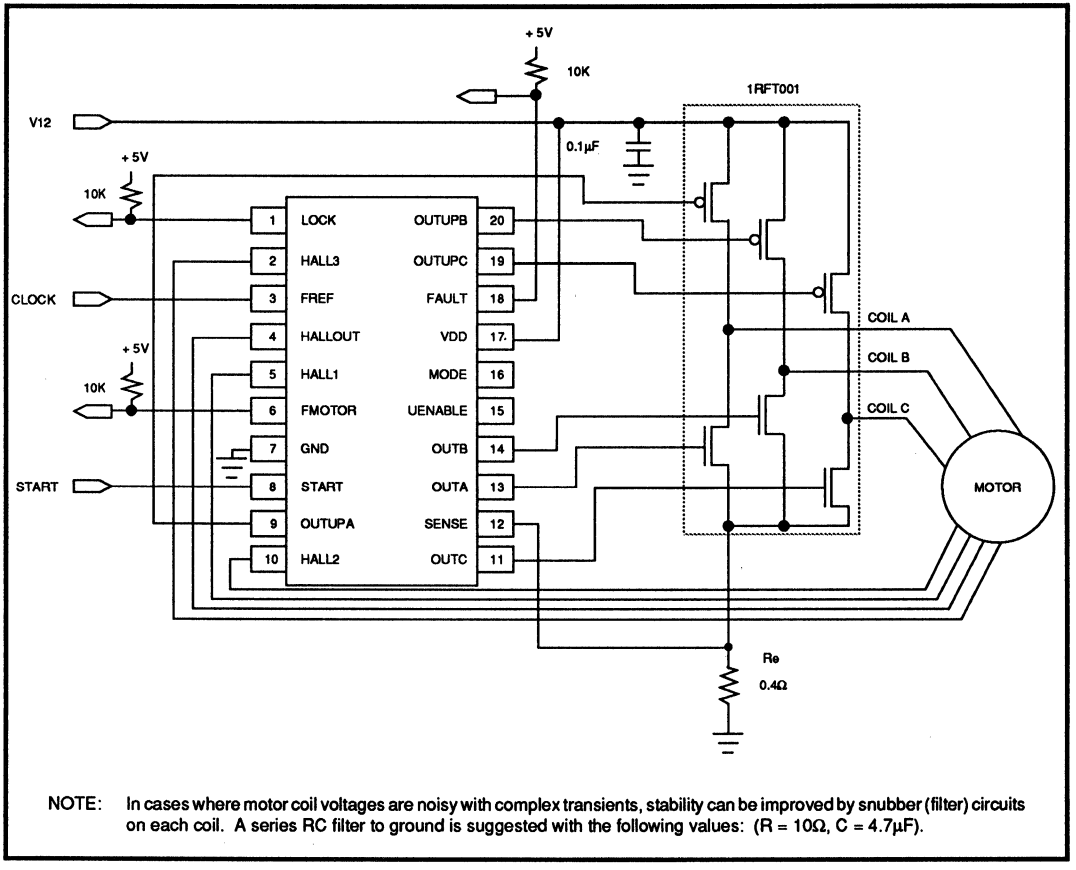
$$H(s) = \frac{Vc(s)}{Fm(s)} = \frac{Ki}{s} + Kp$$

Where: Ki = Integral Channel Gain
Kp = Proportional Channel Gain

Vc(s) is the voltage applied to the external sense resistor (Re) by the modulator. By adjusting the value of Re, the gain the motor sees can be adjusted as can the starting current.

Loop Bandwidth	Nominal motor, Re= 0.40Ω		2		Hz
Loop Zero	Ki/Kp		1.0		Hz
Kp, Proportional Channel Gain		0.198	0.213	0.227	V/rad/s
Ki, Integral Channel Gain		1.23	1.33	1.42	V/rad
Start current	Re = 0.40Ω		2.5		Amps
Running current	Re = 0.40Ω		1.5		Amps

7



NOTE: In cases where motor coil voltages are noisy with complex transients, stability can be improved by snubber (filter) circuits on each coil. A series RC filter to ground is suggested with the following values: (R = 10Ω, C = 4.7µF).

FIGURE 4:Typical Three-Phase, 4-Pole, Bipolar, Non-Center Tapped Motor Using A Power FET Module

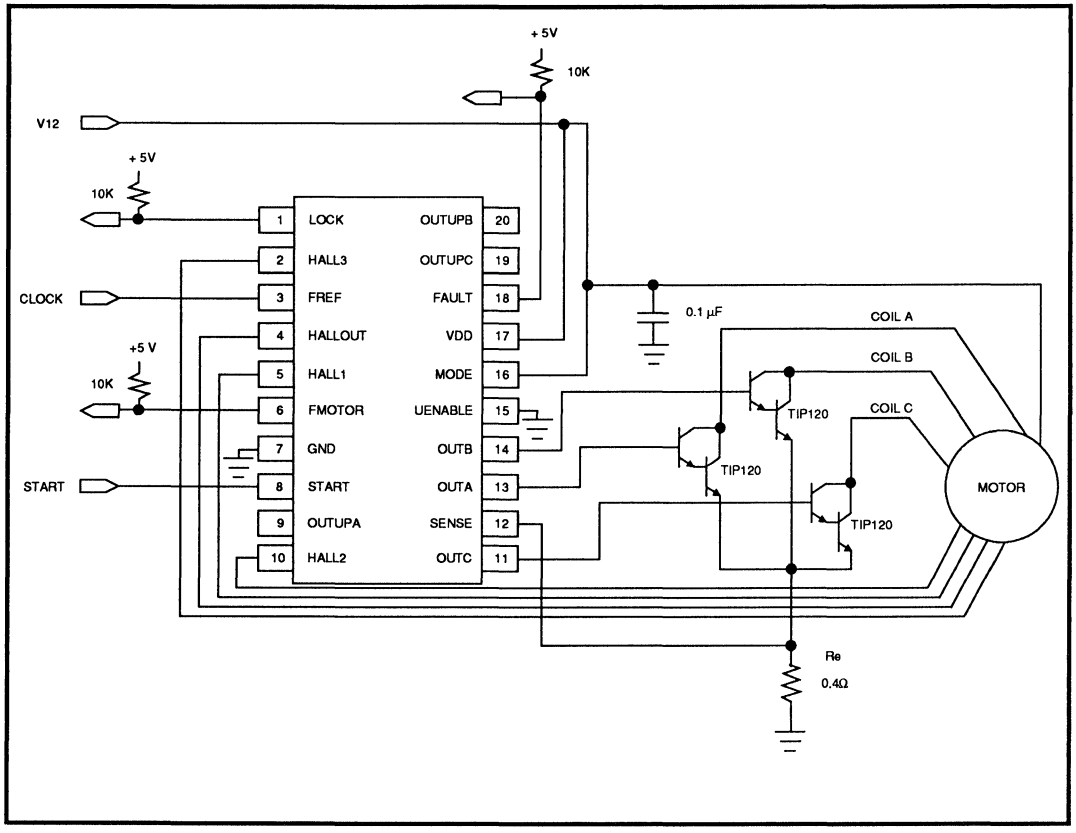


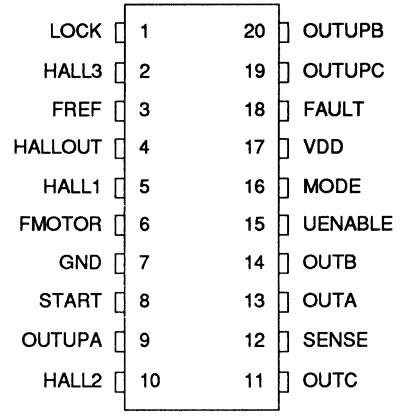
FIGURE 5:Typical Three-Phase, 8-Pole, Unipolar, Center Tapped Motor Using A Power Darlington. UENABLE Must be Tied to GND.

7

SSI 32M593A
Three-Phase Delta
Motor Speed Controller

PACKAGE PIN DESIGNATIONS

(TOP VIEW)



20-Pin DIP or SOL

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32M593A Three-Phase SOL	32M593A-CL	32M593A-CL
SSI 32M593A Three-Phase PDIP	32M593A-CP	32M593A-CP

Silicon Systems, Inc. 14351 Myford Road, Tustin, CA 92680, (714) 731-7110, FAX (714) 573-6914

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A TDK Group Company

SSI 32M594
Three-Phase Delta Motor Speed Controller
Preliminary Data

July 1990

DESCRIPTION

The SSI 32M594 is a motor speed control IC designed to provide all timing and control functions necessary to start, drive, and brake a 3-phase, 4 or 8 pole brushless DC spindle motor. External Darlington power transistors or external power FETs may be used by the SSI 32M594 to drive the spindle motor.

The motor Hall sensors are directly driven and decoded by the device. The controller is optimized for a 3600 rpm motor using a 2 MHz clock. Motor protection features include jammed platter shutdown, supply and clock fault detection, all of which are indicated by a FAULT signal, and coil over-current detection and control. A $\overline{\text{LOCK}}$ signal is provided to indicate that the motor is at speed. The device's linear control loop controls the power drivers using Pulse Amplitude Modulation.

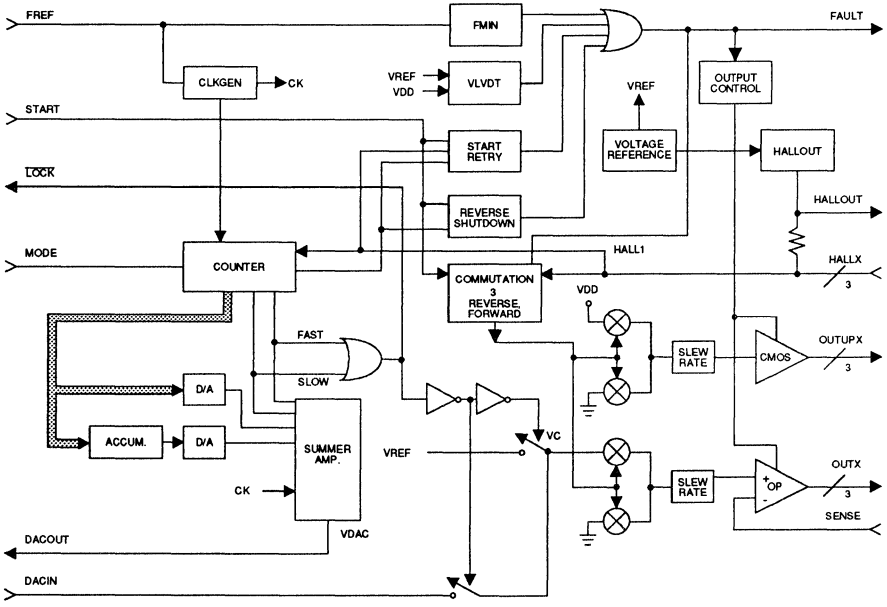
The SSI 32M594 requires a +12V power supply, and is available in 20-pin DIP or SO packages.

FEATURES

- **Supports wide range of DC brushless 3-phase motors, including 3 1/2" motors**
- **4 or 8-pole operation**
- **3600 rpm speed control using a 2 MHz clock**
- **Highly accurate speed regulation of ±0.037%**
- **Provides for gain scaling of the motor current voltage**
- **On-chip digital filter**
- **At speed indication provided**
- **Active braking function**
- **Output pre-driver for center tap or non-center tap windings**
- **Drives complementary Darlington power transistors or complementary power FETs**
- **Power supply fault protection**
- **Motor over-current protection**
- **Multiple retry on jammed spindle**
- **Single +12 volt power supply**

7

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The SSI 32M594 uses a mix of analog and digital techniques to accomplish speed control. The control signal is generated by analog conversion of a digital speed error term developed by examining the contents of a count-down counter once per motor revolution. The sign and magnitude of the remainder controls the amplitude of a correction signal applied to the motor. Commutation timing, developed from motor generated HALL signals, applies the correction in the proper phase sequence.

The device uses a Pulse Amplitude Modulation (PAM) scheme rather than Pulse Width Modulation (PWM) to avoid the switching transients and torque ripple inherent in PWM.

The SSI 32M594 generates a motor current voltage which is related to the motor speed error. This is implemented on the IC by digital/analog techniques, converting a motor frequency error derived from a reference clock and digital counter into a voltage using switched capacitor D/A's. The voltage Vc translates into a motor current across Re regulating motor speed.

In operation, the SSI 32M594 is installed in a closed loop control system that maintains the speed of a 3–Phase Brushless DC motor. By monitoring the HALL signal outputs of the motor, a control voltage is developed using both digital and analog techniques. The analog portion of the control loop uses switched capacitor techniques to eliminate the need for any external passive components required for loop compensation. An operation description of the circuit follows.

CONTROL LOOP

Referring to the block diagram, the major sections of the control loop are a 19-stage Counter, Integral and Proportional channels, D/A's and a Summer.

The speed error is determined by examining the contents of the counter once per revolution. The counter is preset once per revolution by an INDEX signal developed from the HALL1 input, at the same time any remainder resulting from a 500 KHz count-down rate is loaded into a latch.

The lower LSB's of the latch, except for the LSB, are used to drive the Proportional D/A while the entire contents of the latch are accumulated to control the Integral Channel. The MSB's of the accumulator drive the Integral D/A.

If the contents of the counter indicate that the speed is outside the linear regulation range (±0.037%), this is decoded as a "FAST" or "SLOW" condition. Under these conditions the Proportional D/A output is driven to either end of its range, as appropriate. Under a slow condition, a fixed reference voltage is supplied to the output drives resulting in a start current of Vref/Re.

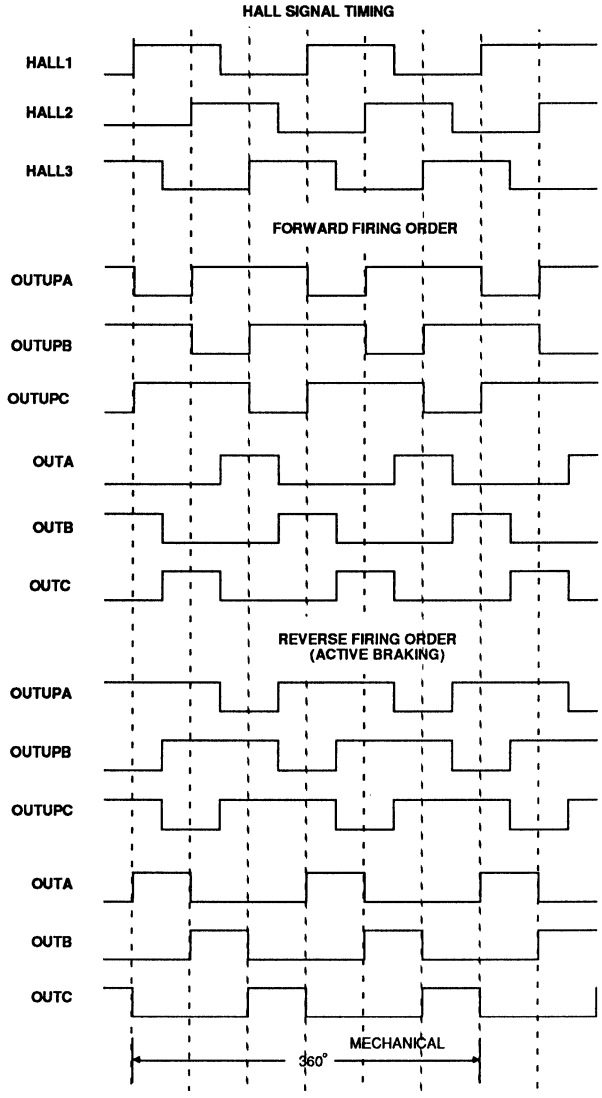
When $\overline{LOCK}$ is low, the control voltage, VDAC, from the summer is used to generate the motor running current. VDAC is a summation of integral channel voltage which cancels out offsets in the loop and motor losses, and a proportional channel voltage which tracks speed variations from the counter. The two channel voltages are then summed and weighted. The control voltage applied is externally scaleable by resistors R1 and R2 at DACOUT and DACIN (see Typical Application diagram) to fit a wide range of motors including those used in 3 1/2" drives. Note that Re affects start current while R1 and R2 affect running current as Irunning = V_{DACIN}/Re.

The Integral and Proportional channels perform several functions related to the operation of the control loop. One function is to control loop stability by maintaining the loop zero at 1 Hz. In operation this translates to the Integral channel responding to major bias point changes while the Proportional channel takes care of minor perturbations to the loop.

COMMUTATION

The summer output is channeled to the appropriate OUTA, B, C output according to the timing shown in Figure 1. To reduce switching transients, the outputs are slew rate controlled during each transition.

OUTUPA, B, C outputs cycle between approximately VDD in the OFF state and GND in the ON state also according to Figure 1. Again, rise and fall times are controlled during transitions.



NOTE: Figure shows commutation of a 4-pole device. 8-pole devices apply same firing order twice per revolution.

FIGURE 1: Commutation Timing Diagram

FUNCTIONAL DESCRIPTION (Continued)

MOTOR COIL OVER-CURRENT

Refer to SENSE input description. Sense voltage is generated by current through Re shown in the typical application. The SENSE input threshold limits the maximum coil current.

FAULT CONDITIONS

Four conditions cause an active high on the FAULT output pin, also disabling all drivers except as noted :

(1) Low power supply - VDD < Vlvdt

(2) No FREF clock - FREF < Fmin

(3) Stalled motor. If the delay from power onset to a positive HALL index transition or the time interval between successive HALL index transitions is greater than the specified time, the device interprets this delay as a stalled motor, reduces the motor current to zero and performs three retry cycles. If the motor continues to be stalled after three retries, then motor current is reduced to zero until such time as one positive HALL index transition is detected, the START pin is toggled, or power or FREF is removed and re-applied. After the fourth try, FAULT goes high. (See Figure 2)

(4) Reverse shutdown speed. During active braking (START = 0) the HALL sensor's phasing is changed to apply a reverse torque to the motor until the motor speed drops below the reverse shutdown speed at which time the drivers turn off to deny power to the motor and FAULT goes high. (See Figure 3)

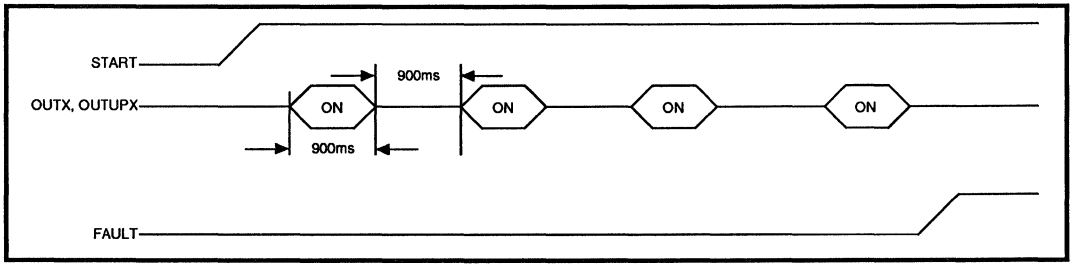


FIGURE 2: Jammed Platter Sequence

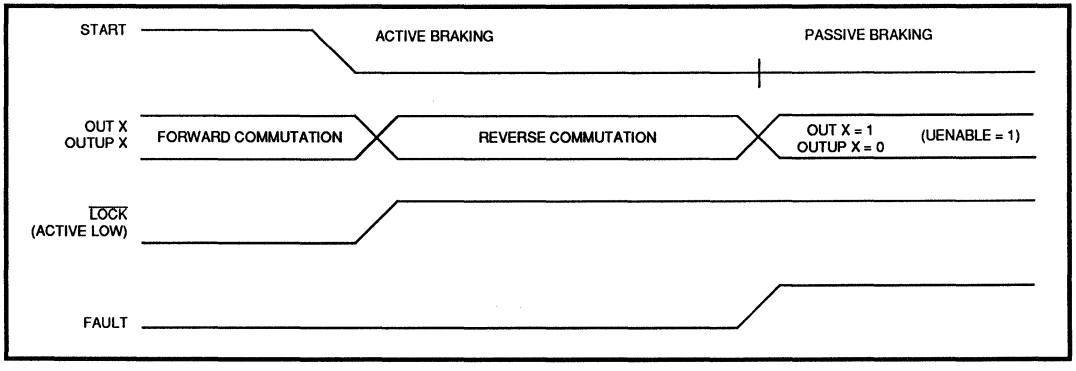


FIGURE 3: Active Braking Sequence

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
VDD	I	+12V Power Supply
GND	I	Ground
FREF	I	The reference clock input used to set motor speed and operate circuit blocks.
START	I	A high level on this pin enables the motor. The START input must be low during power-up and should conform to Ts set-up time. Active braking is enabled by applying a logic "zero". During active braking the commutation is changed to apply a reverse torque to the motor until the motor velocity drops below 281 rpm.
MODE	I	Mode Control. When tied high (to VDD) selects 8-pole operation where HALL1 signal is divided by four to generate an index signal. When left open, 4-pole operation is selected and HALL1 is divided by two.
FAULT	O	FAULT goes active high indicating low VDD, no FREF, a stalled motor, or motor velocity below the reverse shutdown speed.
$\overline{\text{LOCK}}$	O	$\overline{\text{LOCK}}$, open drain active low, goes active low when the motor frequency is within a specified lock range.
SENSE	I	Coil Current Sense Input. Senses the coil current and limits the sense voltage to the specified threshold by limiting the voltage from the lower drivers. (OUTX)
HALLOUT	O	Hall Sensor Bias Output. Provides a regulated bias voltage for the hall effect sensors.
HALL1, 2, 3	I	Hall Sensor inputs that determine commutation. The TTL open-collector type motor outputs drive these inputs, which have internal resistor pullups referenced to the HALLOUT bias voltage.
OUTUPA, B, C	O	Upper motor CMOS level outputs that drive either Darlingtons or PFETs.
OUTA, B, C	O	Lower Driver Outputs. These three driver outputs drive external Bipolar or NFET power transistors to control the motor current through the current setting resistor Re. During normal operation, the drive voltages are adjusted as necessary to maintain the proper motor speed and drive current.
DACIN	I	Reference voltage for motor current.
DACOUT	O	Summer Output (VDAC). The summation of integral and proportional channel voltages.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Operating Characteristics.

PARAMETER	RATING	UNIT
VDD Supply Voltage	-0.5 to +14V	V
Storage Temperature	-65 to +150	°C
Lead Temperature, PDIP (10 sec. soldering)	260	°C
Package Temperature, SO (20 sec. reflow)	215	°C
Input, Output pins	-0.3 to VDD +0.3	V
Inputs and outputs are protected from static charge using built-in ESD and Latchup protection devices.		

ELECTRICAL CHARACTERISTICS (Unless otherwise specified Vlvdt <VDD<13.2V.)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VDD supply voltage		10.8	12	13.2	V
IDD supply current	includes output driver current	-	20	38	mA
PDD power dissipation	IoutA or B, or C = -10 mA IoutupA, or B, or C = 10 mA IHALLOUT = -10 mA	-	240	375	mW
FREF clock frequency		1.998	2	2.002	MHz
TA ambient temperature		0	-	70	°C
TTL Inputs START, FREF					
VIL Input Low Voltage	IIL ≤500 µA	-	-	0.8	V
VIH Input High Voltage	IIH ≤100 µA	2.0	-	-	V
START Set-up time (Ts)	FREF active to START ↑	100			µs
MODE Input					
VIL Input Low Voltage		-	-	0.5	V
VIH Input High Voltage	IIH ≤500 µA	VDD-.5	-	-	V
HALLX Input					
VIL Input Low Voltage		-	-	1.0	V
VIH Input High Voltage	External pullup current ≤1.7 mA	3.0	-	-	V
Input Pullup-Pulldown Resistance					
Internal pullup resistance	START, FREF	40	-	-	kΩ
Internal pullup resistance	HALLX inputs	5	-	20	kΩ
Internal pulldown resistance	MODE input	40	-	-	kΩ
Input capacitance	All inputs	-	-	25	pF

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
SENSE Input						
SENSE voltage threshold		if exceeded, driver voltage is limited	0.9	1.0	1.1	V
Input current			-100	-	+100	µA
Open Drain Outputs $\overline{\text{LOCK}}$, FAULT						
VOL Output Low Voltage		IOL = 2 mA	-	-	0.5	V
Typical external pullup resistor			-	10	-	kΩ
FAULT Indication						
Vlvdt, low voltage			7.0	-	9.5	V
Fmin, loss of FREF			-	-	100	Hz
Stuck motor, start pulses		drivers on, drivers off	-	0.90	-	sec
Number of start pulses			-	4	-	-
Reverse shutdown speed		START = 0	-	281	-	rpm
$\overline{\text{LOCK}}$ Indication						
Lock range		FREF = 2 MHz	3594	3600	3607	rpm
Speed error		10.8 < VDD < 13.2	-0.037		+0.037	%
HALL Sensor Interface						
HALLOUT bias voltage		10.8 < VDD < 13.2, Iload = -5 mA	5.0		6.8	V
		10.8 < VDD < 13.2, Iload = -10 mA	5.0			V
Driver Outputs (FHALLX ≥ 100 Hz, Vlvdt < VDD ≤ 13.2, CL ≤ 500 pF unless otherwise specified.)						
Slew rate		All driver outputs	150	-	500	V/msec
OUTX	VOH	Iload = -7.5 mA	3.75	-	-	V
	VOH	Iload = -100 µA, 10.8 ≤ VDD ≤ 13.2	8.0	-	-	V
	VOL off state	Iload = 3.4mA, 5.0 ≤ VDD ≤ 13.2	-	-	0.5	V
OUTUPX	VOL	Iload = 10 mA	-	-	3.0	V
	VOH off state	Iload = -5 mA	VDD-0.5	-	-	V
	VOH off state	Iload = -2 mA, 5.0 ≤ VDD ≤ Vlvdt	VDD-0.5	-	-	V

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APPLICATION INFORMATION

PARAMETER	RECOMMENDED	MIN	NOM	MAX	UNIT
Power Transistors					
Power Darlington Vbe	Typical device: TIP 125, TIP 120	0.8	-	1.8	V
Power FET Vth	Typical device: IRFT 001	2	-	6	V
Power FET Rds (on)		-	-	0.4	Ω
Power FET BVds		30	-	-	V

R1, R2

R1/(R1 + R2)		0.02	0.2	1.0	
R1 + R2		20	50	200	kΩ

$$I\ running = \frac{R1}{R1+R2} \cdot \frac{VDAC}{Re}$$

Where $VDAC = Kp \cdot \Delta f + Ki \cdot \int \Delta f \cdot \Delta t$

Kp = Proportional constant = .213 V/rad/sec

Ki = Integral constant = 1.33 V/rad

Δf = Frequency error

Motor Parameters

The SSI 32M594 MSC is optimized for use with a wide range of Winchester motors including 3 1/2" motors. Torque Constant Range (KT) of 0.01 to 0.02 Nt - m/A and an Inertia Range (J) from 0.5 to 6.5 x 10^{-4} Nt – m – sec^2. The choice of R1, R2 and Re will be affected by motor parameters, so some care in their selection is recommended.

Control Loop Parameters

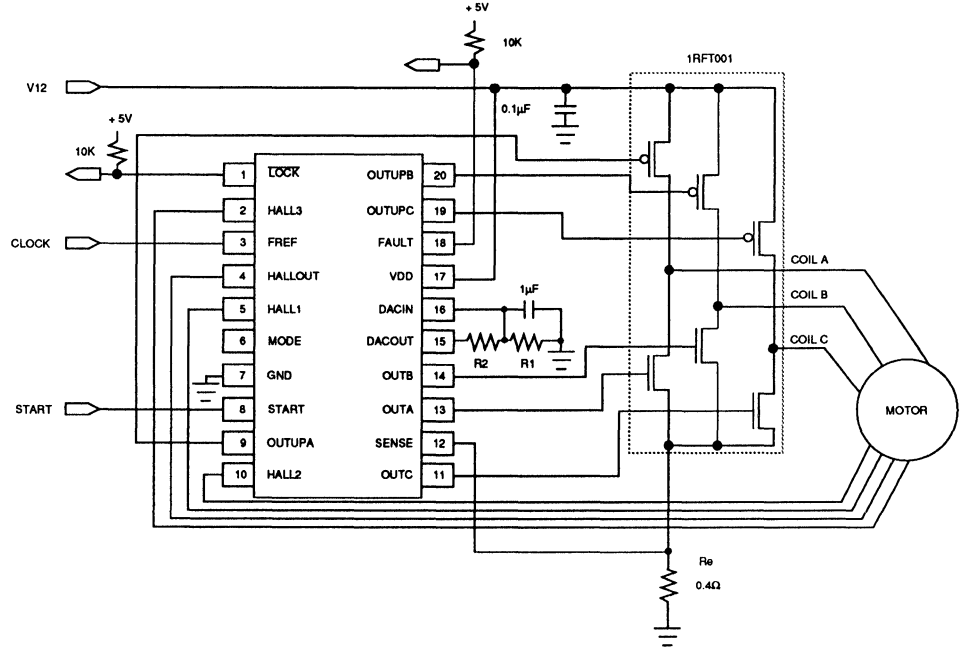
The motor control loop consists of counter, logic, and digital-to-analog converters that provide loop time constants. The continuous time transfer function of the on-chip control can be modeled as follows:

$$H(s) = \frac{Vc(s)}{Fm(s)} = \frac{Ki}{s} + Kp$$

Vc(s) is the voltage applied to the external sense resistor (Re) by the modulator. By adjusting the value of Re, the gain the motor sees can be adjusted as can the starting current.

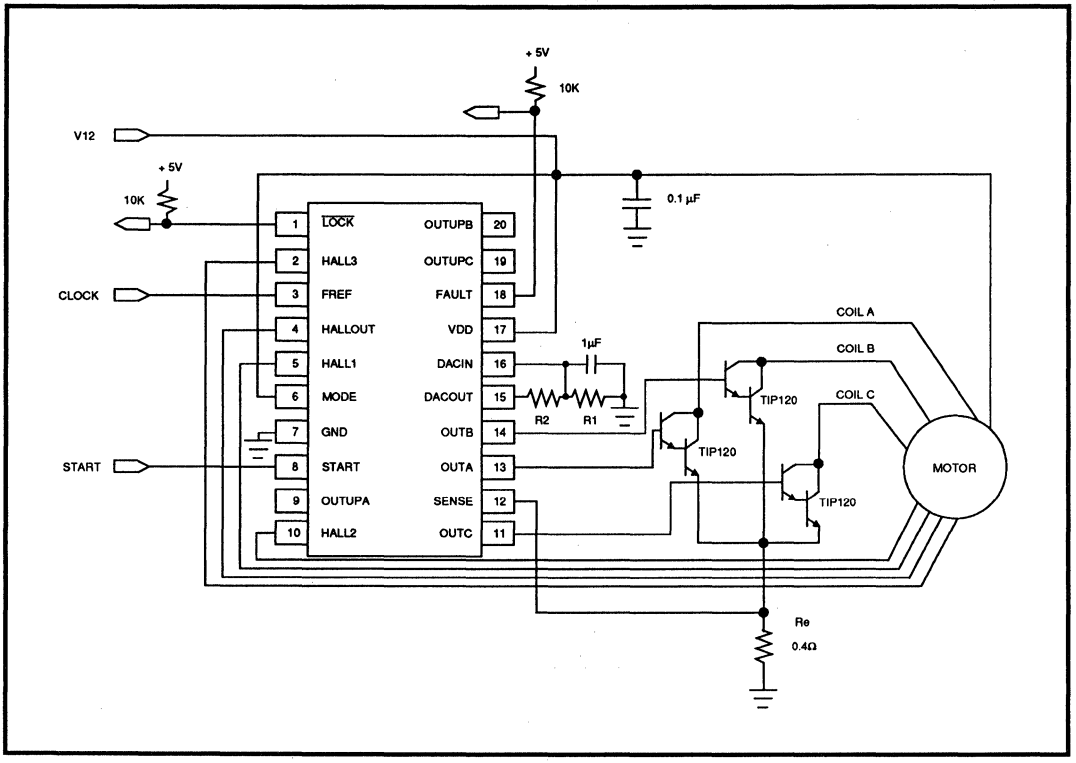
Control Loop Parameters (Continued)

PARAMETER	RECOMMENDED	MIN	NOM	MAX	UNIT
Loop Bandwidth	Nominal motor, Re = 0.4Ω		2		Hz
Loop Zero	Ki/Kp		1.0		Hz
Kp, Proportional Channel Gain		0.198	0.213	0.227	V/rad/s
Ki, Integral Channel Gain		1.23	1.33	1.42	V/rad
Start current		1.0	2.0	3.0	Amps
Running current		0.1	0.2	0.3	Amps



NOTE: In cases where motor coil voltages are noisy with complex transients, stability can be improved by snubber (filter) circuits on each coil. A series RC filter to ground is suggested with the following values: (R = 10Ω, C = 4.7 µF).

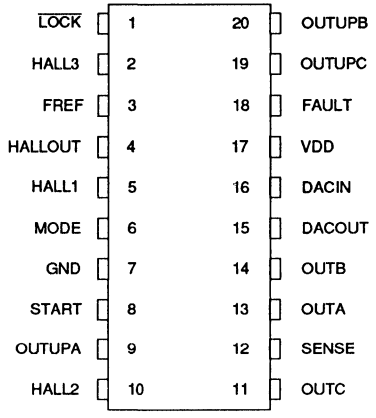
**Typical Three-Phase, 4-Pole, Bipolar,
Non-Center Tapped Motor using a Power FET Module**



**Typical Three-Phase, 8-Pole, Unipolar,
Center Tapped Motor using a Power Darlington. UENABLE must be tied to GND.**

PACKAGE PIN DESIGNATIONS
(TOP VIEW)

CAUTION: Use handling procedures necessary for a static sensitive component.



20-Pin PDIP or SOL

7

ORDERING INFORMATION

PART DESCRIPTION	ORDERING NUMBER	PACKAGE MARK
SSI 32M594 Three-Phase Delta Motor Speed Controller		
20-Pin SOL	32M594-CL	32M594-CL
20-PIN PDIP	32M594-CP	32M594-CP

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc. 14351 Myford Road, Tustin, CA 92680, (714) 731-7110, FAX (714) 573-6914

Notes:

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SSI 32M595
Hall Sensorless Motor Speed Controller
Advance Information

December 1991

DESCRIPTION

The SSI 32M595 is a motor speed control IC designed to provide all timing and control functions necessary to start, drive and brake a 3-phase, 4, 8 or 12 pole brushless DC spindle motor. External Darlington power transistors or external power FETs may be used by the SSI 32M595 to drive the spindle motor.

The SSI 32M595 implements a back EMF sensing circuit which determines when to advance the commutation state of the motor. No external sensors are required when using the 32M595. The drive controlling microprocessor initially starts the motor enabling motor current by asserting the MENABLE pin. The microprocessor then generates a stream of ADVANCE pulses which initially advances the motor. Once the motor has advanced with sufficient speed (usually within one revolution) for the back EMF sense logic to detect motion, the microprocessor work is done. The 32M595 will spin the motor up and regulates the speed all without microprocessor involvement.

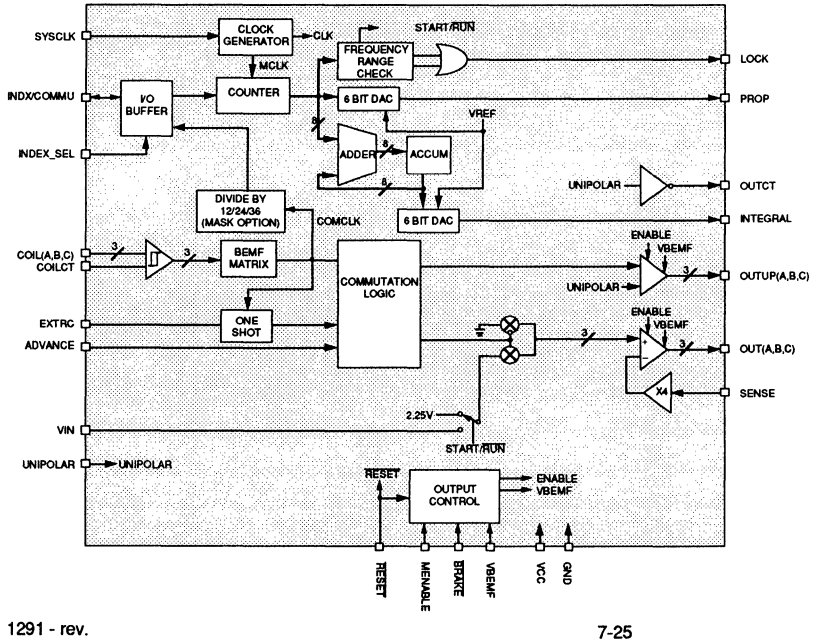
(continued)

FEATURES

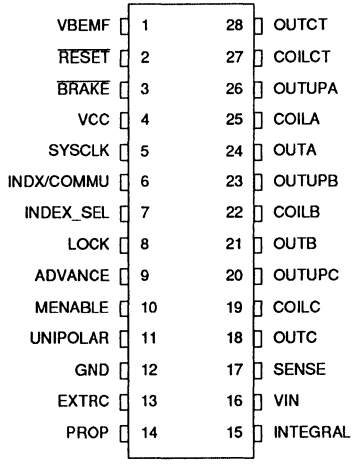
- **Sensorless motor commutation**
- **3-phase, 4, 8 or 12 pole bipolar or unipolar motor operation**
- **Compatible with 5 and 12 volt, DELTA/Y/ STAR motors**
- **3600 rpm precise speed control using 2 MHz clock**
- **External two resistor loop compensation**
- **Drives complementary Darlington power transistors or complementary power FETs**
- **At speed indicator**
- **Dynamic braking on command or power loss**
- **Motor current limiting**
- **Single +5V power supply/low power sleep mode**

7

BLOCK DIAGRAM



PIN DIAGRAM



DESCRIPTION (continued)

Motor speed control is accomplished by measuring the period of each revolution with a 500 kHz clock signal (SYSCLK divided by four). Period resolution is therefore 2 microseconds with the desired period being 8333 counts (16.66 milliseconds, or 3600.144 RPM). Motor armature position is determined by monitoring the coil voltage of the winding that is not presently being driven by the drivers. The back EMF at the coil in conjunction with the state of the output drivers, indicates armature position. The back emf is compared to a reference (COILCT) and initiates commutation "events" when the appropriate comparison is made. Commutation is the sequential switching of drive current to the motor windings. Because the back EMF comparison event occurs prior to the time when optimum commutation should occur, it is preferred to delay commutation by a predetermined time after the comparison. The commutation delay is provided by a non-retriggerable one-shot circuit wherein the time delay is a function of external R and C timing components. The one-shot circuit also provides a "noise filter" function which holds off retriggering and blanks back EMF comparison events for an additional period of time (approximately one half the commutation delay) after commutation since commutation of the motor windings typically results in large transient voltages which could falsely indicate "commutation events." The six commutation states are given below.

TABLE 1: Commutation States

	COMMU	OUTA	OUTB	OUTC	OUTUPA	OUTUPB	OUTUPC
Reset state	0	off	on	off	on	off	off
ADVANCE ↑	1	off	off	on	on	off	off
ADVANCE ↑	0	off	off	on	off	on	off
ADVANCE ↑	1	on	off	off	off	on	off
ADVANCE ↑	0	on	off	off	off	off	on
ADVANCE ↑	1	off	on	off	off	off	on

NOTE: For OUT(S), off is approx. 0 volts. For OUTUP(S), off is approximately VBEMF.

The period counter is loaded with a count of 8333 initially, and the period measurement results in residual counts (ideally zero) in the period counter as it counts down during the index to index time. The residual count is fed to the proportional DAC (5 bits plus sign). When there is no period error the PDAC will output 1/2 full scale (2.25/2 volts) from PROP, too short a period will output a lower voltage, and too long a period will output a higher voltage, each depending on the amount of period error. When the residual count is within ±15 counts of zero, the motor status is indicated as "in lock." The lower eight bits of the period counter are fed to an accumulator which adds the present period residue to the previous accumulation thus accomplishing an integrating effect to force the speed error to zero over time. The upper six bits of the accumulator are fed to the integral DAC whose output is INTEGRAL. Gross period errors will cause PROP and INTEGRAL to saturate at the appropriate extreme to achieve the maximum corrective control voltage.

The outputs PROP and INTEGRAL are connected to VIN with an external resistor network. The resistor values are selected to set the required loop response based on motor and system requirements. Input pin VIN is the non-inverting input of a linear transconductance amplifier which uses the lower driver transistor that is presently active per the commutation state as the power driver element. An external resistor is used to sense the current in the drive transistor source (and hence the motor coil current). The voltage across the sense resistor is amplified by a gain stage (Av = 4) and fed to the inverting input of the transconductance output stage.

When the period error exceeds 256 counts too slow, 2.25 volts is selected as the control voltage in lieu of VIN. Maximum motor current is limited to a value such that Imotor ≤ 2.25v /(4 • Rsense).

A low-power state can be selected if desired. The motor should be de-energized either by invoking RESET or de-asserting MENABLE (either will cause the drivers to the motor to "float" and the motor to coast to a stop). $\overline{\text{BRAKE}}$ can be asserted after $\overline{\text{RESET}}$, and the motor will be actively "braked" to a more rapid stop by routing the motors own back EMF to the lower driver transistors turning them on. When $\overline{\text{BRAKE}}$, $\overline{\text{RESET}}$, and MENABLE are low, the analog circuitry is de-biased, the clock is disabled, the upper pre-driver outputs become logic high (to turn off all upper drivers including the center tap if used), and the lower pre-driver outputs become logic high, turning the lower drivers on.

Motor starting is accomplished with a companion microprocessor utilizing ADVANCE, MENABLE, $\overline{\text{RESET}}$, and COMMU. The microprocessor can assert $\overline{\text{RESET}}$ to initialize the commutation counter and then increment the counter with ADVANCE. ADVANCE at logic high excludes internal commutations. COMMU provides feedback to the microprocessor on motor activity. The microprocessor must enable the drivers with MENABLE and UNIPOLAR bits as required.

TABLE 2

$\overline{\text{BRAKE}}$	$\overline{\text{RESET}}$	MENABLE	MODE/USE	ANALOG	COUNTERS	OUTS	OUTUPS
0	0	0	SLEEP/LOW POWER	OFF	RESET	VBEMF	VBEMF
0	0	1	BRAKE/POWER OFF	ON	RESET	VBEMF	VBEMF
0	1	0	FLOAT/RETRACT	ON	ACTIVE	0V	VBEMF
0	1	1	FLOAT/RETRACT	ON	ACTIVE	ACTIVE	VBEMF
1	0	0	FLOAT/RETRACT	ON	RESET	0V	VBEMF
1	0	1	FLOAT/RETRACT	ON	RESET	0V	VBEMF
1	1	0	FLOAT/IDLE	ON	ACTIVE	0V	VBEMF
1	1	1	RUN	ON	ACTIVE	ACTIVE	ACTIVE

NOTE: MENABLE effective with VCC and VBEMF present. $\overline{\text{BRAKE}}$ and $\overline{\text{RESET}}$ effective with VBEMF present.

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
VBEMF	I	Voltage Back EMF. The motor power supply (VBR) through a power diode is VBEMF. The sources of the external PFETS are connected to VBEMF as is the VBEMF pin of the circuit. During power failure and motor spin down, this voltage is used to provide power for head retraction and subsequently, motor braking.
$\overline{\text{RESET}}$	I	RESET [inverse] pin. When asserted low, internal counters and registers are cleared. Refer to Table 2. $\overline{\text{RESET}}$ and $\overline{\text{BRAKE}}$ will control outputs to external FETs per Table 2 with only VBEMF present (power off retract and dynamic braking).
$\overline{\text{BRAKE}}$	I	Brake [inverse] pin. $\overline{\text{BRAKE}}$ is used to provide a delay between the initiation of Fault-induced head retract and motor braking. A capacitor to ground and a resistor to $\overline{\text{RESET}}$ are selected such that 1.2*R*C is equal to the maximum time required for retract.
SYSCLK	I	System Clock pin. Reference frequency for motor speed measurement. A 2.000 MHz SYSCLK will result in 3600 RPM motor speed for 8 pole motors. SYSCLK can be set to other frequencies to obtain different rotational speed or operate with motors other than 8-pole configuration (use of an external index signal is only valid for 8-pole motors).

PIN DESCRIPTION (continued)

NAME	TYPE	DESCRIPTION
INDX/COMMU	I/O	External Index (input)/Commutation count (output) pin. When selected with INDEX_SEL set high, this pin is used to provide a once-per-revolution indication of rotational position and speed to the circuit. With INDEX_SEL low, COMMU (the LSB of the commutation counter) is presented as an output.
INDX_SEL	I	Index Select pin. See above.
LOCK	O	Lock pin. When the motor period is within ±15 counts of nominal, the motor is indicated as "in lock" with LOCK high.
ADVANCE	I	Advance pin. ADVANCE is used to increment the commutation counter. The rising edge of ADVANCE will increment the counter. ADVANCE held high will inhibit internal incrementing of the counter, ADVANCE held low permits the normal operation of commutation from back EMF events.
MENABLE	I	Motor Enable pin. MENABLE asserted high will place the pre-driver outputs into active mode per the state of the commutation counter. MENABLE low will de-activate pre-driver outputs so that the external driver transistors are all "off," and the motor coils are "floating." In the "sleep" state (MENABLE=$\overline{\text{BRAKE}}$=$\overline{\text{RESET}}$= low), upper drivers are off, lower drivers are all on.
UNIPOLAR	I	Unipolar selection. When asserted high, the unipolar mode of operation is selected. Upper drivers are de-activated and OUTCT goes low to turn on the Center tap driver transistor.
EXTRC	I	External R-C pin. A resistor to VCC and a capacitor to ground are connected to this pin to provide commutation delay. The commutation delay will be 0.56*R*C. After the commutation delay, this timing block provides a noise rejection interval to reject transients on the motor coils due to commutation. The noise rejection interval is an additional 0.29*R*C. The total time (commutation delay and noise rejection interval 0.85*R*C) must be less than a commutation cycle time.
PROP	O	Proportional DAC output pin. The proportional channel output is the lowest 5 bits plus sign of the period measuring counter. The LSB signifies a 2 microsecond period variation.
INTEGRAL	O	Integral DAC output pin. The integral channel output comes from the upper six bits of an eight bit accumulator. The accumulator adds the lower eight bits of the period measurement to the previous value obtained from prior period measurements and accumulations.
VIN	I	Control Voltage input pin. The combination of external driver transistor and internal predriver circuit form a transconductance amplifier which will set motor current in relation to VIN. In conjunction with the SENSE input and the gain of the Sense amplifier, transconductance (Gm) will be Gm = Im/VIN = 1/(Rs*4)
SENSE	I	Current monitoring Sense Amplifier (high side) input pin. The external driver FET sources are connected to a current sensing resistor to monitor motor current. The circuit will control the voltage across this resistor (multiplied by the gain of 4 in the sense amplifier) to match either VIN (during normal operation) or internal 2.25V (during low-speed operation).

PIN DESCRIPTION (continued)

NAME	TYPE	DESCRIPTION
OUTA, OUTB, OUTC	O	Predriver Outputs. These pins provide drive to the gates of the external power N-channel FETS. They are configured as open drain with an internal 10,000 ohm pull-up resistor to the VBEMF pin.
OUTUPA, B, C	O	Predriver Pull-up Outputs. Open drain, internal resistive pull-up (nominal 10KΩ) to VBEMF for use with external PFETS.
OUTCT	O	Center Tap predriver. OUTCT drives an external PFET driver which connects the motor center tap to the positive power supply for unipolar drive applications. OUTCT has the same characteristics as OUTUPA, etc. and is enabled via the UNIPOLAR pin.
COILA, COILB, COILC, COILCT	I	Back EMF inputs from motor coils. Inputs to be connected to their respective motor coils and center tap for sensing generated back emf voltages. The circuit uses the back EMF voltages to determine rotor position and effect commutation.
VCC	I	5 volt power pin.
GND	I	Ground connection. GND is also the low side input to the current SENSE amplifier and care should be taken to see that GND and the low side of the sense resistor are at the same potential.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Exposure to conditions in excess of the conditions given below may result in permanent damage or affect device reliability

PARAMETER		MIN	MAX	UNIT
Supply Voltage	VCC VBEMF	-0.3 -0.3	7.0 25.0	V V
Digital Inputs/ Outputs	SYSCLK, MENABLE ADVANCE, UNIPOLAR INDEX_SEL, INDX/COMMU, LOCK	-0.3	VCC+0.3	V
Analog I/O	PROP, INTEGRAL, EXTRC, VIN	-0.3	VCC+0.3	V
Motor Interface	COIL(CT,A,B,C) UPOUT(A,B,C), OUTCT OUT(A,B,C), $\overline{\text{BRAKE}}$ SENSE, $\overline{\text{RESET}}$	-0.3	25.0	V
Storage temperature	Tstg	-65	150	°C
Lead temperature	Tlead		300	°C

OPERATING CONDITIONS

PARAMETER		MIN	MAX	UNIT
Supply voltage	VCC	4.75	5.25	V
	VBEMF	4.75	13.2	V
Supply current	ICC	1.0	6.0	mA
	ICC, sleep mode	0.05	1.0	mA
	IVBEMF	1.0	10.0	mA
	IVBEMF, sleep	0.1	1.5	mA
Ambient Temp	Ta	0	70	°C
Capacitive Load Digital I/O	Cl	0	100	PF
Resistive load PROP, INTEGRAL	Rla	5000		Ω
Capacitive load PROP, INTEGRAL	Cla	0	40	PF

PARAMETRIC REQUIREMENTS

DIGITAL INPUTS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Fmax, SYSCLK			4.5		MHz
Twh, Twl, SYSCLK width high or low		40			ns
External Index, INDX/COMMU (as input) Pulse width		200			ns
Input Leakage, INDX/COMMU		10			µA
Input Leakage, others		1			µA
Vil (EXTINDX, SYSCLK, MENABLE, ADVANCE, UNIPOLAR, INDX_SEL)				0.8	V
Vih (inputs above)		2.0			V
Vil ($\overline{\text{RESET}}$, $\overline{\text{BRAKE}}$)	VBEMF> 4.5V			0.3	V
Vih ($\overline{\text{RESET}}$, $\overline{\text{BRAKE}}$)	VBEMF> 4.5V	2.0			V

EXTERNAL RC PIN (EXTRC)

Timing resistor		10K		10M	Ω
Timing capacitor		100		-	pF
Delay time variation	relative to T0	-5		+5	%

T0 is the commutation delay and is given by the relationship T0= 0.56RC.
Suggested value for C would be 470 to 1000 pF. An external R and C must always be provided such that the time constant, T0 is greater than 10 microseconds.

PROPORTIONAL (PROP), INTEGRAL (INTEGRAL) DAC OUTPUTS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Output voltage	Iout<0.10mA VCC=5.0v	0		2.25V ±5%	V
DAC Step size Output impedance	 0.5v<V out<2.0v Iout=0.10mA	.032		.039 200	V Ω
Kp, proportional gain Ki, integral gain		0.70 10.48		0.85 12.75	V/rad/s V/rad f

DIGITAL OUTPUTS, LOCK, INDX/COMMU

Voh Vol	Iout=-100uA Iout=2.0mA	2.4		 0.4	V V
Tdts, Time delay to tri-state output	INDX_SEL high to high impedance on INDX/COMMU	10		100	ns
Tdoe, Time delay to enable as output pin	INDX_SEL low to drive state	10		100	ns

VIN

Input Voltage		0		2.25	V
Input current	0<Vin<2.5v	-1		+1	µA

OUTUPA, OUTUPB, OUTUPC, OUTCT

Rout, internal pull-up resistor	Output in high state	5K		20K	Ω
Vout (low)	Iout <3 mAmp VBEMF=13.2 volts			1.0	V

OUTA, OUTB, OUTC

Rout, internal pull-up resistor	Output in high state	5K		20K	Ω
Vout (low)	Iout<5 mAmp			1.0	V

SENSE

Vin, SENSE	normal operation	0.0		0.50	V
Iin, SENSE	0.0<Vin<1.0 volt	-10		+10	µA
Cin				20	pF
Transconductance gain from VIN to motor current (steady-state) will be given by: G= Imotor/VIN =1/RSENSE4 for rotational speeds greater than 3490 RPM.					

COILA, COILB, COILC, COILCT

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Rin	-.3v <Vin<15v	100K			Ω
Rin - COILCT	-.3v<Vin<15v	30K			Ω
Cin				10	pF

OPERATING REQUIREMENTS

LOCK indication range	SYSCLK=2.000 MHz	3593.5		3606.5	RPM
Speed resolution		-.012		+.012	%

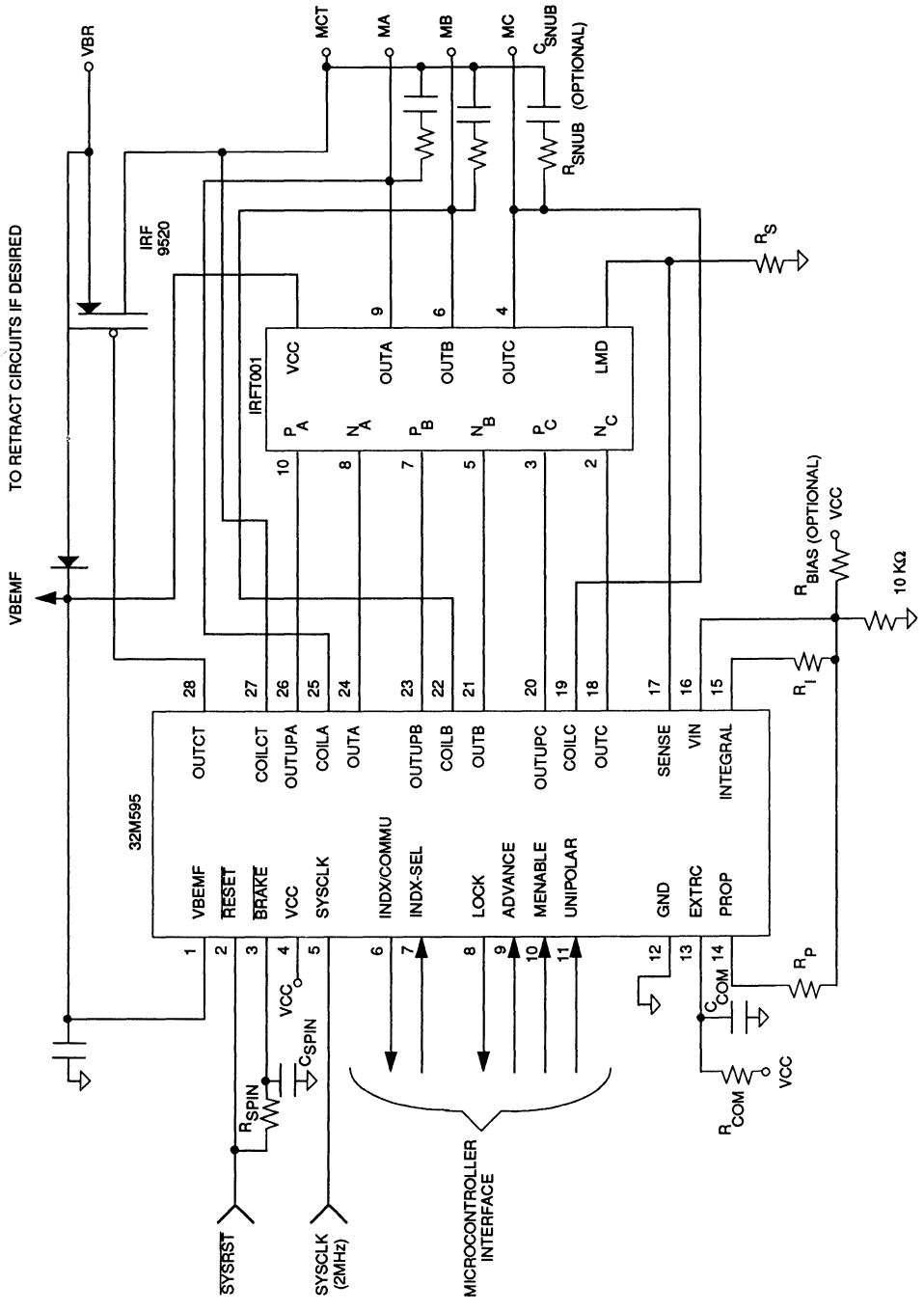
APPLICATIONS INFORMATION

Usage of INDX (External Index input)

Normal operation is performed with an internal Index signal derived from the commutation counter. The period of the Index signal is measured and controlled by the circuit to result in a rotational rate of 3600 revolutions per minute. Within the range of 3593.5 to 3606.5 revolutions per minute the spindle will be "in lock." After the motor is started and accelerated to speed (LOCK bit high), an external Index signal may be selected. Applying external index pulses (at a rate within the lock range) and setting INDEX_SEL bit to high will start the following sequence.

The circuit will complete the period measurement of the latest internal index period and then begin to measure the time between the last internal index and the next external index pulse. This will most likely be shorter than nominal assuming the two events are asynchronous. If the period measured is not within 3 percent of the expected value (16.667 milliseconds), the IDAC and PDAC will not be updated with a new correction value but will continue to output the previous value.

The LOCK output will be set low (indicating out of lock). The next period measured will be between the first and second external index pulses and will presumably be within the lock range so that LOCK will be set high. If the period is within ± 3 percent of the desired value, the IDAC and PDAC will update. Similarly, during operation with external index, a missing index pulse would look like a gross speed error and no IDAC or PDAC update will take place. The microprocessor should verify that after the switch-over to external index, the circuit goes back to LOCK. If external index is used, it should come from a reliable source with low jitter (less than 10 microseconds). The circuit must have an index pulse in order to measure period, and the "status" of LOCK can only be determined with ongoing index timing pulses. Complete removal of index will hold the last LOCK status and IDAC/PDAC values even though the actual speed may be out of the LOCK range.



Typical Bipolar Start/Unipolar Run 32M595 Application

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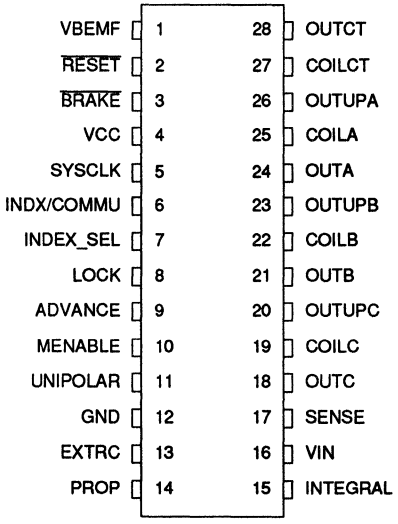
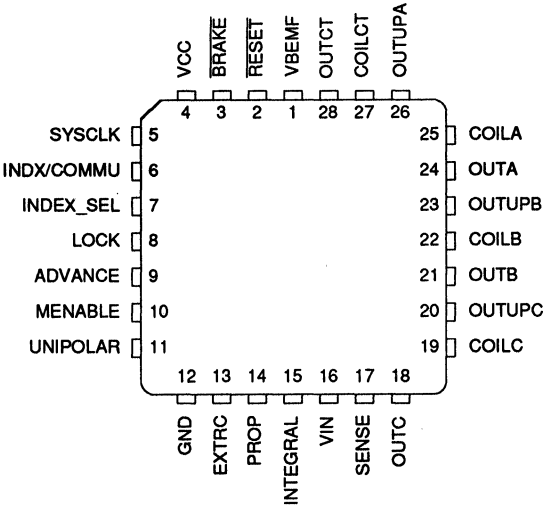
SSI 32M595
Hall Sensorless
Motor Speed Controller

PACKAGE PIN DESIGNATIONS
(Top View)



28-pin PDIP or SOL



28-pin PLCC

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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A TDK Group Company

SSI 32M7010
Hall-Sensorless Motor Speed Control
Preliminary Data

December 1991

DESCRIPTION

The (Spindle) Motor Speed Control in conjunction with several external components, provides starting, accelerating, and precise rotational speed regulation functions. Different circuit versions are provided to control 4-, 8-, or 12-pole brushless DC motors without the need for Hall sensors. Control is accomplished via five pins and operation is monitored via two pins. The complete speed regulation control loop is contained in the circuit and the companion microprocessor is only required during start and to monitor status.

Motor speed control is accomplished by measuring the period of each revolution with a 500 kHz clock signal (SYSCLK divided by four). Period resolution is therefore 2 microseconds with the desired period being 8333 counts (16.66 milliseconds, or 3600.144 RPM).

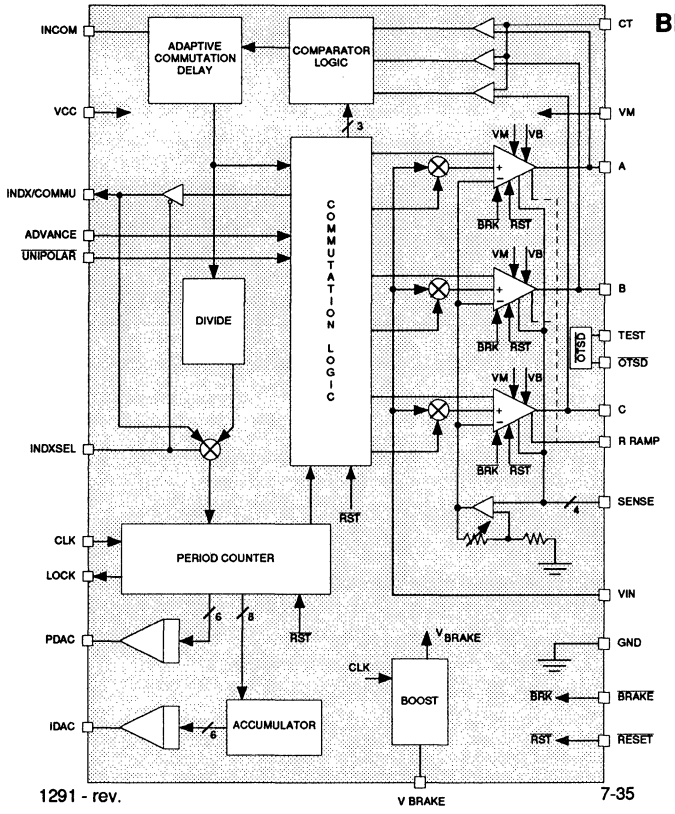
Motor armature position is determined by monitoring the coil voltage of the winding that is not presently being driven by the drivers. The back-emf at the coil in conjunction with the state of the output drivers, indicates armature position. The back emf is compared to a reference (CT) and initiates commutation when the

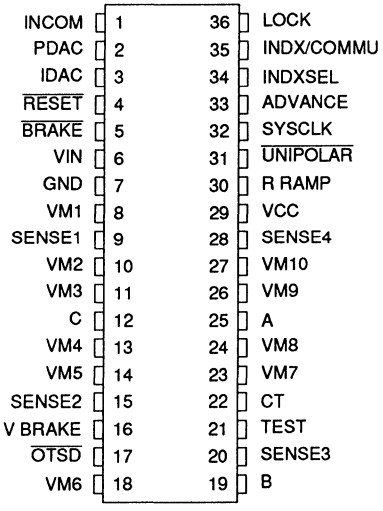
(continued)

FEATURES

- **Precise speed control**
- **1 amp peak drivers**
- **No blocking diode**
- **Adaptive commutation delay**
- **Commutation transient suppression**
- **Convenient Retract / Brake Control**

BLOCK DIAGRAM





36-Pin SOM
PIN DIAGRAM

CAUTION: Use handling procedures necessary for a static sensitive component.

TABLE 1: Output Driver States

STATE	COMMU	PULL DOWNS A	B	C	PULL UP UPA	UPB	UPC
0, (Reset State)	1	off	on, (off)	off	on	off	off
1	0	off	off	on	on	off	off
2	1	off	off	on	off	on	off
3	0	on	off	off	off	on	off
4	1	on	off	off	off	off	on
5	0	off	on	off	off	off	on

DESCRIPTION (Continued)

appropriate comparison is made. Because the back-emf comparison event occurs prior to the time when optimum commutation should occur, commutation is delayed by a predetermined time after the comparison. The commutation delay is provided by a circuit which measures the interval between comparison events and delays commutation by a time equal to 0.43 of the prior interval. (The delay is set at 0.43 not 0.50 in order to compensate for commutation delays and motor current build-up time.) The circuit is adaptive and will provide the optimum delay for a wide range of motor speeds. Since the commutation of motor coils typically causes transients, the circuit also provides a noise blanking function which prevents response to back-emf comparison events for a period of time equal to 5/7 of the interval (between events) after the comparison event. The commutation delay can be externally modified by ±15% with the INCOM pin. The commutation states are shown in Table 1.

The period counter is loaded with a count of 8333 initially, and the period measurement results in residual counts (ideally zero) in the period counter as it counts down during the index to index time. The residual count is fed to the proportional DAC (5 bits plus sign). When there is no period error the PDAC will output 1/2 full scale (2.25/2 volts) from PDAC, too short a period will output a lower voltage, and too long a period will output a higher voltage, each depending on the amount of period error. When the residual count is within ± 15 counts of zero, the motor status is indicated as "in lock." The lower eight bits of the period counter are fed to an accumulator which adds the present period residue to the previous accumulation thus accomplishing an integrating effect which forces the speed error to zero over time. The upper six bits of the accumulator are fed to the integral DAC whose output is IDAC. Gross period errors will cause PDAC and IDAC to saturate at the appropriate extremes to achieve the maximum corrective control voltage.

The outputs PDAC and IDAC are connected to VIN with an external resistor network. The resistor values are selected to set the required loop response based on motor and system requirements. Input pin VIN is the non-inverting input of a linear transconductance amplifier which uses the lower driver transistor that is presently active per the commutation state as the power driver element. An external resistor is used to sense the current in the drive transistor source (and hence the motor coil current). The voltage across the sense resistor is amplified by a gain stage (Av=8) and fed to the inverting input of the transconductance output stage.

When the speed error is more than 3% slow, 2.25 volts is selected as the control voltage in lieu of VIN. Maximum motor current is limited to a value such that Imotor ≤ 2.25V/ (4 • R_{SENSE}).

Four operating conditions are selected via $\overline{BRAKE}$ and $\overline{RESET}$. With $\overline{BRAKE}$ and $\overline{RESET}$ asserted (low), outputs A, B, and C are low impedance to ground, (without current limiting function) and analog circuits are de-biased. This is the "sleep" condition. It also provides dynamic braking to the motor. With $\overline{BRAKE}$ asserted, and $\overline{RESET}$ de-asserted, drivers are low impedance to ground (without current limit function) and the analog circuitry is biased. For $\overline{RESET}$ asserted, $\overline{BRAKE}$ de-asserted, the output drivers are in a high impedance state. This will allow the user to take energy from the back-emf of a spinning motor for retracting heads. Normal operation is given for $\overline{BRAKE}$ and $\overline{RESET}$ de-asserted.

DESCRIPTION (Continued)

TABLE 2: Rout Low to SENSE

$\overline{\text{BRAKE}}$	$\overline{\text{RESET}}$	CONDITION	ANALOG	COUNTERS	A, B, C
0	0	SLEEP/BRAKE	OFF	RESET	Rout low to SENSE
0	1	BRAKE	ON	ACTIVE	Rout low to SENSE
1	0	RETRACT	ON	ACTIVE	FLOAT
1	1	RUN	ON	ACTIVE	ACTIVE

Motor starting is accomplished with a companion microprocessor utilizing ADVANCE, $\overline{\text{RESET}}$ and COMMU. The microprocessor can assert $\overline{\text{RESET}}$ to initialize the commutation counter and then increment the counter with ADVANCE. ADVANCE at logic high excludes internal commutations. COMMU provides feedback to the microprocessor on motor activity.

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
$\overline{\text{RESET}}$	I	When asserted low, internal counters and registers are cleared. Refer to Table 2.
$\overline{\text{BRAKE}}$	I	$\overline{\text{BRAKE}}$ is used to provide a delay between the initiation of Fault-induced head retract and motor braking. A capacitor to ground and a resistor to $\overline{\text{RESET}}$ are selected such that 1.2•R•C is equal to the maximum time required for retract.
SYSCLK	I	Reference frequency for motor speed measurement. A 2.000 MHz SYSCLK will result in 3600 RPM motor speed for 8-pole motors. SYSCLK can be set to other frequencies to obtain a different rotational speed or operate with motors other than 8-pole configurations (use of an external index signal is only valid for 8-pole motors).
INDX/COMMU	I/O	When selected with INDXSEL set high, this pin is used to provide a once-per-revolution indication of rotational position and speed to the circuit. With INDXSEL low, COMMU (the LSB of the commutation counter) is presented as an output.
INDXSEL	I	See above.
LOCK	O	When the motor period is within ±15 counts of nominal, the motor is indicated as "in lock" with LOCK high.
ADVANCE	I	ADVANCE is used to increment the commutation counter. The rising edge of ADVANCE will increment the counter. ADVANCE held high will inhibit internal incrementing of the counter, ADVANCE held low permits the normal operation of commutation from back-emf events.
VM 1 - 10	-	Motor Power Supply.

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PIN DESCRIPTION (continued)

NAME	TYPE	DESCRIPTION
INCOM	I	Adaptive commutator delay test point.
PDAC	O	Proportional DAC output pin. The proportional channel output is the lowest 5 bits plus sign of the period measuring counter. The LSB signifies a 2 microsecond period variation for SYSCLK = 2.00 MHz.
IDAC	O	Integral DAC output pin. The integral channel output comes from the upper six bits of an eight bit accumulator. The accumulator adds the lower eight bits of the period measurement to the previous value obtained from prior period measurements and accumulations.
VIN	I	Control Voltage input pin. The internal driver transistors and internal predriver circuits form a transconductance amplifier which will set motor current in relation to VIN. In conjunction with the SENSE input and the gain of the sense amplifier, transconductance (Gm) will be: Gm = Im/VIN = 1/ (Rs • 8).
SENSE1 SENSE2 SENSE3 SENSE4	I	Current monitoring sense amplifier (high side) input pin. The lower driver transistor current (hence motor current) is sent through a current sensing resistor to monitor motor current. The circuit will control the voltage across this resistor (multiplied by the gain of 8 in the sense amplifier) to match either VIN (during normal operation) or internal 2.25V (during low-speed operation with Av = 4).
A, B, C	O	Motor Drive Outputs. These pins provide drive to the motor coils.
CT	I	Back-EMF input from motor coil center tap. Input connected to the center tap for sensing generated back-emf voltages. The circuit uses the back-emf voltages to determie rotor position and effect commutation.
VCC	-	5V power pin.
V BRAKE	O	External capacitor to store charge for driver circuitry. The stored charge is used by the lower drivers in fault conditions to achieve dynamic braking.
GND	-	Ground connection. GND is the low side input to the current SENSE amplifier and care should be taken to see that GND and the low side of the sense resistor are at the same potential.
$\overline{\text{OTSD}}$	O	Indicates over temperature condition.
R RAMP	I	External resistor. Sets DV/DT for lower driver turn-off. DV/DT is approximately 4E 10 • R RAMP.
$\overline{\text{UNIPOLAR}}$	I	Select line for Unipolar or Bipolar mode.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

(Exposure to conditions in excess of the conditions given below may result in permanent damage or affect device reliability.)

PARAMETER		RATING
Supply Voltage	VCC	-0.3 to 7V
	VM	-0.3 to 15V
Digital Inputs/Outputs	SYSCLK, ADVANCE INDXSEL, INDX/COMMU, LOCK	-0.3 to VCC +0.3V
Analog I/O	PDAC, IDAC, VIN	-0.3 to VCC +0.3V
Motor Interface Voltage	CT, A, B, C, $\overline{\text{BRAKE}}$, SENSE, $\overline{\text{RESET}}$	-0.3 to 20V
Motor Interface Current	A, B, C, VM, SENSE	-1.0 to +1.0A
Storage Temperature, Tstg		-65 to 150°C
Lead Temperature, Tlead		300°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	VCC		4.75		5.25	V
	VM		4.75		5.25	V
Supply Current	ICC		1.0		10.0	mA
	ICC, Sleep Mode		0.05		1.0	mA
	IVM		0		0.75	A
	IVM, Sleep Mode		0.1		1.5	mA
Ambient Temperature	Ta		0		70	°C
Capacitive Load Digital I/O	Cl		0		100	pF
Resistive Load PROP, INTEGRAL	Rla		5000			Ω
Capacitive Load PROP, INTEGRAL	Cla		0		40	pF

ELECTRICAL SPECIFICATIONS (Continued)

DIGITAL INPUTS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Fmax, SYSCLK				4.5	MHz
Twh, Twl, SYSCLK width high or low		40			ns
External Index, INDX/COMMU (as input) Pulse Width		200			ns
Input Leakage, INDX/COMMU				10	µA
Input Leakage, others				1	µA
Vil (EXTINDX, SYSCLK, ADVANCE, INDXSEL)				0.8	V
Vih (inputs above)		2.0			V
Vil ($\overline{\text{RESET}}$, $\overline{\text{BRAKE}}$)	VBRAKE ≥ 4.5V			0.8	V
Vih ($\overline{\text{RESET}}$, $\overline{\text{BRAKE}}$)	VBRAKE ≥ 4.5V	2.0			V

PROPORTIONAL (PDAC), INTEGRAL (IDAC) OUTPUTS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage	Iout ≤ 0.1 mA VCC = 5.0 V	0		2.25V ±5%	V
DAC Step Size	VCC = 5.0V	0.32		0.39	V
Output Impedance	0.5V ≤V out <2.0V Iout = 0.10 mA			200	Ω
Kp, Porportional Gain		0.70		0.85	V/rad/s
Ki, Integral Gain		10.48		12.75	V/rad

DIGITAL OUTPUTS, LOCK, INDX/COMMU

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Voh	Iout = -100 µA	2.4			V
Vol	Iout = 2.0 mA			0.4	V
Tdts, Time delay to tri-state output	INDXSEL high to high impedance on INDX/COMMU	10		100	ns
Tdoe, Time delay to enable as output pin	INDXSEL low to drive state	10		100	ns

ELECTRICAL SPECIFICATIONS (Continued)

VIN

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage		0		2.25	V
Input Current	0 ≤ Vin < 2.5V	-1		+1	µA

OUTPUTS A, B, C

Routup	Output in high state VM = 4.75V	0.05		1.0	Ω
Routlow	Output driving low, VM = 4.75V	0.05		1.0	Ω

SENSE

Vin, SENSE	Normal operation	0.0		0.4	V
	Low speed operation	0.0		0.8	V
Iin, SENSE	0.0 ≤ Vin < 1.0V	-10		+10	µA
Cin				20	pF
Transconductance gain from VIN to motor current (steady-state) will be given by: G = Imotor/VIN = 1/Rsense • 8, for rotational speeds greater than 3490 RPM.					

CT

Rin	-0.3V ≤Vin < 15V	30K			Ω
Cin				10	pF

V BRAKE

Ibst (run)	VCC = 4.75V			100	µA
Ibst (float)	VCC ≤ 0.5V			10	µA
Ibst (brake)	VCC ≤ 0.5V			10	µA

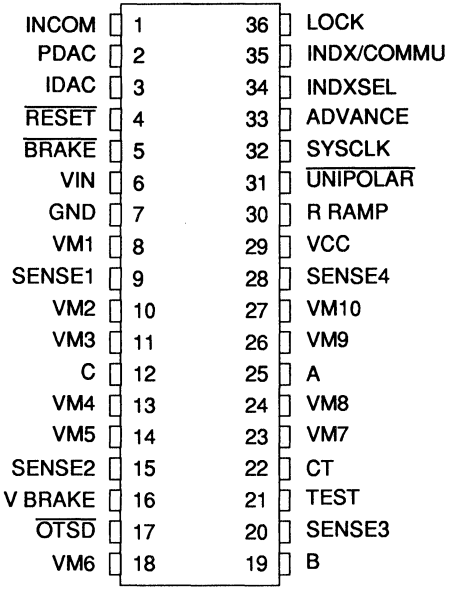
OPERATING REQUIREMENTS

LOCK Indication Range	SYSCLK = 2.000 MHz, 8-pole	3593.5		3606.5	RPM
Speed Resolution		-.012		+0.012	%

SSI 32M7010
Hall-Sensorless
Motor Speed Control

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



36-Pin SOM

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32M7010, Hall-Sensorless Motor Speed Control		
36-Pin SOM	32M7010-CM	32M7010

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 731-7110, FAX (714) 573-6914

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SSI 32M7011
Hall-Sensorless Motor Speed Commutator
Advance Information

December 1991

DESCRIPTION

The (Spindle) Motor Commutator in conjunction with a companion microcontroller, provides starting, accelerating, precise rotational speed regulation functions, coasting (for retract), and dynamic brake. The circuit can be used with 4-, 8-, or 12-pole, 3 phase, brushless DC motors without the need for Hall sensors.

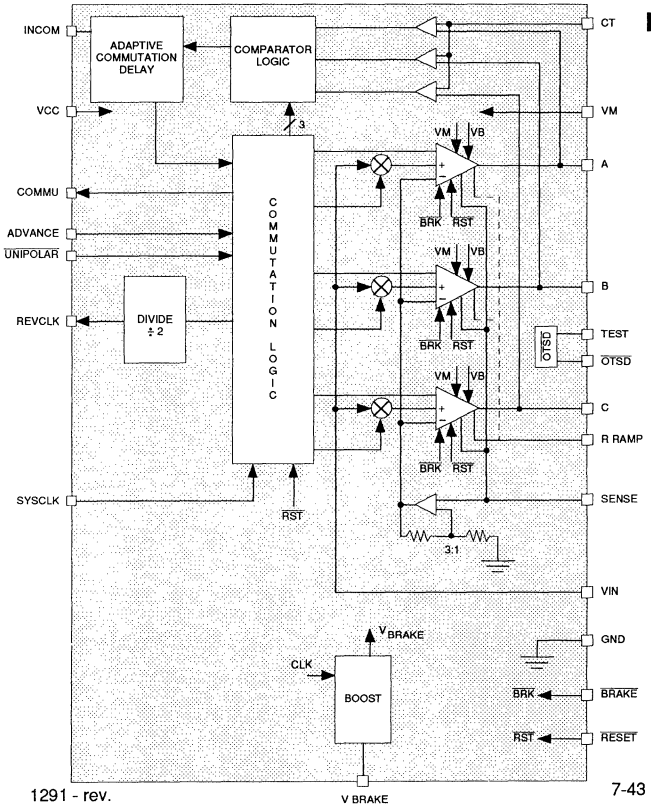
The commutator determines motor armature position by monitoring the coil voltage of the winding that is not presently being driven by the drivers. The back-emf at the coil in conjunction with the state of the output drivers, indicates armature position. The back emf is compared to a reference (CT) and initiates commutation when the appropriate comparison is made.

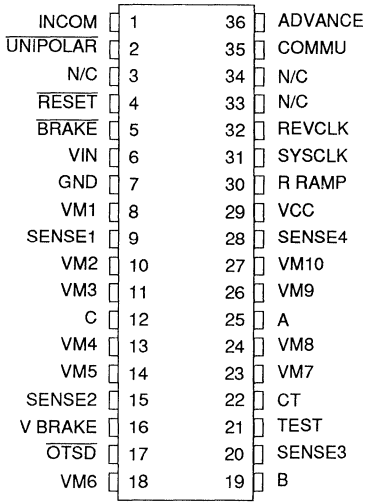
(continued)

FEATURES

- **Optimum commutation without external components**
- **Retract coast and brake modes supported**
- **1Ω FET drivers**
- **Commutation without Hall sensors**
- **Reduced DV/DT on commutation - no snubber networks required**
- **No blocking diode required**
- **Immune to brown outs and load transients**

BLOCK DIAGRAM





36-Pin SOM

PIN DIAGRAM

CAUTION: Use handling procedures necessary for a static sensitive component.

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DESCRIPTION (Continued)

Because the back-emf comparison event occurs prior to the time when optimum commutation should occur, commutation is delayed by a predetermined time after the comparison. The commutation delay is provided by a circuit which measures the interval between prior comparison events and delays commutation by a time equal to 0.43 of the prior interval. (The delay is set at 0.43 not 0.50 in order to compensate for commutation delays and motor current build-up time.) The circuit is adaptive and will provide the optimum delay for a wide range of motor speeds. Since the commutation of motor current typically causes transients, the circuit also provides a noise blanking function which prevents response to back-emf comparison events for a period of time equal to 0.71 of the interval (between events) after the comparison event. The commutation delay can be externally modified by ±15% with the INCOM pin. The commutation states are shown in Table 1.

Input pin VIN is the non-inverting input of a linear transconductance amplifier which uses the lower driver transistor that is presently active per the commutation state as the power driver element. An external resistor is used to sense the current in the drive transistor source (and hence the motor coil current). The voltage across the sense resistor is amplified by a gain stage (Av=4) and fed to the inverting input of the transconductance output stage. Input voltage VIN must be generated from external means that use either REVCLK or other external rotational index indicators to measure rotational speed.

Four operating conditions are selected via $\overline{\text{BRAKE}}$ and $\overline{\text{RESET}}$. With $\overline{\text{BRAKE}}$ and $\overline{\text{RESET}}$ asserted (low), outputs A, B, and C are low impedance to ground, (without current limiting function) and analog circuits are de-biased. This is the "sleep" condition. It also provides dynamic braking to the motor. With $\overline{\text{BRAKE}}$ asserted, and $\overline{\text{RESET}}$ de-asserted, drivers are low impedance to ground (without current limit function) and the analog circuitry is biased. For $\overline{\text{RESET}}$ asserted, $\overline{\text{BRAKE}}$ de-asserted, the output drivers are in a high impedance state. This will allow the user to take energy from the back-emf of a spinning motor for retracting heads. Normal operation is given for $\overline{\text{BRAKE}}$ and $\overline{\text{RESET}}$ de-asserted.

Note that circuit utilizes NMOS driver transistors and does not require a Schottky blocking diode to prevent current flow from the spinning motor to the power supply. During RETRACT conditions, the motor is isolated from VM.

TABLE 1: Output Driver States

STATE	COMMU	PULL DOWNS A	B	C	PULL UP UPA	UPB	UPC
0, (Reset State)	1	off	on, (off)	off	on	off	off
1	0	off	off	on	on	off	off
2	1	off	off	on	off	on	off
3	0	on	off	off	off	on	off
4	1	on	off	off	off	off	on
5	0	off	on	off	off	off	on

TABLE 2: Rout Low to SENSE

$\overline{\text{BRAKE}}$	$\overline{\text{RESET}}$	CONDITION	ANALOG	COUNTERS	A, B, C
0	0	SLEEP/BRAKE	OFF	RESET	Rout low to SENSE
0	1	BRAKE	ON	ACTIVE	Rout low to SENSE
1	0	RETRACT	ON	ACTIVE	FLOAT
1	1	RUN	ON	ACTIVE	ACTIVE

Motor starting is accomplished with a companion microprocessor utilizing ADVANCE, $\overline{\text{RESET}}$ and COMMU. The microprocessor can assert $\overline{\text{RESET}}$ to initialize the commutation counter and then increment the counter with ADVANCE. ADVANCE at logic high excludes internal commutations. COMMU provides feedback to the microprocessor on motor activity.

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
$\overline{\text{RESET}}$	I	Refer to Table 2.
$\overline{\text{BRAKE}}$	I	$\overline{\text{BRAKE}}$ is used to provide a delay between the initiation of Fault-induced head retract and motor braking. A capacitor to ground and a resistor to $\overline{\text{RESET}}$ are selected such that 1.2•R•C is equal to the maximum time required for retract.
SYSCLK	I	2.0 MHz clock input signal.
COMMU	O	COMMU is the LSB of the commutation counter.
REVCLK	O	Indicates 1 revolution of 4-pole motor, 1/2 revolution of 8-pole, and 1/3 revolution of 12-pole motor.
ADVANCE	I	ADVANCE is used to increment the commutation counter. The rising edge of ADVANCE will increment the counter. ADVANCE held high will inhibit internal incrementing of the counter, ADVANCE held low permits the normal commutation due to back-emf events.
VM 1 - 10	Power	Motor Power Supply.
INCOM	I	Adaptive commutator delay trim. Generally a no-connect.
VIN	I	Control Voltage input pin. The internal driver transistors and internal predriver circuits form a transconductance amplifier which will set motor current in relation to VIN. In conjunction with the SENSE input and the gain of the sense amplifier, transconductance (Gm) will be Gm = Im/VIN = 1/ (Rs•4). The voltage at VIN must be controlled by external circuitry to accomplish speed control.
SENSE1 SENSE2 SENSE3 SENSE4	Power	Current monitoring sense amplifier (high side) input pin. The lower driver transistor current (hence motor current) is sent through a current sensing resistor to monitor motor current. The circuit will control the voltage across this resistor (multiplied by the gain of 4 in the sense amplifier) to match VIN.
A, B, C	O	Motor Drive Outputs. These pins provide drive to the motor coils.
CT	I	Back-EMF input from motor coil center tap. Input connected to the center tap for sensing generated back-emf voltages. The circuit uses the back-emf voltages to determine rotor position and effect commutation. 3 equal value resistors from A, B, and C attached to CT will suffice to synthesize a center-tap potential on three terminal motors. 4 terminal motors should use this terminal.
VCC	Power	5-volt power pin.

PIN DESCRIPTION (continued)

NAME	TYPE	DESCRIPTION
V BRAKE	O	External capacitor to store charge for driver circuitry. The stored charge is used by the lower drivers in fault conditions to achieve dynamic braking.
GND	-	Ground connection. GND is the low side input to the current SENSE amplifier and care should be taken to see that GND and the low side of the sense resistor are at the same potential.
$\overline{\text{OTSD}}$	O	Indicates over temperature condition and forces drivers off. Operation after cool down is restored by asserting ADVANCE.
R RAMP	I	External resistor. Sets DV/DT for lower driver turn-off. DV/DT is approximately $25 \cdot \frac{10^9}{\text{RRAMP}}$ (Volts / Second)
$\overline{\text{UNIPOLAR}}$	I	Select line for Unipolar or Bipolar mode. $\overline{\text{UNIPOLAR}}$ = low will de-activate upper drivers. Note: for BRAKE and SLEEP modes user must guarantee that external Unipolar driver transistor(s) do not conflict with lower driver transistors on circuit.
TEST	I/O	No connect, leave open circuited.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

(Exposure to conditions in excess of the conditions given below may result in permanent damage or affect device reliability.)

PARAMETER	SYMBOL	MIN	MAX	UNIT
Supply Voltage	VCC	-0.3	7	V
	VM	-0.3	7	V
Digital Inputs/Outputs	SYSCLK, ADVANCE COMMU, REVCLK	-0.3	VCC +0.3	V
Analog I/O	VIN, RRAMP, INCOM, TEST	-0.3	VCC +0.3	V
Motor Interface Voltage	CT, A, B, C, $\overline{\text{BRAKE}}$, SENSE, $\overline{\text{RESET}}$	-0.3	20	V
Motor Interface Current	A, B, C, VM, SENSE	-1.0	+1.0	A
Storage Temperature, Tstg		-65	150	°C
Lead Temperature, Tlead		-	300	°C

ELECTRICAL SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	VCC		4.75		5.25	V
	VM		4.75		5.25	V
Supply Current	ICC		1.0		10.0	mA
	ICC, Sleep Mode		0.05		1.0	mA
	IVM		0		0.75	A
	IVM, Sleep Mode		0		1.5	mA
Ambient Temperature	Ta		0		70	°C
Capacitive Load Digital I/O	Cl		0		100	pF

DIGITAL INPUTS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Fmax, SYSCLK		1.0	2.0	4.5	MHz
Twh, Twl, SYSCLK width high or low		40			ns
Advance Pulse Width		200			ns
Input Leakage, others				1	µA
Vil (SYSCLK, ADVANCE)				0.8	V
Vih (inputs above)		2.0			V
Vil ($\overline{\text{RESET}}$, $\overline{\text{BRAKE}}$)	VBRAKE ≥ 4.5V			0.8	V
Vih ($\overline{\text{RESET}}$, $\overline{\text{BRAKE}}$)	VBRAKE ≥ 4.5V	2.0			V

DIGITAL OUTPUTS, COMMU, REVCLK

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Voh	Iout = -100 µA	2.4			V
Vol	Iout = 2.0 mA			0.4	V

VIN

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage		0		2.25	V
Input Current	0 ≤ Vin < 2.5V	-1		+1	µA

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ELECTRICAL SPECIFICATIONS (Continued)

OUTPUTS A, B, C

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Routup	Output in high state VM = 4.75V	0.05		1.0	Ω
Routlow	Output driving low, VM = 4.75V	0.05		1.0	Ω

SENSE

Vin, SENSE	Normal operation	0.0		0.5	V
Iin, SENSE	0.0 ≤ Vin < 1.0V	-10		+10	µA
Cin				20	pF
Transconductance gain from VIN to motor current (steady-state) will be given by: G = Imotor/VIN = 1/Rsense • 4.					

CT

Rin	-0.3V ≤Vin < 15V	30K			Ω
Cin				10	pF

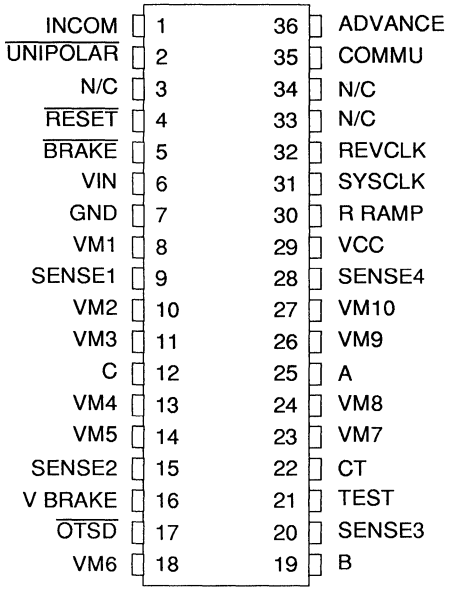
V BRAKE

Ibst (run)	VCC = 4.75V			100	µA
Ibst (float)	VCC ≤ 0.5V		25	100	µA
Ibst (brake)	VCC ≤ 0.5V		3	10	µA

PACKAGE PIN DESIGNATIONS

(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



36-Pin SOM

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Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 731-7110, FAX (714) 573-6914

Notes:

Section 8

HDD CONTROLLER/ INTERFACE

silicon systems®
A TDK Group Company

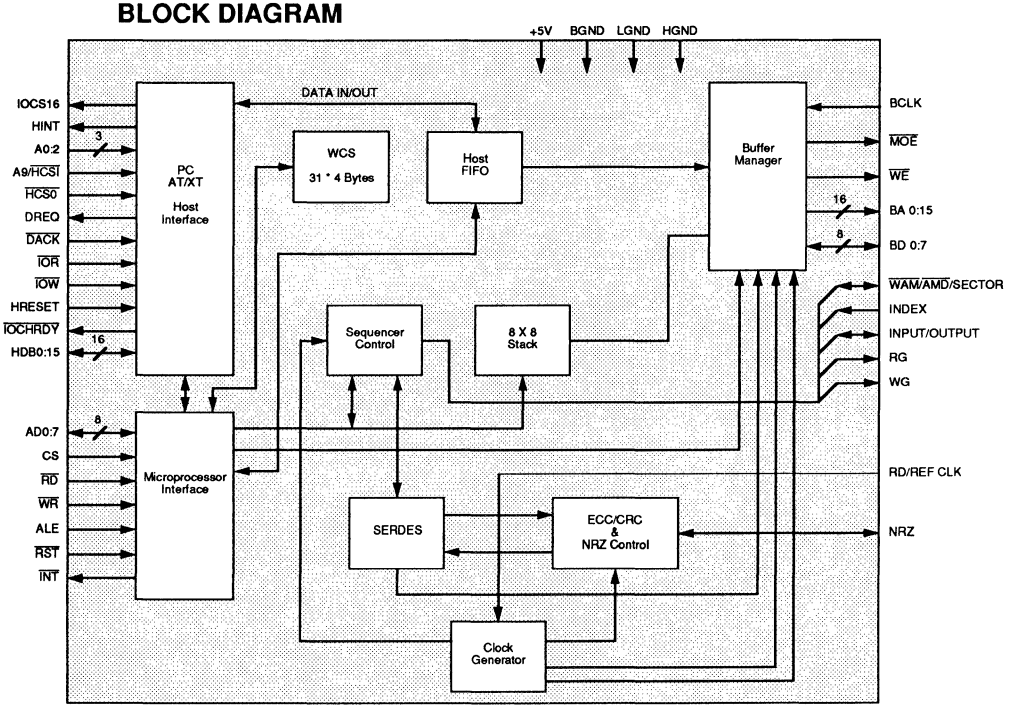
SSI 32C260
PC AT/XT 15 Mbit/s Combo Controller

October 1991

FEATURES

- PC AT/XT Bus Interface
  - Single Chip PC AT/XT Controller
  - Supports ST506/412, ST412HP, ESDI, and SMD disk interfaces
  - Direct bus interface logic with on-chip 24 mA drivers
  - Logic for daisy chaining 2 embedded controller drives on a PC AT
  - Supports 15 Mbit/s concurrent disk transfer on a 12 MHz PC AT without wait states
- Buffer Manager
  - Supports Buffer Memory throughput to 8 Mbytes/s
  - Direct Buffer Memory addressing up to 64 kB static RAM
  - Dual port circular buffer control
- Storage Controller
  - NRZ Data rate up to 15 Mbit/s
  - Selectable 16-bit CRC or 56-bit ECC polynomial with fast hardware correction circuitry
  - Supports sector level defect management
  - Supports 1:1 interleaved operation
- Microprocessor Interface
  - Supports both Intel 8051, and Motorola 68HC11 family of microprocessors
  - Interrupt or polled microprocessor interface
- Others
  - Low power CMOS technology
  - Plug and Play compatible with Cirrus CL-SH 260 chip
  - Available in 84-pin PLCC or 100-pin QFP

BLOCK DIAGRAM



8

1091 - rev.

SSI 32C260
PC AT/XT 15 Mbit/s
Combo Controller

DESCRIPTION

The SSI 32C260 is a CMOS VLSI device which integrates the major portion of the hardware needed to build a PC AT/XT driven hard disk controller. The 32C260 is capable of supporting interleaved data transfer rate up to 15 Mbit/s. This chip represent a major reduction in part count when used with the SSI 32P4620, Pulse Detector and Data Separator combo chip, and the SSI 32R4610, Read/Write device and the SSI 32H4631, Servo and Motor Speed Controller device, implementing a powerful and cost efficient 4-chip set hard disk drive solution. It also has the flexibility to be used as a stand-alone combo controller.

The SSI 32C260 includes all the circuitry for a direct connection to an AT/XT bus interface, a dual port Buffer Manager, a storage controller and an extensive hardware support, including 24 mA drivers, for the PC AT/XT and other compatible interfaces.

The SSI 32C260 performs all the controller functions for the peripheral device, such as serialization/deserialization, ECC generation and checking on the data stream, and CRC generation and checking on the header of the data stream.

FUNCTIONAL DESCRIPTION

The major functional elements and data paths of the SSI 32C260 are shown in the block diagram.

The four major functional blocks are:

Buffer Memory Interface,

Microcontroller Interface,

Disk Formatter,and

Host Interface.

The SSI 32C260 performs the functions to interface a serial data storage device such as a Winchester Disk Drive, to a parallel bus interface for data processing on a byte wide basis. The functions necessary to accurately make this conversion are serialization/deserialization, error detection and correction, and data path control. The SSI 32C260 also has a general purpose interface line to further facilitate control of the data storage device or parallel interface. An eight byte stack allows data to be saved and reviewed by the microprocessor for error handling purposes. The internal sequencer performs most of the operations in conjunction with the control and status registers. The sequencer program is contained in an internal sequencer RAM, which is easily (re)programmed providing almost infinite flexibility in drive format and control features. A microprocessor effects both initialization and control of the SSI 32C260 by writing to and reading from the internal registers, sequencer RAM, stack and general purpose I/O circuitry. The microprocessor interface block of the SSI 32C260 provides the communication and control for the SSI 32C260 to the microprocessor. **For a complete description of the programmable registers, refer to the SSI 32C260 Design Guide.**

BUFFER MEMORY INTERFACE

The buffer memory interface, referred to as the Buffer Manager includes a bi-directional data bus that exchanges data bytes between an external buffer memory and the serializer/deserializer or the host interface. The circuitry allows the use of static RAM as a dual port circular FIFO, and supervises data transfers to and from the RAM. The device contains logic that resolves disk and host requests. The arbitration is achieved by giving priority to the disk and utilizing internal data FIFO's for temporary host and disk data storage.

The Buffer Manager is capable of handling buffer sizes from 256 bytes to 64K bytes. The circuit provides up to 16 direct address signals, along with Memory Output Enable ($\overline{MOE}$) and Write Enable ($\overline{WE}$) signals. The buffer RAM address is generated from one of two 16-bit counters, one of which being the write address pointer (5CH & 5DH) and the other the read pointer (5AH & 5BH). The address generation as well as the memory control signals are synchronous to the Buffer Clock (BCLK), allowing the user many choices of buffer RAM speeds, with different combinations of the disk and host transfer rates.

The Buffer Memory Interface is a dual port buffer controller that allows low speed static RAM's to be configured as a dual port circular FIFO buffer. It generates all the buffer memory addressing required and manages two ports: Port A, a synchronous peripheral device interface and Port B, an asynchronous host interface. The Buffer Manager has arbitration logic to support the AT or XT host transfers under DMA control or Programmed I/O control.

On-chip counters generate the addresses (BA0-BA15) needed to access up to 64K of external static RAM. Along with the addresses, the Buffer Manager block outputs a Memory Output Enable ($\overline{MOE}$) and a Write Enable ($\overline{WE}$) signal for a static RAM buffer.

The address generator contains two 16 bit pointers, the read address pointer (RAP) and the write address pointer (WAP), which indicate where in the external buffer RAM data is to be read or written. During data transfers, these pointers are automatically incremented as the RAM is accessed. The pointers wrap around to 0 when the programmed buffer size is exceeded. To prevent host overruns of the buffer (caused by one of the pointers overtaking the other), the address generator includes a 16-bit stop pointer (5EH & 5FH). The microprocessor loads SP with the last address in buffer memory to be accessed during a host DMA transfer. When the port B address (RAP during an upload to the host or WAP during a download to the peripheral) reaches the value in SP, the DMA transfer is automatically suspended.

The period of the Buffer Memory access cycle is determined by programming bits 6 and 7 of CLOCK CONTROL, register 7FH, and is based on the BCLK input. The period of the Buffer Memory access cycle determines the access time requirement for the buffer RAMs. The C260 samples the data from the RAM at the falling edge of the BCLK signal. Buffer Memory throughput and the RAM speeds can be determined from the following equations:

Buffer Memory Throughput =

1 / Period of Memory Access Cycle

For Buffer Memory Read:

Max. Read Access Time = $T_1 - Av_{max} - Dis_{min}$

Min. Output Enable = $(T_1/2) - Mv_{max} - Dis_{min}$

For Buffer Memory Write:

Address set up to $\overline{WE}\uparrow = T_1 - Av_{max} + Wh_{max}$

Data set up to $\overline{WE}\uparrow$ = Min. Output Enable
$= (T_1/2) - Mv_{max} - Dis_{min}$

Note: For an explanation of Av_{max}, Dis_{min}, Mv_{max}, Wh_{max}, Dov_{max} parameters, refer to Buffer Memory Read/Write Timing Parameters.

MICROPROCESSOR INTERFACE

The microprocessor interface decodes microprocessor read and write requests and provides access to the appropriate register or internal memory location. Since both data and address information are carried on the multiplexed bus lines AD0-AD7, address information is latched from the bus on the falling edge of the microprocessor signal, Address Latch Enable (ALE). When CS is asserted along with either $\overline{RD}$ or $\overline{WR}$, the register whose address was previously latched is selected. The addresses and names of all the accessible registers are shown in the Register Address Map. The microprocessor should not read or write the sequencer RAM while the sequencer is running, since there is no circuitry to resolve conflicting accesses and incorrect sequencer operation will result.

The status and control registers make status information available to the microprocessor and allow the device to be configured for a wide variety of peripheral applications. The microprocessor can monitor the status of transfers in progress and control the ECC register operation, the ECC polynomial, the clock generation hardware, the sequencer program execution, buffer size, read and write pointers, and stop pointers. The microprocessor also has access to the sequencer's microprogram RAM so that it loads the microcode for all controller operations.

DISK FORMATTER

The serializer/deserializer circuit interfaces the parallel buffer memory bus to serial NRZ data stream of the peripheral device. Byte synchronization is maintained with a bit ring, which is an 8-bit recirculating shift register clocked by the peripheral bit clock. During a sector write, the bit ring is initialized explicitly with a sequencer instruction. The bit ring continues to operate until the end of the field (ECC written or read). During write operations, the sequencer may cause address marks and sync patterns to be loaded into the serializer instead of data bytes. These special patterns are contained in a sequencer instruction and are transferred to the serializer over an internal byte wide data path. During read operations, bytes of overhead information may be routed to the stack or sequencer for comparison against target values. This process is controlled by the control field (SEQCONF) in each sequencer instruction.

The eight byte recirculating stack may be used to capture read data for later examination by the microprocessor. Data is pushed onto the stack under se-

quencer control. The control bit STACKEN in the sequencer instruction field SEQCONF in the sequencer instruction field SEQCONF directly controls the stack. If more than 8 bytes are written to the stack, only the last 8 will be saved. When a data byte is read from the top of the stack by the microprocessor via the STACK register, the data is recirculated to the bottom of the stack, allowing the stack contents to be examined more than once without the use of temporary storage in the microprocessor or buffer.

Serial peripheral data is passed through a variable length shift register with programmable exclusive OR feedback that performs ECC or CRC generation and checking. The feedback taps for the desired polynomials are fixed as follows and the user may select between the 16-bit CRC, 32-bit ECC, or the 56-bit ECC as desired. This selection is accomplished by programming the WCS COUNT FIELD and the ECC CONTROL register (Register 71H, bit 6).

In the forward direction, the options available include:

CRC polynomial which is the CCITT CRC code:

$x^{16} + x^{12} + x^5 + 1$

32-bit ECC polynomial:

$x^{32} + x^{28} + x^{26} + x^{19} + x^{17} + x^{10} + x^6 + x^2 + 1$

56-bit ECC polynomial:

$x^{56} + x^{52} + x^{50} + x^{43} + x^{41} + x^{34} + x^{30} + x^{26} + x^{24} + x^8 + 1$

The reverse polynomial options include:

32-bit ECC polynomial:

$x^{32} + x^{30} + x^{26} + x^{22} + x^{15} + x^{13} + x^6 + x^4 + 1$

56-bit ECC polynomial:

$x^{56} + x^{48} + x^{32} + x^{30} + x^{26} + x^{22} + x^{15} + x^{13} + x^6 + x^4 + 1$

The 56-bit polynomial can detect single burst errors up to 56 bits in length, and double-burst errors, where the combination of bursts is less than or equal to 41 bits. This polynomial can also correct single-burst errors up to 23 bits in length. The 32-bit ECC polynomial is the standard polynomial found in IBM PC AT controllers.

The forward and reverse polynomial is selected by programming ECC CONTROL (Register 71H, Bit 7). Whichever polynomial is selected, the ECC/CRC shift registers always start preset to all 1s.

The sequencer controls the time critical operations of the SSI 32C260. It executes programs stored in the 28 word by 32-bit sequencer RAM, and can be programmed to support hard and soft sectored read, write, search, and verify operations for a wide variety of Winchester Disk Drives and other peripherals. The sequencer RAM is loaded by writing to the sequencer instruction registers as outlined in the Sequencer Instructions of this data sheet. Each instruction is comprised of four bytes. Each of the four bytes represents a function of the sequencer operation. They are address field, control field, data type field, and data field. The organization of these fields is shown in the Register Bit Map in the SSI 32C260 Design Guide. The Sequencer Registers provide control from and status to the microprocessor and sequencer. They contain branch, next, and start addresses, and sequencer status information. The SEQUENCER STATUS register provides information on the sequencer state such as whether an ECC error occurred, a compare equal or low occurred, if the branch condition or address mark is active, or whether the sequencer is halted.

HOST INTERFACE

The internal receivers and drivers on the host interface block allow the device to connect directly to the PC Host bus. The drivers are capable of sinking up to 24 mA and drive a load up to 300 pF.

The wait state generator extends the Host I/O cycle and inserts wait states by asserting $\overline{\text{IOCHRDY}}$. This generator is only active during Programmed I/O transfers and works in two ways: 1) inserting programmed number of Buffer Memory Cycles for every host access of the device, and 2) asserting $\overline{\text{IOCHRDY}}$ only when the device is not ready for the transfer. Register 58H, Bits 0 and 1, program the wait states cycles and Bit 2 asserts $\overline{\text{IOCHRDY}}$ whenever the device is not ready for transfer.

The auto decoding circuitry allows the device to speed up the performance of the controller by decoding Write commands that require data transfer from the Host to the Buffer Memory. These commands include Format (5XH), Write Buffer (E8H), Write or Write long (3XH). The device automatically starts accepting data without the local microcontroller control when any of these commands are loaded into the COMMAND REGISTER by the host. If interrupts are enabled, the device generates an interrupt to the local microcontroller. The

PC STOP POINTER (Registers 5EH and 5FH) is initialized to 01FFH. If DISABLE STOP POINTER COMPARE (Register 52H, Bit 6) is set, the local microcontroller must initialize the PC STOP POINTER to enable comparison of the WRITE ADDRESS POINTER (Registers 5CH and 5DH) with the HOST STOP POINTER. The Formatter disconnects from the Buffer Manager on receiving one of these commands. It also disables write access by the local microcontroller to the DMA CONTROL REGISTER (53H) and WRITE ADDRESS POINTERS (5CH and 5DH). In addition, read/write access to the BUFFER MEMORY ACCESS REGISTER. Access to these registers is enabled when the local microcontroller writes to AUTOCOMMAND "LOCK" RELEASE register (73H).

The ECC bytes are transferred to and from the host by enabling by Bit 1 of the command byte by the host, indicating Read and Write Long command. If a Read or Write Long command is received, Buffer Memory transfers to/from the Host will exceed the PC STOP POINTER (Registers 5EH and 5FH) by the count of ECC bytes. Initially the PC STOP POINTER is set at the end of the Data Field. When the active READ ADDRESS POINTER (Registers 5AH and 5BH), or WRITE ADDRESS POINTER (Registers 5CH and 5DH), matches the PC STOP POINTER (Registers 5EH and 5FH), the internal FIFO will be emptied of the word width data, the PC STOP POINTER gets incremented by the count of ECC bytes. The ECC bytes will then be transferred in Byte Mode.

PIN DESCRIPTION

GENERAL

NAME	TYPE	DESCRIPTION
VCC		+5V POWER SUPPLY
BGND		BUFFER BUS GROUND
LGND		LOGIC GROUND
HGND		HOST GROUND

HOST INTERFACE

A0:2	I	HOST ADDRESS LINES. These pins are used to address the internal registers by the AT bus.
A9/$\overline{HCS1}$	I	HOST ADDRESS LINE 9/ HOST CHIP SELECT 1. A9, this pin is used in conjunction with the A0:2 address lines to address the internal task file registers. HCS1 is an active low pin, used to qualify Host access.
$\overline{HCS0}$	I	HOST CHIP SELECT 0. Active low, this pin selects access to the control, status and data registers.
$\overline{IOCS16}$	O	I/O SELECT 16. An open drain output that indicates that a 16-bit sector buffer transfer is active.
HINT	O	HOST INTERRUPT. Asserted to indicate to the Host that the controller needs attention.
$\overline{IOCHRDY}$	O	I/O CHANNEL READY. Active low, this signal is asserted whenever that internal host FIFO is not ready to transfer a word.
DREQ	O	DMA REQUEST. This pin is programmed to function as the PC/AT bus signal in the PC/AT DMA mode.
$\overline{DACK}$	I	DMA ACKNOWLEDGE. Active low, in the PC/AT DMA mode this pin is programmed to be the PC/AT channel signal - DACK.
$\overline{IOR}$	I	INPUT READ SELECT. Active low, this pin is asserted by the Host during a Host read operation.
$\overline{IOW}$	I	INPUT WRITE SELECT. Active low, asserted by the HOST during a HOST write operation.

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NAME	TYPE	DESCRIPTION
HOST INTERFACE (Continued)		
HRESET	I	HOST RESET. This signal resets all commands in progress when active, and initializes the control/status registers.
HDB 15:0	I/O	HOST DATA BUS. Active high bi-directional pins. These bits are used for data transfers between the Host and the Buffer Manager.
DISK INTERFACE		
INDEX	I	INDEX. Input for index pulse received from the drive
INPUT/ OUTPUT	I/O	INPUT/OUTPUT. A general purpose control and status pin. It can be either an input or an output. At power-on, this pin is an input.
$\overline{\text{WAM}}$/ $\overline{\text{AMD}}$/ SECTOR	I/O	WRITE ADDRESS MARK/ADDRESS MARK DETECT/SECTOR. This pin becomes an active low address mark detect if read gate is on, or write address mark if write gate is on. It operates in hard or soft sector modes. The default is soft sector. In hard sector mode this is the input for the sector pulse.
RG	O	READ GATE. During NRZ data read. this pin is asserted.
WG	O	WRITE GATE. During NRZ data write, this pin is asserted.
RD/REF/ CLK	I	READ/REFERENCE CLOCK. This pin is used in conjunction with the NRZ pin to clock data in and out of the SSI 32C260 device.
NRZ	I/O	NRZ. This pin is used in conjunction with the RG and WG when reading and writing from and to the disk.
MICROPROCESSOR INTERFACE		
$\overline{\text{RST}}$	I	RESET. Active low input, when pulled low, the internal registers of the SSI 32C260 are held at reset.
ALE	I	ADDRESS LATCH ENABLE. This control signal latches the address on the address/data lines.
CS	I	CHIP SELECT. Active high signal, when asserted, the internal registers of the SSI 32C260 can be accessed.
$\overline{\text{WR}}$	I	WRITE. Active low input, when active the data is written to the internal registers.
$\overline{\text{RD}}$	I	READ. Active low input, when active that data is read from the internal registers.
$\overline{\text{INT}}$	O	INTERRUPT. Push-pull or open-drain signal, when active, indicates local microcontroller interrupt.
AD7:0	I/O	ADDRESS/DATA BUS. 8-bit bus for both microprocessor register address and data.
BUFFER MANAGER INTERFACE		
BA0:15	O	BUFFER MANAGER ADDRESS LINES. Active high, for direct connection to a static RAM.
BD0:7	I/O	BUFFER MANAGER DATA BUS. 7 through 0. Active high, buffer data bus that connects directly to the buffer RAM.
$\overline{\text{MOE}}$	O	MEMORY OUTPUT ENABLE. Active low select for the buffer RAM.
$\overline{\text{WE}}$	O	WRITE ENABLE. Active low, write enable for the buffer RAM.
BCLK	I	SYSTEM CLOCK. This signal is used to synchronize the buffer RAM access, including the generation of memory address bits, write enable WE, and memory output enable MOE.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Ambient Temperature Under Bias	0 to 70	°C
Storage Temperature	-65 to 150	°C
Voltage On Any Pin With Respect To Ground	GND-0.5 to VCC+0.5	V
Power Dissipation	0.750	Watt
Power Supply Voltage	7	V
Max Current Injection	50	mA
θja = Thermal Resistance (QFP)	60	°C/W
θja = Thermal Resistance (PLCC)	32	°C/W

NOTE: Stress above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
VCC	Power Supply Voltage	Operating	4.5		5.5	V
VIL	Input Low Voltage		-0.5		0.8	V
VIH	Input High Voltage		2.0		VCC+0.5	V
VOL(1)*	Output Low Voltage	IOL = 2 mA			0.4	V
VOL(2)	Output Low Voltage	IOL = 24 mA			0.5	V
VOH	Output High Voltage	IOH = -400µA			2.4	V
ICC	Supply Current				50	mA
ICC_S	Supply Current Standby	All Inputs at GND or VCC			250	µA
IL	Input Leakage Current	0<VIN<VCC	-10		10	µA
CIN	Input Capacitance				10	pF
COUT	Output Capacitance				10	pF

NOTE: (1) All output pins except for host interface signals
(2) Host interface outputs
(*) IOL = 4 mA for RG and WG

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AC CHARACTERISTICS

The following timings assume that all non-Host Bus output pins will drive one Schottky TTL load in parallel with 50 pF, all Host Bus output pins will drive a 300 pF load, and all inputs are at TTL levels. The MIN and MAX timings conform to the operating ranges of a power supply voltage of 5V±10%, and an ambient temperature of 0°C to 70°C.

Host DMA 8/16-Bit Interface Timing Parameters (Figure 1)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
DREQL	DREQ low from $\overline{DACK}$ low				80	ns
RDTA	$\overline{IOR}$ low to HD [0:15] valid				60	ns
RDHLD	$\overline{IOR}$ high to HD [0:15] tri-state		0		20	ns
WDS	HD [0:15] setup to $\overline{IOW}$ high		40			ns
WDHLD	HD [0:15] hold from $\overline{IOW}$ high		10			ns
RWPULSE	$\overline{IOR}$/$\overline{IOW}$ pulse width		80			ns

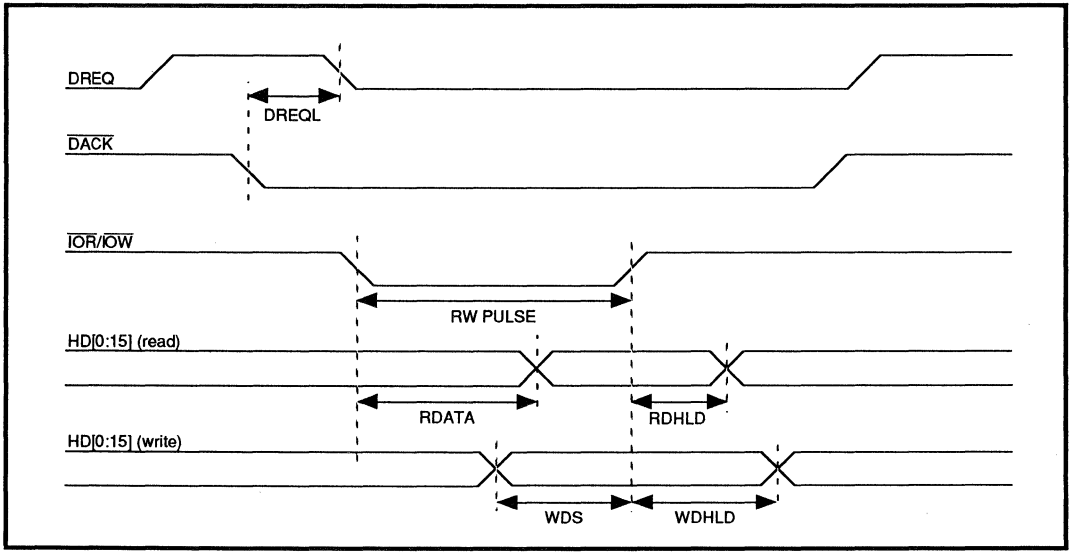


FIGURE 1: Host DMA 8/16-Bit Interface Timing

HOST Programmed I/O 8-16-Bit Timing Parameters (Figure 2)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
CS16L	$\overline{HCS0}$ low, A0:2, A9 low, or $\overline{HCS1}$ high to $\overline{IOCS16}$ low				20	ns
IOCHL	$\overline{IOR}$/$\overline{IOW}$ low to $\overline{IOCHRDY}$ low				25	ns
IOCHTW*	$\overline{IOCHRDY}$ pulse width		0		5xBCLK	ns
RDTA	$\overline{IOR}$ low to HD[0:15] valid				60	ns
RDHLD	$\overline{IOR}$ high to HD[0:15] tri-state		0		20	ns
WDS	HD [0:15] setup to $\overline{IOW}$ high		40			ns
WDHLD	HD[0:15] hold from $\overline{IOW}$ high		10			ns
RWPULSE	$\overline{IOR}$/$\overline{IOW}$ pulse width		80			ns
ADRSET	$\overline{HCS0}$, A0:2, A9/$\overline{HCS1}$, setup to $\overline{IOR}$/$\overline{IOW}$ low		25			ns
ADRHLD	$\overline{HCS0}$, A0:2, A9/$\overline{HCS1}$ hold, from $\overline{IOR}$/$\overline{IOW}$ high		10			ns

*Maximum specification applies when Auto Wait State Generation is disabled (Register 58H, Bit 2 is reset.)

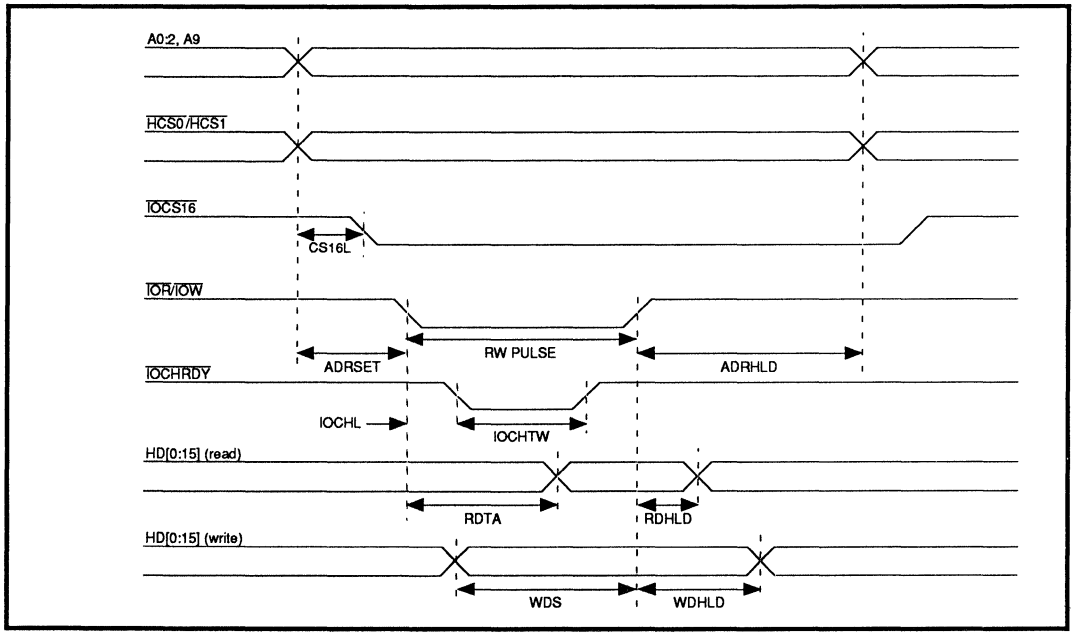


FIGURE 2: Host Programmed 8/16-Bit Timing

Microcontroller Interface Timing Parameters (Figures 3, 4)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Ta	ALE Width		45			ns
Taw	ALE↓to $\overline{\text{WRITE}}$ ↓		25			ns
Tar	ALE↓to $\overline{\text{READ}}$ ↓		25			ns
Tw	$\overline{\text{WR}}$ Width		140			ns
Tr	$\overline{\text{RD}}$ Width		140			ns
As	Address AD [0:7] valid to ALE ↓		5			ns
Ah	ALE↓to Address AD [0:7] invalid		20			ns
Cs	ALE↓to CS valid				5	ns
Ch	$\overline{\text{RD}}$↑or $\overline{\text{WR}}$↑to CS ↓		0			ns
Wds	Write Data AD [0:7] valid to $\overline{\text{WR}}$ ↑		55			ns
Wdh	$\overline{\text{WR}}$↑to Write Data AD [0:7] invalid		10			ns
Tda	$\overline{\text{RD}}$↓to Read Data AD [0:7] valid				100	ns
Tdh	$\overline{\text{RD}}$↑to Read AD [0:7] float (undriven)				50	ns

NOTE: ↓Indicates falling edge. ↑ Indicates rising edge.

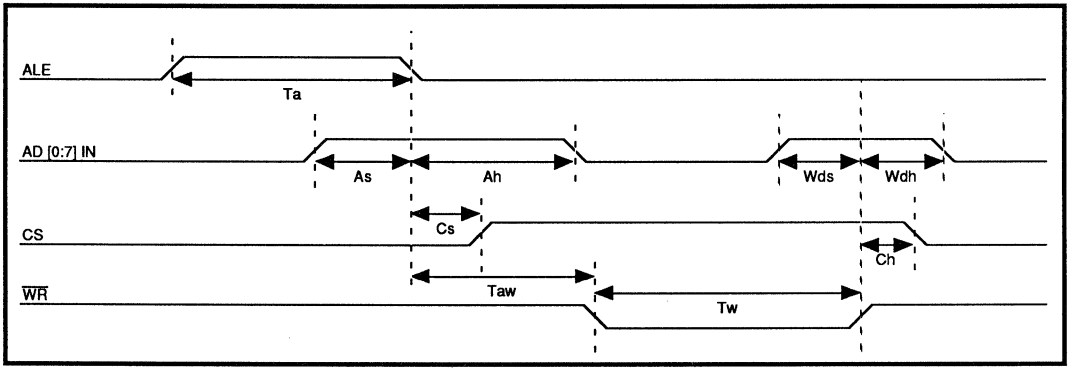


FIGURE 3: Register Write Timing

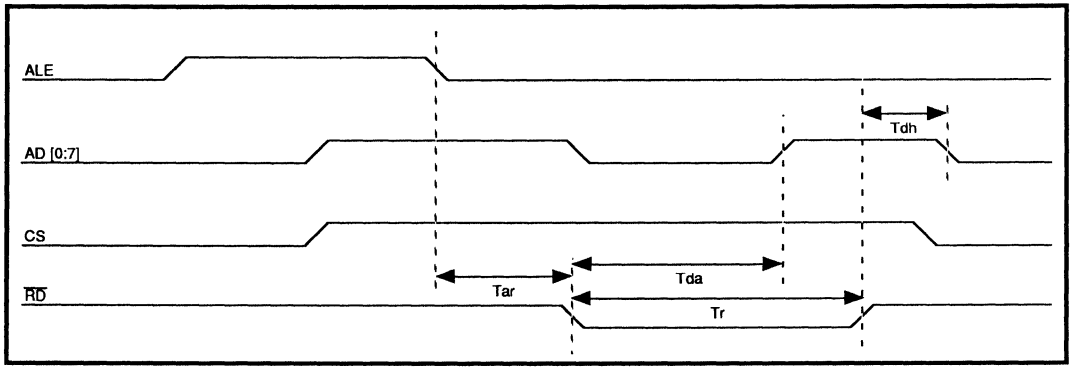


FIGURE 4: Register Read Timing

Disk Read/Write Timing Parameters (Figures 5, 6)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
T	RD/REF CLK Period		62.5			ns
T/2	RD/REF CLK High/Low Time		23			ns
Tr = Tf	RD/REF CLK Rise and Fall time				5	ns
Ds	NRZ valid to RD/REF CLK ↑		15			ns
Dh	RD/REF CLK ↑ to NRZ invalid		10			ns
As*	$\overline{AMD}$ valid to RD/REF CLK ↑		15			ns
Dv	RD/REF CLK ↑ to NRZ		10		40	ns
Wv*	RD/REF CLK ↑ to $\overline{WAM}$		10		40	ns

NOTE: ↓ Indicates falling edge. ↑ Indicates rising edge.

* These specifications are only applicable in the Soft Sector Mode.

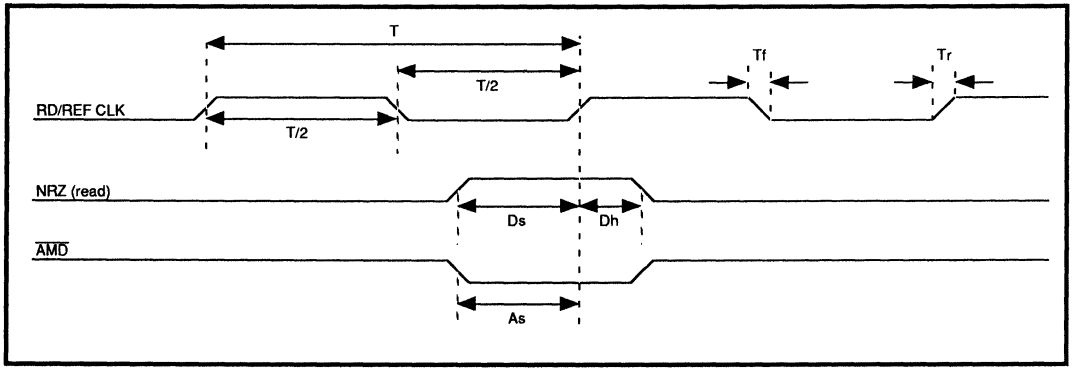


FIGURE 5: Disk Read Timing

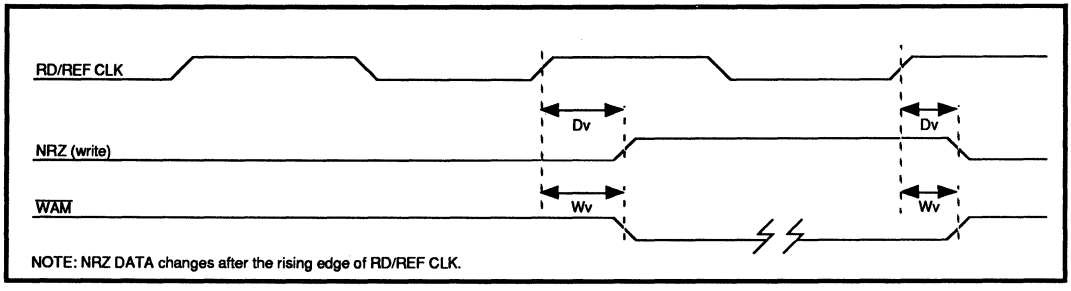


FIGURE 6: Disk Write Timing

Register 70H Access Timing Parameters (Figures 7, 8)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
To	$\overline{RD}$↓to $\overline{MOE}$ ↓				40	ns
Tda	BD[0:7] valid to AD[0:7] valid				55	ns
Trh	$\overline{RD}$↑to AD[0:7] invalid				50	ns
Toh	$\overline{RD}$↑or $\overline{WR}$↑to $\overline{MOE}$ ↑				40	ns
Taw	AD[0:7] valid to $\overline{WE}$ ↓				55	ns
Tao	AD[0:7] valid to $\overline{MOE}$↓				55	ns
Tad	AD[0:7] valid to BD[0:7] valid				55	ns
Twwh	$\overline{WR}$↑to $\overline{WE}$↑				40	ns
Twdh	$\overline{WR}$↑to BD[0:7] invalid		50			ns

NOTE: ↓ Indicates falling edge. ↑ Indicates rising edge.

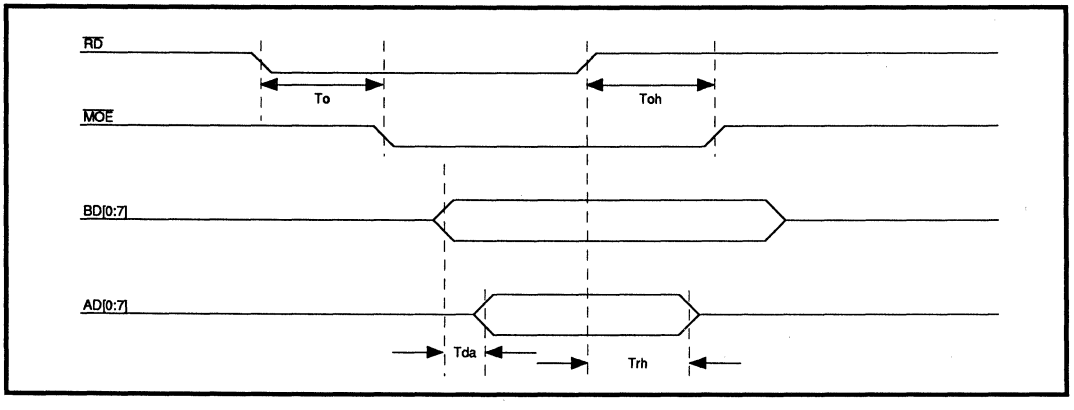


FIGURE 7: Register 70H Read Timing

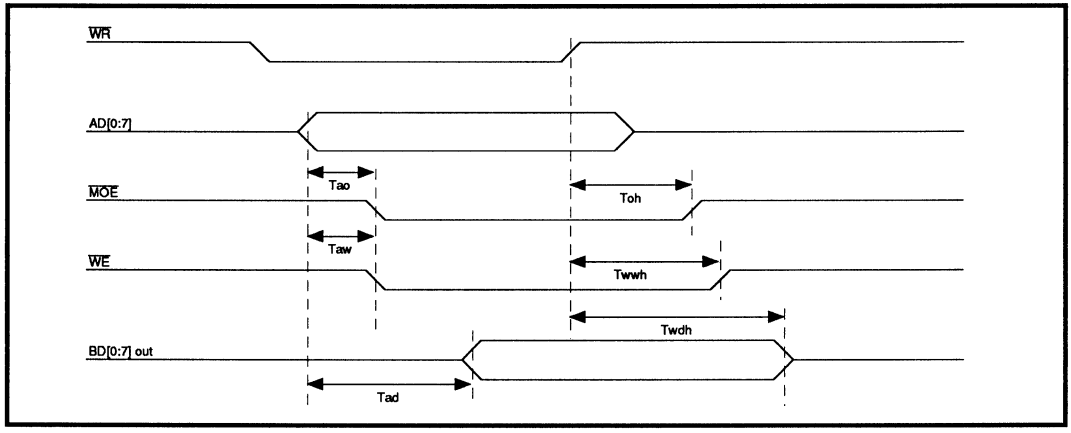


FIGURE 8: Register 70H Write Timing

Buffer Memory Read/Write Timing Parameters (Figure 9)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
T_B	BCLK Period		41			ns
$T_B/2$	BCLK High/Low Time		16			ns
$T_{Br}=T_{Bf}$	BCLK Rise and Fall Time				5	ns
T1	BUFCLK* Period		125			ns
Av	BUFCLK*↓to BA[0:15] valid				65	ns
Dov	BUFCLK*↑to BD[0:7] valid				50	ns
Doh	BUFCLK*↑to BD[0:7] invalid		0			ns
Mv	BUFCLK*↑to $\overline{MOE}$ ↓				30	ns
Mh	BUFCLK*↓to $\overline{MOE}$ ↑		10		35	ns
Wv	BUFCLK*↑to $\overline{WE}$ ↓				30	ns
Wh	BUFCLK*↓to $\overline{WE}$ ↑		5		30	ns
Dma	$\overline{MOE}$ ↑to BA[0:15] Hold		10		30	ns
Dis	BD[0:7] valid to BUFCLK*↓		5			ns
Dih	BUFCLK*↓to BD[0:7] invalid		10			ns
TBbr	BCLK↑to BUFCLK↑				24	ns
TBbf	BCLK↓to BUFCLK↓				21	ns

NOTE: ↓Indicates falling edge. ↑ Indicates rising edge.

* BUFCLK is an internal signal which indicates the period of Buffer Memory Access Cycle. These specifications can be tested when the period of BCLK pin is the same as the period of Buffer Memory Access Cycles (i.e., Register 7FH, Bits 6 and 7 are 1 and 0, respectively). If the Buffer Memory Access Cycle period is programmed to be a multiple of the period of BCLK pin, BUFCLK above refers to the Buffer Memory Access Cycles and the falling edge referred to above would be coinciding with the rising edge of the BCLK pin.

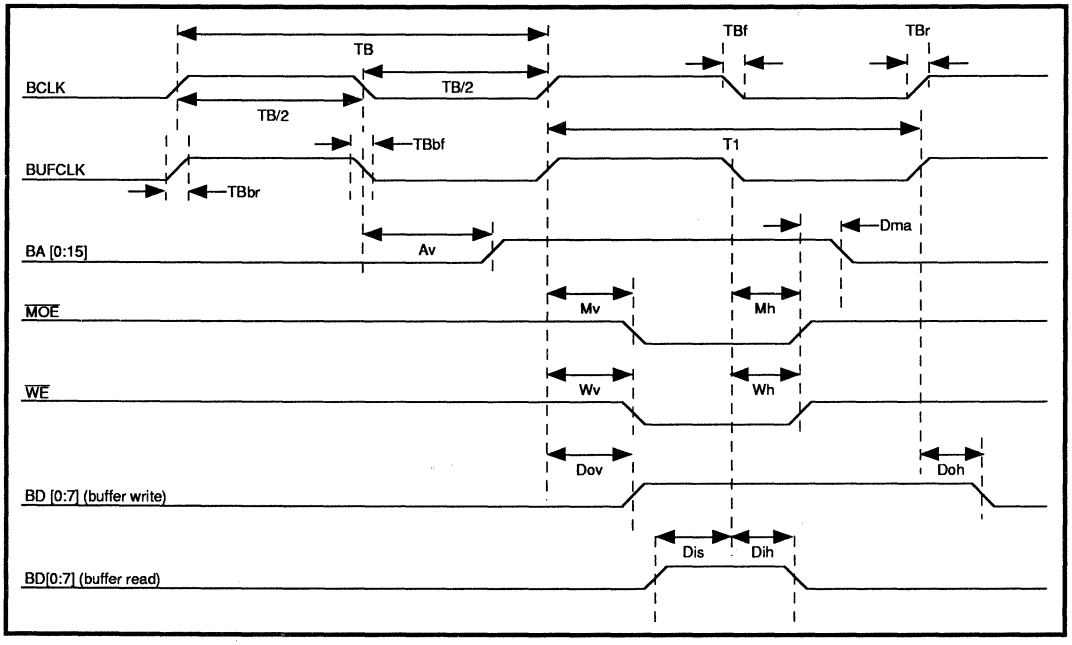
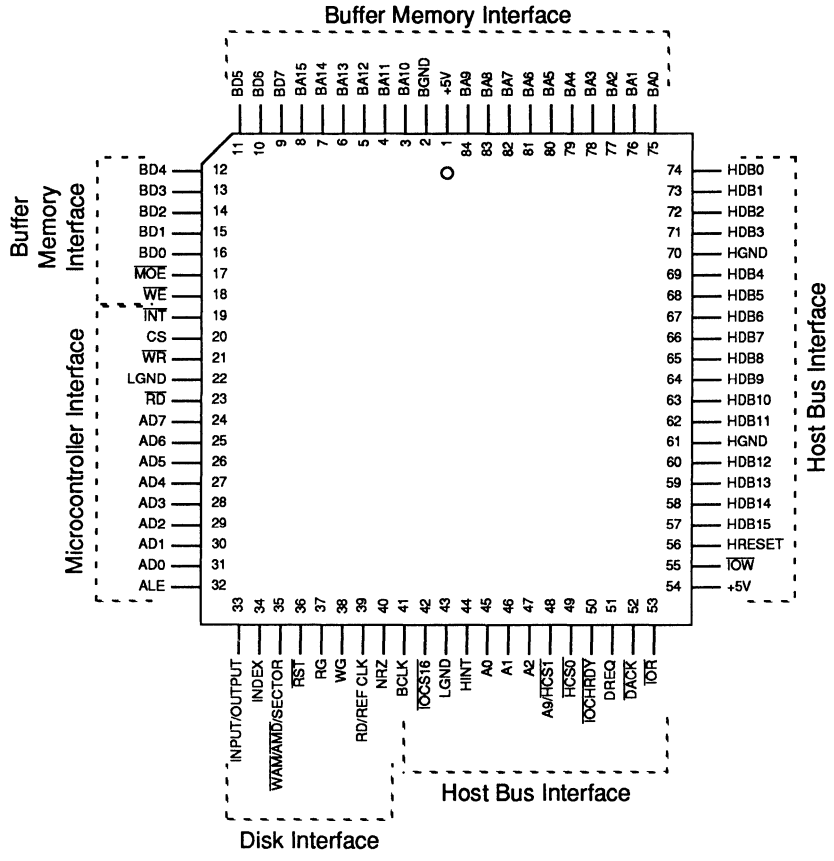


FIGURE 9: Buffer Memory Read/Write Timing

PACKAGE PIN DESIGNATIONS
(TOP VIEW)



84-pin PLCC

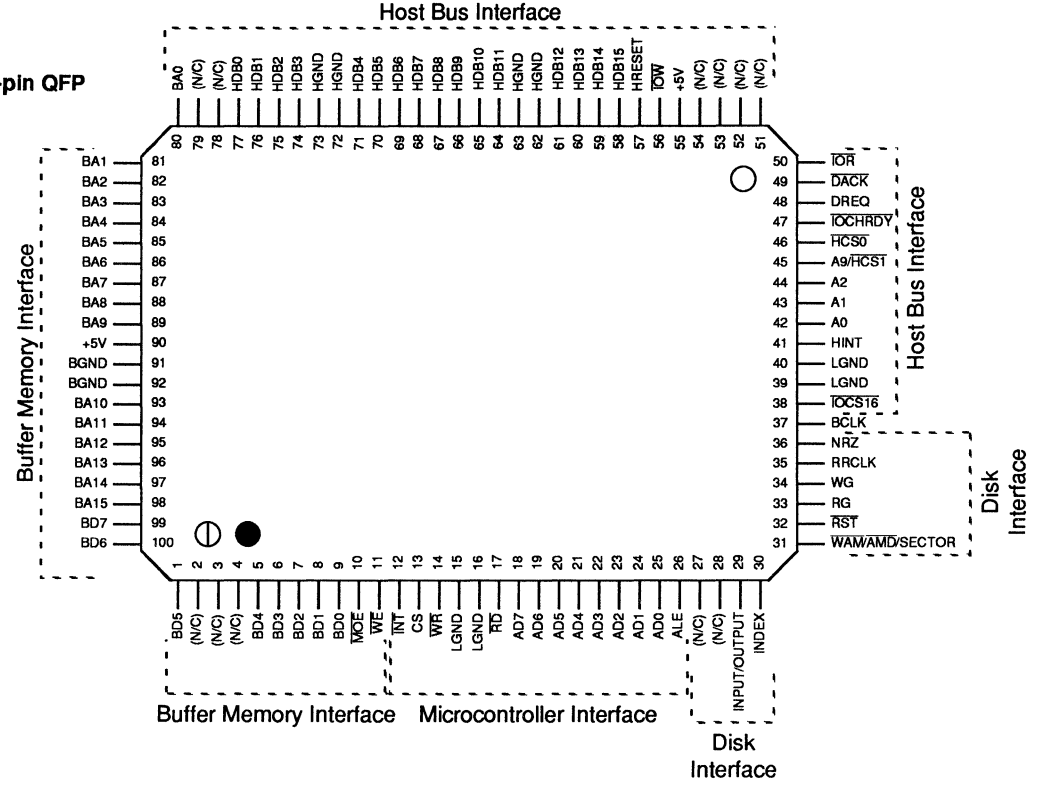
CAUTION: Use handling procedures necessary for a static sensitive component.

8

PACKAGE PIN DESIGNATIONS (Continued)

(TOP VIEW)

CAUTION: Use handling procedures necessary for a static sensitive component.



ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32C260, PC AT/XT Combo Controller		
84-Pin PLCC	32C260-CH	32C260-CH
100-Pin QFP	32C260-CG	32C260-CG

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714) 731-7110, FAX: (714) 573-6914

silicon systems®
A TDK Group Company

SSI 32C261
PC AT/XT Combo Controller With RLL (2, 7) ENDEC

Advance Information

September 1991

DESCRIPTION

The SSI 32C261 is a CMOS VLSI device which integrates the major portion of the hardware needed to build a PC AT/XT driven hard disk controller. The 32C261 is capable of supporting interleaved data transfer rates up to 24 Mbit/s. This chip represents a major reduction in part count when used with the SSI 32P548 Pulse Detector and Data Synchronizer combo chip, the SSI 32R4610 Read/Write device, and the SSI 32H4631 Servo and Motor Speed Controller device, implementing a low power and cost efficient 4-chip set intelligent drive solution.

The SSI 32C261 includes a dual port Buffer Manager, a storage controller and an extensive hardware support, including 24 mA drivers, for the PC AT/XT and other compatible interfaces.

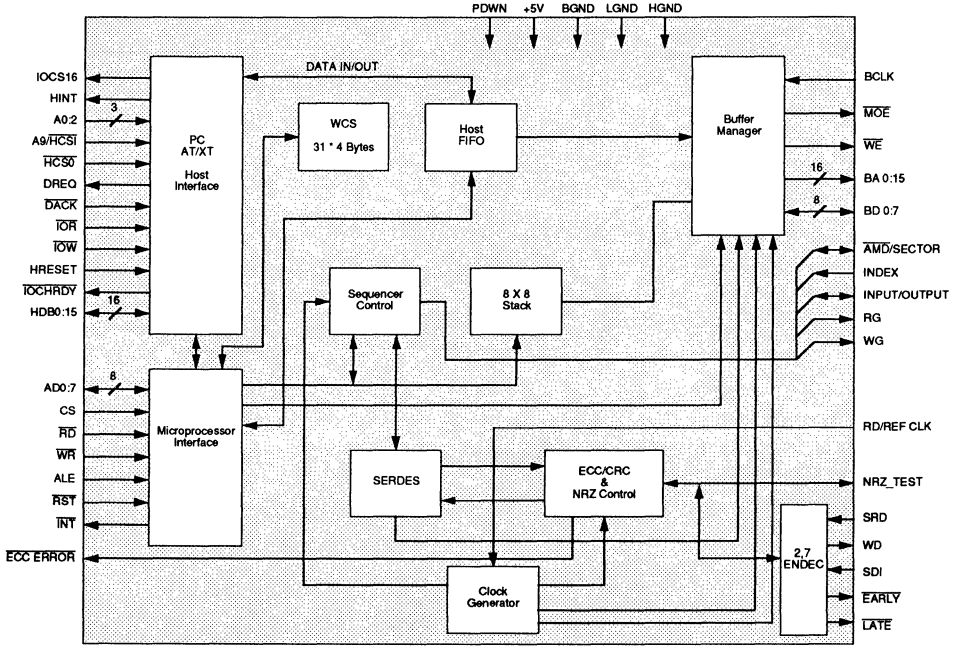
The SSI 32C261 performs all the controller functions for the peripheral device, such as encoding and decoding; serialization and deserialization; ECC generation and checking on the data stream, and CRC generation and checking on the header of the data stream.

FEATURES

- **PC AT/XT Bus Interface**
  - **Single Chip PC AT/XT Controller**
  - **Direct bus interface logic with on-chip 24 mA drivers**
  - **Logic for daisy chaining 2 embedded controller drives on a PC bus in a master/slave configuration**
  - **Supports host data transfer under DMA or programmed I/O for both PC XT and PC AT modes**
- **Buffer Manager**
  - **Supports Buffer Memory throughput to 8 Mbytes/s**
  - **Direct Buffer Memory addressing up to 64 kB static RAM**
  - **Dual port circular buffer control**

(Continued)

BLOCK DIAGRAM



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SSI 32C261
PC AT/XT Combo Controller
With RLL (2, 7) ENDEC

FEATURES (Continued)

- **Storage Controller**
  - **2, 7 RLL ENDEC for up to 24 Mbits/s NRZ data rate**
  - **Selectable 16-bit CRC or 56-bit ECC polynomial with fast hardware correction circuitry**
  - **Supports sector level defect management**
  - **Supports 1:1 interleaved operation**
  - **Mates with SSI 32P548, SSI 32P5481 or SSI 32P551 - Pulse Detector and Data Synchronizer combo for a low power laptop disk drive**
- **Microprocessor Interface**
  - **Supports both Intel 8051, and Motorola 68HC11 family of microprocessors**
  - **Interrupt or polled microprocessor interface**
- **Others**
  - **Internal power down mode**
  - **Low power CMOS technology**
  - **Fully software compatible with the Cirrus Logic CL-SH260 chip**
  - **Available in a 100-pin QFP package**

PIN DESCRIPTION

GENERAL

NAME	TYPE	DESCRIPTION
+5V		POWER SUPPLY PIN, VCC
BGND		BUFFER BUS GROUND
LGND		LOGIC GROUND
HGND		HOST GROUND

HOST INTERFACE

A0:2	I	HOST ADDRESS LINES. These pins are used to address the internal registers by the AT bus.
A9/$\overline{HCS1}$	I	HOST ADDRESS LINE 9/ HOST CHIP SELECT 1. A9, this pin is used in conjunction with the A0:2 address lines to address the internal task file registers. HCS1 is an active low pin, used to qualify Host access.
$\overline{HCS0}$	I	HOST CHIP SELECT 0. Active low, this pin selects access to the control, status and data registers.
$\overline{IOCS16}$	O	I/O SELECT 16. An open drain output that indicates that a 16-bit sector buffer transfer is active.
HINT	O	HOST INTERRUPT. Asserted to indicate to the Host that the controller needs attention.
$\overline{IOCHRDY}$	O	I/O CHANNEL READY. Active low, this signal is asserted whenever that internal host FIFO is not ready to transfer data.
DREQ	O	DMA REQUEST. This pin is programmed to function as the PC/AT bus signal in the PC/AT DMA mode.
$\overline{DACK}$	I	DMA ACKNOWLEDGE. Active low, in the PC/AT DMA mode this pin is programmed to be the PC/AT channel signal - DACK.
$\overline{IOR}$	I	INPUT READ SELECT. Active low, this pin is asserted by the Host during a Host read operation.
$\overline{IOW}$	I	INPUT WRITE SELECT. Active low, asserted by the HOST during a HOST write operation.

HOST INTERFACE (Continued)

NAME	TYPE	DESCRIPTION
HRESET	I	HOST RESET. This signal resets all commands in progress when active, and initializes the control/status registers.
HDB 15:0	I/O	HOST DATA BUS. Active high bidirectional pins. These bits are used for data transfers between the Host and the Buffer Manager.

DISK INTERFACE

INDEX	I	INDEX. Input for index pulse received from the drive.
INPUT/ OUTPUT	I/O	INPUT/OUTPUT. A general purpose control and status pin. It can be either an input or an output. At power-on, this pin is an input.
SECTOR/ $\overline{\text{AMD}}$	I	SECTOR/ADDRESS MARK DETECT. This pin is used in the hard sector mode as the sector input. A pulse on this pin indicates a sector mark is found. RG will be asserted after the sector pulse by the sequencer. In the soft sector mode, this pin is normally not used and can be left floating. In the test mode, however, this pin can be programmed as the address mark detect signal for testing the internal disk to buffer data transfer logic.
RG	O	READ GATE. During disk data read, this pin is asserted. Active high.
WG	O	WRITE GATE. During disk data write, this pin is asserted. Active high.
RRC	I	READ/REFERENCE CLOCK. This pin is used in conjunction with the SRD, and WD pin to clock data in and out of the SSI 32C261 device.
NRZ_TEST	I/O	NRZ TEST PIN. When configured as an output the data transfers between the buffer RAM and the ENDEC can be monitored. When configured as an input (only possible in test mode), data can be redirected from it and transferred to either the buffer data bus BD(0:7), or to the WD pin. This pin is used to test the internal ENDEC logic and the disk data transfer logic.
SRD	I	SYNCHRONIZED READ DATA INPUT FROM THE DISK.
$\overline{\text{PDWN}}$	I	POWER DOWN. When asserted low this pin puts the device in a low power state by shutting off the internal BCLK.
WDO	O	WRITE DATA OUTPUT. 2,7 RLL encoded write data output to the data synchronizer.
$\overline{\text{LATE}}$	O	PRECOMP. CONTROL OUTPUT. Used to shift write data output pulses later. Low true.
$\overline{\text{EARLY}}$	O	PRECOMP. CONTROL OUTPUT. Used to shift write data output pulses earlier. Low true.
SDI	I	SYNC DETECT INPUT. A high level on this pin indicates that a sync field (preamble) pattern is being detected. This pin is used only in the soft sector mode by this chip to assert RG; in the hard sector mode it is ignored and can be left floating.
$\overline{\text{ECC}}$ $\overline{\text{ERROR}}$	O	ECC ERROR DETECTED. A low signal on this pin indicates when an ECC error was detected while reading a sector of the disk. It is reset when the sequencer program is restarted or by a hardware or software reset.

MICROPROCESSOR INTERFACE

$\overline{\text{RST}}$	I	RESET. Active low input, when pulled low, the internal registers of the SSI 32C261 are held at reset.
ALE	I	ADDRESS LATCH ENABLE. This control signal latches the address on the address/data lines.
CS	I	CHIP SELECT. Active high signal, when asserted, the internal registers of the SSI 32C261 can be accessed.

PIN DESCRIPTION (Continued)

MICROPROCESSOR INTERFACE (Continued)

NAME	TYPE	DESCRIPTION
$\overline{WR}$	I	WRITE. Active low input, when active the data is written to the internal registers.
$\overline{RD}$	I	READ. Active low input, when active that data is read from the internal registers.
$\overline{INT}$	O	INTERRUPT. An open drain output, when active, the microprocessor is requesting controller service.
AD7:0	I/O	ADDRESS/DATA BUS. 8-bit bus for both microprocessor register address and data.

BUFFER MANAGER INTERFACE

BA0:15	O	BUFFER MANAGER ADDRESS LINES. Active high, for direct connection to a status RAM.
BD0:7	I/O	BUFFER MANAGER DATA BUS. 7 through 0. Active high, buffer data bus that connects directly to the buffer RAM.
$\overline{MOE}$	O	MEMORY OUTPUT ENABLE. Active low select for the buffer RAM.
$\overline{WE}$	O	WRITE ENABLE. Active low, write enable for the buffer RAM.
BCLK	I	SYSTEM CLOCK. This signal is used to synchronize the buffer RAM access, including the generation of memory address bits, write enable $\overline{WE}$, and memory output enable $\overline{MOE}$.

FUNCTIONAL DESCRIPTION

The major functional elements and data paths of the SSI 32C261 are shown in the block diagram.

The four major functional blocks are:

Buffer Memory Interface

Microcontroller Interface

Disk Formatter

Host Interface

The SSI 32C261 performs the functions to interface a serial data storage device such as a Winchester Disk Drive, to a parallel bus interface for data processing on a byte wide basis. The functions necessary to accurately make this conversion are serialization/deserialization, encoding/decoding, error detection and correction, and data path control. The SSI 32C261 also has a general purpose interface line to further facilitate control of the data storage device or parallel interface. An eight byte stack allows data to be saved and reviewed by the microprocessor for error handling purposes. The internal sequencer performs most of the operations in conjunction with the control and status registers. The sequencer program is contained in an internal sequencer RAM, which is easily (re)programmed providing almost infinite flexibility in drive format and control features. A microprocessor effects both initialization and control of the SSI 32C261 by writing to and reading from the internal registers, sequencer RAM, stack and general purpose I/O circuitry. The microprocessor interface block of the SSI 32C261 provides the communication and control for the SSI 32C261 to the microprocessor. ***For a complete description of the programmable registers, refer to the SSI 32C261 Design Guide.***

BUFFER MEMORY INTERFACE

The buffer memory interface, referred to as the Buffer Manager, includes a bi-directional data bus that exchanges data bytes between an external buffer memory and the serializer/deserializer or the host interface. The circuitry allows the use of static RAM as a dual port circular FIFO, and supervises data transfers to and from the RAM. The device contains logic that resolves disk and host requests. The arbitration is achieved by giving priority to the disk and utilizing internal data FIFOs for temporary host and disk data storage.

The Buffer Manager is capable of handling buffer sizes from 256 bytes to 64K bytes. The circuit provides up to 16 direct address signals, along with Memory Output Enable ($\overline{MOE}$) and Write Enable ($\overline{WE}$) signals. The buffer RAM address is generated from one of two 16-bit counters, one of which being the write address

pointer (5CH & 5DH) and the other the read pointer (5AH & 5BH). The address generation as well as the memory control signals are synchronous to the Buffer Clock (BCLK), allowing the user many choices of buffer RAM speeds, with different combinations of the disk and host transfer rates.

The Buffer Memory Interface is a dual port buffer controller that allows low speed static RAMs to be configured as a dual port circular FIFO buffer. It generates all the buffer memory addressing required and manages two ports: Port A, a synchronous peripheral device interface and Port B, an asynchronous host interface. The Buffer Manager has arbitration logic to support the AT or XT host transfers under DMA control or Programmed I/O control.

On-chip counters generate the addresses (BA0-BA15) needed to access up to 64K of external static RAM. Along with the addresses, the Buffer Manager block outputs a Memory Output Enable ($\overline{MOE}$) and a Write Enable ($\overline{WE}$) signal for a static RAM buffer.

The address generator contains two 16 bit pointers, the read address pointer (RAP) and the write address pointer (WAP), which indicate where in the external buffer RAM data is to be read or written. During data transfers, these pointers are automatically incremented as the RAM is accessed. The pointers wrap around to 0 when the programmed buffer size is exceeded. To prevent host overruns of the buffer (caused by one of the pointers overtaking the other), the address generator includes a 16-bit stop pointer (5EH & 5FH). The microprocessor loads SO with the last address in buffer memory to be accessed during a host DMA transfer. When the port B address (RAP during an upload to the host or WAP during a download to the peripheral) reaches the value in SP, the DMA transfer is automatically suspended.

The period of the Buffer Memory access cycle is determined by programming bits 6 and 7 of CLOCK CONTROL, register 7FH, and is based on the BCLK input. The period of the Buffer Memory access cycle determines the access time requirement for the buffer RAMs. The 32C261 samples the data from the RAM at the falling edge of the BCLK signal. Buffer Memory throughput and the RAM speeds can be determined from the following equations:

Buffer Memory Throughput =

1 / Period of Memory Access Cycle

For Buffer Memory Read:

Max. Read Access Time = $T_1 - Av_{max} - Dis_{min}$

Min. Output Enable = $(T_1/2) - Mv_{max} - Dis_{min}$

For Buffer Memory Write:

Address set up to $\overline{WE}\uparrow = T_1 - Av_{max} + Wh_{max}$

Data set up to $\overline{WE}\uparrow$ = Min. Output Enable
$= (T_1/2) - Mv_{max} - Dis_{min}$

Note: For an explanation of Av_{max}, Dis_{min}, Mv_{max}, Wh_{max}, Dov_{max} parameters, refer to Buffer Memory Read/Write Timing Parameters.

MICROPROCESSOR INTERFACE

The microprocessor interface decodes microprocessor read and write requests and provides access to the appropriate register or internal memory location. Since both data and address information are carried on the multiplexed bus lines AD0-AD7, address information is latched from the bus on the falling edge of the microprocessor signal, Address Latch Enable (ALE). When CS is asserted along with either $\overline{RD}$ or $\overline{WR}$, the register whose address was previously latched is selected. The addresses and names of all the accessible registers are shown in the Register Address Map (See SSI 32C261 Design Guide). The microprocessor should not read or write the sequencer RAM while the sequencer is running, since there is no circuitry to resolve conflicting accesses and incorrect sequencer operation will result.

The status and control registers make status information available to the microprocessor and allow the device to be configured for a wide variety of peripheral applications. The microprocessor can monitor the status of transfers in progress and control the ECC register operation, the ECC polynomial, the clock generation hardware, the sequencer program execution, buffer size, read and write pointers, and stop pointers. The microprocessor also has access to the sequencer's microprogram RAM so that it loads the microcode for all controller operations.

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DISK FORMATTER

The serializer/deserializer circuit interfaces the parallel buffer memory bus to serial NRZ data stream of the peripheral device. Byte synchronism is maintained with a bit ring, which is an 8-bit recirculating shift register clocked by the peripheral bit clock. During a sector write, the bit ring is initialized explicitly with a sequencer instruction. The bit ring continues to operate until the end of the field (ECC written or read). During write operations, the sequencer may cause address marks and sync patterns to be loaded into the serializer instead of data bytes. These special patterns are contained in a sequencer instruction and are transferred to the serializer over an internal byte wide data path. During read operations, bytes of overhead information may be routed to the stack or sequencer for comparison against target values. This process is controlled by the control field (SEQCONF) in each sequencer instruction.

The eight byte recirculating stack may be used to capture read data for later examination by the microprocessor. Data is pushed onto the stack under sequencer control. The control bit STACKEN in the sequencer instruction field SEQCONF in the sequencer instruction field SEQCONF directly controls the stack. If more than 8 bytes are written to the stack, only the last 8 will be saved. When a data byte is read from the top of the stack by the microprocessor via the STACK register, the data is recirculated to the bottom of the stack, allowing the stack contents to be examined more than once without the use of temporary storage in the microprocessor or buffer.

Serial peripheral data is passed through a variable length shift register with programmable exclusive OR feedback that performs ECC or CRC generation and checking. The feedback taps for the desired polynomials are fixed as follows and the user may select between the 16-bit CRC, 32-bit ECC, or the 56-bit ECC as desired. This selection is accomplished by programming the WCS COUNT FIELD and the ECC CONTROL register (Register 71H, bit 6).

In the forward direction, the options available include:

CRC polynomial which is the CCITT CRC code:

$x^{16} + x^{12} + x^5 + 1$

32-bit ECC polynomial:

$x^{32} + x^{28} + x^{26} + x^{19} + x^{17} + x^{10} + x^6 + x^2 + 1$

56-bit ECC polynomial:

$x^{56} + x^{52} + x^{50} + x^{43} + x^{41} + x^{34} + x^{30} + x^{26} + x^{24} + x^8 + 1$

The reverse polynomial options include:

32-bit ECC polynomial:

$x^{32} + x^{30} + x^{26} + x^{22} + x^{15} + x^{13} + x^6 + x^4 + 1$

56-bit ECC polynomial:

$x^{56} + x^{48} + x^{32} + x^{30} + x^{26} + x^{22} + x^{15} + x^{13} + x^6 + x^4 + 1$

The 56-bit polynomial can detect single burst errors up to 56 bits in length, and double-burst errors, where the combination of bursts is less than or equal to 41 bits. This polynomial can also correct single-burst errors up to 23 bits in length. The 32-bit ECC polynomial is the standard polynomial found in IBM PC AT controllers.

The forward and reverse polynomial is selected by programming ECC CONTROL (Register 71H, Bit 7). Whichever polynomial is selected, the ECC/CRC shift registers always start preset to all 1s.

The sequencer controls the time critical operations of the SSI 32C261. It executes programs stored in the 28 word by 32-bit sequencer RAM, and can be programmed to support hard and soft sectored read, write, search, and verify operations for a wide variety of Winchester disk drives and other peripherals. The sequencer RAM is loaded by writing to the sequencer instruction registers as outlined in the Sequencer Instructions of this data sheet. Each instruction is comprised of four bytes. Each of the four bytes represents a function of the sequencer operation. They are address field, control field, data type field, and data field. The organization of these fields is shown in the Register Bit Map in the SSI 32C260 Design Guide. The Sequencer Registers provide control from and status to the microprocessor and sequencer. They contain branch, next, and start addresses, and sequencer status information. The SEQUENCER STATUS register provides information on the sequencer state such as whether an ECC error occurred, a compare equal or low occurred, if the branch condition or address mark is active, or whether the sequencer is halted.

HOST INTERFACE

The internal receivers and drivers on the host interface block allow the device to connect directly to the PC Host bus. The drivers are capable of sinking up to 24 mA and drive a load up to 300 pF.

The wait state generator extends the Host I/O cycle and inserts wait states by asserting $\overline{\text{IOCHRDY}}$. This generator is only active during Programmed I/O transfers and works in two ways: 1) inserting programmed number of Buffer Memory Cycles for every host access of the device, and 2) asserting $\overline{\text{IOCHRDY}}$ only when the device is not ready for the transfer. Register 58H, Bits 0 and 1, program the wait states cycles and Bit 2 asserts $\overline{\text{IOCHRDY}}$ whenever the device is not ready for transfer.

The auto decoding circuitry allows the device to speed up the performance of the controller by decoding Write commands that require data transfer from the Host to the Buffer Memory. These commands include Format (5XH), Write Buffer (E8H), Write or Write long (3XH). The device automatically starts accepting data without the local microcontroller control when any of these commands are loaded into the COMMAND REGISTER by the host. If interrupts are enabled, the device generates an interrupt to the local microcontroller. The PC STOP POINTER (Registers 5EH and 5FH) is initialized to 01FFH. If DISABLE STOP POINTER COMPARE (Register 52H, Bit 6) is set, the local microcontroller must initialize the PC STOP POINTER to enable comparison of the WRITE ADDRESS POINTER (Registers 5CH and 5DH) with the HOST STOP POINTER. The Formatter disconnects from the Buffer Manager on receiving one of these commands. It also disables write access by the local microcontroller to the DMA CONTROL REGISTER (53H) and WRITE ADDRESS POINTERS (5CH and 5DH). In addition, read/write access to the BUFFER MEMORY ACCESS REGISTER. Access to these registers is enabled when the local microcontroller writes to AUTOCOMMAND "LOCK" RELEASE register (73H).

The ECC bytes are transferred to and from the host by enabling Bit 1 of the command byte by the host, indicating Read and Write Long command. If a Read or Write Long command is received, Buffer Memory transfers to/from the Host will exceed the PC STOP POINTER (Registers 5EH and 5FH) by the count of ECC bytes. Initially the PC STOP POINTER is set at the end of the Data Field. When the active READ ADDRESS POINTER (Registers 5AH and 5BH), or WRITE ADDRESS POINTER (Registers 5CH and 5DH), matches the PC STOP POINTER (Registers 5EH and 5FH), the internal FIFO will be emptied of the word width data, the PC STOP POINTER gets incremented by the count of ECC bytes. The ECC bytes will then be transferred in Byte Mode.

ENDEC

The chip includes a 2,7 RLL ENDEC circuitry. The ENDEC is used to convert the data between the NRZ format and the 2,7 RLL coded format. In the case of data encoding, the serial NRZ data generated by the SERDES (serializer/deserializer) is converted to the 2,7 RLL coded data when the WG (write gate) is asserted. The data appears on the WDO (write data) pin and is synchronized at the RRCLK edges. In the case of data decoding, the encoded data received from the SRD (synchronized read data) is converted back to the NRZ data format and fed to the SERDES circuitry. The 2,7 RLL coding rules are given below:

NRZ Data				2,7 RLL Code							
First Bit			Last Bit	First Bit							Last Bit
1	1	-	-	1	0	0	0	-	-	-	-
1	0	-	-	0	1	0	0	-	-	-	-
0	1	1	-	0	0	1	0	0	0	-	-
0	0	0	-	0	0	0	1	0	0	-	-
0	1	0	-	1	0	0	1	0	0	-	
0	0	1	1	0	0	0	0	1	0	0	0
0	0	1	0	0	0	1	0	0	1	0	0

ENCODING OPERATION

In the encoding operation the ENDEC circuitry converts NRZ data from the **SERDES** into 2,7 RLL formatted data for storage onto the disk. The circuit can operate with a soft or hard sectored disk drive. In the Soft Sector Mode (Bit 7 of the **formatter mode selection register**, register 77H, is 0), the device generates a 3T (100) preamble field and can insert a N7V Address mark. The N7V Address Mark is a valid 2,7 RLL pattern which is not contained in the code set. In the Hard Sector Mode (register 77H bit 7 = 1), the device generates a 4T (1000) preamble field and no address mark.

Soft Sector Mode

In the soft sector mode, when **WG** (write gate) transitions high and the serial NRZ data remains low, the device automatically generates the 3T (100) preamble

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ENCODING OPERATION (Continued)

field at the WD (write data) output pin. The 3T preamble field will continue to be generated until the first low to high transition on the serial NRZ data stream coming from the **SERDES**. In order to generate the proper address mark, the first two non-zero NRZ bytes have to be $5EAX_{16}$, where X is an arbitrary hex digit. For this data pattern the first low to high transition on the serial NRZ data stream happens at the second bit position of 5 (0101). The device then automatically changes the '1' in the eleventh position of the 2,7 RLL encoded sequence to a '0'. This generates a pattern of 8091, or seven 0's followed by two 0's. This unique pattern satisfies the 2,7 RLL constraints, but will never occur during a normal encoding sequence. After the address mark is encoded, the address mark generator is disabled and any further 5EAX pattern is encoded as normal data until the next assertion of **WG**.

Hard Sector Mode

In the hard sector mode, when **WG** output goes high and the serial NRZ data stream from the **SERDES** remains low, the device automatically generates the 4T (1000) preamble field at the **WDO** output. The 4T preamble field will be generated between the time **WG** is asserted and the first low to high transition on the NRZ serial data stream. Note that in the hard sector mode, the NRZ data is inverted before the encoder. This is because the leading 00 NRZ data pattern can generate the 4T preamble according to the coding rules after being inverted into 11.

DECODING OPERATION

In the decoding operation, the device converts 2, 7 RLL encoded data received from SRD pin to the NRZ format and feeds the data to the **serdes** circuitry.

Soft Sector Mode

In this mode, the device uses an external preamble detect signal to initiate the read sequence. If the device is mated with the SSI 32P548, the **SDO** output of that device is used. This signal is asserted when the 3T (100) preamble pattern is found. This chip provides an **SDI** input pin to be connected to the **SDO** output of the SSI 32P548 device.

When the disk sequencer program asserts read gate by executing an instruction with the bit 6 (set read gate) of the control field set, the **RG** output will not immediately be set. The **RG** remains low until two bytes after the SDI is asserted indicating the preamble field is found. After the **RG** is asserted then the chip waits for the SDI to go low and then checks the SRD pin for an address mark of 8091 coded data pattern. Note that since each address mark should be preceded by approximately 12 bytes of zeros, **RG** will not be asserted unless two bytes of zeroes are read (SDI remains asserted for two byte times); and address mark is only checked when SDI continues to be high for at least 6 more byte times after **RG** is asserted.

If SDI is asserted for less than 6 byte times after **RG** is asserted, or if an invalid address mark pattern is found (pattern not equal to 8091 hex), then the **RG** output is dropped, the device waits for the SDI to rise and the sequence repeats itself until the correct address mark is found.

If the correct address mark (8091 hex) is found after **SDI** being asserted at least 6 byte times after the **RG** assertion, then an internal Address Mark Detect (AMD) signal is asserted and enables the byte synchronizer circuitry (register 7CH). The byte sync circuitry detects the matching of the address mark with the contents of the register 7CH, and sets up alignment on the byte boundary.

The flowchart of soft sector ready process is shown on the next page.

Hard Sector Mode

In this mode the device utilizes a 4T (1000) preamble field and disregards the **SDI** input and disables the Address Mark detection circuitry. The sequencer program should be set up to wait and branch on sector. When detecting a pulse on the Sector input, the program continues to the next instruction that asserts Read Gate. Th 2,7 RLL decoding is aligned to the leading bit of the 4T data pattern. Note that in the hard sector mode the serial NRZ data stream going to the **serdes** is inverted after the decoder. Since the **SDI** input is not used, it can be left open.

LATE AND EARLY GENERATION

The $\overline{\text{LATE}}$ and $\overline{\text{EARLY}}$ outputs are generated according to the following rules:

RLL Coded Data Pattern									Precompensation
Preceding Bits				Computing Bit	Following Bits				
0	1	0	0	1	0	0	0	1	None
0	1	0	0	1	0	0	0	0	Early
-	0	0	0	1	0	0	0	-	None
1	0	0	0	1	0	0	1	0	None
0	0	0	0	1	0	0	1	0	Late
0	1	0	0	1	0	0	1	0	None

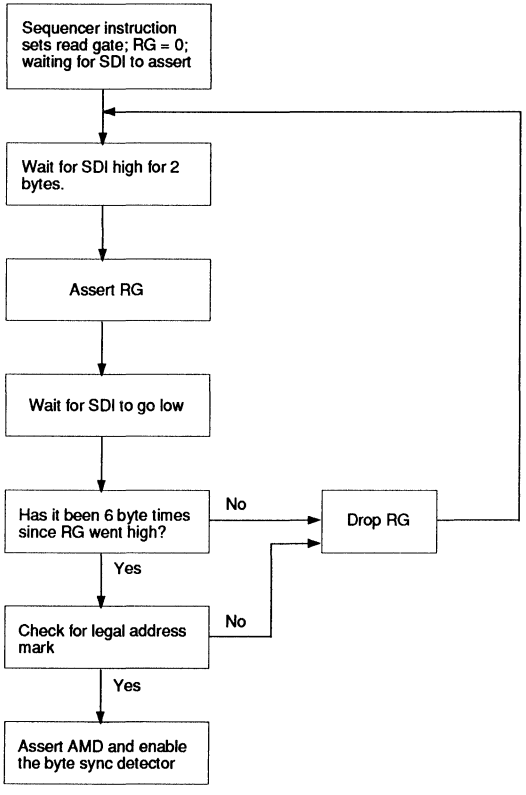

FIGURE 1: Encoder Sequence for Soft Sector Mode

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ECC ERROR INDICATOR

This chip also provides an output pin, $\overline{\text{ECC\_ERR}}$, to indicate the condition when the ECC calculation has resulted in an error (non-zero syndrome) in the case of disk data read. This pin is reset when the microprocessor writes to register 79H (the starting address register) to start the sequencer program, or by a software reset (register 71H bit 5 = 1), or by asserting the $\overline{\text{RESET}}$ pin. The $\overline{\text{ECC\_ERR}}$ pin is also cleared when the **Clear_ECC** bit (bit 3 of register 71H) is set.

POWER DOWN MODE

In the power down mode the internal clocks (BCLK and RRCLK) are disabled. The device only provides means to disable the BCLK , and it relies on the SSI 32P548 to provide the stopped **RRCLK** input. The input pin $\overline{\text{PWDN}}$, when asserted low, switches the BCLK off. This pin has the same effect as the **Bclk_disable bit** (bit 5 of register 7FH). $\overline{\text{PWDN}}$ can be left floating if not used. It should be connected to the $\overline{\text{PDWN1}}$ pin of the SSI 23P548 when used with that chip.

Note that in the power down mode, the SSI 32P548 forces the **RRCLK** to be tri-stated. An internal pull-up resistor is provided on the **RRCLK** input pin by this chip to force it into a high state during the power down time.

The power down mode is automatically recovered when the AT writes to the command register, AT programs a software reset, or when HRESET pin is asserted, even when $\overline{\text{PWDN}}$ is still held low. This allows the BCLK to recover immediately and enables the buffer manager to respond to the host. The 32C261 device asserts an interrupt to the microprocessor (if interrupt is enabled) and the microprocessor releases the $\overline{\text{PDWN}}$ pin in order to recover the disk interface. The BCLK is also reactivated any time $\overline{\text{PDWN}}$ pin is released.

TESTING THE ENDEC USING THE NRZ_TEST PIN

This chip provides an **NRZ_TEST** pin for the testing purposes. Using the **NRZ_TEST** pin data flow between the **BD bus** (buffer data bus) and the ENDEC pins (**SRD** and **WD**) can be monitored. The **NRZ_TEST** pin can also be configured as input so that data can be injected from it and checked at either the **BD bus** or the **WD** pin terminal.

When the **NRZ_TEST** pin is configured as input, data is redirected from **NRZ_TEST** rather than from either the **BD bus** of the **SRD**. For instance, in order to test the ENDEC encoding logic, the data path is configured as from the **NRZ_TEST** pin to the **WD** pin, and the data from the **BD** bus is ignored. In the case of testing the data transfer logic from the **NRZ_TEST** pin to the buffer data, the data coming from the **SRD** pin can be ignored.

Register 7FH bits 3 and 4 are used to redirect the data flow. However, these two bits are qualified only if register 52H bit 7 (Test mode enable bit) is set. The following is a table showing data transfer path in different cases:

Reg 7FH Bits 4.3	WG	RG	DATA PATH
0X	1	0	BD bus → WD (encoded format)
			BD bus → NRZ_test (NRZ format)
X0	0	1	SRD → NRZ_test (serial NRZ)
			SRD → BD bus
X1	0	1	NRZ_text → BD bus
			(Sector/$\overline{\text{AMD}}$ = Address mark detect in the soft sector mode)
1X	1	0	NRZ_test → WD

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Ambient Temperature Under Bias	0 to 70	°C
Storage Temperature	-65 to 150	°C
Voltage On Any Pin With Respect To Ground	GND-0.5 to VCC+0.5	V
Power Dissipation	0.750	Watt
Power Supply Voltage	7	V
Max Current Injection	50	mA

NOTE: Stress above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
VCC	Power Supply Voltage	Operating	4.5		5.5	V
VIL	Input Low Voltage		-0.5		0.8	V
VIH	Input High Voltage		2.0		VCC+0.5	V
VOL(1)*	Output Low Voltage	IOL = 2 mA			0.4	V
VOL(2)	Output Low Voltage	IOL = 24 mA			0.5	V
VOH	Output High Voltage	IOH = -400µA			2.4	V
ICC	Supply Current				50	mA
ICC_S	Supply Current Standby	$\overline{PDWN}$ = low		650		µA
IL	Input Leakage Current	0<VIN<VCC	-10		10	µA
CIN	Input Capacitance				10	pF
COUT	Output Capacitance				10	pF

NOTE: (1) All output pins except for host interface signals
(2) Host interface outputs
(*) IOL = 4 mA for RG and WG

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AC CHARACTERISTICS

The following timings assume that all non-Host Bus output pins will drive one Schottky TTL load in parallel with 50 pF, all Host Bus output pins will drive a 300 pF load, and all inputs are at TTL levels. The MIN and MAX timings conform to the operating ranges of a power supply voltage of 5V ±5%, and an ambient temperature of 0°C to 70°C.

Host DMA 8/16-Bit Interface Timing Parameters (Figure 2)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
DREQL	DREQ low from $\overline{DACK}$ low				80	ns
RDTA	$\overline{IOR}$ low to HD [0:15] valid				60	ns
RDHLD	$\overline{IOR}$ high to HD [0:15] tri-state		0		20	ns
WDS	HD [0:15] setup to $\overline{IOW}$ high		40			ns
WDHLD	HD [0:15] hold from $\overline{IOW}$ high		10			ns
RWPULSE	$\overline{IOR}$/$\overline{IOW}$ pulse width		80			ns

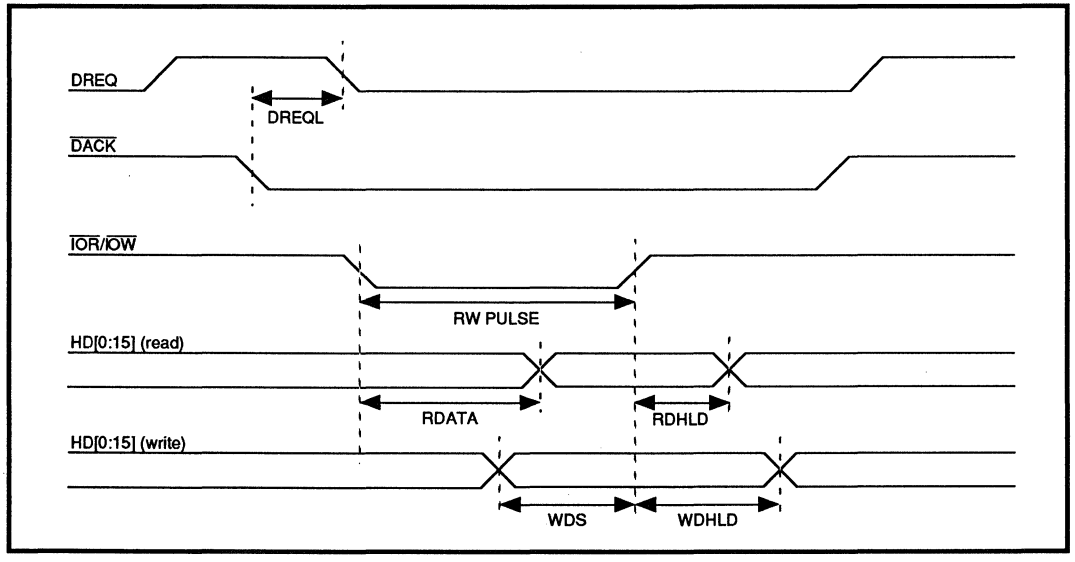

FIGURE 2: Host DMA 8/16-Bit Interface Timing

HOST Programmed I/O 8-16-Bit Timing Parameters (Figure 3)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
CS16L	$\overline{HCS0}$ low, A0:2, A9 low, or $\overline{HCS1}$ high to $\overline{IOCS16}$ low				20	ns
IOCHL	$\overline{IOR}$/$\overline{IOW}$ low to $\overline{IOCHRDY}$ low				25	ns
IOCHTW*	$\overline{IOCHRDY}$ pulse width		0		5xBCLK	ns
RDTA	$\overline{IOR}$ low to HD[0:15] valid				60	ns
RDHLD	$\overline{IOR}$ high to HD[0:15] tri-state		0		20	ns
WDS	HD [0:15] setup to $\overline{IOW}$ high		40			ns
WDHLD	HD[0:15] hold from $\overline{IOW}$ high		10			ns
RWPULSE	$\overline{IOR}$/$\overline{IOW}$ pulse width		80			ns
ADRSET	$\overline{HCS0}$, A0:2, A9/$\overline{HCS1}$, setup to $\overline{IOR}$/$\overline{IOW}$ low		25			ns
ADRHLD	$\overline{HCS0}$, A0:2, A9/$\overline{HCS1}$ hold, from $\overline{IOR}$/$\overline{IOW}$ high		10			ns

*Maximum specification applies when Auto Wait State Generation is disabled (Register 58H, Bit 2 is reset.)

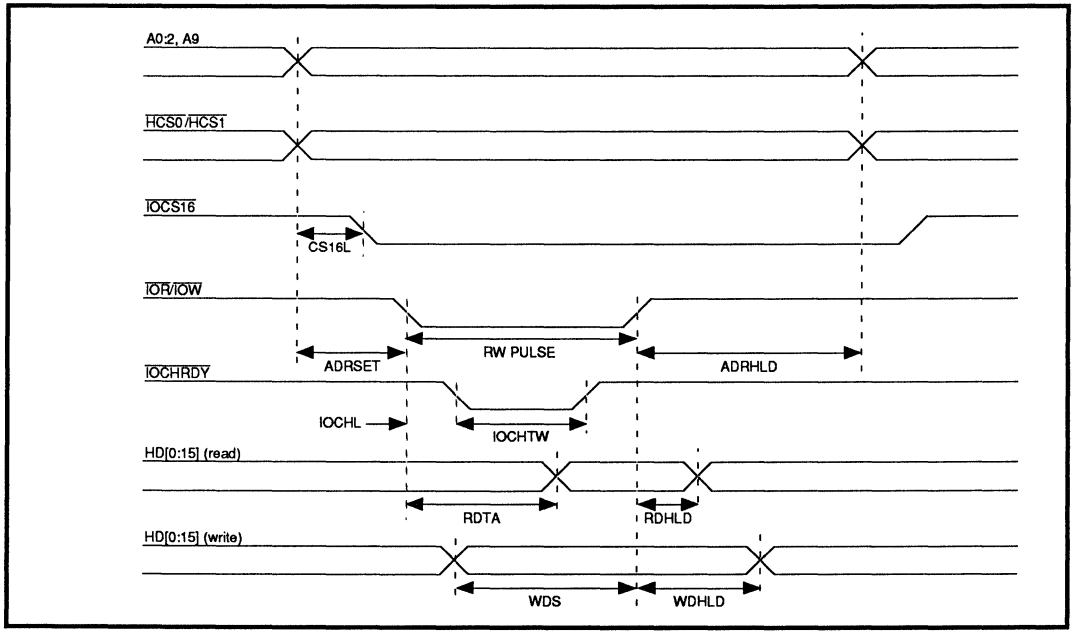

FIGURE 3: Host Programmed 8/16-Bit Timing

Microcontroller Interface Timing Parameters (Figures 4 and 5)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Ta	ALE Width		45			ns
Taw	ALE↓to $\overline{\text{WRITE}}$ ↓		25			ns
Tar	ALE↓to $\overline{\text{READ}}$ ↓		25			ns
Tw	$\overline{\text{WR}}$ Width		140			ns
Tr	$\overline{\text{RD}}$ Width		140			ns
As	Address AD [0:7] valid to ALE↓		5			ns
Ah	ALE↓to Address AD [0:7] invalid		20			ns
Cs	ALE↓to CS valid				5	ns
Ch	$\overline{\text{RD}}$↑or $\overline{\text{WR}}$↑to CS↓		0			ns
Wds	Write Data AD [0:7] valid to $\overline{\text{WR}}$ ↑		55			ns
Wdh	$\overline{\text{WR}}$↑to Write Data AD [0:7] invalid		10			ns
Tda	$\overline{\text{RD}}$↓to Read Data AD [0:7] valid				100	ns
Tdh	$\overline{\text{RD}}$↑to Read AD [0:7] float (undriven)				50	ns

NOTE: ↓Indicates falling edge. ↑ Indicates rising edge.

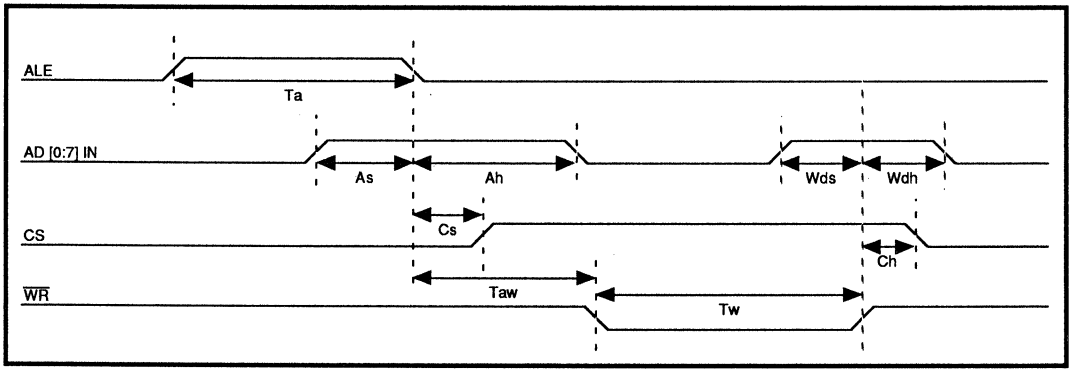

FIGURE 4: Register Write Timing

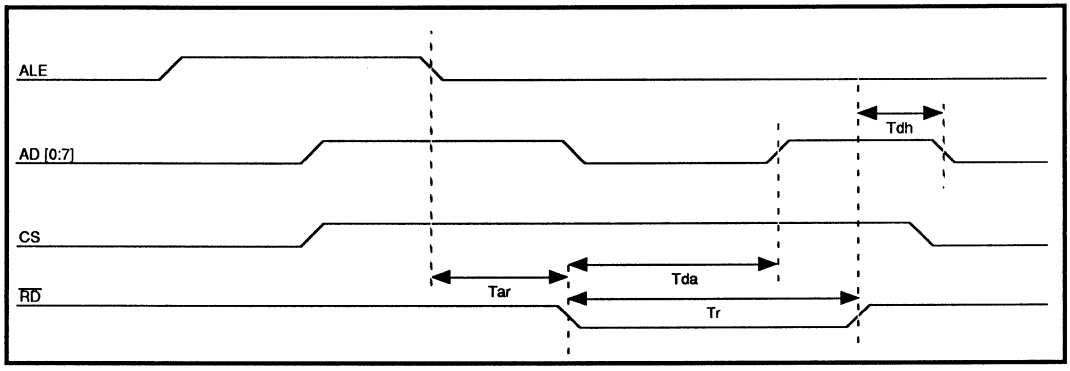

FIGURE 5: Register Read Timing

NRZ - Test Input/Output. Timing Parameters (Figures 6 and 7).

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
T	RD/REF CLK Period					ns
T/2	RD/REF CLK High/Low Time		23			ns
Tr = Tf	RD/REF CLK Rise and Fall time				5	ns
Ds	NRZ_TEST valid to RD/REF CLK ↑		15			ns
Dh	RD/REF CLK↑to NRZ invalid		10			ns
As*	$\overline{AMD}$ valid to RD/REF CLK ↑		15			ns
Dv	RD/REF CLK↑to NRZ		10		40	ns

NOTE: ↓ Indicates falling edge. ↑ Indicates rising edge.

* These specifications are only applicable in the Soft Sector Mode.

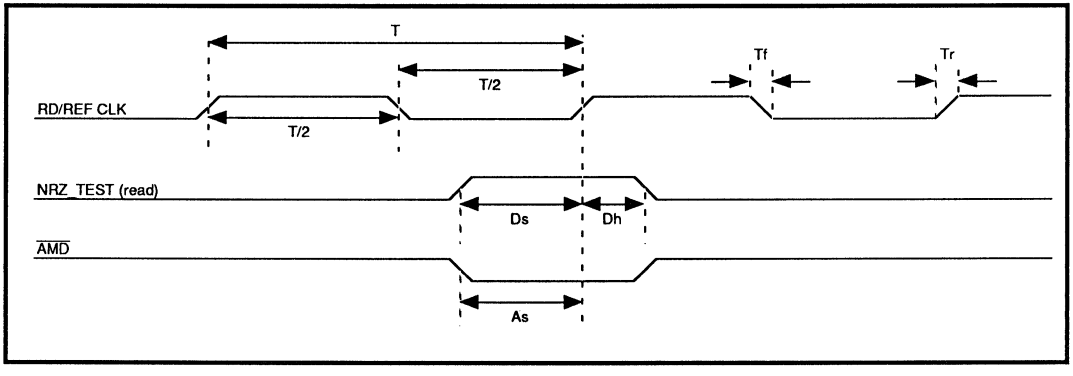

FIGURE 6: NRZ Test Input Timing

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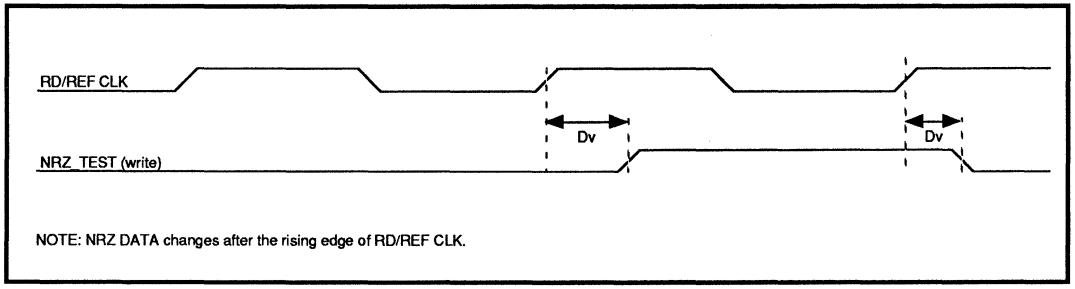


FIGURE 7: NRZ Test Output Timing

Register 70H Access Timing Parameters (Figures 8 and 9)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
To	$\overline{RD}$↓to $\overline{MOE}$ ↓				40	ns
Tda	BD[0:7] valid to AD[0:7] valid				55	ns
Trh	$\overline{RD}$↑to AD[0:7] invalid				50	ns
Toh	$\overline{RD}$↑or $\overline{WR}$↑to $\overline{MOE}$ ↑				40	ns
Taw	AD[0:7] valid to $\overline{WE}$ ↓				55	ns
Tao	AD[0:7] valid to $\overline{MOE}$ ↓				55	ns
Tad	AD[0:7] valid to BD[0:7] valid				55	ns
Twwh	$\overline{WR}$↑to $\overline{WE}$ ↑				40	ns
Twdh	$\overline{WR}$↑to BD[0:7] invalid		50			ns

NOTE: ↓ Indicates falling edge. ↑ Indicates rising edge.

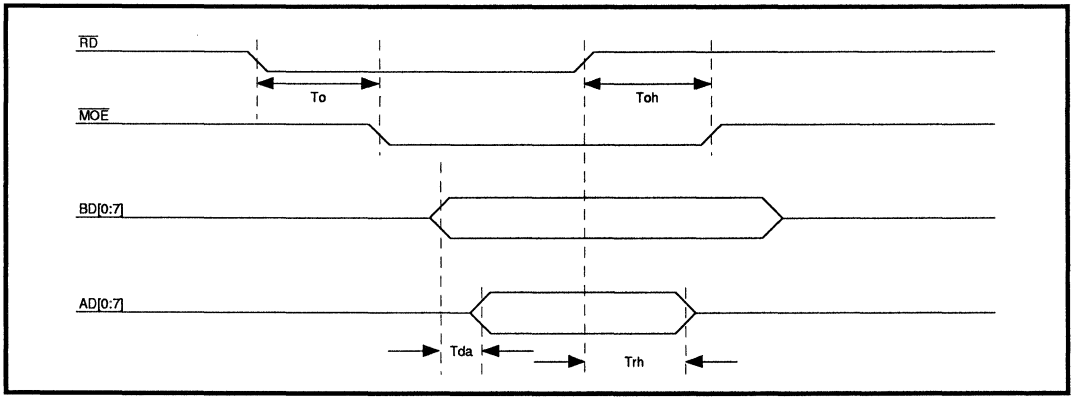


FIGURE 8: Register 70H Read Timing

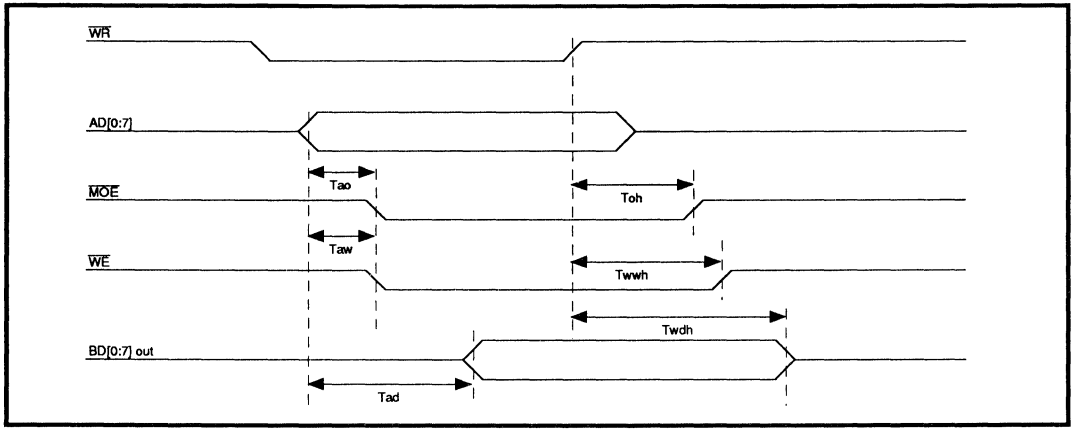


FIGURE 9: Register 70H Write Timing

Buffer Memory Read/Write Timing Parameters (Figure 10)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
T_B	BCLK Period		41			ns
$T_B/2$	BCLK High/Low Time		16			ns
$T_{Br}=T_{Bf}$	BCLK Rise and Fall Time				5	ns
T1	BUFCLK* Period		125			ns
Av	BUFCLK*↓to BA[0:15] valid				65	ns
Dov	BUFCLK*↑to BD[0:7] valid				50	ns
Doh	BUFCLK*↑to BD[0:7] invalid		0			ns
Mv	BUFCLK*↑to $\overline{MOE}$ ↓				30	ns
Mh	BUFCLK*↓to $\overline{MOE}$ ↑		10		35	ns
Wv	BUFCLK*↑to $\overline{WE}$ ↓				30	ns
Wh	BUFCLK*↓to $\overline{WE}$ ↑		5		30	ns
Dma	$\overline{MOE}$ ↑to BA[0:15] Hold		10		30	ns
Dis	BD[0:7] valid to BUFCLK*↓		5			ns
Dih	BUFCLK*↓to BD[0:7] invalid		10			ns
TBbr	BCLK↑to BUFCLK↑				24	ns
TBbf	BCLK↓to BUFCLK↓				21	ns

NOTE: ↓Indicates falling edge. ↑ Indicates rising edge.

* BUFCLK is an internal signal which indicates the period of Buffer Memory Access Cycle. These specifications can be tested when the period of BCLK pin is the same as the period of Buffer Memory Access Cycles (i.e., Register 7FH, Bits 6 and 7 are 1 and 0, respectively). If the Buffer Memory Access Cycle period is programmed to be a multiple of the period of BCLK pin, BUFCLK above refers to the Buffer Memory Access Cycles and the falling edge referred to above would be coinciding with the rising edge of the BCLK pin.

RLL ENDEC Timing Parameters (See Figures 11 and 12.)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
TSWD	Write data output setup time		3		15	ns
THWD	Write data ouput hold time		3		15	ns
TWLE	$\overline{\text{EARLY}}/\overline{\text{LATE}}$ ouput setup or hold time		3		15	ns
TRRCP	RRCLK pulse with		20			ns
TRCRD	SRD leading edge to next RRCLK transition		10			ns
TRDRC	RRCLK transition to next leading SRD egde		5			ns
TSDI	SDI low pulse width		25			ns

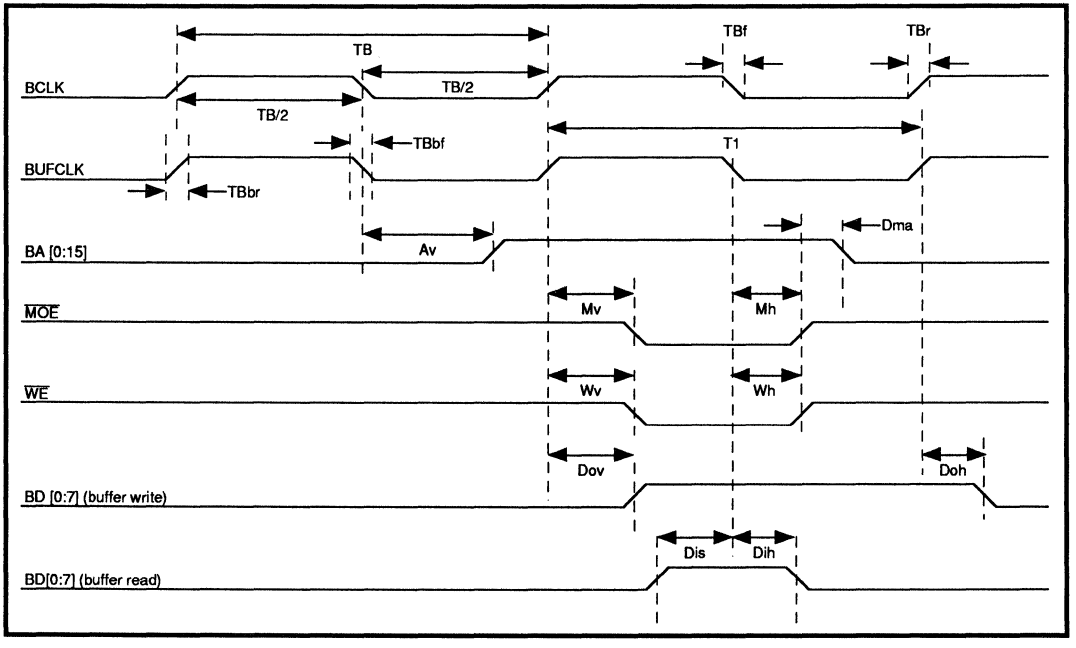


FIGURE 10: Buffer Memory Read/Write Timing

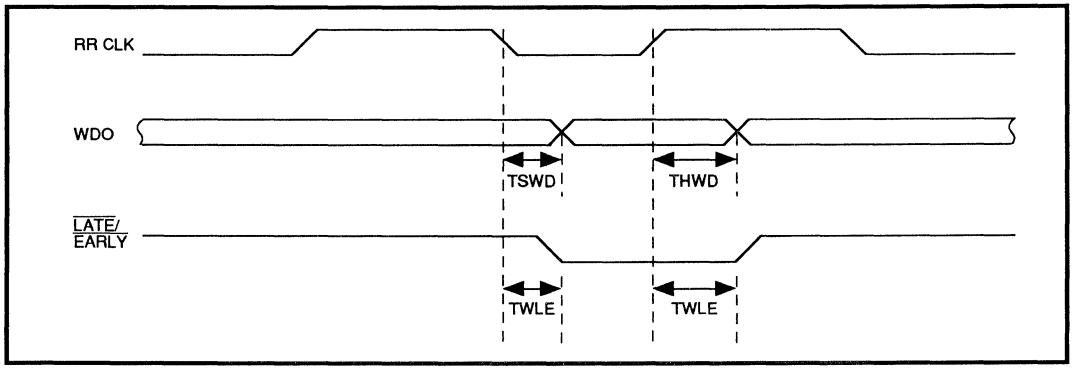


FIGURE 11 : Write Data Timing - RLL ENDEC Mode

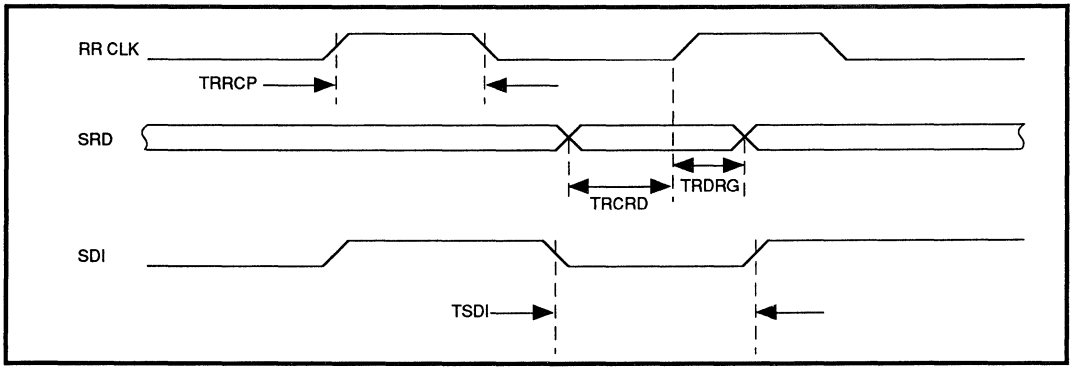
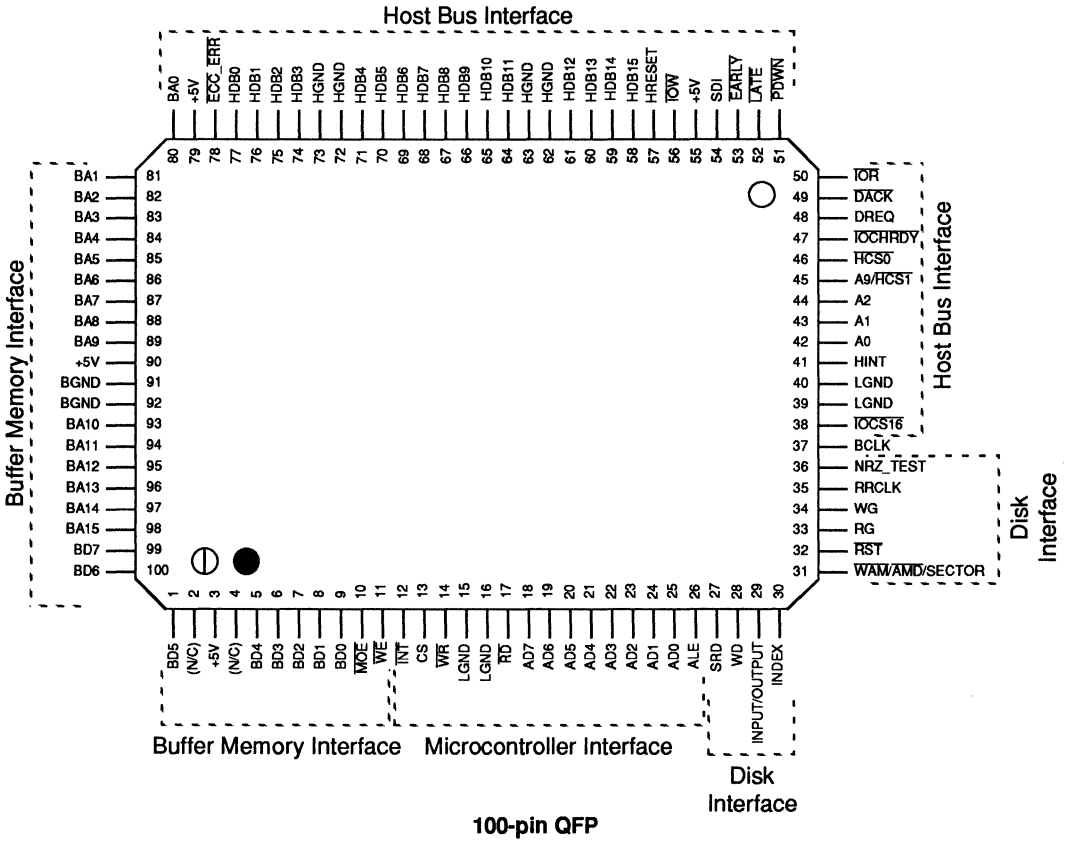


FIGURE 12 : Read Data Timing - RLL ENDEC Mode

SSI 32C261
PC AT/XT Combo Controller
With RLL (2, 7) ENDEC

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



100-pin QFP

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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silicon systems®
A TDK Group Company

SSI 32C263
PC AT/XT Combo Disk Controller
16 Mbit/s, 3V Operation
Advance Information

December 1991

DESCRIPTION

The SSI 32C263 is a CMOS VLSI device which integrates major portions of the hardware needed to build a PC AT/XT driven hard disk drive. The SSI 32C263 is one of the family of Silicon Systems' single chip disk controllers. The SSI 32C263's place in the Silicon Systems' chip family is illustrated in the hierarchy chart in Figure 1. It provides most of the functional circuitry necessary to build a 3V "ATA" embedded disk.

The SSI 32C263 is capable of supporting interleaved data transfer rate up to 16 Mbit/s. It includes a dual port Buffer Manager, a storage controller, and a high performance AT/XT host interface block that incorporates an extensive hardware support — including 24 mA drivers — for the PC AT/XT and other compatible interfaces.

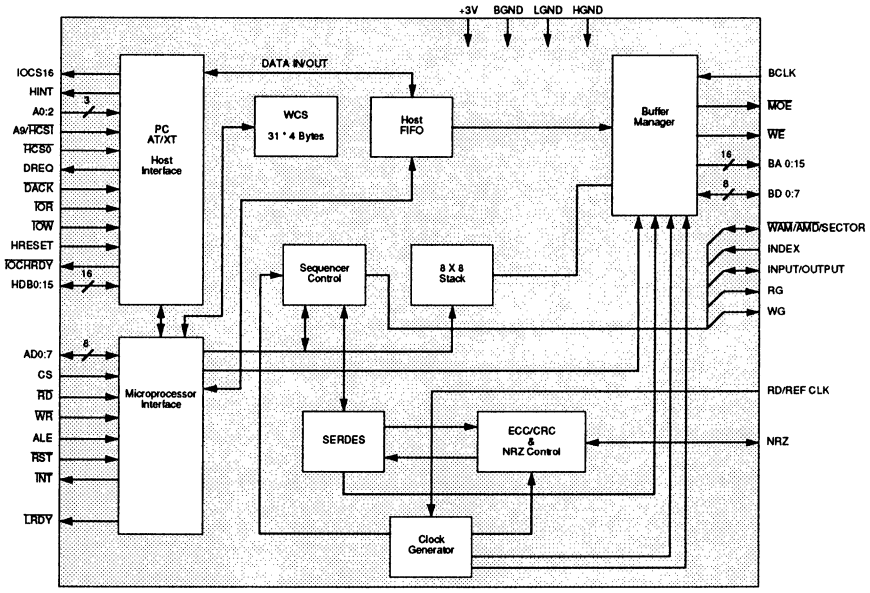
The SSI 32C263 performs all the controller functions for the peripheral device, such as serialization/deserialization; ECC generation and checking on the data stream, and CRC generation and checking on the header of the data stream.

FEATURES

- **PC AT/XT Bus Interface**
  - **Single Chip PC AT/XT Controller**
  - **Direct bus interface logic with on-chip 24 mA drivers**
  - **Logic for daisy chaining 2 embedded ATA drives**
  - **Buffer transfer in single or burst mode DMA or PIO modes**
  - **Provides logic to speed up command response**
  - **Supports 16 Mbit/s concurrent disk transfer on a 1.5M words/s PC-AT without wait states**

(Continued)

BLOCK DIAGRAM



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SSI 32C263
PC AT/XT Combo Disk Controller
16 Mbit/s, 3V Operation

FEATURES (continued)

- Buffer Manager
  - Dual port buffer access with access priority resolver
  - Total Buffer Memory throughput to 5 MByte/s
  - Direct Buffer Memory addressing up to 64 kB Static RAM
  - 4k Buffer segmentation support
  - Provides host overrun control
- Storage Controller
  - NRZ Data Rates up to16 Mbit/s
  - Selectable 16-bit CRC or 32/56 bit ECC polynomial with hardware correction circuitry
  - Microprocessor based split data field processing logic
  - Highly programmable advanced sequencer organized in 31 x 4 bytes
  - 8-byte stack for header information storage
  - Supports programmable sector lengths up to a full track
  - Two-Index counter providing sector I.D. search and retry limits
  - Preset of CRC/ECC generator to either "0's" or "1's"
- Microprocessor Interface
  - Programmable wait state insertion for fast microprocessors
  - Provides microprocessor access to 8 external switch settings
  - Interrupt or polled microprocessor interface
- Others
  - Internal power down mode
  - Operational from 2.7 to 5.5V
  - Plug and play compatible with the Cirrus Logic SH-260, SH-265 and the SH-266
  - Available in 100-pin surface mount QFP

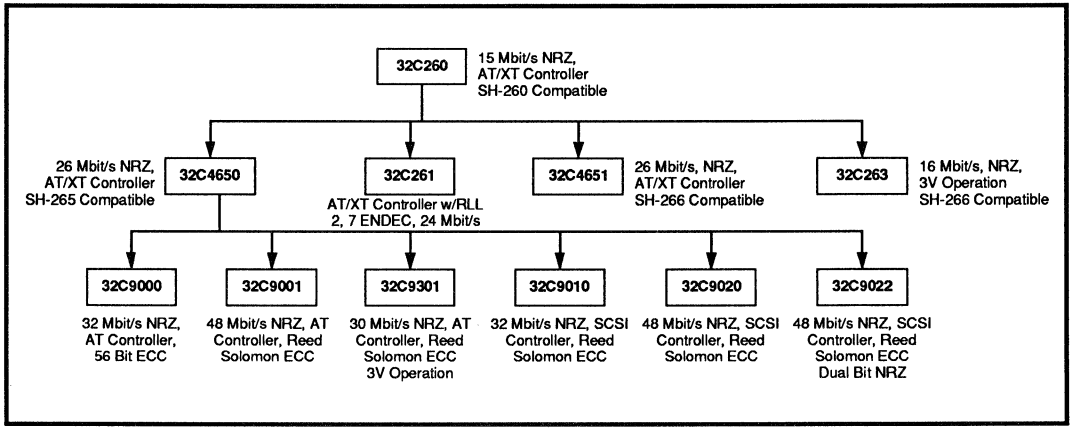

FIGURE 1: Silicon Systems' Disk Controller Chip Hierarchy

FUNCTIONAL DESCRIPTION

The four major functional blocks are:

Microcontroller Interface
Buffer Memory Interface
Disk Formatter
Host Interface

The SSI 32C263 includes a control sequencer with a writeable control store, buffer RAM controller capable of interleaved address generation, direct ATA bus connections, and configuration/status registers which can be programmed by an external microcontroller. The internal hardware also supports automatic looping of the sequencer program, and the interrupt circuitry relieves the supervising microprocessor of having to poll on the status registers. Access to the control store and registers is accomplished through the microprocessor interface which is optimized for eight-bit, mulitplexed address/data processors. **For a complete description of the programmable registers, refer to the SSI 32C4651 Design Guide.**

The device performs all the controller functions for the peripheral device, such as serialization/deserialization; ECC generation, checking, and correction assistance; and CRC generation and checking on the header stream. The contention between the host and the disk requests for buffer RAM access is internally arbitrated and resolved.

PIN DESCRIPTION

The following convention is used in the pin description:

(I) denotes an input
(I/S) denotes a Schmitt trigger input
(O) denotes an output
(I/O) denotes a bidirectional signal
(Z) denotes a tri-state output
(OD) denotes an open drain output

Active low signals are denoted by a bar on top of the signal name and dual function pins are denoted with a slash between the two signals: A9/$\overline{HCS1}$, for example.

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GENERAL

NAME	TYPE	DESCRIPTION
VDD		POWER SUPPLY PIN, VCC
GND		GROUND

HOST INTERFACE

A0:2	I	HOST ADDRESS LINES. The Host Address lines A(2:0) and A9 are used to access the various PC/AT control/status, and data registers.
A9/$\overline{HCS1}$	I	HOST ADDRESS LINE 9/ HOST CHIP SELECT 1. This is a multiplexed input pin. When Register 52H, bit 3 is reset this input is HOST ADDRESS LINE 9, when the bit is set this input is HOST CHIP SELECT 1. When configured as $\overline{HCS1}$ this input is ignored when $\overline{DACK}$ is asserted.
$\overline{HCS0}$	I	HOST CHIP SELECT 0. This pin selects access to the control, status and data registers. This input is ignored when $\overline{DACK}$ is asserted.
$\overline{IOCS16}$	OD	16-BIT DATA TRANSFER. An open drain output when active low indicates that a 16-bit buffer transfer is active.
HINT	O	HOST INTERRUPT. Asserted active high to indicate to the Host that the controller needs attention.
$\overline{IOCHRDY}$	O, Z	I/O CHANNEL READY. Asserted active low whenever the internal host FIFO is not ready to transfer data.

PIN DESCRIPTION (Continued)

HOST INTERFACE (Continued)

NAME	TYPE	DESCRIPTION
DREQ	O, Z	DMA REQUEST. The DMA Request signal is asserted active high during DMA transfer between the Host and the SSI 32C4651.
$\overline{\text{DACK}}$	I	DMA ACKNOWLEDGE. This signal is asserted low by the host during DMA to complete the DMA handshake for data transfer between the host and the controller.
$\overline{\text{IOR}}$	I	INPUT READ SELECT. This pin is asserted active low by the Host during a Host read operation. When asserted with $\overline{\text{HCS0}}$, $\overline{\text{HCS1}}$, or $\overline{\text{DACK}}$, data from the device is enabled onto the host data bus.
$\overline{\text{IOW}}$	I	INPUT WRITE SELECT. Asserted active low by the HOST during a HOST write operation. When asserted with $\overline{\text{HCS0}}$, $\overline{\text{HCS1}}$, or $\overline{\text{DACK}}$, data from the host data bus is strobed into the device.
HRESET	I/S	HOST RESET. This signal, when asserted active high, stops all commands in progress and initializes the control/status registers — see Design Guide for Register Reset conditions. This signal can also "wake up" the device while it is in power down mode.
HDB (15:0)	I/O	HOST DATA BUS. These bits are used for word transfers between the Buffer Memory and the Host; bits (7:0) are also used for status, commands, or ECC byte transfers.

DISK INTERFACE

INDEX	I	INDEX. This input is a pulse that occurs once per revolution and defines the start of sector 0.
INPUT/ OUTPUT	I/O	DISK SEQUENCER INPUT/OUTPUT. A general purpose control (output) and status (input) pin configured by the Output Enable Bit of Sequencer Mode Selection Register 77H, bit 6. At power-on, this pin is an input. As an input, it can be used to synchronize the disk sequencer to an external event. The state of this pin is sampled by reading Formatter interrupt Enable Register 7EH, bit 2. As an output, it is controlled by bit 2 of the Control Field of the disk sequencer.
$\overline{\text{WAM}}$/$\overline{\text{AMD}}$ SECTOR	I/O	WRITE ADDRESS MARK/SECTOR/ADDRESS MARK DETECT. This pin is configured to operate in Hard or Soft Sector mode by initializing the Formatter Mode Selection Register: 77H, bit 7. In the hard sector mode it is used as the sector input — a pulse on this pin indicates a sector mark is found. In the soft sector mode, a one-bit wide active low output pulse is asserted when formatting to allow writing of address mark. When reading, an active low input indicates an address mark was detected. The device powers up in soft sector mode.
RG	O	READ GATE. This output enables the reading of the disk. It is asserted active high at the beginning of the PLO for header and data field by the sequencer Control Field bit 6. It is automatically deasserted at the end of the CRC or ECC, when the sequencer processes servo gaps between data fragments, or when the sequencer goes to the stopped state.
WG	O	WRITE GATE. This active high output enables writing onto the disk. It is asserted and deasserted by the sequencer Control Field bits 5 and 7.
RRCLK	I	READ/REFERENCE CLOCK. This pin is used in conjunction with the NRZ pin to clock data in and out of the SSI 32C4651 device. This input must be glitch-free to ensure correct operation of the chip.
NRZ	I/O	NON RETURN TO ZERO. This signal is the serial read data input from the disk drive when the read gate signal is asserted; it is the write data output to the disk drive when the write gate signal is asserted.

MICROPROCESSOR INTERFACE

NAME	TYPE	DESCRIPTION
$\overline{RST}$	I/S	RESET. An active low input generates a component reset that holds the internal registers of the SSI 32C263 at reset, stops all operations within the chip, and deasserts all output signals. All input/output signals and Host outputs are set to the high-Z state.
ALE	I/S	ADDRESS LATCH ENABLE. This control signal latches the address on the AD 7:0 lines.
CS	I/S	CHIP SELECT. This active high signal must be asserted for all microprocessor accesses to the registers of this chip.
$\overline{WR}$	I/S	WRITE STROBE. Active low $\overline{WR}$ and CS assertion causes the data to be written into the specified registers from the AD lines.
$\overline{RD}$	I/S	READ STROBE. Active low assertion $\overline{RD}$ and CS causes the data from the specified register to be driven on the AD 7:0 lines.
$\overline{INT}$	O,OD	INTERRUPT. An active low signal which indicates the controller is requesting microprocessor service. This signal is programmable for either a push-pull with an internal pull up resistor or open-drain output circuit. This signal powers up in the high-Z state. Formatter Mode Selection Register, 77H: bit 4 set high, disables the pullup on the output pin, leaving an open drain output. This is intended to support multiple interrupt sources.
AD7:0	I/O	ADDRESS/DATA BUS. These lines make up the multiplexed, bidirectional data path to the microprocessor. ALE latches register address from this bus with data transferred during $\overline{RD}$ or $\overline{WR}$ assertion.
$\overline{LRDY}$	O	LOCAL MICROPROCESSOR READY: When this signal is deasserted low, the microprocessor inserts wait states to allow time for the chip to respond to the access. Wait states are programmed by Auxiliary Control 1 Register — 4FH: bits 7-6.

BUFFER MANAGER INTERFACE

BA0:15	O	BUFFER MEMORY ADDRESS LINES 0:15. These sixteen outputs provide address lines for the static memory chips used to implement the buffer memory.
BD0:7	I/O	BUFFER MEMORY DATA BUS. 7 through 0. The bidirectional Data Bus connects the buffer RAM to the buffer manager. This bus is designed for high speed data transfer.
$\overline{MOE}$	O	MEMORY OUTPUT ENABLE. This active low output controls the enabling of data onto the Data Bus from the RAMs. It can also be programmed to control the RAM chip enable.
$\overline{WE}$	O	WRITE ENABLE. This active low output signal is used to strobe the data into the RAMs from the Data bus.
SYSCLK	I	SYSTEM CLOCK. This signal is used to synchronize the buffer RAM access, including the generation of memory address lines, write enable $\overline{WE}$, and memory output enable $\overline{MOE}$. In power down mode, this signal is shut off from the internal logic and hence buffer memory access is inhibited.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Maximum limits indicate where a permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Electrical Characteristics.

PARAMETER	RATING
Power Supply Voltage, VCC	7V
Ambient Temperature	0 to 70°C
Storage Temperature	-65 to 150°C
Input, Output pins	-0.5 to VCC+0.5V

DC ELECTRICAL CHARACTERISTICS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
VCC	Power Supply Voltage		2.7		3.9	V
ICC	Supply Current	Operating			TBD	mA
ICCS	Supply Current	Note 1			TBD	µA
VIL	Input Low Voltage		-0.5		0.5	V
VIH	Input High Voltage		1.8		VCC +0.5	V
VIL	Input Low Voltage	Schmitt triggered signals	-0.5		0.9	V
VIH	Input High Voltage	Schmitt triggered signals	1.9		VCC +0.5	V
VOL	Output Low Voltage	Note 2			0.3	V
VOL	Output Low Voltage	Note 3			0.4	V
VOH	Output High Voltage	IOH = -400 µA	2.0			V
IL	Input Leakage Current	0 < VIN < VCC	-10		10	µA
CIN	Input Capacitance				10	pF
COUT	Output Capacitance				10	pF

Note: (1) In powered down, sleep mode
(2) All interface pins except Host Interface pins. IOL= 2mA.
(3) Host Interface pins, IOL=24mA.
(4) Schmitt triggered signals

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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A TDK Group Company

SSI 32C4650
PC AT/XT Combo Controller

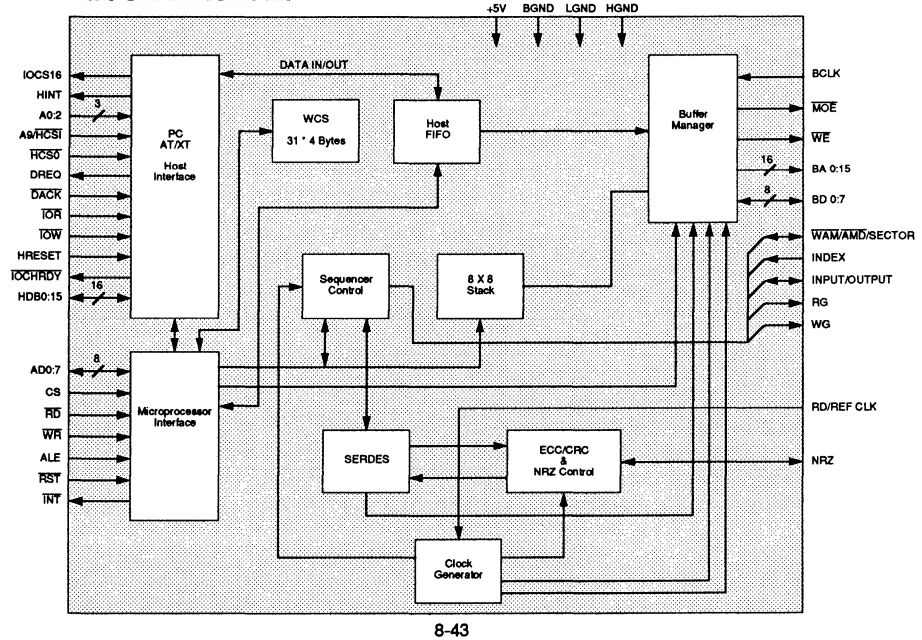
Advance Information

September 1991

FEATURES

- PC AT/XT Bus Interface
  - Single Chip PC AT/XT Controller
  - Supports ST506/412, ST412HP, ESDI, and SMD disk interfaces
  - Direct bus interface logic with on-chip 24 mA drivers
  - Logic for daisy chaining 2 embedded controller drives on a PC AT
  - Supports 15 Mbit/s concurrent disk transfer on a 12 MHz PC AT without wait states
- Buffer Manager
  - Supports Buffer Memory throughput to 8 Mbytes/s
  - Direct Buffer Memory addressing up to 64 kB static RAM
  - Dual port circular buffer control
  - Internal dividers for Buffer Clock include 1, 2, 3, and 4
- Storage Controller
  - NRZ Data rate up to 25 Mbit/s
  - Selectable 16-bit CRC or 56-bit ECC polynomial with fast hardware correction circuitry
  - Supports sector level defect management
  - Supports 1:1 interleaved operation
- Microprocessor Interface
  - Supports both Intel 8051, and Motorola 68HC11 family of microprocessors
  - Interrupt or polled microprocessor interface
  - Power down capability when idle, automatic power up when command is received
- Others
  - Low power CMOS technology
  - Plug and Play compatible with Cirrus CL-SH 260 chip
  - Available in 84-pin PLCC or 100-pin QFP

BLOCK DIAGRAM



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SSI 32C4650
PC AT/XT Combo Controller

DESCRIPTION

The SSI 32C4650 is a CMOS VLSI device which integrates the major portion of the hardware needed to build a PC AT/XT driven hard disk controller. The 32C4650 is capable of supporting interleaved data transfer rate up to 25 Mbit/s. This chip represents a major reduction in part count when used with the SSI 32P4620, Pulse Detector and Data Separator combo chip, and the SSI 32R4610, Read/Write device and the SSI 32H4631, Servo and Motor Speed Controller device, implementing a powerful and cost efficient 4-chip set hard disk drive solution. It also has the flexibility to be used as a stand-alone combo controller.

The SSI 32C4650 includes all the circuitry for a direct connection to an AT/XT bus interface, a dual port Buffer Manager, a storage controller and an extensive hardware support, including 24 mA drivers, for the PC AT/XT and other compatible interfaces.

The SSI 32C4650 performs all the controller functions for the peripheral device, such as serialization/ deserialization, ECC generation and checking on the data stream, and CRC generation and checking on the header of the data stream.

FUNCTIONAL DESCRIPTION

The major functional elements and data paths of the SSI 32C4650 are shown in the block diagram.

The four major functional blocks are:

Buffer Memory Interface,

Microcontroller Interface,

Disk Formatter,and

Host Interface.

The SSI 32C4650 performs the functions to interface a serial data storage device such as a Winchester Disk Drive, to a parallel bus interface for data processing on a byte wide basis. The functions necessary to accurately make this conversion are serialization/ deserialization, error detection and correction, and data path control. The SSI 32C4650 also has a general purpose interface line to further facilitate control of the data storage device or parallel interface. An eight byte stack allows data to be saved and reviewed by the microprocessor for error handling purposes. The internal sequencer performs most of the operations in conjunction with the control and status registers. The sequencer program is contained in an internal sequencer RAM, which is easily (re)programmed providing almost infinite flexibility in drive format and control features. A microprocessor effects both initialization and control of the SSI 32C4650 by writing to and reading from the internal registers, sequencer RAM, stack and general purpose I/O circuitry. The microprocessor interface block of the SSI 32C4650 provides the communication and control for the SSI 32C4650 to the microprocessor. **For a complete description of the programmable registers, refer to the SSI 32C4650 Design Guide.**

BUFFER MEMORY INTERFACE

The buffer memory interface, referred to as the Buffer Manager includes a bi-directional data bus that exchanges data bytes between an external buffer memory and the serializer/deserializer or the host interface. The circuitry allows the use of static RAM as a dual port circular FIFO, and supervises data transfers to and from the RAM. The device contains logic that resolves disk and host requests. The arbitration is achieved by giving priority to the disk and utilizing internal data FIFO's for temporary host and disk data storage.

The Buffer Manager is capable of handling buffer sizes from 256 bytes to 64K bytes. The circuit provides up to 16 direct address signals, along with Memory Output Enable ($\overline{MOE}$) and Write Enable ($\overline{WE}$) signals. The buffer RAM address is generated from one of two 16-bit counters, one of which being the write address pointer (5CH & 5DH) and the other the read pointer (5AH & 5BH). The address generation as well as the memory control signals are synchronous to the Buffer Clock (BCLK), allowing the user many choices of buffer RAM speeds, with different combinations of the disk and host transfer rates.

The Buffer Memory Interface is a dual port buffer controller that allows low speed static RAM's to be configured as a dual port circular FIFO buffer. It generates all the buffer memory addressing required and manages two ports: Port A, a synchronous peripheral device interface and Port B, an asynchronous host interface. The Buffer Manager has arbitration logic to support the AT or XT host transfers under DMA control or Programmed I/O control.

On-chip counters generate the addresses (BA0-BA15) needed to access up to 64K of external static RAM. Along with the addresses, the Buffer Manager block outputs a Memory Output Enable ($\overline{MOE}$) and a Write Enable ($\overline{WE}$) signal for a static RAM buffer.

The address generator contains two 16 bit pointers, the read address pointer (RAP) and the write address pointer (WAP), which indicate where in the external buffer RAM data is to be read or written. During data transfers, these pointers are automatically incremented as the RAM is accessed. The pointers wrap around to 0 when the programmed buffer size is exceeded. To prevent host overruns of the buffer (caused by one of the pointers overtaking the other), the address generator includes a 16-bit stop pointer (5EH & 5FH). The microprocessor loads SP with the last address in buffer memory to be accessed during a host DMA transfer. When the port B address (RAP during an upload to the host or WAP during a download to the peripheral) reaches the value in SP, the DMA transfer is automatically suspended.

The period of the Buffer Memory access cycle is determined by programming bits 6 and 7 of CLOCK CONTROL, register 7FH, and is based on the BCLK input. The period of the Buffer Memory access cycle determines the access time requirement for the buffer RAMs. The C260 samples the data from the RAM at the falling edge of the BCLK signal. Buffer Memory throughput and the RAM speeds can be determined from the following equations:

Buffer Memory Throughput =

1 / Period of Memory Access Cycle

For Buffer Memory Read:

Max. Read Access Time = $T_1 - Av_{max} - Dis_{min}$

Min. Output Enable = $(T_1/2) - Mv_{max} - Dis_{min}$

For Buffer Memory Write:

Address set up to $\overline{WE}\uparrow = T_1 - Av_{max} + Wh_{max}$

Data set up to $\overline{WE}\uparrow$ = Min. Output Enable
$= (T_1/2) - Mv_{max} - Dis_{min}$

Note: For an explanation of Av_{max}, Dis_{min}, Mv_{max}, Wh_{max}, Dov_{max} parameters, refer to Buffer Memory Read/Write Timing Parameters.

MICROPROCESSOR INTERFACE

The microprocessor interface decodes microprocessor read and write requests and provides access to the appropriate register or internal memory location. Since both data and address information are carried on the multiplexed bus lines AD0-AD7, address information is latched from the bus on the falling edge of the microprocessor signal, Address Latch Enable (ALE). When CS is asserted along with either $\overline{RD}$ or $\overline{WR}$, the register whose address was previously latched is selected. The addresses and names of all the accessible registers are shown in the Register Address Map. The microprocessor should not read or write the sequencer RAM while the sequencer is running, since there is no circuitry to resolve conflicting accesses and incorrect sequencer operation will result.

The status and control registers make status information available to the microprocessor and allow the device to be configured for a wide variety of peripheral applications. The microprocessor can monitor the status of transfers in progress and control the ECC register operation, the ECC polynomial, the clock generation hardware, the sequencer program execution, buffer size, read and write pointers, and stop pointers. The microprocessor also has access to the sequencer's microprogram RAM so that it loads the microcode for all controller operations.

DISK FORMATTER

The serializer/deserializer circuit interfaces the parallel buffer memory bus to serial NRZ data stream of the peripheral device. Byte synchronization is maintained with a bit ring, which is an 8-bit recirculating shift register clocked by the peripheral bit clock. During a sector write, the bit ring is initialized explicitly with a sequencer instruction. The bit ring continues to operate until the end of the field (ECC written or read). During write operations, the sequencer may cause address marks and sync patterns to be loaded into the serializer instead of data bytes. These special patterns are contained in a sequencer instruction and are transferred to the serializer over an internal byte wide data path. During read operations, bytes of overhead information may be routed to the stack or sequencer for comparison against target values. This process is controlled by the control field (SEQCONF) in each sequencer instruction.

The eight byte recirculating stack may be used to capture read data for later examination by the microprocessor. Data is pushed onto the stack under se-

quencer control. The control bit STACKEN in the sequencer instruction field SEQCONF in the sequencer instruction field SEQCONF directly controls the stack. If more than 8 bytes are written to the stack, only the last 8 will be saved. When a data byte is read from the top of the stack by the microprocessor via the STACK register, the data is recirculated to the bottom of the stack, allowing the stack contents to be examined more than once without the use of temporary storage in the microprocessor or buffer.

Serial peripheral data is passed through a variable length shift register with programmable exclusive OR feedback that performs ECC or CRC generation and checking. The feedback taps for the desired polynomials are fixed as follows and the user may select between the 16-bit CRC, 32-bit ECC, or the 56-bit ECC as desired. This selection is accomplished by programming the WCS COUNT FIELD and the ECC CONTROL register (Register 71H, bit 6).

In the forward direction, the options available include:

CRC polynomial which is the CCITT CRC code:

$x^{16} + x^{12} + x^5 + 1$

32-bit ECC polynomial:

$x^{32} + x^{28} + x^{26} + x^{19} + x^{17} + x^{10} + x^6 + x^2 + 1$

56-bit ECC polynomial:

$x^{56} + x^{52} + x^{50} + x^{43} + x^{41} + x^{34} + x^{30} + x^{26} + x^{24} + x^8 + 1$

The reverse polynomial options include:

32-bit ECC polynomial:

$x^{32} + x^{30} + x^{26} + x^{22} + x^{15} + x^{13} + x^6 + x^4 + 1$

56-bit ECC polynomial:

$x^{56} + x^{48} + x^{32} + x^{30} + x^{26} + x^{22} + x^{15} + x^{13} + x^6 + x^4 + 1$

The 56-bit polynomial can detect single burst errors up to 56 bits in length, and double-burst errors, where the combination of bursts is less than or equal to 41 bits. This polynomial can also correct single-burst errors up to 23 bits in length. The 32-bit ECC polynomial is the standard polynomial found in IBM PC AT controllers.

The forward and reverse polynomial is selected by programming ECC CONTROL (Register 71H, Bit 7). Whichever polynomial is selected, the ECC/CRC shift registers always start preset to all 1s.

The sequencer controls the time critical operations of the SSI 32C4650. It executes programs stored in the 28 word by 32-bit sequencer RAM, and can be programmed to support hard and soft sectored read, write, search, and verify operations for a wide variety of Winchester Disk Drives and other peripherals. The sequencer RAM is loaded by writing to the sequencer instruction registers as outlined in the Sequencer Instructions of this data sheet. Each instruction is comprised of four bytes. Each of the four bytes represents a function of the sequencer operation. They are address field, control field, data type field, and data field. The organization of these fields is shown in the Register Bit Map in the SSI 32C4650 Design Guide. The Sequencer Registers provide control from and status to the microprocessor and sequencer. They contain branch, next, and start addresses, and sequencer status information. The SEQUENCER STATUS register provides information on the sequencer state such as whether an ECC error occurred, a compare equal or low occurred, if the branch condition or address mark is active, or whether the sequencer is halted.

HOST INTERFACE

The internal receivers and drivers on the host interface block allow the device to connect directly to the PC Host bus. The drivers are capable of sinking up to 24 mA and drive a load up to 300 pF.

The wait state generator extends the Host I/O cycle and inserts wait states by asserting $\overline{\text{IOCHRDY}}$. This generator is only active during Programmed I/O transfers and works in two ways: 1) inserting programmed number of Buffer Memory Cycles for every host access of the device, and 2) asserting $\overline{\text{IOCHRDY}}$ only when the device is not ready for the transfer. Register 58H, Bits 0 and 1, program the wait states cycles and Bit 2 asserts $\overline{\text{IOCHRDY}}$ whenever the device is not ready for transfer.

The auto decoding circuitry allows the device to speed up the performance of the controller by decoding Write commands that require data transfer from the Host to the Buffer Memory. These commands include Format (5XH), Write Buffer (E8H), Write or Write long (3XH). The device automatically starts accepting data without the local microcontroller control when any of these commands are loaded into the COMMAND REGISTER by the host. If interrupts are enabled, the device generates an interrupt to the local microcontroller. The

PC STOP POINTER (Registers 5EH and 5FH) is initialized to 01FFH. If DISABLE STOP POINTER COMPARE (Register 52H, Bit 6) is set, the local microcontroller must initialize the PC STOP POINTER to enable comparison of the WRITE ADDRESS POINTER (Registers 5CH and 5DH) with the HOST STOP POINTER. The Formatter disconnects from the Buffer Manager on receiving one of these commands. It also disables write access by the local microcontroller to the DMA CONTROL REGISTER (53H) and WRITE ADDRESS POINTERS (5CH and 5DH). In addition, read/write access to the BUFFER MEMORY ACCESS REGISTER. Access to these registers is enabled when the local microcontroller writes to AUTOCOMMAND "LOCK" RELEASE register (73H).

The ECC bytes are transferred to and from the host by enabling by Bit 1 of the command byte by the host, indicating Read and Write Long command. If a Read or Write Long command is received, Buffer Memory transfers to/from the Host will exceed the PC STOP POINTER (Registers 5EH and 5FH) by the count of ECC bytes. Initially the PC STOP POINTER is set at the end of the Data Field. When the active READ ADDRESS POINTER (Registers 5AH and 5BH), or WRITE ADDRESS POINTER (Registers 5CH and 5DH), matches the PC STOP POINTER (Registers 5EH and 5FH), the internal FIFO will be emptied of the word width data, the PC STOP POINTER gets incremented by the count of ECC bytes. The ECC bytes will then be transferred in Byte Mode.

PIN DESCRIPTION

GENERAL

NAME	TYPE	DESCRIPTION
VCC		+5V POWER SUPPLY
BGND		BUFFER BUS GROUND
LGND		LOGIC GROUND
HGND		HOST GROUND

HOST INTERFACE

A0:2	I	HOST ADDRESS LINES. These pins are used to address the internal registers by the AT bus.
A9/$\overline{HCS1}$	I	HOST ADDRESS LINE 9/ HOST CHIP SELECT 1. A9, this pin is used in conjunction with the A0:2 address lines to address the internal task file registers. HCS1 is an active low pin, used to qualify Host access.
$\overline{HCS0}$	I	HOST CHIP SELECT 0. Active low, this pin selects access to the control, status and data registers.
$\overline{IOCS16}$	O	I/O SELECT 16. An open drain output that indicates that a 16-bit sector buffer transfer is active.
HINT	O	HOST INTERRUPT. Asserted to indicate to the Host that the controller needs attention.
$\overline{IOCHRDY}$	O	I/O CHANNEL READY. Active low, this signal is asserted whenever that internal host FIFO is not ready to transfer a word.
DREQ	O	DMA REQUEST. This pin is programmed to function as the PC/AT bus signal in the PC/AT DMA mode.
$\overline{DACK}$	I	DMA ACKNOWLEDGE. Active low, in the PC/AT DMA mode this pin is programmed to be the PC/AT channel signal - DACK.
$\overline{IOR}$	I	INPUT READ SELECT. Active low, this pin is asserted by the Host during a Host read operation.
$\overline{IOW}$	I	INPUT WRITE SELECT. Active low, asserted by the HOST during a HOST write operation.

NAME	TYPE	DESCRIPTION
HOST INTERFACE (Continued)		
HRESET	I	HOST RESET. This signal resets all commands in progress when active, and initializes the control/status registers.
HDB 15:0	I/O	HOST DATA BUS. Active high bi-directional pins. These bits are used for data transfers between the Host and the Buffer Manager.
DISK INTERFACE		
INDEX	I	INDEX. Input for index pulse received from the drive
INPUT/ OUTPUT	I/O	INPUT/OUTPUT. A general purpose control and status pin. It can be either an input or an output. At power-on, this pin is an input.
$\overline{\text{WAM}}$/ $\overline{\text{AMD}}$/ SECTOR	I/O	WRITE ADDRESS MARK/ADDRESS MARK DETECT/SECTOR. This pin becomes an active low address mark detect if read gate is on, or write address mark if write gate is on. It operates in hard or soft sector modes. The default is soft sector. In hard sector mode this is the input for the sector pulse.
RG	O	READ GATE. During NRZ data read. this pin is asserted.
WG	O	WRITE GATE. During NRZ data write, this pin is asserted.
RD/REF/ CLK	I	READ/REFERENCE CLOCK. This pin is used in conjunction with the NRZ pin to clock data in and out of the SSI 32C260 device.
NRZ	I/O	NRZ. This pin is used in conjunction with the RG and WG when reading and writing from and to the disk.
MICROPROCESSOR INTERFACE		
$\overline{\text{RST}}$	I	RESET. Active low input, when pulled low, the internal registers of the SSI 32C260 are held at reset.
ALE	I	ADDRESS LATCH ENABLE. This control signal latches the address on the address/data lines.
CS	I	CHIP SELECT. Active high signal, when asserted, the internal registers of the SSI 32C260 can be accessed.
$\overline{\text{WR}}$	I	WRITE. Active low input, when active the data is written to the internal registers.
$\overline{\text{RD}}$	I	READ. Active low input, when active that data is read from the internal registers.
$\overline{\text{INT}}$	O	INTERRUPT. Push-pull or open-drain signal, when active, indicates local microcontroller interrupt.
AD7:0	I/O	ADDRESS/DATA BUS. 8-bit bus for both microprocessor register address and data.
BUFFER MANAGER INTERFACE		
BA0:15	O	BUFFER MANAGER ADDRESS LINES. Active high, for direct connection to a static RAM.
BD0:7	I/O	BUFFER MANAGER DATA BUS. 7 through 0. Active high, buffer data bus that connects directly to the buffer RAM.
$\overline{\text{MOE}}$	O	MEMORY OUTPUT ENABLE. Active low select for the buffer RAM.
$\overline{\text{WE}}$	O	WRITE ENABLE. Active low, write enable for the buffer RAM.
BCLK	I	SYSTEM CLOCK. This signal is used to synchronize the buffer RAM access, including the generation of memory address bits, write enable WE, and memory output enable MOE.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Ambient Temperature Under Bias	0 to 70	°C
Storage Temperature	-65 to 150	°C
Voltage On Any Pin With Respect To Ground	GND-0.5 to VCC+0.5	V
Power Dissipation	0.750	Watt
Power Supply Voltage	7	V
Max Current Injection	50	mA

NOTE: Stress above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
VCC	Power Supply Voltage	Operating	4.5		5.5	V
VIL	Input Low Voltage		-0.5		0.8	V
VIH	Input High Voltage		2.0		VCC+0.5	V
VOL(1)*	Output Low Voltage	IOL = 2 mA			0.4	V
VOL(2)	Output Low Voltage	IOL = 24 mA			0.5	V
VOH	Output High Voltage	IOH = -400µA			2.4	V
ICC	Supply Current				50	mA
ICC_S	Supply Current Standby	All Inputs at GND or VCC			250	µA
IL	Input Leakage Current	0<VIN<VCC	-10		10	µA
CIN	Input Capacitance				10	pF
COUT	Output Capacitance				10	pF

NOTE: (1) All output pins except for host interface signals
(2) Host interface outputs
(*) IOL = 4 mA for RG and WG

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AC CHARACTERISTICS

The following timings assume that all non-Host Bus output pins will drive one Schottky TTL load in parallel with 50 pF, all Host Bus output pins will drive a 300 pF load, and all inputs are at TTL levels. The MIN and MAX timings conform to the operating ranges of a power supply voltage of 5V±10%, and an ambient temperature of 0°C to 70°C.

Host DMA 8/16-Bit Interface Timing Parameters (Figure 1)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
DREQL	DREQ low from $\overline{DACK}$ low				80	ns
RDTA	$\overline{IOR}$ low to HD [0:15] valid				60	ns
RDHLD	$\overline{IOR}$ high to HD [0:15] tri-state		0		20	ns
WDS	HD [0:15] setup to $\overline{IOW}$ high		40			ns
WDHLD	HD [0:15] hold from $\overline{IOW}$ high		10			ns
RWPULSE	$\overline{IOR}$/$\overline{IOW}$ pulse width		80			ns

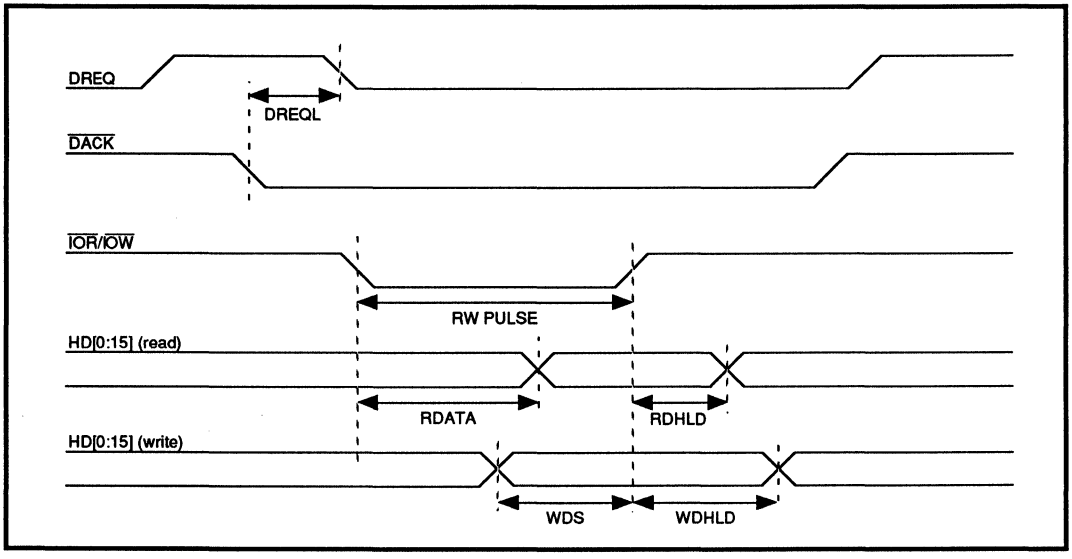


FIGURE 1: Host DMA 8/16-Bit Interface Timing

HOST Programmed I/O 8-16-Bit Timing Parameters (Figure 2)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
CS16L	$\overline{HCS0}$ low, A0:2, A9 low, or $\overline{HCS1}$ high to $\overline{IOCS16}$ low				20	ns
IOCHL	$\overline{IOR}$/$\overline{IOW}$ low to $\overline{IOCHRDY}$ low				25	ns
IOCHTW*	$\overline{IOCHRDY}$ pulse width		0		5xBCLK	ns
RDTA	$\overline{IOR}$ low to HD[0:15] valid				60	ns
RDHLD	$\overline{IOR}$ high to HD[0:15] tri-state		0		20	ns
WDS	HD [0:15] setup to $\overline{IOW}$ high		40			ns
WDHLD	HD[0:15] hold from $\overline{IOW}$ high		10			ns
RWPULSE	$\overline{IOR}$/$\overline{IOW}$ pulse width		80			ns
ADRSET	$\overline{HCS0}$, A0:2, A9/$\overline{HCS1}$, setup to $\overline{IOR}$/$\overline{IOW}$ low		25			ns
ADRHLD	$\overline{HCS0}$, A0:2, A9/$\overline{HCS1}$ hold, from $\overline{IOR}$/$\overline{IOW}$ high		10			ns

*Maximum specification applies when Auto Wait State Generation is disabled (Register 58H, Bit 2 is reset.)

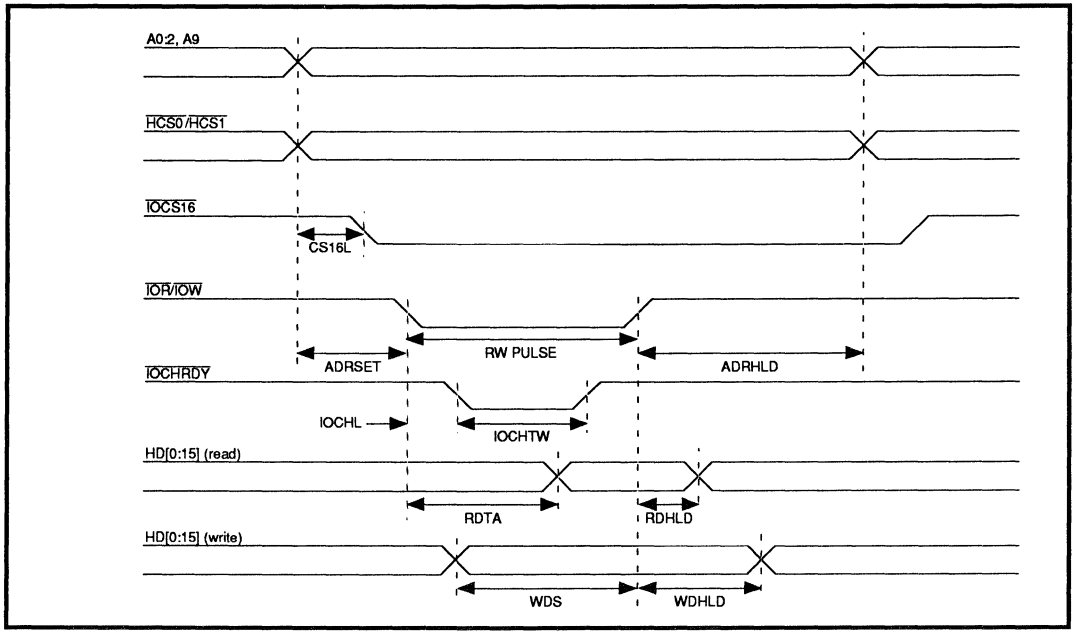


FIGURE 2: Host Programmed 8/16-Bit Timing

Microcontroller Interface Timing Parameters (Figures 3, 4)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Ta	ALE Width		45			ns
Taw	ALE↓to $\overline{\text{WRITE}}$ ↓		25			ns
Tar	ALE↓to $\overline{\text{READ}}$ ↓		25			ns
Tw	$\overline{\text{WR}}$ Width		140			ns
Tr	$\overline{\text{RD}}$ Width		140			ns
As	Address AD [0:7] valid to ALE ↓		5			ns
Ah	ALE↓to Address AD [0:7] invalid		20			ns
Cs	ALE↓to CS valid				5	ns
Ch	$\overline{\text{RD}}$↑or $\overline{\text{WR}}$↑to CS ↓		0			ns
Wds	Write Data AD [0:7] valid to $\overline{\text{WR}}$ ↑		55			ns
Wdh	$\overline{\text{WR}}$↑to Write Data AD [0:7] invalid		10			ns
Tda	$\overline{\text{RD}}$↓to Read Data AD [0:7] valid				100	ns
Tdh	$\overline{\text{RD}}$↑to Read AD [0:7] float (undriven)				50	ns

NOTE: ↓Indicates falling edge. ↑ Indicates rising edge.

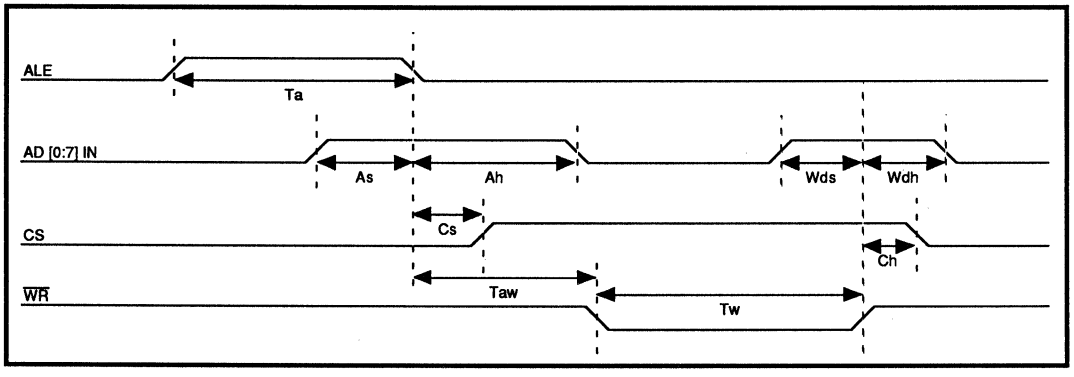


FIGURE 3: Register Write Timing

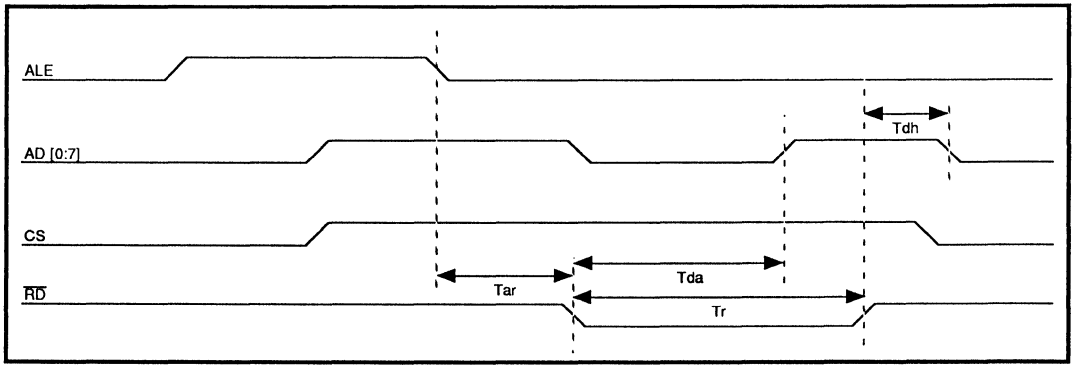


FIGURE 4: Register Read Timing

Disk Read/Write Timing Parameters (Figures 5, 6)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
T	RD/REF CLK Period		38.0			ns
T/2	RD/REF CLK High/Low Time		16			ns
Tr = Tf	RD/REF CLK Rise and Fall time				5	ns
Ds	NRZ valid to RD/REF CLK ↑		15			ns
Dh	RD/REF CLK ↑ to NRZ invalid		7			ns
As*	$\overline{AMD}$ valid to RD/REF CLK ↑		15			ns
Dv	RD/REF CLK ↑ to NRZ		5		25	ns
Wv*	RD/REF CLK ↑ to $\overline{WAM}$		5		25	ns

NOTE: ↓ Indicates falling edge. ↑ Indicates rising edge.

* These specifications are only applicable in the Soft Sector Mode.

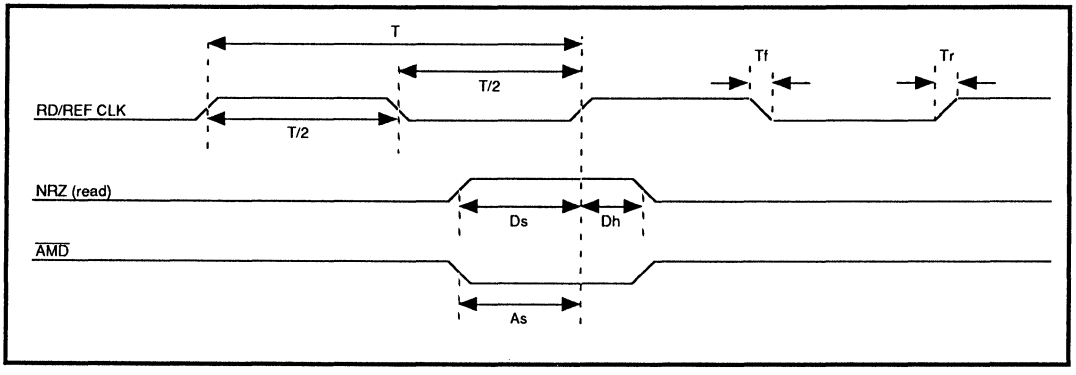


FIGURE 5: Disk Read Timing

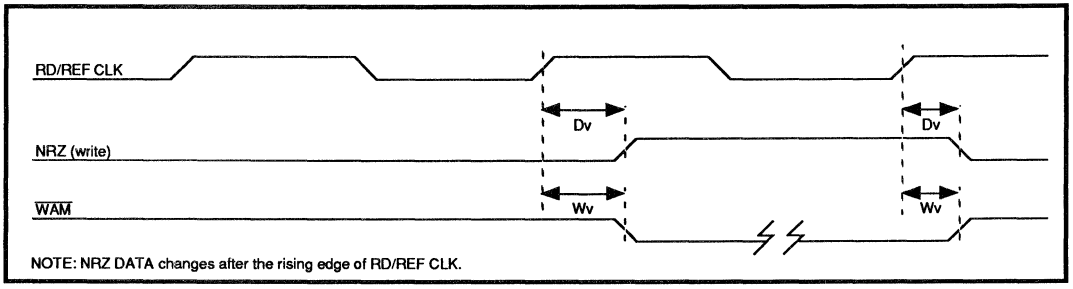


FIGURE 6: Disk Write Timing

Register 70H Access Timing Parameters (Figures 7, 8)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
To	$\overline{RD}$↓to $\overline{MOE}$ ↓				40	ns
Tda	BD[0:7] valid to AD[0:7] valid				55	ns
Trh	$\overline{RD}$↑to AD[0:7] invalid				50	ns
Toh	$\overline{RD}$↑or $\overline{WR}$↑to $\overline{MOE}$ ↑				40	ns
Taw	AD[0:7] valid to $\overline{WE}$ ↓				55	ns
Tao	AD[0:7] valid to $\overline{MOE}$↓				55	ns
Tad	AD[0:7] valid to BD[0:7] valid				55	ns
Twwh	$\overline{WR}$↑to $\overline{WE}$↑				40	ns
Twdh	$\overline{WR}$↑to BD[0:7] invalid		50			ns

NOTE: ↓ Indicates falling edge. ↑ Indicates rising edge.

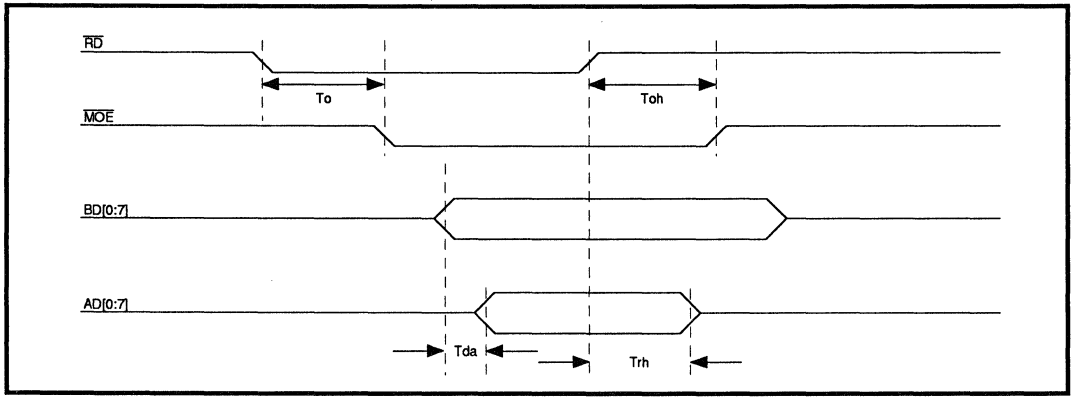


FIGURE 7: Register 70H Read Timing

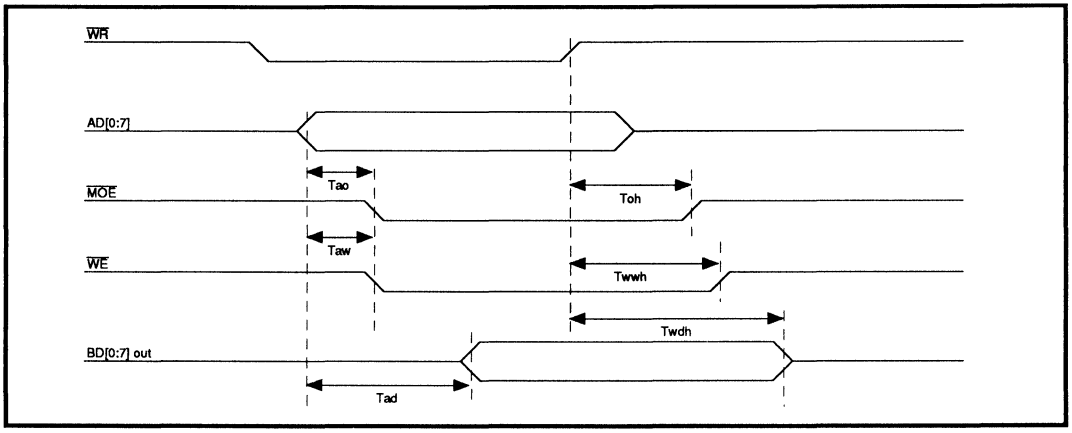


FIGURE 8: Register 70H Write Timing

Buffer Memory Read/Write Timing Parameters (Figure 9)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
T_B	BCLK Period		41			ns
$T_B/2$	BCLK High/Low Time		16			ns
$T_{Br}=T_{Bf}$	BCLK Rise and Fall Time				5	ns
T1	BUFCLK* Period		125			ns
Av	BUFCLK*↓to BA[0:15] valid				65	ns
Dov	BUFCLK*↑to BD[0:7] valid				50	ns
Doh	BUFCLK*↑to BD[0:7] invalid		0			ns
Mv	BUFCLK*↑to $\overline{MOE}$ ↓				30	ns
Mh	BUFCLK*↓to $\overline{MOE}$ ↑		10		35	ns
Wv	BUFCLK*↑to $\overline{WE}$ ↓				30	ns
Wh	BUFCLK*↓to $\overline{WE}$ ↑		5		30	ns
Dma	$\overline{MOE}$ ↑to BA[0:15] Hold		10		30	ns
Dis	BD[0:7] valid to BUFCLK*↓		5			ns
Dih	BUFCLK*↓to BD[0:7] invalid		10			ns
TBbr	BCLK↑to BUFCLK↑				24	ns
TBbf	BCLK↓to BUFCLK↓				21	ns

NOTE: ↓Indicates falling edge. ↑ Indicates rising edge.

* BUFCLK is an internal signal which indicates the period of Buffer Memory Access Cycle. These specifications can be tested when the period of BCLK pin is the same as the period of Buffer Memory Access Cycles (i.e., Register 7FH, Bits 6 and 7 are 1 and 0, respectively). If the Buffer Memory Access Cycle period is programmed to be a multiple of the period of BCLK pin, BUFCLK above refers to the Buffer Memory Access Cycles and the falling edge referred to above would be coinciding with the rising edge of the BCLK pin.

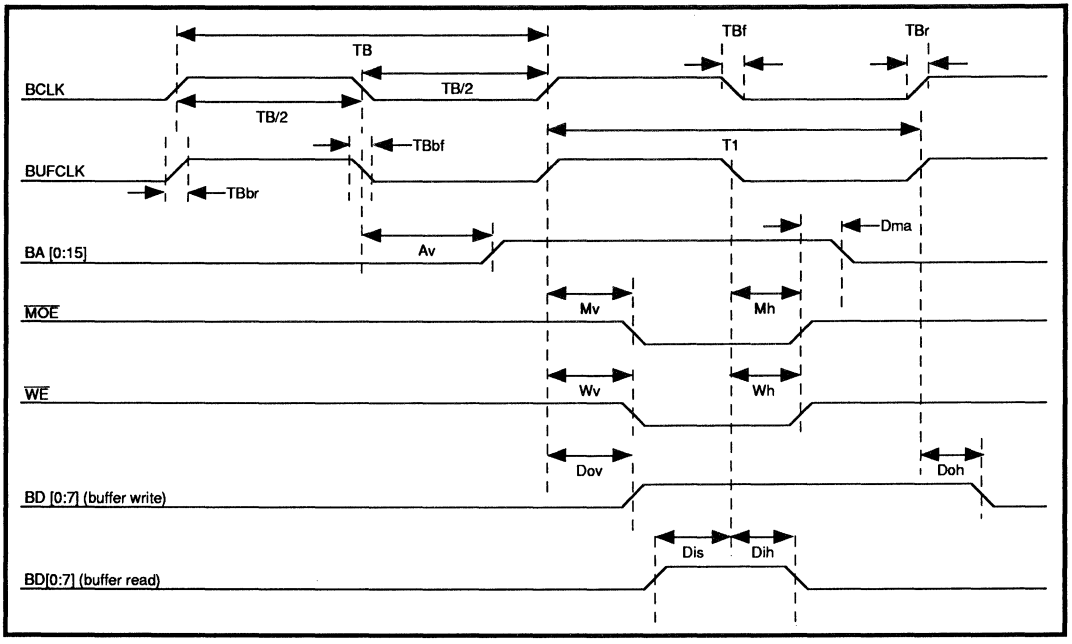
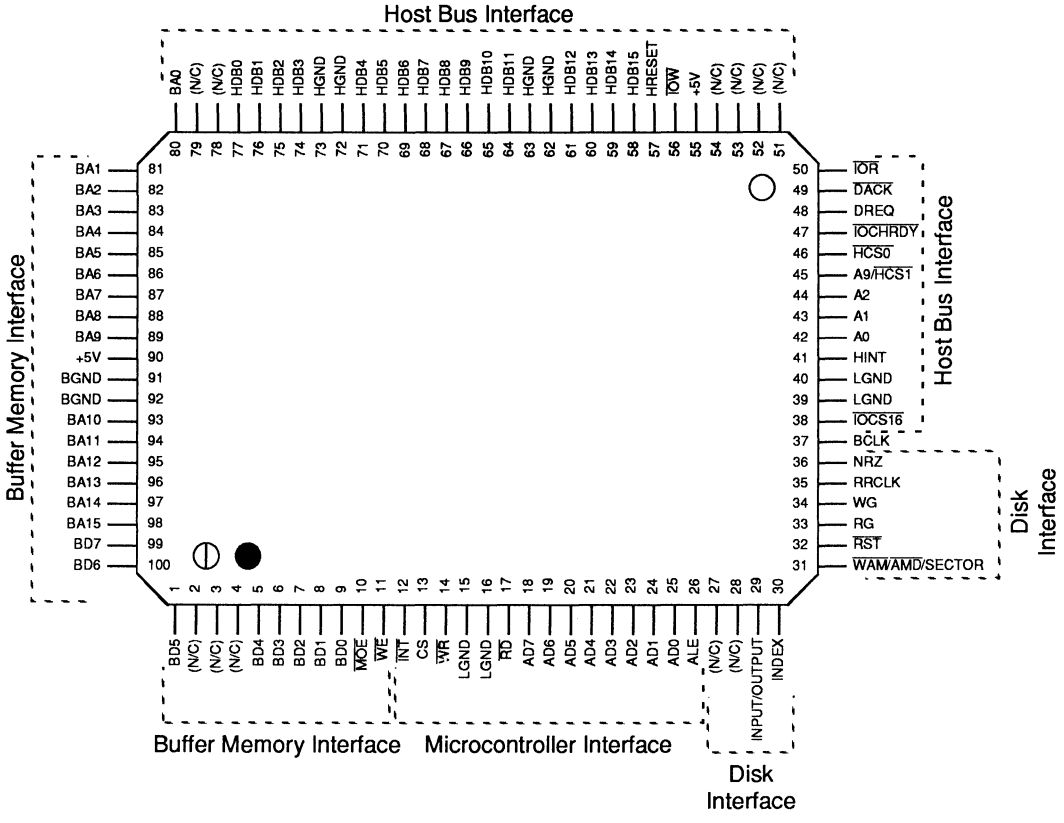


FIGURE 9: Buffer Memory Read/Write Timing

PACKAGE PIN DESIGNATIONS
(TOP VIEW)



100-pin QFP

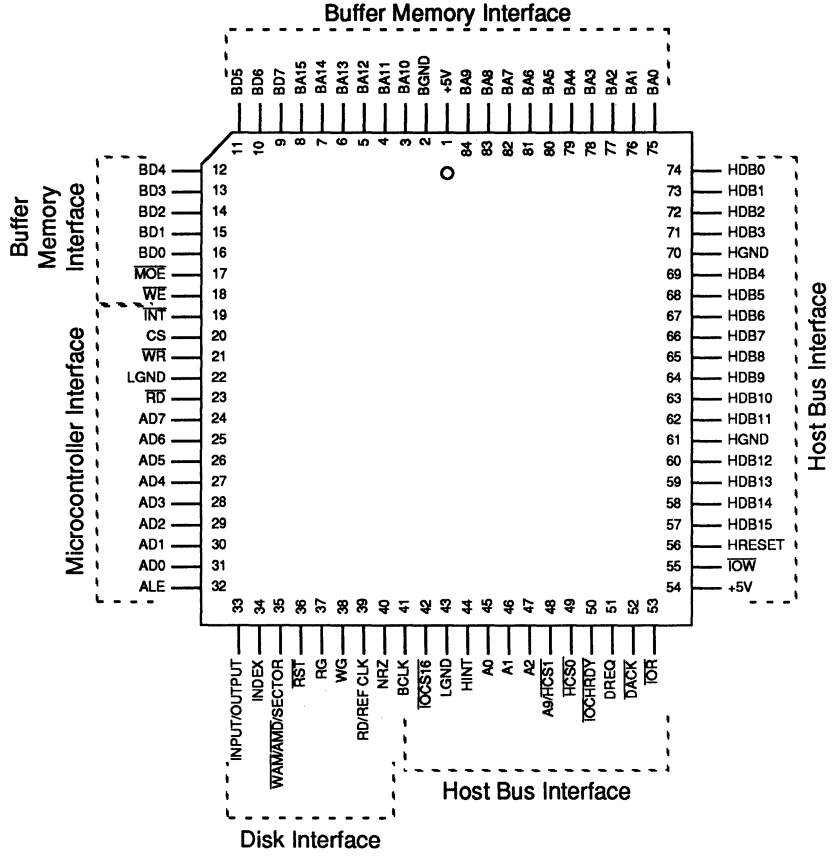
CAUTION: Use handling procedures necessary for a static sensitive component.

8

PACKAGE PIN DESIGNATIONS (Continued)

(TOP VIEW)

CAUTION: Use handling procedures necessary for a static sensitive component.



84-pin PLCC

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714) 731-7110, FAX: (714) 573-6914

SSI 32C4651
PC AT/XT Combo Disk Controller 26 Mbit/s
Advance Information

December 1991

DESCRIPTION

The SSI 32C4651 is a CMOS VLSI device which integrates major portions of the hardware needed to build a PC AT/XT driven hard disk controller. The SSI 32C4651 is one of the family of Silicon Systems' single chip disk controllers. The SSI 32C4651's place in the Silicon Systems' chip family is illustrated in the hierarchy chart in Figure 1. It provides most of the functional circuitry necessary to build an "ATA" embedded disk.

The SSI 32C4651 is capable of supporting interleaved data transfer rate up to 26 Mbit/s. This chip represents a major reduction in part count when used with the SSI 32P4720 Pulse Detector and Data Separator combo, the SSI 32R2010 Read/Write device, the SSI 32H6520 Embedded Servo Controller device, and the SSI 32H6810 Servo and Motor Speed Controller with drivers implementing a low power and cost efficient 5-chip set intelligent drive solution for 24 Mbit/s applications.

The SSI 32C4651 includes a dual port Buffer Manager, a storage controller, and a high performance AT host interface block that incorporates an extensive hardware support — including 24 mA drivers — for the PC AT and other compatible interfaces.

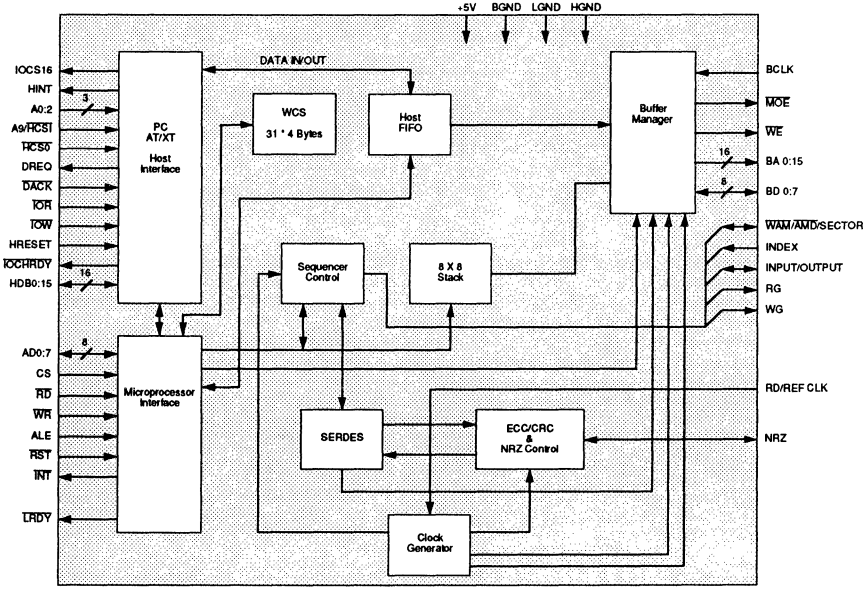
The SSI 32C4651 performs all the controller functions for the peripheral device, such as serialization/deserialization; ECC generation and checking on the data stream, and CRC generation and checking on the header of the data stream.

FEATURES

- **PC AT/XT Bus Interface**
  - **Single Chip PC AT/XT Controller**
  - **Direct bus interface logic with on-chip 24 mA drivers**
  - **Logic for daisy chaining 2 embedded ATA drives**
  - **Buffer transfer in single or burst mode DMA or PIO modes**
  - **Provides logic to speed up command response**

(Continued)

BLOCK DIAGRAM



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SSI 32C4651
PC AT/XT Combo Disk Controller 26 Mbit/s

FEATURES (continued)

- Supports 26 Mbit/s concurrent disk transfer on a 3 M words/s PC-AT without wait states

- Buffer Manager
  - Dual port buffer access with access priority resolver
  - Total Buffer Memory throughput to 10 MByte/s
  - Direct Buffer Memory addressing up to 64 kB Static RAM
  - 4k Buffer segmentation support
  - Provides host overrun control

- Storage Controller
  - NRZ Data Rates to 26 Mbit/s
  - Selectable 16-bit CRC or 32/56 bit ECC polynomial with hardware correction circuitry
  - Microprocessor based split data field processing logic
  - Highly programmable Advanced sequencer organized in 31 x 4 bytes
  - 8-byte stack for header information storage
  - Supports programmable sector lengths up to a full track
  - Two-index counter providing sector I.D. search and retry limits
  - Preset of CRC/ECC generator to either "0's" or "1's"

- Microprocessor Interface
  - Interface to high speed processors — 16 MHz 8051 or 12 MHz 68HC11
  - Programmable wait state insertion for faster microprocessors
  - Provides microprocessor access to 8 external switch settings
  - Interrupt or polled microprocessor interface

- Others
  - Internal power down mode
  - Operational at ±10% of 5V
  - Plug and play compatible with the Cirrus Logic SH-260, SH-265 and the SH-266
  - Available in 100-pin surface mount QFP

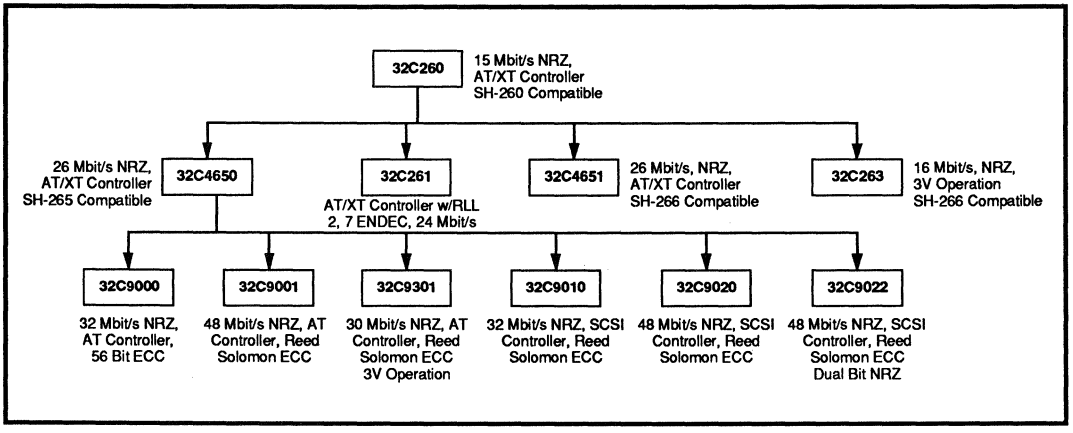

FIGURE 1: Silicon Systems' Disk Controller Chip Hierarchy

FUNCTIONAL DESCRIPTION

The four major functional blocks are:

- Microcontroller Interface
- Buffer Memory Interface
- Disk Formatter
- Host Interface

The SSI 32C4651 includes a control sequencer with a writeable control store, buffer RAM controller capable of interleaved address generation, direct ATA bus connections, and configuration/status registers which can be programmed by an external microcontroller. The internal hardware also supports automatic looping of the sequencer program, and the interrupt circuitry relieves the supervising microprocessor of having to poll on the status registers. Access to the control store and registers is accomplished through the microprocessor interface which is optimized for eight-bit, mulitplexed address/data processors such as the Intel 8051. **For a complete description of the programmable registers, refer to the SSI 32C4651 Design Guide.**

The device performs all the controller functions for the peripheral device, such as serialization/deserialization; ECC generation, checking, and correction assistance; and CRC generation and checking on the header stream. The contention between the host and the disk requests for buffer RAM access is internally arbitrated and resolved.

PIN DESCRIPTION

The following convention is used in the pin description:

(I)	denotes an input
(I/S)	denotes a Schmitt trigger input
(O)	denotes an output
(I/O)	denotes a bidirectional signal
(Z)	denotes a tri-state output
(OD)	denotes an open drain output

Active low signals are denoted by a bar on top of the signal name and dual function pins are denoted with a slash between the two signals: A9/$\overline{\text{HCS1}}$, for example.

GENERAL

NAME	TYPE	DESCRIPTION
VDD		POWER SUPPLY PIN, VCC
GND		GROUND

HOST INTERFACE

A0:2	I	HOST ADDRESS LINES. The Host Address lines A(2:0) and A9 are used to access the various PC/AT control/status, and data registers.
A9/$\overline{\text{HCS1}}$	I	HOST ADDRESS LINE 9/ HOST CHIP SELECT 1. This is a multiplexed input pin. When Register 52H, bit 3 is reset this input is HOST ADDRESS LINE 9, when the bit is set this input is HOST CHIP SELECT 1. When configured as $\overline{\text{HCS1}}$ this input is ignored when $\overline{\text{DACK}}$ is asserted.
$\overline{\text{HCS0}}$	I	HOST CHIP SELECT 0. This pin selects access to the control, status and data registers. This input is ignored when $\overline{\text{DACK}}$ is asserted.
$\overline{\text{IOCS16}}$	OD	16-BIT DATA TRANSFER. An open drain output when active low indicates that a 16-bit buffer transfer is active.
HINT	O	HOST INTERRUPT. Asserted active high to indicate to the Host that the controller needs attention.
$\overline{\text{IOCHRDY}}$	O, Z	I/O CHANNEL READY. Asserted active low whenever the internal host FIFO is not ready to transfer data.

8

PIN DESCRIPTION (Continued)

HOST INTERFACE (Continued)

NAME	TYPE	DESCRIPTION
DREQ	O, Z	DMA REQUEST. The DMA Request signal is asserted active high during DMA transfer between the Host and the SSI 32C4651.
$\overline{DACK}$	I	DMA ACKNOWLEDGE. This signal is asserted low by the host during DMA to complete the DMA handshake for data transfer between the host and the controller.
$\overline{IOR}$	I	INPUT READ SELECT. This pin is asserted active low by the Host during a Host read operation. When asserted with $\overline{HCS0}$, $\overline{HCS1}$, or $\overline{DACK}$, data from the device is enabled onto the host data bus.
$\overline{IOW}$	I	INPUT WRITE SELECT. Asserted active low by the HOST during a HOST write operation. When asserted with $\overline{HCS0}$, $\overline{HCS1}$, or $\overline{DACK}$, data from the host data bus is strobed into the device.
HRESET	I/S	HOST RESET. This signal, when asserted active high, stops all commands in progress and initializes the control/status registers — see Design Guide for Register Reset conditions. This signal can also "wake up" the device while it is in power down mode.
HDB (15:0)	I/O	HOST DATA BUS. These bits are used for word transfers between the Buffer Memory and the Host; bits (7:0) are also used for status, commands, or ECC byte transfers.

DISK INTERFACE

INDEX	I	INDEX. This input is a pulse that occurs once per revolution and defines the start of sector 0.
INPUT/ OUTPUT	I/O	DISK SEQUENCER INPUT/OUTPUT. A general purpose control (output) and status (input) pin configured by the Output Enable Bit of Sequencer Mode Selection Register 77H, bit 6. At power-on, this pin is an input. As an input, it can be used to synchronize the disk sequencer to an external event. The state of this pin is sampled by reading Formatter interrupt Enable Register 7EH, bit 2. As an output, it is controlled by bit 2 of the Control Field of the disk sequencer.
$\overline{WAM}$/$\overline{AMD}$ SECTOR	I/O	WRITE ADDRESS MARK/SECTOR/ADDRESS MARK DETECT. This pin is configured to operate in Hard or Soft Sector mode by initializing the Formatter Mode Selection Register: 77H, bit 7. In the hard sector mode it is used as the sector input — a pulse on this pin indicates a sector mark is found. In the soft sector mode, a one-bit wide active low output pulse is asserted when formatting to allow writing of address mark. When reading, an active low input indicates an address mark was detected. The device powers up in soft sector mode.
RG	O	READ GATE. This output enables the reading of the disk. It is asserted active high at the beginning of the PLO for header and data field by the sequencer Control Field bit 6. It is automatically deasserted at the end of the CRC or ECC, when the sequencer processes servo gaps between data fragments, or when the sequencer goes to the stopped state.
WG	O	WRITE GATE. This active high output enables writing onto the disk. It is asserted and deasserted by the sequencer Control Field bits 5 and 7.
RRCLK	I	READ/REFERENCE CLOCK. This pin is used in conjunction with the NRZ pin to clock data in and out of the SSI 32C4651 device. This input must be glitch-free to ensure correct operation of the chip.
NRZ	I/O	NON RETURN TO ZERO. This signal is the serial read data input from the disk drive when the read gate signal is asserted; it is the write data output to the disk drive when the write gate signal is asserted.

MICROPROCESSOR INTERFACE

NAME	TYPE	DESCRIPTION
$\overline{RST}$	I/S	RESET. An active low input generates a component reset that holds the internal registers of the SSI 32C4651 at reset, stops all operations within the chip, and deasserts all output signals. All input/output signals and Host outputs are set to the high-Z state.
ALE	I/S	ADDRESS LATCH ENABLE. This control signal latches the address on the AD 7:0 lines.
CS	I/S	CHIP SELECT. This active high signal must be asserted for all microprocessor accesses to the registers of this chip.
$\overline{WR}$	I/S	WRITE STROBE. Active low $\overline{WR}$ and CS assertion causes the data to be written into the specified registers from the AD lines.
$\overline{RD}$	I/S	READ STROBE. Active low assertion $\overline{RD}$ and CS causes the data from the specified register to be driven on the AD 7:0 lines.
$\overline{INT}$	O,OD	INTERRUPT. An active low signal which indicates the controller is requesting microprocessor service. This signal is programmable for either a push-pull with an internal pull up resistor or open-drain output circuit. This signal powers up in the high-Z state. Formatter Mode Selection Register, 77H: bit 4 set high, disables the pullup on the output pin, leaving an open drain output. This is intended to support multiple interrupt sources.
AD7:0	I/O	ADDRESS/DATA BUS. These lines make up the multiplexed, bidirectional data path to the microprocessor. ALE latches register address from this bus with data transferred during $\overline{RD}$ or $\overline{WR}$ assertion.
$\overline{LRDY}$	O	LOCAL MICROPROCESSOR READY: When this signal is deasserted low, the microprocessor inserts wait states to allow time for the chip to respond to the access. Wait states are programmed by Auxiliary Control 1 Register — 4FH: bits 7-6.

BUFFER MANAGER INTERFACE

BA0:15	O	BUFFER MEMORY ADDRESS LINES 0:15. These sixteen outputs provide address lines for the static memory chips used to implement the buffer memory.
BD0:7	I/O	BUFFER MEMORY DATA BUS. 7 through 0. The bidirectional Data Bus connects the buffer RAM to the buffer manager. This bus is designed for high speed data transfer.
$\overline{MOE}$	O	MEMORY OUTPUT ENABLE. This active low output controls the enabling of data onto the Data Bus from the RAMs.
$\overline{WE}$	O	WRITE ENABLE. This active low output signal is used to strobe the data into the RAMs from the Data bus.
SYSCLK	I	SYSTEM CLOCK. This signal is used to synchronize the buffer RAM access, including the generation of memory address lines, write enable $\overline{WE}$, and memory output enable $\overline{MOE}$. In power down mode, this signal is shut off from the internal logic and hence buffer memory access is inhibited.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Maximum limits indicate where a permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Electrical Characteristics.

PARAMETER	RATING	UNIT
Power Supply Voltage, VCC	7	V
Ambient Temperature	0 to 70	°C
Storage Temperature	-65 to 150	°C
Power Dissipation	750	mW
Input, Output pins	-0.5 to VCC+0.5	V

DC ELECTRICAL CHARACTERISTICS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
VCC	Power Supply Voltage		4.5		5.5	V
ICC	Supply Current	Operating			40	mA
ICCS	Supply Current	Note 1			500	µA
VIL	Input Low Voltage		-0.5		0.8	V
VIH	Input High Voltage		2.0		VCC +0.5	V
VIL	Input Low Voltage	Schmitt triggered signals	-0.5		0.9	V
VIH	Input High Voltage	Schmitt triggered signals	1.9		VCC +0.5	V
VOL	Output Low Voltage	Note 2			0.4	V
VOL	Output Low Voltage	Note 3			0.5	V
VOH	Output High Voltage	IOH = -400 µA			2.4	V
IL	Input Leakage Current	0 < VIN < VCC	-10		10	µA
CIN	Input Capacitance				10	pF
COUT	Output Capacitance			10		pF

Note: (1) In powered down, sleep mode
(2) All interface pins except Host Interface pins. IOL= 2mA.
(3) Host Interface pins, IOL=24mA.
(4) Schmitt triggered signals

AC CHARACTERISTICS

The following timings assume that all non-Host Bus output pins will drive one Schottky TTL load in parallel with 50 pF, all Host Bus output pins will drive a 300 pF load, and all inputs are at TTL levels. The MIN and MAX timings conform to the operating ranges of a power supply voltage of 5V±10%, and an ambient temperature of 0°C to 70°C.

Host DMA 8/16-Bit Interface Timing Parameters (Non-Demand Mode)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
DREQL	DREQ low from $\overline{DACK}$ low				80	ns
RDTA	$\overline{IOR}$ low to HD [0:15] valid				50	ns
RDHLD	$\overline{IOR}$ high to HD [0:15] invalid		0			ns
RDTRI	$\overline{IOR}$ hight to HDB [0:15] tri-state				40	
WDS	HD [0:15] setup to $\overline{IOW}$ high		30			ns
WDHLD	HD [0:15] hold from $\overline{IOW}$ high		10			ns
RWPULSE	$\overline{IOR}$/$\overline{IOW}$ pulse width		60			ns

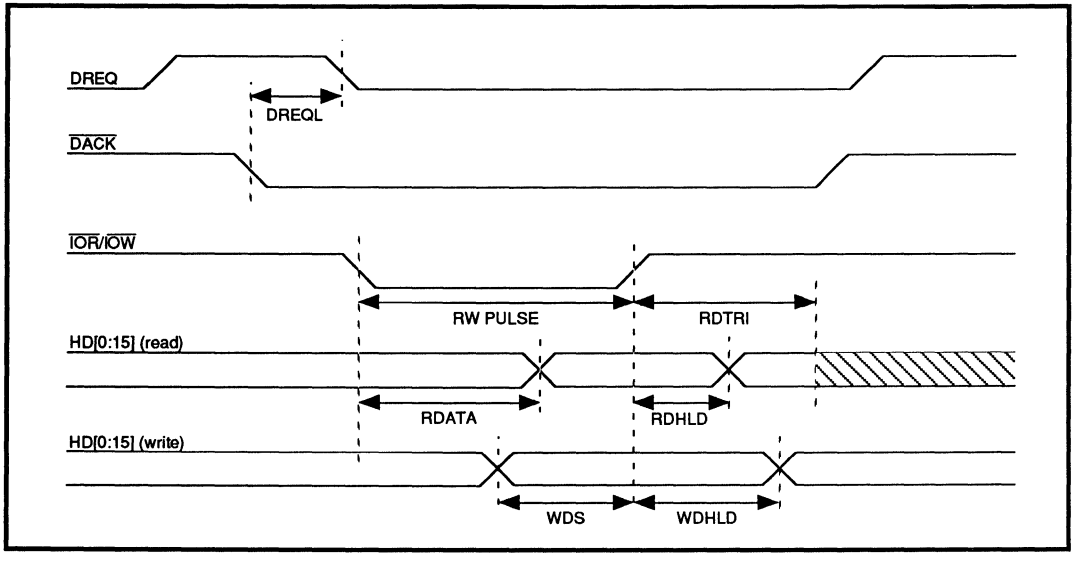

FIGURE 2: Host DMA 8/16-Bit Interface Timing (Non-Demand Mode)

8

Host DMA 8/16-Bit Interface Timing Parameters (Demand Mode)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
DREQL	DREQ low from $\overline{IOR}$ /$\overline{IOW}$ low				40	ns
DMASET	$\overline{DACK}$ low to $\overline{IOR}$/$\overline{IOW}$ low		10			ns
DMAHLD	$\overline{DACK}$ hold from $\overline{IOR}$/$\overline{IOW}$ high		10			ns
RWH	$\overline{IOR}$/$\overline{IOW}$ high to $\overline{IOR}$/$\overline{IOW}$ low		50			ns
RDATA	$\overline{IOR}$ low to HD [0:15] valid				50	ns
RDHLD	$\overline{IOR}$ high to HD [0:15] invalid		0			ns
RDTRI	$\overline{IOR}$ high to HD [0:15] tri-state				40	ns
WDS	HD [0:15] setup to $\overline{IOW}$ high		30			ns
WDHLD	HD [0:15] hold from $\overline{IOW}$ high		10			ns
RWPULSE	$\overline{IOR}$/$\overline{IOW}$ pulse width		60			ns

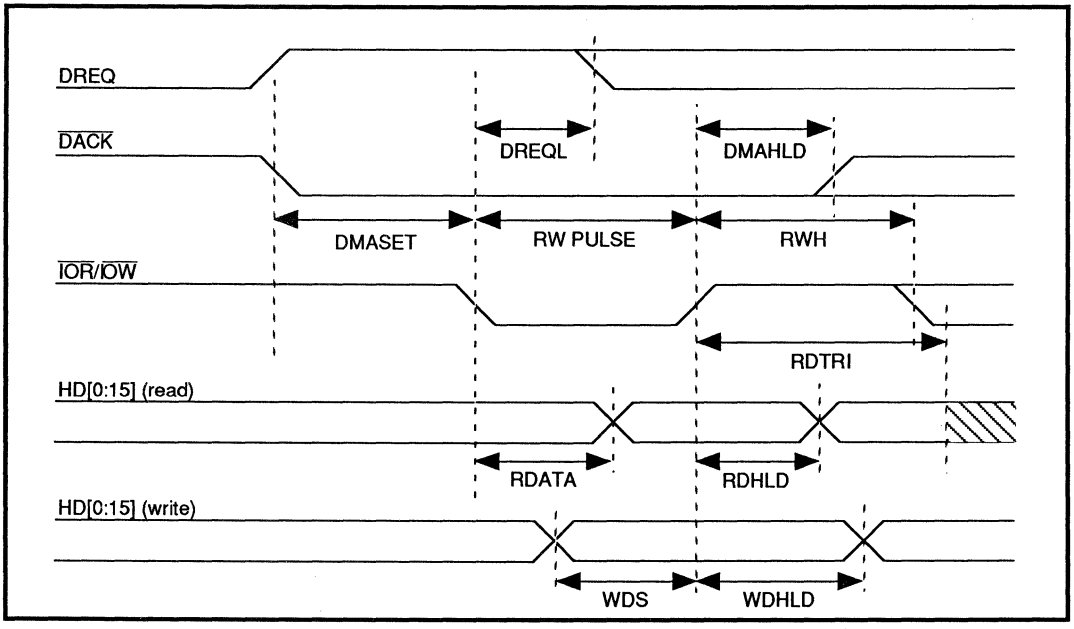

FIGURE 3: Host DMA 8/16-Bit Interface Timing (Demand Mode)

HOST Programmed I/O 8-16-Bit Timing Parameters (Figure 4)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
CS16L	$\overline{HCS0}$ low, A0:2, A9 low, or $\overline{HCS1}$ high to $\overline{IOCS16}$ low				20	ns
IOCHL	$\overline{IOR}$/$\overline{IOW}$ low to $\overline{IOCHRDY}$ low				25	ns
IOCHTW*	$\overline{IOCHRDY}$ pulse width		0		5xBCLK	ns
RDTA	$\overline{IOR}$ low to HD[0:15] valid				50	ns
RDHLD	$\overline{IOR}$ high to HD[0:15] tri-state		0		40	ns
WDS	HD [0:15] setup to $\overline{IOW}$ high		30			ns
WDHLD	HD[0:15] hold from $\overline{IOW}$ high		10			ns
RWPULSE	$\overline{IOR}$/$\overline{IOW}$ pulse width		60			ns
ADRSET	$\overline{HCS0}$, A0:2, A9/$\overline{HCS1}$, setup to $\overline{IOR}$/$\overline{IOW}$ low		25			ns
ADRHLD	$\overline{HCS0}$, A0:2, A9/$\overline{HCS1}$ hold, from $\overline{IOR}$/$\overline{IOW}$ high		10			ns

*Maximum specification applies when Auto Wait State Generation is disabled (Register 58H, Bit 2 is reset.)

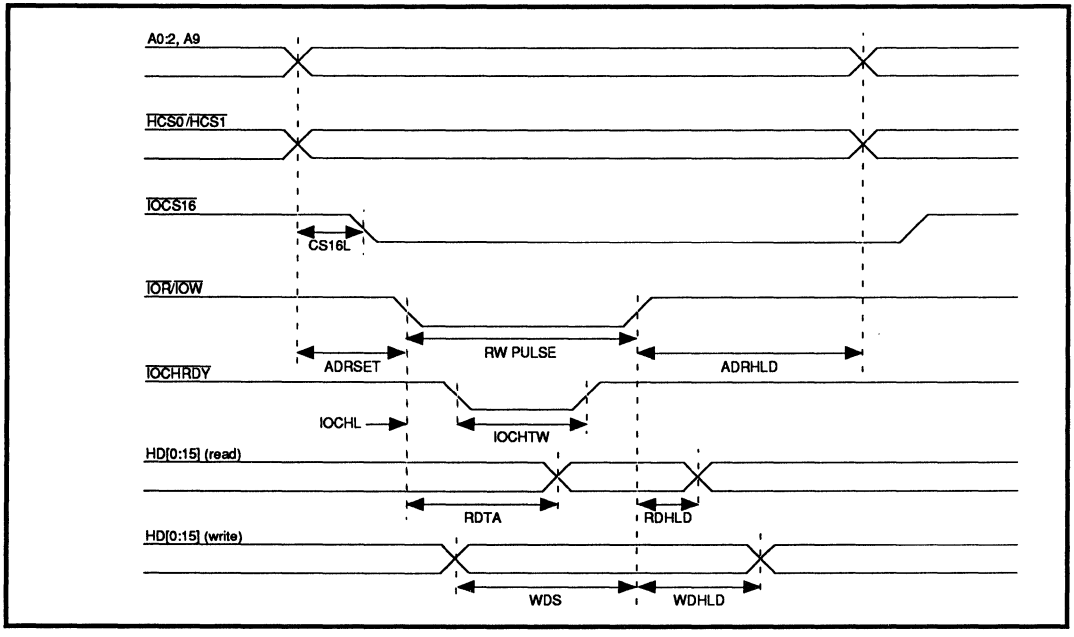

FIGURE 4: Host Programmed 8/16-Bit Timing

Microcontroller Interface Timing Parameters (Figures 5, 6, and 7)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Ta	ALE Width		15			ns
Taw	ALE ↓ to $\overline{\text{WRITE}}$ ↓		15			ns
Tar	ALE ↓ to $\overline{\text{READ}}$ ↓		15			ns
Tw	$\overline{\text{WR}}$ Width		110			ns
Tr	$\overline{\text{RD}}$ Width		110			ns
As	Address AD [0:7] valid to ALE ↓		5			ns
Ah	ALE ↓ to Address AD [0:7] invalid		15			ns
Cs	ALE ↓ to CS valid				5	ns
Ch	$\overline{\text{RD}}$ ↑ or $\overline{\text{WR}}$ ↑ to CS ↓		0			ns
Wds	Write Data AD [0:7] valid to $\overline{\text{WR}}$ ↑		25			ns
Wdh	$\overline{\text{WR}}$ ↑ to Write Data AD [0:7] invalid		10			ns
Tda	$\overline{\text{RD}}$ ↓ to Read Data AD [0:7] valid				100	ns
Tdh	$\overline{\text{RD}}$ ↑ to Read AD [0:7] float (undriven)				50	ns
Tdrdy	ALE ↓ and CS ↑ to $\overline{\text{LRDY}}$ ↓				30	ns

NOTE: ↓ Indicates falling edge. ↑ Indicates rising edge.

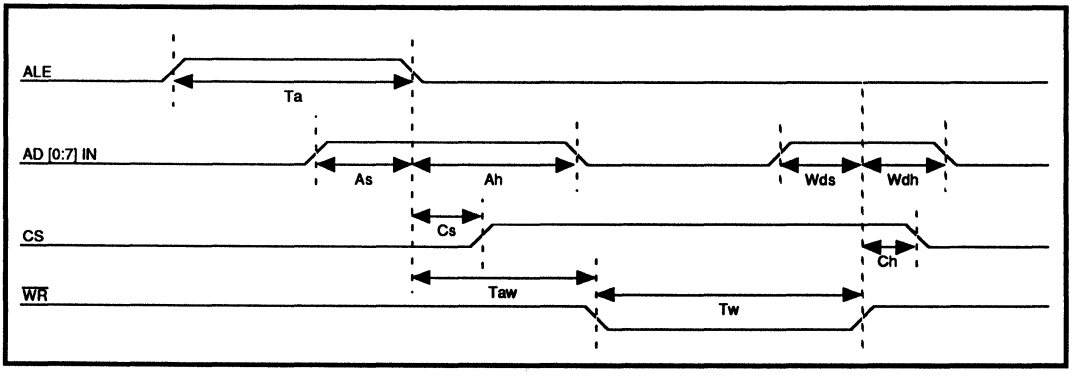

FIGURE 5: Register Write Timing

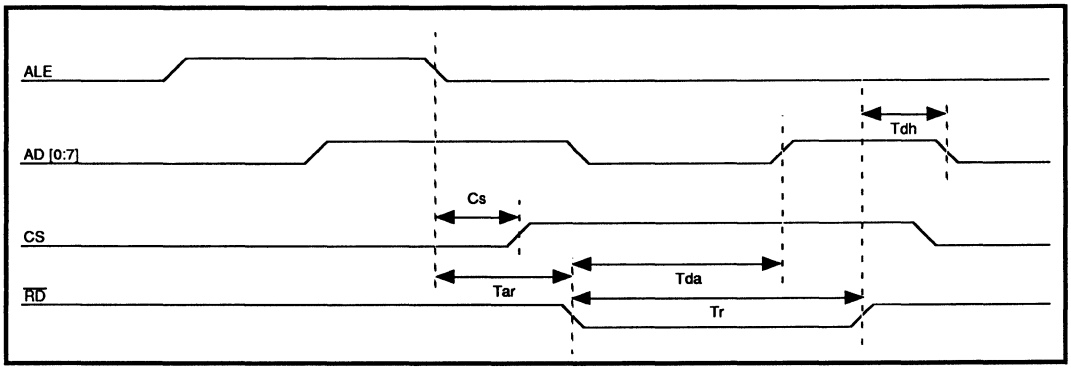

FIGURE 6: Register Read Timing

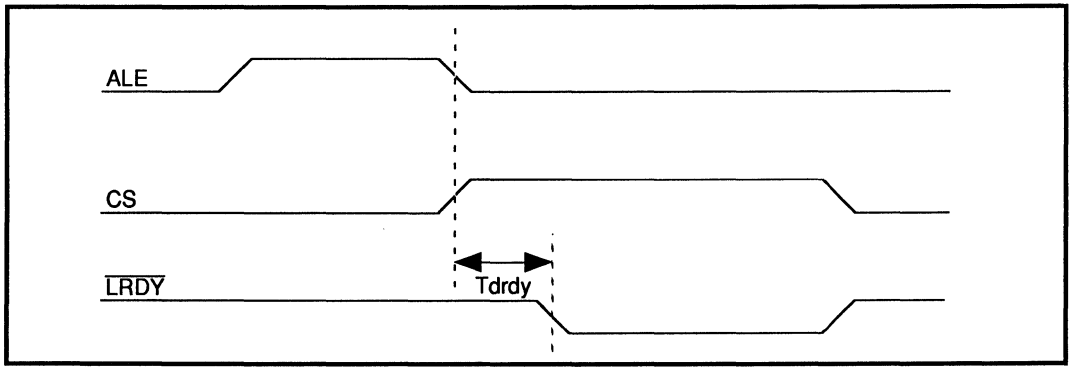

FIGURE 7: Ready Timing

Disk Read/Write Timing Parameters (Figures 8, 9)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
T	RD/REF CLK Period		38			ns
T/2	RD/REF CLK High/Low Time		15			ns
Tr = Tf	RD/REF CLK Rise and Fall time				5	ns
Ds	NRZ valid to RD/REF CLK↑		5			ns
Dh	RD/REF CLK↑to NRZ invalid		5			ns
As*	$\overline{AMD}$ valid to RD/REF CLK↑		10			ns
Dv	RD/REF CLK↑to NRZ		5		25	ns
Wv*	RD/REF CLK↑to $\overline{WAM}$		5		25	ns

NOTE: ↓ Indicates falling edge. ↑ Indicates rising edge.

* These specifications are only applicable in the Soft Sector Mode.

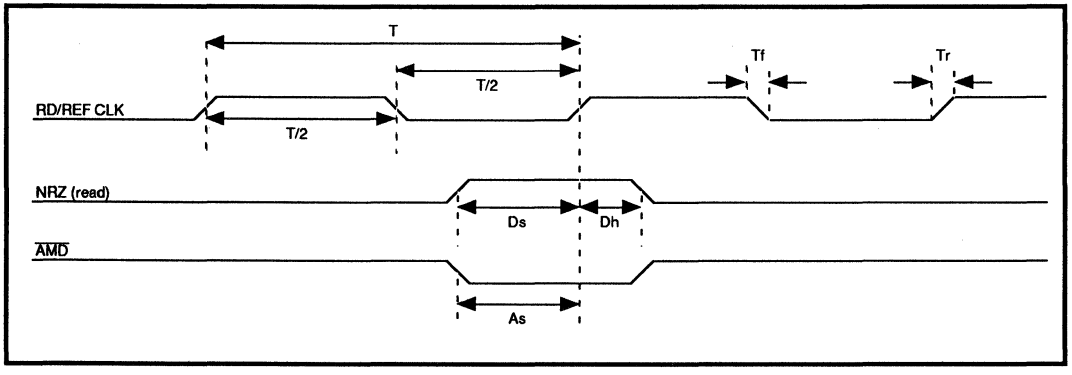

FIGURE 8: Disk Read Timing

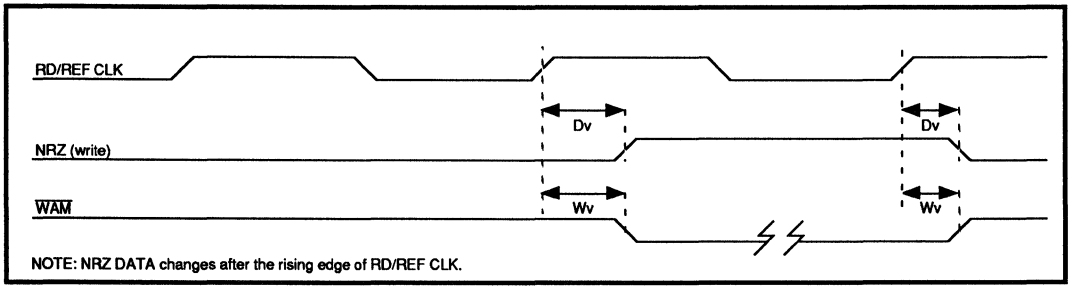

FIGURE 9: Disk Write Timing

Register 70H Access Timing Parameters (Figures 10, 11)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
To	$\overline{RD}$↓to $\overline{MOE}$ ↓				40	ns
Tda	BD[0:7] valid to AD[0:7] valid				55	ns
Trh	$\overline{RD}$↑to AD[0:7] invalid				50	ns
Toh	$\overline{RD}$ ↑or $\overline{WR}$ ↑to $\overline{MOE}$ ↑				40	ns
Taw	AD[0:7] valid to $\overline{WE}$ ↓				55	ns
Tao	AD[0:7] valid to $\overline{MOE}$ ↓				55	ns
Tad	AD[0:7] valid to BD[0:7] valid				55	ns
Twwh	$\overline{WR}$ ↑to $\overline{WE}$ ↑				40	ns
Twdh	$\overline{WR}$ ↑to BD[0:7] invalid		50			ns

NOTE: ↓ Indicates falling edge. ↑ Indicates rising edge.

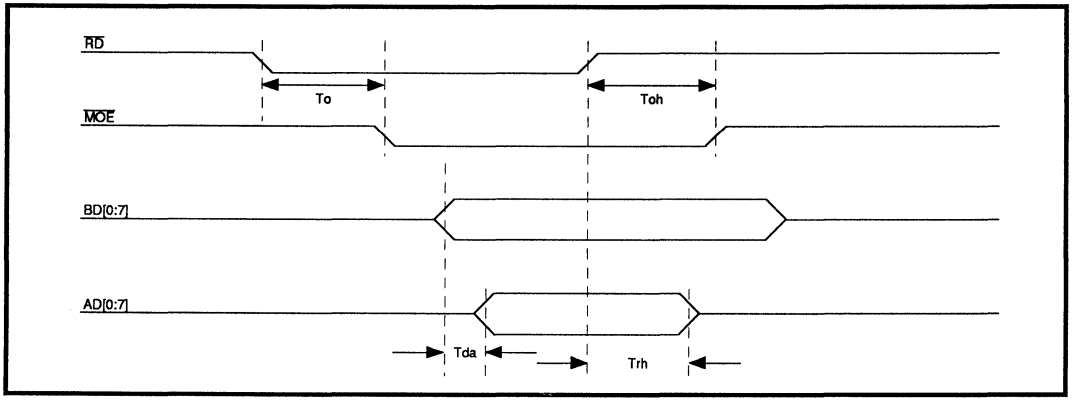

FIGURE 10: Register 70H Read Timing

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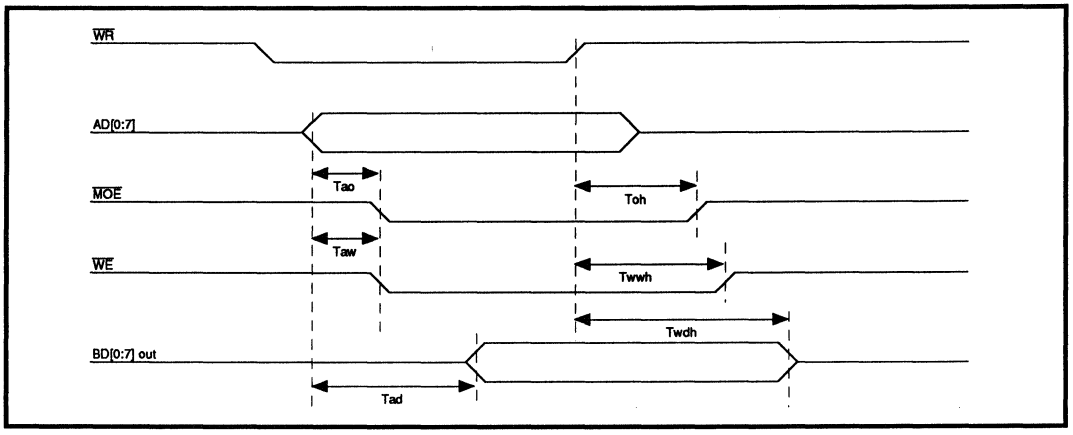

FIGURE 11: Register 70H Write Timing

Buffer Memory Read/Write Timing Parameters (Figure 12)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
T_B	BCLK Period		25			ns
$T_B/2$	BCLK High/Low Time		10			ns
$T_{Br}=T_{Bf}$	BCLK Rise and Fall Time				5	ns
Av	BCLK↓to BA[0:15] valid				80	ns
Dov	BD[0:7] valid to $\overline{WE}$*↑		1/2 BUFCLK Period - 20			ns
Doh	$\overline{WE}$↑to BD[0:7] invalid		5			ns
Mv	BCLK↑to $\overline{MOE}$↓				30	ns
Mh	$\overline{MOE}$↑to Address Hold		5		30	ns
Wv	BCLK↑to $\overline{WE}$↓				30	ns
Wh	$\overline{WE}$↑to Address Hold		5		30	ns
Dis	BD[0:7] valid to $\overline{MOE}$↑		20			ns
Dih	MOE↑to BD[0:7] invalid		5			ns
Bacc	Buffer Access Period		1 BUFCLK Period			
Ww	$\overline{WE}$ Low Time		1/2 BUFCLK Period			
Mw	$\overline{MOE}$ Low Time		1/2 BUFCLK Period			

NOTE: ↓ Indicates falling edge. ↑ Indicates rising edge.

* BUFCLK is an internal signal which indicates the period of Buffer Memory Access Cycle. These specifications can be tested when the period of BCLK pin is the same as the period of Buffer Memory Access Cycles (i.e., Register 7FH, Bits 6 and 7 are 1 and 0, respectively). The minimum Buffer Access Cycle (BUFCLK) is 100 ns.

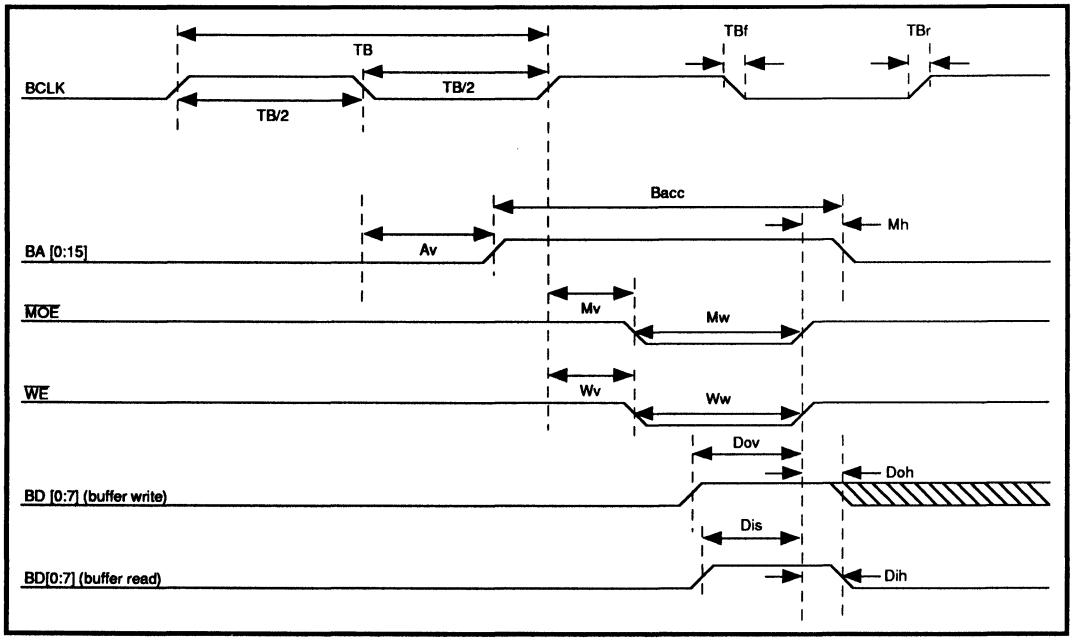

FIGURE 12: Buffer Memory Read/Write Timing

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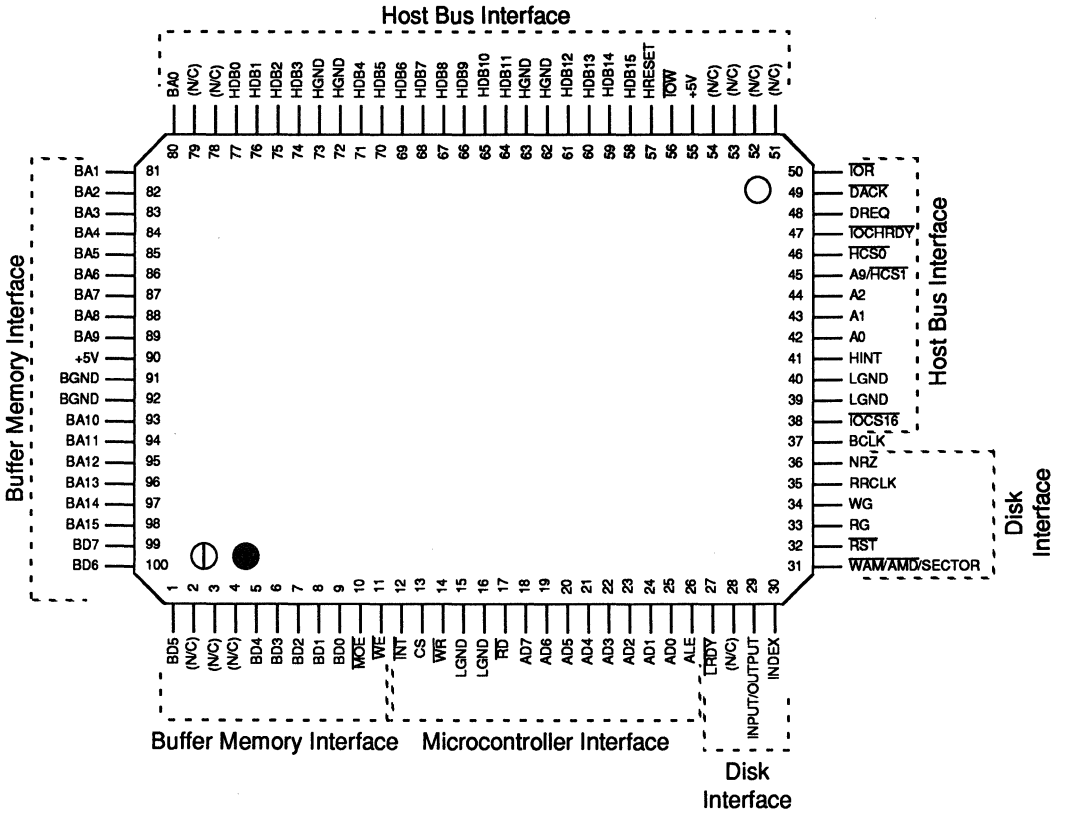
SSI 32C4651
PC AT/XT Combo Disk Controller 26 Mbit/s

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



100-pin QFP

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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silicon systems®
A TDK Group Company

SSI 32C9000
PC AT Combo Disk Controller 32 Mbits/s
Advance Information

December 1991

DESCRIPTION

The SSI 32C9000 is a CMOS VLSI device which integrates major portions of the hardware needed to build a PC AT driven hard disk drive. The SSI 32C9000 is one of the family of Silicon Systems' single chip disk controllers. The SSI 32C9000's place in the Silicon Systems' chip family is illustrated in the hierarchy chart in Figure 1. It provides most of the disk controller functional circuitry necessary to build an embedded AT-disk drive.

The SSI 32C9000 is capable of supporting interleaved data transfer rate up to 32 Mbit/s. This chip represents a major reduction in part count when used with the SSI 32P3010 Pulse Detector, the SSI 32D5373, the SSI 32R2010 Read/Write device, and the SSI 32D4661 Time Base Generator device, implementing a low power and cost efficient 5-chip set intelligent drive solution.

The SSI 32C9000 includes a four port Buffer Manager, a storage controller, and a high performance AT host interface block that incorporates an extensive hardware support — including 24 mA drivers — for the PC AT and other compatible interfaces.

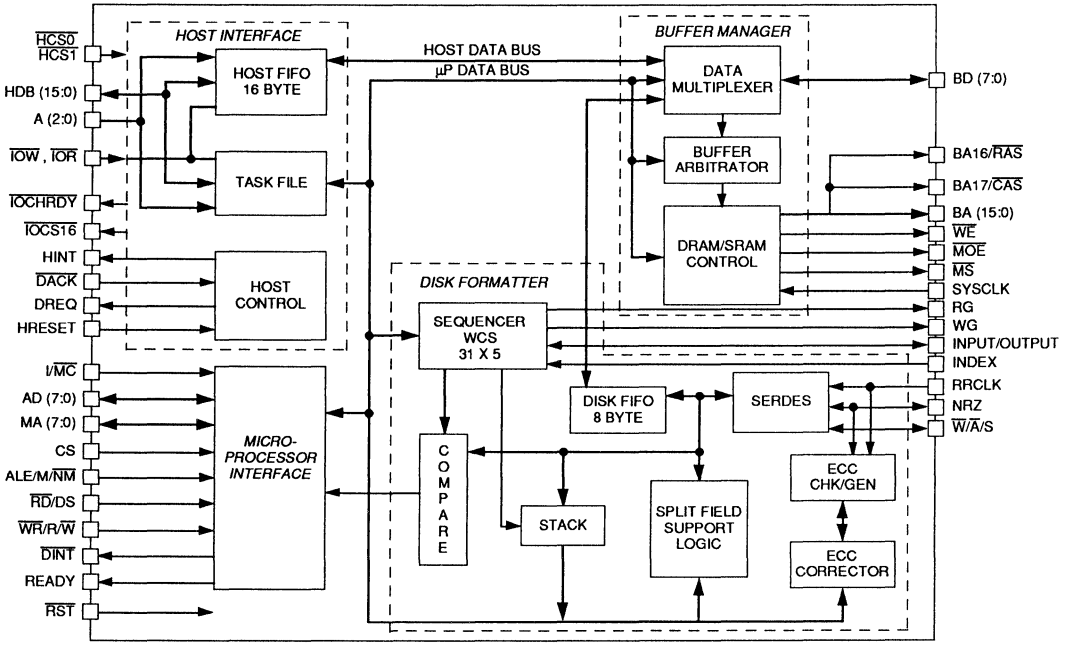
The SSI 32C9000 performs all the controller functions for the peripheral device, such as serialization/deserialization; ECC generation and checking on the data stream, and CRC generation and checking on the header of the data stream.

FEATURES

- **PC AT Bus Interface**
  - **Single chip PC AT Controller**
  - **Direct bus interface logic with on-chip 24 mA drivers**
  - **Logic for daisy chaining 2 embedded ATA drives**
  - **Buffer transfer in single or burst mode DMA and PIO modes**
  - **Automatic command decoding of write, write multiple, and format commands**
  - **Supports ATA's Read Multiple and Write Multiple commands**
  - **Supports Multi-Sector transfers without microprocessor intervention**
  - **Automatic updates of the host task file registers in multiple sector transfers**

(Continued)

BLOCK DIAGRAM



SSI 32C9000
PC AT Combo Disk Controller 32 Mbits/s

FEATURES (Continued)

- Buffer Manager
  - Three port buffer access DMA controller plus auto refresh
  - Dedicated Host, Disk, and Microprocessor Buffer RAM address pointers
  - Total Buffer Memory throughput to 16 MByte/s for SRAM and 13.3 MByte/s for DRAM in Page Mode
  - Direct Buffer Memory addressing up to 256 kB Static RAM or 1 MByte/s Dynamic RAM for various timings and sizes
  - Buffer RAM segmentation with flexible segment sizes for 256 bytes to 1 MByte/s
  - Auto-reload host address pointers and transfer counter
- Storage Controller
  - NRZ Data Rates to 32 MBit/s
  - 16-bit CRC on headers
  - 56-bit Computer Generated Error Correction Code on data with "on-the-fly" fast hardware assisted correction circuitry
  - Multiple sector transfer support
  - Supports sector level defect management
  - Sector header or microprocessor based split data field processing logic
  - Highly programmable advanced sequencer organized in 31 x 5 bytes
  - 8-byte stack for header information storage
  - 8-byte disk FIFO
  - Supports programmable sector lengths up to 64K bytes
  - NRZ byte synchronization time out timer
  - Three-index counter providing sector I.D. search and retry limits
- Microprocessor Interface
  - Direct connection of mulitplexed or non-mux'd bus microprocessors
  - Zero wait state internal register access by 68HC11 at 12 MHz and 80C196 at 16 MHz
  - Programmable wait state insertion for faster microprocessors
  - Low order address latched for direct EPROM connection
- Others
  - Internal power down mode
  - Operational at ±10% of 5V
  - Available in 100-pin surface mount QFP

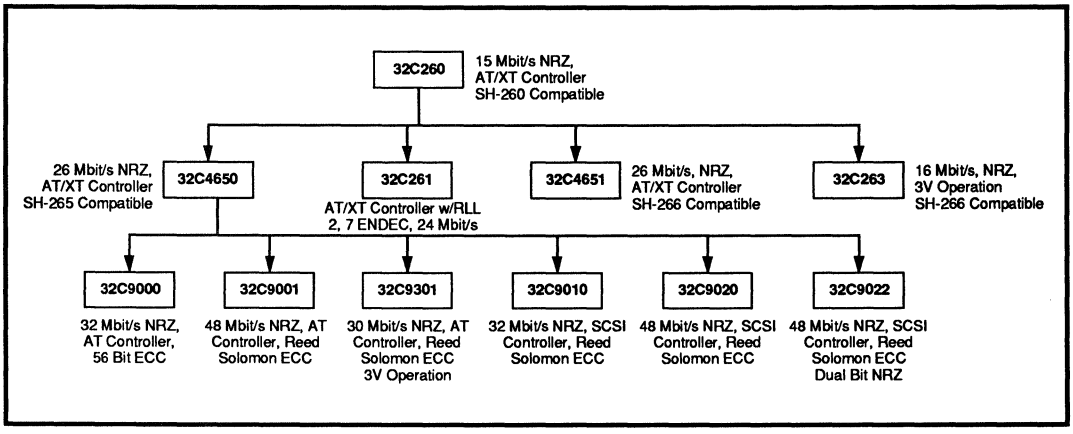


FIGURE 1: Silicon Systems' Disk Controller Chip Hierarchy

FUNCTIONAL DESCRIPTION

The four major functional blocks are:

Microcontroller Interface
Buffer Memory Interface
Disk Formatter
Host Interface

The SSI 32C9000 includes a control sequencer with a writeable control store, buffer RAM controller capable of interleaved address generation, direct ATA bus connections, and configuration/status registers which can be programmed by an external microcontroller. The internal hardware also supports automatic looping of the sequencer program, and the interrupt circuitry relieves the supervising microprocessor of having to poll on the status registers. Access to the control store and registers is accomplished through the microprocessor interface which is optimized for eight-bit, mulitplexed address/data or non-multiplexed processors such as the Intel 80C196 or Motorola 68HC11. **For a complete description of the programmable registers, refer to the SSI 32C9000 Design Guide.**

The device performs all the controller functions for the peripheral device, such as serialization/deserialization; ECC generation, checking, and assisting the local microprocessor in correction of the data stream; and CRC generation and checking on the header stream. It also has the flexibility of defect management and recovery. The contention between the host, the disk request, refresh, and microprocessor requests for buffer RAM access is internally arbitrated and resolved.

PIN DESCRIPTION

The following convention is used in the pin description:

(I) denotes an input
(I/S) denotes a Schmitt trigger input
(O) denotes an output
(I/O) denotes a bidirectional signal
(Z) denotes a tri-state output
(OD) denotes an open drain output

Active low signals are denoted by a bar on top of the signal name and dual function pins are denoted with a slash between the two signals — A9/$\overline{HCS1}$.

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GENERAL

NAME	TYPE	DESCRIPTION
VDD		POWER SUPPLY PIN, VCC
GND		GROUND

HOST INTERFACE

A0:2	I	HOST ADDRESS LINES. The Host Address lines A(2:0) and A9 are used to access the various PC/AT control/status, and data registers.
A9/$\overline{HCS1}$	I	HOST ADDRESS LINE 9/ HOST CHIP SELECT 1. This is a multiplexed input pin. When Register 48H bit 3 is reset this input is HOST ADDRESS LINE 9, when the bit is set this input is HOST CHIP SELECT 1. When configured as active low $\overline{HCS1}$, this input is ignored when $\overline{DACK}$ is asserted.
$\overline{HCS0}$	I	HOST CHIP SELECT 0. This pin selects access to the control, status and data registers. This active low input is ignored when $\overline{DACK}$ is asserted.
$\overline{IOCS16}$	OD	16-BIT DATA TRANSFER. An open drain active low output that indicates that a 16-bit buffer transfer is active.
HINT	O	HOST INTERRUPT. Asserted active high to indicate to the Host that the controller needs attention.
$\overline{IOCHRDY}$	O, Z	I/O CHANNEL READY. Active low, this signal is asserted whenever the internal host FIFO is not ready to transfer data.

PIN DESCRIPTION (Continued)

HOST INTERFACE (Continued)

NAME	TYPE	DESCRIPTION
DREQ	O, Z	DMA REQUEST. The active high DMA Request signal is used during DMA transfer between the Host and the 32C9000.
$\overline{DACK}$	I	DMA ACKNOWLEDGE. This active low signal is used during DMA to complete the DMA handshake for data transfer between the host and the controller.
$\overline{IOR}$	I	INPUT READ SELECT. This pin is asserted by the Host during a Host read operation. When asserted with $\overline{HCS0}$, $\overline{HCS1}$, or $\overline{DACK}$, data from the device is enabled onto the host data bus.
$\overline{IOW}$	I	INPUT WRITE SELECT. Asserted active low by the HOST during a HOST write operation. When asserted with $\overline{HCS0}$, $\overline{HCS1}$, or $\overline{DACK}$, data from the host data bus is strobed into the device.
HRESET	I/S	HOST RESET. This active high signal stops all commands in progress and initializes the control/status registers — see Design Guide for Register Reset conditions. This signal can also "wake up" the device while it is in power down mode.
HDB (15:0)	I/O	HOST DATA BUS. These bits are used for word transfers between the Buffer Memory and the Host; bits (7:0) are used for status, commands, or ECC byte transfers.

DISK INTERFACE

INDEX	I	INDEX. This input is a pulse that occurs once per revolution and defines the start of sector 0.
INPUT/ OUTPUT	I/O	DISK SEQUENCER INPUT/OUTPUT. A general purpose control (output) and status (input) pin configured by the Output Enable Bit of Register 71H, bit 7. At power-on, this pin is an input. As an input, it can be used to synchronize the disk sequencer to an external event. As an output, it is controlled by bit 2 of the Control Field of the disk sequencer.
$\overline{WAM}$/$\overline{AMD}$ SECTOR	I/O	WRITE ADDRESS MARK/ADDRESS MARK DETECT/SECTOR. This pin is configured to operate in Hard or Soft Sector mode by initializing the Disk Formatter Mode Control Register: 4FH, bit 1. In the hard sector mode it is used as the sector input — a pulse on this pin indicates a sector mark is found. In the soft sector mode, an active low output is asserted when formatting to allow writing of address mark. When reading, an active low input indicates an address mark was detected. The device powers up in soft sector mode.
RG	O	READ GATE. This active high output enables the reading of the disk. It is asserted at the beginning of the PLO for header and data field by the sequencer — sequencer Control Field bits 5 and 6. It is automatically deasserted at the end of the CRC or ECC.
WG	O	WRITE GATE. This active high output enables writing onto the disk. It is asserted and deasserted by the sequencer Control Field bits 5 and 6.
RRCLK	I/S	READ/REFERENCE CLOCK. This pin is used in conjunction with the NRZ pin to clock data in and out of the SSI 32C9000 device. This input must be glitch-free to ensure correct operation of the chip.
NRZ	I/O	NON RETURN TO ZERO. This signal is the serial read data input from the disk drive when the read gate signal is asserted; it is the write data output to the disk drive when the write gate signal is asserted.

MICROPROCESSOR INTERFACE

NAME	TYPE	DESCRIPTION
$\overline{RST}$	I	RESET. An active low asserted input generates a component reset that holds the internal registers of the SSI 32C9000 at reset, stops all operations within the chip, and deasserts all output signals. All input/output signals and Host outputs are set to the high-Z state.
ALE/M/$\overline{NM}$	I	ADDRESS LATCH ENABLE/MULTIPLEXED/NON-MULTIPLEXED ADDRESS SELECT. When tied high or left floating after reset, the microprocessor interface is configured as non-multiplexed. When driven low, then the microprocessor interface is configured as multiplexed. In this case this pin functions as the address latch enable, and the MA(7:0) pins are the demultiplexed address outputs.
CS	I	CHIP SELECT. This signal must be asserted high for all microprocessor accesses to the registers of this chip.
$\overline{WR}$/R/$\overline{W}$	I	WRITE STROBE/READ/WRITE. In the Intel bus mode, when an active low signal is present with CS signal high, the data on the AD0:7 is written to the internal registers. In the Motorola bus mode, this signal acts as the R/$\overline{W}$ signal. A high on this input along with the $\overline{RD}$/DS signal high and the CS signal asserted high indicates a read operation. A low on this input along with the $\overline{RD}$/DS signal asserted high and the CS signal asserted high indicates a write operation. See table below.

I/$\overline{MC}$	CS	$\overline{WR}$/R/$\overline{W}$	$\overline{RD}$/DS	Action	Intel/Moto
High	High	Low	High	Write to internal registers.	I
High	High	High	Low	Read from internal registers.	I
Low	High	Low	High	Write to internal registers.	M
Low	High	High	High	Read from internal registers.	M
X	Low	X	X	No action.	I or M

Note: X denotes don't care.

$\overline{RD}$/DS	I	READ STROBE/DATA STROBE. In the Intel bus mode, when an active low signal is present with CS signal high, internal registers will be accessed. In the Motorola mode, this signal acts as the DS signal. A high on the DS, R/$\overline{W}$, and the CS signals, indicates a read operation. A low on the R/$\overline{W}$ signal, highs on both the DS and the CS, indicates a write operation to the internal registers.
$\overline{DINT}$	O, OD, Z	INTERRUPT. An active low signal indicates the controller is requesting microprocessor service. This signal is programmable for either a push-pull with an internal pull up resistor or open-drain output circuit. This signal powers up in the high-Z state. Disk Formatter Mode Control Register, 4FH: bit 3 set high, programs this pin as a push-pull, and when set low programs it as an open drain output signal.
AD7:0	I/O	ADDRESS/DATA BUS. When configured in the multiplexed mode, these lines are multiplexed, bidirectional address and data path to the microprocessor. During the beginning of the memory cycle the bus captures the low order byte of the microprocessor address. These lines provide communication with the controller device's internal registers and the buffer memory. When configured in the non-multiplexed mode, these lines are bidirectional data lines.
MA(7:0)	I/O	MICROPROCESSOR ADDRESS BUS: This 8-bit output bus is the AD(7:0) bus latched by the ALE pin during the low order address phase of a multiplexed microprocessor. These signals are non-multiplexed address input when used with a non-multiplexed bus microprocessor.

8

PIN DESCRIPTION (Continued)

MICROPROCESSOR INTERFACE (Continued)

NAME	TYPE	DESCRIPTION
READY	O	READY: When this signal is deasserted low, the microprocessor inserts wait states to allow time for the chip to respond to the access. Wait states are programmed by Buffer Mode Control Register — 53H: bits 7-6.
I/$\overline{MC}$	I	INTEL/MOTOROLA: This signal selects the microprocessor interface to be used. When this signal is asserted high, it selects the Intel bus control interface. When this signal is deasserted low, it selects the Motorola bus control interface. This signal has an internal pull-up to allow the default selection of the Intel bus control interface.

BUFFER MANAGER INTERFACE

BA0:15	O	BUFFER MEMORY ADDRESS LINES 0:15. These sixteen outputs provide address lines for the dynamic memory or static memory chips used to implement the buffer memory.
BA16/$\overline{RAS}$	O	BUFFER MEMORY ADDRESS 16: In SRAM mode, this pin generates the address:A16 for direct connection to a Static RAM address line 16. BUFFER ROW ADDRESS STROBE: This active low output signal is generated to strobe the row address into the dynamic RAMs. It is intended to be directly tied to the RAM's input control pin.
BA17/$\overline{CAS}$	O	BUFFER MEMORY ADDRESS 17: In SRAM mode, this pin generates the address:A17 for direct connection to a Static RAM address line 17. COLUMN ADDRESS STROBE: This active low output signal is generated to strobe the column address into the dynamic RAM devices.
BD0:7	I/O	BUFFER MEMORY DATA BUS. 7 through 0. This bidirectional Data Bus connects directly to the buffer memory.
$\overline{MOE}$	O	MEMORY OUTPUT ENABLE. This active low output controls the enabling of data onto the data bus by the dynamic RAM's or to indicate when every buffer memory access is active in SRAM mode.
$\overline{WE}$	O	WRITE ENABLE. This active low output signal is used to strobe the data into the RAMs from the Data bus. For both buffer memory applications, this line is tied directly to the SRAM or DRAM control pin.
SYSCLK	I	SYSTEM CLOCK. This signal is used to synchronize the buffer RAM access, including the generation of memory address lines, write enable $\overline{WE}$, and memory output enable $\overline{MOE}$. In power down mode, this signal is shut off from the internal logic and hence buffer memory access is inhibited.
$\overline{MS}$	O	MEMORY SELECT. This signal is asserted low when there is a read or write access to the buffer SRAM. This signal is used to deselect the buffer RAM when not in use so that power can be saved.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Maximum limits indicate where a permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC operating characteristics.

PARAMETER	RATING	UNIT
Power Supply Voltage, VCC	7	V
Ambient Temperature	0 to 70	°C
Storage Temperature	-65 to 150	°C
Power Dissipation	750	mW
Input, Output pins	-0.5 to VCC+0.5	V

DC ELECTRICAL CHARACTERISTICS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
VCC	Power Supply Voltage		4.5		5.5	V
ICC	Supply Current	Operating			40	mA
ICCS	Supply Current	Note 1			500	µA
VIL	Input Low Voltage	Note 2	-0.5		0.8	V
VIH	Input High Voltage	Note 2	2.0		VCC +0.5	V
VIL	Input Low Voltage	Note 3	-0.5		0.9	V
VIH	Input High Voltage	Note 3	1.9		VCC +0.5	V
VOL	Output Low Voltage	Note 4		0.4		V
VOL	Output Low Voltage	Note 5		0.5		V
VOH	Output High Voltage	IOH = -400 µA			2.4	V
IL	Input Leakage Current	0 < VIN < VCC	-10		10	µA
CIN	Input Capacitance				10	pF
COUT	Output Capacitance			10		pF

Note: (1) Synchronization and Clock Control Register, 7FH: bits 3 and 4 set. RRCLK and SYSCLK internally inhibited.
(2) All interface signals except Schmitt inputs.
(3) Schmitt triggered signals only.
(4) All interface pins except Host Interface pins. IOL= 2mA.
(5) Host Interface pins, IOL=24mA.

AC ELECTRICAL CHARACTERISTICS

The following timing assume that all non-Host Bus output pins drive one Schottky TTL load in parallel with 50 pF, all Host Bus output pins will drive a 300 pF load, and all inputs are at TTL levels. The MIN and MAX timings conform to the operating ranges of a power supply voltage of 5V ± 10% and an ambient temperature of 0°C to 70°C.

SSI 32C9000
PC AT Combo Disk Controller 32 Mbits/s

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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SSI 32C9001
PC-AT Combo Controller With Reed Solomon, 48 Mbit/s
Advance Information

December 1991

DESCRIPTION

The SSI 32C9001 is a CMOS VLSI device which integrates major portions of the hardware needed to build a PC AT driven hard disk controller. The SSI 32C9001 is one of the family of Silicon Systems' single chip disk controllers. The SSI 32C9001's place in the Silicon Systems' chip family is illustrated in the hierarchy chart in Figure 1. It provides most of the functional circuitry necessary to build an "ATA" embedded disk.

The SSI 32C9001 is capable of supporting interleaved data transfer rate up to 48 Mbit/s. This chip represents a major reduction in part count when used with the SSI 32P3000 Pulse Detector and Filter combo, the SSI 32R2010 Read/Write device, SSI 32D5391 Data Separator, and the SSI 32H4631 Servo and Motor Speed Controller device, implementing a low power and cost efficient 5-chip set Multiplexed Microprocessors drive solution for 48 Mbit/s applications.

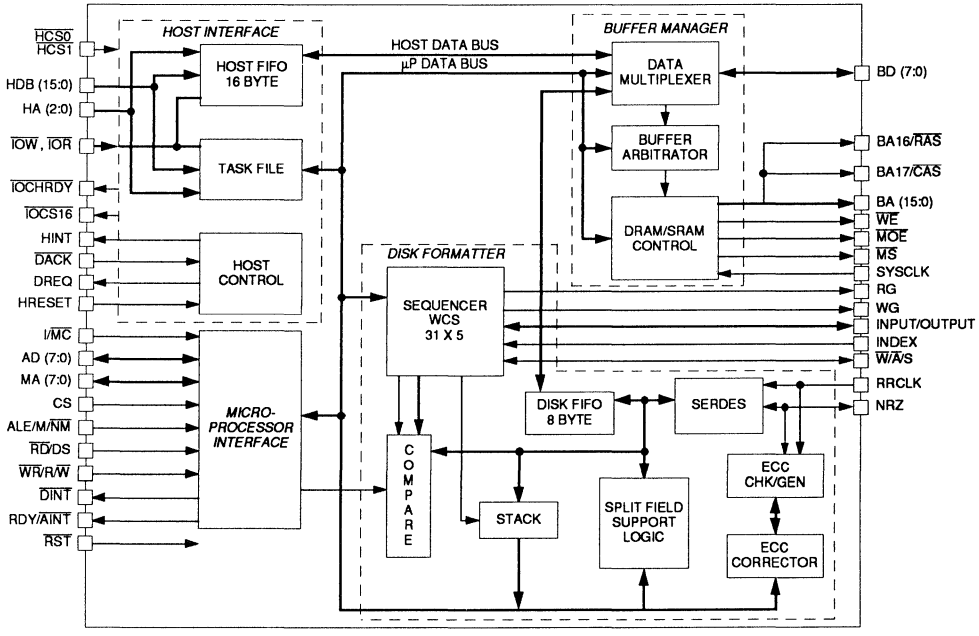
(Continued)

FEATURES

- **PC AT Bus Interface**
  - **Single Chip PC AT Controller**
  - **Direct bus interface logic with on-chip 24 mA drivers**
  - **Logic for daisy chaining 2 embedded ATA drives**
  - **Supports 48 Mbit/s concurrent disk transfer on a 6 M words/s PC-AT in PIO or single or EISA compatible burst DMA mode — type B**
  - **Automatic command decoding of write, write multiple, and format commands.**
  - **Automatic updates of the host task file registers in multiple sector transfers**
- **Buffer Manager**
  - **Supports Buffer Memory throughput to 20 Mbytes/s SRAM or 17.2 Mbytes/s DRAM**
  - **Direct Buffer Memory addressing up to 256 kB Static RAM or 1 MB Dynamic RAM for various timings and sizes**

(Continued)

BLOCK DIAGRAM



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SSI 32C9001
PC-AT Combo Controller
With Reed Solomon, 48 Mbit/s

DESCRIPTION (continued)

The SSI 32C9001 includes a dual port Buffer Manager, a storage controller, and a high performance AT host interface block that incorporates an extensive hardware support — including 24 mA drivers — for the PC AT and other compatible interfaces.

The SSI 32C9001 performs all the controller functions for the peripheral device, such as serialization/deserialization; ECC generation and checking on the data stream, and CRC generation and checking on the header of the data stream.

FEATURES (continued)

- **Buffer Manager (continued)**
  - **Buffer RAM segmentation with flexible segment sizes from 256 bytes to 1Mbyte/s**
  - **Dedicated Host, Disk, and Microprocessor Buffer RAM address pointers**
- **Storage Controller**
  - **NRZ Data Rates up to 48 Mbit/s**
  - **Selectable 16-bit CRC or 88 bit ECC polynomial with "on-the-fly" fast hardware correction circuitry**
  - **Multiple sector transfer support without microprocessor intervention**
  - **Highly programmable Advanced sequencer organized in 31 x 5 bytes**
  - **Support sector level defect management**
  - **Sector header or microprocessor based split data field processing logic**
- **Microprocessor Interface**
  - **Supports both multiplexed and non-multiplexed microprocessor support**
  - **Separate host and disk interrupts**
- **Others**
  - **Internal power down mode**
  - **Operational at ±10% of 5V**
  - **Available in 100-pin surface mount QFP**

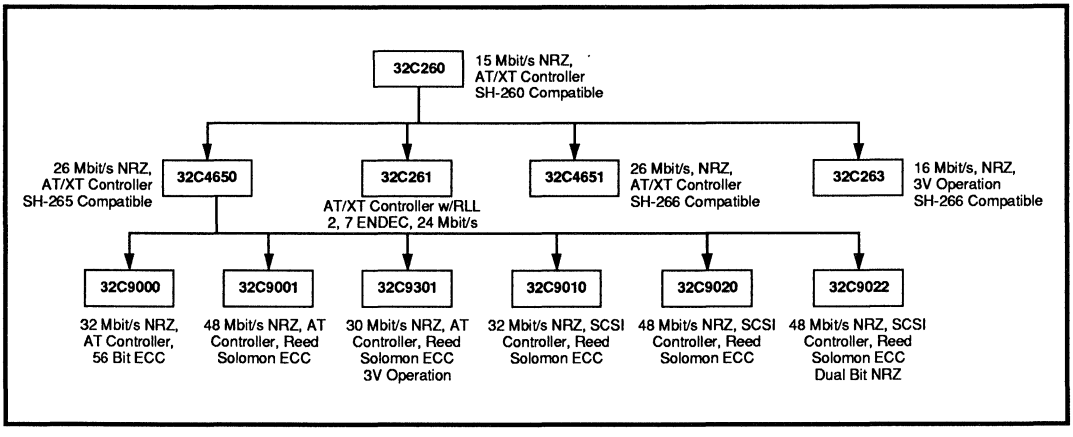

FIGURE 1: Silicon Systems' Disk Controller Chip Hierarchy

FUNCTIONAL DESCRIPTION

The four major functional blocks are:

Microcontroller Interface
Buffer Memory Interface
Disk Formatter
Host Interface

The SSI 32C9001 includes a control sequencer with a writeable control store, buffer RAM controller capable of interleaved address generation, direct ATA bus connections, and configuration/status registers which can be programmed by an external microcontroller. The internal hardware also supports automatic looping of the sequencer program, and the interrupt circuitry relieves the supervising microprocessor of having to poll on the status registers. Access to the control store and registers is accomplished through the microprocessor interface which is optimized for eight-bit, mulitplexed address/data processors such as Intel's 80C196 or non-multiplexed microprocessors — such as Motorola's 68HC11. **For a complete description of the programmable registers, refer to the SSI 32C9001 Design Guide.**

The device performs all the controller functions for the peripheral device, such as serialization/deserialization; ECC generation, checking, and correction assistance; and CRC generation and checking on the header stream. It also has the flexibility of defect management and recovery. The contention between the host, disk, microprocessor, and refresh requests for buffer RAM access is internally arbitrated and resolved.

PIN DESCRIPTION

The following convention is used in the pin description:

(I) denotes an input
(I/S) denotes a Schmitt trigger input
(O) denotes an output
(I/O) denotes a bidirectional signal
(Z) denotes a tri-state output
(OD) denotes an open drain output

Active low signals are denoted by a bar on top of the signal name and dual function pins are denoted with a slash between the two signals — A9/$\overline{\text{HCS1}}$.

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GENERAL

NAME	TYPE	DESCRIPTION
VDD		POWER SUPPLY PIN, VCC
GND		GROUND

HOST INTERFACE

A0:2	I	HOST ADDRESS LINES. The Host Address lines A(2:0) and A9 are used to access the various PC/AT control/status, and data registers.
A9/$\overline{\text{HCS1}}$	I	HOST ADDRESS LINE 9/HOST CHIP SELECT 1. This is a multiplexed input pin. When Register 48H-bit 3 is reset this input is HOST ADDRESS LINE 9, when the bit is set this input is HOST CHIP SELECT 1. When configured as active low $\overline{\text{HCS1}}$, this input is ignored when $\overline{\text{DACK}}$ is asserted.
$\overline{\text{HCS0}}$	I	HOST CHIP SELECT 0. This pin selects access to the control, status and data registers. This active low input is ignored when $\overline{\text{DACK}}$ is asserted.
$\overline{\text{IOCS16}}$	OD	16 BIT DATA TRANSFER. An open drain active low output that indicates that a 16-bit buffer transfer is active.
HINT	O	HOST INTERRUPT. Asserted active high to indicate to the Host that the controller needs attention.

PIN DESCRIPTION (Continued)

HOST INTERFACE (Continued)

NAME	TYPE	DESCRIPTION
$\overline{\text{IOCHRDY}}$	O,Z	I/O CHANNEL READY. Active low, this signal is asserted whenever the internal host FIFO is not ready to transfer data.
DREQ	O,Z	DMA REQUEST. The active high DMA Request signal is used during DMA transfer between the Host and the SSI 32C9001.
$\overline{\text{DACK}}$	I	DMA ACKNOWLEDGE. This active low signal is used during DMA to complete the DMA handshake for data transfer between the host and the controller.
$\overline{\text{IOR}}$	I	INPUT READ SELECT. This active low pin is asserted by the Host during a Host read operation. When asserted with $\overline{\text{HCS0}}$, $\overline{\text{HCS1}}$, or $\overline{\text{DACK}}$, data from the device is enabled onto the host data bus.
$\overline{\text{IOW}}$	I	INPUT WRITE SELECT. Asserted active low by the HOST during a HOST write operation. When asserted with $\overline{\text{HCS0}}$, $\overline{\text{HCS1}}$, or $\overline{\text{DACK}}$, data from the host data bus is strobed into the device.
HRESET	I/S	HOST RESET. This active high signal stops all commands in progress and initializes the control/status registers — see Design Guide for Register Reset conditions. This signal can also "wake up" the device while it is in power down mode.
HDB (15:0)	I/O	HOST DATA BUS. These bits are used for word transfers between the Buffer Memory and the Host; bits (7:0) are used for status, commands, or ECC byte transfers.

DISK INTERFACE

INDEX	I	INDEX. This input is a pulse that occurs once per revolution and defines the start of sector 0.
INPUT/	I/O	DISK SEQUENCER INPUT/OUTPUT. A general purpose control (output) and status (input) pin configured by the Output Enable Bit of Register 71H, bit 7.
OUTPUT		At power-on, this pin is an input. As an input, it can be used to synchronize the disk sequencer to an external event. As an output, it is controlled by bit 2 of the Control Field of the disk sequencer.
$\overline{\text{WAM}}$/ $\overline{\text{AMD}}$/ SECTOR	I/O	WRITE ADDRESS MARK/SECTOR/ADDRESS MARK DETECT. This pin is configured to operate in Hard or Soft Sector mode by initializing the Disk Formatter Mode Control Register: 4FH, bit 1. In the hard sector mode it is used as the sector input — a pulse on this pin indicates a sector mark is found. In the soft sector mode, an active low output is asserted when formatting to allow writing of address mark. When reading, an active low input indicates an address mark was detected. The device powers up in soft sector mode.
RG	O	READ GATE. This active high output enables the reading of the disk. It is asserted at the beginning of the PLO for header and data field by the sequencer — sequencer Control Field bits 5 and 6. It is automatically deasserted at the end of the CRC or ECC.
WG	O	WRITE GATE. This active high output enables writing onto the disk. It is asserted and deasserted by the sequencer Control Field bits 5 and 6.

DISK INTERFACE (Continued)

NAME	TYPE	DESCRIPTION
RRCLK	I/S	READ/REFERENCE CLOCK. This pin is used in conjunction with the NRZ pin to clock data in and out of the SSI 32C9001 device. This input must be glitch-free to ensure correct operation of the chip.
NRZ	I/O	NON RETURN TO ZERO. This signal is the serial read data input from the disk drive when the read gate signal is asserted; it is the write data output to the disk drive when the write gate signal is asserted.

MICROPROCESSOR INTERFACE

$\overline{RST}$	I	RESET. An asserted active low input generates a component reset that holds the internal registers of the SSI 32C9001 at reset, stops all operations within the chip, and deasserts all output signals. All input/output signals and Host outputs are set to the high-Z state.
ALE/M/$\overline{NM}$	I	ADDRESS LATCH ENABLE/MULTIPLEXED/NON-MULTIPLEXED ADDRESS SELECT. When tied high or left floating after reset, the microprocessor interface is configured as non-multiplexed. When driven low, then the microprocessor interface is configured as multiplexed. In this case this pin functions as the address latch enable, and the MA(7:0) pins are the demultiplexed address outputs.
CS	I	CHIP SELECT. This signal must be asserted high for all microprocessor accesses to the registers of this chip.
$\overline{WR}$/R/$\overline{W}$	I	WRITE STROBE/READ/WRITE. In the Multiplexed Microprocessors bus mode, when an active low signal is present with CS signal asserted high, the data on the AD0:7 is written to the internal registers. In the Non-Multiplexed Microprocessors bus mode, this signal acts as the R/$\overline{W}$ signal. A high on this input along with the $\overline{RD}$/DS signal high and the CS signal asserted high indicates a read operation. A low on this input along with the $\overline{RD}$/DS signal asserted and the CS signal asserted high indicates a write operation. See table below.

I/$\overline{MC}$	CS	$\overline{WR}$/R/$\overline{W}$	$\overline{RD}$/DS	Action	Mux/Non-Mux
High	High	Low	High	Write to internal registers.	M
High	High	High	Low	Read from internal registers.	M
Low	High	Low	High	Write to internal registers.	N
Low	High	High	High	Read from internal registers.	N
X	Low	X	X	No action.	M or N

Note: X denotes don't care.

$\overline{RD}$/DS	I	READ STROBE/DATA STROBE. In the Multiplexed Microprocessors bus mode, when an active low signal is present with CS signal high, internal registers will be accessed. In the Non-Multiplexed Microprocessors mode, this signal acts as the DS signal. A high on the DS, R/$\overline{W}$, and the CS signals, indicates a read operation. A low on the R/$\overline{W}$ signal, highs on both the DS and the CS, indicates a write operation to the internal registers.
$\overline{DINT}$	O, OD, Z	INTERRUPT. An active low signal indicates the controller is requesting microprocessor service from the disk side. This signal is programmable for either a push-pull with an internal pull up resistor or open-drain output circuit. This signal powers up in the high-Z state. Disk Formatter Mode Control Register, 4FH: bit 3 set high, programs this pin as a push-pull, and when set low programs it as an open drain output signal.

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MICROPROCESSOR INTERFACE (Continued)

NAME	TYPE	DESCRIPTION
AD7:0	I/O	ADDRESS/DATA BUS. When configured in the Multiplexed Microprocessors mode, these lines are multiplexed, bidirectional data path to the microprocessor. During the beginning of the memory cycle the bus captures the low order byte of the microprocessor address. These lines provide communication with the controller device's internal registers and the buffer memory. When configured in the Non-Multiplexed Microprocessors mode, these lines are bidirectional data lines.
MA(7:0)	I/O	MICROPROCESSOR ADDRESS BUS: This 8-bit output bus is the AD(7:0) bus latched by the ALE pin during the low order address phase of an Multiplexed Microprocessors type microprocessor cycle. These signals are nonmultiplexed address input when used with a non-multiplexed bus microprocessor — Non-Multiplexed Microprocessors interface.
READY/ $\overline{\text{AINT}}$	O	READY: When this signal is deasserted low, the microprocessor inserts wait states to allow time for the chip to respond to the access. Wait states are programmed by Buffer Mode Control Register — 53H: bits 7-6.
$\overline{\text{AINT}}$	O, OD, Z	AT BUS INTERRUPT. An active low signal indicates the controller is requesting microprocessor service from the AT host bus side. This signal is programmable for either a push-pull with an internal pull up resistor or open-drain output circuit. This signal powers up in the high-Z state. Disk Formatter Mode Control Register, 4FH: bit 3 set high, programs this pin as a push-pull, and when set low programs it as an open drain output signal.
I/$\overline{\text{MC}}$	I	INTEL/MOTOROLA: This signal selects the microprocessor interface to be used. When this signal is asserted high, it selects the Intel bus control interface. When this signal is deasserted low, it selects the Motorola bus control interface. This signal has an internal pull-up to allow the default selection of the Intel bus control interface.

BUFFER MANAGER INTERFACE

BA0:15	O	BUFFER MEMORY ADDRESS LINES 0:15. These sixteen outputs provide address lines for the dynamic memory or static memory chips used to implement the buffer memory.
BA16/$\overline{\text{RAS}}$	O	BUFFER MEMORY ADDRESS 16: In SRAM mode, this pin generates the address:A16 for direct connection to a Static RAM address line 16. BUFFER ROW ADDRESS STROBE: This active low output signal is generated to strobe the row — high order — address into the dynamic RAMs. It is intended to be directly tied to the RAMs input control pin.
BA17/$\overline{\text{CAS}}$	O	BUFFER MEMORY ADDRESS 17: In SRAM mode, this pin generates the address:A17 for direct connection to a Static RAM address line 17. COLUMN ADDRESS STROBE: This output signal is generated to strobe the column — low order address — into the dynamic RAM devices.
BD0:7	I/O	BUFFER MEMORY DATA BUS. 7 through 0. The bidirectional Data Bus connects directly to the buffer memory. This bus is designed for high speed data transfer.
BDP	I/O	BUFFER MEMORY DATA PARITY. This signal provides odd parity for the buffer memory data bus during transfers to/from the buffer memory.

BUFFER MANAGER INTERFACE (Continued)

NAME	TYPE	DESCRIPTION
$\overline{MOE}$	O	MEMORY OUTPUT ENABLE. This active low output controls the enabling of data onto the data bus by the dynamic RAMs or to indicate when every buffer memory access is active in SRAM mode.
$\overline{WE}$	O	WRITE ENABLE. This active low output signal is used to strobe the data into the RAMs from the Data bus. For both buffer memory applications, this line is tied directly to the SRAM or DRAM control pin.
SYSCLK	I	SYSTEM CLOCK. This signal is used to synchronize the buffer RAM access, including the generation of memory address lines, write enable $\overline{WE}$, and memory output enable $\overline{MOE}$. In power down mode, this signal is shut off from the internal logic and hence buffer memory access is inhibited.
$\overline{MS}$	O	Memory selected, asserted active low.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC operating characteristics.

PARAMETER	RATING	UNIT
Power Supply Voltage, VCC	7	V
Ambient Temperature	0 to 70	°C
Storage Temperature	-65 to 150	°C
Power Dissipation	220	mW
Input, Output pins	-0.5 to VCC+0.5	V

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ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VCC Power Supply Voltage		4.5		5.5	V
ICC Supply Current				40	mA
ICCS Supply Current	Note 1			5	mA
VIL Input Low Voltage		-0.5		0.8	V
VIH Input High Voltage		2.0		VCC+0.5	V
VOL Output Low Voltage	Note 2			0.4	V
VOL Output Low Voltage	Note 3			0.5	V
VOH Output High Voltage IOH = -400 µA				2.4	V
IL Input Leakage Current 0 < VIN < VCC		-10		10	µA
CIN Input Capacitance				10	pF
COUT Output Capacitance				10	pF

Note: (1) Synchronization and Clock Control Register, 7FH: bits 3 and 4 set. RRCLK and SYSCLK internally inhibited.
(2) All interface pins except Host Interface pins. IOL= 2mA.
(3) Host Interface pins, IOL=24mA.

SSI 32C9001
PC-AT Combo Controller
With Reed Solomon, 48 Mbit/s

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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SSI 32C9010
SCSI Combo Controller
32 Mbit/s; single bit NRZ interface
Advance Information

December 1991

DESCRIPTION

The SSI 32C9010 is a CMOS VLSI device which integrates major portions of the hardware needed to build a SCSI driven hard disk drive. The SSI 32C9010 is one of the family of Silicon Systems' single chip disk controllers. The SSI 32C9010's place in the Silicon Systems' chip family is illustrated in the hierarchy chart in Figure 1. It provides most of the disk controller functional circuitry necessary to build an embedded SCSI-disk drive.

The SSI 32C9010 is capable of supporting interleaved data transfer rate up to 32 Mbit/s. This chip represents a major reduction in part count when used with the SSI 32P3000 Pulse Detector, the SSI 32D537, the SSI 32R2010 Read/Write device, and the SSI 32H4631 Servo and Motor Speed Controller device, implementing a low power and cost efficient 5-chip set 32 Mbit intelligent drive solution.

The SSI 32C9010 includes a four port Buffer Manager, a storage controller and an extensive hardware support, including 48 mA drivers, for the SCSI and other compatible interfaces.

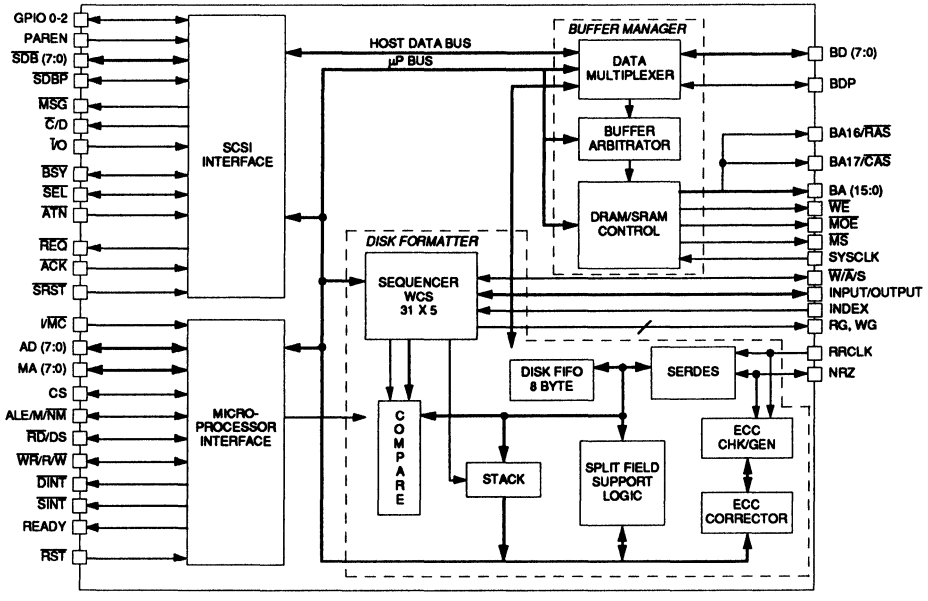
The SSI 32C9010 performs all the controller functions for the peripheral device, such as serialization/deserialization; ECC generation and checking on the data stream, and CRC generation and checking on the header of the data stream.

FEATURES

- **SCSI Bus Interface**
  - **ANSI X3.131-1990 Rev 10C SCSI-2 specification for target devices**
  - **Direct bus interface logic with on-chip 48 mA drivers**
  - **Synchronous transfer rates up to 10 Mbyte/s; 5 Mbyte/s asynchronous**
  - **Parity generation and checking**
  - **High level SCSI sequences without microprocessor intervention**
  - **4-byte Command FIFO supports execution of multiple commands**
  - **Supports SCSI-2 tagged queuing**
  - **SCSI CDB Group Codes decoded "on-the-fly"**
  - **Sixteen-byte data FIFO between the DMA and SCSI channel**
  - **SCSI autodisconnect and reconnect operation supported**

(Continued)

BLOCK DIAGRAM



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SSI 32C9010
SCSI Combo Controller
32 Mbit/s; single bit NRZ interface

FEATURES (Continued)

- Buffer Manager
  - Buffer Memory throughput to 20 MByte/s for SRAM and 17.2 MByte/s for DRAM in Page Mode
  - Up to 256 kB Static RAM or 1MB Dynamic RAM support
  - Buffer RAM segmentation with flexible segment sizes for 256 bytes to 1MBytes
  - Dedicated Host, Disk, and Microprocessor Buffer RAM address pointers
  - Internal buffer protection circuit provides buffer integrity
- Storage Controller
  - NRZ Data Rates to 32Mbit/s--single bit NRZ interface to the Data Separator
  - 88-bit Reed Solomon with "on-the-fly" fast hardware correction circuitry
  - Capable of correcting four 10-bit symbols in error
  - Guaranteed to correct one 31-bit burst or two 11-bit bursts
  - Hardware on-the-fly correction selectable between 11 or 31-bit single burst error within a quarter sector time
  - Detects up to 51-bit burst or three 11-bit burst
  - Multiple sector transfer support
  - Sector header or microprocessor based split data field processing logic
  - Advanced sequencer organized in 31 x 5 bytes
- Microprocessor Interface
  - Supports both Multiplexed or Non-multiplexed family of microprocessors
  - Separate disk and host interrupts
- Others
  - Internal power down mode
  - Available in 100-pin QFP

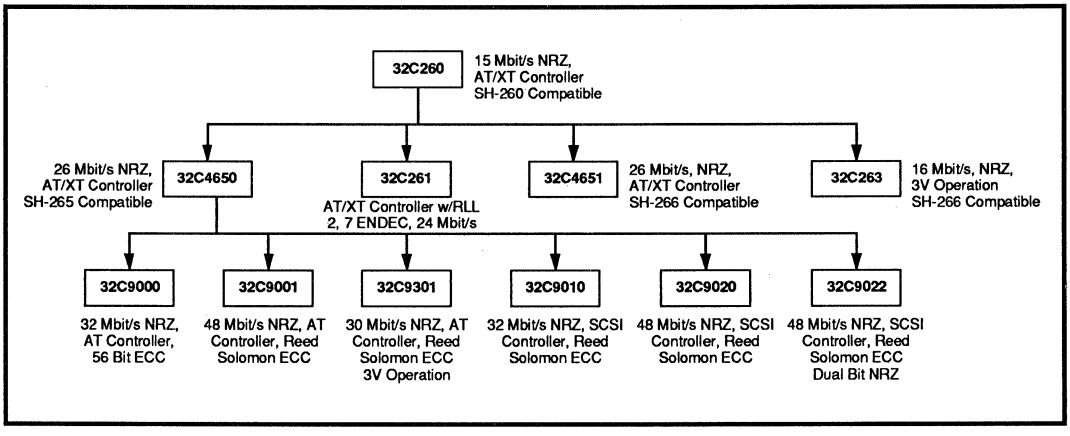

FIGURE 1: Silicon Systems' Disk Controller Chip Hierarchy

FUNCTIONAL DESCRIPTION

The four major functional blocks are:

Microcontroller Interface
Buffer Memory Interface
Disk Formatter
Host Interface

The SSI 32C9010 includes a control sequencer with a writeable control store, buffer RAM controller capable of interleaved address generation, direct SCSI bus connections, and configuration/status registers which can be programmed by an external microcontroller. The internal hardware also supports automatic looping of the sequencer program, and the interrupt circuitry relieves the supervising microprocessor of having to poll on the status registers. Access to the control store and registers is accomplished through the microprocessor interface which is optimized for eight-bit, mulitplexed address/data or non-multiplexed processors such as the Intel 80C196 or Motorola 68HC11. **For a complete description of the programmable registers, refer to the SSI 32C9010/9020 Design Guide.**

The device performs all the controller functions for the peripheral device, such as serialization/deserialization; ECC generation, checking, and correction on the data stream; and CRC generation and checking on the header stream. It also has the flexibility of defect management and recovery. The contention between the host request and the disk request for buffer RAM access is internally arbitrated and resolved utilizing data FIFOs.

PIN DESCRIPTION

The following convention is used in the pin description:

(I) denotes an input
(O) denotes an output
(Z) denotes a tri-state output
(OD) denotes an open drain output

GENERAL

NAME	TYPE	DESCRIPTION
VDD		POWER SUPPLY PIN, VCC
GND		GROUND

HOST INTERFACE

$\overline{SDBP}$	I/O	SCSI DATA BUS PARITY. Odd parity bit for the SCSI data bus.
$\overline{SDB7\text{-}0}$	I/O	SCSI DATA BUS BITS 7-0.
$\overline{ATN}$	I	ATTENTION. This active low signal is used by the initiator to request a message out phase
$\overline{BSY}$	I/O	BUSY. This active low signal is used to indicate when the bus is active.
$\overline{ACK}$	I	ACKNOWLEDGE. This active low signal is used in the handshake protocol to indicate the completion of a data byte transfer.
$\overline{SRST}$	I	SCSI RESET. This active low signal is used to reset the SCSI controller.
$\overline{MSG}$	O	MESSAGE. This active low signal is used to indicate a message phase.
$\overline{SEL}$	I/O	SELECT. This active low signal is used to indicate either a selection or reselection phase.
$\overline{C}$/D	O	COMMAND/DATA. This signal is used to indicate either a command or data phase.
$\overline{REQ}$	I	REQUEST. This active low signal is used in the handshake protocol to initiate a data byte transfer.
$\overline{I}$/O	I	INPUT/OUTPUT. This signal is used to indicate the direction of data transfer.
PAREN	I	SCSI PARITY ENABLE. This active high signal is used to enable parity checking of the SCSI data bus. Parity checking is disabled when this pin is held low.

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PIN DESCRIPTION (Continued)

DISK INTERFACE

NAME	TYPE	DESCRIPTION
GPIO 0-2	I	INPUT/OUTPUT. These pins are used to indicate the SCSI ID of the target device. The pins can be programmed as outputs for test purposes only.
INDEX	I	INDEX. Input for index pulse received from the drive.
INPUT/ OUTPUT	I/O	DISK SEQUENCER INPUT/OUTPUT. A general purpose control (output) and status (input) pin configured by the Output Enable Bit of Register 71H, bit 7.
		At power-on, this pin is an input. As an input, it can be used to synchronize the disk sequencer to an external event. As an output, it is controlled by bit 2 of the Control Field of the disk sequencer.
$\overline{WAM}/\overline{AMD}$/ SECTOR	I/O	WRITE ADDRESS MARK/SECTOR/ADDRESS MARK DETECT. This pin is used in the hard sector mode as the sector input. A pulse on this pin indicates a sector mark is found. In the soft sector mode, a low level output is asserted during write gate to indicate writing of address mark. During read, a low-level input indicates an address mark was detected. The device powers up in soft sector default mode.
RG	O	READ GATE. During disk data read, this pin is asserted. Active high.
WG	O	WRITE GATE. During disk data write, this pin is asserted. Active high.
RRCLK	I	READ/REFERENCE CLOCK. This pin is used in conjunction with the NRZ pin to clock data in and out of the SSI 32C9010 device.
NRZ	I/O	NON RETURN TO ZERO. This signal is the read data input from the disk drive when the read gate signal is asserted; it is the write data output to the disk drive when the write gate signal is asserted.

MICROPROCESSOR INTERFACE

$\overline{RST}$	I	RESET. An asserted low input generates a component reset that holds the internal registers of the SSI 32C9010 at reset, stops all operations within the chip, and deasserts all output signals. All input/output signals are set to the high-Z state during this signal.
ALE/M/$\overline{NM}$	I	ADDRESS LATCH ENABLE/MULTIPLEXED/NON-MULTIPLEXED ADDRESS SELECT. When tied high or left floating after reset, the microprocessor interface is configured as non-multiplexed. When driven low, then the microprocessor interface is configured as multiplexed. In this case this pin functions as the address latch enable, and the MA(7:0) pins are the demultiplexed address outputs.
CS	I	CHIP SELECT. Active high signal, when asserted, the internal registers of the SSI 32C9010 can be accessed.
$\overline{WR}$/R/$\overline{W}$	I	WRITE STROBE/READ/WRITE. In the Intel bus mode, when an active low signal is present with CS signal high, the data is written to the internal registers. In the Motorola bus mode, this signal acts as the R/$\overline{W}$ signal.
$\overline{RD}$/DS	I	READ STROBE/DATA STROBE. In the Intel bus mode, when an active low signal is present with CS signal high, internal register data is read. In the Motorola mode, this signal acts as the DS signal. DS when active high is data strobe.

MICROPROCESSOR INTERFACE (Continued)

NAME	TYPE	DESCRIPTION
$\overline{DINT}$	O, OD,Z	DISK INTERRUPT. An active low signal indicates the controller is requesting microprocessor service from the disk side. This signal is programmable for either a push-pull or open-drain output circuit. This signal powers up in the high-Z state. Register 4F bit 3 when set to one enables the pull-up. This signal is also programmable to be either an active high or low interrupt.
$\overline{SINT}$	O, OD,Z	SCSI INTERRUPT. This signal is generated by the SCSI controller and is an interrupt line to the microprocessor. It is programmable for either a push-pull or open drain output circuit. This signal powers up in the high-Z state. The interrupt is sourced from the SCSI Interrupt Register. Register 4F bit 7 enables the pull-up.
AD7:0	I/O	ADDRESS/DATA BUS. When configured in the Intel mode, these lines are multiplexed, bidirectional microprocessor register address and data lines. When configured in the Motorola mode, these lines are bidirectional data lines.
MA(7:0)	I/O	MICROPROCESSOR ADDRESS BUS: These signals are nonmultiplexed address input or latched address output lines.
READY	O	READY: When this signal is deasserted low, the microprocessor shall insert wait states to allow time for the chip to respond to the access.
I/$\overline{MC}$	I	INTEL/MOTOROLA: This signal selects the microprocessor interface to be used. When this signal is asserted high, it selects the Intel bus control interface. When this signal is deasserted low, it selects the Motorola bus control interface. This signal has an internal pull-up to allow the default selection of the Intel bus control interface.

BUFFER MANAGER INTERFACE

BA0:15	O	BUFFER MEMORY ADDRESS LINES 0:15. Active high, for direct connection to a Static or Dynamic RAM address lines 0:15.
BA16/$\overline{RAS}$	O	BUFFER MEMORY ADDRESS 16: In SRAM mode, for direct connection to a Static RAM address line 16.
		ROW ADDRESS STROBE: In DRAM mode, direct connection to a Dynamic RAM Row Address Strobe signal.
BA17/$\overline{CAS}$	O	BUFFER MEMORY ADDRESS 17: In SRAM mode, for direct connection to a Static RAM address line 17. ROW ADDRESS STROBE: In DRAM mode, active low, for direct connection to a Dynamic RAM Column Address Strobe signal.
BD0:7	I/O	BUFFER MEMORY DATA BUS. 7 through 0. Buffer data bus that connects directly to the buffer RAM data lines.
BDP	I/O	BUFFER MEMORY DATA PARITY. This signal provides odd parity for the buffer memory data bus during transfers to/from the buffer memory to the buffer RAM.
$\overline{MOE}$	O	MEMORY OUTPUT ENABLE. This signal is asserted low only for buffer memory read operations.
$\overline{WE}$	O	WRITE ENABLE. Active low, write enable for the buffer RAM.
SYSCLK	I	SYSTEM CLOCK. This signal is used to synchronize the buffer RAM access, including the generation of memory address bits, write enable $\overline{WE}$, and memory output enable $\overline{MOE}$.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC operating characteristics.

PARAMETER	RATING	UNIT
Power Supply Voltage, VCC	7	V
Ambient Temperature	0 to 70	°C
Storage Temperature	-65 to 150	°C
Power Dissipation	750	mW
Input, Output pins	-0.5 to VCC+0.5	V

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VCC Power Supply Voltage		4.50		5.50	V
ICC Supply Current	Ta=25°C Outputs Unloaded			50	mA
ICCS Supply Current				250	µA
VIL Input Low Voltage		-0.5		0.8	V
V0IH Input High Voltage		2.0		VCC+0.5	V
VOL Output Low Voltage	All pins except SCSI interface, IOL = 2 mA			0.4	
VOL Output Low Voltage	SCSI interface pins, IOL = 48 mA		0.5	V	
VOH Output High Voltage	IOH = -400 µA			2.4	V
IL Input Leakage Current	0 < VIN < VCC	-10		10	µA
CIN Input Capacitance				10	pF
COUT Output Capacitance				10	pF

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SSI 32C9020
SCSI Combo Controller
48 Mbit/s; single bit NRZ interface
Advance Information

December 1991

DESCRIPTION

The SSI 32C9020 is a CMOS VLSI device which integrates major portions of the hardware needed to build a SCSI driven hard disk drive. The SSI 32C9010 is one of the family of Silicon Systems' single chip disk controllers. The SSI 32C9020's place in the Silicon Systems' chip family is illustrated in the hierarchy chart in Figure 1. It provides most of the disk controller functional circuitry necessary to build an embedded SCSI-disk drive.

The SSI 32C9020 is a CMOS VLSI device which integrates the major portion of the hardware needed to build a SCSI driven hard disk controller. The SSI 32C9020 is capable of supporting interleaved data transfer rate up to 48 Mbit/s. This chip represents a major reduction in part count when used with the SSI 32P3000 Pulse Detector and Filter Combo, the SSI 32D5391, the SSI 32R2010 Read/Write device, and the SSI 32H4631 Servo and Motor Speed Controller device, implementing a cost efficient, high performance, 5-chip set intelligent drive solution.

The SSI 32C9020 includes a four port Buffer Manager, a storage controller and an extensive hardware support, including 24 mA drivers, for the SCSI and other compatible interfaces.

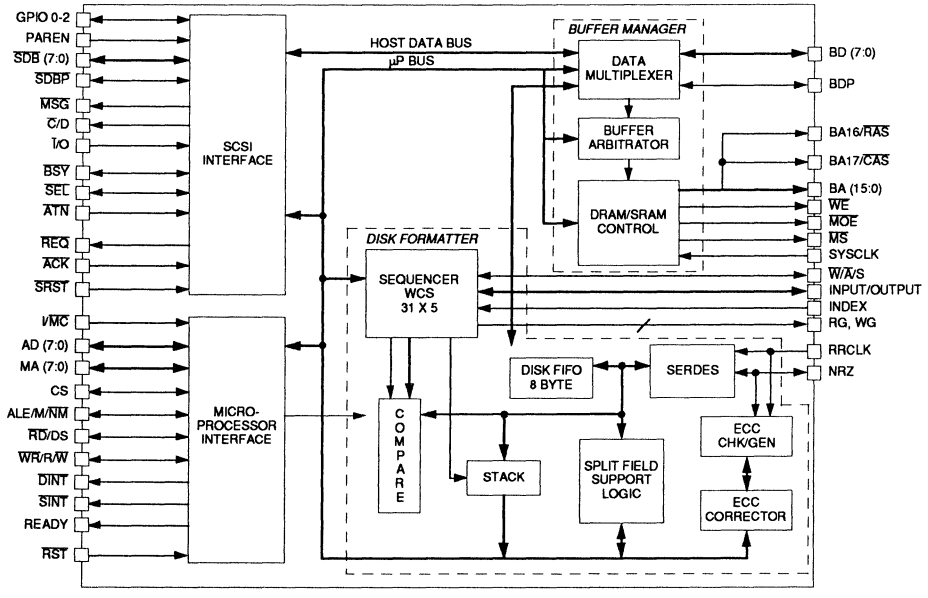
The SSI 32C9020 performs all the controller functions for the peripheral device, such as serialization/deserialization; ECC generation and checking on the data stream, and CRC generation and checking on the header of the data stream.

FEATURES

- **SCSI Bus Interface**
  - **ANSI X3.131-1990 Rev 10C SCSI-2 specification for target devices**
  - **Direct bus interface logic with on-chip 48 mA drivers**
  - **Synchronous transfer rates up to 10 Mbyte/s; 5 Mbyte/s asynchronous**
  - **Parity generation and checking**
  - **High level SCSI sequences without microprocessor intervention**
  - **4-byte Command FIFO supports execution of multiple commands**
  - **Supports SCSI-2 tagged queuing**
  - **SCSI CDB Group Codes decoded "on-the-fly"**
  - **Sixteen-byte data FIFO between the DMA and SCSI channel**
  - **SCSI autodisconnect and reconnect operation supported**

(Continued)

BLOCK DIAGRAM



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SSI 32C9020
SCSI Combo Controller
48 Mbit/s; single bit NRZ interface

FEATURES (Continued)

- **Buffer Manager**
  - **Buffer Memory throughput to 20 MByte/s for SRAM and 17.2 Mbyte/s for DRAM in Page Mode.**
  - **Up to 256 kB Static RAM or 1MB Dynamic RAM support**
  - **Buffer RAM segmentation with flexible segment sizes for 256 bytes to 1MByte**
  - **Dedicated Host, Disk, and Microprocessor Buffer RAM address pointers**
  - **Internal buffer protection circuit provides buffer integrity**
- **Storage Controller**
  - **NRZ Data Rates to 48Mbit/s--single bit NRZ interface to the Data Separator**
  - **88-bit Reed Solomon with "on-the-fly" fast hardware correction circuitry**
  - **Capable of correcting four 10-bit symbols in error**
  - **Guaranteed to correct one 31-bit burst or two 11-bit bursts**
  - **Hardware on-the-fly correction selectable between 11 or 31-bit single burst error within a quarter sector time**
  - **Detects up to 51-bit burst or three 11-bit burst**
  - **Multiple sector transfer support**
  - **Sector header or microprocessor based split data field processing logic**
  - **Advanced sequencer organized in 31 x 5 bytes**
- **Microprocessor Interface**
  - **Supports both multiplexed or non-multiplexed family of microprocessors**
  - **Separate host and disk interrupts**
- **Others**
  - **Internal power down mode**
  - **Available in 100-pin QFP**

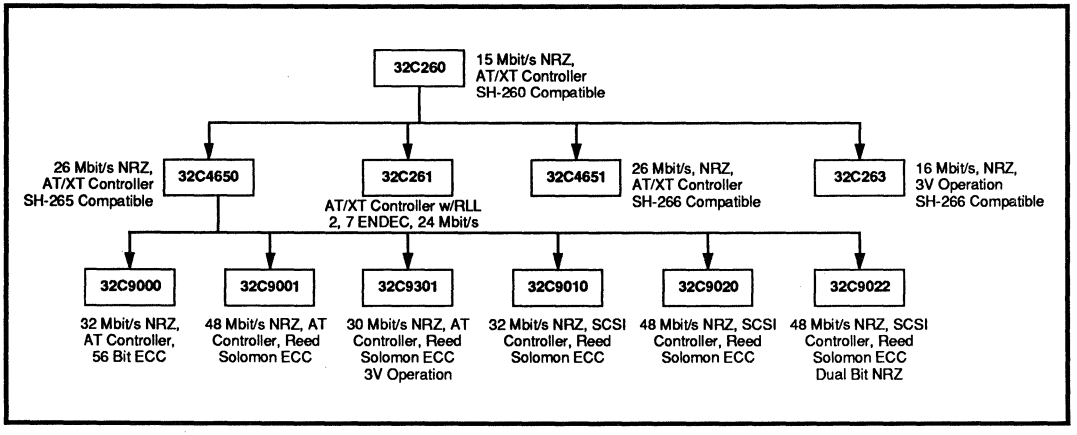

FIGURE 1: Silicon Systems' Disk Controller Chip Hierarchy

FUNCTIONAL DESCRIPTION

The four major functional blocks are:

Microcontroller Interface
Buffer Memory Interface
Disk Formatter
Host Interface

The SSI 32C9020 includes a control sequencer with a writeable control store, buffer RAM controller capable of interleaved address generation, direct SCSI bus connections, and configuration/status registers which can be programmed by an external microcontroller. The internal hardware also supports automatic looping of the sequencer program, and the interrupt circuitry relieves the supervising microprocessor of having to poll on the status registers. Access to the control store and registers is accomplished through the microprocessor interface which is optimized for eight-bit, mulitplexed address/data or non-multiplexed processors such as the Intel 80C196 or Motorola 68HC11. **For a complete description of the programmable registers, refer to the SSI 32C9020 Design Guide.**

The device performs all the controller functions for the peripheral device, such as serialization/deserialization; ECC generation, checking, and correction on the data stream; and CRC generation and checking on the header stream. It also has the flexibility of defect management and recovery. The contention between the host request and the disk request for buffer RAM access is internally arbitrated and resolved utilizing data FIFOs.

PIN DESCRIPTION

The following convention is used in the pin description:

(I) denotes an input
(O) denotes an output
(Z) denotes a tri-state output
(OD) denotes an open drain output

GENERAL

NAME	TYPE	DESCRIPTION
VDD		POWER SUPPLY PIN, VCC
GND		GROUND

HOST INTERFACE

$\overline{SDBP}$	I/O	SCSI DATA BUS PARITY. Odd parity bit for the SCSI data bus.
$\overline{SDB7\text{-}0}$	I/O	SCSI DATA BUS BITS 7-0.
$\overline{ATN}$	I	ATTENTION. This active low signal is used by the initiator to request a message out phase.
$\overline{BSY}$	I/O	BUSY. This active low signal is used to indicate when the bus is active.
$\overline{ACK}$	I	ACKNOWLEDGE. This active low signal is used in the handshake protocol to indicate the completion of a data byte transfer.
$\overline{SRST}$	I	SCSI RESET. This active low signal is used to reset the SCSI controller.
$\overline{MSG}$	O	MESSAGE. This active low signal is used to indicate a message phase.
$\overline{SEL}$	I/O	SELECT. This active low signal is used to indicate either a selection or reselection phase.
$\overline{C}$/D	O	COMMAND/DATA. This signal is used to indicate either a command or data phase.
$\overline{REQ}$	I	REQUEST. This active low signal is used in the handshake protocol to initiate a data byte transfer.
$\overline{I}$/O	I	INPUT/OUTPUT. This signal is used to indicate the direction of data transfer.
PAREN	I	SCSI PARITY ENABLE. This active high signal is used to enable parity checking of the SCSI data bus. Parity checking is disabled when this pin is held low.

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PIN DESCRIPTION (Continued)

DISK INTERFACE

NAME	TYPE	DESCRIPTION
GPIO 2-0	I	INPUT/OUTPUT. These pins are used to indicate the SCSI ID of the target device. The pins can be programmed as outputs for test purposes only.
INDEX	I	INDEX. Input for index pulse received from the drive.
INPUT/ OUTPUT	I/O	DISK SEQUENCER INPUT/OUTPUT. A general purpose control (output) and status (input) pin configured by the Output Enable Bit of Register 71H, bit 7. At power-on, this pin is an input. As an input, it can be used to synchronize the disk sequencer to an external event. As an output, it is controlled by bit 2 of the Control Field of the disk sequencer.
$\overline{\text{WAM}}$/AMD/ SECTOR	I/O	WRITE ADDRESS MARK/SECTOR/ADDRESS MARK DETECT. This pin is used in the hard sector mode as the sector input. A pulse on this pin indicates a sector mark is found. In the soft sector mode, a low level output is asserted during write gate to indicate writing of address mark. During read, a low-level input indicates an address mark was detected. The device powers up in soft sector default mode.
RG	O	READ GATE. During disk data read, this pin is asserted. Active high.
WG	O	WRITE GATE. During disk data write, this pin is asserted. Active high.
RRCLK	I	READ/REFERENCE CLOCK. This pin is used in conjunction with the NRZ pin to clock data in and out of the SSI 32C9020 device.
NRZ	I/O	NON RETURN TO ZERO. This signal is the read data input from the disk drive when the read gate signal is asserted; it is the write data output to the disk drive when the write gate signal is asserted.

MICROPROCESSOR INTERFACE

$\overline{\text{RST}}$	I	RESET. An asserted low input generates a component reset that holds the internal registers of the SSI 32C9020 at reset, stops all operations within the chip, and deasserts all output signals. All input/output signals are set to the high-Z state during this signal.
ALE/M/$\overline{\text{NM}}$	I	ADDRESS LATCH ENABLE/MULTIPLEXED/NON-MULTIPLEXED ADDRESS SELECT. When tied high or left floating after reset, the microprocessor interface is configured as non-multiplexed. When driven low, then the microprocessor interface is configured as multiplexed. In this case this pin functions as the address latch enable, and the MA(7:0) pins are the demultiplexed address outputs.
CS	I	CHIP SELECT. Active high signal, when asserted, the internal registers of the SSI 32C9020 can be accessed.
$\overline{\text{WR}}$/R/$\overline{\text{W}}$	I	WRITE STROBE/READ/WRITE. In the Intel bus mode, when an active low signal is present with CS signal high, the data is written to the internal registers. In the Motorola bus mode, this signal acts as the R/$\overline{\text{W}}$ signal.
$\overline{\text{RD}}$/DS	I	READ STROBE/DATA STROBE. In the Intel bus mode, when an active low signal is present with CS signal high, internal register data is read. In the Motorola mode, this signal acts as the DS signal. DS when active high is data strobe.
$\overline{\text{DINT}}$	O, OD,Z	DISK INTERRUPT. An active low signal indicates the controller is requesting microprocessor service from the disk side. This signal is programmable for either a push-pull or open-drain output circuit. This signal powers up in the high-Z state. Register 4F bit 3 enables the pull-up.

MICROPROCESSOR INTERFACE (Continued)

NAME	TYPE	DESCRIPTION
$\overline{SINT}$	O, OD,Z	SCSI INTERRUPT. This signal is generated by the SCSI controller and is an interrupt line to the microprocessor. It is programmable for either a push-pull or open drain output circuit. This signal powers up in the high-Z state. The interrupt is sourced from the SCSI Interrupt Register. Register 4F bit 3 enables the pull-up. This signal is also programmable to be either an active high or low interrupt.
AD7:0	I/O	ADDRESS/DATA BUS. When configured in the Intel mode, these lines are multiplexed, bidirectional microprocessor register address and data lines. When configured in the Motorola mode, these lines are bidirectional data lines.
MA(7:0)	I/O	MICROPROCESSOR ADDRESS BUS: These signals are nonmultiplexed address input or latched address output lines.
READY	O	READY: When this signal is deasserted low, the microprocessor shall insert wait states to allow time for the chip to respond to the access.
I/$\overline{MC}$	I	INTEL/MOTOROLA: This signal selects the microprocessor interface to be used. When this signal is asserted high, it selects the Intel bus control interface. When this signal is deasserted low, it selects the Motorola bus control interface. This signal has an internal pull-up to allow the default selection of the Intel bus control interface.

BUFFER MANAGER INTERFACE

BA0:15	O	BUFFER MEMORY ADDRESS LINES 0:15. Active high, for direct connection to a Static or Dynamic RAM address lines 0:15.
BA16/$\overline{RAS}$	O	BUFFER MEMORY ADDRESS 16: In SRAM mode, for direct connection to a Static RAM address line 16. ROW ADDRESS STROBE: In DRAM mode, for direct connection to a Dynamic RAM Row Address Strobe signal.
BA17/$\overline{CAS}$	O	BUFFER MEMORY ADDRESS 17: In SRAM mode, for direct connection to a Static RAM address line 17. ROW ADDRESS STROBE: In DRAM mode, active low, for direct connection to a Dynamic RAM Column Address Strobe signal.
BD0:7	I/O	BUFFER MEMORY DATA BUS. 7 through 0. Active high, buffer data bus that connects directly to the buffer RAM data lines.
BDP	I/O	BUFFER MEMORY DATA PARITY. This signal provides odd parity for the buffer memory data bus during transfers to/from the buffer memory to the buffer RAM.
$\overline{MOE}$	O	MEMORY OUTPUT ENABLE. This signal is asserted low only for buffer memory read operations.
$\overline{WE}$	O	WRITE ENABLE. Active low, write enable for the buffer RAM.
SYSCLK	I	SYSTEM CLOCK. This signal is used to synchronize the buffer RAM access, including the generation of memory address bits, write enable $\overline{WE}$, and memory output enable $\overline{MOE}$.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC operating characteristics.

PARAMETER	RATING	UNIT
Power Supply Voltage, VCC	7	V
Ambient Temperature	0 to 70	°C
Storage Temperature	-65 to 150	°C
Power Dissipation	750	mW
Input, Output pins	-0.5 to VCC+0.5	V

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VCC Power Supply Voltage		4.50		5.50	V
ICC Supply Current	Ta = 25°C Outputs Unloaded			50	mA
ICCS Supply Current				250	µA
VIL Input Low Voltage		-0.5		0.8	V
V0IH Input High Voltage		2.0		VCC+0.5	V
VOL Output Low Voltage	All pins except SCSI interface, IOL = 2 mA			0.4	
VOL Output Low Voltage	SCSI interface pins, IOL = 48 mA			0.5	V
VOH Output High Voltage	IOH = -400 µA			2.4	V
IL Input Leakage Current	0 < VIN < VCC	-10		10	µA
CIN Input Capacitance				10	pF
COUT Output Capacitance				10	pF

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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SSI 32C9022
SCSI Combo Controller
48 Mbit/s; dual bit NRZ interface

Advance Information

December 1991

DESCRIPTION

The SSI 32C9022 is a CMOS VLSI device which integrates major portions of the hardware needed to build a SCSI driven hard disk drive. The SSI 32C9022 is one of the family of Silicon Systems' single chip disk controllers. The SSI 32C9022's place in the Silicon Systems' chip family is illustrated in the hierarchy chart in Figure 1. It provides most of the disk controller disk controller functional circuitry necessary to build an intelligent SCSI-disk drive.

The SSI 32C9022 is a CMOS VLSI device which integrates the major portion of the hardware needed to build a SCSI driven hard disk controller. The SSI 32C9022 is capable of supporting interleaved data transfer rate up to 48 Mbit/s. This chip represents a major reduction in part count when used with the SSI 32P3000 Pulse Detector and Filter Combo, the SSI 32D5392, the SSI 32R2010 Read/Write device, and the SSI 32H4631 Servo and Motor Speed Controller device, implementing a cost efficient, high performance, 5-chip set intelligent drive solution.

The SSI 32C9022 includes a four port Buffer Manager, a storage controller and an extensive hardware support, including 24 mA drivers, for the SCSI and other compatible interfaces.

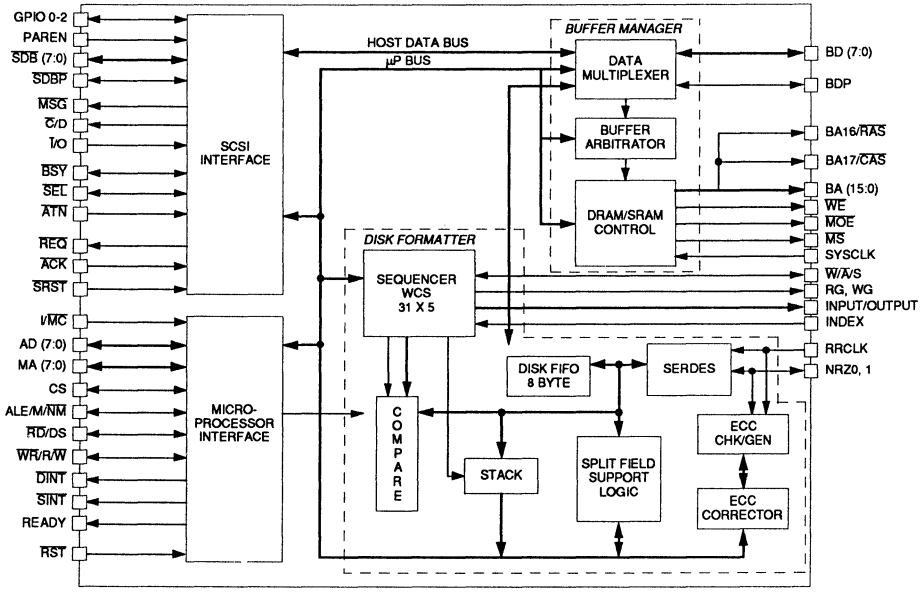
The SSI 32C9022 performs all the controller functions for the peripheral device, such as serialization/deserialization; ECC generation and checking on the data stream, and CRC generation and checking on the header of the data stream.

FEATURES

- **SCSI Bus Interface**
  - **ANSI X3.131-1990 Rev 10C SCSI-2 specification for target devices**
  - **Direct bus interface logic with on-chip 48 mA drivers**
  - **Synchronous transfer rates up to 10 Mbyte/s; 5 Mbyte/s asynchronous**
  - **Parity generation and checking**
  - **High level SCSI sequences without microprocessor intervention**
  - **4-byte Command FIFO supports execution of multiple commands**
  - **Supports SCSI-2 tagged queuing**
  - **SCSI CDB Group Codes decoded "on-the-fly"**
  - **Sixteen-byte data FIFO between the DMA and SCSI channel**
  - **SCSI autodisconnect and reconnect operation supported**

(Continued)

BLOCK DIAGRAM



8

SSI 32C9022
SCSI Combo Controller
48 Mbit/s; dual bit NRZ interface

FEATURES (Continued)

- Buffer Manager
  - Buffer Memory throughput to 20 MByte/s for SRAM and 17.2 Mbyte/s for DRAM in Page Mode.
  - Up to 256 kB Static RAM or 1MB Dynamic RAM support
  - Buffer RAM segmentation with flexible segment sizes for 256 bytes to 1MByte
  - Dedicated Host, Disk, and Microprocessor Buffer RAM address pointers
  - Internal buffer protection circuit provides buffer integrity
- Storage Controller
  - NRZ Data Rates to 48Mbit/s -- single bit NRZ interface to the Data Separator
  - 88-bit Reed Solomon with "on-the-fly" fast hardware correction circuitry
  - Capable of correcting four 10-bit symbols in error
  - Guaranteed to correct one 31-bit burst or two 11-bit bursts
  - Hardware on-the-fly correction selectable between 11 or 31-bit single burst error within a quarter sector time
  - Detects up to one 51-bit burst or three 11-bit burst
  - Multiple sector transfer support
  - Sector header or microprocessor based split data field processing logic
  - Advanced sequencer organized in 31 x 5 bytes
- Microprocessor Interface
  - Supports both multiplexed or non-multiplexed family of microprocessors
  - Separate host and disk interrupts
- Others
  - Internal power down mode
  - Available in 100-pin QFP

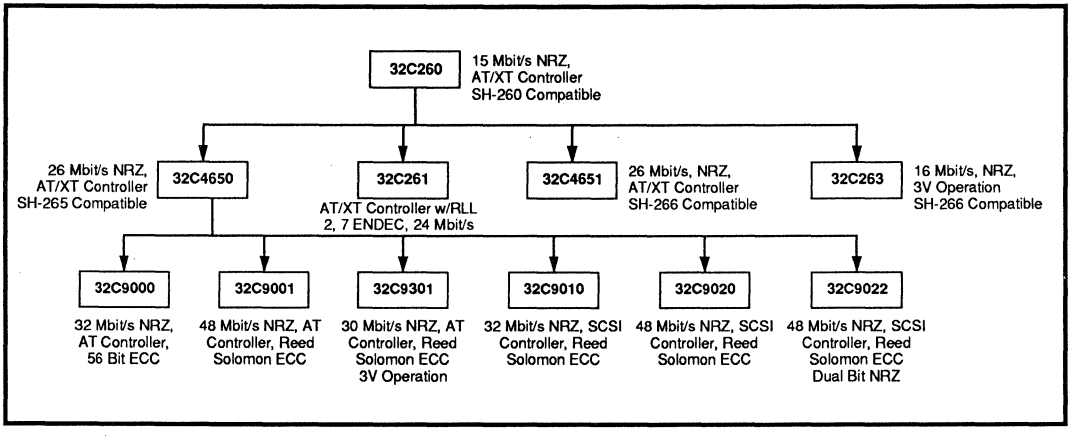


FIGURE 1: Silicon Systems' Single Chip Controller Hierarchy

FUNCTIONAL DESCRIPTION

The four major functional blocks are:

Microcontroller Interface
Buffer Memory Interface
Disk Formatter
Host Interface

The SSI 32C9022 includes a control sequencer with a writeable control store, buffer RAM controller capable of interleaved address generation, direct SCSI bus connections, and configuration/status registers which can be programmed by an external microcontroller. The internal hardware also supports automatic looping of the sequencer program, and the interrupt circuitry relieves the supervising microprocessor of having to poll on the status registers. Access to the control store and registers is accomplished through the microprocessor interface which is optimized for eight-bit, mulitplexed address/data or non-multiplexed processors such as the Intel 80C196 or Motorola 68HC16. **For a complete description of the programmable registers, refer to the SSI 32C9010/9020/9022 Design Guide.**

The device performs all the controller functions for the peripheral device, such as serialization/deserialization; ECC generation, checking, and correction on the data stream; and CRC generation and checking on the header stream. It also has the flexibility of defect management and recovery. The contention between the host request and the disk request for buffer RAM access is internally arbitrated and resolved utilizing data FIFOs.

PIN DESCRIPTION

The following convention is used in the pin description:

(I) denotes an input
(O) denotes an output
(Z) denotes a tri-state output
(OD) denotes an open drain output

GENERAL

NAME	TYPE	DESCRIPTION
VDD		POWER SUPPLY PIN, VCC
GND		GROUND

HOST INTERFACE

$\overline{SDBP}$	I/O	SCSI DATA BUS PARITY. Odd parity bit for the SCSI data bus.
$\overline{SDB7\text{-}0}$	I/O	SCSI DATA BUS BITS 7-0.
$\overline{ATN}$	I	ATTENTION. This active low signal is used by the initiator to request a message out phase.
$\overline{BSY}$	I/O	BUSY. This active low signal is used to indicate when the bus is active.
$\overline{ACK}$	I	ACKNOWLEDGE. This active low signal is used in the handshake protocol to indicate the completion of a data byte transfer.
$\overline{SRST}$	I	SCSI RESET. This active low signal is used to reset the SCSI controller.
$\overline{MSG}$	O	MESSAGE. This active low signal is used to indicate a message phase.
$\overline{SEL}$	I/O	SELECT. This active low signal is used to indicate either a selection or reselection phase.
$\overline{C}/D$	O	COMMAND/DATA. This signal is used to indicate either a command or data phase.
$\overline{REQ}$	I	REQUEST. This active low signal is used in the handshake protocol to initiate a data byte transfer.
$\overline{I}/O$	I	INPUT/OUTPUT. This signal is used to indicate the direction of data transfer.
PAREN	I	SCSI PARITY ENABLE. This active high signal is used to enable parity checking of the SCSI data bus. Parity checking is disabled when this pin is held low.
GPIO2-0	I	INPUT/OUTPUT. These pins are used to indicate the SCSI ID of the target device. The pins can be programmed as outputs for test purposes only.

8

PIN DESCRIPTION (Continued)

DISK INTERFACE

NAME	TYPE	DESCRIPTION
INDEX	I	INDEX. Input for index pulse received from the drive.
INPUT/ OUTPUT	I/O	DISK SEQUENCER INPUT/OUTPUT. A general purpose control (output) and status (input) pin configured by the Output Enable Bit of Register 71H, bit 7. At power-on, this pin is an input. As an input, it can be used to synchronize the disk sequencer to an external event. As an output, it is controlled by bit 2 of the Control Field of the disk sequencer.
$\overline{WAM}/\overline{AMD}$/ SECTOR	I/O	WRITE ADDRESS MARK/SECTOR/ADDRESS MARK DETECT. This pin is used in the hard sector mode as the sector input. A pulse on this pin indicates a sector mark is found. In the soft sector mode, a low level output is asserted during write gate to indicate writing of address mark. During read, a low-level input indicates an address mark was detected. The device powers up in soft sector default mode.
RG	O	READ GATE. During disk data read, this pin is asserted. Active high.
WG	O	WRITE GATE. During disk data write, this pin is asserted. Active high.
RRCLK	I	READ/REFERENCE CLOCK. This pin is used in conjunction with the NRZ pin to clock data in and out of the SSI 32C9020 device.
NRZ0, 1	I/O	NON RETURN TO ZERO. These signals are the read data input 0 and 1 from the disk drive when the read gate signal is asserted; it is the write data output to the disk drive when the write gate signal is asserted.

MICROPROCESSOR INTERFACE

$\overline{RST}$	I	RESET. An asserted low input generates a component reset that holds the internal registers of the SSI 32C9020 at reset, stops all operations within the chip, and deasserts all output signals. All input/output signals are set to the high-Z state during this signal.
ALE/M/$\overline{NM}$	I	ADDRESS LATCH ENABLE/MULTIPLEXED/NON-MULTIPLEXED ADDRESS SELECT. When tied high or left floating after reset, the microprocessor interface is configured as non-multiplexed. When driven low, then the microprocessor interface is configured as multiplexed. In this case this pin functions as the address latch enable, and the MA(7:0) pins are the demultiplexed address outputs.
CS	I	CHIP SELECT. Active high signal, when asserted, the internal registers of the SSI 32C9022 can be accessed.
$\overline{WR}$/R/$\overline{W}$	I	WRITE STROBE/READ/WRITE. In the Intel bus mode, when an active low signal is present with CS signal high, the data is written to the internal registers. In the Motorola bus mode, this signal acts as the R/$\overline{W}$ signal.
$\overline{RD}$/DS	I	READ STROBE/DATA STROBE. In the Intel bus mode, when an active low signal is present with CS signal high, internal register data is read. In the Motorola mode, this signal acts as the DS signal. DS when active high is data strobe.
$\overline{DINT}$	O, OD,Z	DISK INTERRUPT. An active low signal indicates the controller is requesting microprocessor service from the disk side. This signal is programmable for either a push-pull or open-drain output circuit. This signal powers up in the high-Z state. Register 4F bit 3 enables the pull-up.

MICROPROCESSOR INTERFACE (Continued)

NAME	TYPE	DESCRIPTION
$\overline{SINT}$	O, OD,Z	SCSI INTERRUPT. This signal is generated by the SCSI controller and is an interrupt line to the microprocessor. It is programmable for either a push-pull or open drain output circuit. This signal powers up in the high-Z state. The interrupt is sourced from the SCSI Interrupt Register. Register 4F bit 3 enables the pull-up. This signal is also programmable to be either an active high or low interrupt.
AD7:0	I/O	ADDRESS/DATA BUS. When configured in the Intel mode, these lines are multiplexed, bidirectional microprocessor register address and data lines. When configured in the Motorola mode, these lines are bidirectional data lines.
MA(7:0)	I/O	MICROPROCESSOR ADDRESS BUS: These signals are nonmultiplexed address input or latched address output lines.
READY	O	READY: When this signal is deasserted low, the microprocessor shall insert wait states to allow time for the chip to respond to the access.
I/$\overline{MC}$	I	INTEL/MOTOROLA: This signal selects the microprocessor interface to be used. When this signal is asserted high, it selects the Intel bus control interface. When this signal is deasserted low, it selects the Motorola bus control interface. This signal has an internal pull-up to allow the default selection of the Intel bus control interface.

BUFFER MANAGER INTERFACE

BA0:15	O	BUFFER MEMORY ADDRESS LINES 0:15. Active high, for direct connection to a Static or Dynamic RAM address lines 0:15.
BA16/$\overline{RAS}$	O	BUFFER MEMORY ADDRESS 16: In SRAM mode, for direct connection to a Static RAM address line 16. ROW ADDRESS STROBE: In DRAM mode, for direct connection to a Dynamic RAM Row Address Strobe signal.
BA17/$\overline{CAS}$	O	BUFFER MEMORY ADDRESS 17: In SRAM mode, for direct connection to a Static RAM address line 17. ROW ADDRESS STROBE: In DRAM mode, active low, for direct connection to a Dynamic RAM Column Address Strobe signal.
BD0:7	I/O	BUFFER MEMORY DATA BUS. 7 through 0. Active high, buffer data bus that connects directly to the buffer RAM data lines.
BDP	I/O	BUFFER MEMORY DATA PARITY. This signal provides odd parity for the buffer memory data bus during transfers to/from the buffer memory to the buffer RAM.
$\overline{MOE}$	O	MEMORY OUTPUT ENABLE. In SRAM mode this signal is asserted low when every buffer memory access is active. In DRAM mode this signal is asserted low only for buffer memory read operation.
$\overline{MS}$	O	MEMORY SELECT. An active low signal indicates external memory is selected.
$\overline{WE}$	O	WRITE ENABLE. Active low, write enable for the buffer RAM.
SYSCLK	I	SYSTEM CLOCK. This signal is used to synchronize the buffer RAM access, including the generation of memory address bits, write enable $\overline{WE}$, and memory output enable $\overline{MOE}$.

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ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC operating characteristics.

PARAMETER	RATING
Power Supply Voltage, VCC	7V
Ambient Temperature	0 to 70°C
Storage Temperature	-65 to 150°C
Power Dissipation	750 mW
Input, Output pins	-0.5 to VCC+0.5V

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VCC Power Supply Voltage		4.50		5.50	V
ICC Supply Current	Ta = 25°C Outputs Unloaded			50	mA
ICCS Supply Current				500	µA
VIL Input Low Voltage		-0.5		0.8	V
V0IH Input High Voltage		2.0		VCC+0.5	V
VOL Output Low Voltage	All pins except SCSI interface, IOL = 2 mA			0.4	
VOL Output Low Voltage	SCSI interface pins, IOL = 48 mA			0.5	V
VOH Output High Voltage	IOH = -400 µA			2.4	V
IL Input Leakage Current	0 < VIN < VCC	-10		10	µA
CIN Input Capacitance				10	pF
COUT Output Capacitance				10	pF

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SSI 32C9301
PC-AT Combo Controller With Reed Solomon, 3V Operation
Advance Information

December 1991

DESCRIPTION

The SSI 32C9301 is a CMOS VLSI device which integrates major portions of the hardware needed to build a PC AT driven hard disk controller. The SSI 32C9301 is one of the family of Silicon Systems' single chip disk controllers. The SSI 32C9301's place in the Silicon Systems' chip family is illustrated in the hierarchy chart in Figure 1. It provides most of the functional circuitry necessary to build an "ATA" intelligent disk.

The SSI 32C9301 is capable of supporting interleaved data transfer rate up to 30 Mbit/s.

The SSI 32C9301 includes a dual port Buffer Manager, a storage controller, and a high performance AT host interface block that incorporates an extensive hardware support — including 24 mA drivers — for the PC AT and other compatible interfaces.

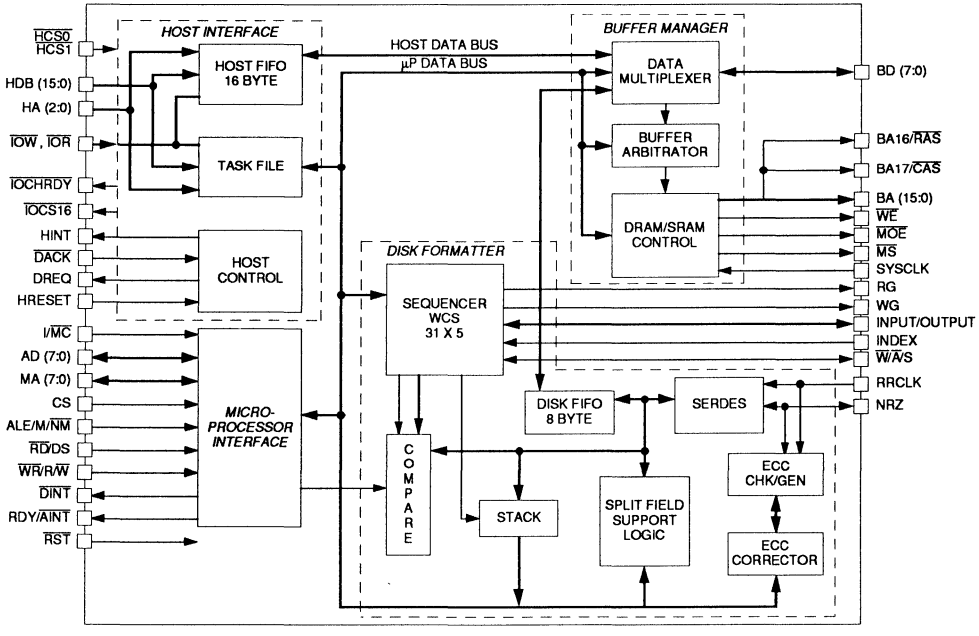
The SSI 32C9301 performs all the controller functions for the peripheral device, such as serialization/deserialization; ECC generation and checking on the data stream, and CRC generation and checking on the header of the data stream.

FEATURES

- **PC AT Bus Interface**
  - **Single Chip PC AT Controller**
  - **Direct bus interface logic with on-chip 24 mA drivers**
  - **Logic for daisy chaining 2 embedded ATA drives**
  - **Supports 30 Mbit/s concurrent disk transfer on a 3 M words/s PC-AT in PIO or single or EISA compatible burst DMA mode — type B**
  - **Automatic command decoding of write, write multiple, and format commands.**
  - **Automatic updates of the host task file registers in multiple sector transfers**
- **Buffer Manager**
  - **Supports Buffer Memory throughput to 10 Mbytes/s SRAM or 8 Mbytes/s for DRAM**
  - **Direct Buffer Memory addressing up to 256 kB Static RAM or 1 MB Dynamic RAM for various timings and sizes**

(Continued)

BLOCK DIAGRAM



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SSI 32C9301
PC-AT Combo Controller
With Reed Solomon, 3V Operation

FEATURES (continued)

- Buffer Manager (continued)
  - Buffer RAM segmentation with flexible segment sizes from 256 bytes to 1 Mbytes/s
  - Dedicated Host, Disk, and Microprocessor Buffer RAM address pointers
- Storage Controller
  - NRZ Data Rates up to 30 Mbit/s
  - Selectable 16-bit CRC or 88 bit ECC polynomial with "on-the-fly" fast hardware correction circuitry
  - Multiple sector transfer support without microprocessor intervention
  - Highly programmable Advanced sequencer organized in 31 x 5 bytes
  - Support sector level defect management
  - Sector header or microprocessor based split data field processing logic
- Microprocessor Interface
  - Supports both multiplexed and non-multiplexed microprocessor support
  - Separate host and disk interrupts
- Others
  - Internal power down mode
  - Operational at 3.3V ± 20%
  - Available in 100-pin surface mount TQFP

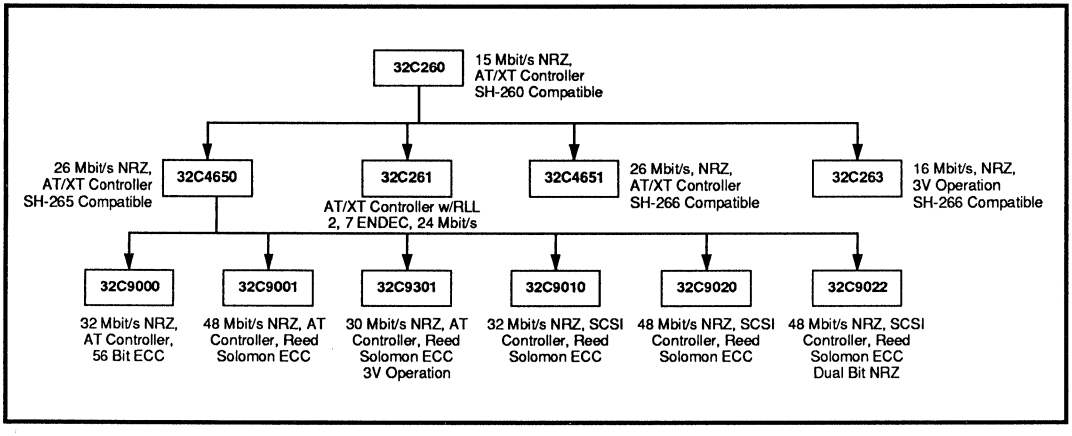

FIGURE 1: Silicon Systems' Disk Controller Chip Hierarchy

FUNCTIONAL DESCRIPTION

The four major functional blocks are:

- Microcontroller Interface
- Buffer Memory Interface
- Disk Formatter
- Host Interface

The SSI 32C9301 includes a control sequencer with a writeable control store, buffer RAM controller capable of interleaved address generation, direct ATA bus connections, and configuration/status registers which can be programmed by an external microcontroller. The internal hardware also supports automatic looping of the sequencer program, and the interrupt circuitry relieves the supervising microprocessor of having to poll on the status registers. Access to the control store and registers is accomplished through the microprocessor interface which is optimized for eight-bit, mulitplexed address/data processors such as Intel's 80C196 or non-multiplexed microprocessors — such as Motorola's 68HC16. **For a complete description of the programmable registers, refer to the SSI 32C9001 Design Guide.**

The device performs all the controller functions for the peripheral device, such as serialization/deserialization; ECC generation, checking, and correction assistance; and CRC generation and checking on the header stream. It also has the flexibility of defect management and recovery. The contention between the host, disk, microprocessor, and refresh requests for buffer RAM access is internally arbitrated and resolved.

PIN DESCRIPTION

The following convention is used in the pin description:

- (I) denotes an input
- (I/S) denotes a Schmitt trigger input
- (O) denotes an output
- (I/O) denotes a bidirectional signal
- (Z) denotes a tri-state output
- (OD) denotes an open drain output

Active low signals are denoted by a bar on top of the signal name and dual function pins are denoted with a slash between the two signals — A9/$\overline{\text{HCS1}}$.

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GENERAL

NAME	TYPE	DESCRIPTION
VDD		POWER SUPPLY PIN, VCC
GND		GROUND

HOST INTERFACE

A0:2	I	HOST ADDRESS LINES. The Host Address lines A(2:0) and A9 are used to access the various PC/AT control/status, and data registers.
A9/$\overline{\text{HCS1}}$	I	HOST ADDRESS LINE 9/HOST CHIP SELECT 1. This is a multiplexed input pin. When Register 48H-bit 3 is reset this input is HOST ADDRESS LINE 9, when the bit is set this input is HOST CHIP SELECT 1. When configured as active low $\overline{\text{HCS1}}$, this input is ignored when $\overline{\text{DACK}}$ is asserted.
$\overline{\text{HCS0}}$	I	HOST CHIP SELECT 0. This pin selects access to the control, status and data registers. This active low input is ignored when $\overline{\text{DACK}}$ is asserted.
$\overline{\text{IOCS16}}$	OD	16 BIT DATA TRANSFER. An open drain active low output that indicates that a 16-bit buffer transfer is active.
HINT	O	HOST INTERRUPT. Asserted active high to indicate to the Host that the controller needs attention.

PIN DESCRIPTION (Continued)

HOST INTERFACE (Continued)

NAME	TYPE	DESCRIPTION
$\overline{\text{IOCHRDY}}$	O,Z	I/O CHANNEL READY. Active low, this signal is asserted whenever the internal host FIFO is not ready to transfer data.
DREQ	O,Z	DMA REQUEST. The active high DMA Request signal is used during DMA transfer between the Host and the SSI 32C9301.
$\overline{\text{DACK}}$	I	DMA ACKNOWLEDGE. This active low signal is used during DMA to complete the DMA handshake for data transfer between the host and the controller.
$\overline{\text{IOR}}$	I	INPUT READ SELECT. This active low pin is asserted by the Host during a Host read operation. When asserted with $\overline{\text{HCS0}}$, $\overline{\text{HCS1}}$, or $\overline{\text{DACK}}$, data from the device is enabled onto the host data bus.
$\overline{\text{IOW}}$	I	INPUT WRITE SELECT. Asserted active low by the HOST during a HOST write operation. When asserted with $\overline{\text{HCS0}}$, $\overline{\text{HCS1}}$, or $\overline{\text{DACK}}$, data from the host data bus is strobed into the device.
HRESET	I/S	HOST RESET. This active high signal stops all commands in progress and initializes the control/status registers — see Design Guide for Register Reset conditions. This signal can also "wake up" the device while it is in power down mode.
HDB (15:0)	I/O	HOST DATA BUS. These bits are used for word transfers between the Buffer Memory and the Host; bits (7:0) are used for status, commands, or ECC byte transfers.

DISK INTERFACE

INDEX	I	INDEX. This input is a pulse that occurs once per revolution and defines the start of sector 0.
INPUT/	I/O	DISK SEQUENCER INPUT/OUTPUT. A general purpose control (output) and status (input) pin configured by the Output Enable Bit of Register 71H, bit 7.
OUTPUT		At power-on, this pin is an input. As an input, it can be used to synchronize the disk sequencer to an external event. As an output, it is controlled by bit 2 of the Control Field of the disk sequencer.
$\overline{\text{WAM}}$/ $\overline{\text{AMD}}$/ SECTOR	I/O	WRITE ADDRESS MARK/SECTOR/ADDRESS MARK DETECT. This pin is configured to operate in Hard or Soft Sector mode by initializing the Disk Formatter Mode Control Register: 4FH, bit 1. In the hard sector mode it is used as the sector input — a pulse on this pin indicates a sector mark is found. In the soft sector mode, an active low output is asserted when formatting to allow writing of address mark. When reading, an active low input indicates an address mark was detected. The device powers up in soft sector mode.
RG	O	READ GATE. This active high output enables the reading of the disk. It is asserted at the beginning of the PLO for header and data field by the sequencer — sequencer Control Field bits 5 and 6. It is automatically deasserted at the end of the CRC or ECC.
WG	O	WRITE GATE. This active high output enables writing onto the disk. It is asserted and deasserted by the sequencer Control Field bits 5 and 6.

DISK INTERFACE (Continued)

NAME	TYPE	DESCRIPTION
RRCLK	I/S	READ/REFERENCE CLOCK. This pin is used in conjunction with the NRZ pin to clock data in and out of the SSI 32C9001 device. This input must be glitch-free to ensure correct operation of the chip.
NRZ	I/O	NON RETURN TO ZERO. This signal is the serial read data input from the disk drive when the read gate signal is asserted; it is the write data output to the disk drive when the write gate signal is asserted.

MICROPROCESSOR INTERFACE

$\overline{RST}$	I	RESET. An asserted active low input generates a component reset that holds the internal registers of the SSI 32C9301 at reset, stops all operations within the chip, and deasserts all output signals. All input/output signals and Host outputs are set to the high-Z state.
ALE/M/$\overline{NM}$	I	ADDRESS LATCH ENABLE/MULTIPLEXED/NON-MULTIPLEXED ADDRESS SELECT. When tied high or left floating after reset, the microprocessor interface is configured as non-multiplexed. When driven low, then the microprocessor interface is configured as multiplexed. In this case this pin functions as the address latch enable, and the MA(7:0) pins are the demultiplexed address outputs.
CS	I	CHIP SELECT. This signal must be asserted high for all microprocessor accesses to the registers of this chip.
$\overline{WR}$/R/$\overline{W}$	I	WRITE STROBE/READ/WRITE. In the Multiplexed Microprocessors bus mode, when an active low signal is present with CS signal asserted high, the data on the AD0:7 is written to the internal registers. In the Non-Multiplexed Microprocessors bus mode, this signal acts as the R/$\overline{W}$ signal. A high on this input along with the $\overline{RD}$/DS signal high and the CS signal asserted high indicates a read operation. A low on this input along with the $\overline{RD}$/DS signal asserted and the CS signal asserted high indicates a write operation. See table below.

I/$\overline{MC}$	CS	$\overline{WR}$/R/$\overline{W}$	$\overline{RD}$/DS	Action	Mux/Non-Mux
High	High	Low	High	Write to internal registers.	M
High	High	High	Low	Read from internal registers.	M
Low	High	Low	High	Write to internal registers.	N
Low	High	High	High	Read from internal registers.	N
X	Low	X	X	No action.	M or N

Note: X denotes don't care.

$\overline{RD}$/DS	I	READ STROBE/DATA STROBE. In the Multiplexed Microprocessors bus mode, when an active low signal is present with CS signal high, internal registers will be accessed. In the Non-Multiplexed Microprocessors mode, this signal acts as the DS signal. A high on the DS, R/$\overline{W}$, and the CS signals, indicates a read operation. A low on the R/$\overline{W}$ signal, highs on both the DS and the CS, indicates a write operation to the internal registers.
$\overline{DINT}$	O, OD, Z	INTERRUPT. An active low signal indicates the controller is requesting microprocessor service from the disk side. This signal is programmable for either a push-pull with an internal pull up resistor or open-drain output circuit. This signal powers up in the high-Z state. Disk Formatter Mode Control Register, 4FH: bit 3 set high, programs this pin as a push-pull, and when set low programs it as an open drain output signal.

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MICROPROCESSOR INTERFACE (Continued)

NAME	TYPE	DESCRIPTION
AD7:0	I/O	ADDRESS/DATA BUS. When configured in the Multiplexed Microprocessors mode, these lines are multiplexed, bidirectional data path to the microprocessor. During the beginning of the memory cycle the bus captures the low order byte of the microprocessor address. These lines provide communication with the controller device's internal registers and the buffer memory. When configured in the Non-Multiplexed Microprocessors mode, these lines are bidirectional data lines.
MA(7:0)	I/O	MICROPROCESSOR ADDRESS BUS: This 8-bit output bus is the AD(7:0) bus latched by the ALE pin during the low order address phase of an Multiplexed Microprocessors type microprocessor cycle. These signals are nonmultiplexed address input when used with a non-multiplexed bus microprocessor — Non-Multiplexed Microprocessors interface.
READY/ $\overline{\text{AINT}}$	O	READY: When this signal is deasserted low, the microprocessor inserts wait states to allow time for the chip to respond to the access. Wait states are programmed by Buffer Mode Control Register — 53H: bits 7-6.
$\overline{\text{AINT}}$	O, OD, Z	AT BUS INTERRUPT. An active low signal indicates the controller is requesting microprocessor service from the AT host bus side. This signal is programmable for either a push-pull with an internal pull up resistor or open-drain output circuit. This signal powers up in the high-Z state. Disk Formatter Mode Control Register, 4FH: bit 3 set high, programs this pin as a push-pull, and when set low programs it as an open drain output signal.
I/$\overline{\text{MC}}$	I	INTEL/MOTOROLA: This signal selects the microprocessor interface to be used. When this signal is asserted high, it selects the Intel bus control interface. When this signal is deasserted low, it selects the Motorola bus control interface. This signal has an internal pull-up to allow the default selection of the Intel bus control interface.

BUFFER MANAGER INTERFACE

BA0:15	O	BUFFER MEMORY ADDRESS LINES 0:15. These sixteen outputs provide address lines for the dynamic memory or static memory chips used to implement the buffer memory.
BA16/$\overline{\text{RAS}}$	O	BUFFER MEMORY ADDRESS 16: In SRAM mode, this pin generates the address: A16 for direct connection to a Static RAM address line 16. BUFFER ROW ADDRESS STROBE: This active low output signal is generated to strobe the row — high order — address into the dynamic RAMs. It is intended to be directly tied to the RAMs input control pin.
BA17/$\overline{\text{CAS}}$	O	BUFFER MEMORY ADDRESS 17: In SRAM mode, this pin generates the address: A17 for direct connection to a Static RAM address line 17. COLUMN ADDRESS STROBE: This output signal is generated to strobe the column — low order address — into the dynamic RAM devices.
BD0:7	I/O	BUFFER MEMORY DATA BUS. 7 through 0. The bidirectional Data Bus connects directly to the buffer memory. This bus is designed for high speed data transfer.
BDP	I/O	BUFFER MEMORY DATA PARITY. This signal provides odd parity for the buffer memory data bus during transfers to/from the buffer memory.

BUFFER MANAGER INTERFACE (Continued)

NAME	TYPE	DESCRIPTION
$\overline{MOE}$	O	MEMORY OUTPUT ENABLE. This active low output controls the enabling of data onto the data bus by the dynamic RAMs or to indicate when every buffer memory access is active in SRAM mode.
$\overline{WE}$	O	WRITE ENABLE. This active low output signal is used to strobe the data into the RAMs from the Data bus. For both buffer memory applications, this line is tied directly to the SRAM or DRAM control pin.
SYSCLK	I	SYSTEM CLOCK. This signal is used to synchronize the buffer RAM access, including the generation of memory address lines, write enable $\overline{WE}$, and memory output enable $\overline{MOE}$. In power down mode, this signal is shut off from the internal logic and hence buffer memory access is inhibited.
$\overline{MS}$	O	Memory selected, asserted active low.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC operating characteristics.

PARAMETER	RATING
Power Supply Voltage, VCC	7V
Ambient Temperature	0 to 70°C
Storage Temperature	-65 to 150°C
Power Dissipation	220 mW
Input, Output pins	-0.5 to VCC+0.5V

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ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VCC Power Supply Voltage		2.7		3.9	V
ICC Supply Current				40	mA
ICCS Supply Current	Note 1			500	µA
VIL Input Low Voltage		-0.5		0.5	V
VIH Input High Voltage		1.8		VCC+0.5	V
VOL Output Low Voltage	Note 2			0.3	V
VOL Output Low Voltage	Note 3			0.4	V
VOH Output High Voltage IOH = -400 µA		2.0			V
IL Input Leakage Current 0 < VIN < VCC		-10		10	µA
CIN Input Capacitance				10	pF
COUT Output Capacitance				10	pF

Note: (1) Synchronization and Clock Control Register, 7FH: bits 3 and 4 set. RRCLK and SYSCLK internally inhibited.
(2) All interface pins except Host Interface pins. IOL= 2 mA.
(3) Host Interface pins, IOL=24 mA.

SSI 32C9301
PC-AT Combo Controller
With Reed Solomon, 3V Operation

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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Section 9

FLOPPY DISK DRIVE CIRCUITS

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SSI 34P553/5531
Pulse Detector & Data Synchronizer
Preliminary Data

December 1991

DESCRIPTION

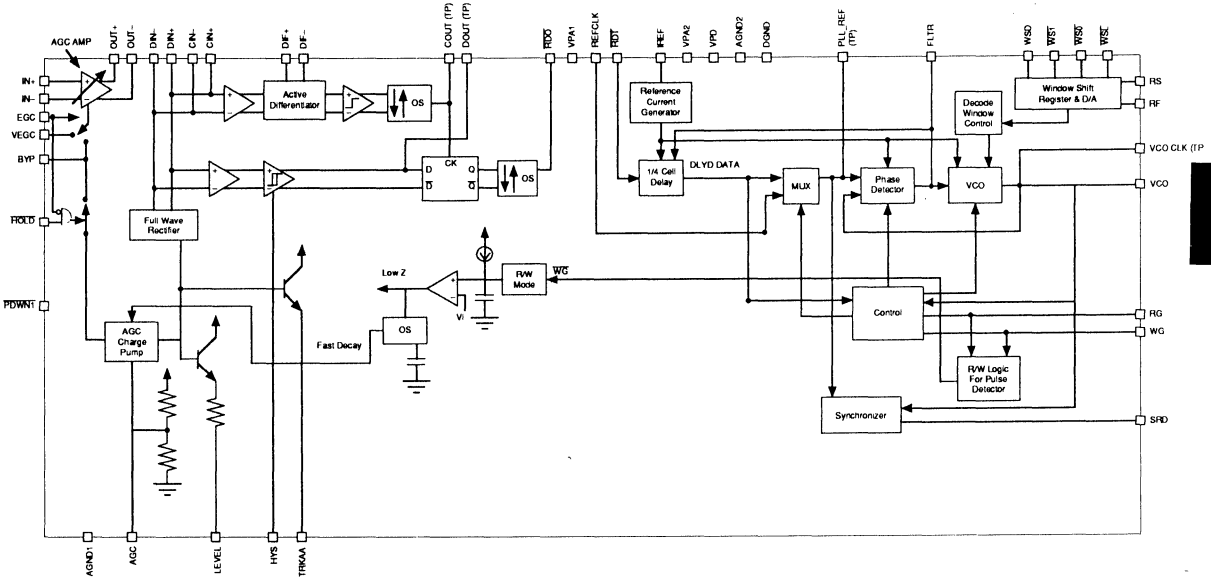
The SSI 34P553/5531 is a low power, high performance Pulse Detection, Data Synchronization combination device. This device is designed for use in low power applications requiring +5V only power supplies. The pulse detection portion of this device detects and validates amplitude peaks in the output from a disk drive read amplifier. The data synchronization portion is an MFM and 1, 7 data synchronizer with window shift capability. The SSI 34P553/5531 achieves low system operating power two ways, with a low operating power (+5V only design) and with a power down mode. The power down mode is a complete shutdown or sleep mode. The SSI 34P553/5531 is available in a 52-pin fine pitch QFP.

The 34P5531 is the same device, but with separate CIN+, DIN+ inputs, for use with active filters such as the SSI 32F8030.

FEATURES

- **Highly Integrated Pulse Detector and Data Synchronizer**
- **+5V only Power Supplies**
- **790 mW max. power**
- **Low Pulse Pairing**
- **0.6-1.6 Mbit/s operation**

BLOCK DIAGRAM



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CAUTION: Use handling procedures necessary for a static sensitive component.

CIRCUIT OPERATION

PULSE DETECTOR SECTION

READ MODE

The SSI 34P553/5531 enters into the read mode when the WG pin is pulled low. In the read mode, the SSI 34P553/5531 provides amplification and pulse level qualification of the signal applied to the input pins of the AGC amplifier.

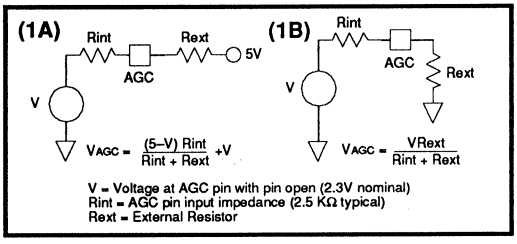
AGC AMPLIFIER

An amplified head output signal is AC coupled to the IN+ and IN- pins of the AGC amplifier. To control the gain of the AGC amplifier, the signal at the DIN± pins is full-wave rectified and amplified. The resulting voltage is compared to the voltage level present at the AGC pin. If the voltage level is higher than the AGC pin reference level, the SSI 34P553/5531 will enter into an attack mode. If it is lower than the AGC pin voltage the device will enter into a decay mode.

Attack Mode. The SSI 34P553/5531 contains a dual rate attack charge pump that is controlled by the instantaneous level at DIN±. When the voltage from the full wave rectifier exceeds the AGC pin voltage by greater than 125%, a fast attack mode is entered. During fast attack, 1.4 mA of current is supplied to the network on the BYP pin. When the full wave rectifier voltage exceeds the AGC pin voltage by 100 to 125%, the slow attack mode is entered. During slow attack the charge current supplied to the BYP pin is 0.18 mA. This dual rate charge pump allows the AGC to recover rapidly during write to read transitions while minimizing distortion once the AGC amplitude is within range.

Decay Mode. Two internally controlled decay modes are provided by the SSI 34P553/5531. Upon a switch to write mode, the device holds the gain at its last value and the AGC inputs are switched to low impedance. When the device is switched back from write to read, the gain remains held and the AGC inputs remain in a low impedance state for 0.9 µs. At this time, if the new gain required is more than the held value the device enters into the decay mode. A fast decay current of 0.12 mA is automatically switched on for a period of 0.9 µs. After 0.9 µs the device will sink a steady state slow decay current of 4.5 µA (reference Figure 7.)

AGC Level Control. The AGC level is controlled by the voltage presented on the AGC pin. The AGC pin is internally biased at approximately 2.3V which sets the signal at the DIN± pins to 1.0 Vpp under nominal conditions. The voltage at the AGC pin can be externally controlled by connecting a resistor between the AGC pin and either VPA1 or AGND1. When a resistor is connected from AGC to VPA1 the voltage on the AGC pin can be increased (Figure 1a). When a resistor is connected from AGC to AGND1 the voltage on the AGC pin can be decreased (Figure 1b). The new DIN± input target level is nominally (VAGC -0.75)•0.64 Vpp. The output of the AGC amplifier has a maximum swing of 3.0 Vpp that can be controlled using the AGC pin. The 3.0 Vpp swing supports the use of external filters that have up to 6 dB of loss. A multi-pole Bessel filter is typically used for its linear phase or constant group delay characteristics.



FIGURES 1A & 1B: AGC Voltage

The gain of the AGC amplifier is directly controlled by the voltage at the BYP pin (VBYP) or the VEGC pin as shown in Figure 2. The AGC amplifier has open collector outputs that can sink up to 4.0 mA of current. For correct operation over the gain range each output should be pulled up to VPAI through a 340 Ω resistor as shown in Figure 3.

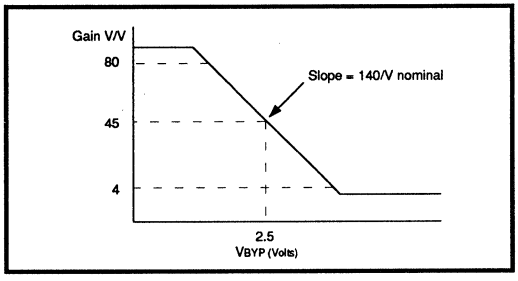


FIGURE 2: AGC Gain

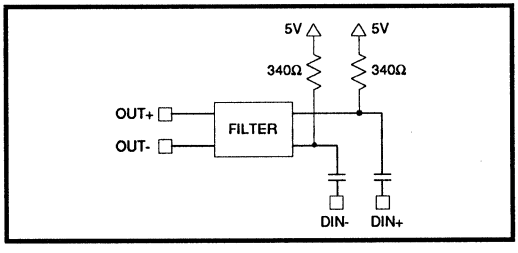


FIGURE 3: AGC Filter

PULSE QUALIFICATION

The SSI 34P553/5531 uses both amplitude and time qualification to digitize the incoming data pulses. In the amplitude channel the signal is sent to a hysteresis comparator. A hysteresis trip level is externally set such that only pulses that exceed the required signal level will trip the comparator. This prevents false qualification of baseband noise. The hysteresis trip level can be either a fixed level or a fraction of the DIN +/- voltage level.

Hysteresis Level. A fixed hysteresis level can be set by applying a DC voltage to the HYS pin. This is a simple method for hysteresis control but it does not compensate well for internal variances from device to device. A more effective approach is to feed forward a percentage of the voltage level at the DIN± pins. This approach is accomplished by using a filter/divider network between the LEVEL and HYS pins. The LEVEL pin output voltage is a rectified and amplified version of the voltage level applied to the DIN± pins. The gain in this circuit is set so that a 1 Vpp signal applied to DIN+/- will result in a 1 Vpk (typical) output signal at the LEVEL pin. An external capacitor to AGND1 should be used on the LEVEL pin to maintain a DC level. An external voltage divider can be connected between the LEVEL pin and AGND1 to provide the hysteresis programming voltage to the HYS pin. The HYS pin voltage determines the percentage of the DIN+/- input signal that will trip the hysteresis comparator of the SSI 34P553/5531. The transfer function of the HYS pin for setting the threshold percentage is:

$$\text{Hysteresis Threshold} = 0.36 \times \text{VHYS}$$

where VHYS is the voltage applied to the HYS pin. For example, with a 1.0 Vpp signal at DIN+/- the LEVEL pin output will be 1.0 Vpk. Using a 50% resistor divider between LEVEL and AGND1 would result in a HYS pin voltage of 0.5 V and that would produce a hysteresis threshold of 0.18 V in both the positive and negative direction. This translates to a hysteresis threshold percentage of 36% of DIN+/-.

Because the SSI 34P553/5531 circuits are internally biased to the same levels, the technique of feeding forward the LEVEL pin voltage helps to offset process related internal tolerance variations. In addition, the feed forward technique speeds up transient recovery by allowing qualification of input pulses while the AGC is still settling, such as during write to read recovery or head change recovery. Care should be taken in selecting the hysteresis level time constant so that pattern induced low amplitude signals are not missed. The SSI 34P553/5531 has a built in minimum of ±50 mV threshold for level qualification even when the HYS pin is grounded. This prevents false triggering due to baseband noise during a DC erase gap.

The outputs of the hysteresis comparator are the "D" inputs of the D-type flip-flop. One side of the hysteresis comparator outputs is provided as the DOUT pin test point. The DOUT pin can be monitored by connecting a 3 to 6 kΩ resistor to AGND2. When the DOUT pin is not used, it can be pulled up to VPA2 to save power.

In the time channel the signal is differentiated to transform signal peaks to zero crossings which are detected and used to trigger a bi-directional one-shot. The one-shot output pulses are used as the clock input of the D flip-flop. The COUT pin provides the one-shot output for test purposes. It also requires an external 3 to 6 KΩ pull-down resistor for testing.

The differentiator function is accomplished by an external network between the DIF+ and DIF- pins. The transfer function from DIN± to the comparator input (not DIF±) is:

$$Av = \frac{-2000Cs}{LCs^2 + C(R+92)s + 1}$$

where: C, L, R are external passive components
$20\ pF < C < 500\ pF$
$s = j\omega = j2\pi f$

During normal operation, the time channel clocks the D flip-flop on every positive and negative peak of the DIN± input. The D input to the flip-flop only changes state when the DIN± input exceeds the hysteresis comparator threshold opposite in polarity to the previous threshold exceeding peak.

The time channel, then, determines signal peak timing and the amplitude channel determines validity by blocking signal peaks that do not exceed the hysteresis comparator threshold. The delays in each of these channels to the D flip-flop inputs are well matched. The D flip-flop output triggers a one-shot that sets the $\overline{RDO}$ output pulse width.

WRITE MODE

In Write Mode the SSI 34P553/5531 Pulse Detector section is disabled and preset for the following Read Mode. The digital circuitry is disabled, ($\overline{RDO}$ pin held high), the input AGC amplifier gain is held at its previous value and the AGC amplifier input impedance is reduced.

Holding the AGC amplifier gain and reducing input impedance shortens system Write to Read recovery times.

The lowered input impedance improves settling time by reducing the time constant of the network between the SSI 34P553/5531 and a head preamplifier such as the SSI 32R1200R. Write to read timing is controlled to maintain the reduced impedance for 0.9 µs before the AGC circuitry is activated. Coupling capacitors should be chosen with as low a value as possible consistent with adequate bandwidth to allow more rapid settling.

DATA SYNCHRONIZER SECTION

The SSI 34P553/5531 is designed to perform data synchronization in rotating memory systems which utilize a 1, 7 RLL and MFM encoding format. In the Read Mode the SSI 34P553/5531 performs Data Synchronization. The interface electronics and architecture of the SSI 34P553/5531 have been optimized for use as a companion device to the WD 42C22 controllers.

The SSI 34P553/5531 can operate with data rates ranging from .6 to 1.6 Mbit/s. This data rate is established by a single 1% external resistor, RR, connected from pin IREF to VPA2. This resistor establishes a reference current which sets the VCO center frequency, the phase detector gain, and the 1/4 cell delay. The value of this resistor is given by:

$$RR = \frac{5.97}{DR} - 1.78\,(k\Omega)\ \text{MFM}$$

$$RR = \frac{7.96}{DR} - 1.78\,(k\Omega)\ 1,7$$

Where: DR = Data Rate in Mbit/s

An external TTL compatible reference may be applied to REFCLK

The SSI 34P553/5531 employs a Dual Mode Phase Detector: Harmonic in the Read Mode and Non-Harmonic in Write and Idle Modes. In the Read Mode the Harmonic Phase Detector updates the PLL with each occurrence of a DLYD DATA pulse. In the Write and Idle Modes the Non-Harmonic Phase Detector is continuously enabled, thus maintaining both phase and frequency lock. By acquiring both phase and frequency lock to the crystal reference oscillator and utilizing a zero phase restart technique, false lock to DLYD DATA is eliminated.

The phase detector incorporates a charge pump in order to drive the loop filter directly. The polarity and width of the output current pulses correspond to the direction and magnitude of the phase error. Figure 4 depicts the average output current as function of the input phase error (relative to the VCO period.)

The READ GATE (RG), and WRITE GATE (WG), inputs control the device mode as described in Table 1. RG is an asynchrouous input and may be initiated or terminated at any position on the disk. WG is also an asynchronous input, but should not be terminated prior to the last output Write Data pulse.

READ OPERATION

The Data Synchronizer utilizes a fully integrated fast acquisition PLL to accurately develp the decode window. Read Gate, RG, initiates the PLL locking sequence and selects the PLL reference input; a high level (Read Mode) selects the Read Data input and low level selects the crystal reference oscillator.

In the Read Mode the rising edge of DLYD DATA enables the Phase Detector while the falling edge is phase compared to the rising edge of the VCO. As depicted in Figure 5, DLYD DATA is a 1/4 cell wide (TVCO/2) pulse whose leading edge is defined by the leading edge of Read Data. VCO is generated from the rising edges of the VCO clock. By utilizing a fully integrated symmetrical VCO running at the code rate, VCO is insured to be accurate and centered symmetrically about the falling edges of DLYD DATA. The accuracy of the 1/4 cell delay only affects the retrace angle of the phase detector and does not influence the accuracy of VCO.

Shifting the symmetry of the VCO clock effectively shifts the relative position of the DLYD DATA pulse within the decode window. This powerful capability easily facilitates defect mappings, automatic calibration, window margin testing, error recovery, and systematic error cancellation. For enhanced disk drive testability and error recovery, decode window control is provided via a µP port ($\overline{WSL}$, WSD, $\overline{WS0}$, $\overline{WS1}$) as described in Table 2. In application not utilizing this feature, $\overline{WSL}$ should be left open or connected to VPA2, while WSD, $\overline{WS0}$, and $\overline{WS1}$ can be left open.

Window shifts in the range of ±5% to ±20% of TVCO are easily programmed by latching the appropriate control word into the Window Shift Register with the WSL pin. Shifts in the positive or negative directions result in early or late decode windows respectively, as depicted in Figure 6. Additionally, for small systematic error cancellation, a resistor, R, connected from either RS (Early) or RF (Late) to ground will provide analog control over the decode window. The magnitude of this shift, TSA is determined by:

$$TSA = 0.25\,TVCO\left(1 - \frac{3260+R}{5950+R}\right)$$

Where: R is in Ω

Pins RF and RS are intended to be used as a trim and should be restricted to ±3% window shifts. They can be used in conjunction with the digital control port.

In Non-Read Modes, the PLL is locked to REFCLK. This forces the VCO to run at a frequency which is very close to that required for tracking actual data and thus minimizes the associated frequency step during acquisition. When RG transitions, the VCO is stopped momentarily, then restarted in an accurate phase alignment with the next PLL reference input pulse. By minimizing the phase alignment in this manner, the acquisition time is substantially reduced.

POWER DOWN MODE

A power down mode is provided to reduce power usage during the idle periods. Taking $\overline{PDWN1}$ low causes the device to go into complete shutdown.

MODE CONTROL

The SSI 34P553/5531 circuit mode is controlled by the $\overline{PDWN1}$, $\overline{HOLD}$, RG, and WG pins as shown in Table 1.

TABLE 1: Mode Control

WG	RG	$\overline{HOLD}$	$\overline{PDWN1}$	
0	0	1	1	Read Mode VCO Locked to XTAL
0	1	1	1	Read Mode VCO Locked to Read Data
0	X	0	1	Read Mode AGC gain held constant*
1	0	X	1	Write Mode AGC gain held constant* Input impedance reduced
X	X	X	0	Power shutdown mode

* AGC gain will drift at a rate determined by BYP capacitor and Hold mode leakage current.

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TABLE 2: Decode Window Symmetry Control

Ts, NOMINAL WINDOW SHIFT	WSD	$\overline{WS1}$	$\overline{WS0}$
+TS3	0	0	0
+TS2	0	0	1
+TS1	0	1	0
0	0	1	1
-TS3	1	0	0
-TS2	1	0	1
-TS1	1	1	0
0	1	1	1

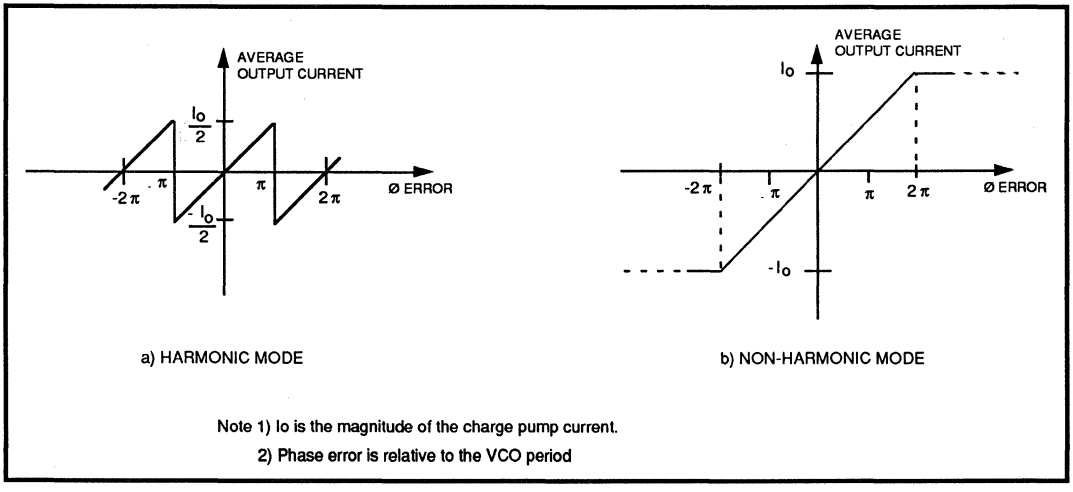

FIGURE 4: Phase Detector Transfer Function

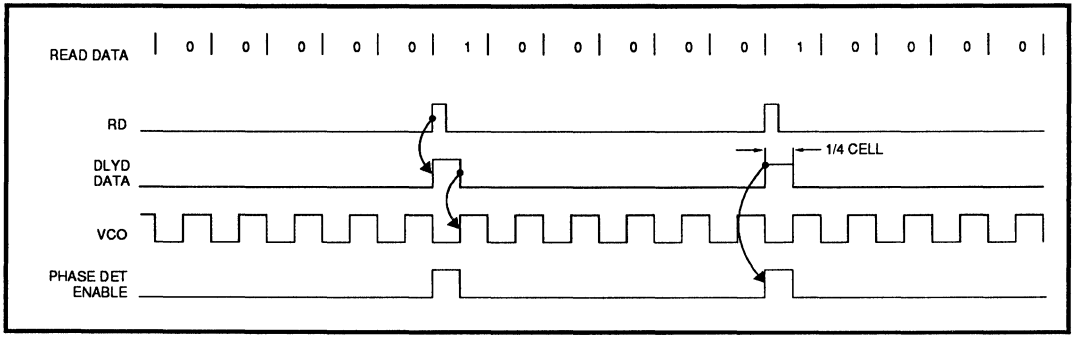

FIGURE 5: Data Synchronization Waveform Diagram

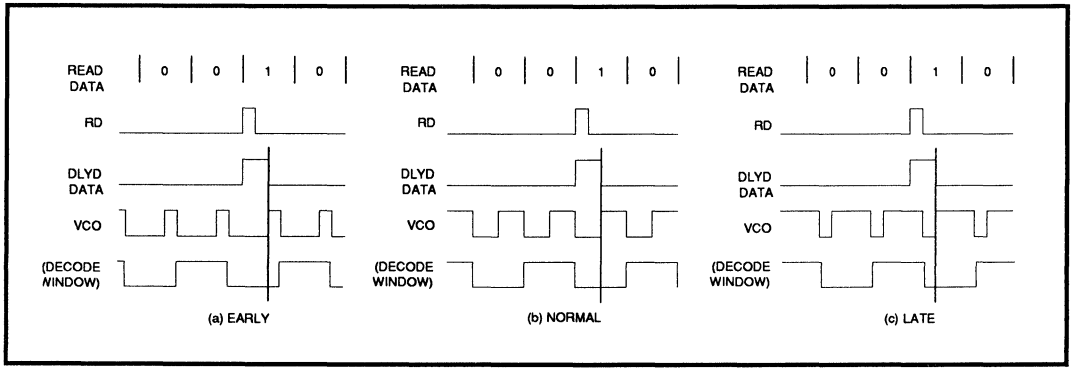

FIGURE 6: Decode Window

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
VPA1	I	Analog (+5V) power supply for pulse detector.
AGND1	I	Analog ground pin for pulse detector block.
VPA2	I	Analog (+5V) supply pin for data synchronizer block.
AGND2	I	Analog ground pin for data synchronizer block.
VPD	I	Digital (+5V) power supply pin.
DGND	I	Digital ground pin.
IN+, IN–	I	Analog signal input pins.
OUT+, OUT–	O	Read path AGC Amplifier output pins.
DIN+, DIN–	I	Analog input to the hysteresis comparator, and differentiator.
CIN+, CIN–	I	Analog input to the clock comparator, differentiator. In the 34P553/5531, CIN+ is connected to DIN+, CIN– is connected to DIN–.
DIF+, DIF–	I/O	Pins for external differentiating network.
COUT	O	Test point for monitoring the flip-flop clock input. Pull down resistor required.
DOUT	O	Test point for monitoring the flip-flop D-input. Pull down resistor required.
BYP	I/O	An AGC timing capacitor or network is tied between this pin and AGND1.
AGC	I	Reference input voltage for the read data AGC loop.
LEVEL	O	Output from fullwave rectifier that may be used for input to the hysteresis comparator.
HYS	I	Hysteresis level setting input to the hysteresis comparator.
TRKAA	O	Full wave rectifier output. This output has the same DC level as the LEVEL pin, i.e., $\leq 0.3V$ with no AC signal and $\approx 1V_{OP}$ with a $1V_{PP}$ AC signal at DIN+/ DIN-.
$\overline{\text{HOLD}}$	I	TTL compatible pin that holds the AGC gain when pulled low.
EGC	I	External Gain Control. This is a TTL input pin that allows the AGC gain to be controlled by either BYP or the VEGC pin voltage. When AGE is high, the AGC gain is controlled by VEGC and the internal charge pump to BYP is disabled.
VEGC	I	The voltage at this pin is used to control the AGC gain when the EGC pin is held high.
$\overline{\text{RDO}}$	O	Read Data Output. This is the TTL output from the pulse detector. This signal may be fed directly into the $\overline{\text{RDT}}$ input.
IREF	I	Timing program pin: the VCO center frequency, Phase Detector Gain and the 1/4 cell delay are a function of the current source into pin IREF. The current is set by an external resistor, RR connected from IREF to VPA2.
FLTR	I/O	Filter pin: the phase detector output and VCO input node. The loop filter is connected to this pin.

PIN DESCRIPTION (Continued)

NAME	TYPE	DESCRIPTION
SRD	O	Synchronized Read Data: read data that has been re-synchronized to VCO clock.
WSD	I	Window Symmetry Direction: controls the directions of the optional window symmetry shift. Pin WSD has an internal resistor pull-up.
$\overline{WS0}$	I	Window symmetry control bit: a low level introduces a window shift of 5% TORC (read reference clock period) in the direction established by WSD pin. $\overline{WS0}$ has an internal resistor pull-up.
$\overline{WS1}$	I	Window Symmetry Control bit: a low level introduces a window shift of 15% TORC (read reference clock period) in the direction established by WSD. A low level at both $\overline{WS0}$ and $\overline{WS1}$ will produce the sum of the two window shifts. Pin $\overline{WS1}$ has an internal resistor pull-up.
$\overline{WSL}$	I	Window Symmetry Latch: used to latch the input window symmetry control bits WSD, $\overline{WS0}$, $\overline{WS1}$ into the internal DAC. An active low level latches the input bits.
RF, RS	I	WINDOW SYMMETRY ADJUST PINS: Provides analog control over the decode window symmetry; typically used to null out any window symmetry offset. A resistor connected from either RF or RS to AGND will provide magnitude and direction control. They can be used in conjunction with the digital control port WSD, $\overline{WS0}$, $\overline{WS1}$.
RG	I	Read gate: selects the PLL reference input and initiates the PLL synchronization sequence. A high level selects the internal RD± inputs. A low level selects the crystal reference oscillator, Pin RG has an internal resistor pullup.
WG	I	Write Gate: enables the write mode. Pin WG has an internal resistor pullup.
VCO CLK	O	VCO CLK: An open emitter ECL output test point. Two external resistors are required to perform this test. They should be removed during normal operation for reduced power dissipation.
$\overline{RDT}$	I	Read Data input. This TTL input comes from the $\overline{RDO}$ output of the pulse detector. This signal is active low.
$\overline{PDWN1}$	I	Power Down input. When this input is low, the chip enters low power mode. This pin has an internal pullup resistor, and may be left open or tied high if not used.
REF CLK	I	Reference Clock. This is a TTL input at the code rate that is used as the reference for the VCO in idle mode.
VCO	O	VCO output. This is the VCO signal converted to a TTL level.
PLL_REF	O	PLL Reference Test Point. In write and idle modes, this is the reference oscillator signal. In read mode, it is the delayed read data (DRD) signal. This is an ECL level output. PLL_REF can be compared to VCOCLK to see the window centering accuracy.

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, 4.75V ≤ VPA 2 ≤ 5.25V, 25°C ≤ Tj ≤ 135°C, 1.2 MHz ≤ 1/TVCO ≤ 2.4 MHz.

ABSOLUTE MAXIMUM RATINGS

Operation outside these rating limits may cause permanent damage to this device.

PARAMETER	RATING	UNIT
5V Supply Voltage, VPA1, VPA2, VPD	6.0	V
Pin Voltage (Analog pins)	-0.3 to VPA1, 2 + 0.3	V
Pin Voltage (All others)	-0.3 to VPD + 0.3 or +12 mA	V
Storage Temperature	-65 to 150	°C
Lead Temperature (Soldering 10 sec.)	260	°C

RECOMMENDED OPERATING CONDITIONS

Currents flowing into the chip are positive.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Supply Voltage (VPA1, 2 & VPD)		4.5	5.0	5.5	V
Tj Junction Temperature		25		135	°C

POWER SUPPLY

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
IVPA1, 2 Supply Current IVPD	Outputs unloaded $\overline{PDWN1}$= high or open		110	143	mA
	$\overline{PDWN1}$ = low Outputs unloaded		44	57	mA
Pd Power dissipation	Ta = 25°C, outputs unloaded $\overline{PDWN1}$= high or open		550	790	mW
	$\overline{PDWN1}$ = low Outputs unloaded		220	315	mW

LOGIC SIGNALS

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
VIL Input Low Voltage		-0.3		0.8	V
VIH Input High Voltage		2.0		VCC+0.3	V
IIL Input Low Current	VIL = 0.4V	0.0		-0.4	mA
IIL WG Input Low Current	VIL = 0.4V	0.0		-0.8	mA
IIH Input High Current	VIH = 2.4V			100	µA
VOL Output Low Voltage	IOL = 4.0 mA			0.5	V
VOH Output High Voltage	IOH = -400 µA	2.4			V
VOHT Test Point Output High Level PLL_ REF, VCOCLK	262Ω to VPD 402Ω to GND VPD = 5.0V VOHT - VPD		-.85		V
VOLT Test Point Output Low Level PLL_REF, VCOCLK	262Ω to VPD 402Ω to GND VPD = 5.0V, VOHT - VPD		-1.75		V

* Output load is a 4K resistor to 5V and a 10 pF capacitor to DGND.

MODE CONTROL

Enable to/from $\overline{\text{PDWN1}}$ Transition Time	Settling time of external capacitors not included, $\overline{\text{PDWN}}$ pin high to/from low			20	µs
Read to Write Transition Time	WG pin low to high			1.0	µs
Write to Read Transition Time	WG pin high to low AGC setting not included	0.4	0.9	1.6	µs
$\overline{\text{HOLD}}$ On to/from $\overline{\text{HOLD}}$ Off Transition Time	$\overline{\text{HOLD}}$ pin high to/from low			1.0	µs
RG Time Delay				100	ns

READ MODE (WG is low)

AGC AMPLIFIER

Unless otherwise specified, recommended operating conditions apply. Input signals are AC coupled to IN±. OUT± are loaded differentially with 340Ω x 2 to VPA1, and each side is loaded with < 10 pF to AGND1, and AC coupled to DIN±. A 0.1 µF capacitor is connected between BYP and AGND1. AGC pin is open.

Gain Range	1.0 Vpp ≤ (OUT+) - (OUT-) ≤ 3.0 Vpp	4		80	V/V
AGC Input Range		25		250	mVpp
Output Offset Voltage Variation	Over entire gain range	-500		+500	mV
Maximum Output Voltage Swing	Set by BYP or VEGC pin	3.0			Vpp
Differential Input Resistance	(IN+) - (IN-) = 100 mVpp @ 2.5 MHz	4	5.4	7.5	kΩ

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AGC AMPLIFIER (Continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Differential Input Capacitance	(IN+) - (IN-) = 100 mVpp @ 2.5 MHz		5	10	pF
Single Ended Input	WG = low, IN+ or IN-	2	2.7	3.8	kΩ
Impedance	WG = high, IN+ or IN-		160	250	Ω
Input Noise Voltage	Gain set to maximum		5	15	nV/√Hz
Bandwidth	-3 dB bandwidth at maximum gain	15			MHz
OUT+ & OUT- Pin Current	No DC path to AGND1	2.5	4.0		mA
CMRR (Input Referred)	(IN+) = (IN-) = 100 mVpp @ 5 MHz, gain set to max	40			dB
PSRR (Input Referred)	VPA1, 2 = 100 mVpp @ 5 MHz, gain set to max	30			dB
(DIN+) - (DIN-) Input Swing vs. AGC Input (DIN+) - (DIN-) = (V_{AGC} - K1) • K2	25 mVpp ≤ (IN+) - (IN-) ≤ 250 mVpp, $\overline{HOLD}$ = high, 0.5 Vpp ≤ (DIN+) - (DIN-) ≤ 1.5 Vpp				
	K1	0.5	0.8	0.95	V
	K2	0.54	0.64	0.74	Vpp/V
(DIN+) - (DIN-) Input Voltage Swing Variation	25 mVpp ≤ (IN+) - (IN-) ≤ 250 mVpp			5.0	%
AGC Voltage	AGC open	2.0	2.3	2.6	V
AGC Pin Input Impedance		1.8	2.5	3.8	kΩ
Slow AGC Discharge Current	(DIN+) - (DIN-) = 0V, AGC pin open	2.8	4.5	6	µA
Fast AGC Discharge Current	Starts at 0.9 µs after WG goes low, stops at 1.8 µs after WG goes low		0.12		mA
BYP Leakage Current	$\overline{HOLD}$ = low	-0.2		+0.2	µA
Slow AGC Charge Current	(DIN+) - (DIN-) = 0.563 VDC, AGC pin open	-0.11	-0.18	-0.25	mA
Fast AGC Charge Current	(DIN+) - (DIN-) = 0.8 VDC, AGC pin open	-0.9	-1.4	-1.9	mA
Fast to Slow Attack Switchover Point	$\frac{[(DIN+)-(DIN-)]}{[(DIN+)-(DIN-)]FINAL}$		125		%

AGC AMPLIFIER (Continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Gain Decay Time (Td)	(IN+) - (IN-) = 250 mVpp to 125 mVpp @ 0.6 MHz, (OUT+) - (OUT-) to 90% final value	60	100	180	µs
	(IN+) - (IN-) = 50 mVpp to 25 mVpp at 0.6 MHz (OUT+) - (OUT-) to 90% final value	190	300	550	µs
Gain Attack Time	WG = high to low (IN+) - (IN-) = 250 mVpp @ 0.6 MHz, (OUT+) - (OUT-) to 110% final value	3	8	15	µs

WRITE MODE (WG is high)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Single Ended Input Impedance (Each Side)	IN+ or IN-		160	250	Ω

HYSTERESIS COMPARATOR

Unless otherwise specified, recommended operating conditions apply. Input (DIN+) - (DIN-) is an AC coupled, 1.0 Vpp, 0.6 MHz sine wave. 0.5 VDC is applied to the HYS pin. WG pin is low.

Input Signal Range				1.5	Vpp
Differential Input Resistance	(DIN+) - (DIN-) = 100 mVpp @ 0.6 MHz	4	5	7	kΩ
Differential Input Capacitance	(DIN+) - (DIN-) = 100 mVpp @ 0.6 MHz		4	8	pF
Single Ended Input Impedance (Each Side)	DIN+ or DIN-	2	2.5	3.5	kΩ
Level Pin Output Voltage vs. (DIN+) - (DIN-)	0.6 Vpp < (DIN+) - (DIN-) < 1.5 Vpp, 10K between LEVEL and AGND	0.85	1	1.15	V/Vpp
Level Pin Output Impedance	I_{LEVEL} = 0.2 mA	100	200	300	Ω
Level pin Maximum Output Current		1.5			mA
Hysteresis Voltage at DIN± vs. HYS Pin Voltage	0.3 V < HYS < 1.0V	0.32	0.36	0.44	V/V

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HYSTERESIS COMPARATOR (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
HYS Pin Current	0.3 V < HYS < 1.0V	0.0		-5	µA
DOUT Pin Output Low Voltage	5 kΩ from DOUT to AGND2	VPA2 -2.5	VPA2 -2	VPA2 -1.35	V
DOUT Pin Output High Voltage	5 kΩ from DOUT to AGND2	VPA2 -2.0	VPA2 -1.6	VPA2 -1.1	V

ACTIVE DIFFERENTIATOR

Unless otherwise specified, recommended operating conditions apply. Input (DIN+) - (DIN-) is an AC-coupled, 1.0 Vpp, 0.6 MHz sine wave. 100Ω in series with 265 pF are tied from DIF+ to DIF-.

Input Signal Range				1.5	Vp-p
Differential Input Resistance	(CIN+) - (CIN-) = 100 mVp-p @ 2.5 MHz	8	10	14	kΩ
Differential Input Capacitance	(CIN+) - (CIN-) = 100 mVp-p @ 2.5 MHz			5.0	pF
Common Mode Input Impedance	Both sides	2.0	2.5	3.5	kΩ
Voltage Gain From CIN± to DIF±	(DIF+ to DIF-) = 2 kΩ		1		V/V
DIF+ to DIF- Pin Current	Differentiator impedance must be set so as to not clip the signal for this current level	±0.7			mA
COUT Pin Output Low Voltage	5 kΩ from COUT to GND	VPA2 -2.5	VPA2 -2	VPA2 -1.35	V
COUT Pin Output High Voltage	5 kΩ from COUT to GND	VPA2 -2	VPA2 -1.6	VPA2 -1.1	V
COUT Pin Output Pulse Width			36		ns

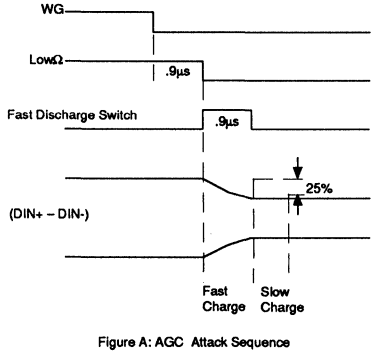


Figure A: AGC Attack Sequence

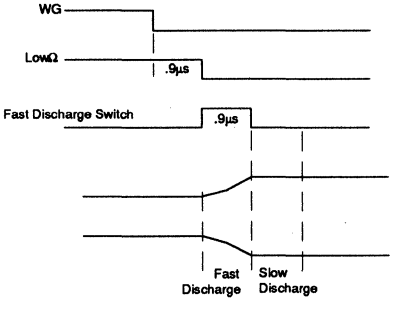


Figure B: AGC Decay Sequence

FIGURE 7: AGC Timing Diagram

QUALIFIER TIMING (See Figure 8)

Unless otherwise specified, recommended operating conditions apply. Inputs (DIN+) - (DIN-) are an AC coupled, 1.0 Vpp, 0.6 MHz sine wave. 100Ω in series with 265 pF are tied from DIF+ to DIF-. 0.5V is applied to the HYS pin. COUT and DOUT have a 5 kΩ pull-down resistor (for test purposes only.) WG pin is low. $\overline{RDO}$ is loaded with a 4 kΩ resistor to VPD and a 10 pF capacitor to DGND.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Td1	D Flip-Flop Set Up Time	Minimum allowable time delay from (DIN+) - (DIN-) exceeding hysteresis point to (DIF+) - (DIF-) hitting a peak value.	0			ns
Td3	Propagation Delay			60	110	ns
|Td3-Td4|	Pulse Pairing				6	ns
Td5	Output Pulse Width		25	36	55	ns

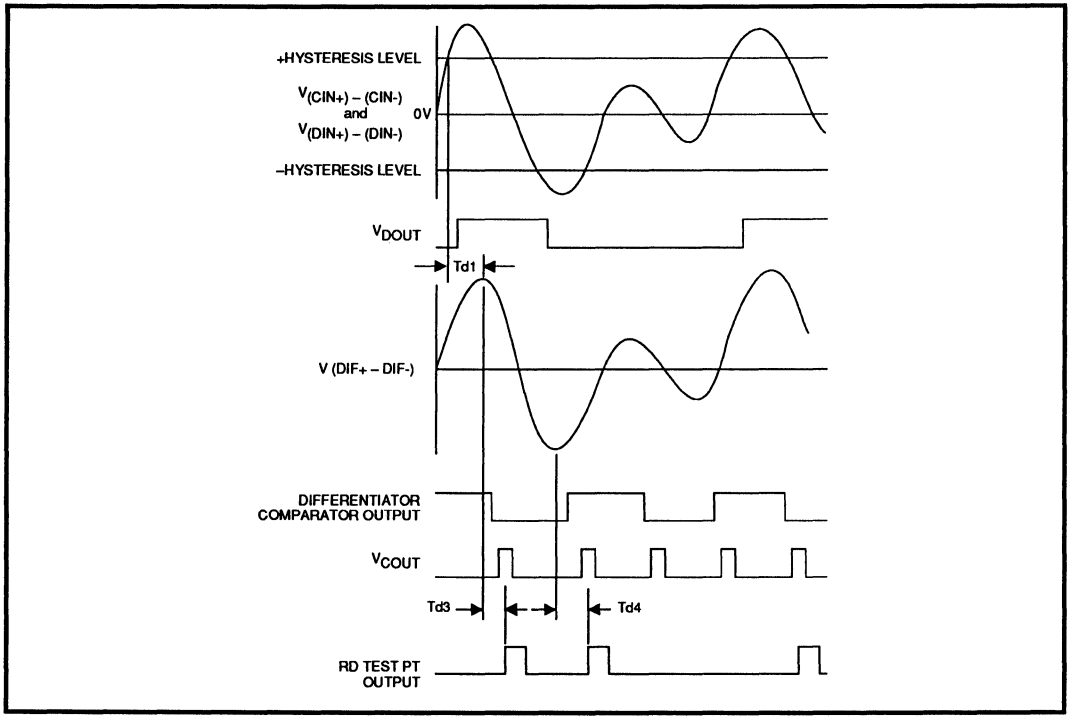


FIGURE 8: Read Mode Digital Section Timing Diagram

9

SYNCHRONIZER SECTION

READ MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
TRVCO, VCO Output Rise Time	0.8V to 2.0V, CL ≤ 15 pF			8	ns
TFVCO, VCO Output Fall Time	2.0V to 0.8V, CL ≤ 15 pF			5	ns
TSRD, SRD Output Pulse Width		(TVCO)-12		(TVCO)+12	ns
TRSRD, Read Data Rise Time	0.8V to 2.0V, CL ≤ 15 pF			10	ns
TFSRD, Read Data Fall Time	2.0V to 0.8V, CL ≤ 15 pF			8	ns
TPSRD, SRD Output Setup/HoldTime	Falling edge of VCO to either edge of SRD	-15		15	ns
TRD, $\overline{RDT}$ Input Pulse Width		20		(TVCO)-20	ns
TFRD, $\overline{RDT}$ Input Fall Time				15	ns
TWVCO, VCO Output Pulse Width (Includes Effects of Window Shift)		.26TVCO -10		.74TVCO +10	ns

WINDOW SYMMETRY CONTROL CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
TWSS $\overline{WS0}$, $\overline{WS1}$, WSD Set Up Time		50			ns
TWSH $\overline{WS0}$, $\overline{WS1}$, WSD Hold Time		0			ns

DATA SYNCHRONIZATION

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TVCO	VCO Center Frequency Period	VCO IN = 2.7V TO = 83.8 (RR + 1.78), RR = 3k to 9k VPA2 = 5.0V	0.8TO		1.2TO	ns
	VCO Frequency Dynamic Range	1.0V ≤ VCO IN ≤ VPA2-0.6V VPA2 = 5.0V	±22		±45	%
KVCO	VCO Control Gain	$\omega o = 2\pi / TO$ 1.0V ≤ VCO IN ≤ VPA2-0.6V	0.16 ωo		0.25 ωo	rad/s V
KD	Phase Detector Gain	KD = 0.538 / (RR+500) VPA2 = 5.0V	0.83 KD		1.17 KD	A/rad

DATA SYNCHRONIZATION (Continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
*	KVCO x KD Product Accuracy		-28		+28	%
*	VCO Phase Restart Error			12		ns
	Decode Window Centering Accuracy		-.02 TVCO		.02 TVCO	ns
	Decode Window		0.9 TVCO			ns
TS1	Decode Window Time Shift	TWS1 = .05 TVCO $\overline{WSO}$ = 0; $\overline{WSI}$ = 1		TWS1		ns
TS2	Decode Window Time Shift	TWS2 = .15 TVCO $\overline{WSO}$ = 1; $\overline{WSI}$ = 0		TWS2		ns
TS3	Decode Window Time Shift	TWS3 = .2 TVCO $\overline{WSO}$ = 0; $\overline{WSI}$ = 0		TWS3		ns
TSA	Decode Window Time Shift	$TWSA = 0.29\,TVCO\left(1-\frac{3260+R}{5950+R}\right)$ $\overline{WSO}$ = 1; $\overline{WSI}$ = 1		TWSA		ns

* Not directly testable; design characteristics

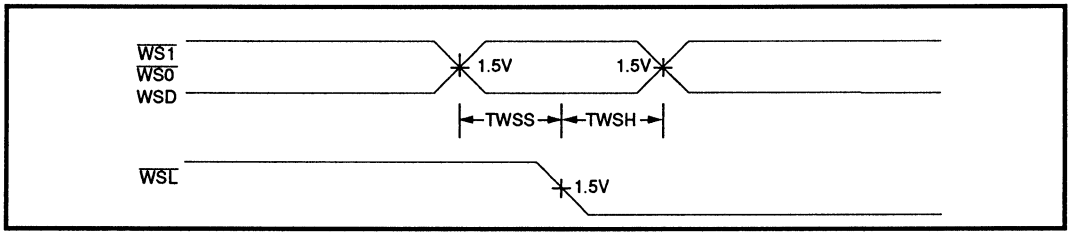


FIGURE 9: Window Symmetry Control Timing

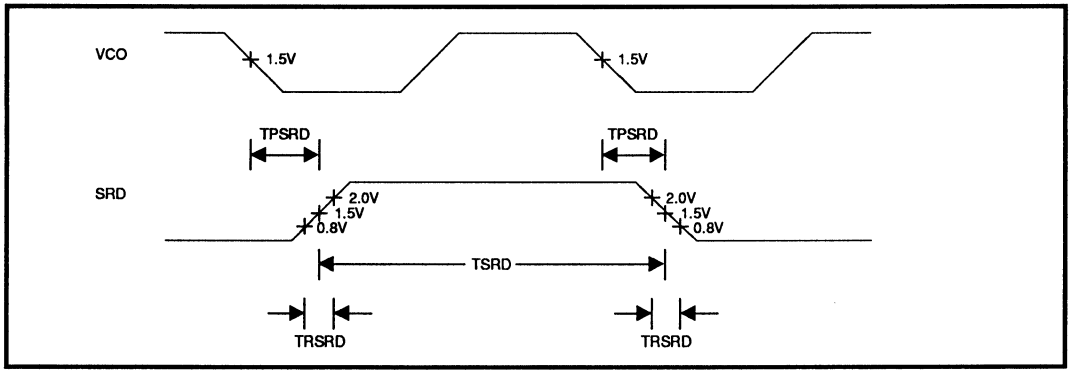


FIGURE 10: Read Mode Timing

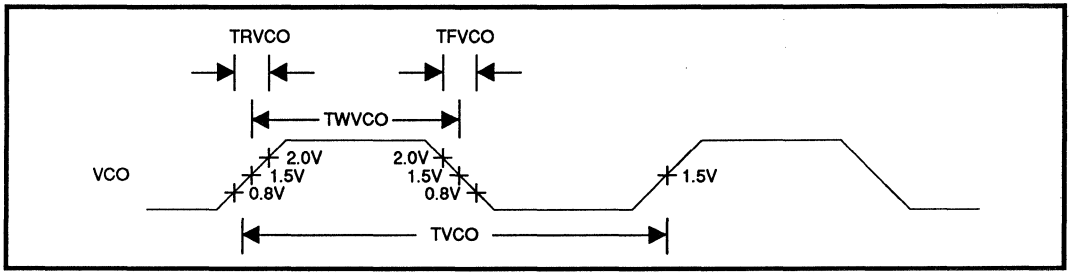


FIGURE 11: VCO Timing

APPLICATIONS INFORMATION

The SSI 34P553/5531 PLL uses a new architecture which incorporates an accurate quarter cell delay circuit. The standard architecture of a data synchronizer PLL is shown in Figure14A. In read mode, the rising edge of the quarter cell delay enables the phase detector, and the falling edge is locked to the VCO. Ideally, the quarter cell delay enables the phase detector one half of an encoded bit cell time before the phase comparison takes place. A data bit could then shift early or late by one half of an encoded bit cell time before a phase detector output error would occur. If the quarter cell delay is not exactly one half of an encoded bit cell time, a phase detector error will occur when the read data shifts by an amount that is smaller than one half of an encoded bit cell time when shifting in one direction and an amount larger than one half of an encoded bit cell time in the other direction. In addition, when an error occurs, the resulting charge pump output goes from maximum output one way to maximum output the other way. This can cause loss of lock to occur. The timing is shown in Figure 15.

The SSI 34P553/5531 achieves an accurate quarter cell delay time by using the VCO control voltage to compensate the quarter cell delay one-shot circuit for process, temperature and power supply induced timing variations. The modified architecture of the SSI 34P553/5531 data synchronizer is shown in Figure 16B. Because the quarter cell delay timing is adjusted by the VCO control voltage, there is an effect on the PLL transfer function due to the new quarter cell delay circuit.

The quarter cell delay circuit produces a time delay output in response to a voltage input. In order to include this function in a phase-locked loop, the time delay function must be converted into a phase function. This is straightforward, since a time delay is equivalent to a phase angle. The equivalent phase representation of the quarter cell delay is derived below.

For the VCO: $$K_o = \frac{d\omega_o}{dV} \quad (1a)$$

$$\frac{dT_o}{dV} = \frac{d}{dV}\left(\frac{1}{f_o}\right) = -\frac{1}{f_o^2}\frac{df_o}{dV} = -T_o^2\frac{df_o}{dV} = -\frac{T_o^2}{2\pi}\frac{dw_o}{dV} \quad (1b)$$

where:

K_0 = VCO gain
ω_0 = VCO center frequency (rad/s)
f_0 = VCO center frequency (Hz)
T_0 = VCO center frequency (sec)

For the quarter cell delay,

$$K_T = \frac{dq_o}{dV} = \frac{2\pi}{T_o}a\frac{dT_0}{dV} = -\alpha T_o\frac{dw_o}{dV} = -\alpha T_o K_o$$

where:

θ_0 = Phase due to quarter cell delay circuit
T_0 = VCO center frequency period
T_Q = Quarter cell delay time
$\alpha = T_Q/T_0 = 0.5$ for the 32P548

The gain of the quarter cell delay block is constant in the SSI 34P553/5531, regardless of the values of other components.

For the SSI 34P553/5531, the nominal value of K_T is 0.17π.

PLL TRANSFER FUNCTION

There are two modes of operation of the PLL, and two transfer functions. In write and idle modes, the PLL is locked to the reference oscillator, and the quarter cell delay does not enter into the transfer function. In read, mode, the PLL is locked to read data, and the quarter cell delay is included in the transfer function. In addition, the effective loop gain of the PLL increases in idle mode due to the phase detector. This will be explained later in more detail.

The transfer functions for read and idle modes are given in (3) and (4), respectively.

$$\frac{\theta_o(s)}{\theta_r(s)} = \frac{\frac{nK_oK_dF(s)}{S}}{1+nK_TK_dF(s)+\frac{nK_oK_dF(s)}{S}} \quad (3)$$

$$\frac{\theta_o(s)}{\theta_r(s)} = \frac{\frac{nK_oK_dF(s)}{S}}{1+\frac{nK_oK_dF(s)}{S}} \quad (4)$$

where:

K_T = Quarter cell delay one-shot gain
K_O = VCO gain
K_d = Phase detector gain
$F(s)$ = Loop filter transfer function
n = Ratio of input freq. to reference freq.

In (3) the K term in the denominator is a result of the quarter cell delay. Substituting $K_T = \alpha K_O T_O$ into (3),

$$\frac{\theta_o(s)}{\theta_r(s)} = \frac{\frac{nK_oK_dF(s)}{S}}{1+(1-s\alpha T_o)\frac{nK_oK_dF(s)}{S}}$$

The additional $-s\alpha T_O$ term in the denominator due to the quarter cell delay introduces positive feedback. However, the gain of the positive feedback is always less than one, so there is no instability. The additional term is not always negligible, and must be taken into account in the loop analysis and design.

Two loop filter configurations, shown in Figure 12, will be considered. Both filters result in a second order type 2 loop transfer function, with only minor differences in the loop equation.

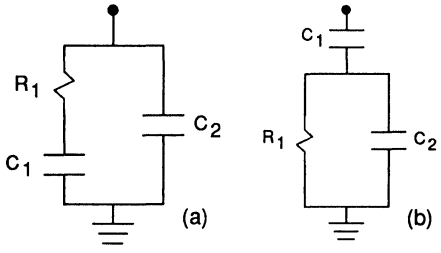


FIGURE 12: Loop Filter

The transfer function of the loop filter for a charge-pump PLL is the transimpedance, V_o/I_i (s), where V_o (s) is the output voltage, and I_i (s) is the input current. The transfer functions of (a) and (b) are given by:

$$F_a(s) = \frac{sR_1C_1+1}{s(C_1+C_2)\left(sR_1\frac{C_1C_2}{C_1+C_2}+1\right)} \quad (6)$$

$$F_b(s) = \frac{sR_1(C_1+C_2)+1}{sC\left(sR_1C_2+1\right)} \quad (7)$$

For loop filter (a), C_2 is normally chosen to be much smaller than C_1 so that it does not affect the loop transfer function significantly. Assuming that $C_1 \gg C_2$ and $sR_1C_1 \ll 1$ at the frequencies of interest, (6) reduces to:

$$F_a(s) = \frac{sR_1C_1+1}{sC_1} \quad (8)$$

For loop filter (b), C_2 is normallly chosen to be much smaller than C_1 so that it does not affect the loop transfer function significantly. Assuming that $C_1 \gg C_2$ and that $sR_1C_2 \ll 1$ at the frequencies of interest, (7) reduces to:

$$F_b(s) = \frac{sR_1C_1+1}{sC_1} \quad (9)$$

Equations (8) and (9) are the same, and either loop filter may be used. Substituting (8) into (3) gives:

$$\frac{\theta_o(s)}{\theta_r(s)} = \frac{\frac{nK_oK_d}{C_1(1-\alpha T_onK_oK_dR_1)}(sR_1C_1+1)}{s^2+s\frac{nK_oK_d}{1-\alpha T_onK_oK_dR_1}\left(R_1-\frac{\alpha T_o}{C_1}\right)+\frac{nK_oK_d}{C_1(1-\alpha T_onK_oK_dR_1)}} \quad (10)$$

This is in the form of a standard second order transfer fucntion. The denominator has the form:

$$D(s) = s^2 + 2\zeta\omega_n s + \omega_n^2 \quad (11)$$

where: ζ = damping factor
ω_n = natural frequency

The damping factor and natural frequency of (10) can be extracted:

$$\omega_n = \sqrt{\frac{nK_oK_d}{C_1(1-\alpha T_o nK_oK_dR_1)}} \quad (12)$$

$$\zeta = \frac{R_1 - \frac{\alpha T_o}{C_1}}{2}\sqrt{\frac{nK_oK_dC_1}{1-\alpha T_o nK_oK_dR_1}} \quad (13)$$

Substituting (8) into (4) gives the transfer function for idle mode:

$$\frac{\theta_o(s)}{\theta_r(s)} = \frac{\frac{nK_oK_d}{C_1}(sR_1C_1+1)}{s^2 + s(nK_oK_dR_1) + \frac{nK_oK_d}{C_1}} \quad (14)$$

Again, this is in the form of a second order transfer function. The damping factor and natural frequency are found to be:

$$\omega_n = \sqrt{\frac{nK_oK_d}{C_1}} \quad (15)$$

$$\zeta = \frac{R_1}{2}\sqrt{nK_oK_dC_1} \quad (16)$$

To design the loop for proper read mode operation using (12) and (13), R, and C, must be found in terms of the damping factor and natural frequency.

To do this, first find ζ/ω_n, then solve for R_1C_1.

$$R_1C_1 = \frac{2\zeta}{\omega_n} + \alpha T_o \quad (17)$$

Substitute this value for R_1C_1 into the equation for ω_n and solve for C_1.

$$C_1 = \frac{nK_oK_d}{\omega_n^2} + \alpha T_o nK_oK_d\left(\frac{2\zeta}{\omega_n} + \alpha T_o\right) \quad (18)$$

Now that C_1 is known, R_1 can be found by dividing (17) through by C_1.

$$R_1 = \left(\frac{2\zeta}{\omega_n} + \alpha T_o\right)\frac{1}{C_1} \quad (19)$$

EXAMPLE 1

Assume that the data rate is 0.6 Mbit/s, $\zeta = 0.7$, a length of 20 2T patterns for the loop to lock is used, and $\omega_n t = 5.7$ for error < 1%.

n = 0.5 due to the 2T pattern.

$$T_0 = \frac{1}{f_0} = \frac{1}{1.2\cdot10^6} = 833\text{ns}$$

$\omega_0 = 2\pi f_0 = 2\pi (1.2 \cdot 10^6) = 7.54 \cdot 10^6$ rad/s

$\alpha_0 = 0.5$

For the SSI 34P553: $RR = \frac{5.97}{DR} - 1.79(\text{k}\Omega) = 8.17\text{k}\Omega$

where DR = Data Rate in Mbit/s

$$K_0 = 0.17\omega_0 = 1.28\cdot10^6 \frac{\text{rad/sec}}{\text{Volt}}$$

$$K_d = \frac{0.62}{RR+500} = 71.51\cdot10^{-6}\text{ A/rad}$$

$K_T = 0.17\pi = 0.534$

Assuming a length of 20 2T patterns, then:
t = (20) (2) (833) ns = 33.3 µs

$$\omega n = \frac{5.7}{33.3\mu s} = 1.71\cdot10^5\text{ rad/s}$$

C_1 = 1565 pF + 165.6 pF = 1.73 nF

R_1 = 5.02 kΩ

The resulting loop filter is shown in Figure 13.

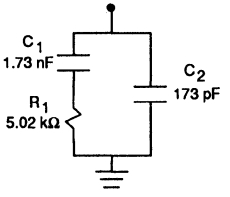


FIGURE 13

The value of $C_2 = C_1/10$ is chosen to damp out transients on the FILT pin and meet the requirement $C_2 \ll C_1$.

When the loop locks to the reference oscillator in idle mode, the loop transfer function is given by (14), and ω_n and ζ are given by (15) and (16). R_1 and C_1 from Example 1 can be substituted into these equations to find the resulting natural frequency and damping factor in idle mode.

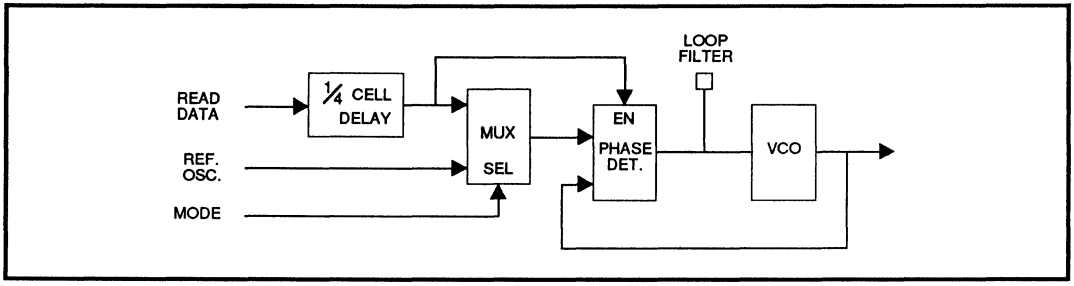


FIGURE 14A: Standard Configuration of a Data Synchronizer Phase-Locked Loop

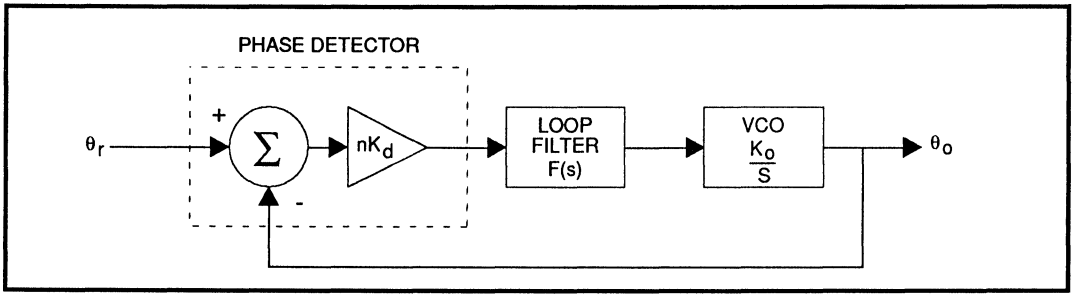


FIGURE 14B: Phase-Lock Loop System Representation

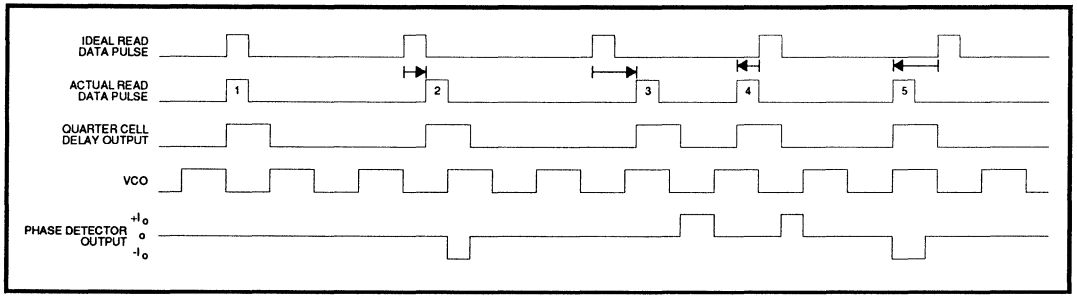


FIGURE 15A: Phase Detector Timing with Ideal Quarter Cell Delay. For an ideal pulse (1), there is no phase detector output. When a pulse is shifted late (2) or early (4) by less than the quarter cell delay time, the phase detector output is negative or positive, respectively. When the read data is shifted late (3) or early (5) by more than the quarter cell delay time, a phase detector output polarity error occurs. In this case, the output polarity becomes positive for a late shifted pulse and negative for an early shifted pulse.

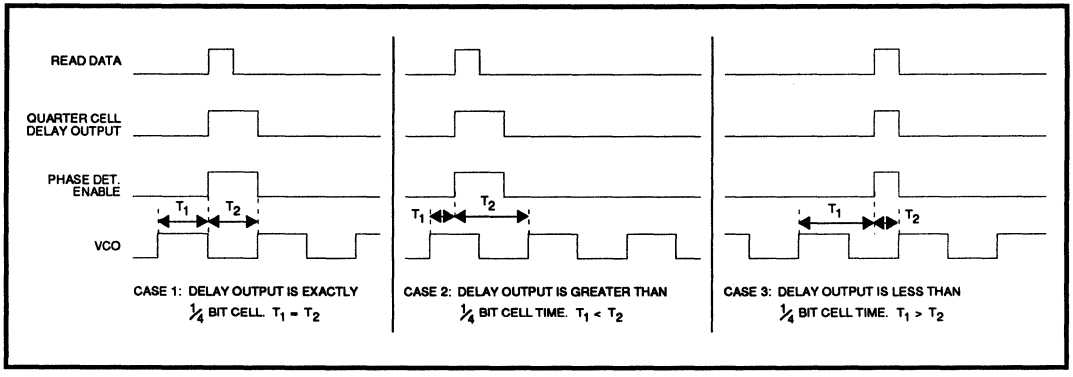


FIGURE 15B: Timing of Phase Detector Enable Logic. The read data input pulse can shift to the left by T1 and to the right by T2 before an error occurs in the phase detector output polarity, If the quarter cell delay output is not exactly 1/4 bit cell wide, then T1 ≠ T2, as shown in cases 2 and 3.

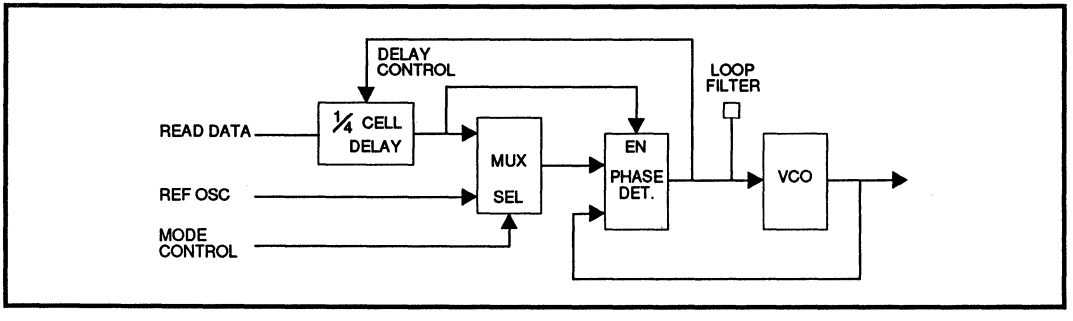


FIGURE 16A: Modified Data Synchronizer Phase-Locked-Loop with Quarter Cell Delay Control

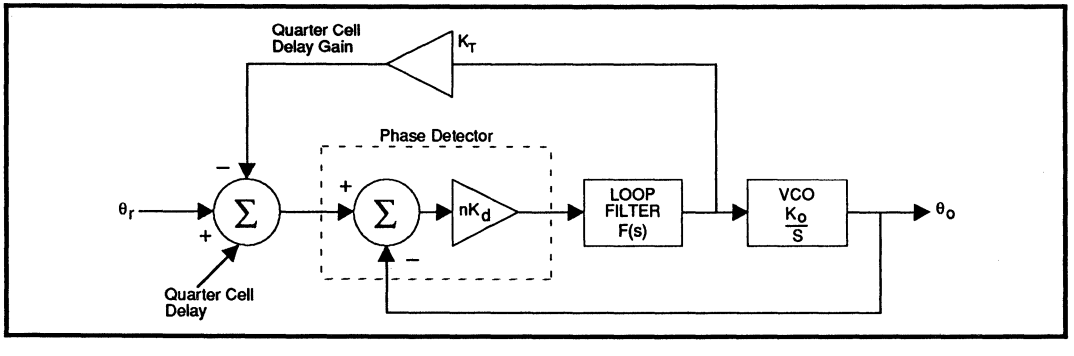
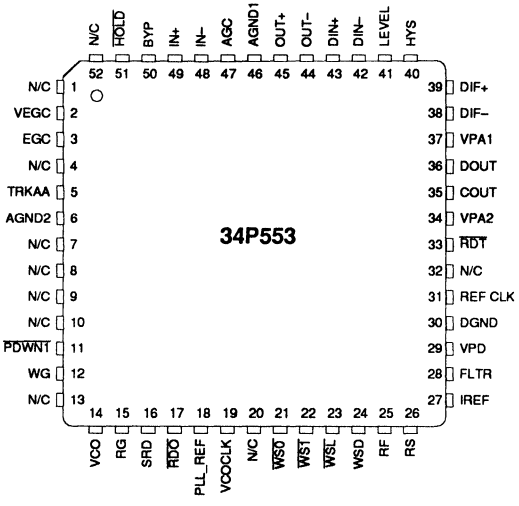


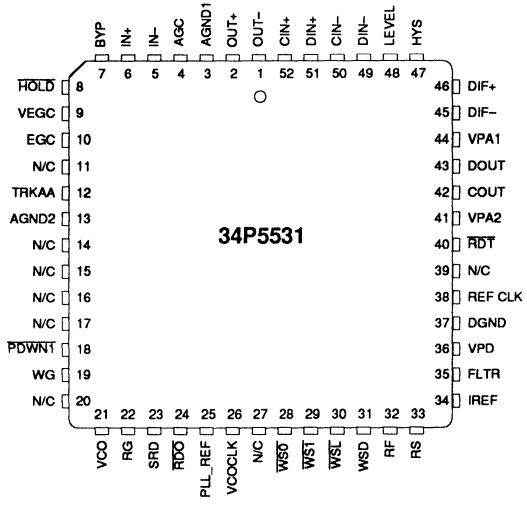
FIGURE 16B: Modified Data Synchronizer System Representation

PACKAGE PIN DESIGNATIONS

(Top View)



52-Pin QFP



52-Pin QFP

ORDERING INFORMATION

PART DESCRIPTION	ORDERING NUMBER	PACKAGE MARK
SSI 32P553 Pulse Detector & Data Synchronizer		
52-Pin QFP	32P553-CG	32P553-CG
SSI 32P5531 Pulse Detector & Data Synchronizer		
52-Pin QFP	32P5531-CG	32P5531-CG

9

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 731-7110, FAX (714) 573-6914

Notes:

silicon systems®
A TDK Group Company

SSI 34R575
2 or 4-Channel Floppy Disk Read/Write Device

November 1991

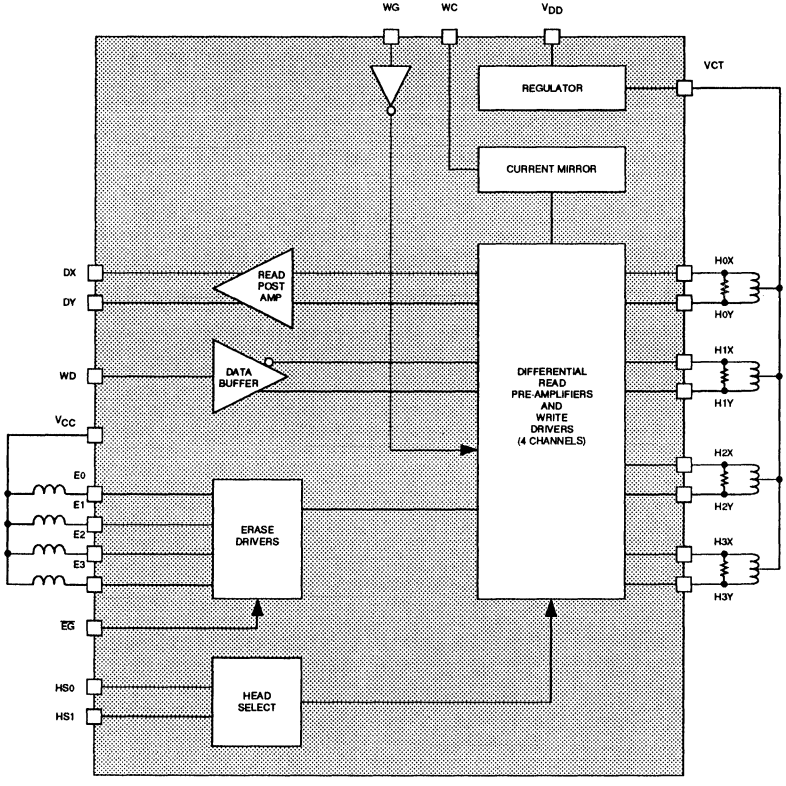
DESCRIPTION

The SSI 34R575 device is a bipolar monolithic integrated circuit used in floppy disk systems for head control and write, erase, and read select functions. The device has either two or four discrete read, write, and erase channels. Channel select inputs are TTL compatible. The SSI 34R575 device requires +5 V and +12 V power supplies and is available in 18-pin (2-channel version) or 24-pin (4-channel version) dual inline packages.

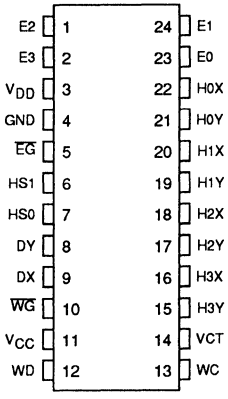
FEATURES

- **Operates on +5 V, +12 V power supplies**
- **Two or four channel capability**
- **TTL compatible control inputs**
- **Read/Write functions on one-chip**
- **Internal center tap voltage source**
- **Supports all disk sizes**
- **Applicable to tape systems**

BLOCK DIAGRAM



PIN DIAGRAM



9

CAUTION: Use handling procedures necessary for a static sensitive component.

SSI 34R575
2 or 4-Channel Floppy Disk Read/Write Device

FUNCTIONAL DESCRIPTION

The SSI 34R575 functions as a write and erase driver or as a read amplifier for the selected head. Two TTL compatible inputs are decoded to select the desired read/write and erase heads. Head select logic is indicated in Table 1. Both the erase gate ($\overline{EG}$) and write gate ($\overline{WG}$) lines have internal pull up resistors to prevent an accidental write or erase condition.

MODE SELECTION

The read or write mode is determined by the write gate ($\overline{WG}$) line. The input is open collector TTL compatible. With the input low, the circuit is in the write mode. With the input high (open), the circuit is in the read mode. In the read mode, or with the +5 V supply off, the circuit will not pass write current.

ERASE

The erase operation is controlled by an open collector TTL compatible input. With erase gate ($\overline{EG}$) input high (open) or the +5 V supply off, the circuit will not pass erase current. With $\overline{EG}$ low, the selected open collector erase output will be low and current will be pulled through the erase heads.

READ MODE

With the $\overline{WG}$ line high, the read mode is enabled. In the read mode the circuit functions as a differential amplifier. The state of the head select input determines which amplifier is active. When the mode or head is switched, the read output will have a voltage level shift. External reactive elements must be allowed to recover before proper reading can commence. A current diverting circuit prevents any possible write current from appearing on a head line.

WRITE MODE

With the $\overline{WG}$ line low, externally generated write current is mirrored to the selected head and is switched between head windings by the state of the write data (WD) signal.

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
V_{CC}		+5 V
V_{DD}		+12 V
H0X-H3X H0Y-H3X		X, Y head connections
DX, DY		X, Y Read Data: Differential read signal out
WG		Write gate: sets write mode of operation
WC		Write current: current mirror used to drive floppy disk heads
WD		Write data line
EG		Erase gate: allows erasure by selected head
E0-E3		Erase head driver connections
HS0-HS1		Head select inputs
GND		Ground
VCT		Center Tap Voltage Source

TABLE 1: HEAD SELECT LOGIC

4 - CHANNELS		
HS1	**HS0**	**HEAD**
0	0	0
0	1	1
1	0	2
1	1	3

2 - CHANNELS	
HS1	**HEAD**
0	0
1	1

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

(Operating above absolute maximum ratings may damage the device.)

PARAMETER		RATING	UNIT
DC Supply Voltage:	Vcc	6.0	V
	Vdd	14.0	V
Write Current		10	mA
Head Port Voltage		18.0	V
Digital Input Voltages:	DX, DY, HS0, HS1, WD	-0.3 to + 10	V
	$\overline{EG}$, $\overline{WG}$	-0.3 to V_{cc} + 0.3	V
DX, DY Output Current		-5	mA
VCT Output Current		-10	mA
Storage Temperature Range		-65 to + 150	°C
Junction Temperature		125	°C
Lead Temperature (Soldering, 10 sec.)		260	°C

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RECOMMENDED OPERATING CONDITIONS (0°C<Ta<50°C, 4.7 V<Vcc<5.3 V, 11 V<V_{DD}<13 V)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Vcc Supply Current					
Read mode	Vcc MAX			15	mA
Write mode	Vcc MAX			35	mA
V_{DD} Supply Current					
Read mode	V_{DD} MAX			25	mA
Write mode	V_{DD} MAX			15	mA
Write Current			5.5		mA

ERASE OUTPUT

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Erase On Voltage	IE = 80 mA	0.7		1.3	VDC
Erase Off Leakage				100	µA

LOGIC SIGNALS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Head Select (HS0, HS1) and Write Data (WD)					
Low Level Voltage		-0.3		0.8	VDC
High Level Voltage		2.0		6.0	VDC
Low Level Current	V_{IN} = 0 volts	-1.6			mA
High Level Current	V_{IN} = 2.7 volts			40	µA
$\overline{\text{WRITE GATE}}$ ($\overline{\text{WG}}$) and $\overline{\text{ERASE GATE}}$ ($\overline{\text{EG}}$)					
Low Level Voltage		-0.3		0.81	VDC
High Level Input Current		-300			µA
Low Level Current	V_{IN} = 0 volts	-2.0			mA

READ MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Differential Gain	f = 100 kHz, Vin = 5 mV Rms R_L = 10 kΩ	80	100	120	V/V
Bandwidth	Vin = 5 mVRms RL = 10 K CL = 15pF	9			MHz
Input Voltage Range for 95% Linearity	f = 100 kHz, RL = 10 K	25			mVpp
Differential Input Resistance	f = 1 MHz	100			kΩ
Differential Input Capacitance	f = 1 MHz			10	pF
Input Bias Current				25	μA
Input Offset Voltage				12	mV
Output Voltage, Common Mode			8		VDC
Output Resistance				35	Ω
Output Current Sink		2			mA
Output Current Source		3			mA
Common Mode Rejection Ratio	f = 1 MHz (input referred)	50			dB
Power Supply Rejection Ratio	f = 1 MHz (input referred)	50			dB
Channel Separation	f = 1 MHz (input referred)	50			dB
Input Noise	BW = 100 Hz to 1 MHz, Z Source = 0		7		μV RMS

WRITE MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Write Current Gain	IW = 5.5 mA	.97		1.05	A/A
Write Current Voltage Level	IW = 5.5 mA	1.2		2.1	VDC
Differential Head Voltage	IW = 5.5 mA	12.5			VDC
Unselected Head Current	IW = 5.5 mA DC Condition			0.1	mA
Write Current Unbalance	IW = 5.5 mA			1	%
Write Current Time Symmetry	IW = 5.5 mA			±10	ns
Read Amplifier Output Level			10.5		VDC
Center Tap Voltage	(Read and Write Modes)		8.5		VDC

SWITCHING CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Write and Erase Gate Switching Delay	Delay to 90% of Write Current			1	µsec
Head Select Switching Delay				1	µsec
Head Current Switching Delay	T1 in Fig. 1		10		nsec
Head Current Switching Time	IW = 5.5 mA Shorted Head		10	30	nsec
Write to Read Recovery Time				2	µsec

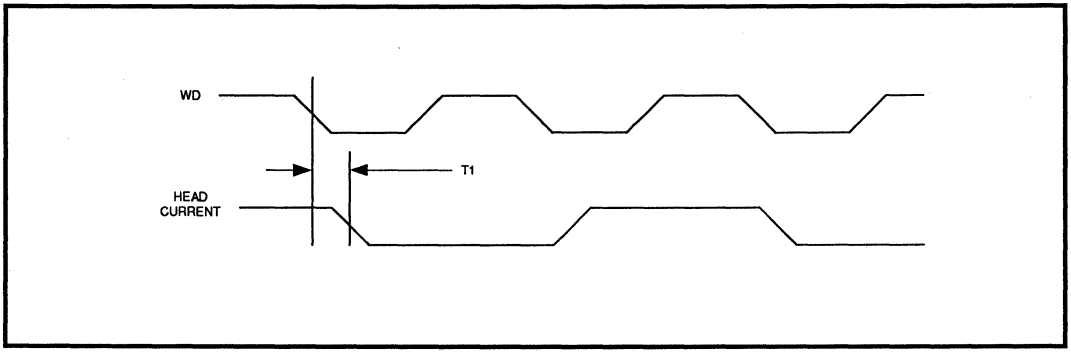
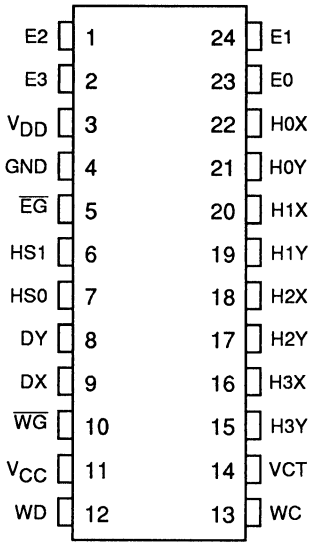


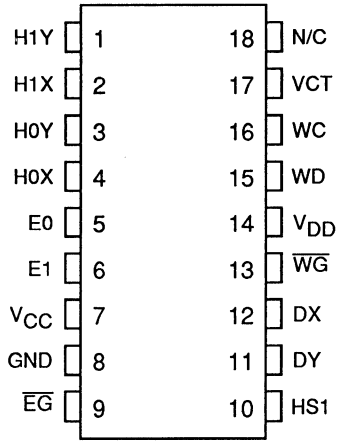
FIGURE 1: Head Current Switching Delay

PACKAGE PIN DESIGNATIONS

(TOP VIEW)



24-Pin DIP



18-Pin DIP

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 34R575 24-Pin DIP	34R575-4CP	34R575-4CP
SSI 34R575 18-Pin DIP	34R575-2CP	34R575-2CP

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Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714) 731-7110, FAX: (714) 573-6914

Notes:

SSI 34B580
Port Expander
Floppy Disk Drive

July 1990

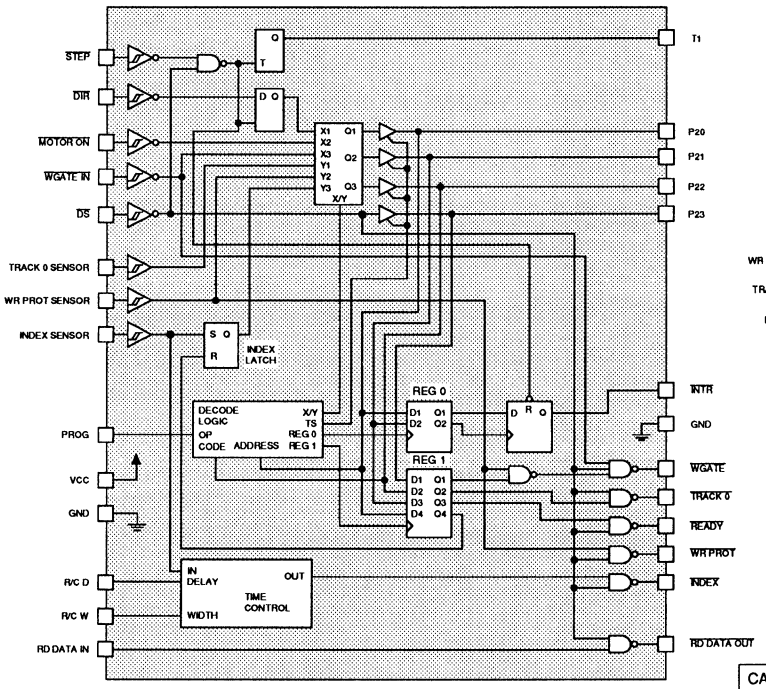
DESCRIPTION

The SSI 34B580 device is a bipolar integrated circuit that serves as an input/output port expander for an 8084 type microprocessor based floppy disk drive system. The device consolidates functions normally performed by a variety of LSTTL, SSI, AND MSI devices. The combination of an SSI 34P570 (read, write, and erase device), an 8048 type microprocessor, and the SSI 34B580 provides the majority of electronics required for a SA400 type floppy disk drive system, including host interface bus driver and receiver. In addition to its port expansion function, the SSI 34B580 processes system data and provides both pulse width and delay control (adjustable by external elements) for the INDEX SENSOR input. The device requires a single +5 V power supply and is available in a 28-pin package.

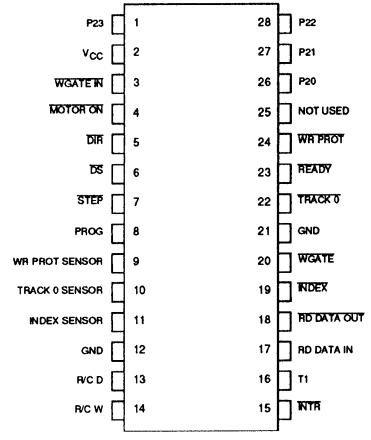
FEATURES

- **Reduces package count in flexible disk drive systems**
- **Replaces bus interface and combinational logic devices between the SSI 34P570, on board microprocessor and mechanical interfaces**
- **Surface mount available for further real estate reduction**
- **Provides drive capability for mechanical and system interfaces**

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

9

FUNCTIONAL DESCRIPTION

PORTS

The SSI 34B580 has two 4-bit input ports, Port A and Port B. Port A receives data from the host interface bus for conveyance to the drive's read/write circuitry and to the microprocessor. Three sensors report the status of the drive to the 34B580 via Port B. Common to both ports is a drive select ($\overline{DS}$) signal from the host interface bus. This allows the host to address separate disk drives. There is also a 4-bit bidirectional port on the SSI 34B580. This is port 2 and it can be used by the microprocessor to write to or read from the SSI 34B580.

READ MODE

Ports A and B can be read by a microprocessor via Port 2. This allows the microprocessor to obtain data from the host interface bus and the status sensors. The PROG signal from the microprocessor provides the timing for the operation. First an OP code and a port address must be placed on Port 2 (see Table 1), then latched in on the falling edge of PROG. When the OP code and addresses have been decoded, the desired input port is selected and output on Port 2. The operation is terminated by the rising edge PROG, which returns Port 2 to the input mode.

WRITE MODE

In the write mode the microprocessor passes system parameters to the SSI 34B580 for logic processing and outputting. Table 2 shows how each bit of Port 2 affects the SSI 34B580. A logic one on the zero bit of Port 2 will reset the index latch. P21, qualified by the $\overline{DS}$ signal, sends a "this drive ready" signal from the microprocessor the the host interface bus. Similarly P22 is $\overline{DS}$ qualified and sent to the host as a signal that the head is positioned over track 0. P23 is used in the logic that sends a R/$\overline{W}$ signal to the drive's read/write circuitry. The write mode occurs when the proper OP code and address is placed on Port 2 and latched in on the falling edge of PROG (see Table 2). The microprocessor writes in the data on PROG's rising edge.

INDEX PULSE

An optical sensor connected to the INDEX SENSOR pin detects the diskette's index marker. The state of the index sensor is latched into the SSI 34B580 and is available to be read by the microprocessor on P22. The latch may be reset by writing a one to P20 from the microprocessor. The pulse received from the sensor also drives the host interface signal $\overline{INDEX}$, the width and delay of which can be controlled by external R/C circuits. The time constant attached to the R/C D pin determines the delay from the INDEX SENSOR input to the $\overline{INDEX}$ signal on the host interface bus. The equation for the delay is Td = 0.59Rd x Cd (seconds). The width of the $\overline{INDEX}$ signal is determined by the circuit attached to the R/C W pin and the equation Tw = 0.59Rw x Cw (seconds).

INTERRUPT

The $\overline{INTR}$ signal is asserted every time a step command is issued to the drive on the host interface bus. Thus when $\overline{INTR}$ is tied to the interrupt pin of 8048 type microprocessor, an interrupt service routine will be executed on each step command. This routine typically obtains information on the direction the heads should move and the status of the track 0 sensor to use for generating the stepper motor control signals. The interrupt signal is cleared (set high) by first placing the the proper OP code and address on Port 2 (seeTable 2). This is latched in on the falling edge of PROG, then on its rising edge logic ones on P20 and P21 will be latched in to set $\overline{INTR}$ back to a high state. Note that an indeterminate operation will result from holding the INDEX SENSOR latch reset (holding P20 high).

T1 PIN

This signal changes state with the $\overline{STEP}$ command of the host interface bus when the drive is selected. It drives the T1 pin on an 8048 type microprocessor which is an input to a counter. The 8048 can use this count and the DIR signal read from Port 2 of the SSI 34B580 to monitor the head position and issue a CB (current boost) command to the SSI 34P570 when a specific track is reached.

INPUT TO PORT2		READ FROM PORT 2				4-BIT
OP Code P22	Addr. P20	P23	P22	P21	P20	Input Port
0	0	$\overline{DS}$	Index Sensor Latch	WR Sensor	Track 0 Sensor	B
0	1	$\overline{DS}$	$\overline{WGATEIN}$	$\overline{MOTORON}$	$\overline{DIR}$	A

TABLE 1: Read Mode

INPUT TO PORT2		DATA PROCESSED FROM PORT 2				
OP Code P22	Addr. P20	$\overline{WGATE}$	$\overline{TRACK0}$	$\overline{READY}$	$\overline{INTR}$	Index Latch Reset
1	0	Z	$(\overline{P22 \cdot DS})$	$(\overline{P21 \cdot DS})$		P20
1	1				See Text	
Where Z = (P23 • WR PROT SENSOR) + $(\overline{DS \cdot WGATEIN})$						

TABLE 2: Write Mode

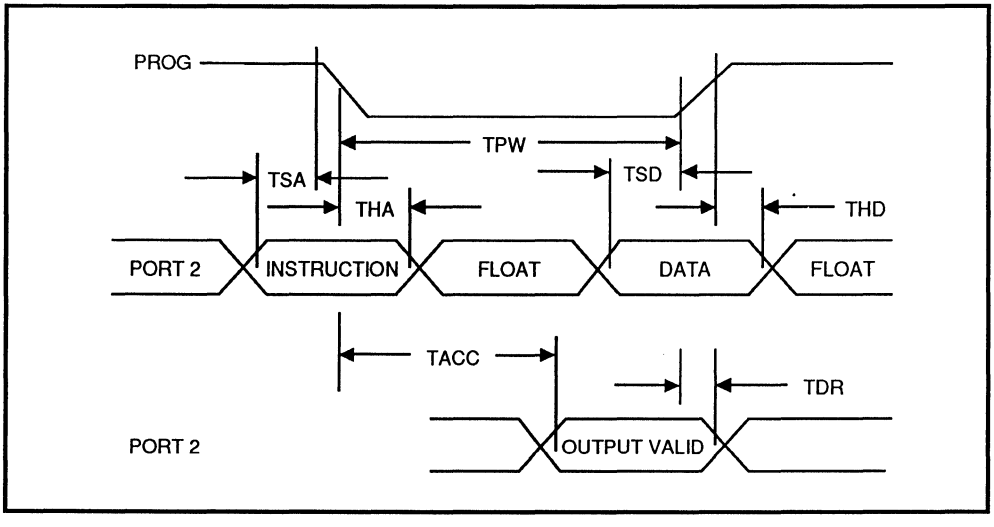


FIGURE 1: Timing Diagram

PIN DESCRIPTIONS

NAME	TYPE	DESCRIPTION
P20 - P23	I/O	4-bit bidirectional port, referred to as Port 2.
$\overline{\text{WGATE IN}}$	I	This input command to write is asserted by the host interface bus.
$\overline{\text{MOTOR ON}}$	I	This input command to turn on the spindle motor comes from the host interface bus.
$\overline{\text{DIR}}$	I	Input from the host interface bus selecting the direction in which the stepper motor should move the head.
$\overline{\text{DS}}$	I	Drive Select
INDEX SENSOR	I	Input from the photodiode that indicates the index marker in the diskette.
WR PROT SENSOR	I	Input from the photodiode that indicates if the diskette is write protected.
TRACK 0 SENSOR	I	Input from the photodiode that detects when the head is positioned over track 0.
$\overline{\text{STEP}}$	I	Input from the host interface bus indicating that the head should be moved.
T1	O	This pin changes state when a $\overline{\text{STEP}}$ command is received from the host interface bus.
RD DATA IN and $\overline{\text{RD DATA OUT}}$	I/O	Read data path
$\overline{\text{WGATE}}$	O	Output to the disk drive's read/write circuitry.
$\overline{\text{INDEX}}$	O	Output to the host interface bus indicating index sensor status.
$\overline{\text{TRACK 0}}$	O	Output to the host interface bus indicating track 0 sensor status.
$\overline{\text{READY}}$	O	Output to the host interface bus indicating track 0 sensor status.
$\overline{\text{WR PROT}}$	O	Output to the host interface bus indicating write protect sensor status.
PROG	I	Input from the 8048 microprocessor for I/O control of the SSI 34B580.
$\overline{\text{INTR}}$	O	Output to the interrupt pin of the 8048 microprocessor.
R/C D and R/C W		The external resistor and capacitor networks tied to these pins determine the delay and width of the output pulse to the $\overline{\text{INDEX}}$ pin.
Vcc		+5 V supply
GND		Ground

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (All voltages referred to GND)
Operation above absolute maximum ratings may permanently damage the device.

PARAMETER	RATING	UNIT
DC Supply	+ 7	VDC
Voltage Range (any pin to GND)	-0.4 to + 7	VDC
Power Dissipation	700	mW
Storage Temperature	-40 to + 125	°C
Lead Temperature (10 sec soldering)	260	°C

ELECTRICAL CHARACTERISTICS
(Unless otherwise specified, 4.75 ≤ Vcc ≤ 5.25 VDC; 0°C < Ta < 70°C)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Totem pole outputs (P20 - P23, $\overline{\text{INTR}}$, T1)					
Output High Voltage	IOH = -400 A	2.5			V
Output Low Voltage	IOL = 2 mA			0.5	V
Open collector outputs ($\overline{\text{RD DATA OUT}}$, $\overline{\text{INDEX}}$, $\overline{\text{WGATE}}$, $\overline{\text{TRACK0}}$,$\overline{\text{READY}}$, $\overline{\text{WR PROT}}$)					
Output High Current	VOH = 5.25 V			250	µA
Output Low Voltage	IOL = 48 mA			0.5 V	V
Inputs (P20 - P23, PROG, RD DATA IN)					
Input High Voltage		2.0			V
Input Low Voltage				0.8	V
Input Low Current	VIL = 0.5 V			-0.8	mA
Input High Current	VIH = 2.4 V			40	µA
Input Current	Vin = 7.0 V			0.1	mA
Schmitt - Trigger Inputs ($\overline{\text{WGATE IN}}$, $\overline{\text{MOTOR ON}}$, $\overline{\text{DIR}}$, $\overline{\text{DS}}$, $\overline{\text{STEP}}$)					
Threshold Voltage	Positive Going, Vcc = 5.0 V	1.3		2.0	V
	Negative Going, Vcc = 5.0 V	0.6		1.1	V
Hysteresis	Vcc = 5.0 V	0.4			V
Input High Current	VIH = 2.4 V			40	µA
Input Low Current	VIL = 0.5 V			-0.4	mA
Input Current	VIN = 7.0 V			0.1	mA

High Impedance Inputs with Hysteresis (WR PROT SENSOR, TRACK 0 SENSOR, INDEX SENSOR)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Input High Voltage				2.0	V
Input Low Voltage		0.8			V
Hysteresis		0.2			V
Input Current	Vin = 0 to Vcc			-0.25	mA

TIMING CHARACTERISTICS (Unless otherwise specified; Ta = 25°C; 4.75V ≤ Vcc≤ 5.25V; CL = 15 pf.)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Propagation Delay Time	RD DATA IN to $\overline{\text{RD DATA OUT}}$			35	ns
	$\overline{\text{DS}}$ to $\overline{\text{WGATE}}$, $\overline{\text{TRACK 0}}$ $\overline{\text{READY}}$ $\overline{\text{WR PROT}}$,$\overline{\text{RD DATA}}$, $\overline{\text{INDEX}}$			80	ns
	PROG to $\overline{\text{INTR}}$, $\overline{\text{WGATE}}$, $\overline{\text{TRACK 0}}$ (Rising edge) $\overline{\text{READY}}$, $\overline{\text{WR PROT}}$			100	ns
	$\overline{\text{WR PROT}}$ to $\overline{\text{WGATE}}$, $\overline{\text{WR PROT SENSOR}}$			250	ns
	$\overline{\text{WGATE}}$ IN to $\overline{\text{WGATE}}$			80	ns
	$\overline{\text{STEP}}$ to T1, P20			80	ns
	TRACK 0 SENSOR WR PROT SENSOR to Port 2 INDEX SENSOR			250	ns
	$\overline{\text{MOTOR ON}}$ $\overline{\text{WGATE IN}}$ to Port 2 $\overline{\text{DS}}$			80	ns
Data Setup Time	$\overline{\text{DIR}}$ to $\overline{\text{STEP}}$	50			ns
Data Hold Time	$\overline{\text{DIR}}$ to $\overline{\text{STEP}}$	0			ns
Delay Accuracy (Pin 13)	Td = 0.59 Rd x Cd R_D = 3.9 K to 10 K C_D = 75 pF to 300 pF	0.8TD		1.2TD	sec
Pulse Width Accuracy (Pin 14)	Tw = 0.59 Rw x Cw Rw = 3.9 K to 10 K Cw = 75 pF to 300 pF	0.8Tw		1.2Tw	sec

PORT 2 (P20 - P23) TIMING (Timing Referenced to PROG signal, Figure 1.)

SYMBOL	DESCRIPTION	MIN	NOM	MAX	UNIT
TSA	Addr. setup time	100			ns
THA	Addr. hold time	80			ns
TSD	Data-in setup time	100			ns
THD	Data-in hold time	80			ns
TACC	Data-out access time			700	ns
TDR	Data-out release time			200	ns
TPW	PROG pulse width	1500			ns

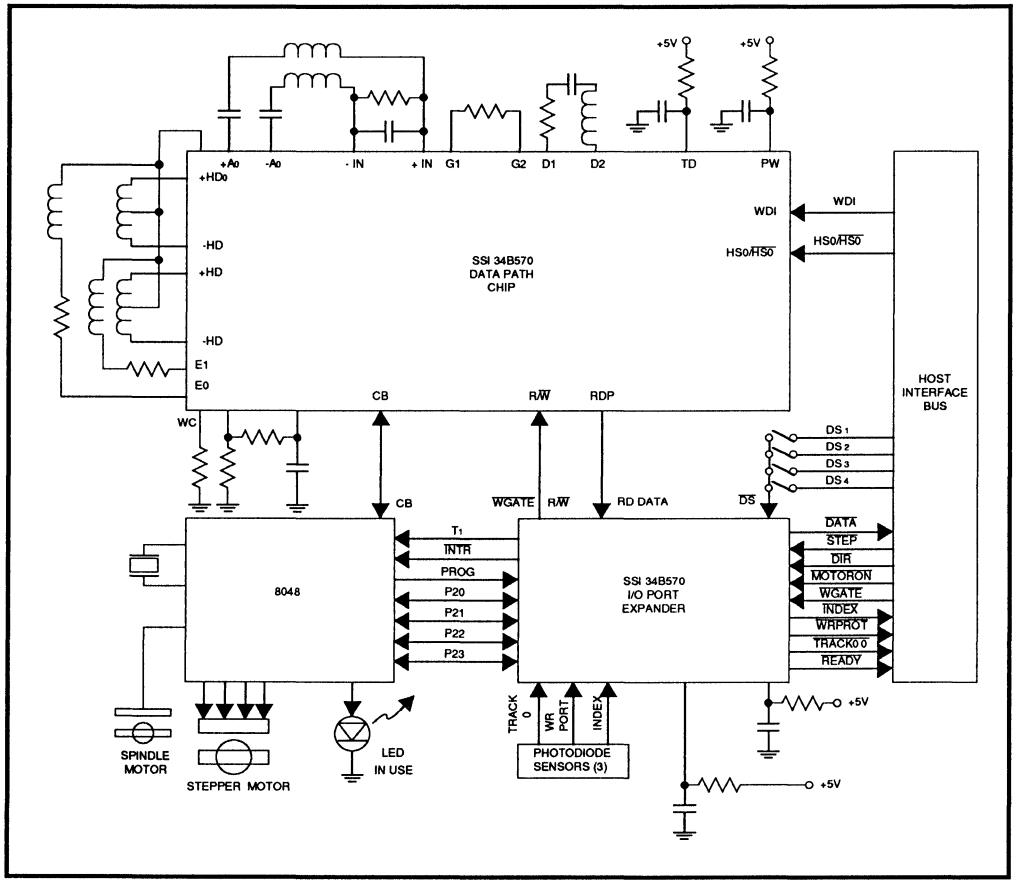
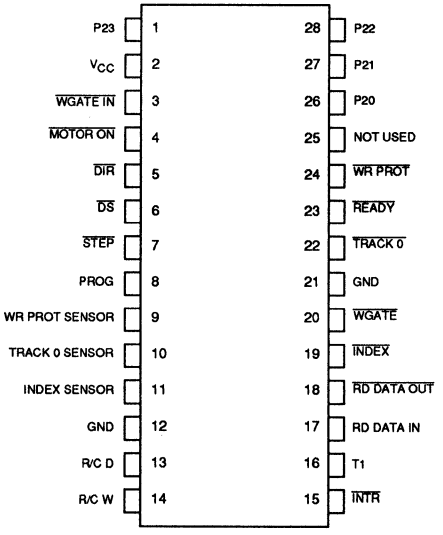


FIGURE 2: Typical Application

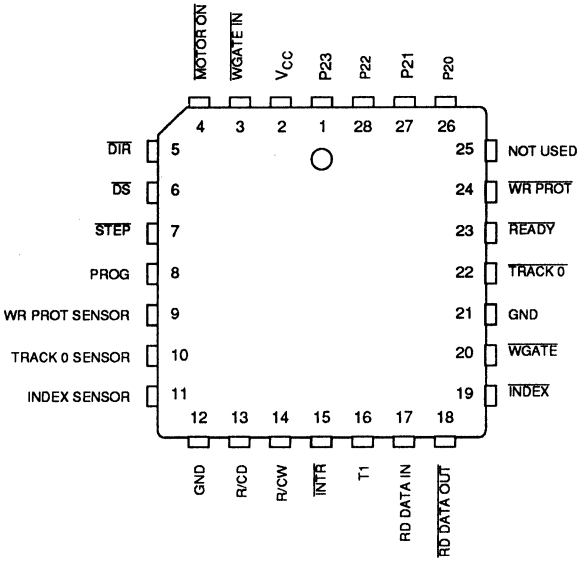
SSI 34B580
Port Expander
Floppy Disk Drive

PACKAGE PIN DESIGNATIONS

(TOP VIEW)



28-Pin DIP



28-Pin PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 34B580 28-Pin DIP	34B580-CP	34B580-CP
SSI 34B580 28-Pin PLCC	34B580-CH	34B580-CH

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714) 731-7110, FAX: (714) 573-6914

Section 10

CUSTOM SOLUTIONS

SILICON SYSTEMS LEADS THE WAY DEVELOPING MIXED-SIGNAL CUSTOM PRODUCTS.

This is a story about leadership. Silicon Systems is dedicated to taking the point in the creation of high-performance, application-specific custom, Mixed-Signal Integrated Circuits (MSICs™).

Such dedication means we bring a lot to the party. Including truly innovative analog, digital, and mixed analog-digital ICs. A full complement of mixed-signal CMOS, BiCMOS and Bipolar wafer fabrication processes, state-of-the-art automated design tools, production, assembly, test, and QA capability.

No one's more experienced

Our nearly 20 years of successful IC design work makes us the most experienced engineering team in the MSICs field. Add it all up and you get a company that saves you time and money while delivering you the most sophisticated mixed-signal custom ICs you can get.

Faster to market for mixed-signal applications

Whatever your mixed-signal design application, Silicon Systems gives you a competitive advantage. In communications, disk drives, other storage products, automotive control systems, or other analog/digital signal processing applications, you can depend on our technical know-how to do the job right and turn your design around faster.

CMOS. Bipolar. Analog. Digital. We've done it

Our designers are an experienced bunch. They're uniquely able to take a look at your specific application problem and move quickly to the right IC solution.

Our team is particularly adept at identifying key issues such as power, cost and performance trade-offs. So we can gear our efforts toward delivering you an optimized solution, manufactured with the appropriate fab process.

Technique	Application	Silicon Systems Designed Examples
CMOS Signal Processing	For analog continuous time and sampled data (switched-capacitor implementation) and Digital Signal Processing (DSP) applications. Low-power capability also allows inclusion of ROMs, RAMs, and other analog/digital subsystems.	• 73K224 complete single-chip 2400 bit/s modem • C301 single-chip telephone headset amplifier • 14.4 kbit modem • Direct-broadcast satellite descrambler • Motor controllers • Hi-resolution analog data acquisition
Bipolar Signal Processing	For high-performance, low noise, wideband signal acquisition and processing applications. Offers TTL and/or ECL logic interfaces with high current drive.	• Sub 1 nV/√Hz HDD R/W amplifiers • AGC, pulse detection amplifiers • High-speed data separators • Wideband transceivers • PLLs (Phase Locked Loops) • Optical signal processing
Digital CMOS	For ASIC controllers, sequencers and data path applications with on-board ROM, RAM, and PLA sub-systems. Offers standard TTL and/or CMOS logic interfaces.	• Hard disk drive controllers • SCSI interface controllers • UARTs • Protocol controllers • Digital signal processors
Digital Bipolar	High-speed logic and interface circuitry. Offers standard logic or custom interfaces.	• Encoders and decoders • High-speed digital transceivers

The right mix of analog and digital

Providing total analog/digital systems on a chip allows you to meet your cost and performance objectives whether you're designing the next generation of communications devices, or perhaps an I/O multiplexer to control electronics in 21st century automobiles.

We've turned to CMOS to effectively implement low-power, highly integrated systems solutions for everything from modems and CATV satellite descramblers to hard disk drive controllers and digital signal processors.

We've gone the Bipolar route to meet the high-performance needs of products like wideband transceivers, R/W amplifiers, low-noise amplifiers, pulse detectors, high-speed data separators and high-performance, low-power combo devices.

On the way is BiCMOS technology. It promises to open up new horizons of product capability for applications demanding optimum performance at the lowest power.

SOPHISTICATED TOOLS FOR A CUSTOM DESIGN

At each of five design centers capable of worldwide service — Tustin, Santa Clara and Nevada City, California; Tokyo and Singapore — Silicon Systems employs PEGASYS™, an internal design automation system developed from carefully selected vendor tools and our own proprietary software. Using Mentor Graphics workstations for both electrical and physical design, PEGASYS helps create complex designs while significantly reducing schedules, costs and errors.

By integrating such helpful third-party tools and custom software, we're better able to design and analyze mixed-signal integrated circuits in all CMOS, Bipolar And BiCMOS technologies. It's an approach that has given us the edge in mixed-signal design and helped put Silicon Systems' customers in a favorably unique position in the marketplace.

Specifically, PEGASYS brings the following to each design:

- Fully integrated design environment
- Methodology for precision circuit design
- Integrated physical design
- Automatic place and route
- Complete layout verification

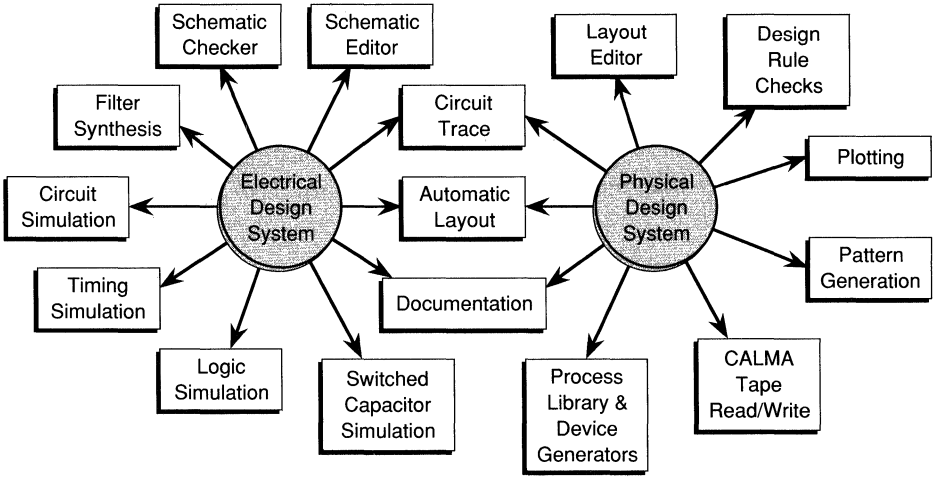
Our design automation staff integrates the third-party tools and optimizes their use on the Mentor platform. This framework can easily accommodate new tools when needed, and it enables us to support a combination of analog and digital design techniques in all CMOS, Bipolar and BiCMOS chip designs. By mixing design methodologies, we can achieve optimum systems performance, even when schedules are tight.

Electrical design

A single CAE (Computer Aided Engineering) environment provides for schematic capture, simulation, synthesis and documentation. We support this software with extensive libraries of pre-designed cells and components. Highly specialized cells or components can be designed and enhanced where required. We simulate each circuit to meet precise performance specifications using:

- Analog circuit simulation
- Digital logic simulation
- Timing simulation
- Mixed-mode simulation
- Switched-capacitor filter simulation
- Behavioral simulation

Admittedly, simulation alone is not the key to perfecting performance. That's why we work aggressively to refine our understanding of models to make them work with simulation. Inside our progressive Device Modeling and Characterization



laboratory, we develop accurate circuit simulation models and parameters. The DMC lab provides complete device model data for our processes using capabilities such as AC measurement, statistical analysis and worst-case modeling. Accurate models are a cornerstone of our design-for-quality approach.

Physical design

Our PEGASYS Layout System aids the mask designer through all physical design phases, ensuring consistency throughout the design cycle. This fully integrated environment provides for both full-custom design and auto place-and-route design including these capabilities:

- Graphic editing
- On-line point-to-point routing
- Compaction
- On-line design rule checking
- Layout-to-schematic verification
- Parasitic extraction/back annotation
- Output in industry standard GDS format

The same physical design environment supports all processes and design methodologies.

Automatic place & route software

The automatic place-and-route capability speeds through physical design far more rapidly than a full-custom, hand-drawn approach. We have combined Cadence Design Systems' TANCELL™, the most area-efficient router on the market, with our proprietary tools. This flexible environment allows for floor planning and automatic routing, and it supports the combination of custom cells, standard cells and compiled blocks.

Layout-to-schematic trace and verification software

Our circuit-trace capability compares the completed IC layout to the schematic database, using proprietary techniques and tools to guarantee quality. We help to eliminate layout errors through verification checks of both connectivity and component values. The resulting layout is an exact match of the schematic design. Further possible layout problems are identified during post-layout simulations using true parasitic modeling of capacitance and resistance interconnect. In short, all potential problems are fixed or addressed before first silicon fabrication.

KADS. A mutual drive for custom design

The Silicon Systems Key Account Design Service (KADS) program is our way of designing and developing custom IC solutions in a high-level cooperative partnership with our customers.

The KADS approach introduces the best minds in your company to Silicon Systems' mixed-signal specialists. Together we work closely, freely exchanging each other's ideas and experience in order to inspire breakthrough technical achievements and raise quality and creativity to a new level.

WHERE PROCESS MEETS NEED: CMOS

Silicon Systems offers two proven CMOS process technologies for creating low-power, highly integrated systems solutions. We use CH for 5V and12V applications and CG for 5V only needs. Both offer excellent analog performance. For a summary, see Table 1.

Our CH process achieves its higher (to 12V) operation via a DDD (Double Diffused Drain) source/drain structure. This increases the S/D junction grading and breakdown voltage while lowering the associated junction capacitance.

The CH process also provides high quality, low voltage coefficient, precision poly-poly capacitors that support high performance switched-capacitor filtering and data conversion (A/D and D/A) circuits. Another important CH process feature for analog applications is found with our high Ω/° poly resistors. Their low voltage coefficient is important for low distortion, continuous time filters such as in anti-aliasing applications. Typical CMOS processes use unacceptable high-value well resistors, and do not provide poly-poly capacitors.

Improved CMOS reliability

Silicon Systems boosts your system's reliability by incorporating a well ring into the CH process. This improves well tie-down and increases latchup immunity. For harsher environments such as motor drivers or the automobile, we use an epitaxial (epi) substrate to provide latchup immunity of more than 200 mA.

CMOS CG. Low-power & high performance

Our CG CMOS process is specifically designed to support your 5V mixed-signal applications. Its smaller feature size (1.5μ, shrinkable to 1.2μ) allows for much higher levels of system integration, higher speed and lower power.

CG supports high performance analog circuitry with precision poly-poly capacitors as well as complex digital circuitry including DSPs, microcontrollers, datapaths and memory.

For a cross-section view of the Silicon Systems CG CMOS process, see Figure 1.

BIPOLAR & BICMOS PROCESS TECHNOLOGIES

Our bipolar MSICs take advantage of two high-performance Bipolar processes: BK (for 12V applications) and BN (for 5V applications). The BK analog/digital process achieves its higher voltage operation and improves lateral PNP transistor performance by using a lightly-doped epi layer.

In BK we provide deep N+ and P+ enhancement layers to reduce both collector series and base resistance. Our use of up-junction isolation to gives us a major reduction in device area, when compared with that of typical junction isolated processes. Metal-Poly capacitors with a nitride dielectric are used for improving capacitor reliability.

BN. Low-power/ 8 Ghz Bipolar at 5 volts

A noteworthy feature of a minimum size BN process transistor is that it's only about 1/5th the size of a minimum size BK transistor. Because we employ full oxide isolation in BN, we can fabricate very fast, very small transistors and reduce sidewall capacitances. This supports not only high speed, but also low power.

The BN process features high-performance NPN transistors to support mixing high-performance emitter coupled logic (ECL) with analog circuitry. To provide for strict TTL I/O compatibility, we use superior PtSi Schottky diodes.

The resulting speed and packing density allows you to effectively implement dense high-performance, low-power Bipolar analog/digital capability into your system designs.

For a feature-by-feature comparison of Silicon Systems' BK and BN bipolar processes, see Table 3.

BiCMOS process technologies

High performance NPNs and CMOS transistors highlight our BiCMOS process. They support mixing high performance analog circuitry with high density digital logic.

We greatly improve response speed through the use of silicided base components and S/D regions that decrease extrinsic resistances in both types of active components while reducing the Emitter-Base and Gate-Source (Drain) space.

Our BiCMOS process offers enhanced reliability and fully supports all 5V mixed-signal designs.

Process	Type	Application Voltage	BVDSS	Drawn Gate Length	Interconnect Pitches Poly 1	Metal 1	Metal 2	Features
CH	Si-Gate, single metal, dual poly, P Well	12V	18V	3.6μ	5.8μ	6.4μ	n/a	• DDD S/D structure • Poly-poly capacitors • Low-voltage coefficient • High Ω/□ poly resistors • Epi substrate option • Buried well-ring
CG	Si-Gate, dual metal, dual poly, P Well	5V	7V	1.5μ	3.0μ	4.5μ	6.0μ	• DDD S/D structure • Poly-poly capacitors • Shrinkable to 1.2μ

TABLE 1: CMOS Process Chart

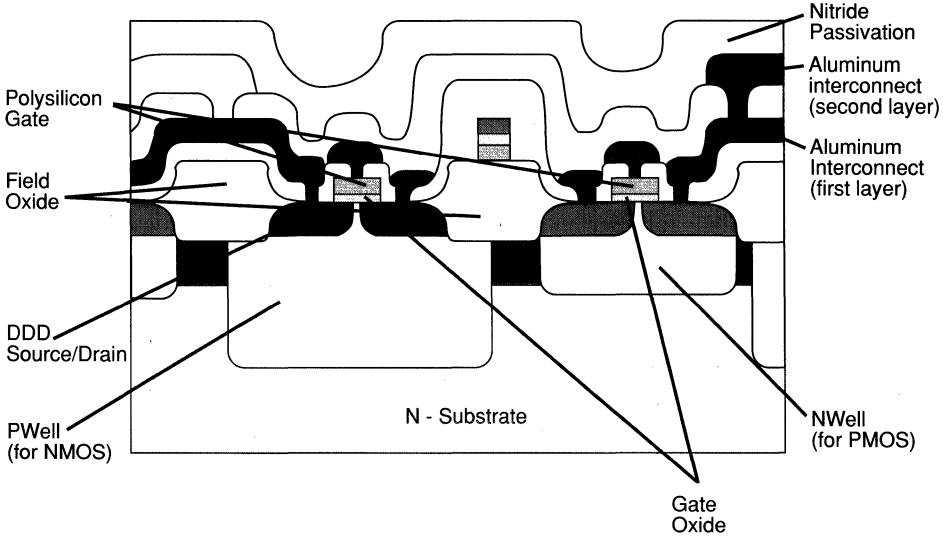


FIGURE 1: CG CMOS Process Transistor

Type	Appl. Voltage	BVDSS	Drawn Gate Length	Interconnect Pitches Poly	M0	M1	M2	BV_{CEO}	NPN Ft	Emitter	Features
Bipolar: Oxide isolated **CMOS:** Si-Gate, single poly, triple metal, P Well	5V	10V	1.0µ	2.6µ	3.2µ	3.8µ	5.0µ	8V	13 GHz	1.0µ	**Bipolar:** •High Perf. NPN'S •PtSi Schottky Diodes •Gate Oxide Capacitors •Poly Capacitors •Sidewall Oxide Isolation •Fuses **CMOS:** •Lightly Doped Drains

TABLE 2: BiCMOS Process Chart

Process	Type	BV_{CEO}	NPN Ft	Emitter Size	M1 Pitch	M2 Pitch	Features
BK	Junction-isolated	12V	2 GHz	2.5µ	9.0µ	14.0µ	• Polysilicon emitters • A1 Schottky diodes • Nitride capacitors • Ion implanted resistors • Up/down junction isolation • Collector/base plugs
BN	Oxide-isolated	6V	8 GHz	2.0µ	4.5µ	8.0µ	• High performance NPNs • PtSi Schotty diodes • Nitride capacitors • Ion implanted resistors • Sidewall oxide isolation • Collector/base plugs

TABLE 3: Bipolar Process Chart

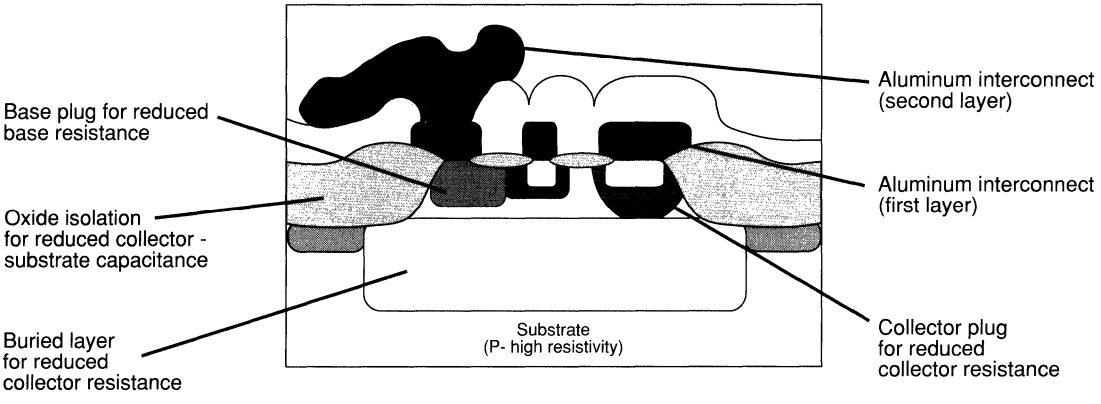


FIGURE 2: BN Bipolar Process NPN Transistor

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A SUPERIOR FINISH FOR CMOS, BIPOLAR AND BICMOS

You might say this is the payoff window. The benefits of our process technologies, design tools and our unique custom approach all come together during wafer fabrication, test and assembly.

Our two manufacturing centers, located in Tustin and Santa Cruz, California, can offer specialized capabilities to match your particular fabrication requirements. Both facilities provide you with high resolution stepper photolithography technology, positive resist, dry plasma etch systems, high current ion implantation and automatic sputtering.

At Fab 1, in Tustin, we focus on Bipolar processes such as high-speed BN.

Our Fab 2, in Santa Cruz, emphasizes advanced mixed-signal CMOS processes. Fab 2, the newer of the two facilities, has been expanded to accommodate Fab 3, also on site in Santa Cruz, dedicated to a new high-speed BiCMOS process and the production of next generation six-inch wafers.

The right package

Silicon Systems offers a wide range of plastic dual-in-line and surface mount packages to meet the small footprint requirements of advanced storage and communication products. We continue to be innovative in surface mount technology by providing PLCC, SO, QFP, VSOP and SSOP packages. At our Singapore assembly & test facility we have the full capability to support high quality automated packaging while also maintaining rapid cycle times.

Promis. Quality through CAM

Process and Management Information System (PROMIS) underscores our commitment to Computer-Aided Manufacturing (CAM). And to delivering you a superior quality product on time.

We use PROMIS to facilitate the data required in our manufacturing, monitoring and Statistical Process Control (SPC) systems.

With PROMIS we more effectively manage our inventory, accurately track wafers in process, closely monitor the clean room environment.

PROMIS also assists our SPC efforts, as does our commitment to fully train all of our manufacturing personnel in SPC basics.

We design for quality

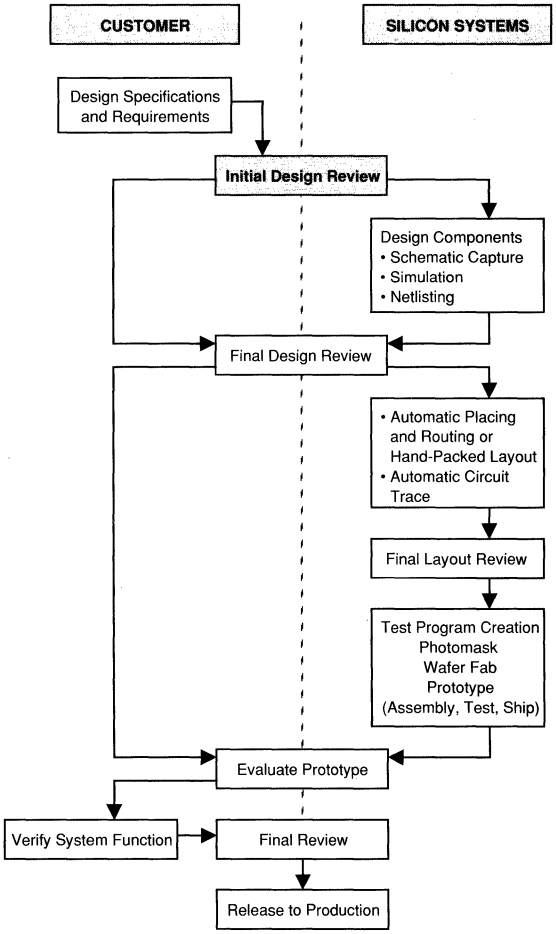
It's our view that quality is nothing less than absolute customer satisfaction. To achieve it, we begin far "upstream" in the product development process. Our design-for-quality approach scrutinizes the design itself with statistically based models, comprehensive simulation tools and vigorous design reviews.

The results of such an effort are IC products that boast lower defect rates, higher parametric performance and far fewer redesigns. Moreover, our persistence in improving quality keeps us focused on finding better and faster ways to satisfy future customer demands.

Quality that delivers

With effective systems such as PROMIS and our design for quality approach in place, Silicon Systems is prepared to deliver you finished products you can really depend on. On time. And under budget.

For details on how you can take best advantage of Silicon Systems' custom mixed-signal IC solutions, see your nearest Silicon Systems representative, or contact us. Silicon Systems, Inc. 14351 Myford Road, Tustin, CA 92680. 714-731-7110. FAX: (714) 573-6914.



CUSTOMER INTERFACE FOR FULL-CUSTOM AND CELL-BASED DESIGNS

Section

RELIABILITY & QUALITY ASSURANCE

11

silicon systems®
A TDK Group Company

Reliability and Quality Assurance

SECTION 1

1.1 INTRODUCTION

Silicon Systems is committed to the goal of customer satisfaction through the on-time delivery of defect free products that meet the customer's expectations and requirements. This statement serves as the corporate quality policy and reflects key elements that are instrumental in attaining true customer satisfaction. This section outlines Silicon Systems' ongoing activities for the control and continual improvement of quality in every aspect of our organization.

Silicon Systems is diligently working to maintain and improve its position as a world-class provider of mixed-signal integrated circuits (MSICs™). Our Corporate Quality Mission describes that commitment: "Achieve Total Customer Satisfaction Through Quality Excellence by Continuous Improvement."

We realize and practice the concept that quality and reliability must be designed and built into our products. In addition, Silicon Systems utilizes rigid inspections and data analysis to evaluate the acceptability and variation existing in incoming materials and performs stringent outgoing quality verification. The manufacturing process flow is encompassed by an effective system of test/inspection checks and in-line monitors which focus on the control and reduction of process variation. These gates and monitors ensure precise adherence to prescribed standards and procedures.

Silicon Systems also incorporates the use of statistical process control techniques into company operations. The control and reduction of the process variation by the use of statistical problem solving techniques, analytical controls and other quantitative methods ensures that Silicon Systems' products maintain the highest levels of quality and reliability. Our Reliability and Quality Assurance organization is committed to working closely with the customer to provide assistance and a continually improving level of product quality.

1.2 RELIABILITY AND QUALITY ASSURANCE

It is the objective of the Reliability and Quality Assurance organization to ensure that proactive quality systems are in place to ensure that Silicon Systems' products will meet or exceed customer requirements and expectations. In addition, the Reliability and Quality Assurance organization works to facilitate the timely implementation of solutions and monitors the effectiveness of corrective actions. These organizational strategies support the continuing enhancement of quality consciousness throughout Silicon Systems, a necessary element in support of world-class quality.

In order to facilitate the close coordination required of the Reliability and Quality function, a combined Reliability and Quality Assurance organization has been established. The R&QA organizational structure is pictured in Figure 1. To reflect corporate commitment, this organization is headed by a Senior Vice President reporting directly to the President/ COO.

SECTION 2: QUALITY ASSURANCE

2.1 QUALITY OBJECTIVES

While all Silicon Systems employees have direct responsibility for quality in their functions, Quality Assurance has the ultimate responsibility for the reliable performance of our products. This is accomplished through the administration of formal quality systems which assure Silicon Systems' management, as well as our customers, that products will fulfill the requirements of customer purchase orders and all other specifications related to design, raw material and in process through completion of the finished product.

Quality Assurance supports, coordinates and actively participates in the formal qualification of suppliers, material, processes, and products, and the administration of quality systems and production monitors to assure that our products meet Silicon Systems quality standards. Quality Assurance

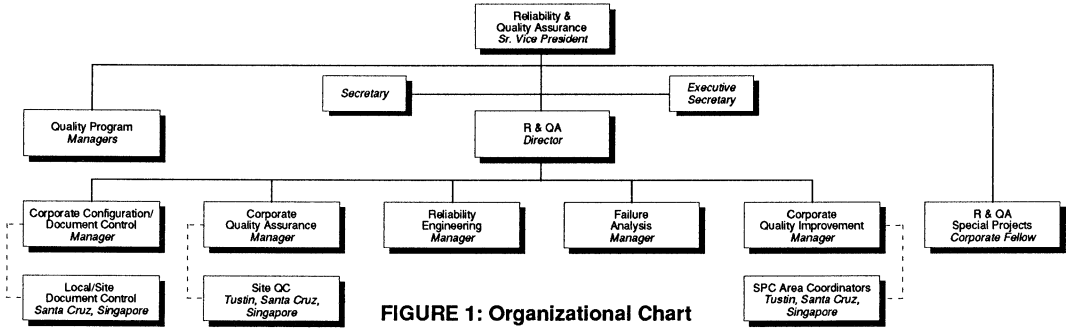


FIGURE 1: Organizational Chart

also provides the liaison between Silicon Systems and the customer for all product quality related concerns.

It is the practice of Silicon Systems to have corporate quality and reliability objectives encompass all of its activities. This starts with a strong commitment of support from the corporate level and continues with exceptional customer support long after the product has been shipped.

Silicon Systems emphasizes the belief that quality and reliability must be built into all of its products by ensuring that all employees are educated in the quality philosophy of the company. Some of the features built into Silicon Systems Quality Culture include:

1. Structured training programs directed at Wafer Fabrication, Test, Process Control personnel and supporting organizations.
   - Team based problem solving methodologies.
   - Corporate-wide training of quality philosophy and statistical methods.
2. Stringent in-process inspection, gates, and monitors.
3. Rigorous evaluation of designs, materials, and processing procedures.
4. Stringent electrical testing (100% and QC AQL/Sample testing).
5. Ongoing reliability monitors and process verifications.
6. Real-time use of statistical process control methodology.
7. Corporate level audits of manufacturing, subcontractors, and suppliers.
8. Timely corrective action system.
9. Control of non-conforming material.

These focused quality methods result in products which deliver superior performance and reliability in the field.

2.2.1 INCOMING INSPECTIONS

Incoming inspection plays a key role in Silicon Systems' quality efforts. Small variations in incoming material can traverse the entire production cycle before being detected much later in the process. By paying strict attention to the monitoring of materials at the earliest possible stage, variation can be reduced, resulting in a stable uniform process.

2.2.2 IN-PROCESS INSPECTIONS

Silicon Systems has established key inspection monitors in such strategic areas as Wafer Fabrication, Wafer Probe, Assembly, and Final Test. These quality monitoring tests are performed in addition to the intermediate and final inspections found in the manufacturing process.

Quality control monitors have been integrated throughout the manufacturing flow, so that data may be collected and analyzed to verify the results of intermediary manufacturing steps. This data is used to document quality trends or long term improvements in the quality of specific operations. Abnormality control is being used to enhance the effectiveness of this process. A generic description of the product flow and QC inspection points is shown in Figure 2. In process monitors such as oxide integrity, electromigration immunity and other parameters monitor long term reliability as well as circuit performance.

2.3 DESIGN FOR QUALITY

Since the foundation of a reliable product is rooted in the design process, the Reliability and Quality Assurance organization actively participates in comprehensive cross-functional reviews of design stages prior to the product's transition to production status. These review stages assure a predictable and effective development cycle. Other important design-related functions include ensuring that process specification revisions are translated into updated design parameters and the translation of manufacturing process capability into design guidelines. This is accomplished through the identification and monitoring of critical process and device

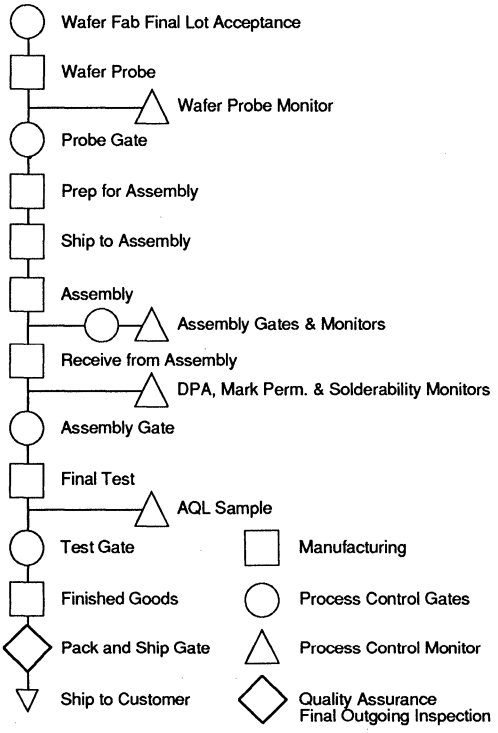


FIGURE 2
Process Control Gates and Monitors

parameters. Wafer level test at the early stages of process development also plays a critical role. These elements, included in Silicon Systems design for quality effort, support the development of robust design rules which are as insensitive as possible to inherent manufacturing variation. The result is a product that delivers predictable and reliable long term performance.

2.4 PPM REDUCTION PROGRAM

The primary purpose of a PPM reduction program is to provide a formalized feedback system in which data from nonconforming products can be used to improve future product consistency and reliability. The action portion of this program is accomplished in three stages:

1. Identification of defects by failure mode.
2. Identification of defect causes and initiation of corrective action.
3. Measurement of results and setting of improved goals.

The data summarized from the established PPM program is compiled as a ratio of units rejected/tested. This ratio is then expressed in terms of defective parts per million (PPM). Founded on a statistically valid database of PPM data and an established five-year strategic plan identifying PPM improvement goals, Silicon Systems has consistently achieved excellent quality standards and will continue to progressively improve PPM standards.

2.5. COMPUTER AIDED MANUFACTURING CONTROL

Computer Aided Manufacturing (CAM) is used throughout Silicon Systems for the identification, control, collection and dissemination of timely information for logistics control. Silicon Systems also uses this type of computerized system for statistical process control and manufacturing monitoring. PROMIS, (PROcess Management and Information System), displays approved/controlled recipes, processes, and procedures; tracks work-in-process; reports accurate inventory information; allows continuous recording of facilities data; contains statistical analysis capabilities; and much more. PROMIS allows for a paperless facility, a major element in minimizing contamination of clean room areas.

The PROMIS system has been configured to meet the specific requirements of Silicon Systems.

SECTION 3: RELIABILITY

3.1 RELIABILITY PROGRAM

Silicon Systems has defined various programs that will characterize product reliability levels on a continuous basis. These programs can be categorically described by:

1. Qualifications
2. Production Monitors
3. Evaluations
4. Failure Analysis
5. Wafer Level Reliability
6. Data collection and presentation for improvement projects

3.2 QUALIFICATIONS

Extensive qualification programs ensures that all new product designs, processes, and packaging configurations meet the absolute maximum ratings of design and the worst case performance criteria for end users. A large database generated by means of accelerated stress testing results in a high degree of confidence in predicting final use performance. The qualification criteria used are periodically reviewed to be consistent with Silicon Systems' increasing quality and reliability goals in support of our customers.

3.3 PRODUCTION MONITORS

This program has been established to randomly select a statistically significant sample of production products for subjection to maximum stress test levels in order to evaluate the useful life of the product in a field use environment.

Table 1 lists reliability test methods that are in use at Silicon Systems. This analysis of production monitor at Silicon Systems provides valuable information on possible design/process changes which assure continued improved reliability. The monitors are periodically reviewed for effectiveness and improvements.

3.4 EVALUATIONS

The evaluation program at Silicon Systems is an ongoing effort that will continue defining standards which address the reliability assessment of the circuit design, process parameters, and package of a new product. This program continuously analyzes updated performance characteristics of product as they undergo improvement efforts at Silicon Systems.

3.5 FAILURE ANALYSIS

The failure analysis function is an integral part of the Quality and Reliability department at Silicon Systems. Silicon Systems has assembled a highly technical and sophisticated failure analysis laboratory and staff. This laboratory provides visual analysis, electrical reject mode analysis, and both

TEST	CONDITIONS	PURPOSE OF EVALUATION
Biased temperature/humidity	85°C/85° %RH	Resistance to high humidity with bias
Highly accelerated stress test (HAST)	SSi Method	Evaluates package integrity
High temperature operating life (HTOL)	Mil 883C, Method 1005	Resistance to electrical and thermal stress
Steam pressure	121°C/15PSI	Resistance to high humidity
Temperature cycling	Mil 883C, Method 1010	Resistance to thermal excursion (air)
Thermal shock	Mil 883C, Method 1011	Resistance to thermal excursion (liquid)
Salt atmosphere	Mil 883C, Method 1009	Resistance to corrosive environment
Constant acceleration	Mil 883C, Method 2001	Resistance to constant acceleration
Mechanical shock	Mil 883C, Method 2002	Resistance to mechanical shocks
Solderability	Mil 883C, Method 2003	Evaluates solderability of leads
Lead integrity	Mil 883C, Method 2004	Evaluates lead integrity before board assembly
Vibration, variable frequency	Mil 883C, Method 2007	Resistance to vibration
Thermal resistance	SSi Method	Evaluates thermal dissipation
Electrostatic damage	Mil 883C, Method 3015	Evaluates ESD susceptability
Latch-up	SSi Method	Evaluates latch-up susceptibility
Seal fine and gross leak	Mil Std 883C, Method 1014	Evaluates hermeticity of sealed packages

TABLE 1: Reliability Stress Tests

destructive and non-destructive data to aid the engineers in developing corrective action for improvement. These test analyses may include metallurgical, optical, chemical, electrical, SEM with X-ray dispersive analysis, and E-Beam non-contact analysis as needed.

These conclusive in-house testing and analysis techniques, are complemented by outside support, such as scanning acoustic microscopy, focused ion beam, and complete surface and material analysis. This allows Silicon Systems to monitor all aspects of product manufacturing to ensure that the product of highest quality is shipped to our customers.

3.6 WAFER LEVEL RELIABILITY PROGRAM

A primary objective at Silicon Systems is to improve the reliability of our products through characterization of our manufacturing operations. The identification of specific failure mechanisms occuring in the wafer fabrication and assembly processes is a prerequisite to effective corrective action aimed at reducing defects and improving quality and reliability.

The primary advantage of wafer level reliability testing is the speed at which results can be derived, thereby providing additional response time and an early warning of process changes. This tool provides Silicon Systems with a very rapid analysis tool which allows for the early identification of possible problems and a determination of their origin.

The continuous improvement approach taken at Silicon Systems uses the wafer level reliability tests as tools to improve the process, identify potential problems, determine the sources of any process weakness and eliminate problems upstream in the process. This results in a focus on reliability improvement that goes well beyond merely determining the projected lifetime of a product to a detailed characterization, measurement and control of the specific parameters which actuallly determine product lifetime.

3.7 DATA COLLECTION AND PRESENTATION FOR IMPROVEMENT PROJECTS

Data collected from each element of the Reliability program is summarized for scope and impact and distributed among all engineering disciplines in the company. This data facilitates improvement and provides our customers an opportunity to review the performance of our product.

3.8 RELIABILITY METHODS

The Reliability Program utilizes a number of stress tests that are presently being used to define performance levels of our products. Many of these stress tests are per MIL-STD-883C as shown in Table 1.

3.9 RELIABILITY PREDICTION METHODOLOGY

At Silicon Systems, the Arrhenius model is used to relate a failure rate at an accelerated temperature test condition to a normal use temperature condition.

The model basically states FR = A exp(-Ea/KT)

Where:

FR = Failure rate

A = Constant

Ea = Activation Energy (eV)

K = Boltzmann's constant 8.62×10^{-5} eV/ degree K

T = Absolute temperature (degree K)

SECTION 4: ELECTROSTATIC DISCHARGE PROGRAM

4.1 ESD PREVENTION

Silicon Systems recognizes that the protection of Electrostatic Discharge (ESD) sensitive devices from damage by electrical transients and static electricity is vital. ESD safe procedures are incorporated throughout all operations which come in contact with these devices. Continuous improvement in the ESD protection levels is being accomplished through the incorporation of increasingly robust protection devices during the circuit design process as well as work area improvements.

Silicon Systems' quality activity incorporates several protection measures for the control of ESD. Some of the preventive measures include handling of parts at static safe-guarded workstations, the wearing of wrist straps during all handling operations, the use of conductive lab coats in all test areas and all areas which handle parts and the packaging of components in conductive or anti-static containers.

NOTES

Section 12

PACKAGING/ORDERING INFORMATION

Silicon Systems
Packaging Index

DUAL-IN-LINE PACKAGE (DIP)	PINS	PAGE NO.
Plastic	8, 14, 16 & 18	12-2
	20, 22, 24 & 24S	12-3
	28, 32 & 40	12-4
Ceramic	8, 14, 16 & 18	12-5
	22, 24 & 28	12-6
SURFACE MOUNTED DEVICES (SMD)		
PLCC (Quad)	20, 28	12-7
	32 & 44	12-8
	52 & 68	12-9
Quad (Flatpack)	52 & 100	12-10
Thin Quad Flatpack	32 & 48	12-11
	64	12-12
Small Outline (SOIC)	8, 14 & 16 SON	12-13
	16, 18, 20, 24 & 28 SOL	12-14
	34 SOL	12-15
	32 SOW	12-15
	36 SOM	12-15
	44 SOM	12-16
VSOP (SOV)	20, 24	12-16

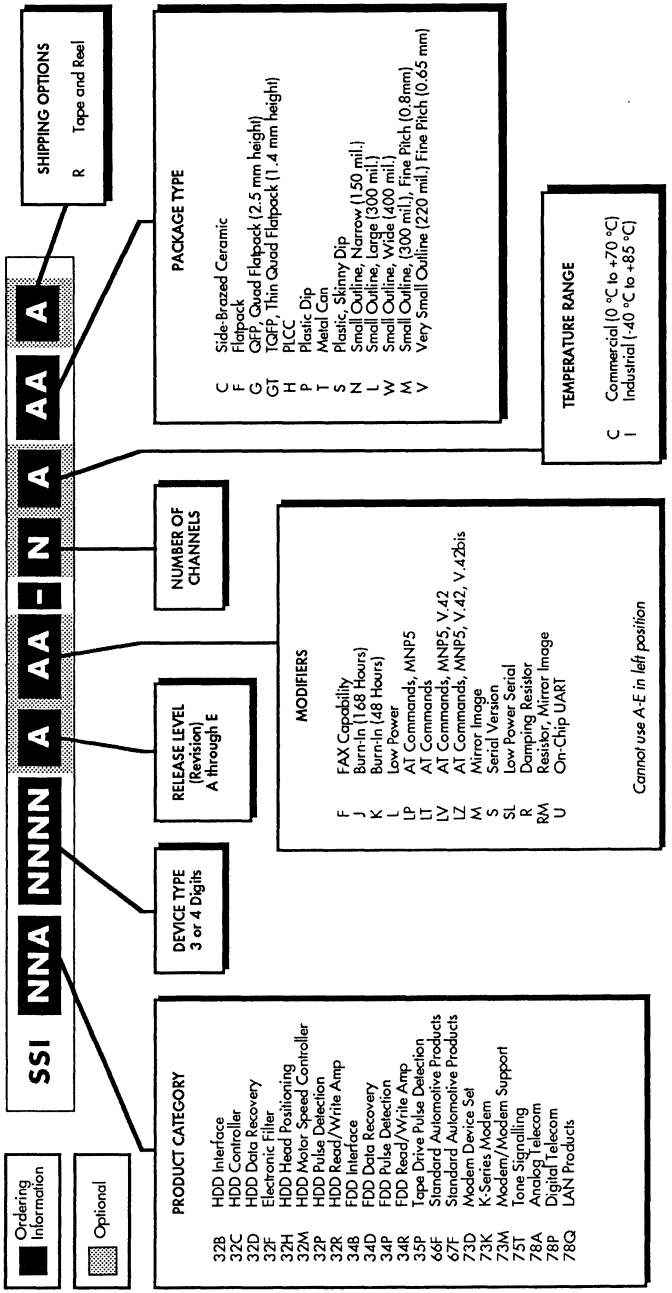
SON is a 150 mil width package.

SOL is a 300 mil width package.

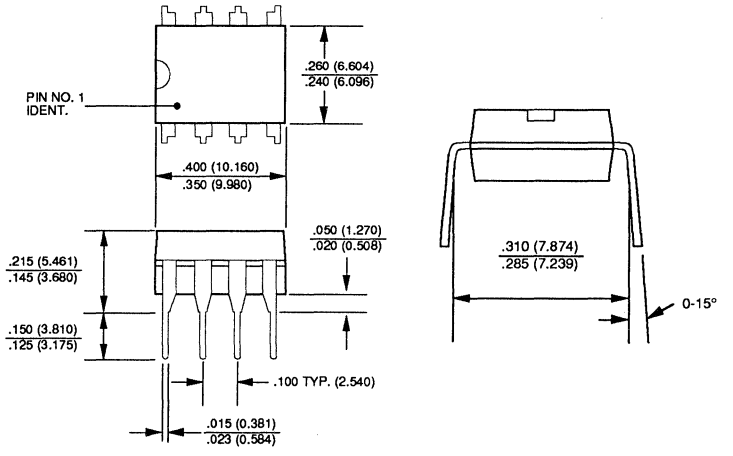
SOW is a 400 mil width package.

SOM is a 300 mil width package, fine pitch (0.8mm).

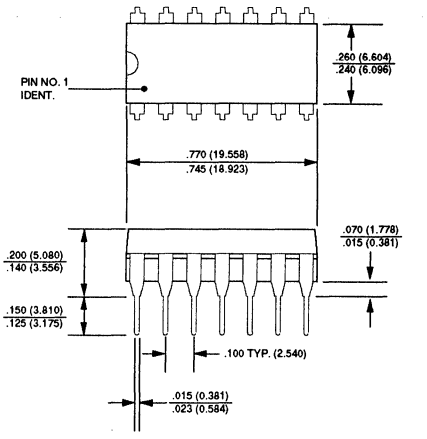
SOV is a 220 mil width package, fine pitch (0.65mm).


Ordering Information
Optional
SSI NNA NNNN A AA - N A AA A
PRODUCT CATEGORY
32B HDD Interface
32C HDD Controller
32D HDD Data Recovery
32E Electronic Filter
32H HDD Head Positioning
32M HDD Motor Speed Controller
32P HDD Pulse Detection
32R HDD Read/Write Amp
34B FDD Interface
34D FDD Data Recovery
34P FDD Pulse Detection
34R FDD Read/Write Amp
35P Tape Drive Pulse Detection
66F Standard Automotive Products
67F Standard Automotive Products
73D Modem Device Set
73K K-Series Modem
73M Modem/Modem Support
75T Tone Signalling
78A Analog Telecom
78P Digital Telecom
78Q LAN Products
DEVICE TYPE 3 or 4 Digits
RELEASE LEVEL (Revision) A through E
MODIFIERS
F FAX Capability
J Burn-In (168 Hours)
K Burn-In (48 Hours)
L Low Power
LP AT Commands, MNP5
LT AT Commands
LV AT Commands, MNP5, V.42
LZ AT Commands, MNP5, V.42, V.42bis
M Mirror Image
S Serial Version
SL Low Power Serial
R Damping Resistor
RM Resistor, Mirror Image
U On-Chip UART
Cannot use A-E in left position
NUMBER OF CHANNELS
PACKAGE TYPE
C Side-Brazed Ceramic
F Flatpack
G QFP, Quad Flatpack (2.5 mm height)
GT TQFP, Thin Quad Flatpack (1.4 mm height)
H PLCC
P Plastic Dip
T Metal Can
S Plastic, Skinny Dip
N Small Outline, Narrow (150 mil.)
L Small Outline, Large (300 mil.)
W Small Outline, Wide (400 mil.)
M Small Outline, (300 mil.), Fine Pitch (0.8mm)
V Very Small Outline (220 mil.) Fine Pitch (0.65 mm)
TEMPERATURE RANGE
C Commercial (0 °C to +70 °C)
I Industrial (-40 °C to +85 °C)
SHIPPING OPTIONS
R Tape and Reel

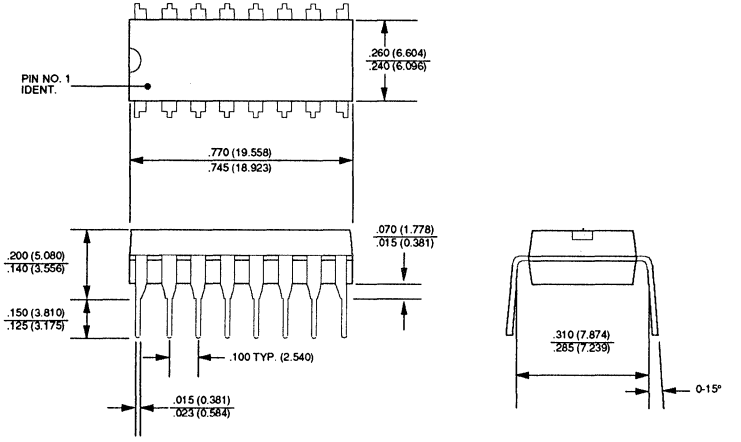
Package Information
(Plastic DIP)



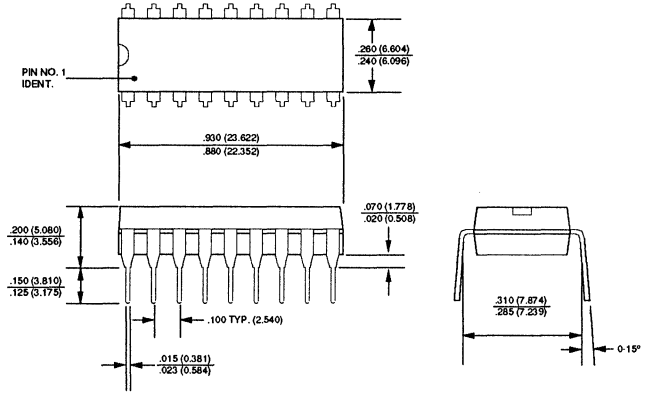
8-Pin Plastic



14-Pin Plastic

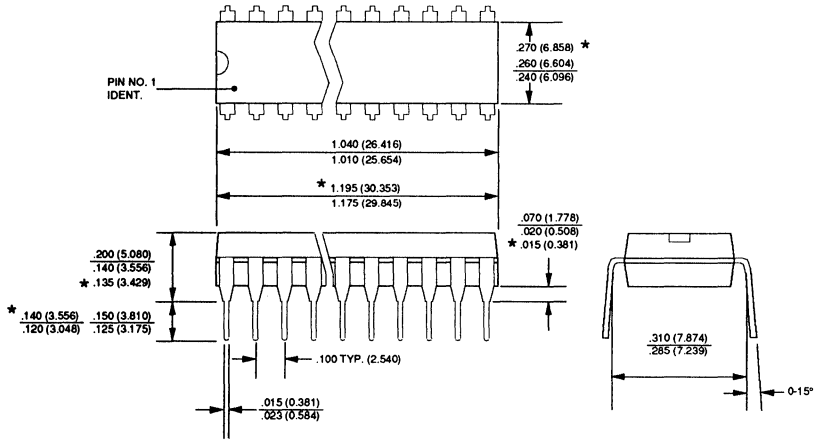


16-Pin Plastic

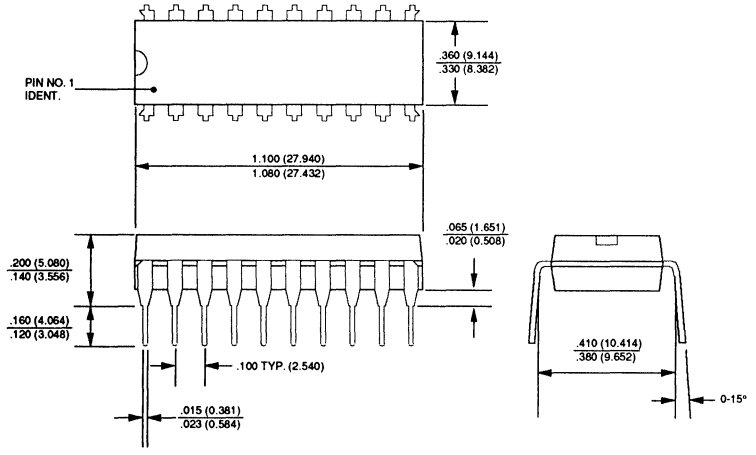


18-Pin Plastic

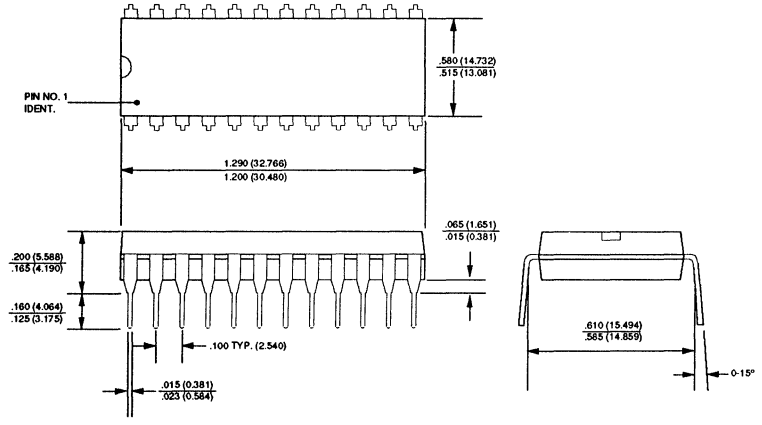
Package Information



20 Pin Plastic
***24S Pin Plastic**



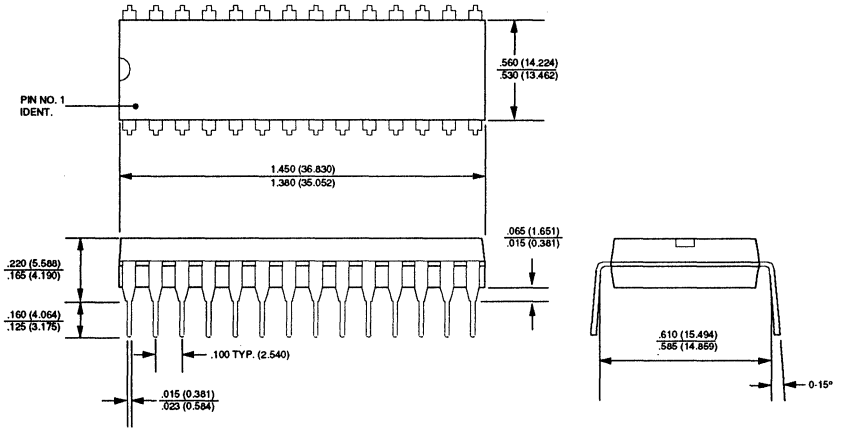
22-Pin Plastic



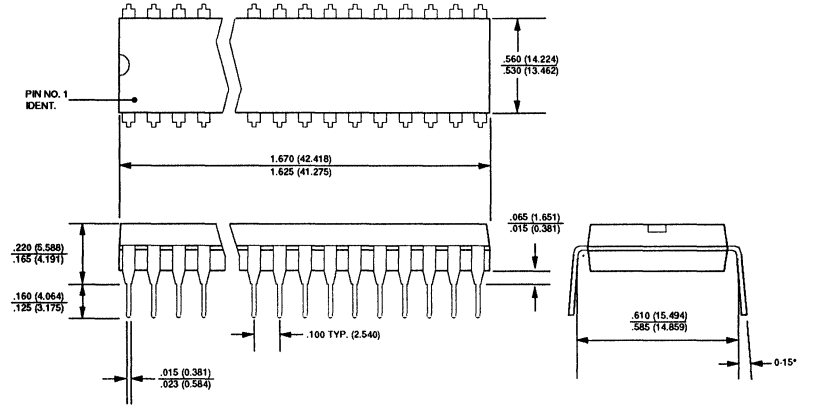
24-Pin Plastic

12

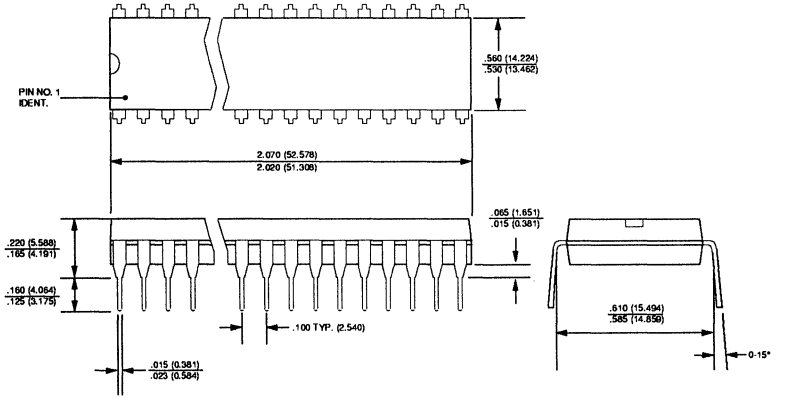
Package Information



28-Pin Plastic

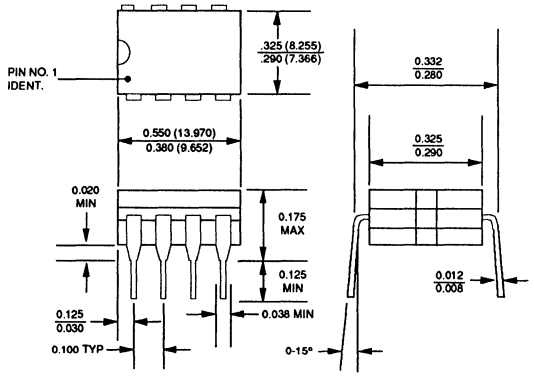


32-Pin Plastic

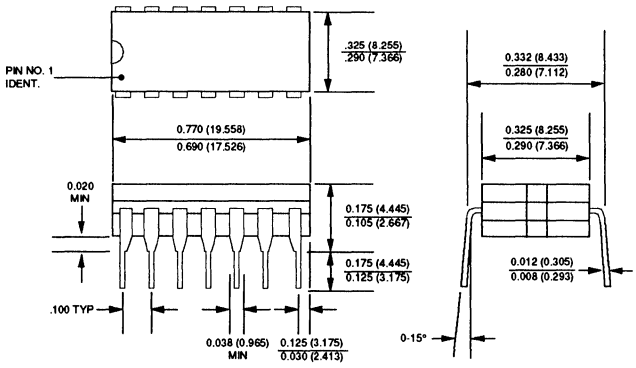


40-Pin Plastic

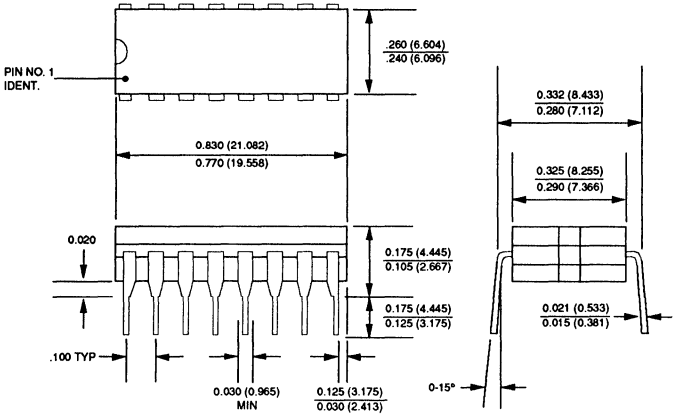
Package Information
Cerdip



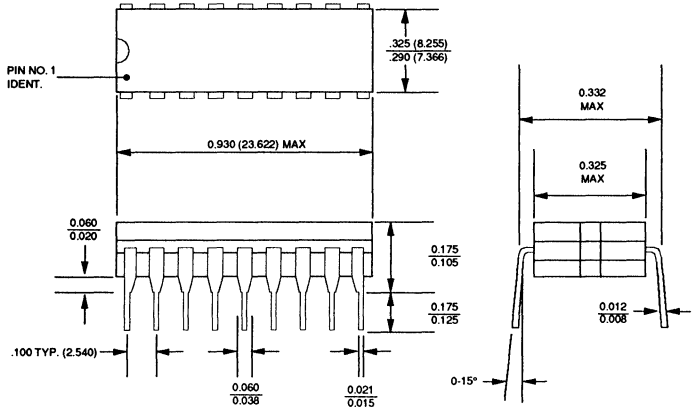
8-Pin Cerdip



14-Pin Cerdip

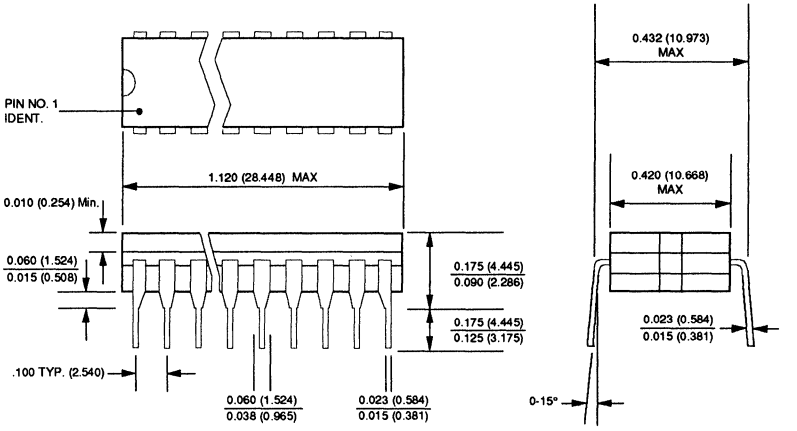


16-Pin Cerdip

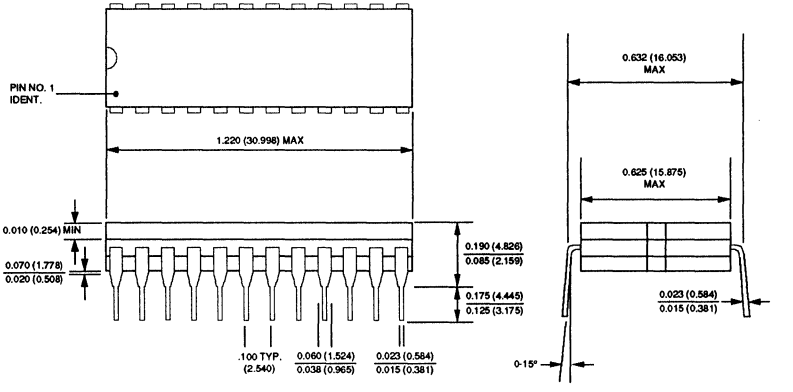


18-Pin Cerdip

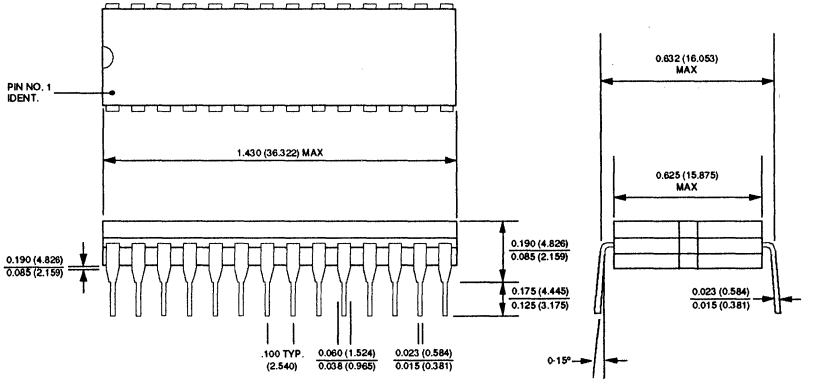
Package Information



22-Pin Cerdip

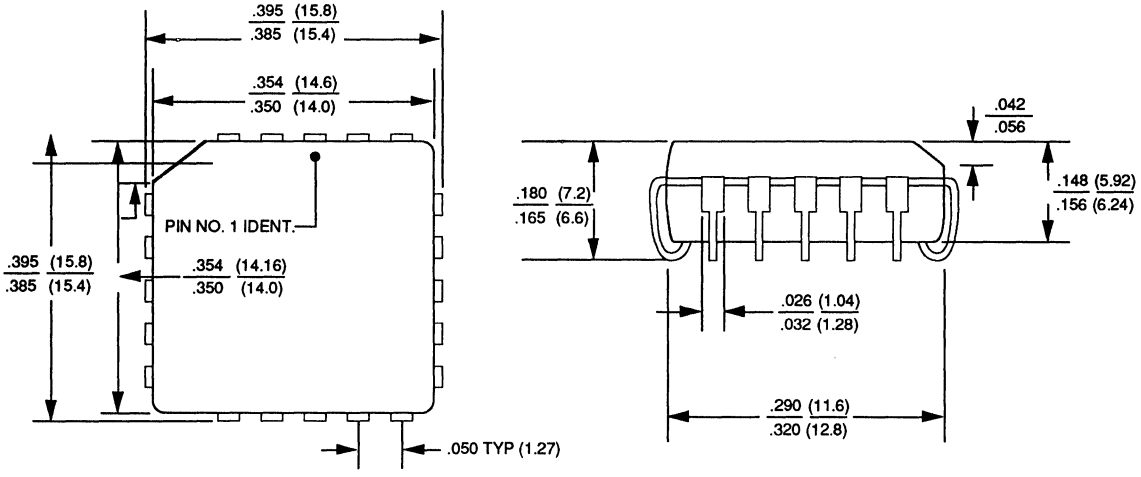


24-Pin Cerdip

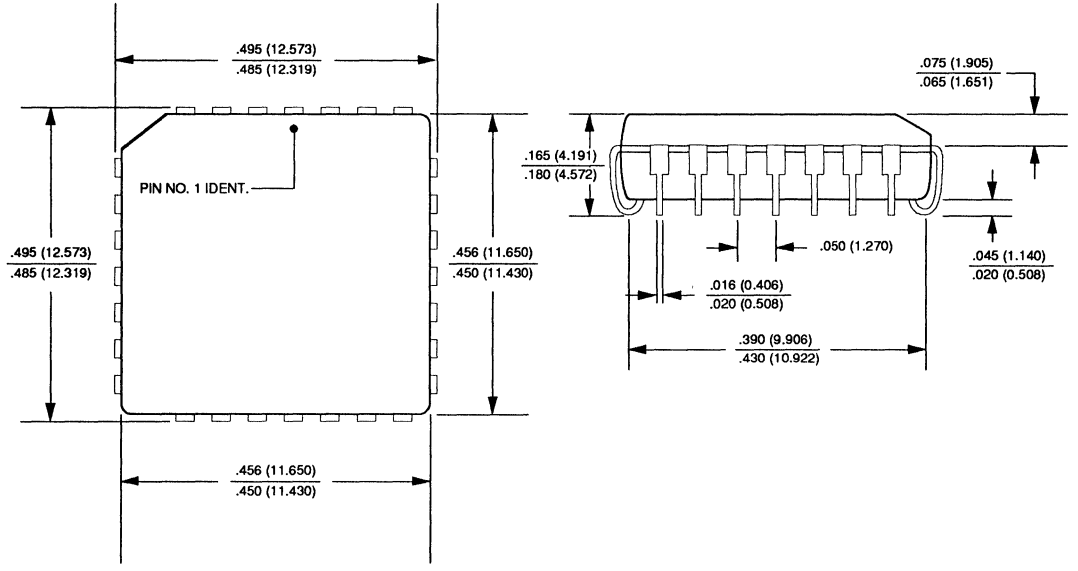


28-Pin Cerdip

Package Information
PLCC (Quad)



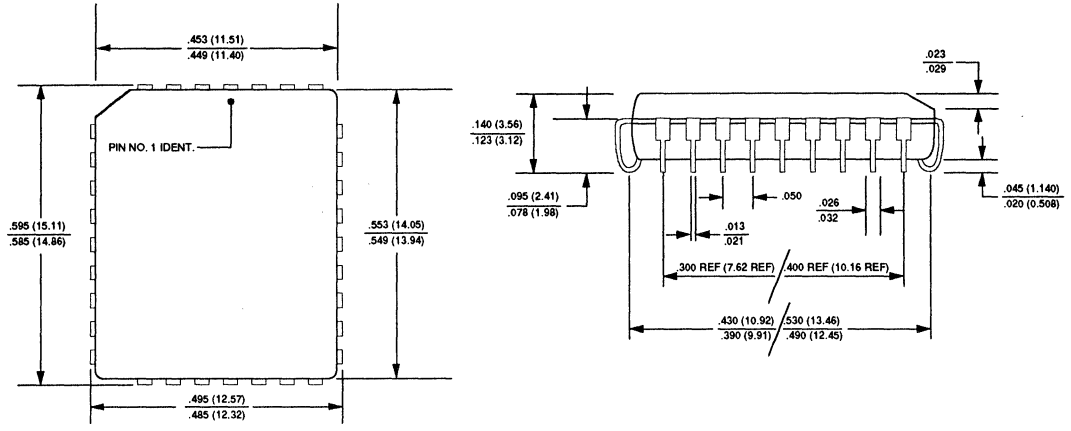
20-Pin Quad PLCC



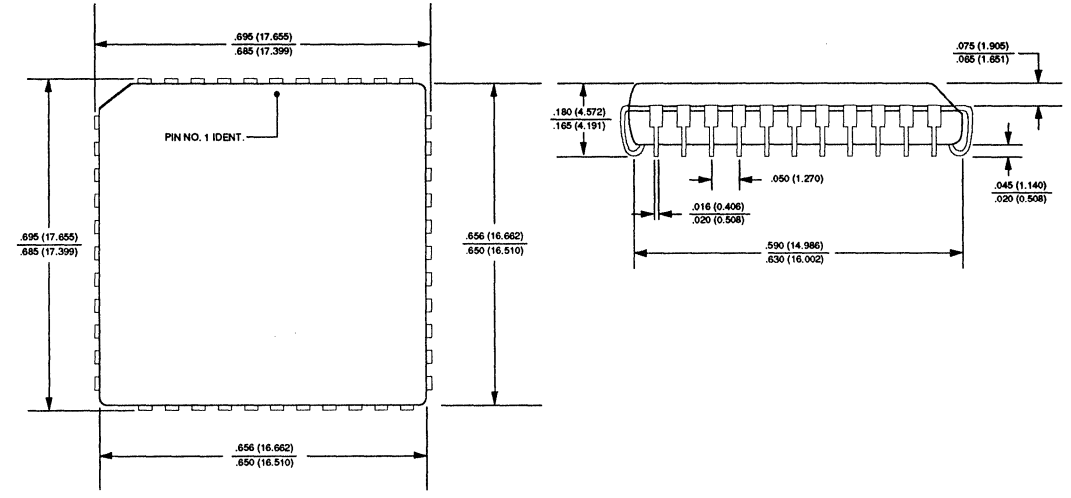
28-Pin Quad PLCC

12

Package Information

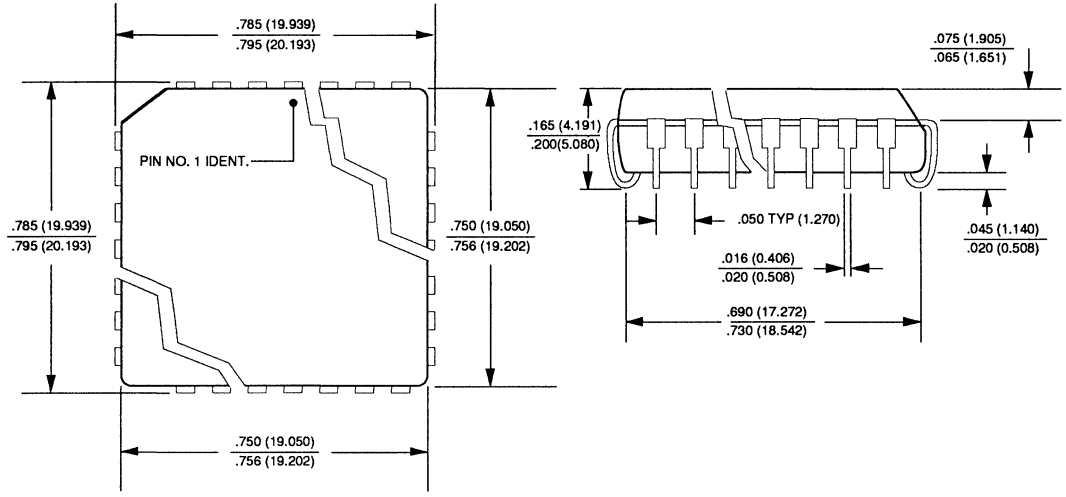


32-Pin Quad PLCC

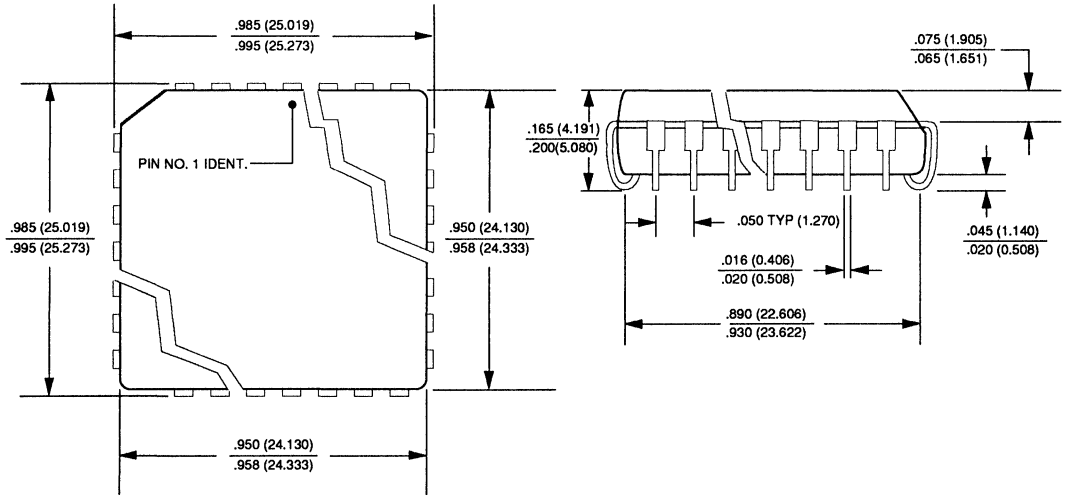


44-Pin Quad PLCC

Package Information
PLCC (Quad)



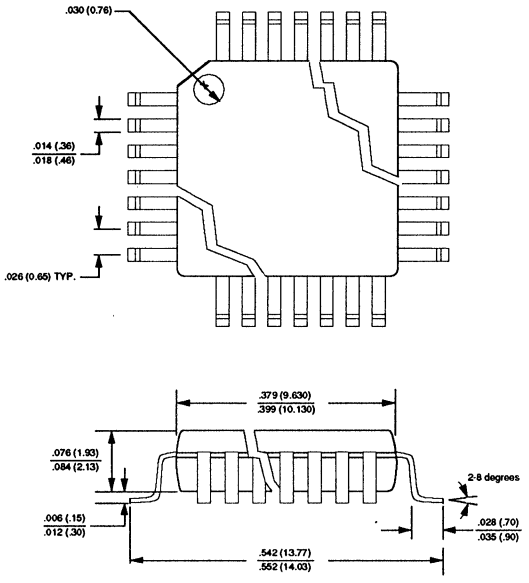
52-Pin Quad PLCC



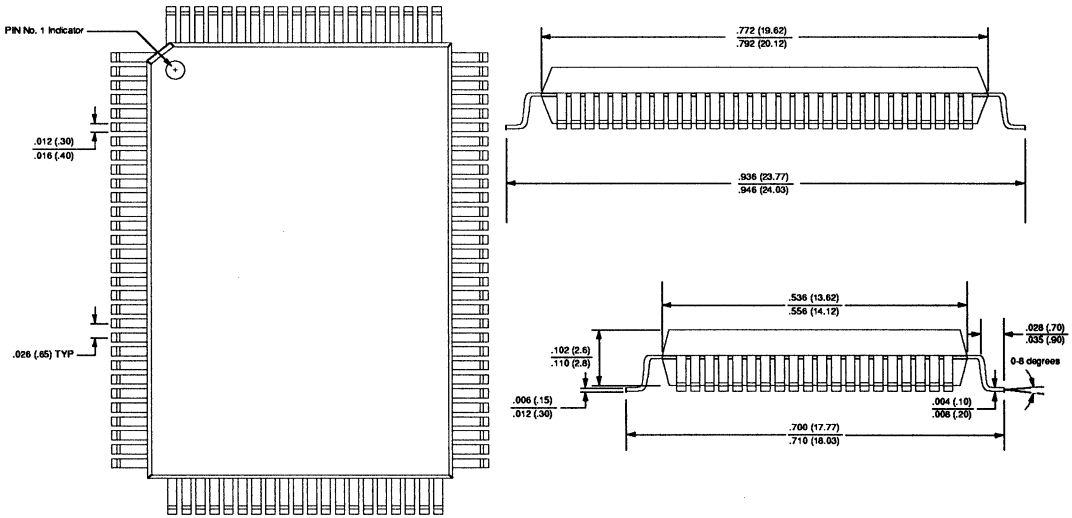
68-Pin Quad PLCC

12

Package Information
Quad Flatpack

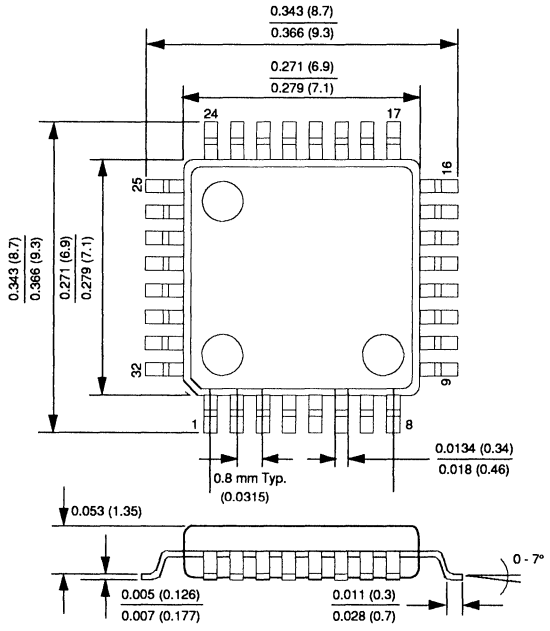


52-Lead Quad Flatpack

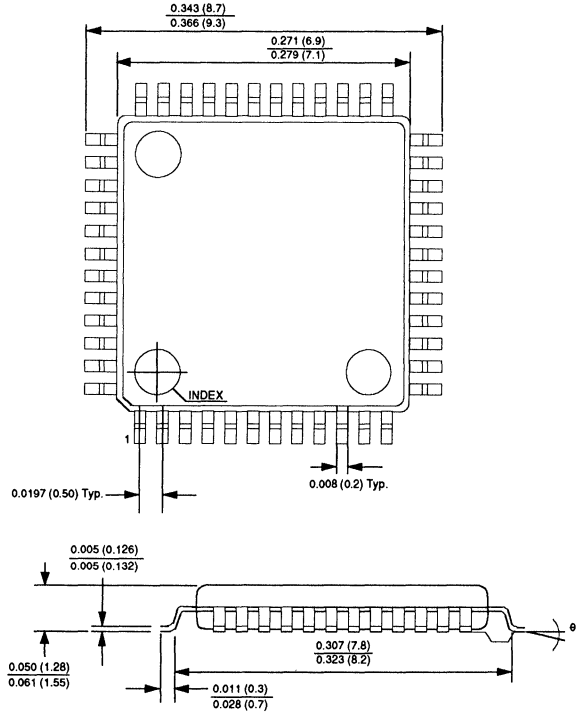


100-Lead Quad Flatpack

Package Information
Thin Quad Flatpack



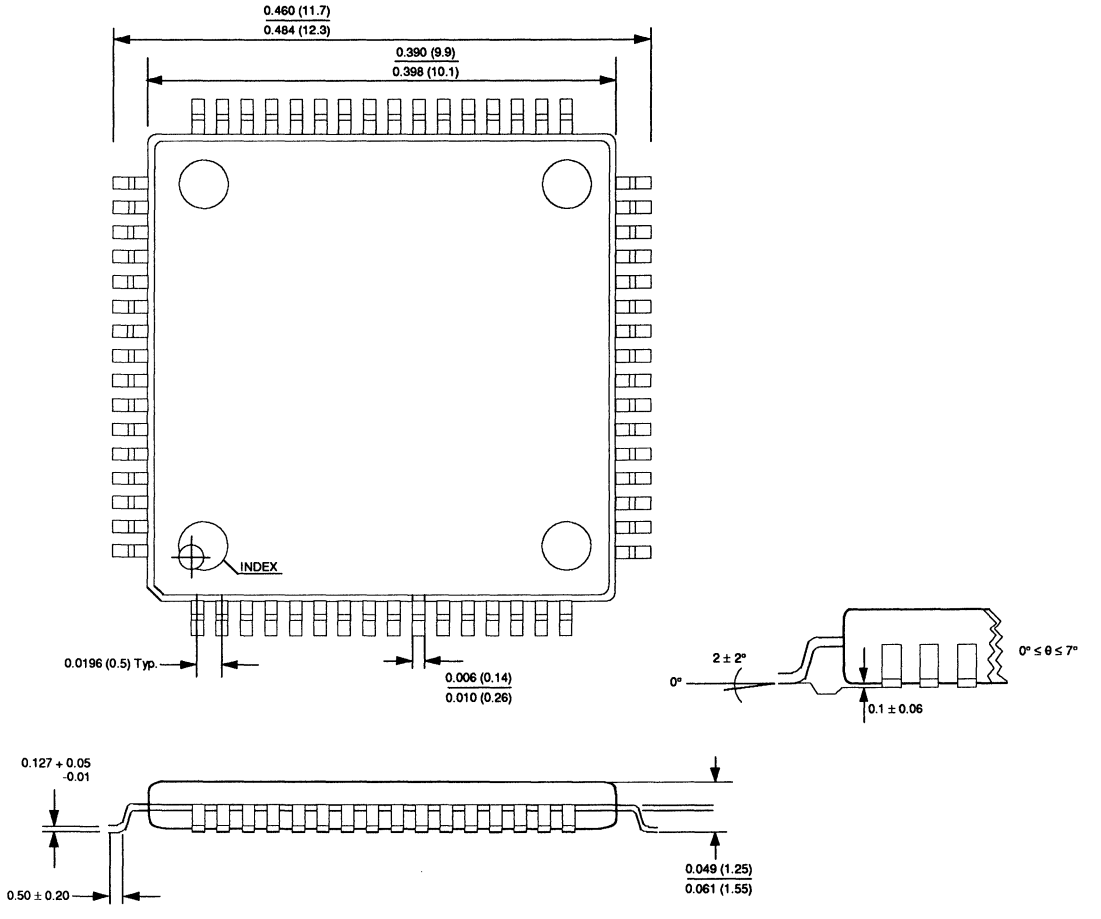
32-Lead Thin Quad Flatpack



48-Lead Thin Quad Flatpack

12

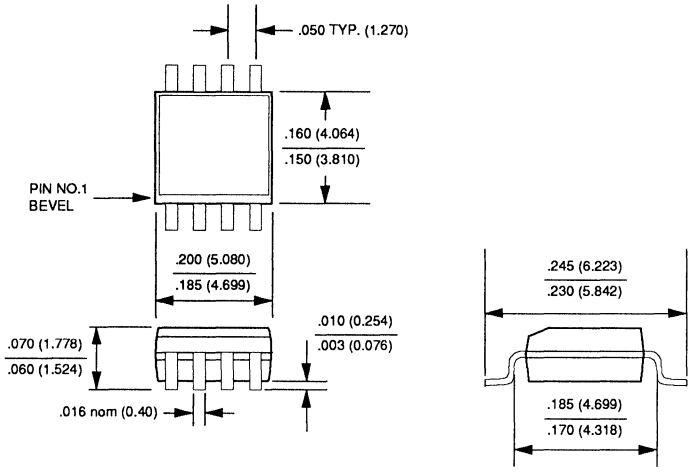
Package Information



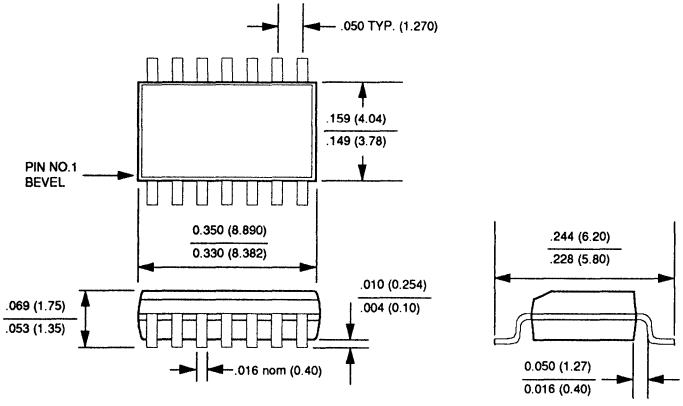
64-Lead Thin Quad Flatpack

Package Information
(SON)

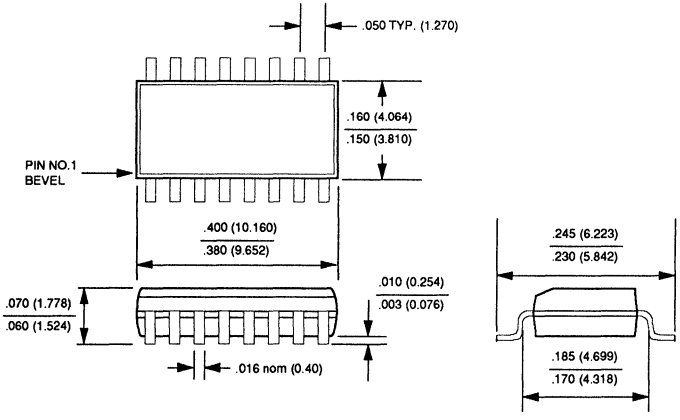
8-Pin SON



14-Pin SON

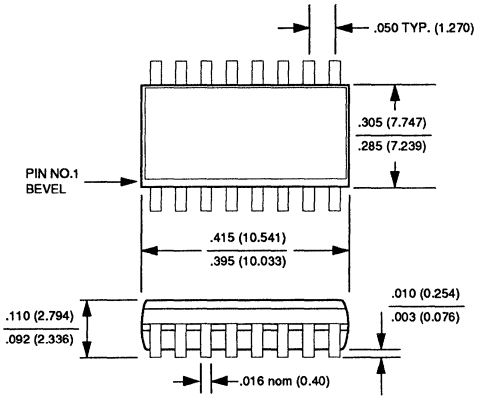


16-Pin SON

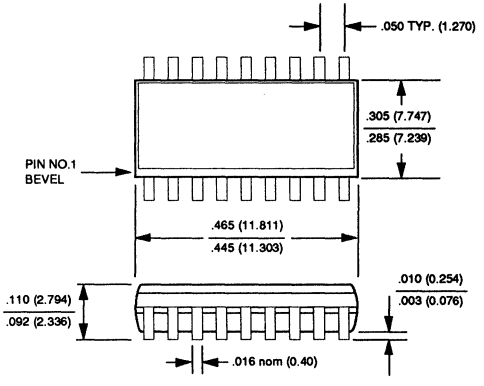


12

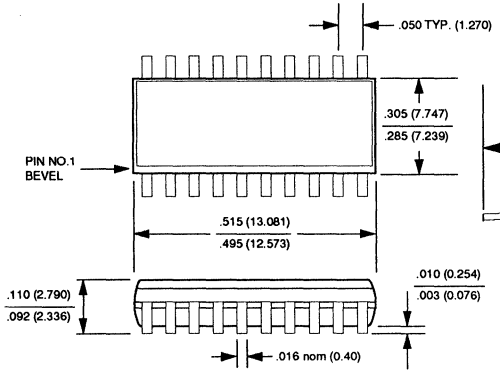
Package Information
(SOL)



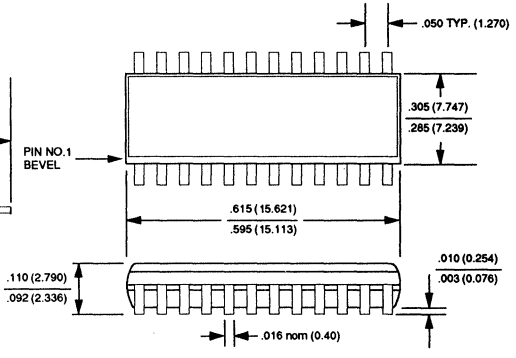
16-Pin SOL



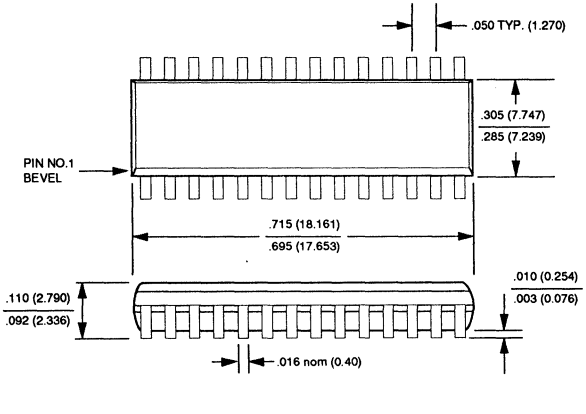
18-Pin SOL



20-Pin SOL

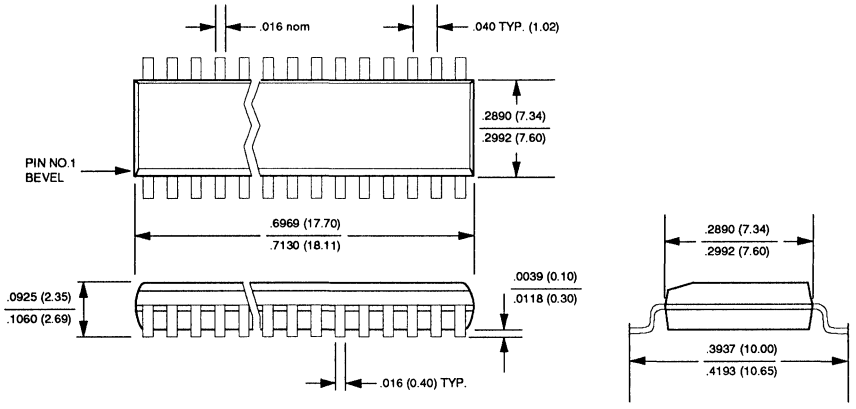


24-Pin SOL

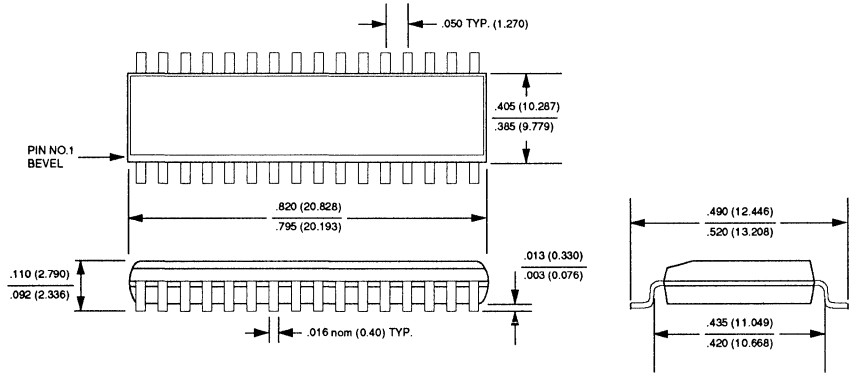


28-Pin SOL

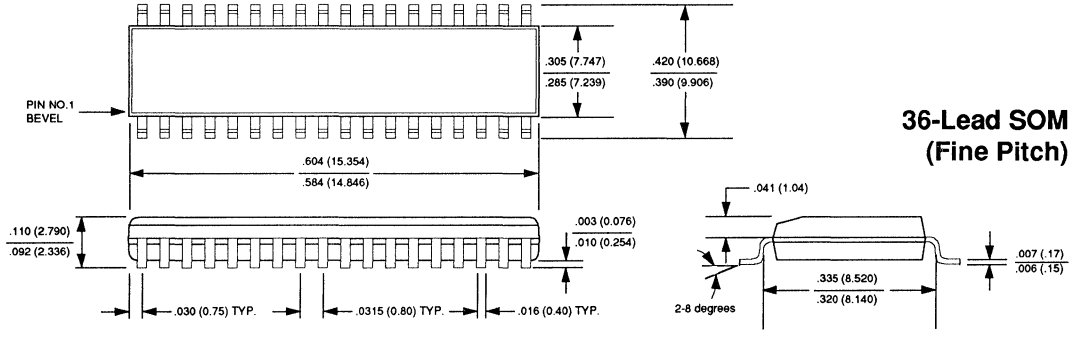
Package Information (SOL/SOM/SOW)



34-Pin SOL

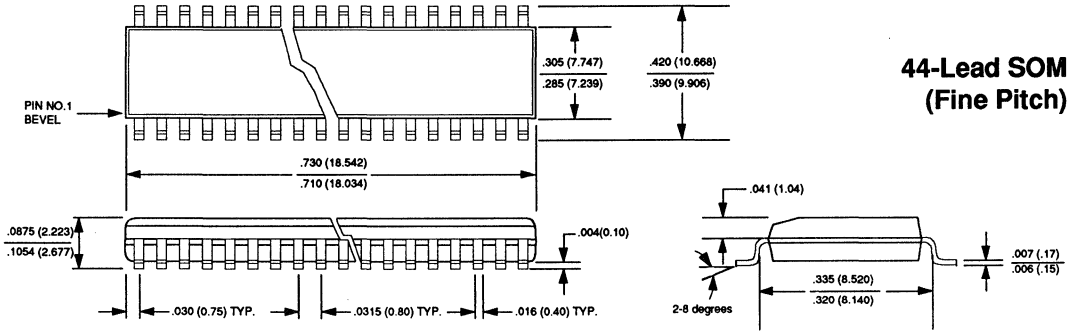


32-Pin SOW

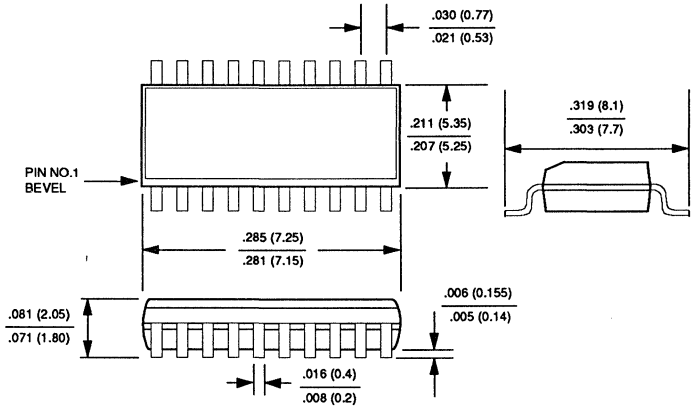


36-Lead SOM (Fine Pitch)

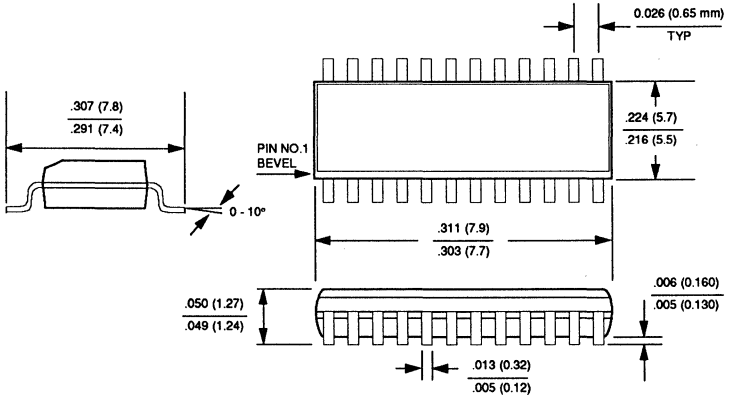
Package Information



44-Lead SOM (Fine Pitch)



20-Pin SOV



24-Pin SOV

Section

SALES OFFICES/ DISTRIBUTORS

North American
Regional Offices & Sales Representatives

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Keith Hively, District Manager
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FAX: (505) 884-2258

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FAX: (801) 484-5408

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FAX: (313) 462-2405

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Itasca
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FAX: (708) 773-2721

INDIANA
Arete Sales, Inc.
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FAX: (219) 420-1440

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FAX: (317) 888-8416

IOWA
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FAX: (319) 377-0958

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FAX: (317) 888-8416

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Trilogy Marketing, Inc.
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FAX: (612) 932-2918

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B. C. Electronics
Bridgeton
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FAX: (314) 344-3180

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