

## Application Note

### 100-kHz switched-mode power supply for 12 V/50 W halogen lamp dimming using low-cost SIPMOS transistors 2 × BUZ 74

A circuit using SIPMOS transistors to supply low-voltage halogen lamps (24 V/ 250 W, 24 V/150 W and 12 V/50 W) has already been published in Siemens Components (1). This was a self-oscillating half bridge circuit as a substitute for a heavy 50-Hz line transformer. As with 50-Hz transformers, the high frequency (120 kHz) approximately sinusoidal lamp voltage was neither regulated nor variable.

In response to a large number of customer enquiries, a new circuit has been developed in which the operating frequency of the switched-mode power supply unit can be varied over a certain range by a potentiometer. This permits lamp dimming from 0 to 100%.

#### Functional description

Figure 1 shows the circuit of the switched-mode power supply (SMPS) for dimming a 12 V/50 W halogen lamp. It comprises a half bridge circuit with its own oscillator.

#### Supply voltage for the drive circuit

When the unit is turned on, the rectified and smoothed line voltage (approx. 300 V) is applied to electrolytic capacitor C 5. The electrolytic capacitor C 10 is slowly charged through the high resistance of R 2. Once the voltage in this capacitor reaches the breakdown voltage of diac D 1, amounting to approx. 24 V, it conducts and a current flows through the diac, resistor R 4 and transistor T 1 into the capacitor C 8, thus charging it. With a voltage of 8 to 10 V applied to C 8, the generator IC 1 and the driver comprising a half circuit with transistors T 2 and T 3 come into operation and the SIPMOS® transistors T 4 and T 5 are driven. As soon as the high frequency AC voltage at the auxiliary winding  $n_2$  of the power transformer Tr2 exceeds 24 V, it is rectified by diode D 4 and applied to the electrolytic capacitor C 10 through the low resistance of R 8. Depending on the lamp brightness setting, this voltage lies between 18 V (at  $f_{\max} = 215$  kHz or  $P_{LP\min} = \text{approx. } 1.5$  W) and 45 V (at  $f_{\min} = 95$  kHz or  $P_{LP\max} = \text{approx. } 46$  W). Should the adjustment range  $P_{LP}$  of 100 to 3% be restricted to 100 to 30%, for example, the voltage at  $f_{\min}$  (95 kHz) applied to C 10 (< 45 V) can be decreased to 30 to 35 V, for example, by reducing the number of turns,  $n_2$  of Tr2, thus reducing the losses in R 3, R 4 and T 1. In the SMPS described here, the cold resistance of the lamp is at least 10 times lower than its hot resistance (lamp at rated power) and the lamp's turn-on current and the drain currents of T 4 and T 5 are approx. 3.5 times higher than normal.

Therefore, the voltage in C 10 can also be 3 to 4 times higher during turning-on than during normal operation. The Z diode D 2 is provided to limit this high turn-on voltage at C 10. In conjunction with R 4 and D 1, the Z diode limits this turn-on voltage to a maximum of 85 V. The lower supply voltage (approx. + 14.5 V) for the drive circuit is derived from the voltage at C 10 (18 V to 45 V during operation) via D 1, R 4 and T 1 and is stabilized by Z diode D 3 in conjunction with R 3 and T 1. To increase the hold current of D 1, resistor R 5 has been connected to the supply voltage ( $V_{CS}$ ), thus ensuring that diac D 1 remains conductive even in the event of 18 V at C 10, and the supply voltage will be maintained in all operating conditions. The voltage drop through the conducting diac (hold voltage  $V_H$ ) is 0.5 V to 1.5 V. Capacitors C6, C7, C9 and C13 are low-inductance metalized polyester types, so the respective voltage across these capacitors hardly have any high frequency AC voltage contributions or spikes.



## Drive circuit

IC 1 is a low-cost standard CMOS IC. It contains a multi-vibrator as oscillator followed by a flipflop. The oscillator frequency corresponds to twice the switching frequency and is determined by the external RC network (R 6, P 1 and C 11). The output signals (pins 10 and 11) have a reasonably accurate duty cycle of 1:1. Adjustment is not necessary. Only one output (pin 10) is used in the circuit shown here. The driver stage consists of the two BC transistors T 2 and T 3, an electrolytic capacitor C 14 and a transformer Tr1.

## Dead time

The output signal of the clock pulse generator IC 1 (pin 10) is fed via a low-pass filter, R 7 and C 12, to the input of the complementary Darlington driver transistors T 2 and T 3. The steep square wave edges from the clock pulse generator are rounded and smoothed by the low-pass filter. Resistors R 9 and R 10 in the secondary circuits of the driver transformer Tr1 and the gate capacitances of the respective SIPMOS transistors also constitute further low-pass filters. In addition R 9 and R 10 prevent the possible generation of partial oscillations and overshoot of gate voltages. These low-pass filters were designed such that the two SIPMOS transistors switch with just the minimum required dead time, i. e. with the longest possible turn-on duration, without simultaneous conduction. The suitably short dead time is not recognizable in Fig. 2a ( $V_{DT5}$ ) because the minimum switching frequency of the power supply is made about 5 kHz higher than the resonance frequency of the oscillator circuit. In other words, with this frequency setting, the oscillator circuit is already slightly inductive and the low dead time leads behind the turn-on and turn-off edges of the drain-source voltages of transistors T 4 and T 5. This lead of the dead time can be seen, for example, from the small reverse component of the T 5 drain current (Fig 2a and 2c). If we chose  $f_{\min} = f_{LCres}$  an exactly symmetrical dead time could be recognized in the  $V_{DT5}$  oscillogram in Fig. 2a (at  $f_{\min}$  setting). Since the frequency of this dimming SMPS supply is always varied individually by the user, depending on the brightness setting, exact agreement of  $f_{\min}$  and  $f_{LCres}$  was not required.

## Driving the SIPMOS transistors

The gate capacitances of T 4 and T 5 are charged and discharged directly by the secondary windings  $n_2$  and  $n_3$  of driver transformer Tr1 via the respective series-connected resistors R 9 and R 10 (Fig. 2a).

## Power transformer, output choke, and oscillator circuit

Transformer Tr2 is a current transformer and its stray inductance  $L_{st}$  is connected in series with the choke inductance ( $L_{ch2}^* = L_{ch2} \times U^2$ ) transformed to the primary side. These two inductances are effective alone on the primary side when  $n_3$  of Tr2 is terminated with a lamp. The total inductance ( $L_{tot} = L_{st} + L_{ch2}^*$ ), effective on the primary side, forms an oscillator circuit with capacitor C 15 during operation with a lamp. Its resonance frequency is determined by  $C_{15}$  and  $L_{tot}$ .

An oscillator circuit Q-factor of approx. 2 was obtained at  $f_{\min} =$  approx. 95 kHz (= 100% load). To reduce the otherwise relatively high inductance of the primary winding  $n_1$ , and thus increase the magnetization current, a transformer core with a 0.16 mm air gap was chosen. This ensures a defined sequence of magnetization and demagnetization in the event of an intentionally reduced load, or even in completely no-load conditions (i. e. defective lamp) and ensure that the edge steepness of the SIPMOS transistors' drain-

source voltage remains almost independent of the load (see  $V_{DT5}$  in Fig. 2a and 3a). These measures, and those described in the section on the dead time, completely prevent simultaneous conduction of the two SIPMOS transistors T4 and T5 in any possible operating state (full load, partial load, no-load, turning-on and short-circuit in the lamp socket).

In the primary winding  $n_1$ , the available window width of the coil former was fully utilized, whereas the whole window width of  $n_2$  and  $n_3$  was not occupied in order to increase the insulation voltage (see winding schematic in Fig. 4).

The voltage at winding  $n_3$  of Tr 2 would be approximately a square-wave (not illustrated) without the choke Ch 2. To smooth this waveform (because of interference emission from the lamp supply leads or the lamp itself) and to make the lamp current and drain currents of T 4 and T 5 sinusoidal (Fig. 2a and 2b), a choke of  $L_{ch2} =$  approx.  $6 \mu\text{H}$  is inserted in the lamp circuit. Fig. 2b shows the voltage at  $n_3$  with Ch 2, the sinusoidal lamp voltage and lamp current. In addition, during turning-on with the lamp cold the choke inductance has a current limiting effect. This also applies in the event of a short circuit in the lamp socket. Due to the high operating frequency and the high  $I_L$  value, the  $L_{ch2}$  value chosen is only  $6 \mu\text{H}$  (for small size and lower losses).

## Operating behavior

### Switching of SIPMOS transistors

Due to the favorable drain-source voltage characteristic and the sinusoidal drain current (at  $P_{LPmax}$  and close to it), the switching performance of transistors T 4 and T 5 is very good (Fig. 2a). The transistors switch with very low edge losses (Fig. 2c).

### No-load

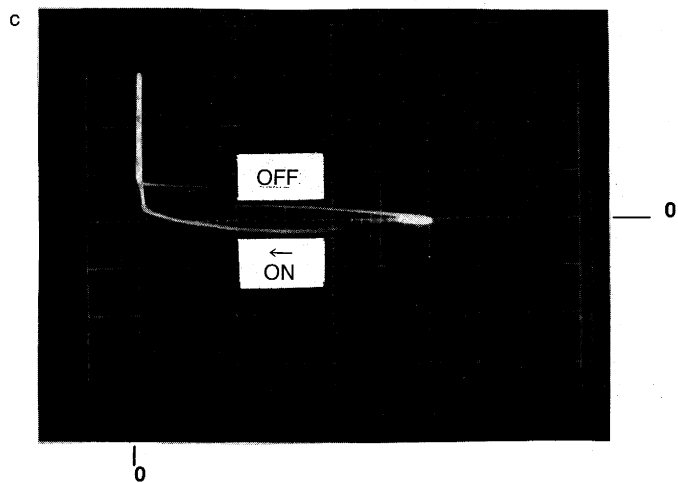
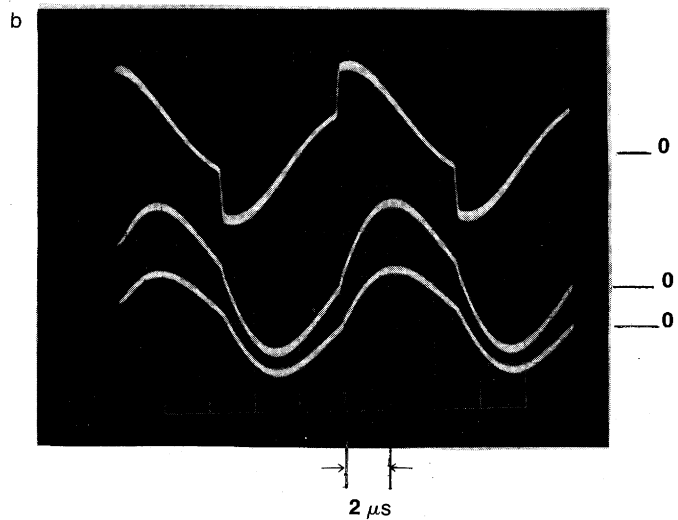
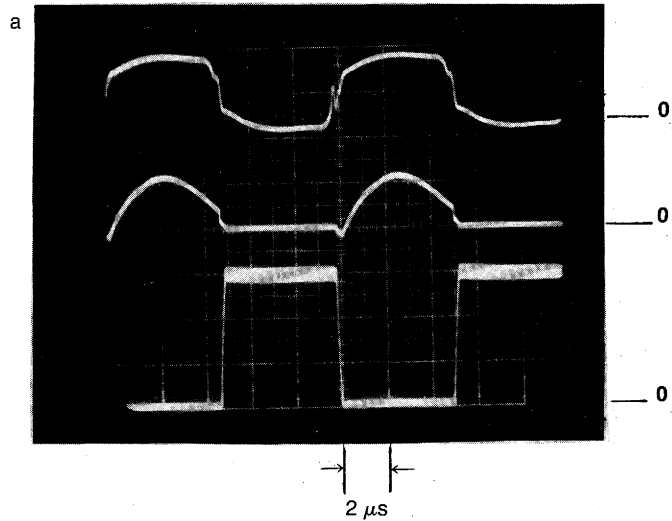
When the lamp is defective (e. g. burnt-out), the output winding  $n_3$  of Tr2 is not loaded and thus runs open-circuit. Now, the primary inductance is too high in relation to loaded operation, despite an air gap in the transformer core. This inductance ( $L \geq 5 \text{ mH}$ ) and the capacitor C 15 ( $C = 3.3 \text{ nF}$ ) cannot constitute a high frequency resonant circuit and thus the operating frequency set by potentiometer P 1 (between 95 and 215 kHz) remains unchanged. The AC voltage at the unloaded winding  $n_3$  now has a square waveform (see Fig 3b) and, depending on the frequency setting, provides 11 to 15 V at the lamp socket.

### Short-circuit

Since the possibility of an accidental short-circuit in the lamp supply leads or socket can never be quite excluded, a slow-blow fuse Si2 is provided on the primary side of the power transformer Tr2 to protect the SIPMOS transistors T 4 and T 5 (without heat sinks) from destruction (Fig. 1). This fuse was chosen such that, during switching-on and in continuous operation, it takes the primary current and only blows after approx. 0.8 s in the event of a complete short-circuit at the output. If such a short-circuit occurs, the drain currents of T 4 and T 5 are approx. 2.5 A when the frequency is set to  $f_{\min}$  ( $\approx P_{LPmax}$ ). Thus, these currents are 4 times higher than during normal operation (Fig. 2a) and are therefore still permissible. A short-circuit is much less harmful at  $f \geq 130 \text{ kHz}$ .

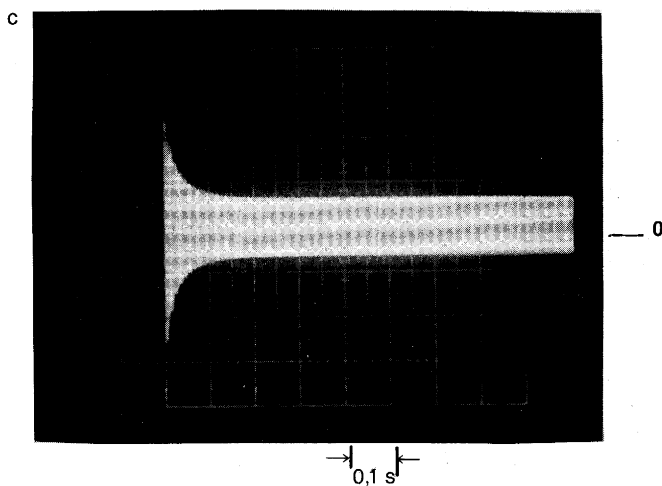
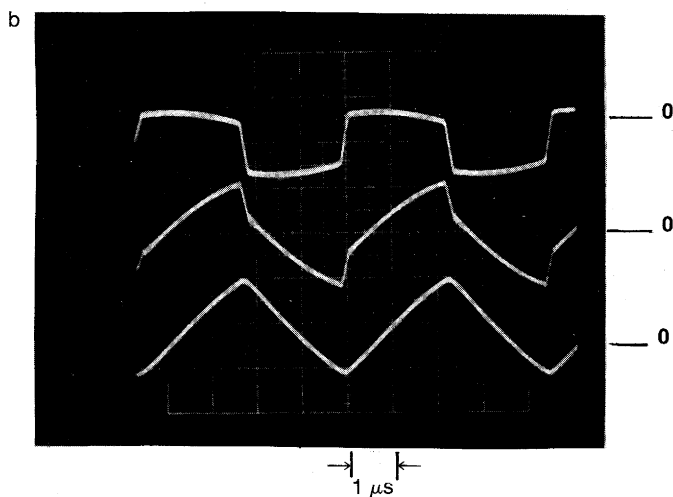
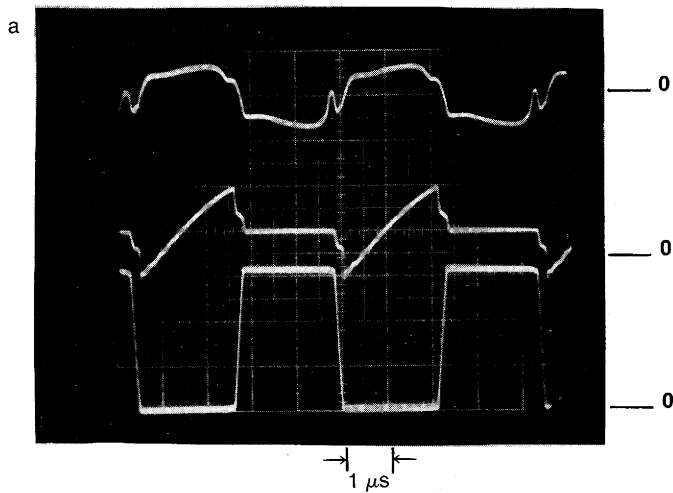
**Figure 2** Oscillograms showing operation of SMPS at maximum brightness setting

- a) top: gate voltage of T5 (10 V/div),  
center: drain current of T5 (0.5 A/div),  
bottom: drain voltage of T5 (100 V/div)
- b) top: voltage through winding  $n_3$  of transformer Tr2 (20 V/div)  
center: lamp voltage (10 V/div)  
bottom: lamp current (5 A/div)
- c) Operating characteristic of transistor T5  
vertical: drain current (0.2 A/div)  
horizontal: drain voltage (50 V/div)

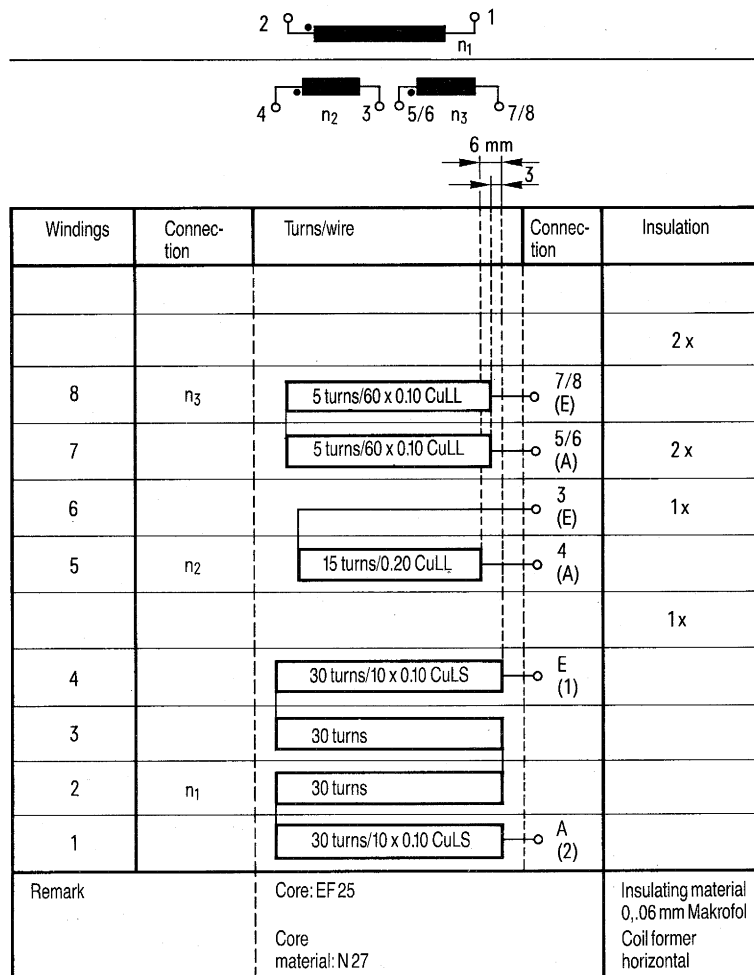


**Figure 3** Oscillograms showing operation of SMPS at minimum brightness setting

- a) top: gate voltage of T5 (10 V/div)  
center: drain current of T5 (0.2 A/div),  
bottom: drain voltage of T5 (100 V/div)
- b) top: voltage through winding  $n_3$  of transformer Tr2 (20 V/div)  
center: lamp voltage (2 V/div),  
bottom: lamp current (2 A/div)
- c) lamp current during turning-on and normal operation (10 A/div)



**Figure 4** Winding and configuration schematic (suggested design 2) for transformer Tr2



## Dimming

As already mentioned, the oscillator frequency and/or switching frequency of the SMPS is determined by an external  $RC$  network. The resistance determining the time was chosen as a partially variable one in the present circuit. The 8.2 k $\Omega$  fixed resistor R 6 is connected in series with P 1. The variable resistor, potentiometer P 1, can be set between 0 and 10 k $\Omega$ . Thus  $R_{tot} = 8.2 \text{ k}\Omega$  to 18.2 k $\Omega$  and  $C_{11} = 120 \text{ pF}$  determine the oscillator, and thus the operating frequency of the SMPS. With the circuit described here, the frequency of the unit can be set continuously as required between 95 and 215 kHz by adjusting P 1. The inductance of choke Ch 2 is 6  $\mu\text{H}$ . Its impedance varies linearly with the operating frequency and, in conjunction with a frequency change of 120 kHz and the tuned circuit Q-factor of 2, a lamp output power range of 50 to 1.5 W  $\approx 100$  to 3% is provided.

This setting range can be reduced or expanded by redesigning the  $RC$  network, but with unchanged values for  $L_{ch2}$  and  $Q$ . The halogen lamp is an ohmic load, but its internal resistance  $R_l$  is very dependent on temperature. If the lamp output is reduced by increasing the operating frequency with P 1, the lamp becomes cooler and its  $R_l$  decreases. This effect is positive and makes (manual) dimming easier and more effective. So a power output adjustment of  $P_{LP} = 50$  to

1.5 W ( $\approx 100$  to 3%) with a 120 kHz frequency change and an oscillator circuit  $Q$  of about 2 is completely adequate. The higher the operating frequency is set by P 1, the more inductive is the oscillator circuit (Fig. 3b to 3c). The chosen operating frequency ( $f_{min} = 95 \text{ kHz}$  at  $P_{LPmax}$ ) is only about 5 kHz higher than the resonance frequency of the oscillator circuit. This 5-kHz difference between the frequencies is naturally greater the higher the operating frequency is set.

## Final remarks

Using SIPMOS transistors, it is possible to devise a simple and very reliable unit with a high operating frequency ( $f_{min} = 95 \text{ kHz}$ ) to supply halogen lamps. The size of the wound components could be kept small because of the high operating frequency. The operating frequency can be varied very simply with a potentiometer, giving an overall adjustment of almost 0 to 100%. Good efficiency, of  $\eta = 88\%$ , is obtained despite the high operating frequency.

**Table 2 Suggested design for 100 kHz SMPS**

Suggested design 1 for Tr.1		Ordering code
Core	: one set of EF 12.6 (N30; ungapped)	B66305-G-X130
Coil former	:	B66202-A1-M1
Yoke	:	B66202-A2001-X
Insulating material	: 0.06 mm Makrofol	
Windings	: $n_1 = 37$ turns/0.15 mm CuLL $n_2 = n_3 = 48$ turns/0.12 mm CuLL	
Winding	: 1. Wind $n_1$ 2. Single insulation 3. Wind $n_2$ 4. Single insulation 5. Wind $n_3$ 6. Double insulation	
Suggested design 2 for Tr.2		Ordering code
Core	: EF 25 (N27) 1 core (ungapped) 1 core (with $0.16 \pm 0.02$ mm air gap $\approx A_L$ approx. 400 nH)	B66317-G-X127  B66317-G160-X127
Coil former	:	B66208-A1003-R1
Yoke	:	B66208-A2001-X
Windings	: $n_1 = 120$ turns/ $10 \times 0.10$ mm CuLS; RF litz wire $n_2 = 15$ turns/0.20 mm CuLL; solid wire $n_3 = 10$ turns/ $60 \times 0.10$ mm CuLL; RF litz wire	
Winding and configuration	: see winding and configuration schematic	
Suggested design 3 for Ch 2		Ordering code
Core	: one set EF 16 (N27; each with a $0.50 \pm 0.05$ mm air gap $\approx A_{Ltot}$ approx. 41 nH)	B66307-G500-X127
Coil former	:	B66308-A1001-T1
Winding	: $n = 12$ turns/ $60 \times 0.10$ mm CuLS; RF litz wire	
$L$ approx. $6 \mu\text{H}$ ( $= 6.3 \mu\text{H}$ )		
The core halves are cemented		

**Table 3 Technical data on 100 kHz SMPS for dimming a 12 V/50 W halogen lamp**

Input AC voltage	$V_{IN} = 220$ V
Lamp voltage	$V_{LP} = 12$ to 1.3 V, variable
Lamp power output	$P_{LP} = 50$ to 1.5 W $\approx 100$ to 3%, variable
Frequency	$f = 95$ to 215 kHz, variable
Efficiency	$\eta$ approx. 88%
Weight	145 g
Ambient temperature	$T_{amb} \leq 60^\circ\text{C}$

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