CMOS LSI



LC895170W

# Preliminary

## **Overview**

The LC895170W is an upwardly compatible version of the LC89517K that supports a larger external buffer RAM capacity and is provided in a more compact package.

# **Functions**

• CD-ROM ECC function, subcode read function, AT interface

# Features

• Support for double-speed operation at a 16.9344 MHz operating frequency Either SRAM (120 ns), DRAM (80 ns), or PSRAM

(85 ns) can be used.

- Support for quad-speed operation at a 33.8688 MF/z operating frequency SRAM (70 ns) must be used.
- On-chip 12-byte output FIFO for sub-CPU to he computer transfers
- On-chip 12-byte input FIFO for host computer to b-CPU transfers
- Subcode data can be written to SRAM by connecting CD-DSP SUB-CODE pin and the sub-CPU the subcode values.
- The sub-CPU can access buffer R .M th. ugh the LC895170W.
- On-chip data transfer function for bullier RAM to baffer RAM transfers
- Pseudo-SRAM (up to 128 ky 1s × 2 bits × 1) can be used.
- DRAM (256 kwords × 4 bits > 2 < 1 Mwords × 4 bits × 2) can be used.

• Transfer speed: 2.8 Mbytes/s (The transfer speed depends the operating frequency.)

CD-ROM Error Correction LSI

• Operating frequencies: 16. `44 N Iz (double speed) or 33.8688 MH7 (quad speed)

# Package Dimonsi

unit: mm

3181, SQFP1



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#### **Block Diagram**



#### LC895170W

#### **Pin Functions**

Ph No. Ph n Type Type   1 RA40 0   2 RA10 0   3 RA11 0   4 RA12 0   5 RA13 0   6 RA41 0   7 RA15 0   8 VSS P   9 100 8   10 K01 8   110 K01 8   121 K03 8   122 K03 8   133 100 8   144 05 8   151 107 8   162 108 8   171 Vop P   172 Vop P   173 Vop P   174 Vop P   175 K04 8   161 107 8   174 Vop P   174 Vop P   175 Vop P   176 K04 8   171 Vop P   172 H07 8   173 K09 P   174 H02 <td< th=""><th></th><th></th><th></th><th>Type: I: Input pin, O: Output pin, B: Bidirectional pin, P: Power supply pin, NC: Unconnected pin</th></td<>				Type: I: Input pin, O: Output pin, B: Bidirectional pin, P: Power supply pin, NC: Unconnected pin
1     RA0     O       2     RA10     O       3     RA11     O       4     RA12     O       5     RA13     O       6     RA14     O       7     RA15     O       8     V35     P       9     OO     B       10     IO1     B       11     IO2     B       12     IO3     B       13     IO4     B       14     IO2     B       15     IO6     B       16     O7     B       17     V00     P       18     V35     P       19     HO0     B       20     HO1     B       14     P     Pull-up resistors on chip       22     HO3     B       24     HO4     B       25     HO5     B       26     HO6     B       27     HO7	Pin No.	Pin	Туре	Function
2     RA10     O       3     RA13     O       4     RM12     O       5     RA13     O       6     RA14     O       7     RA15     O       8     Vsg     P       9     OO     B       10     IO1     B       11     RO2     B       12     RO3     B       13     RO4     B       14     OS     B       15     OA     B       16     Nor,     B       17     Von     B       18     Kor,     B       19     HO0     B       19     HO0     B       21     HO2     B       22     HO1     B       23     Vsg     P       24     HD4     B       25     HO5     B       26     HO6     B       27     HO7     B	1	RA9	0	
3     RA11     0       4     RA12     0       5     RA13     0       6     RA14     0       7     RA15     0       8     V83     P       9     00     R       11     102     R       12     103     R       13     104     R       14     005     R       15     106     R       16     107     R       18     V83     P       19     100     R       19     100     R       19     100     R       21     H02     R       22     100     R       23     V83     P       400     R       22     H02     R       23     V83     P       4003     R       24     H04     R       25     H05     R       26	2	RA10	0	
4     PA12     O     Data buffer RAM address signal outputs       6     RA14     O     Description     Description     Description       7     RA15     O     Description     Description     Description       9     IOO     B     Description     Description     Description       10     IOI     B     Description     Description     Description       11     IO2     B     Description     Description     Description       11     IO2     B     Description     Description     Description       12     IO3     B     Description     Description     Description       13     IO4     B     Description     Description     Description       14     IO5     B     Poli-up resistors on chip     Description     Description       15     IO6     B     Poli-up resistors on chip     Description     Description       16     VSS     P     Poli-up resistors on chip     Description     Description       17     V	3	RA11	0	
S     RA13     O       6     RA14     O       7     RA15     O       8     V <sub>35</sub> P       9     IOO     B       10     IO1     B       11     IO2     B       12     IO3     B       13     IO4     B       14     IO5     B       15     IO7     B       16     IO7     B       17     V <sub>100</sub> P       18     V <sub>35</sub> P       19     IO4     B       20     HD1     B       21     HD2     B       22     HD3     B       24     HD4     B       25     HD5     B       24     HD4     B       25     HD5     B       26     HD7     B       27     HD7     B       28     NC       29     NC       30 </td <td>4</td> <td>RA12</td> <td>0</td> <td>Data buffer RAM address signal outputs</td>	4	RA12	0	Data buffer RAM address signal outputs
6     RA14     0       7     RA15     0       9     IOO     B       9     IOO     B       10     IOI     B       11     IOZ     B       12     IOO     B       13     IOA     B       14     IOS     B       15     IOE     B       16     IOT     B       17     Voc     P       18     VSS     P       19     HDO     B       20     HD1     B       21     HD2     B       22     HD3     B       23     VsS     P       24     HD4     B       25     HD5     B       Pul-up resistors on chip     Pul-up resistors on chip       24     HD4     B       25     HD5     B       Pul-up resistors on chip     Pul-up resistors on chip       24     HD4     B       25	5	RA13	0	
7RA15O8Vs8P9100810101811102812103813104814105815106816107817Vo0P18Vs8P19107820HD1821HD2822HD1823Vs8P24HD2824HD4825HD5826HD6827HD7828Vs8P29Nc29Nc20Nc21HD3822P23Vs8P24HD4825HD5826Nc27HD7828Vs8P29Nc29Nc31Vs8P32Nc33Nc34Nc35Nc36Nc37HO738Nc39Vs8P44Ho445Ho536Nc37Ho738Nc39Nc30Nc31Vs8P32Nc33	6	RA14	0	
8     Vss     P       9     IOO     8       10     IOT     8       11     IOZ     8       12     IOZ     8       13     IOA     8       14     IOS     8       15     IOA     8       14     IOS     8       15     IOA     8       16     IO7     8       17     Vpon     P       18     Vss     P       19     HD0     8       21     HD2     8       22     HB3     8       23     Vss     P       24     HD4     8       25     HD5     8       26     HD5     8       27     HD7     8       28     Vss     P       29     NC     P       20     Vss     P       21     HD5     8       34     NC	7	RA15	0	
9     100     8       10     107     8       11     102     8       12     103     8       13     104     8       14     105     8       15     106     8       16     107     8       177     Vpp     P       18     Vss     P       19     H00     8       20     H01     8       21     H02     8       22     H03     8       23     Vss     P       24     H03     8       25     H05     8       26     H06     8       27     H07     8       28     Vss     P       29     NC     P       21     H07     8       22     H07     8       23     Vss     P       24     H07     8       25     H05     8	8	V <sub>SS</sub>	Р	
10     101     8       11     102     8       11     103     8       13     104     8       14     105     8       14     106     8       14     106     8       16     106     8       16     107     8       17     Vp0     P       18     Vs3     P       19     H00     8       20     H01     8       21     H02     8       22     H03     8       23     Vs3     P       24     H04     8       25     H05     8       91/up resistors on chip     Pulup resistors on chip       24     H04     8       25     H05     8       91/up resistors on chip     Pulup resistors on chip       24     H04     8       25     H05     8       26     H05     9       27 </td <td>9</td> <td>100</td> <td>В</td> <td></td>	9	100	В	
11     IO2     B       12     IO3     B       14     IO5     B       15     IO6     B       16     IO7     B       17     Vp0     P       18     Vg8     P       19     HO0     B       20     HD1     B       21     HO2     B       22     HO3     B       23     Vg8     P       24     HO4     B       25     HO5     B       26     HO6     B       27     HO7     B       28     Vg8     P       29     No     P       21     HO2     B       22     HO3     B       23     Vg8     P       24     HO7     B       25     HO6     B       26     HO6     B       27     HO7     B       28     Vg8     P	10	IO1	В	
12   IO3   B   Data Juffer RAM data signal outputs     13   IO4   B   Delulup resistors on chip     14   IO5   B     15   IO6   B     16   IO7   B     17   Vpb   P     18   Vss   P     19   HO0   B     21   HO2   B     22   HO3   B     24   HO4   B     25   HO5   B     26   HO5   B     27   HO7   B     28   Vss   P     29   HO5   B     21   HO5   B     22   HO5   B     24   HO4   B     25   HO5   B     26   HO5   B     27   HO7   B     28   Vss   P     39   NC   -     30   Vss   P     33   NC   -     34   NC	11	102	В	
13     104     B     Pull-up resistors on chip       14     105     B       15     106     B       16     107     B       17     Vop.     P       18     Vss.     P       19     H00     B       20     H01     B       21     H02     B       22     H03     B       23     Vss.     P       24     H04     B       25     H05     B       26     H05     B       27     H07     B       28     Vss.     P       29     NC     P       21     H05     B       22     H07     B       23     Vss.     P       24     H07     B       25     H05     P       26     NC     NC       27     H07     B       28     Vss     P       2	12	103	В	Data buffer RAM data signal outputs
14     IO5     B       15     IO6     B       16     IO7     B       177     Vpp     P       18     V38     P       18     V9p     B       20     HO1     B       21     HO2     B       22     HO3     B       23     Vss     P       24     HO4     B       25     Vss     P       24     HO4     B       25     Vss     P       26     HO5     B       27     HO7     B       28     Vss     P       29     NC     P       29     NC     P       29     NC     P       20     Vss     P       21     Vss     P       22     NC     P       33     NC     P       34     Vss     P       35     Vss     P	13	IO4	В	Pull-up resistors on chip
15IC6B16IO7B17V <sub>DD</sub> P18V <sub>SS</sub> P19HD0B21HD2B21HD2B22HD3B23V <sub>SS</sub> P24HD4B25HD5B26HD6B27HD7B28V <sub>SS</sub> P29V <sub>SS</sub> P20NC21ND6B22HD5BV <sub>SS</sub> P23V <sub>SS</sub> P24ND6B25HD5BV <sub>SS</sub> P26NC27HD7B28V <sub>SS</sub> P29NC20NC31V <sub>SS</sub> P32NC33NC34In35NC36NC37ENABLE138CMD39V <sub>SS</sub> 40V <sub>SS</sub> 41V <sub>D</sub> 42HWF/143H <sub>D</sub> D44M <sub>D</sub> AT45DFN46STENO47A48F <sub>D</sub> AT49F <sub>D</sub> AT49F <sub>D</sub> AT49F <sub>D</sub> AT40SEDFATC41Hot data transfer mode selection signal input43F <sub>D</sub> ATO44<	14	105	В	
16 $107$ B17 $V_{DD}$ P18 $V_{SS}$ P19HD0B20HD1B21HD2B22HD3B23 $V_{SS}$ P24HD4B25HD5B26HD6B27HD7B28VssP29NC20VssP29NC20VssP20NC21HD7B22MD6B23VssP24HD6B25HD6B26HD6B27HD7B28NC29NC30VssP31VssP32NC33ANC34NC35JAC36VssP37ENABLE148NG39VssP41Vpp-42HWF143HF0044MAT44MAT45JTEN046STEN047Ho348FA149FA144HA144HA145JTEN45JTEN046STEN0 <td< td=""><td>15</td><td>IO6</td><td>В</td><td></td></td<>	15	IO6	В	
17 $V_{DD}$ P18 $V_{SS}$ P19HD0B20HD1B21HD2B22HD3B23 $V_{SS}$ P24HD4B25HD5B26HD6B27HD7B28 $V_{SS}$ P29NC20NC21HD7B23 $V_{SS}$ P24HD6B25HD7B26HD7B27HD7B28 $V_{SS}$ P29NC30 $V_{SS}$ P31 $V_{SS}$ P33P34NC35NC36 $V_{SS}$ P37ENABLE/ 140 $V_{SS}$ P41 $V_{OC}$ 42HW6/I43HE0144 $V_{NT}$ 145JEFN046STEN047EOPC48FA1049NC44 $V_{NT}$ 45STEN046STEN047F048FA1049VaO50SELDFQ/ 140NS50SELDFQ/ 141Ho5 data transfer mode selection signa	16	107	В	
18 $V_{SS}$ P19HD0B20HD1B21HD2B22HD3B23 $V_{SS}$ P24HD4B25HD5B26HD6B27HD7B28 $V_{SS}$ P29NC29NC20VssP29NC20NC30 $V_{SS}$ P31 $V_{SS}$ P33NC34NC35NC36 $V_{SS}$ P37ENABLEI41 $V_{DO}$ P41 $V_{DO}$ P41 $V_{DO}$ P41 $V_{DO}$ P41 $V_{DO}$ P43RFD7I44MR7I45JDTNO46STENO47Host data signal input48RA17O49RA27O49RA27I49RA27I49RA27I40SEEDFRCI41Host data signal input43RFD7I44RA16O45JDTNO46STENO47E anable signal output48RA16O49RA27O49RA27O <td>17</td> <td>V<sub>DD</sub></td> <td>Р</td> <td></td>	17	V <sub>DD</sub>	Р	
19HD0B20HD1B21HD2B22HD3B23VssP24HD4B25HD5B26HD6B27HD7B28VssP29NC29NC30VssP31VssP32NC33NC34NC35NC36Vss37ENABLE38CMD39Vss44NC39Vss44NC30Vss50NC31Vss44NC35P36Vss47ENABLE48KnD49Vss40Vss41Voc42HWF/43HSC44HSC45DTEN46MST47O48RA1649RA1749RA1641Host data signal output43RA1644HSC45DTEN46Atla47Atla48RA1649RA1740Vst data transfer mode selection signal output44RA1645DTEN46Atla47Atla	18	V <sub>SS</sub>	Р	
20     HD1     B     Hot data signals       21     HD2     B     Pull-up resistors on chip       22     HD3     B     Pull-up resistors on chip       23     V <sub>SS</sub> P     Pull-up resistors on chip       24     HD4     B     Pull-up resistors on chip       25     HD5     B     Pull-up resistors on chip       26     HD6     B     Pull-up resistors on chip       27     HD7     B     Pull-up resistors on chip       28     V <sub>SS</sub> P     Pull-up resistors on chip       29     NC     NC     NC       30     V <sub>SS</sub> P     Pull-up resistors on chip       31     V <sub>SS</sub> P     Pull-up resistors on chip       32     NC     NC     Pull-up resistors on chip       34     V <sub>SS</sub> P     Pull-up resistors on chip       35     NC     Pull-up resistors on chip     Pull-up resistors on chip       36     V <sub>SS</sub> P     Pull-up resistors on chip       37     ENABLE     I     Hourc	19	HD0	В	
21     HD2     B     Pull-up resistors on chip       22     HD3     B       23     Vgs     P       24     HD4     B       25     HD5     B       26     HD6     B       27     HD7     B       28     Vgs     P       29     MC     P       29     NC     P       30     Vgs     P       31     Vgs     P       32     NC     P       33     NC     P       34     NC     P       35     MC     P       36     Vgs     P       37     ENABLE     I       38     CMD     I       39     Vgs     P       310     Vgs     P       311     Ngs     P       312     NG     NC       313     Intercent and data standate standa	20	HD1	В	Host data signals
22H03B23 $V_{SS}$ P24H04B25H05B26H06B27H07B28VssP29NC29NC30VssP31VssP33NC34NC35VssP36NC37ENABLENC38CMDNC39VssP30VssNC31VssNC33-NC34NC35VssP36NC37ENABLE140NS38CMD141Vps142HWF143HFD144HFD145DTEN046Arte47O48ArteO49RAtO49RAtO49RAtO40SELDFC141Host data ransfer mode selection signal uiput	21	HD2	В	Pull-up resistors on chip
23 $V_{SS}$ P24HD4B25HD5B26HD6B27HD7B28 $V_{SS}$ P29NCNC29NC31 $V_{SS}$ P33NC34NC35NC36NC37ENABLE40NC38CMD41NC42VSS5P43HC44MQT44MQT45146STEN47448ANAT49AA49RA4740SELDRO41Mode42FO43Host data signal input44MRT45JTEN46STEN47Q48AA4649RA4740VS41Host data signal output43Host Mate signal output44MRTQ45DTENQ46STENQ47Data buffer RAM address signal output48RA46Q49RA47Q40SELDRO141Host data transfer mode selection signal input	22	HD3	В	
24     HD4     B       25     HD5     B       26     HD6     B       27     HD7     B       28     V <sub>SS</sub> P       29     NC       30     V <sub>SS</sub> P       31     V <sub>SS</sub> P       33     NC       34     NC       35     NC       36     V <sub>SS</sub> 7     HO       36     V <sub>SS</sub> 7     NC       36     NC       37     NC       38     CMD       40     NC       38     CMD       40     V <sub>SS</sub> 7     Host data signal input       39     V <sub>SS</sub> 70     P       41     V <sub>DD</sub> 70     Host data virite signal input       42     HVF     I       43     HSO     I       44     JVIAT     J       45     JOT     O </td <td>23</td> <td>V<sub>SS</sub></td> <td>Р</td> <td></td>	23	V <sub>SS</sub>	Р	
25     HD5     B     Hot data signals       26     HD6     B     Pull-up resistors in chip       27     HD7     B       28     V <sub>SS</sub> P       29     NC     NC       30     V <sub>SS</sub> P       31     V <sub>SS</sub> P       32     NC     NC       33     NC     NC       34     NC     NC       35     NC     NC       36     V <sub>SS</sub> P       37     ENABLE     I       40     NC	24	HD4	В	
26HD6BPull-up resistors on chip27HD7B28VssP29NC30VssP31VssP32NC33-NC34NC35-36VssP37ENABLE/38CMD/39VssP39VssP40VssP41VopP42HWFI43Hp544MATO45JTENO46STENO47EOFC48RA16/C49RA17/O40SEDRS/ I41Host data inder signal output42STENO43Hp5I44MATO45JTENO46STENO47EOFC48RA17/O49RA17/O40SEDRS/ I41Host data unifer RAM address signal output42SEDRS/ I43Host data inder signal output44MAT/ O45JTENO46STEN/ O47Host data unifer RAM address signal output48RA17/ O49RA17/ O40SELDRS/ I </td <td>25</td> <td>HD5</td> <td>В</td> <td>Host data signals</td>	25	HD5	В	Host data signals
27HD7B28 $V_{SS}$ P29NCNC30 $V_{SS}$ P31 $V_{SS}$ P32NCNC33-NC34NC-35-NC36VSSP37ENABLEI40 $V_{SS}$ P39 $V_{SS}$ F40 $V_{SS}$ F41 $V_{DD}$ P42HWFI43HFDI44MATD45DTENO46STENO47EOFC48RA16Q49RA17O49RA17O40SELDROI41Host data ransfer mode selection signal output43States enable signal output44MATO45DTENO46STENO47EOFC/48RA16Q/49RA17O49RA17O40SELDROI41Host data transfer mode selection signal input	26	HD6	В	Pull-up resistors on chip
28 $V_{SS}$ P29NCNC30 $V_{SS}$ P31 $V_{SS}$ P32NCNC33NCNC34NC35NC36 $V_{SS}$ P37ENABLE110Notic problem38 $\overline{OMD}$ 140 $V_{SS}$ P41 $V_{DD}$ P42HWR143HEDP44 $WArT$ 045JEEN046STENO47EOPC48RA16O49RA17O41Host data transfer mode selection signal output43STENO44JATAO45STENO46STENO47EOPC'48RA16O'49RA47O49RA47O41Host data transfer mode selection signal output	27	HD7	В	
29NC30 $V_{SS}$ P31 $V_{SS}$ P32NCNC33NC34NC35NC36 $V_{SS}$ P37ENABLE138 $\overline{CMD}$ 139 $V_{SS}$ P40 $V_{SS}$ F41 $V_{DD}$ P43HD44NG/45J46VSST47VDP48 $\overline{MAT}$ O49RA45Q49RA47O41Host data unite signal output43FEN44 $\overline{MAT}$ O45 $\overline{DTEN}$ O46STENO47End of process signal output48 $\overline{RA46}$ Q49 $\overline{RA47}$ O40 $\overline{SELDRO}$ I41Host data transfer mode selection signal outputs	28	V <sub>SS</sub>	Р	
$30$ $V_{SS}$ P $31$ $V_{SS}$ P $32$ NC $32$ NC $33$ NC $34$ NC $34$ NC $35$ NC $36$ $V_{SS}$ $7$ ENABLE $1$ Hu chip select signal input $38$ CMD $1$ $+$ co. nand/data selection signal input $38$ CMD $41$ $V_{DD}$ $41$ $V_{DD}$ $41$ $V_{DD}$ $42$ HWP $1$ Host data virite signal input $43$ HFD $41$ VpD $42$ HWP $1$ Host data virite signal input $43$ HFD $44$ STEN $0$ Jea enable signal output $46$ STEN $0$ Jatu enable signal output $48$ Fr.16 $0$ Data buffer RAM address signal outputs $49$ Fr.17 $0$ Data buffer RAM address signal outputs $50$ SELDRS $1$ Host data ransfer mode selection signal input	29		NC	
31   V <sub>SS</sub> P     32   NC   NC     33   NC     34   NC     35   NC     36   V <sub>SS</sub> 7   ENABLE     1   Hu chip select signal input     38   CMD     7   ENABLE     1   Hu chip select signal input     38   CMD     9   V <sub>SS</sub> 7   ENABLE     1   Hu chip select signal input     38   CMD     1   Hu chip select signal input     39   V <sub>SS</sub> P     40   V <sub>SS</sub> P     41   V <sub>DD</sub> P     42   HWF   1   Host data read signal input     43   HED   1   Host data read signal input     44   W/AT   0   Jala enable signal output     44   STEN   0   Jala enable signal output     45   DTEN   0   Jala buffer RAM address signal output     46   STEN   0   Status enable signal output. Used during DMA data transfers.	30	V <sub>SS</sub>	P	
32NC33NC34NC34NC35AC36VSSP37ENABLE140VSS7F40VSS7P41VDD42HWF143HFO44WAT45JTEN46STEN47EOF48RA4669La buffer RAM address signal outputs49RA4670SELDRS41Host data transfer mode selection signal output	31	V <sub>SS</sub>	P	
33NC34NC35NC36VSS36VSS37ENABLE1He chip select signal input38CMD39VSS40VSS70P41VDD42HWF43HFO44WTIT44WTIT45JTEN46STEN47CO48RA1649RA1749RA1740VSS41Interpretation of the process signal output43USTEN44JTEN45JTEN46STEN47C48RA1649RA1749RA1740VSS data transfer mode selection signal input	32		NC	
34NC35NC36V <sub>SS</sub> P37ENABLE1Hunchip select signal input38CMD1Hunchip select signal input39V <sub>SS</sub> F40V <sub>SS</sub> 741V <sub>DD</sub> P42HWF143HFD144WAIT145DTENO46STENO47EOP48RA16Q49RA17O49SELDRO141Host data ransfer mode selection signal output	33		NC	
35NC36V <sub>SS</sub> P37ENABLEIHu chip select signal input38CMDIt cur nand/data selection signal input39V <sub>SS</sub> F40V <sub>SS</sub> ->41V <sub>DD</sub> P42HWPIHost data vrite signal input43HFDIHost data vrite signal input44/WRITIHost data vrite signal input45DTENOJata enable signal output46STENOJata use label signal output47EOPCEnd of process signal output. Used during DMA data transfers.48RA16OData buffer RAM address signal outputs49RA17OI Host data transfer mode selection signal input	34		NC	
36VSSP37ENABLE1Hu chip select signal input38CMD1Hu chip select signal input39VSSFI40VSS241VDDP42HWP1Host data read signal input43HFO1Host data read signal input44W/IT0Hest vait signal. Can be switched to function as a DRQ signal.45DTEN0Jea enable signal output46STEN0Jataus enable signal output. Used during DMA data transfers.48RA16QData buffer RAM address signal outputs49RA170I Host data ransfer mode selection signal input	35			
37ENABLEIHe chip select signal input38CMDIinterchip select signal input39V <sub>SS</sub> F40V <sub>SS</sub> 741V <sub>DD</sub> P42HWRI43HFDI44 <i>W</i> TiTI45DTENO46STENO47EOP48RA16O49RA17O41Host data transfer mode selection signal output43IDF44IDF45IDF46STEN47EOP48RA1649RA1740ID ta buffer RAM address signal output41Host data transfer mode selection signal input	36	V <sub>SS</sub>	р 1 —	
38CMDII contact contant/data selection signal input39V <sub>SS</sub> F40V <sub>SS</sub> C41V <sub>DD</sub> P42HWRI43HFDI44WAITJ45DTENO46STENO47EOP48RA16O49RA17O41Host data transfer mode selection signal output43HFD44Host data transfer mode selection signal input	37	ENABLE		Hu chip select signal input
39V <sub>SS</sub> H40V <sub>SS</sub> 741V <sub>DD</sub> P42HWF1Host da'a vrite signal input43HED1Host da'a vrite signal input44WAIT0Host vait signal. Can be switched to function as a DRQ signal.45DTEN0Jeta enable signal output46STEN0Status enable signal output48RA16QEnd of process signal outputs49RA170It host data transfer mode selection signal input	38	CMD		co. nand/data selection signal input
40V <sub>SS</sub> 41V <sub>DD</sub> P42HWF1Host data vrite signal input43HED1Host data read signal input44Writ0Host vait signal. Can be switched to function as a DRQ signal.45DTEN0Deta enable signal output46STEN0Status enable signal output7EOFCEnd of process signal output. Used during DMA data transfers.48RA16OData buffer RAM address signal outputs50SELDROIHost data transfer mode selection signal input	39	V <sub>SS</sub>	H H	
41   V <sub>DD</sub> P     42   HWP   1   Host data write signal input     43   HED   1   Host data read signal input     44   W/IT   0   Host vait signal. Can be switched to function as a DRQ signal.     45   //TEN   0   Jeta enable signal output     46   STEN   0   /status enable signal output     47   EOF   C   End of process signal output. Used during DMA data transfers.     48   RA16   O   Data buffer RAM address signal outputs     49   RA17   O   Data buffer RAM address signal input     50   SELDHO   I   Host data transfer mode selection signal input	40	V <sub>SS</sub>		
42   HWH   Host data yinte signal input     43   HED   I   Host data read signal input     44   W/AT   D   Host vait signal. Can be switched to function as a DRQ signal.     45   /DTEN   O   De a enable signal output     46   STEN   O   Status enable signal output     47   EOP   C/   End of process signal output. Used during DMA data transfers.     48   RA16   O   Data buffer RAM address signal outputs     49   RA17   O   I Host data transfer mode selection signal input	41	V <sub>DD</sub>	<u>Р</u>	
43   HFD   I   Host data read signal input     44   WAIT   D   Host vait signal. Can be switched to function as a DRQ signal.     45   DTEN   O   Deta enable signal output     46   STEN   O   Status enable signal output     7   EOF   C   End of process signal output. Used during DMA data transfers.     48   RA16   O   Data buffer RAM address signal outputs     49   RA17   O   I     50   SELDRO   I   Host data transfer mode selection signal input	42			Host da'a virite signal input
44   W/11   0   Host wait signal. Can be switched to function as a DRQ signal.     45   // TEN   0   Deta enable signal output     46   STEN   0   Status enable signal output     7   EOP   C   End of process signal output. Used during DMA data transfers.     48   RA16   O   Data buffer RAM address signal outputs     49   RA17   O   Interference and transfer mode selection signal input     50   SELDRO   I   Host data transfer mode selection signal input	43			Host data read signal input
45   DTEN   O   Data enable signal output     46   STEN   O   Status enable signal output     7   EOP   C   End of process signal output. Used during DMA data transfers.     48   RA16   O   Data buffer RAM address signal outputs     50   SELDRO   I   Host data transfer mode selection signal input	44		⊥ /	Host wait signal. Can be switched to function as a DRQ signal.
40   STEIN   O   Status enable signal output     7   EOP   C   End of process signal output. Used during DMA data transfers.     48   RA16   O   Data buffer RAM address signal outputs     49   RA17   O   Data buffer RAM address signal outputs     50   SELDRO   I   Host data transfer mode selection signal input	45			Joz a enable signal output
V EOP C End of process signal output. Used during DMA data transfers.   48 RA16 O Data buffer RAM address signal outputs   49 RA17 O Data buffer RAM address signal outputs   50 SELDRO I Host data transfer mode selection signal input	46	SIEN		potatus enable signal output
48 HA10 O   49 RA17 O   50 SELDRO I   Host data transfer mode selection signal input			+	End of process signal output. Used during DMA data transfers.
49 HFU/ U   50 SELDRO I Host data transfer mode selection signal input	48	HA16		Data buffer RAM address signal outputs
DU SELURE I Host data transfer mode selection signal input	49			
	50	SELDHU		

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#### Continued from preceding page.

Din Mo	Din	Turne	Type: I: Input pin, O: Output pin, B: Bidirectional pin, P: Power supply pin, NC: Unconnected pin
PIN NO.		Туре	
51	RD	 	Microprocessor data read signal input
52	WR		Microprocessor data write signal input
53	CS	1	Chip select signal input (from microprocessor)
54	RS		Register selection signal
55	V <sub>DD</sub>	Р	
56	V <sub>SS</sub>	P	
57	D0	В	
58	D1	В	
59	D2	В	
60	D3	В	Microprocessor data signals
61	D4	В	Pull-up resistors on chip
62	D5	В	
63	D6	В	
64	D7	В	
65	V <sub>SS</sub>	Р	
66	INT	0	Interrupt request signal output (to the microplocessor) Open-drain output with on-chip pull-up resistor
67	SWAIT	0	Sub-CPU wait signal
68	TEST0	I	
69	TEST1	I	
70	TEST2	I	lest inputs should be tied low in normal operation.
71	TEST3	I	
72	EXCK	0	
73	WFCK	I	
74	SBSO	I	Subcode I/O pins
75	SCOR	I	
76	V <sub>DD</sub>	Р	
77	SDATA	I	Serial data input
78	BCK	I	Serial data ir put cloc'r
79	LRCK	I	44.1 kHz strobe signal t
80	C2PO	I	C2 roir ter input
81	V <sub>SS</sub>	Р	
82	XTALCK	I.	Crystal oshille circe input
83	XTAL	0	Crystal sillator ci. it output
84	MCK	S	XTA <sup>1</sup> -oK-div. ٦-by-2 outpu
85	RESET		Reset. 'ne LC895170W is ruset on a low level input.
86	RCS	0	n vrom, ett
87	RWE	0	TAM the signal
88	ROE	C	RAI, tata read signal
89	V <sub>DD</sub>	P	
90	V <sub>SS</sub>	P	
91	RA0	<u> </u>	
92	RA1		
93	F.A?.		
94	F.A3	0	Data buffer BAM address signals output
95	RA4	0	
93	RA5	0	
97	PA6	0	
98	RA7	5	
99	V <sub>SS</sub>	Р	
100	RA8	0	Data buffer RAM address signal output.

# Specifications

#### Absolute Maximum Ratings at $V_{SS} = 0$ V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V <sub>DD</sub> max	Ta = 25°C	-0.3 to +7.0	V
I/O voltages	VIVO	Ta = 25°C	–0.3 to V <sub>DD</sub> + 0.3	V
Allowable power dissipation	Pd max	Ta ≤ 70°C	350	mW
Operating temperature	Topr		–30 to ∿70	°C
Storage temperature	Tstg		-55 to +125	°C
Soldering thermal stress limit (pins only)		10 seconds	260	°C

#### Allowable Operating Ranges at Ta = -30 to $+70^{\circ}C$ , $V_{SS} = 0$ V

Allowable Operating Ranges at Ta = $-30$ to $+70^{\circ}$ C, V <sub>SS</sub> = 0 V							
Parameter	Symbol	Conditions		min	Чт.	max	Unit
Supply voltage	V <sub>DD</sub>			5	5.0	5.5	V
Input voltage range	V <sub>IN</sub>			0		V <sub>DD</sub>	V

# DC Characteristics at Ta = -30 to $+70^{\circ}$ C, V<sub>SS</sub> = 0 V, V<sub>DD</sub> = 4.5 to 5.5 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Input high level voltage	V <sub>IH1</sub>	All input pipe other than (1) and (T) I CK				V
Input low level voltage V <sub>IL1</sub>		All input pins other than (1) and ALALOK			0.8	V
Input high level voltage	V <sub>IH2</sub>	RESET, all bus pins (HRD, HV/R, ENABLE, 0, RD,	2.5			V
Input low level voltage	V <sub>IL2</sub>	CS, WR, WFCK, SBSO, SCOR) (1)			0.6	V
Output high level voltage	V <sub>OH1</sub>	$I_{OH1} = -2$ mA: All output runs (incluoi. $r_{3}$ pins) other than (2) and X7.A'_CK	2.4			v
Output low level voltage	V <sub>OL1</sub>	I <sub>OL1</sub> = 2 mA: All cutrut pins ( <sup>2</sup> ing bus pins) other than (2) and XTALCK			0.4	V
Output low level voltage	V <sub>OL2</sub>	$I_{OL2} = 2 \text{ mA}: \overline{N^{T}}$ (on-chi pun resi jr, open ara'n) (2)			0.4	V
Output high level voltage	V <sub>OH3</sub>	I <sub>OH3</sub> = -6 .nA.: HD0 tr .D7	2.4			V
Output low level voltage	V <sub>OL3</sub>	I <sub>OL3</sub> = € mA: HD0 to h⊾			0.4	V
Input leakage current	١L	$V_{I} = V_{SS}, V_{DD}$ : All in <sub>F</sub> pins	-25		+25	μA
Pull-up resistance	R <sub>UP</sub>	Al/bi.s pins, Il	40	80	160	kΩ

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