

# CD-ROM Error Correction LSI

with Built-In SCSI Interface

# Preliminary

## **Overview**

The LC89512W integrates a real-time error correction circuit and a SCSI interface in a single chip.

## **Functions**

• CD-ROM error correction function, subcode readout function, SCSI interface

## **Features**

• Support for double-speed drives at an operating frequency of 16.9344 MHz Either SRAM (120 ns), DRAM (80 ns) or pseudo

SRAM (85 ns) can be used.

• Support for quad-speed drives at an operating frequency of 33.8688 MHz

SRAM (70 ns) must be used.

- Built-in SCSI interface with built-in 48 mA sink buffer (Only the TARGET function is supported.)
- Built-in 12-byte output FIFO for sub-CPU to host computer data transmission
- Built-in 12-byte input FIFO for host computer to sub-CPU data transmission
- Subcode data can be written to buffer RAM and the sub-CPU can read the subcode values by connecting the LC89512 to the CD-DSP subcode pin.
- Sub-CPU access of buffer RAM through the LC89512
- Built-in function for buffer RAM internal data transfer
- Pseudo-SRAM (128-kword × 8-bit and smaller) can be used.
- DRAM (two 256-kword × 4-bit chips or two 1-Mword × 4-bit chips) can be used.
- Transfer speeds:

2.8 MB/second (asynchronous mode) (for CD-ROM decode only operation)

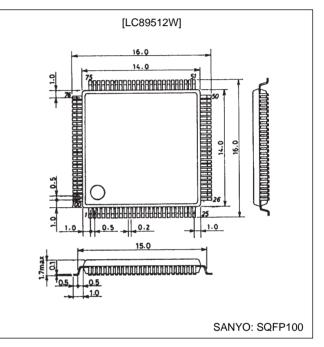
4.2 MB/second (synchronous mode) (CD-ROM decode operation is not supported in synchronous mode)Both of these transfer modes use a 16.9344 MHz clock. (The transfer speed depends on the frequency used.)

• Operating frequencies: 16.9344 MHz (up to double speed), 33.8688 (quad speed)

# **Package Dimensions**

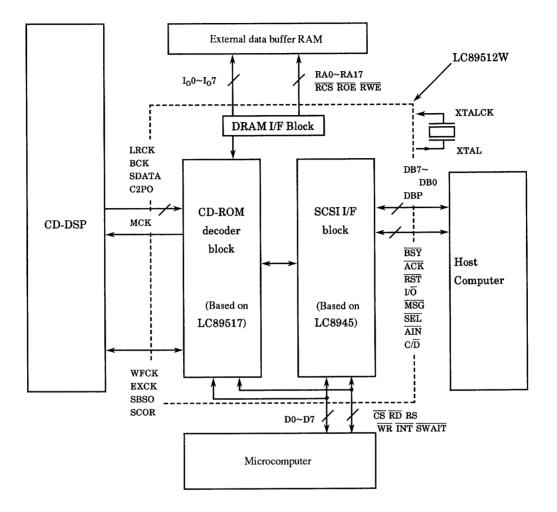
unit: mm

#### 3181A-SQFP100



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### **Block Diagram**



#### **Pin Functions**

u	nctions		Type: I: Input pin, O: Output pin, B: Bidirectional pin, P: Power supply pin, NC: No connection pin
	Pin	Туре	Function
	DB7	В	SCSI connection
	V <sub>SS</sub> 1	Р	
	DBP	В	SCSI connection
	ATN	В	SCSI connection
	V <sub>SS</sub> 1	Р	
	BSY	В	SCSI connection
	ACK	В	SCSI connection
	V <sub>SS</sub> 1	Р	
	RST	В	SCSI connection
	MSG	В	SCSI connection
	V <sub>SS</sub> 1	Р	
	SEL	В	SCSI connection
	C/D	В	SCSI connection
	V <sub>SS</sub> 1	Р	
	REQ	В	SCSI connection
	I/O	В	SCSI connection
	V <sub>SS</sub> 0	Р	
	I <sub>O</sub> 0	В	
	l <sub>O</sub> 1	В	
	l <sub>O</sub> 2	В	
	I <sub>O</sub> 3	В	Data buffer RAM data signals
	I <sub>O</sub> 4	В	These pins have built-in pull-up resistors.
	I <sub>O</sub> 5	В	
	I <sub>O</sub> 6	В	
	l <sub>0</sub> 7	В	
	ĪNT1	0	SCSI block interrupt request signal output (set using a register)
	V <sub>SS</sub> 0	Р	
	V <sub>SS</sub> 0	Р	
	D0	В	
	D1	В	
	D2	В	
	D3	В	Microprocessor data signals These pins have built-in pull-up resistors.
	D4	В	These pins have built-in pull-up resistors.
	D5	В	
	D6	В	
	D7	В	
	ĪNT0	0	Microprocessor interrupt request signal output
	XTALCK	I	Crystal oscillator circuit input
	XTAL	0	Crystal oscillator circuit output
	V <sub>SS</sub> 0	Р	
	V <sub>DD</sub>	Р	
	RA0	0	
	RA1	0	
	RA2	0	
	RA3	0	
	RA4	0	
_			

Data buffer RAM address signal outputs

RA5

RA6

RA7

RA8

RA9

RA10

RA11

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Pin No.	Pin	Туре	Function			
54	RA12	0				
55	RA13	0				
56	RA14	0				
57	RA15	0	Data buffer RAM address signal outputs			
58	RA16	0				
59	RA17	0				
60	V <sub>DD</sub>	P				
61	V <sub>SS</sub> 0	Р				
62	RESET	1	Reset			
63	TEST1	I				
64	TEST2	I	t inputs. These pins should be tied low in normal operation.			
65	TEST3	I	· · ·			
66	WFCK	I				
67	SBSO	I	Subcode I/O			
68	SCOR	I				
69	SDATA	I	Serial data input			
70	BCK	I	Serial data input clock			
71	LRCK	I	44.1 kHz strobe signal input			
72	C2PO	I	C2 pointer input			
73	RD	I	Microprocessor data read signal input			
74	WR	I	Microprocessor data write signal input			
75	CS	I	Chip select signal input (from the microprocessor)			
76	RS	I	Register selection signal input			
77	V <sub>SS</sub> 0	Р				
78	SWAIT	0	Sub-CPU wait signal			
79	EXCK	0	Sub code I/O			
80	MCK	0	Crystal oscillator frequency output			
81	TEST0	I	Test inputs. These pins should be tied low in normal operation			
82	RCS	0	RAM chip select			
83	RWE	0	RAM data write signal output			
84	ROE	0	RAM data read signal output			
85		NC				
86		NC				
87		NC				
88		NC				
89	V <sub>DD</sub>	Р				
90	V <sub>SS</sub> 1	Р				
91	DB0	В	SCSI connection			
92	DB1	В	SCSI connection			
93	V <sub>SS</sub> 1	Р				
94	DB2	В	SCSI connection			
95	DB3	В	SCSI connection			
96	V <sub>SS</sub> 1	Р				
97	DB4	В	SCSI connection			
98	DB5	В	SCSI connection			
99	V <sub>SS</sub> 1	Р				
100	DB6	В	SCSI connection			

Type: I: Input pin, O: Output pin, B: Bidirectional pin, P: Power supply pin, NC: No connection pin Note: 1. NC must be left open. Do not connect any signals to these pins. 2. V<sub>SS</sub>0 is the logic system ground and V<sub>SS</sub>1 is the SCSI interface ground. (from the standard cell version)

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# **Specifications**

#### Absolute Maximum Ratings at $V_{SS} = 0 V$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V <sub>DD</sub> max	Ta = 25°C	-0.3 to +7.0	V
I/O voltages	V <sub>I</sub> V <sub>O</sub>	Ta = 25°C	–0.3 to V <sub>DD</sub> + 0.3	V
Allowable power dissipation	Pd max	Ta ≤ 70°C	350	mW
Operating temperature	Topr		-30 to +70	°C
Storage temperature	Tstg		-55 to +125	°C
Soldering thermal stress limit (pins only)		10 seconds	260	°C

#### Allowable Operating Ranges at Ta = -30 to $+70^{\circ}$ C, V<sub>SS</sub> = 0 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V <sub>DD</sub>		4.5	5.0	5.5	V
Input voltage range	V <sub>IN</sub>		0		V <sub>DD</sub>	V

#### DC Characteristics at Ta = -30 to $+70^{\circ}$ C, V<sub>SS</sub> = 0 V, V<sub>DD</sub> = 4.5 to 5.5 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Input high level voltage	V <sub>IH</sub> 1	All input pipe other than (1) (2) and VTALCK	2.2			V
Input low level voltage	V <sub>IL</sub> 1	All input pins other than (1), (3), and XTALCK			0.8	V
Input high level voltage	V <sub>IH</sub> 2	$\overline{\text{RESET}}$ , I <sub>O</sub> 0 to I <sub>O</sub> 7, D0 to D7, $\overline{\text{RD}}$ , $\overline{\text{CS}}$ , $\overline{\text{WR}}$ , WFCK,	2.5			V
Input low level voltage	V <sub>IL</sub> 2	SBSO and SCOR(1)			0.6	V
Input high level voltage	V <sub>IH</sub> 3	ACK ATN and the input pipe (2)	2.0			V
Input low level voltage V <sub>IL</sub> 3		ACK, ATN and the input pins (3)			0.8	V
Output high level voltage	V <sub>OH</sub> 1	$I_{OH}$ 1 = -3 mA: $I_O$ 0 to $I_O$ 7, D0 to D7 and all output pins other than (2), (3) and XTALCK	2.4			V
Output low level voltage	V <sub>OL</sub> 1	$I_{OL}$ 1 = 3 mA: $I_O$ 0 to $I_O$ 7, D0 to D7 and all output pins other than (2), (3) and XTALCK			0.4	V
Output low level voltage	V <sub>OL</sub> 2	I <sub>OL</sub> 2 = 3 mA: INT1 and INT0 (pull-up resistor open drain) (2)			0.4	V
Output low level voltage	V <sub>OL</sub> 3	$I_{OL}3 = 48 \text{ mA: }\overline{\text{DB0}} \text{ to }\overline{\text{DB7}}, \overline{\text{DBP}}, \overline{\text{BSY}}, I/O, \overline{\text{MSG}}, \overline{\text{SEL}}, \overline{\text{RST}}, \overline{\text{REQ}}, C/D (2)$			0.4	V
Input leakage current	١L	$V_{I} = V_{SS}, V_{DD}$ : All input pins	-25		+25	μA
Pull-up resistance	R <sub>UP</sub>	$I_0$ to $I_0$ 7, D0 to D7, $\overline{INT1}$ and $\overline{INT0}$	40	80	160	kΩ

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