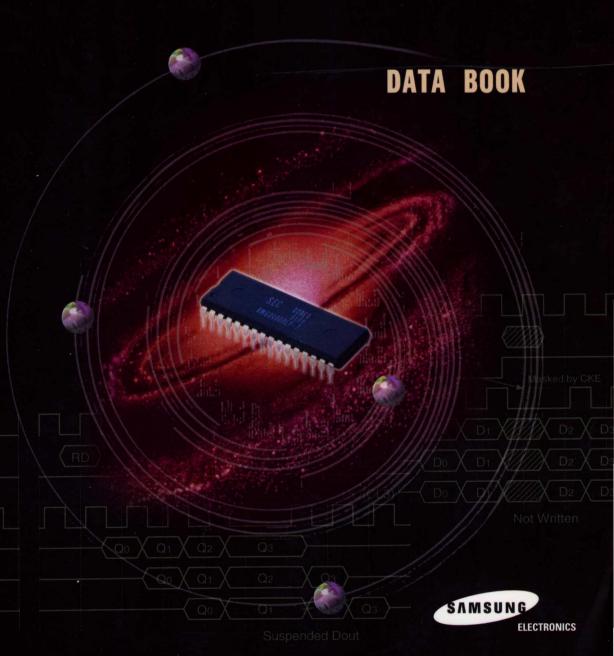
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308, 357, 402	" NOTE: Above test conditions are ~ " below TEST CONDITIONS	Remove "NOTE: Above test conditions are ~" below TEST CONDITIONS				
411, 439, 467	Blank below TEST CONDITIONS	Add "NOTE: Above test conditions are also applied at industrial temperature range" below TEST CONDITIONS				
411, 439, 467	Blank below READ CYCLE	Add " NOTE: Above parameters are also guaranteed at industrial temperature range" below READ CYCLE				
412, 440, 468	Blank below WRITE CYCLE	Add "NOTE: Above parameters are also guaranteed at industrial temperature range" below WRITE CYCLE				
932, 941, 950	DC ELECTRICAL CHARACTERISTICS Standby Current, ISB1, Test conditions: f=Max, 100% Duty, Device deselected, ~	DC ELECTRICAL CHARACTERISTICS Standby Current, Iss1, Test conditions: f=0 MHz, Device deselected, ~				

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A-1. SYNCHRONOUS PIPELINE BURST TRUTH TABLE(Data field)

CCS	ECS	ADSP	CADS	CADV	WRITE	K	Address Accessed	Operation
Н	X*	Х	L	X	Х	••	· N/A	Not Selected
L	Н	L	X	X	X	••	N/A	Not Selected
L	Н	X	L	X	Х	••	N/A	Not Selected
L	L	L	Х	X	Х	••	External Address	Begin Burst Read Cycle
L	L	Н	L	X	L	••	External Address	Begin Burst Write Cycle
L	L	Н	L	Х	Н	••	External Address	Begin Burst Read Cycle
Х	X	Н	Н	L	Н	••	Next Address	Continue Burst Read Cycle
Н	Х	Х	Н	L	Н	••	Next Address	Continue Burst Read Cycle
Х	Х	Н	Н	L	L	••	Next Address	Continue Burst Write Cycle
Н	Х	Х	Н	L	L	••	Next Address	Continue Burst Write Cycle
Х	Х	Н	Н	Н	Н	••	Current Address	Suspend Burst Read Cycle
Н	Х	Х	Н	Н	Н	••	Current Address	Suspend Burst Read Cycle
х	х	Н	Н	Н	L	••	Current Address	Suspend Burst Write Cycle
Н	Х	Х	Н	Н	L	••	Current Address	Suspend Burst Write Cycle

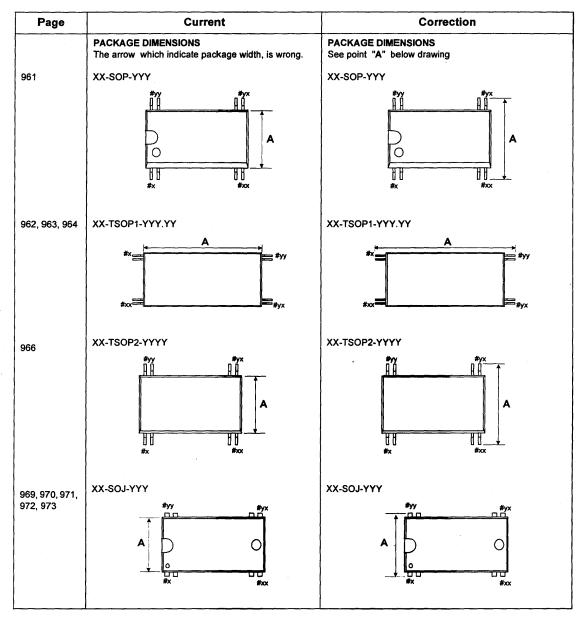
Page	Current	Correction
930, 939, 948	A-1. SYNCHRONOUS PIPELINE BURST TRUTH TABLE(Data field), 512KB Single Bank Module KMM764V72G2,KMM764V72G7, KMM764V75G	Refer to below table

A-1. SYNCHRONOUS PIPELINE BURST TRUTH TABLE(Data field)

CCS	ADSP	CADS	CADV	WRITE	K	Address Accessed	Operation
Н	X	L	х	Х	••	N/A	Not Selected
Н	L	Х	Х	X	•• N/A		Not Selected
L	L	Х	X	X	••	External Address	Begin Burst Read Cycle
L	Н	L	Х	L	••	External Address	Begin Burst Write Cycle
L	Н	L	х	Н	••	External Address	Begin Burst Read Cycle
Х	Н	Н	L	н	••	Next Address	Continue Burst Read Cycle
Н	X	Н	L	Н	••	Next Address	Continue Burst Read Cycle
х	Н	Н	L	L	••	Next Address	Continue Burst Write Cycle
Н	X	Н	L	L	••	Next Address	Continue Burst Write Cycle
X	Н	Н	Н	Н	••	Current Address	Suspend Burst Read Cycle
Н	X	Н	Н	Н	••	Current Address	Suspend Burst Read Cycle
X	Н	Н	Н	L	••	Current Address	Suspend Burst Write Cycle
Н	Х	Н	Н	L	••	Current Address	Suspend Burst Write Cycle

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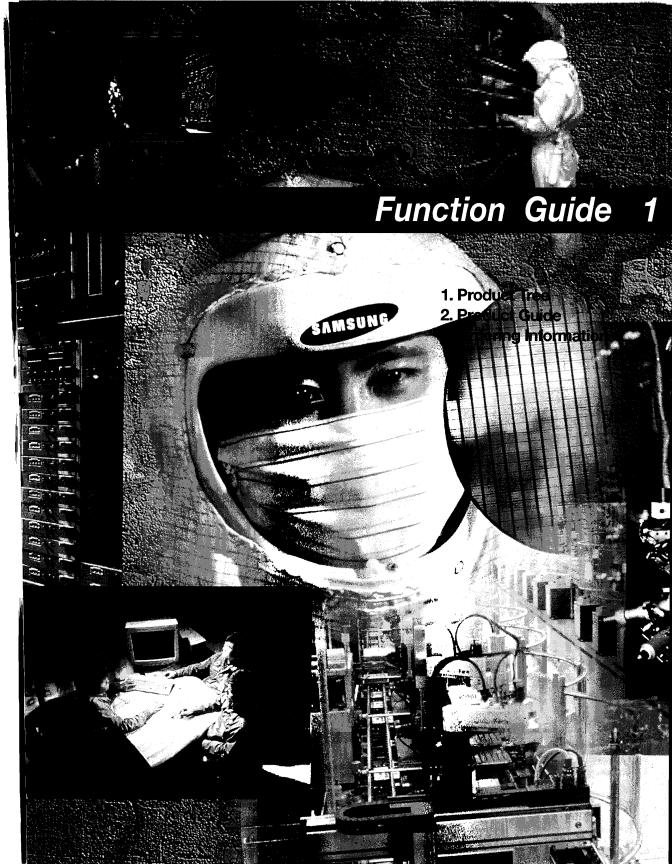
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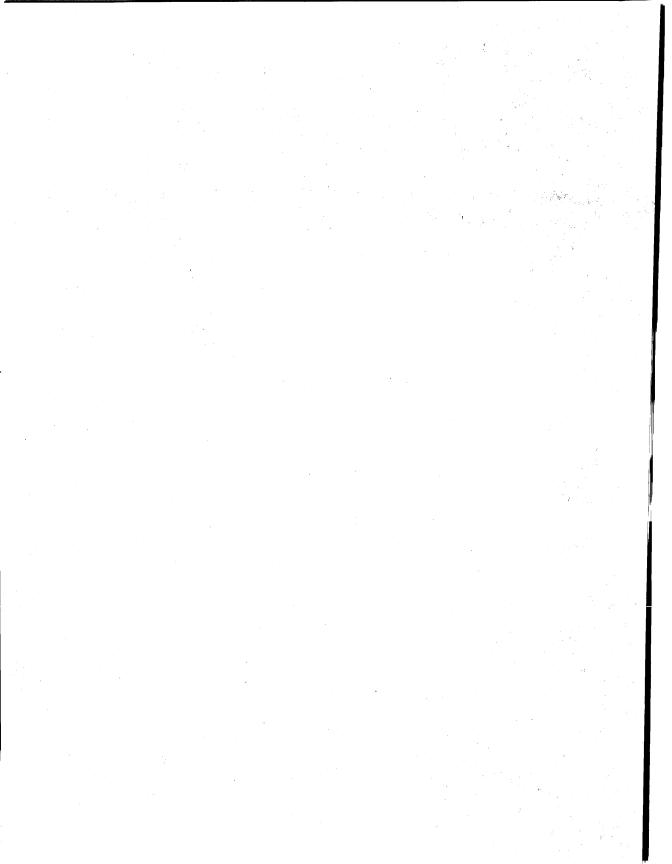
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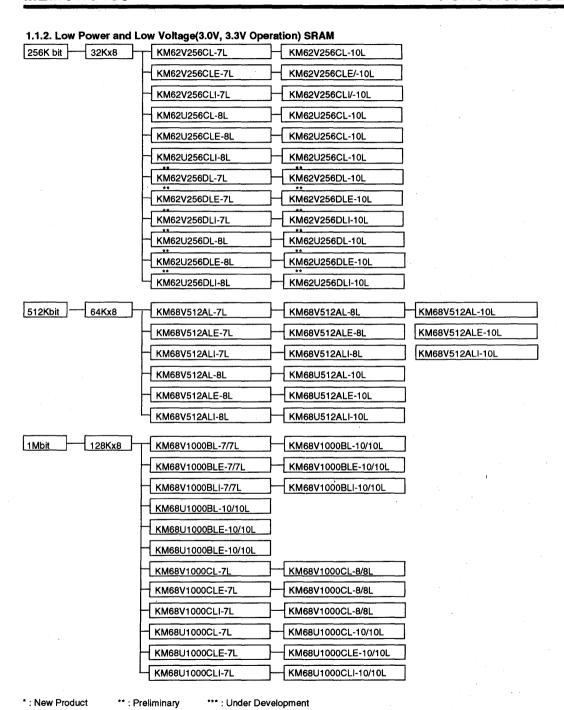
1. SRAM PRODUCT TREE

1.1.1. Low Power(5.0V Operation) SRAM 256K bit KM62256CL-7/7L 32Kx8 KM62256CL-4/4L KM62256CL-5/5L KM62256CLI/-7/7L KM62256CLI/-10/10L KM62256DL-5/5L KM62256DL-7/7L KM62256DLI/-7/7L KM62256DLI/-10/10L 64Kx8 512K bit KM68512AL-4/4L KM68512AL-5/5L KM68512AL--7/7L KM68512ALI-7/7L KM68512ALI-10/10L 128Kx8 KM681000BL-5/5L KM681000BL-7/7L 1Mbit KM681000BLE-7/7L KM681000BLE-10/10L KM681000BLI-7/7L KM681000BLI-10/10L KM681000CL-4/4L KM681000CL-5/5L KM681000CL-7/7L KM681000CLI-5/5L KM681000CLI-7/7L KM681000CLI-10/10L 64Kx16 KM6161000BL-5/5L KM6161000BL-7/7L KM6161000BLI-7/7 KM6161000BLI-10/10L 4Mbit 512Kx8 KM684000AL-5/5L KM684000AL-7/7L KM684000ALI-7/7L KM684000ALI-10/10L KM684000BL-5/5L KM684000BL-7/7L KM684000BLI-7/7L KM684000BLI-10/10L 256Kx16 KM6164000BL-5/5L KM6164000BL-7/7L KM6164000BLI-7/7I KM6164000BLI-10/10L



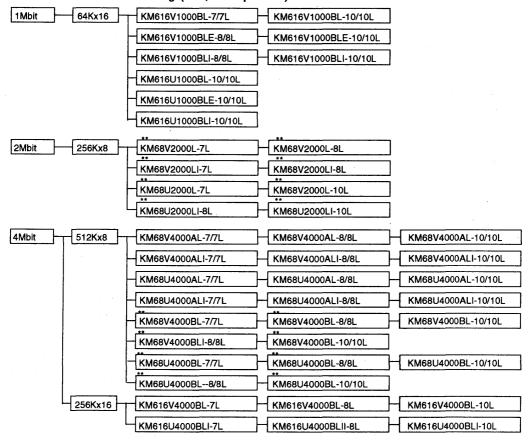
^{** :} Preliminary







1.1.2. Low Power and Low Voltage(3.0V, 3.3V Operation) SRAM

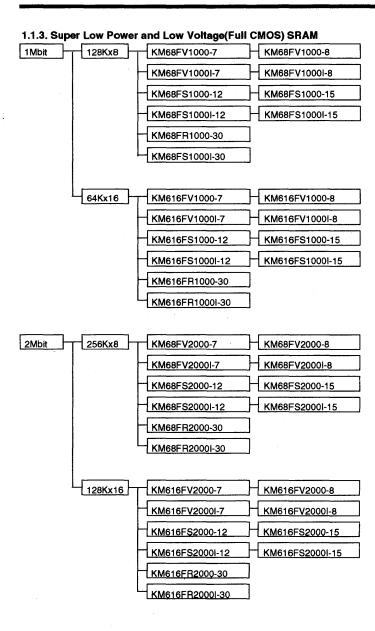


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*** : Under Development

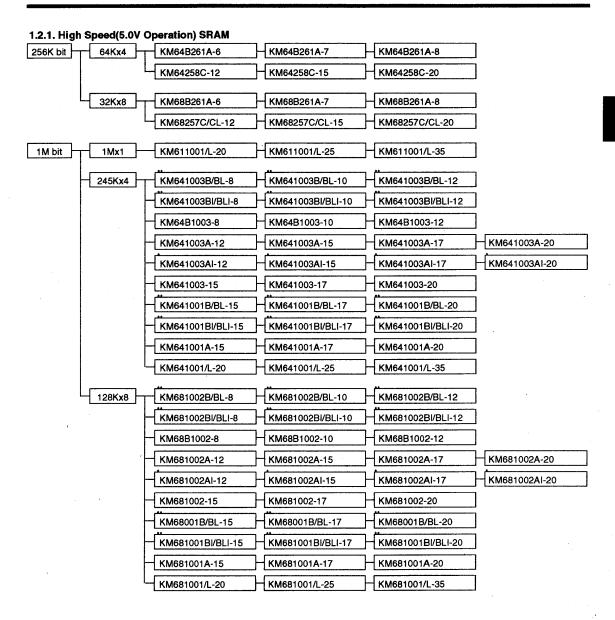




*: New Product

** : Preliminary

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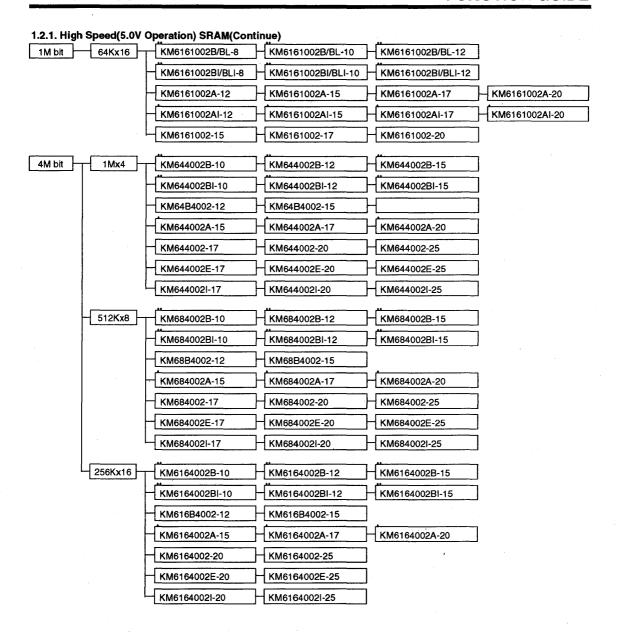


^{*** :} Under Development



^{*:} New Product

^{** :} Preliminary

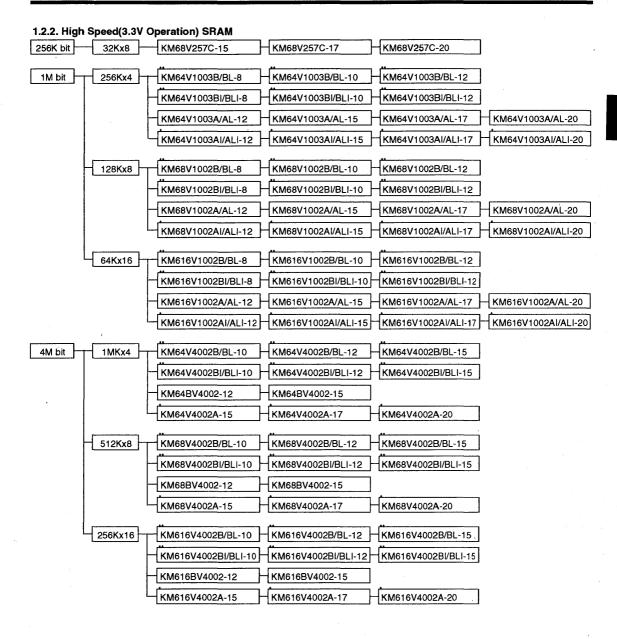




^{*:} New Product

^{** :} Preliminary

^{*** :} Under Development





^{*:} New Product

^{** :} Preliminary

^{*** :} Under Development

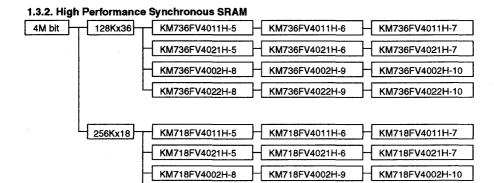
1.3.1. Synchronous SRAM 1M bit 32Kx32 KM732V589G/T-13 KM732V589G/T-15 KM732V589G/T-17 KM732V589LG/T-17 KM732V589LG/T-13 KM732V589LG/T-15 KM732V589AG/T-13 KM732V589AG/T-15 KM732V589ALG/T-15 KM732V589ALG/T-13 KM732V595AT-6 KM732V595AT-7 KM732V595AT-8 KM732V595AT-10 KM732V595ALT-6 KM732V595ALT-7 KM732V595ALT-8 KM732V595ALT-10 KM732V596AT-13 KM732V596AT-15 KM732V596ALT-13 KM732V596ALT-15 KM732V599AT-7 KM732V599AT-8 KM732V599AT-10 KM732V599ALT-7 KM732V599ALT-8 KM732V599ALT-10 32Kx36 KM736V595AT-10 KM736V595AT-6 KM736V595AT-7 KM736V595AT-8 KM736V595ALT-6 KM736V595ALT-7 KM736V595ALT-8 KM736V595ALT-10 KM736V599AT-7 KM736V599AT-8 KM736V599AT-10 KM736V599ALT-7 KM736V599ALT-8 KM736V599ALT-10 KM736V587T-8 KM736V587T-9 KM736V587T-10 64Kx18 KM718BV87J-9 KM718BV87J-10 KM718BV87J-12 KM718V687T-8 KM718V687T-9 KM718687T-10 KM718B90J-11 KM718B90J-8 KM718B90J-9 KM718B90J-10 KM718B86J-8 KM718B86J-9 KM718B86J-10 KM718B86J-12 2M bit 64Kx32 KM732V688G/T-13 KM732V688G/T-15 KM732V688LG/T-13 KM732V688LG/T-15 KM732V696T-13 KM732V696T-15 KM732V696LT-13 KM732V696LT-15 64Kx36 KM736V689T-11 KM736V689T-7 KM736V689T-8 KM736V689T-10 KM736V689LT-7 KM736V689LT-8 KM736V689LT-10 KM736V689LT-11 KM736V687T-10 KM736V687T-8 KM736V687T-9 KM718V789T-11 128Kx18 KM718V789T-7 KM718V789T-8 KM718V789T-10 KM718V789LT-7 KM718V789LT-8 KM718V789LT-10 KM718V789LT-11 KM718V787T-8 KM718V787T-9 KM718V787T-10



** : Preliminary

*** : Under Development

*: New Product



KM718FV4022H-9

KM718FV4022H-10

KM718FV4022H-8

2. SRAM FUNCTION GUIDE

2.1.1. Low Power(5.0V Operation) SRAM

Den.	Org.	Product No ^{Note1}	Op.Temp	Speed	Icc2/Isв1 (mA/μA)	Package
256K	32K x 8	KM62256CL KM62256CL-L	0~70℃	45/55/70	70/100 70/20	28-TSOP(I) Rew/Forward
		KM62256CLE KM62256CLE-L	-25~85℃	70/100	70/100 70/50	28-DIP
		KM62256CLI KM62256CLI-L	-40~85℃	70/100	70/100 70/50	28-SOP
		KM62256DL** KM62256DL-L**	0~70℃	55/70	70/50 70/10	28-TSOP(I) Rew/Forward
		KM62256DLI** KM62256DLI-L**	-40~85℃	70/100	70/50 70/15	28-DIP
512K	64K x 8	KM68512AL KM68512AL-L	0~70℃	45/55/70	70/100 70/20	32-TSOP(I) Forward
		KM68512ALI KM68512ALI-L	-40~85℃	70/100	70/100 70/50	32-SOP
1 M	128K x 8	KM681000BL KM681000BL-L	0~70℃	55/70	70/100 70/20	
		KM681000BLE KM681000BLE-L	-25~85℃	70/100	70/100 70/50	32-TSOP(I) Rev/Forward
		KM681000BLI KM681000BLI-L	-40~85℃	70/100	70/100 70/50	32-DIP
		KM681000CL KM681000CL-L	0~70℃	45/55/70	90/50 90/10	32-SOP
		KM681000CLI KM681000CLI-L	-40~85℃	55/70/100	90/50 90/15	
	64K x 16	KM6161000BL KM6161000BL-L	0~70℃	55/70	120/100 120/20	44-TSOP(i)
		KM6161000BLI KM6161000BLI-L	-40~85℃	70/100	120/100 120/50	Rev/Forward
4M	512K x 8	KM684000AL KM684000AL-L	0~70℃	55/70	90/100 90/20	
		KM684000ALI KM684000ALI-L	-40~85℃	70/100	90/100 90/50	32-TSOP(II) Rev/Forward
		KM684000BL KM684000BL-L	0~70℃	55/70	90/100 90/20	32-SOP 32-DIP
		KM684000BLI KM684000BL-LI	-40~85℃	70/100	90/100 90/50	32 3
	256Kx16	KM6164000BL-L	0~70℃	55/70	130/20	AATCOD(!!)
		KM6164000BLI-L	-40~85℃	70/100	130/50	44TSOP(II)

Note1. Refer to the ordering information for more detail description of each product.

^{*** :} Under development



^{* :} New Product

^{** :} Preliminary

2.1.2. Low Power and Low Voltage(3.0V, 3.3V Operation) SRAM

Den.	Org. & Vcc	Product No note1	Op.Temp	Speed	Icc2/IsB1 (mA/#A)	Package
256K	32K x 8 (Vcc=3.0~3.6V)	KM62V256CL-L KM62V256CLE-L KM62V256CLI-L	0~70℃ -25~85℃ -40~85℃	70/100 70/100 70/100	35/10 35/20 35/20	
	32K x 8 (Vcc=2.7~3.3V)	KM62U256CL-L KM62U256CLE-L KM62U256CIL-L	0~70℃ -25~85℃ -40~85℃	85/100 85/100 85/100	35/10 35/15 35/15	28-TSOP(I) Reverse 28-TSOP(I)
	32K x 8 (Vcc=3.0~3.6V)	KM62V256DL-L** KM62V256DLE-L** KM62V256DIL-L**	0~70℃ -25~85℃ -40~85℃	70/100 70/100 70/100	35/10 35/20 35/20	Forward 28-SOP
	32K x 8 (Vcc=2.7~3.3V)	KM62U256DL-L** KM62U256DLE-L** KM62U256DIL-L**	0~70℃ -25~85℃ -40~85℃	85/100 85/100 85/100	35/10 35/15 35/15	
512K	64K x 8 (Vcc=3.0~3.6V)	KM68V512AL-L KM68V512ALE-L KM68V512ALI-L	0~70℃ -25~85℃ -40~85℃	70/85/100 70/85/100 70/85/100	40/10 40/20 40/20	32-TSOP(I) Forward
	64K x 8 (Vcc=2.7~3.3V)	KM68U512AL-L KM68U512ALE-L KM68U512ALI-L	0~70℃ -25~85℃ -40~85℃	85/100 85/100 85/100	45/10 45/15 45/15	32-SOP
1 M	128K x 8 (Vcc=3.0~3.6V)	KM68V1000BL KM68V1000BL-L KM68V1000BLE KM68V1000BLE-L KM68V1000BLI KM68V1000BLI-L	0~70℃ -25~85℃ -40~85℃	70/100 70/100 70/100 70/100 70/100 70/100	40/50 40/15 40/100 40/20 40/100 40/20	32-TSOP(I) Rev/Forward 32-SOP
		KM68V1000CL-L KM68V1000CLE-L KM68V1000CLI-L	0~70℃ -25~85℃ -40~85℃	70/85 70/85 70/85	40/10 40/20 40/20	32-TSOP(I) Rev/Forward 32-SOP
	128K x 8 (Vcc=2.7~3.3V)	KM68U1000BL KM68U1000BL-L KM68U1000BLE KM68U1000BLE-L KM68U1000BLI-L	0~70℃ -25~85℃ -40~85℃	100 100 100 100 100 100	40/50 40/15 40/50 40/15 40/50 40/15	32-TSOP(I) Rev/Forward 32-SOP
	128K x 8 (Vcc=2.7~3.3V)	KM68U1000CL-L KM68U1000CLE-L KM68U1000CLI-L	0~70˚C -25~85˚C -40~85˚C	70/100 70/100 70/100	40/10 40/20 40/20	32-TSOP(I) 32-sTSOP 32-SOP
	64K x 16 (Vcc=3.0~3.6V)	KM616V1000BL KM616V1000BL-L KM616V1000BLE KM616V1000BLE-L KM616V1000BLI KM616V1000BLI-L	0~70℃ -25~85℃ -40~85℃	70/100 70/100 85/100 85/100 85/100 85/100	65/50 65/15 65/100 65/20 65/100 65/20	44-TSOP(II) Reverse
	64K x 16 (Vcc=2.7~3.3V)	KM616U1000BL KM616U1000BL-L KM616U1000BLE KM616U1000BLE-L KM616U1000BLI KM616U1000BLI-L	0~70℃ -25~85℃ -40~85℃	100 100 100 100 100 100	65/50 65/15 65/100 65/20 65/100 65/20	44-TSOP(II) Forward
2M	256K x 8 (Vcc=2.7~3.6V)	KM68V2000L-L** KM68V2000LI-L**	0~70˚C -40~85˚C	70/85 85/100	40/15 40/30	32-TSOP(I) 32-sTSOP(I)
		KM68U2000L-L** KM68U2000LI-L**	0~70℃ -40~85℃	70/100 85/100	40/15 40/30	32-TSOP(I) 32-sTSOP(I)

2.1.2. Low Power and Low Voltage(3.0V, 3.3V Operation) SRAM(Continue)

Den.	Org. & Vcc	Product No note1	Op.Temp	Speed	Icc2/Isв1 (mA/µA)	Package
4M	512K x 8 (Vcc=3.0~3.6V)	KM68V4000AL KM68V4000AL-L	0~70℃	70/85/100 70/85/100	50/50 50/15	32-TSOP(II) Rev/Forward
		KM68V4000ALI KM68V4000ALI-L	-40~85℃	70/85/100 70/85/100	50/50 50/20	32-SOP
	512K x 8 (Vcc=2.7~3.3V)	KM68U4000AL KM68U4000AL-L	0~70℃	70/85/100 70/85/100	50/30 50/10	32-SOP
	, , , , ,	KM68U4000ALI KM68U4000ALI-L	-40~85℃	70/85/100 70/85/100	50/30 50/15	32-TSOP(II)
	512K x 8 (Vcc=3.0~3.6V)	KM68V4000BL** KM68V4000BL-L**	0~70℃	70/85/100 70/85/100	50/50 50/15	32-SOP
		KM68V4000BLI** KM68V4000BLI-L**	-40~85℃	85/100 85/100	50/50 50/20	32-TSOP(II)
	512K x 8 (Vcc=2.7~3.3V)	KM68U4000BL** KM68U4000BL-L**	0~70℃	70/85/100 70/85/100	50/30 50/15	32-SOP
		KM68U4000BLI** KM68U4000BLI-L**	-40~85℃	85/100 85/100	50/30 50/20	32-TSOP(II)
	256K x 16 (Vcc=3.0~3.6V)	KM616V4000BL-L KM616V4000BLI-L	0~70℃ -40~85℃	70/85/100 70/85/100	70/15 70/20	44-TSOP(II)

Note1. Refer to the ordering information for more detail description of each product.



^{* :} New Product

^{** :} Preliminary

^{*** :} Under development

2.1.3. Super Low Power and Low Voltage(Full CMOS) SRAM

Den.	Org.	Product No ^{Note1}	Op.Temp	Speed	lcc2/lsa1 (mÅ/#Å)	Package
1M	128K x 8	KM68FV1000	0~70℃	70/85	55/5	
		KM68FV1000I	-40~85℃	70/85	55/5	32-TSOP(I)
		KM68FS1000	0~70℃	120/150 70/85	30/5 50/5	Forward/Reverse 32-sTSOP(I)
		KM68FS1000I	-40~85℃	120/150 70/85	30/5 50/5	Forward/Reverse
		KM68FR1000	0~70℃	300	15/5	7
		KM68FR1000I	-40~85℃	300	15/5	7
	64Kx16	KM616FV1000	0~70℃	70/85	80/5	
		KM616FV1000I	-40~85℃	70/85	80/5	1
		KM616FS1000	0~70℃	120/150 70/85	50/5 80/5	44-TSOP(II) Forward/Reverse
		KM616FS1000I	-40~85℃	120/150 70/85	50/5 80/5	Totward/Neverse
		KM616FR1000	0~70℃	300	20/5	
		KM616FR1000I	-40~85℃	300	20/5	
2M	256K x 8	KM68FV2000	0~70℃	70/85	60/10	
		KM68FV2000I	-40~85℃	70/85	60/10	32-TSOP(I)
		KM68FS2000	0~70℃	120/150 70/85	30/10 55/10	Forward/Reverse 32-sTSOP(I)
		KM68FS2000I	-40~85℃	120/150 70/85	30/10 55/10	Forward/Reverse 32-SOP
		KM68FR2000	0~70℃	300	15/10	
		KM68FR2000I	-40~85 C	300	15/10	
	128Kx16	KM616FV2000	0~70℃	70/85	80/10	
		KM616FV2000I	-40~85℃	70/85	80/10	
		KM616FS2000	0~70℃	120/150 70/85	50/10 80/10	44-TSOP(II) Forward/Reverse
		KM616FS2000I	-40~85℃	120/150 70/85	50/10 80/10	1 Olwalu/nevelse
		KM616FR2000	0~70℃	300	20/10	
		KM616FR2000I	-40~85℃	300	20/10]

Note1. Refer to the ordering information for more detail description of each product.



^{* :} New Product

^{** :} Preliminary

^{*** :} Under development

2.2.1. High Speed SRAM(5V Operation)

	Org.	Product No ^{Note1}	Speed(ns)	Tech.	Power Di	issipation	
Den.					Active Max(mA)	Standby Max(mA)	Package
256K	64K x 4	KM64B261A KM64258C	6/7/8 12/15/20	BICMOS CMOS	160 160	20 2	28SOJ 28DIP/SOJ
250K	32K x 8	KM68B261A KM68257C/CL	6/7/8 12/15/20	BICMOS CMOS	170 165	20 2/0.1	32SOJ 28DIP/SOJ/TSOP1F
1 M	1M x 1	KM611001/L	20/25/35	смоѕ	130	2/0.5	28DIP/SOJ
256K x 4 KM641003B/BL/BI/BLI** 8/10/12 CM: KM64B1003 B/10/12 BICM: KM641003A 12/15/17/20 CM: KM641003 15/17/20 CM: KM641001B/BL/BI/BLI** 15/17/20 CM:		CMOS BICMOS CMOS CMOS CMOS CMOS	150 165 150 170 120 125 150	10/1 10 8 10 5/0.5 8 2/0.5	32SOJ/TSOP2F 32SOJ 32SOJ/TSOP2F 32SOJ 28SOJ 28SOJ		
	128K x 8	KM641001/L KM681002B/BL/BI/BLI** KM681002 KM681002A KM681002	8/10/12 8/10/12 8/10/12 12/15/17/20 15/17/20	CMOS BICMOS CMOS CMOS	160 170 170 170	10/1 10 8 10	28DIP/SOJ 32SOJ(300/400)/TSOP2F 32SOJ 32SOJ(300/400)/TSOP2F 32SOJ
		KM681001B/BL/BI/BLI** KM681001A KM681001/L	15/17/20 15/17/20 20/25/35	CMOS CMOS CMOS	130 125 170	5/0.5 8 2/0.5	32SOJ(300/400) 32SOJ(300/400) 32DIP/SOJ
	64K x 16	KM6161002B/BL/BI/BLI** KM6161002A KM6161002	8/10/12 12/15/17/20 15/17/20	CMOS CMOS CMOS	200 190 230	10/1 8 10	44SOJ/TSOP2F 44SOJ/TSOP2F 44SOJ
4M	1 M x 4	KM644002B/BI** KM64B4002 KM644002A* KM644002	10/12/15 12/15 15/17/20 17/20/25	CMOS BICMOS CMOS CMOS	190 185 150 170	10 30 10 10	32SOJ/TSOP2F 32SOJ 32SOJ 32SOJ
	512K x 8	KM684002B/B ** KM68B4002 KM684002A* KM684002	10/12/15 12/15 15/17/20 17/20/25	CMOS BICMOS CMOS CMOS	200 195 170 180	10 30 10 10	36SOJ/TSOP2F 36SOJ 36SOJ 36SOJ
	256K x 16	6K x 16 KM6164002B/BI** 10/12/1 KM616B4002 12/15 KM6164002A* 15/17/2 KM6164002 20/25/3		CMOS BICMOS CMOS CMOS	250 270 210 240	10 30 10 10	44SOJ/TSOP2F 44SOJ 44SOJ 44SOJ



^{*:} New product **: Preliminary

^{*** :} Under development

2.2.2. High Speed SRAM(3.3V Operation)

Den.	Org.	Product No ^{Note1}	Speed(ns)	Tech.	Power Dissipation			
					Active Max(m ^A)	Standby Max(mA)	Package	
256K	32K x 8	KM68V257C	15/17/20	смоѕ	90	0.1	28DIP/SOJ/TSOP1F	
1M	256K x 4	KM64V1003B/BL/BI/BLI** KM64V1003A/AL/AI/ALI	8/10/12 12/15/17/20	CMOS CMOS	150 130	5/0.5 5/0.5	32SOJ/TSOP2F 32SOJ/TSOP2F	
	128K x 8	KM68V1002B/BL/BI/BLI** KM68V1002A/AL/AI/ALI	8/10/12 12/15/17/20	CMOS CMOS	160 140	5/0.5 5/0.5	32SOJ(300/400)/TSOP2F 32SOJ(300/400)/TSOP2F	
	64K x 16	KM616V1002B/BL/BI/BLI** KM616V1002A/AL/AI/ALI	8/10/12 12/15/17/20	CMOS CMOS	200 170	5/0.5 5/0.5	44SOJ/TSOP2F 44SOJ/TSOP2F	
4M	1M x 4	KM64V4002B/BL/BI/BLI** KM64BV4002 KM64V4002A*	10/12/15 12/15 15/17/20	CMOS BICMOS CMOS	160 160 140	10/1 30 10	32SOJ/TSOP2F 32SOJ 32SOJ	
	512K x 8	KM68V4002B/BL/BI/BLI** KM68BV4002 KM68V4002A*	10/12/15 12/15 15/17/20	CMOS BICMOS CMOS	170 170 160	10/1 30 10	36SOJ/TSOP2F 36SOJ 36SOJ	
	256K x 16	KM616V4002B/BL/BI/BLI** KM616BV4002 KM616V4002A*	10/12/15 12/15 15/17/20	CMOS BICMOS CMOS	240 240 200	10/1 30 10	44SOJ/TSOP2F 44SOJ 44SOJ	

^{* :} New product ** : Preliminary

^{***:} Under development

2.3.1. Specialty SRAM

Den.	Org. & Vcc	Product No*	Mode	Op.Temp	1/0	tCYC	tCD	Package
1M	32Kx32, 3.3V	KM732V589 KM732V589A KM732V595A KM732V596A KM732V599A	SPB SPB SPB SPB SPB	CMOS CMOS CMOS CMOS CMOS	3.3V 3.3V 2.5V 2.5V/3.3V 3.3V	13/15 13/15 6.6/7.5/8.6/10 13/15 7.5/8.6/10	7/8 7/8 4.4/5/5/5.5 7/8 4.5/5/5	(T)QFP (T)QFP TQFP TQFP TQFP
	32Kx36, 3.3V	KM736V595A KM736V599A KM736V587	SPB SPB SB	CMOS CMOS CMOS	2.5V 3.3V 3.3V	6.6/7.5/8.6/10 7.5/8.6/10 12/15/17	4.4/5/5/5.5 4.5/5/5 8.5/9/10	TQFP TQFP TQFP
	64Kx18, 3.3V	KM718BV87 KM718V687	SB SB	BICMOS CMOS	3.3V 3.3V	12/15/17 12/15/17	8.5/9/10 8.5/9/10	52PLCC TQFP
	64Kx18, 5V	KM718B90 KM718B86	SB SB	BICMOS BICMOS	5.0V 5.0V	11/15/17/20 12/15/17/20	8/9/10/12 8/9/10/12	52PLCC 52PLCC
2M	64Kx32, 3.3V	KM732V688 KM732V696	SPB SPB	CMOS CMOS	3.3V 2.5V/3.3V	13/15 13/15	7/8 7/8	(T)QFP TQFP
	64Kx36, 3.3V	KM736V689 KM736V687	SPB SB	CMOS CMOS	3.3V 3.3V	7.5/8.6/10 12/15/17	4.5/5/5 8.5/9/10	TQFP TQFP
	128Kx18, 3.3V	KM718V789 KM718V787	SPB SB	CMOS CMOS	3.3V 3.3V	7.5/8.6/10 12/15/17	4.5/5/5 8.5/9/10	TQFP TQFP
4M	128Kx36, 3.3V	KM736FV4011 KM736FV4021 KM736FV4002 KM736FV4022	SP SP RL RL	CMOS CMOS CMOS CMOS	1.5V 3.3V 2.5V 3.3V	5/6/7 5/6/7 8/9/10 8/9/10	2.5/3.0/3.5 2.5/3.0/3.5 7/8/9 7/8/9	119BGA 119BGA 119BGA 119BGA
	256Kx18, 3.3V	KM718FV4011 KM718FV4021 KM718FV4002 KM718FV4022	SP SP RL RL	CMOS CMOS CMOS CMOS	1.5V 3.3V 2.5V 3.3V	5/6/7 5/6/7 8/9/10 8/9/10	2.5/3.0/3.5 2.5/3.0/3.5 7/8/9 7/8/9	119BGA 119BGA 119BGA 119BGA

*: New product

** : Preliminary

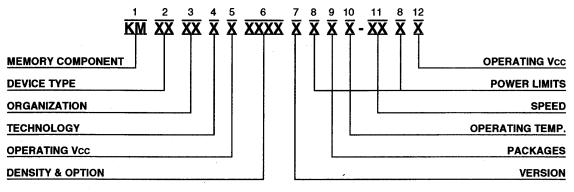
*** : Under development

- SPB : Synchronous pipelined burst - SB : Synchronous burst - RL : Register to Latch



3. ORDERING INFORMATION

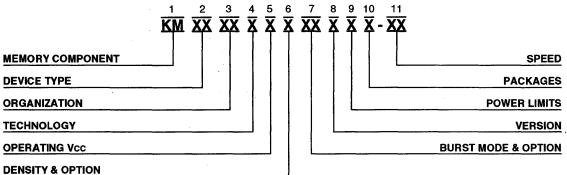
3.1.1. Asynchronous SRAM



1. MEMORY COMPONENT		8. POWER LIMITS	
A DEMOS TABLE		. BLANK	High Power(Fast)
2. DEVICE TYPE		In Full CMOS Low F	Power SRAM(Slow)
. 6	Asynch, SRAM	• • • • • • • • • • • • • • • • • • • •	Low Power
.7	Synch. SRAM	. L-L	Low Low Power
3. ORGANIZATION		9. PACKAGES	
.1	x1 bit	. P	DIP
. 4	x4 bit	C	SOI
. 2 or 8	x8 bit	. J	SOJ or PLCC
. 9	x9 bit	. T	TSOP(Standard)
. 16	x16 bit	. R	TSOP(Standard)
. 32	x32 bit		, ,
4. TECHNOLOGY		10. OPERATING TEMP.	
		. BLANK	Commercial
. BLANK	CMOS	· E	Extended
. BLANK	BICMOS		Industrial
	Full CMOS	• •	
5. OPERATING Vcc		11. SPEED	
. BLANK	5.0V	SLOW SRAM	
_ V	3.3V		4Ema
. Ů · · · · · · · · · · · · · · · · · ·	3.0V	. 4	45f18 55no
. S	2.5V	. 7 · · · · · · · · · · · · · · · · · ·	70no
. T	2.0V	. 8	7011S
		. 10	10000
6. DENSITY & OPTION		12	100115 120nc
	64:64K Slow	. 12	15000
. 64	256:256K Slow	. 15	130118
. 257	257:257K Fast	FAST SRAM	
. 258	258:256K Fast(with OE)		_
. 512	512:512K Slow	. 6	6ns
. 1000	1000:1M Slow	. 7	7ns
. 1001	1001:1M Fast	. 8	8ns
. 1002	1002:1M Fast(Revolutionary)	. 10	10ns
		. 12	12ns
- 2000.	2000: 2M Slow	. 15	15ns
. 4000	4000:4M Slow	. 17	17ns
- 2000 · · · · · · · · · · · · · · · · ·	4002:4M Fast(Revolutionary)	. 20	20ns
7. VERSION	• • • • • • • • • • • • • • • • • • • •	. 25	25ns
	First Con	. 30	30ns
• BLANK • • • • • • • • • • • • • • • • • • •	First Gen.		
• A	Second Gen.		

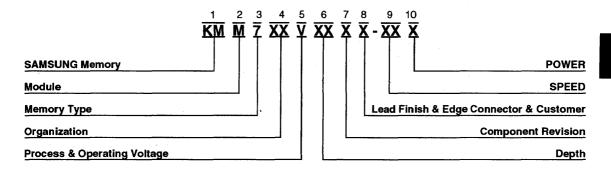
Third Gen.

3.2.1. Synchronous Burst SRAM



DENSITY & OPTION	
1. MEMORY COMPONENT 2. DEVICE TYPE	8. VERSION . BLANK First Gen A Second Gen B Third Gen.
• 6 · · · · · · · · · · · · · · · · · Asynch, SRAM • 7 · · · · · · · · · · Synch, SRAM	. C · · · · · · · Forth Gen.
3. ORGANIZATION . 16 x16 bit	9. POWER LIMITS BLANK LUBBER B
. 18	10. PACKAGES . H BGA . T TSOP/TQFP
4. TECHNOLOGY	. J PLCC . G QFP
BLANK CMOS or AMOS B BICMOS	11. SPEED Sync Bust(CLOCK ACCESS TIME)
5. OPERATING Vcc . BLANK 5.0V . V	Sync Bust(CLOCK ACCESS TIME) . 8
BLANK 32Kx9 or 64Kx18 5 32K Depth 6 64K Depth 7 128K Depth	Sync Pipe & Burst(CLOCK CYCLE TIME) . 7
7. BURST MODE & OPTION . 86	. 13······ 75MHz . 15····· 66MHz . 17···· 60MHz . 20···· 50MHz
. 89	KM732V589(Pipelined/Non-Pipelined) . 10 100MHz, 6ns/40MHz, 17ns . 15 66MHz, 8ns/40MHz, 17ns . 20 66MHz, 8ns/50MHz, 15ns . 25 60MHz, 9ns/40MHz, 17ns

3.2.2. Synchronous Burst SRAM Module



1. SAMSUNG Memory

2. Module

3. Memory Type

- -1:FLASH
- 2 : Mask ROM
- 3 : DRAM DIMM
- 4 : DRAM SIP
- 5 : DRAM SIMM
- 6 : Async SRAM - 7 : Sync SRAM
- 8 : M-ROM and SRAM
- -9: VRAM

4. Organization

- 8 : x8 bit
- 9 : x9 bit
- 16: x16 bit
- 18 : x18 bit - 32 : x32 bit
- 32 : x32 bit
- 64 : x64 bit
- 72 : x72 bit

5. Process & Operating Voltage

- Blank : CMOS 5V - V : CMOS 3.3V - B : BiCMOS 5V 6. Depth

- 32, 33, 34, 35, 36 : 32K - 64, 65, 66, 67, 68 : 64K - 128, 129, 130, 131 ... : 128K - 512, 513, 514, 515 : 512K - 544, 545, 546 : 544K

7. Component Revision

- Blank : First Gen. - A : Second Gen - B : Third Gen

8. Lead Finish & Edge Connector & Customer

- Blank : Solder DIMM - G : Gold DIMM

9. Speed

10. Power Dissipation.

- Blank : Nomal Power - L : Low Power

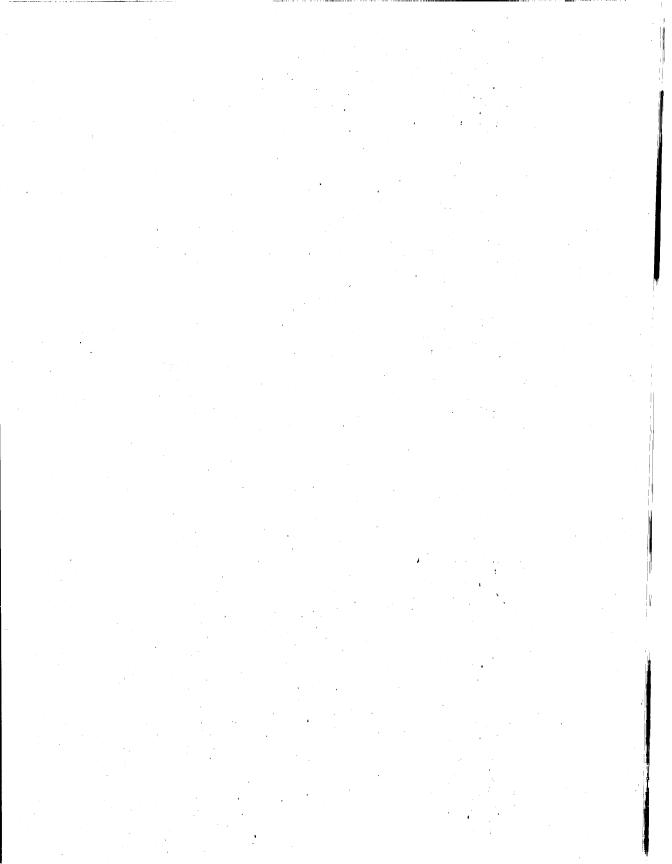


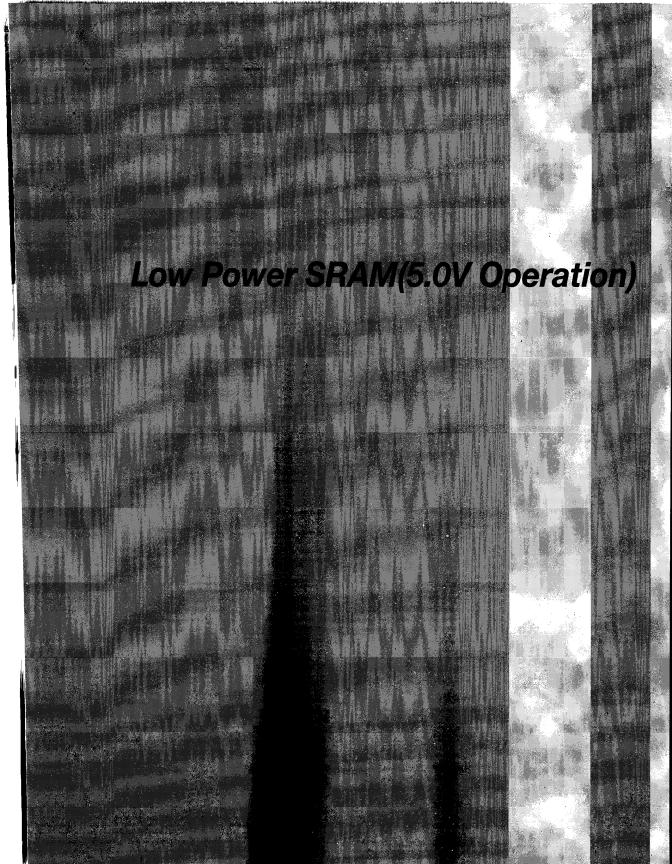
NOTES

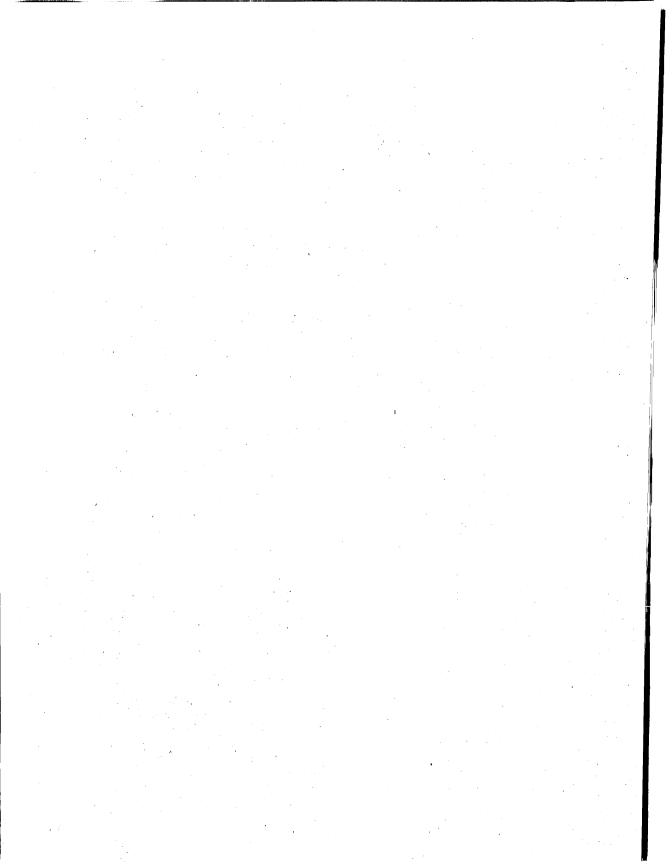


Data Sheets 2









32Kx8 bit Low Power CMOS Static RAM

FEATURES

• Process Technology: 0.7

m CMOS

· Organization: 32Kx8

• Power Supply Voltage : Single 5V \pm 10%

Low Data Retention Voltage: 2V(Min)

· Three state output and TTL Compatible

· Package Type: JEDEC Standard

28-DIP, 28-SOP, 28-TSOP I -Forward/Reverse

GENERAL DESCRIPTION

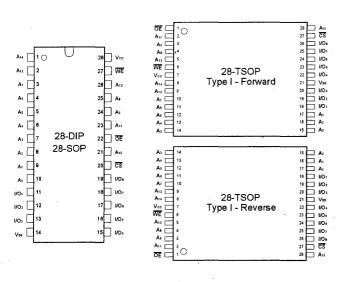
The KM62256C family is fabricated by SAMSUNG's advanced CMOS process technology. The family can support various operating temperature ranges and has various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

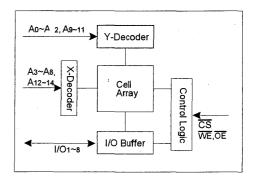
Product Family	0			Power Dissipation		
	Operating Temperature.	Speed (ns)	PKG Type	Standby (ISB1, Max)	Operating (Icc2)	
KM62256CL KM62256CL-L	Commercial (0~70℃)	45*/55/70ns	28-DIP, 28-SOP 28-TSOP R/F	100 µA 20 µA		
KM62256CLE KM62256CLE-L	Extended (-25~85°C)	70/100ns	28-SOP 28-TSOP R/F	100 µA 50 µA	70mA	
KM62256CLI KM62256CLI-L	Industrial (-40~85℃)	70/100ns	28-SOP 28-TSOP R/F	100 μA 50 μA		

^{*} The parameter is measured with 30pF test load.

PIN DESCRIPTION



FUNCTIONAL BLOCK DIAGRAM



NameName	Function
A0~A14	Address Inputs
WE	Write Enable Input
CS	Chip Select Input
ŌĒ	Output Enable Input
I/O1~I/O8	Data Inputs/Outputs
Vcc	Power(5V)
Vss	Ground

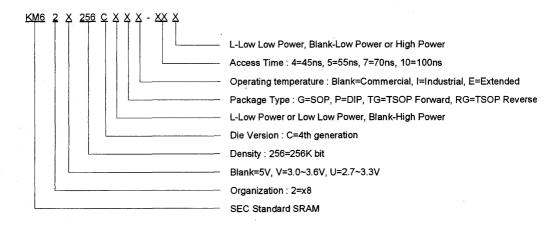


PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST

Commercial Temp Product (0~70°C)			Temp Products 5~85℃)	Industrial Temp Products (-40~85℃)			
Part Name	Function	Part Name	Function	Part Name	Function		
KM62256CLP-4	28-DIP, 45ns, L-pwr	KM62256CLGE-7	28-SOP, 70ns, L-pwr	KM62256CLGI-7	28-SOP, 70ns, L-pwr		
KM62256CLP-4L	28-DIP, 45ns, LL-pwr	KM62256CLGE-7L	28-SOP, 70ns, LL-pwr	KM62256CLGI-7L	28-SOP, 70ns, LL-pwr		
KM62256CLP-5	28-DIP, 55ns, L-pwr	KM62256CLGE-10	28-SOP, 100ns, L-pwr	KM62256CLGI-10	28-SOP, 100ns, L-pwr		
KM62256CLP-5L	28-DIP, 55ns, LL-pwr	KM62256CLGE-10L	28-SOP, 100ns, LL-pwr	KM62256CLGI-10L	28-SOP, 100ns, LL-pwr		
KM62256CLP-7	28-DIP, 70ns, L-pwr	KM62256CLTGE-7	28-TSOP F, 70ns, L-pwr	KM62256CLTGI-7	28-TSOP F, 70ns, L-pwr		
KM62256CLP-7L	28-DIP, 70ns, LL-pwr	KM62256CLTGE-7L	28-TSOP F, 70ns, LL-pwr	KM62256CLTGI-7L	28-TSOP F, 70ns, LL-pwr		
KM62256CLG-4	28-SOP, 45ns, L-pwr	KM62256CLTGE-10	28-TSOP F, 100ns, L-pwr	KM62256CLTGI-10	28-TSOP F, 100ns, L-pwr		
KM62256CLG-4L	28-SOP, 45ns, LL-pwr	KM62256CLTGE-10L	28-TSOP F, 100ns, LL-pwr	KM62256CLTGI-10L	28-TSOP F, 100ns, LL-pwr		
KM62256CLG-5	28-SOP, 50ns, L-pwr	KM62256CLRGE-7	28-TSOP R, 70ns, L-pwr	KM62256CLRGI-7	28-TSOP R, 70ns, L-pwr		
KM62256CLG-5L	28-SOP, 50ns, LL-pwr	KM62256CLRGE-7L	28-TSOP R, 70ns, LL-pwr	KM62256CLRGI-7L	28-TSOP R, 70ns, LL-pwr		
KM62256CLG-7	28-SOP, 70ns, L-pwr	KM62256CLRGE-10	28-TSOP R, 100ns, L-pwr	KM62256CLRGI-10	28-TSOP R, 100ns, L-pwr		
KM62256CLG-7L	28-SOP, 70ns, LL-pwr	KM62256CLRGE-10L	28-TSOP R, 100ns, LL-pwr	KM62256CLRGI-10L	28-TSOP R, 100ns, LL-pwr		
KM62256CLTG-4	28-TSOP F, 45ns, L-pwr						
KM62256CLTG-4L	28-TSOP F, 45ns, LL-pwr						
KM62256CLTG-5	28-TSOP F, 55ns, L-pwr						
KM62256CLTG-5L	28-TSOP F, 55ns, LL-pwr						
KM62256CLTG-7	28-TSOP F, 70ns, L-pwr						
KM62256CLTG-7L	28-TSOP F, 70ns, LL-pwr						
KM62256CLRG-4	28-TSOP R, 45ns, L-pwr						
KM62256CLRG-4L	28-TSOP R, 45ns, LL-pwr						
KM62256CLRG-5	28-TSOP R, 55ns, L-pwr						
KM62256CLRG-5L	28-TSOP R, 55ns, LL-pwr						
KM62256CLRG-7	28-TSOP R, 70ns, L-pwr						
KM62256CLRG-7L	28-TSOP R, 70ns, LL-pwr						

ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	Vin,Vout	-0.5 to Vcc+0.5	V	-
Voltage on Vcc supply relative to Vss	Vcc	-0.5 to 7.0	V	<u>-</u>
Power Dissipation	Po	1.0	W	-
Storage temperature	Тѕтс	-65 to 150	°	. -
	TA	0 to 70	င	KM62256CL/L-L
Operating Temperature		-25 to 85	°	KM62256CLE/LE-L
		-40 to 85	°	KM62256CLI/LI-L
Soldering temperature and time	TSOLDER	260℃, 10sec (Lead Only)	-	-

^{*} Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*

Item	Symbol	Min	Typ**	Max	Unit
Supply voltage	Vcc	4.5	5.0	5.5	٧ .
Ground	Vss	0	0	0	V
Input high voltage	ViH	2.2	•	Vcc+0.5V	V
Input low voltage	VIL	-0.5***	-	0.8	Ý

^{* 1)} Commercial Product : Ta=0 to 70°C, unless otherwise specified

CAPACITANCE* (f=1MHz, TA=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	Cin	VIN=0V	-	6	pF
Input/Output capacitance	Cio	Vio=0V		8	pF

^{*} Capacitance is sampled not 100% tested



²⁾ Extended Product : Ta=-25 to 85 $^{\circ}\mathrm{C}$, unless otherwise specified

³⁾ Industrial Product : Ta=-40 to 85 $^{\circ}\mathrm{C}$, unless otherwise specified ** Ta=25 $^{\circ}\mathrm{C}$

^{***} VIL(min)=-3.0V for \(\le \) 50ns pulse width

DC AND OPERATING CHARACTERISTICS

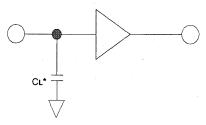
It	em	Symbol	Test	Conditions*	Min	Typ**	Max	Unit
Input leakage curi	rent	lu	Vin=Vss to Vcc			-	1	μA
Output leakage cu	urrent	lLO	CS=VIH or WE=V VIO=Vss to Vcc	IL	-1	-	1	μA
Operating powers	supply current	lcc	CS=VIL, VIN=VIH	or VIL, 110=0mA	-	7	15***	mA
Average operating current		lcc1	Cycle time=1 µs 10 CS ≤ 0.2V, VIL ≤ 0 VIN ≥ Vcc -0.2V,	0.2V		,	7****	mA
, '			Min cycle, 100% duty CS=VIL, IIo=0mA			-	70	mA
Output low voltage	e ⁷	Vol	loL=2.1mA		-	-	0.4	٧
Output high voltag	је	Vон	Iон=-1.0mA		2.4	-	-	V
Standby Current(TTL)	ISB	CS=ViH		-	-	1****	mA
	KM62256CL KM62256CL-L	:	-	L(Low Power) LL(L Low Power)	-	2 1	100 20	μA μA
Standby Current (CMOS)	KM62256CLE KM62256CLE-L	ISB1	$\overline{\text{CS}} \ge \text{Vcc-0.2V}$ $\text{Vin} \ge 0.2\text{V}$ or $\text{Vin} \le \text{Vcc-0.2V}$	L(Low Power) LL(L Low Power)	-		100 50	μA μA
KM62256CLI KM62256CLI-L				L(Low Power) LL(L Low Power)	-	-	100 50	μA μA

^{*1)} Commercial Product : Ta=0 to 70 ℃, Vcc=5V±10% unless otherwise specified 2) Extended Product : Ta=-25 to 85 ℃, Vcc=5V±10% nless otherwise specified 3) Industrial Product : Ta=-40 to 85 ℃, Vcc=5V±10% unless otherwise specified

A.C CHARACTERISTICS

TEST CONDITIONS (1.Test Load and Test Input/Output Reference)*

Item	Value	Remark
Input pulse level	0.8 to 2.4V	-
Input rising & falling time	5ns	-
input and output reference voltage	1.5V	-
Output load (See right)	CL=100pF+1TTL	-
Output road (See right)	**CL=30pF+1TTL	-



* Including scope and jig capacitance



^{**} TA=25°C

^{*** 20}mA for Extended and Industrial Products
****10mA for Extended and Industrial Products
****2mA for Extended and Industrial Products

^{*} See DC Operating conditions
** Test load for 45ns commercial products

TEST CONDITIONS (2. Temperature and Vcc Conditions)

Product Family	Temperature	Power Supply(Vcc)	Speed Bin	Comments
KM62256CL/L-L	0~70℃	5V ± 10%	45*/55/70ns	Commercial
KM62256CLE/LE-L	-25~85℃	5V ± 10%	70/100ns	Extended
KM62256CLI/LI-L	-40~85℃	5V ± 10%	70/100ns	Industrial

^{*} The parameter is measured with 30pF test load

PARAMETER LIST FOR EACH SPEED BIN

						Spe	ed Bins				
	Parameter List	Symbol	45	ins*	5!	ins	70)ns	10	0ns	Units
			Min	Max	Min	Max	Min	Max	Min	Max	
Read	Read cycle time	tRC	45	-	55	-	70	-	100	-	ns
	Address access time	tAA	-	45	-	55	-	70	-	100	ns
	Chip select to output	tco	-	45	-	55	-	70	-	100	ns
	Output enable to valid output	tOE	-	25	-	25	-	35	-	50	ns
	Chip select to low-Z output	tLZ	10	-	10		10	-	10	-	ns
	Output enable to low-Z output	toLZ	5	-	5	-	5	-	5	-	ns
	Chip disable to high-Z output	tHZ	0	20	0	20	0	30	0	35	ns
	Output disable to high-Z output	tonz	0	20	0	20	0	30	0	35	ns
	Output hold from address change	tон	5	-	5	-	5	-	5	-	ns
Write	Write cycle time	twc	45	-	55	-	70	-	100	-	ns
	Chip select to end of write	tcw	45	-	45	-	60	-	80	-	ns
	Address set-up time	tAS	0	-	0	-	0	-	0	-	ns
	Address valid to end of write	tAW	45	-	45	-	60	-	80	-	ns
	Write pulse width	tWP	40	-	40	-	50	-	60	-	ns
	Write recovery time	tWR	0	-	0	-	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	20	0	20	0	25	0	35	ns
	Data to write time overlap	tDW	25	-	25	-	30	-	50	-	ns
	Data hold from write time	tDH	0	-	0	-	0	-	0	-	ns
	End write to output low-Z	tow	5	-	-5	-	5	-	5	-	ns

^{*} The parameter is measured with 30pF test load

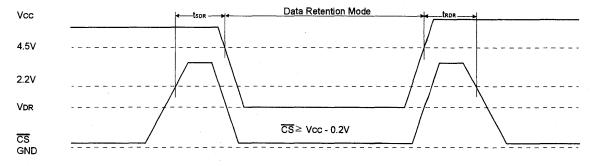
DATA RETENTION CHARACTERISTICS

Item Symbol		Symbol	Test Cond	Min	Typ**	Max	Unit	
Vcc for data retention	VDR		CS ≥Vcc-0.2V	2.0	-	5.5	V	
		KM62256CL KM62256CL-L		L-Ver LL-Ver	-	,1 0.5	50 10	
Data retention current	IDR KM62256CLE KM62256CLE-L	Vcc=3.0V CS≥Vcc-0.2V	L-Ver LL-Ver	· -	-	50 25	μA·	
·		KM62256CLI KM62256CLI-L		L-Ver LL-Ver	-	-	50 25	
Data retention set-up time	tSDF	2	See data retentio	n	0	-	-	
Recovery time	tRDF		waveform		5	-	-	ms

^{* 1)} Commercial Product : Ta=0 to 70 °C, unless otherwise specified 2) Extended Product : Ta=-25 to 85 °C, nless otherwise specified 3) Industrial Product : Ta=-40 to 85 °C, unless otherwise specified ** Ta=25 °C

DATA RETENTION WAVE FORM

1) CS Controlled



FUNCTIONAL DESCRIPTION

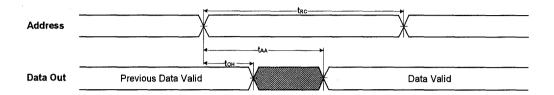
cs	WE	ŌĒ	Mode	I/O Pin	Current Mode
Н	Х	Х	Power Down	High-Z	ISB ISB1
L	Н	Н	Output Disable	High-Z	1cc
<u>L</u>	Н	L	Read	Dout	Icc
L	L	X	Write	Din	Icc

^{*} X means don't care

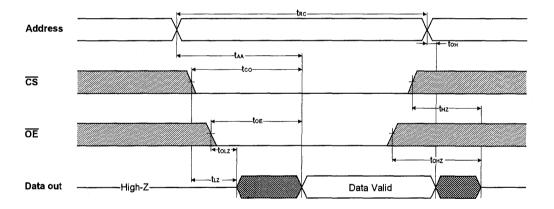


TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (1) (Address Controlled) ($\overline{CS}=\overline{OE}=VIL, \overline{WE}=VIH)$



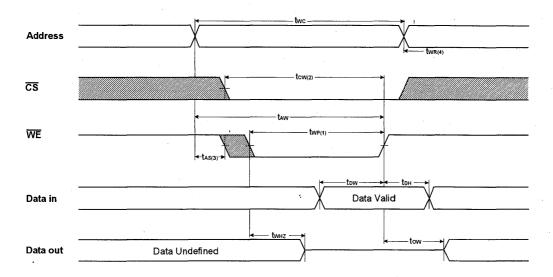
TIMING WAVEFORM OF READ CYCLE(2) (WE=VIH)



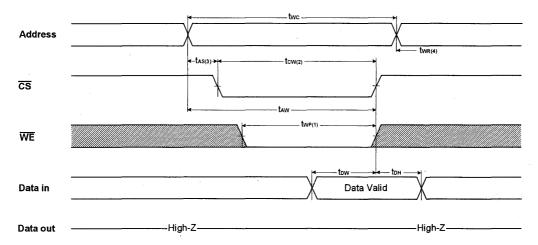
NOTES (READ CYCLE)

- 1. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
- 2. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device.

TIMING WAVEFORM OF WRITE CYCLE(1) (WE Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) (CS Controlled)



NOTES (WRITE CYCLE)

- 1. A write occurs during the overlap(tWP) of low \overline{CS} and low \overline{WE} . A write begins at the latest transition among \overline{CS} goes low and \overline{WE} going low: A write end at the earliest transition among \overline{CS} going high and \overline{WE} going high, \overline{tWP} is measured from the beginning of write to the end of write.
- 2. \mbox{TCW} is measured from the $\overline{\mbox{CS}}$ going low to end of write.
- 3. tAS is measured from the address valid to the beginning of write.
- 4. tWR is measured from the end of write to the address change. tWR applied in case a write ends as $\overline{\text{CS}}$ or $\overline{\text{WE}}$ going high.



32Kx8 bit Low Power CMOS Static RAM

FEATURES

• Process Technology: 0.4 µm CMOS

· Organization: 32Kx8

• Power Supply Voltage : Single 5V ± 10%

Low Data Retention Voltage: 2V(Min)

Three state output and TTL Compatible
 Package Type: JEDEC Standard

28-DIP, 28-SOP, 28-TSOP I -Forward/Reverse

GENERAL DESCRIPTION

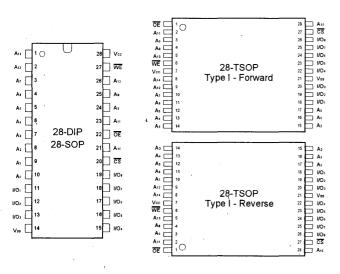
The KM62256D family is fabricated by SAMSUNG's advanced CMOS process technology. The family can support various operating temperature ranges and has various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

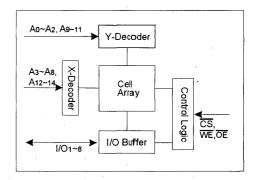
Product	G#			Power Dissipation			
Family	Operating Temperature.	Speed (ns)	PKG Type	Standby (ISB1, Max)	Operating (Icc2)		
KM62256DL KM62256DL-L	Commercial (0~70℃)	45*/55/70ns	28-DIP,28-SOP 28-TSOP(I) R/F	50µA 10µA	70mA		
KM62256DLI KM62256DLI-L	Industrial (-40~85℃)	70/100ns	28-SOP 28-TSOP(I) R/F	50µA 15µA`	, onia		

^{*} The parameter is measured with 30pF test load.

PIN DESCRIPTION



FUNCTIONAL BLOCK DIAGRAM



Pin Name	Function
A0~A14	Address Inputs
WE	Write Enable Input
CS	Chip Select Input
ŌĒ	Output Enable Input
I/O1~I/O8	Data Inputs/Outputs
Vcc	Power(5V)
Vss .	Ground



64Kx8 bit Low Power CMOS Static RAM

FEATURES

• Process Technology: 0.6 µm CMOS

· Organization: 64Kx8

Power Supply Voltage: Single 5V ± 10%
 Low Data Retention Voltage: 2V(Min)
 Three state output and TTL Compatible

· Package Type : JEDEC Standard

32-SOP, 32-TSOP I -Forward

GENERAL DESCRIPTION

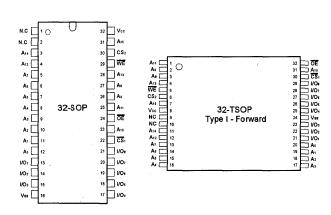
The KM68512A family is fabricated by SAMSUNG's advanced CMOS process technology. The family can support various operating temperature ranges and has various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

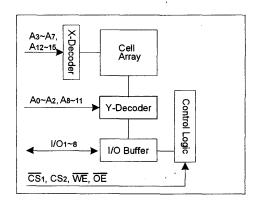
Dandonk	0	Van Para	S		Power Di	sipation	
Product Family	Operating Temperature.	Vcc Range (V)	Speed (ns)	PKG Type	Standby (IsB1, Max)	Operating (Icc2)	
KM68512AL	Commercial	5V±0.5V	45*/55/70ns	32-SOP	100 µA		
KM68512AL-L	(0~70℃)	3V ±0.5V	45 /55// 0/18	32-TSOP I F	20 <i>µ</i> A	70mA	
KM68512ALI	Industrial	5V±0.5V	70/100ns	32-SOP	100 µA	, one	
(M68512ALI-L (-40~85℃)		5 v = 0.5 v 70/100hs		32-TSOP I F	50 <i>μ</i> Α		

^{*} The parameter measured with 30pF test load

PIN DESCRIPTION



FUNCTIONAL BLOCK DIAGRAM



Name	Function
A0~A15	Address Inputs
WE	Write Enable Input
CS1, CS2	Chip Select Inputs
ŌĒ	Output Enable Input
1/01~1/016	Data Inputs/Outputs
Vcc	Power
Vss	Ground
N.C	No Connection



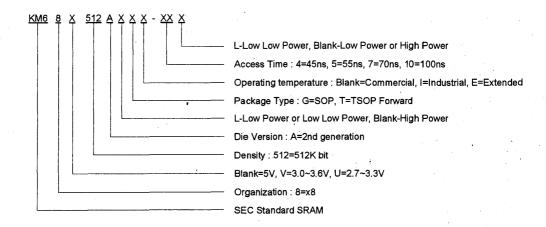
PRODUCT LIST & ORDERING INFORMATION PRODUCT LIST

32-TSOP F, 70ns, LL-pwr

Commercial Temp Product (0~70℃)		Industrial Temp Products (-40~85℃)				
Part Name	Function	Part Name	Function			
KM68512ALG-4	32-SOP, 45ns, L-pwr	KM68512ALGI-7	32-SOP, 70ns, L-pwr			
KM68512ALG-4L	32-SOP, 45ns, LL-pwr	KM68512ALGI-7L	32-SOP, 70ns, LL-pwr			
KM68512ALG-5	32-SOP, 55ns, L-pwr	KM68512ALGI-10	32-SOP, 100ns, L-pwr			
KM68512ALG-5L	32-SOP, 55ns, LL-pwr	KM68512ALGI-10L	32-SOP, 100ns, LL-pwr			
KM68512ALG-7	32-SOP, 70ns, L-pwr	KM68512ALTI-7	32-TSOP F, 70ns, L-pwr			
KM68512ALG-7L	32-SOP, 70ns, LL-pwr	KM68512ALTI-7L	32-TSOP F, 70ns, LL-pwr			
KM68512ALT-4	32-TSOP F, 45ns, L-pwr	KM68512ALTI-10	32-TSOP F, 100ns, L-pwr			
KM68512ALT-4L	32-TSOP F, 45ns, LL-pwr	KM68512ALTI-10L	32-TSOP F, 100ns, LL-pwr			
KM68512ALT-5	32-TSOP F, 55ns, L-pwr					
KM68512ALT-5L	32-TSOP F, 55ns, LL-pwr					
KM68512ALT-7	32-TSOP F, 70ns, L-pwr					

ORDERING INFORMATION

KM68512ALT-7L



ABSOLUTE MAXIMUM RATINGS*

ltem .	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	VIN, VOUT	-0.5 to 7.0	V	·
Voltage on Vcc supply relative to Vss	Vcc	-0.5 to 7.0	V	
Power Dissipation	Po	1.0	W	-
Storage temperature	Тѕтҫ	-65 to 150	°C	-
Operation Towns and the	TA	0 to 70	°C	KM68512AL/L-L
Operating Temperature	'^	-40 to 85	င	KM68512ALI/LI-L
Soldering temperature and time	TSOLDER	260℃, 10sec (Lead Only)	-	•

^{*} Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*

Item	Symbol	Min	Typ**	Max	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V 1
Ground	Vss	0	0	0	V
Input high voltage	ViH	2.2	-	Vcc+0.5V	٧
Input low voltage	Vil	-0.5***	-	0.8	V

^{* 1)} Commercial Product : Ta=0 to 70 $^{\circ}\mathrm{C}$, unless otherwise specified

CAPACITANCE* (f=1MHz, Ta=25°C)

Item	Symbol		Min	Max	Unit
Input capacitance	CIN	VIN=0V	-	6	pF
Input/Output capacitance	Cio	Vio=0V	-	8 :	pF.

^{*} Capacitance is sampled not 100% tested



²⁾ Industrial Product : Ta=-40 to 85 °C, unless otherwise specified

^{**} Ta=25℃

^{***} VIL(min)=-3.0V for 50ns pulse width

DC AND OPERATING CHARACTERISTICS

lte	em	Symbol	Test	Conditions*	Мі	Typ**	Max	Uni
Input leakage curre	nt	lu	Vin=Vss to Vcc		-1	-	1	μA
Output leakage curr	ent	lLO	CS1=VIH or CS2=\ VIO=Vss to Vcc	VIL or WE=VIL	-1	-	1	μÀ
Operating power su	pply current	lcc	CS1=VIL, CS2=VIH	I, VIN=VIH or VIL, IIO=0mA	-	7	15	mA
Average operating current		Icc1	Cycle time=1 µs 100% duty CS1≤ 0.2V, CS2≥ Vcc-0.2V VIL ≤ 0.2V, VIH ≥ Vcc -0.2V, IIo=0mA		-	-	10	mA
			Min cycle, 100% duty CS1=VIL, CS2=VIH IIO=0mA			-	70	mA
Output low voltage		VoL	IoL=2.1mA		-	-	0.4	V
Output high voltage		Vон	lон=-1.0mA		2.4	•		V
Standby Current(TT	L)	ISB	CS1=VIH, CS2=VIL		-	-	3	mA
Standby Current (CMOS)	KM68512AL/L-L	ISB1	CS ₁ ≥ Vcc-0.2V CS ₂ ≤ 0.2V ViN≤0.2V or	L(Low Power) LL(L Low Power)	-	2	100 20	μA μA
	KM68512ALI/LI-L		VIN≥Vcc-0.2V	L(Low Power) LL(L Low Power)	-	2	100 50	μA μΑ

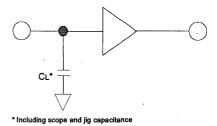
^{* 1)} Commercial Product : Ta=0 to 70 $^{\circ}$, Vcc=5V $^{\pm}$ 10% unless otherwise specified 2) Industrial Product : Ta=-40 to 85 $^{\circ}$, Vcc=5V $^{\pm}$ 10% unless otherwise specified ** Ta=25 $^{\circ}$

A.C CHARACTERISTICS

TEST CONDITIONS (1.Test Load and Test Input/Output Reference)*

Item	Value	Remark
Input pulse level	0.8 to 2.4V	-
Input rising & falling time	5ns	-
input and output reference voltage	1.5V	
Output load (See right)	CL=100pF+1TTL	-
	**CL=30pF+1TTL	-

^{*} See DC Operating conditions **KM68512AL/AL-4L



TEST CONDITIONS (2. Temperature and Vcc Conditions)

Product Family	Temperature	Power Supply(Vcc)	Speed Bin	Comments
KM68512AL/L-L	0~70℃	5V ± 10%	45*/55/70ns	Commercial
KM68512ALI/LI-L	-40~85℃	5V ± 10%	70/100ns	Industrial

^{*} The parameter is measured with 30pF test load.

PARAMETER LIST FOR EACH SPEED BIN

						Spe	ed Bins	i .			
Parameter List		Symbol	45	ns*	58	ins	70	ins	10	Ons	Units
			Min	Max	Min	Max	Min	Max	Min	Max	
Read	Read cycle time	tRC	45	-	55	-	70	-	100	-	ns
	Address access time	taa	-	45	-	55	-	70	-	100	ns
	Chip select to output	` tco	-	45	-	55	-	70	-	100	ns
	Output enable to valid output	tOE	-	25	-	25	-	35	-	50	ns
	Chip select to low-Z output	tLZ	10	-	10	-	10	-	10	-	ns
	Output enable to low-Z output	toLZ	· 5	-	5	-	5	-	5	-	ns
	Chip disable to high-Z output	tHZ	0	20	0	20	0	25	0	30	ns
	Output disable to high-Z output	tonz	0	20	0	20	0	25	. 0	30	ns
	Output hold from address change	ton	10	-	10	-	10	-	10	-	ns
Write	Write cycle time	twc	45		55	-	70	-	100	-	ns
	Chip select to end of write	tcw	45	-	45	-	60	-	80	-	ns
	Address set-up time	tAS	0	-	0	-	0	-	0	-	ns
	Address valid to end of write	tAW	45	-	45	-	60	-	80	-	ns
	Write pulse width	tWP	40	-	40	-	50	-	60	-	ns
	Write recovery time	twr	0	-	0	-	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	20	0	20	0	25	0	30	ns .
	Data to write time overlap	tDW	25	-	25	-	30	-	40	-	ns
	Data hold from write time	tDH	0	-	0	-	0	-	0	-	ns
	End write to output low-Z	tow	5	-	5	-	5	-	10	-	ns

^{*} The parameters is measured with 30pf test load.



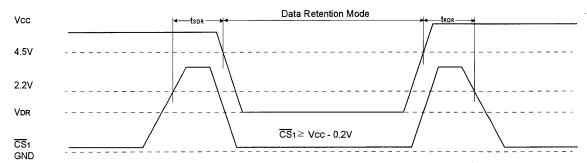
DATA RETENTION CHARACTERISTICS

Item		Symbol	Test Condi	Test Condition*		Typ**	Max	Unit
Vcc for data retention VDR		<u> </u>	*** CS 1≥Vcc-0.2V		2.0	-	5.5	٧
Data retention current	lan	KM68512AL/L-L	Vcc=3.0V CS1≥ Vcc-0.2V	L-Ver LL-Ver	-	1 0.5	50 10	μA
	IDR	KM68512ALI/LI-L		L-Ver LL-Ver	-	-	50 25	
Data retention set-up time	tSDF	?	See data retention	1	0	-	-	
Recovery time	tRDF	₹	waveform		5	-	-	ms

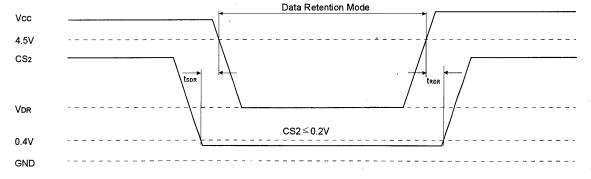
^{* 1)} Commercial Product : Ta=0 to 70 °C, unless otherwise specified 2) Industrial Product : Ta=-40 to 85 °C, unless otherwise specified ** Ta=25 °C

DATA RETENTION WAVE FORM

1) CS₁ Controlled



2) CS2 Controlled



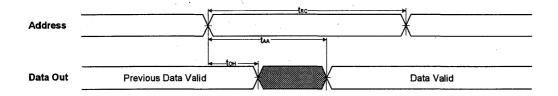


^{***} $\overline{CS}_1 \ge Vcc-2.0V$, CS₂ $\ge Vcc-2.0V$ (\overline{CS}_1 controlled) or CS₂ $\le 0.2V$ (CS₂ controlled)

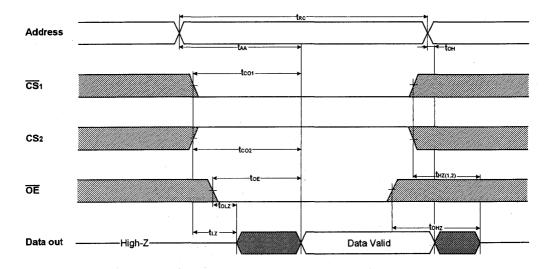
TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (1) (Address Controlled)

(CS1=OE=VIL, CS2= WE=VIH)



TIMING WAVEFORM OF READ CYCLE(2) (WE=VIH)

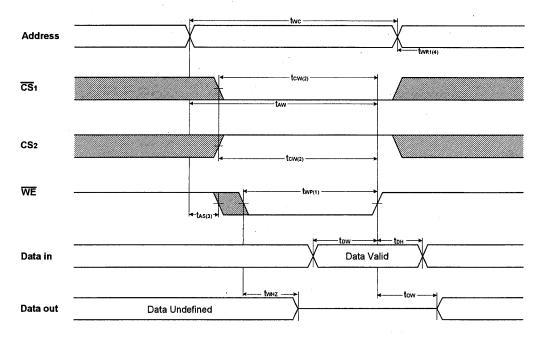


NOTES (READ CYCLE)

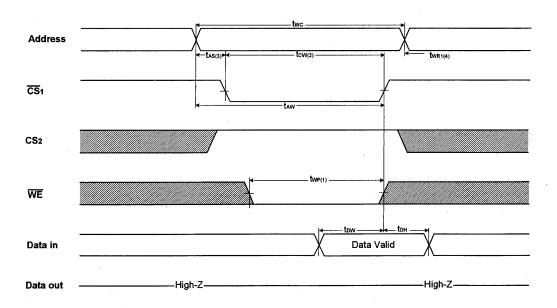
- 1. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
- 2. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device interconnection.



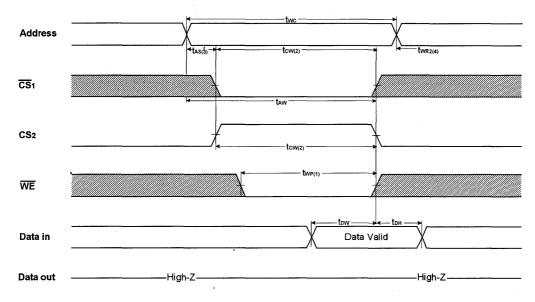
TIMING WAVEFORM OF WRITE CYCLE(1) (WE Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) (CS1 Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) (CS2 Controlled)



NOTES (WRITE CYCLE)

- 1. A write occurs during the overlap of low \overline{CS}_1 , high CS_2 and low \overline{WE} . A write begins at the latest transition among \overline{CS}_1 goes low, CS_2 going high and \overline{WE} going low: A write ends at the earliest transition among \overline{CS}_1 going high, CS_2 going low and \overline{WE} going high, tWP is measured from the begining of write to the end of write.
- 2. tCW is measured from the $\overline{\text{CS}}_1$ going low or CS2 going high to the end of write.
- 3. tAS is measured from the address valid to the beginning of write.
- 4. tWR is measured from the end of write to the address change. tWR1 applied in case a write ends as CS1 or WE going high tWR2 applied in case a write ends as CS2 going to low.

FUNCTIONAL DESCRIPTION

CS ₁	CS2	WE	ŌĒ	Mode	I/O Pin	Current Mode
Н	X	Х	Х	Power Down	High-Z	ISB, ISB1
X	L	X	Х	Power Down	High-Z	ISB, ISB1
L	H ·	Н	Н	Output Disable	High-Z	lcc
L	Н	Н	L	Read	Dout	lcc
Ľ	Н	L	Х	Write	Din	lcc

^{*} X means don't care



128K x8 bit Low Power CMOS Static RAM

FEATURES

• Process Technology: 0.6

m CMOS

Organization: 128Kx8

• Power Supply Voltage : Single 5.0V ± 10%

Low Data Retention Voltage: 2V(Min)

. Three state output and TTL Compatible

· Package Type: JEDEC Standard

32-DIP, 32-SOP, 32-TSOP I R/F

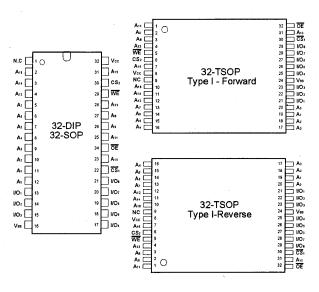
GENERAL DESCRIPTION

The KM681000B family is fabricated by SAMSUNG's advanced CMOS process technology. The family can support various operating temperature ranges and have various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

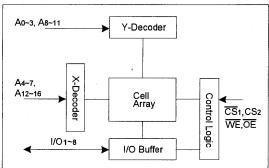
PRODUCT FAMILY

Paradica.	0			Power Di	ssipation
Product Family	Operating Temperature	Speed	PKG Type	Standby (IsB1, Max)	Operating (Icc2)
KM681000BL	Commercial(0~7°C)	55/70ns	32-DIP,32-SOP	100 <i>µ</i> A	
KM681000BL-L	Commercial(0-7-0)	33/7 0118	32-TSOP I R/F	20 <i>µ</i> A	
KM681000BLE	Extended(-25~85°C)	70/100ns	32-SOP	100μΑ	70mA
KM681000BLE-L	Extended(-25 *05 0)	70/100113	32-TSOP I R/F	50 <i>μ</i> A	701114
KM681000BLI	Industrial(-40~85℃)	Industrial(-40~85°C) 70/100ns 32-		100 <i>µ</i> A	
KM681000BLI-L	middstrai(-40 -05 0)	70/100/19	32-TSOP I R/F	50 <i>µ</i> Å	

PIN DESCRIPTION



FUNCTIONAL BLOCK DIAGRAM



Name	Function
A0~A16	Address Inputs
WE	Write Enable Input
CS1,CS2	Chip Select Inputs
ŌĒ	Output Enable Input
I/O1~I/O18	Data Inputs/Outputs
Vcc	Power
Vss	Ground
N.C	No Connection

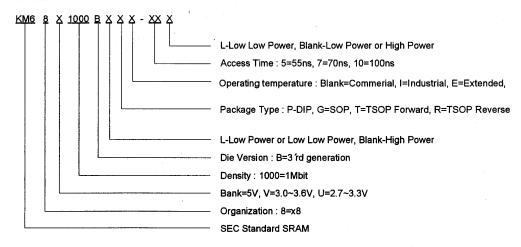


PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST

	lal Temp Product 0~70℃)		Temp Products 5~85℃)	Industrial Temp Products (-40~85°C)			
Part Name	Function	Function Part Name		Function Part Name Function Part Name		Part Name	Function
KM681000BLP-5	32-DIP,55ns,L-pwr	KM681000BLGE-7	32-SOP,70ns,L-pwr	KM681000BLGI-7	32-SOP,70ns,L-pwr		
KM681000BLP-5L	32-DIP,55ns,LL-pwr	KM681000BLGE-7L	32-SOP,70ns,LL-pwr	KM681000BLGI-7L	32-SOP,70ns,LL-pwr		
KM681000BLP-7	32-DIP,70ns,L-pwr	KM681000BLGE-10	32-SOP,100ns,L-pwr	KM681000BLGI-10	32-SOP,100ns,L-pwr		
KM681000BLP-7L	32-DIP,70ns,LL-pwr	KM681000BLGE-10L	32-SOP,100ns,LL-pwr	KM681000BLGI-10L	32-SOP,100ns,LL-pwr		
KM681000BLG-5	32-SOP,55ns,L-pwr	KM681000BLTE-7	32-TSOP F,70ns,L-pwr	KM681000BLTI-7	32-TSOP F,70ns,L-pwr		
KM681000BLG-5L	32-SOP,55ns,LL-pwr	KM681000BLTE-7L	32-TSOP F,70ns,LL-pwr	KM681000BLTI-7L	32-TSOP F,70ns,LL-pwr		
KM681000BLG-7	32-SOP,70ns,L-pwr	KM681000BLTE-10	32-TSOP F,100ns,L-pwr	KM681000BLTI-10	32-TSOP F,100ns,L-pwr		
KM681000BLG-7L	32-SOP,70ns,LL-pwr	KM681000BLTE-10L	32-TSOP F,100ns,LL-pwr	KM681000BLTI-10L	32-TSOP F,100ns,LL-pwi		
KM681000BLT-5	32-TSOP F,55ns,L-pwr	KM681000BLRE-7	32-TSOP R,70ns,L-pwr	KM681000BLRI-7	32-TSOP R,70ns,L-pwr		
KM681000BLT-5L	32-TSOP F,55ns,LL-pwr	KM681000BLRE-7L	32-TSOP R,70ns,LL-pwr	KM681000BLRI-7L	32-TSOP R,70ns,LL-pwr		
KM681000BLT-7	32-TSOP F,70ns,L-pwr	KM681000BLRE-10	32-TSOP R,100ns,L-pwr	KM681000BLRI-10	32-TSOP R,100ns,L-pwr		
KM681000BLT-7L	32-TSOP F,70ns,LL-pwr	KM681000BLRE-10L	32-TSOP R,100ns,LL-pwr	KM681000BLRI-10L	32-TSOP R,100ns,LL-pw		
KM681000BLR-5	32-TSOP R,55ns,L-pwr		·				
KM681000BLR-5L	32-TSOP R,55ns,LL-pwr	•					
KM681000BLR-7	32-TSOP R,70ns,L-pwr	-					
KM681000BLR-7L	32-TSOP R,70ns,LL-pwr						

ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	VIN,VOUT	-0.5 to 7.0	V	-
Voltage on Vcc supply relative to Vss	Vcc	-0.5 to 7.0	V	-
Power Dissipation	PD	1.0	W	_
Storage temperature	Тѕтс	-65 to 150	င	-
		0 to 70	ပ	KM681000BL/L-L
Operating Temperature	TA	-25 to 85	ာ	KM681000BLE/LE-L
		-40 to 85	°	KM681000BLI/LI-L
Soldering temperature and time	TSOLDER	260℃, 10sec (Lead Only)	-	-

^{*} Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*

Item	Symbol	Min	Typ**	Max	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input high voltage	ViH	2.2	-	Vcc+0.5	V
Input low voltage	VIL	-0.5***	-	0.8	V

^{* 1)} Commercial Product : Ta=0 to 70 ℃, unless otherwise specified 2) Extended Product : Ta=-25 to 85 ℃, unless otherwise specified

CAPACITANCE* (f=1MHz, Ta=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	CIN	Vin=0V	-	. 6	pF
Input/Output capacitance	Cio	Vio=0V	-	8	pF

^{*} Capacitance is sampled not 100% tested



³⁾ Industrial Product : Ta=-40 to 85 °C , unless otherwise specified

^{**} Ta=25℃

^{***} VIL(min)=-3.0V for \leq 50ns pulse width

DC AND OPERATING CHARACTERISTICS

ı	tem	Symbol	Test Con	ditions*	Mi	Typ**	Max	Unit
Input leakage cur	rent	lu	Vin=Vss to Vcc	Vin=Vss to Vcc		-	1	μA
Output leakage cu	urrent	lLO	CS1=VIH or CS2=VIL or WE=VIL, VIO=Vss to Vcc		-1	-	1	μA
Operating power	supply current	Icc	CS1=VIL, CS2=VIH, VIN=	VIH or VIL, IIO=0mA	-	7	15**	mA
Average operating current		ICC1	Cycle time=1 µs 100% o	•	-	-	10***	mA
		ICC2	IIO=0mA CS1=VIL,CS2=VIH Min cycle, 100% duty		-	-	70	mA
Output low voltage	e	Vol	IoL=2.1mA		-	-	0.4	٧
Output high voltag	је	Voн	Iон=-1.0mA		2.4	-	-	٧
Standby Current(TTL)	ISB	CS1=VIH, CS2=VIL		-	-	3	mA
	KM681000BL KM681000BL-L		CS1≥Vcc-0.2V	L (Low Power) LL (Low Low Power)	- 1	-	100 20	μA μA
Standby Current (CMOS)	KM681000BLE KM681000BLE-L	ISB1 CS2≥Vcc-0.2V or CS2≤0.2V	L (Low Power) LL (Low Low Power)	-	-	100 50	μA μA	
	KM681000BLI KM681000BLI-L		Other input=0~Vcc	L (Low Power) LL (Low Low Power)	-	-	100 50	μA μA

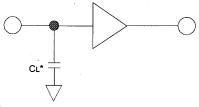
^{* 1)} Commercial Product : Ta=0 to 70°C, Vcc=5.0V±10%, unless otherwise specified 2) Extended Product : Ta=-25 to 85°C, Vcc=5.0V±10%, unless otherwise specified 2) Industrial Product : Ta=-40 to 85°C, Vcc=5.0V±10%, unless otherwise specified *** 20mA for Extended and Industrial Products *** 15mA for Extended and Industrial Products

A.C CHARACTERISTICS

TEST CONDITIONS (1.Test Load and Test Input/Output Reference)*

Item	Value	Remark
Input pulse level	0.8 to 2.4V	-
Input rising & falling time	5ns	-
input and output reference voltage	1.5V	-
Output load (See right)	CL=100pF+1TTL	-

^{*} See DC Operating conditions



* Including scope and jig capacitance

TEST CONDITIONS (2. Temperature and Vcc Conditions)

Product Family	Temperature	Power Supply(Vcc)	Speed Bin	Comments
KM681000BL/L-L	0~70℃	5.0V±10%	55/70ns	Commercial
KM681000BLE/LE-L	-25~85℃	5.0V±10%	70/100ns	Extended
KM681000BLI/LI-L	-40~85℃	5.0V±10%	70/100ns	Industrial

PARAMETER LIST FOR EACH SPEED BIN

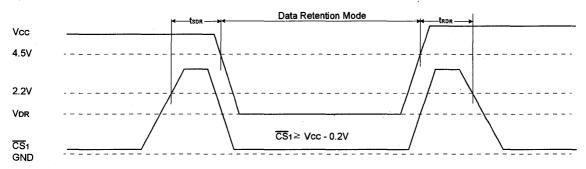
					Spec	d Bins			
	Parameter List	Symbol	55ns		70ns		100ns		Units
			Min	Max	Min	Max	Min	Max	
Read	Read cycle time	tRC	55	-	70	-	100	-	ns
	Address access time	tAA	-	55	-	70	-	100	ns
	Chip select to output	tCO1,tCO2	-	55		70	-	100	ns
	Output enable to valid output	tOE	-	25	-	35	-	50	ns
	Chip select to low-Z output	tLZ1,tLZ2	10	-	10	-	10	-	ns
	Output enable to low-Z output	tolz	5	-	5	-	5	-	ns
	Chip disable to high-Z output	tHZ1,tHZ2	0	20	0	25	0	30	ns
	Output disable to high-Z output	tonz	0	20	0	25	0	30	ns
	Output hold from address change	tон	10	-	10	-	10	-	ns
Write	Write cycle time	twc	55	-	70	-	100	-	ns
	Chip select to end of write	tcw	45	-	60	-	80	-	ns
	Address set-up time	tAS	0	-	0	-	0	-	ns
	Address valid to end of write	tAW	45	-	60	-	80	-	ns
	Write pulse width	tWP	40	-	50	-	60	-	ns
	Write recovery time	twr	0	-	0	-	0	-	ns
	Write to output high-Z	twnz	0	20	0	25	0	30	ns
4	Data to write time overlap	tDW	25	-	30	-	40	-	ns
	Data hold from write time	tDH	0	-	0	-	0	-	ns
	End write to output low-Z	tow	5	-	5	-	5	_	ns

DATA RETENTION CHARACTERISTICS

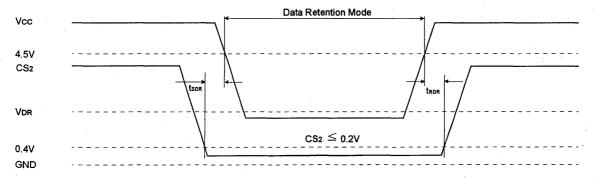
Item		Symbol Test Condition*		Min	Typ**	Max	Unit		
Vcc for data retention	VDR		<u>CS</u> 1***≥Vcc-0.2V	2.0	-	5.5	V		
		KM681000BL KM681000BL-L		L-Ver LL-Ver	-	1 0.5 - -	50 10 50 25		
Data retention current	IDR K	KM681000BLE KM681000BLE-L	Vcc=3.0V CS1≥ Vcc-0.2V	L-Ver LL-Ver				μA	
		KM681000BLI KM681000BLI-L		L-Ver LL-Ver	-	-	50 25		
Data retention set-up time	tRD	₹	See data retention wavefo		0	-	•	ms	
Recovery time	tRDF	₹	Cee data reterition	i wavelollii	5	-	-	7 1118	

DATA RETENTION TIMING DIAGRAM

1) CS1 Controlled



2) CS2 controlled





^{* 1)} Commercial Product : Ta=0 to 70 °C, unless otherwise specified 2) Extended Product : Ta=-25 to 85 °C, unless otherwise specified 2) Industrial Product : Ta=-40 to 85 °C, unless otherwise specified

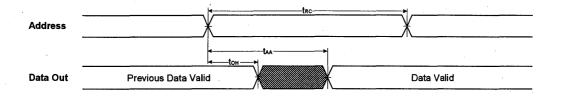
^{**} TA=25°C

^{***} $\overline{\text{CS}}_1 \geq \text{Vcc-0.2V,CS}_2 \geq \text{Vcc-0.2V}(\overline{\text{CS}}_1 \text{ controlled}) \text{ or CS}_2 \leq 0.2 \text{V}(\text{CS}_2 \text{ controlled})$

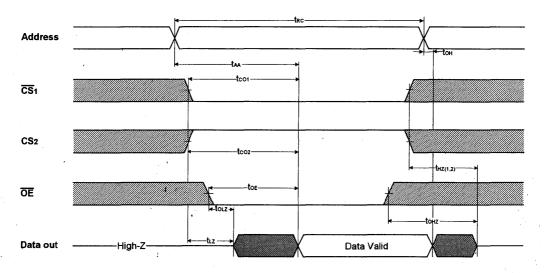
TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (1) (Address Controlled)

(CS1=OE=VIL, CS2= WE= VIH)



TIMING WAVEFORM OF READ CYCLE (WE=VIH)

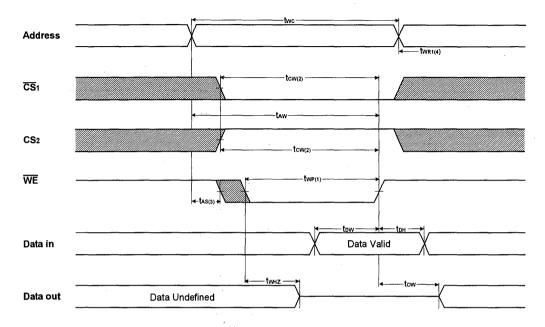


NOTES (READ CYCLE)

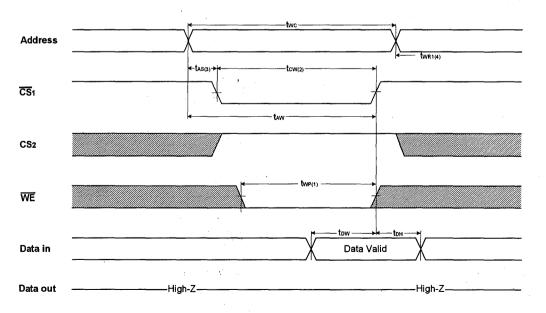
- 1. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
- 2. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device.



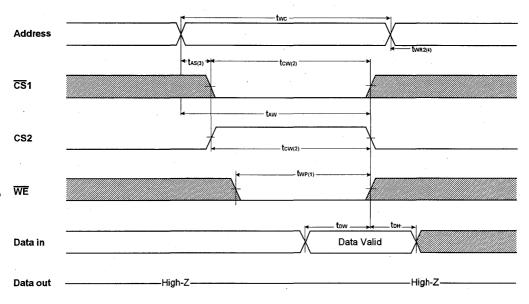
TIMING WAVEFORM OF WRITE CYCLE (1) (WE Controlled)



TIMING WAVEFORM OF WRITE CYCLE (2) (CS1 Controlled)



TIMING WAVEFORM OF WRITE CYCLE (2) (CS2 Controlled)



NOTES (WRITE CYCLE)

- 1. A write occurs during the overlap of low \overline{CS}_1 , high CS_2 and low \overline{WE} . A write begins at the latest transition among \overline{CS}_1 going low, CS_2 going low, CS_2 going low, CS_2 going low and CS_1 going low and CS_2 going low and CS_3 going low and CS_4 going high, CS_2 going low and CS_4 going high, CS_4 going high and CS_4 going high a
- 2. tCW is measured from the later of CS1 going low or CS2 going high to the end of write.
- 3. tAS is measured from the address calld to the beginning of write.
- 4. tWR is measured from the end of write to the address change. tWR1 applied in case a write ends at CS₁, or WE going high, tWR2 applied in case a write ends at CS₂ going to low.

FUNCTIONAL DESCRIPTION

CS ₁	CS2	WE	ŌĒ	Mode	I/O Pin	Current Mode
Н	Х	Х	Х	Power Down	High-Z	ISB,ISB1
Х	L	Х	X.	Power Down	High-Z	ISB,ISB1
L	Н	Н	Н	Output Disable	High-Z	Icc
L	Н	Н	L	Read	Dout	lcc
L	Н	L	Х	Write	Din	Icc

^{*} X means don't care



128K x8 bit Low Power CMOS Static RAM

FEATURES

• Process Technology: 0.4 m CMOS

· Organization: 128K x8

Power Supply Voltage: Single 5.0V±10%
 Low Data Retention Voltage: 2V(Min)
 Three state output and TTL Compatible

· Package Type : JEDEC Standard

32-DIP, 32-SOP, 32-TSOP(I)-Forward/Reverse

GENERAL DESCRIPTION

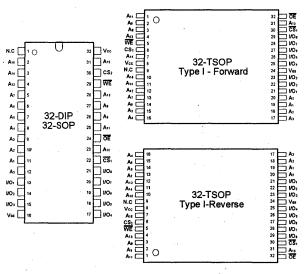
The KM681000C family is fabricated by SAMSUNG's advanced CMOS process technology. The family can support various operating temperature ranges and have various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

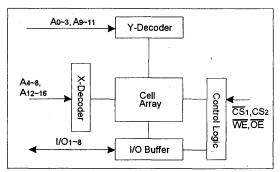
					Power Di	ssipation	
Product Family	Operating Temperature	Vcc Range(V)	Speed	PKG Type	Standby (Iss1, Max)	Operating (ICC2)	
KM681000CL KM681000CL-L	Commercial(0~70°C)	4.5~5.5V	45*/55/70ns	32-DIP,32-SOP 32-TSOP(I) R/F	50μA 10μA	00 4	
KM681000CLI-L	Industrial(-40~85℃)	4.5~5.5V	55*/70/85ns	32-DIP,32-SOP 32-TSOP(I) R/F	50μA 15μA	- 90mA	

^{*}The parameter is measured with 30pF test load

PIN DESCRIPTION



FUNCTIONAL BLOCK DIAGRAM



Name	Function
A0~A16	Address Inputs
WE	Write Enable Input
<u>CS</u> 1,CS2	Chip Select Input
<u>OE</u>	Output Enable Input
I/O1~I/O8	Data Inputs/Outputs
Vcc	Power (+5.0V)
Vss	Ground
N.C	No Connection

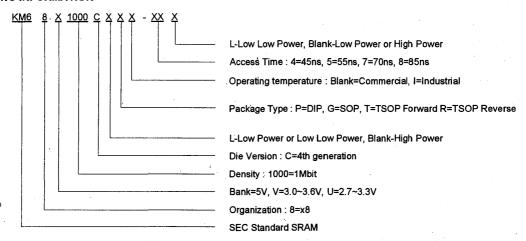


PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST

Comm	nercial Temp Product (0~70℃)	Indus	trial Temp Products (-40~85℃)			
Part Name	Function	Part Name	Function			
KM681000CLP-4	32-DIP, 45ns, L-pwr	KM681000CLGI-5	32-SOP, 55ns, L-pwr			
KM681000CLP-5	32-DIP, 55ns, L-pwr	KM681000CLGI-7	32-SOP, 70ns, L-pwr			
KM681000CLP-7	32-DIP, 70ns, L-pwr	KM681000CLGI-8	32-SOP, 85ns, L-pwr			
KM681000CLP-4L	32-DIP, 45ns, LL-pwr	KM681000CLGI-5L	32-SOP, 55ns, LL-pwr			
KM681000CLP-5L	32-DIP, 55ns, LL-pwr	KM681000CLGI-7L	32-SOP, 70ns, LL-pwr			
KM681000CLP-7L	32-DIP, 70ns, LL-pwr	KM681000CLGI-8L	32-SOP, 85ns, LL-pwr			
KM681000CLG-4	32-SOP, 45ns, L-pwr	KM681000CLTI-5	32-TSOP(I) F, 55ns, L-pwr			
KM681000CLG-5	32-SOP, 55ns, L-pwr	KM681000CLTI-7	32-TSOP(I) F, 70ns, L-pwr			
KM681000CLG-7	32-SOP, 70ns, L-pwr	KM681000CLTI-8	32-TSOP(I) F, 85ns, L-pwr			
KM681000CLG-4L	32-SOP, 45ns, LL-pwr	KM681000CLTI-5L	32-TSOP(I) F, 55ns, LL-pwr			
KM681000CLG-5L	32-SOP, 55ns, LL-pwr	KM681000CLTI-7L	32-TSOP(I) F, 70ns, LL-pwr			
KM681000CLG-70L	32-SOP, 70ns, LL-pwr	KM681000CLTI-8L	32-TSOP(I) F, 85ns, LL-pwr			
KM681000CLT-4	32-TSOP(I) F, 45ns, L-pwr	KM681000CLRI-5	32-TSOP(I) R, 55ns, L-pwr			
KM681000CLT-5	32-TSOP(I) F, 55ns, L-pwr	KM681000CLRI-7	32-TSOP(I) R, 70ns, L-pwr			
KM681000CLT-7	32-TSOP(I) F, 70ns, L-pwr	KM681000CLRI-8	32-TSOP(I) R, 85ns, L-pwr			
KM681000CLT-4L	32-TSOP(I) F, 45ns, LL-pwr	KM681000CLRI-5L	32-TSOP(I) R, 55ns, LL-pwr			
KM681000CLT-5L	32-TSOP(I) F, 55ns, LL-pwr	KM681000CLRI-7L	32-TSOP(I) R, 70ns, LL-pwr			
KM681000CLT-70L	32-TSOP(I) F, 70ns, LL-pwr	KM681000CLRI-8L	32-TSOP(I) R, 85ns, LL-pwr			
KM681000CLR-4	32-TSOP(I) R, 45ns, L-pwr					
KM681000CLR-5	32-TSOP(I) R, 55ns, L-pwr	•				
KM681000CLR-7	32-TSOP(I) R, 70ns, L-pwr					
KM681000CLR-4L	32-TSOP(I) R, 45ns, LL-pwr					
KM681000CLR-5L	32-TSOP(I) R, 55ns, LL-pwr	'				
KM681000CLR-70L	32-TSOP(I) R, 70ns, LL-pwr	-				

ORDERING INFORMATION





ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	VIN, VOUT	-0.5 to 7.0	V	-
Voltage on Vcc supply relative to Vss	Vcc	-0.5 to 7.0	٧.	
Power Dissipation	PD	1.0	W	<u>-</u>
Storage temperature	Тѕтс	-65 to 150	c	_
Operating Temperature	TA	0 to 70	င	KM681000CL/L-L
		-40 to 85	င	KM681000CLI/LI-L
Soldering temperature and time	TSOLDER	260°C, 10sec (Lead Only)	· -	·

^{*} Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*

Item	Symbol	Min	Typ**	Max	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	. 0	0	. 0	V
Input high voltage	ViH	2.2	· -	Vcc+0.5	V
Input low voltage	VIL	-0.5***	-	0.8	V

^{* 1)} Commercial Product : Ta=0 to 70 $^{\circ}$ C, unless otherwise specified

CAPACITANCE* (f=1MHz, TA=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	Cin	VIN=0V	-	6	pF
Input/Output capacitance	Cio	Vio=0V	-	8	pF

^{*} Capacitance is sampled not 100% tested

²⁾ Industrial Product : Ta=-40 to 85°C, unless otherwise specified

^{**} Ta=25℃

^{***} VIL(min)=-3.0V for \leq 50ns pulse width

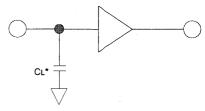
DC AND OPERATING CHARACTERISTICS

I	tem	Symbol	Test Conditions*			Typ**	Max	Unit
Input leakage cu	rrent	lu	Vin=Vss to Vcc		-1	-	1	μA
Output leakage	current	lLO	CS1=VIH or CS2=VIL or VIO=Vss to Vcc			-	1	μA
Operating power	supply current	Icc	CS1=VIL, CS2=VIH,	Read	-	-	15	mA
		l icc	VIN=VIH or VIL, IIO=0mA Write				35	
		ICC1	Cycle time=1 µs 100% duty	Read	-	-	15	mA
Average operating current		ICC1	'CS1≤0.2V, CS2≥Vcc-0.2V, lio=0mA	Write			35	ımA
, worder operation	Average operating current		lio=0mA, CS1=ViL,CS2=Viн Min cycle, 100% duty		-	-	90	mA
Output low volta	ge	Vol	IoL=2.1mA		-	-	0.4	٧
Output high volta	age	Vон	Iон=-1.0mA		2.4	-	-	٧
Standby Current	(TTL)	ISB	CS1=VIH, CS2=VIL		-	-	3	mA
Standby Current (CMOS)	KM681000C KM681000CL-L	ISB1	CS 1≥ Vcc-0.2V CS2≥ Vcc-0.2V or	L(Low Power) LL(L Low Power)	-	-	50 10	μA
	KM681000CLI KM681000CLI-L	1381	CS2 ≤ 0.2V Other input=0~Vcc	L(Low Power) LL(L Low Power)	-	- -	50 15	μA

A.C CHARACTERISTICS

TEST CONDITIONS (1.Test Load and Test Input/Output Reference)*

Item	Value	Remark
input pulse level	0.8 to 2.4V	-
Input rising & falling time	5ns	-
input and output reference voltage	1.5V	-
Output load (See right)	CL=100pF+1TTL **CL=30pF+1TTL	



* Including scope and jig capacitance

^{* 1)} Commercial Product : Ta=0 to 70 °C , Vcc=5V \pm 10% Unless otherwise specified 2) Industrial Product : Ta=-40 to 85 °C , Vcc=5V \pm 10% Unless otherwise specified
** Ta=25 °C

^{*} See DC Operating conditions

** Test load for 45ns(Commercial product)/55ns(Industrial product)

TEST CONDITIONS (2. Temperature and Vcc Conditions)

Product Family	Temperature	Power Supply(Vcc)	Speed Bin	Comments
KM681000CL/L-L	0~70℃	5V±10%	45*/55/70ns	Commercial
KM681000CLI/LI-L	-40~85℃	5V±10%	55*/70/85ns	Industrial

^{*}The parameter is measured with 30pF test load

PARAMETER LIST FOR EACH SPEED BIN

						Spee	d Bins				
	Parameter List	Symbol	45ns		55ns		70ns		85ns		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
Read	Read cycle time	tRC	45	-	55	-	70	-	85	-	ns
	Address access time	tAA	-	45	-	55	-	70	-	85	ns
	Chip select to output	tco1,tco	-	45	-	55	-	70		85	ns
	Output enable to valid output	tOE	-	20	-	25	-	35	-	40	ns
	Chip select to low-Z output	tLZ1,tLZ2	10	· -	10	-	10	-	10	-	ns
	Output enable to low-Z output	toLZ	5	-	5	-	5	-	5	-	ns
	Chip disable to high-Z output	tHZ1,tHZ2	0	15	0	20	0	25	0	25	ns
	Output disable to high-Z output	tonz	0	15	0	20	0	25	0	25	ns
	Output hold from address change	tон	10	-	10	-	10	-	10	-	ns
Write	Write cycle time	tWC	45	-	55	-	70	-	85	-	ns
	Chip select to end of write	tcw	40	-	45	-	60	-	70	-	ns
	Address set-up time	tAS	0	-	. 0	-	0	-	0	-	ns
	Address valid to end of write	tAW	40	-	45	- ,	60	-	70 .	,-	ns
	Write pulse width	tWP	35	-	40	-	50	-	60	-	ns
	Write recovery time	tWR	0	-	0	_	0	-	0	-	ns
	Write to output high-Z	twnz	0	15	0	20	0	25	0	25	ns
	Data to write time overlap	tDW	25	-	25	-	30	-	35	-	ns
	Data hold from write time	tDH	0	-	0	-	0	-	0	-	ns
	End write to output low-Z	tow	5	-	5	-	5	-	5	-	ns

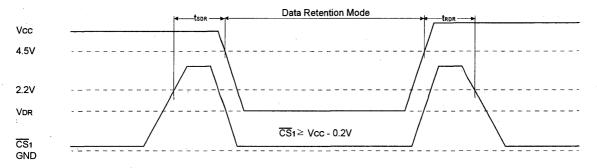
DATA RETENTION CHARACTERISTICS

Item	Symbol VDR		Test Condition* CS1*** ≥ Vcc-0.2V		Min 2.0	Тур**	Max 5.5	Unit
Vcc for data retention								
Data retention current	İDR	KM681000CL KM681000CL-L	Vcc=3.0V CS 1≥Vcc-0.2V	L-Ver LL-Ver	- -	1 0.5	20 10	μA
		KM681000CLI KM681000CLI-L		L-Ver LL-Ver	-	-	25 10	
Data retention set-up	tsdr		See data retention waveform		0	-	-	ms
Recovery time tRDR		See data retention wavelonin		5	-	•] ""5	

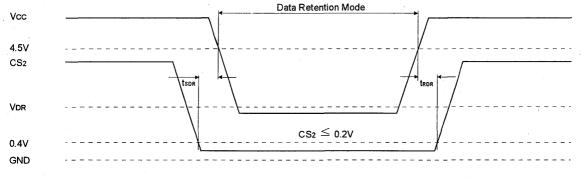
^{* 1)} Commercial Product : Ta=0 to 70℃, unless otherwise specified 2) Industrial Product : Ta=-40 to 85℃, unless otherwise specified

DATA RETENTION TIMING DIAGRAM

1) CS1 Controlled









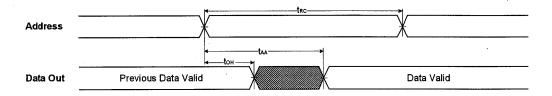
^{**} TA=25℃

^{***} CS1>Vcc-0.2V,CS2>Vcc-0.2V(CS1 controlled) or CS2≤0.2V(CS2 controlled)

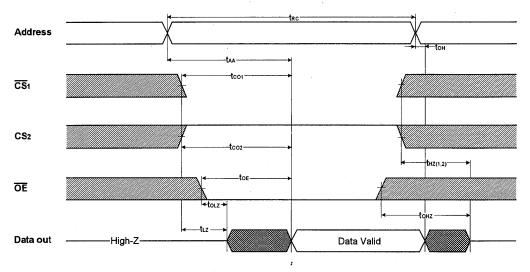
TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (1) (Address Controlled)

(CS1=OE=VIL, CS2=WE=VIH)



TIMING WAVEFORM OF READ CYCLE (WE=VIH)

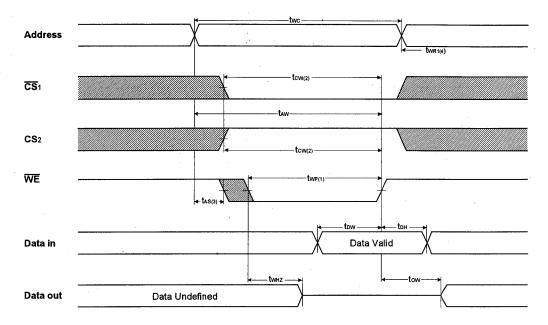


NOTES (READ CYCLE)

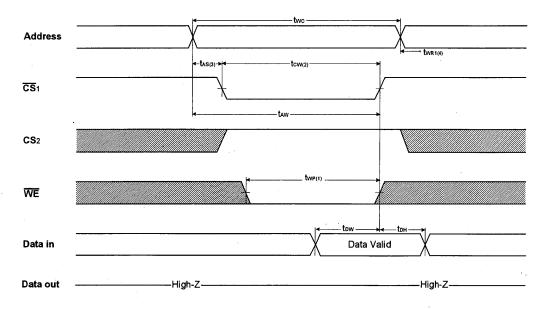
- 1. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
- 2. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device.



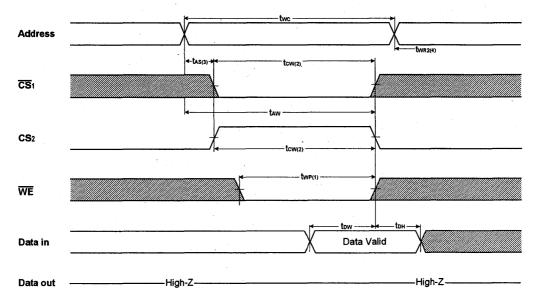
TIMING WAVEFORM OF WRITE CYCLE (1) (WE Controlled)



TIMING WAVEFORM OF WRITE CYCLE (2) (CS1 Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) (CS2 Controlled)



NOTES (WRITE CYCLE)

- 1. A write occurs during the overlap of low CS1, high CS2 and low WE. A write begins at the latest transition among CS1 going low, CS2 going high and WE going low. A write ends at the earliest transition among CS1 going high, CS2 going low and WE going high, tWP is measured from the beginning or write to the end of write.
- 2. TCW is measured from the later of CS1 going low or CS2 going high to the end of write.
- 3. tAS is measured from the address calld to the beginning of write.
- 4. tWR is measured from the end of write to the address change. tWR1 applied in case a write ends at CS1, or WE going high, tWR2 applied in case a write ends at CS2 going to low.

FUNCTIONAL DESCRIPTION

CS ₁	CS2	WE	ŌĒ	Mode	I/O Pin	Current Mode
Н	X	Х	х	Power Down	High-Z	ISB,ISB1
·X	L	Х	Х	Power Down	High-Z	ISB,ISB1
L	Н	Н	Н	Output Disable	High-Z	Icc
L	Η	Н	L	Read	Dout	Icc
L	н	L	Х	Write	Din	lcc

^{*} X means don't care



64K x16 bit Low Power CMOS Static RAM

FEATURES SUMMARY

• Process Technology: 0.6 µm CMOS

Organization: 64K x16

Data Byte Control : LB=I/O1~8, UB=I/O9~16
 Power Supply Voltage : 5.0V ±10%

Low Data Retention Voltage: 2V(Min)

. Three state output and TTL Compatible

· Package Type : JEDEC Standard

44-TSOP(II)-Forward/Reverse

GENERAL DESCRIPTION

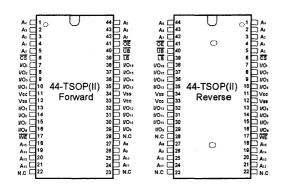
The KM6161000B family is fabricated by SAMSUNG's advanced CMOS process technology. The family can support various operating temperature ranges and has various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

n				Power Di	ssipation	
Product Family	Operating Temperature	Vcc Range(V)	Speed	Standby (IsB1, Max)	Operating (Icc2)	PKG Type
KM6161000BLT/LT-L KM6161000BLR/LR-L	Commercia (0~70℃)	4.5 to 5.5	55*/70	100/20 <i>µ</i> A	120mA	44-TSOP(II)
KM6161000BLTI/LTI-L KM6161000BLRI/LRI-L	Industrial (-40~85℃)	4.5 to 5.5	70/100	100/50 <i>µ</i> Å	12UIIIA	Forward/Reverse

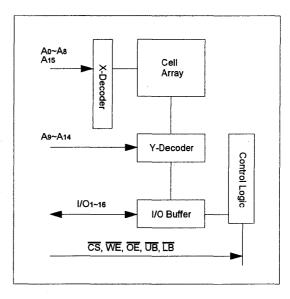
^{*} The parameter is measured with 30pF test load.

PIN DESCRIPTION



Name	Function	Name	Function
A0~A15	Address Inputs	LB	Lower Byte (I/O1~8)
WE	Write Enable Input	ŪB	Upper Byte(I/O9~16)
cs	Chip Select Input	Vcc	Power
ŌĒ	Output Enable Input	Vss	Ground
1/01~16	Data Inputs/Outputs	N.C	No Connection

FUNCTIONAL BLOCK DIAGRAM



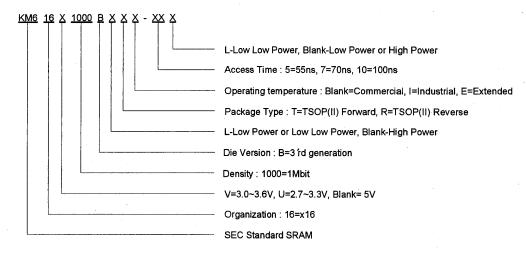


PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST

Comr	nercial Temp Product (0~70°C)	Indus	strial Temp Products (-40~85℃)
Part Name Function		Part Name	Function
KM6161000BLT-5	44-TSOP(II), F, 5V, 55ns, L-pwr	KM6161000BLTI-5	44-TSOP(II), F, 5V, 70ns, L-pwr
KM6161000BLT-5L	44-TSOP(II), F, 5V, 55ns, LL-pwr	KM6161000BLTI-5L	44-TSOP(II), F, 5V, 70ns, LL-pwr
KM6161000BLT-7	44-TSOP(II), F, 5V, 70ns, L-pwr	KM6161000BLTI-7	44-TSOP(II), F, 5V, 100ns, L-pwr
KM6161000BLT-7L	44-TSOP(II), F, 5V, 70ns, LL-pwr	KM6161000BLTI-7L	44-TSOP(II), F, 5V, 100ns, LL-pwr
KM6161000BLR-5	44-TSOP(II), R, 5V, 55ns, L-pwr	KM6161000BLRI-5	44-TSOP(II), R, 5V, 70ns, L-pwr
KM6161000BLR-5L	44-TSOP(II), R. 5V, 55ns, LL-pwr	KM6161000BLRI-5L	44-TSOP(II), R, 5V, 70ns, LL-pwr
KM6161000BLR-7	44-TSOP(II), R, 5V, 70ns, L-pwr	KM6161000BLRI-7	44-TSOP(II), R, 5V, 100ns, L-pwr
KM6161000BLR-7L	44-TSOP(II), R, 5V, 70ns, LL-pwr	KM6161000BLRI-7L	44-TSOP(II), R, 5V, 100ns, LL-pwr

ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	Vin,Vout	-0.5 to Vcc+0.5	V	
Voltage on Vcc supply relative to Vss	Vcc	-0.5 to 7.0	V	-
Power Dissipation	Po	1.0	W	-
Storage temperature	Тѕтс	-65 to 150	°C	-
On and in a Tours and the	TA	0 to 70	°C	KM6161000BLT/LT-L KM6161000BLR/LR-L
Operating Temperature		-40 to 85	င	KM6161000BLTI/LTI-L KM6161000BLRI/LRI-L
Soldering temperature and time	TSOLDER	260°C, 10sec (Lead Only)	-	-

^{*} Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*

Item	Symbol	Min	Typ**	Max	Unit
Supply voltage	Vcc	4.5	5	5.5	V
Ground	Vss	0	0	0	V
Input high voltage	ViH	2.2	. -	Vcc+0.5	V
Input low voltage	VIL	-0.5***	-	0.8	V

^{* 1)} Commercial Product : Ta=0 to 70 $^{\circ}$, unless otherwise specified 2) Industrial Product : Ta=-40 to 85 $^{\circ}$, unless otherwise specified ** Ta=25 $^{\circ}$

CAPACITANCE* (f=1MHz, TA=25℃)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	CIN	VIN=0V	-	6	pF
Input/Output capacitance	Cio	Vio=0V	-	8	pF

^{*} Capacitance is sampled not 100% tested



^{***} Vil(min)=-3.0V for \(\le \) 50ns pulse width

DC AND OPERATING CHARACTERISTICS

	Item	Symbol	Test Conditions*			Typ**	Max	Unit
Input leak	age current	lu	VIN=Vss to Vcc		-1	-	1	μA
Output lea	kage current	lLO	CS=VIH or WE=VIL, UB=VIH or LB=\	CS=ViH or WE=ViL, UB=ViH or LB=ViH, Vio=Vss to Vcc			1	μA
		lcc	CS=VIL, VIN=VIH	Read	-	-	10	mA
Operating power supply current Average operatingcurrent	ICC	or VIL, IIO=0mA	Write	-	-	35	""	
		land	Cycle time=1 µs 100% duty	Read	-	-	15	
, worde operating differen		ICC1	CS≤0.2V, lio=0mA	Write	-	-	40	mA
		ICC2	Min cycle, 100% duty, CS=VIL, Ito=0mA			-	120	mA
Output low	voltage	Vol	IoL=2.1mA		-	-	0.4	٧
Output hig	h voltage	Voн	IOH=-1.0mA		2.4	-	-	V
Standby C	urrent(TTL)	ISB	CS=ViH		-	-	3	mA
	IAMONO CANDODO NA L			L(Low Power)			100	
Standby Current (CMOS) KM6161000BL/L-L		CS ≥Vcc-0.2V	LL(L Low Power)	-	· -	20		
	ISB1	VIN≥Vcc-0.2V or VIN≤0.2V	L(Low Power)	-	-	100		
	KM6161000BLI/LI-L			LL(L Low Power)	-	-	50	μA

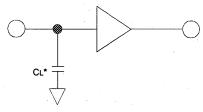
^{* 1)} Commercial Product : Ta=0 to 70 $^{\circ}\mathrm{C}$, Unless otherwise specified 2) Industrial Product : Ta=-40 to 85 $^{\circ}\mathrm{C}$, Unless otherwise specified ** TA=25 $^{\circ}\mathrm{C}$

A.C CHARACTERISTICS

TEST CONDITIONS (1.Test Load and Test Input/Output Reference)*

Item	Value	Remark
Input pulse level	0.8 to 2.4V	-
Input rising and faling time	5ns	-
input and output reference voltage	1.5V	-
Output load (See right)	CL=100 pF+1TTL **CL=30 pF+1TTL	- .

^{*} See DC Operating conditions
** Test load for 55ns product



* Including scope and jig capacitance

TEST CONDITIONS (2. Temperature and Vcc Conditions)

Product Family	Temperature	Power Supply(Vcc)	Speed Bin	Comments
KM6161000BL/L-L	0~70℃	5.0V ± 10%	55*/70ns	Commercial
KM6161000BLI/LI-L	-40~85℃	5.0V ± 10%	70/100ns	Industrial

^{*} The parameter is measured with 30pF test load.

PARAMETER LIST FOR EACH SPEED BIN

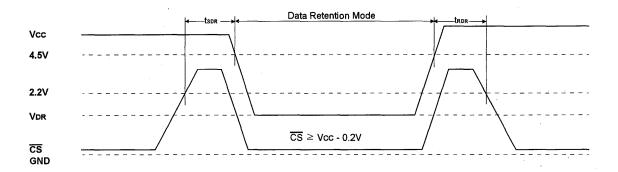
	And the second second				Spec	ed Bins			
	Parameter List	Symbol	5	5ns	70)ns	10	Ons	Units
			Min	Max	Min	Max	Min	Max	
Read	Read cycle time	tRC	55	-	70	-	100	-	ns
	Address access time	tAA		55	-	70	-	100	ns
	Chip select to output	tco	-	55	-	70	-	100	ns
	Output enable to valid output	tOE	ļ -	25	-	35	-	50	ns
	UB,LB Access Time	tBA	-	25	-	35	-	50	ns
	Chip select to low-Z output	tLZ	10	-	10	-	10	-	ns
	UB,LB enable to low-Z output	tBLZ	5	-	5	-	5	-	ns
	Output enable to low-Z output	toLZ	5	-	5	-	5	-	ns
	Chip disable to high-Z output	tHZ	0	20	0	25	0	30	ns
	UB,LB disable to high-Z output	tBHZ	0	20	0	25	0	30	ns
	Output disable to high-Z output	tonz	0	20	0	25	0	30	ns
	Output hold from address change	tон	10	-	15	-	15	-	ns
Write	Write cycle time	twc	55	-	70	-	100	-	ns
	Chip select to end of write	tcw	45	-	60	-	80	-	ns
	Address set-up time	tAS	0	-	0	-	0	-	ns
	Address valid to end of write	' tAW	45	-	60	-	80	-	ns
	Write pulse width	tWP ,	40	-	50	-	70	-	ns
	UB, LB valid to end of write	tBW	45	-	60	-	80	-	ns
	Write recovery time	twr	0	-	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	25	0	30	0	35	ns
	Data to write time overlap	tDW	25	-	30	-	40	-	ns
	Data hold from write time	tDH	0	-	0		0	-	ns
	End write to output low-Z	tow	5	-	5	-	5		ns

DATA RETENTION CHARACTERISTICS

Item		Symbol Test Condition*		Min	Typ**	Max	Unit	
Vcc for data retention	VDR		CS ≥Vcc-0.2V		2.0	-	5.5	V
Data retention current		KM6161000B Family	Vcc=3.0V	L-Ver LL-Ver	-	-	50 15	μА
	IDR	KM6161000BI Family	<u>CS</u> ≥Vcc-0.2V	L-Ver LL-Ver	-	-	50 15	μA
Data retention set-up time	tsdr	:	See data retention waveform		0	-	-	
Recovery time	tRDF	R			5	-	-	ms

^{* 1)} Commercial Product : Ta=0 to $70^\circ\mathbb{C}$, unless otherwise specified 2) Industrial Product : Ta=-40 to $85^\circ\mathbb{C}$, unless otherwise specified ** Ta=25 $^\circ\mathbb{C}$

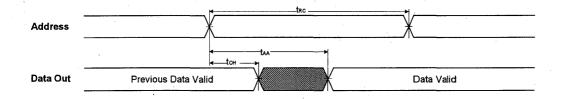
DATA RETENTION TIMING DIAGRAM



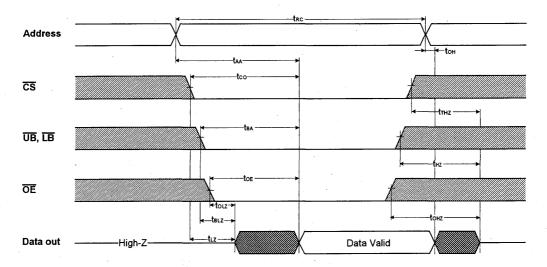
TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (1) (Address Controlled)

(CS=OE=VIL, WE=VIH, UB or and LB=VIL)



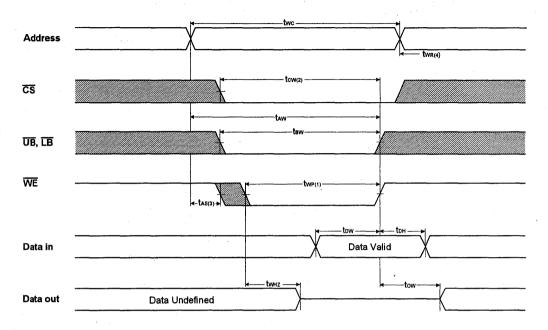
TIMING WAVEFORM OF READ CYCLE(2) (WE=VIH)



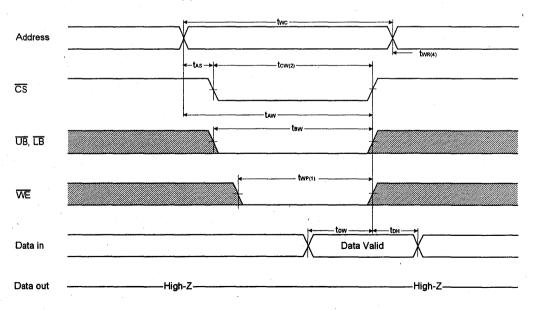
NOTES (READ CYCLE)

- 1. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
- 2. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device.

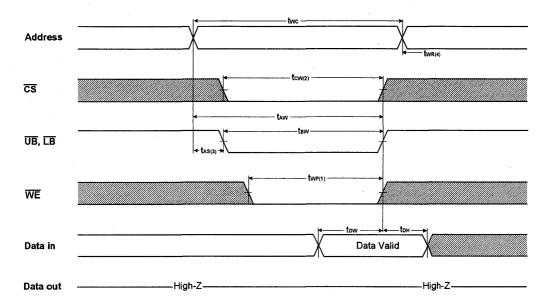
TIMING WAVEFORM OF WRITE CYCLE (1) (WE Controlled)



TIMING WAVEFORM OF WRITE CYCLE (2) (CS Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) (UB, LB Controlled)



NOTES (WRITE CYCLE)

- 1. A write occurs during the overlap (tWP) of a low \overline{CS} and low \overline{WE} . A write begins when \overline{CS} goes low and \overline{WE} goes low with asserting \overline{UB} or \overline{LB} for single byte operation or simultenious asserting \overline{UB} and \overline{LB} for double byte operation. A write ends at the earliest transition when \overline{CS} goes high and \overline{WE} goes high. The tWP is measured from the beginning of write to the end of write.
- 2. tCW is measured from the CS going low to end of write.
- 3. tAS is measured from the address valid to the beginning of write.
- 4. tWR is measured from the end or write to the address change. tWR applied in case a write ends as CS or WE going high.

FUNCTIONAL DESCRIPTION

cs	ŪB .	ŪB	WE	ŌĒ	Mode	I/O1~8	I/O9~16	Current Mode
Н	х	Х	х	Х	Not Select	High-Z	High-Z	ISB1
L	х	Х	Н	Н	Output	High-Z	High-Z	los
L	Н	Н	X	Х	Disable	High-Z	High-Z	- Icc
L	L H L	H L L	н	L	Read	Dout High-Z Dout	High-Z Dout Dout	lcc
L	L H L	H L L	L	х	Write	Din High-Z Din	High Din Din	loc

^{*} X means dont care (Must be in low or high state)



512Kx8 bit Low Power CMOS Static RAM

FEATURES

- Process Technology: 0.4

 m CMOS
- · Organization: 512Kx8
- Power Supply Voltage: Single 5V ± 10%
- . Low Data Retention Voltage: 2V(Min)
- . Three state output and TTL Compatible
- Package Type: JEDEC Standard 32-DIP, 32-SOP, 32-TSOP(II)-Forward/Reverse

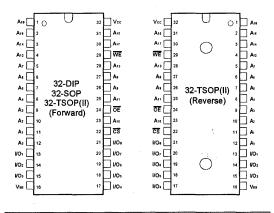
GENERAL DESCRIPTION

The KM684000A family is fabricated by SAMSUNG's advanced CMOS process technology. The family can support various operating temperature ranges and has various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

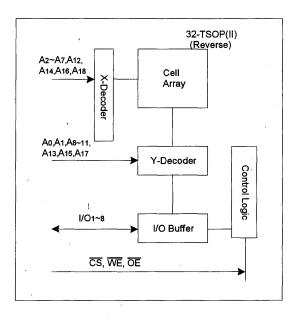
	Temperature.					
Product Family					ing	PKG Type
KM684000AL KM684000AL-L	Commercial (0~70°C)	4.5~5.5V	55/70ns	i .	90m A	32-DIP,32SOP 32-TSOP(II)-R/F
KM684000ALI KM684000ALI-L	Industrial (-40~85°C)	4.5~5.5V	70/100ns	100¼Å 50 <i>μ</i> Å	JOHA	32-SOP 32-TSOP(II)-R/F

PIN DESCRIPTION



Pin Name	Function
Aó~A18	Address Inputs
WE	Write Enable Input
<u>cs</u>	Chip Select Input
ŌĒ	Output Enable Input
I/O1~I/O8	Data Inputs/Outputs
Vcc	Power (5V)
Vss	Ground

FUNCTIONAL BLOCK DIAGRAM



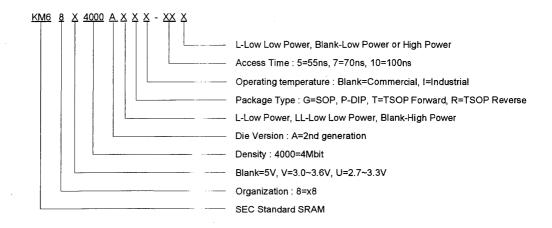


PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST

	Temp Product 70℃)	Industrial Temp Products (-40~85℃)				
Part Name	Function	Part Name	Function			
KM684000ALP-5	32-DIP, 55ns, L-pwr	KM684000ALGI-7	32-SOP,70ns, L-pwr			
KM684000ALP-5L	32-DIP, 55ns, LL-pwr	KM684000ALGI-7L	32-SOP, 70ns, LL-pwr			
KM684000ALP-7	32-DIP, 70ns, L-pwr	KM684000ALGI-10	32-SOP, 100ns, L-pwr			
KM684000ALP-7L	32-DIP, 70ns, LL-pwr	KM684000ALGI-10L	32-SOP, 100ns, LL-pwr			
KM684000ALG-5	32-SOP, 55ns, L-pwr	KM684000ALTI-7	32-TSOP(II)F, 70ns, L-pwr			
KM684000ALG-5L	32-SOP, 55ns, LL-pwr	KM684000ALTI-7L	32T-SOP(II)F, 70ns, LL-pwr			
KM684000ALG-7	32-SOP, 70ns, L-pwr	KM684000ALTI-10	32-TSOP(II)F, 100ns, L-pwr			
KM684000ALG-7L	32-SOP, 70ns, LL-pwr	KM684000ALTI-10L	32-TSOP(II)F, 100ns, LL-pwr			
KM684000ALT-5	32-TSOP(II)F, 55ns, L-pwr	KM684000ALRI-7	32-TSOP(II)R, 70ns, L-pwr			
KM684000ALT-5L	32-TSOP(II)F, 55ns, LL-pwr	KM684000ALRI-7L	32T-SOP(II)R, 70ns, LL-pwr			
KM684000ALT-7	32-TSOP(II)F, 70ns, L-pwr	KM684000ALRI-10	32-TSOP(II)R, 100ns, L-pwr			
KM684000ALT-7L	32-TSOP(II)F, 70ns, LL-pwr	KM684000ALRI-10L	32-TSOP(II)R, 100ns, LL-pwr			
KM684000ALR-5	32-TSOP(II)R, 55ns, L-pwr					
KM684000ALR-5L	32-TSOP(II)R, 55ns, LL-pwr					
KM684000ALR-7	32-TSOP(II)R, 70ns, L-pwr					
KM684000ALR-7L	32-TSOP(II)R, 70ns, LL-pwr					

ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	VIN,VOUT	-0.5 to 7.0	V	-
Voltage on Vcc supply relative to Vss	Vcc	-0.5 to 7.0	٧	. •
Power Dissipation	Po	1.0	W	-
Storage temperature	Тѕтс	-65 to 150	°C	
On anothing Towns and the	TA	0 to 70	င	KM684000AL/L-L
Operating Temperature		-40 to 85	င	KM684000ALI/LI-L
Soldering temperature and time	TSOLDER	260°C, 10sec (Lead Only)	-	-

^{*} Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*

Item	Symbol	Min	Typ**	Max	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input high voltage	ViH	2.2	-	Vcc+0.5V	V
Input low voltage	VIL	-0.5***	-	0.8	V

^{* 1)} Commercial Product : Ta=0 to 70℃, unless otherwise specified 2) Industrial Product : Ta=-40 to 85℃, unless otherwise specified

CAPACITANCE* (f=1MHz, TA=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	CIN	VIN=0V	-	8	pF
Input/Output capacitance	Сю	Vio=0V	-	, 10	pF

^{*} Capacitance is sampled, not 100% tested



^{**} Ta=25℃

^{***} VIL(min)=-3.0V for ≤ 50ns pulse width

DC AND OPERATING CHARACTERISTICS

	Item	Symbol	Test Conditions*		Min	Typ**	Max	Unit
Input leak	age current	ILI	VIN=Vss to Vcc		-1	-	1	μA
Output lea	kage current	ILO	CS=VIH or OE=VIH or WE=VIL VIO=V	ss to Vcc	-1	-	1	μA
Operating	power supply current	Icc	CS=VIL, VIN=VIL or VIH, IIO=0mA	Read	-	-	15	mA
		100	CS-VIE, VIN-VIE OF VIA, IIO-OFFIA	Write	-	-	- 15 - 35 - 15 - 35 - 90 - 0.4 	111/2
		lcc1	Cycle time=1 µs 100% duty lio=0mA	ele time=1 µs 100% duty lio=0mA Read 15		15	mA.	
Average o	perating current	1001	<u>CS</u> ≤0.2V, VIL≤0.2V VIH≥Vcc-0.2V	Write	-	-	35	"
		ICC2	Min cycle, 100% duty CS=VIL, VIN=VI	or VIH, IIO=0mA	-	: -	90	mA
Output lov	v voltage	Vol	IoL=2.1mA		-	-	0.4	٧
Output hig	h voltage	Vон	Іон=-1.0mA		2.4	-	-	٧
Standby C	current(TTL)	IsB	CS =ViH		-	-	3	mΑ
	KM684000AL/L-L			Low Power	-	-	100	μA
Standby Current	KWO04000AL/L-L	lone	CS ≥Vcc-0.2V	Low Low Power	-	-	20	μA
(CMOS)	KM684000ALI/L-L	ICC2 IN VOL I VOH I ISB C	Others=0~Vcc	Low Power	-	-	100	μA
. •	KIVIOO4000ALI/L-L			Low Low Power	-	-	50	μA

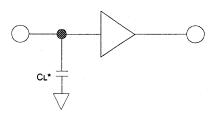
^{* 1)} Commercial Product : TA=0 to 70 °C, Vcc=5V \pm 10% unless otherwise specified 2) Industrial Product : TA=-40 to 85 °C, Vcc=5V \pm 10% unless otherwise specified ** TA=25 °C

A.C CHARACTERISTICS

TEST CONDITIONS (1.Test Load and Test input/Output Reference)*

Item	Value	Remark
Input pulse level	0.8 to 2.4V	-
Input rising & falling time	5ns	-
input and output reference voltage	1.5V	-
Output load (See right)	*CL=100pF+1TLL	-

^{*} See DC Operating conditions



^{*} Including scope and jig capacitance

TEST CONDITIONS (2. Temperature and Vcc Conditions)

Product Family	Temperature	Power Supply(Vcc)	Speed Bin	Comments
KM684000AL/L-L	0~70℃	5V ± 10%	55/70ns	Commercial
KM684000ALI/LI-L	-40~85℃	5V ± 10%	70/100ns	Industrial

PARAMETER LIST FOR EACH SPEED BIN

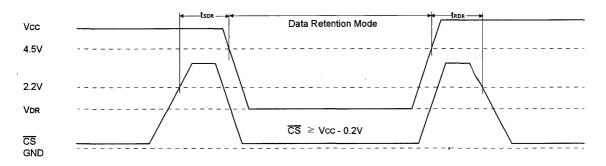
					Spec	d Bins			
	Parameter List	Symbol	5!	ins	70)ns	10	0ns	Units
			Min	Max	Min	Max	Min	Max	
Read	Read cycle time	tRC	55	-	70	-	100	-	ns
	Address access time	tAA	-	55	-	70	-	100	ns
	Chip select to output	tco	-	55	-	70	-	100	ns
	Output enable to valid output	toE	-	25	-	35	-	50	ns
	Chip select to low-Z output	tLZ	10	-	10	-	10	-	ns
	Output enable to low-Z output	tolz	5	-	5	-	5	-	ns
	Chip disable to high-Z output	tHZ	0	20	0	25	0	30	ns
	Output disable to high-Z output	tonz	0	20	0	25	0	30	ns
	Output hold from address change	ton	10	-	10	-	10	-	' ns
Write	Write cycle time	twc	55	-	70	-	100	-	ns
	Chip select to end of write	tcw	45	-	60	-	80	-	ns
	Address set-up time	tAS	. 0	-	0	-	0	-	ns
	Address valid to end of write	tAW	45	-	60	-	80	-	ns
	Write pulse width	tWP	40	-	50	-	60	-	ns
	Write recovery time	twr	0	-	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	20	0	25	0	30	ns
	Data to write time overlap	tDW	25	-	30	-	40	-	ns
	Data hold from write time	tDH	0	-	0	-	0	-	ns
	End write to output low-Z	tow	5	-	5	-	5	-	ns

DATA RETENTION CHARACTERISTICS

Item		Symbol	Test Condition*		Min	Typ**	Max	Unit
Vcc for data retention	VDR , .		CS≥Vcc-0.2V	2.0	-	5.5	٧	
Data retention current		KM684000AL/L-L		L-Ver	-	-	50	
	lan	KIVIOO4UUUAL/L-L	Vcc=3.0V <u>CS</u> ≥ Vcc-0.2V	LL-Ver	-	-	15	μA
Data retention current	IDR	1/14004000411/		L-Ver	-	-	50]
		KM684000ALI/LI-L		-	-	20	.0	
Data retention set-up time	tspi	₹	See data retentio	n	0	-	-	
Recovery time	wayoform		waveform		5	-	-	ms

^{* 1)} Commercial Product : Ta=0 to 70 $^{\circ}$, unless otherwise specified 2) Industrial Product : Ta=-40 to 85 $^{\circ}$, unless otherwise specified ** Ta=25 $^{\circ}$

DATA RETENTION TIMING DIAGRAM



FUNCTIONAL DESCRIPTION

ĊŚ	WE	ŌĒ	Mode	1/O Pin	Current Mode
Н	Х	Х	Power Down	High-Z	ISB, ISB1
L	Н	Н	Output Disable	High-Z	Icc
L	Н	L	Read	Dout	Icc
L	L	Х	Write	Din	Icc

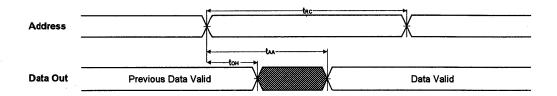
^{*} X means don't care



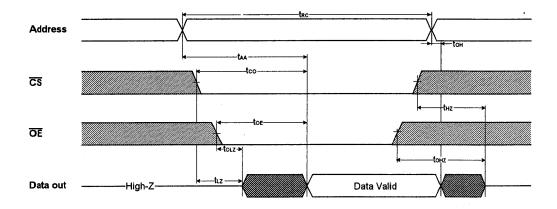
TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled)

(CS=OE=VIL, WE=VIH)



TIMING WAVEFORM OF READ CYCLE(2) (WE=VIH)

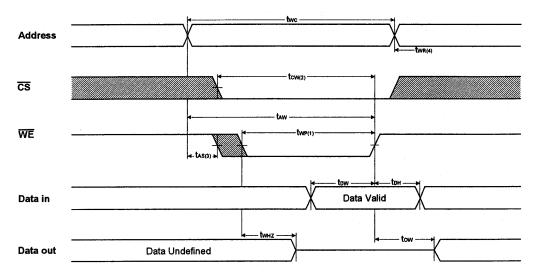


NOTES (READ CYCLE)

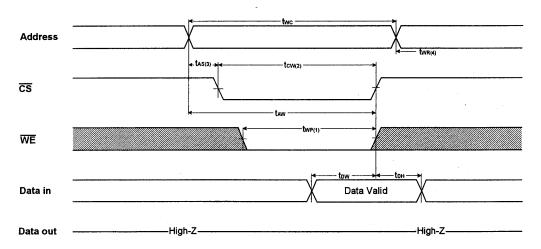
- 1, tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
- 2. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device.



TIMING WAVEFORM OF WRITE CYCLE(1) (WE Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) (CS Controlled)



NOTES (WRITE CYCLE)

- 1. A write occurs during the overlap(tWP) of a low \overline{CS} and low \overline{WE} . A write begins at the latest transition among \overline{CS} going low and \overline{WE} going low: A write end at the earliest transition among \overline{CS} going high and \overline{WE} going high, tWP is measured from the beginning of write to the end of write.
- 2. tCW is measured from the CS going low to end of write.
- 3. tAS is measured from the address valid to the beginning of write.
- 4. tWR is measured from the end of write to the address change. tWR applied in case a write ends as \overline{CS} , or \overline{WE} going high.



512Kx8 bit Low Power CMOS Static RAM

FEATURES

• Process Technology: 0.4 µm CMOS

· Organization: 512Kx8

Power Supply Voltage: Single 5V ± 10%
 Low Data Retention Voltage: 2V(Min)
 Three state output and TTL Compatible

Package Type: JEDEC Standard 32-DIP, 32-SOP,

32-TSOP(II)-Forward/Reverse

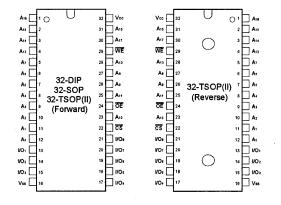
GENERAL DESCRIPTION

The KM684000B family is fabricated by SAMSUNG's advanced CMOS process technology. The family can support various operating temperature ranges and has various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

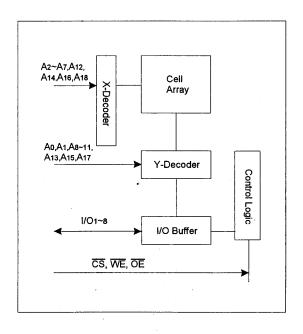
Product	Operating	Vcc Range	Speed	Power Di			
Family	Temperature.	(V)	(ns)	Standby (IsB1, Max)	Operating (ICC2)	PKG Type	
KM684000BL	Commercial (0~70℃)	4.5~5.5V	55/70ns	100 <i>µ</i> A		32-DIP,32SOP	
KM684000BL-L	,			20 <i>µ</i> A	90mA	32-TSOP(II)-R/F	
KM684000BLI Industrial (-40~85		4.5~5.5V	70/100ns	100µA	001111	32-SOP	
KM684000BLI-L	mademar (40 00 0)		7 67 100110	50µA		32-TSOP(II)-R/F	

PIN DESCRIPTION



NameName	Function
A0~A18	Address inputs
WE	Write Enable Input
CS	Chip Select Input
ŌĒ	Output Enable Input
I/O1~I/O8	Data Inputs/Outputs
Vcc	Power(5V)
Vss	Ground

FUNCTIONAL BLOCK DIAGRAM



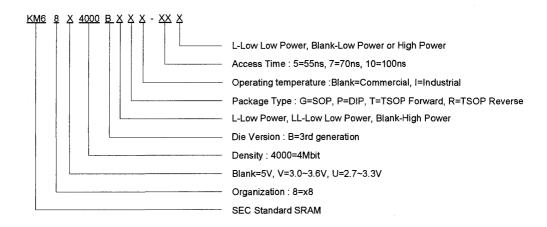


PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST

	sial Temp Product (0~70℃)	Industrial Temp Products (-40~85°C)				
Part Name	Function	Part Name	Function			
KM684000BLP-5	32-DIP, 55ns, L-pwr	KM684000BLGI-7	32-SOP,70ns, L-pwr			
KM684000BLP-5L	32-DIP, 55ns, LL-pwr	KM684000BLGI-7L	32-SOP, 70ns, LL-pwr			
KM684000BLP-7	32-DIP, 70ns, L-pwr	KM684000BLGI-10	32-SOP, 100ns, L-pwr			
KM684000BLP-7L	32-DIP, 70ns, LL-pwr	KM684000BLGI-10L	32-SOP, 100ns, LL-pwr			
KM684000BLG-5	32-SOP, 55ns, L-pwr	KM684000BLTI-7L	32-TSOP(II)F, 70ns, LL-pwr			
KM684000BLG-5L	32-SOP, 55ns, LL-pwr	KM684000BLTI-10L	32-TSOP(II)F, 100ns, LL-pwr			
KM684000BLG-7	32-SOP, 70ns, L-pwr	KM684000BLRI-7L	32-TSOP(II)R, 70ns, LL-pwr			
KM684000BLG-7L	32-SOP, 70ns, LL-pwr	KM684000BLRI-10L	32-TSOP(II)R, 100ns, LL-pwr			
KM684000BLT-5L	32-TSOP(II)F, 55ns, LL-pwr					
KM684000BLT-7L	32-TSOP(II)F, 70ns, LL-pwr					
KM684000BLR-5L	32-TSOP(II)R, 55ns, LL-pwr					
KM684000BLR-7L	32-TSOP(II)R, 70ns, LL-pwr					

ORDERING INFORMATION





ABSOLUTE MAXIMUM RATINGS*

ltem .	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	VIN,VOUT	-0.5 to 7.0	V	-
Voltage on Vcc supply relative to Vss	Vcc	-0.5 to 7.0	V	-
Power Dissipation	Po	1.0	w	-
Storage temperature	Тѕтс	-65 to 150	°C	
O	TA	0 to 70	°C	KM684000BL/L-L
Operating Temperature		-40 to 85	°C	KM684000BLI/LI-L
Soldering temperature and time	TSOLDER	260℃, 10sec (Lead Only)	-	-

^{*} Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*

Item	Symbol	Min	Typ**	Max	Unit
Supply voltage	Vcc	4.5	5.0	5.5	٧
Ground	Vss	0	0	0	٧
Input high voltage	ViH	2.2	-	Vcc+0.5V	V
Input low voltage	VIL	-0.5***	-	0.8	V

^{* 1)} Commercial Product : TA=0 to 70 °C , unless otherwise specified

CAPACITANCE* (f=1MHz, Ta=25°C)

ltem	Symbol	Test Condition	Min	Max	Unit
Input capacitance	CIN	VIN=0V	-	8	pF
Input/Output capacitance	Cio	Vio=0V	-	10	pF

^{*} Capacitance is sampled not 100% tested



²⁾ Industrial Product : Ta=-40 to 85 °C, unless otherwise specified

^{**} TA=25°C

^{***} $V_{IL}(min)$ =-3.0V for \leq 50ns pulse width

DC AND OPERATING CHARACTERISTICS

	Item	Symbol	Test Condition	ns*	Min	Typ**	Max	Unit
Input leak	age current	lu .	Vin=Vss to Vcc		-1	-	1	μA
Output lea	kage current	lLO	CS=VIH or OE=VIH or WE=VIL, V	/io=Vss to Vcc	-1 - 1		μA	
Operating	power supply current	lcc	CS=VIL, VIN=VIL or VIH,	Read	-	-	15	mA
		100	p=0mA Write		-	-	45	IIIA
		ICC1	Cycle time=1 µs 100% duty	Read	-	-	10	
Average o	perating current	1001	CS≤0.2V, VIH≤Vcc-0.2V,	Write	-	-	45	mA
		ICC2	Min cycle, 100% duty, CS=VIL, V	IN=VIL or VIH, IIO=0mA	-	90		mA
Output lov	vvoltage	Vol	IoL=2.1mA		-	-	0.4	٧
Output hig	h voltage	Voн	IOH=-1.0mA		2.4	-	-	٧
Standby C	urrent(TTL)	ISB	CS=VIH		-	-	3	mA
	KM684000BL/L-L	ISB1	CS≥Vcc-0.2V	L(Low Power)	-	-	100	μA
Standby Current	KW004000BDL-L		Others=0~Vcc	LL(L Low Power)	-	- '	20	μA
(CMOS)	KM684000BLI/L-L			L(Low Power)	-	-	100	μA
				LL(L Low Power)	-	-	50	μA

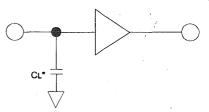
^{* 1)} Commercial Product : Ta=0 to 70°C , Vcc=5V±10% unless otherwise specified 2) Industrial Product : Ta=-40 to 85°C , Vcc=5V±10% unless otherwise specified ** Ta=25°C

A.C CHARACTERISTICS

TEST CONDITIONS (1.Test Load and Test Input/Output Reference)*

Item	Value	Remark
Input pulse level	0.8 to 2.4V	-
Input rising and falling time	5ns	_
input and output reference voltage	1.5V	-
Output load (See right)	CL=100pF+1TTL	-

^{*} See DC Operating conditions



^{*} Including scope and jig capacitance

TEST CONDITIONS (2. Temperature and Vcc Conditions)

Product Family	Temperature	Power Supply(Vcc)	Speed Bin	Comments
KM684000BL/L-L	0~70℃	5V ± 10%	55/70ns	Commercial
KM684000BLI/LI-L	-40~85℃	5V ± 10%	70/100ns	Industrial

PARAMETER LIST FOR EACH SPEED BIN

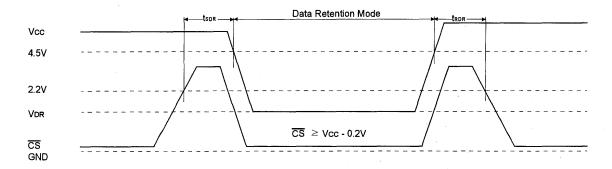
					Spec	d Bins			
Parameter List		Symbol	55ns		70ns		100ns		Units
			Min	Max	Min	Max	Min	Max	
Read	Read cycle time	tRC	55	-	70	-	100	-	ns
	Address access time	tAA	-	55	-	70	-	100	ns
	Chip select to output	tco	-	55	-	70	-	100	ns
	Output enable to valid output	tOE	-	25	-	35	-	50	ns
	Chip select to low-Z output	tLZ	10	-	10	-	10	-	ns
	Output enable to low-Z output	tOLZ	5	-	5	-	5	-	ns
	Chip disable to high-Z output	tHZ	0	20	0	25	0	30	ns
	Output disable to high-Z output	tonz	0	20	0	25	0	30	ns
	Output hold from address change	ton	10	-	10	-	10	_	ns
Write	Write cycle time	twc	55	-	70	-	100	-	ns
	Chip select to end of write	tcw	45	-	60	-	80	-	ns
	Address set-up time	tas	0	-	0	-	0	-	ns
	Address valid to end of write	tAW	45	-	60	-	80	-	ns
	Write pulse width	tWP	40	-	50	-	60	-	ns
	Write recovery time	tWR	0	-	0	-	0	-	ns
	Write to output high-Z	twnz	0	20	0	25	0	30	ns
	Data to write time overlap	tDW	25	-	30	-	40	-	ns
	Data hold from write time	tDH	0	-	0	-	0	-	ns
	End write to output low-Z	tow	5	-	5	-	5	-	ns

DATA RETENTION CHARACTERISTICS

Item		Symbol	Test Condition*		Min	Typ**	Max	Unit
Vcc for data retention	VDR		CS≥Vcc-0.2V	2.0	- 1	5.5	٧	
Data retention current	IDR	KM684000BL/L-L	<u>Vcc</u> =3.0V	L-Ver	-	-	50	μA
	ŀ		CS≥Vcc-0.2V	LL-Ver	-	-	15] '
	İ	KM684000BLI/LI-L	1	L-Ver	-	-	50	1
				LL-Ver	-	-	20] .
Data retention set-up time	tSDF	3	See data retention	n	0	-	-	ms
Recovery time	tRDF	₹	waveform	,	5	-	_	

^{* 1)} Commercial Product : Ta=0 to 70 °C , Vcc=5V \pm 10% unless otherwise specified 2) Industrial Product : Ta=-40 to 85 °C , Vcc=5V \pm 10% unless otherwise specified ** Ta=25 °C

DATA RETENTION TIMING DIAGRAM



FUNCTIONAL DESCRIPTION

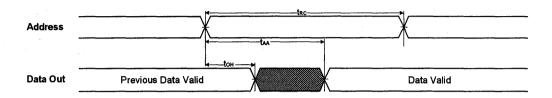
ĊŚ	WE	ŌĒ	Mode	I/O Pin	Current Mode
Н	X	Х	Power Down	High-Z	ISB, ISB1
L	Н	Н	Output Disable	High-Z	lcc
L	Н	L	Read .	Dout	Icc
L	L	X	Write	Din	Icc

^{*} X means don't care

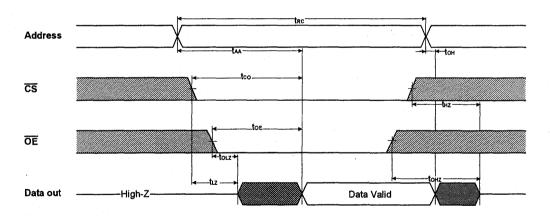


TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled) (CS=OE=VIL, WE=VIH)



TIMING WAVEFORM OF READ CYCLE(2) (WE=VIH)

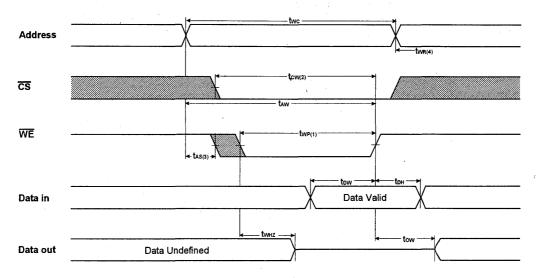


NOTES (READ CYCLE)

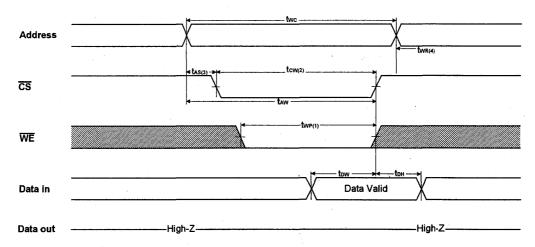
- 1. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
- 2. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device.



TIMING WAVEFORM OF WRITE CYCLE(1) (WE Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) (CS Controlled)



NOTES (WRITE CYCLE)

- 1. A write occurs during the overlap(tWP) of a low \overline{CS} and low \overline{WE} . A write begins at the latest transition among \overline{CS} going low and \overline{WE} going low: A write end at the earliest transition among \overline{CS} going high and \overline{WE} going high, tWP is measured from the beginning of write to the end of write.
- 2. tCW is measured from the $\overline{\text{CS}}$ going low to end of write.
- 3. tAS is measured from the address valid to the beginning of write.
- 4. tWR is measured from the end of write to the address change. tWR applied in case a write ends as $\overline{\text{CS}}$, or $\overline{\text{WE}}$ going high.



256Kx16 bit Low Power CMOS Static RAM

FEATURES

- Process Technology: 0.4 µm CMOS
- · Organization: 256Kx16
- Power Supply Voltage: Single 5V ± 10%
- · Low Data Retention Voltage: 2V(Min)
- · Three state output and TTL Compatible
- Package Type: JEDEC Standard 44-TSOP(II)-Forward/Reverse

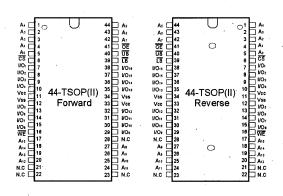
GENERAL DESCRIPTION

The KM616V4000B family is fabricated by SAMSUNG's advanced CMOS process technology. The family can support various operating temperature ranges and has various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

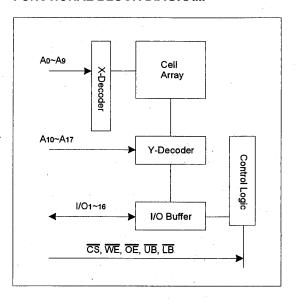
Product	Operating	Vcc	Speed	Power Di	ssipation		
List	Temp.	Range	(ns)	Standby (IsB1, Max)	Operating (Icc2)	PKG Type	
KM6164000BL-L	Commercial(0~70°C)	4.5~5.5V	55/70ns	20 <i>µ</i> A	130mA	AA TSOD(II) D/F	
KM6164000BLI-L	Industrial(-40~85℃)	4.5~5.5V	70/100ns	50,µA	ISUMA	44-TSOP(II)-R/F	

PIN DESCRIPTION



Name	Function	Name	Function
A0~A17	Address Inputs	ĹВ	Lower Byte (I/O1~8)
WE	Write Enable Input	ŪB	Upper Byte(I/O9~16)
CS	Chip Select Input	Vcc	Power
ŌĒ	Output Enable Input	Vss	Ground
I/O1~I/O16	Data Inputs/Outputs	N.C	No Connection

FUNCTIONAL BLOCK DIAGRAM



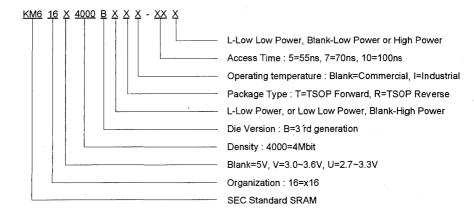


PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST

	Temp Product 70℃)		emp Products i~85℃)
Part Name	Function	Part Name	Function
KM6164000BLT-5L	44-TSOP(II)F, 55ns, LL-pwr	KM6164000BLTI-7L	44-TSOP(II)F, 70ns, LL-pwr
KM6164000BLT-7L	44-TSOP(ii)F, 70ns, LL-pwr	KM6164000BLTI-10L	44-TSOP(II)F, 100ns, LL-pwr
KM6164000BLR-5L	44-TSOP(II)R, 55ns, LL-pwr	KM6164000BLRI-7L	44-TSOP(II)R, 70ns, .LL-pwr
KM6164000BLR-7L	44-TSOP(II)R, 70ns, LL-pwr	KM6164000BLRI-10L	44-TSOP(II)R, 100ns,LL-pwr

ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	VIN,VOUT	-0.5 to 7.0	V	-
Voltage on Vcc supply relative to Vss	Vcc	-0.5 to7.0	V	-, .
Power Dissipation	PD	1.0	W	
Storage temperature	Тѕтс	-65 to 150	°C	-
O	TA	0 to 70	°C	KM6164000BL-L
Operating Temperature	e ·	-40 to 85	°C	KM6164000BLI-L
Soldering temperature and time	Tsolder	260℃, 10sec (Lead Only)	-	•

^{*} Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions forxtended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*

ltem	Symbol	Min	Typ**	Max	Unit
Supply voltage	Vcc	4.5	5.0	5.5	٧
Ground	Vss	0.	0	0	٧
Input high voltage	VIH	2.2	-	Vcc+0.5	V
Input low voltage	VIL	-0.5***	-	0.8	V

^{* 1)} Commercial Product : Ta=0 to 70°C, unless otherwise specified

CAPACITANCE* (f=1MHz, TA=25°C)

Item	Symbol	Test Condition	Min	Max	- Unit
Input capacitance	CIN	VIN=0V	-	8	pF
Input/Output capacitance	Cio	Vio=0V	· -	10	pF

^{*} Capacitance is sampled, not 100% tested



²⁾ Industrial Product : Ta=-40 to 85 °C, unless otherwise specified

^{**} TA=25°C

^{***} V_{IL} (min)=-3.0V for \leq 50ns pulse width

DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions*		Min	Тур**	Max	Unit
Input leakage current	İLŀ	Vin=Vss to Vcc		-1 ·	-	1	μA
Output leakage current	lLO	CS=VIH or OE =VIH or WE = VIL			-	1	μA
Operating power supply current	Icc	CS=VIL, VIN=VIL or VIH, IIO=0mA	Read	-	-	15	mΑ
,	100	CS-VIL, VIN-VIL OF VIH, IIO-OMA	Write	15 75 15 75	"		
		Cycle time=1 µs100% duty,lio=0mA	Read	-	-	15	mΑ
Average operatingcurrent	ICC1	CS ≤ 0.2V, VIH≥ Vcc-0.2V VIL ≤ 0.2V	Write	-1 · - 1 -1 - 15 75 15 75 130 0.4	75		
	ICC2	Min cycle,100%duty, CS=VIL, VIN=VII	or VIL,VIO=0mA		130	mA	
Output low voltage	Vol	IOL=2.1mA		-	-	0.4	٧
Output high voltage	Voн	Iон=-1.0mA		2.4	-	-	٧
Standby Current (TTL)	ISB	CS=ViH		-	-	3	mA
Standby KM6164000BL-L	ISB1	CS ≥Vcc-0.2V	Low Low Power	-	-	20	μA
Current (CMOS) KM6164000BLI-L	1981	Others inputs=0~Vcc	Low Low Power	-	• -	50	μA

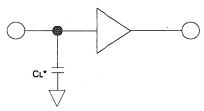
^{* 1)} Commercial Product : Ta=0 to 70℃, Vcc=5V±10% unless otherwise specified 2) Industrial Product : Ta=-40 to 85℃, Vcc=5V±10% unless otherwise specified

A.C CHARACTERISTICS

TEST CONDITIONS (1.Test Load and Test Input/Output Reference)*

Item	Value	Remark
Input pulse level	0.8 to 2.4V	-
Input rising and falling time	5ns	
Input and output reference voltage	1.5V	-
Output load (See right)	CL=100pF+1TTL	-

^{*} See DC Operating conditions



* Including scope and jig capacitance

TEST CONDITIONS (2. Temperature and Vcc Conditions)

Product Family	Temperature	Power Supply(Vcc)	Speed Bin	Comments
KM6164000BL-L	0~70℃	5V ± 10%	55/70ns	Commercial
KM6164000BLI-L	-40~85℃	5V ± 10%	70/100ns	Industrial

^{*} All parameters are measured with 30pF test load.

PARAMETER LIST FOR EACH SPEED BIN

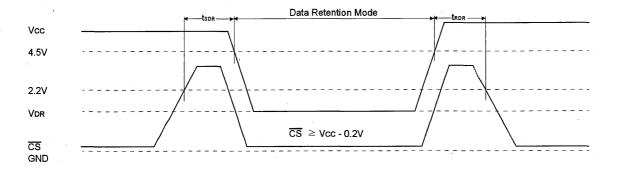
					Spec	d Bins			
	Parameter List	Symbol	Symbol 55ns		70ns		100ns		Units
			Min	Max	Min	Max	Min	Max	
Read	Read cycle time	tRC	55	-	70	-	100	-	ns
	Address access time	tAA	-	55	-	70	-	100	ns
	Chip select to output	tco	-	55	-	70	-	100	ns
	Output enable to valid output	tOE	-	25	-	35	-	50	ns
	Chip select to low-Z output	tLZ	10	-	10	-	10	-	ns
	Output enable to low-Z output	tolz	5	-	5	-	5	-	ns
	Chip disable to high-Z output	tHZ	0	20	0	25	0	30	ns
	OE disable to high-Z output	tonz	0	20	0	25	0	30	ns
	Output hold from address change	tон	10	-	10	-	10	-	ns
	LB, UB valid to data output	tBA		25	-	35	-	50	ns
	UB, LB disable to high-Z output	tBHZ	0	20	0	25	0	30	ns
Write	Write cycle time	twc	55	-	70	-	100	-	ns
	Chip select to end of write	tcw	45	-	60	-	80	-	ns
	Address set-up time	tAS	0	-	0	-	0	-	ns
	Address valid to end of write	taw	45	-	60	-	80	-	ns
	Write pulse width	tWP	40	-	50	-	600	-	ns
	Write recovery time	tWR	0	-	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	20	0	25	0	30	ns
	Data to write time overlap	tDW	25	-	30	-	40	-	ns
	Data hold from write time	tDH	0	-	0	-	0	-	ns
	End write to output low-Z	tow	5	-	5	-	5	-	ns
	LB, UB valid to end of write	tBW	45	-	60	-	-	80	ns

DATA RETENTION CHARACTERISTICS

Item		Symbol	Test Condition*		Min	Typ**	Max	Unit
Vcc for data retention	VDR		CS≥Vcc-0.2V		2.0	-	5.5	٧
D-4	IDR	KM6164000BL-L	Vcc=3.0V	LL-Ver	-	-	15	
Data retention current		KM6164000BLI-L		LL-Ver	-	-	20	μA
Data retention set-up time	tsdr		See data retention waveform		0	-	-	mo
Recovery time	trdr				5	_	-	ms

^{* 1)} Commercial Product : Ta=0 to 70 $^{\circ}$, unless otherwise specified 2) Industrial Product : Ta=-40 to 85 $^{\circ}$, unless otherwise specified ** TA=25 $^{\circ}$

DATA RETENTION TIMING DIAGRAM



FUNCTIONAL DESCRIPTION

CS	LB	UB	WE	ŌĒ	Mode	1/01~8	I/O9~16	Current Mode
Н	Х	х	Х	Х	Not Select	High-Z	High-Z	ISB1
L	Х	Х	• н	Н	Output Disable	High-Z	High-Z	lec
L	Н	Н	Х	Х		High-Z	High-Z	
L	L H L	H L L	Н	L	Read	Dout High-Z Dout	High-Z Dout Dout	lcc
L	L H L	H L L	L	х	Write	Din High-Z Din	High-Z Din Din	lcc

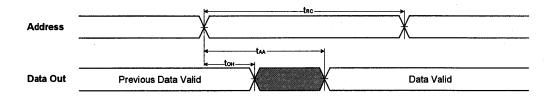
^{*} X means don't care (Must be in low or high state)



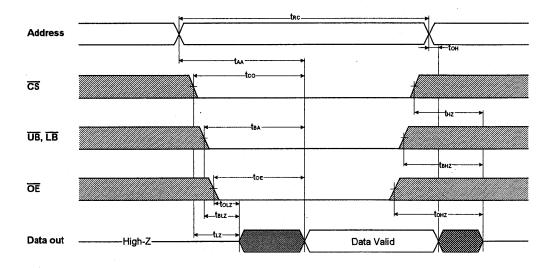
TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled)

(CS=OE=VIL, WE=VIH, UB or and LB=VIL)



TIMING WAVEFORM OF READ CYCLE(2) (WE=VIH)

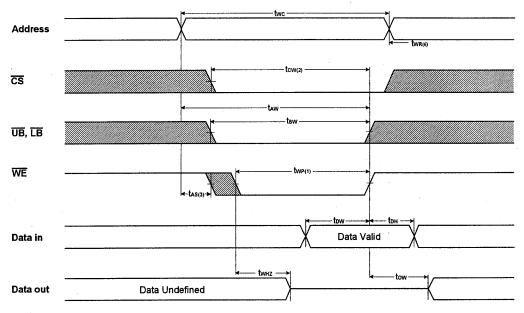


NOTES (READ CYCLE)

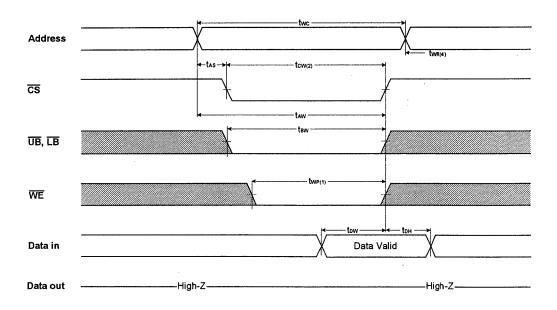
- 1. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
- 2. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device.



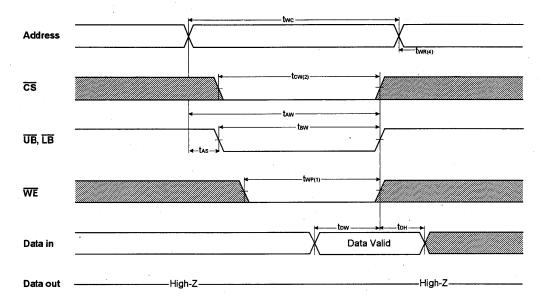
TIMING WAVEFORM OF WRITE CYCLE(1) (WE Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) (CS Controlled)



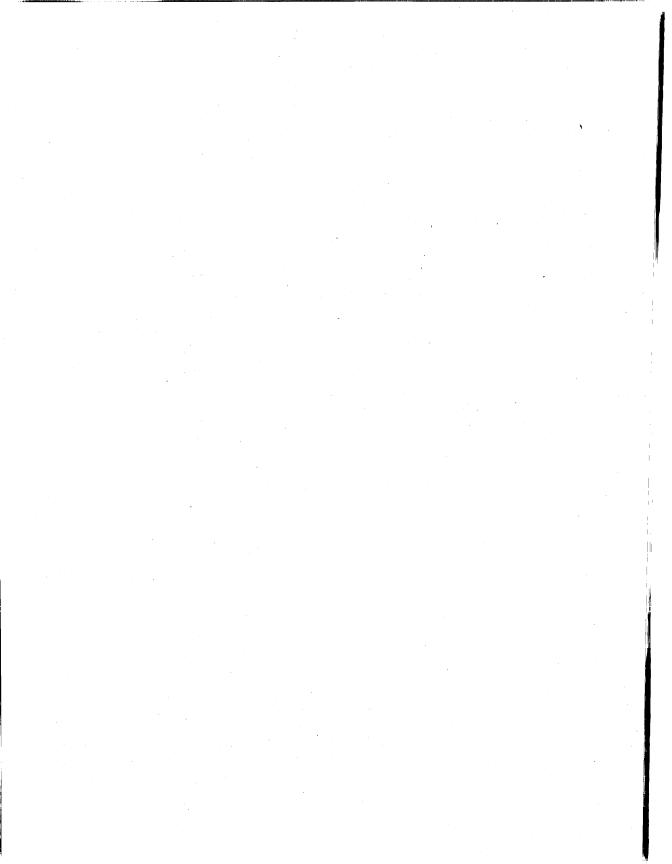
TIMING WAVEFORM OF WRITE CYCLE(3) (UB, LB Controlled)



Notes (WRITE CYCLE)

- 1. A write occurs during the overlap(tWP) of a low \overline{CS} and low \overline{WE} . A write begins when \overline{CS} goes low and \overline{WE} goes low with asserting \overline{UB} or \overline{LB} for single byte operation or simultaneous asserting \overline{UB} and \overline{LB} for double byte operation. A write ends at the earliest transition when \overline{CS} goes high and \overline{WE} goes high. The tWP is measured from the beginning of write to the end of write.
- 2. tCW is measured from the \overline{CS} going low to end of write.
- 3. tAS is measured from the address valid to the beginning of write.
- 4. tWR is measured from the end or write to the address change. tWR applied in case a write ends as $\overline{\text{CS}}$ or $\overline{\text{WE}}$ going high.

Low Power and Low Voltage SRAM (3.0V, 3.3V Operation)



32Kx8 bit Low Power and Low Voltage CMOS Static RAM

FEATURES

• Process Technology: 0.7 μm CMOS

Organization: 32Kx8

· Power Supply Voltage

KM62V256C family : 3.3V \pm 0.3V KM62U256C family : $3.0V \pm 0.3V$

. Low Data Retention Voltage: 2V(Min)

· Package Type: JEDEC Standard 28-SOP, 28-TSOP(I)-Forward/Reverse

· Three state output and TTL Compatible

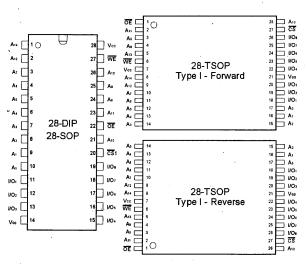
GENERAL DESCRIPTION

The KM62V256C and KM62U256C family are fabricated by SAMSUNG's advanced CMOS process technology. The family can support various operating temperature ranges and has various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

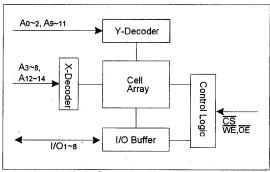
PRODUCT FAMILY

Product	Countries		8	Power Di	PKG Type	
Family	Vcc Range		Speed (ns)	Standby (IsB/i, Max)		
KM62V256CL-L KM62U256CL-L	Commercial (0~70°C)	3.0 ~ 3.6V 2.7 ~ 3.3V	70*/100ns 85*/100ns	10μA 10μA		28-SOP** 28-TSOP(I) R/F
KM62V256CLE-L	Extended (-25~85°C)	3.0 ~ 3.6V	70*/100ns	20µA	35mA	28-SOP**
KM62U256CLE-L	· · · · · · · · · · · · · · · · · · ·	2.7 ~ 3.3V	85*/100ns	15 µA		28-TSOP(I) R/F
KM62V256CL-LI	Industrial (-40~85°C)	3.0 ~ 3.6V	70*/100ns	20 <i>µ</i> A		28-SOP**
KM62U256CLI-L	110001101 (-40 00 0)	2.7 ~ 3.3V	85*/100ns	15 <i>µ</i> A		28-TSOP(I) R/F

PIN DESCRIPTION



FUNCTIONAL BLOCK DIAGRAM



Pin Name	Function
A0~A14	Address Inputs
WE	Write Enable Input
cs	Chip Select Input
ŌĒ	Output Enable Input
I/O1~I/O8	Data Inputs/Outputs
Vcc ,	Power
Vss	Ground



^{*}The parameter is measured with 30pF test load.

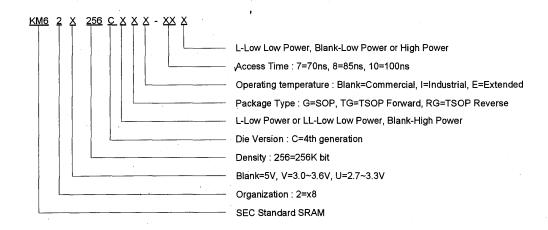
**The deviced with 100ns SOP package in 3.0~3.6V Vcc range which is not produced.

PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST

	Commercial Temp Product (0~70°C)		emp Products ~85°C)	Industrial Temp Products (-40~85℃)		
Part Name	Function	Part Name	Function	Part Name	Function	
KM62V256CLG-7L	28-SOP, 70ns, 3.3V	KM62V256CLGE-7L	28-SOP, 70ns, 3.3V	KM62V256CLGI-7L	28-SOP, 70ns, 3.3V	
KM62V256CLG-10L	28-SOP, 100ns, 3.3V	KM62V256CLGE-10L	28-SOP, 100ns, 3.3V	KM62V256CLGI-10L	28-SOP, 100ns, 3.3V	
KM62V256CLTG-7L	28-TSOP F, 70ns, 3.3V	KM62V256CLTGE-7L	28-TSOP F, 70ns, 3.3V	KM62V256CLTGI-7L	28-TSOP F, 70ns, 3.3V	
KM62V256CLTG-10L	28-TSOP F, 100ns, 3.3V	KM62V256CLTGE-10L	28-TSOP F, 100ns, 3.3V	KM62V256CLTGI-10L	28-TSOP F, 100ns, 3.3V	
KM62V256CLRG-7L	28-TSOP R, 70ns, 3.3V	KM62V256CLRGE-7L	28-TSOP R, 70ns, 3.3V	KM62V256CLRGI-7L	28-TSOP R, 70ns, 3.3V	
KM62V256CLRG-10L	28-TSOP R, 100ns, 3.3V	KM62V256CLRGE-10L	28-TSOP R, 100ns, 3.3V	KM62V256CLRGI-10L	28-TSOP R, 100ns, 3.3V	
KM62U256CLG-8L	28-SOP, 85ns, 3.0V	KM62U256CLGE-8L	28-SOP, 85ns, 3.0V	KM62U256CLGI-8L	28-SOP, 85ns, 3.0V	
KM62U256CLG-10L	28-SOP, 100ns, 3.0V	KM62U256CLGE-10L	28-SOP, 100ns, 3.0V	KM62U256CLGI-10L	28-SOP, 100ns, 3.0V	
KM62U256CLTG-8L	28-TSOP F, 85ns, 3.0V	KM62U256CLTGE-8L	28-TSOP F, 85ns, 3.0V	KM62U256CLTGI-8L	28-TSOP F, 85ns, 3.0V	
KM62U256CLTG-10L	28-TSOP F, 100ns, 3.0V	KM62U256CLTGE-10L	28-TSOP F, 100ns, 3.0V	KM62U256CLTGI-10L	28-TSOP F, 100ns, 3.0V	
KM62U256CLRG-8L	28-TSOP R, 85ns, 3.0V	KM62U256CLRGE-8L	28-TSOP R, 85ns, 3.0V	KM62U256CLRGI-8L	28-TSOP R, 85ns, 3.0V	
KM62U256CLRG-10L	28-TSOP R, 100ns, 3.0V	KM62U256CLRGE-10L	28-TSOP R, 100ns, 3.0V	KM62U256CLRGI-10L	28-TSOP R, 100ns, 3.0V	

ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	VIN, VOU	-0.5 to Vcc+0.5	V	-
Voltage on Vcc supply relative to Vss	Vcc	-0.3 to 4.6	V	-
Power Dissipation	Pb	0.7	w	-
Storage temperature	TsTG	-65 to 150	င	
		0 to 70	°C	KM62V256CL-L, KM62U256CL-L
Operating Temperature	TA	-25 to 85	င	KM62V256CLE-L, KM62U256CLE-L
		-40 to 85	°C	KM62V256CLI-L, KM62U256CLI-L
Soldering temperature and time	TSOLDER	260℃, 10sec (Lead Only)	-	-

^{*} Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*

Item	Symbol	Product	Min	Typ**	Max	Unit
Supply voltage	Vcc	KM62V256C Family KM62U256C Family	3.0 2.7	3.3 3.0	3.6 3.3	V
Ground	Vss	All	0	0	0	V
Input high voltage	ViH	KM62V256C Family KM62U256C Family	2.2	-	Vcc+0.3V Vcc+0.3V	V
Input low voltage	VIL	KM62V256C Family KM62U256C Family	-0.3 -0.3***	-	0.4 0.4	V

^{* 1)} Commercial Product : Ta=0 to 70 °C, unless otherwise specified

CAPACITANCE* (f=1MHz, Ta=25 °C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	Cin	V0=NIV	-	6	pF
Input/Output capacitance	Cio	Vio=0V	-	8	pF

^{*} Capacitance is sampled not 100% tested



²⁾ Extended Product : Ta=-25 to 85 ℃, unless otherwise specified 3) Industrial Product : Ta=-40 to 85 ℃, unless otherwise specified

^{**} Ta=25℃

^{***} VIL(min)=-3.0V for ≤ 30 ns pulse width

DC AND OPERATING CHARACTERISTICS

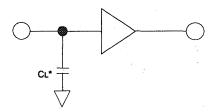
I	tem	Symbol	Test Conditions ¹⁾			Typ ²⁾	Max	Unit
Input leakage cur	rent	lu	Vin=Vss to Vcc		-1	-	1	μA
Output leakage cu	ırrent	ILO	CS=VIH or VIL or	WE=ViL, Vio=Vss to Vcc	-1	-	1	μA
Operating power	supply current	Icc	CS=VIL, VIN=VIH C	r VIL, LIO=0mA	-	1.0	2.0	mA
Average operating	g current	lcc1	Cycle time=1 µs 100% duty CS ≤ 0.2V, V _{IL} ≤ -0.2V V _{IN} ≥ V _{CC} -0.2V, Lio=0mA		-	2.5	5	mA
		ICC2	Min cycle, 100% duty, CS=VIL, Lio=0mA		-	203)	35 ⁴)	mA
Output low voltag	e	Vol loL=2.1mA			-	-	0.4	٧
Output high voltage	је	Vон	юн=-1.0mA		2.2	-	-	V
Standby Current(TTL)	ISB	CS =ViH		-	-	0.3	mA
Standby Current	KM62V256CL-L KM62V256CLE-L KM62V256CLI-L	ISB1	CS ≥ Vcc-2.0V Vin≤2.0V or	Low Low Power Low Low Power Low Low Power	-	1.5 1.5 1.5	10 20 20	μΑ μΑ - μΑ
(CMOS)	KM62U256CL-L KM62U256CLE-L KM62U256CLI-L	1881	VIN ≥ Vcc-2.0V	Low Low Power Low Low Power Low Low Power	-	1.0 1.0 1.0	10 15 15	μΑ μΑ μΑ

^{1) -} Commercial Product : Ta=0 to 70°C , Vcc=3.3 ± 0.3V (62V256C Family), Vcc=3.0 ± 0.3V (62U256C Family)

A.C CHARACTERISTICS

TEST CONDITIONS (1.Test Load and Test Input/Output Reference)*

Item	Value	Remark
Input pulse level	0.4 to 2.2V	-
Input rising & falling time	5ns	
Input and output reference voltage	1.5V	-
Output load (See right)	CL=100pF+1TTL **CL=30pF+1TTL	-



* Including scope and jig capacitance



⁻ Extended Product : Ta=-25 to 85°C , Vcc=3.3 ± 0.3V (62V256CE Family) , Vcc=3.0 ± 0.3V (62U256CE Family)

⁻ Industrial Product : Ta=-40 to 85°C, Vcc=3.3±0.3V (62V256CI Family), Vcc=3.0±0.3V (62U256CI Family)

²⁾ Ta=25℃

^{3) 25}mA for KM62V256C Family
4) 30mA for KM62U256C Family but it is not 100% tested but obtained statistically

^{*} See DC Operating conditions
** KM62V256CL-7L Family, KM62U256CL-8L Family

TEST CONDITIONS (2. Temperature and Vcc Conditions)

Product Family	Temperature	Power Supply(Vcc)	Speed Bin	Comments
KM62V256CL-L	0~70℃	3.3V ± 0.3	70*/100ns	Commercial
KM62V256CLE-L	-25~85℃	3.3V ± 0.3	70*/100ns	Extended
KM62V256CLI-L	-40~85℃	3.3V ± 0.3	70*/100ns	Industrial
KM62U256CL-L	0~70℃	3.0V ± 0.3	85*/100ns	Commercial
KM62U256CLE-L	-25~85℃	3.0V ± 0.3	85*/100ns	Extended
KM62U256CL-L	-40~85℃	3.0V ± 0.3	85*/100ns	Industrial

^{*} The parameter is measured with 30pF test load.

PARAMETER LIST FOR EACH SPEED BIN

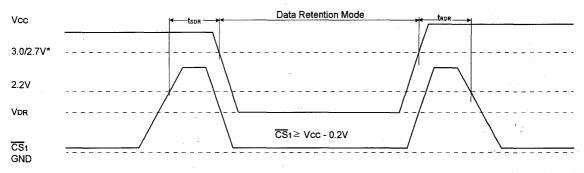
					Spe	ed Bins			
Parameter List		Symbol	nbol 70ns		85ns		10	l0ns	Units
			Min	Max	Min	Max	Min	Max	1
Read	Read cycle time	tRC	70	-	85	-	100	-	ns
	Address access time	tAA	-	70	-	85	-	100	ns
	Chip select to output	tco	-	70	-	85	-	100	ns
	Output enable to valid output	tOE	-	35	-	40	-	50	ns
	Chip select to low-Z output	tLZ	10	-	10	-	10	-	ns
	Output enable to low-Z output	toLZ	5	-	5	-	5	-	ns
	Chip disable to high-Z output	tHZ .	0	30	0	30	0	35	ns
	Output disable to high-Z output	tonz	0	30	0	30	0	35	ns
	Output hold from address change	ton	5	-	10	-	15	-	ns
Write	Write cycle time	twc	70	-	85	-	100	-	ns
	Chip select to end of write	tcw	60	-	70	-	70	-	ns
	Address set-up time	tAS	0	-	0	-	0		ns
	Address valid to end of write	tAW	60	-	70	_	. 70	-	ns
	Write pulse width	tWP	50	-	60		60	-	ns
	Write recovery time	twR	0	-	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	- 25	Ò	25	0	30	ns
	Data to write time overlap	tDW	50	-	60	-	60	-	ns
	Data hold from write time	tDH	0	-	0	-	0	-	ns
	End write to output low-Z	tow	5	-	10	-	10	-	ns

DATA RETENTION CHARACTERISTICS

Item		Symbol	Test Condition*	Min	Typ**	Max	Unit
Vcc for data retention	VDR		CS≥Vcc-0.2V	2.0		3.6	٧
Data retention current		KM62V256CL-L KM62U256CL-L		-	1 0.6	8 8	
	IDR	KM62V256CLE-L KM62U256CLE-L	Vcc=3.0V CS≥Vcc-0.2V	-	1 0.6	10 10	μA
		KM62V256CLI-L KM62U256CLI-L		-	1 0.6	10 10	
Data retention set-up time		tsdr	See data retention	0	-	. .	ms
Recovery time		trdr	waveform	5	-	-	1115

^{*1)} Commercial Product : Ta=0 to $70^{\circ}C$, unless otherwise specified 2) Extended Product : Ta=-25 to $85^{\circ}C$, nless otherwise specified 3) Industrial Product : Ta=-40 to $85^{\circ}C$, unless otherwise specified ** $T_A=25^{\circ}C$

DATA RETENTION WAVE FORM



^{* 3.0}V for KM62V256C Family, 2.7V for KM62U256C Family.

FUNCTIONAL DESCRIPTION

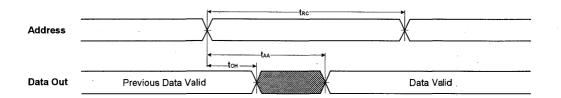
ĊŚ	WE	ŌĒ	Mode	I/O Pin	Current Mode
Н	Х	Х	Power Down	High-Z	ISB, ISB1
L	Н	H	Output Disable	High-Z	Icc
L	Н	L	Read	Dout	Icc
L	L	X	Write	Din	Icc

^{*} X means don't care.

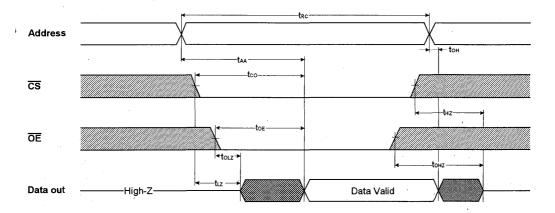


TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (1) (Address Controlled) ($\overline{CS}=\overline{OE}=VIL, \overline{WE}=VIH)$



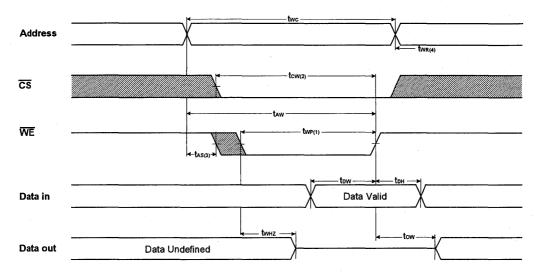
TIMING WAVEFORM OF READ CYCLE(2) (WE=VIH)



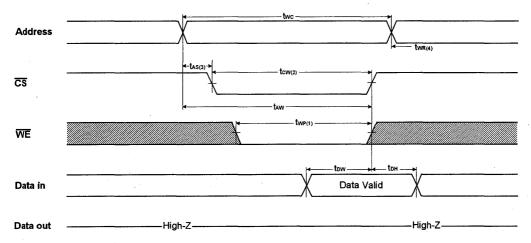
NOTES (READ CYCLE)

- 1. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
- 2. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device.

TIMING WAVEFORM OF WRITE CYCLE(1) (WE Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) (CS Controlled)



NOTES (WRITE CYCLE)

- 1. A write occurs during the overlap(fWP) of a low \overline{CS} and low \overline{WE} . A write begins at the latest transition among \overline{CS} going low and \overline{WE} going low: A write end at the earliest transition among \overline{CS} going high and \overline{WE} going high, fWP is measured from the beginning of write to the end of write.
- 2. tCW is measured from the CS going low to end of write.3. tAS is measured from the address valid to the beginning of write.
- 4. tWR is measured from the end of write to the address change. tWR applied in case a write ends as $\overline{\text{CS}}$ or $\overline{\text{WE}}$ going high.



32Kx8 bit Low Power and Low Voltage CMOS Static RAM

FEATURES

• Process Technology: 0.4 m CMOS

Organization : 32Kx8Power Supply Voltage

KM62V256D family : $3.3V \pm 0.3V$ KM62U256D family : $3.0V \pm 0.3V$

Low Data Retention Voltage : 2V(Min)
 Three state output and TTL Compatible

 Package Type: JEDEC Standard 28-SOP, 28-TSOP1-Forward/Reverse

GENERAL DESCRIPTION

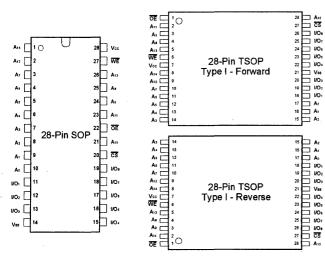
The KM62V256D and KM62U256D family is fabricated by SAM-SUNG's advanced CMOS process technology. The family can support various operating temperature ranges and has various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

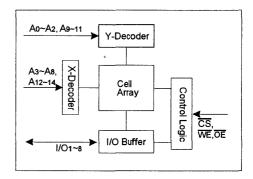
.					Power Dissipation		
Product Family	Operating Temperature.	Vcc Range	Speed (ns)	PKG Type	Standby (IsB1, Max)	Operating (Icc2)	
KM62V256DL-L KM62U256DL-L	Commercial (0~70℃)	3.0V ~3.6V 2.7V ~ 3.3V	70*/100 85*/100	28-SOP** 28-TSOP(I) R/F	10μA 10μA		
KM62V256DLE-L KM62U256DLE-L	Extended(-25~85℃)	3.0V ~3.6V 2.7V ~ 3.3V	70*/100 85*/100	28-SOP** 28-TSOP(I) R/F	20μA 15μA	35mA	
KM62V256DLI-L KM62U256DLI-L	Industrial (-40~85℃)	3.0V ~3.6V 2.7V ~ 3.3V	70*/100 85*/100	28-SOP** 28-TSOP(I) R/F	20μA 15μA		

^{*} The parameter is measured with 30pF test load.

PIN DESCRIPTION



FUNCTIONAL BLOCK DIAGRAM



Pin Name	Function
A0~A14	Address Inputs
WE	Write Enable Input
CS	Chip Select Input
ŌĒ	Output Enable Input
I/O1~I/O8	Data Inputs/Outputs
Vcc	Power
Vss	Ground



64Kx8 bit Low Power and Low Voltage CMOS Static RAM

FEATURES

• Process Technology: 0.6 µm CMOS

Organization : 64Kx8Power Supply Voltage

KM68V512A family : 3.3V ± 0.3V KM68U512A family : 3.0V ± 0.3V • Low Data Retention Voltage : 2V(Min)

Three state output and TTL Compatible
 Package Type: JEDEC Standard

32-SOP, 32-TSOP(I)-Forward, 32-sTSOP(I)-Forward

GENERAL DESCRIPTION

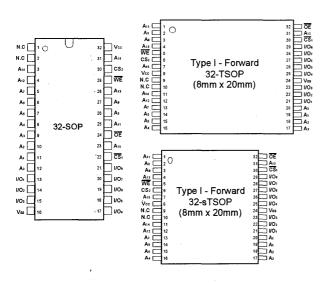
The KM68V512A and KM68U512A family are fabricated by SAMSUNG's advanced CMOS process technology. The family can support various operating temperature ranges and has various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

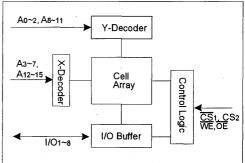
Product		Vcc Range	8	Power Dis		
Family	Operating Temperature.		Speed (ns)	Standby (1sb1, Max)	Operating (1cc2)	PKG Type
KM68V512AL-L	Commercial (0~70°C)	3.0 ~ 3.6V	70*/85/100ns	10 <i>µ</i> A		22 000
KM68U512AL-L	,	2.7 ~ 3.3V	85*/100ns	10 <i>µ</i> A		
KM68V512ALE-L	Extended (-25~85℃)	3.0 ~ 3.6V	70*/85/100ns	20 <i>µ</i> A	40mA	32-SOP 32-TSOP(I) F
KM68U512ALE-L		2.7 ~ 3.3V	85*/100ns	15 <i>µ</i> A	40mA	32-sTSOP(I) F
KM68V512ALI-L	Industrial (-40~85℃)	3.0 ~ 3.6V	70*/85/100ns	20 <i>µ</i> A		,
KM68U512ALI-L		2.7 ~ 3.3V	85*/100ns	15 <i>µ</i> A		

^{*} The parameter is measured with 30pF test load.

PIN DESCRIPTION



FUNCTIONAL BLOCK DIAGRAM



Name Name	Function
A0~A15	Address Inputs
WE	Write Enable Input
CS1,CS2	Chip Select Inputs
ŌĒ	Output Enable Input
I/O1~I/O8	Data Inputs/Outputs
Vcc	Power
Vss	Ground
N.C	No Connection

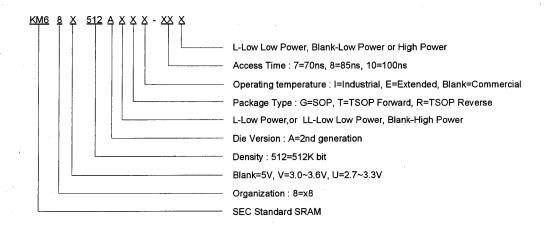


PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST

	al Temp Product J~70℃)		Temp Products 5~85°C)	Industrial Temp Products (-40~85°C)	
Part Name	Function	Part Name	Function	Part Name	Function
KM68V512ALG-7L	32-SOP, 70ns, 3.3V, LL	KM68V512ALGE-7L	32-SOP, 70ns, 3.3V, LL	KM68V512ALGI-7L	32-SOP, 70ns, 3.3V, LL
KM68V512ALG-8L	32-SOP, 85ns, 3.3V, LL	KM68V512ALGE-8L	32-SOP, 85ns, 3.3V, LL	KM68V512ALGI-8L	32-SOP, 85ns, 3.3V, LL
KM68V512ALG-10L	32-SOP, 100ns, 3.3V, LL	KM68V512ALGE-10L	32-SOP, 100ns, 3.3V, LL	KM68V512ALGI-10L	32-SOP, 100ns, 3.3V, LL
KM68V512ALT-7L	32-TSOP F, 70ns, 3.3V, LL	KM68V512ALTE-7L	32-TSOP F, 70ns, 3.3V, LL	KM68V512ALTI-7L	32-TSOP F, 70ns, 3.3V, LL
KM68V512ALT-8L	32-TSOP F, 85ns, 3.3V, LL	KM68V512ALTE-8L	32-TSOP F, 85ns, 3.3V, LL	KM68V512ALTI-8L	32-TSOP F, 85ns, 3.3V, LL
KM68V512ALT-10L	32-TSOP F, 100ns, 3.3V,LL	KM68V512ALTE-10L	32-TSOP F, 100ns, 3.3V,LL	KM68V512ALTI-10L	32-TSOP F, 100ns, 3.3V,LL
KM68V512ALTG-7L	32-sTSOP F,70ns,3.3V,LL	KM68V512ALTGE-7L	32-sTSOP F,70ns,3.3V,LL	KM68V512ALTGI-7L	32-sTSOP F,70ns,3.3V,LL
KM68V512ALTG-8L	32-sTSOP F,85ns,3.3V,LL	KM68V512ALTGE-8L	32-sTSOP F,85ns,3.3V,LL	KM68V512ALTGI-8L	32-sTSOP F,85ns,3.3V,LL
KM68V512ALTG-10L	32-sTSOP F,100ns,3.3V,LL	KM68V512ALTGE-10L	32-sTSOP F,100ns,3.3V,LL	KM68V512ALTGI-10L	32-sTSOP F,100ns,3.3V,LL
KM68U512ALG-8L	32-SOP, 85ns, 3.0V, LL	KM68U512ALGE-8L	32-SOP, 85ns, 3.0V, LL	KM68U512ALGI-8L	32-SOP, 85ns, 3.0V, LL
KM68U512ALG-10L	32-SOP, 100ns, 3.0V, LL	KM68U512ALGE-10L	32-SOP, 100ns, 3.0V, LL	KM68U512ALGI-10L	32-SOP, 100ns, 3.0V, LL
KM68U512ALT-8L	32-TSOP F, 85ns, 3.0V, LL	KM68U512ALTE-8L	32-TSOP F, 85ns, 3.0V, LL	KM68U512ALTI-8L	32-TSOP F, 85ns, 3.0V, LL
KM68U512ALT-10L	32-TSOP F, 100ns, 3.0V, LL	KM68U512ALTE-10L	32-TSOP F, 100ns, 3.0V, LL	KM68U512ALTI-10L	32-TSOP F, 100ns, 3.0V, LL
KM68U512ALTG-8L	32-sTSOP F, 85ns, 3.0V, LL	KM68U512ALTGE-8L	32-sTSOP F, 85ns, 3.0V, LL	KM68U512ALTGI-8L	32-sTSOP F, 85ns, 3.0V, LL
KM68U512ALTG-10L	32-sTSOP F, 100ns,3.0V, LL	KM68U512ALTGE-10L	32-sTSOP F, 100ns,3.0V, LL	KM68U512ALTGI-10L	32-sTSOP F, 100ns,3.0V, LL

ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	VIN, VOUT	-0.5 to Vcc+0.5	٧	-
Voltage on Vcc supply relative to	Vcc	-0.3 to 4.6	٧	-
Power Dissipation	Pb	0.7	w	
Storage temperature	Тѕтс	-65 to 150	°C	-
		0 to 70	°°C	KM68V512AL-L, KM68U512AL-L
Operating Temperature	TA	-25 to 85	င	KM68V512ALE-L, KM68U512ALE-L
		-40 to 85	°C	KM68V512ALI-L, KM68U512ALI-L
Soldering temperature and time	TSOLDER	260°C, 10sec (Lead Only)	-	-

^{*} Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*

Item	Symbol	Product	Min	Typ**	Max	Unit
Supply voltage	Vcc	KM68V512A Family KM68U512A Family	3.0 2.7	3.3 3.0	3.6 3.3	V
Ground	Vss	All Family	0	0	0	٧
Input high voltage	ViH	KM68V512A Family KM68U512A Family	2.2 2.2	-	Vcc+0.3V Vcc+0.3V	< <
Input low voltage	VIL	KM68V512A Family KM68U512A Family	-0.3*** -0.3***	-	0.4 0.4	V V

^{* 1)} Commercial Product : TA=0 to 70 °C, unless otherwise specified
2) Extended Product : TA=-25 to 85 °C, unless otherwise specified

CAPACITANCE* (f=1MHz, Ta=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	Cin	VIN=0V	-	6	pF
Input/Output capacitance	Сю	Vio=0V	-	8	pF

^{*} Capacitance is sampled, not 100% tested



³⁾ Industrial Product : Ta=-40 to 85 ℃, unless otherwise specified

^{**} TA=25°C

^{***} V_{IL} (min)=-3.0V for \leq 30ns pulse width

DC AND OPERATING CHARACTERISTICS

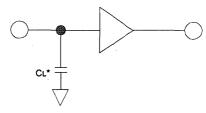
ı	tem	Symbol	Test Condit	ons*	Min	Typ**	Max	Unit
Input leakage cui	rrent	lu	Vin=Vss to Vcc		-1	-	1	μA
Output leakage o	current	lLO	CS1=VIH or CS2=VIL or WE=	VIL, VIO=Vss to Vcc	-1	-	- 1	μA
Operating power	supply current	Icc	CS1=VIL, CS2=VIH, VIN=VIH	or VIL, IIO=0mA	-	-	5	mA
Average operating current		Icc1	Cycle time=1 <i>μ</i> s 100% duty, Iιο=0mA CS1≤ 0.2V, CS2≥ Vcc-0.2V		-	-	5	mA
		Icc2	Min cycle, 100% duty, lio=0mA CS1=ViL, CS2=ViH		-	-	40	mA
Output low voltage	Output low voltage \		IoL=2.1mA			-	0.4	٧
Output high volta	ge	Voн	Юн=-1.0mA		2.4	-	-	٧
Standby Current(TTL)	İSB	CS1=VIH, CS2=VIL			-	0.3	mA
	KM68V512AL-L			L(Low Power)	-	-	10	μA
Standby	KM68V512ALE-L KM68V512ALI-L		CS ₁ ≥ Vcc-0.2V CS ₂ ≥ Vcc-0.2V or	LL(L Low Power)	-	-	20	μA
Current(CMOS)	KM68V512AL-L	ISB1	CS2 ≤ 0.2V Other input = 0~Vcc	L(Low Power)	-	-	10	μA
	KM68V512ALE-L KM68V512ALI-L		Outer input – 0-vcc	LL(L Low Power)	-	• -	15	μA

^{*1)} Commercial Product : Ta=0 to 70 ℃, Vcc=3.3V ±0.3V(68V512A Family), Vcc=3.0V ±0.3V(68U512A Family).

A.C CHARACTERISTICS

TEST CONDITIONS (1.Test Load and Test Input/Output Reference)*

Item	Value	Remark
Input pulse level	0.4 to 2.2V	-
Input rising & falling time	5ns	_
input and output reference voltage	1.5V	-
Output load (See right)	CL=100pF+1TTLL **CL=30pF+1TTLL	-



* Including scope and jig capacitance

^{.)} Extended Product : Ta=-25 to 85°C, Vcc=3.3V±0.3V(68V512A Family), Vcc=3.0V±0.3V(68U512A Family).

3) Industrial Product : Ta=-40 to 85°C, Vcc=3.3V±0.3V(68V512AF Family), Vcc=3.0V±0.3V(68U512AF Family).

** Ta=25°C

^{*} See DC Operating conditions
** KM68V512AL-7L Family, KM68U512AL-8L Family

TEST CONDITIONS (2. Temperature and Vcc Conditions)

Product Family	Temperature	Power Supply(Vcc)	Speed Bin	Comments
KM68V512AL-L	0~70℃	3.3V ± 0.3	70*/85/100ns	Commercial
KM68V512ALE-L	-25~85℃	3.3V ± 0.3	70*/85/100ns	Extended
KM68V512ALII-L	-40~85℃	3.3V ± 0.3	70*/85/100ns	Industrial
KM68U512AL-L	0~70℃	3.0V ± 0.3	85*/100ns	Commercial
KM68U512ALE-L	-25~85℃	3.0V ± 0.3	85*/100ns	Extended
KM68U512AL-L	-40~85℃	3.0V ± 0.3	85*/100ns	Industrial

^{*} The parameter is measured with 30pF test load.

PARAMETER LIST FOR EACH SPEED BIN

					Spe	ed Bins			
	Parameter List	Symbol	*7	0ns	**8	5ns	10	0ns	Units
			Min	Max	Min	Max	Min	Max	
Read	Read cycle time	tRC	70	-	85	-	100	-	ns
	Address access time	tAA	-	70	-	85	-	100	ns
	Chip select to output	tco	-	70	-	85	-	100	ns
	Output enable to valid output	tOE	-	35	-	45	-	50	ns
	Chip select to low-Z output	tLZ	10	-	10	-	10	-	ns
	Output enable to low-Z output	toLZ	5	-	5	-	5	-	ns
	Chip disable to high-Z output	tHZ	0	25	0	30	0	30	ns
	Output disable to high-Z output	tonz	0	25	0	20	0	20	ns
	Output hold from address change	toH	10	-	10	-	15	-	ns
Write	Write cycle time	twc	70	-	85	-	100	-	ns
	Chip select to end of write	tcw	60	-	70		80	-	ns
	Address set-up time	tAS	0	-	0	-	0	-	ns
	Address valid to end of write	tAW	60	_	70	-	80	-	ns
	Write pulse width	tWP	55	-	60	-	70	-	ns
	Write recovery time	tWR	0	-	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	25	0	30	0	35	ns
	Data to write time overlap	tow	30	-	35	-	40	-	ns
	Data hold from write time	tDH	0	-	0	-	0	-	ns
	End write to output low-Z	tow	5	-	5	-	5	-	ns



^{*} The parameter is measured with 30pF test load for KM68V512AL-7L Family.
** The parameter is measured with 30pF test load for KM68U512AL-8L Family.

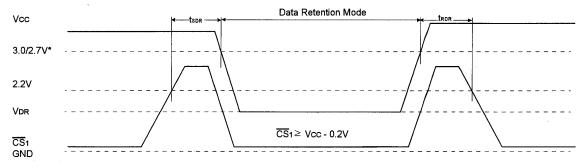
DATA RETENTION CHARACTERISTICS

Item		Symbol	Test Condition* CS₁***≥ Vcc-2.0V		Min	Typ**	Max	Unit
Vcc for data retention	VDR				2.0	-	3.6	٧
Data retention current	IDR	KM68V512AL-L KM68V512ALE-L KM68V512ALI-L KM68U512AL-L KM68U512ALE-L KM68U512ALI-L	Vcc=3.0V CS1≥Vcc-0.2V	LL-Ver LL-Ver LL-Ver LL-Ver LL-Ver	-	-	10 15 15 15 8 10	μA
Data retention set-up time	tSDF	₹	See data retention		0 '	-	-	ms
Recovery time	tRDF	₹	waveform		5	-	-	1115

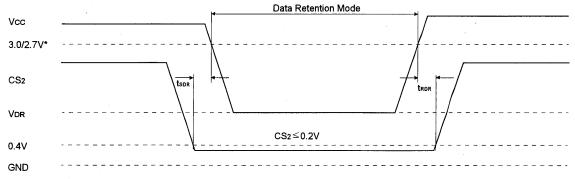
^{* 1)} Commercial Product : Ta=0 to 70 °C, unless otherwise specified

DATA RETENTION WAVE FORM

1) CS1 Controlled



2) CS2 Controlled



^{*3.0}V for KM68V512A Family, 2.7V for KM68U512A Family



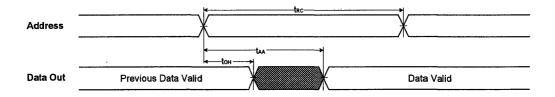
²⁾ Extended Product : Ta=-25 to 85°C, nless otherwise specified
3) Industrial Product : Ta=-40 to 85°C, unless otherwise specified
** Ta=25°C

^{***} $\overline{CS}_1 \ge Vcc-0.2V$, CS₂ $\ge Vcc-0.2V$ (\overline{CS}_1 controlled) or CS₂ $\le 0.2V$ (CS₂ controlled)

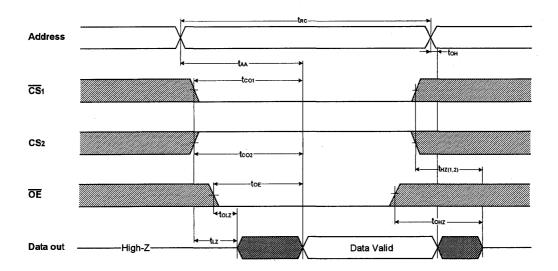
TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (1) (Address Controlled)

(CS=OE=VIL, CS2= WE=VIH)



TIMING WAVEFORM OF READ CYCLE(2) (WE=VIH)

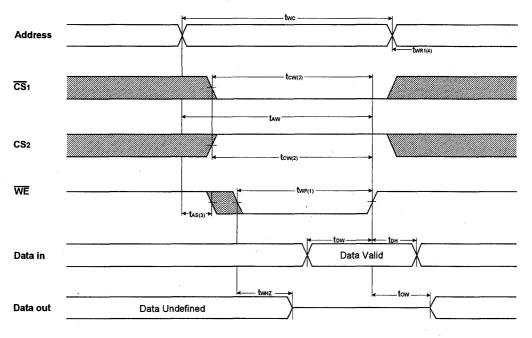


NOTES (READ CYCLE)

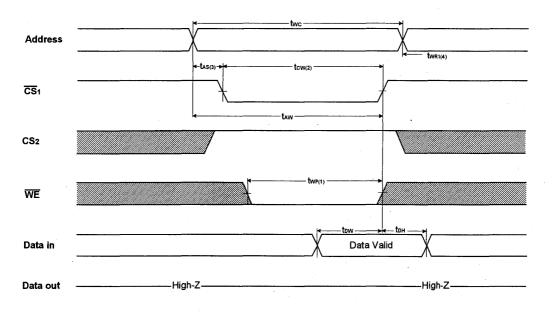
- 1. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
- 2. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device interconnection.



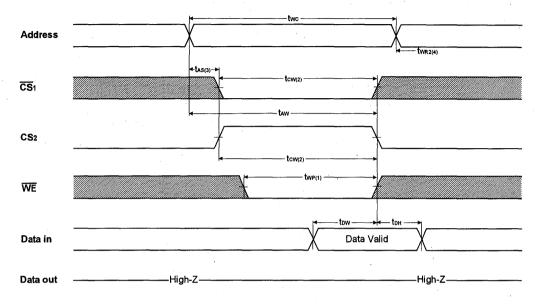
TIMING WAVEFORM OF WRITE CYCLE(1) (WE Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) (CS1 Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) (CS2 Controlled)



NOTES (WRITE CYCLE)

- I. A write occurs during the overlap of a low $\overline{\mathbb{CS}}_1$, a high \mathbb{CS}_2 and a low $\overline{\mathbb{WE}}$. A write begins at the latest transition among $\overline{\mathbb{CS}}_1$ goes low, \mathbb{CS}_2 going high and $\overline{\mathbb{WE}}$ going low: A write ends at the earliest transition among $\overline{\mathbb{CS}}_1$ going high, \mathbb{CS}_2 going low and \mathbb{WE} going high, \mathbb{WE} going high, \mathbb{WE} is measured from the begining of write to the end of write.
- 2. tCW is measured from the \overline{CS}_1 going low or CS_2 going high to the end of write.
- 3. $\ensuremath{\text{TAS}}$ is measured from the address valid to the beginning of write.
- 4. tWR is measured from the end of write to the address change. tWR1 applied in case a write ends as CS1 or WE going high tWR2 applied in case a write ends as CS2 going to low.

FUNCTIONAL DESCRIPTION

CS ₁	CS ₂	WE	ŌĒ	Mode	I/O Pin	Current Mode
Н	Х	Х	X	Power Down	High-Z	lsb, lsb1
X	L	Х	X	Power Down	High-Z	lsb, lsb1
L	• н	H.	н	Output Disable	High-Z	lcc
LL	Н	H	L	Read	Dout _	Icc
L /	н	L	X	Write	Din	Icc

^{*} X means don't care(Must be in high or low)



128K x8 bit Low Power and Low Voltage CMOS Static RAM

FEATURES

- . Process Technology ; 0.6 μm CMOS
- Organization : 128K x8
- Power Supply Voltage
 - KM68V1000B family : $3.3V \pm 0.3V$ KM68U1000B family : $3.0V \pm 0.3V$
- . Low Data Retention Voltage: 2V(Min)
- . Three state output and TTL Compatible
- Package Type: JEDEC Standard 32-SOP, 32-TSOP(I)-Forward/Reverse

GENERAL DESCRIPTION

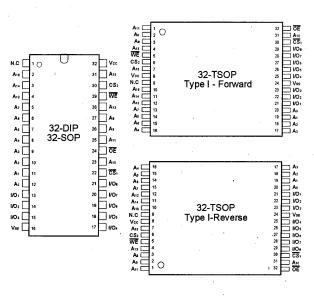
The KM68V1000B and KM68U1000B family are fabricated by SAMSUNG's advanced CMOS process technology. The family can support various operating temperature ranges and has various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

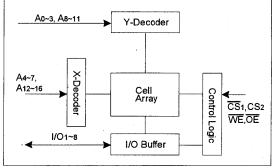
Product	0	,,,,		Power Dis				
Family	Operating Temperature	Vcc Range	Speed	Standby (IsB1, Max)	Operating (Icc2)	PKG Type		
KM68V1000BL/L-L	Commercial(0~70°C) `	3.0~3.6V	70*/100	50/15 <i>µ</i> Å	-			
KM68U1000BL/L-L	Commercial(0~70°C)	2.7~3.3V	100	50/15 <i>µ</i> A		32-SOP		
KM68V1000BEL/LE-L	Extended(-25~85 ℃)	3.0~3.6V	70*/100	100/20µÅ				
KM68U1000BEL/LE-L	Extended(-25~65 C)	2.7~3.3V	100	50/15 <i>µ</i> A	40mA	32-TSOP(I) R/F		
KM68V1000BLI/LI-L	Industrial (40-95°C)	3.0~3.6V	70*/100	100/20 <i>µ</i> A	1	•		
KM68U1000BLI/LI-L	Industrial(-40~85℃)	2.7~3.3V	100	50/15 <i>µ</i> A				

^{*}The parameter is measured with 30pF test load.

PIN DESCRIPTION



FUNCTIONAL BLOCK DIAGRAM



Name	Function
A0~A16	Address Inputs
WE	Write Enable Input
CS1,CS2	Chip Select Input
ŌĒ	Output Enable Input
I/O1~I/O8	Data Inputs/Outputs
Vcc	Power
Vss	Ground
N.C	No Connection

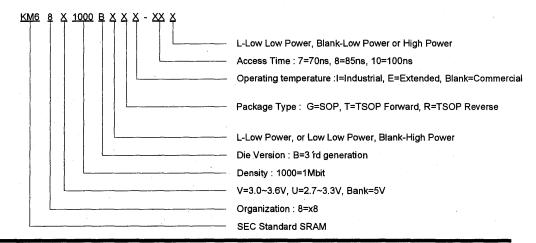


PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST

	al Temp Product 0~70℃)		Temp Products 5~85℃)		Temp Products 0~85°C)
Part Name	Function	Part Name	Function	Part Name	Function
KM68V1000BLG-7	32-SOP,70ns,3.3V,L	KM68V1000BLGE-7	32-SOP,70ns,3.3V,L	KM68V1000BLGI-7	32-SOP,70ns,3.3V,L
KM68V1000BLG-7L	32-SOP,70ns,3.3V,LL	KM68V1000BLGE-7L	32-SOP,70ns,3.3V,LL	KM68V1000BLGI-7L	32-SOP,70ns,3.3V,LL
KM68V1000BLG-10	32-SOP,100ns,3.3V,L	KM68V1000BLGE-10	32-SOP,100ns,3.3V,L	KM68V1000BLGI-10	32-SOP,100ns,3.3V,L
KM68V1000BLG-10L	32-SOP,100ns,3.3V,LL	KM68V1000BLGE-10L	32-SOP,100ns,3.3V,LL	KM68V1000BLGI-10L	32-SOP,100ns,3.3V,LL
KM68V1000BLT-7	32-TSOP F,70ns,3.3V,L	KM68V1000BLTE-7	32-TSOP F,70ns,3.3V,L	KM68V1000BLTI-7	32-TSOP F,70ns,3.3V,L
KM68V1000BLT-7L	32-TSOP F,70ns,3.3V,LL	KM68V1000BLTE-7L	32-TSOP F,70ns,3.3V,LL	KM68V1000BLTI-7L	32-TSOP F,70ns,3.3V,LL
KM68V1000BLT-10	32-TSOP F,100ns,3.3V,L	KM68V1000BLTE-10	32-TSOP F,100ns,3.3V,L	KM68V1000BLTI-10	32-TSOP F,100ns,3.3V,L
KM68V1000BLT-10L	32-TSOP F,100ns,3.3V,LL	KM68V1000BLTE-10L	32-TSOP F,100ns,3.3V,LL	KM68V1000BLTI-10L	32-TSOP F,100ns,3.3V,LL
KM68V1000BLR-7	32-TSOP R,70ns,3.3V,L	KM68V1000BLRE-7	32-TSOP R,70ns,3.3V,L	KM68V1000BLRI-7	32-TSOP R,70ns,3.3V,L
KM68V1000BLR-7L	32-TSOP R,70ns,3.3V,LL	KM68V1000BLRE-7L	32-TSOP R,70ns,3.3V,LL	KM68V1000BLRI-7L	32-TSOP R,70ns,3.3V,LL
KM68V1000BLR-10	32-TSOP R,100ns,3.3V,L	KM68V1000BLRE-10	32-TSOP R,100ns,3.3V,L	KM68V1000BLRI-10	32-TSOP R,100ns,3.3V,L
KM68V1000BLR-10L	32-TSOP R,100ns,3.3V,LL	KM68V1000BLRE-10L	32-TSOP R,100ns,3.3V,LL	KM68V1000BLRI-10L	32-TSOP R,100ns,3.3V,LL
KM68U1000BLG-8	32-SOP,85ns,3.0V,L	KM68U1000BLGE-10	32-SOP,100ns,3.0V,L	KM68U1000BLGI-10	32-SOP,100ns,3.0V,L
KM68U1000BLG-8L	32-SOP,85ns,3.0V,LL	KM68U1000BLGE-10L	32-SOP,100ns,3.0V,LL	KM68U1000BLGI-10L	32-SOP,100ns,3.0V,LL
KM68U1000BLG-10	32-SOP,100ns,3.0V,L	KM68U1000BLTE-10	32-TSOP F,100ns,3.0V,L	KM68U1000BLTI-10	32-TSOP F,100ns,3.0V,L
KM68U1000BLG-10L	32-SOP,100ns,3.0V,LL	KM68U1000BLTE-10L	32-TSOP F,100ns,3.0V,LL	KM68U1000BLTI-10L	32-TSOP F,100ns,3.0V,LL
KM68U1000BLT-8	32-TSOP F,85ns,3.0V,L	KM68U1000BLRE-10	32-TSOP R,100ns,3.0V,L	KM68U1000BLRI-10	32-TSOP R,100ns,3.0V,L
KM68U1000BLT-8L	32-TSOP F,85ns,3.0V,LL	KM68U1000BLRE-10L	32-TSOP R,100ns,3.0V,LL	KM68U1000BLRI-10L	32-TSOP R,100ns,3.0V,LL
KM68U1000BLT-10	32-TSOP F,100ns,3.0V,L	ľ	·		
KM68U1000BLT-10L	32-TSOP F,100ns,3.0V,LL]	,		j .
KM68U1000BLR-8	32-TSOP R,85ns,3.0V,L				
KM68U1000BLR-8L	32-TSOP R,85ns,3.0V,LL	1			
KM68U1000BLR-10	32-TSOP R,100ns,3.0V,L	1			
KM68U1000BLR-10L	32-TSOP R,100ns,3.0V,LL				

ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	Vin,Vout	-0.5 to Vcc+0.5	٧	-
Voltage on Vcc supply relative to Vss	Vcc	-0.3 to 4.6	V	-
Power Dissipation	Po	0.7	w	-
Storage Temperature	Тѕтс	-65 to 150	ဗ	-
		0 to 70	င	68V1000BL/L-L,68U1000BL/L-L
Operating Temperature	TA	-25 to 85	°C	68V1000BLE/LE-L,68U1000BLE/LE-L
		-40 to 85	င	68V1000BLI/LI-L,68U1000BLI/LI-L
Soldering temperature and time	TSOLDER	260℃, 10sec (Lead Only)	-	-

^{*} Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*

Item	Symbol	Product	Min	Typ**	Max	Unit
Supply voltage	Vcc	KM68V1000B Family KM68U1000B Family	3.0 2.7	3.3 3.0	3.6 3.3	٧
Ground	Vss	All Family	0	0	0	٧
Input high voltage	ViH	KM68V1000B Family KM68U1000B Family	2.2 2.2	-	Vcc+0.3 Vcc+0.3	٧
Input low voltage	VIL	KM68V1000B Family KM68U1000B Family	-0.3*** -0.3***	-	0.4 0.4	V

^{* 1)} Commercial Product : Ta=0 to 70 ℃, unless otherwise specified

CAPACITANCE* (f=1MHz, Ta=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	CIN	VIN=0V	-	6	pF
Input/Output capacitance	Cio	Vio=0V	•	8	pF

^{*} Capacitance is sampled not 100% tested



²⁾ Extended Product : Ta=-25 to 85 ℃, unless otherwise specified

³⁾ Industrial Product : Ta=-40 to 85 °C, unless otherwise specified

^{**} TA=25℃

^{***} $V_{IL}(min)$ =-3.0V for \leq 30ns pulse width

DC AND OPERATING CHARACTERISTICS

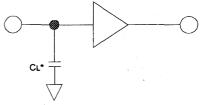
	Item	Symbol	Test Condition	ons*	Min	Typ**	Max	Unit
Input leak	age current	lu lu	VIN= Vss to Vcc		-1	-	1	μA
Output lea	kage current	lLO	CS1=VIH or CS2=VIL or WE=VIL,	Vio=Vss to Vcc	-1	-	1	μA
Operating	power supply current	Icc	CS1=VIL, CS2=VIH, VIN=VIH or VI	L, IIO=0mA	-	2	5	mA
Average o	perating current	ICC1	1 μs cycle 100% duty, lio=0mA CS1≤ 0.2V, CS2≥ Vcc-0.2V		-	3	5	mA
		ICC2	CS1=VIL, CS2=VIH, Min cycle, 100% duty, lio=0mA		-	30	40	mA
Output low	v voltage	Vol	IoL=2.1mA		-	-	0.4	٧
Output hig	h voltage	Voн	IOH=-1.0mA		2.2	-	-	· v
Standby C	current(TTL)	IsB	CS1=ViH, CS2=ViH		-	-	0.3	mA
	68V1000BL/L-L			L (Low Power) LL (Low Low Power)	-	1 0.5	50 15	μA
Standby Current	68V1000BLE/LE-L 68V1000BLI/LI-L	ISB1		L (Low Power) LL (Low Low Power)	-	1 0.5	100 20	μA
(CMOS)	68U1000BL/L-L	1581	Other input = 0~Vcc	L (Low Power) LL (Low Low Power)	-	1 0.5	50 15	μA
	68U1000BLE/LE-L 68U1000BLI/LI-L			L (Low Power) LL (Low Low Power)	-	1 0.5	50 15	μA

A.C CHARACTERISTICS

TEST CONDITIONS (1.Test Load and Test Input/Output Reference)*

Item	Value	Remark
Input pulse level	0.4 to 2.2V	-
Input riseing and falling time	5ns	-
input and output reference voltage	1.5V	
Output load (See right)	CL=100pF+1TTL	-

^{*} See DC Operating conditions



^{*} Including scope and jig capacitance

^{* 1)} Commercial Product : Ta=0 to 70°C, Vcc=3.3V±0.3V(68V1000B Family), Vcc=3.0V±0.3V(68U1000B Family)
2) Extended Product : Ta=-25 to 85°C, Vcc=3.3V±0.3V(68V1000BE Family), Vcc=3.0V±0.3V(68U1000BE Family)
2) Industrial Product : Ta=-40 to 85°C, Vcc=3.3V±0.3V(68V1000BI Family), Vcc=3.0V±0.3V(68U1000BI Family)

^{**} TA=25℃

TEST CONDITIONS (2. Temperature and Vcc Conditions)

Product Family	Temperature	Power Supply(Vcc)	Speed Bin	Comments
KM68V1000BL/L-L	0~70℃	3.3V±0.3	70*/100ns	Commercial
KM68V1000BLE/LE-L	-25~85℃	3.3V±0.3	70*/100ns	Extended
KM68V1000BLI/LI-L	-40~85℃	3.3V±0.3	70*/100ns	Industrial
KM68U1000BL/L-L	0~70℃	3.0V±0.3	70ns	Commercial
KM68U1000BLE/LE-L	-25~85℃	3.0V±0.3	100ns	Extended
KM68U1000BLI/LI-L	-40~85℃	. 3.0V±0.3	100ns	Industrial

^{*} The parameter is measured with 30pF test load.

PARAMETER LIST FOR EACH SPEED BIN

				Spee	d Bins		
	Parameter List	Symbol	*7	Ons	100ns		Units
			Min	Max	Min	Max	
Read	Read cycle time	tRC	70	-	100	-	ns
	Address access time	tAA	-	70	-	100	ns
	Chip select to output	tco	-	70	-	100	ns
	Output enable to valid output	toE	-	35	-	50	ns
	Chip select to low-Z output	tLZ	10	-	10	-	ns
	Output enable to low-Z output	tOLZ	5	-	5	-	ns
	Chip disable to high-Z output	tHZ	0	25	0	30	ns
	Output disable to high-Z output	tonz	0	25	0	30	ns
	Output hold from address change	ton	10	-	15	-	ns
Write	Write cycle time	twc	70	-	100	-	ns
	Chip select to end of write	tcw	60	-	80	-	ns
	Address set-up time	tAS	0	-	0	-	ns
	Address valid to end of write	tAW	60	-	80	-	ns
	Write pulse width	tWP	55	-	70	-	ns
	Write recovery time	twr	0		0	-	ns
	Write to output high-Z	tWHZ	0	25	0	30	ns
	Data to write time overlap	tow	30	-	40	-	ns
	Data hold from write time	t DH	0	-	0	-	ns
	End write to output low-Z	tow	5	-	5	-	ns

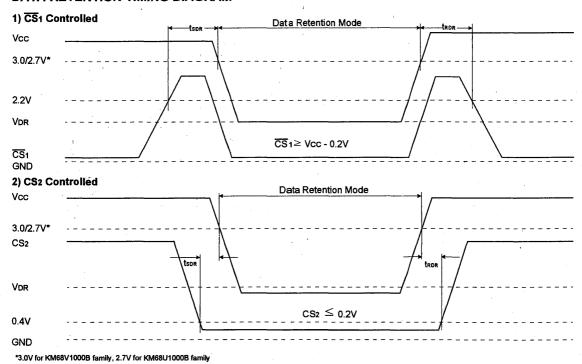
^{*} The parameter is measured with 30pF test load.

DATA RETENTION CHARACTERISTICS

Item	Symbol		Test Condit	ion*	Min	Typ**	Max	Unit
Vcc for data retention	VDR		CS1*** ≥ Vcc-2.0V	,	2.0	-	3.6	V
		KM68V1000BL KM68V1000BL-L		L-Ver LL-Ver	-	1 0.5	30 15	
		KM68V1000BLE KM68V1000BLE-L	V cc=3.0V CS1≥Vcc-0.2V	L-Ver LL-Ver	-	-	50 20	
		KM68V1000BLI-L KM68V1000BL KM68U1000BL KM68U1000BL-L		L-Ver LL-Ver	-	-	50 20	μA
Data retention current	IDR			L-Ver LL-Ver	-	-	25 10	
		KM68U1000BLE KM68U1000BLE-L		L-Ver LL-Ver	-	-	25 15	
		KM68U1000BLI KM68U1000BLI-L		L-Ver LL-Ver	-	-	25 15	
Data retention set-up time	tSDF	₹	See data retention	wovoform	0	-	-	
Recovery time	tRDF	₹	- See data retention	See data retention waveform		-	-	ms

^{* 1)} Commercial Product : Ta=0 to 70 °C, unless otherwise specified

DATA RETENTION TIMING DIAGRAM

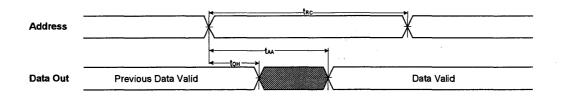


²⁾ Extended Product : TA=-25 to 85°C, unless otherwise specified
2) Industrial Product : TA=-40 to 85°C, unless otherwise specified
** TA=25°C

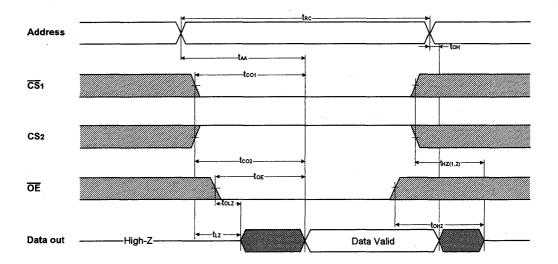
^{***} CS1 > Vcc-0.2V, CS2 > Vcc-0.2V(CS1 controlled) or CS2 < 0.2V(CS2 controlled)

TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (1) (Address Controlled) (CS=OE=VIL, CS2=WE=VIH)



TIMING WAVEFORM OF READ CYCLE(2) (WE=VIH)

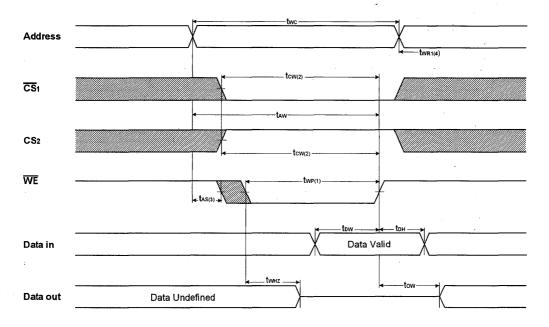


NOTES (READ CYCLE)

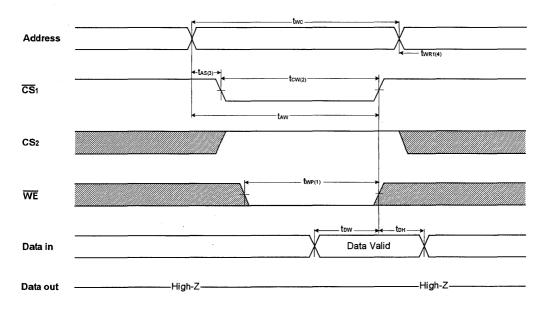
- 1. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
- 2. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device.



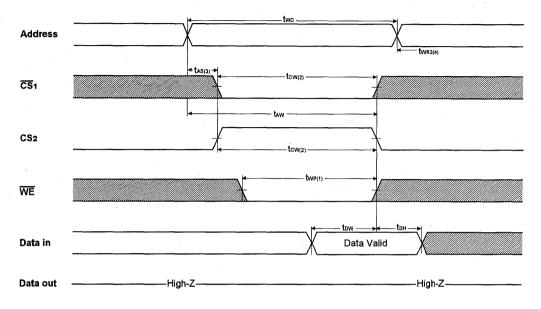
TIMING WAVEFORM OF WRITE CYCLE(1) (WE Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) (CS1 Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) (CS2 Controlled)



NOTES (WRITE CYCLE)

- 1. A write occurs during the overlap of low \overline{CS}_1 , high CS2 and low \overline{WE} . A write begins at the latest transition among \overline{CS}_1 going low, CS2 going high and \overline{WE} going low. A write ends at the earliest transition among \overline{CS}_1 going high, CS2 going low and \overline{WE} going high, \overline{tWP} is measured from the beginning or write to the end of write.
- 2. tCW is measured from the later of CS1 going low or CS2 going high to the end of write.
- 3. tAS is measured from the address valid to the beginning of write.
- 4. tWR is measured from the end of write to the address change. tWR1 applied in case a write ends at CS1, or WE going high, tWR2 applied in case a write ends at CS2 going to low.

FUNCTIONAL DESCRIPTION

CS ₁	CS2	WE	ŌĒ	Mode	I/O Pin	Current Mode
. H	Х	Х	х	Power Down	High-Z	ISB,ISB1
Х	L	·X	Х	Power Down	High-Z	ISB,ISB1
L	Н	Н	Н	Output Disable	High-Z	Icc
L	Н	Н	L	Read	Dout	Icc
·L	Н	L	Х	Write	Din	Icc

^{*} X means don't care (Must be in high or low state)



128K x8 bit Low Power and Low Voltage CMOS Static RAM

FEATURES

• Process Technology: 0.4 µm CMOS

• Organization : 128K x8

Power Supply Voltage :

KM68V1000C family: 3.3V±0.3V KM68U1000C family: 3.0V±0.3V • Low Data Retention Voltage: 2V(Min)

. Three state output and TTL Compatible

• Package Type : JEDEC Standard

32-SOP, 32-TSOP(I)-F/R, 32-sTSOP(I)-F/R

GENERAL DESCRIPTION

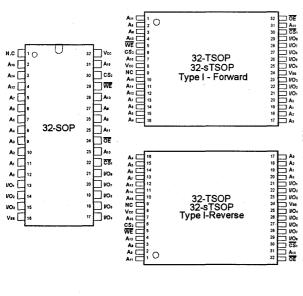
The KM68V1000C and KM68U1000C family are fabricated by SAMSUNG's advanced CMOS process technology. The family can support various operating temperature ranges and has various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

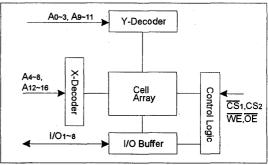
Product	O	Vec		Power Di	Power Dissipation				
Family	Operating Temperature	Range(V)	Speed	Standby (Isa1, Max)	Operating (Icc2)	PKG Type			
KM68V1000CL-L	Commercial	Commercial 3.0~3.6V		10 <i>µ</i> Å					
KM68U1000CL-L	(0~70℃)	2.7~3.3V	70*/100ns			32-SOP 32-sTSOP(I) R/F			
KM68V1000CLE-L	Extended	3.0~3.6V	70/85ns	20 <i>µ</i> A	404				
KM68U1000CLE-L	(-25~85℃)	2.7~3.3V	70*/100ns		40mA	32-TSOP(I) R/F			
KM68V1000CLI-L	Industrial	3.0~3.6V	70/85ns	20 <i>µ</i> A					
KM68U1000CLI-L	(-25~85℃)	2.7~3.3V	70*/100ns						

^{*}The parameter is measured with 30pF test load.

PIN DESCRIPTION



FUNCTIONAL BLOCK DIAGRAM



Name	Function
A0~A16	Address Inputs
WE	Write Enable Input
CS1,CS2	Chip Select Inputs
ŌĒ	Output Enable Input
I/O1~I/O8	Data Inputs/Outputs
Vcc	Power
Vss	Ground
N.C	No Connection

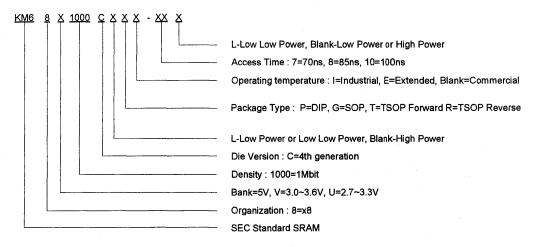


PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST

	al Temp Product I~70℃)		Temp Products 5~85°C)	Industrial Temp Products (-40~85°C)	
Part Name	Function	Part Name	Function	Part Name	Function
KM68V1000CLG-7L	32-SOP,70ns,3.3V,LL	KM68V1000CLGE-7L	32-SOP,70ns,3.3V,LL	KM68V1000CLGI-7L	32-SOP,70ns,3.3V,LL
KM68V1000CLG-8L	32-SOP,85ns,3.3V,LL	KM68V1000CLGE-8L	32-SOP,85ns,3.3V,LL	KM68V1000CLGI-8L	32-SOP,85ns,3.3V,LL
KM68V1000CLT-7L	32-TSOP F,70ns,3.3V,LL	KM68V1000CLTE-7L	32-TSOP F,70ns,3.3V,LL	KM68V1000CLTI-7L	32-TSOP F,70ns,3.3V,LL
KM68V1000CLT-8L	32-TSOP F,85ns,3.3V,LL	KM68V1000CLTE-8L	32-TSOP F,85ns,3.3V,LL	KM68V1000CLTI-8L	32-TSOP F,85ns,3.3V,LL
KM68V1000CLR-7L	32-TSOP R.70ns.3.3V.LL	KM68V1000CLRE-7L	32-TSOP R,70ns,3.3V,LL	KM68V1000CLRI-7L	32-TSOP R,70ns,3.3V,LL
KM68V1000CLR-8L	32-TSOP R,85ns,3.3V,LL	KM68V1000CLRE-8L	32-TSOP R,85ns,3.3V,LL	KM68V1000CLRI-8L	32-TSOP R,85ns,3.3V,LL
KM68U1000CLG-7L	32-SOP.70ns.3.0V.LL	KM68U1000CLGE-7L	32-SOP,70ns,3.0V,LL	KM68U1000CLGI-7L	32-SOP,70ns,3.0V,LL
KM68U1000CLG-10L	32-SOP.85ns,3.0V.LL	KM68U1000CLGE-10L	32-SOP,85ns,3.0V,LL	KM68U1000CLGI-10L	32-SOP,85ns,3.0V,LL
KM68U1000CLT-7L	32-TSOP F.70ns.3.0V.LL	KM68U1000CLTE-7L	32-TSOP F,70ns,3.0V,LL	KM68U1000CLTI-7L	32-TSOP F.70ns.3.0V.LL
KM68U1000CLT-10L	32-TSOP F.100ns,3.0V,LL	KM68U1000CLTE-10L	32-TSOP F,100ns,3.0V,LL	KM68U1000CLTI-10L	32-TSOP F,100ns,3.0V,LL
KM68U1000CLR-7L	32-TSOP R.70ns.3.0V.LL	KM68U1000CLRE-7L	32-TSOP R.70ns,3.0V,LL	KM68U1000CLRI-7L	32-TSOP R,70ns,3.0V,LL
KM68U1000CLR-10L	32-TSOP R,100ns,3.0V,LL	KM68U1000CLRE-10L	32-TSOP R,100ns,3.0V,LL	KM68U1000CLRI-10L	32-TSOP R,100ns,3.0V,LL
KM68V1000CLTG-7L	32-sTSOP F.70ns.3.3V.LL	KM68V1000CLTGE-7L	32-sTSOP F,70ns,3.3V,LL	KM68V1000CLTGI-7L	32-sTSOP F,70ns,3.3V,LL
KM68V1000CLTG-8L	32-sTSOP F.85ns.3.3V.LL	KM68V1000CLTGE-8L	32-sTSOP F,85ns,3.3V,LL	KM68V1000CLTGI-8L	32-sTSOP F.85ns.3.3V LL
KM68V1000CLRG-7L	32-sTSOP R,70ns,3,3V,LL	KM68V1000CLRGE-7L	32-sTSOP R,70ns,3.3V,LL	KM68V1000CLRGI-7L	32-sTSOP R,70ns,3.3V,LL
KM68V1000CLRG-8L	32-sTSOP R,85ns,3.3V,LL	KM68V1000CLRGE-8L	32-sTSOP R,85ns,3.3V,LL	KM68V1000CLRGI-8L	32-sTSOP R,85ns,3.3V,LL
KM68U1000CLTG-7L	32-sTSOP F,70ns,3.0V,LL	KM68U1000CLTGE-7L	32-sTSOP F,70ns,3.0V,LL	KM68U1000CLTGI-7L	32-sTSOP F,70ns,3.0V,LL
KM68U1000CLTG-10L	32-sTSOP F 100ns 3.0V,LL	KM68U1000CLTGE-10L	32-sTSOP F,100ns,3.0V,LL	KM68U1000CLTGI-10L	32-sTSOP F,100ns,3.0V,LI
KM68U1000CLRG-7L	32-sTSOP R,70ns,3.0V,LL	KM68U1000CLRGE-7L	32-sTSOP R,70ns,3.0V,LL	KM68U1000CLRGI-7L	32-sTSOP R,70ns,3.0V,LL
KM68U1000CLRG-10L		KM68U1000CLRGE-10L	32-sTSOP R 100ns,3.0V,LL	KM68U1000CLRGI-10L	32-sTSOP R,100ns,3.0V,L

ORDERING INFORMATION





ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	VIN, VOUT	-0.5 to Vcc+0.5	٧	-
Voltage on Vcc supply relative to Vss	Vcc	-0.3 to 4.6	V	· · · · · · · ·
Power Dissipation	Po	0.7	W	- 1
Storage temperature	Тѕтс	-65 to 150	°C	
		0 to 70	°C	KM68V1000CL-L/KM68U1000CL-L
Operating Temperature	TA	-25 to 85	င	KM68V1000CLE-L/KM68U1000CLE-L
		-40 to 85	င	KM68V1000CLI-L/KM68U1000CLI-L
Soldering temperature and time	TSOLDER	260°C, 10sec (Lead Only)	-	-

^{*} Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*

ltem	Symbol	Product	Min	Typ**	Max	Unit
Supply voltage	Vcc	KM68V1000C Family KM68U1000C Family	3.0 2.7	3.3 3.0	3.6 3.3	٧
Ground	Vss	All Family	0	0	0	V
Input high voltage	ViH	KM68V1000C Family KM68U1000C Family	2.2 2.2	-	Vcc+0.3 Vcc+0.3	٧
Input low voltage	VIL	KM68V1000C Family KM68U1000C Family	-0.3*** -0.3***	-	0.4 0.4	٧

^{* 1)} Commercial Product : Ta=0 to 70 °C, unless otherwise specified

CAPACITANCE* (f=1MHz, TA=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	Cin	VIN=0V	-	6	pF
Input/Output capacitance	Cio	Vio=0V	-	8	pF

^{*} Capacitance is sampled, not 100% tested



²⁾ Extended Product : Ta=-25 to 85℃, unless otherwise specified

³⁾ Industrial Product : Ta=-40 to 85 $^{\circ}\mathrm{C}$, unless otherwise specified

^{**} Ta=25℃

^{***} VIL(min)=-3.0V for \(\le \) 30ns pulse width

DC AND OPERATING CHARACTERISTICS

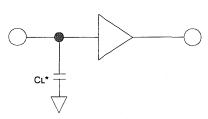
	Item	Symbol	Test Conditions*		Min	Тур**	Max	Unit
Input leak	age current	lu	VIN=Vss to Vcc		-1	-	1	μA
Output lea	akage current	ILO	CS1=VIH or CS2=VIL or WE=VIL, Vio=	CS1=VIH or CS2=VIL or WE=VIL, Vio=Vss to Vcc		-	1	μA
Operating	power supply current	Icc	CS1=VIL,CS2=VIH,VIN=VIH or VIL	Read	-	-	5	mA
		100	lio=0mA	Write			15	
		ICC1	Cycle time=1 µs 100% duty, Iio=0mA	Read	-	-	5	mA
Average o	verage operating current		<u>CS</u> 1≤0.2V, CS2≥Vcc-0.2V	Write			15	"'
		ICC2	Min cycle, 100% duty, Iio=0mA, CS1=VIL, CS2=VIH		-	30	40	mA
Output lov	v voltage	Vol	IoL=2.1mA		-	-	0.4	V
Output hig	jh voltage	Voн	Iон=-1.0mA		2.2	-	-	V
Standby 0	Current(TTL)	ISB	CS1=VIH, CS2=VIL		-	-	0.3	mA
Standby Current (CMOS)	KM68V1000CL-L KM68V1000CLE-L KM68V1000CLI-L	lsB1	$\overline{CS}_1 \ge V_{CC}$ -0.2V Low Low Po $CS_2 \ge V_{CC}$ -0.2V or $CS_2 \le 0.2$ V Other input =0~Vcc		-	0.5 0.5 0.5	10 20 20	μΑ
•	KM68U1000CL-LI KM68U1000CLE-L KM68U1000CLI-L				-	0.5 0.5 0.5	10 20 20	μA

A.C CHARACTERISTICS

TEST CONDITIONS (1.Test Load and Test Input/Output Reference)*

Item	Value	Remark
Input pulse level	0.4 to 2.2V	-
Input rising and falling time	5ns	-
input and output reference voltage	1.5V	<u>.</u>
Output load (See right)	CL=100pF+1TTL **CL=30pF+1TTL	-

^{*} See DC Operating conditions ** KM68U1000CL-7L Family



* Including scope and jig capacitance



^{* 1)} Commercial Product : TA=0 to 70°C, Vcc=3.3V±0.3V(68V1000C Family), Vcc=3.0V±0.3V(68U1000C Family) 2) Extended Product : TA=-25 to 85°C, Vcc=3.3V±0.3V(68V1000CE Family), Vcc=3.0V±0.3V(68U1000CE Family) 3) Industrial Product : TA=-40 to 85°C, Vcc=3.3V±0.3V(68V1000CI Family), Vcc=3.0V±0.3V(68U1000CI Family)

** TA=25°C

TEST CONDITIONS (2. Temperature and Vcc Conditions)

Product Family	Temperature	Power Supply(Vcc)	Speed Bin	Comments
KM68V1000CL-L	0~70℃	3.3V±0.3	70/85ns	Commercial
KM68V1000CLE-L	-25~85℃	3.3V±0.3	70/85ns	Extended
KM68V1000CLI-L	-40~85℃	3.3V±0.3	70/85ns	Industrial
KM68U1000CL-L	0~70℃	3.0V±0.3	70*/100ns	Commercial
KM68U1000CLE-L	-25~85℃	3.0V±0.3	70*/100ns	Extended
KM68U1000CLI-L	-40~85℃	3.0V±0.3	70*/100ns	Industrial

^{*} The parameter is measured with 30pF test load.

PARAMETER LIST FOR EACH SPEED BIN

					Spec	d Bins			
	Parameter List	Symbol	70	70ns		ins	100ns		Units
			Min	Max	Min	Max	Min	Max	
Read	Read cycle time	tRC	70	-	85	-	100	-	ns
	Address access time	tAA	-	70	-	85	-	100	ns
	Chip select to output	tco	-	70	-	85	-	100	ns
	Output enable to valid output	toE	-	35	-	40	-	50	ns
	Chip select to low-Z output	tLZ	10	-	10	-	10	-	ns
	Output enable to low-Z output	toLZ	5	-	5	-	5	-	ns
	Chip disable to high-Z output	tHZ	0	25	0	25	0	30	ns
	Output disable to high-Z output	tonz	0	25	0	25	0	30	ns
	Output hold from address change	tон	10	-	15	-	15	-	ns
Write	Write cycle time	twc	70	-	85	-	100	-	ns
	Chip select to end of write	tcw	60	-	70	-	80	-	ns
	Address set-up time	tAS	0	-	0		0	-	ns
	Address valid to end of write	tAW	60	-	70	-	80	-	ns .
	Write pulse width	tWP	55	-	60	-	70	-	ns
	Write recovery time	twr	0	-	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	25	0	30	0	30	ns
	Data to write time overlap	tDW	30	-	35	-	40	-	ns
	Data hold from write time	tDH	0	-	0	-	0	-	ns
	End write to output low-Z	tow	5	-	5	-	5		ns

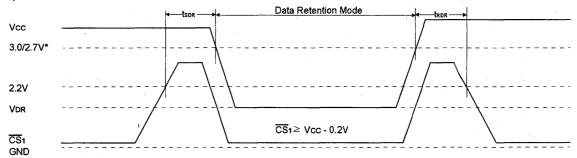
DATA RETENTION CHARACTERISTICS

Item	Symbol VDR		Test Condition* CS₁*** ≥ Vcc-0.2V		Min	Typ**	Max	Unit
Vcc for data retention					2.0	-	3.6	V
Data retention current	IDR	KM68V1000CL-L KM68V1000CLE-L KM68V1000CLI-L KM68U1000CL-L KM68U1000CLE-L KM68U1000CLI-L	Vcc=3.0V CS1≥Vcc-0.2V	Low Low Power	- - - -	0.5 0.5 0.5 0.5 0.5	10 20 20 10 20 20	μΑ
Data retention set-up time	tsDR		See data retention waveform		0	_	-	ms
Recovery time	trdr				5	-	-	

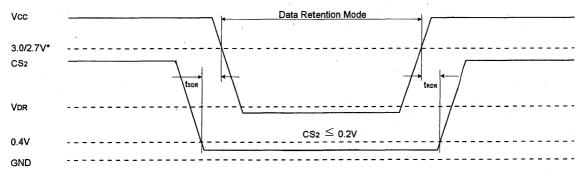
^{* 1)} Commercial Product : Ta=0 to 70 $^{\circ}\mathrm{C}$, unless otherwise specified

DATA RETENTION TIMING DIAGRAM

1) CS1 Controlled



2) CS2 Controlled



^{*3.0}V for KM68V1000C family, 2.7V for KM68U1000C family



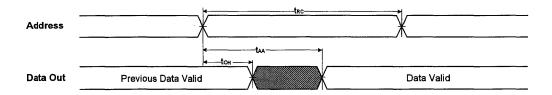
²⁾ Extended Product: Ta=-25 to 85°C, unless otherwise specified

²⁾ Industrial Product : Ta=-40 to 85 ℃, unless otherwise specified ** Ta=25 ℃

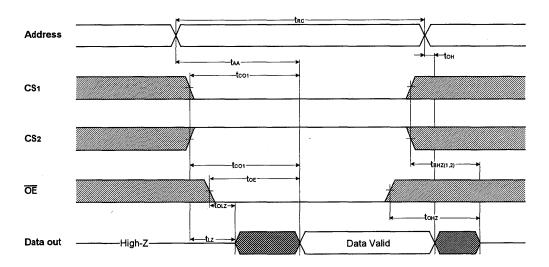
^{***} $\overline{\text{CS}}_1 \ge \text{Vcc-0.2V}$, $\text{CS}_2 \ge \text{Vcc-0.2V}(\overline{\text{CS}}_1 \text{ controlled})$ or $\text{CS}_2 \le 0.2 \text{V}(\text{CS}_2 \text{ controlled})$

TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled) (CS1=OE=VIL, CS2=WE=VIH)



TIMING WAVEFORM OF READ CYCLE(2) (WE=VIH)

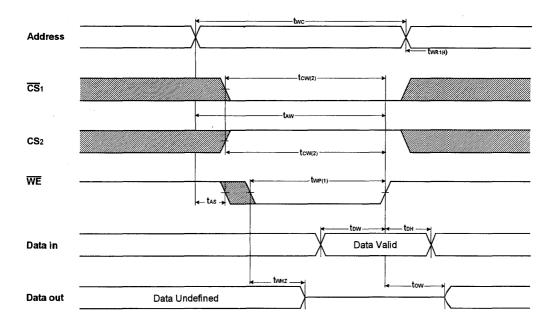


NOTES (READ CYCLE)

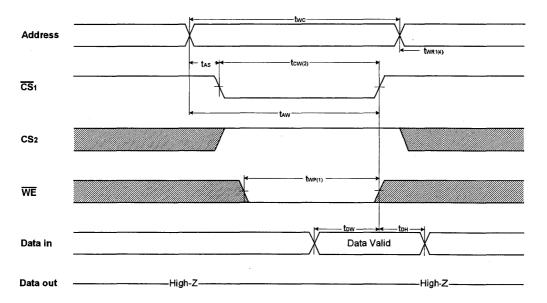
- 1. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
- 2. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device.



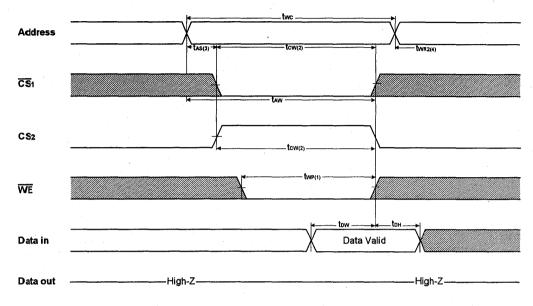
TIMING WAVEFORM OF WRITE CYCLE(1) (WE Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) (CS1 Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) (CS2 Controlled)



NOTES (WRITE CYCLE)

- 1. A write occurs during the overlap of low $\overline{CS_1}$, high CS2 and low \overline{WE} . A write begins at the latest transition among $\overline{CS_1}$ going low, CS2 going high and \overline{WE} going low. A write ends at the earliest transition among $\overline{CS_1}$ going high, CS2 going low and \overline{WE} going high, tWP is measured from the beginning or write to the end of write
- 2. tCW is measured from the later of CS1 going low or CS2 going high to the end of write.
- 3. tAS is measured from the address calld to the beginning of write.
- 4. tWR is measured from the end of write to the address change. tWR1 applied in case a write ends at CS1, or WE going high, tWR2 applied in case a write ends at CS2 going to low.

FUNCTIONAL DESCRIPTION

CS1	CS2	WE	ŌĒ	Mode	I/O Pin	Current Mode
Н	Х	Х	, X	Power Down	High-Z	ISB,ISB1
X	L	Х	Х	Power Down	High-Z	ISB,ISB1
L	Н	Н	Н	Output Disable	High-Z	lcc
L	Н	Н	L	Read	Dout	lcc
L	Н	L	. X	Write	Din	lcc

^{*} X means don't care (Must be in high or low status.)



64K x16 bit Low Power and Low Voltage CMOS Static RAM

FEATURES

• Process Technology: 0.6 µm CMOS

Organization: 64K x16

• Data Byte Control : LB=I/O1~8, UB=I/O9~16

· Power Supply Voltage :

KM616V1000B family : 3.3V \pm 0.3V KM616U1000B family : 3.0V \pm 0.3V

Low Data Retention Voltage : 2V(Min)

Three state output and TTL Compatible
 Package Type: JEDEC Standard

44-TSOP(II)-Forward/Reverse

GENERAL DESCRIPTION

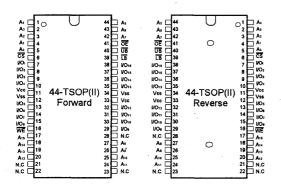
The KM616v1000B and KM616U1000B family are fabricated by SAMSUNG s advanced CMOS process technology. The family can support various operating temperature ranges and have various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

Product	Operating	Vec	Speed	Power Di	ssipation		
List	Temp.	(Isb1, Max) (Icc2) (I	Operating (Icc2)	PKG Type			
KM616V1000BL/L-L KM616U1000BL/L-L	Commercia (0~70℃)						
KM616V1000BLE/LE-L KM616U1000BLE/LE-L	Extended (-25~85℃)	0.0		1	65mA	44-TSOP(II) Forward/Reverse	
KM616V1000BLI/LI-L KM616U1000BLI/LI-L	Industrial (-40~85℃)	3.0~3.6V 2.7~3.3V	85*/100 100	100/20 μA 100/20 μA			

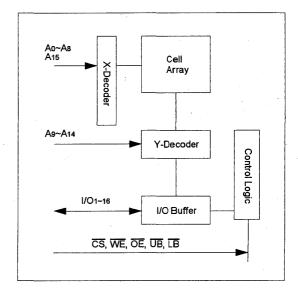
^{*} The parameter is measured with 30pF test load.

PIN DESCRIPTION



Name	Function	Name	Function
A0~A15	Address Inputs	LB	Lower Byte (I/O1~8)
WE	Write Enable Input	ŪB	Upper Byte(I/O9~16)
cs	Chip Select Input	Vcc	Power
ŌĒ	Output Enable Input	Vss	Ground
I/O0~16	Data Inputs/Outputs	N.C	No Connection

FUNCTIONAL BLOCK DIAGRAM



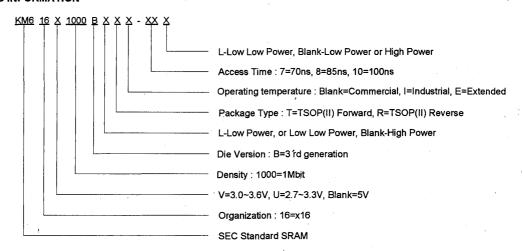


PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST

	ial Temp Product 0~70℃)		al Temp Product 25~85℃)		Temp Products 40~85℃)
Part Name	Function	Part Name	Function	Part Name	Function
KM616V1000BLT-7	44-TSOP(II), F, 3.3V, 70ns, L	KM616V1000BLTE-8	44-TSOP(II), F, 3.3V, 85ns, L	KM616V1000BLTI-8	44-TSOP(II), F, 3.3V, 85ns, L
KM616V1000BLT-7L	44-TSOP(II), F, 3.3V, 70ns, LL	KM616V1000BLTE-8L	44-TSOP(II), F, 3.3V, 85ns, LL	KM616V1000BLTI-8L	44-TSOP(II), F, 3.3V, 85ns, LL
KM616V1000BLT-10	44-TSOP(II), F, 3.3V, 100ns, L	KM616V1000BLTE-10	44-TSOP(II), F, 3.3V,100ns, L	KM616V1000BLTI-10	44-TSOP(II), F, 3.3V,100ns, L
KM616V1000BLT-10L	44-TSOP(II), F, 3.3V, 100ns, LL	KM616V1000BLTE-10L	44-TSOP(II), F, 3.3V, 100ns, LL	KM616V1000BLTI-10L	44-TSOP(II), F, 3.3V, 100ns, LL
KM616U1000BLT-10	44-TSOP(II), F, 3.0V, 100ns, L	KM616U1000BLTE-10	44-TSOP(II), F, 3.0V,100ns, L	KM616U1000BLTI-10	44-TSOP(II), F, 3.0V,100ns, L
KM616U1000BLT-10L	44-TSOP(II), F, 3.0V, 100ns, LL	KM616U1000BLTE-10L	44-TSOP(II), F, 3.0V, 100ns, LL	KM616U1000BLTI-10L	44-TSOP(II), F, 3.0V, 100ns, LL
KM616V1000BLR-7	44-TSOP(II), R, 3.3V, 70ns, L	KM616V1000BLRE-8	44-TSOP(II), R, 3.3V, 85ns, L	KM616V1000BLRI-8	44-TSOP(II), R, 3.3V, 85ns, L
KM616V1000BLR-7L	44-TSOP(II), R, 3.3V, 70ns, LL	KM616V1000BLRE-8L	44-TSOP(II), R, 3.3V, 85ns, LL	KM616V1000BLRI-8L	44-TSOP(II), R, 3.3V, 85ns, LL
KM616V1000BLR-10	44-TSOP(II), R, 3.3V, 100ns, L	KM616V1000BLRE-10	44-TSOP(II), R, 3.3V,100ns, L	KM616V1000BLRI-10	44-TSOP(II), R, 3.3V,100ns, L
KM616V1000BLR-10L	44-TSOP(II), R, 3.3V, 100ns, LL	KM616V1000BLRE-10L	44-TSOP(II), R, 3.3V, 100ns, LL	KM616V1000BLRI-10L	44-TSOP(II), R, 3.3V, 100ns, LL
KM616U1000BLR-10	44-TSOP(II), R, 3.0V, 100ns, L	KM616U1000BLRE-10	44-TSOP(II), R, 3.0V,100ns, L	KM616U1000BLRI-10	44-TSOP(II), R, 3.0V,100ns, L
KM616U1000BLR-10L	44-TSOP(II), R, 3.0V, 100ns, LL	KM616U1000BLRE-10L	44-TSOP(II), R, 3.0V, 100ns, LL	KM616U1000BLRI-10L	44-TSOP(II), R, 3.0V, 100ns, LL

ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	VIN,VOUT	-0.5 to Vcc+0.5	V	-
Voltage on Vcc supply relative to Vss	Vcc	-0.5 to 4.6	V	-
Power Dissipation	PD	1.0	w	-
Storage temperature	Тѕтс	-65 to 150	°C	-
		0 to 70	Ĉ	KM616V1000BL/L-L KM616U1000BL/L-L
Operating Temperature	Та	-25 to 85	°	KM616V1000BLE/LE-L KM616U1000BLE/LE-L
		-40 to 85	c	KM616V1000BLI/LI-L KM616U1000BLI/LI-L
Soldering temperature and time	TSOLDER	260°C, 10sec (Lead Only)	-	-

^{*} Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*

Item	Symbol	Product	Min	Typ**	Max	Unit
Supply voltage	Vcc	KM616V1000B Family KM616U1000B Family	3.0 2.7	3.3 3.0	3.6 3.3	V V
Ground	Vss	All Family	0	0	0	٧
Input high voltage	ViH	KM616V1000B Family KM616U1000B Family	2.2 2.2	-	Vcc+0.3 Vcc+0.3	V V
Input low voltage	VIL	KM616V1000B Family KM616U1000B Family	-0.5*** -0.5***	-	0.4 0.4	V V

^{* 1)} Commercial Product : Ta≃0 to 70 ℃, unless otherwise specified 2) Industrial Product : Ta=-40 to 85 ℃, unless otherwise specified

CAPACITANCE* (f=1MHz, TA=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	Cin	Vin=0V	-	6	pF
Input/Output capacitance	Cio	Vio=0V	-	8	pF

^{*} Capacitance is sampled not 100% tested



^{**} Ta=25℃

^{***} Vil(min)=-3.0V for ≤ 30ns pulse width

DC AND OPERATING CHARACTERISTICS

	ltem	Symbol	Test Conditions*			Typ**	Max	Unit	
Input leakag	e current	lu	VIN=Vss to Vcc		-1	-	1	μA	
Output leaka	age current	lıo	CS=VIH or WE=VIL, UB=VIH or VIO=Vss to Vcc	IB =Vін	-1	-	1	μA	
	power supply current peratingcurrent lc v voltage ph voltage current(TTL) ls 616V1000BL-L-L		CS=VIL, VIN=VIH or VIL,	Read	-	-	10	mA	
		100	lio=0mA	Write	-	-	35	mA	
		Icc1	Cycle time=1 µs 100% duty	Read	-1 - 1 -1 - 1 -1 - 1 -1 - 1 -1 - 1 -1 - 1 -1 - 1 -1 - 1 -1 - 1 -1 - 1 -1 - 1 -1 - 1 -1 - 10 -1 - 35 -1 - 40 -1 - 65 -1 - 65 -1 - 0.4 -1 - 0.5 -1 -			mA	
		ICC1	CS≤0.2V, lio=0mA	Write	A 65		40	IIIA	
	•	ICC2	Min cycle, 100% duty, CS=VIL	, lio=0mA			65	mA	
Output low v	/oltage	VôL	IoL=2.1mA		-	-	0.4	V	
Output high	voltage	Voн	Iон=-1.0mA		2.2	-	-	V	
Standby Cu	rrent(TTL)	ISB	CS=VIH		-	-	0.5	mA	
	616V1000BL-L-L			L(Low Power) LL(L Low Power)	-	-	1	μA	
Standby	tandby 616V1000BLI/Li-L 616V1000BLE/LE-L IsB1 CS≥Vcc-0.2V VIN≥Vcc-0.2V Other inputs = 0~Vcc CS≥Vcc-0.2V CS≥Vcc-		1	L(Low Power) LL(L Low Power)	-	-	1	μA	
(CMOS)			L(Low Power) LL(L Low Power)	-	-		μA		
	616U1000BLI/LI-L 616U1000BLE/LE-L			L(Low Power) LL(L Low Power)	-	-	100 20	μA	

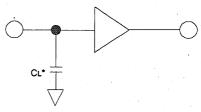
^{* 1)} Commercial Product : Ta=0 to 70 $^{\circ}$, Vcc=3.3V $^{\pm}$ 0.3V(616V1000B Family), Vcc=3.0V $^{\pm}$ 0.3V(616U1000B Family)

A.C CHARACTERISTICS

TEST CONDITIONS (1.Test Load and Test Input/Output Reference)*

Item	Value	Remark
Input pulse level	0.4 to 2.4V	<u>.</u>
Input rise fall time	5ns	-
input and output reference voltage	1.5V	. <u>-</u>
Output load (See right)	CL=100pF+1TTL **CL=30pF+1TTL	_

^{*} See DC Operating conditions ** for 70ns, 85ns products



* Including scope and jig capacitance



¹⁾ Commercial roduct : TA=-25 to 85°C, Vcc=3.3V ± 0.3V(616V100BI Family), Vcc=3.0V ± 0.3V(616U1000BI Family)
3) Industrial Product : TA=-40 to 85°C, Vcc=3.3V ± 0.3V(616V1000BI Family), Vcc=3.0V ± 0.3V(616U1000BI Family)

^{***} Industrial Product : Icc(Read/Write)=10mA/40mA, Icc2(Read/Write)=20mA/45mA

TEST CONDITIONS (2. Temperature and Vcc Conditions)

Product Family	Temperature	Power Supply(Vcc)	Speed Bin	Comments
KM616V1000BL-L KM616V1000BLE-L KM616V1000BLI-L	0~70℃ -25~85℃ -40~85℃	3.3V ± 0.3	70*/100ns 85*/100ns 85*/100ns	Commercial Extended Industrial
KM616U1000BL-L KM616U1000BLE-L KM616U1000BLI-L	0~70℃ -25~85℃ -40~85℃	3.0V ± 0.3	100ns	Commercial Extended Industrial

^{*} The parameter is measured with 30pF test load

PARAMETER LIST FOR EACH SPEED BIN

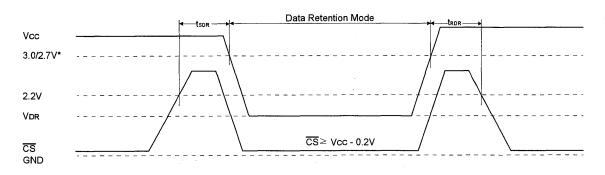
					Spec	ed Bins			
	Parameter List	Symbol	70	Ons	8:	5ns	10	0ns	Units
			Min	Min Max		Max	Min	Max	
Read	Read cycle time	tRC	70	-	85	-	100	-	ns
	Address access time	tAA	-	70	-	85	-	100	ns
	Chip select to output	tco	-	70	-	85	-	100	ns
	Output enable to valid output	tOE	-	35	-	40	-	50	ns
	UB,LB Access Time	tBA	-	35	-	40	-	50	ns
	Chip select to low-Z output	tLZ	5	-	5	-	5	-	ns
	UB,LB enable to low-Z output	tBLZ	10	-	10	-	10	-	ns
	Output enable to low-Z output	toLZ	5	-	5	-	5	-	ns
	Chip disable to high-Z output	tHZ	0	25	0	25	0	30	ns
	UB,LB disable to high-Z output	tBHZ	0	25	0	25	0	30	ns
	Output disable to high-Z output	tonz	0	25	0	25	0	30	ns
	Output hold from address change	tон	10	-	10	-	15	-	ns
Write	Write cycle time	twc	70	-	85	-	100	-	ns
	Chip select to end of write	tcw	60	-	70	-	80	-	ns
	Address set-up time	tAS	0	-	0	-	0	-	ns
	Address valid to end of write	tAW	60	-	70	-	80	-	ns
	Write pulse width	tWP	50	-	60	-	70	-	ns
	UB, LB valid to end of write	tBW	60	-	70	-	80	-	ns
	Write recovery time	tWR	0	-	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	30	0	30	0	35	ns
	Data to write time overlap	tDW	30	-	35	-	40	-	ns
	Data hold from write time	tDH	0	-	0	-	0	-	ns
	End write to output low-Z	tow	5		5	-	5	-	ns

DATA RETENTION CHARACTERISTICS

Item		Symbol Test Condition*		Min	Typ**	Max	Unit	
Vcc for data retention	VDR		CS≥Vcc-2.0V		2.0	-	3.6	V
		616V1000BL/L-L		L-Ver LL-Ver	-	-	30 15	μΑ
		616V1000BLE/LE-L 616V1000BLI/LI-L	Vcc=3.0V CS≥Vcc-0.2V	L-Ver LL-Ver	-	-	50 20	
Data retention current	IDR	616U1000BL/L-L		L-Ver LL-Ver	-	-	30 15	
		616U1000BLE/LE-L 616U1000BLI/LI-L		L-Ver LL-Ver	-	-	50 20	
Data retention set-up time	tSDF	?	See data retention		0	-	-	
Recovery time	tRDF	?	waveform		5	-	-	ms

^{* 1)} Commercial Product : Ta=0 to 70 $^{\circ}$ C, unless otherwise specified 2) Industrial Product : Ta=-25 to 85 $^{\circ}$ C, unless otherwise specified 3) Industrial Product : Ta=-40 to 85 $^{\circ}$ C, unless otherwise specified

DATA RETENTION TIMING DIAGRAM



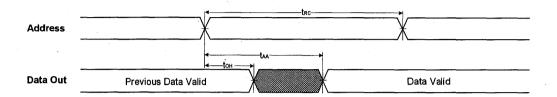
*3.0V for KM616V1000B family, 2.7V for KM616U1000B family



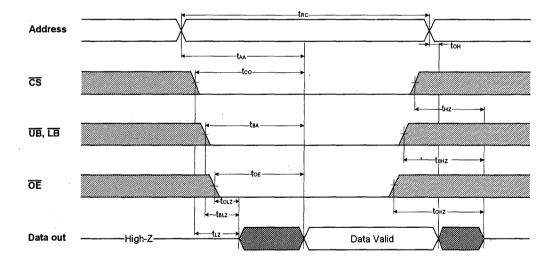
^{**} Ta=25℃

TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (1) (Address Controlled) ($\overline{CS}=\overline{OE}=Vil, \overline{WE}=Vih, \overline{UB}$ or and $\overline{LB}=Vil)$



TIMING WAVEFORM OF READ CYCLE(2) (WE=VIH)

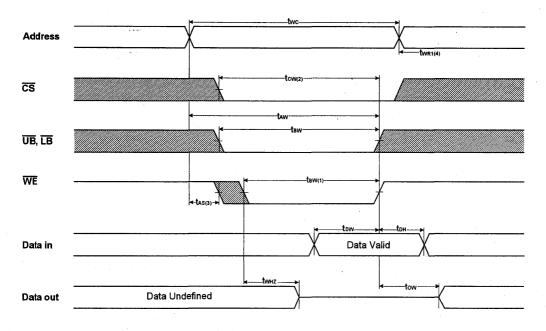


NOTES (READ CYCLE)

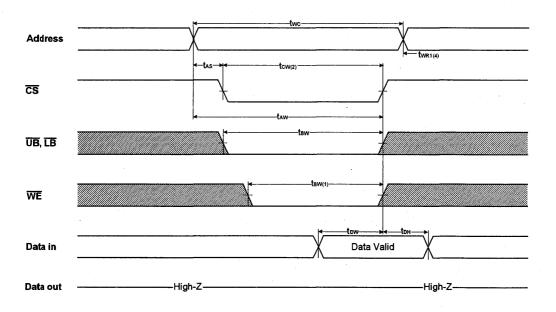
- 1. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
- 2. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device.



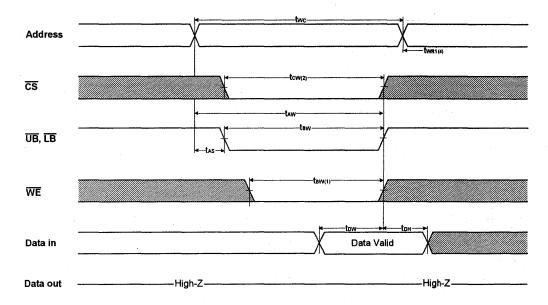
TIMING WAVEFORM OF WRITE CYCLE(1) (WE Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) (CS Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) (UB, LB Controlled)



NOTES (WRITE CYCLE)

- 1. A write occurs during the overlap (tWP) of low \overline{CS} and low \overline{WE} . A write begins when \overline{CS} goes low and \overline{WE} goes low with asserting \overline{UB} or \overline{LB} for single byte operation or simultaneously asserting \overline{UB} and \overline{LB} for double byte operation. A write ends at the earliest transition when \overline{CS} goes high and \overline{WE} goes high. The tWP is measured from the beginning of write to the end of write.
- 2. tCW is measured from the CS going low to end of write.
- 3. tAS is measured from the address valid to the beginning of write.
- 4. tWR is measured from the end or write to the address change. tWR applied in case a write ends as CS or WE going high.

FUNCTIONAL DESCRIPTION

CS	LB .	UB	WE	ŌĒ	Mode	I/O1~8	1/09-16	Current Mode
Н	Х	X	Х	Х	Not Select	High-Z	High-Z	isb,isb1
L	x	Х	Н	Н	Output	High-Z	High-Z	lcc
L	Н	H	_ X	Х	District	High-Z	High-Z	100
L	H L	HLL	н	L	Read	Dout High-Z Dout	High-Z Dout Dout	lcc
L	L H L	H L L	L	х	Write	Din High-Z Din	High Din Din	lcc

^{*}X means don tcare (Must be in low or high state)



256Kx8 bit Low Power and Low Voltage CMOS Static RAM **FEATURES**

• Process Technology: 0.4 µm CMOS

Organization: 256Kx8 Power Supply Voltage

KM68V2000A Family: 3.0V ~ 3.6V KM68U2000A Family: 2.7V ~ 3.3V . Low Data Retention Voltage: 2V(Min)

Three state output and TTL Compatible Package Type: JEDEC Standard

32-TSOP(I)-F/R, 32-sTSOP(I)-Forward/Reverse

GENERAL DESCRIPTION

The KM68V2000 and KM68U2000 family are fabricated by SAMSUNG's advanced CMOS process technology. The family can support various operating temperature ranges and have various package types for user flexibility of system design. The family also support low data retention voltage for battery backup operation with low data retention current.

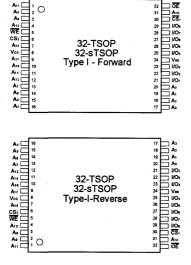
PRODUCT FAMILY

Product	Onesetten	Vcc	Parad		Power Dissipation		
List	Operating Temp.	Range	Speed (ns)	PKG Type	Standby (IsB1, Max)	Operating (Icc2)	
KM68V2000L-L	Commercial	3.0~3.6V	70/85		15 <i>µ</i> A	40mA	
KM68U2000L-L	(0~70℃)	2.7~3.3V	70*/100	32-TSOP I-R/F	15 <i>µ</i> A		
KM68V2000LI-L	Industria	3.0~3.6V	70/85	32-sTSOP I-R/F	30 <i>µ</i> A		
KM68U2000LI-L	(-40~85℃)	2.7~3.3V	85*/100		30 <i>µ</i> A		

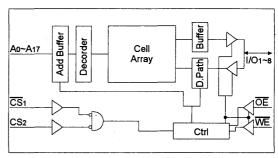
^{*} The parameter is measured with 30pF test load.

PIN DESCRIPTION

0



FUNCTIONAL BLOCK DIAGRAM



Name	Function	Name	Function
A0~A17	Address Inputs	Vcc	Power
WE	Write Enable	Vss	Ground
CS _{1,CS2}	Chip Select Input	I/O1~I/O8	Data Inputs/Outputs
Œ	Output Enable	N.C.	No Connection

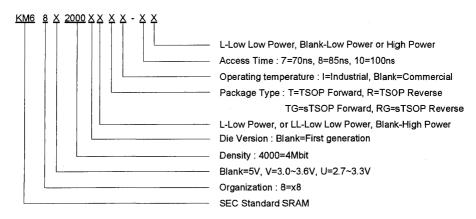


PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST

l .	Temp Product 70℃)	Industrial Temp Products (-40~85℃)				
Part Name	Function	Part Name	Function			
KM68V2000LT-7L	32-TSOP F, 70ns, 3.3V, LL	KM68V2000LTI-7L	32-TSOP F, 70ns, 3.3V, LL			
KM68V2000LT-8L	32-TSOP F, 85ns, 3.3V, LL	KM68V2000LIT-8L	32-TSOP F, 85ns, 3.3V, LL			
KM68V2000LR-7L	32-TSOP R, 70ns, 3.3V, LL	KM68V2000LRI-7L	32-TSOP R, 70ns, 3.3V, LL			
KM68V2000LR-8L	32-TSOP R, 85ns, 3.3V, LL	KM68V2000LRI-8L	32-TSOP R, 85ns, 3.3V, LL			
KM68U2000LT-7L	32-TSOP F, 70ns, 3.0V, LL	KM68U2000LTi-8L	32-TSOP F, 85ns, 3.0V, LL			
KM68U2000LT-10L	32-TSOP F, 100ns, 3.0V, LL	KM68U2000LTI-10L	32-TSOP F, 100ns, 3.0V, LL			
KM68U2000LR-7L	32-TSOP R, 70ns, 3.0V, LL	KM68U2000LRI-8L	32-TSOP R, 85ns, 3.0V, LL			
KM68U2000LR-10L	32-TSOP R, 100ns, 3.0V, LL	KM68U2000LRI-10L	32-TSOP R, 100ns, 3.0V, LL			
KM68V2000LTG-7L	32-sTSOP F, 70ns, 3.3V,LL	KM68V2000LTGI-7L	32-sTSOP F, 70ns, 3.3V,LL			
KM68V2000LTG-8L	32-sTSOP F, 85ns, 3.3V,LL	KM68V2000LTGI-8L	32-sTSOP F, 85ns, 3.3V,LL			
KM68V2000LRG-7L	32-sTSOP R, 70ns, 3.3V,LL	KM68V2000LRGI-7L	32-sTSOP R, 70ns, 3.3V,LL			
KM68V2000LRG-8L	32-sTSOP R, 85ns, 3.3V,LL	KM68V2000LRGI-8L	32-sTSOP R, 85ns, 3.3V,LL			
KM68U2000LTG-7L	32-sTSOP F, 70ns, 3.0V, LL	KM68U2000LTGI-8L	32-sTSOP F, 85ns, 3.0V, LL			
KM68U2000LTG-10L	32-sTSOP F, 100ns, 3.0V, LL	KM68U2000LTGI-10L	32-sTSOP F, 100ns, 3.0V, LL			
KM68U2000LRG-7L	32-sTSOP R, 70ns, 3.0V, LL	KM68U2000LRGI-8L	32-sTSOP R, 85ns, 3.0V, LL			
KM68U2000LRG-10L	32-sTSOP R, 100ns, 3.0V, LL	KM68U2000LRGI-10L	32-sTSOP R, 100ns, 3.0V, LL			

ORDERING INFORMATION





ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	Vin,Vout	-0.5 to Vcc+0.5	V	-
Voltage on Vcc supply relative to Vss	Vcc	-0.3 to 4.6	V	-
Power Dissipation	Po	0.7	w	-
Storage temperature	Тѕтс	-65 to 150	°	-
Operating Temperature	TA	0 to 70	Ĉ	KM68V2000L/L KM68U2000L/L
Operating Temperature		-40 to 85	C	KM68V2000LI/L KM68U2000LI/L
Soldering temperature and time	TSOLDER	260°C, 10sec (Lead Only)		-

^{*} Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*

ltem	Symbol	Product	Min	Typ**	Max	Unit
Supply voltage	Vcc	KM68V2000 Family KM68U2000 Family	3.0 2.7	3.3 3.0	3.6 3.3	V
Ground	Vss	All Family	0	0	0	V
Input high voltage	ViH	KM68V2000 Family KM68U2000 Family	2.2 2.2	-	Vcc+0.3 Vcc+0.3	V
Input low voltage	VIL	KM68V2000 Family	-0.3***	-	0.4	V
		KM68U2000 Family	-0.3***	-	0.4	V

^{* 1)} Commercial Product : TA=0 to 70 °C , unless otherwise specified

CAPACITANCE* (f=1MHz, TA=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	Cin	Vin=0V	-	8	pF
Input/Output capacitance	Cio	Vio=0V	•	10	pF

^{*} Capacitance is sampled not 100% tested



²⁾ Industrial Product : Ta=-40 to 85 °C, unless otherwise specified

^{**} Ta=25℃

^{***} ViL(min)=-3.0V for ≤ 30 ns pulse width

KM68V2000, KM68U2000 Family DC AND OPERATING CHARACTERISTICS

	Item	Symbol	Test Conditions*		Min	Typ**	Max	Unit
Input leaka	ge current	lu	Vin=Vss to Vcc		-1	-	1	μA
Output leal	age current	llo	CS1=VIH or CS2=VIL or WE=VIL, VIO=	=Vss to Vcc	-1	-	. 1	μA
Operating power supply current		Icc	CS1=VIL, CS2=VIH, IIO=0mA	Read	-	-	5	mA
		100	VIN=VIH or VIL	Write	-	-	15	,,,,
Average operatingcurrent		Icc1	Cycle time=1 µs 100%duty, lio=0mA	Read	-	-	5	mA
		1001	CS1≤0.2V, CS2≥Vcc-0.2V	Write			15	""
		ICC2	CS₁=VIL, CS₂=VIH, IIO=0mA, Min cycle, 100% duty			30	40	mΑ
Output low	voltage	Vol	IOL=2.1mA	-	-	-	0.4	٧
Output high	ı voltage	Voн	IOH=-1.0mA	,	2.2	-	-	٧
Standby Cu	urrent(TTL)	Isa	CS1=VIH, CS2=VIL		-	-	0.3	mA.
Standby Current (CMOS)	KM68V2000L-I KM68V2000LI-L	ISB1	CS1 ≥ Vcc-2.0V CS2 ≥ Vcc-2.0V or CS2 ≤ 0.2V Other inpts=0~Vcc	Low Low Power Low Low Power	-	0.5 0.5	15 30	μA μA
. ,	KM68U2000L-L KM68U2000LI-L			Low Low Power Low Low Power	-	0.5 0.5	15 30	μA μA

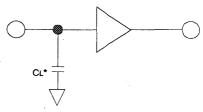
^{* 1)} Commercial Product : Ta=0 to 70°C , Vcc=3.3±0.3V (68V2000 Family) , Vcc=3.0±0.3V (68U2000 Family)

A.C CHARACTERISTICS

TEST CONDITIONS (1.Test Load and Test Input/Output Reference)*

Item	Value	Remark
Input pulse level	0.4 to 2.2V	-
Input rising and falingl time	5ns	-
input and output reference voltage	1.5V	-
Output load (See right)	CL=100pF+1TTL **CL=30pF+1TTL	-

^{*} See DC Operating conditions



^{*} Including scope and jig capacitance



²⁾ Industrial Product : Ta=-40 to 85℃, Vcc=3.3±0.3V (68V2000I Family), Vcc=3.0±0.3V (68U2000I Family)

^{**} TA=25°C

TEST CONDITIONS (2. Temperature and Vcc Conditions)

Product Family	Temperature	Power Supply(Vcc)	Speed Bin	Comments
KM68V2000L-L	0~70℃	$3.3V \pm 0.3$	70/85ns	Commercial
KM68V2000LI-L	-40~85℃	3.3V ± 0.3	70/85ns	Industrial
KM68U2000L-L	0~70℃	3.0V ± 0.3	70*/100ns	Commercial
KM68U2000LI-L	-40~85℃	$3.0V \pm 0.3$	85*/100ns	Industrial

^{*} The parameters are measured with 30pF test load.

PARAMETER LIST FOR EACH SPEED BIN

					Spee	d Bins			
	Parameter List	Symbol	70)ns	8	ins	10	0ns	Units
			Min	Max	Min	Max	Min	Max	
Read	Read cycle time	tRC	70	-	85	-	100	-	ns
	Address access time	tAA	-	70	-	85	-	100	ns
	Chip select to output	tco	-	70	-	`85	-	100	ns
	Output enable to valid output	toE		35	-	40	-	50	ns
	Chip select to low-Z output	tLZ	10	-	10	-	10	-	ns
	Output enable to low-Z output	toLZ	5	-	5	-	5	-	ns
	Chip disable to high-Z output	tHZ	0	25	0	25	0	30	ns
	Output disable to high-Z output	tonz	0	25	0	25	0	30	ns
	Output hold from address change	ton	10	-	15	-	15	-	ns
	Write cycle time	twc	70	-	85	-	100	-	ns
	Chip select to end of write	tcw	60	-	70	-	80	-	ns
Write	Address set-up time	tAS	0	-	0	-	0	-	ns
	Address valid to end of write	tAW	60	-	70	-	80	-	ns
	Write pulse width	tWP	55	-	60	-	70	-	ns
	Write recovery time	tWR	0	-	0	-	0	-	ns
	Write to output high-Z	twnz	0	25	0	30	0	30	ns
	Data to write time overlap	tDW	30	-	35	-	40	-	ns
	Data hold from write time	tDH	0	-	0	-	0	-	ns
	End write to output low-Z	tow	5		5	-	5	-	ns



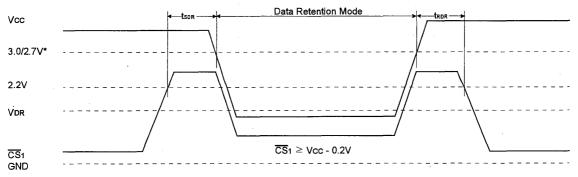
DATA RETENTION CHARACTERISTICS

Item		Symbol	Test Condition*		Min	Typ**	Max	Unit
Vcc for data retention	VDR		CS1***≥ Vcc-2.0\	2.0	-	3.6	٧	
Data retention current	lon	KM68V2000L-L KM68V2000LI-L	Vcc=3.0V	LL-Ver LL-Ver	-	0.5 0.5	15 30	μA
	IDR	KM68U2000L-L KM68U2000LI-L	CS₁≥Vcc-0.2V	LL-Ver LL-Ver	-	0.5 0.5	15 30	
Data retention set-up time	tsdf	8	See data retention	n	0	-	-	me
Recovery time tRDR		?	waveform		5	-	-	ms

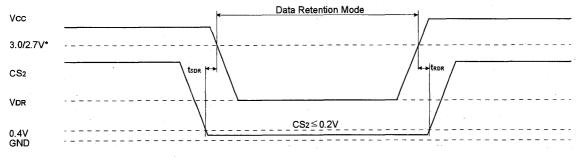
^{* 1)} Commercial Product : Ta=0 to 70°C, unless otherwise specified 2) Industrial Product : Ta=-40 to 85°C, unless otherwise specified ** Ta=25°C

DATA RETENTION WAVE FORM

1) CS1 controlled







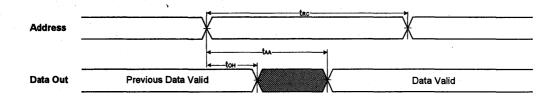
*3.0V for KM68V2000 family, 2.7V KM68U2000 family



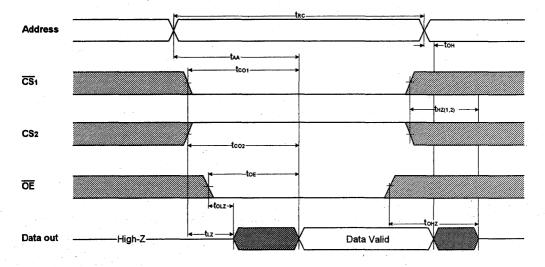
^{***} $\overline{CS}_1 \ge Vcc-0.2V$, $CS_2 \ge Vcc-0.2V(\overline{CS}_1)$ controlled) or $CS_2 \le 0.2V(CS_2)$ controlled)

TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (1) (Address Controlled) (CS=OE=VIL, WE=VIH)



TIMING WAVEFORM OF READ CYCLE(2) (WE=VIH)

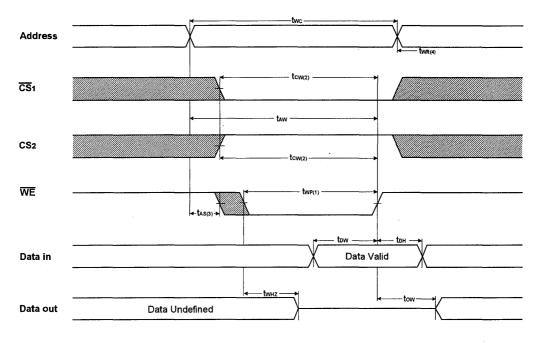


NOTES (READ CYCLE)

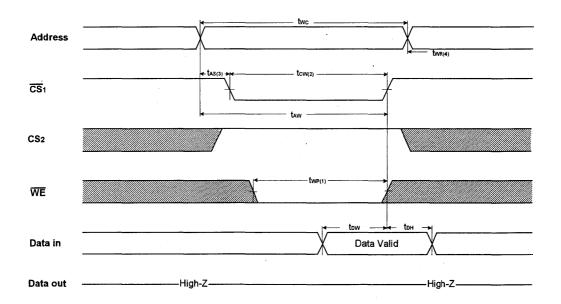
- 1. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
- 2. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device interconnection.



TIMING WAVEFORM OF WRITE CYCLE(1) (WE Controlled)

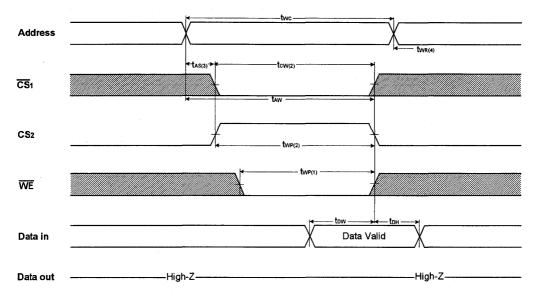


TIMING WAVEFORM OF WRITE CYCLE(2) (CS1 Controlled)





TIMING WAVEFORM OF WRITE CYCLE(3) (CS1 Controlled)



NOTES (WRITE CYCLE)

- 1. A write occurs during the overlap of a low \overline{CS}_1 , a high CS2 and a low \overline{WE} . A write begins at the latest transition among \overline{CS}_1 goes low, CS2 going high and \overline{WE} going low: A write end at the earliest transition among \overline{CS}_1 going high, CS2 going low and \overline{WE} going high, tWP is measured from the begining of write to the end of write.
- 2. TCW is measured from the CS1 going low or CS2 going high to the end of write.
- 3. tAS is measured from the address valid to the beginning of write.
- 4. tWR is measured from the end of write to the address change. tWR(1) applied in case a write ends as CS1 or WE going high tWR(2) applied in case a write ends as CS2 going to low.

FUNCTIONAL DESCRIPTION

CS ₁	CS2	WE	ŌĒ	Mode	1/0	Current Mode
Н	X	Х	X	Power Down	High-Z	İSB1
X	L	Х	X	Power Down_	High-Z	ISB, ISB1
L	H.	Н	Н	Output Disable	High-Z	lcc
L	Н	Н	L	Read	Dout	lcc
L	Н	L	X	Write	Din	lcc

^{*} X means don't care (Must be in high or low states)



512Kx8 bit Low Power and Low Voltage CMOS Static RAM **FEATURES**

• Process Technology: 0.4 µm CMOS

 Organization: 512Kx8 · Power Supply Voltage

KM68V4000A Family : 3.3 \pm 0.3V KM68U4000A Family : 3.0 \pm 0.3V

· Low Data Retention Voltage: 2V(Min) · Three state output and TTL Compatible

· Package Type: JEDEC Standard

32-SOP, 32-TSOP(II)-Forward/Reverse

GENERAL DESCRIPTION

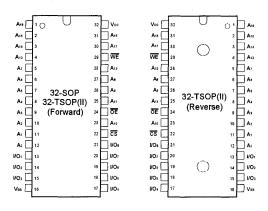
The KM68V4000A and KM68U4000A family are fabricated by SAMSUNG's advanced CMOS process technology. The family can support various operating temperature ranges and have various package types for user flexibility of system design. The family also support low data retention voltage for battery backup operation with low data retention current.

PRODUCT FAMILY

Product	0			Power Di		
List	Operating Temp.	Vcc Range	Speed (ns)	Standby (isB1, Max)	Operating (Icc2)	PKG Type
KM68V4000AL KM68V4000AL-L	Commercial (0~70°C)	3.0~3.6V	70*/85*/100	50/15 <i>μ</i> Α		
KM68V4000ALI LM68V4000ALI-L	Industrial (-40~85℃)	3.0~3.6V	70*/85*/100	70*/85*/100 50/20 µA		32-SOP
KM68U4000AL KM68U4000ALI-L	Commercial (0~70°C)	2.7~3.3V	70*/85*/100	30/10 µÅ	50mA	32-TSOP(II)-R/F
KM68U4000ALI KM68U4000ALI-L	Industria (-40∼85℃)	2.7~3.3V	70*/85*/100	30/15 <i>µ</i> Å		

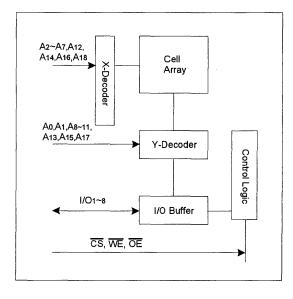
^{*} The parameter is measured with 30pF test load.

PIN DESCRIPTION



Name	Function	Name	Function
A0~A18	Address Inputs	Vcc	Power
WE	Write Enable Input	Vss	Ground
<u>cs</u>	Chip Select Input	I/O1~I/O8	Data Inputs/Outputs
ŌĒ	Output Enable Input		

FUNCTIONAL BLOCK DIAGRAM



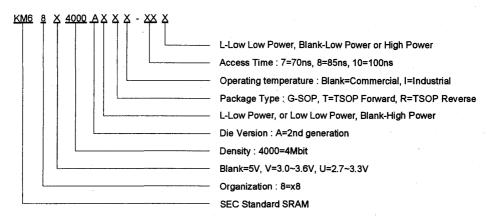


PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST

	Temp Product -70 ℃)	Industrial Temp Products (-40~85℃)				
Part Name	Function	Part Name	Function			
KM68V4000ALT-7	32-SOP, 70ns, 3.3V,L	KM68V4000ALG-7	32-SOP, 70ns, 3.3V,L			
KM68V4000ALT-7L	32-SOP, 70ns, 3.3V,LL	KM68V4000ALG-7L '	32-SOP, 70ns, 3.3V,LL			
KM68V4000ALT-8	32-SOP, 85ns, 3.3V,L	KM68V4000ALG-8	32-SOP, 85ns, 3.3V,L			
KM68V4000ALT-8L	32-SOP, 85ns, 3.3V,LL	KM68V4000ALG-8L	32-SOP, 85ns, 3.3V,LL			
KM68V4000ALT-10	32-SOP, 100ns, 3.3V,L	KM68V4000ALG-10	32-SOP, 100ns, 3.3V,L			
KM68V4000ALT-10L	32-SOP, 100ns, 3.3V,LL	KM68V4000ALG-10L	32-SOP, 100ns, 3.3V,LL			
KM68V4000ALT-7L	32-TSOP(II)F, 70ns, 3.3V,LL	KM68V4000ALT-7L	32-TSOP(II)F, 70ns, 3.3V,LL			
KM68V4000ALT-8L	32-TSOP(II)F, 85ns, 3.3V,LL	KM68V4000ALT-8L	32-TSOP(II)F, 85ns, 3.3V,LL			
KM68V4000ALT-10L	32-TSOP(II)F, 100ns, 3.3V,LL	KM68V4000ALT-10L	32-TSOP(II)F, 100ns, 3.3V,LL			
KM68V4000ALR-7L	32-TSOP(II)R, 70ns, 3.3V,LL	KM68V4000ALR-7L	32-TSOP(II)R, 70ns, 3.3V,LL			
KM68V4000ALR-8L	32-TSOP(II)R, 85ns, 3.3V,LL	KM68V4000ALR-8L	32-TSOP(II)R, 85ns, 3.3V,LL			
KM68V4000ALR-10L	32-TSOP(II)R, 100ns, 3.3V,LL	KM68V4000ALR-10L	32-TSOP(II)R, 100ns, 3.3V,LL			
KM68U4000ALG-7	32-SOP, 70ns, 3.0V,L	KM68U4000ALGI-7	32-SOP, 70ns, 3.0V,L			
KM68U4000ALG-7L	32-SOP, 70ns, 3.0V,LL	KM68U4000ALGI-7L	32-SOP, 70ns, 3.0V,LL			
KM68U4000ALG-8	32-SOP, 85ns, 3.0V,L	KM68U4000ALGI-8	32-SOP, 85ns, 3.0V,L			
KM68U4000ALG-8L	32-SOP, 85ns, 3.0V,LL	KM68U4000ALGI-8L	32-SOP, 85ns, 3.0V,LL			
KM68U4000ALG-10	32-SOP, 100ns, 3.0V,L	KM68U4000ALGI-10	32-SOP, 100ns, 3.0V,L			
KM68U4000ALG-10L	32-SOP, 100ns, 3.0V,LL	KM68U4000ALGI-10L	32-SOP, 100ns, 3.0V,LL			
KM68U4000ALT-7L	32-TSOP(II)F, 70ns, 3.0V,LL	KM68U4000ALTI-7L	32-TSOP(II)F, 70ns, 3.0V,LL			
KM68U4000ALT-8L	32-TSOP(II)F, 85ns, 3.0V,LL	KM68U4000ALTI-8L	32-TSOP(II)F, 85ns, 3.0V,LL			
KM68U4000ALT-10L	32-TSOP(II)F, 100ns, 3.0V,LL	KM68U4000ALTI-10L	32-TSOP(II)F, 100ns, 3.0V,LL			
KM68U4000ALR-7L	32-TSOP(II)R, 70ns, 3.0V,LL	KM68U4000ALRI-7L	32-TSOP(II)R, 70ns, 3.0V,LL			
KM68U4000ALR-8L	32-TSOP(II)R, 85ns, 3.0V,LL	KM68U4000ALRI-8L	32-TSOP(II)R, 85ns, 3.0V,LL			
KM68U4000ALR-10L	32-TSOP(II)R, 100ns, 3.0V,LL	KM68U4000ALRI-10L	32-TSOP(II)R, 100ns, 3.0V,LL			
		· · · · · · · · · · · · · · · · · · ·				

ORDERING INFORMATION





KM68V4000A, KM68U4000A Family



CMOS SRAM

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	VIN,VOUT	-0.5 to Vcc+0.5	V	-
Voltage on Vcc supply relative to Vss	Vcc	-0.3 to 4.6	V	-
Power Dissipation	Po	0.7	w	-
Storage temperature	Тѕтс	-65 to 150	°	-
		0 to 70	င	KM68V4000AL/L-L KM68U4000AL/L-L
Operating Temperature		-40 to 85	ొ	KM68V4000ALI/LI-L KM68U4000ALI/LI-L
Soldering temperature and time	TSOLDER	260℃, 10sec (Lead Only)	-	-

^{*} Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*

Item	Symbol	Product	Min	Typ**	Max	Unit
Supply voltage	Vcc	KM68V4000A Family KM68U4000A Family	3.0 2.7	3.3 3.0	3.6 3.3	V V
Ground	Vss	All Family	0	0	0	V
Input high voltage	VIH	KM68V4000A Family KM68U4000A Family	2.2 2.2	-	Vcc+0.3 Vcc+0.3	V V
Input low voltage	VIL	KM68V4000A Family KM68U4000A Family	-0.3*** -0.3***		0.4 0.4	V

^{* 1)} Commercial Product : Ta=0 to 70°C, unless otherwise specified

CAPACITANCE* (f=1MHz, Ta=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	Cin	Vin=0V	-	8	pF
Input/Output capacitance	Сю	Vio=0V	-	10	pF

^{*} Capacitance is sampled, not 100% tested.



²⁾ Industrial Product : Ta=-40 to 85 °C, unless otherwise specified

^{**} TA=25°C

^{***} VIL(min)=-3.0V for \(\le \) 30ns pulse width

DC AND OPERATING CHARACTERISTICS

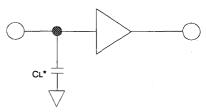
	Item	Symbol	Test Conditions*			Typ**	Max	Unit
input leak	age current	lu	VIN=Vss to Vcc		-1	-	1	μA
Output lea	kage current	lLO	CS=ViH or ViL, Vio=Vss to Vcc		-1	-	1	μA
Operating	power supply current	Icc	CS=Vil, ViN=ViH or Vil, Lio=0mA	Read	-	-	10	mA
Operating	power supply current	100	OS-VIE, VIN-VIE OF VIE, EIG-OFFA	Write	-	-	20	'''^
		lcc1	Cycle time=1 µs 100% duty, Iio=0mA	Read	-	-	10	mA
Average operatingcurrent		1001	<u>CS</u> ≤0.2V, V _I L≤0.2V, V _I H≥V _{CC} -0.2V	Write	-	-	20	'''^
		ICC2	Min cycle, 100% duty CS=VIL, LIO=0mA,VIN=VIH or VIL		-	-	50	mA
Output lov	v voltage	Vol	IoL=2.1mA		-	-	0.4	V
Output hig	h voltage	Vон	ЮH=-1.0mA			-	-	V
Standby C	Current(TTL)	ISB	CS =ViH			-	0.5	mA
	KM68V4000AL KM68V4000AL-L			Low Power Low Low Power	-	-	50 15	μA μA
Standby	Standby KM68V4000ALI KM68V4000ALI-L		CS ≥Vcc-0.2V, Others=0~Vcc	Low Power Low Low Power	-	-	50 20	μA μA
Current (CMOS) KM68U4000AL KM68U4000AL-L		ISB1	032 vcc-0.2v, Others-0-vcc	Low Power Low Low Power	-	-	30 10	μA μA
	KM68U4000ALI KM68U4000ALI-L		·	Low Power Low Low Power	-	<u>-</u>	30 15	μA μA

^{* 1)} Commercial Product : Ta=0 to 70% , Vcc=3.3 \pm 0.3V (68V4000A Family), Vcc=3.0 \pm 0.3V (68U4000A Family)

A.C CHARACTERISTICS

TEST CONDITIONS (1.Test Load and Test Input/Output Reference)*

Item	Value	Remark
Input pulse level	0.4 to 2.2V	-
Input rising and falling time	5ns	-
input and output reference voltage	1.5V	-
Output load (See right)	CL=100pF+1TTL **CL=30pF+1TTL	-



* Including scope and jig capacitance



²⁾ Industrial Product : Ta=-40 to 85 °C, Vcc=3.3 ± 0.3V (68V4000Al Family), Vcc=3.0 ± 0.3V (68U4000Al Family)
** Ta=25 °C

^{*} See DC Operating conditions
** KM68V4000A-7/KM68V4000A-8 Family, KM68U4000A-7/KM68U4000A-8 Family

TEST CONDITIONS (2. Temperature and Vcc Conditions)

Product Family	Temperature	Power Supply(Vcc)	Speed Bin	Comments
KM68V4000AL/L-L	0~70℃	3.3V ± 0.3	70*/85*/100ns	Commercial
KM68V4000ALI/LI-L	-40~85℃	3.3V ± 0.3	70*/85*/100ns	Industrial
KM68U4000AL/L-L	0~70℃	2.7V ± 0.3	70*/85*/100ns	Commercial
KM68U4000AL/LII-L	-40~85℃	2.7V ± 0.3	70*/85*/100ns	Industrial

^{*} All the parameters are measured with 30pF test load

PARAMETER LIST FOR EACH SPEED BIN

					Spec	ed Bins			
	Parameter List	Symbol	*7	Ons	*8	5ns	10	Ons	Units
			Min	Max	Min	Max	Min	Max]
Read	Read cycle time	tRC	70	-	85	-	100	-	ns
	Address access time	tAA	-	70	-	85	-	100	ns
	Chip select to output	tco	-	70	-	85	-	100	ns
	Output enable to valid output	tOE	-	35	-	40	-	50	ns
	Chip select to low-Z output	tLZ	10	-	10	-	10	-	ns
	Output enable to low-Z output	toLZ	5	-	5	-	5	-	ns
	Chip disable to high-Z output	tHZ	0	25	0	25	0	30	ns
	Output disable to high-Z output	tonz	0	25	0	25	0	30	ns
	Output hold from address change	tон	10	-	10	-	15	-	ns
	Write cycle time	twc	70	-	85	-	100	-	ns
	Chip select to end of write	tcw	60	-	70	-	80	-	ns
Write	Address set-up time	tAS	0	-	0	-	0	-	ns
	Address valid to end of write	tAW	60	-	70	-	80	-	ns
	Write pulse width	twp	55	-	55	-	70	-	ns
	Write recovery time	twr	0	-	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	25	0	25	0	30	ns
	Data to write time overlap	tDW	30	-	35	-	40	-	ns
	Data hold from write time	tDH	0	-	0	-	0	-	ns
	End write to output low-Z	tow	5	-	5	-	5	-	ns

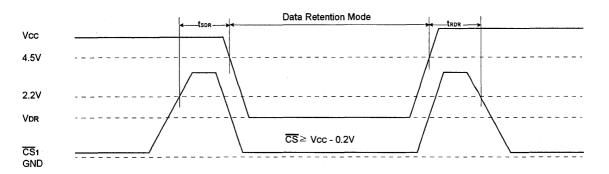
^{*} The parameter is measured with 30pF test load.

DATA RETENTION CHARACTERISTICS

Item	Symbol		Test Cond	Test Condition*		Typ**	Max	Unit
Vcc for data retention	VDR		CS ≥Vcc-2.0V		2.0	-	3.6	V
Data retention current	IDR	KM68V4000AL/L-L	Vcc=3.0V CS≥Vcc-0.2V	L-Ver LL-Ver	-	1 0.5	30 15	μA
		KM68V4000ALI/LI-L		L-Ver LL-Ver	-	-	30 20	
		KM68U4000AL/L-L		L-Ver LL-Ver	-	1 0.5	30 10	
		KM68U4000ALI/LI-L		L-Ver LL-Ver	-	-	30 15	
Data retention set-up time	tsdr	₹	See data retentio	n	0	-	-	me
Recovery time	tRDF	₹	waveform		5	-	-	ms

^{* 1)} Commercial Product : Ta=0 to 70 $^{\circ}$, unless otherwise specified 2) Industrial Product : Ta=-40 to 85 $^{\circ}$, unless otherwise specified ** Ta=25 $^{\circ}$

DATA RETENTION TIMING DIAGRAM



FUNCTIONAL DESCRIPTION

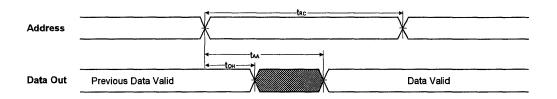
<u>cs</u>	WE	ŌĒ	Mode	1/0	Current Mode
н	х	Х	Power Down	High-Z	ISB, ISB1
L	Н	Н	Output Disable	High-Z	lcc
L	Н	L	Read	Dout	lcc
L	L	Х	Write	Din	lcc

^{*} X means don't care (Must be in low or high state)

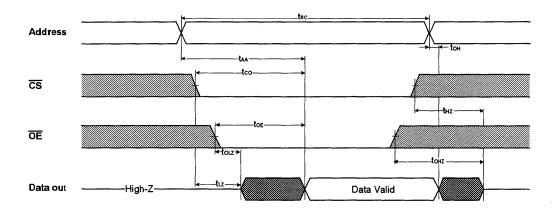


TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled) ($\overline{\text{CS}}=\overline{\text{OE}}=\text{VIL}$, $\overline{\text{WE}}=\text{VIH}$)



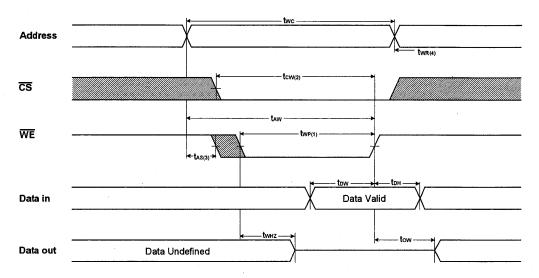
TIMING WAVEFORM OF READ CYCLE(2) (WE=VIH)



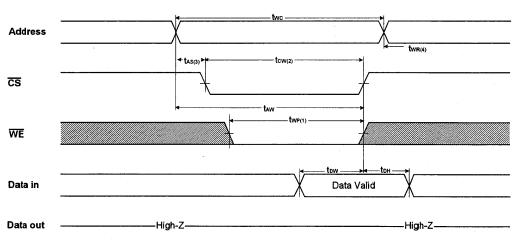
NOTES (READ CYCLE)

- 1. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
- 2. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device.

TIMING WAVEFORM OF WRITE CYCLE(1) (WE Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) (CS Controlled)



NOTES (WRITE CYCLE)

- 1. A write occurs during the overlap(tWP) of a low $\overline{\text{CS}}$ and low $\overline{\text{WE}}$. A write begins at the latest transition among $\overline{\text{CS}}$ goes low and $\overline{\text{WE}}$ going low : A write end at the earliest transition among $\overline{\text{CS}}$ going high and $\overline{\text{WE}}$ going high, tWP is measured from the beginning of write to the end of write.
- 2. tCW is measured from the $\overline{\text{CS}}$ going low to end of write.
- 3. $\overline{\text{tAS}}$ is measured from the address valid to the beginning of write.
- 4. tWR is measured from the end of write to the address change. tWR applied in case a write ends as $\overline{\text{CS}}$ or $\overline{\text{WE}}$ going high.



512Kx8 bit Low Power and Low Voltage CMOS Static RAM

FEATURES

• Process Technology: 0.4 µm CMOS

Organization : 512Kx8Power Supply Voltage

KM68V4000B Family : 3.3 ± 0.3 V KM68U4000B Family : 3.0 ± 0.3 V

- Low Data Retention Voltage : 2V(Min)
- Three state output and TTL Compatible
 Design of the state of 22 COS
- Package Type : JEDEC Standard 32-SOP, 32-TSOP(II)-Forward/Reverse

The KM68V4000B and KM68U4000B family are fabricated by SAMSUNG's advanced CMOS process technology. The family can support various operating temperature ranges and have various package types for user flexibility of system design. The family also support low data retention voltage for battery back-

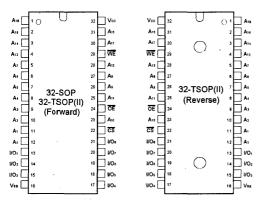
up operation with low data retention current.

GENERAL DESCRIPTION

PRODUCT FAMILY

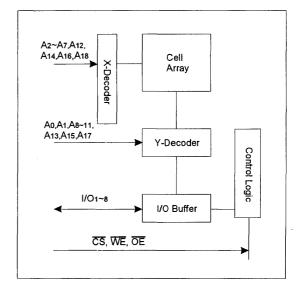
Product	0		63	Power Di	ssipation		
List	Operating Temp.	Vcc Range	Speed (ns)	Standby (IsB1, Max)	Operating (Icc2)	PKG Type	
KM68V4000BL KM68V4000BL-L	Commercial (0~70℃)	3.0~3.6V	70*/85*/100	50/15 <i>μ</i> Α			
KM68V4000BLI LM68V4000BLI-L	Industrial (-40~85 ℃)	3.0~3.6V	85*/100	50/20μA	50mA	32-SOP	
KM68U4000BL KM68U4000BLI-L	Commercial (0~70°C)	2.7~3.3V	70*/85*/100	30/15 <i>µ</i> A	301114	32-TSOP(II)-R/F	
KM68U4000BLI-L KM68U4000BLI-L	Industria (-40~85℃)	2.7~3.3V	85*/100	30/20 µA			

PIN DESCRIPTION



Name	Function	Name	Function
A0~A18	Address Inputs	Vcc	Power
WE	Write Enable Input	Vss	Ground
cs	Chip Select Input	I/O1~I/O8	Data Inputs/Outputs
ŌĒ	Output Enable Input		

FUNCTIONAL BLOCK DIAGRAM



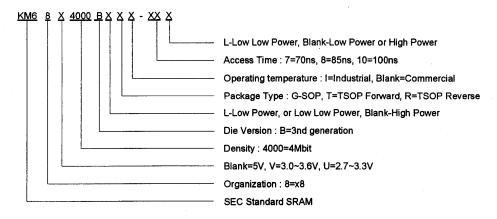


PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST

	Temp Product 70°C)		emp Products I~85℃)
Part Name	Function	Part Name	Function
KM68V4000BLT-7	32-SOP, 70ns, 3.3V,L	KM68V4000BLGI-8	32-SOP, 85ns, 3.3V,L
KM68V4000BLT-7L	32-SOP, 70ns, 3.3V,LL	KM68V4000BLGI-8L	32-SOP, 85ns, 3.3V,LL
KM68V4000BLT-8	32-SOP, 85ns, 3.3V,L	KM68V4000BLGI-10	32-SOP, 100ns, 3.3V,L
KM68V4000BLT-8L	32-SOP, 85ns, 3.3V,LL	KM68V4000BLGI-10L	32-SOP, 100ns, 3.3V,LL
KM68V4000BLT-10	32-SOP, 100ns, 3.3V,L		
KM68V4000BLT-10L	32-SOP, 100ns, 3.3V,LL	KM68V4000BLTI-8	32-TSOP(II)F, 85ns, 3.3V,LL
		KM68V4000BLTI-8L	32-TSOP(II)F, 100ns, 3.3V,LL
KM68V4000BLT-7L	32-TSOP(II)F, 70ns, 3.3V,LL	KM68V4000BLRI-10	32-TSOP(II)R, 85ns, 3.3V,LL
KM68V4000BLT-8L	32-TSOP(II)F, 85ns, 3.3V,LL	KM68V4000BLRI-10L	32-TSOP(II)R, 100ns, 3.3V,LL
KM68V4000BLT-10L	32-TSOP(II)F, 100ns, 3.3V,LL		
KM68V4000BLR-7L	32-TSOP(II)R, 70ns, 3.3V,LL	KM68U4000BLGI-8	32-SOP, 85ns, 3.0V,L
KM68V4000BLR-8L	32-TSOP(II)R, 85ns, 3.3V,LL	KM68U4000BLGI-8L	32-SOP, 85ns, 3.0V,LL
KM68V4000BLR-10L	32-TSOP(II)R, 100ns, 3.3V,LL	KM68U4000BLGI-10	32-SOP, 100ns, 3.0V,L
		KM68U4000BLGI-10L	32-SOP, 100ns, 3.0V,LL
KM68U4000BLG-7	32-SOP, 70ns, 3.0V,L		
KM68U4000BLG-7L	32-SOP, 70ns, 3.0V,LL	KM68U4000BLTI-8	32-TSOP(II)F, 85ns, 3.0V,LL
KM68U4000BLG-8	32-SOP, 85ns, 3.0V,L	KM68U4000BLTI-8L	32-TSOP(II)F, 100ns, 3.0V,LL
KM68U4000BLG-8L	32-SOP, 85ns, 3.0V,LL	KM68U4000BLRI-10	32-TSOP(II)R, 85ns, 3.0V,LL
KM68U4000BLG-10	32-SOP, 100ns, 3.0V,L	KM68U4000BLRI-10L	32-TSOP(II)R, 100ns, 3.0V,LL
KM68U4000BLG-10L	32-SOP, 100ns, 3.0V,LL		
KM68U4000BLT-7L	32-TSOP(II)F, 70ns, 3.0V,LL		
KM68U4000BLT-8L	32-TSOP(II)F, 85ns, 3.0V,LL		
KM68U4000BLT-10L	32-TSOP(II)F, 100ns, 3.0V,LL		
KM68U4000BLR-7L	32-TSOP(II)R, 70ns, 3.0V,LL	•	
KM68U4000BLR-8L	32-TSOP(II)R, 85ns, 3.0V,LL	•	
KM68U4000BLR-10L	32-TSOP(II)R, 100ns, 3.0V,LL		

ORDERING INFORMATION





KM68V4000B, KM68U4000B Family

ABSOLUTE MAXIMUM RATINGS*

ltem .	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	VIN, VOUT	-0.5 to Vcc+0.5	V	<u>.</u>
Voltage on Vcc supply relative to Vss	Vcc	-0.3 to 4.6	V	•
Power Dissipation	Pb	0.7	w	-
Storage temperature	Тѕтс	-65 to 150	°	-
Operating Temperature	TA	0 to 70	°	KM68V4000BL/L-L KM68U4000BL/L-L
Operating Temperature	14	-40 to 85	°C	KM68V4000BLI/LI-L KM68U4000BLI/LI-L
Soldering temperature and time	TSOLDER	260°C, 10sec (Lead Only)	-	-

^{*} Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*

Item	Symbol	Product	Min	Typ**	Max	Unit
Supply voltage	Vcc	KM68V4000B Family KM68U4000B Family	3.0 2.7	3.3 3.0	3.6 3.3	V V
Ground	Vss	All Family	0	0	0	٧
Input high voltage	ViH	KM68V4000B Family KM68U4000B Family	2.2 2.2	-	Vcc+0.3 Vcc+0.3	V V
Input low voltage	VIL	KM68V4000B Family KM68U4000B Family	-0.3*** -0.3***	-	0.4 0.4	V V

^{* 1)} Commercial Product : Ta=0 to 70℃, unless otherwise specified 2) Industrial Product : Ta=-40 to 85℃, unless otherwise specified

CAPACITANCE* (f=1MHz, Ta=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	Cin	Vin=0V	-	. 8	pF
Input/Output capacitance	Cio	Vio=0V	-	10	pF

^{*} Capacitance is sampled not 100% tested



^{**} TA=25°C

^{***} $V_{iL}(min)$ =-3.0V for \leq 30ns pulse width

DC AND OPERATING CHARACTERISTICS

	Item	Symbol	Test Conditions	s*	Min	Typ**	Max	Unit
Input leak	age current	lц	VIN=Vss to Vcc		-1	-	1	μA
Output lea	kage current	llo	CS=VIH or VIL, Vio=Vss to Vcc		-1	-	1	μA
Operating power supply current		Icc	CS=VIL, VIN=VIH or VIL,	Read	-	-	10	
		1.100	lio=0mA	Write	-	. .	20	mA
		lcc1	Cycle time=1 µs 100%duty	Read	2.2 -	10	mA	
Average o	perating current	ICCI	<u>CS</u> ≤0.2V, VIL≤0.2V,	Write		-	20	
		ICC2	Min cycle, 100%duty, lio=0mA, CS	S=VIL, VIN=VIH or VIL	-	-	50	mA
Output low	voltage	Vol	IoL=2.1mA	IoL=2.1mA		-	0.4	٧
Output hig	h voltage	Voн	Юн=-1.0mA		2.2	-	-	V
Standby C	urrent(TTL)	IsB	CS=ViH		-	-	0.5	mA
	KM68V4000BL KM68V4000BL-L			Low Power Low Low Power	-	-	50 15	μA A
Standby Current	KM68V4000BLI KM68V4000BLI-L	ISB1	CS ≥Vcc-0.2V. Others=0~Vcc	Low Power Low Low Power	-	-	50 20	μA Aμ
(CMOS)			05 - vcc-0.2v, Ollers-0-vcc	Low Power Low Low Power	-	-	30 15	μΑ μΑ
	KM68U4000BLI KM68U4000BLI-L			Low Power Low Low Power	-	-	30 20	μΑ Α μ

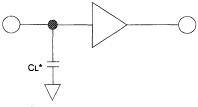
^{* 1)} Commercial Product : Ta=0 to 70 $^{\circ}$ C, Vcc=3.3 $^{\pm}$ 0.3V (68V4000B Family), Vcc=3.0 $^{\pm}$ 0.3V (68U4000B Family)

A.C CHARACTERISTICS

TEST CONDITIONS (1. Test Load and Test Input/Output Reference)*

Item	Value	Remark
Input pulse level	0.4 to 2.2V	-
Input rising and falling time	5ns	-
input and output reference voltage	1.5V	-
Output load (See right)	CL=100pF+1TTL **CL=30pF+1TT	**

^{*} See DC Operating conditions



* Including scope and jig capacitance



²⁾ Industrial Product : Ta=-40 to 85°C, Vcc=3.3 ±0.3V (68V4000BI Family), Vcc=3.0 ±0.3V (68U4000BI Family) ** Ta=25°C

TEST CONDITIONS (2. Temperature and Vcc Conditions)

Product Family	Temperature	Power Supply(Vcc)	Speed Bin	Comments
KM68V4000BL/L-L	0~70℃	$3.3V \pm 0.3$	70*/85*/100ns	Commercial
KM68V4000BLI/LI-L	-40~85℃	$3.3V \pm 0.3$	85*/100ns	Industrial
KM68U4000BL/L-L	0~70℃	3.0V ± 0.3	70*/85*/100ns	Commercial
KM68U4000BLI/LI-L	-40~85℃	3.0V ± 0.3	85*/100ns	Industrial

^{*} All the parameters are measured with 30pF test load

PARAMETER LIST FOR EACH SPEED BIN

					Spec	d Bins			
	Parameter List	Symbol	*70ns		*8	5ns	10	0ns	Units
			Min	Max	Min	Max	Min	Max	
Read	Read cycle time	tRC	70	-	85	-	100	-	ns
	Address access time	tAA	-	70	-	85	-	100	ns
	Chip select to output	tco	-	70	-	85	-	100	ns
	Output enable to valid output	tOE	-	35	-	40	-	50	ns
	Chip select to low-Z output	tLZ	10	-	10		10	-	ns
	Output enable to low-Z output	tOLZ	5	-	5	-	5	-	ns
	Chip disable to high-Z output	tHZ	0	25	0	25	0	30	ns
	Output disable to high-Z output	tonz	0	25	0	25	0	30	ns
	Output hold from address change	ton	10	-	10	-	15	-	ns
Write	Write cycle time	twc	70	-	85	-	100	-	ns
	Chip select to end of write	tcw	60	-	70	-	80	-	ns
	Address set-up time	tAS	0	-	0	-	0	-	ns
	Address valid to end of write	tAW	60	-	70	-	80	-	ns
	Write pulse width	tWP	55	-	55	-	70	-	ns
	Write recovery time	twr	0	-	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	25	0	25	0	30	ns
	Data to write time overlap	tDW	30	-	35	-	40	-	ns
	Data hold from write time	tDH	0	-	0	-	0	-	ns
	End write to output low-Z	tow	5	-	5	-	5	-	ns

^{*} All the parameters are measured with 30pF test load

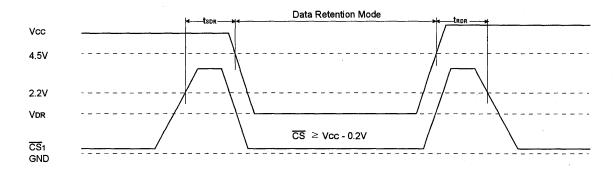


DATA RETENTION CHARACTERISTICS

Item	Symbol VDR		Test Condi	tion*	Min	Typ**	Max	Unit
Vcc for data retention			CS≥Vcc-0.2.0V		2.0	-	3.6	V
		KM68V4000BL/L-L		L-Ver LL-Ver	-	1 0.5	30 15	
		KM68V4000BLI/LI-L	<u>Vcc=3.0V</u> <u>CS</u> ≥ Vcc-0.2V	L-Ver LL-Ver	-	-	30 20	μA
Data retention current	IDR	KM68U4000BL/L-L		L-Ver LL-Ver	-	1 0.5	30 15	,
		KM68U4000BLI/LI-L		L-Ver LL-Ver	-	-	30 20	-
Data retention set-up time	tsDF	₹	See data retention)	0	-	-	
Recovery time	tRDI	₹	waveform		5	-	;	ms

^{* 1)} Commercial Product : Ta=0 to 70 $^{\circ}$, unless otherwise specified 2) Industrial Product : Ta=-40 to 85 $^{\circ}$, unless otherwise specified ** Ta=25 $^{\circ}$

DATA RETENTION TIMING DIAGRAM



FUNCTIONAL DESCRIPTION

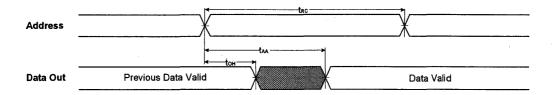
CS	WE	ŌĒ	, Mode	1/0	Current Mode
Н	Х	Х	Power Down	High-Z	lsb1
L	Н	Н	Output Disable	High-Z	lcc
L	Н	L	Read	Dout	lcc
L	L	Х	Write	Din	lcc

^{*}X means don't care (Must be in low or high state)

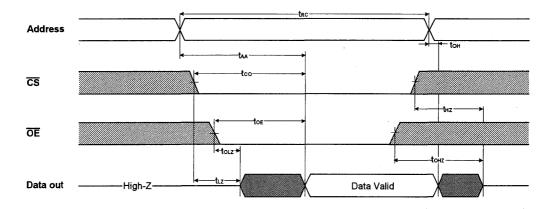


TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled) (CS=OE=VIL, WE=VIH)



TIMING WAVEFORM OF READ CYCLE(2) (WE=VIH)

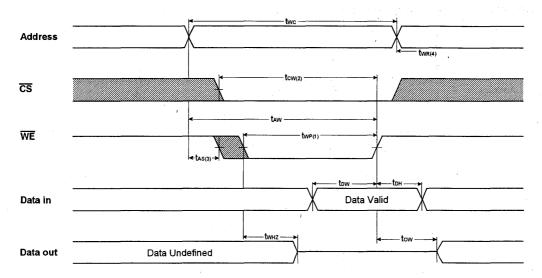


NOTES (READ CYCLE)

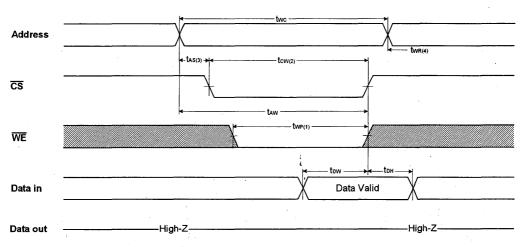
- 1. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
- 2. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device.



TIMING WAVEFORM OF WRITE CYCLE(1) (WE Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) (CS Controlled)



NOTES (WRITE CYCLE)

- 1. A write occurs during the overlap(tWP) of a low \overline{CS} and low \overline{WE} . A write begins at the latest transition among \overline{CS} goes low and \overline{WE} going low: A write end at the earliest transition among \overline{CS} going high and \overline{WE} going high, tWP is measured from the beginning of write to the end of write.
- 2. tCW is measured from the \overline{CS} going low to end of write.
- 3. tAS is measured from the address valid to the beginning of write.
- 4. tWR is measured from the end of write to the address change. tWR applied in case a write ends as $\overline{\text{CS}}$ or $\overline{\text{WE}}$ going high.



512Kx8 bit Low Power and Low Voltage CMOS SRAM with 48-CSP(Chip Size Package)

FEATURES

• Process Technology: 0.4 \(\mu \text{ CMOS} \)

Organization : 512Kx8Power Supply Voltage

KM68V4000BZ Family : $3.3V\pm0.3V$ KM68U4000BZ Family : $3.0V\pm0.3V$

Low Data Retention Voltage : 2V(Min)

There exists a state and TTL Commetible

• Three state output and TTL Compatible

• Package Type: 48-CSP with 0.75mm ball pitch

GENERAL DESCRIPTION

The KM68V4000BZ and KM68U4000BZ family are fabricated by SAMSUNG's advanced Full CMOS process technology. The family can support various operating temperature ranges and has very samll from factor with 0.75 ball pitch and 6 x 8 ball array. The family also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

B decade	Operating Temp.Range	Vcc Range	Speed (ns)	Power Dis	Power Dissipation	
Product Family				Operating (Icc2)	Standby (ISB1)	PKG Type
KM68V4000BLZ-L	Commercial	3.0~3.6V	85	70mA(Max)	15 <i>µ</i> A	48-CSP (6x8 ball area with 0.75mm ball pitch)
KM68U4000BLZ-L	(0~70℃)	2.7~3.3V	100	70mA(Max)	(max)	
KM68V4000BLI-L	Industria	3.0~3.6V	85	70mA(Max)	20 <i>µ</i> A	
KM68U4000BLI-L	(-40~85℃)	2.7~3.3V	100	70mA(Max)	(max)	

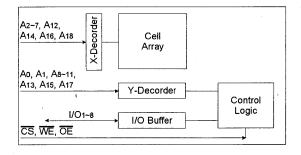
^{*} The parameter is measured with 30pF test load.

48-CSP PIN TOP VIEW

	1	2	3	4	5	6
Α	Ao	A1	CS2	Аз	A6	A8
В	1/05	A2	WE	A4	A7	1/01
С	I/O6		NC	A5		1/02
D	Vss					Vcc
Ε	Vcc					Vss
F	1/07		A18	A17		I/O3
G	I/Os	ŌE	CS ₁	A16	A15	1/04
Н	A9	A10	A11	A12	А13	A14

^{*} See last page for package dimension.

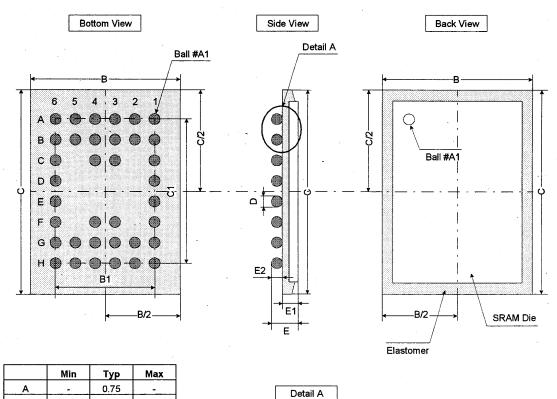
FUNCTIONAL BLOCK DIAGRAM



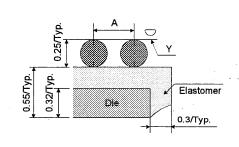
Name	Function	Name	Function
Ao~A18	Address Inputs	Vcc	Power
WE	Write Enable Input	Vss	Ground
<u>cs</u>	Chip Select Input	1/01~1/08	Data Inputs/Outputs
ŌĒ	Output Enable Input		



PACKAGE DIMENSIONS (Units: mm)



	Min	Тур	Max
Α	-	0.75	
В	7.10	7.20	7.30
B1	-	3.75	-
 C	11.55	11.65	11.75
C1	-	5.25	
D	0.30	0.35	0.40
Е	-	0.80	0.81
E1	-	0.55	-
E2		0.25	-
Υ	-	-	0.08



Notes.

- 1. Bump counts : 48(8row x 6row)
- 2. Bump pitch: (x,y)=(0.75 x 0.75)(typ.)
- All tolerence are +/-0.050 unless otherwise specified.
- 4. Typ : Typical
- 5. Y is copianarity: 0.08(max)



256Kx16 bit Low Power and Low Voltage CMOS Static RAM

FEATURES

• Process Technology: 0.4

m CMOS

Organization: 256K x16

· Power Supply Voltage

KM68V4000B Family : 3.3 ± 0.3 V KM68U4000B Family : 3.0 ± 0.3 V

Low Data Retention Voltage : 2V(Min)
 Three state output and TTL Compatible

Package Type : JEDEC Standard

44-TSOP(II)-Forward/Reverse

GENERAL DESCRIPTION

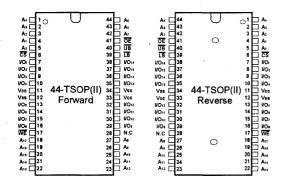
The KM616V4000B and KM616U4000B family are fabricated by SAMSUNG's advanced CMOS process technology. The family can support various operating temperature ranges and have various package types for user flexibility of system design. The family also support low data retention voltage for battery backup operation with low data retention current.

PRODUCT FAMILY

5		V	S	Power Di			
Product List	Operating Temp.	Vcc Range	Speed (ns)	Standby (IsB1, Max)	Operating (ICC2)	PKG Type	
KM616V4000BL-L	Commercial(0~7°C)	mmercial(0~7°C) 3.0~3.6V 70*/85*/1		15 <i>µ</i> A			
KM616V4000BLI-L	Industrial(-40~85°C)	3.0~3.6V	70*/85*/100	20 <i>µ</i> A	70mA	44 TCOD(II) B/F	
KM616U4000BL-L	Commercial(0~7°C)	2.7~3.3V	70*/85*/100	15 <i>µ</i> A	70mA	44-TSOP(II)-R/F	
KM616U4000BLI-L	Industrial(-40~85°C)	2.7~3.3V	70*/85*/100	20 µA			

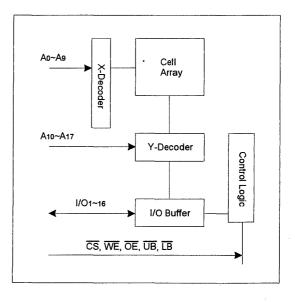
^{*} The parameter is measured with 30pF test load.

PIN DESCRIPTION



Name	Function	Name	Function
A0~A17	Address Inputs	ĽΒ	Lower Byte (I/O1~8)
WE	Write Enable Input	ŪB	Upper Byte(I/O9~16)
CS	Chip Select Input	Vcc	Power
ŌĒ	Output Enable Input	Vss	Ground
I/O1~I/O16	Data Input/Output	N.C	No Connection

FUNCTIONAL BLOCK DIAGRAM



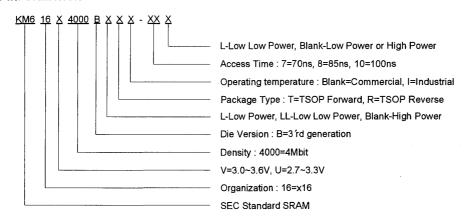


PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST

	Temp Product 70°C)	Industrial Temp Products (-40~85℃)				
Part Name	Function	Part Name	Function			
KM616V4000BLT-7L	44-TSOP(II)F, 70ns, 3.3V,LL	KM616V4000BLTI-7L	44-TSOP(II)F, 70ns, 3.3V,LL			
KM616V4000BLT-8L	44-TSOP(II)F, 85ns, 3.3V,LL	KM616V4000BLTI-8L	44-TSOP(II)F, 85ns, 3.3V,LL			
KM616V4000BLT-10L	44-TSOP(II)F, 100ns, 3.3V,LL	KM616V4000BLTI-10L	44-TSOP(II)F, 100ns, 3.3V,LL			
KM616V4000BLR-7L	44-TSOP(II)R, 70ns, 3.3V,LL	KM616V4000BLRI-7L	44-TSOP(II)R, 70ns, 3.3V,LL			
KM616V4000BLR-8L	44-TSOP(II)R, 85ns, 3.3V,LL	KM616V4000BLRI-8L	44-TSOP(II)R, 85ns, 3.3V,LL			
KM616V4000BLR-10L	44-TSOP(II)R, 100ns, 3.3V,LL	KM616V4000BLRI-10L	44-TSOP(II)R, 100ns, 3.3V,LL			
KM616U4000BLT-7L	44-TSOP(II)F, 70ns, 3.0V,LL	KM616U4000BLTI-7L	44-TSOP(II)F, 70ns, 3.0V,LL			
KM616U4000BLT-8L	44-TSOP(II)F, 85ns, 3.0V,LL	KM616U4000BLTI-8L	44-TSOP(II)F, 85ns, 3.0V,LL			
KM616U4000BLT-1OL	44-TSOP(II)F, 100ns, 3.0V,LL	KM616U4000BLTI-10L	44-TSOP(II)F, 100ns, 3.0V,LL			
KM616U4000BLR-7L	44-TSOP(II)R, 70ns, 3.0V,LL	KM616U4000BLRI-7L	44-TSOP(II)R, 70ns, 3.0V,LL			
KM616U4000BLR-8L	44-TSOP(II)R, 85ns, 3.0V,LL	KM616U4000BLRI-8L	44-TSOP(II)R, 85ns, 3.0V,LL			
KM616U4000BLR-10L	44-TSOP(II)R, 100ns, 3.0V,LL	KM616U4000BLRI-10L	44-TSOP(II)R, 100ns, 3.0V,LL			

ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	VIN, VOUT	-0.5 to Vcc+0.5	V	-
Voltage on Vcc supply relative to Vss	Vcc	-0.3 to 4.6	V	-
Power Dissipation	PD	0.7	W	•
Storage temperature	Тѕтс	-65 to 150	°C	-
Operating Temperature	TA	0 to 70	c	KM616V4000BL-L KM616U4000BL-L
Operating reinperature	'^	-40 to 85	c	KM616V4000BLI-L KM616U4000BLI-L
Soldering temperature and time	TSOLDER	260°C, 10sec (Lead Only)	-	

^{*} Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*

ltem	Symbol	Product	Min	Typ**	Max	Unit
Supply voltage	, Acc	KM616V4000B Family KM616U4000B Family	3.0 2.7	3.3 3.0	3.6 3.3	V V
Ground	Vss	All Family	0	0	0	٧
Input high voltage	VIN	KM616V4000B Family KM616U4000B Family	2.2 2.2	-	Vcc+0.3 Vcc+0.3	V V
Input low voltage	VIL	KM616V4000B Family KM616U4000B Family	-0.3*** -0.3***	-	0.4 0.4	V

^{* 1)} Commercial Product : Ta=0 to 70 °C, unless otherwise specified

CAPACITANCE* (f=1MHz, Ta=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	CIN	Vin=0V	-	8	pF
Input/Output capacitance	Cio	Vio=0V	-	10	pF

^{*} Capacitance is sampled not 100% tested



²⁾ Industrial Product : Ta=-40 to 85 °C, unless otherwise specified

^{**} Ta=25℃

^{***} VIL(min)=-3.0V for \(\le \) 30ns pulse width

DC AND OPERATING CHARACTERISTICS

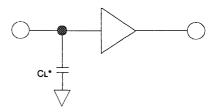
	Item	Symbol	Test Conditions*			Typ**	Max	Unit	
Input leaka	ige current	lu	VIL=Vss to Vcc	VIL=Vss to Vcc			1	μA	
Output leal	kage current	ILO	CS=ViH or ViL		-1	-	1	μА	
Operating	power supply current	Icc	CS=VIL, VIN=VIH or VIL, VIL=0mA	Read	-	-	10	mA	
Operating	power supply current	100	CS-VIL, VIN-VIA OF VIL, VIL-OTTIA	Write	, -		45	IIIA	
		lcc1	Cycle time=1 µs 100% duty	Read	-	•	10		
Average operatingcurren		1001	<u>CS</u> ≤,0.2V, VIL≤0.2V,		-	-	45	mA	
		lcc2	Min cycle, 100% duty, ViL=0mA CS=ViL, ViL=Viн or ViL			-	70	mA	
Output low	voltage	VoL	IoL=2.1mA		-	-	0.4	٧	
Output high	h voltage	Voн	IOH=-1.0mA		2.2	-	-	V	
Standby C	urrent(TTL)	İSB	CS=ViH		-	-	0.5	mA	
	KM616V4000BL-L			Low Low Power	-	-	15	μA	
Standby Current	KM616V4000BLI-L	ISB1	CS≥Vcc-0.2V. Others=0~Vcc	Low Low Power	-	-	20	μA	
(CMOS)	KM616U4000BL-L	1961		Low Low Power	-	-	15	μA	
	KM616U4000BLI-L	1		Low Low Power	-	-	20	μA	

^{* 1)} Commercial Product : Ta=0 to 70°C, Vcc=3.3±0.3V (616V4000B Family), Vcc=3.0±0.3V (616U4000B Family)

A.C CHARACTERISTICS

TEST CONDITIONS (1.Test Load and Test Input/Output Reference)*

Item	Value	Remark
Input pulse level	0.4 to 2.2V	•
Input rise fall time	5ns	-
input and output reference voltage	1.5V	•
Output load (See right)	CL=100pF+1TTL **CL=30pF+1TT	-



* Including scope and jig capacitance

²⁾ Industrial Product : Ta=-40 to 85 °C, Vcc=3.3 ± 0.3V (616V4000BI Family), Vcc=3.0 ± 0.3V (616U4000BI Family) ** Ta=25 °C

^{*} See DC Operating conditions
** KM616V4000BL-7L/8L Family, KM616U4000BL-7L/8L Family

TEST CONDITIONS (2. Temperature and Vcc Conditions)

Product Family	Temperature	Power Supply(Vcc)	Speed Bin	Comments
KM68V4000BL-L	0~70℃	3.3V ± 0.3	70*/85*/100ns	Commercial
KM68V4000BLI-L	-40~85℃	3.3V ± 0.3	70*/85*/100ns	Industrial
KM68U4000BL-L	0~70℃	3.0V ± 0.3	70*/85*/100ns	Commercial
KM68U4000BLI-L	-40~85℃	3.0V ± 0.3	70*/85*/100ns	Industrial

^{*} All the parameters are measured with 30pF test load.

PARAMETER LIST FOR EACH SPEED BIN

					Spec	d Bins			
	Parameter List		70)ns	88	ins	10	0ns	Units
			Min Max		Min Max		Min	Max	
Read	Read cycle time	tRC	70	-	85	-	100	-	ns
	Address access time	tAA	-	70	-	85	-	100	ns
	Chip select to output	tco	-	70	-	85	-	100	ns
	Output enable to valid output	tOE	-	35		40	-	50	ns
	Chip select to low-Z output	tLZ	10	-	10	-	10	-	ns
	Output enable to low-Z output	toLZ	5	-	5	-	5	-	ns
	Chip disable to high-Z output	tHZ	0	25	0	25	0	30	ns
	OE disable to high-Z output	tonz	0	25	0	25	0	30	ns
	Output hold from address change	tон	10	-	10	-	15	-	ns
	LB, UB valid to data output	tBA	-	35	-	40		50	ns
Write	UB, LB disable to high-Z output	tBHZ	0	25	0	25	0	30	ns
	Write cycle time	twc	70	-	85	-	100	-	ns
	Chip select to end of write	tcw	60	-	70	-	80	-	ns
	Address set-up time	tAS	0	-	0	-	0	-	ns
	Address valid to end of write	tAW	60	-	70	-	80	-	ns
	Write pulse width	tWP	55	-	55	-	70	-	ns
	Write recovery time	twr	0	-	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	25	0	25	0	30	ns
	Data to write time overlap	tDW	30	-	35	-	40	-	ns
	Data hold from write time	tDH	0	-	0	-	0	-	ns
	End write to output low-Z	tow	5	-	- 5	-	5	-	ns
	LB, UB valid to end of write	tBW	60	-	70	-	80	-	ns

^{*} All the parameters are measured with 30pF test load.

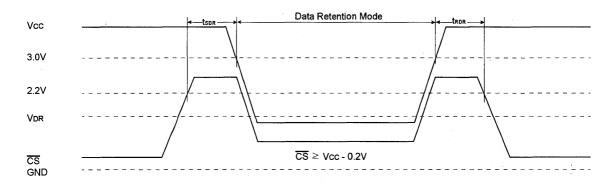


DATA RETENTION CHARACTERISTICS

Item		Symbol Test Condition*		Min	Typ**	Max	Unit	
Vcc for data retention	VDR		CS≥Vcc-0.2V	2.0	-	3.6	V	
		KM68V4000BL-L	Vcc=3.0V CS≥Vcc-0.2V	LL-Ver	-	0.5 15	15) μA
. Data retention current	IDR	KM68V4000BLI-L		LL-Ver	-	-	20	
Data retention current		KM68U4000BL-L		LL-Ver	-	0.5	15	
		KM68U4000BLI-L		LL-Ver	-	-	20	
Data retention set-up time	tsDF	?	See data retentio	n	0	-	-	
Recovery time	tRDF	₹ .	waveform		5	-	-	ms

^{* 1)} Commercial Product : Ta=0 to 70°C, unless otherwise specified 2) Industrial Product : Ta=-40 to 85°C, unless otherwise specified ** Ta=25°C

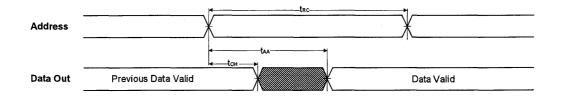
DATA RETENTION WAVE FORM



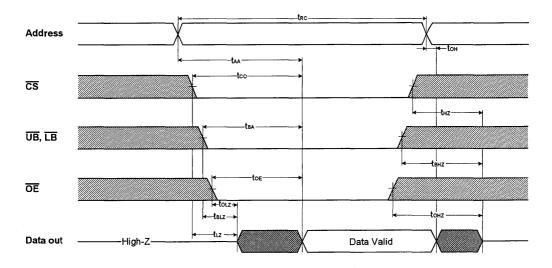
TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled)

(CS=OE=VIL, WE=VIH, UB or and LB=VIL)



TIMING WAVEFORM OF READ CYCLE(2) (WE=VIH)

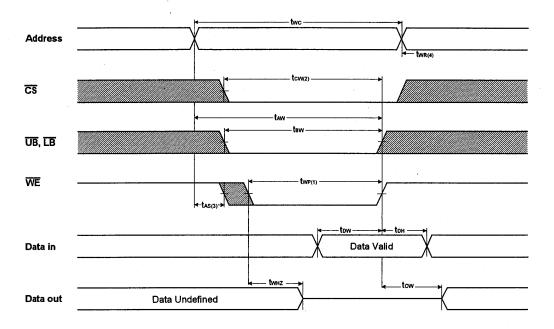


NOTES (READ CYCLE)

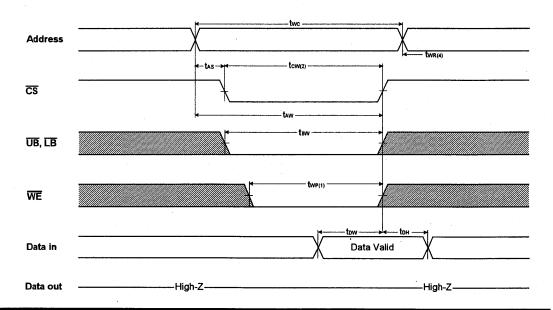
- 1. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
- 2. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device.



TIMING WAVEFORM OF WRITE CYCLE(1) (WE Controlled)

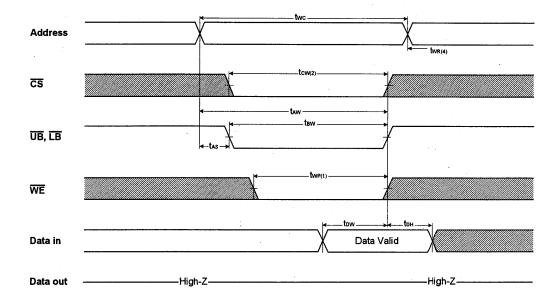


TIMING WAVEFORM OF WRITE CYCLE(2) (CS Controlled)





TIMING WAVEFORM OF WRITE CYCLE(3) (UB, LB Controlled)



NOTES (WRITE CYCLE)

- 1. A write occurs during the overlap(tWP) of a low \overline{CS} and low \overline{WE} . A write begins when \overline{CS} goes low and \overline{WE} goes low with asserting \overline{UB} or \overline{LB} for single byte operation or simultenious asserting \overline{UB} and \overline{LB} for double byte operation. A write ends at the earliest transition when \overline{CS} goes high and \overline{WE} goes high. The tWP is measured from the beginning of write to the end of write.
- 2. tCW is measured from the CS going low to end of write.
- 3. tAS is measured from the address valid to the beginning of write.
- 4. tWR is measured from the end or write to the address change. tWR applied in case a write ends as CS or WE going high.

FUNCTIONAL DESCRIPTION

CS	LB	UB	WE	ŌĒ	Mode	I/O1~8	I/O9~16	Current Mode
Н	Х	Х	Х	Х	Not Select	High-Z	High-Z	ISB1
L	Х	Х	Н	Н	Output	High-Z	High-Z	Icc
L	Н	Н	×	х	Disable	High-Z	High-Z	1
L	L H L	H L L	Н	L	Read	Dout High-Z Dout	High-Z Dout Dout	lcc
L	L H L	H L L	L	х	Write	Din High-Z Din	High Din Din	Icc

^{*} X means don't care (Must be in low or high state)



256Kx16bit Low Power and Low Voltage CMOS SRAM with 48-CSP(Chip Size Package)

FEATURES

• Process Technology: 0.4 µm CMOS

Organization :256Kx16Power Supply Voltage

KM616V4000BZ Family : $3.3V \pm 0.3V$ KM616U4000BZ Family : $3.0V \pm 0.3V$

. Low Data Retention Voltage: 2V(Min)

· Three state output and TTL Compatible

· Package Type: 48-CSP with 0.75 pitch

GENERAL DESCRIPTION

The KM616V4000BZ and KM616U4000BZ family are fabricated by SAMSUNG's advanced Full CMOS process technology. The family can support various operating temperature ranges and has very samll from factor with 0.75 ball pitch and 6 x 8 ball array. he family also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

Product	0	Operating emp.Range (min~max) Speed(ns)		Power Diss		
Family	Temp.Range			Operating (Icc2)	Standby (IsB1)	PKG Type
KM616V4000BLZ-L	Commercial	3.0~3.6V	85	90mA(Max)	15 <i>µ</i> A	40 CCD
KM616U4000BLZ-L	(0~70℃)	1.8~2.7V	100	90mA(Max)	(max)	48-CSP (6x8 ball area
KM616V4000BLZI-L	V4000BLZI-L Industria 3.0~3.6		85	90mA(Max)	20 <i>µ</i> A	with 0.75mm
KM616U4000BLZ	(-40~85℃)	2.7~3.3V	100	90mA(Max)	(max)	ball pitch)

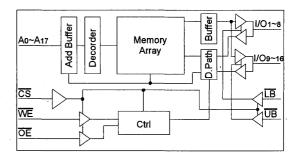
^{*} The parameter is measured with 30pF test load.

48-CSP PIN TOP VIEW

	1	2	3	4	5	6
Α	LB	ŌĒ	Ao	A1	A ₂	NC
В	I/O9	ŪB	Аз	A4	cs	1/01
С	I/O10	1/011	A5	A6	I/O ₂	I/O3
D	Vss	I/O12	A17	A7	1/04	Vcc
Е	Vcc	I/O13	NC	A16	I/O ₅	Vss
F	I/O15	I/O14	A14	A15	1/06	1/07
G	I/O16	NC	A12	A13	WE	1/08
Н	NC	A8	A9	A10	A11	NC

^{*} See last page for package dimension.

FUNCTIONAL BLOCK DIAGRAM

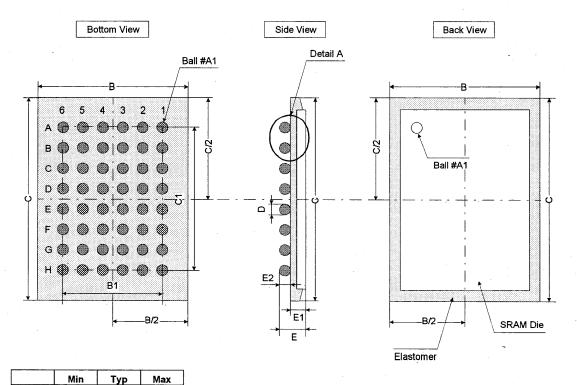


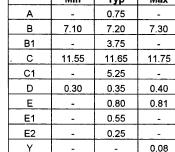
Name	Function	Name	Function
A0~A17	Address Inputs	ĽВ	Lower Byte(I/O1 ~ 8)
WE	Write Enable Input	ŪB	Upper Byte(I/O9~16)
CS	Chip Select Input	Vcc	Power .
ŌĒ	Output Enable Input	Vss	Ground
1/01~1/016	Data Inputs/Outputs	N.C.	No Connection

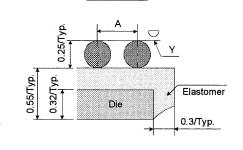


KM616V4000BZ, KM616U4000BZ Family

PACKAGE DIMENSIONS (Units : mm)







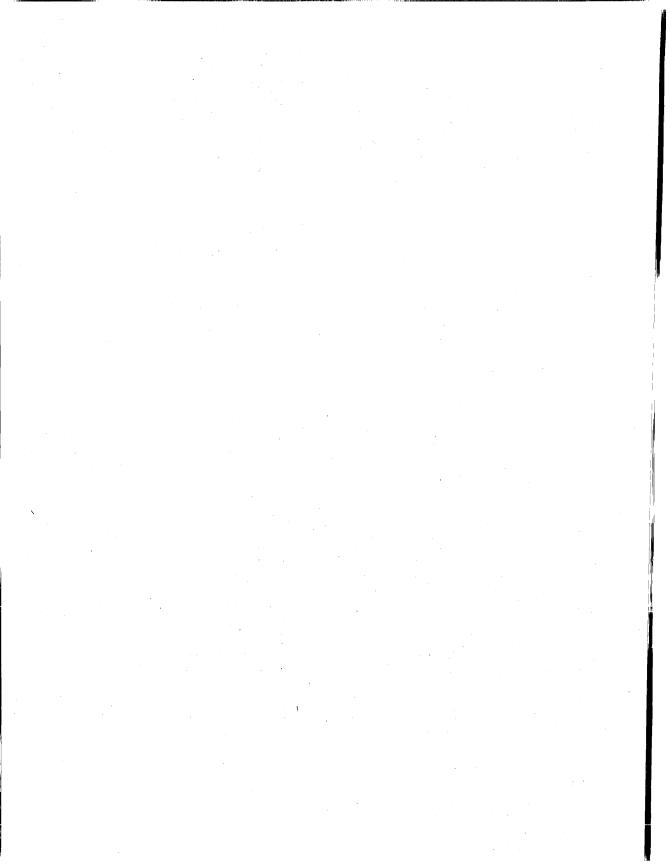
Detail A

Notes.

- 1. Bump counts: 48(8row x 6row)
- 2. Bump pitch: $(x,y)=(0.75 \times 0.75)(typ.)$
- All tolerence are +/-0.050 unless otherwise specified.
- 4. Typ : Typical
- 5. Y is copianarity: 0.08(max)



Super Low Power and Low Voltage SRAM (Full CMOS)



256Kx8 bit Super Low Power and Low Voltage Full CMOS Static RAM

FEATURES

Process Technology: 0.4

m Full CMOS

Organization : 128Kx8Power Supply Voltage

KM68FV1000 Family: 3.0V(Min) ~ 3.6V(Max) KM68FS1000 Family: 2.3V(Min) ~ 3.3V(Max) KM68FR1000 Family: 1.8V(Min) ~ 2.7V(Max)

Low Data Retention Voltage: 1.5V(Min)
 Three state output and TTL Compatible

· Package Type : JEDEC Standard

32-SOP, 32-TSOP(I)-F/R, 32-sTSOP(I)-Forward/Reverse

GENERAL DESCRIPTION

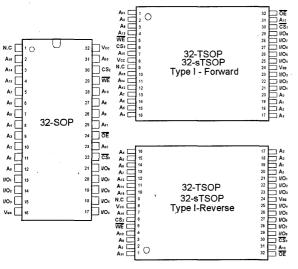
The KM68FV1000, KM68FS1000 and KM68FR1000 family are fabricated by SAMSUNG's advanced Full CMOS process technology. The family can support various operating temperature ranges and have various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

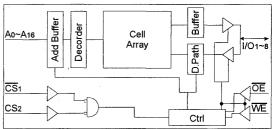
Product	Operating	Vec	Speed	Power	Dissipation		
Family	Temp.Range	Range (ns)		Standby (IsB1)	Operating (Icc2)	PKG Type	
KM68FV1000		3.0~3.6V	70*/85@Vcc=3.3±0.3V		55mA(Max)	00 TOOD(I)	
KM68FS1000	M68FS1000 Commercial (0~70°C)		70*/85@Vcc=3.0±0.3V 120*/150@VCC=2.5±0.2V	1μΑ*** /5μΑ** (Max)	50mA(Max) 30mA(Max)	32-TSOP(I) Forward/ Reverse	
KM68FR1000		1.8~2.7V	300*@Vcc=2.0±0.2V	(Wax)	15mA(Max)	32-sTSOP(I)	
KM68FV1000I		3.0~3.6V	70*/85@Vcc=3.3±0.3V		55mA(Max)	Forward/	
KM68FS1000I	Industrial (-40~85℃)	2.3~3.3V	70*/85@Vcc=3.0±0.3V 120*/150@VCC=2.5±0.2V	1 μA*** /5 μA** (Max)	50mA(Max) 30mA(Max)	Reverse	
KM68FR1000I			(IVIAX)	15mA(Max)	02-001		

^{*} measured with 30pF test load, ** for low power version, *** for super low power version with special handling.

PIN DESCRIPTION



FUNCTIONAL BLOCK DIAGRAM



Name	Function	Name	Function
A0~A16	Address Inputs	Vcc	Power
WE	Write Enable Input	Vss	Ground
CS1,CS2	Chip Select Input	I/O1~I/O8	Data Inputs/Outputs
Œ	Output Enable	N.C.	No Connection

PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST FOR LOW LOW POWER CONSUMPTION

Comm	ercial Temp Product (0~70°C)	Industrial Temp Product (-40~85℃)			
Part Name	Function	Part Name	Function		
KM68FV1000G-7	32-SOP, 70ns, 3.3V, LL	KM68FV1000GI-7	32-SOP, 70ns, 3.3V, LL		
KM68FV1000G-8	32-SOP, 85ns, 3.3V, LL	KM68FV1000GI-8	32-SOP, 85ns, 3.3V, LL		
KM68FV1000T-7	32-TSOP F, 70ns, 3.3V, LL	KM68FV1000TII-7	32-TSOP F, 70ns, 3.3V, LL		
KM68FV1000T-8	32-TSOP F, 85ns, 3.3V, LL	KM68FV1000T-8	32-TSOP F, 85ns, 3.3V, LL		
KM68FV1000R-7	32-TSOP R, 70ns, 3.3V, LL	KM68FV1000RI-7	32-TSOP R, 70ns, 3.3V, LL		
KM68FV1000R-8	32-TSOP R, 85ns, 3.3V, LL	KM68FV1000RI-8	32-TSOP R, 85ns, 3.3V, LL		
KM68FS1000G-12	32-SOP, 120/70ns, *2.5/3.0V, LL	KM68FS1000GI-12	32-SOP, 120/70ns, 2.5/3.0V, LL		
KM68FS1000G-15	32-SOP, 150/85ns, 2.5/3.0V, LL	KM68FS1000GI-15	32-SOP, 150/85ns, 2.5/3.0V, LL		
KM68FS1000T-12	32-TSOP F, 120/70ns, *2.5/3.0V, LL	KM68FS1000TI-12	32-TSOP F, 120/70ns, 2.5/3.0V, LL		
KM68FS1000T-15	32-TSOP F, 150/85ns, 2.5/3.0V, LL	KM68FS1000TI-15	32-TSOP F, 150/85ns, 2.5/3.0V, LL		
KM68FS1000R-12	32-TSOP R, 120/70ns, 2.5/3.0V, LL	KM68FS1000RI-12	32-TSOP R, 120/70ns, 2.5/3.0V, LL		
KM68FS1000R-15	32-TSOP R, 150/85ns, 2.5/3.0V, LL	KM68FS1000RI-15	32-TSOP R, 150/85ns, 2.5/3.0V, LL		
KM68FS1000TG-12	32-sTSOP F, 120/70ns, 2.5/3.0V, LL	KM68FS1000TGI-12	32-sTSOP F, 120/70ns, 2.5/3.0V, LL		
KM68FS1000TG-15	32-sTSOP F, 150/85ns, 2.5/3.0V, LL	KM68FS1000TGI-15	32-sTSOP F, 150/85ns, 2.5/3.0V, LL		
KM68FS1000RG-12	32-sTSOP R, 120/70ns, 2.5/3.0V, LL	KM68FS1000RGI-12	32-sTSOP R, 120/70ns, 2.5/3.0V, LL		
KM68FS1000RG-15	32-sTSOP R, 150/85ns, 2.5/3.0V, LL	KM68FS1000RGI-15	32-sTSOP R, 150/85ns, 2.5/3.0V, LL		
KM68FR1000G-30	32-SOP, 300ns, **2.0/2.5V, LL	KM68FR1000GI-30	32-SOP, 300ns, 2.0/2.5V, LL		
KM68FR1000T-30	32-TSOP F, 300ns, 2.0/2.5V, LL	KM68FR1000TI-30	32-TSOP F, 300ns, 2.0/2.5V, LL		
KM68FR1000R-30	32-TSOP R, 300ns, 2.0/2.5V, LL	KM68FR1000RI-30	32-TSOP R, 300ns, 2.0/2.5V, LL		
KM68FR1000TG-30	32-sTSOP F, 300ns, **2.0/2.5V, LL	KM68FR1000TGI-30	32-sTSOP F, 300ns, 2.0/2.5V, LL		
KM68FR1000RG-30	32-sTSOP R, 300ns, 2.0/2.5V, LL	KM68FR1000RGI-30	32-sTSOP R, 300ns, 2.0/2.5V, LL		

^{*} The meaning of 2.5V/3.0V, 120/70ns is that the operating Vcc is ranged from 2.3V(Min) to 3.3V(Max) with speed 120ns @2.5V±0.2 and 70ns @3.0V±0.2. This type of meaning is applied to other notations like the example.

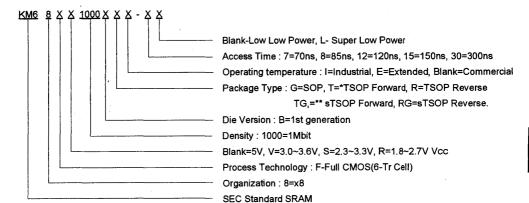
PRODUCT LIST FOR SUPER LOW POWER CONSUMPTION

The product names for super low power version has letter[L] at the end of product name of low low power version. The part name for 128Kx16 Super Low Power product operating at 2.3~3.3V with 70ns @ 3.0V and 120ns @ 2.5V will be KM68FS1000TI-12L. And if suppliment is required for those products please contact Samsung Electronics Branch near your office. Samsung will support with special treatment.



^{**} But in case of KM68FR1000G-30, there is only one speed bin, 300ns though it supports wide range operating VCC.

ORDERING INFORMATION



NOTES: * The size of X x Y for TSOP package is 08 x 20mm.
**The size of X x Y for sTSOP package is 08 x 13.40mm.

ABSOLUTE MAXIMUM RATINGS*

ltem	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	VIN, VOUT	-0.2 to 3.6V ¹⁾	V	-
Voltage on Vcc supply relative to Vss	Vcc	-0.2 to 4.0V ²⁾	V -	-
Power Dissipation	Po	1.0	w	-
Storage temperature	Тѕтс	-55 to 150	င	-
OtiTti	т.	0 to 70	င	KM68FV1000 KM68FS1000 KM68FR1000
Operating Temperature	TA	-40 to 85	ဗ	KM68FV1000I KM68FS1000I KM68FR1000I
Soldering temperature and time	TSOLDER	260°C, 5sec (Lead Only)	-	-

^{*} Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*

ltem	Symbol	Produc	Min	Тур**	Max	Unit	
Supply voltage	Vcc	KM68FV1000 KM68FS1000 KM68FR1000	3.0 2.3 1.8	3.3 2.5/3.0 2.0/2.5	3.6 3.3 2.7	V V V	
Ground	Vss	All Family		0	0	0	٧
	KM68FV1000 Family	Vcc=3.3±0.3V	2.2	-	Vcc+0.2	٧	
		KM68FS1000 Family	Vcc=3.0±0.3V	2.2	-	Vcc+0.2	V
Input high voltage	ViH	KINIOOFS 1000 Faililly	Vcc=2.5±0.2V	2.0	-	Vcc+0.2	٧
		KM68FR1000 Family	Vcc=2.5 ± 0.2V	2.0	-	Vcc+0.2	٧
			Vcc=2.5±0.2V	1.6	-	Vcc+0.2	٧
Input low voltage	VIL	All Family		-0.2***	-	0.4	V

^{* 1)} Commercial Product : TA=0 to 70 ℃, unless otherwise specified 2) Industrial Product : TA=-40 to 85 °C, unless otherwise specified
** TA=25 °C

CAPACITANCE* (f=1MHz, TA=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	CIN	Vin=0V	-	8	pF
Input/Output capacitance	Сю	Vio=0V	-	10	pF

^{*} Capacitance is sampled not 100% tested



¹⁾ VIN/VOUT=0.2 to 3.9V for KM68FV1000 Family.

²⁾ Maximum VCC=-0.2 to 4.6V for KM68F12000 Family.

^{***} VIL(min)=-1.5V for \(\le \) 30ns pulse width

DC AND OPERATING CHARACTERISTICS

	Item	Sym-		Test Con	ditions	(1)	Min	Typ**	Max	Unit	
Input leaka	ge current	lu	Vin=Vss to Vcc			-1	-	1	μA		
Output leal	age current	lLO		=ViH or CS2=ViH or Vss to Vcc	WE=	VIL,	-1	_	1	μА	
Operating	power supply current	lcc	CS ₁	=VIL, CS2=VIH		Read	-	3	5 ⁵⁾	mA	
		ICC	VIN=	VIH or VIL, IIO=0mA	Ą	Write	-	10	15 ⁵⁾	IIIA	
,			Cycl	e time=1 µs 100%d	uty	Read	-	3	5 ⁵⁾		
		lcc1		≤0.2V, ≥Vin≥Vcc-2.0V		Write	-	10	15 ⁵⁾	mA	
Average or	peratingcurrent		CS ₁	=VIH or CS2=VIH	Vcc	=3.3V@70ns	-	-	50 ⁴⁾		
		ICC2	lio=0	lio=0mA Vcc		=2.7V@120ns	-	-	30	mA	
			Min			=2.2V@300ns	-	-	15	}	
			loL Vcc=3.0/3.3V Vcc=2.5V Vcc=2.0V			2.1mA	-	-	0.4		
Output low	voltage	VoL				0.5mA	-	-	0.4	V	
						0.33mA	-	-	0.4		
				Vcc=3.0/3.3V		-1.0mA	2:4	-	-		
Output high	voltage	Voн	Іон	Vcc=2.5V		-0.5mA	2.0	-	-	\ \ \ \	
				Vcc=2.0V		-0.44mA	1.6	-	-	1	
Standby Co	ırrent(TTL)	Isa	CS ₁ :	=VIH, CS ₂ =VIL				-	0.3	mA	
KM68FV1000					Sup	er Low Power	-	0.053)	22)		
Standby Current	KM68FS1000 KM68FR1000	ISB1	<u>CS</u> 1≥Vcc-2.0V CS2≥Vcc-2.0V or		Low	Low Power	-	-	102)	μA	
(CMOS)	KM68FV1000I	1301		≤0.2V erinput =0~Vcc	Sup	er Low Power	-	0.053)	22)		
	KM68FS1000I KM68FR1000I			·		Low Power	-	-	10 ²⁾	μA	

1) -Commercial Product

TA=0 to 70 °C, Vcc=3.3 ± 0.3V for 68FV1000 Family, Vcc=2.3(Min)~3.3V(Max)V for 68FS1000 Family,

Vcc=1.8(Min)~2.7V(Max)V for 68FR1000 Family.

Industrial Product: TA=-40 to 85°C, Vcc=3.3±0.3V for 68FV1000I Family, Vcc=2.3(Min)~3.3V(Max)V for 68FS1000I Family, Vcc=1.8(Min)~2.7V(Max)V for 68FS1000I Family.

2) The value has difference by ±1 µA

Measured at Vcc=3.3(Max).

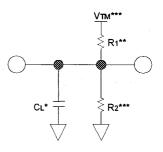
- 3) The value is not 100% tested but obtained statistically at Temp=25 $^{\circ}$ 4) The value is measured at Vcc=3.0 $^{\pm}$ 0.3V
- ICC2=55mA with 70ns at Vcc=3.3 ± 0.3V, but this value is not 100% tested but obtained statistically.
 ICC2=30mA with 120ns cycle at Vcc=2.5 ± 0.2V, but this value is not 100% tested but obtained statistically.
- ICC2=15mA with 300ns cycle at Vcc=2.0±0.2V, but this value is not 100% tested but obtained statistically.
- 5) The value is measured at Vcc=3.0±0.3V, The value measured at Vcc=2.5±2.0V is under the calue of Vcc=3.0±0.3V.

A.C CHARACTERISTICS

TEST CONDITIONS (1.Test Load and Test Input/Output Reference)*

Item	Value	Remark
Input pulse level	0.4 to 2.2V	Vcc=3.3V, 3.0V, 2.5V
input puise revei	0.4 to 1.8V	Vcc=2.0V
Input rise fall time	5ns	-
	1.5V	Vcc=3.3V, 3.0V
input and output reference voltage	1.1V	Vcc=2.5V
	0.9V	Vcc=2.0V,
Output load (See right)	CL=100pF	See Test Condition #2
Output load (See right)	CL=30pF	Jee rest Condition #2

^{*} See test condition of DC and Operating characteristics



^{*} Including scope and jig capacitance **R1=3070 Ω , R2=3150 Ω

TEST CONDITIONS (2. Temperature and Vcc Conditions)

Product Family	Temperature	Vcc Range	Typical Supply Vcc	Speed	Comments
KM68FR1000	0~70℃	1.8(Min)~2.7(Max)	2.0V ± 0.2 Operation	300*ns	
KM68FS1000	0~70℃	2.3(Min)~3.3(Max) -	2.5V ± 0.2 Operation	120*/150ns	Commercial
KIVIOUFS 1000	0-700	2.3(WIII)~3.3(WIAX)	3.0V ± 0.3 Operation	85ns	Commercial
KM68FV1000	0~70℃	3.0(Min)~3.6(Max)	3.3V ± 0.3 Operation	70*/85ns	
KM68FR1000I	-40~85℃	1.8(Min)~2.7(Max)	2.0V ± 0.2 Operation	300*ns	
KM68FS100I0 -4	-40~85℃	2.3(Min)~3.3(Max)	2.5V ± 0.2 Operation	120*/150ns	Industrial
	-40-650	2.5(WIII) -5.5(WIAX)	3.0V ± 0.3 Operation	85ns	muusulai
KM68FV1000I	-40~85℃	3.0(Min)~3.6(Max)	3.3V ± 0.3 Operation	70*/85ns] ·

^{*} All the parameters are measured with 30pF test load

^{***}VTM=2.8V for VCC=3.0/3.3V =2.3V for VCC=2.5V =1.8V for VCC=2.0V

KM68FV1000, KM68FS1000, KM68FR1000 Family

CMOS SRAM

PARAMETER LIST FOR EACH SPEED BIN

								Spee	d Bins						Γ
	Parameter List		nbol 70ns		88	ins	100ns 120ns		Ons	150ns		300ns		Units	
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read	Read cycle time	tRC	70	-	85	-	100	-	120	-	150	-	300	-	ns
	Address access time	tAA	-	70	-	85	-	100	-	120	-	150	-	300	ns
	Chip select to output	tCO1 tCO2	-	70	-	85	-	100	-	120	-	150	-	300	ns
	Output enable to valid output	tOE	-	35	-	45	-	50	-	60	-	75	-	150	ns
	Chip select to low-Z output	tLZ1 tLZ2	10	-	10	-	10	-	10	-	20	-	50	-	ns
	Output enable to low-Z output	toLZ	5	-	5	-	5	-	5	-	10	-	30	-	ns
	Chip disable to high-Z output	tHZ1 tHZ2	0	25	0	25	0	30	0	35	0	40	0	60	ns
	Output disable to high-Z output	tonz	0	25	0	25	0	30	0	35	0	40	0	. 60	ns
	Output hold from address	tOH	10	-	15	-	15	-	15	-	15	-	30	٠-	ns
Write	Write cycle time	twc	70	-	85	-	100	-	120	-	150	_	300	-	ns
	Chip select to end of write	tcw	65	-	70	-	80		100	-	120	-	300	-	ns
	Address set-up time	tAS	0	-	0	-	0	-	0	-	0	-	0	-	ns
	Address valid to end of write	tAW	65	-	70	-	80	-	100	-	120	-	300	-	ns
	Write pulse width	tWP	55	-	60	-	70	-	80	-	100	-	200	-	ns
	Write recovery time	tWR	0	-	0	-	0	-	0	-	0	-	0	-	ns
	Write to output high-Z	twHz	0	25	0	25	0	30	0	35	0	40	0	60	ns
	Data to write time overlap	tDW	30	-	35	-	40	-	50	. -	60	-	120	-	ns
	Data hold from write time	tDH	0	-	0	-	0	-	0	-	0	-	0	-	ns
	End write to output low-Z	tow	5	-	5	-	5	-	5	-	5	-	20	-	ns

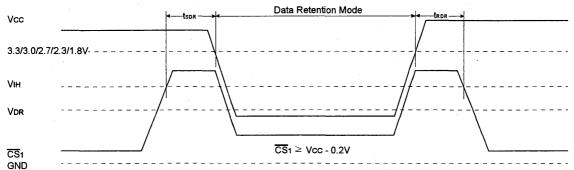
^{*} not yet available, only for reserved speed bins.

DATA RETENTION CHARACTERISTICS

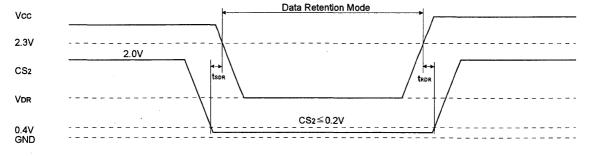
Item	Symbol	Test C	ondition*	Min	Тур**	Max	Unit
Vcc for data retention	VDR	CS1****≥Vcc-2.0	V	1.5	-	3.6	٧
Data retention current	IDR	Vcc=3.0V	Super Low Power	***	0.1	1.0	μA
		CS 1≥Vcc-0.2V	-	-	5.0		
Data retention set-up time	tsdr	See data retention	0	-	-		
Recovery time	tRDR	waveform		tRC	-	-	ns

DATA RETENTION WAVE FORM

1) CS1 controlled



2) CS2 controlled



^{* 1)} Commercial Product : Ta=0 to 70 ℃, unless otherwise specified
2) Industrial Product : Ta=-40 to 85 ℃, unless otherwise specified
** TA=25 ℂ, the value is too small to detect by test machine, 0.01

A statistically

^{***}The min value is almost 0.0 small to use of year.

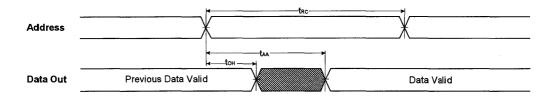
**The min value is almost 0.0 A statistically

***CS1 ≥ Vco-2.0V, CS2 ≥ Vco-2.0V(CS1 controlled) or CS2 ≤ 0.2V(CS2 controlled)

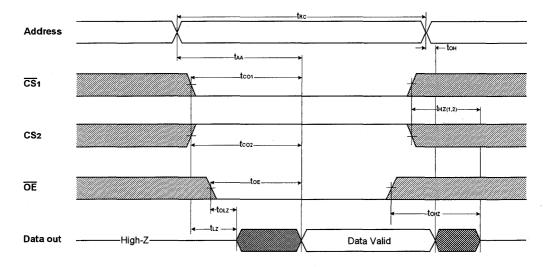
TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (1) (Address Controlled)

(CS=OE=VIL, WE=VIH)



TIMING WAVEFORM OF READ CYCLE (WE=VIH)

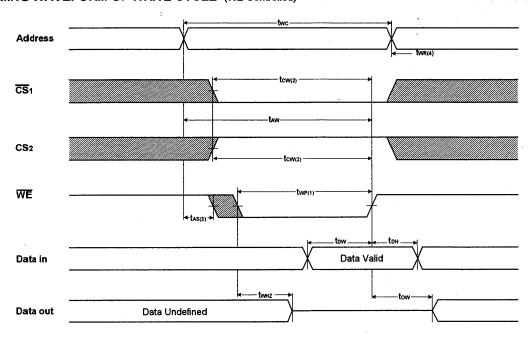


NOTES (READ CYCLE)

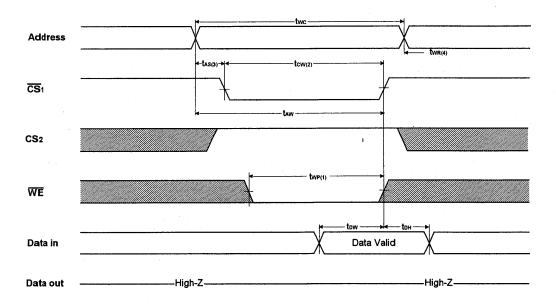
- 1. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
- 2. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device interconnection.



TIMING WAVEFORM OF WRITE CYCLE (WE Controlled)

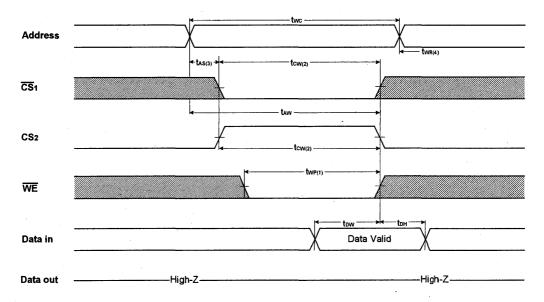


TIMING WAVEFORM OF WRITE CYCLE (CS1 Controlled)





TIMING WAVEFORM OF WRITE CYCLE (CS2 Controlled)



NOTES (WRITE CYCLE)

- 1. A write occurs during the overlap of a low CS1, a high CS2 and a low WE. A write begins at the latest transition among CS1 goes low, CS2 going high and WE going low: A write end at the earliest transition among CS1 going high, CS2 going low and WE going high, tWP is measured from the begining of write to the end of write.
- 2. tCW is measured from the CS1 going low or CS2 going high to the end of write.
- 3. tAS is measured from the address valid to the beginning of write.
- 4. tWR is measured from the end of write to the address change. tWR(1) applied in case a write ends as CS1 or WE going high tWR(2) applied in case a write ends as CS2 going to low.

FUNCTIONAL DESCRIPTION

CS ₁	CS2	WE	ŌĒ	Mode .	I/O	Current Mode
Н	X*	Х	Х	Power Down	High-Z	lsb, lsb1
X	L	X	х	Power Down	High-Z	lsb, lsb1
L	Н	Н	н	Output Disable	High-Z	lcc
L	H	Н	L	Read	Dout	lcc
L	Н	L	X	Write	Din	lcc

^{*} X means don't care (Must be in high or low states)



128Kx8 bit Super Low Power and Low Voltage Full CMOS SRAM with 48-CSP(Chip Size Package)

FEATURES

• Process Technology: 0.4 µm Full CMOS

Organization : 128Kx8Power Supply Voltage

KM68FS1000Z Family : $2.3V(Min) \sim 3.3V(Max)$ KM68FR1000Z Family : $1.8V(Min) \sim 2.7V(Max)$

Low Data Retention Voltage: 1.5V(Min)
 Three state output and TTL Compatible

· Package Type: 48-CSP with 0.75mm ball pitch

GENERAL DESCRIPTION

The KM68FS1000Z and KM68FR1000Z family are fabricated by SAMSUNG's advanced Full CMOS process technology. The family can support various operating temperature ranges and has very samll from factor with 0.75 ball pitch and 6 x 8 ball array. The family also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

Product	ti	ng Vcc Spee		Power Diss	ipation		
Family	Operating Temp.Range	Range	Speed (ns)	Operating (Icc2)	Standby (Isa1)	PKG Type	
KM68FS1000Z	Commercial (0~70°C)	2.3~3.3V	100*@Vcc=3.0±0.3V 150*@Vcc=2.5±0.2V	55mA(Max) 30mA(Max)	10 µÅ (max)	48-CSP	
KM68FR1000Z	(0,700)	1.8~2.7V	300*@Vcc=2.0±0.2V	15mA(Max)] (IIIax)	(6x8 ball area	
KM68FS1000ZI	Industria (-40∼85°C)	2.3~3.3V	100*@Vcc=3.0±0.3V 150*@Vcc=2.5±0.2V	55mA(Max) 30mA(Max)	10 µÅ (max)	with 0.75mm ball pitch)	
KM68FR1000ZI	(-40 00 0)	1.8~2.7V	300*@Vcc=2.0±0.2V	15mA(Max)	(max)		

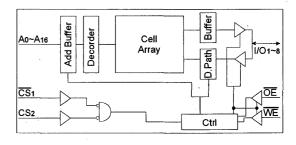
^{*} The parameter is measured with 30pF test load.

48-CSP PIN TOP VIEW

	1	2	3	4	5	6
Α	A ₀	A1.	CS2	Аз	A6	A8
В	I/O5	A2	WE	A4	A7	1/01
С	I/O ₆		NC	A5		I/O2
D	Vss					Vcc
E	Vcc					Vss
F	1/07		NC	NC		I/O3
G	I/O8	ŌĒ	CS ₁	A16	A15	1/04
Н	A9	A10	A11	A12	A13	A14

^{*} See last page for package dimension.

FUNCTIONAL BLOCK DIAGRAM



Name	Function	Name	Function
A0~A16	Address Inputs	Vcc	Power
WE	Write Enable Input	Vss	Ground
CS _{1,CS2}	Chip Select Input	1/01~1/08	Data Inputs/Outputs
ŌĒ	Output Enable	N.C.	No Connection

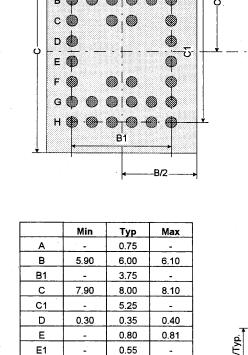


KM68FS1000Z, KM68FR1000Z Family

PACKAGE DIMENSIONS (Units: mm)

E2

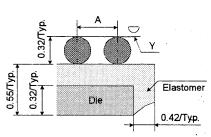
Υ



0.25

	Bottom View		Side View	Back View
		Ball #A1	Detail A	
 	В			B
6 A B C D E F G H	5 4 3 2		E2 E1	Ball #A1
	- ∢ -B/	'∠	E	SRAM Die
			•	Elastomer

-	
6.10	
-	
8.10	
-	
0.40	
0.81	
-	
-	
0.08	



Detail A

Notes.

- 1. Bump counts: 48(8row x 6row)
- 2. Bump pitch: $(x,y)=(0.75 \times 0.75)(typ.)$
- 3. All tolerence are +/-0.050 unless otherwise specified.
- 4. Typ : Typical
- 5. Y is copianarity: 0.08(max)



64Kx16 bit Super Low Power and Low Voltage Full CMOS Static RAM

FEATURES

Process Technology: 0.4

m Full CMOS

Organization : 64Kx16Power Supply Voltage

KM616FV1000 Family: 3.0V(Min) ~ 3.6V(Max) KM616FS1000 Family: 2.3V(Min) ~ 3.3V(Max) KM616FR1000 Family: 1.8V(Min) ~ 2.7V(Max)

Low Data Retention Voltage: 1.5V(Min)

. Three state output status and TTL Compatible

Package Type : JEDEC Standard 44-TSOP(II)-Forward/Reverse

GENERAL DESCRIPTION

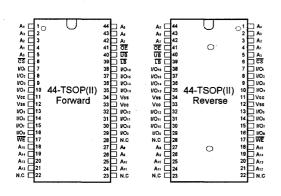
The KM616FV1000, KM616FS1000 and KM616FR1000 family are fabricated by SAMSUNG's advanced Full CMOS process technology. The family can support various operating temperature ranges and have various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

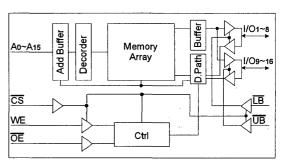
Product	Operating	Voc	Vcc Speed		Dissipation					
Family	Temp.Range	Range	(ns)	Standby (IsB1)	Operating (Icc2)	PKG Type				
KM616FV1000		3.0~3.6V	70*/85@Vcc=3.3±0.3V		4 8 ***	4 1+++	4 4 4 4 4 4		80mA(Max)	
KM616FS1000	Commercial (0~70℃)	2.3~3.3V	70*/85@Vcc=3.3±0.3V 120*/150@VCC=2.5±0.2V	1μΑ*** /5μΑ** (Max)	80mA(Max) 50mA(Max)	44-TSOP(II)				
KM616FR1000]	1.8~2.7V	300*@Vcc=2.0±0.2V	(Wax)	20mA(Max)	Forward/				
KM616FV1000I		3.0~3.6V	70*/85@Vcc=3.3±0.3V	4 8***	80mA(Max)	Reverse				
KM616FS1000I	Industria (-40~85°C)	2.3~3.3V	70*/85@Vcc=3.3±0.3V 120*/150@VCC=2.5±0.2V	1 μΑ*** /5μΑ** (Max)	· J DUMA(Max) I					
KM616FR1000I		1.8~2.7V	300*@Vcc=2.0±0.2V	(WIAX)	20mA(Max)	1				

^{*} measured with 30pF test load, ** for low power version, *** for super low power version with special handling.

PIN DESCRIPTION



FUNCTIONAL BLOCK DIAGRAM



Name	Function	Name	Function
A0~A15	Address Inputs	<u>LВ</u>	Lower Byte(I/O1~8)
WE	Write Enable Input	ŪB	Upper Byte(I/O9~16)
cs	Chip Select Input	Vcc	Power
ŌĒ	Output Enable	Vss	Ground
1/01~1/016	Data Inputs/Out-	N.C.	No Connection



PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST FOR LOW LOW POWER CONSUMPTION

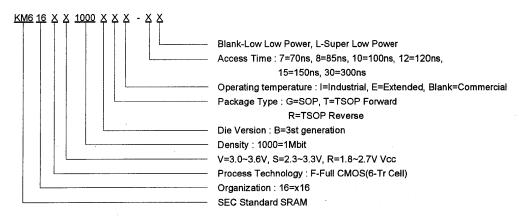
Commo	ercial Temp Product (0~70℃)	Industrial Temp Product (-40~85℃)			
Part Name Function		Part Name	Function		
KM616FV1000T-7	44-TSOP F, 70ns, 3.3V, LL	KM616FV1000TI-7	44-TSOP F, 70ns, 3.3V, LL		
KM616FV1000T-8	44-TSOP F, 85ns, 3.3V, LL	KM616FV1000TI-8	44-TSOP F, 85ns, 3.3V, LL		
KM616FV1000R-7	44-TSOP R, 70ns, 3.3V, LL	KM616FV1000RI-7	44-TSOP R, 70ns, 3.3V, LL		
KM616FV1000R-8	44-TSOP R, 85ns, 3.3V, LL	KM616FV1000RI-8	44-TSOP R, 85ns, 3.3V, LL		
KM616FS1000T-12	44-TSOP F, 120/70ns, *2.5/3.0V, LL	KM616FS1000TI-12	44-TSOP F, 120/70ns, 2.5/3.0V, LL		
KM616FS1000T-15	44-TSOP F, 150/85ns, 2.5/3.0V, LL	KM616FS1000TI-15	44-TSOP F, 150/85ns, 2.5/3.0V, LL		
KM616FS1000R-12	44-TSOP R, 120/70ns, 2.5/3.0V, LL	KM616FS1000RI-12	44-TSOP R, 120/70ns, 2.5/3.0V, LL		
KM616FS1000R-15	44-TSOP R, 150/85ns, 2.5/3.0V, LL	KM616FS1000RI-15	44-TSOP R, 150/85ns, 2.5/3.0V, LL		
KM616FR1000T-30 KM616FR1000R-30	44-TSOP F, 300ns, **2.0/2.5V, LL 44-TSOP F, 300ns, 2.0/2.5V, LL	KM616FR1000TI-30 KM616FR1000RI-30	44-TSOP F, 300ns, 2.0/2.5V, LL 44-TSOP F, 300ns, 2.0/2.5V, LL		

^{*} The meaning of 2.5V/3.0V, 120/70ns is that the operating Vcc is ranged from 2.3V(Min) to 3.3V(Max) with speed 120ns @2.5V ± 0.2 and 70ns @3.0V ± 0.3. This type of meaning is applied to other notations like the example.

PRODUCT LIST FOR SUPER LOW POWER CONSUMPTION

The product names for super low power version has letter[L] at the end of product name of low low power version. The part name for 64Kx16 Super Low Power product operating at 2.3~3.3V with 70ns @ 3.0V and 120ns @ 2.5V will be KM616FA1000TI-12L. And if suppliment is required for those products please contact Samsung Electronics Branch near your office. Samsung will support with special treatment.

ORDERING INFORMATION



^{**} But in case of KM616FR1000T-30, there is only one speed bin, 300ns though it supports wide range operating VCC.

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	VIN,VOUT	-0.2 to 3.6V ¹⁾	V	-
Voltage on Vcc supply relative to Vss	Vcc	-0.2 to 4.0V ²⁾	V	•
Power Dissipation	PD	1.0	W	-
Storage temperature	Тѕтс	-55 to 150	°C	-
Operating Temperature	т.	0 to 70	°C	KM616FV1000 KM616FS1000 KM616FR1000
Operating Temperature	TA	-40 to 85	°	KM616FV1000I KM616FS1000I KM616FR1000I
Soldering temperature and time	Tsolder	260°C, 5sec (Lead Only)	-	

^{*} Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*

Item	Symbol	Produc	at .	Min	Typ**	Max	Unit
Supply voltage	Vcc	KM616FV100 KM616FS100 KM616FR100	0 Family	3.0 2.3 1.8	3.3 2.5/3.0 2.0/2.5	3.6 3.3 2.7	V V V
Ground	Vss	All Fami	ily	0	0	0	V
		KM616FV1000 Family	Vcc=3.3±0.3V	2.2	-	Vcc+0.2	V
		KM616FS1000 Family	Vcc=3.0 ± 0.3V	2.2	-	Vcc+0.2	. V
Input high voltage	ViH	NIVIOTOES TOOU Family	Vcc=2.5 ± 0.2V	2.0	-	Vcc+0.2	V
		KM616FR1000 Family	Vcc=2.5 ± 0.2V	2.0	-	Vcc+0.2	V
		1.6	-	Vcc+0.2	· V		
Input low voltage	VIL	All Fami	-0.2***	-	0.4	V	

^{* 1)} Commercial Product : Ta=0 to 70 °C, unless otherwise specified

CAPACITANCE* (f=1MHz, Ta=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	Cin	Vin=0V		8	pF
Input/Output capacitance	Cıo	Vio=0V	•	10	pF

^{*} Capacitance is sampled not 100% tested



¹⁾ VIN/VOUT=0.2 to 3.9V for KM616FV1000 Family.

²⁾ Vcc=-0.2 to 4.6V for KM616FV1000 Family.

²⁾ Industrial Product : Ta=-40 to 85 °C, unless otherwise specified

^{**} Ta=25℃

^{***} VIL(min)=-1.5V for \leq 30ns pulse width

DC AND OPERATING CHARACTERISTICS

	Item	Sym-		Test Con	(1)	Min	Typ**	Max	Unit	
input leaka	ge current	lu	VIN=	Vss to Vcc			-1	-	1	μA
Output leak	kage current	lLO		VIH or WE=VIL, Vss to Vcc		-1	-	1	μA	
Operating	power supply current	Icc	1	CS1=VIL Read VIN=VIH or VIL, IIo=0mA Write			-	-	10 ⁵⁾	mA
		icc	VIN=				-	-	20 ⁵⁾	mA .
		ICC1	Cycl	e time=1 µs 100%d	uty	Read	-	-	10 ⁵⁾	mΛ
		1001	CS1	≤0.2V	Write	-	-	20 ⁵⁾	mA	
Average op	peratingcurrent				Vcc	=3.3V@70ns	-	-	804)	
		ICC2		СS=Vін, lio=0mA Min cycle, 100% duty		Vcc=2.7V@120ns		-	50	mA
					Vcc	Vcc=2.2V@300ns		-	25	
				Vcc=3.0/3.3V	•	2.1mA	-	-	0.4	
Output low	voltage	Vol	loŁ	IOL Vcc=2.5V		0.5mA	-	-	0.4	V
				Vcc=2.0V		0.33mA	-	-	0.4	
				Vcc=3.0/3.3V		-1.0mA	2.4	-	-	
Output high	n voltage	Voн	Іон	IOH Vcc=2.5V Vcc=2.0V		-0.5mA	2.0	-	-	V
						-0.44mA	1.6 -		-	
Standby Cu	urrent(TTL)	IsB	CS1	=ViH			-	-	0.3	mA
	KM616FV1000 KM616FS1000				Sup	Super Low Power		0.05 ³)	1 ²⁾	μA
Standby Current	KM616FS1000 KM616FR1000	ISB1	CS ≥Vcc-2.0V		Low Low Power		-	-	5 ²⁾	μΛ
(CMOS)	KM616FV1000 KM616FS1000]	Othe	erinput =0~Vcc	Super Low Power		-	0.053)	1 ²⁾	μA
	KM616FR1000					Low Low Power		-	5 ²⁾	1

1) -Commercial Product

Ta=0 to 70 °C, Vcc=3.3 ± 0.3V for 616FV1000 Family, Vcc=2.3(Min)~3.3V(Max)V for 616FS1000 Family,

 $\label{local-loc$ Vcc=1.8(Min)~2.7V(Max)V for 616FR1000I Family.

2) The value has difference by $\pm 1\mu\text{Å}$

Measured at Vcc=3.3(Max).

- 3) The value is not 100% tested but obtained statistically at Temp=25℃
- 4) The value is measured at Vcc=3.0±0.3V lcc2=80mA with 70ns at Vcc=3.3±0.3V, but this value is not 100% tested but obtained statistically.
 - lcc2=50mA with 120ns cycle at Vcc=2.5 ± 0.2V, but this value is not 100% tested but obtained statistically.
 - Icc2=25mA with 300ns cycle at Vcc=2.0 ± 0.2V, but this value is not 100% tested but obtained statistically.
- 5) The value is measured at Vcc=3.0 \pm 0.3V, The value measured at Vcc=2.5 \pm 2.0V is under the calue of Vcc=3.0 \pm 0.3V.

A.C CHARACTERISTICS

TEST CONDITIONS (1.Test Load and Test Input/Output Reference)*

Item	Value	Remark
Input pulse level	0.4 to 2.2V	Vcc=3.3V, 3.0V, 2.5V
input puise level	0.4 to 1.8V	Vcc=2.0V
Input rise fall time	5ns	
	1.5V	Vcc=3.3V, 3.0V
input and output reference voltage	1.1V	Vcc=2.5V
	0.9V	Vcc=2.0V,
Outruit land (Coorinht)	CL=100pF+1TTL	See Test Condition #2
Output load (See right)	CL=30pF+1TTL	See rest Condition #2

R2***

TEST CONDITIONS (2. Temperature and Vcc Conditions)

Product Family	Temperature	Vcc Range	TypicalSupply Vcc	Speed	Comments	
KM616FR1000	0~70℃	1.8(Min)~2.7(Max)	2.0V ± 0.2 Operation	300*ns		
KM616FS1000 0~70°C	2.3(Min)~3.3(Max)	2.5V ± 0.2 Operation	120*/150ns	Commercial		
	2.5(Will)~5.5(Wax)	3.0V ± 0.3 Operation	70*/85ns	Commercial		
KM616FV1000	0~70℃	3.0(Min)~3.6(Max)	3.3V ± 0.3 Operation	70*/85ns		
KM616FR1000I	-40~85℃	1.8(Min)~2.7(Max)	2.0V ± 0.2 Operation	300*ns		
KM616FS100I0 -40~85°C	40 850	2.2/84(=) 2.2/84==	2.5V ± 0.2 Operation	120*/150ns	- Industrial	
	-40~65 C	2.3(Min)~3.3(Max)	3.0V ± 0.3 Operation	70*/85ns		
KM616FV1000I -40~85℃		3.0(Min)~3.6(Max)	3.3V ± 0.3 Operation	70*/85ns	1	

^{*} All the parameters are measured with 30pF test load



^{*} Including scope and jig capacitance **R1=3070 Ω_{+} R2=3150 Ω_{-}

^{***}VTM=2.8V for Vcc=3.0/3.3V

^{=2.3}V for Vcc=2.5V

^{=1.8}V for Vcc=2.0V

^{*} See DC Operating conditions

PARAMETER LIST FOR EACH SPEED BIN

			Speed Bins												
	Parameter List	Symbol	70ns		85	ins	10	Ons	12	Ons	150ns		300ns		Units
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read	Read cycle time	tRC	70	-	85	-	100	-	120	-	150	-	300	-	ns
	Address access time	tAA	-	70	-	85	-	100	-	120	-	150	-	300	ns
	Chip select to output	tCO1 tCO2	-	70	-	85	-	100	-	120	-	150	-	300	ns
	Output enable to valid output	toE	-	35	-	45	-	50	-	60	-	75	-	150	ns
	UB, LB Access Time	tBA	-	35	-	45	-	50	-	60	-	75	-	150	ns
	Chip select to low-Z output	tLZ1 tLZ2	10		10	-	10	-	20	-	20	-	50	-	ns
	Output enable to low-Z output	tOLZ tBLZ	5	-	5	-	5	-	20	-	20	-	30	-	ns
	Chip disable to high-Z output	tHZ1 tHZ2	0	25	0	25	0	30	0	35	0	40	0	60	ns
	Output disable to high-Z output	toHZ tBHZ	0	25	0	25	0	30	0	35	0	40	0	60	ns
	Output hold from address	ton	10	-	15	-	15	-	15	-	15	-	30	-	ns
Write	Write cycle time	twc	70	-	85	-	100	-	120	-	150	-	300	-	ns
	Chip select to end of write	tcw	65	-	70	-	80	-	100	-	120	-	300	-	ns
	Address set-up time	tAS	0	-	0	-	0	-	0	-	0	•	0	-	ns
	Address valid to end of write	tAW	65	•	70	-	80	-	100	1	120	-	300	-	ns
	Write pulse width	tWP	55	-	60	-	70	-	80	-	100	-	200	-	ns
	UB, LB Valid to End of Write	tBW	65	-	70	-	80	-	100	-	120	-	300	-	ns
	Write recovery time	twr	0	-	0	-	0	-	0	-	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	25	0	25	0	30	0	35	0	40	0	60	ns
	Data to write time overlap	tow	30	•	35	-	40	•	50	-	60	-	120	-	ns
	Data hold from write time	tDH	0	-	0	-	0	-	0	-	0	-	0	•	ns
	End write to output low-Z	tow	5		5	-	5	-	5	-	5	-	20	-	ns

^{*} not yet available, only for reserved speed bins.

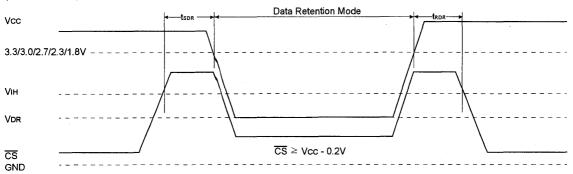
DATA RETENTION CHARACTERISTICS

Item	Symbol	Test C	ondition*	Min	Typ**	Max	Unit
Vcc for data retention	VDR	CS ≥Vcc-2.0V	-	1.5	-	3.6	V
Data retention current	1	Vcc=3.0V	Super Low Power	***	**	1.0	
	IDR	CS≥Vcc-0.2V	Low Low Power	-	-	5.0	μA
Data retention set-up time	tsdr	See data retention	0	-	-		
Recovery time	tRDR	waveform	tRC	-	-	ns	

^{* 1)} Commercial Product : Ta=0 to 70 ℃, unless otherwise specified 2) Industrial Product : Ta=-40 to 85 ℃, unless otherwise specified

DATA RETENTION WAVE FORM

(CS controlled)





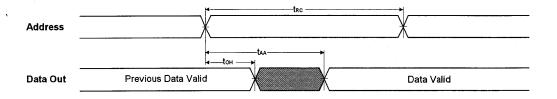
^{**} TA=25°C, the value is too small to detect by test machine, 0.01 μ A statistically

^{***} The min value is almost 0nA statistically

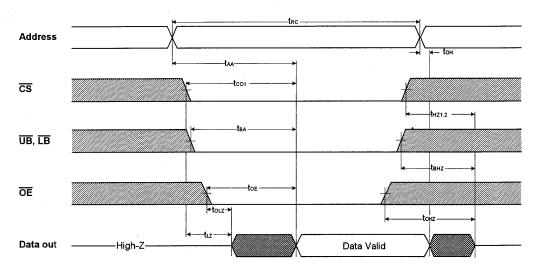
TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (1) (Address Controlled)

(CS=OE=VIL, WE=VIH, UB or, and LB=VIL)



TIMING WAVEFORM OF READ CYCLE (WE=VIH)

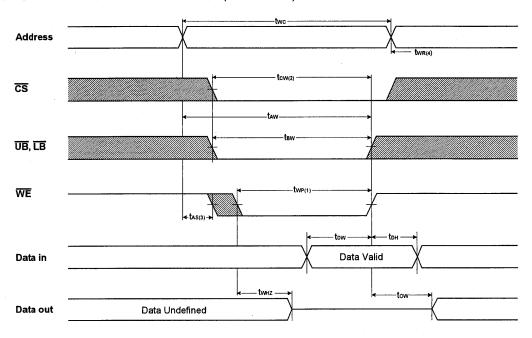


NOTES (READ CYCLE)

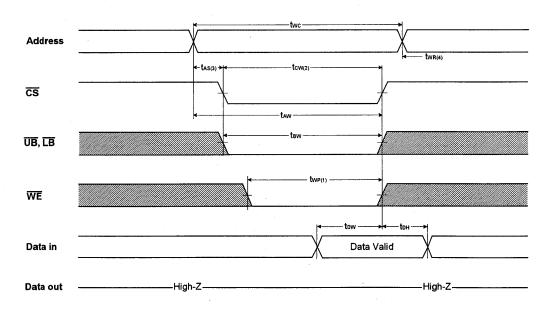
- 1. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
- 2. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device interconnection.



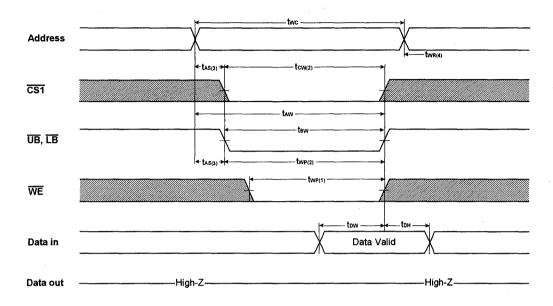
TIMING WAVEFORM OF WRITE CYCLE (WE Controlled)



TIMING WAVEFORM OF WRITE CYCLE (CS Controlled)



TIMING WAVEFORM OF WRITE CYCLE (UB, LB Controlled)



NOTES (WRITE CYCLE)

- 1. A write occurs during the overlap (tWP) of a low \overline{CS} and low \overline{WE} . A write begins when \overline{CS} goes low and \overline{WE} goes low with asserting \overline{UB} or \overline{LB} for single byte operation or simultenious asserting \overline{UB} and \overline{LB} for double byte operation. A write ends at the earliest transition when \overline{CS} goes high and \overline{WE} goes high. The tWP is measured from the beginning of write to the end of write.
- 2. tCW is measured from the CS going low to end of write.
- 3. tAS is measured from the address valid to the beginning of write.
- 4. tWR is measured from the end or write to the address change. tWR applied in case a write ends as $\overline{\text{CS}}$ or $\overline{\text{WE}}$ going high.

FUNCTIONAL DESCRIPTION

<u>cs</u>	LB	UB	WE	ŌĒ	Mode	1/01~8	1/09~16	Current Mode
Н	Х	Х	Х	Х	Not Select	High-Z	High-Z	lsb1
L	Х	Х	Н	Н	Output Disable	High-Z	High-Z	lcc
L	Н	Н	Х	Х	Output Disable	High-Z	High-Z	Icc
L	L	Н	Н	L	Read	Dout	High-Z	
L	Н	L	Н	L	Read	High-Z	Dout	Icc
L_	L	L_	H	L	Read	Dout	Dout	
L	L	Н	L	Х	Write	Din	High-Z	1
L	H	L	L	Х	Write	High-Z	Din	lcc
L_	L	L	L	Х	Write	Din	Din	:

^{*} X means don't care (Must be in high or low states)

64Kx16 bit Super Low Power and Low Voltage Full CMOS SRAM with 48-CSP(Chip Size Package)

FEATURES

• Process Technology: 0.4 µm Full CMOS

· Organization:64Kx16

· Power Supply Voltage

KM616FS2000Z Family : $2.3V(Min) \sim 3.3V(Max)$ KM616FR2000Z Family : $1.8V(Min) \sim 2.7V(Max)$

Low Data Retention Voltage: 1.5V(Min)

. Three state output status and TTL Compatible

· Package Type: 48-CSP with 0.75mm ball pitch

GENERAL DESCRIPTION

The KM616FS1000Z and KM616FR1000Z family are fabricated by SAMSUNG's advanced Full CMOS process technology. The family can support various operating temperature ranges and has very samll from factor with 0.75 ball pitch and 6 x 8 ball array. The family also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

Product		n		Power Diss	ipation		
Family	Operating Temp.Range	Vcc Range (min~max)	Speed(ns)	Operating (Icc2)	Standby (Isa1)	PKG Type	
KM616FS1000Z	Commercial (0~70°C)	2.3~3.3V	100*@Vcc=3.0±0.3V 150*@Vcc=2.5±0.2V	80mA(Max) 50mA(Max)	5 <i>μ</i> Α (max)	48-CSP	
KM616FR1000Z	(6 75 0)	1.8~2.7V	300*@Vcc=2.0±0.2V	25mA(Max)	(IIIax)	(6x8 ball area	
KM616FS1000ZI	Industria	2.3~3.3V	100*@Vcc=3.0±0.3V 150*@Vcc=2.5±0.2V	80mA(Max) 50mA(Max)	5 <i>μ</i> Α (max)	with 0.75mm ball pitch)	
KM616FR1000ZI	1 (4.5 55 5)	1.8~2.7V	300*@Vcc=2.0±0.2V	25mA(Max)	(max)		

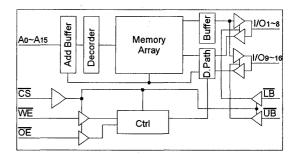
^{*} The parameter is measured with 30pF test load.

48-CSP PIN TOP VIEW

*	1	2	3	4	5	6
Α	ĹВ	ŌĒ	Ao	A1	A2	NC
В,	I/O9	UB	Аз	A4	ĊS	1/01
С	I/O10	J/O11	A5	A6	I/O ₂	I/O3
D	Vss	1/012	NC	A7	1/04	Vcc
Ε	Vcc	I/O13	NC	NC	I/O5	Vss
F	I/O15	I/O14	A14	A15	I/O6	1/07
G	I/O16	NC	A12	A13	WE	I/O8
Н	NC	Ав	A9	A10	A11	NC

^{*} See last page for package dimension.

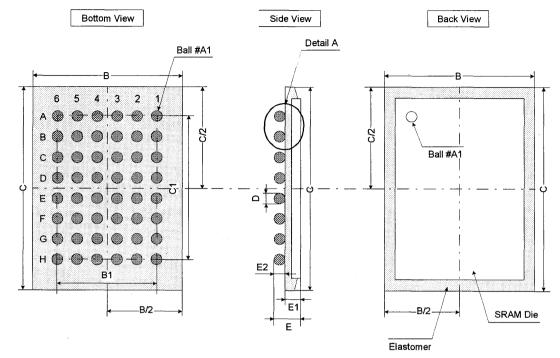
FUNCTIONAL BLOCK DIAGRAM



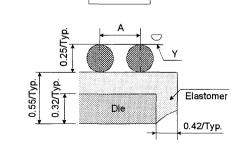
Name	Function	Name	Function
A0~A15	Address Inputs	LB.	Lower Byte(I/O1 ~ 8)
WE	Write Enable Input	ŪB	Upper Byte(I/O9~16)
CS	Chip Select Input	Vcc	Power
ŌĒ	Output Enable Input	Vss	Ground
1/01~1/016	Data Inputs/Outputs	N.C.	No Connection



PACKAGE DIMENSIONS (Units: mm)



	Min	Тур	Max
Α	-	0.75	
В	5.90	6.00	6.10
B1		3.75	-
С	7.90	8.00	8.10
C1	-	5.25	
D	0.30	0.35	0.40
E	-	0.80	0.81
E1	-	0.55	-
E2	-	0.25	-
Υ		-	0.08



Detail A

Notes.

- 1. Bump counts: 48(8row x 6row)
- 2. Bump pitch: $(x,y)=(0.75 \times 0.75)(typ.)$
- 3. All tolerence are +/-0.050 unless otherwise specified.
- 4. Typ : Typical
- 5. Y is copianarity : 0.08(max)



256Kx8 bit Super Low Power and Low Voltage Full CMOS Static RAM **FEATURES**

- Process Technology: 0.4 µm Full CMOS
- Organization: 256Kx8
- · Power Supply Voltage

KM68FV2000 Family: 3.0V(Min) ~ 3.6V(Max)

KM68FS2000 Family: 2.3V(Min) ~ 3.3V(Max) KM68FR2000 Family: 1.8V(Min) ~ 2.7V(Max)

- Low Data Retention Voltage: 1.5V(Min)
- . Three state output and TTL Compatible
- · Package Type: JEDEC Standard

32-TSOP(I)-Forward/Reverse

GENERAL DESCRIPTION

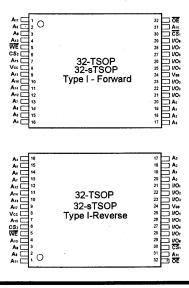
The KM68FV2000, KM68FS2000 and KM68FR2000 family are fabricated by SAMSUNG's advanced Full CMOS process technology. The family can support various operating temperature ranges and have various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

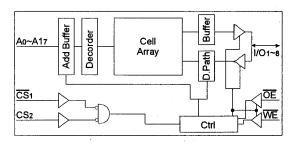
Product		Vec	لبديره	Powe	r Dissipation		
Family	Operating Temp.Range	Range	Speed (ns)	Standby (ISB1)	Operating (Icc2)	PKG Type	
KM68FV2000		3.0~3.6V	70*/85@Vcc=3.3±0.3V	2#A***	60mA(Max)]	
KM68FS2000	Commercial (0~70°C)	2.3~3.3V	85@Vcc=3.0±0.3V 120*/150@VCC=2.5±0.2V	/10 µA**	- SEmA(May)	32-TSOP(I) Forward/ Reverse	
KM68FR2000		1.8~2.7V	300*@Vcc=2.0±0.2V	(IVIAX)	15mA(Max)	7	
KM68FV2000I		3.0~3.6V	70*/85@Vcc=3.3±0.3V	0.4***	60mA(Max)		
KM68FS2000I	Industria (-40~85℃)	2.3~3.3V	85@Vcc=3.0±0.3V 120*/150@VCC=2.5±0.2V	2μΑ*** /10μΑ** (Max)	55mA(Max) 30mA(Max)	32-TSOP(I) Forward/ Reverse	
KM68FR2000I		1.8~2.7V	300*@Vcc=2.0±0.2V	(IVIGA)	15mA(Max)		

^{*} measured with 30pF test load, ** for low power version, *** for super low power version with special handling.

PIN DESCRIPTION



FUNCTIONAL BLOCK DIAGRAM



Name	Function	Namé	Function
A0~A17	Address Inputs	Vcc	Power
WE /	Write Enable Input	Vss	Ground
CS _{1,CS2}	Chip Select Input	1/01~1/08	Data Inputs/Outputs
ŌĒ	Output Enable	N.C.	No Connection



PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST FOR LOW LOW POWER CONSUMPTION

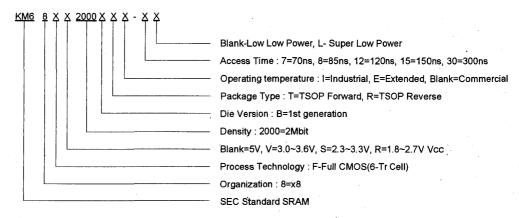
Comm	ercial Temp Product (0~70 ℃)	Industrial Temp Product (-40~85℃)			
Part Name	Function	Part Name	Function		
KM68FV2000T-7	32-TSOP F, 70ns, 3.3V, LL	KM68FV2000TI-7	32-TSOP F. 70ns. 3.3V. LL		
KM68FV2000T-8	32-TSOP F, 85ns, 3.3V, LL	KM68FV2000TI-8	32-TSOP F, 85ns, 3.3V, LL		
KM68FV2000R-7	32-TSOP R, 70ns, 3.3V, LL	KM68FV2000RI-7	32-TSOP R, 70ns, 3.3V, LL		
KM68FV2000R-8	32-TSOP R, 85ns, 3.3V, LL	KM68FV2000RI-8	32-TSOP R, 85ns, 3.3V, LL		
KM68FS2000T-12	32-TSOP F, 120/85ns, *2.5/3.0V, LL	KM68FS2000TI-12	32-TSOP F, 120/85ns, 2.5/3.0V, LL		
KM68FS2000T-15	32-TSOP F, 150/85ns, 2.5/3.0V, LL	KM68FS2000TI-15	32-TSOP F, 150/85ns, 2.5/3.0V, LL		
KM68FS2000R-12	32-TSOP R, 120/85ns, 2.5/3.0V, LL	KM68FS2000RI-12	32-TSOP R, 120/85ns, 2.5/3.0V, LL		
KM68FS2000R-15	32-TSOP R, 150/85ns, 2.5/3.0V, LL	KM68FS2000RI-15	32-TSOP R, 150/85ns, 2.5/3.0V, LL		
KM68FR2000T-30 KM68FR2000R-30	32-TSOP F, 300ns, **2.0/2.5V, LL 32-TSOP F, 300ns, 2.0/2.5V, LL	KM68FR2000TI-30 KM68FR2000RI-30	32-TSOP F, 300ns, 2.0/2.5V, LL 32-TSOP F, 300ns, 2.0/2.5V, LL		

^{*} The meaning of 2.5V/3.0V, 120/85ns is that the operating VCC is ranged from 2.3V(Min) to 3.3V(Max) with speed 120ns @2.5V ± 0.2 and 85ns @3.0V ± 0.3. This type of meaning is applied to other notations like the example

PRODUCT LIST FOR SUPER LOW POWER CONSUMPTION

The product names for super low power version has letter[L] at the end of product name of low low power version. The part name for 128Kx16 Super Low Power product operating at 2.3~3.3V with 85ns @ 3.0V and 120ns @ 2.5V will be KM68FS2000TI-12L. And if suppliment is required for those products please contact Samsung Electronics Branch near your office. Samsung will support with special treatment.

ORDERING INFORMATION



meaning is applied to other notations like the example.

** But in case of KM68FR2000T-30, there is only one speed bin, 300ns though it supports wide range operating VCC.

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	VIN,VOUT	-0.2 to 3.6V ¹⁾	V	-
Voltage on Vcc supply relative to Vss	Vcc	-0.2 to 4.0V ²⁾	V	-
Power Dissipation	Po	1.0	w	-
Storage temperature	Тѕтс	-55 to 150	°C	
Operating Temperature	Та	0 to 70	r	KM68FV2000 KM68FS2000 KM68FR2000
		-40 to 85	°	KM68FV2000I KM68FS2000I KM68FR2000I
Soldering temperature and time	TSOLDER	260 ℃, 5sec (Lead Only)	-	

^{*} Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*

Item	Symbol	Produc	ot	Min	Typ**	Max	Unit
Supply voltage	Vcc	KM68FV2000 KM68FS2000 KM68FR2000) Family	3.0 2.3 1.8	3.3 2.5/3.0 2.0/2.5	3.6 3.3 2.7	V V V
Ground	Vss	All Fam	ily ·	0	0	0	٧
Input high voltage	ViH	KM68FV2000 Family	Vcc=3.3±0.3V	2.2	-	Vcc+0.2	V
	,	KM68FS2000 Family	Vcc=3.0 ± 0.3V	2.2	-	Vcc+0.2	V
			Vcc=2.5±0.2V		j -	Vcc+0.2	V
		KM68FR2000 Family	Vcc=2.5±0.2V	2.0	-	Vcc+0.2	V
			Vcc=2.5±0.2V	1.6	-	Vcc+0.2	V
Input low voltage	VIL	All Fam	All Family		-	0.4	V

^{* 1)} Commercial Product : TA=0 to 70 °C, unless otherwise specified 2) Industrial Product : TA=-40 to 85 ℃, unless otherwise specified ** TA=25 ℃

CAPACITANCE* (f=1MHz, TA=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	Cin	Vin=0V	-	8	pF
Input/Output capacitance	Cio	Vio=0V	-	10	pF

^{*} Capacitance is sampled not 100% tested



¹⁾ VIN/VOUT=0.2 to 3.9V for KM68FV2000 Family.
2) Maximum VCC=-0.2 to 4.6V for KM68FV2000 Family.

^{***} VIL(min)=-1.5V for \(\le \) 30ns pulse width

CMOS SRAM

KM68FV2000, KM68FS2000, KM68FR2000 Family

DC AND OPERATING CHARACTERISTICS

	Item	Sym-		Test Con	ditions	j ¹⁾	Min	Typ**	Max	Unit
Input leaka	ge current	łu	VIN=	VIN=Vss to Vcc			-1	-	1	μA
Output leal	kage current	ILO		CS1=VIH or CS2=VIH or WE=VIL, VIO=Vss to Vcc		-1	-	1	μA	
Operating	Operating power supply current		CS ₁	=VIL, CS2=VIH		Read	-	-	10 ⁵⁾	mA
	· · · · · · · · · · · · · · · · · · ·	lcc	VIN=	VIH or VIL, IIO=0mA	١	Write	-	-	15 ⁵⁾	1 /11/
			Cycl	e time=1 µs 100%d	uty	Read	-	-	10 ⁵⁾	
A.v	a ratio may read	lcc1	1	CS1 ≤ 0.2V, Write CS2 ≥ VIN ≥ Vcc-2.0V		-	-	15 ⁵⁾	mA	
Average of	Average operatingcurrent		CS ₁	=VIH or CS2=VIH	Vcc=	=3.3V@85ns	554)			
		ICC2	I Min cycle 100% duty □		Vcc=2.7V@120ns		-	-	30	mA
					Vcc=	=2.2V@300ns	-	-	15	
		Vol		Vcc=2.5V		2.1mA	-		0.4	
Output low	voltage		loL			0.5mA		-	0.4	V
						0.33mA	-	-	0.4	
				Vcc=3.0/3.3V		-1.0mA	2.4	-	-	
Output high	n voltage	Vон	Іон	Vcc=2.5V	-0.5mA		2.0	-	-] v
			J	Vcc=2.0V		-0.44mA	1.6	-	-	
Standby Co	urrent(TTL)	Isa	CS ₁ :	=ViH, CS2=ViL			-	-	0.3	mA
	KM68FV2000				Supe	er Low Power	-	0.05 ³⁾	2 ²⁾	
Standby Current (CMOS)	KM68FS2000 KM68FR2000	ISB1	CS ₂	≥Vcc-2.0V ≥Vcc-2.0V or	Low Low Power		-	-	10 ²⁾	μΑ
	KM68FV2000I KM68FS2000I	1301		CS2≤0.2V Otherinput =0~Vcc		Super Low Power		0.053)	2 ²⁾	μA
	KM68FR2000I					Low Power	-	-	10 ²⁾	١٠٠٠

TA=0 to 70°C, Vcc=3.3±0.3V for 68FV2000 Family, Vcc=2.3(Min)~3.3V(Max)V for 68FS2000 Family, Vcc=1.8(Min)~2.7V(Max)V for 68FR2000 Family.

-Industrial Product: TA=-40 to 85°C, Vcc=3.3±0.3V for 68FV2000I Family, Vcc=2.3(Min)~3.3V(Max)V for 68FS2000I Family,

Vcc=1.8(Min)~2.7V(Max)V for 68FR2000I Family.

4) - The value is measured at Vcc=3.0 ± 0.3V

²⁾ The value has difference by $\pm 1\mu$ A Measured at Vcc=3.3(Max).

³⁾ The value is not 100% tested but obtained statistically at Temp=25°C

⁻ ICC2=60mA with 70ns at Vcc=3.3 ± 0.3V, but this value is not 100% tested but obtained statistically.

⁻ ICC2=30mA with 120ns cycle at Vcc= 2.5 ± 0.2 V, but this value is not 100% tested but obtained statistically. - ICC2=15mA with 300ns cycle at Vcc= 2.0 ± 0.2 V, but this value is not 100% tested but obtained statistically.

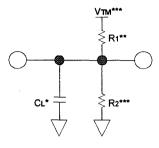
⁵⁾ The value is measured at Vcc=3.0±0.3V, The value measured at Vcc=2.5±2.0V is under the calue of Vcc=3.0±0.3V.

A.C CHARACTERISTICS

TEST CONDITIONS (1.Test Load and Test Input/Output Reference)*

Item	Value	Remark
Input pulse level	0.4 to 2.2V	Vcc=3.3V, 3.0V, 2.5V
Iliput puise level	0.4 to 1.8V	Vcc=2.0V
Input rise fall time	5ns	-
	1.5V	Vcc=3.3V, 3.0V
input and output reference voltage	1.1V	Vcc=2.5V
	0.9V	Vcc=2.0V,
Output load (See right)	CL=100pF	See Test Condition #2
Output load (See fight)	CL=30pF	Jee rest Condition #2

^{*} See DC Operating conditions



^{*} Including scope and jig capacitance **R1=3070 Ω , R2=3150 Ω

TEST CONDITIONS (2. Temperature and Vcc Conditions)

Product Family	Temperature	Vcc Range	Typical Supply Vcc	Speed	Comments
KM68FR2000	0~70℃	1.8(Min)~2.7(Max)	2.0V ± 0.2 Operation	300*ns	
VM60E63000	0-70°	2.3(Min)~3.3(Max)	2.5V ± 0.2 Operation	120*/150ns	Commercial
KM68FS2000 0~70°C	0~70 C	2.5(Mill)~5.5(Max)	3.0V ± 0.3 Operation	85ns	Commercial
KM68FV2000	0~70℃	3.0(Min)~3.6(Max)	3.3V ± 0.3 Operation	70*/85ns	
KM68FR2000I	-40~85℃	1.8(Min)~2.7(Max)	2.0V ± 0.2 Operation	300*ns	
KMESESSOOIO	-40~85℃	2.2(Min) 2.2(May)	2.5V ± 0.2 Operation	120*/150ns	Industrial
KM68FS200I0	-40~65 C	2.3(Min)~3.3(Max)	3.0V ± 0.3 Operation	85ns	moustrial
KM68FV2000I	-40~85℃	3.0(Min)~3.6(Max)	3.3V ± 0.3 Operation	70*/85ns	

^{*} All the parameters are measured with 30pF test load

^{***}VTM=2.8V for VCC=3.0/3.3V =2.3V for VCC=2.5V =1.8V for VCC=2.0V

PARAMETER LIST FOR EACH SPEED BIN

								Spee	d Bins						
	Parameter List	Symbol	70	ns .	85	ins	10	Ons	120	Ons	15	150ns		300ns	
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read	Read cycle time	tRC	70	-	85	-	100	-	120	-	150	-	300	-	ns
	Address access time	tAA	-	70	٠.	85	-	100	-	120	-	150	-	300	ns
	Chip select to output	tCO1 tCO2	-	70	-	85	-	100	•	120	-	150	-	300	ns
	Output enable to valid output	tOE	-	35	-	45	-	50	-	60	-	75	-	150	ns
	Chip select to low-Z output	tLZ1 tLZ2	10	-	10	-	10	-	10	-	20	-	50	-	ns
	Output enable to low-Z output	tOLZ	5	-	5	-	5	-	5	-	10	-	30	-	ns
	Chip disable to high-Z output	tHZ1 tHZ2	0	25	0	25	0	30	0	35	0	40	0	60	ns
	Output disable to high-Z output	tonz	0	25	0	25	0.	30	0	35	0	40	0	60	ns
	Output hold from address	toh	10	-	15	-	15	-	15	-	15	-	30	-	ns
Write	Write cycle time	twc	70	-	85	-	100	-	120	-	150	-	300	-	ns
	Chip select to end of write	tcw	65	-	70	-	80	-	100	-	120	-	300	-	ns
	Address set-up time	tAS	0	-	0	-	0	-	0	-	0	-	0	-	ns
	Address valid to end of write	tAW	65	-	70	-	80	-	100	-	120	-	300	-	ns
	Write pulse width	tWP	55	-	60	-	70	-	80	-	100	-	200	-	ns
	Write recovery time	tWR	0	-	0	-	0	-	0	-	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	25	0	25	0	30	0	35	0	40	0	60	ns
	Data to write time overlap	tDW	30	-	35	•	40	-	50	-	60	-	120	-	ns
	Data hold from write time	tDH	0	-	0	-	0	-	0	-	0	-	0	-	ns
	End write to output low-Z	tow	5	-	5	-	5	-	5	-	5	-	20	-	ns

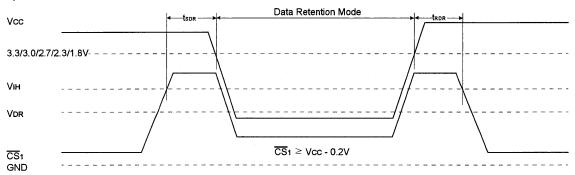
^{*} not yet available, only for reserved speed bins.

DATA RETENTION CHARACTERISTICS

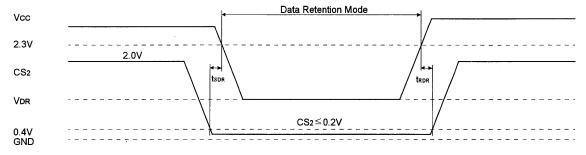
Item	Symbol	Test C	ondition*	Min	Typ**	Max	Unit
Vcc for data retention	VDR	<u>CS</u> 1****≥Vcc-2.0V		1.5	-	3.6	V
Data vatantian assurant		CS4 > 1/22 0.31/	Super Low Power	***	0.1 2.0	2.0	μА
Data retention current	IDR		Low Low Power	-	-	10	
Data retention set-up time	tsdr	See data retention waveform		0	-	-	
Recovery time	tRDR			tRC	-	-	ns

DATA RETENTION WAVE FORM

1) CS1 controlled



2) CS2 controlled



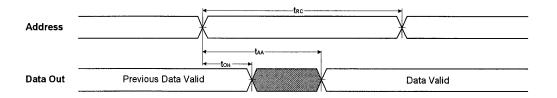


^{* 1)} Commercial Product : Ta=0 to 70 °C, unless otherwise specified 2) Industrial Product : Ta=-40 to 85 °C, unless otherwise specified ** TA=25 °C, the value is too small to detect by test machine, 0.01 µÅ statistically **** The min value is almost 0nA statistically **** CS1 ≥ Vcc-2.0V, CS2 ≥ Vcc-2.0V(CS1 controlled) or CS2 ≤ 0.2V(CS2 controlled)

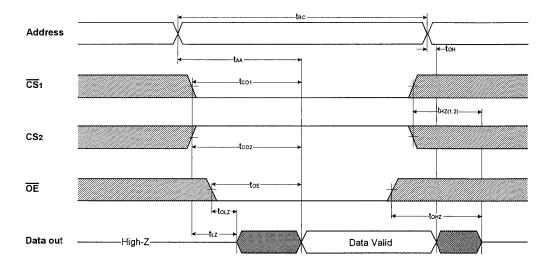
TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (1) (Address Controlled)

(CS=OE=VIL, WE=VIH)



TIMING WAVEFORM OF READ CYCLE (WE=VIH)

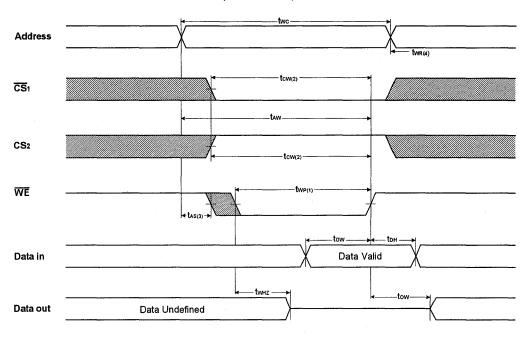


NOTES (READ CYCLE)

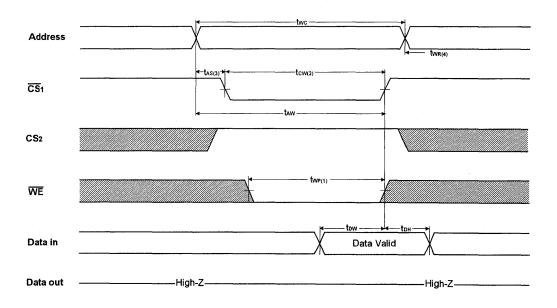
- 1. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
- 2. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device interconnection.



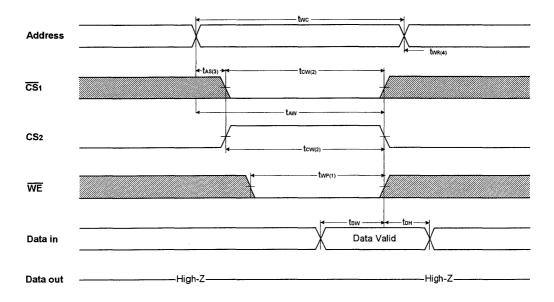
TIMING WAVEFORM OF WRITE CYCLE (WE Controlled)



TIMING WAVEFORM OF WRITE CYCLE (CS1 Controlled)



TIMING WAVEFORM OF WRITE CYCLE (CS2 Controlled)



NOTES (WRITE CYCLE)

- 1. A write occurs during the overlap of a low \overline{CS}_1 , a high CS2 and a low \overline{WE} . A write begins at the latest transition among \overline{CS}_1 goes low, CS2 going high and \overline{WE} going low: A write end at the earliest transition among \overline{CS}_1 going high, CS2 going low and \overline{WE} going high, tWP is measured from the begining of write to the end of write.
- 2. tCW is measured from the \overline{CS}_1 going low or CS_2 going high to the end of write.
- 3. tAS is measured from the address valid to the beginning of write.
- 4. tWR is measured from the end of write to the address change. tWR(1) applied in case a write ends as CS1 or WE going high tWR(2) applied in case a write ends as CS2 going to low.

FUNCTIONAL DESCRIPTION

CS ₁	CS2	WE	ŌĒ	Mode	1/0	Current Mode
Н	Х	X	Х	Power Down	High-Z	lsb1
Х	L	X	Х	Power Down	High-Z	lsb, lsb1
L	Н	Н	Н	Output Disable	High-Z	lcc
L	Н	Н	L	Read	Dout	lcc
L	Н	L	Х	Write	Din	lcc

^{*} X means don't care (Must be in high or low states)



256Kx8 bit Super Low Power and Low Voltage Full CMOS SRAM with 48-CSP(Chip Size Package)

FEATURES

• Process Technology: 0.4 µm Full CMOS

• Organization : 256Kx8

Power Supply Voltage

KM68FS2000Z Family : $2.3V(Min) \sim 3.3V(Max)$ KM68FR2000Z Family : $1.8V(Min) \sim 2.7V(Max)$

Low Data Retention Voltage: 1.5V(Min)
Three state output and TTL Compatible

• Package Type: 48-CSP with 0.75mm ball pitch

GENERAL DESCRIPTION

The KM68FS2000Z and KM68FR2000Z family are fabricated by SAMSUNG's advanced Full CMOS process technology. The family can support various operating temperature ranges and has very samll from factor with 0.75 ball pitch and 6 x 8 ball array. The family also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

n1-1		V D		Power Diss		
Product Family	Operating Temp.Range	Vcc Range (min~max)	Speed(ns)	Operating (Icc2)	Standby (Isa1)	PKG Type
KM68FS2000Z	Commercial (0~70°C)	2.3~3.3V	100*@Vcc=3.0±0.3V 150*@Vcc=2.5±0.2V	55mA(Max) 30mA(Max)	10 µÅ (max)	48-CSP
KM68FR2000Z	(0 70 0)	1.8~2.7V	300*@Vcc=2.0±0.2V	15mA(Max)	(IIIax)	(6x8 ball area
KM68FS2000ZI	Industria (-40~85℃)	2.3~3.3V	100*@Vcc=3.0±0.3V 150*@Vcc=2.5±0.2V	55mA(Max) 30mA(Max)	10 <i>μ</i> Α (max)	with 0.75mm ball pitch)
KM68FR2000ZI	(=40 000)	1.8~2.7V	300*@Vcc=2.0±0.2V	15mA(Max)	(IIIax)	

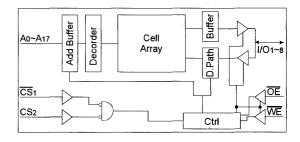
^{*} The parameter is measured with 30pF test load.

48-CSP PIN TOP VIEW

	1	2	3	4	5	6
Α	A0	A1	CS2	Аз	A6	A8
В	1/05	A2	WE	A4	A7	1/01
С	1/06		NC	A5		I/O ₂
D	Vss					Vcc
Е	Vcc					Vss
F	1/07		NC	A17		I/O3
G	1/O8	ŌĒ	CS ₁	A16	A15	1/04
Н	A9	A10	A11	A12	A13	A14

^{*} See last page for package dimension.

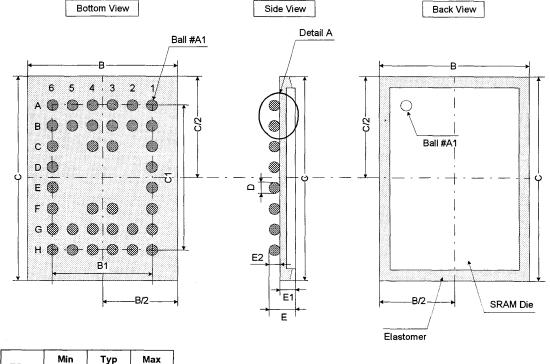
FUNCTIONAL BLOCK DIAGRAM



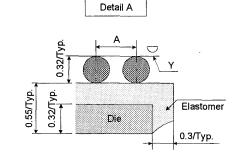
Name	Function	Name	Function
A0~A17	Address Inputs	Vcc	Power
WE	Write Enable Input	Vss	Ground
CS1,CS2	Chip Select Input	I/O1~I/O8	Data Inputs/Outputs
ŌĒ	Output Enable Input	N.C.	No Connection



KM68FS2000Z, KM68FR2000Z Family PACKAGE DIMENSIONS (Units: mm)



		Min	Тур	Max
	Α		0.75	-
	В	6.10	6.20	6.30
	B1	-	3.75	-
	С	13.65	13.75	13.85
	C1	•	5.25	-
ĺ	D	0.30	0.35	0.40
	E		0.80	0.81
	E1	-	0.55	-
	E2	-	0.25	_
	Υ	-		0.08



Notes.

- 1. Bump counts: 48(8row x 6row)
- 2. Bump pitch: $(x,y)=(0.75 \times 0.75)(typ.)$
- All tolerence are +/-0.050 unless otherwise specified.
- 4. Typ : Typical
- 5. Y is copianarity : 0.08(max)



128Kx16 bit Super Low Power and Low Voltage Full CMOS Static RAM FEATURES GENERAL DESCRIPTION

Process Technology: 0.4
 µm Full CMOS

Organization : 128Kx16Power Supply Voltage

KM616FV2000 Family: 3.0V(Min) ~ 3.6V(Max) KM616FS2000 Family: 2.3V(Min) ~ 3.3V(Max) KM616FR2000 Family: 1.8V(Min) ~ 2.7V(Max)

Low Data Retention Voltage: 1.5V(Min)

Three state output status and TTL Compatible

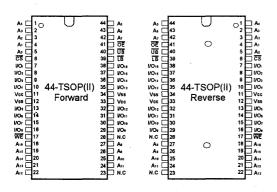
 Package Type: JEDEC Standard 44-TSOP(II)-Forward/Reverse The KM616FV2000, KM616FS2000 and KM616FR2000 family are fabricated by SAMSUNG's advanced Full CMOS process technology. The family can support various operating temperature ranges and have various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

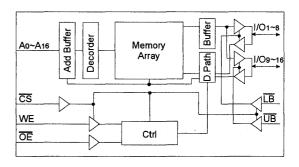
Dandon A	D		Speed		r Dissipation		
	Operating Temp.Range	- I VCC RANGE	(ns)	Standby (IsB1)	Operating (Icc2)	PKG Type	
KM616FV2000		3.0~3.6V	70*/85@Vcc=3.3±0.3V	0 4***	80mA(Max)		
KM616FS2000	Commercial (0~70°C)	2.3~3.3V	85@Vcc=3.0±0.3V 120*/150@VCC=2.5±0.2V	2μΑ*** /10μΑ** (Max)	80mA(Max) 50mA(Max)	44-TSOP(II) Forward/ Reverse	
KM616FR2000]	1.8~2.7V	300*@Vcc=2.0±0.2V	(IVIAX)	20mA(Max)		
KM616FV2000I		3.0~3.6V	70*/85@Vcc=3.3±0.3V		80mA(Max)		
KM616FS2000I	Industria (-40~85℃)	2.3~3.3V	85@Vcc=3.0±0.3V 120*/150@VCC=2.5±0.2V	2μΑ*** /10μΑ** (Max)	80mA(Max) 50mA(Max)	44-TSOP(II) Forward/ Revers	
KM616FR2000I	1	1.8~2.7V	300*@Vcc=2.0±0.2V	(IVIAA)	20mA(Max)		

^{*} measured with 30pF test load, ** for low power version, *** for super low power version with special handling.

PIN DESCRIPTION



FUNCTIONAL BLOCK DIAGRAM



Name	Function	Name	Function
A0~A16	Address Inputs	LB	Lower Byte(I/O1~8)
WE	Write Enable Input	ŪB	Upper Byte(I/O9~16)
ĊŚ	Chip Select Input	Vcc	Power
ŌĒ	Output Enable	Vss	Ground
1/01~1/016	Data Inputs/Out-	N.C.	No Connection



KM616FV2000, KM616FS2000, KM616FR2000 Family

PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST FOR LOW LOW POWER CONSUMPTION

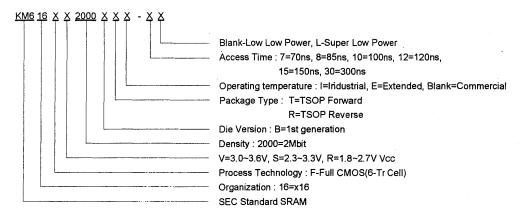
Comme	ercial Temp Product (0~70°C)	Industrial Temp Product (-40~85℃)			
Part Name	Function	Part Name	Function		
KM616FV2000T-7	44-TSOP F, 70ns, 3.3V, LL	KM616FV2000TI-7	44-TSOP F, 70ns, 3.3V, LL		
KM616FV2000T-8	44-TSOP F, 85ns, 3.3V, LL	KM616FV2000TI-8	44-TSOP F, 85ns, 3.3V, LL		
KM616FV2000R-7	44-TSOP R, 70ns, 3.3V, LL	KM616FV2000RI-7	44-TSOP R, 70ns, 3.3V, LL		
KM616FV2000R-8	44-TSOP R, 85ns, 3.3V, LL	KM616FV2000RI-8	44-TSOP R, 85ns, 3.3V, LL		
KM616FS2000T-12	44-TSOP F, 120/85ns, *2.5/3.0V, LL	KM616FS2000TI-12	44-TSOP F, 120/85ns, 2.5/3.0V, LL		
KM616FS2000T-15	44-TSOP F, 150/85ns, 2.5/3.0V, LL	KM616FS2000TI-15	44-TSOP F, 150/85ns, 2.5/3.0V, LL		
KM616FS2000R-12	44-TSOP R, 120/85ns, 2.5/3.0V, LL	KM616FS2000RI-12	44-TSOP R, 120/85ns, 2.5/3.0V, LL		
KM616FS2000R-15	44-TSOP R, 150/85ns, 2.5/3.0V, LL	KM616FS2000RI-15	44-TSOP R, 150/85ns, 2.5/3.0V, LL		
KM616FR2000T-30 KM616FR2000R-30	44-TSOP F, 300ns, **2.0/2.5V, LL 44-TSOP F, 300ns, 2.0/2.5V, LL	KM616FR2000TI-30 KM616FR2000RI-30	44-TSOP F, 300ns, 2.0/2.5V, LL 44-TSOP F, 300ns, 2.0/2.5V, LL		

^{*} The meaning of 2.5V/3.0V, 120/85ns is that the operating VCC is ranged from 2.3V(Min) to 3.3V(Max) with speed 120ns @2.5V ± 0.2 and 85ns @3.0V ± 0.3. This type of meaning is applied to other notations like the example.

PRODUCT LIST FOR SUPER LOW POWER CONSUMPTION

The product names for super low power version has letter[L] at the end of product name of low low power version. The part name for 128Kx16 Super Low Power product operating at 2.3~3.3V with 85ns @ 3.0V and 120ns @ 2.5V will be KM616FA2000TI-12L. And if suppliment is required for those products please contact Samsung Electronics Branch near your office. Samsung will support with special treatment.

ORDERING INFORMATION





^{**} But in case of KM616FR2000T-30, there is only one speed bin, 300ns though it supports wide range operating VCC.

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	VIN, VOUT	-0.2 to 3.6V ¹⁾	v	-
Voltage on Vcc supply relative to Vss	Vcc	-0.2 to 4.0V ²⁾	V	-
Power Dissipation	Pb	1.0	w	-
Storage temperature	Тѕтс	-55 to 150	°C	-
Operating Townsysters	TA	0 to 70	°	KM616FV2000 KM616FS2000 KM616FR2000
Operating Temperature	IA	-40 to 85	c	KM616FV2000I KM616FS2000I KM616FR2000I
Soldering temperature and time	TSOLDER	260℃, 5sec (Lead Only)	-	-

^{*} Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*

Item	Symbol	Produc	at	Min	Typ**	Max	Unit
Supply voltage	Vcc	KM616FV2000 KM616FS2000 KM616FR2000	3.0 2.3 1.8	3.3 2.5/3.0 2.0/2.5	3.6 3.3 2.7	V V	
Ground	Vss	All Family		0	0	0	V
		KM616FV2000 Family	Vcc=3.3±0.3V	2.2	-	Vcc+0.2	V
		KM616FS2000 Family	Vcc=3.0 ± 0.3V	2.2	-	Vcc+0.2	V
Input high voltage	ViH	KINIO 10F32000 Family	Vcc=2.5 ± 0.2V	2.0	-	Vcc+0.2	V
		KM616FR2000 Family	Vcc=2.5 ± 0.2V	2.0	-	Vcc+0.2	· V
			Vcc=2.5 ± 0.2V	1.6	-	Vcc+0.2	V
Input low voltage	VIL	All Fami	-0.2***	-	0.4	V	

^{* 1)} Commercial Product : Ta=0 to 70°C, unless otherwise specified 2) Industrial Product : Ta=-40 to 85°C, unless otherwise specified

CAPACITANCE* (f=1MHz, Ta=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	Cin	Vin=0V	-	8	pF
Input/Output capacitance	Cio	Vio=0V	-	10	pF

^{*} Capacitance is sampled not 100% tested



¹⁾ VIN/Vout=0.2 to 3.9V for KM616FV2000 Family.

²⁾ Maximum Vcc=-0.2 to 4.6V for KM616FV2000 Family.

^{**} TA=25°C

^{***} $V_{IL}(min)$ =-1.5V for \leq 30ns pulse width

KM616FV2000, KM616FS2000, KM616FR2000 Family

DC AND OPERATING CHARACTERISTICS

	Item	Sym-		Test Cond	litions	1)	Min	Typ**	Max	Unit	
· Input leaka	ge current	lLI	VIN=	Vss to Vcc			-1	-	1	μA	
Output leak	age current	ILO	cs =	VIH or WE=VIL,		7.	-1	-	1	μA	
Operating p	power supply current	Icc		CS=VIL Read			-	-	10 ⁵⁾	mA	
·		100	VIN=	VIH or VIL, IIO=0mA	١.	Write	-	-	20 ⁵⁾] '''^	
			Cycl	e time=1 µs 100%di	uty	Read	-	-	10 ⁵⁾	mA	
		Icc1	ੋਂ ਫੋਂ ਫੋਂ ਫੋਂ	0.2V		Write	-	-	20 ⁵⁾	11112	
Average op	eratingcurrent				Vcc=	3.3V@85ns	-	-	804)		
				CS=VIH, IIO=0mA Min cycle, 100% duty		2.7V@120ns	-	-	60	mA	
			• • • • • • • • • • • • • • • • • • • •		Vcc=	=2.2V@300ns	-	-	25		
				Vcc=3.0/3.3V		2.1mA	-	-	0.4		
Output low	voltage	Vol	loL	Vcc=2.5V		0.5mA	-	-	0.4	V	
			Vcc=2.0V			0.33mA	-	-	0.4]	
				Vcc=3.0/3.3V		-1.0mA	2.4	-	-		
Output high	voltage	Vон	Юн	Vcc=2.5V		-0.5mA	2.0	-	-	v	
			!	Vcc=2.0V		-0.44mA	1.6	-	-		
Standby Cu	rrent(TTL)	ISB	CS =	ViH			-	-	0.3	mA	
	KM616FV1000				Supe	er Low Power	-	0.053)	2 ²⁾	μA	
Standby KM616FR1000			cs ≥	:Vcc-2.0V	Low	Low Low Power		-	52)	μη	
Current (CMOS)	KM616FV1000 KM616FS1000	ISB1	Othe	rinput =0~Vcc	Super Low Power		-	0.053)	2 ²⁾	- μΑ	
	KM616FR1000					Low Power	-	-	5 ²⁾		

1) -Commercial Product

Ta=0 to 70 °C, Vcc=3.3 ± 0.3V for 616FV2000 Family, Vcc=2.3(Min)~3.3V(Max)V for 616FS2000 Family,

Vcc=1.8(Min)~2.7V(Max)V for 616FR2000 Family.
-Industrial Product: Τλ=-40 to 85 °C, Vcc=3.3±0.3V for 616FV2000I Family, Vcc=2.3(Min)~3.3V(Max)V for 616FS2000I Family, Vcc=1.8(Min)~2.7V(Max)V for 616FR2000I Family.

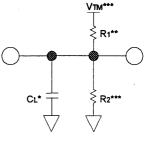
- 2) The value has difference by $\pm 1\mu\text{\AA}$
 - Measured at Vcc=3.3(Max).
- 3) The value is not 100% tested but obtained statistically at Temp=25 $\ensuremath{\mathbb{C}}$
- 4) The value is measured at Vcc=3.0±0.3V
 - lcc_2 =70mA with 70ns at Vcc=3.3 \pm 0.3V, but this value is not 100% tested but obtained statistically.
 - lcc2=40mA with 100ns cycle at Vcc=2.5 \pm 0.2V, but this value is not 100% tested but obtained statistically.
 - lcc2=20mA with 150ns cycle at Vcc=2.0±0.2V, but this value is not 100% tested but obtained statistically.
- 5) The value is measured at Vcc=3.0±0.3V, The value measured at Vcc=2.5±2.0V is under the calue of Vcc=3.0±0.3V.

A.C CHARACTERISTICS

TEST CONDITIONS (1.Test Load and Test Input/Output Reference)*

Item	Value	Remark
input pulse level	0.4 to 2.2V	Vcc=3.3V, 3.0V, 2.5V
input puise level	0.4 to 1.8V	Vcc=2.0V
Input rise fall time	5ns	-
	1.5V	Vcc=3.3V, 3.0V
input and output reference voltage	1.1V	Vcc=2.5V
	0.9V	Vcc=2.0V,
Output load (See right)	CL=100pF	See Test Condition #2
Output load (See right)	CL=30pF	See rest condition #2

^{*} See DC Operating conditions



^{*} Including scope and jig capacitance **R1=3070 Ω , R2=3150 Ω

TEST CONDITIONS (2. Temperature and Vcc Conditions)

Product Family	Temperature	Vcc Range	Typical Supply Vcc	Speed	Comments
KM616FR2000	0~70℃	1.8(Min)~2.7(Max)	2.0V ± 0.2 Operation	300*ns	
KM616FS2000	0~70℃	2.3(Min)~3.3(Max)	2.5V ± 0.2 Operation	120*/150ns	Commercial
KIVIO 10F52000	0~70 C	2.3(MIII)~3.3(Max)	3.0V ± 0.3 Operation	85ns	Commercial
KM616FV2000	0~70℃	3.0(Min)~3.6(Max)	3.3V ± 0.3 Operation	70*/85ns	
KM616FR2000I	-40~85℃	1.8(Min)~2.7(Max)	2.0V ± 0.2 Operation	300*ns	
IAMACA CE CODOLO	-40~85℃	2.2(Min), 2.2(Man)	2.5V ± 0.2 Operation	120*/150ns	144
KM616FS200I0	-40~85 C	2.3(Min)~3.3(Max)	3.0V ± 0.3 Operation	85ns	Industrial
KM616FV2000I	-40~85℃	3.0(Min)~3.6(Max)	3.3V ± 0.3 Operation	70*/85ns	1

^{*} All the parameters are measured with 30pF test load



^{***}VTM=2.8V for VCC=3.0/3.3V =2.3V for VCC=2.5V =1.8V for VCC=2.0V

KM616FV2000, KM616FS2000, KM616FR2000 Family

PARAMETER LIST FOR EACH SPEED BIN

								Spee	d Bins						
	Parameter List	Symbol	70)ns	85	ins	10	Ons	12	Ons	15	Ons	30	Ons	Units
			Min	Max	Min	Max	Min	Мах	Min	Max	Min	Max	Min	Max	
Read	Read cycle time	tRC	70	-	85	-	100	-	120	-	150	-	300	-	ns
	Address access time	tAA	-	70	-	85	-	100	-	120	-	150	-	300	ns
	Chip select to output	tCO1 tCO2	-	70	-	85	-	100	-	120	-	150	-	300	ns
	Output enable to valid output	tOE	-	35	-	45	-	50	-	60	-	75	-	150	ns
	UB, LB Access Time	tBA	-	35	-	45	-	50	-	60	-	75	-	150	ns
	Chip select to low-Z output	tLZ1 tLZ2	10	-	10	-	10	-	20	-	20	-	50	-	ns
	Output enable to low-Z output	tOLZ tBLZ	5	-	5	-	5	-	20	-	20	-	30	-	ns
	Chip disable to high-Z output	tHZ1 tHZ2	0	25	0	25	0	30	0	35	0	40	0	60	ns
	Output disable to high-Z output	tOHZ tBHZ	0	25	0	25	0	30	0	35	0	40	0	60	üs
	Output hold from address	ton	10	-	15	-	15	-	15	-	15	-	30	-	ns
Write	Write cycle time	twc	70	-	85	-	100	-	120	-	150	-	300	-	ns
	Chip select to end of write	tcw	60	-	70	-	80	-	100	-	120	-	300	-	ns
	Address set-up time	tAS	0	-	0	-	0	•	0	-	0	-	0	-	ns
	Address valid to end of write	tAW	65	-	70	-	80		100	-	120	-	300	-	ns
	Write pulse width	tWP	55	-	60	-	70		80	-	100	-	200	-	ns
	UB, LB Valid to End of Write	tBW	65	-	70	-	80	-	100	-	120	-	300	-	ns
	Write recovery time	twR	0 .	-	0	-	0	-	0	-	0	-	0		ns
	Write to output high-Z	tWHZ	0	25	0	25	0	30	0	35	0	40	0	60	ns
	Data to write time overlap	tDW	30	-	35	-	40		50	•	60	-	120	-	ns
	Data hold from write time	tDH	0	-	0	-	0	-	0	-	0	-	0	-	ns
	End write to output low-Z	tow	5	-	5	-	5	-	5	-	5	-	20	-	ns

^{*} not yet available, only for reserved speed bins.

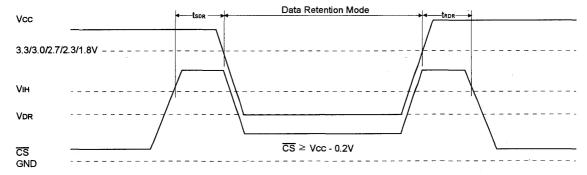
DATA RETENTION CHARACTERISTICS

Item	Symbol	Test 0	Condition*	Min	Typ**	Max	Unit	
Vcc for data retention	VDR	CS ≥Vcc-2.0V		1.5	-	3.6	٧	
Data retention current	IDR	Vcc=3.0V	Super Low Power	***	**	2.0		
		CS≥Vcc-0.2V	Low Low Power	-	-	5.0	μA	
Data retention set-up time	tsdr	See data retentio	0	-	-	ns		
Recovery time	tRDR	waveform	tRC	-	-	115		

^{* 1)} Commercial Product : Ta=0 to 70 °C, unless otherwise specified 2) Industrial Product : Ta=-40 to 85 °C, unless otherwise specified

DATA RETENTION WAVE FORM

(CS controlled)





^{**} Ta=25 °C, the value is too small to detect by test machine, 0.01 $\mu \text{\AA}$ statistically

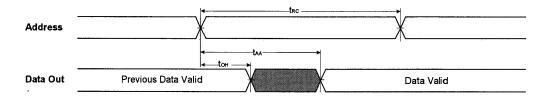
^{***} The min value is almost 0nA statistically

KM616FV2000, KM616FS2000, KM616FR2000 Family

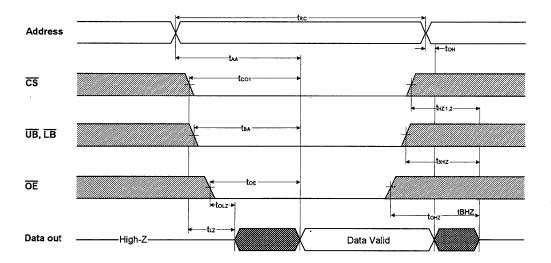
TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled)

(CS=OE=VIL, WE=VIH, UB or, and LB=VIL)



TIMING WAVEFORM OF READ CYCLE(2) (WE=VIH)

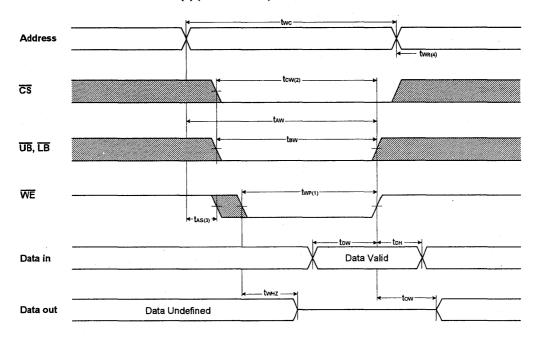


NOTES (READ CYCLE)

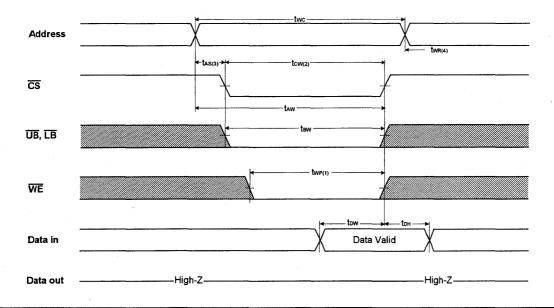
- 1. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
- 2. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device interconnection.



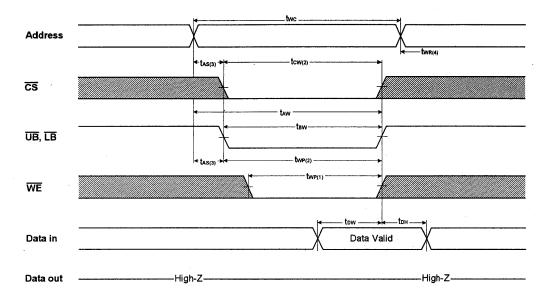
TIMING WAVEFORM OF WRITE CYCLE(1) (WE Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) (CS Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) (UB, LB Controlled)



NOTES (WRITE CYCLE)

- 1. A write occurs during the overlap(tWP) of a low \overline{CS} and low \overline{WE} . A write begins when \overline{CS} goes low and \overline{WE} goes low with asserting \overline{UB} or \overline{LB} for single byte operation or simultenious asserting \overline{UB} and \overline{LB} for double byte operation. A write ends at the earliest transition when \overline{CS} goes high and \overline{WE} goes high. The tWP is measured from the beginning of write to the end of write.
- 2. tCW is measured from the CS going low to end of write.
- 3. ${\sf tAS}$ is measured from the address valid to the beginning of write.
- 4. tWR is measured from the end or write to the address change. tWR applied in case a write ends as CS or WE going high.

FUNCTIONAL DESCRIPTION

CS	LB	ŪB	WE	ŌĒ	Mode	I/O1~8	1/09~16	Current Mode
Н	Х	Х	Х	Х	Not Select	High-Z	High-Z	ISB1
L	Х	Х	Н	Н	Output Disable	High-Z	High-Z	lcc
L	Н	Н	Х	Х	Odtput Disable	High-Z	High-Z	100
L	L	Н	Н	L		Dout	High-Z	
L	Н	L	Н	L	Read	High-Z	Dout	lcc
L	L	L	Н	L		Dout	Dout	
L	L	Н	L	Х		Din	High-Z	
L	Н	L	L	Х	Write	High-Z	Din	lcc
L	L	L	L	Х		Din	Din	

^{*} X means don't care (Must be in high or low states)



128Kx16bit Super Low Power and Low Voltage Full CMOS SRAM with 48-CSP(Chip Size Package)

FEATURES

Process Technology: 0.4
 pm Full CMOS

• Organization :128Kx16

Power Supply Voltage

KM616FS2000Z Family : $2.3V(Min) \sim 3.3V(Max)$ KM616FR2000Z Family : $1.8V(Min) \sim 2.7V(Max)$

. Low Data Retention Voltage: 1.5V(Min)

. Three state output status and TTL Compatible

• Package Type: 48-CSP with 0.75mm ball pitch

GENERAL DESCRIPTION

The KM616FS2000Z and KM616FR2000Z family are fabricated by SAMSUNG's advanced Full CMOS process technology. The family can support various operating temperature ranges and has very samll from factor with 0.75 ball pitch and 6 x 8 ball array. The family also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

Budget	Opposition Von Benne			Power Diss			
Product Family	Operating Temp.Range	Vcc Range (min~max)	Speed(ns)	Operating (Icc2)	Standby (IsB1)	PKG Type	
KM616FS2000Z	Commercial (0~70°C)	2.3~3.3V	100*@Vcc=3.0±0.3V 150*@Vcc=2.5±0.2V	80mA(Max) 50mA(Max)	10 µÅ (max)	48-CSP	
KM616FR2000Z	(0 70 0)	1.8~2.7V	300*@Vcc=2.0±0.2V	25mA(Max)	(IIIax)	(6x8 ball area	
KM616FS2000ZI	Industria (-40~85℃)	2.3~3.3V	100*@Vcc=3.0±0.3V 150*@Vcc=2.5±0.2V	80mA(Max) 50mA(Max)	10 µA (max)	with 0.75mm ball pitch)	
KM616FR2000ZI	1 (.5 55 5)	1.8~2.7V	300*@Vcc=2.0±0.2V	25mA(Max)	(max)		

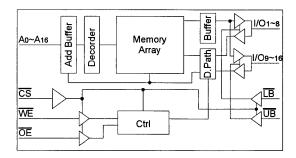
^{*} The parameter is measured with 30pF test load.

48-CSP PIN TOP VIEW

	1	2	3	4	5	6
Α	LΒ	ŌĒ	Ao	A1	A2	NC
В	1/09	ŪB	Аз	A4	cs	1/01
С	I/O10	1/011	A5	A6	I/O ₂	I/O3
D	Vss	i/O12	NC -	A7	1/04	Vcc
Ε	Vcc	I/O13	NC	A16	I/O5	Vss
F	I/O15	I/O14	A14	A15	I/O6	1/07
G	I/O16	NC	A12	A13	WE	1/08
Н	NC	A8	Аэ	A10	A11	NC

^{*} See last page for package dimension.

FUNCTIONAL BLOCK DIAGRAM

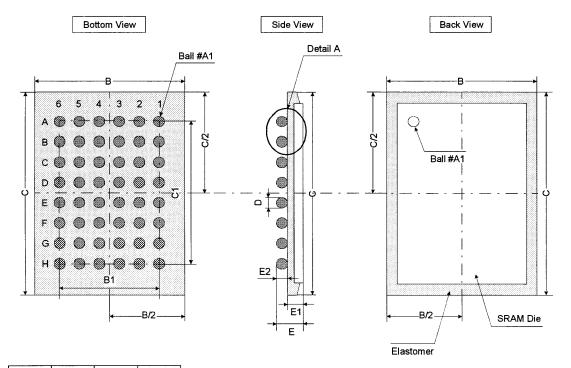


Name	Function	Name	Function
A0~A16	Address Inputs	<u>ГВ</u>	Lower Byte(I/O1 ~ 8)
WE	Write Enable Input	ŪB	Upper Byte(I/O9 ~ 16)
CS	Chip Select Input	Vcc	Power
ŌĒ	Output Enable Input	Vss	Ground
1/01~1/016	Data Inputs/Outputs	N.C.	No Connection

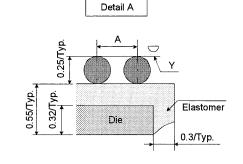


KM616FS2000Z, KM616FR2000Z Family

PACKAGE DIMENSIONS (Units: mm)



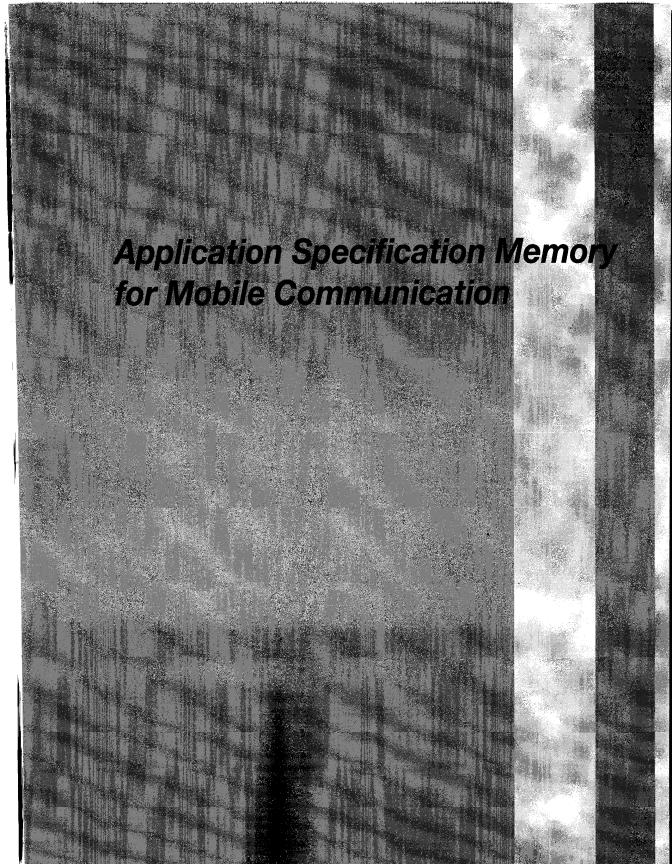
	Min	Тур	Max
Α	-	0.75	-
В	6.10	6.20	6.30
B1	-	3.75	-
С	C 13.65 13.7		13.85
C1	-	5.25	-
D	0.30	0.35	0.40
E	-	0.80	0.81
E1	-	0.55	-
E2	-	0.25	-
Υ	-	-	0.08



Notes.

- 1. Bump counts: 48(8row x 6row)
- 2. Bump pitch : $(x,y)=(0.75 \times 0.75)(typ.)$
- All tolerence are +/-0.050 unless otherwise specified.
- 4. Typ : Typical
- 5. Y is copianarity: 0.08(max)





Integrated 256K x 8 bit MaskROM with 128K x 8 bit SRAM

FEATURES

Process Technology: 0.4 µm Full CMOS
Both ROM and RAM in one chip

 Organization : 256Kx8(ROM), 128K x 8(SRAM)

Power Supply Voltage

KM88FS87 Family : 2.3V(Min) ~ 2.7V(Max) KM88FR87 Family : 1.8V(Min) ~ 2.2V(Max)

• Low Data Retention Voltage : 1.5V(Min)

. Three state output status and TTL Compatible

Package Type: 32-TSOP1 - Forward

32-sTSOP I - Forward

GENERAL DESCRIPTION

The KM88FS87 is fabricated by SAMSUNG's advanced Full CMOS process technology. The family is a combination chip consist of 2Mbit ROM organized as 256K words by 8bits and 1Mbit SRAM organized as 128K words by 8bits.

The family can support various operating temperature ranges and super low voltage operation. The family also support low data retention voltage for battery back-up operations with low data retention current.

PRODUCT FAMILY

Product	Q		S		Power Dissipation		
Family	Operating Temp.Range Vcc Range Speed (ns)* Commercial (0~70°C) 2.3~2.7V 250/500 1.8~2.2V 250/500		PKG Type	Standby (Iss1, Max)	Operating (Icc2)		
KM88FS87	Commercial	2.3~2.7V	250/500			7/5mA	
KM88FR87	(0~70℃)	1.8~2.2V	250/500	32-TSOP I 32-sTSOP I	5 <i>µ</i> A	4/3mA	
KM88FS87I	Industria	2.3~2.7V	250/500	Forward	5#4	7/5mA	
KM88FR87I	(-40~85℃)	1.8~2.2V	250/500			4/3mA	

^{*} measured with 30pF test load

PIN DESCRIPTION

SMA16 11 SMA12 12 SMA7 13 SMA6 14 SMA6 15	32-TSOP(I)- Forward 32-sTSOP(I)- Forward	32
SMA. 16		17 SMA

Name	Function	1/0
SMA0~16	Addresses for ROM & SRAM array	I
MA17	MSB address for only ROM	1
SCE	SRAM array select	Ī
MCE	ROM array select	1
WE	SRAM Write Enable	1
G	Output Enable	ı
I/O1~8	Inputs & Output signals	1/0

^{*} MA17 is used only for ROM

ADDRESS SCRAMBLE

	LSB MSB	
SRAM	SMA0, SMA16	
ROM	SMA0, SMA16, MA17*	

^{*} MA17 is not used for 128Kx8 RAM

KEY APPLICATION

Alpha-numeric pager, CT2, Cellular phone, POS, PDA, Electronic Data Bank, etc.



256K High Speed SRAM (5.0V Operation)

64K x 4 Bit High-Speed BiCMOS Static RAM

FEATURES

- Fast Access Time 6, 7, 8, ns (Max.)
- · Low Power Dissipation

Standby (TTL) : 90mA(Max.)

(CMOS): 20mA(Max.)

Operating Current :160mA(f=100MHz)

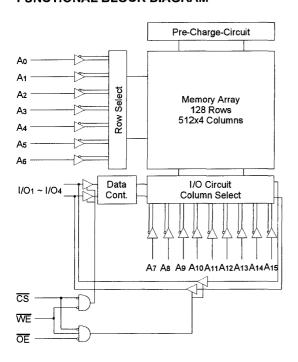
- Single 5.0V ± 5% Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
 No Clock or Refresh required
- No Clock of Refresh requ
- Three State Outputs
- · Center Power/Ground Pin Configuration
- · Standard Pin Configuration

KM64B261AJ: 28-SOJ-300

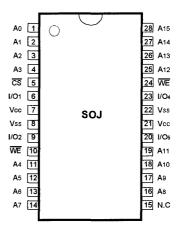
GENERAL DESCRIPTION

The KM64B261A is a 262,144-bit high-speed Static Random Access Memory organized as 65,536 words by 4 bits. The KM64B261A uses four common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using SAMSUNG's advanced BiCMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM64B261A is packaged in a 300 mil 28-pin plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION(Top View)



PIN FUNCTION

Pin Name	Pin Function
A0 - A15	Address Inputs
WE	Write Enable
CS	Chip Select
ŌĒ	Output Enable
I/O1 ~ I/O4	Data Inputs/Outputs
Vcc	Power(5.0V)
Vss	Ground
N.C	No Connection



ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	Vin, Vout	-0.5 to 7.0	
Voltage on Vcc Supply Relative to Vss	Vcc	-0.5 to 7.0	V
Power Dissipation	PD	1.0	W
Storage Temperature	Тѕтс	-65 to 150	Ĉ
Operating Temperature	TA	0 to 70	°C

^{*} Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (TA = 0 to 70°C)

Parameter	Symbol	Min	Тур	Max	Unit
Supply Voltage	Vcc	4.75	5.0	5.25	V
Ground	Vss	0	0	0	V
Input Low Voltage	ViH	2.2	-	Vcc + 0.5**	V
Input Low Voltage	VIL	-0.5*	-	0.8	V

^{*} VIL(Min) = -2.0(Pulse Width≤3ns) for 1 ≤ 20mA

DC AND OPERATING CHARACTERISTICS(TA = 0 to 70 °C, Vcc= 5.0V ± 10%, unless otherwise specified)

Parameter	Parameter Symbol		Min	Max	Unit	
Input Leakage Current	lu	Vin = Vss to Vcc	-10	10	μA	
Output Leakage Current	tput Leakage Current ILO CS=VIH or OE=VIH or WE=VIL VOUT = Vss to Vcc		-10	10	- μΑ	
Operating Current	lcc	f=100MHz, 100% Duty CS=VIL, VIN = VIH or VIL, IOUT=0mA	-	160	mA	
Standby Current	ISB	Min. Cycle, CS=VIH	-	90	mA	
	ISB1	f=0MHz, $\overline{CS} \ge Vcc-0.2V$, Vin $\ge Vcc-0.2V$ or Vin $\le 0.2V$	-	20	mA	
Output Low Voltage Level	Vol	loL=8mA	-	0.4	V	
Output High Voltage Level	Voн	IOH=-4mA	2.4	-	V	

CAPACITANCE*(TA = 25°C, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	CI/O	VI/o=0V	-	7	pF
Input Capacitance	CIN	Vin=0V	-	7	pF

^{*} NOTE: Capacitance is sampled and not 100% tested.

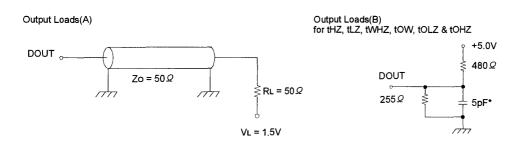


^{**} VIH(Max) = Vcc + 2.0V(Pulse Width≤8ns) for I ≤ 20mÅ

AC CHARACTERISTICS(TA = 0 to 70 $^{\circ}$ C, Vcc = 5.0V $^{\pm}$ 5%, unless otherwise noted.)

TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below



* Including Scope and Jig Capacitance

READ CYCLE

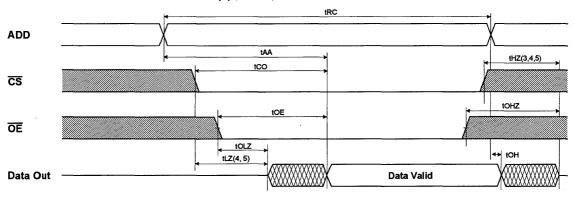
Parameter	Symbol KM64B261A-6		KM64B261A-7		KM64B261A-8		- Unit	
Parameter	Sylfidol	Min	Max	Min	Max	Min	Max	Onit
Read Cycle Time	tRC	6	-	7	-	8	-	ns
Address Access Time	tAA	-	6	-	7	-	8	ns
Chip Select to Output	tCO	-	6	-	7	-	8	ns
Output Enable to Valid Output	tOE	-	4	-	4	-	4	ns
Chip Enable to Low-Z Output Access Time	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	1	-	1	-	1	-	ns
Chip Disable to High-Z Output	tHZ	0	3	0	3.5	0	4	ns
Output Disable to High-Z Output	tOHZ	0	3	0	3.5	0	4	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns

WRITE CYCLE

Parameter	Symbol	KM64B261A-6		KM64B261A-7		KM64B261A-8		
		Min	Max	Min	Max	Min	Max	Unit
Write Cycle Time	tWC	6	-	7	-	8		ns
Chip Select to End of Write	tCW	6	-	7	-	8	-	ns
Address Setup Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	3.5	-	4	-	4.5	-	пѕ
Write Pulse Width(OE High)	·tWP	3.5	-	4	-	4.5	-	ns
Write Pulse Width(OE Low)	tWP1 '	6	-	7	-	8	-	ns
Write Recovery Time	tWR	1	-	1	-	1	-	ns
Write to Output High-Z	tWHZ	0	3	0	3.5	0	4	ns
Data to Write Time Overlap	tDW	3	-	3.5	-	4	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

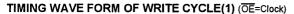
TIMING DIAGRAMS

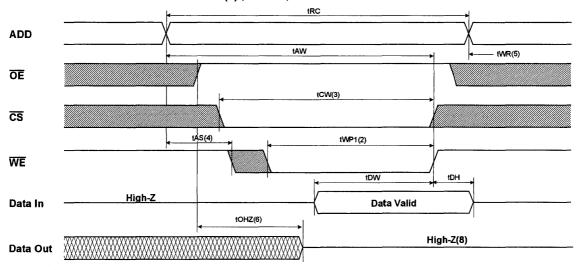
TIMING WAVE FORM OF READ CYCLE(2) (WE=VIH)



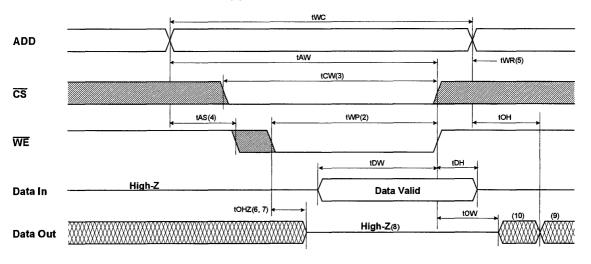
NOTES(READ CYCLE)

- 1. WE is high for read cycle.
- 2. All read cycle timing is referenced from the last valid address to the first transition address.
- 3 tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VoH or VoL Levels.
- 4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
- 5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
- 6. Device is continuously selected with CS=VIL.
- 7. Address valid prior to coincident with CS transition low.
- 8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

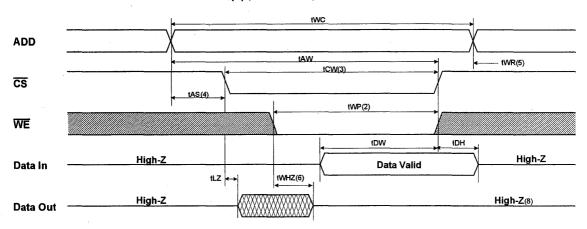




TIMING WAVE FORM OF WRITE CYCLE(2) (OE=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) (CS=Controlled)



NOTES(WRITE CYCLE)

- 1. All write cycle timing is referenced from the last valid address to the first transition address.
- 2. A write occurs during the overlap of a low $\overline{\text{CS}}$ and $\overline{\text{WE}}$. A write begins at the latest transition $\overline{\text{CS}}$ going low and $\overline{\text{WE}}$ going low; A write ends at the earliest transition $\overline{\text{CS}}$ going high or $\overline{\text{WE}}$ going high. tWP is measured from the beginning of write to the end of write.
- 3. tCW is measured from the later of CS going low to end of write.
- 4. tAS is measured from the address valid to the beginning of write.
- 5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as $\overline{\text{CS}}$ or $\overline{\text{WE}}$ going high.
- 6. If \overline{OE} , \overline{CS} and \overline{WE} are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
- 7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
- 8. If \overline{CS} goes low simultaneously with \overline{WE} going or after \overline{WE} going low, the outputs remain high impedance state.
- 9. Dout is the read data of the new address.
- 10. When CS is low: I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

ĊŚ	WE	ŌĒ	Mode	I/O Pin	Supply Current
Н	Х	X*	Not Select	High-Z	ISB, ISB1
L	H	Н	Output Disable	High-Z	lcc
L	Н	L	Read	Dout	lcc
L	L	Х	Write	Din	lcc

^{*} NOTE : X means Don't Care.



64K x 4 Bit High-Speed CMOS Static RAM

FEATURES

- Fast Access Time 12, 15, 20 ns (Max.)
- · Low Power Dissipation

Standby (TTL) : 40mÅ(Max.) (CMOS): 2mÅ(Max.)

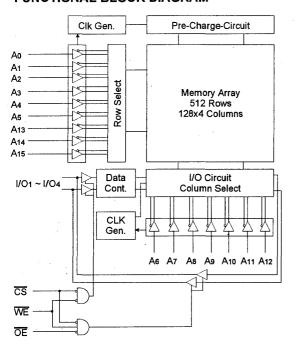
Operating KM64258C - 12 : 150mA(Max.)

KM64258C - 15: 140mA(Max.) KM64258C - 20: 130mA(Max.)

- Single 5.0V ± 10% Power Supply
- . TTL Compatible Inputs and Outputs
- . I/O Compatible With 3.3V Device
- Fully Static Operation
 - No Clock or Refresh required
- . Three State Outputs
- . Standard Pin Configuration

KM64258CP : 28-DIP-300 KM64258CJ : 28-SQJ-300

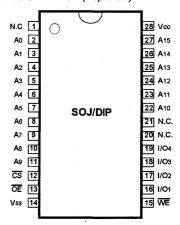
FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The KM64258C is a 262,144-bit high-speed Static Random Access Memory organized as 65,536 words by 4 bits. The KM64258C uses 4 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM64258C is packaged in a 300 mil 28-pin plastic DIP or SOJ.

PIN CONFIGURATION(Top View)



PIN FUNCTION

Pin Name	Pin Function					
A0 - A15	Address Inputs					
WE	Write Enable					
CS	Chip Select					
ŌĒ	Output Enable					
1/01 ~ 1/04	Data Inputs/Outputs					
Vcc	Power(+5.0V)					
Vss	Ground					
N.C	No Connection					



ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	Vin, Vout	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	Vcc	-0.5 to 7.0	V
Power Dissipation	Po	1.0	W
Storage Temperature	Тѕтс	-65 to 150	°C
Operating Temperature	TA	0 to 70	C

^{*} Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(TA = 0 to 70°C)

Parameter	Symbol	Min	Тур	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	. 0	0	0	٧.
Input Low Voltage	ViH	2.2	-	Vcc + 0.5**	V
Input Low Voltage	VIL	-0.5*	-	0.8	. V

^{*} $VIL(Min) = -2.0(Pulse Width \le 10ns)$ for $1 \le 20mA$

DC AND OPERATING CHARACTERISTICS(TA = 0 to 70 °C, Vcc= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	lu	VIN = Vss to Vcc		-2	2	μA
Output Leakage Current	lLO	CS=VIH or OE=VIH or WE=VIL VOUT = Vss to Vcc		-2	2	μA
Operating Current	Icc	Min. Cycle, 100% Duty	17ns	-	150	mA
	,	CS=VIL, VIN = VIH or VIL, IOUT=0mA	20ns	-	140	1
			25ns	-	130	1
Standby Current	ISB	Min. Cycle, СS=Vін		-	40	mA
	ISB1	f=0MHz, $\overline{\text{CS}} \ge \text{Vcc-0.2V}$, Vin $\ge \text{Vcc-0.2V}$ or Vih or Vin $\le 0.2\text{V}$. -	2	mA
Output Low Voltage Level	Vol	loL=8mA		-	0.4	V
Output High Voltage Level	Voн	IOH=-4mA		2.4	-	V
	VoH1*	Iон1=-0.1mA			3.95	V

^{*} NOTE : Vcc= 5.0V \pm 5%, Temp.=25 $^{\circ}$ C

CAPACITANCE*(TA =25°C, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	CI/O	Vi/o=0V	-	8	pF
Input Capacitance	CIN	Vin=0V	-	7	pF

^{*} NOTE : Capacitance is sampled and not 100% tested.



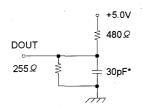
^{**} VIH(Max) = Vcc + 2.0V(Pulse Width \le 10ns) for I \le 20mA

AC CHARACTERISTICS(TA = 0 °C to 70 °C , Vcc = 5.0V \pm 10%, unless otherwise noted.)

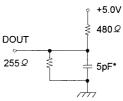
TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3 ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

Output Loads(A)



Output Loads(B) for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

	A	KM64258C-12		KM64258C-15		KM64258C-20		T
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit
Read Cycle Time	tRC	12	-	15	-	20	-	ns
Address Access Time	tAA	-	12	-	15	-	20	ns
Chip Select to Output	tCO	-	12	-	15	-	20	ns
Output Enable to Valid Output	tOE	-	6	-	7	-	9	ns
Chip Enable to Low-Z Output Access	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	, -	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	6	0	7	0	, 10	ns
Output Disable to High-Z Output	tOHZ	0	6	0	7	0	10	ns
Output Hold from Address Change	tOH .	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	0	-	ns
Chip Selection to Power DownTime	tPD	-	12		15	-	20	ns

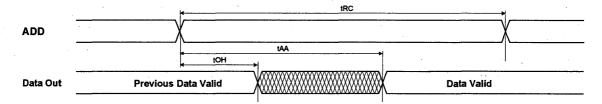


WRITE CYCLE

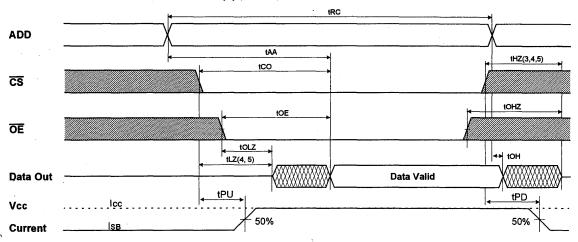
D		KM64258C-12		KM64258C-15		KM64258C-20		T
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit
Write Cycle Time	tWC	12	-	15	-	20	-	ns
Chip Select to End of Write	tCW	9	-	11	-	13	·	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	9	-	12	-	13	-	ns
Write Pulse Width(OE High)	tWP	9	_	12	-	13	-	ns
Write Pulse Width(OE Low)	tWP1	12	-	15	-	20	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	6	0	8	0	8	ns
Data to Write Time Overlap	tDW	7	-	8	-	10		ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	. tOW	0	-	0	-	0	-	ns

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS} = \overline{OE} = VIL, \overline{WE} = VIH)$



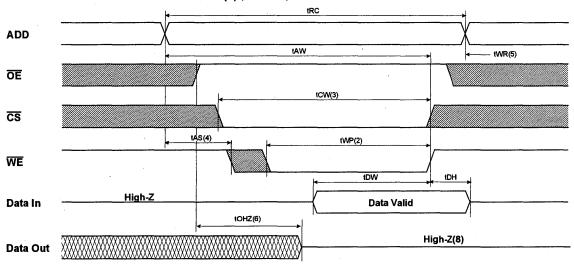
TIMING WAVE FORM OF READ CYCLE(2) (WE=VIH)



NOTES(READ CYCLE)

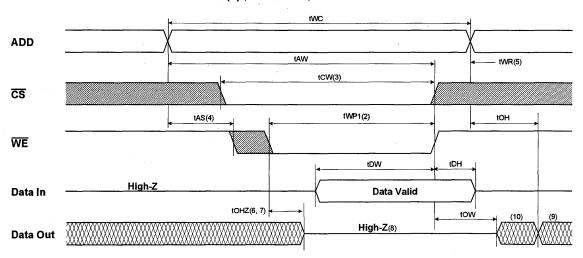
- 1. WE is high for read cycle.
- 2. All read cycle timing is referenced from the last valid address to the first transition address.
- 3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VoH or VoL Levels.
- 4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
- 5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
- 6. Device is continuously selected with CS=Vil.
- 7. Address valid prior to coincident with CS transition low.
- 8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVE FORM OF WRITE CYCLE(1) (OE=Clock)

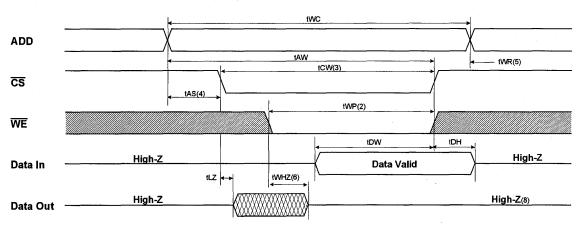




TIMING WAVE FORM OF WRITE CYCLE(2) (OE=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) (CS=Controlled)



NOTES(WRITE CYCLE)

- 1. All write cycle timing is referenced from the last valid address to the first transition address.
- 2. A write occurs during the overlap of a low $\overline{\text{CS}}$ and $\overline{\text{WE}}$. A write begins at the latest transition $\overline{\text{CS}}$ going low and $\overline{\text{WE}}$ going low; A write ends at the earliest transition \overline{CS} going high or \overline{WE} going high. tWP is measured from the beginning of write to the end of write.

 3. tCW is measured from the later of \overline{CS} going low to end of write.
- 4. tAS is measured from the address valid to the beginning of write.
- 5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as CS or WE going high.
- 6. If OE. CS and WE are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
- 7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
- 8. If CS goes low simultaneously with WE going or after WE going low, the outputs remain high impedance state.
- 9. Dout is the read data of the new address.
- 10. When \overline{CS} is low: I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

CS	WE	ŌĒ	Mode	I/O Pin	Supply Current
Н	Х	X*	Not Select	High-Z	ISB, ISB1
L	Н	H	Output Disable	High-Z	lcc
L	I	L	Read	Dout	lcc
L	L	X	Write	Din	lcc

^{*} NOTE : X means Don't Care.

32K x 8 Bit High-Speed BiCMOS Static RAM

FEATURES

- Fast Access Time 6, 7, 8, ns (Max.)
- . Low Power Dissipation

Standby (TTL) : 110mA(Max.)

(CMOS): 20mA(Max.)

Operating Current : 170mA(f=100MHz)

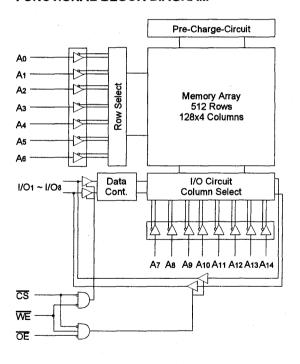
- Single 5.0V ± 5% Power Supply
- . TTL Compatible Inputs and Outputs
- Fully Static Operation
- No Clock or Refresh required
- Three State Outputs
- Center Power/Ground Pin Configuration
- . Standard Pin Configuration

KM68B261AJ: 32-SOJ-300

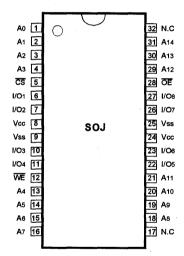
GENERAL DESCRIPTION

The KM68B261A is a 262,144-bit high-speed Static Random Access Memory organized as 32,768 words by 8 bits. The KM68B261A uses eight common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using SAMSUNG's advanced BiCMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM68B261A is packaged in a 300 mil 32-pin plastic SOJ

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION(Top View)



PIN FUNCTION

Pin Name	Pin Function
A0 - A14	Address Inputs
WE	Write Enable
टड	Chip Select
ŌĒ	Output Enable
I/O1 ~ I/O8	Data Inputs/Outputs
Vcc	Power(5.0V)
Vss	Ground
N.C	No Connection



ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	Vin, Vout	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	Vcc	-0.5 to 7.0	٧
Power Dissipation	PD	1.0	W
Storage Temperature	Тѕтс	-65 to 150	°
Operating Temperature	TA	0 to 70	°

^{*} Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(TA = 0 to 70°C)

Parameter	Symbol	Min	Тур	Max	Unit
Supply Voltage	Vcc	4.75	5.0	5.25	٧
Ground	Vss	0	0	0	V
Input Low Voltage	ViH	2.2	-	Vcc + 0.5**	V
Input Low Voltage	VIL	-0.5*	-	0.8	V

^{*} VIL(Min) = -2.0(Pulse Width≤3ns) for I ≤ 20mÅ

DC AND OPERATING CHARACTERISTICS (TA = 0 to 70 °C, Vcc= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Max	Unit	
Input Leakage Current	lu .	VIN = Vss to Vcc	-10	10	μA	
Output Leakage Current	lLO	CS=VIH or OE=VIH or WE=VIL VOUT = Vss to Vcc	-10	10	μA	
Operating Current	lcc	f=100MHz, 100% Duty CS=VIL, VIN = VIH or VIL, IOUT=0mA	-	170	mA	
Standby Current	ISB	Min. Cycle, CS=Viн	-	110	mA	
Is	ISB1	f=0MHz, CS ≥ Vcc-0.2V, Vin ≥ Vcc-0.2V or Vin ≤ 0.2V	-	20	mA	
Output Low Voltage Level	Vol	loL=8mA	-	0.4	٧	
Output High Voltage Level	Voн	IOH=-4mA	2.4	•	٧	

CAPACITANCE*(TA =25°C, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	Ci/o	V1/0=0V	-	7	pF
Input Capacitance	Cin	VIN=0V	-	7	pF

^{*} NOTE: Capacitance is sampled and not 100% tested.

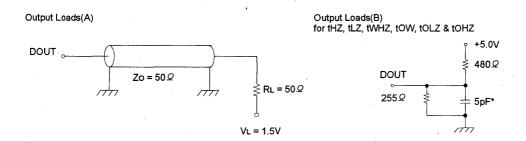


^{**} VIH(Max) = VCC + 2.0V(Pulse Width ≤ 8ns) for I ≤ 20mA

AC CHARACTERISTICS(Ta = 0 to 70 °C, Vcc = $5.0V\pm10\%$, unless otherwise noted.)

TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below



* Including Scope and Jig Capacitance

READ CYCLE

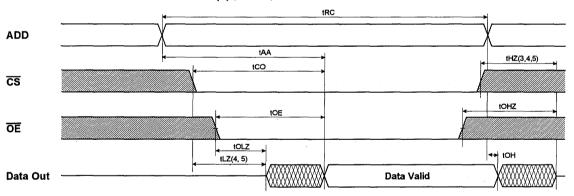
Parameter	S	KM68E	3261A-6	KM68E	261A-7	KM68E	1261A-8	11
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit
Read Cycle Time	tRC	6	-	7	-	8	-	ns
Address Access Time	tAA	•	6	-	7 .	-	8	ns
Chip Select to Output	tCO	-	6	-	7	-	8	ns
Output Enable to Valid Output	tOE	-	4	-	4	-	4	ns
Chip Enable to Low-Z Output Access	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	1	-	1	-	1	-	ns
Chip Disable to High-Z Output	tHZ	0	3	0	3.5	0	4	ns
Output Disable to High-Z Output	tOHZ	0	3	0	3.5	0	4	ns
Output Hold from Address Change	tOH	3 .	-	3	-	3	-	ns

WRITE CYCLE

Parameter	Same bal	KM68B261A-6		KM68B261A-7		KM68B261A-8		11-14
	Symbol	Min	Max	Min	Max	Min .	Max	Unit
Write Cycle Time	tWC	6	-	7	-	. 8	•	ns
Chip Select to End of Write	tCW	6	-	7	-	8	-	ns
Address Setup Time	tAS	0		0	-	0	-	ns
Address Valid to End of Write	tAW	3.5	-	4	-	4.5	-	ns
Write Pulse Width(OE High)	tWP	3.5	-	4	-	4.5	•	ns
Write Pulse Width(OE Low)	tWP1	6	-	7	-	8	-	ns
Write Recovery Time	tWR	1	-	1	-	1	-	ns
Write to Output High-Z	tWHZ	0 .	3	0	3.5	0	4	ns
Data to Write Time Overlap	tDW	3	-	3.5	-	4	-	ns
Data Hold from Write Time	tDH	0	-	0	-	. 0	_	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

TIMING DIAGRAMS

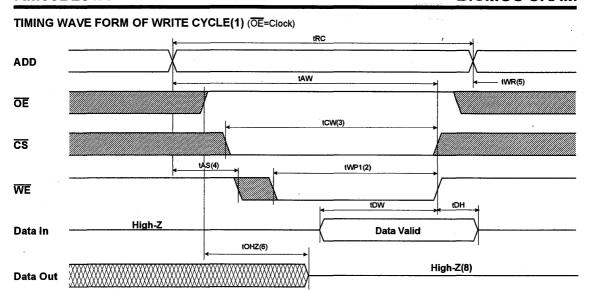
TIMING WAVE FORM OF READ CYCLE(2) (WE=VIH)



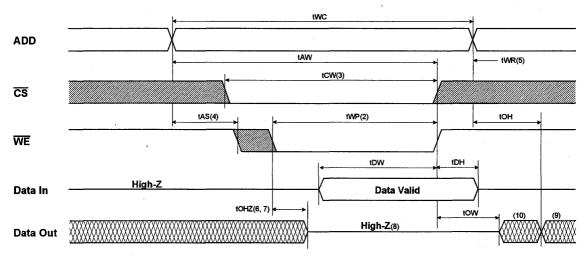
NOTES(READ CYCLE)

- 1. WE is high for read cycle.
- 2. All read cycle timing is referenced from the last valid address to the first transition address.
- 3 tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to Voн or VoL Levels.
- 4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
- 5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
- 6. Device is continuously selected with CS=VIL.
- 7. Address valid prior to coincident with CS transition low.
- 8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

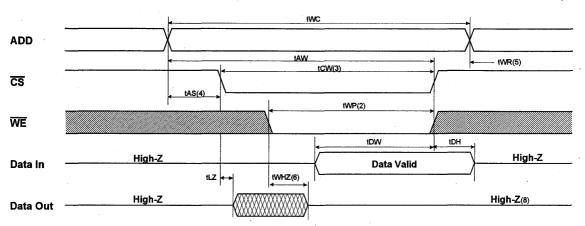




TIMING WAVE FORM OF WRITE CYCLE(2) (OE=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) (CS=Controlled)



NOTES(WRITE CYCLE)

- 1. All write cycle timing is referenced from the last valid address to the first transition address.
- 2. A write occurs during the overlap of a low $\overline{\text{CS}}$ and $\overline{\text{WE}}$. A write begins at the latest transition $\overline{\text{CS}}$ going low and $\overline{\text{WE}}$ going low; A write ends at the earliest transition \overline{CS} going high or \overline{WE} going high. tWP is measured from the beginning of write to the end of write.

 3. tCW is measured from the later of \overline{CS} going low to end of write.
- 4. tAS is measured from the address valid to the beginning of write.
- 5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as CS or WE going high.
- 6. If OE, CS and WE are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
- 7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
- 8. If CS goes low simultaneously with WE going or after WE going low, the outputs remain high impedance state.
- 9. Dout is the read data of the new address.
- 10. When $\overline{\text{CS}}$ is low: I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

ĊŚ	WE	ŌĒ	Mode	I/O Pin	Supply Current
Н	Х	X*	Not Select	High-Z	ISB, ISB1
L	Н	Н	Output Disable	High-Z	lcc
L	Н	L	Read	Dout	lcc
L	L	Х	Write	Din	lcc

^{*} NOTE: X means Don't Care.



32K x 8 Bit High-Speed CMOS Static RAM

FEATURES

• Fast Access Time 12, 15, 20 ns (Max.)

· Low Power Dissipation

Standby (TTL) : 40mA(Max.) (CMOS) : 2mA(Max.)

0.1mA(Max.)- L-ver. only

Operating KM68257C/CL - 12: 165mA(Max.)

KM68257C/CL - 15: 150mA(Max.)

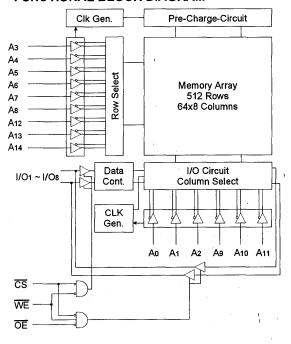
KM68257C/CL - 20: 140mA(Max.)

- Single 5.0V ± 10% Power Supply
- . TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Device
- Fully Static Operation
 - No Clock or Refresh required
- · Three State Outputs
- . Low Data Retention Voltage: 2V (min.)- L-ver. only
- . Standard Pin Configuration

KM68257C/CLP: 28-DIP-300 KM68257C/CLJ: 28-SOJ-300

KM68257C/CLTG: 28-TSOP1-0813, 4F

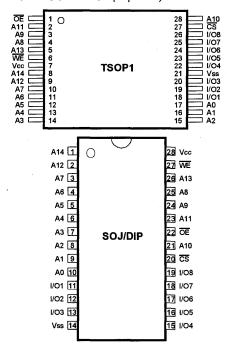
FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The KM68257C is a 262,144-bit high-speed Static Random Access Memory organized as 32,768 words by 8 bits. The KM68257C uses 8 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM68257C is packaged in a 300 mil 28-pin plastic DIP, SOJ or TSOP1 forward.

PIN CONFIGURATION(Top View)



PIN FUNCTION

Pin Name	Pin Function
A0 - A14	Address Inputs
WE	Write Enable
CS	Chip Select
ŌĒ	Output Enable
I/O1 ~ I/O8	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	VIN, VOUT	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	Vcc	-0.5 to 7.0	٧
Power Dissipation	PD	1.0	W
Storage Temperature	Тѕтс	-65 to 150	C
Operating Temperature	TA	0 to 70	Ĉ

^{*} Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(TA = 0 to 70°)

Parameter	Symbol	Min	Тур	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input Low Voltage	ViH	2.2	-	Vcc + 0.5**	٧
Input Low Voltage	VIL	-0.5*	-	0.8	V.

^{*} VIL(Min) = -2.0(Pulse Width \leq 10ns) for $1 \leq$ 20mÅ

DC AND OPERATING CHARACTERISTICS(TA = 0 to 70 °C, Vcc=5.0V ± 10% unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	lu	Vin = Vss to Vcc		-2	2	μA
Output Leakage Current	llo	CS=VIH or OE=VIH or WE=VIL VOUT = Vss to Vcc		-2	2	μA
Operating Current	Icc	Min. Cycle, 100% Duty	12ns	-	165	mA
		CS=VIL, VIN = VIH or VIL,	15ns	· -	150	
		IOUT=0mA	20ns	-	140	
Standby Current	İsB	Min. Cycle, CS=VIH		-	40	· mA
	ISB1	f=0MHz, CS ≥ Vcc-0.2V,	Normal		2	^
		$VIN \ge VCC-0.2V$ or $VIN \le 0.2V$	L-ver		0.1	mA .
Output Low Voltage Level	Vol	IoL=8mA		-	0.4	V
Output High Voltage Level	Voн	IOH=-4mA		2.4	-	V
	VoH1*	Iон1=0.1mA		-	3.95	V

^{*} Vcc=5.0V ± 5% Temp. = 25℃

CAPACITANCE*(TA = 25 °C, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	CI/O	V1/0=0V	-	8	pF
Input Capacitance	CIN	VIN=0V	-	-7	pF

^{*} NOTE: Capacitance is sampled and not 100% tested.



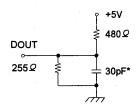
^{**} VIH(Max) = VCC + 2.0V(Pulse Width \leq 10ns) for I \leq 20mÅ

AC CHARACTERISTICS(TA = 0 °C to 70 °C, Vcc = 5.0V ± 10%, unless otherwise noted.)

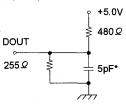
TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

Output Loads(A)



Output Loads(B) for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

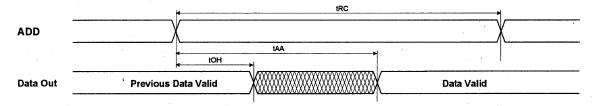
	6tt	KM6825	7C/CL-12	KM68257C/CL-15		KM68257C/CL-20		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit
Read Cycle Time	tRC	12	-	15	-	20	-	ns
Address Access Time	tAA	-	12	-	15	-	20	ns
Chip Select to Output	tCO	-	12	-	15	-	20	ns
Output Enable to Valid Output	tOE	-	6	-	7	-	9	ns
Chip Enable to Low-Z Output Access Time	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0 -	-	ns
Chip Disable to High-Z Output	tHZ	0	6	0	7	0	10	ns
Output Disable to High-Z Output	tOHZ	0	6	0	7	0	10	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	0	-	ns
Chip Selection to Power DownTime	tPD	-	12	-	15	-	20	ns

WRITE CYCLE

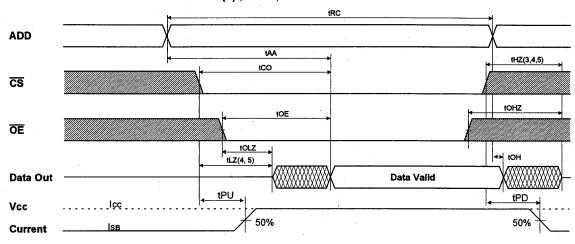
B	Sumbal	KM6825	7C/CL-12	KM6825	7C/CL-15	KM6825	7C/CL-20	Unit
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit
Write Cycle Time	tWC	12	-	15	-	20	-	ns
Chip Select to End of Write	tCW	9	-	11	-	13	-	ns
Address Setup Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	9	-	12	-	13	-	ns
Write Pulse Width(OE High)	, tWP	9	-	12	-	13	-	ns
Write Pulse Width(OE Low)	tWP1	12	-	15	-	20	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	.6	0	8	0	8	ns
Data to Write Time Overlap	tDW	7	-	8	-	10	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	, tOW	0	-	0	-	0	-	ns

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS} = \overline{OE} = VIL, \overline{WE} = VIH)$



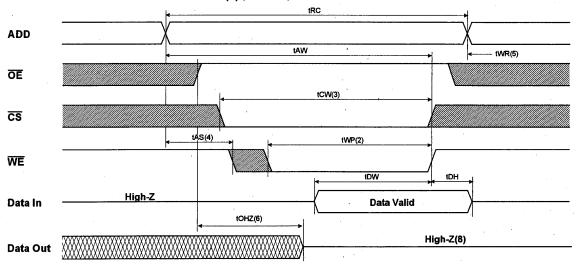
TIMING WAVE FORM OF READ CYCLE(2) (WE=VIH)



NOTES(READ CYCLE)

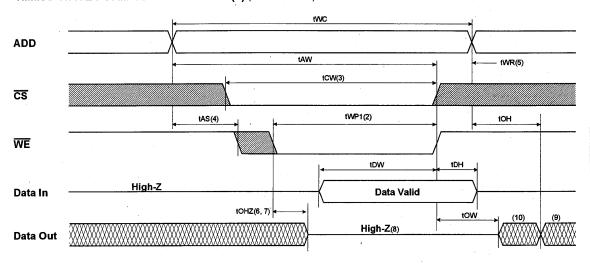
- 1. WE is high for read cycle.
- 2. All read cycle timing is referenced from the last valid address to the first transition address.
- 3 tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VoH or VoL Levels.
- 4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
- 5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
- 6. Device is continuously selected with CS=VIL.
- 7. Address valid prior to coincident with CS transition low.
- 8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVE FORM OF WRITE CYCLE(1) (OE=Clock)

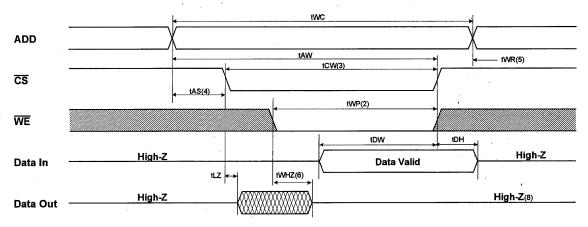




TIMING WAVE FORM OF WRITE CYCLE(2) (OE=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) (CS=Controlled)



NOTES(WRITE CYCLE)

- 1. All write cycle timing is referenced from the last valid address to the first transition address.
- 2. A write occurs during the overlap of a low \overline{CS} and \overline{WE} . A write begins at the latest transition \overline{CS} going low and \overline{WE} going low; A write ends at the earliest transition \overline{CS} going high or \overline{WE} going high. tWP is measured from the beginning of write to the end of write.
- 3. tCW is measured from the later of CS going low to end of write.
- 4. tAS is measured from the address valid to the beginning of write.
- 5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as CS or WE going high.
- 6. If OE, CS and WE are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
- 7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
- 8. If CS goes low simultaneously with WE going or after WE going low, the outputs remain high impedance state.
- 9. Dout is the read data of the new address.
- 10. When \overline{CS} is low: I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

cs	WE	ŌĒ	Mode	I/O Pin	Supply Current
н	X	X*	Not Select	High-Z	ISB, ISB1
L	Н	Н	Output Disable	High-Z	· lcc
L	H	L	Read	Dout	lcc
L	L	Х	Write	Din	lcc

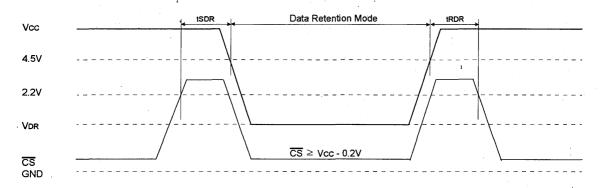
^{*} NOTE : X means Don't Care.

DATA RETENTION CHARACTERISTICS*(TA = 0° to 70°)

Parameter	Symbol	Test Condition	Min.	Тур.	Max.	Unit
Vcc for Data Retention	VDR	CS ≥ Vcc - 0.2V	2.0	-	5.5	V
Data Retention Current	IDR	IDR $Vcc = 2.0V, \overline{CS} \ge Vcc - 0.2V$ $Vin \ge Vcc - 0.2V \text{ or } Vin \le 0.2V$		-	0.07	mA ·
Data Retention Set-Up Time	tSDR	See Data Retention	0	-	-	ns .
Recovery Time	tRDR	Wave form(below)	5	-	_	ms

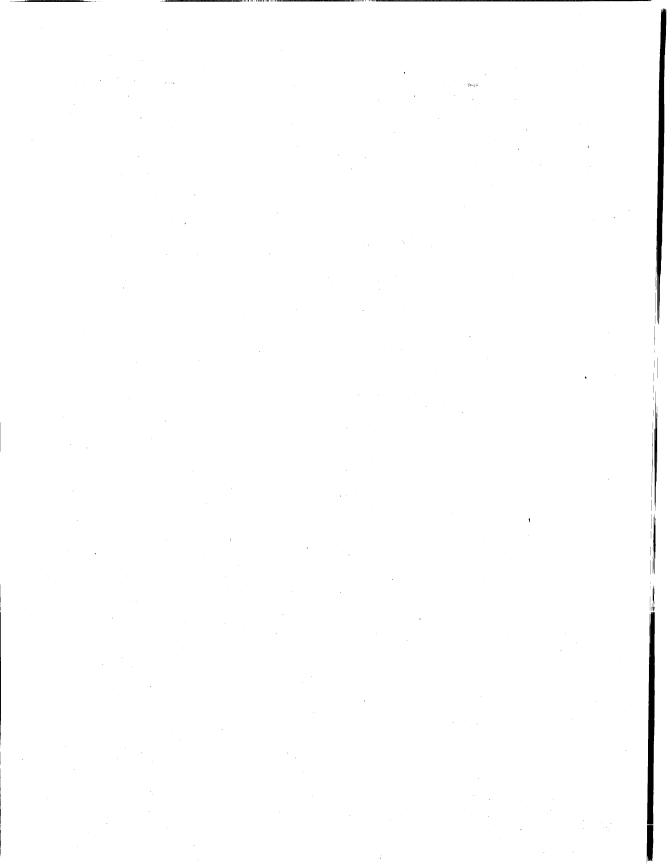
^{*} L-Ver only.

DATA RETENTION WAVE FORM(CS Controlled)





1M High Speed SRAM (5.0V Operation)



1M x 1 Bit High-Speed CMOS Static RAM

FEATURES

• Fast Access Time 20, 25, 35 ns (Max.)

· Low Power Dissipation

Standby (TTL) : 40mA(Max.) (CMOS): 2mA(Max.)

0.5mA(Max.); L-ver. only

Operating KM611001/L - 20: 130mA(Max.)

KM611001/L - 25: 110mA(Max.)

KM611001/L - 35: 100mA(Max.)

Single 5.0V ± 10% Power Supply

. TTL Compatible Inputs and Outputs

Fully Static Operation

- No Clock or Refresh required

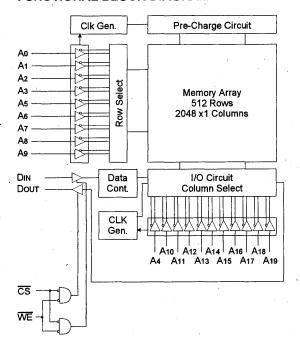
· Three State Outputs

2V Minimum Data Retention; 2V(Min.) - L-ver. only

· Standard Pin Configuration

KM611001/LP: 28-DIP-400 KM611001/LJ: 28-SOJ-400A

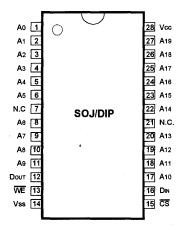
FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The KM611001/L is a 1,048,576-bit high-speed Static Random Access Memory organized as 1,048,576 words by 1 bit. The KM611001/L has separate input and output line for fast read and write access. The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM611001/L is packaged in a 400 mil 28-pin plastic DIP or SOJ.

PIN CONFIGURATION(Top View)



PIN FUNCTION

Pin Name	Pin Function						
A0 - A19	Address Inputs						
WE	Write Enable						
cs	Chip Select						
DIN	Data Input						
Dout	Data Output						
Vcc	Power(+5V)						
Vss	Ground						
N.C	No Connection						

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	Vin, Vout	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	Vcc	-0.5 to 7.0	V
Power Dissipation	PD	1.0	W
Storage Temperature	Тѕтс	-65 to 150	°C
Operating Temperature	TA	0 to 70	°C

^{*} Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(TA = 0 to 70°)

Parameter	Symbol	Min	Тур	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	Ó	٧
Input Low Voltage	ViH	2.2	-	Vcc + 0.5**	V
Input Low Voltage	VIL	-0.5*	-	0.8	V

^{*} VIL(Min) = -2.0V a.c(Pulse Width≤10ns) for I ≤ 20mÅ

DC AND OPERATING CHARACTERISTICS(TA = 0 to 70 °C, Vcc= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	lu	Vin = Vss to Vcc		-2	2	μA
Output Leakage Current	lLO	CS =VIH or WE=VIL VOUT = Vss to Vcc		-2	2	μΑ
Operating Current	lcc	Min. Cycle, 100% Duty	20ns	-	130	mA
	.	CS=VIL, VIN = VIH or VIL,	25ns	-	110	
		IOUT=0mA	35ns	•	100	
Standby Current	ISB	Min. Cycle, CS=Viн		-	40	mA
	ISB1	f=0MHz, CS ≥ Vcc-0.2V,	Normal	-	2	mA.
		$VIN \ge VCC-0.2V \text{ or } VIN \le 0.2V$	L-Ver.		0.5	1 mA
Output Low Voltage Level	Vol	IoL=8mA			0.4	V
Output High Voltage Level	Voн	Іон=-4mА		2.4	-	V

CAPACITANCE*(TA =25°C, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	CI/O	VI/0=0V	-	7	pF
Input Capacitance	Cin	Vin=0V	-	7	pF

^{*} NOTE : Capacitance is sampled and not 100% tested.



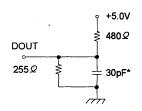
^{**} VIH(Max) = Vcc + 2.0V a.c (Pulse Width \le 10ns) for I \le 20mA

AC CHARACTERISTICS(TA = 0 $^{\circ}\text{C}$ to 70 $^{\circ}\text{C}$, Vcc = 5.0V $^{\pm}$ 10%, unless otherwise noted.)

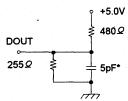
TEST CONDITIONS

Parameter _.	Value .
Input Pulse Levels	OV to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

Output Loads(A)



Output Loads(B) for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	6	KM611001/L-20		KM611001/L-25		KM611001/L-35		Unit
	Symbol	Min	Max	Min	Max	Min	Max	Unit
Read Cycle Time	tRC	20	-	25	-	35	-	ns
Address Access Time	tAA	-	20	-	25	-	35	ns
Chip Select to Output	tCO	-	20	-	25	-	35	ns
Chip Enable to Low-Z Output Access	tLZ	5	-	5	-	5	-	ns
Chip Disable to High-Z Output	tHZ	0	12	0	15	0	15	ns
Output Hold from Address Change	tOH	3	-	5	-	5	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	0	-	ns
Chip Selection to Power DownTime	tPD	-	20		25	-	35	ns

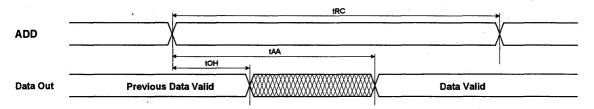
WRITE CYCLE

Parameter	Sumbal	KM611001/L-		20 KM611001/L-25		KM611001/L-35		T.,_,
	Symbol	Min	Max	Min	Max	Min	Max	Unit
Write Cycle Time	tWC	20	-	25	-	35	- '	ns
Chip Select to End of Write	tCW	17	-	20	-	30		ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	17	-	20	-	30	-	ns
Write Pulse Width	tWP	15	-	20	-	. 25	-	ns
Write Recovery Time	tWR	2	-	3	-	3	-	ns
Write to Output High-Z	tWHZ	0	8	0	10	0	12	ns
Data to Write Time Overlap	tDW	12		15	-	20	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	4	-	5	-	ns

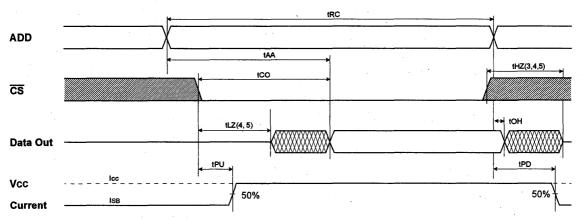


TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, CS=VIL, WE=VIH)

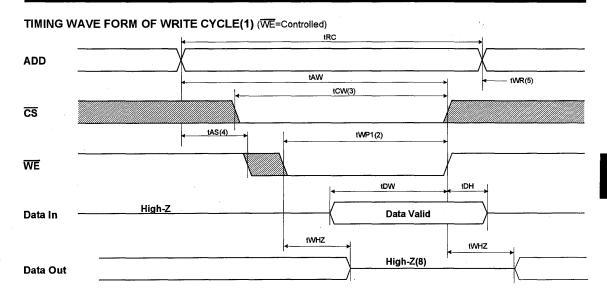


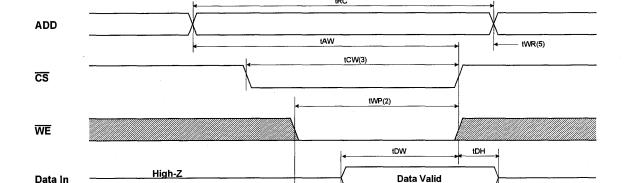
TIMING WAVE FORM OF READ CYCLE(2) (WE=VIH)



NOTES(READ CYCLE)

- 1. WE is high for read cycle.
- 2. All read cycle timing is referenced from the last valid address to the first transition address.
- 3. tHZ is defined as the time at which the output achieve the open circuit condition and is not referenced to VOH or VOL Levels. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
- 4. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
- 5. Device is continuously selected with CS=VIL.
- 6. Address valid prior to coincident with CS transition low.





NOTES(WRITE CYCLE)

Data Out

- 1. All write cycle timing is referenced from the last valid address to the first transition address.
- 2. A write occurs during the overlap of a low \overline{CS} and \overline{WE} . A write begins at the latest transition \overline{CS} going low and \overline{WE} going low; A write ends at the earliest transition \overline{CS} going high or \overline{WE} going high. tWP is measured from the beginning of write to the end of write.

tWHZ

- 3. tCW is measured from the later of $\overline{\text{CS}}$ going low to end of write.
- 4. tAS is measured from the address valid to the beginning of write.

TIMING WAVE FORM OF WRITE CYCLE(2) (CS=Controlled)

- 5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as CS or WE going high.
- 6. If CS goes low simultaneously with WE going or after WE going low, the outputs remain high impedance state.
- 7. Dout is the read data of the new address.



High-Z

FUNCTIONAL DESCRIPTION

<u>cs</u>	WE	Mode	Supply Current		
Н	X*	Not Select	High-Z	ISB, ISB1	
L	Н	Read	Dout	lcc	
L	L	Write	Din	Icc	

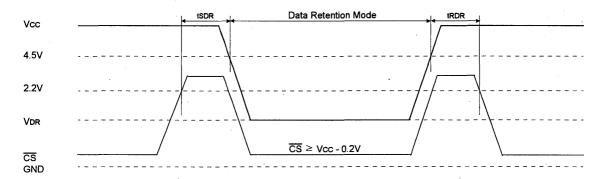
^{*} NOTE : X means Don't Care.

DATA RETENTION CHARACTERISTICS*(TA = 0° to 70°)

Parameter	Symbol	Test Condition	Min.	Тур.	Max.	Unit
Vcc for Data Retention	VDR	CS ≥ Vcc - 0.2V	2.0	-	5.5	٧
Data Retention Current	IDR $ \begin{array}{c} Vcc = 2.0V, \overline{CS} \geq Vcc - 0.2V \\ ViN \geq Vcc - 0.2V \text{ or } ViN \leq 0.2V \end{array} $		<u>-</u>	-	0.1	mA
Data Retention Set-Up Time	tSDR	See Data Retention	0	-	-	ns
Recovery Time	tRDR	Wave form(below)	5	-	-	ms

^{*} NOTE : L-Ver only.

DATA RETENTION WAVE FORM(CS Controlled)



256K x 4 Bit (with \overline{OE})High-Speed CMOS Static RAM

FEATURES

- Fast Access Time 8,10,12ns(Max.)
- Low Power Dissipation

Standby (TTL) : 30mA(Max.)

(CMOS): 10mA(Max.)

1mA(Max.) - L-Ver. only

Operating KM641003B/BL - 8: 150mA(Max.)

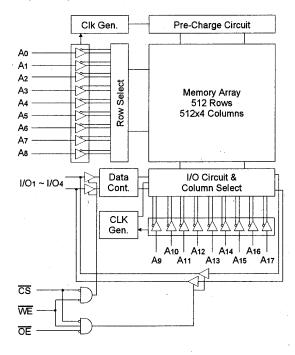
KM641003B/BL - 10: 140mA(Max.)

KM641003B/BL - 12: 130mA(Max.)

- Single 5.0V ± 10% Power Supply
- . TTL Compatible Inputs and Outputs
- . I/O Compatible with 3.3V Device
- · Fully Static Operation
- No Clock or Refresh required
- · Three State Outputs
- · 2V Minimum Data Retention ; L-Ver. only
- Center Power/Ground Pin Configuration
- · Standard Pin Configuration

KM641003B/BLJ: 32-SOJ-400 KM641003B/BLT: 32-TSOP2-400F

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The KM641003B/BL is a 1,048,576-bit high-speed Static Random Access Memory organized as 262,144 words by 4 bits. The KM641003B/BL uses 4 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM641003B/BL is packaged in a 400 mil 32-pin plastic SOJ or TSOP2 forward.

ORDERING INFORMATION

KM641003B/BL -8/10/12	Commercial Temp.
KM641003BI/BLI -8/10/12	Industrial Temp.

PIN CONFIGURATION(Top View)

		-	
N.C. 1		32	A17
A0 2		31	A 16
A1 3		30	A 15
A2 4		29	A14
A3 5		28	A 13
CS 6		27	ŌĒ
1/01 7	·	26	I/O4
Vcc 8	SOJ/	25	Vss
Vss 9	TSOP2	24	Vcc
I/O2 10		23	I/O3
WE 11		22	A 12
A4 12		21	A11
A5 13		20	A 10
A6 14		19	A 9
A7 15		18	A 8
N.C. 16		17	N.C.
		1	

PIN FUNCTION

Pin Name	Pin Function					
A0 - A17	Address Inputs					
WE	Write Enable					
ਟੇਡ	Chip Select					
ŌĒ	Output Enable					
I/O1 ~ I/O4	Data Inputs/Outputs					
Vcc	Power(+5.0V)					
Vss	Ground					
N.C	No Connection					

ABSOLUTE MAXIMUM RATINGS*

Param	eter	Symbol	Rating	Unit
Voltage on Any Pin Relati	ge on Any Pin Relative to Vss		-0.5 to 7.0	V
Voltage on Vcc Supply R	elative to Vss	Vcc	-0.5 to 7.0	٧
Power Dissipation		PD	1.0	W .
Storage Temperature		Тѕтс	-65 to 150	°C
Operating Temperature	Commercial	TA	0 to 70	°C
	Industrial	TA	-40 to 85	°C

^{*} Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(TA = 0 to 70°C)

Parameter	Symbol	Min	Тур	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	٧
Input Low Voltage	VIH	2.2	-	Vcc + 0.5**	V
Input Low Voltage	VIL	-0.5*		0.8	٧

NOTE: Above parameters are also guaranteed at industrial temperature range.

DC AND OPERATING CHARACTERISTICS(TA = 0 to 70 °C, Vcc= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Max	Unit	
Input Leakage Current	lu	Vin = Vss to Vcc		-2	2	μA
Output Leakage Current	ILO	CS=VIH or OE=VIH or WE=VIL VOUT = Vss to Vcc	-2	2 ·	μA	
Operating Current Icc		Min. Cycle, 100% Duty	8ns		150	mA
		CS=VIL, VIN = VIH or VIL,	10ns	•	140	
		IOUT=0mA	12ns	- 130	1	
Standby Current	IsB	Min. Cycle, CS=Viн		-	30	mA
	ISB1	f=0MHz, CS ≥ Vcc-0.2V,	Normal	-	10	, mA
		$VIN \ge VCC-0.2V$ or $VIN \le 0.2V$	L-Ver.	-	1	
Output Low Voltage Level	Vol	IoL=8mA			0.4	V
Output High Voltage Level	Voн	IOH=-4mA		2.4	-	V
	VoH1*	Iон1=-0.1mA '	-	3.95	V	

NOTE: Above parameters are also guaranteed at industrial temperature range.

CAPACITANCE*(TA =25°C, f=1.0MHz)

ltem	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	CI/O	VI/0=0V	-	8	pF
Input Capacitance	Cin	Vin=0V	-	6	pF

^{*} NOTE : Capacitance is sampled and not 100% tested.



^{*} VIL(Min) = -2.0V a.c(Pulse Width≤6ns) for I ≤ 20mA

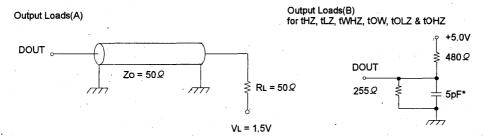
^{**} VIH(Max) = Vcc + 2.0V a.c (Pulse Width ≤ 6ns) for I ≤ 20mÅ

^{*} Vcc=5.0V ± 5% Temp. = 25 ℃

AC CHARACTERISTICS(TA = 0 to 70 °C, Vcc = $5.0V\pm10\%$, unless otherwise noted.) TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

NOTE: Above test conditions are also applied at industrial temperature range.



* Including Scope and Jig Capacitance

READ CYCLE

	KM641003B/BL-8		KM641003B/BL-10		KM641003B/BL-12		1	
Parameter	Symbol	Min	Max	Min	Max	Min	Max	- Unit
Read Cycle Time	tRC	8	-	10	-	12	-	ns
Address Access Time	tAA	-	8	-	10	-	12	ns
Chip Select to Output	tco	-	8	-	10	-	12	ns
Output Enable to Valid Output	tOE	-	4	-	5		. 6	ns
Chip Enable to Low-Z Output	tl.Z	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	4	0	5	0	-6	ns
Output Disable to High-Z Output	tOHZ	0	4	0	5	0	6	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	tPU	0		0	-	0	-	ns
Chip Selection to Power DownTime	tPD	-	8	-	10	-	- 12	ns

NOTE: Above parameters are also guaranteed at industrial temperature range.

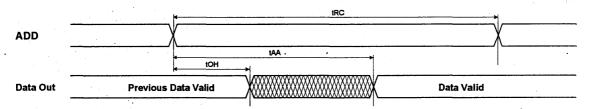
WRITE CYCLE

Parameter	Symbol	KM641003B/BL-8		KM641003B/BL-10		KM641003B/BL-12		T
		Min	Max	Min	Max	Min	Max	Unit
Write Cycle Time	tWC	8	-	10	-	12	-	ns
Chip Select to End of Write	tCW	6	•	7	-	8	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	6	-	7 :	-	8	-	ns
Write Pulse Width(OE High)	· tWP	6	-	7		. 8	-	ns
Write Pulse Width(OE Low)	tWP1	8	-	10	-	12	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	. 4	0	5	0	6	ns
Data to Write Time Overlap	tDW	4	-	5		6	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

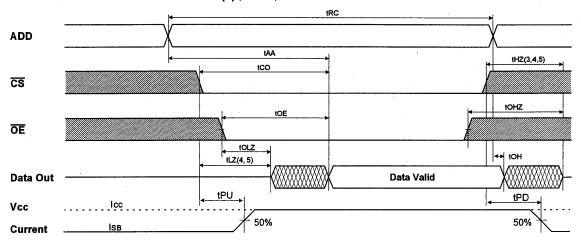
NOTE: Above parameters are also guaranteed at industrial temperature range.

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, CS=OE=VIL, WE=VIH)



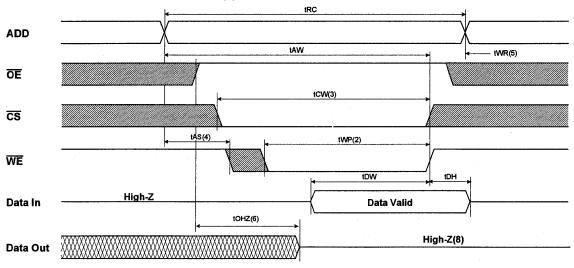
TIMING WAVE FORM OF READ CYCLE(2) (WE=VIH)



NOTES(READ CYCLE)

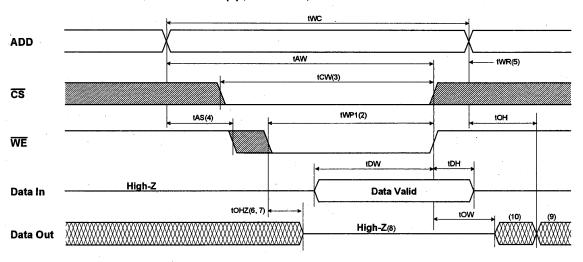
- 1. WE is high for read cycle.
- 2. All read cycle timing is referenced from the last valid address to the first transition address.
- 3) tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL Levels.
- 4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
- 5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
- 6. Device is continuously selected with $\overline{\text{CS}} = \text{Vil.}$
- 7. Address valid prior to coincident with $\overline{\text{CS}}$ transition low.
- 8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVE FORM OF WRITE CYCLE(1) (OE=Clock)

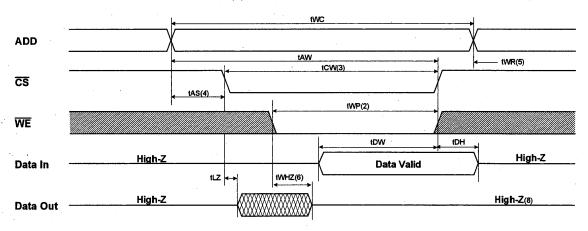




TIMING WAVE FORM OF WRITE CYCLE(2) (OE=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) (CS=Controlled)



NOTES(WRITE CYCLE)

- 1. All write cycle timing is referenced from the last valid address to the first transition address.
- 2. A write occurs during the overlap of a low $\overline{\text{CS}}$ and $\overline{\text{WE}}$. A write begins at the latest transition $\overline{\text{CS}}$ going low and $\overline{\text{WE}}$ going low; A write ends at the earliest transition $\overline{\text{CS}}$ going high or $\overline{\text{WE}}$ going high. tWP is measured from the beginning of write to the end of write.
- 3. tCW is measured from the later of CS going low to end of write.
- 4. tAS is measured from the address valid to the beginning of write.
- 5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as CS or WE going high.
- 6. If \overline{OE} , \overline{CS} and \overline{WE} are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
- 7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
- 8. If $\overline{\text{CS}}$ goes low simultaneously with $\overline{\text{WE}}$ going or after $\overline{\text{WE}}$ going low, the outputs remain high impedance state.
- 9. Dout is the read data of the new address.
- 10. When \overline{CS} is low: I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

	<u>cs</u>	WE	ŌĒ	Mode	I/O Pin	Supply Current ISB, ISB1		
	Н	Х	X*	Not Select	High-Z			
1	Ļ	Н	Η	Output Disable	High-Z	lcc		
.	L.	Н	L	Read	Dout	lcc		
	L	L	X	Write	DIN	lcc		

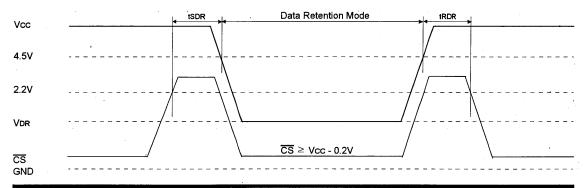
^{*} NOTE: X means Don't Care.

DATA RETENTION CHARACTERISTICS*(TA = 0° to 70°)

Parameter	Symbol	Test Condition	Min.	Тур.	Max.	Unit
Vcc for Data Retention	VDR	CS ≥ Vcc - 0.2V	2.0	-	5.5	>
Data Retention Current	IDR	$ \begin{array}{c} \text{Vcc} = 3.0 \text{V, } \overline{\text{CS}} \geq \text{Vcc} - 0.2 \text{V} \\ \text{Vin} \geq \text{Vcc} - 0.2 \text{V or Vin} \leq 0.2 \text{V} \\ \end{array} $	-	-	0.9	mA
		$ \begin{array}{c} \text{Vcc} = 2.0 \text{V, } \overline{\text{CS}} \geq \text{Vcc} - 0.2 \text{V} \\ \text{Vin} \geq \text{Vcc} - 0.2 \text{V or Vin} \leq 0.2 \text{V} \\ \end{array} $		-	0.7	
Data Retention Set-Up Time	tSDR	See Data Retention	0	-	-	ns
Recovery Time	tRDR	Wave form(below)	5	-	-	ms

NOTE: Above parameters are also guaranteed at industrial temperature range.

DATA RETENTION WAVE FORM(CS Controlled)





^{*} L-Ver only.

256K x 4 Bit (with OE)High-Speed CMOS Static RAM

FEATURES

- Fast Access Time 8,10,12ns (Max.)
- · Low Power Dissipation

Standby (TTL) : 60mA(Max.)

(CMOS): 10mA(Max.)

Operating KM64B1003 - 8: 165mA(Max.)

KM64B1003 - 10: 155mA(Max.)

KM64B1003 - 12: 145mA(Max.)

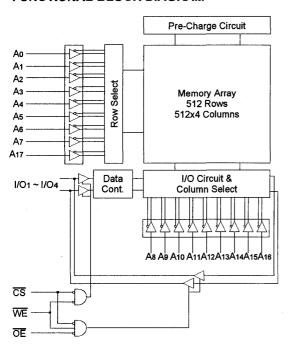
- Single 5 0V ± 10% Power Supply
- . TTL Compatible Inputs and Outputs
- Fully Static Operation
 - No Clock or Refresh required
- Three State Outputs
- · Center Power/Ground Pin Configuration
- · Standard Pin Configuration

KM64B1003J: 32-SOJ-400

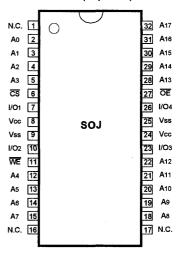
GENERAL DESCRIPTION

The KM64B1003 is a 1,048,576-bit high-speed Static Random Access Memory organized as 262,144 words by 4 bits. The KM64B1003 uses 4 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using SAMSUNG's advanced BiCMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM64B1003 is packaged in a 400 mil 32-pin plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION(Top View)



PIN FUNCTION

Pin Name	Pin Function
A0 - A17	Address Inputs
WE	Write Enable
<u>cs</u>	Chip Select
ŌĒ	Output Enable
I/O1 ~ I/O4	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground
N.C	No Connection



ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	VIN, VOUT	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	Vcc	-0.5 to 7.0	V
Power Dissipation	PD	1.0	W
Storage Temperature	Тѕтс	-65 to 150	°C
Operating Temperature	TA	0 to 70	°

^{*} Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(TA = 0 to 70°C)

Parameter	Symbol	Min	Тур	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	٧
Ground	Vss	0	0	0	V
Input Low Voltage	ViH	2.2	-	Vcc + 0.5**	V
Input Low Voltage	VIL	-0.5*	-	0.8	V

^{*} VIL(Min) = -2.0V a.c(Pulse Width≤6ns) for 1 ≤ 20mA

DC AND OPERATING CHARACTERISTICS(TA = 0 to 70 °C, Vcc= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	lLi	VIN = Vss to Vcc		-2	2	μA
Output Leakage Current	ILO	CS=VIH or OE=VIH or WE=VIL VOUT = Vss to Vcc	-10	10	μA	
Operating Current	Icc	Min. Cycle, 100% Duty	8ns	-	165	mA
		CS=VIL, VIN = VIH or VIL,	10ns	-	155	
		IOUT=0mA	12ns	-	145	
Standby Current	ISB	Min. Cycle, CS=Viн		-	60	mΑ
	ISB1	f=0MHz, $\overline{CS} \ge Vcc-0.2V$, Vin $\ge Vcc-0.2V$ or Vin $\le 0.2V$		-	10	mA
Output Low Voltage Level	Vol	IoL=8mA		-	0.4	V
Output High Voltage Level	Voн	IOH=-4mA		2.4	-	٧

CAPACITANCE*(TA =25°C, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	CI/O	Vi/o=0V	-	8	ρF
Input Capacitance	CIN	Vin=0V	•	7	pF

^{*} NOTE: Capacitance is sampled and not 100% tested.

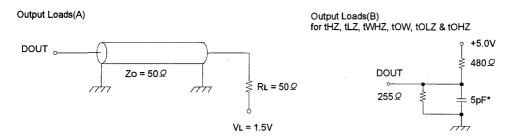


^{**} ViH(Max) = Vcc + 2.0V a.c (Pulse Width ≤6ns) for I ≤ 20mA

AC CHARACTERISTICS(TA = 0 to 70 $^{\circ}$ C, Vcc = 5.0V \pm 10%, unless otherwise noted.)

TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3 ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	6	KM64B1003-8		KM64B1003-10		KM64B1003-12		
raiameter	Symbol	Min	Max	Min	Max	Min	Max	Unit
Read Cycle Time	tRC	8	-	10	-	12	-	ns
Address Access Time	tAA	-	8	-	10	-	12	ns
Chip Select to Output	tCO	-	8	-	10	-	12	ns
Output Enable to Valid Output	tOE	-	4	-	5	-	6	ns
Chip Enable to Low-Z Output Access	tLZ	3	-	. 3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	4	0	5	0	6	ns
Output Disable to High-Z Output	tOHZ	0	4	0	5	0	6	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns

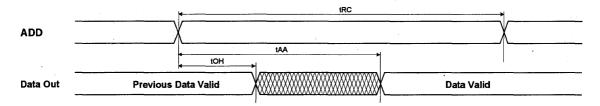


WRITE CYCLE

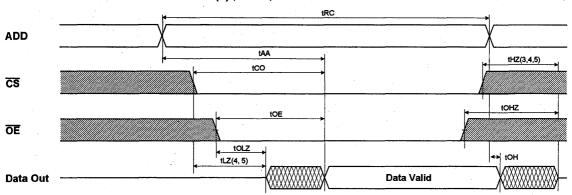
Parameter	at.i	KM64B1003-8		KM64B1003-10		KM64B1003-12		T
	Symbol	Min	Max	Min	Max	Min	Max	- Unit
Write Cycle Time	tWC	8		10	-	12	-	ns
Chip Select to End of Write	tCW	6	-	7	-	8	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	6	-	7	-	8	-	ns
Write Pulse Width(OE High)	tWP	6	-	7	-	8	• -	ns
Write Pulse Width(OE Low)	tWP1	8	-	9	-	10	-	ns
Write Recovery Time	tWR	1	-	1	-	1	-	ns
Write to Output High-Z	tWHZ	0	4	0	5	0	6	ns
Data to Write Time Overlap	tDW	4	-	5	-	6	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS} = \overline{OE} = VIL$, $\overline{WE} = VIH$)



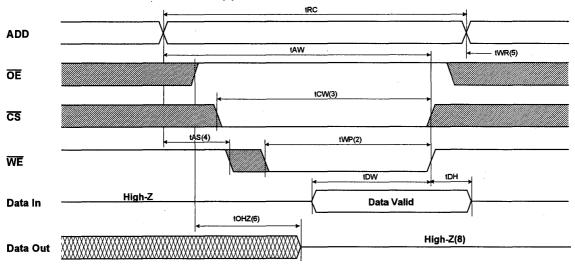
TIMING WAVE FORM OF READ CYCLE(2) (WE=VIH)



NOTES(READ CYCLE)

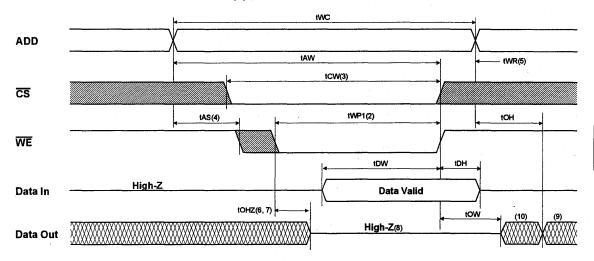
- 1 WE is high for read cycle.
- 2. All read cycle timing is referenced from the last valid address to the first transition address.
- 3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VoH or VoL Levels.
- 4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
- 5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
- 6. Device is continuously selected with CS=VIL.
- 7. Address valid prior to coincident with CS transition low.
- 8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVE FORM OF WRITE CYCLE(1) (OE=Clock)

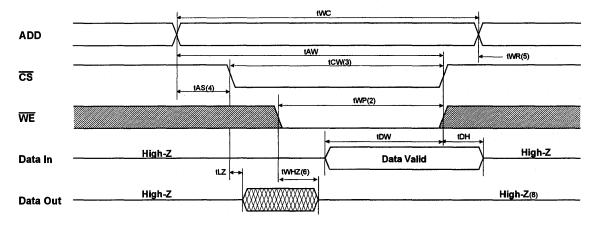




TIMING WAVE FORM OF WRITE CYCLE(2) (OE=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) (CS=Controlled)



NOTES(WRITE CYCLE)

- 1. All write cycle timing is referenced from the last valid address to the first transition address.
- 2. A write occurs during the overlap of a low \overline{CS} and \overline{WE} . A write begins at the latest transition \overline{CS} going low and \overline{WE} going low; A write ends at the earliest transition \overline{CS} going high or \overline{WE} going high. tWP is measured from the beginning of write to the end of write.
- 3. tCW is measured from the later of $\overline{\text{CS}}$ going low to end of write.
- 4. tAS is measured from the address valid to the beginning of write.
- 5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as CS or WE going high.
- 6. If OE, CS and WE are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
- 7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
- 8. If CS goes low simultaneously with WE going or after WE going low, the outputs remain high impedance state.
- 9. Dout is the read data of the new address.
- 10. When \overline{CS} is low: I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

CS	WE	ŌĒ	Mode	I/O Pin	Supply Current
Н	Х	X*	Not Select	High-Z	ISB, ISB1
L	Н	Н	Output Disable	High-Z	Icc
L	Н	L	Read	Dout	lcc
L	L	Х	Write	DIN	Icc

^{*} NOTE: X means Don't Care.



256K x 4 Bit (with OE) High-Speed CMOS Static RAM

FEATURES

- Fast Access Time 12, 15, 17, 20 ns (Max.)
- · Low Power Dissipation

Standby (TTL) : 25mA(Max.)

(CMOS): 8mA(Max.)

Operating KM641003A - 12: 150mA(Max.)

KM641003A - 15: 145mA(Max.)

KM641003A - 17: 145mA(Max.)

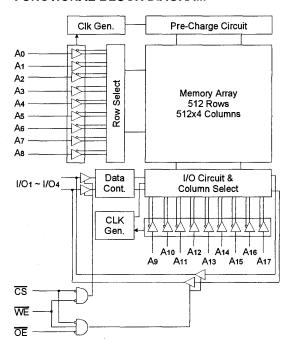
KM641003A - 20: 140mA(Max.)

- Single 5.0V ± 10% Power Supply
- TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Device
- · Fully Static Operation
 - No Clock or Refresh required
- . Three State Outputs
- · Center Power/Ground Pin Configuration
- · Standard Pin Configuration

KM641003AJ: 32-SOJ-400

KM641003AT: 32-TSOP2-400F

FUNCTIONAL BLOCK DIAGRAM



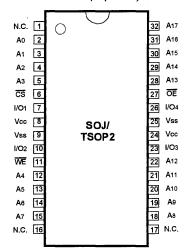
GENERAL DESCRIPTION

The KM641003A is a 1,048,576-bit high-speed Static Random Access Memory organized as 262,144 words by 4 bits. The KM641003A uses 4 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM641003A is packaged in a 400 mil 32-pin plastic SOJ or TSOP2 forward.

ORDERING INFORMATION

KM641003A -12/15/17/20	Commercial Temp.
KM641003AI -12/15/17/20	Industrial Temp.

PIN CONFIGURATION(Top View)



PIN FUNCTION

Pin Name	Pin Function
A0 - A17	Address Inputs
WE	Write Enable
CS	Chip Select
ŌĒ	Output Enable
1/01 ~ 1/04	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parame	eter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss		VIN, VOUT	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss		Vcc	-0.5 to 7.0	V
Power Dissipation		PD	1.0	W
Storage Temperature		Тѕтс	-65 to 150	°C
Operating Temperature	Commercial	TA	0 to 70	°
	Industrial	TA	-40 to 85	°C

^{*} Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(TA = 0 to 70°C)

Parameter	Symbol	Min	Тур	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	Ÿ
Input Low Voltage	. VIH	2.2	-	Vcc + 0.5**	V
Input Low Voltage	ViL	-0.5*		0.8	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

DC AND OPERATING CHARACTERISTICS(TA = 0 to 70°C, Vcc= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	ILI	Vin = Vss to Vcc	VIN = Vss to Vcc		2	μA
Output Leakage Current	lLO	CS=VIH or OE=VIH or WE=VIL VOUT = Vss to Vcc	-2	2	μA	
Operating Current	Icc	Min. Cycle, 100% Duty	12ns	-	150	mΑ
		CS=VIL, VIN = VIH or VIL,	15ns	-	145	
		lout≅0mA	17ns	-	145	
			20ns	-	140	1
Standby Current	ISB	Min. Cycle, CS =Vін		-	25	mA
	ISB1	f=0MHz, $\overline{CS} \ge Vcc-0.2V$, Vin $\ge Vcc-0.2V$ or Vin $\le 0.2V$		-	8	mA
Output Low Voltage Level	Vol	IoL=8mA		•	0.4	V
Output High Voltage Level	Voн	IOH=-4mA		2.4	-	V
	Vон1*	Iон1=-0.1mA		-	3.95	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

CAPACITANCE*(TA =25°C, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	CI/O	VI/0=0V	-	8	pF
Input Capacitance	, Cin	VIN=0V	-	.6	pF

^{*} NOTE: Capacitance is sampled and not 100% tested.



^{*} VIL(Min) = -2.0V a.c(Pulse Width≤10ns) for I ≤ 20mA

^{**} VIH(Max) = Vcc + 2.0V a.c (Pulse Width ≤ 10ns) for I ≤ 20mA

^{*} Vcc=5.0V ± 5% Temp = 25℃

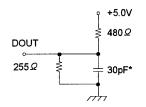
AC CHARACTERISTICS(TA = 0 to 70 $^{\circ}$ C, Vcc = 5.0V $^{\pm}$ 10%, unless otherwise noted.)

TEST CONDITIONS

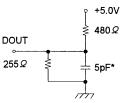
Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3 ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

NOTE: Above test conditions are also applied at industrial temperature range.

Output Loads(A)



Output Loads(B) for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

Parameter		KM641	003A-12	KM641	003A-15	KM641	003A-17	KM641	003A-20	Unit
	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Read Cycle Time	tRC	12	-	15	-	17	-	20	-	ns
Address Access Time	tAA	-	12	-	15	-	17	-	20	ns
Chip Select to Output	tCO	-	12	-	15	-	17	-	20	ns
Output Enable to Valid Output	tOE	-	6	-	7	-	8	-	9	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	6	0	7	0	8	0	9	ns
Output Disable to High-Z Output	tOHZ	0	6	0	7	0	8	0	9	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	0	-	0	-	ns
Chip Selection to Power DownTime	tPD	-	12	-	15	-	17	-	20	ns

NOTE: Above parameters are also guaranteed at industrial temperature range.

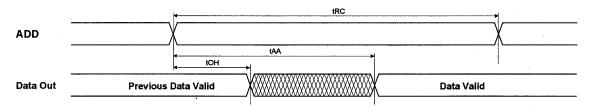
WRITE CYCLE

Parameter		KM641003A-12		KM641003A-15		KM641003A-17		KM641003A-20		Unit
	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Write Cycle Time	tWC	12	-	15	-	17	-	20	-	ns
Chip Select to End of Write	tCW	8	-	10	-	11	-	12	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	8	-	10	-	11	-	12	-	ns
Write Pulse Width(OE High)	tWP	8	-	10	-	11	-	12	-	nis
Write Pulse Width(OE Low)	tWP1	12		15	-	17		20	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	.6	0	7	. 0	8	0	9	ns
Data to Write Time Overlap	tDW	6	-	7	-	8	-	9	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	3	-	ns

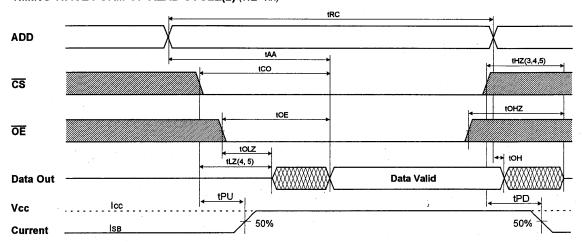
NOTE: Above parameters are also guaranteed at industrial temperature range.

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, CS=OE=VIL, WE=VIH)



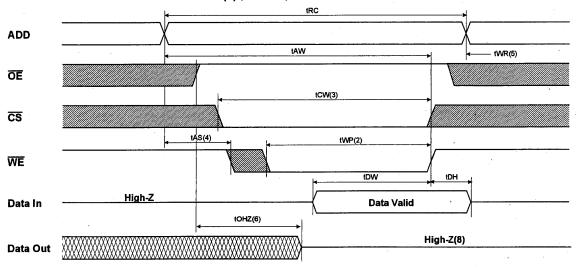
TIMING WAVE FORM OF READ CYCLE(2) (WE=VIH)



NOTES(READ CYCLE)

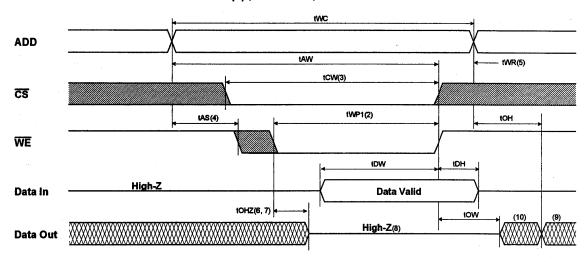
- 1. WE is high for read cycle.
- 2. All read cycle timing is referenced from the last valid address to the first transition address.
- tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VoH or VoL Levels.
- 4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
- 5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
- 6. Device is continuously selected with CS=VIL.
- 7. Address valid prior to coincident with CS transition low.
- 8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVE FORM OF WRITE CYCLE(1) (OE=Clock)

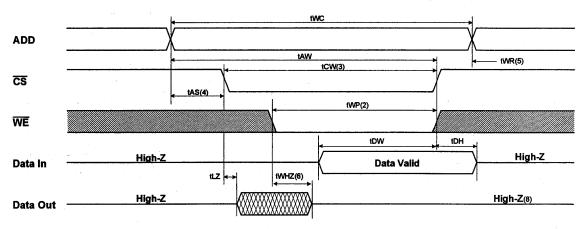




TIMING WAVE FORM OF WRITE CYCLE(2) (OE=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) (CS=Controlled)



NOTES(WRITE CYCLE)

- 1. All write cycle timing is referenced from the last valid address to the first transition address.
- 2. A write occurs during the overlap of a low \overline{CS} and \overline{WE} . A write begins at the latest transition \overline{CS} going low and \overline{WE} going low; A write ends at the earliest transition \overline{CS} going high or \overline{WE} going high. tWP is measured from the beginning of write to the end of write.
- 3. tCW is measured from the later of \overline{CS} going low to end of write.
- 4. tAS is measured from the address valid to the beginning of write.
- 5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as CS or WE going high.
- 6. If \overline{OE} , \overline{CS} and \overline{WE} are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
- 7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
- 8. If CS goes low simultaneously with WE going or after WE going low, the outputs remain high impedance state.
- 9. Dout is the read data of the new address.
- 10. When $\overline{\text{CS}}$ is low: I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

ĊŚ	WE	ŌĒ	Mode	I/O Pin	Supply Current
Н	Х	X*	Not Select	High-Z	ISB, ISB1
L	Н .	H	Output Disable	High-Z	lcc
L	H	٦	Read	Dout	lcc
L	L	Х	Write	Din	lcc

^{*} NOTE: X means Don't Care.

256K x 4 Bit (with OE)High-Speed CMOS Static RAM

FEATURES

- Fast Access Time 15, 17, 20 ns (Max.)
- Low Power Dissipation

Standby (TTL) : 40mA(Max.)

(CMOS): 10mA(Max.)

Operating KM641003 - 15: 170mA(Max.)

KM641003 - 17: 160mA(Max.)

KM641003 - 20: 150mA(Max.)

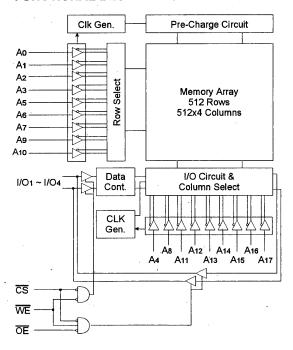
- Single 5.0V ± 10% Power Supply
- . TTL Compatible Inputs and Outputs
- . I/O Compatible with 3.3V Device
- · Fully Static Operation
- No Clock or Refresh required
- . Three State Outputs
- · Center Power/Ground Pin Configuration
- · Standard Pin Configuration

KM641003J: 32-SOJ-400

GENERAL DESCRIPTION

The KM641003 is a 1,048,576-bit high-speed Static Random Access Memory organized as 262,144 words by 4 bits. The KM641003 uses 4 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM641003 is packaged in a 400 mil 32-pin plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION(Top View)

			1	
N.C.	1		32	A 17
A0	2		31	A16
A 1	3		30	A 15
A 2	4		29	A14
Аз	5		28	A13
CS	6		27	ŌĒ
I/O1	7		26	1/04
Vcc	8	SOJ	25	Vss
Vss	9	, 000	24	Vcc
1/02	10		23	I/O3
WE	11		22	A 12
A 4	12		21	A11
A 5	13		20	A10
A 6	14		19	A 9
A 7	15	•	18	A 8
N.C.	16		17	N.C.
			1	

PIN FUNCTION

Pin Name	Pin Function
A0 - A17	Address Inputs
WE	Write Enable
cs	Chip Select
ŌĒ	Output Enable
1/01 ~ 1/04	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	Vin, Vout	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	Vcc	-0.5 to 7.0	V
Power Dissipation	PD	1.0	W
Storage Temperature	Тѕтс	-65 to 150	°C
Operating Temperature	TA	0 to 70	°C

^{*} Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(TA = 0 to 70°C)

Parameter	Symbol	Min	Тур	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input Low Voltage	ViH	2.2	-	Vcc + 0.5**	V
Input Low Voltage	VIL	-0.5*	-	0.8	V

^{*} VIL(Min) = -2.0V a.c(Pulse Width≤10ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS(TA = 0 to 70°C, Vcc= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions	Test Conditions		Max	Unit
Input Leakage Current	ILI	VIN = Vss to Vcc		-2	2	μA
Output Leakage Current	lLO	CS=VIH or OE=VIH or WE=VIL VOUT = Vss to Vcc		-2	2	μA
Operating Current	lcc	Min. Cycle, 100% Duty	15ns	•	170	mA
		CS=VIL, VIN = VIH or VIL,	17ns.	-	160	
		IOUT=0mA 2		-	155	
Standby Current	IsB	Min. Cycle, CS=Vін		-	40	mA
	ISB1	f=0MHz, $\overline{CS} \ge Vcc-0.2V$, Vin $\ge Vcc-0.2V$ or Vin $\le 0.2V$		-	10	· mA
Output Low Voltage Level	Vol	IoL=8mA		-	0.4	V
Output High Voltage Level	Voн	IOH=-4mA		2.4	-	V
	Vон1*	юн1=-0.1mA		-	3.95	V

^{*} Vcc=5.0V ± 5% Temp. = 25℃

CAPACITANCE*(TA =25°C, f=1.0MHz)

ltem	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	Ci/o	V1/0=0V	-	8	pF
Input Capacitance	Cin	Vin=0V	-	6	pF

^{*} NOTE : Capacitance is sampled and not 100% tested.



^{**} VIH(Max) = Vcc + 2.0V a.c (Pulse Width ≤ 10ns) for I ≤ 20mA

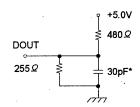
AC CHARACTERISTICS(TA = 0 to 70 °C, Vcc = 5.0V ± 10%, unless otherwise noted.)

TEST CONDITIONS

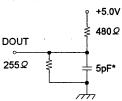
Parameter	Value
Input Pulse Levels	OV to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

NOTE: Above test conditions are also applied at industrial temperature range.





Output Loads(B) for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

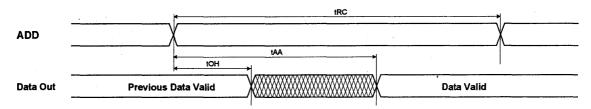
Parameter		KM64	KM641003-15		KM641003-17		KM641003-20	
	Symbol	Min	Max	Min	Max	Min	Max	- Unit
Read Cycle Time	tRC	15	-	17	-	20	•	ns
Address Access Time	tAA	-	15		17	•	20	ns
Chip Select to Output	tCO	-	15	-	17	-	20	ns
Output Enable to Valid Output	tOE		8	-	9	•	10	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3 .	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	6	0	7	0	8	ns
Output Disable to High-Z Output	tOHZ	0	6	0	7	0.	8	ns
Output Hold from Address Change	tOH	3	-	3	-	- 5	-	ns
Chip Selection to Power Up Time	tPU	0	-	0		0	-	ns
Chip Selection to Power DownTime	tPD	-	15	-	17	-	20	ns

WRITE CYCLE

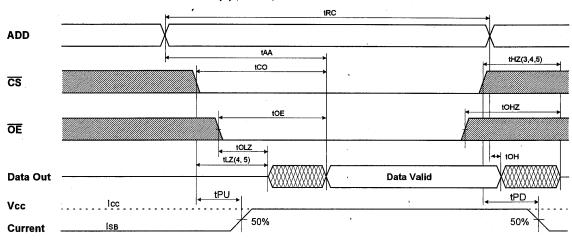
Parameter	G	KM641003-15		KM641003-17		KM641003-20		1
	Symbol	Min	Max	Min	` Max	Min	Max	Unit
Write Cycle Time	tWC	15	-	17	-	20	-	ns
Chip Select to End of Write	tCW	12	-	12	-	13	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	12	-	12	-	13	-	ns
Write Pulse Width(OE High)	tWP	9	-	10	-	11	-	ns
Write Pulse Width(OE Low)	tWP1	15	-	17	-	20	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	8	0	8	0	10	ns
Data to Write Time Overlap	tDW	8	-	9	-	10	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	4	-	5	-	ns

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, CS=OE=VIL, WE=VIH)



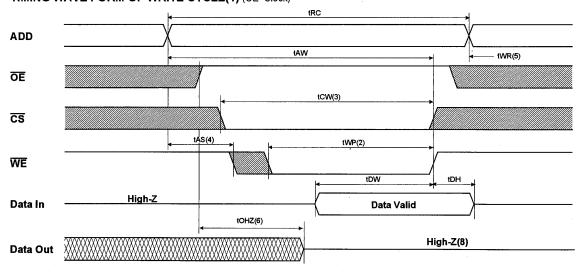
TIMING WAVE FORM OF READ CYCLE(2) (WE=VIH)



NOTES(READ CYCLE)

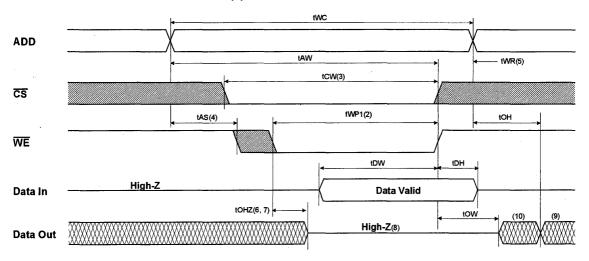
- 1. WE is high for read cycle.
- 2. All read cycle timing is referenced from the last valid address to the first transition address.
- tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VoH or VoL Levels.
- 4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
- 5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
- 6. Device is continuously selected with CS=VIL.
- 7. Address valid prior to coincident with CS transition low.
- 8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVE FORM OF WRITE CYCLE(1) (OE=Clock)

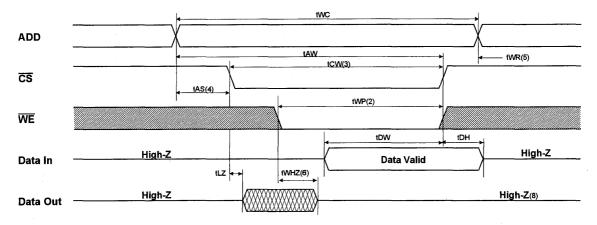




TIMING WAVE FORM OF WRITE CYCLE(2) (OE=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) (CS=Controlled)



NOTES(WRITE CYCLE)

- 1. All write cycle timing is referenced from the last valid address to the first transition address.
- 2. A write occurs during the overlap of a low $\overline{\text{CS}}$ and $\overline{\text{WE}}$. A write begins at the latest transition $\overline{\text{CS}}$ going low and $\overline{\text{WE}}$ going low; A write ends at the earliest transition \overline{CS} going high or \overline{WE} going high. tWP is measured from the beginning of write to the end of write.

 3. tCW is measured from the later of \overline{CS} going low to end of write.
- 4. tAS is measured from the address valid to the beginning of write.
- 5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as CS or WE going high.
- 6. If OE, CS and WE are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
- 7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
- 8. If CS goes low simultaneously with WE going or after WE going low, the outputs remain high impedance state.
- 9. Dout is the read data of the new address.
- 10. When \overline{CS} is low: I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

ĊS	WE	ŌĒ	Mode	I/O Pin	Supply Current
Н	Х	X*	Not Select	High-Z	ISB, ISB1
L	Н	Н	Output Disable	High-Z	lcc
L	Н	L	Read	Dout	lcc
L.	L	X	Write	DIN	lcc

^{*} NOTE: X means Don't Care.

KM641001B/BL, KM641001BI/BLI

256K x 4 Bit (with OE)High-Speed CMOS Static RAM

FEATURES

- Fast Access Time 15, 17, 20 ns (Max.)
- Low Power Dissipation

Standby (TTL) : 20mA(Max.)

(CMOS): 5mA(Max.)

0.5mA(Max.) - L-Ver. only

Operating KM641001B/BL - 15: 120mA(Max.)

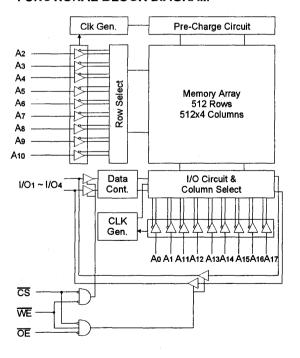
KM641001B/BL - 17: 110mA(Max.)

KM641001B/BL - 20: 100mA(Max.)

- Single 5.0V ± 10% Power Supply
- . TTL Compatible Inputs and Outputs
- . I/O Compatible with 3.3V Device
- . Fully Static Operation
 - No Clock or Refresh required
- . Three State Outputs
- 2V Minimum Data Retention : L-Ver. only
- · Standard Pin Configuration

KM641001B/BLJ: 28-SOJ-400A

FUNCTIONAL BLOCK DIAGRAM



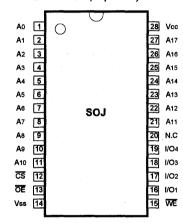
GENERAL DESCRIPTION

The KM641001B/BL is a 1,048,576-bit high-speed Static Random Access Memory organized as 262,144 words by 4 bits. The KM641001B/BL uses 4 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM641001B/BL is packaged in a 400 mil 28-pin plastic SOJ.

ORDERING INFORMATION

KM641001B/BL -15/17/20	Commercial Temp.
KM641001BI/BLI -15/17/20	Industrial Temp.

PIN CONFIGURATION(Top View)



PIN FUNCTION

Pin Name	Pin Function
A0 - A17	Address Inputs
WE	Write Enable
CS	Chip Select
ŌĒ	Output Enable
1/01 ~ 1/04	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS*

Paramo	eter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss		VIN, VOUT	-0.5 to 7.0	V
Voltage on Vcc Supply R	elative to Vss	Vcc	-0.5 to 7.0	٧
Power Dissipation		Pp	1.0	W
Storage Temperature		Тѕтс	-65 to 150	°C.
Operating Temperature	Commercial	TA	0 to 70	Ĉ
	Industrial	TA	-40 to 85	°C

^{*} Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(TA = 0 to 70°C)

Parameter	Symbol	Min	Тур	Max	Unit
Supply Voltage	· Vcc	4.5	5.0	5.5	٧
Ground	Vss	0	. 0	0	٧
Input Low Voltage	ViH	2.2	-	Vcc + 0.5**	V
Input Low Voltage	VIL	-0.5*	-	0.8	٧

NOTE: Above parameters are also guaranteed at industrial temperature range.

DC AND OPERATING CHARACTERISTICS(TA = 0 to 70 °C, Vcc= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	` lu	Vin = Vss to Vcc		-2	2	μA
Output Leakage Current	ILO	CS=ViH or OE=ViH or WE=ViL Vout = Vss to Vcc		-2	2	μA
Operating Current	lcc	Min. Cycle, 100% Duty	15ns	-	120	
		CS=VIL, VIN = VIH or VIL,	17ns	-	110	mA
	IOUT=0mA	20ns	-	- 100	1	
Standby Current	ISB	Min. Cycle, CS=Viн		-	20	mA
	ISB1	f=0MHz, CS ≥ Vcc-0.2V,	Normal	-	5	
		$Vin \ge Vcc-0.2V \text{ or } Vin \le 0.2V$	L-Ver.	-	0.5	mA
Output Low Voltage Level	Vol	IoL=8mA.		-	0.4	V
Output High Voltage Level	Voн	loн=-4mA		2.4	-	V
	Von1*	lон1=-0.1mA		-	3.95	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

CAPACITANCE*(TA =25°C, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	CI/O	V1/0=0V	-	8	pF
Input Capacitance	Cin	Vin=0V	-	6	pF

^{*} NOTE: Capacitance is sampled and not 100% tested.



^{*} VIL(Min) = -2.0V a.c(Pulse Width≤10ns) for I ≤ 20mA

^{**} VIH(Max) = Vcc + 2.0V a.c (Pulse Width

10ns) for I

20mA

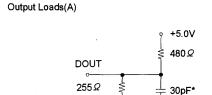
^{*} Vcc=5.0V ± 5% Temp. = 25°C

AC CHARACTERISTICS(TA = 0 to 70 °C, Vcc = 5.0V ± 10%, unless otherwise noted.)

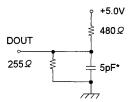
TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

NOTE: Above test conditions are also applied at industrial temperature range.



Output Loads(B) for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

	A	KM64100	1B/BL-15	KM64100	01B/BL-17	KM64100	01B/BL-20	1
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit
Read Cycle Time	tRC	15	-	17	-	20	-	ns
Address Access Time	tAA	-	15	-	17	-	20	ns
Chip Select to Output	tCO	-	15	-	17	-	20	ns
Output Enable to Valid Output	tOE	-	8	-	9	-	10	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	6	0	7	0	8	ns
Output Disable to High-Z Output	tOHZ	0	6	0	7	0	8	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	0	-	ns
Chip Selection to Power DownTime	tPD	-	15	-	17	-	20	ns

NOTE: Above parameters are also guaranteed at industrial temperature range.



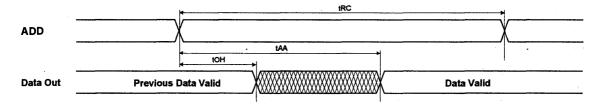
WRITE CYCLE

		KM6410	01B/BL-15	KM64100	KM641001B/BL-17		KM641001B/BL-20	
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit
Write Cycle Time	tWC	15	-	17	•	20	-	ns
Chip Select to End of Write	tCW	10	-	11	•	12	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	10	-	11	-	12	-	ns
Write Pulse Width(OE High)	tWP	10		11		12	-	ns
Write Pulse Width(OE Low)	tWP1	15	-	17	-	20	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	. 0	8	0	9	0	10	ns
Data to Write Time Overlap	tDW	7	-	8	-	9	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

NOTE: Above parameters are also guaranteed at industrial temperature range.

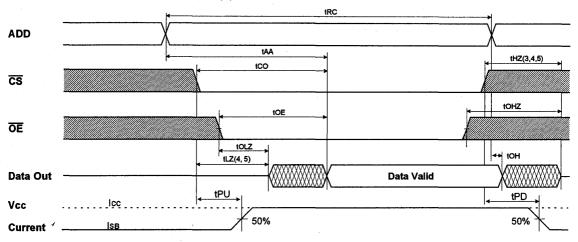
TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, CS=OE=VIL, WE=VIH)





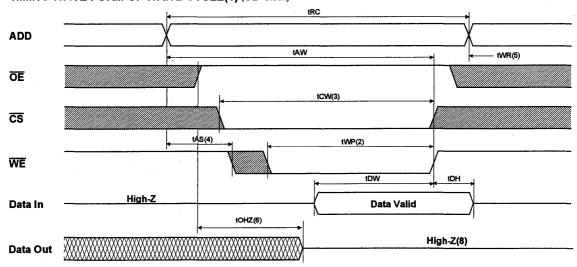
TIMING WAVE FORM OF READ CYCLE(2) (WE=VIH)



NOTES(READ CYCLE)

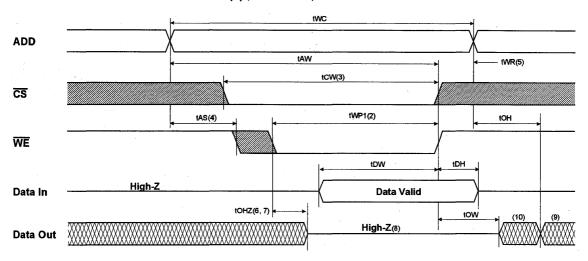
- 1. WE is high for read cycle.
- 2. All read cycle timing is referenced from the last valid address to the first transition address.
- 3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VoH or VoL Levels.
- 4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
- 5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
- 6. Device is continuously selected with CS=VIL.
- 7. Address valid prior to coincident with CS transition low.
- 8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVE FORM OF WRITE CYCLE(1) (OE=Clock)

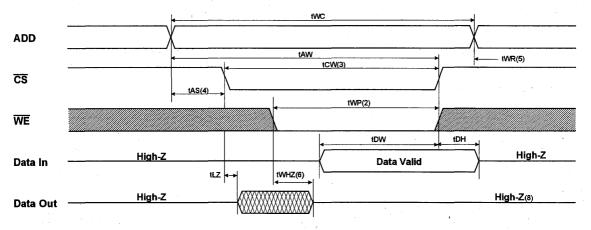




TIMING WAVE FORM OF WRITE CYCLE(2) (OE=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) (CS=Controlled)



NOTES(WRITE CYCLE)

- 1. All write cycle timing is referenced from the last valid address to the first transition address.
- 2. A write occurs during the overlap of a low \overline{CS} and \overline{WE} . A write begins at the latest transition \overline{CS} going low and \overline{WE} going low; A write ends at the earliest transition \overline{CS} going high or \overline{WE} going high. tWP is measured from the beginning of write to the end of write.
- 3. tCW is measured from the later of CS going low to end of write.
- 4. tAS is measured from the address valid to the beginning of write.
- 5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as \overline{CS} or \overline{WE} going high.
- 6. If \overline{OE} , \overline{CS} and \overline{WE} are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
- 7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
- 8. If CS goes low simultaneously with WE going or after WE going low, the outputs remain high impedance state.
- 9. Dout is the read data of the new address.
- 10. When \overline{CS} is low: I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

CS	WE	ŌĒ	Mode	I/O Pin	Supply Current
Н	X	X*	Not Select	High-Z	ISB, ISB1
L	н	Н	Output Disable	High-Z	lcc
· L	H	L	Read	Dout	lcc
L	L	Х	Write	Din	lcc

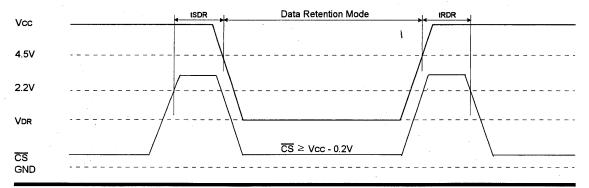
^{*} NOTE: X means Don't Care.

DATA RETENTION CHARACTERISTICS*(TA = 0° to 70°)

Parameter	Symbol	Symbol Test Condition		Тур.	Max.	Unit	
Vcc for Data Retention	VDR	CS ≥ Vcc - 0.2V	2.0	-	5.5	٧	
Data Retention Current	IDR	$Vcc = 3.0V, \overline{CS} \ge Vcc - 0.2V$ $Vin \ge Vcc - 0.2V \text{ or } Vin \le 0.2V$	-	-	0.40	mA	
		$ \begin{array}{c} \text{Vcc} = 2.0 \text{V, } \overline{\text{CS}} \geq \text{Vcc} - 0.2 \text{V} \\ \text{Vin} \geq \text{Vcc} - 0.2 \text{V or Vin} \leq 0.2 \text{V} \\ \end{array} $		-	0.35		
Data Retention Set-Up Time	tSDR	See Data Retention	0	-	-	ns	
Recovery Time	tRDR	Wave form(below)	5	-	-	ms	

NOTE: Above parameters are also guaranteed at industrial temperature range.

DATA RETENTION WAVE FORM(CS Controlled)



^{*} L-Ver only.

256K x 4 Bit (with OE)High-Speed CMOS Static RAM

FEATURES

- Fast Access Time 15, 17, 20 ns (Max.)
- · Low Power Dissipation

Standby (TTL) : 25mA(Max.)

(CMOS): 8mA(Max.)

Operating KM641001A - 15: 125mA(Max.)

KM641001A - 17: 125mA(Max.)

KM641001A - 20: 120mA(Max.)

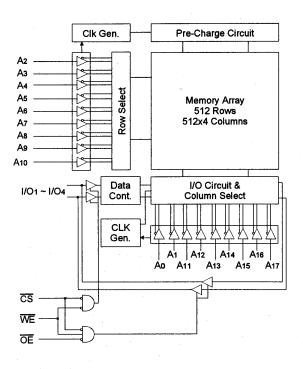
- Single 5.0V±10% Power Supply
- TTL Compatible Inputs and Outputs
- . I/O Compatible with 3.3V Device
- Fully Static Operation
- No Clock or Refresh required
- . Three State Outputs
- Standard Pin Configuration

KM641001AJ: 28-SOJ-400A

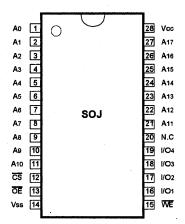
GENERAL DESCRIPTION

The KM641001A is a 1,048,576-bit high-speed Static Random Access Memory organized as 262,144 words by 4 bits. The KM641001A uses 4 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM641001A is packaged in a 400 mil 28-pin plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION(Top View)



PIN FUNCTION

Pin Name	Pin Function
A0 - A17	Address Inputs
WE	Write Enable
CS	Chip Select
ŌĒ	Output Enable
I/O1 ~ I/O4	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	VIN, VOUT	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	Vcc	-0.5 to 7.0	V
Power Dissipation	PD	1.0	W
Storage Temperature	Тѕтс	-65 to 150	°
Operating Temperature	TA	0 to 70	°

^{*} Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(TA = 0 to 70°C)

Parameter	Symbol	Min	Тур	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	٧
Ground	Vss	0	0	0	V
Input Low Voltage	VIH	2.2	-	Vcc + 0.5**	V
Input Low Voltage	VIL	-0.5*	-	0.8	٧

^{*} VIL(Min) = -2.0V a.c(Pulse Width≤10ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS(TA = 0 to 70 °C, Vcc= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Max	Unit	
Input Leakage Current	lu '	VIN = Vss to Vcc		-2	2	μA
Output Leakage Current	ILO	CS=ViH or OE=ViH or WE=ViL Vout = Vss to Vcc		-2	2	μA
Operating Current	Icc	Min. Cycle, 100% Duty	15ns	-	125	mA
		CS=VIL, VIN = VIH or VIL, 17ns -	L, 17ns	-	125	
		IOUT=0mA	20ns	-	120	
Standby Current	ISB	Min. Cycle, CS=Vін		-	25	mA
	ISB1	$f=0MHz$, $\overline{CS} \ge Vcc-0.2V$, $Vin \ge Vcc-0.2V$ or $Vin \le 0.2V$:	-	8	mA
Output Low Voltage Level	Vol	loL=8mA		-	0.4	٧
Output High Voltage Level	Voн	IOH=-4mA		2.4	-	V
	Von1*	Iон1=-0.1mA		-	3.95	V

^{*} Vcc=5.0V ± 5% Temp. = 25°C

CAPACITANCE*(TA =25°C, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	CI/O	Vi/o=0V		8	pF
Input Capacitance	CIN	Vin=0V	·	6	pF

^{*} NOTE: Capacitance is sampled and not 100% tested.



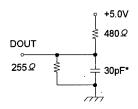
^{**} VIH(Max) = Vcc + 2.0V a.c (Pulse Width \le 10ns) for I \le 20mA

AC CHARACTERISTICS(TA = 0 to 70 $^{\circ}$ C, Vcc = 5.0V \pm 10%, unless otherwise noted.)

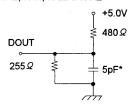
TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

Output Loads(A)



Output Loads(B) for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

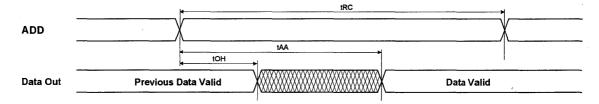
Parameter	a	KM641	001A-15	KM641	KM641001A-17		KM641001A-20	
	Symbol	Min	Max	Min	Max	Min	Max	- Unit
Read Cycle Time	tRC	15	-	17	-	20	-	ns
Address Access Time	tAA	-	15	-	17	-	20	ns
Chip Select to Output	tCO	-	15	-	17	-	20	ns
Output Enable to Valid Output	tOE	-	8	-	9	-	10	ns
Chip Enable to Low-Z Output	tLZ	3		3		3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	,0	6	0	7	0	8	ns
Output Disable to High-Z Output	tOHZ	0	6	0	7	0	8	ns
Output Hold from Address Change	tQH	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	0	-	ns
Chip Selection to Power DownTime	· tPD	-	15	-	17	-	20	ns

WRITE CYCLE

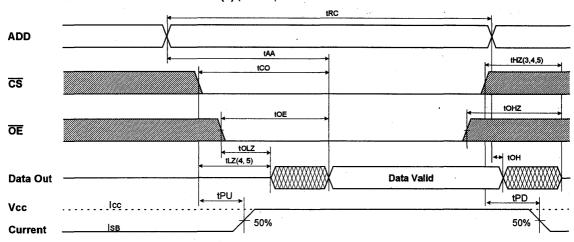
Parameter	S	KM641001A-15		KM641	KM641001A-17		KM641001A-20	
raiametei	Symbol	Min	Max	Min	Max	Min	Max	- Unit
Write Cycle Time	tWC	. 15	-	17	-	20	-	ns
Chip Select to End of Write	tCW	10	-	11	-	12	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	10	-	11	-	12	-	ns
Write Pulse Wrdth(OE High)	tWP	10	-	11 ·	-	12	-	ns
Write Pulse Width(OE Low)	tWP1	15	-	17	-	20	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	8	0	9	0.	10	ns
Data to Write Time Overlap	tDW	7	-	8	-	9	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	nş
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, CS=OE=VIL, WE=VIH)



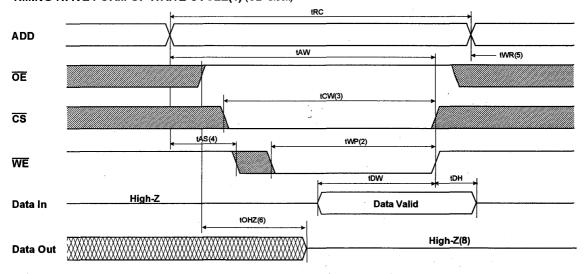
TIMING WAVE FORM OF READ CYCLE(2) (WE=VIH)



NOTES(READ CYCLE)

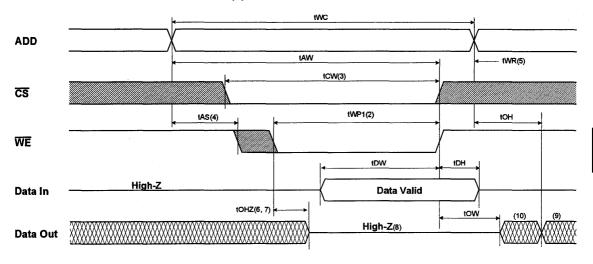
- 1. WE is high for read cycle.
- 2. All read cycle timing is referenced from the last valid address to the first transition address.
- 3 tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VoH or VoL Levels.
- 4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
- 5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
- 6. Device is continuously selected with CS=VIL.
- 7. Address valid prior to coincident with CS transition low.
- 8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVE FORM OF WRITE CYCLE(1) (OE=Clock)

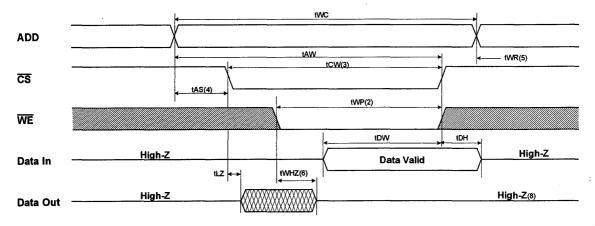




TIMING WAVE FORM OF WRITE CYCLE(2) (OE=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) (CS=Controlled)



KM641001A

NOTES(WRITE CYCLE)

- 1. All write cycle timing is referenced from the last valid address to the first transition address.
- 2. A write occurs during the overlap of a low \overline{CS} and \overline{WE} . A write begins at the latest transition \overline{CS} going low and \overline{WE} going low; A write ends at the earliest transition \overline{CS} going high or \overline{WE} going high. tWP is measured from the beginning of write to the end of write.
- 3. tCW is measured from the later of CS going low to end of write.
- 4. tAS is measured from the address valid to the beginning of write.
- 5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as CS or WE going high.
- 6. If OE, CS and WE are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
- 7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
- 8. If CS goes low simultaneously with WE going or after WE going low, the outputs remain high impedance state.
- 9. Dout is the read data of the new address.
- 10. When \overline{CS} is low: I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

ĊŚ	WE	ŌĒ	Mode	I/O Pin	Supply Current	
Н	X	X*	Not Select	High-Z	ISB, ISB1	
L	Н	Н	Output Disable	High-Z	Icc	
L	Н	L	Read	Dout	lcc	
L	L	Х	Write	DIN	Icc	

^{*} NOTE: X means Don't Care.

256K x 4 Bit (with OE)High-Speed CMOS Static RAM

FEATURES

- Fast Access Time 20,25,35 ns (Max.)
- . Low Power Dissipation

Standby (TTL) : 40mA(Max.)

(CMOS): 2mA(Max.)

0.5mA(Max.) - L-Ver. only

Operating KM641001/L - 20: 150mA(Max.)

KM641001/L - 25: 130mA(Max.)

KM641001/L - 35: 110mA(Max.)

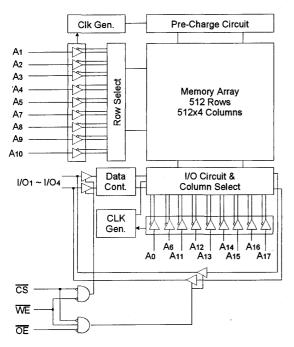
- Single 5.0V ± 10% Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
 - No Clock or Refresh required
- . Three State Outputs
- 2V Minimum Data Retention; 2V(Min.) L-ver. only
- . Standard Pin Configuration

KM641001/LP: 28-DIP-400 KM641001/LJ: 28-SOJ-400B

GENERAL DESCRIPTION

The KM641001/L is a 1,048,576-bit high-speed Static Random Access Memory organized as 262,144 words by 4 bits. The KM641001/L uses 4 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM641001/L is packaged in a 400 mil 28-pin plastic DIP or SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION(Top View)

	1		•	
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 CS OE	1 2 3 4 5 6 7 8 9 10 11 12	SOJ/DIP	28 27 26 25 24 23 22 21 20 19 18 17	Vcc A17 A16 A15 A14 A13 A12 A11 N.C I/O4 I/O3 I/O2 I/O1
ŌE Vss			16 15	I/O1 WE

PIN FUNCTION

Pin Name	Pin Function		
A0 - A17	Address Inputs		
WE	Write Enable		
cs	Chip Select		
ŌĒ	Output Enable		
I/O1 ~ I/O4	Data Inputs/Outputs		
Vcc	Power(+5.0V)		
Vss	Ground		
N.C	No Connection		



ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	VIN, VOUT	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	Vcc	-0.5 to 7.0	V
Power Dissipation	PD	1.0	W
Storage Temperature	Тѕтс	-65 to 150	°C
Operating Temperature	TA	0 to 70	°C

^{*} Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(TA = 0 to 70°C)

Parameter	Symbol	Min	Тур	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input Low Voltage	ViH	2.2	-	Vcc + 0.5**	٧
Input Low Voltage	VIL	-0.5*	-	0.8	V

^{*} VIL(Min) = -2.0V a.c(Pulse Width≤10ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS(TA = 0 to 70 °C, Vcc= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	ILI	Vin = Vss to Vcc		-2	2	μA
Output Leakage Current	lLO	CS =VIH or OE=VIH or WE=VIL VOUT = Vss to Vcc	-2	2	μA	
Operating Current	lcc	Min. Cycle, 100% Duty CS=VIL, VIN = VIH or VIL, IOUT=0mA	20ns	-	150	mA
			25ns	-	130	
			35ns	-	110	
Standby Current	İSB	Min. Cycle, CS=Viн		-	40	mA
	ISB1	f=0MHz, CS ≥ Vcc-0.2V,	Normal	-	2	mA
		$VIN \ge VCC-0.2V$ or $VIN \le 0.2V$	L-Ver.	-	0.5	1 1111
Output Low Voltage Level	VoL	IoL=8mA		-	0.4	V
Output High Voltage Level	Voн	Iон=-4mA		2.4	-	V

CAPACITANCE* (TA =25°C, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	CI/O	Vi/o=0V	-	7	pF
Input Capacitance	CIN	VIN=0V	-	7	pF

^{*} NOTE : Capacitance is sampled and not 100% tested.



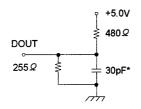
^{**} VIH(Max) = Vcc + 2.0V a.c (Pulse Width≤10ns) for I ≤ 20mA

AC CHARACTERISTICS(TA = 0 to 70 $^{\circ}$ C, Vcc = 5.0V \pm 10%, unless otherwise noted.)

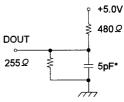
TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

Output Loads(A)



Output Loads(B) for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

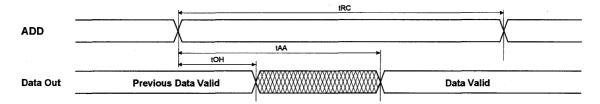
		KM641	KM641001/L-20		KM641001/L-25		KM641001/L-35	
Parameter	Symbol -	Min	Max	Min	Max	Min	Max	- Unit
Read Cycle Time	tRC	20	-	25	-	35	-	ns
Address Access Time	tAA	•	20	-	25	-	35	ns
Chip Select to Output	tCO	•	20	-	25	-	35	ns
Output Enable to Valid Output	tOE	-	10	-	13	-	15	ns
Chip Enable to Low-Z Output	tLZ	0	-	0	-	0	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	12	0 .	15	0	15	ns
Output Disable to High-Z Output	tOHZ	0	8	0	10	0	15	ns
Output Hold from Address Change	tOH	3	-	5	-	5	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	0	-	ns
Chip Selection to Power DownTime	tPD	-	20	-	25	-	35	ns

WRITE CYCLE

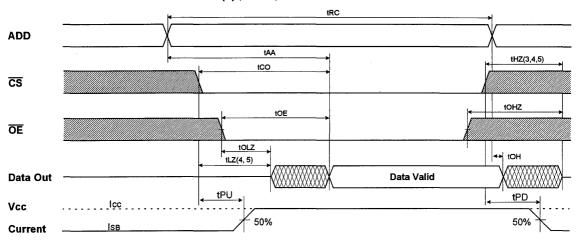
B	a	KM641001/L-20		KM641001/L-25		KM641001/L-35		1
Parameter	Symbol	Min	Max	Min	Max	Min	Max	- Unit
Write Cycle Time	tWC	20	-	25	-	35	-	ns
Chip Select to End of Write	tcW	17	-	20	-	30	-	ns
Address Set-up Time	tAS	0	-	0		0	-	ns
Address Valid to End of Write	tAW	17	-	20	-	30	-	ns
Write Pulse Width(OE High)	tWP	15	-	20	-	25		ns
Write Pulse Width(OE Low)	tWP1	20	-	25	-	35	-	ns
Write Recovery Time	tWR	2	-	3	-	3	-	ns
Write to Output High-Z	tWHZ	0	. 8	0	10	0	12	ns
Data to Write Time Overlap	tDW	12	-	15		20	-	ns
Data Hold from Write Time	tDH	0	-	0	-	Ö	-	ns
End Write to Output Low-Z	tOW	3	-	4	,-	5	-	ns

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS} = \overline{OE} = VIL, \overline{WE} = VIH)$



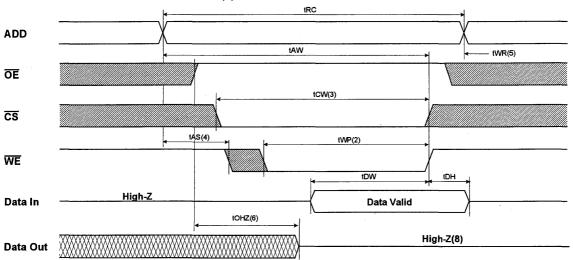
TIMING WAVE FORM OF READ CYCLE(2) (WE=VIH)



NOTES(READ CYCLE)

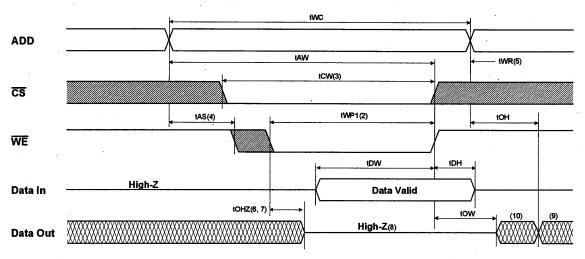
- 1. WE is high for read cycle.
- 2. All read cycle timing is referenced from the last valid address to the first transition address.
- 3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VoH or VoL Levels.
- 4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
- 5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
- 6. Device is continuously selected with CS=VIL.
- 7. Address valid prior to coincident with CS transition low.
- 8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVE FORM OF WRITE CYCLE(1) (OE=Clock)

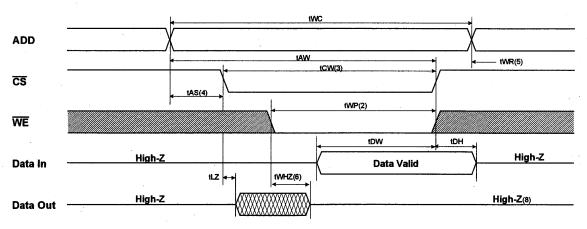




TIMING WAVE FORM OF WRITE CYCLE(2) (OE=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) (CS=Controlled)



NOTES(WRITE CYCLE)

- 1. All write cycle timing is referenced from the last valid address to the first transition address.
- 2. A write occurs during the overlap of a low $\overline{\text{CS}}$ and $\overline{\text{WE}}$. A write begins at the latest transition $\overline{\text{CS}}$ going low and $\overline{\text{WE}}$ going low; A write ends at the earliest transition \overline{CS} going high or \overline{WE} going high. tWP is measured from the beginning of write to the end of write.

 3. tCW is measured from the later of \overline{CS} going low to end of write.
- 4. tAS is measured from the address valid to the beginning of write.
- 5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as CS or WE going high.
- 6. If OE, CS and WE are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
- 7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
- 8. If CS goes low simultaneously with WE going or after WE going low, the outputs remain high impedance state.
- 9. Dout is the read data of the new address.
- 10. When CS is low: I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

<u>cs</u>	WE	ŌĒ	Mode	I/O Pin	Supply Current
Н	Х	X*	Not Select	High-Z	ISB, ISB1
L	Н	H	Output Disable	High-Z	lcc
L	Н	لــ	Read	Dout	Icc
L	L	Х	Write	DIN ,	lcc

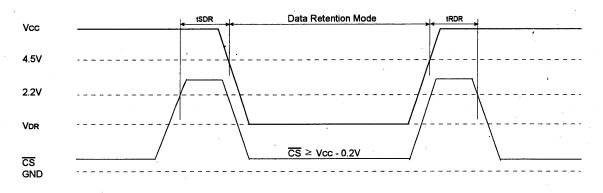
^{*} NOTE: X means Don't Care.

DATA RETENTION CHARACTERISTICS*(TA = 0° to 70°)

Parameter	Symbol	Test Condition	Min.	Тур.	Max.	Unit
Vcc for Data Retention	VDR	CS ≥ Vcc - 0.2V	2.0	-	5.5	٧
Data Retention Current	IDR	$Vcc = 2.0V$, $\overline{CS} \ge Vcc - 0.2V$ $Vin \ge Vcc - 0.2V$ or $Vin \le 0.2V$	-	-	0.1	mА
Data Retention Set-Up Time	tSDR	See Data Retention	0	-	-	ns
Recovery Time	tRDR	Wave form(below)	5	-	-	ms

^{*} NOTE : L-Ver only.

DATA RETENTION WAVE FORM(CS Controlled)





128K x 8 Bit High-Speed CMOS Static RAM

FEATURES

- Fast Access Time 8,10,12ns (Max.)
- · Low Power Dissipation

Standby (TTL) : 30mA(Max.) (CMOS): 10mA(Max.)

1mA(Max.) - L-Ver. only

Operating KM681002B/BL - 8: 160mA(Max.)

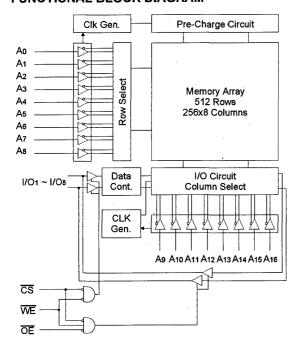
KM681002B/BL - 10: 150mA(Max.)

KM681002B/BL - 12: 140mA(Max.)

- Single 5.0V ± 10% Power Supply
- . TTL Compatible Inputs and Outputs
- . I/O Compatible with 3.3V Device
- . Fully Static Operation
 - No Clock or Refresh required
- . Three State Outputs
- . 2V Minimum Data Retention; L-Ver. only
- Center Power/Ground Pin Configuration
- . Standard Pin Configuration

KM681002B/BLJ: 32-SOJ-400 KM681002B/BLSJ: 32-SOJ-300 KM681002B/BLT: 32-TSOP2-400F

FUNCTIONAL BLOCK DIAGRAM



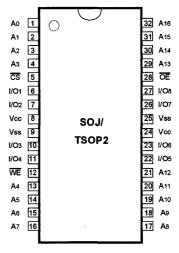
GENERAL DESCRIPTION

The KM681002B/BL is a 1,048,576-bit high-speed Static Random Access Memory organized as 131,072 words by 8 bits. The KM681002B/BL uses 8 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM681002B/BL is packaged in a 400/300 mil 32-pin plastic SOJ or TSOP2 forward.

ORDERING INFORMATION

KM681002B/BL -8/10/12	Commercial Temp.			
KM681002BI/BLI -8/10/12	Industrial Temp.			

PIN CONFIGURATION(Top View)



PIN FUNCTION

Pin Name	Pin Function
A0 - A16	Address Inputs
WE	Write Enable
CS	Chip Select
Œ	Output Enable
I/O1 ~ I/O8	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground
N.C	No Connection



ABSOLUTE MAXIMUM RATINGS*

Param	eter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss		VIN, VOUT	-0.5 to 7.0	V .
Voltage on Vcc Supply Relative to Vss		Vcc	-0.5 to 7.0	. V
Power Dissipation Storage Temperature		Po	1.0	W
		Тѕтҫ	-65 to 150	င
Operating Temperature	Commercial	TA	0 to 70	°C
	Industrial	TA	-40 to 85	Ĉ

^{*} Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(TA = 0 to 70°C)

Parameter	Symbol	Min	Тур	Max .	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input Low Voltage	ViH	2.2	-	Vcc + 0.5**	V
Input Low Voltage	VIL	-0.5*	-	0.8	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

- * $VIL(Min) = -2.0V \text{ a.c}(Pulse Width \le 6ns) \text{ for } 1 \le 20\text{ mÅ}$
- ** VIH(Max) = Vcc + 2.0V a.c (Pulse Width ≤ 6ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS(TA = 0 to 70 °C, Vcc= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions	Test Conditions		Max	Unit
Input Leakage Current	lu	Vin = Vss to Vcc		-2	2	μA
Output Leakage Current	ILO	CS=VIH or OE=VIH or WE=VIL VOUT = Vss to Vcc	-2	2	μА	
Operating Current	lcc	Min. Cycle, 100% Duty	8ns	-	160	mA
	$\overline{CS}=VIL, VIN = VIH \text{ or } VIL,$ $IOUT=0mA$	CS=VIL, VIN = VIH or VIL,	10ns	-	150	1
		IOUT=UMA	12ns	-	140	
Standby Current	ISB	Min. Cycle, CS=Viн		-	30	mA
·	ISB1	f=0MHz, CS ≥ Vcc-0,2V,		•	10	mA
i.		$Vin \ge Vcc-0.2V \text{ or } Vin \le 0.2V$	L-Ver.	-	1	
Output Low Voltage Level	Vol	IoL=8mA			0.4	- V
Output High Voltage Level	Voн	IOH=-4mA IOH1=-0.1mA		2.4	-	٧
	Von1*			-	3.95	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

CAPACITANCE*(TA =25°C, f=1.0MHz)

ltem	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	CI/O	Vi/o=0V	-	8	pF
Input Capacitance	Cin	Vin=0V	-	6.	pF

^{*} NOTE: Capacitance is sampled and not 100% tested.

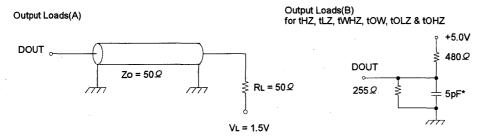


^{*} Vcc=5.0V ± 5% Temp. = 25℃

AC CHARACTERISTICS(TA = 0 to 70 $^{\circ}$ C, Vcc = 5.0V \pm 10%, unless otherwise noted.) TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns .
Input and Output timing Reference Levels	1.5V
Output Loads	See below

NOTE: Above test conditions are also applied at industrial temperature range.



* Including Scope and Jig Capacitance

READ CYCLE

Parameter		KM681002B/BL-8		KM681002B/BL-10		KM681002B-12		1
	Symbol	Min	Max	Min	Max	Min	Max	- Unit
Read Cycle Time	tRC	8	-	10	-	12	-	ns
Address Access Time	tAA	•	8	-	10	-	12	ns
Chip Select to Output	tCO '	-	8	-	10	-	12	ns
Output Enable to Valid Output	tOE	-	4	-	5	-	6	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	- 1	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0.	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	4	0	5	0	6	ns
Output Disable to High-Z Output	tOHZ	0	4	0	. 5	0	6	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	0	-	ns
Chip Selection to Power DownTime	tPD	-	8	-	10	-	12	ns

NOTE: Above parameters are also guaranteed at industrial temperature range.

WRITE CYCLE

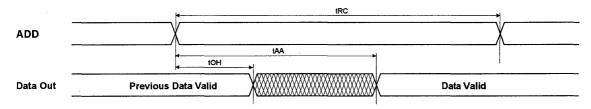
Parameter		KM681002B/BL-8		KM681002B/BL-10		KM681002B/BL-12		11-14
	Symbol	Min	Max	Min	Max	Min	Max	- Unit
Write Cycle Time	tWC	8	-	10	-	12	-	ns
Chip Select to End of Write	tCW	6	-	7	-	8	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	6	-	7	-	8	-	ns
Write Pulse Width(OE High)	tWP	6	· -	7	-	8	-	ns
Write Pulse Width(OE Low)	tWP1	8	-	10	-	12	-	ns
Write Recovery Time	tWR	0	-	. 0	-	0	-	ns
Write to Output High-Z	tWHZ	0	4	0	5	0	6	ns
Data to Write Time Overlap	tDW	4	-	5	-	6	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

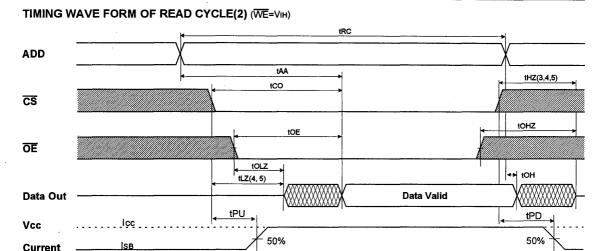
NOTE: Above parameters are also guaranteed at industrial temperature range.

KM681002B/BL, KM681002BI/BLI

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, CS=OE=VIL, WE=VIH)

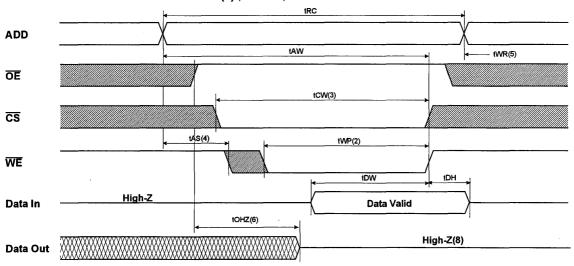




NOTES(READ CYCLE)

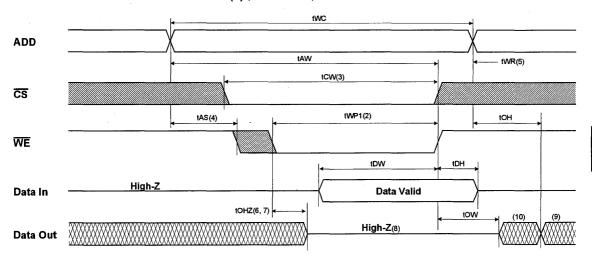
- 1. WE is high for read cycle.
- 2. All read cycle timing is referenced from the last valid address to the first transition address.
- 3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VoH or VoL Levels.
- 4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
- 5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
- 6. Device is continuously selected with CS=ViL.
- 7. Address valid prior to coincident with CS transition low.
- 8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVE FORM OF WRITE CYCLE(1) (OE=Clock)

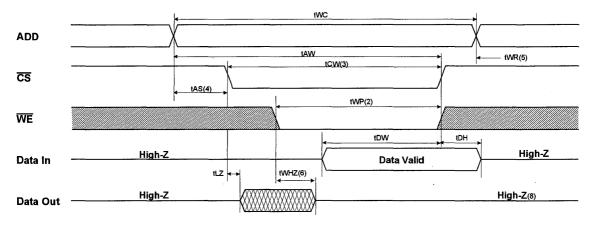




TIMING WAVE FORM OF WRITE CYCLE(2) (OE=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) (CS=Controlled)



NOTES(WRITE CYCLE)

- 1. All write cycle timing is referenced from the last valid address to the first transition address.
- 2. A write occurs during the overlap of a low \overline{CS} and \overline{WE} . A write begins at the latest transition \overline{CS} going low and \overline{WE} going low; A write ends at the earliest transition \overline{CS} going high or \overline{WE} going high. tWP is measured from the beginning of write to the end of write.
- 3. tCW is measured from the later of CS going low to end of write.
- 4. tAS is measured from the address valid to the beginning of write.
- 5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as CS or WE going high.
- 6. If \overline{OE} , \overline{CS} and \overline{WE} are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
- 7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
- 8. If $\overline{\text{CS}}$ goes low simultaneously with $\overline{\text{WE}}$ going or after $\overline{\text{WE}}$ going low, the outputs remain high impedance state.
- 9. Dout is the read data of the new address.
- 10. When $\overline{\text{CS}}$ is low: I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

CS	WE	ŌĒ	Mode	I/O Pin	Supply Current
H	Х	X*	Not Select	High-Z	ISB, ISB1
L	Н	Н	Output Disable	High-Z	lcc
L	. Н	L	Read	Dout	lcc
L	L	Х	Write	Din	lcc

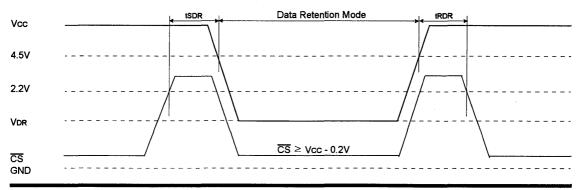
^{*} NOTE: X means Don't Care.

DATA RETENTION CHARACTERISTICS*(TA = 0° to 70°)

Parameter	Symbol	Symbol Test Condition VDR CS ≥ Vcc - 0.2V		Тур.	Max.	Unit	
Vcc for Data Retention	VDR			-	5.5	٧	
Data Retention Current	IDR	IDR $Vcc = 3.0V, \overline{CS} \ge Vcc - 0.2V$ $Vin \ge Vcc - 0.2V$ or $Vin \le 0.2V$		-	0.9	mA	
		$Vcc = 2.0V, \overline{CS} \ge Vcc - 0.2V$ $Vin \ge Vcc - 0.2V$ or $Vin \le 0.2V$	-		0.7		
Data Retention Set-Up Time	tSDR	See Data Retention	0	-	-	ns	
Recovery Time	tRDR	Wave form(below)	5	_	-	ms	

NOTE: Above parameters are also guaranteed at industrial temperature range.

DATA RETENTION WAVE FORM(CS Controlled)





^{*} L-Ver only.

128K x 8 Bit High-Speed CMOS Static RAM

FEATURES

- Fast Access Time 8,10,12ns (Max.)
- Low Power Dissipation

Standby (TTL) : 60mA(Max.)

(CMOS): 10mA(Max.)

Operating KM68B1002 - 8: 175mA(Max.)

KM68B1002 - 10: 165mA(Max.)

KM68B1002 - 12: 155mA(Max.)

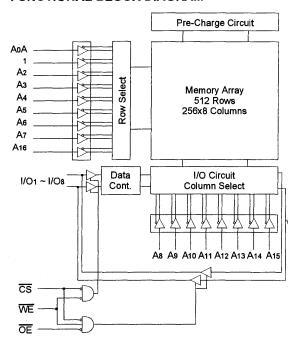
- Single 5.0V ± 10% Power Supply
- TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Device
- · Fully Static Operation
- No Clock or Refresh required
- · Three State Outputs
- · Center Power/Ground Pin Configuration
- · Standard Pin Configuration

KM68B1002J: 32-SOJ-400

GENERAL DESCRIPTION

The KM68B1002 is a 1,048,576-bit high-speed Static Random Access Memory organized as 131,072 words by 8 bits. The KM68B1002 uses 8 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using Samsung's advanced BiCMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM68B1002 is packaged in a 400 mil 32-pin plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION(Top View)

	 ,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	
A0 1	\bigcup	32 A16
A1 2		31 A ₁₅
A2 3		30 A14
A3 4		29 A13
CS 5		28 O E
1/01 6		27 I/O8
1/02 7		26 1/07
Vcc 8	SOJ	25 Vss
Vss 9		24 Vcc
I/O3 10		23 1/06
I/O4 11		22 1/05
WE 12		21 A12
A4 13		20 A ₁₁
A5 14		19 A10
A6 15		18 A9
A7 16		17 A8
l	 	

PIN FUNCTION

Pin Name	Pin Function
A0 - A16	Address Inputs
WE	Write Enable
CS	Chip Select
ŌĒ	Output Enable
I/O1 ~ I/O8	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground
N.C	No Connection



ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	VIN, VOUT	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	Vcc	-0.5 to 7.0	V
Power Dissipation	PD	1.0	W
Storage Temperature	Тѕтс	-65 to 150	°C
Operating Temperature	TA	0 to 70	°C

^{*} Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(TA = 0 to 70°C)

Parameter	Symbol	Min	Тур	Max	Unit
Supply Voltage	, Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input Low Voltage	ViH	2.2	-	Vcc + 0.5**	V
Input Low Voltage	VIL	-0.5*	-	0.8	V

^{*} VIL(Min) = -2.0V a.c(Pulse Width≤6ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS(TA = 0 to 70 °C, Vcc= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	ILI	Vin = Vss to Vcc		-2	2	μA
Output Leakage Current	lLO	CS=ViH or OE=ViH or WE=ViL Vout = Vss to Vcc		-10	10	μA
Operating Current	Icc	Min. Cycle, 100% Duty CS=VIL, VIN = VIH or VIL, IOUT=0mA	8ns	-	175	mA
			10ns	-	165	
			12ns	-	155	
Standby Current	İSB	Min. Cycle, CS=Viн		-	60	mA
	ISB1	f=0MHz, $\overline{CS} \ge Vcc-0.2V$, Vin $\ge Vcc-0.2V$ or Vin $\le 0.2V$		-	10	mA
Output Low Voltage Level	Vol	loL=8mA		-	0.4	V
Output High Voltage Level	Voн	IOH=-4mA		2.4	-	V

CAPACITANCE*(TA =25°C, f=1.0MHz)

ltem .	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	CI/O	Vi/o=0V	-	8	pF
Input Capacitance	CIN	Vin=0V	-	7	pF

^{*} NOTE: Capacitance is sampled and not 100% tested.



^{**} VIH(Max) = VCC + 2.0V a.c (Pulse Width ≤ 6ns) for I ≤ 20 mÅ

AC CHARACTERISTICS(TA = 0 to 70 $^{\circ}$ C, Vcc = 5.0V $^{\pm}$ 10%, unless otherwise noted.)

TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

* Including Scope and Jig Capacitance

READ CYCLE

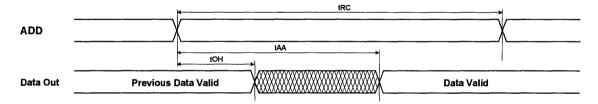
D	Cumbal	KM68B1002-8		KM68B1002-10		KM68B1002-12		T
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit
Read Cycle Time	tRC	8	-	10	-	12	-	ns
Address Access Time	tAA	-	8	_	10	-	12	ns
Chip Select to Output	tCO	-	8	-	10 .	-	12	ns
Output Enable to Valid Output	tOE	-	4	-	5	-	6	ns
Chip Enable to Low-Z Output Access	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	4	0	5 .	0	6	ns
Output Disable to High-Z Output	tOHZ	0	4	0	5	0	6	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns

WRITE CYCLE

Parameter		KM68B1002-8		KM68B1002-10		KM68B1002-12		T
	Symbol	Min	Max	Min	Max	Min	Max	Unit
Write Cycle Time	tWC	8	-	10	-	12	-	ns
Chip Select to End of Write	tcw	6	-	7	-	8	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	6	-	7	-	8	-	ns
Write Pulse Width(OE High)	tWP	6	-	7	-	8	-	ns
Write Pulse Width(OE Low)	tWP1	8	-	9	-	10	-	ns
Write Recovery Time	tWR	1	-	1	-	1	-	ns
Write to Output High-Z	tWHZ	0	4	0	5	0	6	ns
Data to Write Time Overlap	tDW	4	-	5	-	6	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

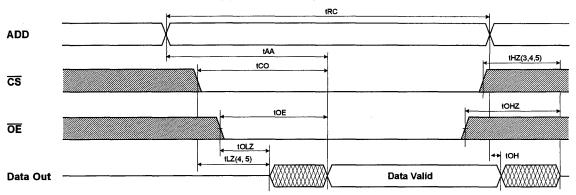
TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS} = \overline{OE} = VIL, \overline{WE} = VIH)$





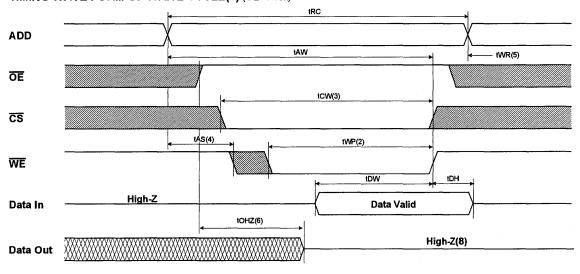
TIMING WAVE FORM OF READ CYCLE(2) (WE=VIH)



NOTES(READ CYCLE)

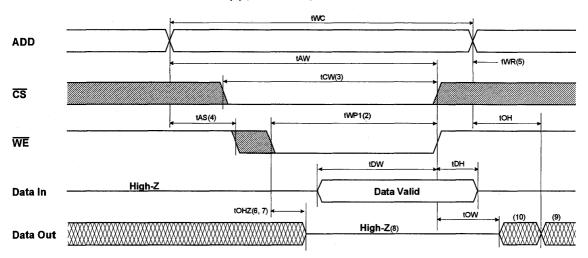
- 1. WE is high for read cycle.
- 2. All read cycle timing is referenced from the last valid address to the first transition address.
- 3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VoH or VoL Levels.
- 4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
- 5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
- 6. Device is continuously selected with CS=VIL.
- 7. Address valid prior to coincident with CS transition low.
- 8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVE FORM OF WRITE CYCLE(1) (OE=Clock)

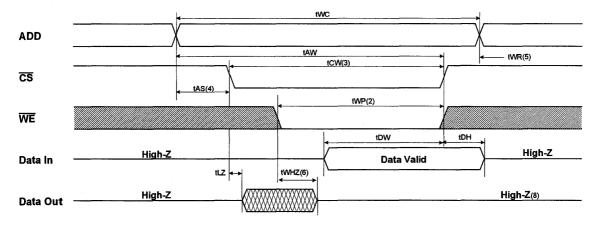




TIMING WAVE FORM OF WRITE CYCLE(2) (OE=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) (CS=Controlled)



NOTES(WRITE CYCLE)

- 1. All write cycle timing is referenced from the last valid address to the first transition address.
- A write occurs during the overlap of a low CS and WE. A write begins at the latest transition CS going low and WE going low; A write ends at the earliest transition CS going high or WE going high. tWP is measured from the beginning of write to the end of write.
 tCW is measured from the later of CS going low to end of write.
- 4. tAS is measured from the address valid to the beginning of write.
- 5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as CS or WE going high.
- 6. If OE, CS and WE are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
- 7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
- 8. If $\overline{\text{CS}}$ goes low simultaneously with $\overline{\text{WE}}$ going or after $\overline{\text{WE}}$ going low, the outputs remain high impedance state.
- 9. Dout is the read data of the new address.
- 10. When CS is low: I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

CS	WE	ŌĒ	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	ISB, ISB1
L	Н	Н	Output Disable	High-Z	Icc
L	Н	L	Read	Dout	lcc
L	L	Х	Write	Din	Icc

^{*} NOTE : X means Don't Care.

128K x 8 Bit High-Speed CMOS Static RAM

FEATURES

- Fast Access Time 12, 15, 17, 20 ns (Max.)
- · Low Power Dissipation

Standby (TTL) : 25mA(Max.)

(CMOS): 8mA(Max.)

Operating KM681002A - 12: 170mA(Max.)

KM681002A - 15: 165mA(Max.)

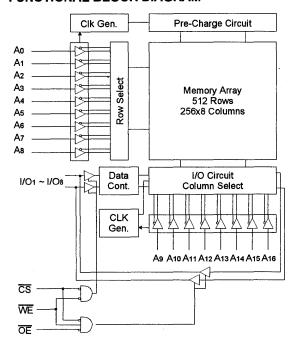
KM681002A - 17: 165mA(Max.)

KM681002A - 20: 160mA(Max.)

- Single 5.0V±10% Power Supply
- . TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Device
- Fully Static Operation
 - No Clock or Refresh required
- Three State Outputs
 Center Payer/Cround Pir
- · Center Power/Ground Pin Configuration
- · Standard Pin Configuration

KM681002AJ: 32-SOJ-400 KM681002ASJ: 32-SOJ-300 KM681002AT: 32-TSOP2-400F

FUNCTIONAL BLOCK DIAGRAM



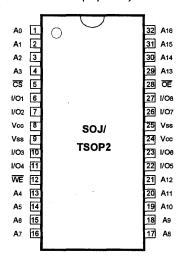
GENERAL DESCRIPTION

The KM681002A is a 1,048,576-bit high-speed Static Random Access Memory organized as 131,072 words by 8 bits. The KM681002A uses 8 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM681002A is packaged in a 400/300 mil 32-pin plastic SOJ or TSOP2 forward.

ORDERING INFORMATION

KM681002A -12/15/17/20	Commercial Temp.
KM681002AI -12/15/17/20	Industrial Temp.

PIN CONFIGURATION(Top View)



PIN FUNCTION

Pin Name	Pin Function
A0 - A16	Address Inputs
WE	Write Enable
CS	Chip Select
ŌĒ	Output Enable
I/O1 ~ I/O8	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground

ABSOLUTE MAXIMUM RATINGS*

Param	eter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss		VIN, VOUT	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss		Vcc	-0.5 to 7.0	. V
Power Dissipation		Po	1.0	W
Storage Temperature	Storage Temperature		-65 to 150	°C
Operating Temperature	Commercial	TA	0 to 70	°C
	Industrial	TA	-40 to 85	°C

^{*} Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(TA = 0 to 70°C)

Parameter	Symbol	Min	Тур	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input Low Voltage	ViH	2.2	-	Vcc + 0.5**	V
Input Low Voltage	VIL	-0.5*	-	0.8	٧

NOTE: Above parameters are also guaranteed at industrial temperature range.

- * VIL(Min) = -2.0V a.c(Pulse Width≤10ns) for I ≤ 20mA
- ** VIH(Max) = VCC + 2.0V a.c (Pulse Width \leq 10ns) for I \leq 20mÅ

DC AND OPERATING CHARACTERISTICS(TA = 0 to 70 °C, Vcc= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	ILI	Vin = Vss to Vcc		-2	2	μA
Output Leakage Current	lLO	CS=Vih or OE=Vih or WE=Vil Vout = Vss to Vcc		-2	2	μA
Operating Current	Icc	Min. Cycle, 100% Duty	12ns	-	170	mA
		CS=VIL, VIN = VIH or VIL, IOUT=0mA	15ns	-	165	
			17ns	-	165	
			20ns	-	160	ĺ
Standby Current	ISB	Min. Cycle, CS=Viн		-	25	mA
	ISB1 $f=0MHz$, $\overline{CS} \ge Vcc-0.2V$, $Vin \ge Vcc-0.2V$ or $Vin \le 0.2V$			-	8	mA
Output Low Voltage Level	VoL	IoL=8mA		-	0.4	V
Output High Voltage Level	VoH	IOH=-4mA		2.4	-	V
	Vон1*	IOH1=-0.1mA		-	3.95	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

CAPACITANCE* (TA =25°C, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	CI/O	VI/o=0V	-	8	pF
Input Capacitance	Cin	Vin=0V	-	6	pF

^{*} NOTE: Capacitance is sampled and not 100% tested.



^{*} Vcc=5.0V \pm 5% Temp. = 25 $^{\circ}$ C

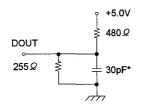
AC CHARACTERISTICS(Ta = 0 to 70 °C, Vcc = $5.0V \pm 10\%$, unless otherwise noted.)

TEST CONDITIONS

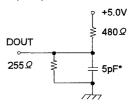
Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

NOTE: Above test conditions are also applied at industrial temperature range.

Output Loads(A)



Output Loads(B) for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

Parameter ,	G	KM681	002A-12	KM681	002A-15	KM681	002A-17	KM681	002A20	Unit
	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Read Cycle Time	tRC	12	-	15	-	17	-	20	-	ns
Address Access Time	tAA	-	12	-	15	-	17	7	20	ns
Chip Select to Output	tCO	_	12	-	15	-	17	-	20	ns
Output Enable to Valid Output	tOE	-	6		7	-	8	-	9	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	6	0	7	0	8	0	9	ns
Output Disable to High-Z Output	tOHZ	0	6	0	7	0	8	0	9	ns
Output Hold from Address Change	tOH	3	-	3		3	-	3	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	0	-	0	-	ns
Chip Selection to Power DownTime	tPD	-	12	-	15	-	17	-	20	ns

NOTE: Above parameters are also guaranteed at industrial temperature range.



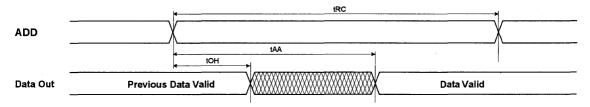
WRITE CYCLE

Parameter	6b.d	KM681002A-12		KM681002A-15		KM681002A-17		KM681002A-20		Unit
	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Write Cycle Time	tWC	12	-	15	-	17	-	20	-	ns
Chip Select to End of Write	tCW	8	-	10	-	11	-	12	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	8	-	10	-	11	-	12	-	ns
Write Pulse Width(OE High)	tWP	8	-	10	-	11	-	12	-	ns
Write Pulse Width(OE Low)	tWP1	12	-	15	-	17		20	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	6	0	7	0	8	0	9	ns
Data to Write Time Overlap	tDW	6	-	7	-	8	-	9	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3		3	-	ns

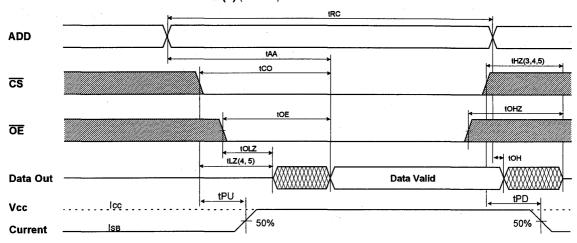
NOTE: Above parameters are also guaranteed at industrial temperature range.

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS} = \overline{OE} = VIL, \overline{WE} = VIH)$



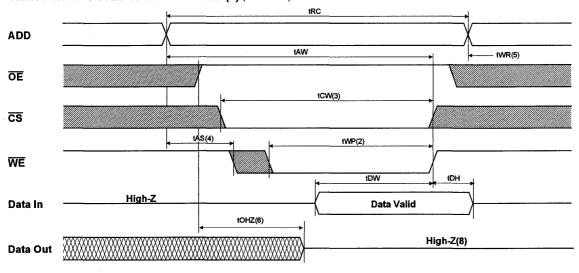
TIMING WAVE FORM OF READ CYCLE(2) (WE=VIH)



NOTES(READ CYCLE)

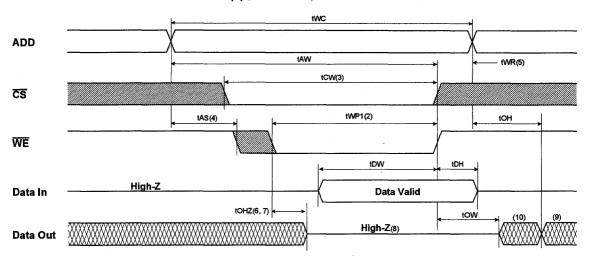
- 1. WE is high for read cycle.
- 2. All read cycle timing is referenced from the last valid address to the first transition address.
- 3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VoH or VoL Levels.
- 4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
- 5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
- 6. Device is continuously selected with CS=VIL.
- 7. Address valid prior to coincident with CS transition low.
- 8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVE FORM OF WRITE CYCLE(1) (OE=Clock)

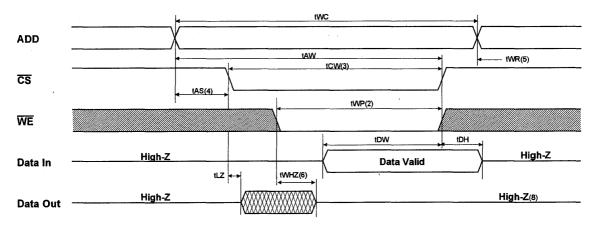




TIMING WAVE FORM OF WRITE CYCLE(2) (OE=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) (CS=Controlled)



NOTES(WRITE CYCLE)

- 1. All write cycle timing is referenced from the last valid address to the first transition address.
- 2. A write occurs during the overlap of a low \overline{CS} and \overline{WE} . A write begins at the latest transition \overline{CS} going low and \overline{WE} going low; A write ends at the earliest transition \overline{CS} going high or \overline{WE} going high. tWP is measured from the beginning of write to the end of write.
- 3. tCW is measured from the later of CS going low to end of write.
- 4. tAS is measured from the address valid to the beginning of write.
- 5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as CS or WE going high.
- 6. If \overline{OE} , \overline{CS} and \overline{WE} are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
- 7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
- 8. If $\overline{\text{CS}}$ goes low simultaneously with $\overline{\text{WE}}$ going or after $\overline{\text{WE}}$ going low, the outputs remain high impedance state.
- 9. Dout is the read data of the new address.
- 10. When $\overline{\text{CS}}$ is low: I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

ĊS	WE	ŌĒ	Mode	I/O Pin	Supply Current
Н	Х	X*	Not Select	High-Z	ISB, ISB1
L	Н	Τ	Output Disable	High-Z	Icc
L	Н	L	Read	Dout	lcc
L	L	Х	Write	DIN	lcc

^{*} NOTE: X means Don't Care.



128K x 8 Bit High-Speed CMOS Static RAM

FEATURES

- Fast Access Time 15, 17, 20 ns (Max.)
- · Low Power Dissipation

Standby (TTL) : 40mA(Max.)

(CMOS): 10mA(Max.)

Operating KM681002 - 15: 170mA(Max.)

KM681002 - 17: 160mA(Max.)

KM681002 - 20: 150mA(Max.)

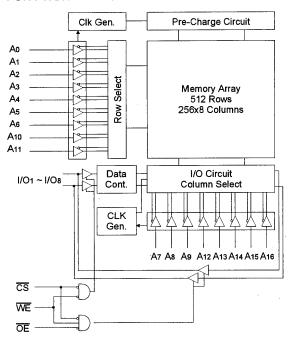
- Single 5.0V ± 10% Power Supply
- . TTL Compatible Inputs and Outputs
- . I/O Compatible with 3.3V Device
- Fully Static Operation
 - No Clock or Refresh required
- Three State Outputs
- · Center Power/Ground Pin Configuration
- . Standard Pin Configuration

KM681002J: 32-SOJ-400

GENERAL DESCRIPTION

The KM681002 is a 1,048,576-bit high-speed Static Random Access Memory organized as 131,072 words by 8 bits. The KM681002 uses 8 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM681002 is packaged in a 400 mil 32-pin plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION(Top View)

	1	 			
A 0	1	\bigcup	3	32	A16
A 1	2			31	A 15
A2	3		3	30	A14
Аз	4		2	29	A13
CS	5		2	28	Œ
I/O1	6		2	27	I/O8
1/02	7		12	26	1/07
Vcc	8	SOJ	3	25	Vss
Vss	9		2	24	Vcc
I/O3	10		2	23	I/ O 6
1/04	11		2	22	I/ O 5
WE	12		2	21	A12
A4	13		2	20	A11
A 5	14		1	19	A1 0
A6	15			18	A 9
A 7	16		1	17	A 8

PIN FUNCTION

Pin Name	Pin Function
A0 - A16	Address Inputs
WE	Write Enable
cs	Chip Select
ŌĒ	Output Enable
I/O1 ~ I/O8	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground



ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	Vin, Vout	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	Vcc	-0.5 to 7.0	V
Power Dissipation	PD	1.0	W
Storage Temperature	Тѕтс	-65 to 150	C
Operating Temperature	TA	0 to 70	C

^{*} Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(TA = 0 to 70°C)

Parameter	Symbol	Min	Тур	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	٧
Ground	Vss	0	0	0	V
Input Low Voltage	ViH	2.2	-	Vcc + 0.5**	V
Input Low Voltage	VIL	-0.5*	-	0.8	V

^{*} VIL(Min) = -2.0V a.c(Pulse Width≤10ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS(TA = 0 to 70 °C, Vcc= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Max	Unit	
Input Leakage Current	İLI	Vin = Vss to Vcc		-2	2	μA
Output Leakage Current	lLO	CS=ViH or OE=ViH or WE=ViL Vout = Vss to Vcc	-2	2	μA	
Operating Current	Icc	Min. Cycle, 100% Duty	15ns	-	170	mΑ
		CS=VIL, VIN = VIH or VIL,	17ns	-	160	1
	i	IOUT=0mA	-	150		
Standby Current	ISB	Min. Cycle, CS=Viн		-	40	mA
	ISB1	$f=0MHz$, $\overline{CS} \ge Vcc-0.2V$, $Vin \ge Vcc-0.2V$ or $Vin \le 0.2V$	-	10	mA	
Output Low Voltage Level	VoL	IoL=8mA		-	0.4	V
Output High Voltage Level	Voн	IOH=-4mA		2.4	-	V
•	Vон1*	Iон1=-0.1mA	-	3.95	V	

^{*} Vcc=5.0V ± 5% Temp. = 25 ℃

CAPACITANCE*(TA =25°C, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	CI/O	V1/0=0V	-	8	pF
Input Capacitance	CIN	VIN=0V	-	6	pF

^{*} NOTE: Capacitance is sampled and not 100% tested.



^{**} VIH(Max) = Vcc + 2.0V a.c (Pulse Width≤10ns) for I ≤ 20mA

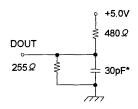
AC CHARACTERISTICS(TA = 0 to 70 ℃, Vcc = 5.0V ± 10%, unless otherwise noted.)

TEST CONDITIONS

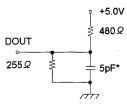
Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3 ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

NOTE: Above test conditions are also applied at industrial temperature range.





Output Loads(B) for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

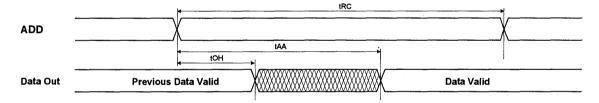
Parameter		KM681	31002-15 KM6810		1002-17	KM68	KM681002-20	
	Symbol -	Min	Max	Min	Max	Min	Max	- Unit
Read Cycle Time	tRC	15	-	17	-	20	-	ns
Address Access Time	tAA	-	15	-	17	-	20	ns
Chip Select to Output	tCO	_	15	-	17	-	20	ns
Output Enable to Valid Output	tOE	-	8	-	9	-	10	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	6	0	7	0	8	ns
Output Disable to High-Z Output	tOHZ	0	6	0	7	0	8	ns
Output Hold from Address Change	tOH	3	-	3	-	4	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	0	•	ns
Chip Selection to Power DownTime	tPD	-	15	-	17	_	20	ns

WRITE CYCLE

Parameter		KM681002-15		KM681002-17		KM681002-20		[,]
	Symbol	Min	Max	Min	Max	Min	Max	Unit
Write Cycle Time	tWC	15	-	17	-	20	-	ns
Chip Select to End of Write	tCW	12	-	12	-	13	-	ns
Address Set-up Time	tAS	0	-	0	-	. 0	-	ns
Address Valid to End of Write	tAW	12	-	12	-	13	-	ns
Write Pulse Width(OE High)	tWP	9	-	10	-	11		ns
Write Pulse Width(OE Low)	tWP1	15	-	17	-	20	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	8	0	8	0	10	ns
Data to Write Time Overlap	tDW	8	-	9	-	10	-	ns
Data Hold from Write Time	tDH	0	_	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	4	-	5	-	ns

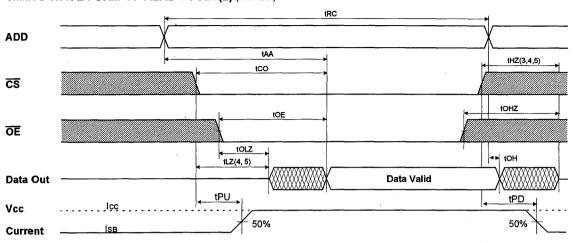
TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS} = \overline{OE} = VIL, \overline{WE} = VIH)$





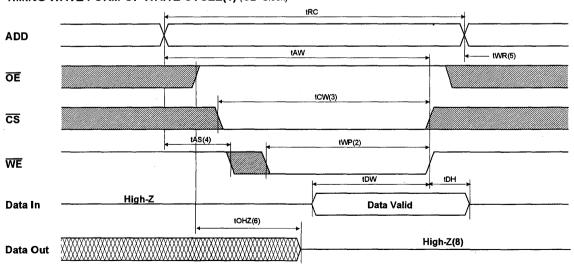
TIMING WAVE FORM OF READ CYCLE(2) (WE=VIH)



NOTES(READ CYCLE)

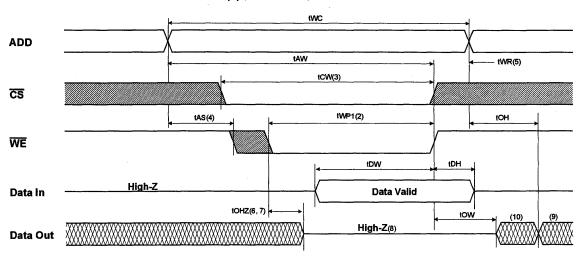
- 1. WE is high for read cycle.
- 2. All read cycle timing is referenced from the last valid address to the first transition address.
- 3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL Levels.
- 4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
- 5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
- 6. Device is continuously selected with CS=VIL.
- 7. Address valid prior to coincident with CS transition low.
- 8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVE FORM OF WRITE CYCLE(1) (OE=Clock)

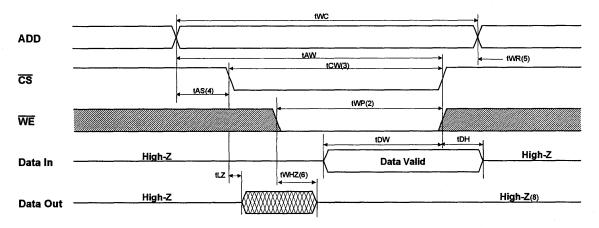




TIMING WAVE FORM OF WRITE CYCLE(2) (OE=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) (CS=Controlled)



NOTES(WRITE CYCLE)

- 1. All write cycle timing is referenced from the last valid address to the first transition address.
- 2. A write occurs during the overlap of a low \overline{CS} and \overline{WE} . A write begins at the latest transition \overline{CS} going low and \overline{WE} going low; A write ends at the earliest transition \overline{CS} going high or \overline{WE} going high. tWP is measured from the beginning of write to the end of write.
- 3. tCW is measured from the later of CS going low to end of write.
- 4. tAS is measured from the address valid to the beginning of write.
- 5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as CS or WE going high.
- 6. If \overline{OE} , \overline{CS} and \overline{WE} are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
- 7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
- 8. If CS goes low simultaneously with WE going or after WE going low, the outputs remain high impedance state.
- 9. Dout is the read data of the new address.
- 10. When CS is low: I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

CS	WE	δĒ	Mode	I/O Pin	Supply Current
Н	X	X*	Not Select	High-Z	ISB, ISB1
L	Н	Н	Output Disable	High-Z	Icc
L	Н	L	Read	Dout	loc
L	L	X	Write	Din	lcc

^{*} NOTE: X means Don't Care.

128K x 8 Bit High-Speed CMOS Static RAM

FEATURES

- Fast Access Time 15, 17, 20 ns (Max.)
- · Low Power Dissipation

Standby (TTL) : 20mA(Max.)

(CMOS): 5mA(Max.)

0.5mA(Max.) - L-Ver. only

Operating KM681001B/BL - 15: 130mA(Max.)

KM681001B/BL - 17: 120mA(Max.)

KM681001B/BL - 20: 110mA(Max.)

- Single $5.0V \pm 10\%$ Power Supply
- . TTL Compatible Inputs and Outputs
- . I/O Compatible with 3.3V Device
- · Fully Static Operation
- No Clock or Refresh required
- · Three State Outputs
- . 2V Minimum Data Retention; L-Ver. only
- . Standard Pin Configuration

KM681001B/BLJ: 32-SOJ-400 KM681001B/BLSJ: 32-SOJ-300

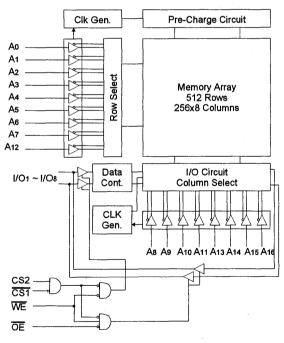
GENERAL DESCRIPTION

The KM681001B/BL is a 1,048,576-bit high-speed Static Random Access Memory organized as 131,072 words by 8 bits. The KM681001B/BL uses 8 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM681001B/BL is packaged in a 400/300 mil 32-pin plastic SOJ and TSOP1.

ORDERING INFORMATION

KM681001B/BL -15/17/20	Commercial Temp.
KM681001BI/BLI -15/17/20	Industrial Temp.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION(Top View)

	늬 ㅇ	\sim	32	
A 0	2		31	A16
A1 [3		30	CS2
A 2	4		29	WE
Аз [5		28	A15
A4 [6		27	A14
A 5	7		26	A13
A 6	8	SOJ	25	A12
A 7	9		24	Œ
A 8	10		23	A11
A 9	11		22	CS1
A10 [12		21	1/08
1/01	13		20	1/07
1/02	14		19	1/06
I/O3 [15		18	1/05
Vss [16		17	1/04
	1			

PIN FUNCTION

Pin Name	Pin Function
A0 - A16	Address Inputs
WE	Write Enable
CS1, CS2	Chip Selects
ŌĒ	Output Enable
I/O1 ~ I/O8	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground
N.C	No Connection

KM681001B/BL, KM681001BI/BLI

ABSOLUTE MAXIMUM RATINGS*

Param	eter	Symbol	Rating	Unit
Voltage on Any Pin Relat	ive to Vss	VIN, VOUT	-0.5 to 7.0	V
Voltage on Vcc Supply R	elative to Vss	Vcc	-0.5 to 7.0	٧
Power Dissipation		Po	1.0	W
Storage Temperature		Тѕтс	-65 to 150	C
Operating Temperature	Commercial	TA	0 to 70	C
	Industrial	TA	-40 to 85	°C

^{*} Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(TA = 0 to 70°)

Parameter	Symbol	Min	Тур	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	. 0	V
Input Low Voltage	ViH	2.2	-	Vcc + 0.5**	V
Input Low Voltage	VIL	-0.5*	_	0.8	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

- * VIL(Min) = -2.0V a.c(Pulse Width≤10ns) for I ≤ 20mA
- ** VIH(Max) = Vcc + 2.0V a.c (Pulse Width ≤ 10ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS(TA = 0 to 70 °C, Vcc= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Max	Unit	
Input Leakage Current	lu	VIN = Vss to Vcc		-2	2	μA
Output Leakage Current	ILO	CS=VIH or OE=VIH or WE=VIL VOUT = Vss to Vcc		-2	2	μA
Operating Current	Icc	Min. Cycle, 100% Duty 15ns		-	130	, , , , ,
	1	CS=VIL, VIN = VIH or VIL,	17ns	-	120	mA
		IOUT=0mA	20ns	-	110	
Standby Current	ISB	Min. Cycle, CS=Viн		-	20	mA
	ISB1	f=0MHz, CS ≥ Vcc-0.2V, Normal		-	5	
		$Vin \ge Vcc-0.2V \text{ or } Vin \le 0.2V$	L-Ver.	-	0.5	- mA
Output Low Voltage Level .	Vol	IoL=8mA	IoL=8mA		0.4	V
Output High Voltage Level	Voн	IOH=-4mA		2.4	-	V
•	Vон1*	Iон1=-0.1mA			3.95	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

CAPACITANCE*(TA =25°C, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	CI/O	VI/0=0V	-	8	pF
Input Capacitance	Cin	Vin=0V	-	6	pF

^{*} NOTE : Capacitance is sampled and not 100% tested.



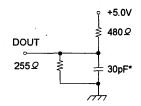
^{*} Vcc=5.0V ± 5% Temp. = 25°C

AC CHARACTERISTICS(TA = 0 to 70 °C, Vcc = $5.0V \pm 10\%$, unless otherwise noted.) TEST CONDITIONS

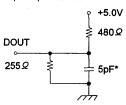
Parameter	Value	
Input Pulse Levels	0V to 3V	
Input Rise and Fall Times	3ns	
Input and Output timing Reference Levels	1.5V	
Output Loads	See below	

NOTE: Above test conditions are also applied at industrial temperature range.





Output Loads(B) for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

Parameter Parameter	KM681001B/BL-15		KM681001B/BL-17		KM681001B/BL-20		Unit	
	Symbol	Min	Max	Min	Max	Min	Max	Onit
Read Cycle Time	tRC	15	-	17	-	20	-	ns
Address Access Time	tAA	-	15	-	17	-	20	ns
Chip Select to Output	tCO*	-	15	-	17	-	20	ns
Output Enable to Valid Output	tOE	-	8	-	9	-	10	ns
Chip Enable to Low-Z Output	tLZ*	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ*	0	6	0	7	0	8	ns
Output Disable to High-Z Output	tOHZ	0	6	0 .	7	0	8	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	0	-	ns
Chip Selection to Power DownTime	tPD	-	15	-	17	-	20	ns

NOTE 1: Above parameters are also guaranteed at industrial temperature range.

NOTE 2: tCO = tCO1, tCO2 / tLZ = tLZ1, tLZ2 / tHZ = tHZ1, tHZ2



KM681001B/BL, KM681001BI/BLI

WRITE CYCLE

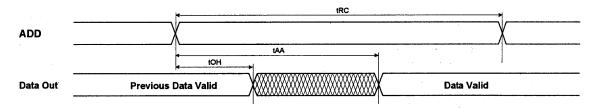
Parameter	KM681001B/BL-15		KM681001B/BL-17		KM681001B/BL-20		- Unit	
	Symbol	Min	Max	Min	Max	Min	Max	Unit
Write Cycle Time	tWC	15	-	17	-	20 ·	-	ns
Chip Select to End of Write	tCW	10	-	11	-	12	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	10	-	11	-	12	-	ns
Write Pulse Width(OE High)	tWP	10	-	11	-	12	-	ns
Write Pulse Width(OE Low)	tWP1	15	-	17	-	20	-	ns
Write Recovery Time	tWR*	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	8	0	9	0	10	ns
Data to Write Time Overlap	tDW	7	-	8	-	9	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

NOTE 1: Above parameters are also guaranteed at industrial temperature range.

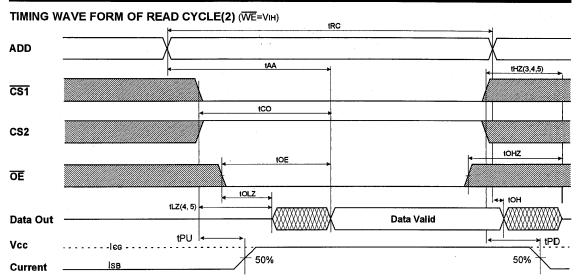
NOTE 2: tWR = tWR1, tWR2

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, CS1=OE=VIL, CS2=WE=VIH)



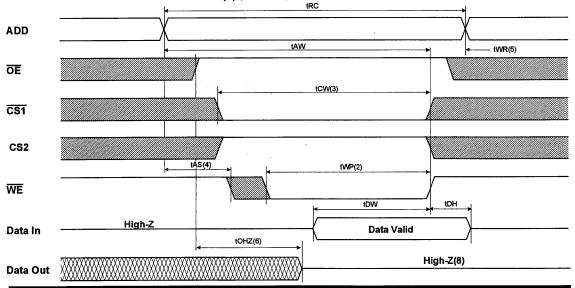
KM681001B/BL, KM681001BI/BLI



NOTES(READ CYCLE)

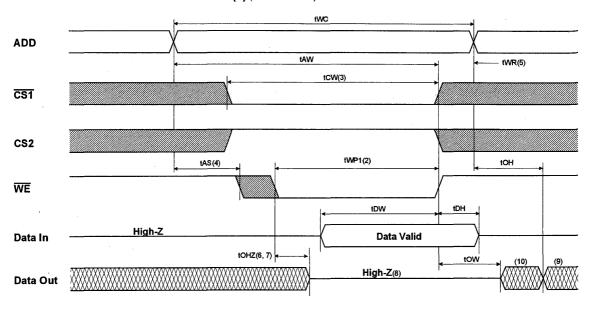
- 1. WE is high for read cycle.
- 2. All read cycle timing is referenced from the last valid address to the first transition address.
- 3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VoH or VoL Levels.
- 4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
- 5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
- 6. Device is continuously selected with CS1=VIL and CS2=VIH.
- 7. Address valid prior to coincident with CS1 transition low and CS2 transition high.
- 8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVE FORM OF WRITE CYCLE(1) (OE=Clock)

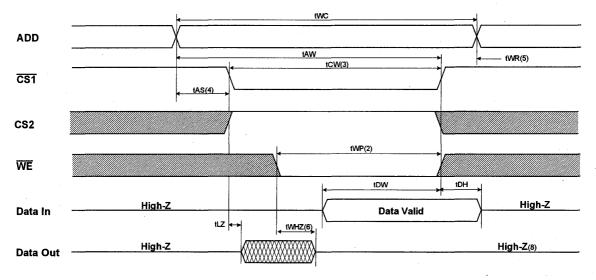




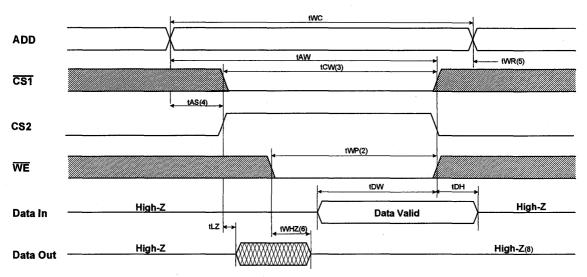
TIMING WAVE FORM OF WRITE CYCLE(2) (OE=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) (CS1=Controlled)



TIMING WAVE FORM OF WRITE CYCLE(4) (CS2=Controlled)



NOTES(WRITE CYCLE)

- 1. All write cycle timing is referenced from the last valid address to the first transition address.
- 2. A write occurs during the overlap of a low $\overline{CS1}$, a high CS2 and a low \overline{WE} . A write begins at the latest transition $\overline{CS1}$ going low, CS2 going high and \overline{WE} going low; A write ends at the earliest transition $\overline{CS1}$ going high or CS2 going low or \overline{WE} going high. tWP is measured from the beginning of write to the end of write.
- 3. tCW is measured from the later of CS1 going low or CS2 going high to end of write.
- 4. tAS is measured from the address valid to the beginning of write.
- 5. tWR is measured from the end of write to the address change. tWR1 applied in case a write ends as CS1 or WE going high. tWR2 applied in case a write ends as CS2 going low.
- 6. If OE, CS1, CS2 and WE are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
- 7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
- 8. If CS1 goes low and CS2 goes high simultaneously with WE going or after WE going low, the outputs remain high impedance state.
- 9. Dout is the read data of the new address.
- 10. When CS1 is low and CS2 is high: I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

CS1	CS2	WE	ŌĒ	Mode	I/O Pin	Supply Current
Н	X	X	X*	Not Select	High-Z	ISB, ISB1
X	L	X	Х	Not Select	High-Z	ISB, ISB1
L	н	Н	Н	Output Disable	High-Z	Icc
L	н	H	L	Read	Dout	lcc
L	H	L	X	Write	Din	lcc

^{*} NOTE: X means Don't Care.

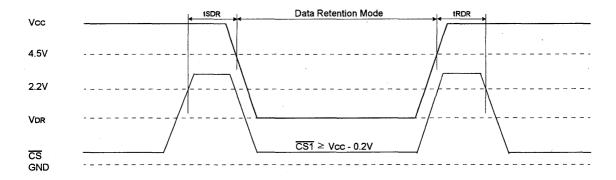


DATA RETENTION CHARACTERISTICS*(TA = 0° to 70°)

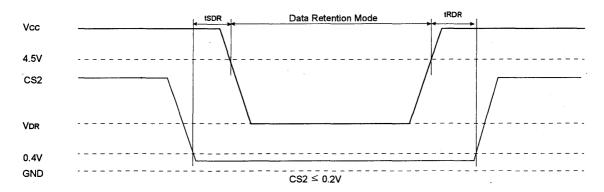
Parameter	Symbol	Test Condition		Тур.	Max.	Unit
Vcc for Data Retention	VDR	$\overline{CS1} \ge Vcc - 0.2VB \text{ or } CS2 \le 0.2V$	2.0	-	5.5	V
Data Retention Current	IDR	$Vcc = 3.0V$, $\overline{CS}1 \ge Vcc - 0.2V$ or $CS2 \le 0.2V$ $Vin \ge Vcc - 0.2V$ or $Vin \le 0.2V$		-	0.40	mA
		$ \begin{array}{c} \text{Vcc} = 2.0 \text{V, } \overline{\text{CS}} \geq \text{Vcc} - 0.2 \text{V} \\ \text{Vin} \geq \text{Vcc} - 0.2 \text{V or Vin} \leq 0.2 \text{V} \\ \end{array} $	-	-	0.35	
Data Retention Set-Up Time	tSDR	See Data Retention	0	-	-	ns
Recovery Time	tRDR	Wave form(below)	5	-	-	ms

NOTE: Above parameters are also guaranteed at industrial temperature range.

DATA RETENTION WAVE FORM 1 (CS1 Controlled)



DATA RETENTION WAVE FORM 2 (CS2 Controlled)



^{* :} L-Ver only.

128K x 8 Bit High-Speed CMOS Static RAM

FEATURES

- Fast Access Time 15, 17, 20ns (Max.)
- Low Power Dissipation

Standby (TTL) : 25mA(Max.)

(CMOS): 8mA(Max.)

Operating KM681001A - 15: 125mA(Max.)

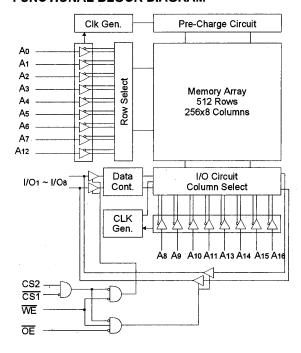
KM681001A - 17: 125mA(Max.)

KM681001A - 20: 120mA(Max.)

- Single 5.0V±10% Power Supply
- · TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Device
- Fully Static Operation
- No Clock or Refresh required
- Three State Outputs
- Standard Pin Configuration

KM681001AJ: 32-SOJ-400 KM681001ASJ: 32-SOJ-300

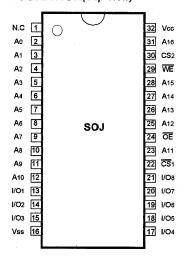
FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The KM681001A is a 1,048,576-bit high-speed Static Random Access Memory organized as 131,072 words by 8 bits. The KM681001A uses 8 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM681001A is packaged in a 400/300 mil 32-pin plastic SOJ.

PIN CONFIGURATION(Top View)



PIN FUNCTION

Pin Name	Pin Function
A0 - A16	Address Inputs
WE	Write Enable
CS1, CS2	Chip Selects
ŌĒ .	Output Enable
I/O1 ~ I/O8	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground
N.C	No Connection



ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	VIN, VOUT	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	Vcc	-0.5 to 7.0	V
Power Dissipation	PD	1.0	W
Storage Temperature	Тѕтв	-65 to 150	°C
Operating Temperature	TA	0 to 70	°C

^{*} Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(TA = 0 to 70°C)

Parameter	Symbol	Min	Тур	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input Low Voltage	ViH	2.2	-	Vcc + 0.5**	V
Input Low Voltage	VIL	-0.5*	-	0.8	V

^{*} VIL(Min) = -2.0V a.c(Pulse Width≤10ns) for 1 ≤ 20mA

DC AND OPERATING CHARACTERISTICS(TA = 0 to 70 °C, Vcc= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	ILI	VIN = Vss to Vcc		-2	2	μA
Output Leakage Current	llo	CS1=Vih or CS2=Vil or OE=Vih or Vout = Vss to Vcc	-2	2	μA	
Operating Current	lcc	Min. Cycle, 100% Duty	15ns	-	125	mA
		CS1=VIL, CS2=VIH,	17ns	-	125	
		VIN = VIH or VIL, IOUT=0mA	20ns	-	120	
Standby Current	ISB	Min. Cycle, CS1=VIH or CS2=VIL	-	25	mA	
	ISB1	f=0MHz, $\overline{CS1} \ge Vcc$ -0.2V or $CS2$ Vin $\ge Vcc$ -0.2V or Vin ≤ 0.2 V	-	8	mA	
Output Low Voltage Level	Vol	IoL=8mA		-	0.4	V
Output High Voltage Level	Voн	IOH=-4mA		2.4	-	V
	Von1*	Iон1=-0.1mA	-	3.95	V	

^{*} Vcc=5.0V ± 5% Temp. = 25°C

CAPACITANCE*(TA =25°C, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	Ci/o	VI/O=0V	-	8	pF
Input Capacitance	CIN	VIN=0V	-	6	pF

^{*} NOTE: Capacitance is sampled and not 100% tested.



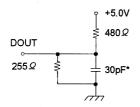
^{**} VIH(Max) = Vcc + 2.0V a.c (Pulse Width ≤ 10ns) for i ≤ 20mA

AC CHARACTERISTICS(TA = 0 to 70 °C, Vcc = $5.0V \pm 10\%$, unless otherwise noted.)

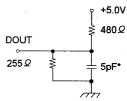
TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

Output Loads(A)



Output Loads(B) for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

Parameter		KM681001A-15		KM681	KM681001A-17		KM681001A-20	
	Symbol -	Min	Max	Min	Max	Min	Max	- Unit
Read Cycle Time	tRC	15	•	17	-	20	-	ns
Address Access Time	tAA	-	15	•	17	-	20	ns
Chip Select to Output	tCO*	-	15	-	17 .	-	20	ns
Output Enable to Valid Output	tOE	-	8	-	9.	-	10	ns
Chip Enable to Low-Z Output	tLZ*	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ*	0	6	0	7	0	8	ns
Output Disable to High-Z Output	tOHZ	0	6	0	7	0	8	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	0	-	ns
Chip Selection to Power DownTime	tPD	-	15	-	17	-	20	ns

NOTE: tCO = tCO1, tCO2 / tLZ = tLZ1, tLZ2 / tHZ = tHZ1, tHZ2

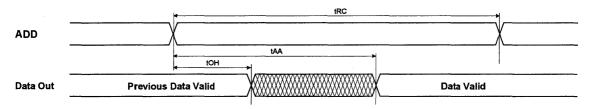
WRITE CYCLE

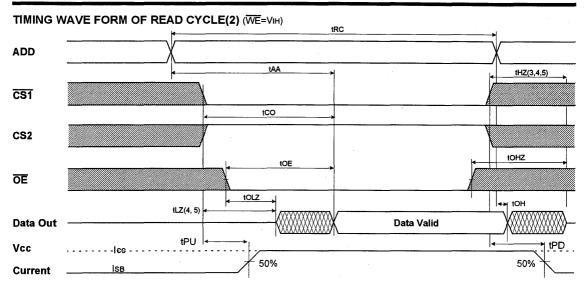
Parameter	S	KM681	001A-15	KM681001A-17		KM681001A-20		- Unit
	Symbol -	Min	Max	Min	Max	Min	Max	– Unit
Write Cycle Time	tWC	15	-	17	-	20	-	ns
Chip Select to End of Write	tCW	10	-	11	-	12	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	10	-	11	-	12	-	ns
Write Pulse Width(OE High)	tWP	-10	-	11	-	12	-	ns
Write Pulse Width(OE Low)	tWP1	15	-	17	-	20	-	ns
Write Recovery Time	tWR*	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	8	0	9	0	10	ns
Data to Write Time Overlap	tDW	7 .	-	8	-	9	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

NOTE: tWR = tWR1, tWR2

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, CS1=OE=VIL, CS2=WE=VIH)





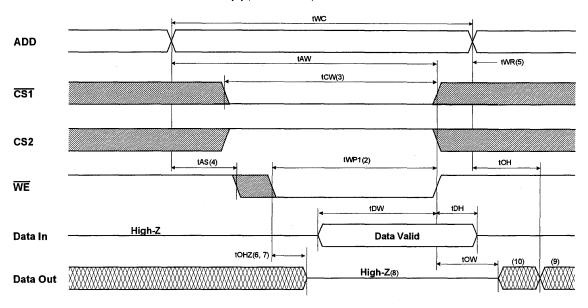
NOTES(READ CYCLE)

- 1. WE is high for read cycle.
- 2. All read cycle timing is referenced from the last valid address to the first transition address.
- 3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VoH or VoL Levels.
- 4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
- 5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
- 6. Device is continuously selected with CS1=VIL and CS2=VIH.
- 7. Address valid prior to coincident with CS1 transition low and CS2 transition high.
- 8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

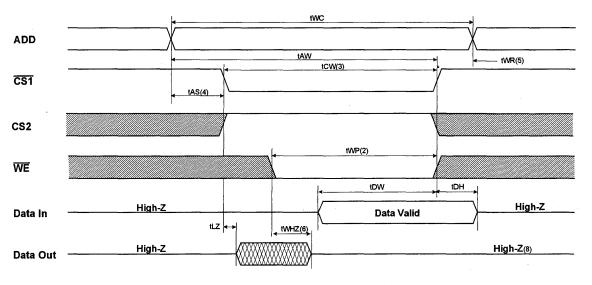
TIMING WAVE FORM OF WRITE CYCLE(1) (OE=Clock) tRC ADD tAW tWR(5) ŌĒ tCW(3) CS₁ CS₂ tAS(4) tWP(2) WE tDW tDH High-Z Data In **Data Valid** tOHZ(6) High-Z(8) **Data Out**



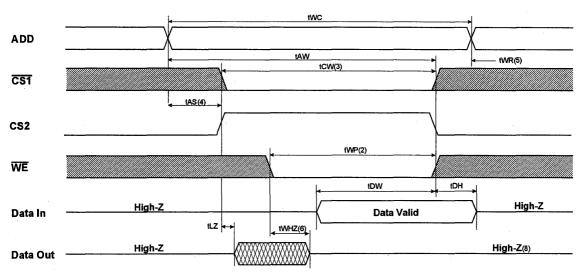
TIMING WAVE FORM OF WRITE CYCLE(2) (OE=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) (CS1=Controlled)



TIMING WAVE FORM OF WRITE CYCLE(4) (CS2=Controlled)



NOTES(WRITE CYCLE)

- 1. All write cycle timing is referenced from the last valid address to the first transition address.
- 2. A write occurs during the overlap of a low $\overline{CS1}$, a high CS2 and a low \overline{WE} . A write begins at the latest transition $\overline{CS1}$ going low, CS2 going high and \overline{WE} going low; A write ends at the earliest transition $\overline{CS1}$ going high or CS2 going low or \overline{WE} going high. tWP is measured from the beginning of write to the end of write.
- 3. tCW is measured from the later of CS1 going low or CS2 going high to end of write.
- 4. tAS is measured from the address valid to the beginning of write.
- 5. tWR is measured from the end of write to the address change. tWR1 applied in case a write ends as CS1 or WE going high. tWR2 applied in case a write ends as CS2 going low.
- 6. If \overline{OE} , $\overline{CS1}$, CS2 and \overline{WE} are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
- 7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
- 8. If CS1 goes low and CS2 goes high simultaneously with WE going or after WE going low, the outputs remain high impedance state.
- 9. Dout is the read data of the new address.
- 10. When CS1 is low and CS2 is high: I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

CS1	CS2	WE	ŌĒ	Mode	I/O Pin	Supply Current
Н	X	Х	X*	Not Select	High-Z	ISB, ISB1
Х	L	Х	Х	Not Select	High-Z	ISB, ISB1
L	Н	Н	Н	Output Disable	High-Z	Icc
L	Н	H	L	Read	Dout	Icc
L	Н	L	Х	Write	Din	, Icc

^{*} NOTE: X means Don't Care.



128K x 8 Bit High-Speed CMOS Static RAM

FEATURES

- Fast Access Time 20,25,35 ns (Max.)
- Low Power Dissipation

Standby (TTL) : 40mA(Max.) (CMOS): 2mA(Max.)

: 2mA(Max.)

0.5mA(Max.) - L-Ver. only

Operating KM681001/L - 20: 170mA(Max.)

KM681001/L - 25: 150mA(Max.)

KM681001/L - 35: 130mA(Max.)

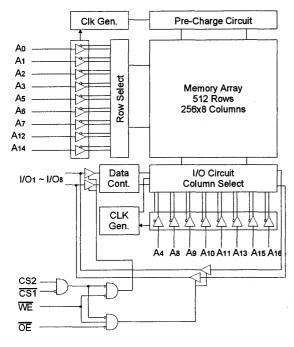
- Single 5.0V ± 10% Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
 - No Clock or Refresh required
- · Three State Outputs
- . 2V Minimum Data Retention; 2V(Min.) L-ver. only
- · Standard Pin Configuration

KM681001/LP: 32-DIP-400 KM681001/LJ: 32-SOJ-400

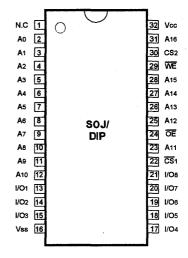
GENERAL DESCRIPTION

The KM681001/L is a 1,048,576-bit high-speed Static Random Access Memory organized as 131,072 words by 8 bits. The KM681001/L uses 8 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM681001/L is packaged in a 400 mil 32-pin plastic DIP or SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION(Top View)



PIN FUNCTION

Pin Name	Pin Function
Ao - A16	Address Inputs
WE	Write Enable
CS1, CS2	Chip Selects
ŌĒ	Output Enable
I/O1 ~ I/O8	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground
N.C	No Connection



KM681001/L CMOS SRAM

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	VIN, VOUT	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	Vcc	-0.5 to 7.0	V
Power Dissipation	Po	1.0	W
Storage Temperature	Тѕтв	-65 to 150	°C
Operating Temperature	TA	0 to 70	°C

^{*} Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(TA = 0 to 70°C)

Parameter	Symbol	Min	Тур	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input Low Voltage	Vih	2.2	-	Vcc + 0.5**	V
Input Low Voltage	VIL	-0.5*	-	0.8	V

^{*} VIL(Min) = -2.0V a.c(Pulse Width≤10ns) for I ≤ 20mÅ

DC AND OPERATING CHARACTERISTICS(TA = 0 to 70 °C, Vcc= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	lLi	VIN = Vss to Vcc		-2	2	μA
Output Leakage Current	lLO	CS1=VIH or CS2=VIL or OE=VIH or VOUT = Vss to Vcc	-2	2	μA	
Operating Current	lcc	Min. Cycle, 100% Duty	20ns	-	170	mΑ
		S1=VIL, CS2=VIH,	25ns	-	150	
	VIN = VIH or VIL, IOUT=0mA		35ns	-	130	1
Standby Current	ISB	Min. Cycle, CS1=VIH or CS2=VIL		-	40	mA
	ISB1	f=0MHz, CS1 ≥ Vcc-0.2V or	Normal	-	2	
	$CS2 \le 0.2V,$ $VIN \ge VCC-0.2V \text{ or } VIN \le 0.2V$		L-Ver.	-	0.5] mA
Output Low Voltage Level	Vol	IoL=8mA		-	0.4	V
Output High Voltage Level	Voн	IOH=-4mA	2.4	-	V	

CAPACITANCE*(TA =25°C, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	C1/0	VI/0=0V	-	7	pF
Input Capacitance	Cin	VIN=0V	-	7	pF

^{*} NOTE: Capacitance is sampled and not 100% tested.



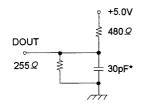
^{**} VIH(Max) = Vcc + 2.0V a.c (Pulse Width \leq 10ns) for I \leq 20mÅ

AC CHARACTERISTICS(TA = 0 to 70 °C, Vcc = 5.0V ± 10%, unless otherwise noted.)

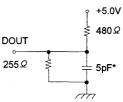
TEST CONDITIONS

Parameter	Value
Input Pulse Levels	OV to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

Output Loads(A)



Output Loads(B) for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

	C	KM681	001/L-20	KM681001/L-25		KM681001/L-35		Unit
Parameter	Symbol -	Min	Max	Min	Max	Min	Max	Unit
Read Cycle Time	tRC	20	-	25	-	35	-	ns
Address Access Time	tAA	-	20	-	25	-	35	ns
Chip Select to Output	tCO*	-	20	-	25	-	35	ns
Output Enable to Valid Output	tOE	-	10	-	13	-	15	ns
Chip Enable to Low-Z Output	tLZ*	0	-	0	-	0	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ*	0	12	0	15	0	15	ns
Output Disable to High-Z Output	tOHZ	0	8	0	10	0	15	ns
Output Hold from Address Change	tOH	3	-	5	-	5	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	0	-	ns
Chip Selection to Power DownTime	tPD	-	20	-	25	-	35	ns

NOTE: tCO = tCO1, tCO2 / tLZ = tLZ1, tLZ2 / tHZ = tHZ1, tHZ2

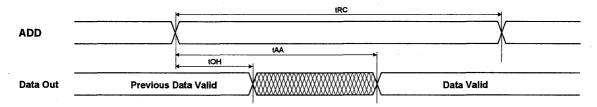
WRITE CYCLE

Parameter	S	KM681001/L-20		KM681	KM681001/L-25		KM681001/L-35	
	Symbol	Min	Max	Min	Max	Min	. Max	- Unit
Write Cycle Time	tWC	20	-	25	-	35	-	ns
Chip Select to End of Write	tCW	17	-	20	-	30	-	ns
Address Set-up Time	tAS	0	_	0	-	0	-	· ns
Address Valid to End of Write	tAW	17	-	20	-	30	-	ns
Write Pulse Width(OE High)	tWP	15		20	-	25	-	ns
Write Pulse Width(OE Low)	tWP1	20	-	25	-	35	-	ns
Write Recovery Time	tWR*	2	•	3	-	3	-	ns
Write to Output High-Z	tWHZ	0	8	0	10	0	12	ns
Data to Write Time Overlap	tDW	12	-	15	-	20	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	4	-	5	-	ns

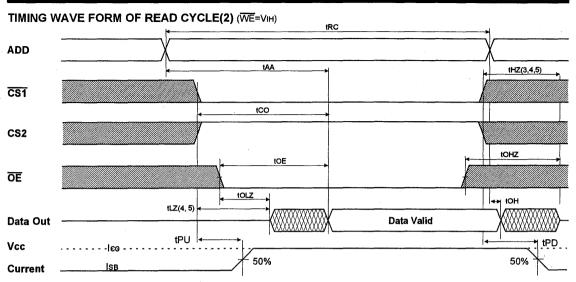
NOTE: tWR = tWR1, tWR2

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, CS1=OE=VIL, CS2=WE=VIH)

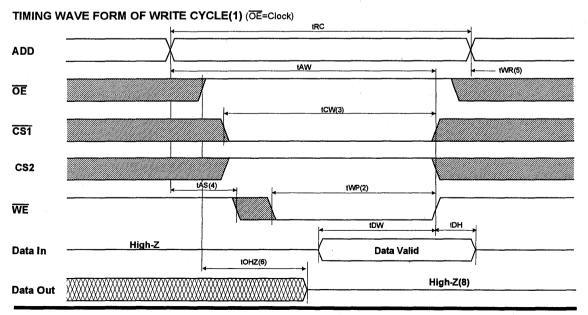






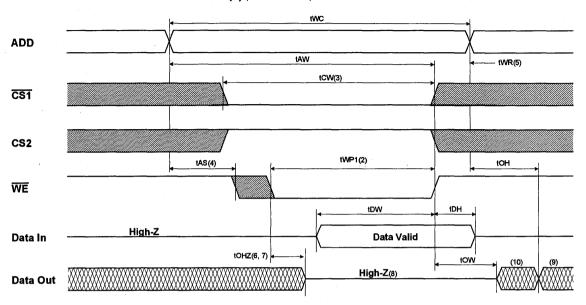
NOTES(READ CYCLE)

- 1. WE is high for read cycle.
- 2. All read cycle timing is referenced from the last valid address to the first transition address.
- 3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL Levels.
- 4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
- 5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
- 6. Device is continuously selected with CS1=VIL and CS2=VIH.
- 7. Address valid prior to coincident with CS1 transition low and CS2 transition high.
- 8 For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

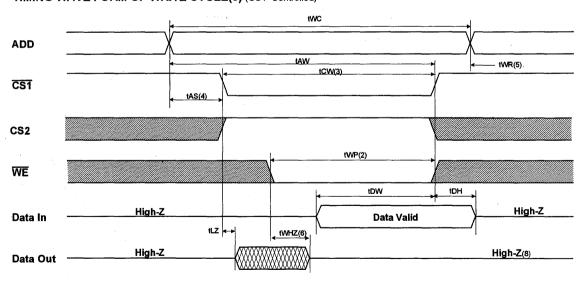




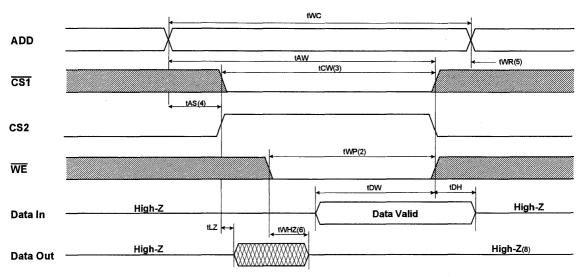
TIMING WAVE FORM OF WRITE CYCLE(2) (OE=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) (CS1=Controlled)



TIMING WAVE FORM OF WRITE CYCLE(4) (CS2=Controlled)



NOTES(WRITE CYCLE)

- 1. All write cycle timing is referenced from the last valid address to the first transition address.
- 2. A write occurs during the overlap of a low $\overline{CS1}$, a high CS2 and a low \overline{WE} . A write begins at the latest transition $\overline{CS1}$ going low, CS2 going high and \overline{WE} going low; A write ends at the earliest transition $\overline{CS1}$ going high or CS2 going low or \overline{WE} going high. tWP is measured from the beginning of write to the end of write.
- 3. tCW is measured from the later of CS1 going low or CS2 going high to end of write.
- 4. tAS is measured from the address valid to the beginning of write.
- 5. tWR is measured from the end of write to the address change. tWR1 applied in case a write ends as CS1 or WE going high. tWR2 applied in case a write ends as CS2 going low.
- 6. If \overline{OE} , $\overline{CS1}$, CS2 and \overline{WE} are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
- 7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
- 8. If CS1 goes low and CS2 goes high simultaneously with WE going or after WE going low, the outputs remain high impedance state.
- 9. Dout is the read data of the new address.
- 10. When CS1 is low and CS2 is high: I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

CS1	CS2	WE	ŌĒ	Mode	I/O Pin	Supply Current
Н	Н	X	X*	Not Select	High-Z	ISB, ISB1
Х	L	Х	Х	Not Select	High-Z	ISB, ISB1
L	L	Н	н	Output Disable	High-Z	lcc
L	L	Н	L	Read	Dout	loc
L	L	L	Х	Write	Din	Icc

^{*} NOTE: X means Don't Care.

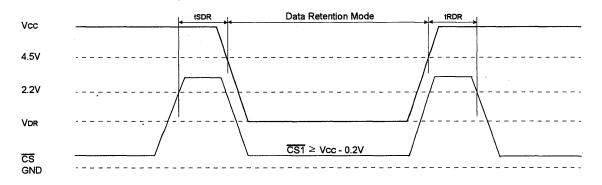


DATA RETENTION CHARACTERISTICS*(TA = 0° to 70°)

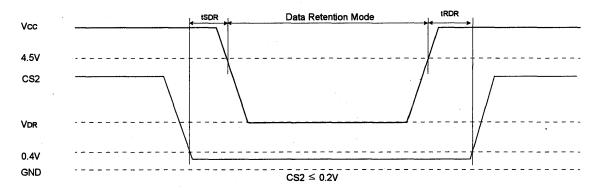
Parameter	Symbol	Test Condition	Min.	Тур.	Max.	Unit
Vcc for Data Retention	VDR	<u>CS</u> 1 ≥ Vcc - 0.2V or CS2 ≤ 0.2V	2.0	-	5.5	V
Data Retention Current	IDR	$Vcc = 2.0V$, $\overline{CS}1 \ge Vcc - 0.2V$ or $CS2 \le 0.2V$ $Vin \ge Vcc - 0.2V$ or $Vin \le 0.2V$		-	0.1	mA
Data Retention Set-Up Time	tSDR	See Data Retention	0	-	-	ns
Recovery Time	tRDR	Wave form(below)	5	-	_	ms

^{*} NOTE : L-Ver only.

DATA RETENTION WAVE FORM 1 (CS1 Controlled)



DATA RETENTION WAVE FORM 2 (CS2 Controlled)



64K x 16 Bit High-Speed CMOS Static RAM

FEATURES

- Fast Access Time 8,10,12ns (Max.)
- · Low Power Dissipation

Standby (TTL) : 30mA(Max.)

(CMOS): 10mA(Max.)

1mA(Max.) - L-Ver. only

Operating KM6161002B/BL - 8: 200mA(Max.)

KM6161002B/BL - 10: 190mA(Max.)

KM6161002B/BL - 12: 180mA(Max.)

- Single 5.0V±10% Power Supply
- . TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Device
- Fully Static Operation
 - No Clock or Refresh required
- . Three State Outputs
- · 2V Minimum Data Retention; L-Ver. only
- · Center Power/Ground Pin Configuration
- Data Byte Control : LB : I/O1~ I/O8, UB : I/O9~ I/O16

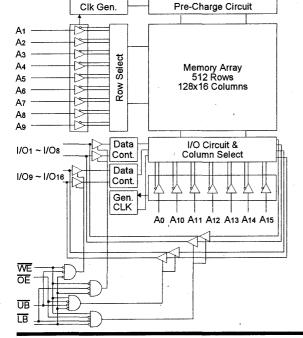
. Standard Pin Configuration

KM6161002B/BLJ: 44-SOJ-400 KM6161002B/BLT: 44-TSOP2-400F

ORDERING INFORMATION

i	KM6161002B/BL -8/1012	Commercial Temp.
	KM6161002BI/BLI -8/10/12	Industrial Temp.

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The KM6161002B/BL is a 1,048,576-bit high-speed Static Random Access Memory organized as 65,536 words by 16 bits. The KM6161002B/BL uses 16 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. Also it allows that lower and upper byte access by data byte control ($\overline{\text{UB}}$, $\overline{\text{LB}}$). The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM6161002B/BL is packaged in a 400mil 44-pin plastic SOJ or TSOP2 forward.

PIN CONFIGURATION (Top View)

				<u>_</u>	
A0 🔟	0	\bigcirc		44	A 15
A1 2				43	A14
A2 3	ł			42	A13
A3 4	l .			41	Œ
A4 5				40	UB
CS 6	į			39	LB
1/01 7				38	I/O16
I/O2 8	}			37	1/015
I/O3 9				36	I/O14
I/O4 10		SOJ	1	35	1/013
Vcc 11		TOOL		34	Vss
Vss 12		TSOF	' <u>2</u>		Vcc
I/O5 13				32	1/012
1/06 14	!			31	1/011
1/07 15				30	1/010
I/O8 16	l			29	1/09
WE [17				28	N.C.
A5 18				27	A12
A6 19				26	A11
A7 20				25	A10
A8 21				24	A 9
N.C. 22				23	N.C.
				ı	

PIN FUNCTION

Pin Name	Pin Function
A0 - A15	Address Inputs
WE	Write Enable
CS	Chip Select
ŌĒ	Output Enable
LB	Lower-byte Control(I/O1~I/O8)
ŪB	Upper-byte Control(I/O9~I/O16)
I/O1 ~ I/O16	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS*

Param	eter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss		VIN, VOUT	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss		Vcc	-0.5 to 7.0	V
Power Dissipation		Po	1.0	W
Storage Temperature		Тѕтҫ	-65 to 150	°C
Operating Temperature	Commercial	TA	0 to 70	°C
	Industrial	TA	-40 to 85	°C

^{*} Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(TA = 0 to 70°C)

Parameter	Symbol	Min	Тур		Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input Low Voltage	ViH	2.2	-	Vcc + 0.5**	٧
Input Low Voltage	VIL	-0.5*	-	0.8	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

DC AND OPERATING CHARACTERISTICS(TA = 0 to 70 °C, Vcc= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	lu	VIN = Vss to Vcc		-2	2	μA
Output Leakage Current	lLO	CS=VIH or OE=VIH or WE=VIL VOUT = Vss to Vcc		-2	2	μA
Operating Current	lcc	Min. Cycle, 100% Duty	8ns	-	200	mA
		CS=VIL, VIN = VIH or VIL,	10ns	-	190	
		IOUT=0mA	12ns	-	180	1
Standby Current	ISB	Min. Cycle, CS=Viн	<u> </u>	-	30	mA
	ISB1	f=0MHz, CS ≥ Vcc-0.2V,	Normal	-	10	mA
		$Vin \ge Vcc-0.2V$ or $Vin \le 0.2V$	L-Ver.	4	1	
Output Low Voltage Level	VoL	loL=8mA	· · · · · · · · · · · · · · · · · · ·	-	0.4	V
Output High Voltage Level	Vон	Iон=-4mA		2.4	-	V
	Von1*	Iон1=-0.1mA	-	3.95	V	

NOTE: Above parameters are also guaranteed at industrial temperature range.

CAPACITANCE*(TA =25°C, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	CI/O	VI/0=0V	-	8	рF
Input Capacitance	CIN	Vin=0V	-	6	pF

^{*} NOTE : Capacitance is sampled and not 100% tested.



^{*} VIL(Min) = -2.0V a.c(Pulse Width ≤ 6ns) for I ≤ 20mA

^{**} VIH(Max) = Vcc + 2.0V a.c (Pulse Width ≤ 6ns) for I ≤ 20mA

^{*} Vcc=5.0V ± 5% Temp. = 25°C

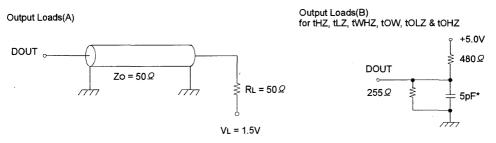
KM6161002B/BL, KM6161002BI/BLI

AC CHARACTERISTICS(TA = 0 to 70°C, Vcc = 5.0V ± 10%, unless otherwise noted.)

TEST CONDITIONS

Parameter	Value
Input Pulse Levels	. 0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

NOTE: Above test conditions are also applied at industrial temperature range.



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Combal	KM6161002B/BL-8		KM61610	KM6161002B/BL-10		KM6161002B/BL-12	
rarameter ,	Symbol	Min	Max	Min	Max	Min	Max	Unit
Read Cycle Time	tRC .	8	-	10	-	12	-	ns
Address Access Time	tAA	-	8	-	10	-	12	ns
Chip Select to Output	tCO	-	8	-	10	-	12	ns
Output Enable to Valid Output	tOE	-	4	-	5	-	6	ns
UB, LB Access Time	tBA	-	4	, -	5	-	6	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
UB, LB Enable to Low-Z Output	tBLZ	0	- '	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	4	0	5	0	6	ns
Output Disable to High-Z Output	tOHZ	0	4	. 0	5	0	6	ns
UB, LB Disable to High-Z Output	tBHZ	0	4	0	5	0	6	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns

NOTE: Above parameters are also guaranteed at industrial temperature range.



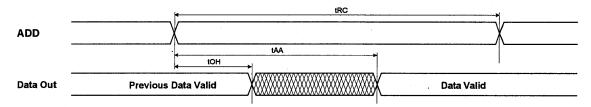
WRITE CYCLE

Parameter		KM61610	002B/BL-8	KM61610	KM6161002B/BL-10		02B/BL-12	T
raidilletei	Symbol	Min	Max	Min	Max	Min	Max	Unit
Write Cycle Time	tWC	8	-	10	-	12	-	ns
Chip Select to End of Write	tCW	6	-	7	-	8	-	ns
Address Set-up Time	tAS	0	-	. 0	-	0	-	ns
Address Valid to End of Write	tAW	6 ,	-	7	-	8	-	ns
Write Pulse Width(OE High)	tWP	6	-	7	-	8	-	ns
Write Pulse Width(OE Low)	tWP1	8	-	10	-	12	-	ns
UB, LB Valid to End of Write	tBW	6	-	7	-	8	-	ns
Write Recovery Time	tWR	0 -	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	4	0	5	0	6	ns
Data to Write Time Overlap	tDW	4	-	5	-	6	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	- 3	-	ns

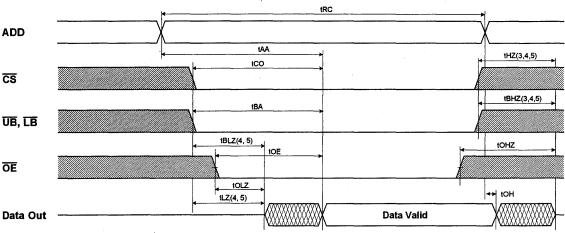
NOTE: Above parameters are also guaranteed at industrial temperature range.

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS} = \overline{OE} = \overline{UB} = \overline{LB} = V_{IL}$, $\overline{WE} = V_{IH}$)



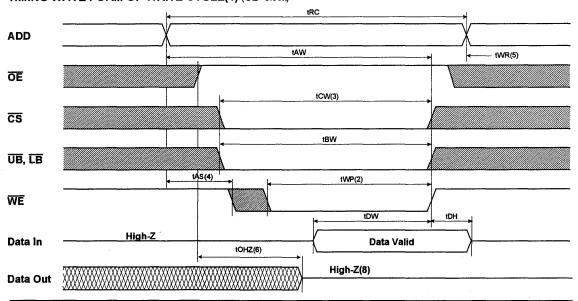
TIMING WAVE FORM OF READ CYCLE(2) (WE=VIH)



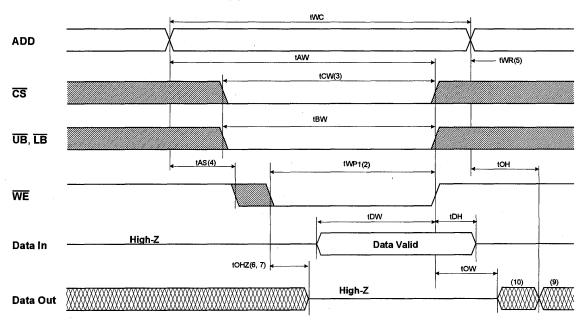
NOTES(READ CYCLE)

- 1. WE is high for read cycle.
- 2. All read cycle timing is referenced from the last valid address to the first transition address.
- 3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VoH or VoL Levels
- 4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
- 5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
- 5. Device is continuously selected with CS=VIL.
- 7. Address valid prior to coincident with CS transition low.
- 8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

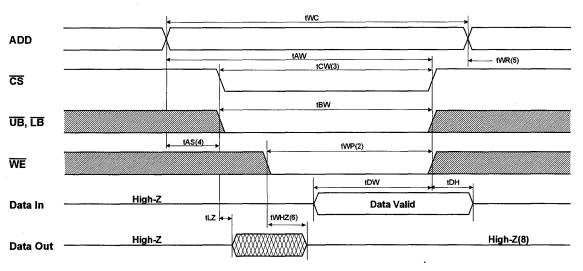
TIMING WAVE FORM OF WRITE CYCLE(1) (OE=Clock)



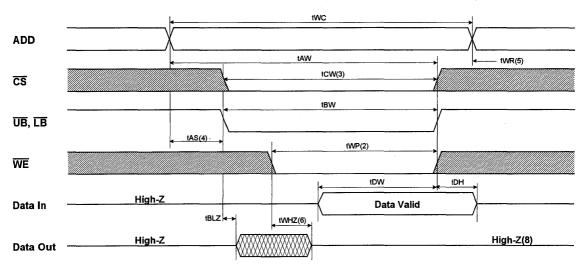




TIMING WAVE FORM OF WRITE CYCLE(3) (CS=Controlled)



TIMING WAVE FORM OF WRITE CYCLE(4) (UB, LB Controlled)



NOTES(WRITE CYCLE)

- 1. All write cycle timing is referenced from the last valid address to the first transition address.
- 2. A write occurs during the overlap of a low \overline{CS} , \overline{WE} , \overline{LB} and \overline{UB} . A write begins at the latest transition \overline{CS} going low and \overline{WE} going low; A write ends at the earliest transition \overline{CS} going high or \overline{WE} going high. tWP is measured from the beginning of write to the end of write.
- 3. tCW is measured from the later of $\overline{\text{CS}}$ going low to end of write.
- 4. tAS is measured from the address valid to the beginning of write.
- 5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as CS, or WE going high.
- 6. If \overline{OE} . \overline{CS} and \overline{WE} are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
- 7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
- 8. If \overline{CS} goes low simultaneously with \overline{WE} going or after \overline{WE} going low, the outputs remain high impedance state.
- 9. Dout is the read data of the new address.
- 10. When \overline{CS} is low: I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

CS	WE	ŌĒ	EB.	UB	Mode	1/0	Supply Current	
US	VVC	OE.	LD	OB	Midde	1/01~1/08	I/O9~I/O16	Supply Current
Н	Х	X*	X	X	Not Select	High-Z		ISB, ISB1
L	н	Н	X	X	Output Disable	High-Z	High-Z	Icc
L	X	Х	Н	H				
L	Н	L	L	Н	Read	Dout	High-Z	lcc
			Н	L		High-Z	Dout	
			L	L		Dout	Dout	
L	L	Х	L	Ι	Write	Din	High-Z	lcc
			Н	L		High-Z	Din	
			L	L		DIN	DIN	

^{*} NOTE: X means Don't Care.

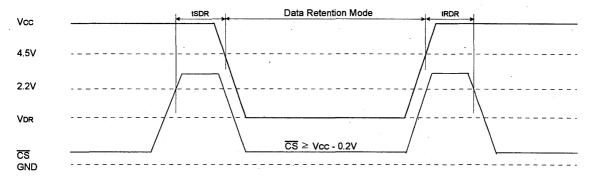


DATA RETENTION CHARACTERISTICS*(TA = 0° to 70°)

Parameter	Symbol	Test Condition	Min. Typ. M			Unit
Vcc for Data Retention	VDR	CS ≥ Vcc - 0.2V	2.0	-	5.5	٧
Data Retention Current	IDR	$Vcc = 3.0V, \overline{CS} \ge Vcc - 0.2V$ $Vin \ge Vcc - 0.2V$ or $Vin \le 0.2V$	-	-	0.9	mA
		$ \begin{array}{c} \text{Vcc} = 2.0 \text{V, } \overline{\text{CS}} \geq \text{Vcc} - 0.2 \text{V} \\ \text{Vin} \geq \text{Vcc} - 0.2 \text{V or Vin} \leq 0.2 \text{V} \\ \end{array} $	-	-	0.7	
Data Retention Set-Up Time	tSDR	See Data Retention	0	-	-	ns
Recovery Time	tRDR	Wave form(below)	5	-	-	ms

NOTE: Above parameters are also guaranteed at industrial temperature range.

DATA RETENTION WAVE FORM(CS Controlled)





^{*} L-Ver only.

64K x 16 Bit High-Speed CMOS Static RAM

FEATURES

- Fast Access Time 12, 15, 17, 20 ns (Max.)
- Low Power Dissipation

Standby (TTL) : 25mA(Max.)

(CMOS): 8mA(Max.)

Operating KM6161002A - 12: 190mA(Max.)

KM6161002A - 15 : 185mA(Max.)

KM6161002A - 17 : 185mA(Max.)

KM6161002A - 20: 180mA(Max.)

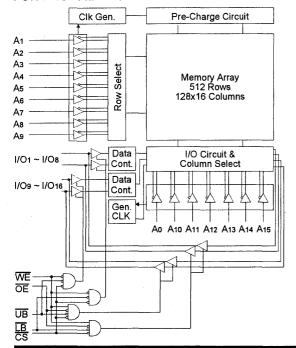
- Single 5.0V ± 10% Power Supply
- . TTL Compatible Inputs and Outputs
- . I/O Compatible with 3.3V Device
- . Fully Static Operation
 - No Clock or Refresh required
- . Three State Outputs
- · Center Power/Ground Pin Configuration
- Data Byte Control : LB : I/O1~ I/O8, UB : I/O9~ I/O16
- . Standard Pin Configuration

KM6161002AJ: 44-SOJ-400 KM6161002AT: 44-TSOP2-400F

ORDERING INFORMATION

KM6161002A -12/15/17/20	Commercial Temp.
KM6161002AI -12/15/17/20	Industrial Temp.

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The KM6161002A is a 1,048,576-bit high-speed Static Random Access Memory organized as 65,536 words by 16 bits. The KM6161002A uses 16 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. Also it allows that lower and upper byte access by data byte control (UB, LB). The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM6161002A is packaged in a 400mil 44-pin plastic SOJ or TSOP2 forward.

PIN CONFIGURATION (Top View)

A0 1	\cap	\bigcup		44	A 15
A1 2				43	A14
A2 3	Ì			42	A13
A3 4	ł			41	ŌĒ
A4 5	ł			40	ŪB
CS 6	ł			39	LB
1/01 7	ł			38	I/O16
1/02 8	l			37	I/O15
I/O3 9	i			36	1/014
I/O4 10	ł	SOJ	'	35	1/013
Vcc 11	ł	TCOD	_	34	Vss
Vss 12		TSOP	2	33	Vcc
1/05 13	İ			32	1/012
I/O6 14	ł			31	1/011
1/07 15				30	1/010
I/O8 16	ł			29	1/09
WE 17	ł			28	N.C.
A5 18				27	A12
A6 19	İ			26	A11
A7 20	ł			25	A10
A8 21				24	A 9
N.C. 22	l			23	N.C.
_					

PIN FUNCTION

Pin Name	Pin Function
A0 - A15	Address Inputs
WE	Write Enable
CS	Chip Select
ŌĒ	Output Enable
LB	Lower-byte Control(I/O1~I/O8)
ŪB	Upper-byte Control(I/O9~I/O16)
I/O1 ~ I/O16	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS*

Param	eter	Symbol	Rating	Unit
Voltage on Any Pin Relat	ve to Vss	VIN, VOUT	-0.5 to 7.0	V
Voltage on Vcc Supply R	elative to Vss	Vcc	V	
Power Dissipation		PD	1.0	W
Storage Temperature		Тѕтс	-65 to 150	°C
Operating Temperature	Commercial	TA	0 to 70	°C
	Industrial	TA	-40 to 85	°C

^{*} Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(TA = 0 to 70°C)

Parameter	Symbol	Min	Тур	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0 .	V
Input Low Voltage	ViH	2.2	-	Vcc + 0.5**	V
Input Low Voltage	VIL	-0.5*	-	0.8	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

- * $ViL(Min) = -2.0V a.c(Pulse Width \le 10ns)$ for $I \le 20mA$
- ** VIH(Max) = Vcc + 2.0V a.c (Pulse Width ≤ 10ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS(TA = 0 to 70 °C, Vcc= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	lu	VIN = Vss to Vcc		-2	2	μA
Output Leakage Current	lLO	CS=VIH or OE=VIH or WE=VIL VOUT = Vss to Vcc	-2	2	μА	
Operating Current	Icc	Min. Cycle, 100% Duty	12ns	-	190	mA
		IOUT=0mA	15ns	_	185	
			17ns	-	185	
		2		-	180	1
Standby Current	IsB	Min. Cycle, CS=Vін	-	25	mA	
		f=0MHz, $\overline{CS} \ge Vcc-0.2V$, Vin $\ge Vcc-0.2V$ or Vin $\le 0.2V$				mΑ
Output Low Voltage Level	Vol	IoL=8mA	-	0.4	٧	
Output High Voltage Level	Voн	Iон=-4mA		2.4	-	٧
	Vон1*	lон1=-0.1mA		-	3.95	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

CAPACITANCE*(TA =25°C, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	CI/O	Vi/o=0V	<u>-</u>	8	pF
Input Capacitance	Cin	VIN=0V	-	6	pF

^{*} NOTE: Capacitance is sampled and not 100% tested.



^{*} Vcc=5.0V ± 5% Temp = 25°C

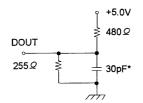
AC CHARACTERISTICS(TA = 0 to 70°C, Vcc = 5.0V±10%, unless otherwise noted.)

TEST CONDITIONS

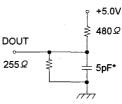
Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3 ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

NOTE: Above test conditions are also applied at industrial temperature range.

Output Loads(A)



Output Loads(B) for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

				KM6161002A-15		KM6161002A-17		KM6161002A-20		Unit
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Read Cycle Time	tRC	12	-	15	-	17	-	20	-	ns
Address Access Time	tAA	-	12	-	15	-	17	-	20	ns
Chip Select to Output	tCO	-	12	-	15	-	17	-	-20	ns
Output Enable to Valid Output	tOE	-	6	-	7	-	8	-	9	ns
UB, LB Access Time	tBA	-	6	-	7	-	8	-	9	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	0	-	ns
UB, LB Enable to Low-Z Output	tBLZ	0	-	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	6	0	7	0	8	0	9	ns
Output Disable to High-Z Output	tOHZ	0	6	0	7	0	8	0	9	ns
UB, LB Disable to High-Z Output	tBHZ	0	6	0	7	0	8	0	9	ns
Output Hold from Address Change	tOH	3	-	3	-	3	_	3	-	ns

NOTE: Above parameters are also guaranteed at industrial temperature range.

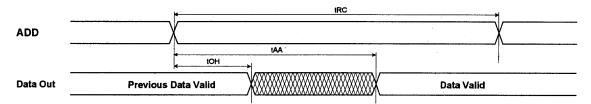
WRITE CYCLE

Parameter	Sbal	KM6161002A-12		KM6161002A-15		KM6161002A-17		KM6161002A-20		
	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Write Cycle Time	tWC	12	-	15	-	17	-	20	-	ns
Chip Select to End of Write	tCW	8	-	10	-	11	-	12	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	8	-	10	-	11		12	-	ns
Write Pulse Width(OE High)	tWP	8	-	10	-	11	-	12	-	ns
Write Pulse Width(OE Low)	tWP1	12	-	15	-	17	-	20	-	ns
UB, LB Valid to End of Write	tBW	8	-	10	-	11	-	12	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	6	0	7	0	8	0	9	ns
Data to Write Time Overlap	tDW	6	-	7	-	8	-	9		ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	- , ,	3	-	3	-	ns

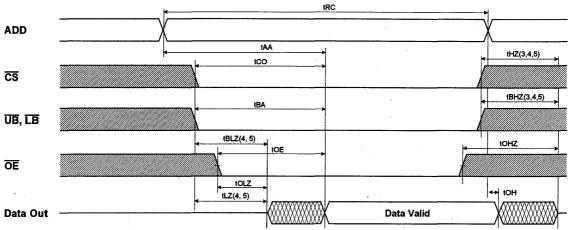
NOTE: Above parameters are also guaranteed at industrial temperature range.

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS} = \overline{OE} = \overline{UB} = \overline{LB} = V_{IL}$, $\overline{WE} = V_{IH}$)



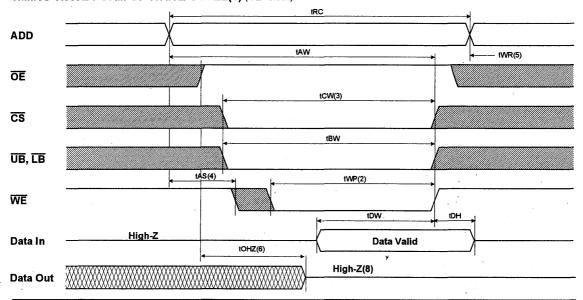
TIMING WAVE FORM OF READ CYCLE(2) (WE=VIH)



NOTES(READ CYCLE)

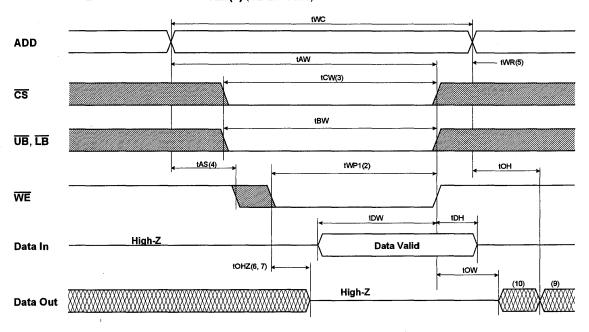
- 1. WE is high for read cycle.
- 2. All read cycle timing is referenced from the last valid address to the first transition address.
- 3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VoH or VoL Levels.
- 4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
- 5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
- 6. Device is continuously selected with CS=VIL.
- 7. Address valid prior to coincident with CS transition low.
- 8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVE FORM OF WRITE CYCLE(1) (OE=Clock)

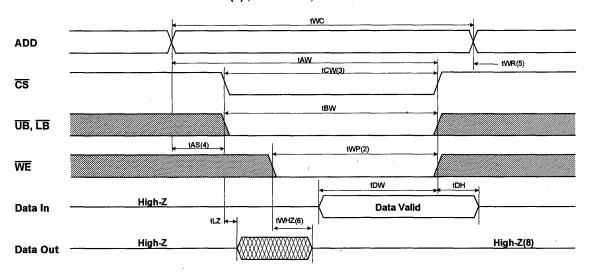




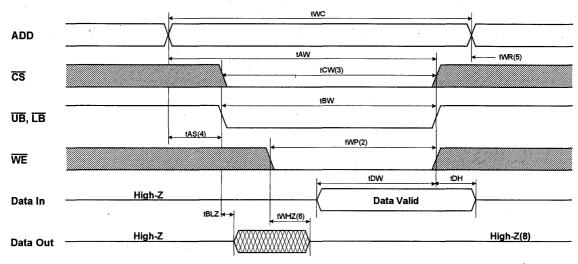
TIMING WAVE FORM OF WRITE CYCLE(2) (OE=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) (CS=Controlled)



TIMING WAVE FORM OF WRITE CYCLE(4) (UB, LB Controlled)



NOTES(WRITE CYCLE)

- 1. All write cycle timing is referenced from the last valid address to the first transition address.
- 2. A write occurs during the overlap of a low \overline{CS} , \overline{WE} , \overline{LB} and \overline{UB} . A write begins at the latest transition \overline{CS} going low and \overline{WE} going low; A write ends at the earliest transition \overline{CS} going high or \overline{WE} going high. tWP is measured from the beginning of write to the end of write.
- 3. tCW is measured from the later of CS going low to end of write.
- 4. tAS is measured from the address valid to the beginning of write.
- 5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as CS, or WE going high.
- 6. If \overline{OE} . \overline{CS} and \overline{WE} are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
- 7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
- 8. If $\overline{\text{CS}}$ goes low simultaneously with $\overline{\text{WE}}$ going or after $\overline{\text{WE}}$ going low, the outputs remain high impedance state.
- 9. Dout is the read data of the new address.
- 10. When $\overline{\text{CS}}$ is low: I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

CS	WE	ŌĒ	CB	UB	Mode	1/0	Pin	Supply Current
- 03	WL	OL.	LD	OB	Mode	I/O1~I/O8	I/O9~I/O16	Supply Current
Н	Х	X*	Х	X	Not Select	High-Z		ISB, ISB1
L	Н	Н	X	Х	Output Disable	High-Z	High-Z	Icc
L	X	Х	Н	Н				
L	Н	L	L	Н	Read	Dout	High-Z	Icc
			Н	L		High-Z	Dout	
			٠	L	, .	Dout	Dout	
L	. L	Х	L	Н	Write	Din	High-Z	lcc
			H	L		High-Z	Din	
			L	L		Din	Din	

^{*} NOTE : X means Don't Care.



64K x 16 Bit High-Speed CMOS Static RAM

FEATURES

• Fast Access Time 15, 17, 20ns (Max.)

· Low Power Dissipation

Standby (TTL) : 40mA(Max.)

(CMOS):10mA(Max.)

Operating KM6161002 - 15: 230mA(Max.)

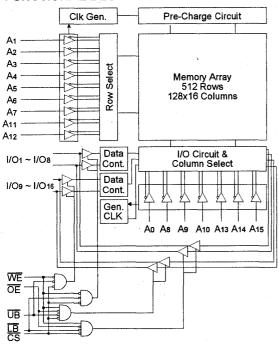
KM6161002 - 17: 220mA(Max.)

KM6161002 - 20 : 210mA(Max.)

- Single 5.0V±10% Power Supply
- · TTL Compatible Inputs and Outputs
- . I/O Compatible with 3.3V Device
- · Fully Static Operation
- No Clock or Refresh required
- · Three State Outputs
- · Center Power/Ground Pin Configuration
- Data Byte Control : LB : I/O1~ I/O8, UB : I/O9~ I/O16
- · Standard Pin Configuration

KM6161002J: 44-SOJ-400

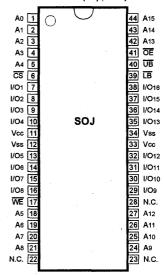
FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The KM6161002 is a 1,048,576-bit high-speed Static Random Access Memory organized as 65,536 words by 16 bits. The KM6161002 uses 16 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. Also it allows that lower and upper byte access by data byte control (UB, LB). The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM6161002 is packaged in a 400mil 44-pin plastic SOJ.

PIN CONFIGURATION (Top. View)



PIN FUNCTION

Pin Name	Pin Function
A0 - A15	Address Inputs
WE	Write Enable
CS	Chip Select
ŌĒ	Output Enable
LB	Lower-byte Control(I/O1~I/O8)
ŪB	Upper-byte Control(I/O9~I/O16)
I/O1 ~ I/O16	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground
N.C	No Connection



ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	VIN, VOUT	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	Vcc	-0.5 to 7.0	V
Power Dissipation	PD	1.0	W
Storage Temperature	Тѕтс	-65 to 150	°C
Operating Temperature	TA	0 to 70	°C

^{*} Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(TA = 0 to 70°C)

Parameter	Symbol	Min	Тур	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	٧
Ground	Vss	0	. 0	0	V
Input Low Voltage	ViH	2.2	-	Vcc + 0.5**	V
Input Low Voltage	VIL	-0.5*	-	8.0	٧

^{*} Vil(Min) = -2.0V a.c(Pulse Width $\leq 10ns$) for $1 \leq 20mÅ$

DC AND OPERATING CHARACTERISTICS(TA = 0 to 70 °C, Vcc= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	lu	Vin = Vss to Vcc		-2	2	μA
Output Leakage Current	ILO	CS=VIH or OE=VIH or WE=VIL VOUT = Vss to Vcc	-2	2	μA	
Operating Current	Operating Current Icc Min. C		15ns	-	230	mA
		CS=VIL, VIN = VIH or VIL,	17ns	-	220	
			20ns	-	210	
Standby Current	ISB	Min. Cycle, CS=Viн		-	40	mA
	ISB1	f=0MHz, $\overline{CS} \ge Vcc-0.2V$, Vin $\ge Vcc-0.2V$ or Vin $\le 0.2V$		-	10	mA
Output Low Voltage Level	Vol	IoL=8mA		-	0.4	٧
Output High Voltage Level	Voн	IOH=-4mA		2.4	-	٧
	Von1*	Iон1=-0.1mA		-	3.95	٧

^{*} Vcc=5.0V ± 5% Temp. = 25℃

CAPACITANCE*(TA =25°C, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	Ci/o	V1/0=0V	-	8	pF
Input Capacitance	Cin	Vin=0V	-	6	pF

^{*} NOTE: Capacitance is sampled and not 100% tested.



^{**} VIH(Max) = Vcc + 2.0V a.c (Pulse Width ≤ 10ns) for I ≤ 20mA

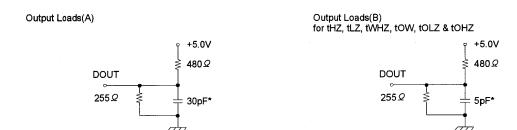
KM6161002

AC CHARACTERISTICS(TA = 0 to 70 °C, Vcc = 5.0V ± 10%, unless otherwise noted.)

TEST CONDITIONS

Parameter	Value	
Input Pulse Levels	0V to 3V	
Input Rise and Fall Times	3ns	
Input and Output timing Reference Levels	1.5V	
Output Loads	See below	

NOTE: Above test conditions are also applied at industrial temperature range.



* Including Scope and Jig Capacitance

READ CYCLE

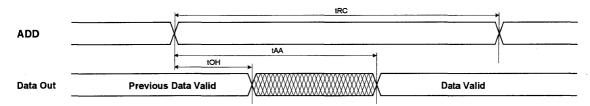
		. KM6161002-15		KM6161002-17		KM6161002-20		11
Parameter	Symbol	Min	Max	Min	Max	Min	Max	- Unit
Read Cycle Time	tRC	15	-	17	-	20	-	ns
Address Access Time	tAA	-	15	-	17	-	20	ns
Chip Select to Output	tCO	-	15	-	17	-	20	ns
Output Enable to Valid Output	tOE	-	8	-	9	-	10	ns
UB, LB Access Time	tBA	-	8	-	9	-	20	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
UB, LB Enable to Low-Z Output	tBLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	6	0	7	0	8	ns
Output Disable to High-Z Output	tOHZ	0	6	0	7	0	8	ns
UB, LB Disable to High-Z Output	tBHZ	0	6	0	7	0	8	ns
Output Hold from Address Change	tOH	3	-	3	-	4	-	ns

WRITE CYCLE

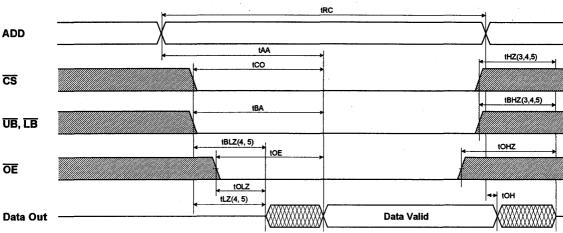
Parameter		KM6161002-15		KM6161002-17		KM6161002-20		T
	Symbol -	Min	Max	Min	Max	Min	Max	- Unit
Write Cycle Time	tWC	15	-	17	-	20	-	ns
Chip Select to End of Write	tCW	12	-	13	-	14	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	12	-	13	-	14	-	ns
Write Pulse Width(OE High)	tWP	12	-	13	-	14	-	ns
Write Pulse Width(OE Low)	tWP1	15	-	17	-	20	-	ns
UB, LB Valid to End of Write	tBW	12	-	13	-	14	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	8	0	8	0	9	ns
Data to Write Time Overlap	tDW	8	-	9	-	10	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	4	-	5	-	ns

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS} = \overline{OE} = \overline{UB} = \overline{LB} = VIL, \overline{WE} = VIH)$



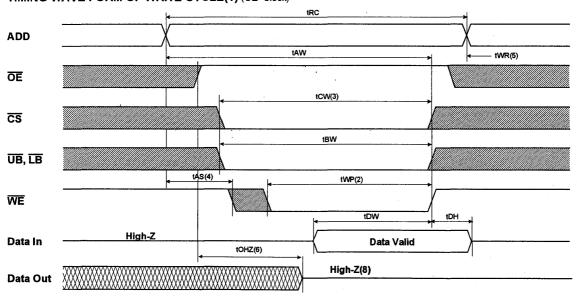
TIMING WAVE FORM OF READ CYCLE(2) (WE=VIH)



NOTES(READ CYCLE)

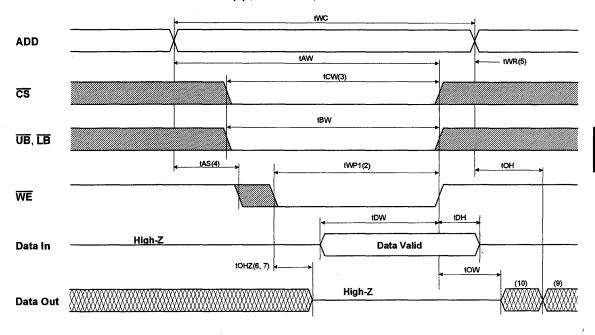
- 1. WE is high for read cycle.
- 2. All read cycle timing is referenced from the last valid address to the first transition address.
- 3 tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VoH or VoL Levels.
- 4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
- 5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
- 6. Device is continuously selected with CS=VIL.
- 7. Address valid prior to coincident with CS transition low.
- 8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVE FORM OF WRITE CYCLE(1) (OE=Clock)

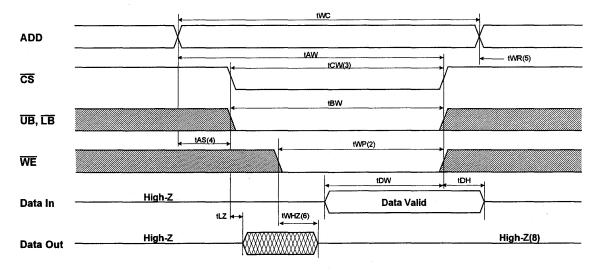




TIMING WAVE FORM OF WRITE CYCLE(2) (OE=Low Fixed)

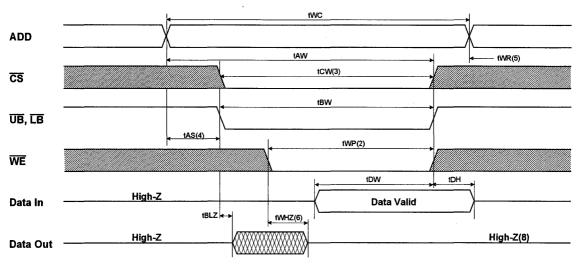


TIMING WAVE FORM OF WRITE CYCLE(3) (CS=Controlled)



KM6161002

TIMING WAVE FORM OF WRITE CYCLE(4) (UB, LB Controlled)



NOTES(WRITE CYCLE)

- 1. All write cycle timing is referenced from the last valid address to the first transition address.
- A write occurs during the overlap of a low \overlap \
- 3. tCW is measured from the later of CS going low to end of write.
- 4. tAS is measured from the address valid to the beginning of write.
- 5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as CS, or WE going high.
- 6. If \overline{OE} . \overline{CS} and \overline{WE} are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
- 7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
- 8. If CS goes low simultaneously with WE going or after WE going low, the outputs remain high impedance state.
- 9. Dout is the read data of the new address.
- 10. When CS is low: I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

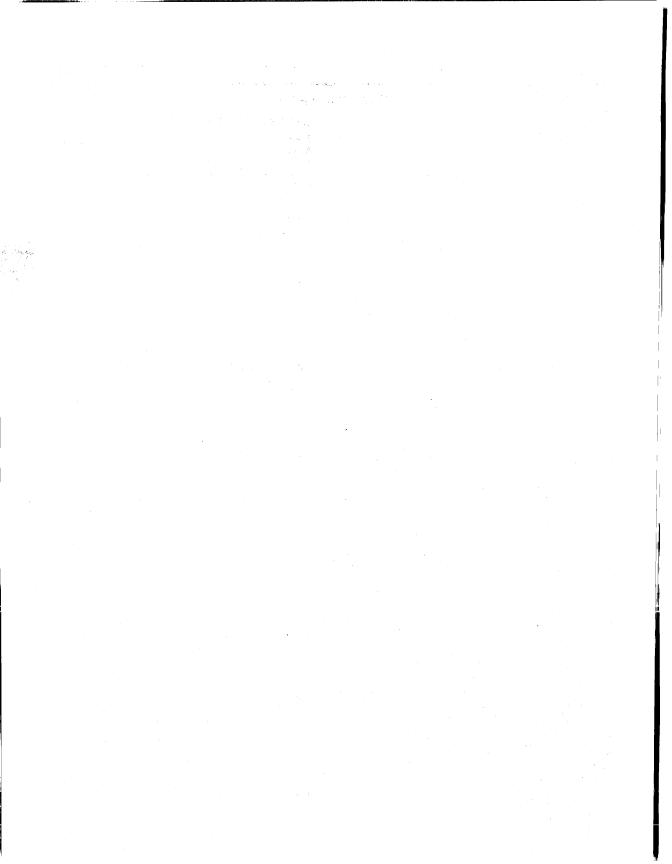
FUNCTIONAL DESCRIPTION

CS	WE	ŌĒ	CB	UB	Mode	I/O Pin		Supply Current
U3	***	OL.	LD	- 05	Mode	I/O1~I/O8	1/09~1/016	Supply Current
Н	Х	X*	Х	Х	Not Select	High-Z		ISB, ISB1
L	Н	н	Х	Х	Output Disable	High-Z	High-Z	Icc
L	Х	Х	н	Н	,			
L	Н	L	L	Н	Read	Dout	High-Z	Icc
			Н	L]	High-Z	Dout	
			L	L		Dout	Dout	
L	L	X	L	Н.	Write	DIN	High-Z	lcc
			Н	L		High-Z	DIN	
			L	L		Din	DIN	

^{*} NOTE: X means Don't Care.



4M High Speed SRAM (5.0V Operation)



1M x 4 Bit (with OE)High-Speed CMOS Static RAM

FEATURES

- Fast Access Time 10,12,15 ns (Max.)
- · Low Power Dissipation

Standby (TTL) : 40mA(Max.)

(CMOS): 10mA(Max.)

Operating KM644002B - 10: 190mA(Max.)

KM644002B - 12: 180mA(Max.)

KM644002B - 15: 170mA(Max.)

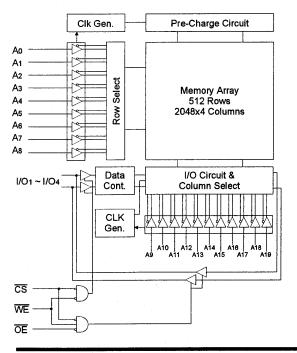
- Single 5.0V ± 10% Power Supply
- . TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Device
- · Fully Static Operation
- No Clock or Refresh required
- . Three State Outputs
- · Center Power/Ground Pin Configuration
- · Standard Pin Configuration

KM644002BJ: 32-SOJ-400 KM644002BT: 32-TSOP2-400F The KM644002B is a 4,194,304-bit high-speed Static Random Access Memory organized as 1,048,576 words by 4 bits. The KM644002B uses 4 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM644002B is packaged in a 400 mil 32-pin plastic SOJ or TSOP(II) forward.

ORDERING INFORMATION

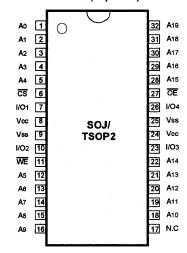
KM644002B -10/12/15	Commercial Temp.
KM644002BI -10/12/15	Industrial Temp.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION(Top View)

GENERAL DESCRIPTION



PIN FUNCTION

Pin Name	Pin Function
A0 - A19	Address Inputs
WE	Write Enable
cs	Chip Select
ŌĒ -	Output Enable
I/O1 ~ I/O4	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground
N.C	No Connection



ABSOLUTE MAXIMUM RATINGS*

Parami	eter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss		Vin, Vout	-0.5 to 7.0	V
Voltage on Vcc Supply Re	oltage on Vcc Supply Relative to Vss		-0.5 to 7.0	V
Power Dissipation		Po	1.0	W
Storage Temperature		Тѕтс	-65 to 150	°C
Operating Temperature	Commercial	TA	0 to 70	°C
	Industrial	TA	-40 to 85	°C

^{*} Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(TA = 0 to 70°C)

Parameter	Symbol	Min	Тур	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	٧
Input Low Voltage	ViH	2.2	-	Vcc + 0.5**	V
Input Low Voltage	VIL	-0.5*	-	0.8	٧

NOTE: Above parameters are also guaranteed at industrial temperature range.

DC AND OPERATING CHARACTERISTICS(TA = 0 to 70 °C, Vcc= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	ILI	Vin = Vss to Vcc		-2	2	μA
Output Leakage Current	lLO	CS=ViH or OE=ViH or WE=ViL Vout = Vss to Vcc		-2	2	μΑ
Operating Current	lcc	Min. Cycle, 100% Duty	10ns	-	190	mA
		CS=VIL, VIN = VIH or VIL, IOUT=0mA	12ns	-	180	
			15ns	-	170]
Standby Current	ISB	Min. Cycle, CS=Viн		-	40	mA
	ISB1	f=0MHz, $\overline{CS} \ge Vcc-0.2V$, Vin $\ge Vcc-0.2V$ or Vin $\le 0.2V$		-	10	mA
Output Low Voltage Level	Vol	IoL=8mA		-	0.4	V
Output High Voltage Level Vo		IOH=-4mA		2.4	-	V
	VoH1*	Iон1=-0.1mA		-	3.95	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

CAPACITANCE*(TA =25°C, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	CI/O	V1/0=0V	-	8	pF
Input Capacitance	Cin	Vin=0V	-	7	pF

^{*} NOTE: Capacitance is sampled and not 100% tested.



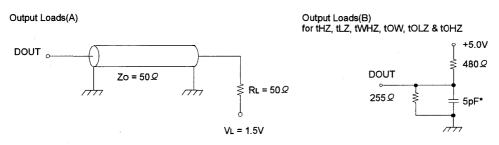
^{*} VIL(Min) = -2.0V a.c(Pulse Width≤8ns) for I ≤ 20mA

^{**} VIH(Max) = Vcc + 2.0V a.c (Pulse Width ≤ 8ns) for I ≤ 20mA

^{*} Vcc=5.0V ± 10% Temp. = 25℃

AC CHARACTERISTICS(TA = 0 to 70 °C, Vcc = $5.0V\pm10\%$, unless otherwise noted.) TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3 ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below



* Including Scope and Jig Capacitance

READ CYCLE

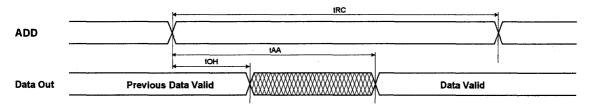
Parameter	C	KM644002B-10		KM644002B-12		KM644002B-15		- Unit
	Symbol	Min	Max	Min	Max	Min	Max	- onit
Read Cycle Time	tRC	10	-	12	-	15	-	ns
Address Access Time	tAA	-	10	-	12	-	15	ns
Chip Select to Output	tCO	-	10	-	12	-	15	ns
Output Enable to Valid Output	tOE	-	5	-	6	-	7	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	5	0	6	0	7	ns
Output Disable to High-Z Output	tOHZ	0	5	0	6	0	7	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	0	_	ns
Chip Selection to Power DownTime	tPD	-	10	_	12	-	15	ns

WRITE CYCLE

Parameter		KM644002B-10		KM644002B-12		KM644002B-15		1
	Symbol -	Min	Max	Min	Max	Min	Max	- Unit
Write Cycle Time	tWC	10	-	12	-	15	-	ns
Chip Select to End of Write	tCW	7	-	8	-	10	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	7	-	8	-	10	-	ns
Write Pulse Width(OE High)	tWP	7	-	8	-	10	-	ns
Write Pulse Width(OE Low)	tWP1	10	-	12	-	15	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	5	0	6	0	7	ns
Data to Write Time Overlap	tDW	. 5	-	6	-	7	-	ns
Data Hold from Write Time	tDH	0	•	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

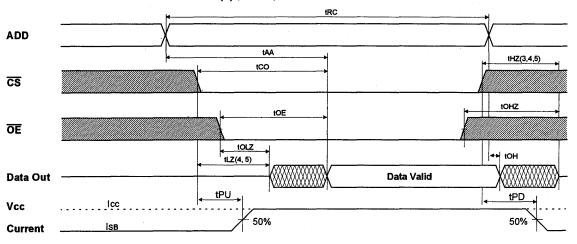
TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, CS=OE=VIL, WE=VIH)





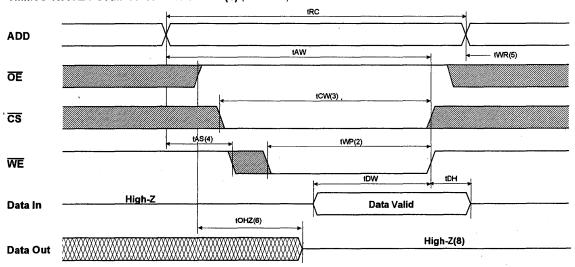
TIMING WAVE FORM OF READ CYCLE(2) (WE=VIH)



NOTES(READ CYCLE)

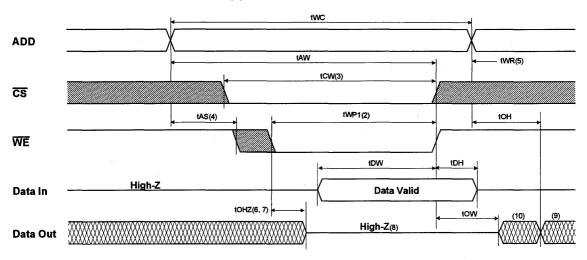
- 1. WE is high for read cycle.
- 2. All read cycle timing is referenced from the last valid address to the first transition address.
- tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL Levels.
- 4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
- 5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
- 6. Device is continuously selected with CS=VIL.
- 7. Address valid prior to coincident with CS transition low.
- 8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVE FORM OF WRITE CYCLE(1) (OE=Clock)

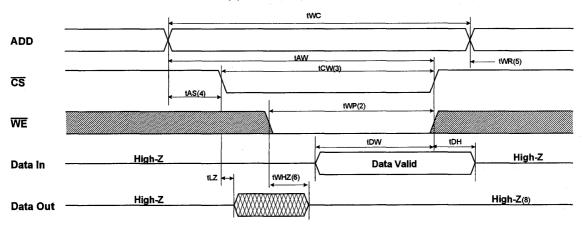




TIMING WAVE FORM OF WRITE CYCLE(2) (OE=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) (CS=Controlled)





NOTES(WRITE CYCLE)

- 1. All write cycle timing is referenced from the last valid address to the first transition address.
- 2. A write occurs during the overlap of a low \overline{CS} and \overline{WE} . A write begins at the latest transition \overline{CS} going low and \overline{WE} going low; A write ends at the earliest transition \overline{CS} going high or \overline{WE} going high. tWP is measured from the beginning of write to the end of write.
- 3. tCW is measured from the later of CS going low to end of write.
- 4. tAS is measured from the address valid to the beginning of write.
- 5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as $\overline{\text{CS}}$ or $\overline{\text{WE}}$ going high.
- 6. If \overline{OE} , \overline{CS} and \overline{WE} are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
- 7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
- 8. If CS goes low simultaneously with WE going or after WE going low, the outputs remain high impedance state.
- 9. Dout is the read data of the new address.
- 10. When $\overline{\text{CS}}$ is low: I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

ĊS	WE	ŌĒ	Mode	I/O Pin	Supply Current
Н	X	X*	Not Select	High-Z	ISB, ISB1
L	Н	Н	Output Disable	High-Z	lcc
L	Н	L	Read	Dout	lcc
L	L	Х	Write	Din	Icc

^{*} NOTE: X means Don't Care.

1M x 4 Bit (with OE)High-Speed CMOS Static RAM

FEATURES

- Fast Access Time 12,13,15 ns (Max.)
- Low Power Dissipation

Standby (TTL) : 60 mA(Max.)

(CMOS): 30mA(Max.)

Operating KM64B4002 - 12: 185mA(Max.)

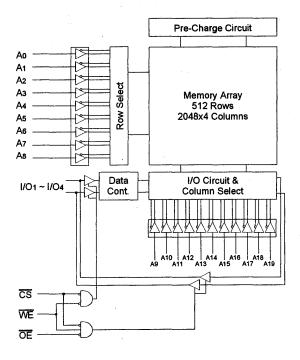
KM64B4002 - 13: 185mA(Max.)

KM64B4002 - 15: 180mA(Max.)

- Single 5.0V ± 10% Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
- No Clock or Refresh required
- . Three State Outputs
- · Center Power/Ground Pin Configuration
- Standard Pin Configuration

KM64B4002J: 32-SOJ-400

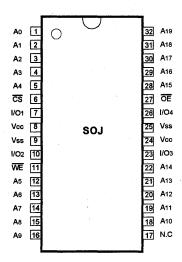
FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The KM64B4002 is a 4,194,304-bit high-speed Static Random Access Memory organized as 1,048,576 words by 4 bits. The KM64B4002 uses 4 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using SAMSUNG's advanced BiCMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM64B4002 is packaged in a 400 mil 32-pin plastic SOJ.

PIN CONFIGURATION(Top View)



PIN FUNCTION

Pin Name	Pin Function
A0 - A19	Address Inputs
WE	Write Enable
<u>cs</u>	Chip Select
ŌĒ	Output Enable
1/01 ~ 1/04	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	VIN, VOUT	-0.5 to 7.0	٧
Voltage on Vcc Supply Relative to Vss	Vcc	-0.5 to 7.0	٧
Power Dissipation	Po	1.0	W
Storage Temperature	Тѕто	-65 to 150	°C
Operating Temperature	TA	0 to 70	°C

^{*} Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(TA = 0 to 70°C)

Parameter	Symbol	Min	Тур	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	٧
Ground	Vss	0	0	0	V
Input Low Voltage	ViH	2.2	-	Vcc + 0.5**	V
Input Low Voltage	VIL	-0.5*	-	0.8	V

^{*} $VIL(Min) = -2.0V a.c(Pulse Width \le 10ns)$ for $1 \le 20mA$

DC AND OPERATING CHARACTERISTICS(TA = 0 to 70 °C, Vcc= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Max	Unit	
Input Leakage Current	lLi	VIN = Vss to Vcc		-2	2	μA
Output Leakage Current	lLO	CS=ViH or OE=ViH or WE=ViL Vout = Vss to Vcc	-10	10	μA	
Operating Current	Icc	Min. Cycle, 100% Duty	12ns		185	mA
		CS=VIL, VIN = VIH or VIL, IOUT=0mA	13ns	-	185	
			15ns	-	180	
Standby Current	ISB	Min. Cycle, CS=Viн		-	60	. mA
	ISB1	f=0MHz, $\overline{\text{CS}} \ge \text{Vcc-0.2V}$, Vin $\ge \text{Vcc-0.2V}$ or Vin $\le \text{0.2V}$		-	30	mA
Output Low Voltage Level	VoL	loL=8mA		-	0.4	V
Output High Voltage Level	Voн	IOH=-4mA	2.4	-	V	

CAPACITANCE*(TA =25°C, f=1.0MHz)

ltem	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	Ci/o	VI/0=0V	-	8	pF
Input Capacitance	Cin	VIN=0V	-	7	pF

^{*} NOTE: Capacitance is sampled and not 100% tested.

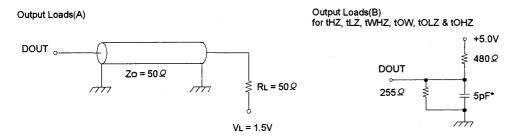


^{**} VIH(Max) = Vcc + 2.0V a.c (Pulse Width \leq 10ns) for I \leq 20mÅ

AC CHARACTERISTICS(TA = 0 to 70 °C, Vcc = 5.0V ± 10%, unless otherwise noted.)

TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below



* Including Scope and Jig Capacitance

READ CYCLE

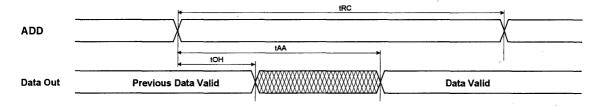
Parameter			34002-12 KM		KM64B4002-13		KM64B4002-15	
	Symbol	Min	Max	Min	Max	Min	Max	- Unit
Read Cycle Time	tRC	12	-	13	-	15	-	ns
Address Access Time	tAA	-	12	-	13	-	15	ns
Chip Select to Output	tCO	-	12	-	13	-	15	ns
Output Enable to Valid Output	tOE	-	6		6	-	7	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	O	-	ns
Chip Disable to High-Z Output	tHZ	0	6	0	6	0	7	ns
Output Disable to High-Z Output	tOHZ	0	6	0	6	Ō	7	ns
Output Hold from Address Change	tOH	3 ,	-	3	-	3	-	ns

WRITE CYCLE

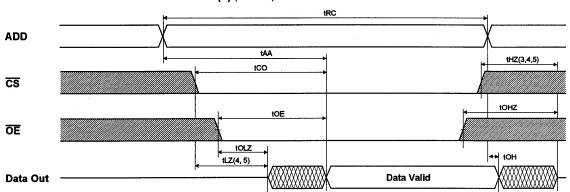
Parameter		KM64B4002-12		KM64B	KM64B4002-13		KM64B4002-15	
	Symbol -	Min	Max	Min	Max	Min	Max	Unit
Write Cycle Time	tWC	12	-	13	-	15	-	ns
Chip Select to End of Write	tCW	8	-	9	-	10	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	8	-	9	-	10	-	ns
Write Pulse Width(OE High)	tWP	8	-	9	-	10	-	ns
Write Pulse Width(OE Low)	tWP1	10	-	11	-	, 12	-	ns
Write Recovery Time	tWR	0	-	0		0	-	ns
Write to Output High-Z	tWHZ	0	6	0	6	. 0	7	ns
Data to Write Time Overlap	tDW	6	-	6	-	7		ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS} = \overline{OE} = VIL, \overline{WE} = VIH)$



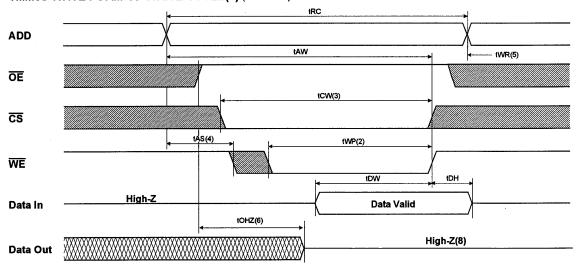
TIMING WAVE FORM OF READ CYCLE(2) (WE=VIH)



NOTES(READ CYCLE)

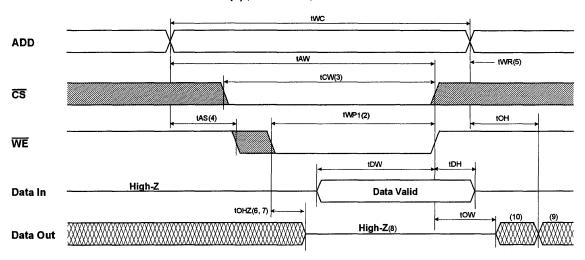
- 1. WE is high for read cycle.
- 2. All read cycle timing is referenced from the last valid address to the first transition address.
- tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VoH or VoL Levels.
- 4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
- 5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
- 6. Device is continuously selected with CS=VIL.
- 7. Address valid prior to coincident with CS transition low.
- 8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVE FORM OF WRITE CYCLE(1) (OE=Clock)

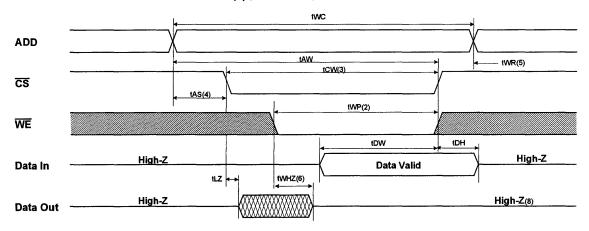




TIMING WAVE FORM OF WRITE CYCLE(2) (OE=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) (CS=Controlled)



NOTES(WRITE CYCLE)

- 1. All write cycle timing is referenced from the last valid address to the first transition address.
- 2. A write occurs during the overlap of a low \overline{CS} and \overline{WE} . A write begins at the latest transition \overline{CS} going low and \overline{WE} going low; A write ends at the earliest transition \overline{CS} going high or \overline{WE} going high. tWP is measured from the beginning of write to the end of write.
- 3. tCW is measured from the later of \overline{CS} going low to end of write.
- 4. tAS is measured from the address valid to the beginning of write.
- 5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as CS or WE going high.
- 6. If \overline{OE} , \overline{CS} and \overline{WE} are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
- 7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
- 8. If $\overline{\text{CS}}$ goes low simultaneously with $\overline{\text{WE}}$ going or after $\overline{\text{WE}}$ going low, the outputs remain high impedance state.
- 9. Dout is the read data of the new address.
- 10. When \overline{CS} is low: I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

ĊŚ	WE	ŌĒ	Mode	I/O Pin	Supply Current
Н	Х	X*	Not Select	High-Z	ISB, ISB1
L	Н	Н	Output Disable	High-Z	lcc
L	Н	L	Read	Dout	Icc
L	L	Х	Write	Din	lcc

^{*} NOTE : X means Don't Care.



1M x 4 Bit (with OE)High-Speed CMOS Static RAM

FEATURES

- Fast Access Time 15,17,20 ns (Max.)
- Low Power Dissipation

Standby (TTL) : 50mA(Max.)

(CMOS): 10mA(Max.)

Operating KM644002A - 15: 150mA(Max.)

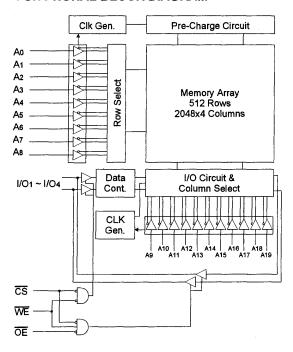
KM644002A - 17: 145mA(Max.)

KM644002A - 20: 140mA(Max.)

- Single 5.0V±10% Power Supply
- . TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Device
- · Fully Static Operation
- No Clock or Refresh required
- · Three State Outputs
- · Center Power/Ground Pin Configuration
- · Standard Pin Configuration

KM644002AJ: 32-SOJ-400

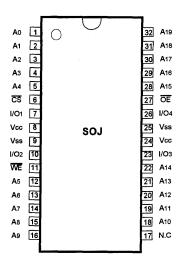
FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The KM644002A is a 4,194,304-bit high-speed Static Random Access Memory organized as 1,048,576 words by 4 bits. The KM644002A uses 4 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM644002A is packaged in a 400 mil 32-pin plastic SOJ.

PIN CONFIGURATION(Top View)



PIN FUNCTION

Pin Name	Pin Function
A0 - A19	Address Inputs
WE	Write Enable
cs	Chip Select
ŌĒ	Output Enable
1/01 ~ 1/04	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground
N.C	No Connection



ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	VIN, VOUT	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	Vcc	-0.5 to 7.0	V
Power Dissipation	PD	1.0	W
Storage Temperature	Тѕтс	-65 to 150	°C
Operating Temperature	TA	0 to 70	°C

^{*} Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(TA = 0 to 70°C)

Parameter	Symbol	Min	Тур		Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input Low Voltage	ViH	2.2	-	Vcc + 0.5**	V
Input Low Voltage	ViL	-0.5*	-	0.8	V

^{*} VIL(Min) = -2.0V a.c(Pulse Width≤10ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS (TA = 0 to 70 °C, Vcc= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Max	Unit	
Input Leakage Current	ILI	VIN = Vss to Vcc		-2	2	μA
Output Leakage Current	lLO	CS=VIH or OE=VIH or WE=VIL VOUT = Vss to Vcc	-2	2	μA	
Operating Current	Icc	Min. Cycle, 100% Duty	15ns	-	150	mA
		CS=VIL, VIN = VIH or VIL, IOUT=0mA	17ns	-	- 145	-
			20ns	-	140	
Standby Current	ISB	Min. Cycle, CS=Viн	-	50	mA	
	ISB1	f=0MHz, $\overline{CS} \ge Vcc-0.2V$, Vin $\ge Vcc-0.2V$ or Vin $\le 0.2V$		-	10	mA
Output Low Voltage Level	VoL	IoL=8mA		-	0.4	V
Output High Voltage Level	Voн	IOH=-4mA		2.4	-	V
	Vон1*	Iон1=-0.1mA	-	3.95	V	

^{*} Vcc=5.0V ± 5% Temp. = 25℃

CAPACITANCE*(TA =25°C, f=1.0MHz)

ltem	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	CI/O	VI/o=0V	-	8	pF
Input Capacitance	CIN	VIN=0V	-	7	pF

^{*} NOTE: Capacitance is sampled and not 100% tested.

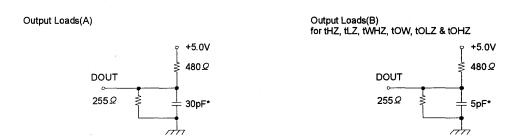


^{**} VIH(Max) = Vcc + 2.0V a.c (Pulse Width ≤ 10ns) for I ≤ 20mA

AC CHARACTERISTICS(TA = 0 to $70\,^{\circ}$, Vcc = $5.0V\pm10\%$, unless otherwise noted.)

TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below



* Including Scope and Jig Capacitance

READ CYCLE

Parameter		KM644	002A-15	KM644002A-17		KM644002A-20		Unit
	Symbol	Min	Max	Min	Max	Min	Max	- Onit
Read Cycle Time	tRC	15	-	17	-	20	-	ns
Address Access Time	tAA	-	15	-	17	-	20	ns
Chip Select to Output	tCO	-	15	-	17	-	20	ns
Output Enable to Valid Output	tOE	-	7	-	8	-	9	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	7	0	8	0	9	ns
Output Disable to High-Z Output	tOHZ	0	7	0	8	0	9	ns
Output Hold from Address Change	tOH	3	-	3		3	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	0	-	ns
Chip Selection to Power DownTime	tPD	-	15	-	17	-	20	ns

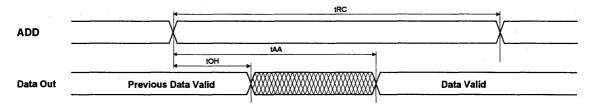


WRITE CYCLE

Parameter		KM644002A-15		KM644002A-17		KM644002A-20		1114
	Symbol -	Min	Max	Min	Max	Min	Max	- Unit
Write Cycle Time	tWC	15	-	17	-	20	-	ns
Chip Select to End of Write	tCW	12	-	13	-	14	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	12	-	13	-	14	-	ns
Write Pulse Width(OE High)	tWP	12	-	13	-	14	-	ns
Write Pulse Width(OE Low)	tWP1	15	-	17	-	20	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	7	0	8	0	9	ns
Data to Write Time Overlap	tDW	8	-	9	-	10	_	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

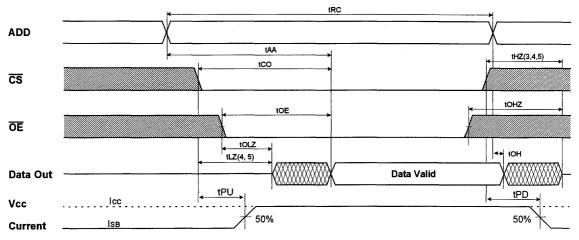
TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS} = \overline{OE} = VIL, \overline{WE} = VIH)$





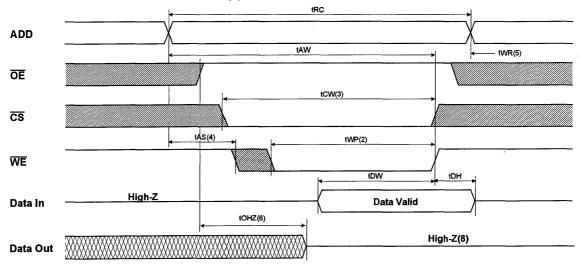
TIMING WAVE FORM OF READ CYCLE(2) (WE=VIH)



NOTES(READ CYCLE)

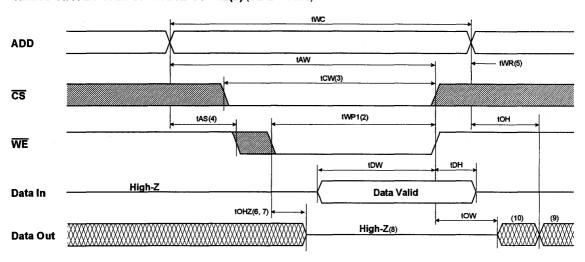
- 1. WE is high for read cycle.
- 2. All read cycle timing is referenced from the last valid address to the first transition address.
- 3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VoH or VoL Levels.
- 4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
- 5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
- 6. Device is continuously selected with CS=VIL.
- 7. Address valid prior to coincident with CS transition low.
- 8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVE FORM OF WRITE CYCLE(1) (OE=Clock)

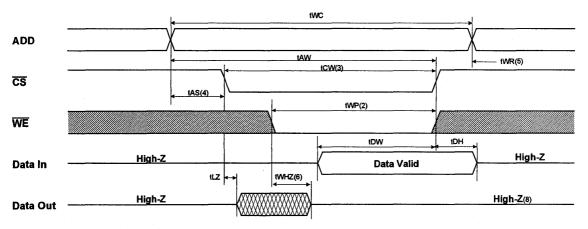




TIMING WAVE FORM OF WRITE CYCLE(2) (OE=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) (CS=Controlled)





NOTES(WRITE CYCLE)

- 1. All write cycle timing is referenced from the last valid address to the first transition address.
- 2. A write occurs during the overlap of a low \overline{CS} and \overline{WE} . A write begins at the latest transition \overline{CS} going low and \overline{WE} going low; A write ends at the earliest transition \overline{CS} going high or \overline{WE} going high. tWP is measured from the beginning of write to the end of write.
- 3. tCW is measured from the later of CS going low to end of write.
- 4. tAS is measured from the address valid to the beginning of write.
- 5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as CS or WE going high.
- 6. If OE, CS and WE are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
- 7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
- 8. If $\overline{\text{CS}}$ goes low simultaneously with $\overline{\text{WE}}$ going or after $\overline{\text{WE}}$ going low, the outputs remain high impedance state.
- 9. Dout is the read data of the new address.
- 10. When \overline{CS} is low: I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

CS	WE	ŌĒ	Mode	I/O Pin	Supply Current
Н	X	X*	Not Select	High-Z	ISB, ISB1
L	Н	Н	Output Disable	High-Z	lcc
L	Н	L	Read	Dout	lcc
L	Ĺ	Х	Write	Din	Icc

^{*} NOTE: X means Don't Care.

1M x 4 Bit (with OE)High-Speed CMOS Static RAM

FEATURES

- Fast Access Time 17,20,25 ns (Max.)
- · Low Power Dissipation

Standby (TTL) : 60mA(Max.)

(CMOS): 10mA(Max.)

Operating KM644002 - 17: 170mA(Max.)

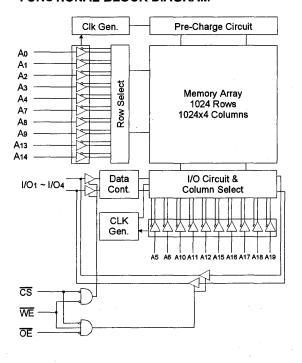
KM644002 - 20: 150mA(Max.)

KM644002 - 25: 130mA(Max.)

- Single 5.0V ± 10% Power Supply
- . TTL Compatible Inputs and Outputs
- . I/O Compatible with 3.3V Device
- Fully Static Operation
- No Clock or Refresh required
- · Three State Outputs
- · Center Power/Ground Pin Configuration
- · Standard Pin Configuration

KM644002J: 32-SOJ-400

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The KM644002 is a 4,194,304-bit high-speed Static Random Access Memory organized as 1,048,576 words by 4 bits. The KM644002 uses 4 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM644002 is packaged in a 400 mil 32-pin plastic SOJ.

ORDERING INFORMATION

KM644002 -17/20/25	Commercial Temp.
KM644002E -17/20/25	Extended Temp.
KM644002I -17/20/25	Industrial Temp.

PIN CONFIGURATION(Top View)

	1		7
A ₀	1		32 A19
A1	2		31 A18
A 2	3		30 A17
Аз	4		29 A16
A4	5		28 A15
cs	6		27 OE
1/01	7		26 1/04
Vcc	8	SOJ	25 Vss
Vss	9		24 Vcc
I/ O 2	10		23 I/O3
WE	11		22 A14
A 5	12		21 A13
A 6	13		20 A12
A 7	14	,	19 A11
A 8	15		18 A10
A 9	16		17 N.C

PIN FUNCTION

Pin Name	Pin Function
A0 - A19	Address Inputs
WE	Write Enable
<u>cs</u>	Chip Select
ŌĒ	Output Enable
1/01 ~ 1/04	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter		Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss		Vin, Vout	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss		Vcc	-0.5 to 7.0	, V
Power Dissipation		Po	Po 1.0	
Storage Temperature		Тѕтс	-65 to 150	°C
Operating Temperature	Commercial	TA	0 to 70	°
	Extended	TA	-25 to 85	. ℃
	Industrial	TA	-40 to 85	°C

^{*} Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(TA = 0 to 70°C)

Parameter	Symbol	Min	Тур	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss .	0	0	0	V
Input Low Voltage	ViH	2.2	-	Vcc + 0.5**	V
Input Low Voltage	' VIL	-0.5*	-	0.8	V

NOTE: Above parameters are also guaranteed at extended and industrial temperature ranges.

- * VIL(Min) = -2.0V,a.c(Pulse Width≤10ns) for I ≤ 20mA
- ** VIH(Max) = Vcc + 2.0V a.c (Pulse Width \leq 10ns) for I \leq 20mÅ

DC AND OPERATING CHARACTERISTICS(TA = 0 to 70°C, Vcc= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Max	Unit	
Input Leakage Current	ILI	Vin = Vss to Vcc	-2	2.	μA	
Output Leakage Current	lLO	CS=ViH or OE=ViH or WE=ViL VOUT = Vss to Vcc	-2	2	μА	
Operating Current	Icc Min. Cycle, 100% Duty		17ns	-	170	mA
		CS=VIL, VIN = VIH or VIL, IOUT=0mA	20ns	-	150	1
			25ns	-	130	1
Standby Current	IsB	Min. Cycle, CS=Viн	-	60	mA	
	ISB1	f=0MHz, $\overline{CS} \ge Vcc-0.2V$, Vin $\ge Vcc-0.2V$ or Vin $\le 0.2V$		-	10	mA
Output Low Voltage Level	VoL	IoL=8mA		: -	0.4	V
Output High Voltage Level	Voн	IOH=-4mA		2.4	-	· v
	Vон1*	Iон1=-0.1mA		-	3.95	V

NOTE: Above parameters are also guaranteed at extended and industrial temperature ranges.

CAPACITANCE*(TA =25°C, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	CI/O	V1/0=0V	-	8	pF
Input Capacitance	CIN	VIN=0V	-	6	pF

^{*} NOTE : Capacitance is sampled and not 100% tested.



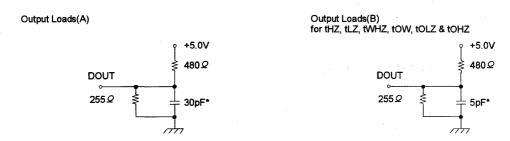
^{*} Vcc=5.0V ± 5% Temp. = 25℃

AC CHARACTERISTICS(TA = 0 to 70°C, Vcc = 5.0V ± 10%, unless otherwise noted.)

TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

NOTE: Above test conditions are also applied at extended and industrial temperature ranges.



* Including Scope and Jig Capacitance

READ CYCLE

	A	KM644002-17		KM644002-20		KM644002-25		
Parameter	Symbol -	Min	Max	Min	Max	Min	Max	Unit
Read Cycle Time	tRC	17	-	20	-	25	-	ns
Address Access Time	tAA	-	17	-	20	-	25	ns
Chip Select to Output	tCO.	-	17	-	20	_	25	ns
Output Enable to Valid Output	tOE	-	8	-	10	-	12	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	7	0	8	0	10	ns
Output Disable to High-Z Output	tOHZ	0	7	0	8	0	- 10	ns
Output Hold from Address Change	tOH	3	-	4	-	5	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	0	-	ns
Chip Selection to Power DownTime	tPD	-	17		20	-	25	ns

NOTE: Above parameters are also guaranteed at extended and industrial temperature ranges.

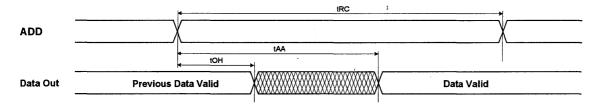
WRITE CYCLE

Daramatar	S	KM644002-17		KM644002-20		KM644002-25		T
Parameter	Symbol -	Min	Max	Min	Max	Min	Max	Unit
Write Cycle Time	tWC	.17	-	20	-	25	-	ns
Chip Select to End of Write	tCW	12	-	13	-	15	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	12	-	13	-	15	-	ns
Write Pulse Width(OE High)	tWP	12	_ :	13		15	- •	ns
Write Pulse Width(OE Low)	tWP1	17	-	20	_	25	-	ns
Write Recovery Time	tWR	0	-	0	-	. 0	-	ns
Write to Output High-Z	tWHZ	0	8	0	8	0	10	ns
Data to Write Time Overlap	tDW	8	-	9	-	10	•	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	4	-	5	-	ns

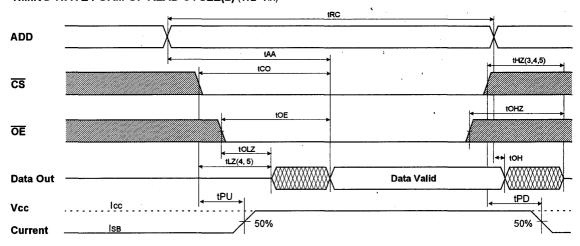
NOTE: Above parameters are also guaranteed at extended and industrial temperature range.

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, CS=OE=VIL, WE=VIH)



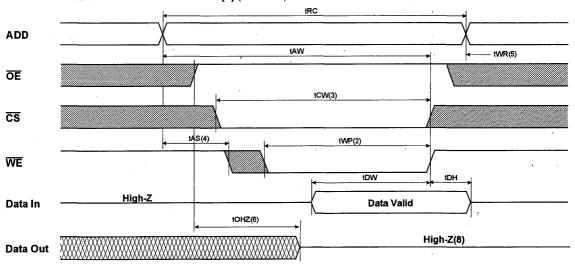
TIMING WAVE FORM OF READ CYCLE(2) (WE=VIH)



NOTES(READ CYCLE)

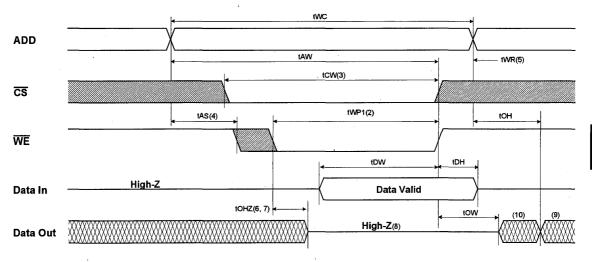
- 1. WE is high for read cycle.
- 2. All read cycle timing is referenced from the last valid address to the first transition address.
- 3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL Levels.
- 4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
- 5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
- 6. Device is continuously selected with CS=VIL.
- 7. Address valid prior to coincident with CS transition low.
- 8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVE FORM OF WRITE CYCLE(1) (OE=Clock)

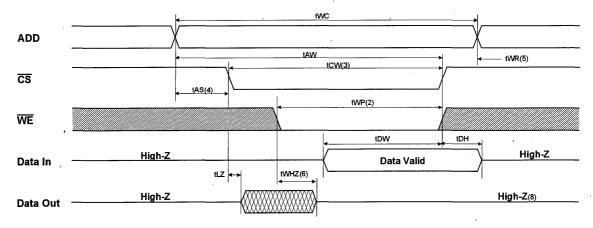




TIMING WAVE FORM OF WRITE CYCLE(2) (OE=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) (CS=Controlled)



NOTES(WRITE CYCLE)

- 1. All write cycle timing is referenced from the last valid address to the first transition address.
- 2. A write occurs during the overlap of a low \overline{CS} and \overline{WE} . A write begins at the latest transition \overline{CS} going low and \overline{WE} going low; A write ends at the earliest transition \overline{CS} going high or \overline{WE} going high. tWP is measured from the beginning of write to the end of write.
- 3. tCW is measured from the later of CS going low to end of write.
- 4. tAS is measured from the address valid to the beginning of write.
- 5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as CS or WE going high.
- 6. If \overline{OE} , \overline{CS} and \overline{WE} are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
- 7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
- 8. If \overline{CS} goes low simultaneously with \overline{WE} going or after \overline{WE} going low, the outputs remain high impedance state.
- 9. Dout is the read data of the new address.
- 10. When \overline{CS} is low: I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

<u>cs</u>	WE	ŌĒ	Mode	I/O Pin	Supply Current
Н	Х	X*	Not Select	High-Z	ISB, ISB1
L	Н	Н	Output Disable	High-Z	Icc
L	Н	L	Read	Dout	lcc
L	L	X	Write	DIN	lcc

^{*} NOTE : X means Don't Care.

512K x 8 Bit High-Speed CMOS Static RAM

FEATURES

- Fast Access Time 10,12,15 ns (Max.)
- · Low Power Dissipation

Standby (TTL) : 40mA(Max.)

(CMOS): 10mA(Max.)

Operating KM684002B - 10: 200mA(Max.)

KM684002B - 12: 190mA(Max.)

KM684002B - 15: 180mA(Max.)

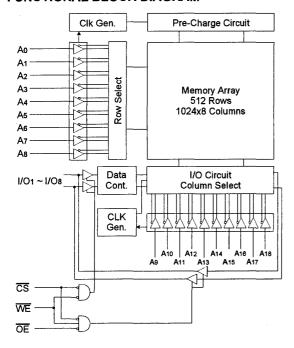
- Single 5.0V ± 10% Power Supply
- . TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Device
- Fully Static Operation
- No Clock or Refresh required
- Three State Outputs
- · Center Power/Ground Pin Configuration
- · Standard Pin Configuration

KM684002BJ: 36-SOJ-400 KM684002BT: 36-TSOP2-400F

ORDERING INFORMATION

KM684002B -10/12/15	Commercial Temp.
KM684002BI -10/12/15	Industrial Temp.

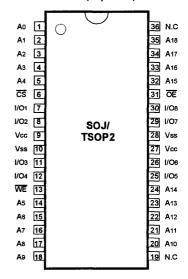
FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The KM684002B is a 4,194,304-bit high-speed Static Random Access Memory organized as 524,288 words by 8 bits. The KM684002B uses 8 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM684002B is packaged in a 400 mil 36-pin plastic SOJ or TSOP(II) forward.

PIN CONFIGURATION(Top View)



PIN FUNCTION

Pin Name	Pin Function			
Ao - A18	Address Inputs			
WE	Write Enable			
CS	Chip Select			
ŌĒ	Output Enable			
I/O1 ~ I/O8	Data Inputs/Outputs			
Vcc	Power(+5.0V)			
Vss	Ground			
N.C	No Connection			



ABSOLUTE MAXIMUM RATINGS*

Param	eter	Symbol	Rating Unit		
Voltage on Any Pin Relati	ive to Vss	VIN, VOUT	-0.5 to 7.0	V	
Voltage on Vcc Supply R	elative to Vss	Vcc	-0.5 to 7.0	V	
Power Dissipation	•	PD	1.0	W	
Storage Temperature		Тѕтс	-65 to 150	°C	
Operating Temperature	Commercial	TA ·	0 to 70	°C	
	Industrial	TA	-40 to 85	°C	

^{*} Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(TA = 0 to 70°C)

Parameter	Symbol	Min	Тур	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0 '	0	0	V
Input Low Voltage	. Viн	2.2	-	Vcc + 0.5**	V
Input Low Voltage	VIL	-0.5*	-	0.8	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

DC AND OPERATING CHARACTERISTICS(TA = 0 to 70 °C, Vcc= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	ILI	VIN = Vss to Vcc		-2	2	μA
Output Leakage Current	lLO	CS=VIH or OE=VIH or WE=VIL VOUT = Vss to Vcc		-2	2	μA
Operating Current	Icc	Min. Cycle, 100% Duty	10ns	-	200	mA
		CS=VIL, VIN = VIH or VIL, IOUT=0mA	12ns	-	190	1 .
			15ns	-	180	
Standby Current	ISB	Min. Cycle, СS=Viн		-	40	mA
	Isb1 $f=0MHz$, $\overline{CS} \ge Vcc-0.2V$, $Vin \ge Vcc-0.2V$ or $Vin \le 0.2V$			-	10	mA
Output Low Voltage Level	Vol	IoL=8mA		-	0.4	· V
Output High Voltage Level	Voн	IOH=-4mA		2.4	-	V
	Vон1*	IOH1=-0.1mA		-	3.95	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

CAPACITANCE*(TA =25°C, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	CI/O	V1/0=0V	-	8	pF
Input Capacitance	CIN	VIN=0V	-	7	pF

^{*} NOTE : Capacitance is sampled and not 100% tested.



^{*} VIL(Min) = -2.0V a.c(Pulse Width≤8ns) for I ≤ 20mA

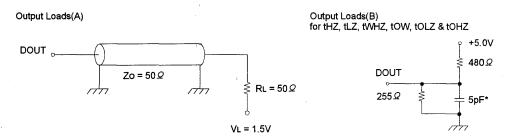
^{**} VIH(Max) = Vcc + 2.0V a.c (Pulse Width \leq 8ns) for I \leq 20 mÅ

^{*} Vcc=5.0V \pm 10% Temp. = 25 $^{\circ}$ C

AC CHARACTERISTICS(TA = 0 to 70 °C, Vcc = $5.0V \pm 10\%$, unless otherwise noted.)

TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below



* Including Scope and Jig Capacitance

READ CYCLE

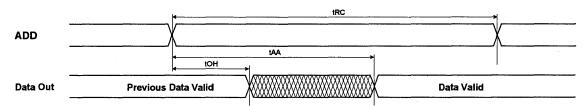
		KM684002B-10		KM684002B-12		KM684002B-15		T
Parameter	Symbol	Min	Max	Min	Max	Min	Max	- Unit
Read Cycle Time	tRC	10	-	12	-	15	-	ns
Address Access Time	tAA	-	10	-	12	-	15	ns
Chip Select to Output	tCO	-	10	-	12	-	15	ns
Output Enable to Valid Output	tOE	-	5	-	6	-	7	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	5	0	6	0	7	ns
Output Disable to High-Z Output	tOHZ	0	5	0	6	0	7	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	_	0	-	ns
Chip Selection to Power DownTime	tPD	-	15	-	12	-	15	ns

WRITE CYCLE

		KM684002B-10		KM684002B-12		KM684002B-15		T.,
Parameter	Symbol	Min	Max	Min.	Max	Min	Max	Unit
Write Cycle Time	tWC	10	-	12	•	15	-	ns
Chip Select to End of Write	tCW	7	-	8	-	10	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	7	-	8		10	-	ns
Write Pulse Width(OE High)	tWP	7	-	8	-	10	-	ns
Write Pulse Width(OE Low)	tWP1	10		12	-	14	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	. 0	5	0	6	0	7	ns
Data to Write Time Overlap	tDW	5	-	6	-	7	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

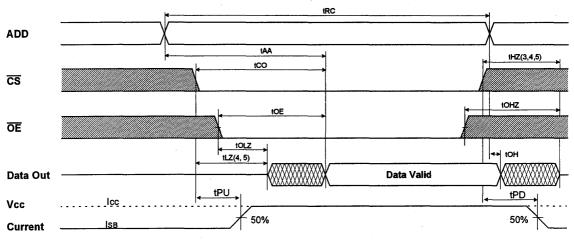
TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, CS=OE=VIL, WE=VIH)





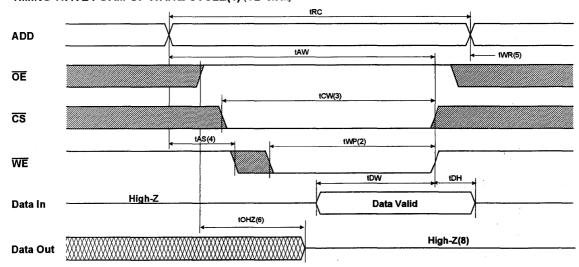
TIMING WAVE FORM OF READ CYCLE(2) (WE=VIH)



NOTES(READ CYCLE)

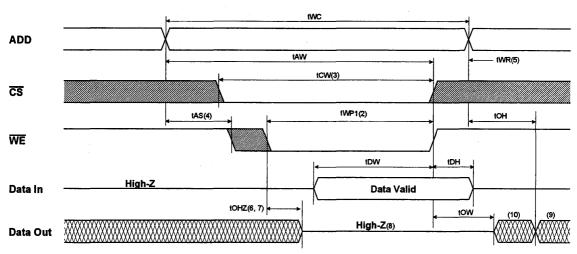
- 1. WE is high for read cycle.
- 2. All read cycle timing is referenced from the last valid address to the first transition address.
- 3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VoH or VoL Levels.
- 4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
- 5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
- 6. Device is continuously selected with CS=VIL.
- 7. Address valid prior to coincident with CS transition low.
- 8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVE FORM OF WRITE CYCLE(1) (OE=Clock)

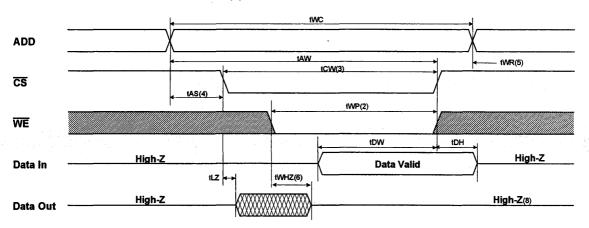




TIMING WAVE FORM OF WRITE CYCLE(2) (OE=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) (CS=Controlled)





NOTES(WRITE CYCLE)

- 1. All write cycle timing is referenced from the last valid address to the first transition address.
- 2. A write occurs during the overlap of a low $\overline{\text{CS}}$ and $\overline{\text{WE}}$. A write begins at the latest transition $\overline{\text{CS}}$ going low and $\overline{\text{WE}}$ going low; A write ends at the earliest transition \overline{CS} going high or \overline{WE} going high. tWP is measured from the beginning of write to the end of write.

 3. tCW is measured from the later of \overline{CS} going low to end of write.
- 4. tAS is measured from the address valid to the beginning of write.
- 5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as CS or WE going high.
- 6. If OE, CS and WE are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
- 7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
- 8. If $\overline{\text{CS}}$ goes low simultaneously with $\overline{\text{WE}}$ going or after $\overline{\text{WE}}$ going low, the outputs remain high impedance state.
- 9. Dout is the read data of the new address.
- 10. When CS is low: I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

ĊŚ	WE	ŌĒ	Mode	I/O Pin	Supply Current
Н	X	X*	Not Select	High-Z	ISB, ISB1
L	H	Н	Output Disable	High-Z	lcc
L	H	L	Read	Dout	Icc
L	L	Х	Write	Din	Icc

^{*} NOTE: X means Don't Care.

512K x 8 Bit High-Speed CMOS Static RAM

FEATURES

- Fast Access Time 12,13,15ns (Max.)
- · Low Power Dissipation

Standby (TTL) : 60mA(Max.)

(CMOS): 30mA(Max.)

Operating KM68B4002 - 12: 195mA(Max.)

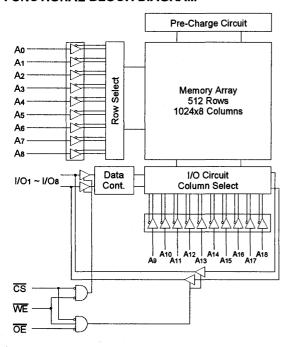
KM68B4002 - 13: 195mA(Max.)

KM68B4002 - 15: 190mA(Max.)

- Single 5.0V±10% Power Supply
- TTL Compatible Inputs and Outputs
- . I/O Compatible with 3.3V Device
- · Fully Static Operation
- No Clock or Refresh required
- · Three State Outputs
- · Center Power/Ground Pin Configuration
- · Standard Pin Configuration

KM68B4002J: 36-SOJ-400

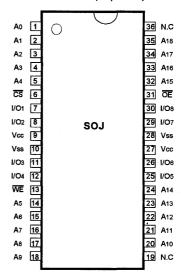
FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The KM68B4002 is a 4,194,304-bit high-speed Static Random Access Memory organized as 524,288 words by 8 bits. The KM68B4002 uses 8 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using Samsung's advanced BiCMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM68B4002 is packaged in a 400 mil 36-pin plastic SOJ.

PIN CONFIGURATION(Top View)



PIN FUNCTION

Pin Name	Pin Function			
A0 - A18	Address Inputs			
WE	Write Enable			
CS	Chip Select			
ŌĒ	Output Enable			
I/O1 ~ I/O8	Data Inputs/Outputs			
Vcc	Power(+5.0V)			
Vss	Ground			
N.C	No Connection			



ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	VIN, VOUT	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	Vcc	-0.5 to 7.0	V
Power Dissipation	PD	1.0	W
Storage Temperature	Тѕтс	-65 to 150	°C
Operating Temperature	TA	0 to 70	°

^{*} Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(TA = 0 to 70°C)

Parameter	Symbol	Min	Тур	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	٧
Ground	Vss	0	0	0	V
Input Low Voltage	VIH	2.2	-	Vcc + 0.5**	٧
Input Low Voltage	ViL	-0.5*	-	0.8	٧

^{*} VIL(Min) = -2.0V a.c(Pulse Width ≤ 10 ns) for $1 \leq 20$ mÅ

DC AND OPERATING CHARACTERISTICS(TA = 0 to 70 °C, Vcc= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	lu	VIN = Vss to Vcc		-2	2	μA
Output Leakage Current	lLO	CS=VIH or OE=VIH or WE=VIL VOUT = Vss to Vcc	-10	10	μA	
Operating Current	Icc	Min. Cycle, 100% Duty	12ns	-	195	mA
		CS=VIL, VIN = VIH or VIL, IOUT=0mA	13ns	-	195	1
			15ns	-	190	1
Standby Current	'ISB	Min. Cycle, CS=Vін		-	60	mA
	ISB1	f=0MHz, $\overline{\text{CS}} \ge \text{Vcc-0.2V}$, Vin $\ge \text{Vcc-0.2V}$ or Vin $\le 0.2\text{V}$		-	30	mA
Output Low Voltage Level	Vol	IOL=8mA		-	0.4	V
Output High Voltage Level	Voн	IOH=-4mA		2.4	-	V

CAPACITANCE*(TA =25°C, f=1.0MHz)

	Item	Symbol	Test Conditions	MIN	Max	Unit
	Input/Output Capacitance	CI/O	V1/0=0V	-	8	pF
l	Input Capacitance	CIN	VIN=0V	-	7	pF

^{*} NOTE : Capacitance is sampled and not 100% tested.

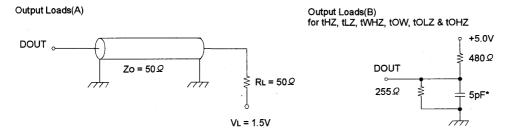


^{**} VIH(Max) = Vcc + 2.0V a.c (Pulse Width \le 10ns) for I \le 20mA

AC CHARACTERISTICS(TA = 0 to 70 °C, Vcc = 5.0V ± 10%, unless otherwise noted.)

TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below



* Including Scope and Jig Capacitance

READ CYCLE

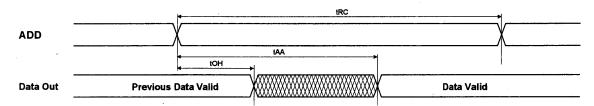
Parameter	KM68B4002-12		4002-12	KM68B4002-13		KM68B4002-15		Unit
	Symbol	Min	Max	Min	Max	Min	Max	Unit
Read Cycle Time	tRC	12	-	13	-	15	-	ns
Address Access Time	tAA	-	12	-	13	-	15	ns
Chip Select to Output	tCO		. 12	-	13	-	15	ns
Output Enable to Valid Output	tOE	-	- 6	-	- 6	-	7	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	6	0	6	. 0	7	ns
Output Disable to High-Z Output	tOHZ	0	6	0	6	0 ·	7	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns

WRITE CYCLE

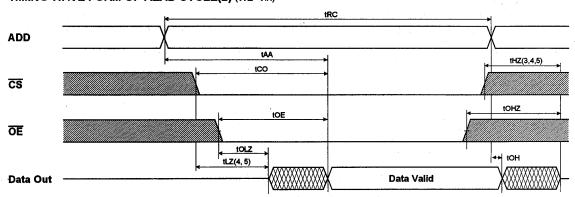
Parameter	SL.1	KM68B4002-12		KM68B4002-13		KM68B4002-15		Unit
	Symbol -	Min	Max	Min	Max	Min	Max	7 Ona
Write Cycle Time	tWC	12	-	13	-	15	-	ns
Chip Select to End of Write	tCW	8	-	9	-	10	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	пѕ
Address Valid to End of Write	tAW	8	-	9	-	10	-	ns
Write Pulse Width(OE High)	tWP	8	•	. 9		10	-	ns
Write Pulse Width(OE Low)	tWP1	10	-	11	-	12	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	6	0	6	0	7	ns
Data to Write Time Overlap	tDW	6	-	6	-	7	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{\text{CS}} = \overline{\text{OE}} = \text{VIL}, \overline{\text{WE}} = \text{VIH})$



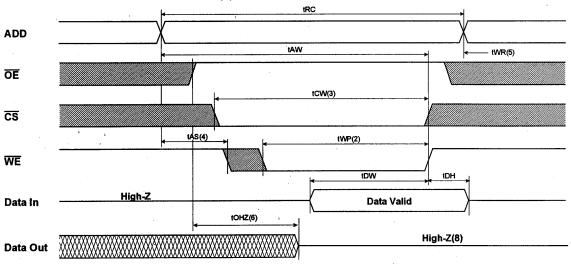
TIMING WAVE FORM OF READ CYCLE(2) (WE=VIH)



NOTES(READ CYCLE)

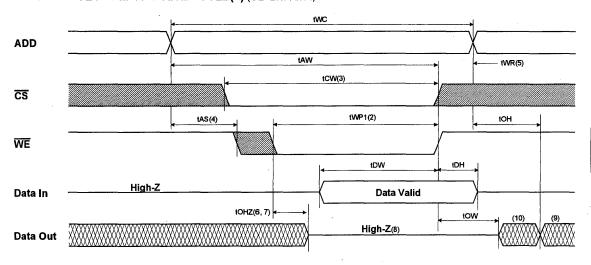
- 1. WE is high for read cycle.
- 2. All read cycle timing is referenced from the last valid address to the first transition address.
- 3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL Levels.
- 4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
- 5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
- 6. Device is continuously selected with CS=VIL.
- 7. Address valid prior to coincident with CS transition low.
- 8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVE FORM OF WRITE CYCLE(1) (OE=Clock)

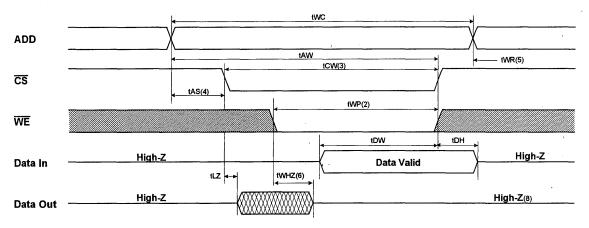




TIMING WAVE FORM OF WRITE CYCLE(2) (OE=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) (CS=Controlled)



NOTES(WRITE CYCLE)

- 1. All write cycle timing is referenced from the last valid address to the first transition address.
- 2. A write occurs during the overlap of a low \overline{CS} and \overline{WE} . A write begins at the latest transition \overline{CS} going low and \overline{WE} going low; A write ends at the earliest transition \overline{CS} going high or \overline{WE} going high. tWP is measured from the beginning of write to the end of write.
- 3. tCW is measured from the later of CS going low to end of write.
- 4. tAS is measured from the address valid to the beginning of write.
- 5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as CS or WE going high.
- 6. If \overline{OE} , \overline{CS} and \overline{WE} are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
- 7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
- 8. If CS goes low simultaneously with WE going or after WE going low, the outputs remain high impedance state.
- 9. Dout is the read data of the new address.
- 10. When $\overline{\text{CS}}$ is low: I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

ĊŚ	. WE	ŌĒ	Mode	I/O Pin	Supply Current
Н	X	X* ′	Not Select	High-Z	ISB, ISB1
L	Н	Н	Output Disable	High-Z	lcc lcc
L	Н	L	Read	Dout	lcc
L	L	Х	Write	Din	Icc

^{*} NOTE : X means Don't Care.

512K x 8 Bit High-Speed CMOS Static RAM

FEATURES

- Fast Access Time 15,17,20 ns (Max.)
- · Low Power Dissipation

Standby (TTL) : 50mA(Max.)

(CMOS): 10mA(Max.)

Operating KM684002A - 15: 170mA(Max.)

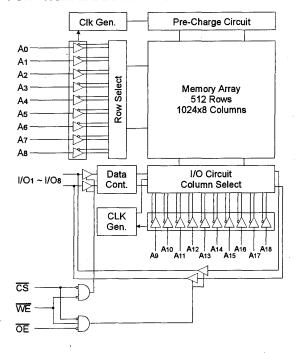
KM684002A - 17: 165mA(Max.)

KM684002A - 20: 160mA(Max.)

- Single 5.0V±10% Power Supply
- . TTL Compatible Inputs and Outputs
- . I/O Compatible with 3.3V Device
- · Fully Static Operation
- No Clock or Refresh required
- . Three State Outputs
- · Center Power/Ground Pin Configuration
- · Standard Pin Configuration

KM684002AJ: 36-SOJ-400

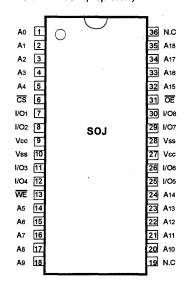
FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The KM684002A is a 4,194,304-bit high-speed Static Random Access Memory organized as 524,288 words by 8 bits. The KM684002A uses 8 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM684002A is packaged in a 400 mil 36-pin plastic SOJ.

PIN CONFIGURATION(Top View)



PIN FUNCTION

Pin Name	Pin Function
A0 - A18	Address Inputs
WE	Write Enable
CS	Chip Select
ŌĒ	Output Enable
1/01 ~ 1/08	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground
N.C	No Connection



KM684002A CMOS SRAM

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	VIN, VOUT	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	Vcc	-0.5 to 7.0	' V
Power Dissipation	Po	1.0	W
Storage Temperature	Тѕтс	-65 to 150	°
Operating Temperature	TA	0 to 70	Ĉ

^{*} Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(TA = 0 to 70°C)

Parameter	Symbol	Min	Тур	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	· V
Input Low Voltage	ViH	2.2	-	Vcc + 0.5**	V
Input Low Voltage	VIL	-0.5*	-	0.8	V

^{*} VIL(Min) = -2.0V a.c(Pulse Width \leq 10ns) for $1 \leq$ 20mÅ

DC AND OPERATING CHARACTERISTICS(TA = 0 to 70 °C, Vcc= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	lu	VIN = Vss to Vcc		-2	2	μA
Output Leakage Current	lLO	CS=VIH or OE=VIH or WE=VIL Vout = Vss to Vcc		-2	2	μA
Operating Current	Icc	Min. Cycle, 100% Duty CS=VIL, VIN = VIH or V _I L, IOUT=0mA	15ns	•	170	mΑ
			17ns	•	165	
			20ns	-	160	
Standby Current	IsB	Min. Cycle, CS=Vін		•	50	mA
	ISB1	f=0MHz, $\overline{CS} \ge Vcc-0.2V$, Vin $\ge Vcc-0.2V$ or Vin $\le 0.2V$		-	10	mA
Output Low Voltage Level	Vol	IOL=8mA		-	0.4	٧
Output High Voltage Level	Voн	IOH=-4mA		2.4		٧
	Vон1*	Iон1=-0.1mA		-	3.95	٧,

^{*} Vcc=5.0V ± 5% Temp. = 25℃

CAPACITANCE*(TA =25°C, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	CI/O	VI/0=0V	-	8	pF
Input Capacitance	CIN	VIN=0V	•	7	pF

^{*} NOTE : Capacitance is sampled and not 100% tested.



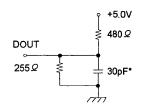
^{**} VIH(Max) = Vcc + 2.0V a.c (Pulse Width ≤ 10ns) for I ≤ 20mA

AC CHARACTERISTICS(TA = 0 to 70 °C, Vcc = $5.0V\pm10\%$, unless otherwise noted.)

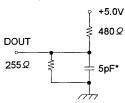
TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

Output Loads(A)



Output Loads(B) for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

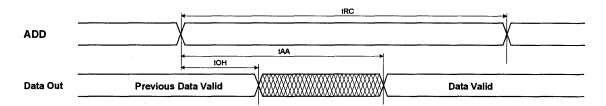
READ CYCLE

Parameter	C	KM684	002A-15	KM68400	02A-17	KM6840	002A-20	Unit
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Onit
Read Cycle Time	tRC	15	-	17	-	20	-	ns
Address Access Time	tAA	_	15	-	17	-	20	ns
Chip Select to Output	tCO	-	15	-	17	-	20	ns
Output Enable to Valid Output	tOE	-	7	- 1	8	-	9	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	7	0	8	0	9	ns
Output Disable to High-Z Output	tOHZ	0	. 7	0	8	0	9	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	0	_	ns
Chip Selection to Power DownTime	tPD	-	15		17	-	20	ns

WRITE CYCLE

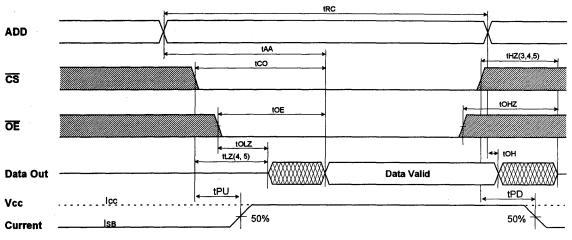
Parameter		KM684	002A-15	KM684	002A-17	KM684	002A-20	
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit
Write Cycle Time	tWC	15	-	17	-	20	-	ns
Chip Select to End of Write	tCW	12	-	13	-	14	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	12	-	13	-	14	-	ns
Write Pulse Width(OE High)	tWP	12	-	13	<i>'</i> -	14	-	ns
Write Pulse Width(OE Low)	tWP1	15	-	17	-	20	-	ns
Write Recovery Time	tWR	0	-	0	-	0	1 -	ns
Write to Output High-Z	tWHZ	0	7	0	8	0	9	ns
Data to Write Time Overlap	tDW	- 8	-	9	-	10	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

TIMING DIAGRAMS TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, CS=OE=VIL, WE=VIH)





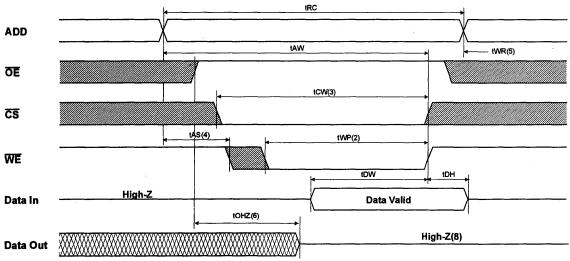
TIMING WAVE FORM OF READ CYCLE(2) (WE=VIH)



NOTES(READ CYCLE)

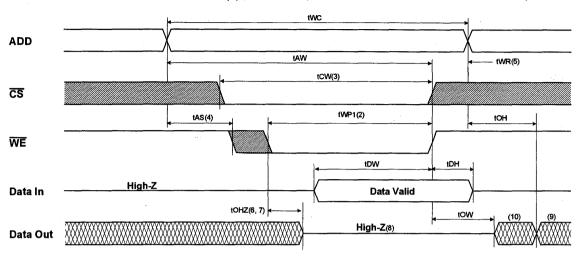
- 1. WE is high for read cycle.
- 2. All read cycle timing is referenced from the last valid address to the first transition address.
- 3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VoH or VoL Levels.
- 4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
- 5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
- 6. Device is continuously selected with CS=VIL.
- 7. Address valid prior to coincident with CS transition low.
- 8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVE FORM OF WRITE CYCLE(1) (OE=Clock)

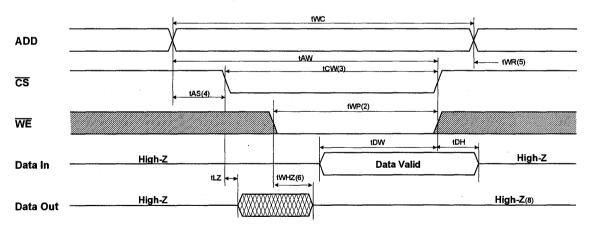




TIMING WAVE FORM OF WRITE CYCLE(2) (OE=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) (CS=Controlled)



NOTES(WRITE CYCLE)

- 1. All write cycle timing is referenced from the last valid address to the first transition address.
- A write occurs during the overlap of a low CS and WE. A write begins at the latest transition CS going low and WE going low; A write ends at the earliest transition CS going high or WE going high. tWP is measured from the beginning of write to the end of write.
 tCW is measured from the later of CS going low to end of write.
- 4. tAS is measured from the address valid to the beginning of write.
- 5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as CS or WE going high.
- 6. If OE, CS and WE are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
- 7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
- 8. If \overline{CS} goes low simultaneously with \overline{WE} going or after \overline{WE} going low, the outputs remain high impedance state.
- 9. Dout is the read data of the new address.
- 10. When CS is low: I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

CS	WE	ŌĒ	Mode	I/O Pin	Supply Current
Н	Х	X*	Not Select	High-Z	ISB, ISB1
L	Н	H	Output Disable	High-Z	lcc
L	н	L	Read	Dout	lcc
L	L	Χ	Write	DIN	lcc

^{*} NOTE : X means Don't Care.



512K x 8 Bit High-Speed CMOS Static RAM

FEATURES

Fast Access Time 17,20,25 ns (Max.)

· Low Power Dissipation

Standby (TTL) : 60mA(Max.)

(CMOS): 10mA(Max.)

Operating KM684002 - 17: 180mA(Max.)

KM684002 - 20: 170mA(Max.)

KM684002 - 25 : 160mA(Max.)

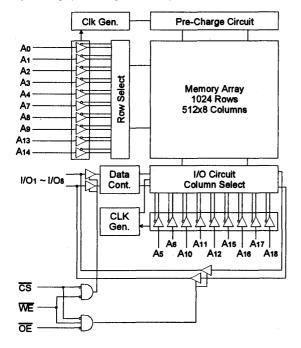
- Single 5.0V ± 10% Power Supply
- TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Device
- · Fully Static Operation
- No Clock or Refresh required
- . Three State Outputs
- · Center Power/Ground Pin Configuration
- · Standard Pin Configuration

KM684002J: 36-SOJ-400

ORDERING INFORMATION

KM684002 -17/20/25	Commercial Temp.
KM684002E -17/20/25	Extended Temp.
KM684002I -17/20/25	Industrial Temp.

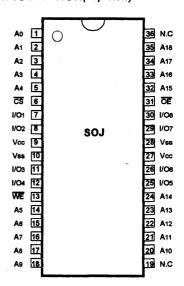
FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The KM684002 is a 4,194,304-bit high-speed Static Random Access Memory organized as 524,288 words by 8 bits. The KM684002 uses 8 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM684002 is packaged in a 400 mil 36-pin plastic SOJ.

PIN CONFIGURATION(Top View)



PIN FUNCTION

Pin Name	Pin Function
A0 - A18	Address Inputs
WE	Write Enable
CS	Chip Select
ŌĒ	Output Enable
1/01 ~ 1/08	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS*

Param	eter	Symbol	Rating	Unit
Voltage on Any Pin Relati	ve to Vss	VIN, VOUT	-0.5 to 7.0	V
Voltage on Vcc Supply R	elative to Vss	Vcc	-0.5 to 7.0	V
Power Dissipation		PD	1.0	W
Storage Temperature		Тѕтс	-65 to 150	°C
Operating Temperature	Commercial	TA	0 to 70	°C
	Extended	TA	-25 to 85	°C
	Industrial	TA	-40 to 85	°C

^{*} Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(TA = 0 to 70°C)

Parameter	Symbol	Min	Тур	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	٧
Input Low Voltage	ViH	2.2	-	Vcc + 0.5**	V
Input Low Voltage	VIL	-0.5*	-	0.8	V

NOTE: Above parameters are also guaranteed at extended and industrial temperature ranges.

- * VIL(Min) = -2.0V a.c(Pulse Width≤10ns) for I ≤ 20mA
- ** VIH(Max) = Vcc + 2.0V a.c (Pulse Width \leq 10ns) for I \leq 20mA

DC AND OPERATING CHARACTERISTICS(TA = 0 to 70 °C, Vcc= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	ILI	Vin = Vss to Vcc		-2	2	μA
Output Leakage Current	lLO	CS=Vih or OE=Vih or WE=ViL Vout = Vss to Vcc		-2	2	μA
Operating Current	Icc	Min. Cycle, 100% Duty	17ns	-	180	mA
		CS=VIL, VIN = VIH or VIL, IOUT=0mA	20ns	-	170	
			25ns	-	160	
Standby Current	ISB	Min. Cycle, CS=VIH		-	60	mΑ
	ISB1	f=0MHz, $\overline{\text{CS}} \ge \text{Vcc-0.2V}$, Vin $\ge \text{Vcc-0.2V}$ or Vin $\le 0.2\text{V}$		-	10	mА
Output Low Voltage Level	VoL	IOL=8mA		-	0.4	٧
Output High Voltage Level	Voн	IOH=-4mA		2.4	-	V
	Vон1*	Юн1=-0.1mA		-	3.95	>

NOTE: Above parameters are also guaranteed at extended and industrial temperature ranges.

CAPACITANCE*(TA =25°C, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	CI/O	VI/0=0V	-	8	pF ·
Input Capacitance	CIN	VIN=0V	-	6	pF

^{*} NOTE: Capacitance is sampled and not 100% tested.



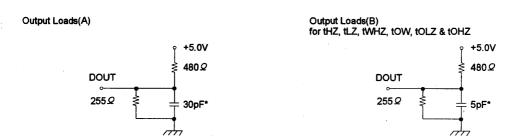
^{*}Vcc=5.0V ± 5% Temp. = 25°C

AC CHARACTERISTICS(TA = 0 to 70 °C, Vcc = $5.0V \pm 10\%$, unless otherwise noted.)

TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

NOTE: Above test conditions are also applied at industrial temperature range.



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	0b1	KM684002-17		KM684002-20		KM684002-25		11
	Symbol	Min	Max	Min	Max	Min	Max	- Unit
Read Cycle Time	tRC	17	•	20	-	25	-	ns
Address Access Time	tAA	-	17	-	20	-	25	ns
Chip Select to Output	tCO	-	17	-	20	-	25	ns
Output Enable to Valid Output	tOE	-	8	-	10	-	12	ns
Chip Enable to Low-Z Output	tLZ	3	•	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	7	0	8	0	10	ns
Output Disable to High-Z Output	tOHZ	0	7	0	8	0	10	ns
Output Hold from Address Change	tOH	3	-	4	-	5	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	0	-	ns
Chip Selection to Power DownTime	tPD	-	17	-	20	•	25	ns

NOTE: Above parameters are also guaranteed at extended and industrial temperature ranges.



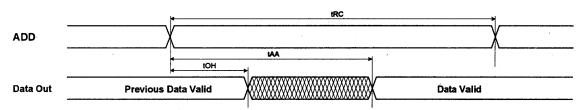
WRITE CYCLE

Parameter	6	KM684002-17		KM684002-20		KM684002-25		T
	Symbol -	Min	Max	Min	Max	Min	Max	Unit
Write Cycle Time	tWC	17	-	20	-	25	-	ns
Chip Select to End of Write	tCW	12	-	13	-	15	-	ns
Address Set-up Time	tAS	0	-	0	•	0		ns
Address Valid to End of Write	tAW	12	-	13	-	15	-	ns
Write Pulse Width(OE High)	tWP	12	-	13	-	15	-	ns
Write Pulse Width(OE Low)	tWP1	17	-	20	-	25	-	ns
Write Recovery Time	tWR	0	-	0	-	0	•	ns
Write to Output High-Z	tWHZ	0	8	0	8	0	10	ns
Data to Write Time Overlap	tDW	8	-	9	-	10	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	4	-	5	-	ns

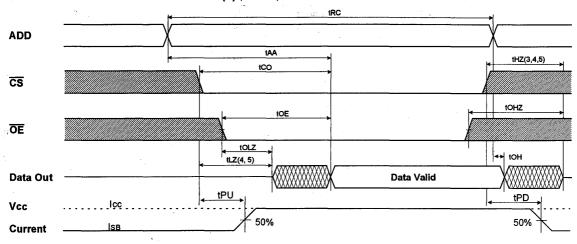
NOTE: Above parameters are also guaranteed at extended and industrial temperature range.

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS} = \overline{OE} = VIL, \overline{WE} = VIH)$



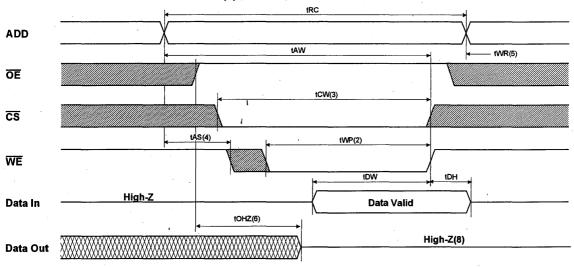
TIMING WAVE FORM OF READ CYCLE(2) (WE=VIH)



NOTES(READ CYCLE)

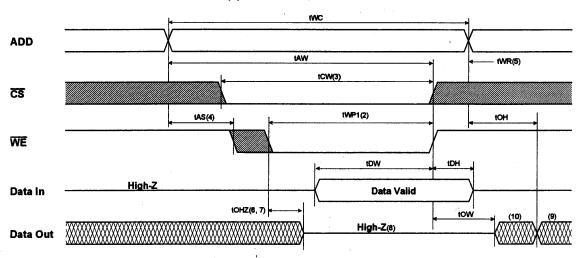
- 1. WE is high for read cycle.
- 2. All read cycle timing is referenced from the last valid address to the first transition address.
- 3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL Levels.
- 4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
- 5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
- 6. Device is continuously selected with CS=VIL.
- 7. Address valid prior to coincident with $\overline{\text{CS}}$ transition low.
- 8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVE FORM OF WRITE CYCLE(1) (OE=Clock)

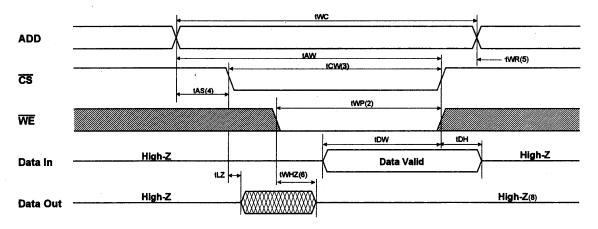




TIMING WAVE FORM OF WRITE CYCLE(2) (OE=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) (CS=Controlled)



NOTES(WRITE CYCLE)

- 1. All write cycle timing is referenced from the last valid address to the first transition address.
- A write occurs during the overlap of a low CS and WE. A write begins at the latest transition CS going low and WE going low; A write ends at the earliest transition CS going high or WE going high. tWP is measured from the beginning of write to the end of write.
 tCW is measured from the later of CS going low to end of write.
- 4. tAS is measured from the address valid to the beginning of write.
- 5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as CS or WE going high.
- 6. If OE, CS and WE are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
- 7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
- 8. If CS goes low simultaneously with WE going or after WE going low, the outputs remain high impedance state.
- 9. Dout is the read data of the new address.
- 10. When CS is low: I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

ĊŚ	WE	ŌĒ	Mode	I/O Pin	Supply Current
Н	. X	X*	Not Select	High-Z	ISB, ISB1
L	Н	Н	Output Disable	High-Z	lcc
L	Н	L	Read	Dout	lcc
L	L	X	Write	Din	lcc

^{*} NOTE: X means Don't Care.

KM6164002B, KM6164002BI

256K x 16 Bit High-Speed CMOS Static RAM

FEATURES

- Fast Access Time 10,12,15 ns (Max.)
- · Low Power Dissipation

Standby (TTL) : 40mA(Max.)

(CMOS): 10mA(Max.)

Operating KM6164002B - 10: 250mA(Max.)

KM6164002B - 12: 240mA(Max.)

KM6164002B - 15: 230mA(Max.)

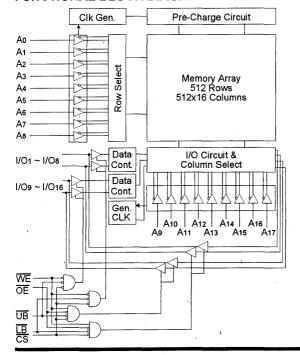
- Single 5.0V ± 10% Power Supply
- . TTL Compatible Inputs and Outputs
- . I/O Compatible with 3.3V Device
- Fully Static Operation
- No Clock or Refresh required
- · Three State Outputs
- · Center Power/Ground Pin Configuration
- Data Byte Control : LB : I/O1~ I/O8, UB : I/O9~ I/O16
- · Standard Pin Configuration

KM6164002BJ: 44-SOJ-400 KM6164002BT: 44-TSOP2-400F

ORDERING INFORMATION

KM6164002B -10/12/15	Commercial Temp.
KM6164002BI -10/12/15	Industrial Temp.

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The KM6164002B is a 4,194,304-bit high-speed Static Random Access Memory organized as 262,144 words by 16 bits. The KM6164002B uses 16 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. Also it allows that lower and upper byte access by data byte control (UB, LB). The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM6164002B is packaged in a 400mil 44-pin plastic SOJ or TSOP(II) forward.

PIN CONFIGURATION (Top View)

		\ 7		Щ	
A0 1	\bigcirc	\bigcirc		44	A17
A1 2	_			43	A 16
A2 3	ł			42	A 15
A3 4	l			41	Œ
A4 5	l			40	ŪΒ
CS 6				39	ĹВ
1/01 7				38	1/016
1/02 8	ł			37	I/O15
I/O3 9	į			36	1/014
1/04 10	ł	SOJ/		35	1/013
Vcc 11	ł	TSOP2	2		Vss
Vss 12	ł			33	Vcc
1/05 13	ŀ			32	I/O12
1/06 14	ł			31	1/011
1/07 15				30	1/010
1/08 16	l			29	1/09
WE 17	l	,		28	N.C
A5 18				27	A14
A6 19	ł				A13
	l				
A7 20	l		i	25	A12
A8 21	ł			24	A11
A9 22	J.			23	A10

PIN FUNCTION

Pin Name	Pin Function
Ao - A17	Address Inputs
WE	Write Enable
CS	Chip Select
ŌĒ	Output Enable
LB	Lower-byte Control(I/O1~I/O8)
UB	Upper-byte Control(I/O9~I/O16)
I/O1 ~ I/O16	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground
N.C	No Connection



ABSOLUTE MAXIMUM RATINGS*

Param	eter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss		VIN, VOUT	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss		Vcc	-0.5 to 7.0	V .
Power Dissipation		PD	1.0	W
Storage Temperature		Тѕтс	-65 to 150	°C
Operating Temperature	Commercial	ТА	0 to 70	°C
	Industrial	TA	-40 to 85	Ç

^{*} Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(TA = 0 to 70°C)

Parameter	Symbol	Min	Тур	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input Low Voltage	ViH	2.2	-	Vcc + 0.5**	V
Input Low Voltage	VIL	-0.5*	-	0.8	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

* VIL(Min) = -2.0V a.c(Pulse Width≤8ns) for I ≤ 20mA

** VIH(Max) = Vcc + 2.0V a.c (Pulse Width \leq 8ns) for I \leq 20mÅ

DC AND OPERATING CHARACTERISTICS (TA = 0 to 70 °C, Vcc= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	lu	VIN = Vss to Vcc		-2	2	μA
Output Leakage Current	lLO	ÇS=Vih or OE=Vih or WE=Vil Vout = Vss to Vcc		-2	2	μA
Operating Current	lcc	Min. Cycle, 100% Duty	10ns		250	mA
		CS=VIL, VIN = VIH or VIL, IOUT=0mA	12ns	-	240	
		·	15ns	-	230	
Standby Current	ISB	Min. Cycle, CS=ViH	-	40	mΑ	
	ISB1	f=0MHz, $\overline{\text{CS}} \ge \text{Vcc-0.2V}$, Vin $\ge \text{Vcc-0.2V}$ or Vin $\le 0.2\text{V}$		-	10	mА
Output Low Voltage Level	Vol	IoL=8mA		-	0.4	V
Output High Voltage Level	Voн	IOH=-4mA		2.4	-	V
	VoH1*	юн1=-0.1mA	•	3.95	٧٠	

NOTE: Above parameters are also guaranteed at industrial temperature range.

CAPACITANCE*(TA =25°C, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	CI/O	VI/0=0V	-	8	pF
Input Capacitance	Cin	VIN=0V	-	7	pF

^{*} NOTE: Capacitance is sampled and not 100% tested.



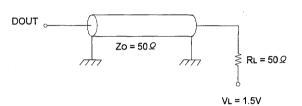
^{*} Vcc=5.0V ± 10% Temp. = 25°C

AC CHARACTERISTICS(TA = 0 to 70 $^{\circ}$ C, Vcc = 5.0V $^{\pm}$ 10%, unless otherwise noted.)

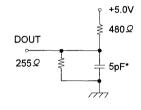
TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3 ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below





Output Loads(B) for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

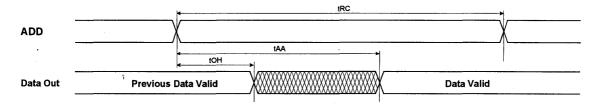
Parameter		KM6164002B-10		KM6164002B-12		KM6164002B-15		Unit
	Symbol	Min	Max	Min	Max	Min	Max	- Unit
Read Cycle Time	tRC	10	-	12	-	15	-	ns
Address Access Time	tAA	-	10	-	12	-	15	ns
Chip Select to Output	tCO	-	10	-	12	-	15	ns
Output Enable to Valid Output	tOE	-	5	-	6	-	7	ns
UB, LB Access Time	tBA	-	5	-	6	-	7	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ ·	0	-	0	-	0	-	ns
UB, LB Enable to Low-Z Output	tBLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	5	0	6	0	7	ns
Output Disable to High-Z Output	tOHZ	0	5	0	6	0	7	ns
UB, LB Disable to High-Z Output	tBHZ	0	5	. 0	6	0	7	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns

WRITE CYCLE

	Symbol	KM6164002B-10		KM6164002B-12		KM6164002B-15		·
Parameter		Min	Max	Min	Max	Min	Max	Unit
Write Cycle Time	tWC	10	-	12	-	15	-	ns
Chip Select to End of Write	tCW	7	-	8	-	10	-	ns
Address Set-up Time	tAS	0	-	0 .		0	-	ns
Address Valid to End of Write	tAW	7	-	8	-	10	-	ns
Write Pulse Width(OE High)	tWP	7	-	8	-	10	-	ns
Write Pulse Width(OE Low)	tWP1	10	-	12	-	15	-	ns
UB, LB Valid to End of Write	tBW	7	-	8	-	10	-	ns
Write Recovery Time	tWR	0	_	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	5	0	6	0	7	ns
Data to Write Time Overlap tDW		5	-	6	-	7	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3 .	-	3	-	3	-	ns

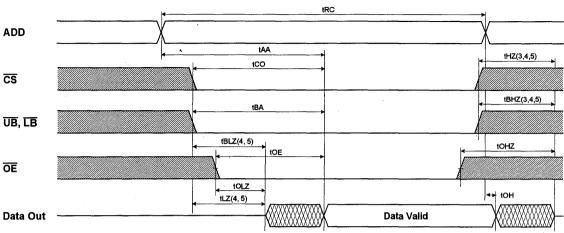
TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS} = \overline{DE} = \overline{UB} = \overline{LB} = VIL, \overline{WE} = VIH)$





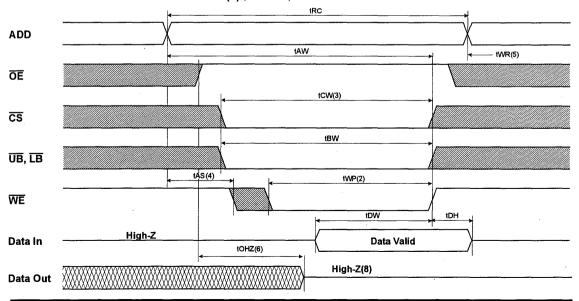
TIMING WAVE FORM OF READ CYCLE(2) (WE=VIH)



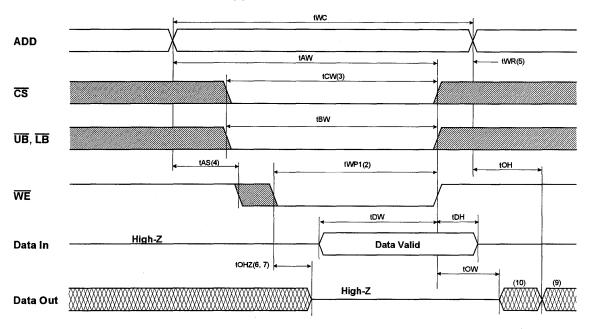
NOTES(READ CYCLE)

- 1. WE is high for read cycle.
- 2. All read cycle timing is referenced from the last valid address to the first transition address.
- 3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VoH or VoL Levels.
- 4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
- 5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
- 6. Device is continuously selected with CS=VIL.
- 7. Address valid prior to coincident with CS transition low.
- 8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

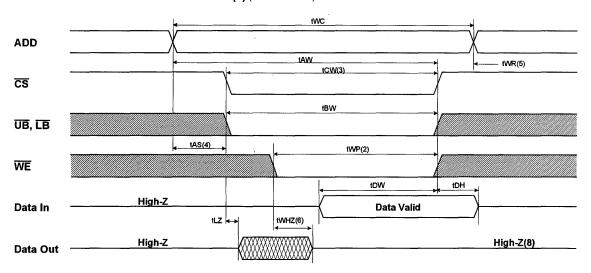
TIMING WAVE FORM OF WRITE CYCLE(1) (OE=Clock)



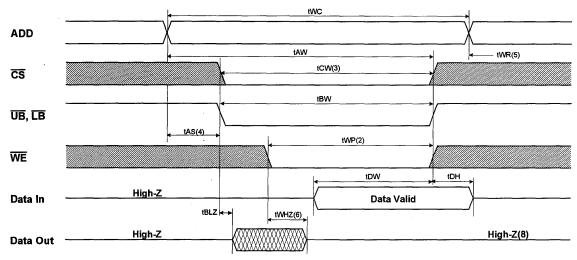
TIMING WAVE FORM OF WRITE CYCLE(2) (OE=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) (CS=Controlled)



TIMING WAVE FORM OF WRITE CYCLE(4) (UB, LB Controlled)



NOTES(WRITE CYCLE)

- 1. All write cycle timing is referenced from the last valid address to the first transition address.
- 2. A write occurs during the overlap of a low \overline{CS} , \overline{WE} , \overline{LB} and \overline{UB} . A write begins at the latest transition \overline{CS} going low and \overline{WE} going low; A write ends at the earliest transition \overline{CS} going high or \overline{WE} going high. tWP is measured from the beginning of write to the end of write.
- 3. tCW is measured from the later of \overline{CS} going low to end of write.
- 4. tAS is measured from the address valid to the beginning of write.
- 5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as $\overline{\text{CS}}$, or $\overline{\text{WE}}$ going high.
- 6. If OE. CS and WE are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
- 7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
- 8. If $\overline{\text{CS}}$ goes low simultaneously with $\overline{\text{WE}}$ going or after $\overline{\text{WE}}$ going low, the outputs remain high impedance state.
- 9. Dout is the read data of the new address.
- 10. When $\overline{\text{CS}}$ is low: I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

CS WE	WE	ŌĒ	LB	UB	Mode	1/0	Supply Current	
	**					1/01~1/08	I/O9~I/O16	Supply Curren
Н	Χ	Χ*	Х	X	Not Select	High-Z		ISB, ISB1
L	Н	Н	X	X	Output Disable	High-Z	High-Z	Icc
L	X	Х	Н	Н				
L	Н	L	L	Н	Read	Dout	High-Z	Icc
			Н_	L		High-Z	Dout	
			L	L		Dout	Dout	
L	L	Х	L	Н	Write	DIN	High-Z	lcc
			Н	L		High-Z	DIN	
			L	L		DIN	DIN	

^{*} NOTE: X means Don't Care.



256K x 16 Bit High-Speed BiCMOS Static RAM

FEATURES

- Fast Access Time 12,13,15 ns (Max.)
- · Low Power Dissipation

Standby (TTL) : 60mA(Max.)

(CMOS): 30mA(Max.)

Operating KM616B4002 - 12: 270mA(Max.)

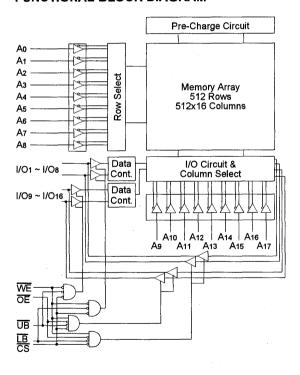
KM616B4002 - 13 : 265mA(Max.)

KM616B4002 - 15 : 260mA(Max.)

- Single 5.0V±10% Power Supply
- . TTL Compatible Inputs and Outputs
- · Fully Static Operation
 - No Clock or Refresh required
- . Three State Outputs
- · Center Power/Ground Pin Configuration
- Data Byte Control : LB : I/O1~ I/O8, UB : I/O9~ I/O16
- . Standard Pin Configuration

KM616B4002J: 44-SOJ-400

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The KM616B4002 is a 4,194,304-bit high-speed Static Random Access Memory organized as 262,144 words by 16 bits. The KM616B4002 uses 16 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. Also it allows that lower and upper byte access by data byte control (UB, LB). The device is fabricated using SAMSUNG's advanced BicMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM616B4002 is packaged in a 400mil 44-pin plastic SOJ.

PIN CONFIGURATION (Top View)

A0 1 2 3 4 4 5 6 7 8 10 10 10 10 10 10 10 10 10 10 10 10 10	0	soJ	i selesi iselesi iselesi iselesi iselesi iselesi iselesi iselesi iselesi iselesi iselesi iselesi iselesi iselesi	43 42 41 40 39 38 37 36 35 33 33 32 28 27 26	A17 A16 A15 OE UB I/O10
A7 20 A8 21					A12 A11
A9 22			Į.	=	A10

PIN FUNCTION

Pin Name	Pin Function				
A0 - A17	Address Inputs				
WE	Write Enable				
CS	Chip Select				
ŌĒ	Output Enable				
LB	Lower-byte Control(I/O1~I/O8)				
UB	Upper-byte Control(I/O9~I/O16)				
1/01 ~ 1/016	Data Inputs/Outputs				
Vcc	Power(+5.0V)				
Vss	Ground				
N.C_	No Connection				

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	VIN, VOUT	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	Vcc	-0.5 to 7.0	V
Power Dissipation	Pp	1.0	W
Storage Temperature	Тѕтс	-65 to 150	°C
Operating Temperature	TA	0 to 70	°C

^{*} Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(TA = 0 to 70°C)

Parameter	Symbol	Min	Тур	Max	
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input Low Voltage	VIH	2.2	-	Vcc + 0.5**	V
Input Low Voltage	ViL	-0.5*	-	0.8	V

^{*} VIL(Min) = -2.0V a.c(Pulse Width \leq 10ns) for $1 \leq 20$ mÅ

DC AND OPERATING CHARACTERISTICS(TA = 0 to 70 °C, Vcc= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	lLi	Vin = Vss to Vcc		-2	2	μA
Output Leakage Current	llo	CS=VIH or OE=VIH or WE=VIL VOUT = Vss to Vcc	-10	10	μA	
Operating Current			12ns	-	270	mΑ
		CS=VIL, VIN = VIH or VIL, IOUT=0mA	13ns	-	265	
			15ns	-	260	
Standby Current	İSB	Min. Cycle, CS=Viн		-	60	mA
Isb1			-	30	mA	
Output Low Voltage Level	Vol	IoL=8mA		-	0.4	٧
Output High Voltage Level	Voн	IOH=-4mA		2.4	-	V

CAPACITANCE*(TA =25°C, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	CI/O	Vi/o=0V	-	8	pF
Input Capacitance	Cin	VIN=0V	-	7	pF

^{*} NOTE: Capacitance is sampled and not 100% tested.

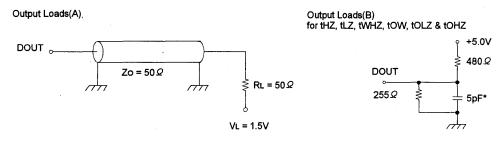


^{**} $VIH(Max) = Vcc + 2.0V a.c (Pulse Width \le 10ns) for I \le 20mA$

AC CHARACTERISTICS(TA = 0 to 70 °C, Vcc = $5.0V \pm 10\%$, unless otherwise noted.)

TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below



* Including Scope and Jig Capacitance

READ CYCLE

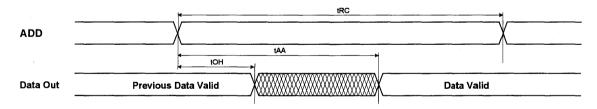
Parameter		KM616B4002-12		KM616B4002-13		KM616B4002-15		
	Symbol	Min	Max	Min	Max	Min	Max	Unit
Read Cycle Time	tRC	12 .	-	13	-	15	-	ns
Address Access Time	tAA	•	12	-	13	-	15	ns
Chip Select to Output	tCO	-	12	-	13	-	15	ns
Output Enable to Valid Output	tOE	-	6	-	6	-	7	ns
UB, LB Access Time	tBA	-	6	-	6	-	7	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
UB, LB Enable to Low-Z Output	tBLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	6	0	6	0	7	ns
Output Disable to High-Z Output tOH		0	6	0	6	0	7	ns
UB, LB Disable to High-Z Output tBHZ		0	6	0	6	0	7	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns

WRITE CYCLE

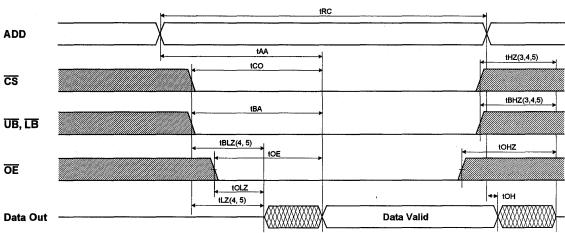
Parameter	Symbol	KM616B4002-12		KM616B4002-13		KM616B4002-15		T., .,
		Min	Max	Min	Max	Min	Max	Unit
Write Cycle Time	tWC	12	-	13	-	15	-	ns
Chip Select to End of Write	tCW	8	-	9	-	10	-	ns
Address Set-up Time tAS		0		0	_	. 0	-	ns
Address Valid to End of Write tA		8	-	9	-	10	-	ns
Write Pulse Width(OE High)	tWP	8	-	9	-	10	-	ns
Write Pulse Width(OE Low)	tWP1	10	-	11	-	12	-	ns
UB, LB Valid to End of Write tBW		8	-	9	-	10	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	6	0	6	0	7	ns
Data to Write Time Overlap tDW		6	-	6	-	7	-	ns
Data Hold from Write Time tDH		0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS} = \overline{OE} = \overline{UB} = \overline{LB} = VIL, \overline{WE} = VIH)$



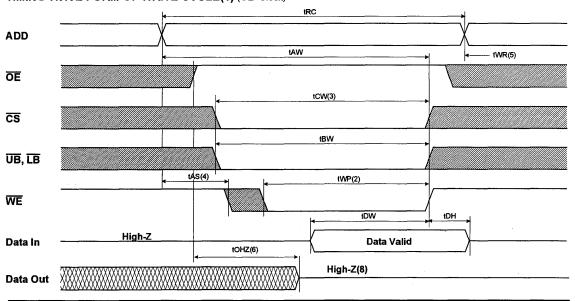
TIMING WAVE FORM OF READ CYCLE(2) (WE=VIH)



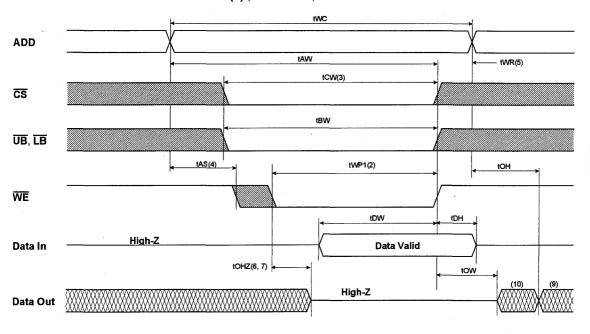
NOTES(READ CYCLE)

- 1. WE is high for read cycle.
- 2. All read cycle timing is referenced from the last valid address to the first transition address.
- tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL Levels.
- 4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
- 5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
- 6. Device is continuously selected with CS=VIL.
- 7 Address valid prior to coincident with CS transition low.
- 8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

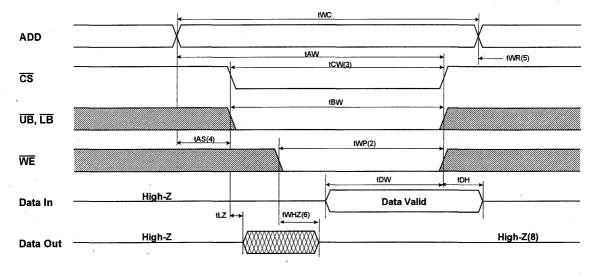
TIMING WAVE FORM OF WRITE CYCLE(1) (OE=Clock)



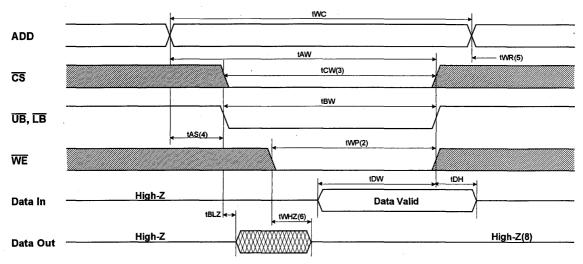
TIMING WAVE FORM OF WRITE CYCLE(2) (OE=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) (CS=Controlled)



TIMING WAVE FORM OF WRITE CYCLE(4) (UB, LB Controlled)



NOTES(WRITE CYCLE)

- 1. All write cycle timing is referenced from the last valid address to the first transition address.
- 2. A write occurs during the overlap of a low \overline{CS} , \overline{WE} , \overline{LB} and \overline{UB} . A write begins at the latest transition \overline{CS} going low and \overline{WE} going low; A write ends at the earliest transition \overline{CS} going high or \overline{WE} going high. tWP is measured from the beginning of write to the end of write.
- 3. tCW is measured from the later of CS going low to end of write.
- 4. tAS is measured from the address valid to the beginning of write.
- 5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as \overline{CS} , or \overline{WE} going high.
- 6. If OE. CS and WE are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
- 7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
- 8. If $\overline{\text{CS}}$ goes low simultaneously with $\overline{\text{WE}}$ going or after $\overline{\text{WE}}$ going low, the outputs remain high impedance state.
- 9. Dout is the read data of the new address.
- 10. When \overline{CS} is low: I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

cs	WE OE LB		B UB Mode		1/0	Supply Correct		
	WE	OL.	LD	06	Mode	I/O1~I/O8	I/O9~I/O16	Supply Current
H	Х	X*	X	Х	Not Select	High-Z		ISB, ISB1
L	н	H	Х	Х	Output Disable	High-Z	High-Z	Icc
L	Х	Х	н	Н		•		
L	Н	L	L	Н	Read	Dout	High-Z	lcc
			Н	. L		High-Z	Dout	
			L	L		Dout	Dout	
L	L	Х	L	Н	Write	Din	High-Z	Icc
			Н	L] [High-Z	Din]
			L	L		DIN	DIN	

^{*} NOTE : X means Don't Care.



256K x 16 Bit High-Speed CMOS Static RAM

FEATURES

- Fast Access Time 15, 17, 20ns (Max.)
- · Low Power Dissipation

Standby (TTL) : 50mA(Max.)

(CMOS): 10mA(Max.)

Operating KM6164002A - 15: 210mA(Max.)

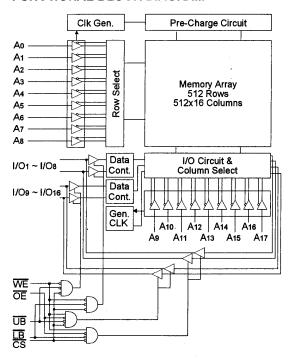
KM6164002A - 17: 205mA(Max.)

KM6164002A - 20: 200mA(Max.)

- Single 5.0V±10% Power Supply
- TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Device
- . Fully Static Operation
- No Clock or Refresh required
- . Three State Outputs
- . Center Power/Ground Pin Configuration
- Data Byte Control : LB : I/O1~ I/O8, UB : I/O9~ I/O16
- Standard Pin Configuration

KM6164002AJ: 44-SOJ-400

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The KM6164002A is a 4,194,304-bit high-speed Static Random Access Memory organized as 262,144 words by 16 bits. The KM6164002A uses 16 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. Also it allows that lower and upper byte access by data byte control (UB, LB). The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM6164002A is packaged in a 400mil 44-pin plastic SOJ.

PIN CONFIGURATION (Top View)

PIN FUNCTION

Pin Name	Pin Function
A0 - A17	Address Inputs
WE	Write Enable
CS	Chip Select
ŌĒ	Output Enable
<u>ГВ</u>	Lower-byte Control(I/O1~I/O8)
UB	Upper-byte Control(I/O9~I/O16)
I/O1 ~ I/O16	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground
N.C	No Connection



ABSOLUTE MAXIMUM RATINGS*

Parameter	· Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	VIN, VOUT	-0.5 to 7.0	٧
Voltage on Vcc Supply Relative to Vss	Vcc	-0.5 to 7.0	V
Power Dissipation	PD	1.0	W
Storage Temperature	Тѕтс	-65 to 150	°C
Operating Temperature	TA	0 to 70	°C

^{*} Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(TA = 0 to 70°C)

Parameter	Symbol	Min	Тур	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0 .	0	V
Input Low Voltage	ViH	2.2	-	Vcc + 0.5**	V
Input Low Voltage	VIL	-0.5*	•	0.8	V

^{*} VIL(Min) = -2.0V a.c(Pulse Width≤10ns) for 1 ≤ 20mA

DC AND OPERATING CHARACTERISTICS (TA = 0 to 70°C, Vcc= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	ILI	Vin = Vss to Vcc		-2	2	μA
Output Leakage Current	lLO	CS=VIH or OE=VIH or WE=VIL VOUT = Vss to Vcc		-2	2	μA
Operating Current	lcc	Min. Cycle, 100% Duty	15ns	-	210	mA
		CS=VIL, VIN = VIH or VIL, IOUT=0mA	17ns	-	205	
			20ns	-	200	
Standby Current	IsB	Min. Cycle, CS=Vін		-	50	mA
	ISB1	f=0MHz, $\overline{CS} \ge Vcc-0.2V$, Vin $\ge Vcc-0.2V$ or Vin $\le 0.2V$		-	10	mA
Output Low Voltage Level	Vol	IoL=8mA		-	0.4	V
Output High Voltage Level	Voн	IOH=-4mA		2.4	-	V
	Von1*	Iон1=-0.1mA		-	3.95	٧

^{*} Vcc=5.0V ± 5% Temp. = 25℃

CAPACITANCE*(TA =25°C, f=1.0MHz)

ltem	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	CI/O	VI/O=0V	-	8	pF
Input Capacitance	Cin	VIN=0V	-	7	pF

^{*} NÓTE : Capacitance is sampled and not 100% tested.



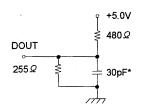
^{**} VIH(Max) = Vcc + 2.0V a.c (Pulse Width ≤ 10ns) for I ≤ 20mA

AC CHARACTERISTICS(TA = 0 to 70 °C, Vcc = $5.0V \pm 10\%$, unless otherwise noted.)

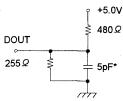
TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

Output Loads(A)



Output Loads(B) for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

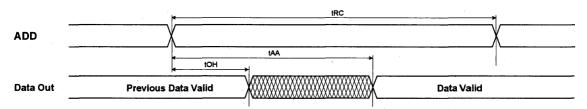
Parameter	 	KM6164002A-15		KM6164002A-17		KM6164002A-20		T
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit
Read Cycle Time	tRC	15	-	17	•	20	-	ns
Address Access Time	tAA	-	15	-	17	-	20	ns
Chip Select to Output	tCO	-	15	-	17	-	20	, ns
Output Enable to Valid Output	tOE	-	7	-	8	-	9	ns
UB, LB Access Time	tBA		7	-	8		9	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0,	-	0	-	ns
UB, LB Enable to Low-Z Output	tBLZ	0 .	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	7	. 0	8	0	9	ns
Output Disable to High-Z Output	tOHZ	0	7	0	8	0	9	ns
UB, LB Disable to High-Z Output	tBHZ	0	7	0	8	0	9	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns

WRITE CYCLE

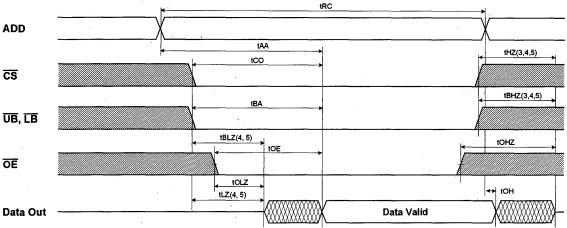
		KM6164002A-15		KM6164002A-17		KM6164002A-20		1
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit
Write Cycle Time	tWC	15	-	17	-	20	-	ns
Chip Select to End of Write	tCW	12 .	-	13	-	14	-	ns
Address Set-up Time	tAS	.0	-	0	-	. 0	-	ns
Address Valid to End of Write	tAW	12	-	13	-	14	-	ns
Write Pulse Width(OE High)	tWP	12	-	13	-	14	-	ns
Write Pulse Width(OE Low)	tWP1	15	-	17	-	20	- :	ns
UB, LB Valid to End of Write	tBW	12	-	13	-	14	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	7	0	8	0	9	ns
Data to Write Time Overlap	tDW	8	-	9	-	10	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	_	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS} = \overline{OE} = \overline{UB} = \overline{LB} = VIL$, $\overline{WE} = VIH$)



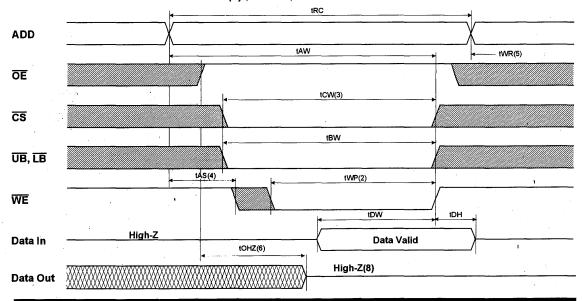
TIMING WAVE FORM OF READ CYCLE(2) (WE=VIH)



NOTES(READ CYCLE)

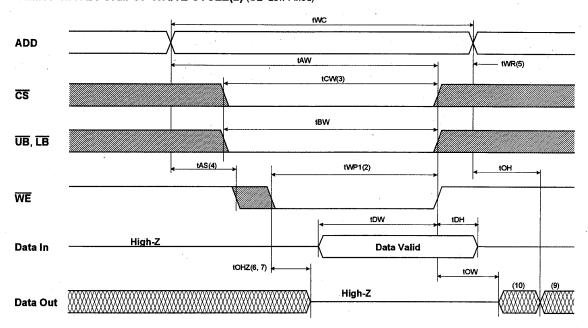
- 1. WE is high for read cycle.
- 2. All read cycle timing is referenced from the last valid address to the first transition address.
- 3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VoH or VoL Levels.
- 4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
- 5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
- 6. Device is continuously selected with CS=VIL.
- 7. Address valid prior to coincident with CS transition low.
- 8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVE FORM OF WRITE CYCLE(1) (OE=Clock)

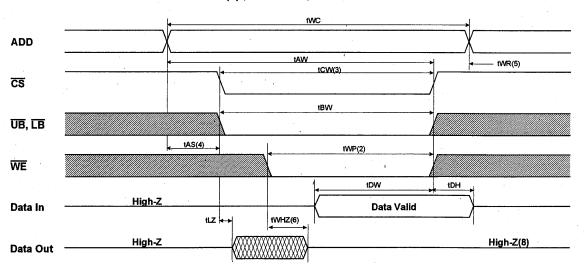




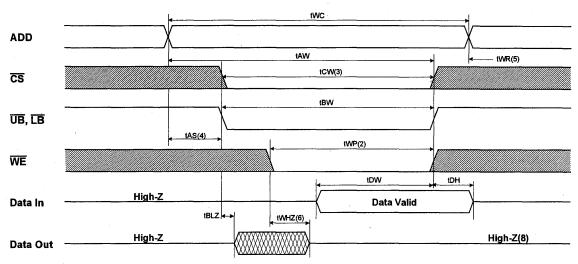
TIMING WAVE FORM OF WRITE CYCLE(2) (OE=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) (CS=Controlled)



TIMING WAVE FORM OF WRITE CYCLE(4) (UB, LB Controlled)



NOTES(WRITE CYCLE)

- 1. All write cycle timing is referenced from the last valid address to the first transition address.
- 2. A write occurs during the overlap of a low CS, WE, LB and UB. A write begins at the latest transition CS going low and WE going low; A write ends at the earliest transition CS going high or WE going high. tWP is measured from the beginning of write to the end of write.
- 3. tCW is measured from the later of CS going low to end of write.
- 4. tAS is measured from the address valid to the beginning of write.
- 5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as CS, or WE going high.
- 6. If \overline{OE} . \overline{CS} and \overline{WE} are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
- 7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
- 8. If CS goes low simultaneously with WE going or after WE going low, the outputs remain high impedance state.
- 9. Dout is the read data of the new address.
- 10. When $\overline{\text{CS}}$ is low: I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

CS	WE	ŌĒ	LB.	UB	Mode I/O Pin Supply	I/O Pin		Supply Current
- 03	WE	OL.	LD	OB	Mode	I/O1~I/O8	1/09~1/016	Supply Guitent
н	Х	X*	Х	Х	Not Select	High-Z		ISB, ISB1
L	Н	н	Х	Х	Output Disable	High-Z	High-Z	Icc
L	Х	Х	Н	Н			<u> </u>	1
L	Н	L	L	Н	Read	Dout	High-Z	lcc
			Н	L		High-Z	Dout	
			L	L		Dout	Dout	
L	L	Х	L	Н	Write	DIN	High-Z	Icc
ļ ·		Ì	Н	L		High-Z	DIN	
			L_	L		DIN	DIN	

^{*} NOTE: X means Don't Care.



256K x 16 Bit High-Speed CMOS Static RAM

FEATURES

- Fast Access Time 20,25 ns (Max.)
- · Low Power Dissipation

Standby (TTL) : 60mA(Max.)

(CMOS) : 10mA(Max.)

Operating KM6164002 - 20: 240mA(Max.)

KM6164002 - 25: 220mA(Max.)

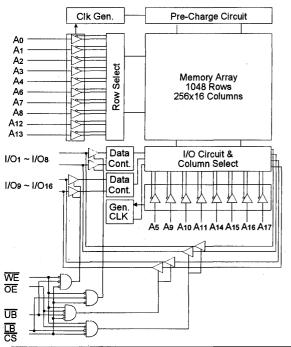
- Single $5.0V \pm 10\%$ Power Supply
- TTL Compatible Inputs and Outputs
- . I/O Compatible with 3.3V Device
- . Fully Static Operation
- No Clock or Refresh required
- · Three State Outputs
- · Center Power/Ground Pin Configuration
- Data Byte Control : LB : I/O1~ I/O8, UB : I/O9~ I/O16
- · Standard Pin Configuration

KM6164002J: 44-SOJ-400

ORDERING INFORMATION

KM6164002 -20/25	Commercial Temp.
KM6164002E -20/25	Extended Temp.
KM6164002I -20/25	Industrial Temp.

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The KM6164002 is a 4,194,304-bit high-speed Static Random Access Memory organized as 262,144 words by 16 bits. The KM6164002 uses 16 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. Also it allows that lower and upper byte access by data byte control (UB, LB). The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM6164002 is packaged in a 400mil 44-pin plastic SOJ.

PIN CONFIGURATION (Top View)

A0 1 A1 2 A2 3 A3 4 A4 5 C5 6 I/O1 7 I/O2 8 I/O4 10 Vcc 11 Vss 12 I/O5 13 I/O6 14 I/O7 15 I/O8 17 A5 18 A6 19 A7 20 A8 21 A9 22	soJ	44 44 44 33 33 33 33 33 32 22 22 22 22 22	3 A16 A16 A17 A17 A17 A17 A17 A11 A11 A11 A11 A17 A17

PIN FUNCTION

Pin Name	Pin Function
A0 - A17	Address Inputs
WE	Write Enable
cs	Chip Select
ŌĒ	Output Enable
LB	Lower-byte Control(I/O1~I/O8)
UB	Upper-byte Control(I/O9~I/O16)
I/O1 ~ I/O16	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground



ABSOLUTE MAXIMUM RATINGS*

Param	eter	Symbol	Rating	Unit
Voltage on Any Pin Relati	ive to Vss	VIN, VOUT	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss		Vcc	-0.5 to 7.0	V
Power Dissipation		PD	1.0	W
Storage Temperature		Тѕтс	-65 to 150	°C
Operating Temperature	Commercial	TA	0 to 70	°C
	Extended	. TA	-25 to 85	Ĉ
	Industrial	TA	-40 to 85	°C

^{*} Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(TA = 0 to 70°C)

Parameter	Symbol	Min	Тур	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input Low Voltage	ViH	2.2	-	Vcc + 0.5**	V
Input Low Voltage	ViL	-0.5*	-	0.8	V

NOTE: Above parameters are also guaranteed at extended and industrial temperature ranges.

- * VIL(Min) = -2.0V a.c(Pulse Width≤10ns) for 1 ≤ 20mA
- ** VIH(Max) = VCC + 2.0V a.c (Pulse Width \le 10ns) for I \le 20mA

DC AND OPERATING CHARACTERISTICS(TA = 0 to 70 °C, Vcc= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	ILI	Vin = Vss to Vcc		-2	2	μA
Output Leakage Current	lLO	CS=ViH or OE=ViH or WE=ViL Vout = Vss to Vcc		-2	2	μA
Operating Current	Icc	Min. Cycle, 100% Duty	20ns	-	240	mA
		CS=VIL, VIN = VIH or VIL, IOUT=0mA	25ns	-	220	
Standby Current	ISB	Min. Cycle, CS=Vін		_	60	mA
	ISB1	f=0MHz, $\overline{CS} \ge Vcc-0.2V$, $Vin \ge Vcc-0.2V$ or $Vin \le 0.2V$		-	10	mA
Output Low Voltage Level	Vol	IoL=8mA		-	0.4	٧
Output High Voltage Level	Voн	IOH=-4mA		2.4	-	٧
	VoH1*	Iон1=-0.1mA			3.95	٧

NOTE: Above parameters are also guaranteed at extended and industrial temperature ranges.

CAPACITANCE*(TA =25°C, f=1.0MHz)

	Item	Symbol	Test Conditions	MIN	Max	Unit
ſ	Input/Output Capacitance	Ci/o	V1/0=0V	-	8	pF
Γ	Input Capacitance	Cin	VIN=0V	-	6	pF

^{*} NOTE: Capacitance is sampled and not 100% tested.



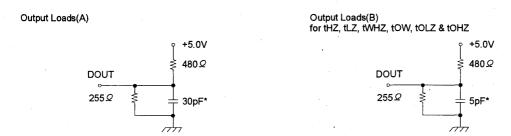
^{*} Vcc=5.0V ± 5% Temp. = 25 ℃

AC CHARACTERISTICS(TA = 0 to 70 °C, Vcc = 5.0V ± 10%, unless otherwise noted.)

TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

NOTE: Above test conditions are also applied at extended and industrial temperature ranges.



* Including Scope and Jig Capacitance

READ CYCLE

Parameter		KM61	64002-20	KM616	4002-25	11
	Symbol —	Min	Max	Min	Max	Unit
Read Cycle Time	tRC	20	-	25	-	ns
Address Access Time	tAA	-	20		25	ns
Chip Select to Output	tCO	-	20	-	25	ns
Output Enable to Valid Output	tOE	-	10	-	12	ns
UB, LB Access Time	tBA	-	10	-	12	ns
Chip Enable to Low-Z Output	tLZ	5	-	5	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	ns
UB, LB Enable to Low-Z Output	tBLZ	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	7	0	8	ns
Output Disable to High-Z Output	tOHZ	0	7	0	8	ns
UB, LB Disable to High-Z Output	tBHZ	0	7	0	8	ns
Output Hold from Address Change	tOH	4		5	-	ns

NOTE: Above parameters are also guaranteed at extended and industrial temperature ranges.



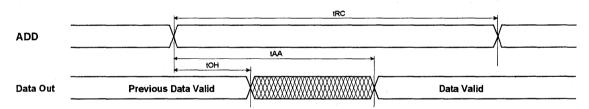
WRITE CYCLE

Parameter		KM618	KM6164002-20		4002-25	Unit
	Symbol -	Min	Max	Min	Max	Unit
Write Cycle Time	tWC	20	-	25	-	ns
Chip Select to End of Write	tCW	15	-	17	-	ns
Address Set-up Time	tAS	0	-	. 0	-	ns
Address Valid to End of Write	tAW	15	-	17	-	ns
Write Pulse Width(OE High)	tWP	15	-	17	-	ns
Write Pulse Width(OE Low)	tWP1	20	-	25		ns
UB, LB Valid to End of Write	tBW	15	-	17	-	ns
Write Recovery Time	tWR	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	8	0	8	ns
Data to Write Time Overlap	tDW	10	-	12	-	ns
Data Hold from Write Time	tDH	0	-	, 0	-	ns
End Write to Output Low-Z	tOW	3	-	4	-	ns

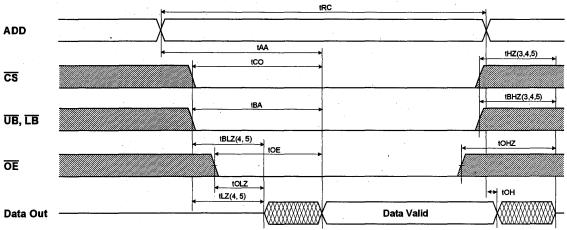
NOTE: Above parameters are also guaranteed at extended and industrial temperature ranges.

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, CS=OE=UB=LB=VIL, WE=VIH)



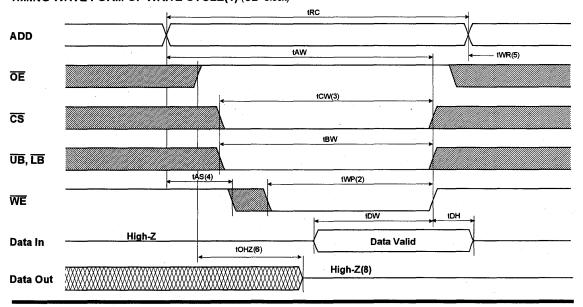
TIMING WAVE FORM OF READ CYCLE(2) (WE=VIH)



NOTES(READ CYCLE)

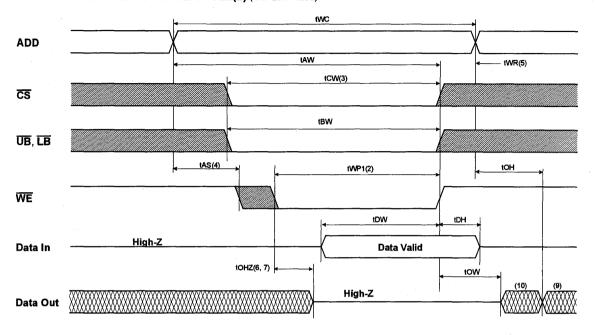
- 1. WE is high for read cycle.
- 2. All read cycle timing is referenced from the last valid address to the first transition address.
- 3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VoH or VoL Levels.
- 4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
- 5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
- 6. Device is continuously selected with CS=VIL.
- 7. Address valid prior to coincident with $\overline{\text{CS}}$ transition low.
- 8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVE FORM OF WRITE CYCLE(1) (OE=Clock)

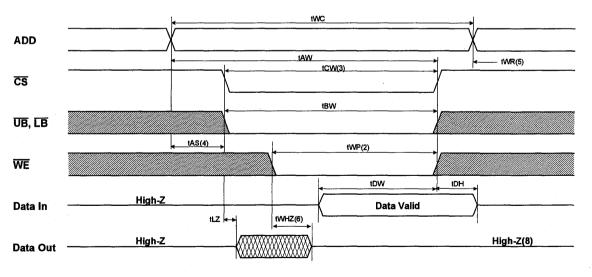




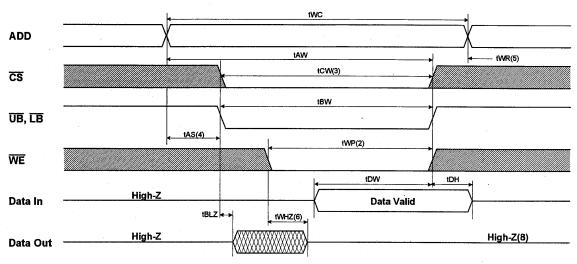
TIMING WAVE FORM OF WRITE CYCLE(2) (OE=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) (CS=Controlled)



TIMING WAVE FORM OF WRITE CYCLE(4) (UB, LB Controlled)



NOTES(WRITE CYCLE)

- 1. All write cycle timing is referenced from the last valid address to the first transition address.
- 2. A write occurs during the overlap of a low \overline{CS} , \overline{WE} , \overline{LB} and \overline{UB} . A write begins at the latest transition \overline{CS} going low and \overline{WE} going low; A write ends at the earliest transition \overline{CS} going high or \overline{WE} going high. tWP is measured from the beginning of write to the end of write.
- 3. tCW is measured from the later of $\overline{\text{CS}}$ going low to end of write.
- 4. tAS is measured from the address valid to the beginning of write.
- 5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as CS, or WE going high.
- 6. If OE. CS and WE are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
- 7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
- 8. If CS goes low simultaneously with WE going or after WE going low, the outputs remain high impedance state.
- 9. Dout is the read data of the new address.
- 10. When $\overline{\text{CS}}$ is low: I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

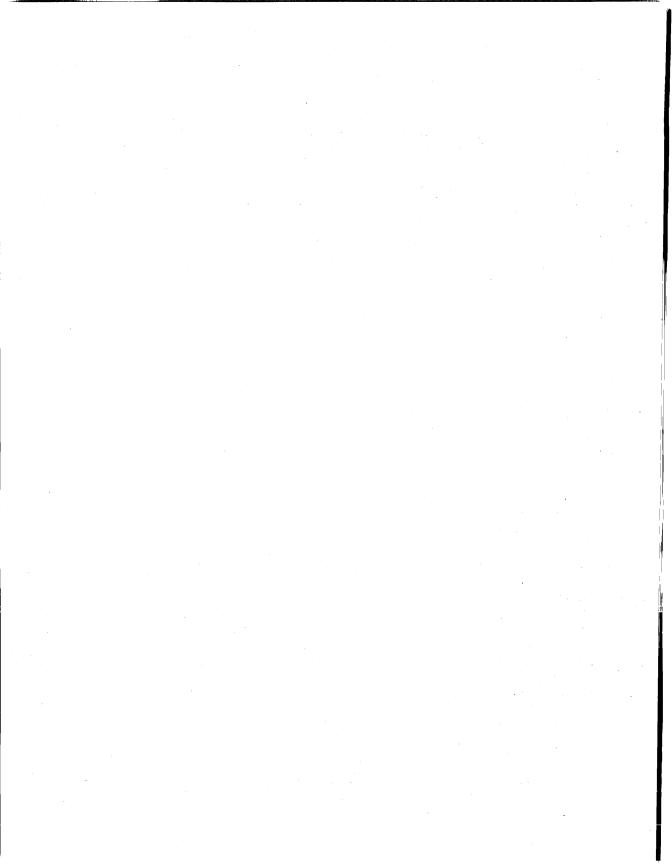
FUNCTIONAL DESCRIPTION

cs	WE	ŌĒ	ĪB	UB	Mode	1/0	I/O Pin	
-00	***	0_		OG.	Mode	1/01~1/08	1/09~1/016	Supply Current
Н	Х	Χ*	X	Х	Not Select	High-Z		ISB, ISB1
L	H '	н	Х	Х	Output Disable	utput Disable High-Z High-Z		lcc
L	Х	Х	н	Н				
L	Н	L	L	Н	Read	Dout	High-Z	lcc
			Н	L		High-Z	Dout	
			L	L		Dout	Dout	
L	L	Х	L	Н	Write	Din	High-Z	lcc
			Н	L		High-Z	DIN	•
			L	L		Din	DIN	

^{*} NOTE: X means Don't Care.



256K High Speed SRAM (3.3V Operation)



32K x 8 Bit High-Speed CMOS Static RAM (3.3V Operating)

FEATURES

- Fast Access Time 15, 17, 20 ns (Max.)
- · Low Power Dissipation

Standby (TTL) : 30mA(Max.)

(CMOS): 0.1mA(Max.)

Operating KM68V257C - 15: 90mA(Max.)

KM68V257C - 17:80mA(Max.)

KM68V257C - 20: 70mA(Max.)

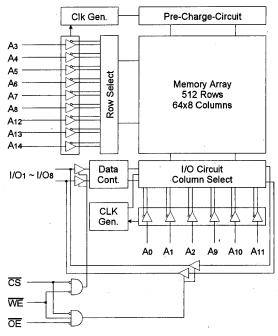
- Single 3.3V \pm 0.3V Power Supply
- . TTL Compatible Inputs and Outputs
- · Fully Static Operation
- No Clock or Refresh required
- · Three State Outputs
- Low Data Retention Voltage: 2V (min)
- · Standard Pin Configuration

KM68V257CP: 28-DIP-300

KM68V257CJ: 28-SOJ-300

KM68V257CTG: 28-TSOP1-0813, 4F

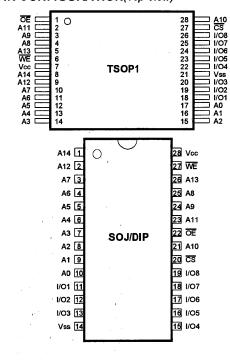
FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The KM68V257C is a 262,144-bit high-speed Static Random Access Memory organized as 32,768 words by 8 bits. The KM68V257C uses 8 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM68V257C is packaged in a 300 mil 28-pin plastic DIP, SOJ or TSOP1 forward.

PIN CONFIGURATION(Top View)



PIN FUNCTION

Pin Name	Pin Function				
A0 - A14	Address Inputs				
WE	Write Enable				
CS	Chip Select				
ŌĒ .	Output Enable				
I/O1 ~ I/O8	Data Inputs/Outputs				
Vcc	Power(+3.3V)				
Vss	Ground				

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	VIN, VOUT	-0.5 to 4.6	. V
Voltage on Vcc Supply Relative to Vss	Vcc	-0.5 to 5.5	V
Power Dissipation	Po	1.0	W
Storage Temperature	Тѕтс	-65 to 150	Ĉ
Operating Temperature	TA	0 to 70	င

^{*} Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(TA = 0 to 70°C)

Parameter	Symbol	Min	Тур	Max	Unit
Supply Voltage	Vcc	3.0	3.3	3.6	V
Ground	Vss	0	0	0	٧
Input Low Voltage	ViH	2.2	-	Vcc + 0.3**	٧
Input Low Voltage	VIL	-0.3*	-	0.8	٧.

^{*} VIL(Min) = -2.0(Pulse Width≤12ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS(TA = 0 to 70 °C, Vcc= 3.3V ± 0.3V, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	Iu	VIN = Vss to Vcc		-2	2	μA
Output Leakage Current	lLO	CS=VIH or OE=VIH or WE=VIL VOUT = Vss to Vcc		-2	2	μA
Operating Current	Icc	Min. Cycle, 100% Duty	15ns	-	90	mA
		CS=VIL, VIN = VIH or VIL,	17ns	-	80	1
		IOUT=0mA	20ns	-	70	1
Standby Current	IsB	Min. Cycle, CS=Viн		-	30	mA
	ISB1	f=0MHz, $\overline{CS} \ge Vcc$ -0.2V, Vin $\ge Vcc$ -0.2V or Vin $\le 0.2V$		-	0.1	mA
Output Low Voltage Level	VoL	IOL=8mA		-	0.4	٧
Output High Voltage Level	Von '	IOH=-4mA		2.4	-	٧

CAPACITANCE*(TA =25°C, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit .
Input/Output Capacitance	CI/O	V1/0=0V	-	8	pF
Input Capacitance	CIN	Vin=0V	-	7	pF

^{*} NOTE: Capacitance is sampled and not 100% tested.



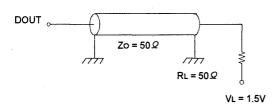
^{**} VIH(Max) = Vcc + 2.0V(Pulse Width \le 12ns) for I \le 20mA

AC CHARACTERISTICS(TA = 0 $^{\circ}$ C to 70 $^{\circ}$ C, Vcc = 3.3V $^{\pm}$ 0.3V, unless otherwise noted.)

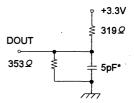
TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below





Output Loads(B) for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



READ CYCLE

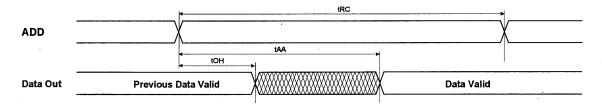
Parameter	O	KM68V	257C-15	257C-15 KM68V257C-17		KM68V257C-20		l
	Symbol	Min	Max	Min	Max	Min	Max	Unit
Read Cycle Time	tRC	15	-	17	-	20		ns
Address Access Time	tAA	-	15	-	17	-	20	ns
Chip Select to Output	tCO	-	15	-	17	-	20	ns
Output Enable to Valid Output	tOE	-	7	-	· 8	-	10	ns
Chip Enable to Low-Z Output Access Time	tLZ	3	-	3	-	. 3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	7	0	8	0	10	ns
Output Disable to High-Z Output	tOHZ	0	7	0	8	0	10	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	0	-	ns
Chip Selection to Power DownTime	tPD	-	15	-	17	-	20	ns

WRITE CYCLE

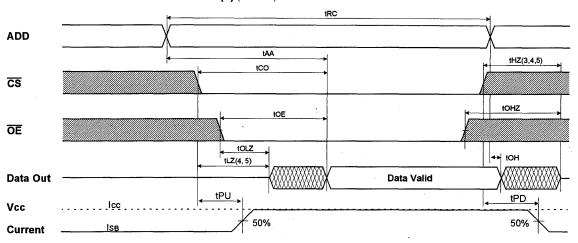
B	Sumb at	KM68V	257C-15	KM68V	257C-17	KM68V	257C-20	11-14
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit
Write Cycle Time	tWC	15	-	- 17	_	20	- :	ns
Chip Select to End of Write	tCW	, 11	-	12	-	13	-	ns
Address Setup Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	11	-	12	-	13		ns
Write Pulse Width(OE High)	tWP	11	-	12	-	13	-	ns
Write Pulse Width(OE Low)	tWP1	15	-	17	-	20	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	6	0	6	0	8	ns
Data to Write Time Overlap	tDW	8	-	8	-	10	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	0	-	0	-	0	-	ns

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{\text{CS}} = \overline{\text{OE}} = \text{VIL}$, $\overline{\text{WE}} = \text{VIH}$)



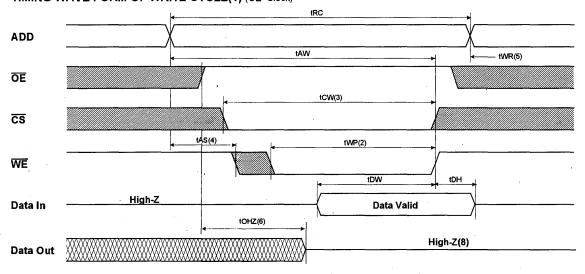
TIMING WAVE FORM OF READ CYCLE(2) (WE=VIH)



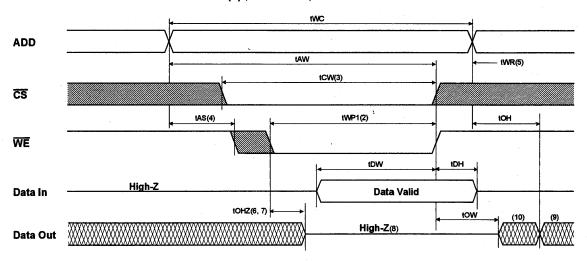
NOTES(READ CYCLE)

- 1. WE is high for read cycle.
- 2. All read cycle timing is referenced from the last valid address to the first transition address.
- 3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VoH or VoL Levels.
- 4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
- 5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
- 6. Device is continuously selected with CS=VIL.
- 7. Address valid prior to coincident with \overline{CS} transition low.
- 8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

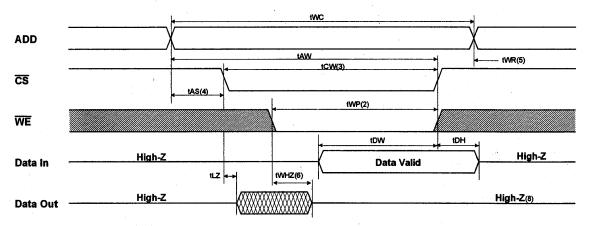
TIMING WAVE FORM OF WRITE CYCLE(1) (OE=Clock)



TIMING WAVE FORM OF WRITE CYCLE(2) (OE=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) (CS=Controlled)



NOTES(WRITE CYCLE)

- 1. All write cycle timing is referenced from the last valid address to the first transition address.
- 2. A write occurs during the overlap of a low CS and WE. A write begins at the latest transition CS going low and WE going low; A write ends at the earliest transition \overline{CS} going high or \overline{WE} going high. tWP is measured from the beginning of write to the end of write.

 3. tCW is measured from the later of \overline{CS} going low to end of write.
- 4. tAS is measured from the address valid to the beginning of write.
- 5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as CS or WE going high.
- 6. If OE, CS and WE are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
- 7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
- 8. If CS goes low simultaneously with WE going or after WE going low, the outputs remain high impedance state.
- 9. Dout is the read data of the new address.
- 10. When CS is low: I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

<u>cs</u>	WE	ŌĒ	Mode	I/O Pin	Supply Current
Н	Х	X*	Not Select	High-Z	ISB, ISB1
L	Н	Н	Output Disable	High-Z	lcc
L	, н	L	Read	Dоит	lcc
L	L	x	Write	Din	lcc

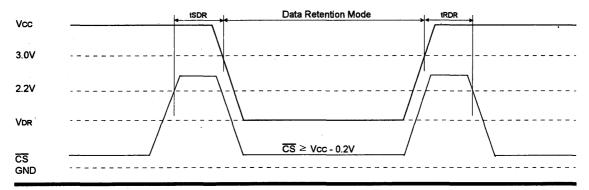
^{*} NOTE: X means Don't Care.

DATA RETENTION CHARACTERISTICS*(TA = 0° to 70°)

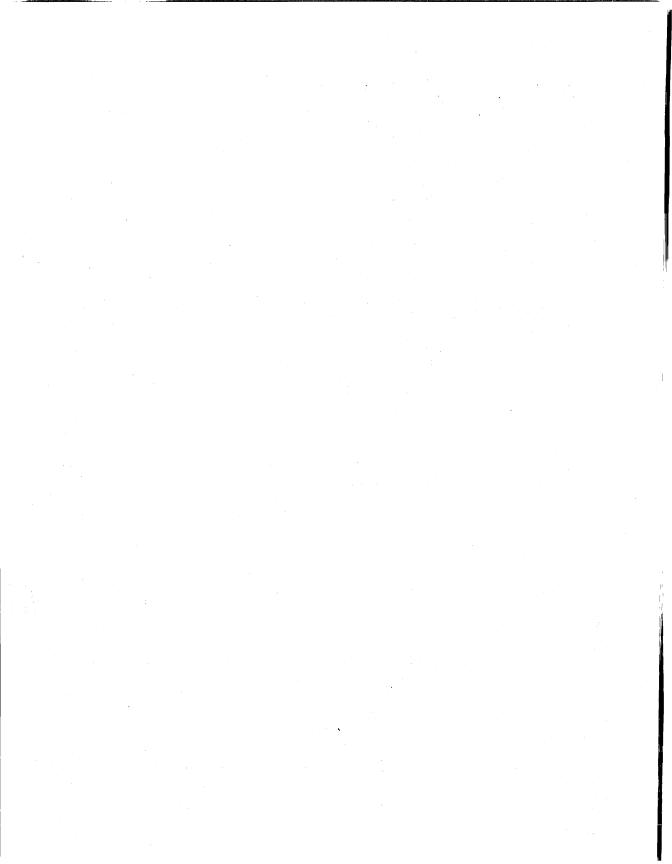
Parameter	Symbol	Test Condition	Min.	Тур.	Max.	Unit
Vcc for Data Retention	VDR	<u>CS</u> ≥ Vcc - 0.2V	2.0	-	3.6	٧
Data Retention Current	IDR	$\begin{aligned} &\text{Vcc} = 2.0\text{V}, \overline{\text{CS}} \ge \text{Vcc} - 0.2\text{V} \\ &\text{Vin} \ge \text{Vcc} - 0.2\text{V} \text{ or Vin} \le 0.2\text{V} \end{aligned}$	-	-	0.07	mA
Data Retention Set-Up Time	tSDR	See Data Retention	0		_	ns
Recovery Time	tRDR	Wave form(below)	5	-	-	ms

^{*} L-Ver only.

DATA RETENTION WAVE FORM(CS Controlled)







256K x 4 Bit (with \overline{OE})High-Speed CMOS Static RAM(3.3V Operating)

FEATURES

- Fast Access Time 8,10,12ns (Max.)
- · Low Power Dissipation

Standby (TTL) : 30mA(Max.)

(CMOS): 5mA(Max.)

0.5mA(Max.) - L-Ver. only

Operating KM64V1003B/BL - 8: 150mA(Max.)

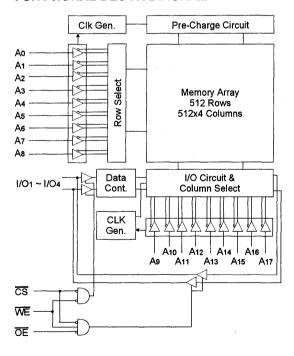
KM64V1003B/BL - 10: 140mA(Max.)

KM64V1003B/BL - 12: 130mA(Max.)

- Single 3.3V ±0.3V Power Supply
- . TTL Compatible Inputs and Outputs
- . Fully Static Operation
- No Clock or Refresh required
- · Three State Outputs
- · 2V Minimum Data Retention; L-Ver. only
- · Center Power/Ground Pin Configuration
- . Standard Pin Configuration

KM64V1003B/BLJ: 32-SOJ-400 KM64V1003B/BLT: 32-TSOP2-400F

FUNCTIONAL BLOCK DIAGRAM



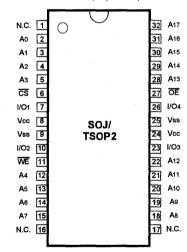
GENERAL DESCRIPTION

The KM64V1003B/BL is a 1,048,576-bit high-speed Static Random Access Memory organized as 262,144 words by 4 bits. The KM64V1003B/BL uses 4 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM64V1003B/BL is packaged in a 400 mil 32-pin plastic SOJ or TSOP2 forward.

ORDERING INFORMATION

KM64V1003B/BL -8/10/12	Commercial Temp.
KM64V1003BI/BLI -8/10/12	Industrial Temp.

PIN CONFIGURATION(Top View)



PIN FUNCTION

Pin Name	Pin Function
A0 - A17	Address Inputs
WE	Write Enable
CS	Chip Select
ŌĒ	Output Enable
I/O1 ~ I/O4	Data Inputs/Outputs
Vcc	Power(+3.3V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS*

Paramo	eter	Symbol	Rating	Unit
Voltage on Any Pin Relati	ve to Vss	Vin, Vout	-0.5 to 4.6	V
Voltage on Vcc Supply Re	elative to Vss	Vcc	-0.5 to 5.5	V
Power Dissipation		PD	1.0	W
Storage Temperature		Тѕтс	-65 to 150	°C
Operating Temperature	Commercial	TA TA	0 to 70	°C
	Industrial	TA	-40 to 85	°C

^{*} Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(TA = 0 to 70°)

Parameter	Symbol	Min	Тур	WAX	Unit
Supply Voltage	Vcc	3.0	3.3	3.6	V
Ground	Vss	0	0	0	V
Input Low Voltage	ViH	2.0	-	Vcc + 0.3**	V
Input Low Voltage	ViL	-0.3*	-	0.8	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

DC AND OPERATING CHARACTERISTICS(TA = 0 to 70 °C, Vcc= 3.3V ± 0.3V, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	ILI	Vin = Vss to Vcc		-2	2	μA
Output Leakage Current	lLO	CS=VIH or OE=VIH or WE=VIL VOUT = Vss to Vcc		-2	2	μA
Operating Current	lcc	Min. Cycle, 100% Duty	8ns	-	150	mA
		CS=VIL, VIN = VIH or VIL,	10ns	-	140	1
		IOUT=0mA	12ns	-	130	1.
Standby Current	ISB	Min. Cycle, CS=Vін		-	30	mA
	ISB1	f=0MHz, CS ≥ Vcc-0.2V,	Normal	-	5	mA
		$Vin \ge Vcc-0.2V$ or $Vin \le 0.2V$	L-Ver.	-	0.5	1
Output Low Voltage Level	Vol	IoL=8mA	1	•	0.4	٧
Output High Voltage Level	Vон	IOH=-4mA		2.4	-	٧

NOTE: Above parameters are also guaranteed at industrial temperature range.

CAPACITANCE*(TA =25°C, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	CI/O	VI/0=0V	-	8	pF
Input Capacitance	Cin	Vin=0V	-	6	pF

^{*} NOTE: Capacitance is sampled and not 100% tested.



^{*} VIL(Min) = -2.0V a.c(Pulse Width≤6ns) for 1 ≤ 20mA

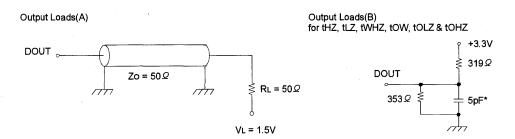
^{**} VIH(Max) = Vcc + 2.0V a.c (Pulse Width ≤ 6ns) for I ≤ 20mA

AC CHARACTERISTICS(TA = 0 to 70 °C, Vcc = 3.3V ± 0.3V, unless otherwise noted.)

TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3 ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

NOTE: Above test conditions are also applied at industrial temperature range.



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM64V1003B/BL-8		KM64V1003B/BL-10		KM64V1003B/BL-12		Unit
		Min	Max	Min	Max	Min	Max	- Unit
Read Cycle Time	tRC	8	-	10	-	12	-	ns
Address Access Time	tAA	-	8	-	10	-	12	ns
Chip Select to Output	tCO	-	8	-	10	-	12	ns
Output Enable to Valid Output	tOE	-	4	-	5	-	6	ns
Chip Enable to Low-Z Output	tLZ	3	_	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	4	0	5	0	6	ns
Output Disable to High-Z Output	tOHZ	0	4	0	5	0	6	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	0	-	ns
Chip Selection to Power DownTime	tPD	-	8	-	10	-	12	ns

NOTE: Above parameters are also guaranteed at industrial temperature range.

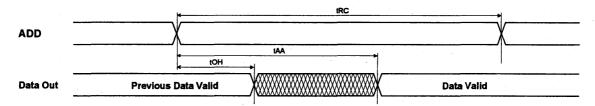
WRITE CYCLE

Parameter	Symbol	KM64V1003B/BL-6		KM64V1003B/BL-10		KM64V1003B/BL-12		
		Min	Max	Min	Max	Min	Max	Unit
Write Cycle Time	tWC	8	-	10	-	12	-	ns
Chip Select to End of Write	tCW	6	-	7	-	8	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	6	-	7	-	8	-	ns
Write Pulse Width(OE High)	tWP	6	-	7	-	8	-	ns
Write Pulse Width(OE Low)	tWP1	. 8	-	10	-	12	-	ns
Write Recovery Time	tWR	0	-	0	-	0		ns
Write to Output High-Z	tWHZ	0	4	0	5	0	6	ns
Data to Write Time Overlap	tDW	4	-	5	-	6	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

NOTE: Above parameters are also guaranteed at industrial temperature range.

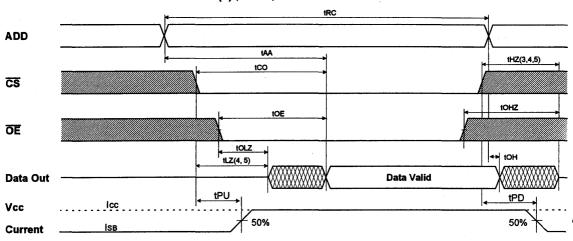
TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, CS=OE=VIL, WE=VIH)





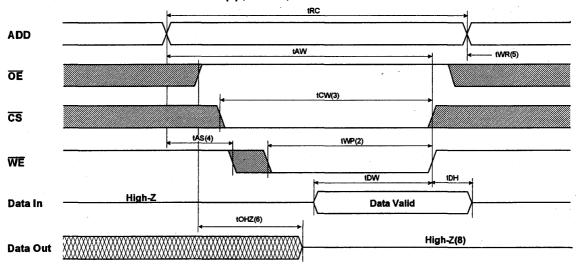
TIMING WAVE FORM OF READ CYCLE(2) (WE=VIH)



NOTES(READ CYCLE)

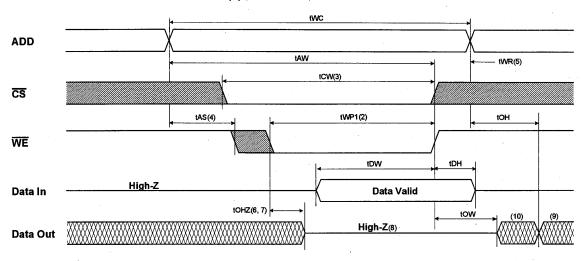
- 1. WE is high for read cycle.
- 2. All read cycle timing is referenced from the last valid address to the first transition address.
- 3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL Levels.
- 4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
- 5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
- 6. Device is continuously selected with CS=VIL.
- 7. Address valid prior to coincident with CS transition low.
- 8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVE FORM OF WRITE CYCLE(1) (OE=Clock)

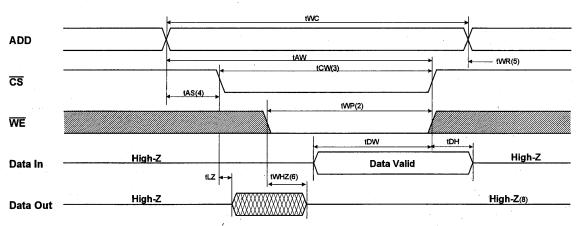




TIMING WAVE FORM OF WRITE CYCLE(2) (OE=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) (CS=Controlled)



NOTES(WRITE CYCLE)

- 1. All write cycle timing is referenced from the last valid address to the first transition address.
- 2. A write occurs during the overlap of a low CS and WE. A write begins at the latest transition CS going low and WE going low; A write ends at the earliest transition \overline{CS} going high or \overline{WE} going high. tWP is measured from the beginning of write to the end of write.

 3. tCW is measured from the later of \overline{CS} going low to end of write.
- 4. tAS is measured from the address valid to the beginning of write.
- 5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as CS or WE going high.
- 6. If OE, CS and WE are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
- 7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
- 8. If CS goes low simultaneously with WE going or after WE going low, the outputs remain high impedance state.
- 9. Dout is the read data of the new address.
- 10. When CS is low: I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

CS	WE	ŌĒ	Mode	I/O Pin	Supply Current
Н	X	X*	Not Select	High-Z	ISB, ISB1
L	Н	H	Output Disable	. High-Z	lcc
L	H	L	Read	Dout	Icc
L	L	Х	Write	Din	lcc

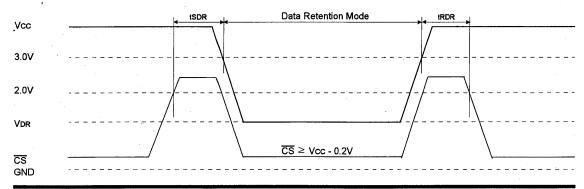
^{*} NOTE: X means Don't Care.

DATA RETENTION CHARACTERISTICS*(TA = 0° to 70°)

Parameter	Symbol	Symbol Test Condition		Тур.	Max.	Unit	
Vcc for Data Retention	VDR	CS ≥ Vcc - 0.2V	2.0	-	3.6	V	
Data Retention Current	IDR	$Vcc = 3.0V, \overline{CS} \ge Vcc - 0.2V$ $Vin \ge Vcc - 0.2V \text{ or } Vin \le 0.2V$	•	-	0.4	mA	
		$Vcc = 2.0V, \overline{CS} \ge Vcc - 0.2V$ $Vin \ge Vcc - 0.2V$ or $Vin \le 0.2V$	-	, -	0.3		
Data Retention Set-Up Time	tSDR	See Data Retention	0	-	-	ns	
Recovery Time	tRDR	Wave form(below)	5	-	-	ms	

NOTE: Above parameters are also guaranteed at industrial temperature range.

DATA RETENTION WAVE FORM(CS Controlled)



^{*} L-Ver only.

256K x 4 Bit(with OE) High-Speed CMOS Static RAM(3.3V Operating)

FEATURES

- Fast Access Time 12, 15, 17, 20 ns (Max.)
- · Low Power Dissipation

Standby (TTL) : 20mA(Max.)

(CMOS): 5mA(Max.)

0.5mA(Max.); L-ver. only

Operating KM64V1003A/AL - 12: 130mA(Max.)

KM64V1003A/AL - 15: 125mA(Max.) KM64V1003A/AL - 17: 125mA(Max.)

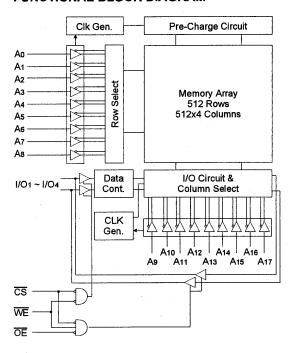
KM64V1003A/AL - 20: 120mA(Max.)

- Single 3.3V±0.3V Power Supply
- . TTL Compatible Inputs and Outputs
- · Fully Static Operation
 - No Clock or Refresh required
- Three State Outputs
- . 2V Minimum Data Retention; L-Ver. only
- · Center Power/Ground Pin Configuration
- Standard Pin Configuration

KM64V1003A/ALJ: 32-SOJ-400

KM64V1003A/ALT: 32-TSOP2-400F

FUNCTIONAL BLOCK DIAGRAM



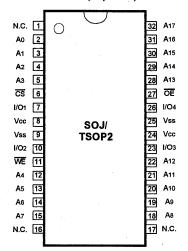
GENERAL DESCRIPTION

The KM64V1003A/AL is a 1,048,576-bit high-speed Static Random Access Memory organized as 262,144 words by 4 bits. The KM64V1003A/AL uses 4 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM64V1003A/AL is packaged in a 400 mil 32-pin plastic SOJ or TSOP2 forward.

ORDERING INFORMATION

KM64V1003A/AL -12/15/17/20	Commercial Temp.
KM64V1003AI/ALI -12/15/17/20	Industrial Temp.

PIN CONFIGURATION(Top View)



PIN FUNCTION

Pin Name	Pin Function					
A0 - A17	Address Inputs					
WE	Write Enable					
<u>cs</u>	Chip Select					
ŌĒ	Output Enable					
I/O1 ~ I/O4	Data Inputs/Outputs					
Vcc	Power(+3.3V)					
Vss	Ground					
N.C	No Connection					



ABSOLUTE MAXIMUM RATINGS*

Param	eter	Symbol	Rating	Unit
Voltage on Any Pin Relati	ve to Vss	VIN, VOUT	VIN, VOUT -0.5 to 4.6	
Voltage on Vcc Supply R	elative to Vss	Vcc -0.5 to 5.5		V
Power Dissipation		Po	1.0	W
Storage Temperature		Тѕтс	-65 to 150	°C
Operating Temperature	Commercial	TA	0 to 70	°C
	Industrial	TA	-40 to 85	°C

^{*} Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(TA = 0 to 70°C)

Parameter	Symbol	Min	Тур	Max	Unit
Supply Voltage	Vcc	3.0	3.3	3.6	٧
Ground	Vss	0	0	0	V
Input Low Voltage	ViH	2.2	-	Vcc + 0.3**	V
Input Low Voltage	VIL	-0.3*	-	0.8	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

- * VIL(Min) = -2.0V a.c(Pulse Width≤10ns) for I ≤ 20mA
- ** ViH(Max) = Vcc + 2.0V a.c (Pulse Width≤10ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS(TA = 0 to 70 °C, Vcc= 3.3V ± 0.3V, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Max	Unit	
Input Leakage Current	lLi	Vin = Vss to Vcc		-2	2	μA
Output Leakage Current	lLO	CS=VIH or OE=VIH or WE=VIL VOUT = Vss to Vcc	-2	2	μA	
Operating Current	Icc	Min. Cycle, 100% Duty	12ns	-	130	mA
		CS=VIL, VIN = VIH or VIL, IOUT=0mA	15ns	-	125	
	į		17ns	-	125	
			20ns	-	120	
Standby Current	ISB	Min. Cycle, CS=Viн	1	-	20	mA
	ISB1	f=0MHz, CS ≥ Vcc-0.2V,	Normal	-	5	mΑ
		$VIN \ge VCC-0.2V$ or $VIN \le 0.2V$	L-Ver.	•	0.5	
Output Low Voltage Level	Vol	IoL=8mA		•	0.4	V
Output High Voltage Level	Voh	IOH=-4mA		2.4	-	V
					l	L

NOTE: Above parameters are also guaranteed at industrial temperature range.

CAPACITANCE*(TA =25 °C, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	CI/O	V1/0=0V	-	8	pF
Input Capacitance	CIN	VIN=0V	-	6	pF

^{*} NOTE: Capacitance is sampled and not 100% tested.

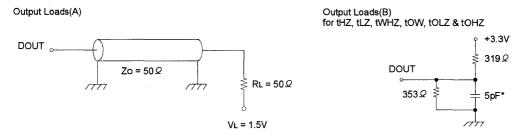


AC CHARACTERISTICS(TA = 0 to 70 $^{\circ}\text{C}$, Vcc = 3.3V \pm 0.3V, unless otherwise noted.)

TEST CONDITIONS

Parameter	Value
Input Pulse Levels	OV to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

NOTE: Above test conditions are also applied at industrial temperature range.



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM64V1003A/ AL-12		KM64V1003A/ AL-15		KM64V1003A/ AL-17		KM64V1003A/ AL-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	1
Read Cycle Time	tRC	12	-	15	-	17	-	20	-	ns
Address Access Time	tAA	-	12	-	15	-	17	-	20	ns
Chip Select to Output	tCO	-	12	-	15	-	17	-	20	ns
Output Enable to Valid Output	tOE	-	6	-	7	-	8	-	9	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	6	0	7	0	8	0	9	ns
Output Disable to High-Z Output	tOHZ	0	6	0	7	0	8	0	9	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	0	-	0	-	ns
Chip Selection to Power DownTime	tPD	-	12	-	15	_	17	-	20	ns

NOTE: Above parameters are also guaranteed at industrial temperature range.

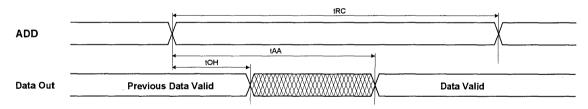
WRITE CYCLE

Parameter	Symbol	KM64V1003A/ AL-12		KM64V1003A/ AL-15		KM64V1003A/ AL-17		KM64V1003A/ AL-20		Unit
		Min	Max	Mín	Max	Min	Max	Min	Max	1
Write Cycle Time	tWC	12	-	15	-	17	-	20	-	ns
Chip Select to End of Write	tCW	8	-	10	-	11	-	12	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	8	-	10	-	11	-	12	-	ns
Write Pulse Width(OE High)	tWP	8	-	10	-	11	-	12	-	ns
Write Pulse Width(OE Low)	tWP1	12	-	15	-	17	-	- 20	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	6	0	7	0	8	0	9	ns
Data to Write Time Overlap	tDW	6	-	7	-	8	-	9	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	3	-	ns

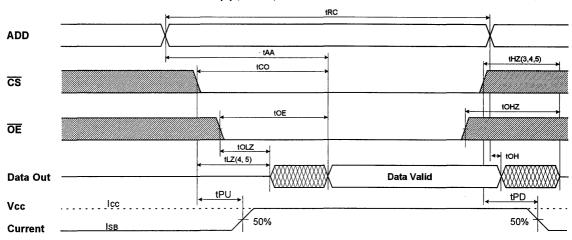
NOTE: Above parameters are also guaranteed at industrial temperature range.

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, CS=OE=VIL, WE=VIH)



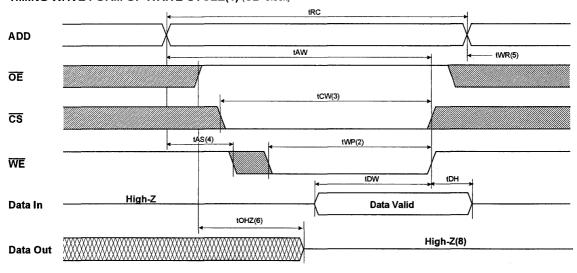
TIMING WAVE FORM OF READ CYCLE(2) (WE=VIH)



NOTES(READ CYCLE)

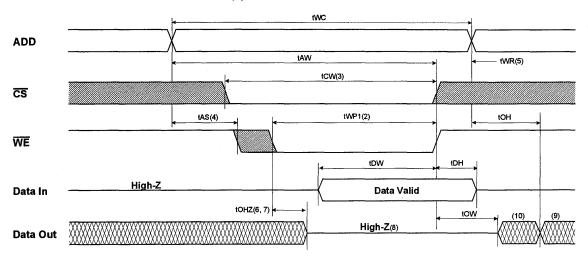
- 1. WE is high for read cycle.
- 2. All read cycle timing is referenced from the last valid address to the first transition address.
- 3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VoH or VoL Levels.
- 4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
- 5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
- 6. Device is continuously selected with CS=VIL.
- 7. Address valid prior to coincident with CS transition low.
- 8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVE FORM OF WRITE CYCLE(1) (OE=Clock)

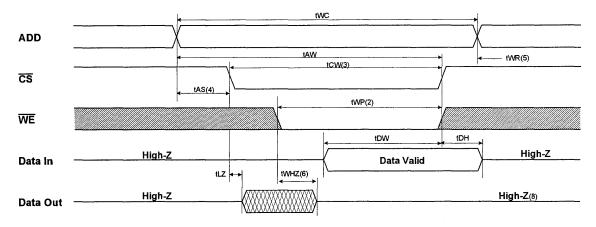




TIMING WAVE FORM OF WRITE CYCLE(2) (OE=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) (CS=Controlled)



NOTES(WRITE CYCLE)

- 1. All write cycle timing is referenced from the last valid address to the first transition address.
- 2. A write occurs during the overlap of a low \overline{CS} and \overline{WE} . A write begins at the latest transition \overline{CS} going low and \overline{WE} going low; A write ends at the earliest transition \overline{CS} going high or \overline{WE} going high. tWP is measured from the beginning of write to the end of write.
- 3. tCW is measured from the later of \overline{CS} going low to end of write.
- 4. tAS is measured from the address valid to the beginning of write.
- 5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as CS or WE going high.
- 6. If $\overline{\text{OE}}$, $\overline{\text{CS}}$ and $\overline{\text{WE}}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
- 7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
- 8. If CS goes low simultaneously with WE going or after WE going low, the outputs remain high impedance state.
- 9. Dout is the read data of the new address.
- 10. When \overline{CS} is low: I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

<u>cs</u>	WE	ŌĒ	Mode	I/O Pin	Supply Current
Н	Х	X*	Not Select	High-Z	ISB, ISB1
L	Н	Н	Output Disable	High-Z	· lcc
L	Н	L	Read	Dout	lcc
L	L	Х	Write	Din	lcc

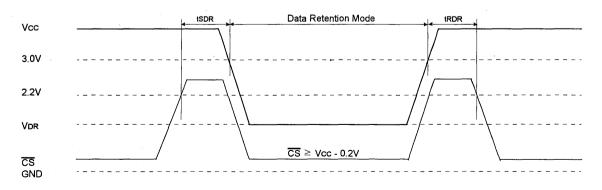
^{*} NOTE : X means Don't Care.

DATA RETENTION CHARACTERISTICS*(TA = 0° to 70°)

Parameter	Symbol	Test Condition	Min.	Тур.	Max.	Unit
Vcc for Data Retention	VDR	CS ≥ Vcc - 0.2V	2.0	-	3.6	V
Data Retention Current	IDR	$Vcc = 2.0V, \overline{CS} \ge Vcc - 0.2V$ $Vin \ge Vcc - 0.2V \text{ or } Vin \le 0.2V$	-	-	0.5	mA
Data Retention Set-Up Time	tSDR	See Data Retention	0	-	-	ns
Recovery Time	tRDR	Wave form(below)	5	-	-	ms

NOTE: Above parameters are also guaranteed at industrial temperature range.

DATA RETENTION WAVE FORM(CS Controlled)





^{*} L-Ver only.

128K x 8 Bit High-Speed CMOS Static RAM(3.3V Operating)

FEATURES

• Fast Access Time 8,10,12ns (Max.)

· Low Power Dissipation

Standby (TTL) : 30mA(Max.)

(CMOS): 5mA(Max.)

0.5mA(Max.) - L-Ver. only

Operating KM68V1002B/BL - 8 : 160mA(Max.)

KM68V1002B/BL - 10: 150mA(Max.)

KM68V1002B/BL - 12: 140mA(Max.)

• Single 3.3V ±0.3V Power Supply

. TTL Compatible Inputs and Outputs

· Fully Static Operation

- No Clock or Refresh required

. Three State Outputs

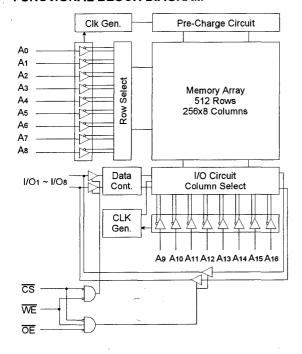
. 2V Minimum Data Retention; L-Ver. only

· Center Power/Ground Pin Configuration

· Standard Pin Configuration

KM68V1002B/BLJ: 32-SOJ-400 KM68V1002B/BLSJ: 32-SOJ-300 KM68V1002B/BLT: 32-TSOP2-400F

FUNCTIONAL BLOCK DIAGRAM



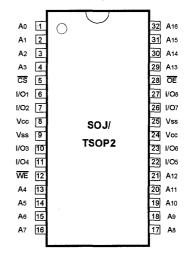
GENERAL DESCRIPTION

The KM68V1002B/BL is a 1,048,576-bit high-speed Static Random Access Memory organized as 131,072 words by 8 bits. The KM68V1002B/BL uses 8 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM68V1002B/BL is packaged in a 400/300 mil 32-pin plastic SOJ or TSOP2 forward.

ORDERING INFORMATION

KM68V1002B/BL -8/10/12	Commercial Temp.
KM68V1002BI/BLI -8/10/12	Industrial Temp.

PIN CONFIGURATION(Top View)



PIN FUNCTION

Pin Name	Pin Function
A0 - A16	Address Inputs
WE	Write Enable
<u>CS</u>	Chip Select
ŌĒ	Output Enable
I/O1 ~ I/O8	Data Inputs/Outputs
Vcc	Power(+3.3V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS*

Param	eter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss		VIN, VOUT	-0.5 to 4.6	V
Voltage on Vcc Supply Relative to Vss		Vcc -0.5 to 5.5		V
Power Dissipation		PD	1.0	W
Storage Temperature		Тѕтс	-65 to 150	°C
Operating Temperature	Commercial	TA	0 to 70	°
	Industrial	TA	-40 to 85	°C

^{*} Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(TA = 0 to 70°C)

Parameter	Symbol	Min	Тур	Max	Unit
Supply Voltage	Vcc	3.0	3.3	3.6	V
Ground	Vss	0	0	0	٧
Input Low Voltage	VIH	2.0	-	Vcc + 0.3**	V
Input Low Voltage	VIL	-0.3*	-	0.8	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

DC AND OPERATING CHARACTERISTICS(TA = 0 to 70 °C, Vcc= 3.3V ± 0.3V, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	İLI	Vin = Vss to Vcc		-2	2	μA
Output Leakage Current	lLO	CS=VIH or OE=VIH or WE=VIL VOUT = Vss to Vcc	-2	2	μA	
Operating Current	Icc	Min. Cycle, 100% Duty	8ns		160	mΑ
		CS=VIL, VIN = VIH or VIL,	10ns	-	150	
		IOUT=0mA 12n		-	140]
Standby Current	IsB	Min. Cycle, СS=Vін		-	30	mA
	ISB1	f=0MHz, CS ≥ Vcc-0.2V,	Normal	-	5	mA
		$Vin \ge Vcc-0.2V \text{ or } Vin \le 0.2V$	L-Ver.	-	0.5	
Output Low Voltage Level	Vol	IoL=8mA		-	0.4	V
Output High Voltage Level	Voн	IOH=-4mA		2.4	-	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

CAPACITANCE*(TA =25°C, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	CI/O	VI/0=0V	-	8	pF
Input Capacitance	Cin	VIN=0V	-	6	pF

^{*} NOTE: Capacitance is sampled and not 100% tested.



^{*} VIL(Min) = -2.0V a.c(Pulse Width≤6ns) for I ≤ 20mA

^{**} VIH(Max) = Vcc + 2.0V a.c (Pulse Width ≤ 6ns) for I ≤ 20mA

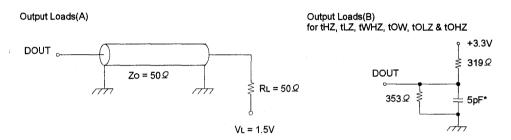
KM68V1002B/BL, KM68V1002BI/BLI

AC CHARACTERISTICS(TA = 0 to 70°, Vcc = 3.3V ± 0.3V, unless otherwise noted.)

TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

NOTE: Above test conditions are also applied at industrial temperature range.



^{*} Including Scope and Jig Capacitance

READ CYCLE

Parameter		KM68V1002B/BL-8		KM68V1002B/BL-10		KM68V1002B/BL-12		
	Symbol	Min	Max	Min	Max	Min	Max	Unit
Read Cycle Time	tRC	8	-	10	•	12	-	ns
Address Access Time	tAA	-	8	-	10	-	12	ns
Chip Select to Output	tCO	-	8	-	10	-	12	ns
Output Enable to Valid Output	tOE	•	4	-	5	-	6	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	4	0	5	0	6	ns
Output Disable to High-Z Output	tOHZ	0	4	0	5	0	6	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	0	-	ns
Chip Selection to Power DownTime	tPD	-	8	-	10	-	12	ns

NOTE: Above parameters are also guaranteed at industrial temperature range.

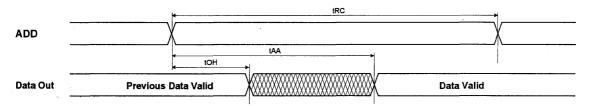
WRITE CYCLE

Parameter	0	KM68V1002B/BL-8		KM68V1002B/BL-10		KM68V1002B/BL-12		
	Symbol	Min	Max	Min	Max	Min	Max	Unit
Write Cycle Time	tWC	8	-	10	-	12	-	ns
Chip Select to End of Write	tCW	6	-	7	-	8	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	6	-	7	-	8	-	ns
Write Pulse Width(OE High)	tWP	6	-	7	-	8	-	ns
Write Pulse Width(OE Low)	tWP1	8	-	10	-	12	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	4	0	5	0	6	ns
Data to Write Time Overlap	tDW	4	-	5	-	6	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

NOTE: Above parameters are also guaranteed at industrial temperature range.

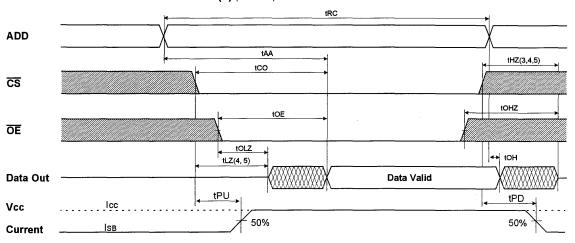
TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, CS=OE=VIL, WE=VIH)





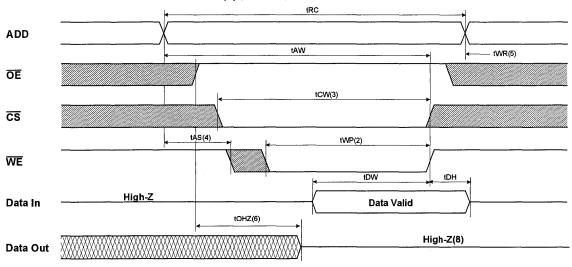
TIMING WAVE FORM OF READ CYCLE(2) (WE=VIH)



NOTES(READ CYCLE)

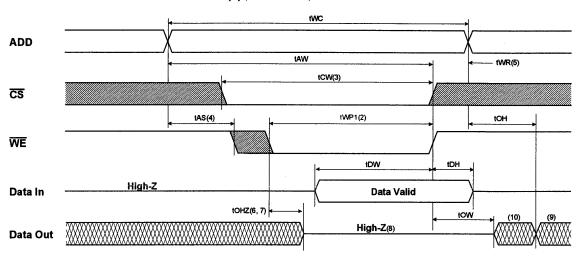
- 1. WE is high for read cycle.
- 2. All read cycle timing is referenced from the last valid address to the first transition address.
- 3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VoH or VoL Levels.
- 4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
- 5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
- 6. Device is continuously selected with CS=VIL.
- 7. Address valid prior to coincident with CS transition low.
- 8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVE FORM OF WRITE CYCLE(1) (OE=Clock)

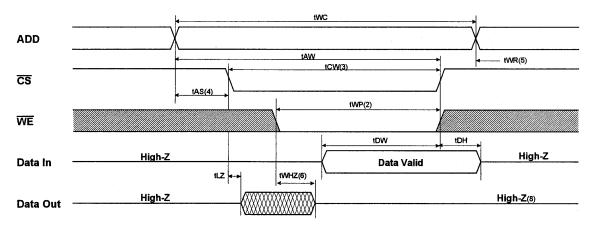




TIMING WAVE FORM OF WRITE CYCLE(2) (OE=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) (CS=Controlled)





NOTES(WRITE CYCLE)

- 1. All write cycle timing is referenced from the last valid address to the first transition address.
- 2. A write occurs during the overlap of a low \overline{CS} and \overline{WE} . A write begins at the latest transition \overline{CS} going low and \overline{WE} going low; A write ends at the earliest transition \overline{CS} going high or \overline{WE} going high. tWP is measured from the beginning of write to the end of write.
- 3. tCW is measured from the later of CS going low to end of write.
- 4. tAS is measured from the address valid to the beginning of write.
- 5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as CS or WE going high.
- 6. If \overline{OE} , \overline{CS} and \overline{WE} are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
- 7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
- 8. If $\overline{\text{CS}}$ goes low simultaneously with $\overline{\text{WE}}$ going or after $\overline{\text{WE}}$ going low, the outputs remain high impedance state.
- 9. Dout is the read data of the new address.
- 10. When \overline{CS} is low: I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

<u>cs</u>	WE	ŌĒ	Mode	I/O Pin	Supply Current
Н	Х	X*	Not Select	High-Z	ISB, ISB1
L	Н	Н	Output Disable	High-Z	Icc
L	Н	L .	Read	Dout	. Icc
L	L	Х	Write	Din	lcc

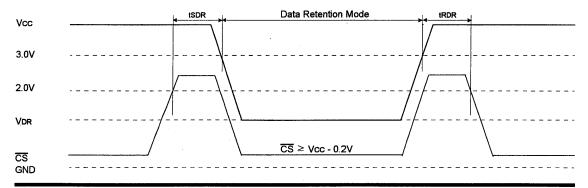
^{*} NOTE: X means Don't Care.

DATA RETENTION CHARACTERISTICS*(TA = 0° to 70°)

Parameter	Symbol	Test Condition	Min.	Тур.	Max.	Unit
Vcc for Data Retention	VDR	CS ≥ Vcc - 0.2V	2.0	-	3.6	V
Data Retention Current	IDR	$Vcc = 3.0V, \overline{CS} \ge Vcc - 0.2V$ $Vin \ge Vcc - 0.2V$ or $Vin \le 0.2V$	-	-	0.4	mA
		$ \begin{array}{c} \text{Vcc} = 2.0 \text{V, } \overline{\text{CS}} \geq \text{Vcc} - 0.2 \text{V} \\ \text{Vin} \geq \text{Vcc} - 0.2 \text{V or Vin} \leq 0.2 \text{V} \\ \end{array} $	-	-	0.3	
Data Retention Set-Up Time	tSDR	See Data Retention	0	-	-	ns
Recovery Time	tRDR	Wave form(below)	5	-	-	ms

NOTE: Above parameters are also guaranteed at industrial temperature range.

DATA RETENTION. WAVE FORM(CS Controlled)





^{*} L-Ver only.

128K x 8 Bit High-Speed CMOS Static RAM(3.3V Operating)

FEATURES

- Fast Access Time 12, 15, 17, 20 ns (Max.)
- · Low Power Dissipation

Standby (TTL) : 20mA(Max.) (CMOS): 5mA(Max.)

0.5mA(Max.); L-ver. only

Operating KM68V1002A/AL - 12: 140mA(Max.)

KM68V1002A/AL - 15: 135mA(Max.)

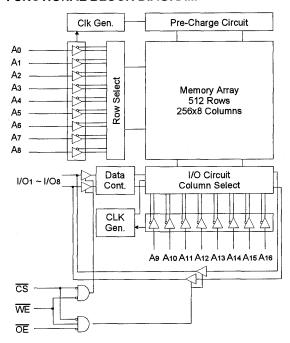
KM68V1002A/AL - 17: 135mA(Max.)

KM68V1002A/AL - 20: 130mA(Max.)

- Single 3.3V±0.3V Power Supply
- . TTL Compatible Inputs and Outputs
- . Fully Static Operation
 - No Clock or Refresh required
- Three State Outputs
- · 2V Minimum Data Retention; L-Ver. only
- · Center Power/Ground Pin Configuration
- · Standard Pin Configuration

KM68V1002A/ALJ: 32-SOJ-400 KM68V1002A/ALSJ: 32-SOJ-300 KM68V1002A/ALT: 32-TSOP2-400F

FUNCTIONAL BLOCK DIAGRAM



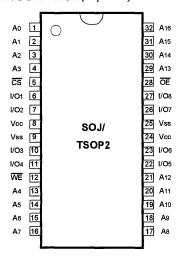
GENERAL DESCRIPTION

The KM68V1002A/AL is a 1,048,576-bit high-speed Static Random Access Memory organized as 131,072 words by 8 bits. The KM68V1002A/AL uses 8 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM68V1002A/AL is packaged in a 400/300 mil 32-pin plastic SOJ or TSOP2 forward.

ORDERING INFORMATION

KM68V1002A/AL -12/15/17/20	Commercial Temp.
KM68V1002AI/ALI -12/15/17/20	Industrial Temp.

PIN CONFIGURATION(Top View)



PIN FUNCTION

Pin Name	Pin Function
A0 - A16	Address Inputs
WE	Write Enable
CS	Chip Select
ŌĒ	Output Enable
I/O1 ~ I/O8	Data Inputs/Outputs
Vcc	Power(+3.3V)
Vss	Ground



ABSOLUTE MAXIMUM RATINGS*

Param	eter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss		VIN, VOUT	-0.5 to 4.6	V
Voltage on Vcc Supply Relative to Vss		Vcc -0.5 to 5.5		V
Power Dissipation		PD	1.0	W
Storage Temperature		Тѕтс	-65 to 150	°C
Operating Temperature	Commercial	TA	0 to 70	°C
	Industrial	TA	-40 to 85	°C

^{*} Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(TA = 0 to 70°C)

Parameter	Symbol	Min	Тур	Max	Unit
Supply Voltage	Vcc	3.0	3.3	3.6	V
Ground	Vss	0	0	0	V
Input Low Voltage	ViH	2.2	-	Vcc + 0.3**	V
Input Low Voltage	VIL	-0.3*	-	0.8	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

- * VIL(Min) = -2.0V a.c(Pulse Width≤10ns) for I ≤ 20mÅ
- ** VIH(Max) = Vcc + 2.0V a.c (Pulse Width \leq 10ns) for I \leq 20mÅ

DC AND OPERATING CHARACTERISTICS(TA = 0 to 70 °C, Vcc= 3.3V ± 0.3V, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	İLI	VIN = Vss to Vcc		-2	2	μA
Output Leakage Current	lLO	CS=VIH or OE=VIH or WE=VIL VOUT = Vss to Vcc		-2	2	μA
Operating Current Icc Min. Cycle,		Min. Cycle, 100% Duty	12ns	-	140	mA
		CS=VIL, VIN = VIH or VIL,	15ns	-	135	1
		IOUT=0mA	17ns	•	135	
			20ns	-	130	1
Standby Current	ISB	Min. Cycle, CS=Viн		-	20	mA
	ISB1	f=0MHz, CS ≥ Vcc-0.2V,	Normal	-	5	mA
		$VIN \ge VCC-0.2V \text{ or } VIN \le 0.2V$	L-Ver.	-	0.5	1
Output Low Voltage Level	VoL	IoL=8mA		-	0.4	V
Output High Voltage Level	Voн	Iон=-4mA		2.4	-	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

CAPACITANCE*(TA =25°C, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	CI/O	V1/0=0V	-	8	pF
Input Capacitance	CIN	VIN=0V	-	6	pF

^{*} NOTE: Capacitance is sampled and not 100% tested.

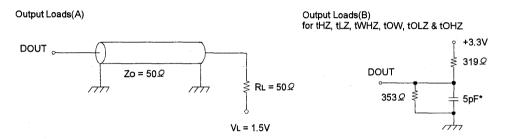


AC CHARACTERISTICS(TA = 0 to 70 °C, Vcc = 3.3V ± 0.3V, unless otherwise noted.)

TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

NOTE: Above test conditions are also applied at industrial temperature range.



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol		/1002A/ 12	1	/1002A/ 15		/1002A/ 17		/1002A/ 20	Unit
		Min	Max	Min	Max	Min	Max	Min	Max	1
Read Cycle Time	tRC	12	-	15	-	17	-	20		ns
Address Access Time	tAA	-	12	-	15	-	17	-	20	ns
Chip Select to Output	tCO	-	12	-	15	-	17	-	20	ns
Output Enable to Valid Output	tOE	-	6	-	7	-	8	_	9	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	6	0	7	0	8	0	9	ns
Output Disable to High-Z Output	tOHZ	0	6	0	7	0	8	0	9	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	0	-	0	-	ns
Chip Selection to Power DownTime	tPD	-	12	-	15	-	17	-	20	ns

NOTE: Above parameters are also guaranteed at industrial temperature range.

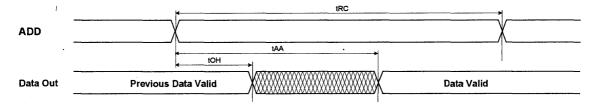
WRITE CYCLE

· Parameter	Symbol	Symbol KM6161002A AL-12		KM6161002A/ · AL-15		KM6161002A/ AL-17		KM6161002A/ AL-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	12	-	15	-	17	-	20	-	ns
Chip Select to End of Write	tCW	8	-	10	-	11	-	12	-	ns
Address Set-up Time	tAS	0	-	0	-	Ó	-	0	-	ns
Address Valid to End of Write	tAW	. 8	-	10	-	11	-	12		ns
Write Pulse Width(OE High)	tWP	8	-	10	-	11	-	12	-	ns
Write Pulse Width(OE Low)	tWP1	12	-	15	-	17	-	20	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	6	0	7	0	8	0	9	ns
Data to Write Time Overlap	tDW	6	-	7	-	8	-	9	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	3	-	ns

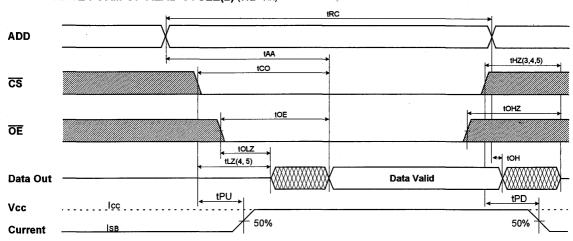
NOTE: Above parameters are also guaranteed at industrial temperature range.

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, CS=OE=VIL, WE=VIH)



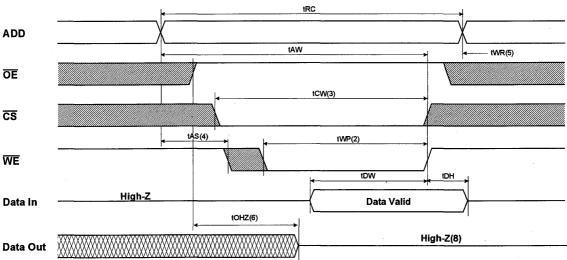
TIMING WAVE FORM OF READ CYCLE(2) (WE=VIH)



NOTES(READ CYCLE)

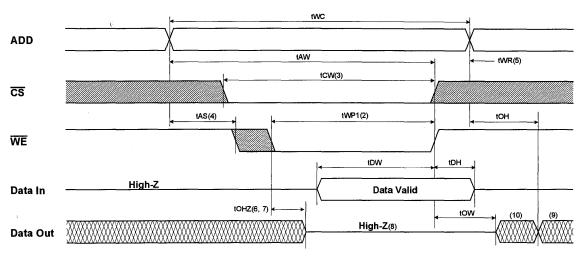
- 1. WE is high for read cycle.
- 2. All read cycle timing is referenced from the last valid address to the first transition address.
- 3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VoH or VoL Levels.
- 4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
- 5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
- 6. Device is continuously selected with CS=VIL.
- 7. Address valid prior to coincident with CS transition low.
- 8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVE FORM OF WRITE CYCLE(1) (OE=Clock)

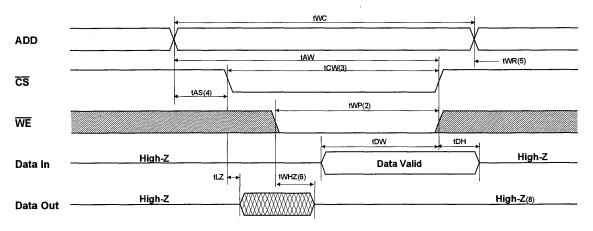




TIMING WAVE FORM OF WRITE CYCLE(2) (OE=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) (CS=Controlled)



NOTES(WRITE CYCLE)

- 1. All write cycle timing is referenced from the last valid address to the first transition address.
- 2. A write occurs during the overlap of a low CS and WE. A write begins at the latest transition CS going low and WE going low; A write ends at the earliest transition \overline{CS} going high or \overline{WE} going high. tWP is measured from the beginning of write to the end of write.

 3. tCW is measured from the later of \overline{CS} going low to end of write.
- 4. tAS is measured from the address valid to the beginning of write.
- 5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as CS or WE going high.
- 6. If OE, CS and WE are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
- 7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
- 8. If $\overline{\text{CS}}$ goes low simultaneously with $\overline{\text{WE}}$ going or after $\overline{\text{WE}}$ going low, the outputs remain high impedance state.
- 9. Dout is the read data of the new address.
- 10. When CS is low: I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

<u>cs</u>	WE	ŌĒ	Mode	I/O Pin	Supply Current
Н	X	X*	Not Select	High-Z	ISB, ISB1
· L	Н	Н	Output Disable	High-Z	lcc
L	Н	L .	Read	Dout	lcc
L	L	Х	Write	Din	lcc

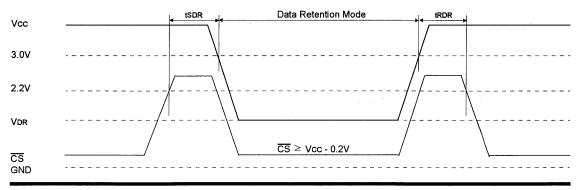
^{*} NOTE: X means Don't Care.

DATA RETENTION CHARACTERISTICS*(TA = 0° to 70°)

Parameter	Symbol	Test Condition	Min.	Тур.	Max.	Unit
Vcc for Data Retention	VDR	CS ≥ Vcc - 0.2V	2.0	-	3.6	V
Data Retention Current	IDR	$Vcc = 2.0V$, $\overline{CS} \ge Vcc - 0.2V$ $Vin \ge Vcc - 0.2V$ or $Vin \le 0.2V$	-		0.5	mA
Data Retention Set-Up Time	tSDR	See Data Retention	0	-	_	ns
Recovery Time	tRDR	Wave form(below)	5	_	_	ms

NOTE: Above parameters are also guaranteed at industrial temperature range.

DATA RETENTION WAVE FORM(CS Controlled)





^{*} L-Ver only.

64K x 16 Bit High-Speed CMOS Static RAM(3.3V Operating)

FEATURES

- Fast Access Time 8,10,12ns (Max.)
- · Low Power Dissipation

Standby (TTL) : 30mA(Max.)

(CMOS): 5mA(Max.)

0.5mA(Max.) - L-Ver. only

Operating KM616V1002B/BL - 8: 200mA(Max.)

KM616V1002B/BL - 10: 190mA(Max.)

KM616V1002B/BL - 12: 180mA(Max.)

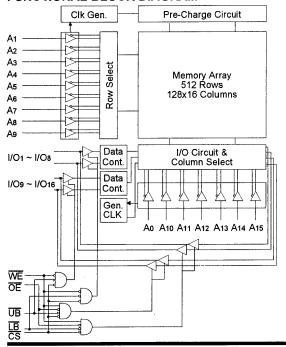
- Single 3.3V \pm 0.3V Power Supply
- TTL Compatible Inputs and Outputs
- · Fully Static Operation
- No Clock or Refresh required
- . Three State Outputs
- . 2V Minimum Data Retention; L-Ver. only
- Center Power/Ground Pin Configuration
- Standard Pin Configuration

KM616V1002B/BLJ: 44-SOJ-400 KM616V1002B/BLT: 44-TSOP2-400F

ORDERING INFORMATION

KM616V1002B/BL -8/10/12	Commercial Temp.				
KM616V1002BI/BLI -8/10/12	Industrial Temp.				

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The KM616V1002B/BL is a 1,048,576-bit high-speed Static Random Access Memory organized as 65,536 words by 16 bits. The KM616V1002B/BL uses 16 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. Also it allows that lower and upper byte access by data byte control ($\overline{\text{UB}}$, $\overline{\text{LB}}$). The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM616V1002B/BL is packaged in a 400mil 44-pin plastic SOJ or TSOP2 forward.

PIN CONFIGURATION (Top View)

A0 1 2 A1 2 A2 3 A3 4 A4 5 CS 6 IV/O2 B1/O3 9 IV/O4 10 IV/O5 11 IV/O5 11 IV/O5 11 IV/O5 11 A5 18 A6 12 A6 2 IV/O5 A8 2 IV/O5 2 IV/O5 A8 2 IV/O5 A8 2 IV/O5 A8 2 IV/O5 A8 2 IV/O5 A8 2 IV/O5 A8 2 IV/O5 A8 2 IV/O5 A8 2 IV/O5 A8 2 IV/O5 A8 2 IV/O5 A8 2 IV/O5 A8 2 IV/O5 A8 2 IV/O5 A8 2 IV/O5 A8 2 IV/O5 A8 2 IV/O5 A8 2 IV/O5 A8 2 IV/O5 A8 2 IV/O5 A1 A6 IV/O5 A8 2 IV/O5 A8 2 IV/O5 A1 A6 IV/O5 A8 2 IV/O5 A8 2 IV/O5 A8 2 IV/O5 A8 2 IV/O5 A1 A6 IV/O5 A8 2 IV/O5 A1 A6 IV/O5 A8 2 IV/O5 A1 A6 IV/O5 A1 A1 A6 IV/O5 A1 A6 IV/O5 A1 A6 IV/O5 A1 A6 IV/O5 A1 A6 IV/O5 A1 A6		SOJ/ TSOP	44 43 42 41 40 39 38 37 36 35 31 30 29 28 27 26 22 24 23	A15 A14 A13 OE UB UB I/O16 I/O15 I/O14 I/O10 I/O9 N.C. A12 A11 A10 A9 N.C.
	L			

PIN FUNCTION

Pin Name	Pin Function
A0 - A15	Address Inputs
WE	Write Enable
cs	Chip Select
ŌĒ	Output Enable
LB	Lower-byte Control(I/O1~I/O8)
ŪB	Upper-byte Control(I/O9~I/O16)
I/O1 ~ I/O16	Data Inputs/Outputs
Vcc	Power(+3.3V)
Vss	Ground
N.C	No Connection



ABSOLUTE MAXIMUM RATINGS*

Param	eter	Symbol	Rating	Unit
Voltage on Any Pin Relati	ve to Vss	VIN, VOUT	-0.5 to 4.6	V
Voltage on Vcc Supply Relative to Vss		Vcc	-0.5 to 5.5	V
Power Dissipation		Po	1.0	W
Storage Temperature		Тѕтс	-65 to 150	°C
Operating Temperature	Commercial	TA	0 to 70	°
	Industrial	TA	-40 to 85	°C

^{*} Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(TA = 0 to 70°C)

Parameter	Symbol	Min	Тур	Max	Unit
Supply Voltage	Vcc	3.0	3.3	3.6	V
Ground	Vss	0	0	0	V
Input Low Voltage	VIH	2.0	-	Vcc + 0.3**	V
Input Low Voltage	VIL	-0.3*	-	0.8	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

- * VIL(Min) = -2.0V a.c(Pulse Width≤6ns) for 1 ≤ 20mA
- ** VIH(Max) = Vcc + 2.0V a.c (Pulse Width ≤ 6ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS(TA = 0 to 70 °C, Vcc= 3.3V ± 0.3V, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	lLi	VIN = Vss to Vcc		-2	2	μA
Output Leakage Current	ILO	CS=VIH or OE=VIH or WE=VIL VOUT = Vss to Vcc	-2	2	μA	
Operating Current	lcc	Min. Cycle, 100% Duty	8ns	-	200	mA
		CS=VIL, VIN = VIH or VIL,	10ns	-	190	
		Iout=0mA	12ns		180	
Standby Current	ISB	Min. Cycle, СS=Vін		-	30	mA
	ISB1	f=0MHz, CS ≥ Vcc-0.2V,	Normal	-	5	mA
		$VIN \ge VCC-0.2V$ or $VIN \le 0.2V$	L-Ver.	-	0.5	
Output Low Voltage Level	VOL	IoL=8mA		-	0.4	٧
Output High Voltage Level	Voн	Iон=-4mA		2.4	-	٧

NOTE: Above parameters are also guaranteed at industrial temperature range.

CAPACITANCE*(TA =25°C, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	Ci/o	Vi/o=0V	-	8	pF
Input Capacitance	Cin	VIN=0V	-	6	pF

^{*} NOTE: Capacitance is sampled and not 100% tested.



AC CHARACTERISTICS(TA = 0 to 70° C, Vcc = $3.3V \pm 0.3V$, unless otherwise noted.)

TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

NOTE: Above test conditions are also applied at industrial temperature range.

Output Loads(A)

Output Loads(B) for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ

DOUT $Zo = 50 \Omega$ VL = 1.5VOutput Loads(B) for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ

* Including Scope and Jig Capacitance

READ CYCLE

P	Symbol KM616V1002B/BL-6		1002B/BL-8	KM616V1002B/BL-10		KM616V1002B/BL-12		Unit
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Uill
Read Cycle Time	tRC	8	-	10	-	12	-	ns
Address Access Time	tAA	-	8	-	10	-	12	ns
Chip Select to Output	tCO	-	8	-	10	-	12	ns
Output Enable to Valid Output	tOE	-	4	-	5	-	6	ns
UB, LB Access Time	tBA	-	8		10	-	12	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
UB, LB Enable to Low-Z Output	tBLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	4	0	5	0	6	ns
Output Disable to High-Z Output	tOHZ	0	4	0	5	0	6	ns
UB, LB Disable to High-Z Output	tBHZ	0	4	0	5	0	6	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns

NOTE: Above parameters are also guaranteed at industrial temperature range.

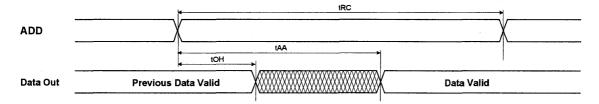
WRITE CYCLE

B	A	KM616V1002B/BL-8		KM616V1002B/BL-10		KM616V1002B/BL-12		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit
Write Cycle Time	tWC	8	-	10	-	12	-	ns
Chip Select to End of Write	tCW	6	-	7	-	8	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	6	-	7	-	8	-	ns.
Write Pulse Width(OE High)	tWP	6	-	7	-	8	-	ns
Write Pulse Width(OE Low)	tWP1	8	-	10	-	12	-	ns
UB, LB Valid to End of Write	tBW	6	-	7	-	8	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	4	0	5	0	6	ns
Data to Write Time Overlap	tDW	4	-	5	-	6	-	ns
Data Hold from Write Time	tDH	0	-	.0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

NOTE: Above parameters are also guaranteed at industrial temperature range.

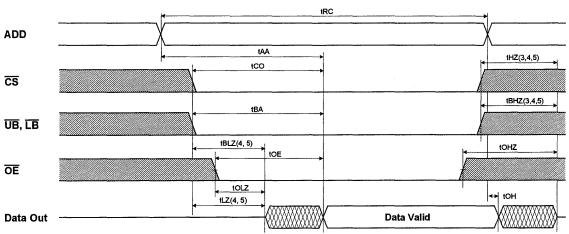
TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS} = \overline{OE} = \overline{UB} = \overline{LB} = VIL, \overline{WE} = VIH)$





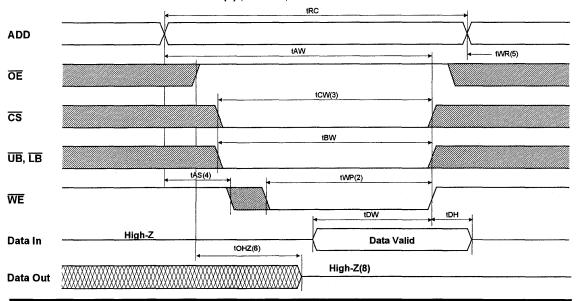
TIMING WAVE FORM OF READ CYCLE(2) (WE=VIH)



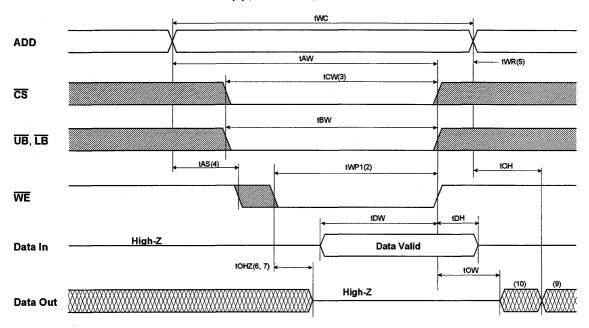
NOTES(READ CYCLE)

- 1. WE is high for read cycle.
- 2. All read cycle timing is referenced from the last valid address to the first transition address.
- 3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VoH or VoL Levels.
- 4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
- 5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
- 6. Device is continuously selected with CS=VIL.
- 7. Address valid prior to coincident with $\overline{\text{CS}}$ transition low.
- 8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

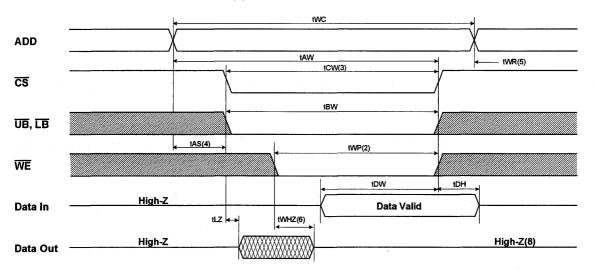
TIMING WAVE FORM OF WRITE CYCLE(1) (OE=Clock)



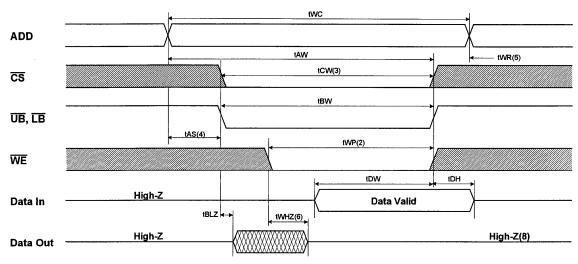




TIMING WAVE FORM OF WRITE CYCLE(3) (CS=Controlled)



TIMING WAVE FORM OF WRITE CYCLE(4) (UB, LB Controlled)



NOTES(WRITE CYCLE)

- 1. All write cycle timing is referenced from the last valid address to the first transition address.
- 2. A write occurs during the overlap of a low \overline{CS} , \overline{WE} , \overline{LB} and \overline{UB} . A write begins at the latest transition \overline{CS} going low and \overline{WE} going low; A write ends at the earliest transition \overline{CS} going high or \overline{WE} going high. tWP is measured from the beginning of write to the end of write.
- 3. tCW is measured from the later of CS going low to end of write.
- 4. tAS is measured from the address valid to the beginning of write.
- 5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as CS, or WE going high.
- 6. If OE. CS and WE are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
- 7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
- 8. If CS goes low simultaneously with WE going or after WE going low, the outputs remain high impedance state.
- 9. Dout is the read data of the new address.
- 10. When \overline{CS} is low: I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

CS	WE	ŌĒ	LB	UB	Mode	1/0	Pin	Supply Current
- 03	VVE	OE.	LD	UB.	Mode	I/O1~I/O8	1/09~1/016	Supply Current
Н	Х	X*	Х	Х	Not Select	High-Z		ISB, ISB1
L	Н	Н	Х	X	X Output Disable		High-Z	Icc
L	Х	Х	Н	Н				
L	Н	L	L	Н	Read	Dout	High-Z	lcc
			H	L		High-Z	Dout]
			L	· L		Dout	Dout	
L	L	Х	L	Н	Write	Din	High-Z	Icc
			н	L		High-Z	DIN	
			L	L		Din	DIN]

^{*} NOTE: X means Don't Care.

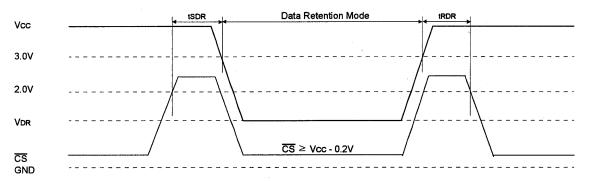


DATA RETENTION CHARACTERISTICS*(TA = 0° to 70°)

Parameter	Symbol	Test Condition	Min.	Тур.	Max.	Unit
Vcc for Data Retention	VDR	<u>CS</u> ≥ Vcc - 0.2V	2.0	-	3.6	V
Data Retention Current	IDR	$Vcc = 3.0V$, $\overline{CS} \ge Vcc - 0.2V$ $Vin \ge Vcc - 0.2V$ or $Vin \le 0.2V$	-	-	0.4	mA
		$ \begin{array}{c} \text{Vcc} = 2.0 \text{V, } \overline{\text{CS}} \geq \text{Vcc} - 0.2 \text{V} \\ \text{Vin} \geq \text{Vcc} - 0.2 \text{V or Vin} \leq 0.2 \text{V} \\ \end{array} $		-	0.3	
Data Retention Set-Up Time	tSDR	See Data Retention	0	-	-	ns
Recovery Time	tRDR	Wave form(below)	5	-	-	ms

NOTE: Above parameters are also guaranteed at industrial temperature range.

DATA RETENTION WAVE FORM(CS Controlled)





^{*} L-Ver only.

64K x 16 Bit High-Speed CMOS Static RAM(3.3V Operating)

FEATURES

- Fast Access Time 12, 15, 17, 20ns (Max.)
- Low Power Dissipation

Standby (TTL) : 20mA(Max.)

(CMOS): 5mA(Max.)

0.5mA(Max.); L-ver. only

Operating KM616V1002A/AL - 12: 170mA(Max.)

KM616V1002A/AL - 15: 165mA(Max.)

KM616V1002A/AL - 17: 165mA(Max.)

KM616V1002A/AL - 20: 160mA(Max.)

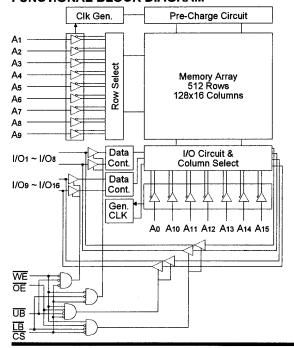
- Single 3.3V ±0.3V Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
- No Clock or Refresh required
- · Three State Outputs
- · 2V Minimum Data Retention; L-Ver. only
- · Center Power/Ground Pin Configuration
- Data Byte Control : LB : I/O1~ I/O8, UB : I/O9~ I/O16
- Standard Pin Configuration

KM616V1002A/ALJ: 44-SOJ-400 KM616V1002A/ALT: 44-TSOP2-400F

ORDERING INFORMATION

KM616V1002A/AL -12/15/17/20	Commercial Temp.
KM616V1002AI/ALI -12/15/17/20	Industrial Temp.

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The KM616V1002A/AL is a 1,048,576-bit high-speed Static Random Access Memory organized as 65,536 words by 16 bits. The KM616V1002A/AL uses 16 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. Also it allows that lower and upper byte access by data byte control (UB, LB). The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM616V1002A/AL is packaged in a 400mil 44-pin plastic SOJ or TSOP2 forward.

PIN CONFIGURATION (Top View)

A0 1 2 A2 3 A3 A4 5 CS 6 I/O1 7 I/O2 B1 I/O3 9 I/O4 10 I/O7 15 I/O8 16 WE 17 A5 18 A6 19 A7 20 A8 21 N.C. 22	0	SO		44 43 42 41 40 39 38 37 36 35 34 33 32 29 28 27 26 25 24 23	A15 A14 A13 OE UB I/O16 I/O15 I/O14 I/O10 I/O9 N.C. A12 A11 A10 A9 N.C.

PIN FUNCTION

Pin Name	Pin Function
A0 - A15	Address inputs
WE	Write Enable
CS	Chip Select
ŌĒ	Output Enable
LB	Lower-byte Control(I/O1~I/O8)
ŪB	Upper-byte Control(I/O9~I/O16)
I/O1 ~ I/O16	Data Inputs/Outputs
Vcc	Power(+3.3V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter		Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss		VIN, VOUT	-0.5 to 4.6	V
Voltage on Vcc Supply Re	elative to Vss	Vcc	,-0.5 to 5.5	V
Power Dissipation		PD	1.0	W
Storage Temperature		Тѕтс	-65 to 150	°
Operating Temperature	Commercial	TA	0 to 70	°C
	Industrial	TA	-40 to 85	C

^{*} Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(TA = 0 to 70°C)

Parameter	Symbol	Min	Тур	Max	Unit
Supply Voltage	Vcc	3.0	3.3	3.6	V
Ground	Vss	0	0	0	V
Input Low Voltage	ViH	2.2	-	Vcc + 0.3**	V
Input Low Voltage	VIL	-0.3*	-	0.8	٧

NOTE: Above parameters are also guaranteed at industrial temperature range.

- * VIL(Min) = -2.0V a.c(Pulse Width≤10ns) for 1 ≤ 20mA
- ** VIH(Max) = Vcc + 2.0V a.c (Pulse Width≤10ns) for I ≤ 20mÅ

DC AND OPERATING CHARACTERISTICS(TA = 0 to 70°C, Vcc= 3.3V ± 0.3V, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	lLi	VIN = Vss to Vcc	-2	2	μA	
Output Leakage Current	lLO	CS=VIH or OE=VIH or WE=VIL VOUT = Vss to Vcc	-2	2	μA	
Operating Current	lcc	Min. Cycle, 100% Duty	12ns	_	170	mA
		CS=VIL, VIN = VIH or VIL,	15ns	-	165	
		IOUT=0mA	17ns	-	165	
			20ns	-	160	
Standby Current	ISB	Min. Cycle, CS=Viн		-	20	mA
	ISB1	f=0MHz, CS ≥ Vcc-0.2V,	Normal	-	5	mΑ
		$VIN \ge VCC-0.2V$ or $VIN \le 0.2V$	-	0.5		
Output Low Voltage Level	Vol	IoL=8mA	-	0.4	٧	
Output High Voltage Level	Voн	IOH=-4mA	2.4	-	٧	

NOTE: Above parameters are also guaranteed at industrial temperature range.

CAPACITANCE*(TA =25°C, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	C1/0	VI/o=0V		8	рF
Input Capacitance	Cin	VIN=0V	-	6	рF

^{*} NOTE: Capacitance is sampled and not 100% tested.

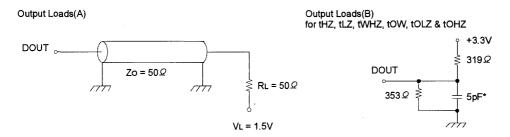


AC CHARACTERISTICS(TA = 0 to 70 °C, Vcc = 3.3V ± 0.3V, unless otherwise noted.) TEST CONDITIONS

Parameter Value Input Pulse Levels 0V to 3V Input Rise and Fall Times 3ns Input and Output timing Reference Levels 1.5V

See below

NOTE: Above test conditions are also applied at industrial temperature range.



* Including Scope and Jig Capacitance

READ CYCLE

Output Loads

Parameter	Symbol		V1002A/ 12		V1002A/ 15		V1002A/ -17		V1002A/ 20	Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	12	-	15	-	17	-	20	-	ns
Address Access Time	tAA	_	12	-	15	-	17	-	20	ns
Chip Select to Output	tCO	-	12	-	15	-	17	-	20	ns
Output Enable to Valid Output	tOE	-	6	-	7	-	8	-	9	ns
UB, LB Access Time	tBA	-	6	-	7	-	8	-	9	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	0	-	ns
UB, LB Enable to Low-Z Output	tBLZ	0	-	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	6	0	7	0	8	0	9	ns
Output Disable to High-Z Output	tOHZ	0	6	0	7	0	8	0	9	ns
UB, LB Disable to High-Z Output	tBHZ	0	6	0	7	0	8	0	9	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	3	-	ns

NOTE: Above parameters are also guaranteed at industrial temperature range.

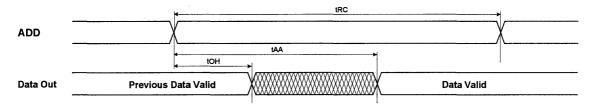
WRITE CYCLE

Parameter	Symbol	KM616\ AL	/1002A/ -12		/1002A/ -15		/1002A/ -17		V1002A/ -20	Unit
		Min	Max	Min	Max	Min	Max	Min	Max	ns ns ns ns ns ns ns ns ns ns ns
Write Cycle Time	tWC	12	-	15	-	17	-	20	-	ns
Chip Select to End of Write	tCW	8	-	10	-	11	-	12	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	8	-	10	-	11	•	12	-	ns
Write Pulse Width(OE High)	tWP	8	-	10	-	11	-	12	-	ns
Write Pulse Width(OE Low)	tWP1	12	· -	15	-	17	-	20	-	ns
UB, LB Valid to End of Write	tBW	. 8		10	-	11	-	12	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	6	0	7	0	8	0	9	ns
Data to Write Time Overlap	tDW	6	-	7	-	8	-	9	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	3	-	ns

NOTE: Above parameters are also guaranteed at industrial temperature range.

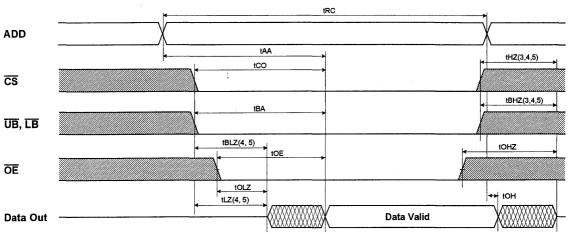
TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS} = \overline{OE} = \overline{UB} = \overline{LB} = VIL, \overline{WE} = VIH)$





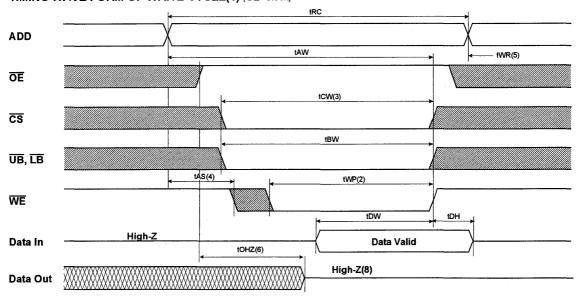
TIMING WAVE FORM OF READ CYCLE(2) (WE=VIH)



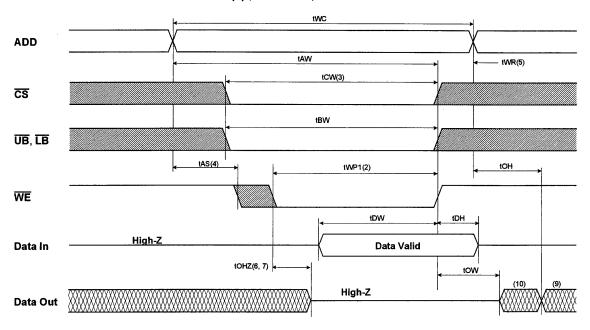
NOTES(READ CYCLE)

- 1. WE is high for read cycle.
- 2. All read cycle timing is referenced from the last valid address to the first transition address.
- 3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VoH or VoL Levels.
- 4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
- 5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
- 6. Device is continuously selected with CS=VIL.
- 7. Address valid prior to coincident with CS transition low.
- 8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

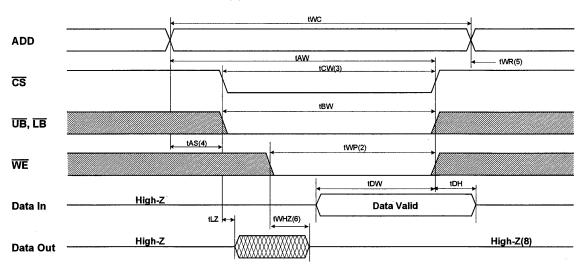
TIMING WAVE FORM OF WRITE CYCLE(1) (OE=Clock)



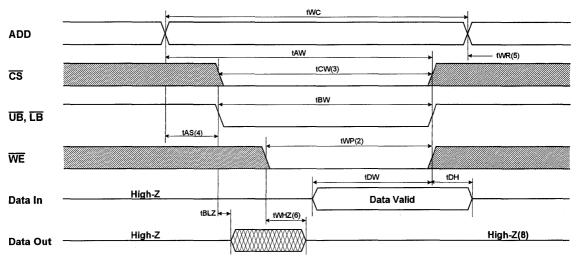
TIMING WAVE FORM OF WRITE CYCLE(2) (OE=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) (CS=Controlled)



TIMING WAVE FORM OF WRITE CYCLE(4) (UB, LB Controlled)



NOTES(WRITE CYCLE)

- 1. All write cycle timing is referenced from the last valid address to the first transition address.
- 2. A write occurs during the overlap of a low \overline{CS} , \overline{WE} , \overline{LB} and \overline{UB} . A write begins at the latest transition \overline{CS} going low and \overline{WE} going low; A write ends at the earliest transition \overline{CS} going high or \overline{WE} going high. tWP is measured from the beginning of write to the end of write.
- 3. tCW is measured from the later of $\overline{\text{CS}}$ going low to end of write.
- 4. tAS is measured from the address valid to the beginning of write.
- 5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as CS. or WE going high.
- 6. If \overline{OE} . \overline{CS} and \overline{WE} are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
- 7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
- 8. If $\overline{\text{CS}}$ goes low simultaneously with $\overline{\text{WE}}$ going or after $\overline{\text{WE}}$ going low, the outputs remain high impedance state.
- 9. Dout is the read data of the new address.
- 10. When \overline{CS} is low: I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

cs	WE	ŌĒ	ĽΒ	UB	Mode I/O Pin	I/O Pin		
US	VVE	OE.	LD	0.5	Mode	1/01~1/08	1/09~1/016	Supply Current
Н	Х	X*	Х	Х	Not Select	High-Z		ISB, ISB1
L	Н	H	X	X	Output Disable	High-Z	High-Z	lcc
L	Х	X	Н	н				
L	Н	L	L	Н	Read	Dout	High-Z	lcc
			Ξ	L		High-Z	Dout	
			L	L		Dout	Dout	
L	L	Х		Н	Write	Din	High-Z	lcc
			Ξ	L		High-Z	Din	
			L	L		Din	Din	

^{*} NOTE: X means Don't Care.

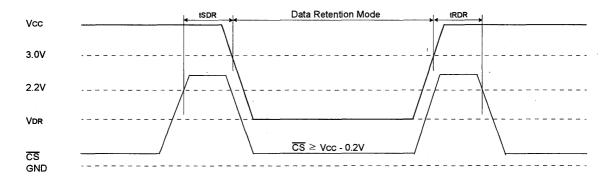


DATA RETENTION CHARACTERISTICS*(TA = 0° to 70°)

Parameter	Symbol	Test Condition	Min.	Тур.	Max.	Unit
Vcc for Data Retention	VDR	CS ≥ Vcc - 0.2V	2.0	-	3.6	V
Data Retention Current	IDR	$Vcc = 2.0V, \overline{CS} \ge Vcc - 0.2V$ $Vin \ge Vcc - 0.2V \text{ or } Vin \le 0.2V$	- ,	-	0.5	mA
Data Retention Set-Up Time	tSDR	See Data Retention	0	-	-	ns
Recovery Time	tRDR	Wave form(below)	5	-	-	ms

NOTE: Above parameters are also guaranteed at industrial temperature range.

DATA RETENTION WAVE FORM(CS Controlled)





^{*} L-Ver only.

4M High Speed SRAM (3.3V Operation)

1M x 4 Bit (with OE)High-Speed CMOS Static RAM(3.3V Operating)

FEATURES

- Fast Access Time 10,12,15 ns (Max.)
- · Low Power Dissipation

Standby (TTL) : 40mA(Max.)

(CMOS) : 10mA(Max.)

1mA(Max.)- L-Ver.

Operating KM64V4002B/BL - 10: 160mA(Max.)

KM64V4002B/BL - 12: 150mA(Max.)

KM64V4002B/BL - 15: 140mA(Max.)

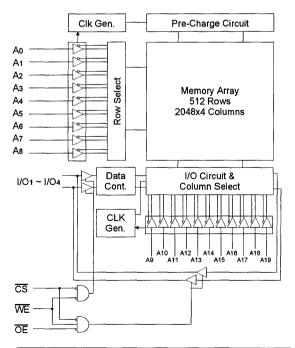
- Single $3.3V \pm 0.3V$ Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
 - No Clock or Refresh required
- . Three State Outputs
- · Low Data Retention Voltage: 2V(Min.) L-Ver. Only
- · Center Power/Ground Pin Configuration
- . Standard Pin Configuration

KM64V4002B/BLJ: 32-SOJ-400 KM64V4002B/BLT: 32-TSOP2-400F

ORDERING INFORMATION

KM64V4002B/BL -10/12/15	Commercial Temp.
KM64V4002B/BLI -10/12/15	Industrial Temp.

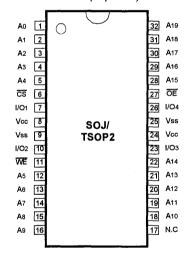
FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The KM64V4002B/BL is a 4,194,304-bit high-speed Static Random Access Memory organized as 1,048,576 words by 4 bits. The KM64V4002B/BL uses 4 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM64V4002B/BL is packaged in a 400 mil 32-pin plastic SOJ or TSOP(II) forward.

PIN CONFIGURATION(Top View)



PIN FUNCTION

Pin Name	Pin Function
A0 - A19	Address Inputs
WE	Write Enable
CS	Chip Select
ŌĒ	Output Enable
I/O1 ~ I/O4	Data Inputs/Outputs
Vcc	Power(+3.3V)
Vss	Ground
N.C	No Connection



ABSOLUTE MAXIMUM RATINGS*

Param	eter	Symbol	Rating	Unit
Voltage on Any Pin Relat	ive to Vss	VIN, VOUT -0.5 to 4.6		V
Voltage on Vcc Supply R	elative to Vss	Vcc	-0.5 to 5.5	V
Power Dissipation		PD	1.0	W
Storage Temperature		Тѕтс	-65 to 150	°
Operating Temperature	Commercial	TA	0 to 70	°C
	Industrial	TA	-40 to 85	C

^{*} Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(TA = 0 to 70°C)

Parameter	Symbol	Min	Тур	Max	Unit
Supply Voltage	Vcc	3.0	3.3	3.6	V
Ground	Vss	0	0	0	٧
Input Low Voltage	ViH	2.0	-	Vcc + 0.3**	٧
Input Low Voltage	VIL	-0.3*	-	0.8	٧

NOTE: Above parameters are also guaranteed at industrial temperature range.

DC AND OPERATING CHARACTERISTICS(TA = 0 to 70 °C, Vcc= 3.3V ± 0.3V, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Max	Unit	
Input Leakage Current	lu	VIN = Vss to Vcc		-2	2	μA
Output Leakage Current	ILO	CS=ViH or OE=ViH or WE=ViL Vout = Vss to Vcc	-2	2	μA	
Operating Current	lcc	Min. Cycle, 100% Duty	10ns	-	160	mA
		CS=VIL, VIN = VIH or VIL, IOUT=0mA	12ns	-	150	1
			15ns	-	140	1
Standby Current	IsB	Min. Cycle, CS=Viн	-	40	mA	
	ISB1	f=0MHz, CS ≥ Vcc-0.2V,	Normal	-	10	mA
		$VIN \ge VCC-0.2V$ or $VIN \le 0.2V$	L-Ver.	-	1	
Output Low Voltage Level	VoL	IOL=8mA	-	0.4	V	
Output High Voltage Level	Voн	IOH=-4mA	2.4	-	V	

NOTE: Above parameters are also guaranteed at industrial temperature range.

CAPACITANCE*(TA =25°C, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	Ci/o	V1/0=0V	-	8	рF
Input Capacitance	CIN	Vin=0V	-	7	pF

^{*} NOTE: Capacitance is sampled and not 100% tested.



^{*} VIL(Min) = -2.0V a.c(Pulse Width≤8ns) for 1 ≤ 20mA

^{**} VIH(Max) = Vcc + 2.0V a.c (Pulse Width \le 8ns) for I \le 20mA

AC CHARACTERISTICS(TA = 0 to 70°C, Vcc = 3.3V ± 0.3V, unless otherwise noted.)

KM64V4002B/BL, KM64V4002B/BLI

TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

NOTE: Above test conditions are also applied at industrial temperature range.

Output Loads(A) Output Loads(B) for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ +3.3V ≶ 319Ω DOUT Zo = 50Ω $RL = 50 \Omega$ 353Ω VL = 1.5V

* Including Scope and Jig Capacitance

READ CYCLE

	KM64V4002B/BL		02B/BL-10	KM64V4002B/BL-12		KM64V4002B/BL-15		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit
Read Cycle Time	tRC	10	-	12	-	15	-	ns
Address Access Time	tAA	-	10	-	12	-	15	ns
Chip Select to Output	tCO	-	10	-	12	-	15	ns
Output Enable to Valid Output	tOE	-	5	-	6	-	7	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	5	0	6	0	7	ns
Output Disable to High-Z Output	tOHZ	0	5	0	6	0	7	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	0	-	ns
Chip Selection to Power DownTime	tPD	-	10	-	12	-	15	ns

NOTE: Above parameters are also guaranteed at industrial temperature range.



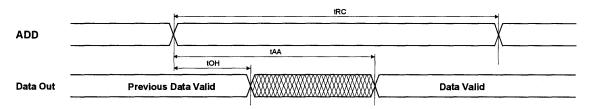
WRITE CYCLE

D	S	KM64V4002B/BL-10		KM64V4002B/BL-12		KM64V4002B/BL-15		T
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit
Write Cycle Time	tWC	10	-	12	-	15	-	ns
Chip Select to End of Write	tCW	7	-	8	-	10	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	7	-	8	-	10	-	ns
Write Pulse Width(OE High)	tWP	7	-	8	-	10	-	ns
Write Pulse Width(OE Low)	tWP1	10	-	12	-	15	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	5	Ū	6	0	7	ns
Data to Write Time Overlap	tDW	5	-	6	-	7	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

NOTE: Above parameters are also guaranteed at industrial temperature range.

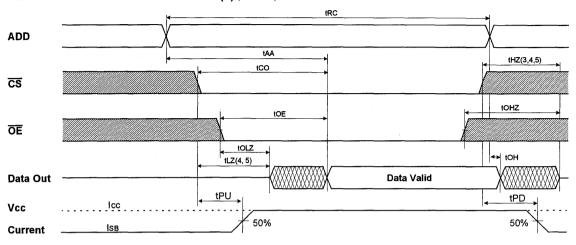
TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS} = \overline{OE} = VIL$, $\overline{WE} = VIH$)





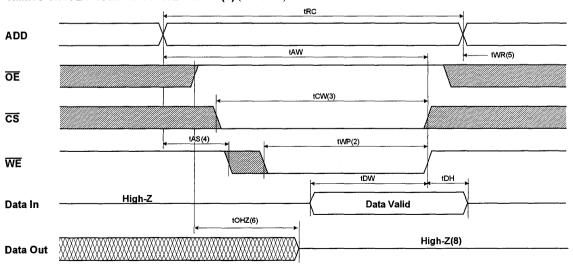
TIMING WAVE FORM OF READ CYCLE(2) (WE=VIH)



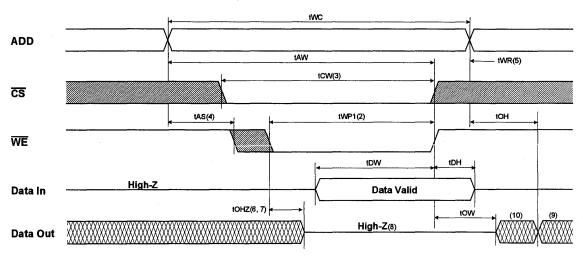
NOTES(READ CYCLE)

- 1. WE is high for read cycle.
- 2. All read cycle timing is referenced from the last valid address to the first transition address.
- 3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VoH or VoL Levels.
- 4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
- 5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
- 6. Device is continuously selected with CS=VIL.
- 7. Address valid prior to coincident with CS transition low.
- 8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

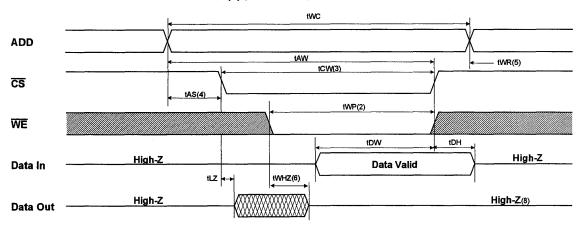
TIMING WAVE FORM OF WRITE CYCLE(1) (OE=Clock)



TIMING WAVE FORM OF WRITE CYCLE(2) (OE=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) (CS=Controlled)





NOTES(WRITE CYCLE)

- 1. All write cycle timing is referenced from the last valid address to the first transition address.
- 2. A write occurs during the overlap of a low \overline{CS} and \overline{WE} . A write begins at the latest transition \overline{CS} going low and \overline{WE} going low; A write ends at the earliest transition \overline{CS} going high or \overline{WE} going high. tWP is measured from the beginning of write to the end of write.
- 3. tCW is measured from the later of CS going low to end of write.
- 4. tAS is measured from the address valid to the beginning of write.
- 5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as CS or WE going high.
- 6. If OE, CS and WE are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
- 7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
- 8. If CS goes low simultaneously with WE going or after WE going low, the outputs remain high impedance state.
- 9. Dout is the read data of the new address.
- 10. When \overline{CS} is low: I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

CS	WE	ŌĒ	Mode	I/O Pin	Supply Current
Н	X	X*	Not Select	High-Z	ISB, ISB1
L	Н	Н	Output Disable	High-Z	Icc
L	Н	L	Read	Dout	Icc
L	L	. X	Write	Din .	Icc

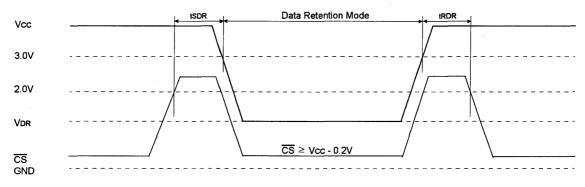
^{*} NOTE : X means Don't Care.

DATA RETENTION CHARACTERISTICS*(TA = 0° to 70°)

Parameter	Symbol	Test Condition	Min.	Тур.	Max.	Unit
Vcc for Data Retention	VDR	VDR CS ≥ Vcc - 0.2V		-	3.6	٧
Data Retention Current		$Vcc = 3.0V, \overline{CS} \ge Vcc - 0.2V$ $Vin \ge Vcc - 0.2V \text{ or } Vin \le 0.2V$	-	-	0.9	mA
	IDR	$Vcc = 2.0V, \overline{CS} \ge Vcc - 0.2V$ $Vin \ge Vcc - 0.2V$ or $Vin \le 0.2V$	-	-	0.7	mA
Data Retention Set-Up Time	tSDR	See Data Retention	0	-	-	ns
Recovery Time	tRDR	Wave form(below)	5	-	-	ms

NOTE: Above parameters are also guaranteed at industrial temperature range.

DATA RETENTION WAVE FORM(CS Controlled)



^{*} L-Ver only.

1M x 4 Bit (with OE)High-Speed CMOS Static RAM(3.3V Operating)

FEATURES

- Fast Access Time 12,13,15 ns (Max.)
- · Low Power Dissipation

Standby (TTL) : 60 mA(Max.)

(CMOS): 30mA(Max.)

Operating KM64BV4002 - 12: 160mA(Max.)

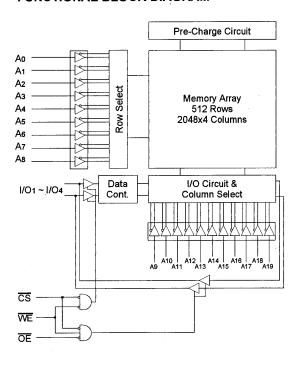
KM64BV4002 - 13: 155mA(Max.)

KM64BV4002 - 15: 150mA(Max.)

- Single 3.3V+10%/-5% Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
 - No Clock or Refresh required
- · Three State Outputs
- · Center Power/Ground Pin Configuration
- · Standard Pin Configuration

KM64BV4002: 32-SOJ-400

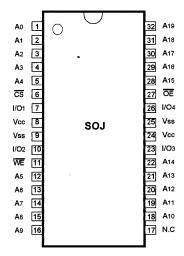
FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The KM64BV4002 is a 4,194,304-bit high-speed Static Random Access Memory organized as 1,048,576 words by 4 bits. The KM64BV4002 uses 4 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using SAMSUNG's advanced BiCMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM64BV4002 is packaged in a 400 mil 32-pin plastic SOJ.

PIN CONFIGURATION(Top View)



PIN FUNCTION

Pin Name	Pin Function
A0 - A19	Address inputs
WE	Write Enable
cs	Chip Select
ŌĒ	Output Enable
I/O1 ~ I/O4	Data Inputs/Outputs
Vcc	Power(+3.3V)
Vss	Ground
N.C	No Connection



ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	VIN, VOUT	-0.5 to 4.6	V
Voltage on Vcc Supply Relative to Vss	Vcc	-0.5 to 5.5	V
Power Dissipation	PD	1.0	W
Storage Temperature	Тѕтс	-65 to 150	°C
Operating Temperature	TA	0 to 70	°C

^{*} Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(TA = 0 to 70°C)

Parameter	Symbol	Min	Тур	Max	Unit
Supply Voltage	Vcc	3.13	3.3	3.6	V
Ground	Vss	0	0	0	V
Input Low Voltage	ViH	2.2	-	Vcc + 0.3**	V
Input Low Voltage	VIL	-0.3*	•	0.8	V

^{*} VIL(Min) = -2.0V a.c(Pulse Width≤10ns) for I ≤ 20mÅ

DC AND OPERATING CHARACTERISTICS (TA = 0 to 70 °C, Vcc= 3.3V+10%/-5%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	lLi	Vin = Vss to Vcc		-2	2	μA
Output Leakage Current	lLO	CS=VIH or OE=VIH or WE=VIL VOUT = Vss to Vcc	-10	10	μA	
	Min. Cycle, 100% Duty	12ns	-	160	mA	
		CS=VIL, VIN = VIH or VIL, IOUT=0mA	13ns	-	155	1
			15ns	-	150	1
Standby Current	ISB	Min. Cycle, CS=Viн		•	60	mA
ISB1		f=0MHz, $\overline{\text{CS}} \ge \text{Vcc-0.2V}$, VIN $\ge \text{Vcc-0.2V}$ or VIN $\le 0.2\text{V}$	-	30	mA	
Output Low Voltage Level	VoL	IoL=8mA		-	0.4	V
Output High Voltage Level	Voн	IOH=-4mA		2.4	-	V

CAPACITANCE*(TA =25°C, f=1.0MHz)

ltem	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	CI/O	VI/0=0V	-	8	pF
Input Capacitance	CIN	VIN=0V	-	7	pF

^{*} NOTE: Capacitance is sampled and not 100% tested.



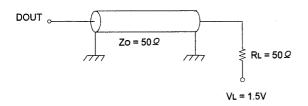
^{**} VIH(Max) = Vcc + 2.0V a.c (Pulse Width \leq 10ns) for I \leq 20mÅ

AC CHARACTERISTICS(TA = 0 to 70°C, Vcc =3.3V +10%/-5%, unless otherwise noted.)

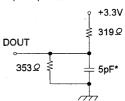
TEST CONDITIONS

Parameter	Value
Input Pulse Levels	OV to 3V
Input Rise and Fall Times	3 ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

Output Loads(A)



Output Loads(B) for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

Parameter		KM64BV4002-12		KM64BV4002-13		KM64BV4002-15		Unit
	Symbol	Min	Max	Min	Max	Min	Max	- Onit
Read Cycle Time	tRC	12	-	13	-	15	-	ns
Address Access Time	tAA	-	12	-	13	-	15	ns
Chip Select to Output	tCO	:-	12	-	13	-	15	ns
Output Enable to Valid Output	tOE	-	6	-	6	-	7	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	6	0	6	0	7	ns
Output Disable to High-Z Output	tOHZ	0	6	0	6	0	7	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns

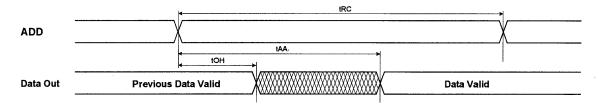


WRITE CYCLE

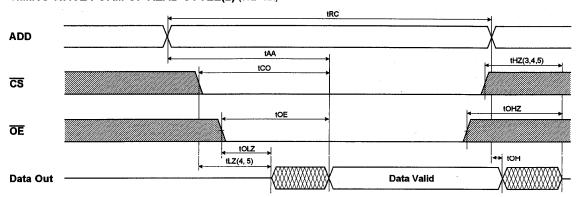
Parameter		KM64BV4002-12		KM64BV4002-13		KM64BV4002-15		
	Symbol -	Min	Max	Min	Max	Min	Max	- Unit
Write Cycle Time	tWC	12	-	13	-	15	-	ns
Chip Select to End of Write	tCW	9	-	10	-	10	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	9	-	10	-	10	-	ns
Write Pulse Width(OE High)	tWP	9	-	10	-	10	-	ns
Write Pulse Width(OE Low)	tWP1	10	-	11	-	12	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	6.5	0	7	0	7.5	ns
Data to Write Time Overlap	tDW	7	-	7	-	8	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, CS=OE=VIL, WE=VIH)



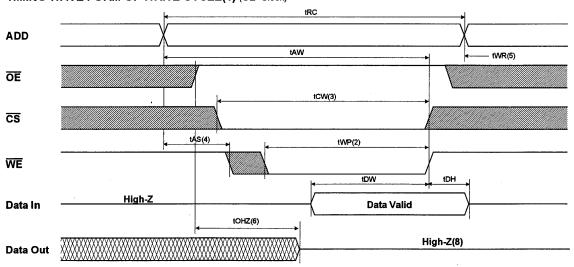
TIMING WAVE FORM OF READ CYCLE(2) (WE=VIH)



NOTES(READ CYCLE)

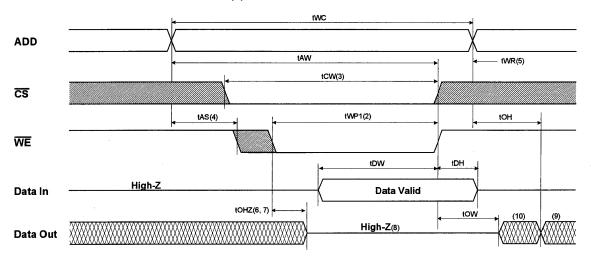
- 1. WE is high for read cycle.
- 2. All read cycle timing is referenced from the last valid address to the first transition address.
- 3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VoH or VoL Levels.
- 4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
- 5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
- 6. Device is continuously selected with CS=VIL.
- 7. Address valid prior to coincident with CS transition low.
- 8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVE FORM OF WRITE CYCLE(1) (OE=Clock)

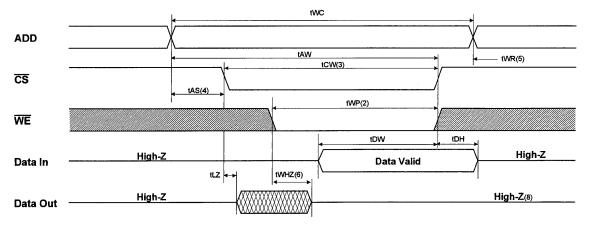




TIMING WAVE FORM OF WRITE CYCLE(2) (OE=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) (CS=Controlled)



NOTES(WRITE CYCLE)

- 1. All write cycle timing is referenced from the last valid address to the first transition address.
- 2. A write occurs during the overlap of a low \overline{CS} and \overline{WE} . A write begins at the latest transition \overline{CS} going low and \overline{WE} going low; A write ends at the earliest transition \overline{CS} going high or \overline{WE} going high. tWP is measured from the beginning of write to the end of write.
- 3. tCW is measured from the later of $\overline{\text{CS}}$ going low to end of write.
- 4. tAS is measured from the address valid to the beginning of write.
- 5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as CS or WE going high.
- 6. If \overline{OE} , \overline{CS} and \overline{WE} are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
- 7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
- 8. If \overline{CS} goes low simultaneously with \overline{WE} going or after \overline{WE} going low, the outputs remain high impedance state.
- 9. Dout is the read data of the new address.
- When \(\overline{\overl

FUNCTIONAL DESCRIPTION

ĊŠ	WE	ŌĒ	Mode	I/O Pin	Supply Current
Н	Х	X*	Not Select	High-Z	ISB, ISB1
L	Н	Н	Output Disable	High-Z	Icc
L	Н	L	Read	Dout	lcc
L	L	Х	Write	DIN	Icc

^{*} NOTE : X means Don't Care.

1M x 4 Bit (with OE)High-Speed CMOS Static RAM

FEATURES

- Fast Access Time 15,17,20 ns (Max.)
- · Low Power Dissipation

Standby (TTL) : 50mA(Max.)

(CMOS): 10mA(Max.)

Operating KM64V4002A - 15: 140mA(Max.)

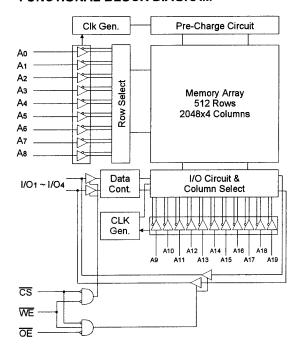
KM64V4002A - 17: 135mA(Max.)

KM64V4002A - 20: 130mA(Max.)

- Single $3.3V \pm 0.3V$ Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
 - No Clock or Refresh required
- Three State Outputs
- · Center Power/Ground Pin Configuration
- · Standard Pin Configuration

KM64V4002AJ: 32-SOJ-400

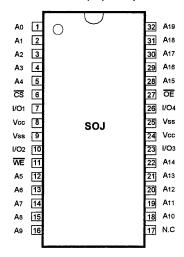
FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The KM64V4002A is a 4,194,304-bit high-speed Static Random Access Memory organized as 1,048,576 words by 4 bits. The KM64V4002A uses 4 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM64V4002A is packaged in a 400 mil 32-pin plastic SOJ.

PIN CONFIGURATION(Top View)



PIN FUNCTION

Pin Name	Pin Function				
A0 - A19	Address Inputs				
WE	Write Enable				
CS	Chip Select				
ŌĒ	Output Enable				
I/O1 ~ I/O4	Data Inputs/Outputs				
Vcc	Power(+3.3V)				
Vss	Ground				
N.C	No Connection				



ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	Vin, Vout	-0.5 to 4.6	V
Voltage on Vcc Supply Relative to Vss	Vcc	-0.5 to 4.6	V
Power Dissipation	PD	1.0	W
Storage Temperature	Тѕтс	-65 to 150	°C
Operating Temperature	TA	0 to 70	°C

^{*} Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(TA = 0 to 70°C)

Parameter	Symbol	Min	Тур	Max	Unit
Supply Voltage	Vcc	3.0	3.3	3.6	V
Ground	Vss	0	0	0	٧
Input Low Voltage	VIH	2.2	-	Vcc + 0.3**	٧
Input Low Voltage	VIL	-0.3*	-	0.8	٧

^{*} VIL(Min) = -2.0V a.c(Pulse Width \leq 10ns) for $1 \leq 20$ mÅ

DC AND OPERATING CHARACTERISTICS(TA = 0 to 70 °C, Vcc= 3.3V ± 0.3V, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Max	Unit	
Input Leakage Current	ÎLI	Vin = Vss to Vcc		-2	2	μA
Output Leakage Current	lLO	CS=ViH or OE=ViH or WE=ViL Vout = Vss to Vcc	-2	2	μA	
Operating Current	Icc	Min. Cycle, 100% Duty	15ns	-	140	mA
		CS=VIL, VIN = VIH or VIL, IOUT=0mA	17ns	-	135	1
			20ns	-	130	1
Standby Current	ISB	Min. Cycle, CS=Vін		-	50	mA
	ISB1	f=0MHz, $\overline{CS} \ge Vcc$ -0.2V, Vin $\ge Vcc$ -0.2V or Vin $\le 0.2V$		-	10	mA
Output Low Voltage Level	Vol	IoL=8mA		-	0.4	٧
Output High Voltage Level	Voн	IOH=-4mA		2.4	-	٧

CAPACITANCE*(TA =25°C, f=1.0MHz)

ltem	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	CI/O	Vi/o=0V	-	8	pF
Input Capacitance	CIN	Vin=0V	-	7	pF

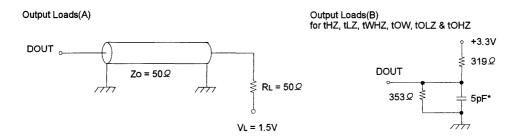
^{*} NOTE : Capacitance is sampled and not 100% tested.



^{**} VIH(Max) = Vcc + 2.0V a.c (Pulse Width \le 10ns) for I \le 20mA

AC CHARACTERISTICS(TA = 0 to 70 °C, Vcc = $3.3V \pm 0.3V$, unless otherwise noted.) TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	6t	KM64V	4002A-15	KM64V4002A-17		KM64V4002A-20		Unit
	Symbol	Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	15	-	17	-	20	-	ns
Address Access Time	tAA	-	15	-	17	-	20	ns
Chip Select to Output	tCO	-	15	-	17	-	20	ns
Output Enable to Valid Output	tOE	-	7	-	8	-	9	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	7	0	8	0	9	ns
Output Disable to High-Z Output	tOHZ	0	7	0	8	0	9	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	0	-	ns
Chip Selection to Power DownTime	tPD	-	15	-	17	-	20	ns



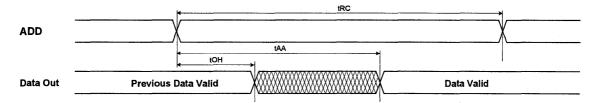
KM64V4002A CMOS SRAM

WRITE CYCLE

Parameter		KM64V4002A-15		KM64V4002A-17		KM64V4002A-20		T
	Symbol -	Min	Max	Min	Max	Min	Max	- Unit
Write Cycle Time	tWC	15	-	17	-	20	-	ns
Chip Select to End of Write	tCW	12	-	13	-	14	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	12	-	13	-	14	_	ns
Write Pulse Width(OE High)	tWP	12	-	13	-	14	-	ns
Write Pulse Width(OE Low)	tWP1	15	-	17	-	20	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	7	0	8	0	9	ns
Data to Write Time Overlap	tDW	8	-	9	-	10		ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

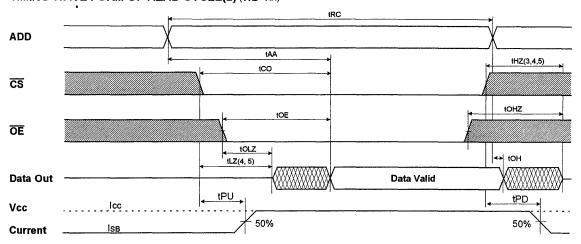
TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS} = \overline{OE} = VIL, \overline{WE} = VIH)$





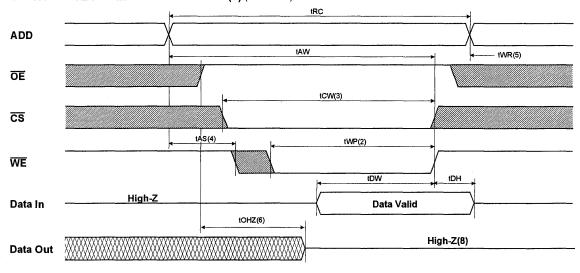
TIMING WAVE FORM OF READ CYCLE(2) (WE=VIH)



NOTES(READ CYCLE)

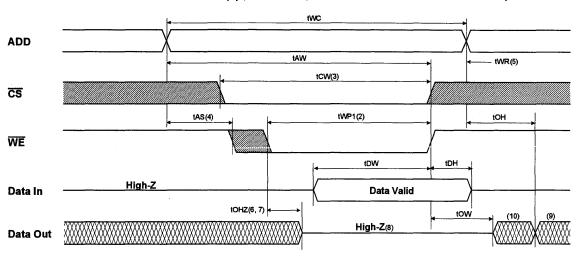
- 1. WE is high for read cycle.
- 2. All read cycle timing is referenced from the last valid address to the first transition address.
- 3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VoH or VoL Levels.
- 4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
- 5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
- 6. Device is continuously selected with $\overline{\text{CS}}=\text{Vil.}$
- 7. Address valid prior to coincident with $\overline{\text{CS}}$ transition low.
- 8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVE FORM OF WRITE CYCLE(1) (OE=Clock)

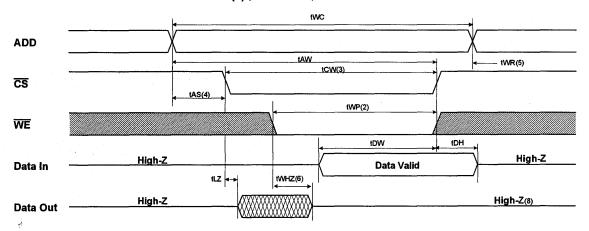




TIMING WAVE FORM OF WRITE CYCLE(2) (OE=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) (CS=Controlled)



NOTES(WRITE CYCLE)

- 1. All write cycle timing is referenced from the last valid address to the first transition address.
- 2. A write occurs during the overlap of a low \overline{CS} and \overline{WE} . A write begins at the latest transition \overline{CS} going low and \overline{WE} going low; A write ends at the earliest transition \overline{CS} going high or \overline{WE} going high. tWP is measured from the beginning of write to the end of write.
- 3. tCW is measured from the later of \overline{CS} going low to end of write.
- 4. tAS is measured from the address valid to the beginning of write.
- 5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as CS or WE going high.
- 6. If \overline{OE} , \overline{CS} and \overline{WE} are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
- 7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
- 8. If \overline{CS} goes low simultaneously with \overline{WE} going or after \overline{WE} going low, the outputs remain high impedance state.
- 9. Dout is the read data of the new address.
- When CS is low: I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

CS	WE	ŌĒ	Mode	I/O Pin	Supply Current
Н	Х	X*	Not Select	High-Z	ISB, ISB1
L	Н	Н	Output Disable	High-Z	Icc
L	Н	L	Read	Dout	lcc
L	L	X	Write	DIN	lcc

^{*} NOTE : X means Don't Care.

512K x 8 Bit High-Speed CMOS Static RAM(3.3V Operating)

FEATURES

- Fast Access Time 10,12,15 ns (Max.)
- · Low Power Dissipation

Standby (TTL) : 40mA(Max.)

(CMOS): 10mA(Max.)

1mA(Max.)- L-Ver.

Operating KM68V4002B/BL - 10: 170mA(Max.)

KM68V4002B/BL - 12: 160mA(Max.)

KM68V4002B/BL - 15: 150mA(Max.)

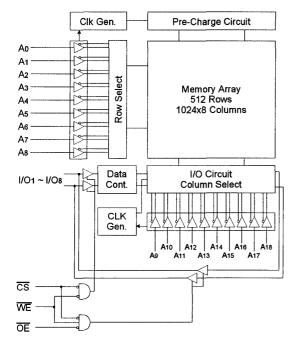
- Single 3.3V ± 0.3V Power Supply
- · TTL Compatible Inputs and Outputs
- . Fully Static Operation
- No Clock or Refresh required
- · Three State Outputs
- Low Data Retention Voltage: 2V(Min.) L-Ver. Only
- · Center Power/Ground Pin Configuration
- · Standard Pin Configuration

KM68V4002B/BLJ: 36-SOJ-400 KM68V4002B/BLT: 36-TSOP2-400F

ORDERING INFORMATION

KM68V4002B/BL -10/12/15	Commercial Temp.
KM68V4002B/BLI -10/12/15	Industrial Temp.

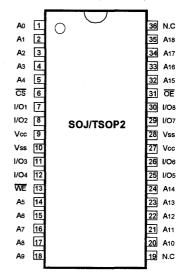
FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The KM68V4002B/BL is a 4,194,304-bit high-speed Static Random Access Memory organized as 524,288 words by 8 bits. The KM68V4002B/BL uses 8 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM68V4002B/BL is packaged in a 400 mil 36-pin plastic SOJ or TSOP(II) forward.

PIN CONFIGURATION(Top View)



PIN FUNCTION

Pin Name	Pin Function
A0 - A18	Address Inputs
WE	Write Enable
CS	Chip Select
ŌE _	Output Enable
1/01 ~ 1/08	Data Inputs/Outputs
Vcc	Power(+3.3V)
Vss	Ground
N.C	No Connection

KM68V4002B/BL, KM68V4002B/BLI

ABSOLUTE MAXIMUM RATINGS*

Param	eter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss		VIN, VOUT	-0.5 to 4.6	V
Voltage on Vcc Supply Relative to Vss		Vcc -0.5 to 5.5		V
Power Dissipation		PD	1.0	W
Storage Temperature		Тѕтс	-65 to 150	°C
Operating Temperature	Commercial	TA	0 to 70	°C
	Industrial	TA	-40 to 85	°C

^{*} Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(TA = 0 to 70°C)

Parameter	Symbol	Min	Тур	Max	Unit
Supply Voltage	Vcc	3.0	3.3	3.6	V
Ground	Vss	0	0	0	V
Input Low Voltage	VIH	2.0	-	Vcc + 0.3**	V
Input Low Voltage	VIL	-0.3*	-	0.8	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

- * VIL(Min) = -2.0V a.c(Pulse Width \leq 8ns) for $1 \leq 20$ mÅ
- ** VIH(Max) = Vcc + 2.0V a.c (Pulse Width ≤ 8ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS(TA = 0 to 70 °C, Vcc= 3.3V ± 0.3V, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	lLi	VIN = Vss to Vcc		-2	2	μA
Output Leakage Current	lLO	CS=VIH or OE=VIH or WE=VIL Vout = Vss to Vcc		-2	2	μΑ
Operating Current	Icc	Min. Cycle, 100% Duty	10ns	-	170	mΑ
		CS=VIL, VIN = VIH or VIL, IOUT=0mA	12ns	-	160	
			15ns	-	150	
Standby Current	IsB	Min. Cycle, CS=Viн		-	40	mА
	ISB1	f=0MHz, CS ≥ Vcc-0.2V,	Normal	-	10	mA
		$VIN \ge VCC-0.2V$ or $VIN \le 0.2V$	L-Ver.	-	1	
Output Low Voltage Level	Vol	IoL=8mA		-	0.4	V
Output High Voltage Level	Voн	IOH=-4mA		2.4	-	· V

NOTE: Above parameters are also guaranteed at industrial temperature range.

CAPACITANCE*(TA =25°C, f=1.0MHz)

	Item	Symbol	Test Conditions	MIN	Max	Unit
Γ	Input/Output Capacitance	Ci/o	VI/0=0V	-	8	pF
	Input Capacitance	CIN	VIN=0V	-	7	pF

^{*} NOTE: Capacitance is sampled and not 100% tested.

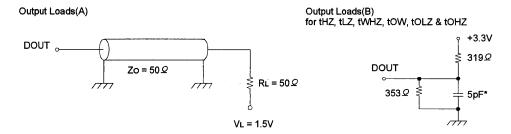


AC CHARACTERISTICS(TA = 0 to 70° , Vcc =3.3V \pm 0.3V, unless otherwise noted.)

TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

NOTE: Above test conditions are also applied at industrial temperature range.



* Including Scope and Jig Capacitance

READ CYCLE

	[l	KM68V4002B/BL-1		KM68V4002B/BL-12		KM68V4002B/BL-15		Unit
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit
Read Cycle Time	tRC	10	-	12	-	15	-	ns
Address Access Time	tAA	-	10	-	12	-	15	ns
Chip Select to Output	tCO	-	10	-	12	-	15	ns
Output Enable to Valid Output	tOE	-	5	-	6	-	7	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	5	0	6	0	7	ns
Output Disable to High-Z Output	tOHZ	0	5	0	6	0	7	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	0	-	ns
Chip Selection to Power DownTime	tPD	-	15	-	12	-	15	ns

NOTE: Above parameters are also guaranteed at industrial temperature range.



WRITE CYCLE

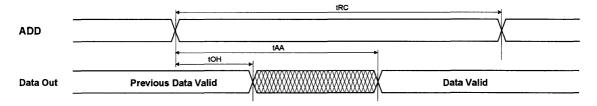
D		KM68V4002B/BL-10		KM68V4002B/BL-12		KM68V4002B/BL-15		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit
Write Cycle Time	tWC	10	•	12	-	15	-	ns
Chip Select to End of Write	tCW	7	-	8	-	10	-	ns
Address Set-up Time	tAS	0	-	0	-	0	- .	ns
Address Valid to End of Write	tAW	7	•	8	-	10	-	ns
Write Pulse Width(OE High)	tWP	7	-	8	-	10	-	ns
Write Pulse Width(OE Low)	tWP1	10	-	12	-	15	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	5	0	6	.0	7	ns
Data to Write Time Overlap	tDW	5	-	6	-	7	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

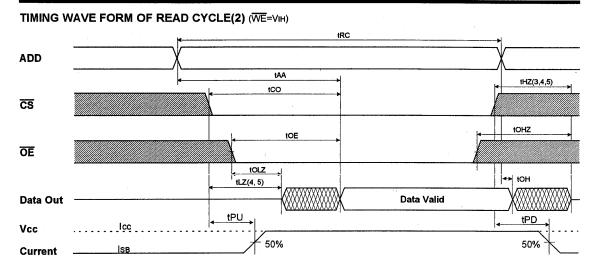
NOTE: Above parameters are also guaranteed at industrial temperature range.

KM68V4002B/BL, KM68V4002B/BLI

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, CS=OE=VIL, WE=VIH)

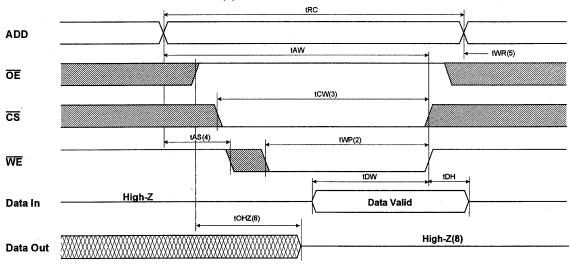




NOTES(READ CYCLE)

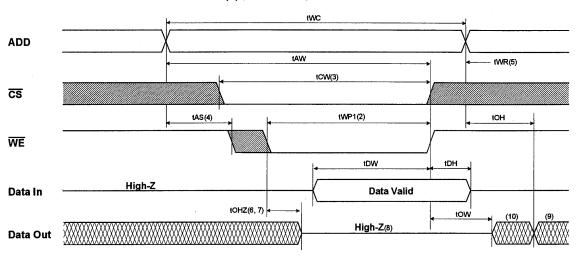
- 1. WE is high for read cycle.
- 2. All read cycle timing is referenced from the last valid address to the first transition address.
- 3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VoH or VoL Levels.
- 4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
- 5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
- 6. Device is continuously selected with CS=Vil.
- 7. Address valid prior to coincident with CS transition low.
- 8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVE FORM OF WRITE CYCLE(1) (OE=Clock)

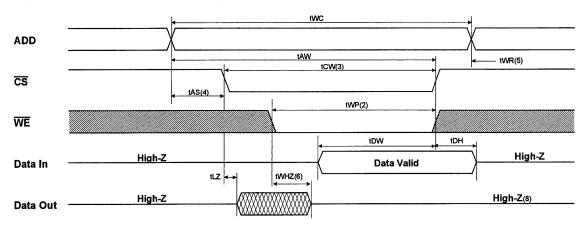




TIMING WAVE FORM OF WRITE CYCLE(2) (OE=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) (CS=Controlled)



NOTES(WRITE CYCLE)

- 1. All write cycle timing is referenced from the last valid address to the first transition address.
- 2. A write occurs during the overlap of a low $\overline{\text{CS}}$ and $\overline{\text{WE}}$. A write begins at the latest transition $\overline{\text{CS}}$ going low and $\overline{\text{WE}}$ going low; A write ends at the earliest transition $\overline{\text{CS}}$ going high or $\overline{\text{WE}}$ going high. tWP is measured from the beginning of write to the end of write.
- 3. tCW is measured from the later of $\overline{\text{CS}}$ going low to end of write.
- 4. tAS is measured from the address valid to the beginning of write.
- 5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as CS or WE going high.
- 6. If \overline{OE} , \overline{CS} and \overline{WE} are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
- 7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
- 8. If CS goes low simultaneously with WE going or after WE going low, the outputs remain high impedance state.
- 9. Dout is the read data of the new address.
- 10. When $\overline{\text{CS}}$ is low: I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

<u>cs</u>	WE	ŌĒ	Mode	I/O Pin	Supply Current
Н	X	X*	Not Select	High-Z	ISB, ISB1
L	Н	Н	Output Disable	High-Z	lcc
. L	Н	L	Read	Dout	lcc
L	L	Х	Write	DIN	lcc

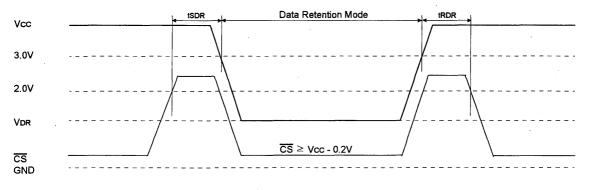
^{*} NOTE : X means Don't Care.

DATA RETENTION CHARACTERISTICS*(TA = 0° to 70°)

Parameter	Symbol	Test Condition	Min.	Тур.	Max.	Unit
Vcc for Data Retention	VDR	CS ≥ Vcc - 0.2V	2.0	-	3.6	٧
		$ \begin{array}{c} \text{Vcc} = 3.0 \text{V, } \overline{\text{CS}} \geq \text{Vcc} - 0.2 \text{V} \\ \text{Vin} \geq \text{Vcc} - 0.2 \text{V or Vin} \leq 0.2 \text{V} \\ \end{array} $	-	-	0.9	mA
Data Retention Current	IDR	$Vcc = 2.0V, \overline{CS} \ge Vcc - 0.2V$ $Vin \ge Vcc - 0.2V$ or $Vin \le 0.2V$	-	-	0.7	mA
Data Retention Set-Up Time	tSDR	See Data Retention	0	-	-	ns
Recovery Time	tRDR	Wave form(below)	5	· -	_	ms

NOTE: Above parameters are also guaranteed at industrial temperature range.

DATA RETENTION WAVE FORM(CS Controlled)





^{*} L-Ver only.

512K x 8 Bit High-Speed CMOS Static RAM(3.3V Operating)

FEATURES

- Fast Access Time 12,13,15 ns (Max.)
- · Low Power Dissipation

Standby (TTL) : 60mA(Max.)

(CMOS): 30mA(Max.)

Operating KM68BV4002 - 12: 170mA(Max.)

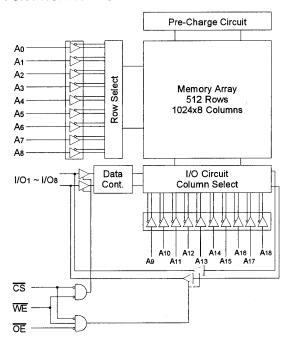
KM68BV4002 - 13: 165mA(Max.)

KM68BV4002 - 15: 160mA(Max.)

- Single 3.3V + 10%/-5% Power Supply
- . TTL Compatible Inputs and Outputs
- Fully Static Operation
 - No Clock or Refresh required
- · Three State Outputs
- · Center Power/Ground Pin Configuration
- · Standard Pin Configuration

KM68BV4002J: 36-SOJ-400

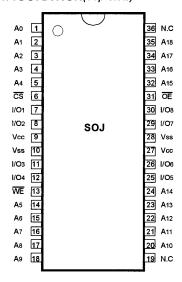
FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The KM68BV4002 is a 4,194,304-bit high-speed Static Random Access Memory organized as 524,288 words by 8 bits. The KM68BV4002 uses 8 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using Samsung's advanced BiCMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM68BV4002 is packaged in a 400 mil 36-pin plastic SOJ.

PIN CONFIGURATION(Top View)



PIN FUNCTION

Pin Name	Pin Function		
A0 - A18	Address inputs		
WE	Write Enable		
CS	Chip Select		
ŌĒ	Output Enable		
I/O1 ~ I/O8	Data Inputs/Outputs		
Vcc	Power(+3.3V)		
Vss	Ground		
N.C	No Connection		



ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	VIN, VOUT	-0.5 to 4.6	V
Voltage on Vcc Supply Relative to Vss	Vcc	-0.5 to 5.5	V
Power Dissipation	Po	1.0	W
Storage Temperature	Тѕтс	-65 to 150	°C
Operating Temperature	TA	0 to 70	°C

^{*} Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(TA = 0 to 70°C)

Parameter	Symbol	Min	Тур	Max	Unit
Supply Voltage	Vcc	3.13	3.3	3.6	V
Ground	Vss	0	0	0	V
Input Low Voltage	ViH	2.2	-	Vcc + 0.3**	V
Input Low Voltage	VIL	-0.3*	-	0.8	V

^{*} VIL(Min) = -2.0V a.c(Pulse Width≤10ns) for I ≤ 20mÅ

DC AND OPERATING CHARACTERISTICS(TA = 0 to 70°C, Vcc= 3.3V+10%/-5%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	lu	VIN = Vss to Vcc		-2	2	μA
Output Leakage Current	lLO	CS=ViH or OE=ViH or WE=ViL Vout = Vss to Vcc		-10	10	μA
Operating Current	Icc	Min. Cycle, 100% Duty	12ns	- •	170	mA
		CS=VIL, VIN = VIH or VIL, IOUT=0mA	13ns	-	165	1
			15ns	-	160	1
Standby Current	IsB	Min. Cycle, CS=Vін		-	60	mA
	ISB1 $f=0MHz$, $\overline{CS} \ge Vcc-0.2V$, $Vin \ge Vcc-0.2V$ or $Vin \le 0.2V$			-	30	mA
Output Low Voltage Level	Vol	IoL=8mA		-	0.4	V
Output High Voltage Level	Voн	loн=-4mA		2.4	-	V

CAPACITANCE*(TA =25°C, f=1.0MHz)

Input Capacitance	CIN	VIN=0V	-	7	pF
Input/Output Capacitance	CI/O	V1/0=0V	-	8	pF
Item	Symbol	Test Conditions	MIN	Max	Unit

^{*} NOTE : Capacitance is sampled and not 100% tested.



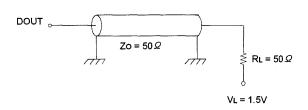
^{**} VIH(Max) = Vcc + 2.0V a.c (Pulse Width \le 10ns) for I \le 20mA

AC CHARACTERISTICS(TA = 0 to 70 °C, Vcc =3.3V +10%/-5%, unless otherwise noted.)

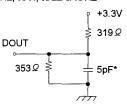
TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below





Output Loads(B) for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

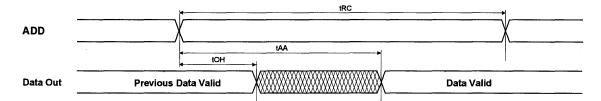
Parameter	Symbol	KM68BV4002-12		KM68BV4002-13		KM68BV4002-15		- Unit
		Min	Max	Min	Max	Min	Max	Unit
Read Cycle Time	tRC	12	•	13	-	15	-	ns
Address Access Time	tAA	-	12	-	13	-	15	ns
Chip Select to Output	tCO	-	12	-	13	-	15	ns
Output Enable to Valid Output	tOE	-	6	-	6	-	7	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	6	0	6	0	7	ns
Output Disable to High-Z Output	tOHZ	0	6	0	6	0	7	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns

WRITE CYCLE

Parameter	Combal	KM68BV4002-12		KM68BV4002-13		KM68BV4002-15		Unit
	Symbol	Min	Max	Min	Max	Min	Max	- Unit
Write Cycle Time	tWC	12	-	13	-	15	-	ns
Chip Select to End of Write	tCW	8.5	-	8.5	-	10	-	ns
Address Set-up Time	tAS	0 .	-	0	-	0	-	ns
Address Valid to End of Write	tAW	8.5	-	8.5		10	_	ns
Write Pulse Width(OE High)	tWP	8.5	-	8.5	-	10	-	ns
Write Pulse Width(OE Low)	tWP1	10	-	10	-	12	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	6	0.	6	0	7	ns
Data to Write Time Overlap	tDW	7	-	7	-	8	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	•	3	-	ns

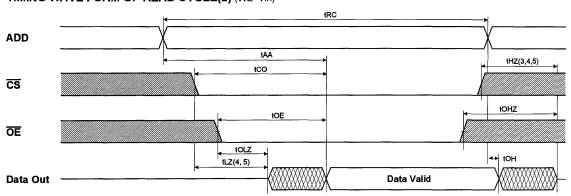
TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS} = \overline{OE} = VIL, \overline{WE} = VIH)$





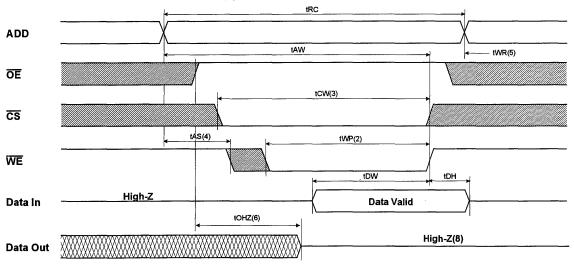
TIMING WAVE FORM OF READ CYCLE(2) (WE=VIH)



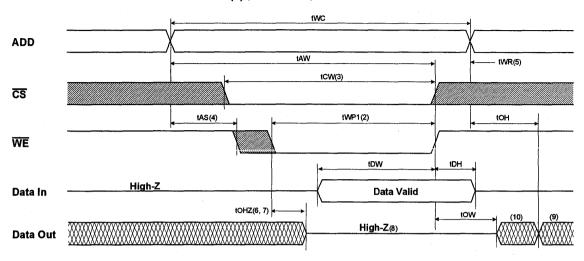
NOTES(READ CYCLE)

- 1. WE is high for read cycle.
- 2. All read cycle timing is referenced from the last valid address to the first transition address.
- 3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VoH or VoL Levels.
- 4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
- 5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
- 6. Device is continuously selected with CS=VIL.
- 7. Address valid prior to coincident with CS transition low.
- 8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

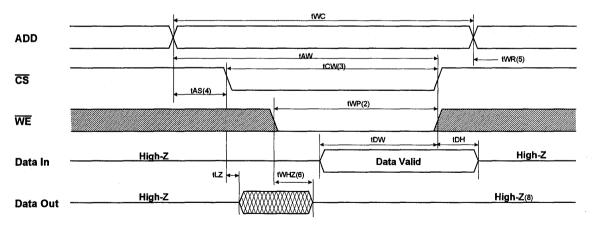
TIMING WAVE FORM OF WRITE CYCLE(1) (OE=Clock)



TIMING WAVE FORM OF WRITE CYCLE(2) (OE=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) (CS=Controlled)



NOTES(WRITE CYCLE)

- 1. All write cycle timing is referenced from the last valid address to the first transition address.
- 2. A write occurs during the overlap of a low \overline{CS} and \overline{WE} . A write begins at the latest transition \overline{CS} going low and \overline{WE} going low; A write ends at the earliest transition \overline{CS} going high or \overline{WE} going high. tWP is measured from the beginning of write to the end of write.
- 3. tCW is measured from the later of CS going low to end of write.
- 4. tAS is measured from the address valid to the beginning of write.
- 5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as CS or WE going high.
- 6. If \overline{OE} , \overline{CS} and \overline{WE} are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
- 7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
- 8. If $\overline{\text{CS}}$ goes low simultaneously with $\overline{\text{WE}}$ going or after $\overline{\text{WE}}$ going low, the outputs remain high impedance state.
- 9. Dout is the read data of the new address.
- 10. When \overline{CS} is low: I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

CS	WE	ŌĒ	Mode	I/O Pin	Supply Current
Н	Х	X*	Not Select	High-Z	ISB, ISB1
L	н	Н	Output Disable	High-Z	lcc
L	Н	L	Read	Dout	lcc
L	L	X	Write	DIN	lcc

^{*} NOTE : X means Don't Care.

512K x 8 Bit High-Speed CMOS Static RAM

FEATURES

• Fast Access Time 15,17,20 ns (Max.)

Low Power Dissipation

Standby (TTL) : 50mÅ(Max.) (CMOS): 10mÅ(Max.)

Operating KM68V4002A - 15: 160mA(Max.)

KM68V4002A - 17: 155mA(Max.) KM68V4002A - 20: 150mA(Max.)

Single 3.3V±0.3V Power Supply

. TTL Compatible Inputs and Outputs

Fully Static Operation

- No Clock or Refresh required

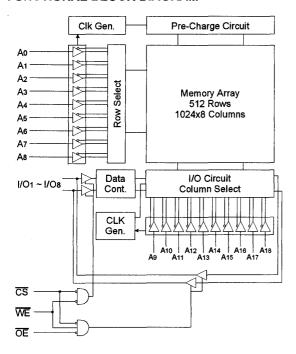
Three State Outputs

· Center Power/Ground Pin Configuration

· Standard Pin Configuration

KM68V4002AJ: 36-SOJ-400

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The KM68V4002A is a 4,194,304-bit high-speed Static Random Access Memory organized as 524,288 words by 8 bits. The KM68V4002A uses 8 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM68V4002A is packaged in a 400 mil 36-pin plastic SOJ.

PIN CONFIGURATION(Top View)

Αo	1	\circ	36	N.C
A1	2		35	A 18
A2	3	'	34	A17
Аз	4		33	A 16
A 4	5		32	A15
cs	6		31	Œ
!/01	7		30	1/08
1/02	8	SOJ	29	1/07
Vcc	9		28	Vss
Vss	10		27	Vcc
I/O3	11		26	1/06
1/04	12		25	1/05
WE	13		24	A 14
A 5	14		23	A 13
A6	15		22	A 12
A 7	16		21	A11
A8	17		20	A 10
A 9	18		19	N.C
			1	

PIN FUNCTION

Pin Name	Pin Function
A0 - A18	Address Inputs
WE	Write Enable
CS	Chip Select
ŌĒ	Output Enable
I/O1 ~ I/O8	Data Inputs/Outputs
Vcc	Power(+3.3V)
Vss	Ground
N.C	No Connection



ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	VIN, VOUT	-0.5 to 4.6	V
Voltage on Vcc Supply Relative to Vss	Vcc	-0.5 to 4.6	٧
Power Dissipation	PD	1.0	W
Storage Temperature	Тѕтс	-65 to 150	°C
Operating Temperature	TA	0 to 70	°C

^{*} Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(TA = 0 to 70°C)

Parameter	Symbol	Min	Тур	Max	Unit
Supply Voltage	Vcc	3.0	3.3	3.6	V
Ground	Vss	0	0	0	V
Input Low Voltage	ViH	2.2	-	Vcc + 0.3**	V
Input Low Voltage	VIL	-0.3*	-	0.8	V

^{*} VIL(Min) = -2.0V a.c(Pulse Width≤10ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS(TA = 0 to 70 °C, Vcc= 3.3V ± 0.3V, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Max	Unit	
Input Leakage Current	ILI	Vin = Vss to Vcc	Vin = Vss to Vcc			μA
Output Leakage Current	lLO	CS=VIH or OE=VIH or WE=VIL VOUT = Vss to Vcc	-2	2	μA	
Operating Current	lcc ·	Min. Cycle, 100% Duty	15ns	-	160	mA
		CS=VIL, VIN = VIH or VIL, IOUT=0mA	17ns	-	155	
			20ns	-	150	
Standby Current	ISB	Min. Cycle, CS=Vін		-	50	mΑ
	ISB1	f=0MHz, $\overline{CS} \ge Vcc-0.2V$, $Vin \ge Vcc-0.2V$ or $Vin \le 0.2V$		=	10	mA
Output Low Voltage Level	Vol	IoL=8mA		-	0.4	٧
Output High Voltage Level	Vон	IOH=-4mA	2.4	-	٧	

CAPACITANCE*(TA =25°C, f=1.0MHz)

(tem	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	Ci/O	Vi/o=0V	-	8	pF
Input Capacitance	CIN	Vin=0V	-	7	pF

^{*} NOTE: Capacitance is sampled and not 100% tested.

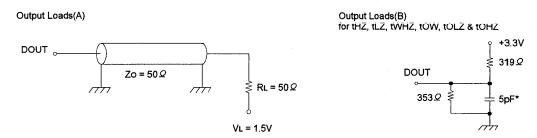


^{**} VIH(Max) = Vcc + 2.0V a.c (Pulse Width ≤ 10ns) for I ≤ 20mÅ

AC CHARACTERISTICS(TA = 0 to 70 °C, Vcc =3.3V \pm 0.3V, unless otherwise noted.)

TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below



* Including Scope and Jig Capacitance

READ CYCLE

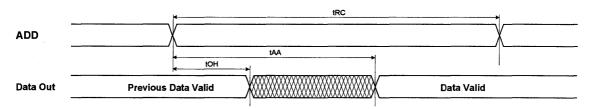
Parameter	S	KM68V	KM68V4002A-15		KM68V4002A-17		4002A-20	T
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit
Read Cycle Time	tRC	15	•	17	-	20	-	ns
Address Access Time	tAA	-	15	-	17	-	20	ns
Chip Select to Output	tCO	-	15	-	17	-	20	ns
Output Enable to Valid Output	tOE	-	7	-	8	-	9	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	7	0	8 `	0	9	ns
Output Disable to High-Z Output	tOHZ	0	7	0	8	0	9	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	0	-	ns
Chip Selection to Power DownTime	tPD	-	15	-	17	_	20	ns

WRITE CYCLE

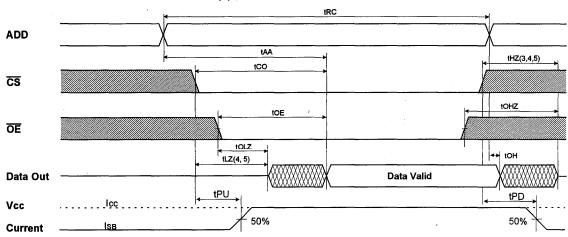
Parameter	6	KM68V4002A-15		KM68V4002A-17		KM68V4002A-20		
	Symbol	Min	Max	Min	Max	Min	Max	Unit
Write Cycle Time	tWC	15	-	17	-	20	-	ns
Chip Select to End of Write	tCW	12	-	13	-	14	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	12	-	13	-	14	-	ns
Write Pulse Width(OE High)	tWP	12	-	13	-	14	-	ns
Write Pulse Width(OE Low)	tWP1	15	-	17	-	20	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	7	0	8	0	9	ns
Data to Write Time Overlap	tDW	8	-	9	-	10	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3		3	-	ns

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, CS=OE=VIL, WE=VIH)



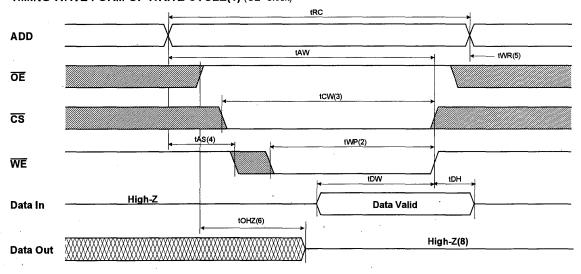
TIMING WAVE FORM OF READ CYCLE(2) (WE=VIH)



NOTES(READ CYCLE)

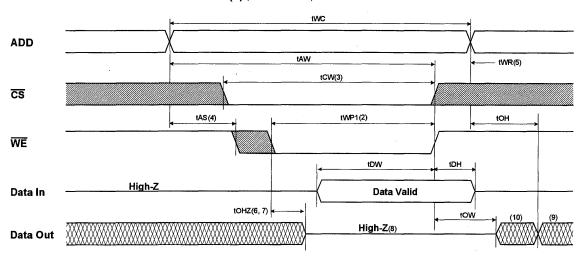
- 1. WE is high for read cycle.
- 2. All read cycle timing is referenced from the last valid address to the first transition address.
- 3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VoH or VoL Levels.
- 4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
- 5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
- 6. Device is continuously selected with CS=VIL.
- 7. Address valid prior to coincident with CS transition low.
- 8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVE FORM OF WRITE CYCLE(1) (OE=Clock)

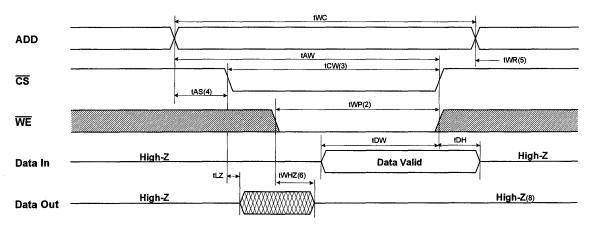




TIMING WAVE FORM OF WRITE CYCLE(2) (OE=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) (CS=Controlled)



NOTES(WRITE CYCLE)

- 1. All write cycle timing is referenced from the last valid address to the first transition address.
- 2. A write occurs during the overlap of a low CS and WE. A write begins at the latest transition CS going low and WE going low; A write ends at the earliest transition CS going high or WE going high. tWP is measured from the beginning of write to the end of write.
- 3. tCW is measured from the later of CS going low to end of write.
- 4. tAS is measured from the address valid to the beginning of write.
- 5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as CS or WE going high.
- 6. If OE, CS and WE are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
- 7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
- 8. If CS goes low simultaneously with WE going or after WE going low, the outputs remain high impedance state.
- 9. Dout is the read data of the new address.
- 10. When \overline{CS} is low: I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

ĊŚ	WE	ŌĒ	Mode	I/O Pin	Supply Current
Н	Х	X*	Not Select	High-Z	ISB, ISB1
L	Н	Н	Output Disable	High-Z	lcc
L	Н	L	Read	Dout	lcc
L	L	Х	Write	DIN	lcc

^{*} NOTE : X means Don't Care.

256K x 16 Bit High-Speed CMOS Static RAM(3.3V Operating)

FEATURES

- Fast Access Time 10,12,15ns (Max.)
- · Low Power Dissipation

Standby (TTL) 40mA(Max.) (CMOS): 10mA(Max.)

1mA(Max.)- L-Ver.

Operating KM616V4002B/BL - 10 : 240mA(Max.)

KM616V4002B/BL - 12: 230mA(Max.)

KM616V4002B/BL - 15: 220mA(Max.)

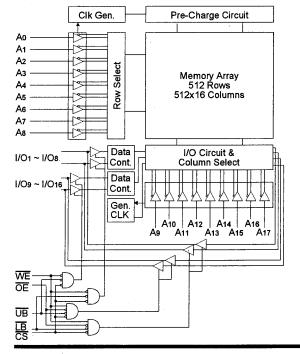
- Single 3.3V ± 0.3V Power Supply
- . TTL Compatible Inputs and Outputs
- Fully Static Operation
- No Clock or Refresh required
- · Three State Outputs
- Low Data Retention Voltage: 2V(Min.) L-Ver. Only
- · Center Power/Ground Pin Configuration
- Data Byte Control : LB : I/O1~ I/O8, UB : I/O9~ I/O16
- · Standard Pin Configuration

KM616V4002B/BLJ: 44-SOJ-400 KM616V4002B/BLT: 44-TSOP2-400F

ORDERING INFORMATION

KM616V4002B/BL -10/12/15	Commercial Temp.
KM616V4002B/BLI -10/12/15	Industrial Temp.

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The KM616V4002B/BL is a 4,194,304-bit high-speed Static Random Access Memory organized as 262,144 words by 16 bits. The KM616V4002B/BL uses 16 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. Also it allows that lower and upper byte access by data byte control (UB, LB). The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM616V4002B/BL is packaged in a 400mil 44-pin plastic SOJ or TSOP(II) forward.

PIN CONFIGURATION (Top View)

A0 1 A1 2 A2 3 A3 4 A4 5 CS 6 I/O1 7 I/O2 8 I/O3 9 I/O4 10 Vcc 11 Vss 12 I/O5 134 I/O7 15 I/O8 16 WE 17 A5 18 A6 21 A8 21 A9 22	0	SOJ/ TSOP2		A17 A16 A15 OE UB LB I/O16 I/O15 I/O14 I/O10 I/O9 N.C A14 A13 A12 A11

PIN FUNCTION

Pin Name	Pin Function
A0 - A17	Address Inputs
WE	Write Enable
cs	Chip Select
ŌĒ	Output Enable
LB	Lower-byte Control(I/O1~I/O8)
ŪB	Upper-byte Control(I/O9~I/O16)
I/O1 ~ I/O16	Data Inputs/Outputs
Vcc	Power(+3.3V)
Vss	Ground
N.C	No Connection



ABSOLUTE MAXIMUM RATINGS*

Param	eter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss		VIN, VOUT	-0.5 to 4.6	. V
Voltage on Vcc Supply Relative to Vss		Vcc -0.5 to 5.5		V
Power Dissipation		Po	1.0	W
Storage Temperature		Тѕтс	-65 to 150	°C
Operating Temperature	Commercial	TA	0 to 70	°C
	Industrial	TA	-40 to 85	°C

^{*} Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(TA = 0 to 70°C)

Parameter	Symbol	Min	Тур	Max	Unit
Supply Voltage	Vcc	3.0	3.3	3.6	V
Ground	Vss	0	0	0	V
Input Low Voltage	ViH	2.0	-	Vcc + 0.3**	V
Input Low Voltage	VIL	-0.3*	=	0.8	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

DC AND OPERATING CHARACTERISTICS(TA = 0 to 70 °C, Vcc= 3.3V ± 0.3V, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	lu .	VIN = Vss to Vcc	-2	2	μA	
Output Leakage Current	lLO	CS=VIH or OE=VIH or WE=VIL VOUT = Vss to Vcc		-2	2	μA
Operating Current	Icc	Min. Cycle, 100% Duty	10ns		240	mA
		CS=VIL, VIN = VIH or VIL, IOUT=0mA	12ns	-	230	
			15ns	-	220	
Standby Current	ISB	Min. Cycle, CS=Vін		-	. 40	mA
	ISB1	f=0MHz, CS ≥ Vcc-0.2V,	Normal	-	10	mΑ
		$VIN \ge VCC-0.2V$ or $VIN \le 0.2V$	L-Ver.	-	1	
Output Low Voltage Level	Vol	IoL=8mA		-	0.4	٧
Output High Voltage Level	Voн	IOH=-4mA		2.4	-	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

CAPACITANCE*(TA =25 °C, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	CI/O	Vi/o=0V	-	8	pF
Input Capacitance	Cin	VIN=0V	-	7	pF

^{*} NOTE: Capacitance is sampled and not 100% tested.



^{*} VIL(Min) = -2.0V a.c(Pulse Width≤8ns) for I ≤ 20mA

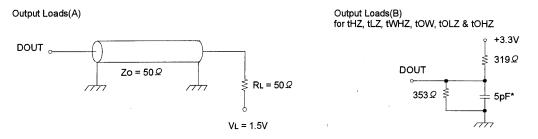
^{**} VIH(Max) = Vcc + 2.0V a.c (Pulse Width \le 8ns) for I \le 20mA

AC CHARACTERISTICS(TA = 0 to 70°C, Vcc =3.3V ± 0.3V, unless otherwise noted.)

TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3 ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

NOTE: Above test conditions are also applied at industrial temperature range.



* Including Scope and Jig Capacitance

READ CYCLE

		KM616V4002B/BL-10		KM616V4002B/BL-12		KM616V4002B/BL-15		Unit
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit
Read Cycle Time	tRC	10	-	12	-	15	-	ns
Address Access Time	tAA	-	10	-	12	-	15	ns
Chip Select to Output	tCO	-	10	-	12	-	15	ns
Output Enable to Valid Output	tOE	-	5	-	6	-	7	ns
UB, LB Access Time	tBA	-	5	-	6	· -	7	ns
Chip Enable to Low-Z Output	tLZ	3 ،	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
UB, LB Enable to Low-Z Output	tBLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	5	0	6	0	. 7	ns
Output Disable to High-Z Output	tOHZ	0	5	0	6	0	7	ns
UB, LB Disable to High-Z Output	tBHZ	0	5	0	6	0	7	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns

NOTE: Above parameters are also guaranteed at industrial temperature range.



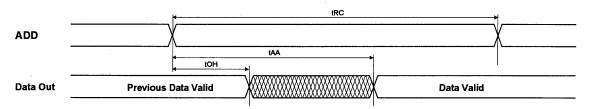
WRITE CYCLE

Parameter	Company	KM616V4002B/BL-10		KM616V4002B/BL-12		KM616V4002B/BL-15		
	Symbol	Min	Max	Min	Max	Min	Max	Unit
Write Cycle Time	tWC	10	-	12	-	15		ns
Chip Select to End of Write	tCW	7	-	8	-	10	-	ns
Address Set-up Time	tAS	0		0	-	0	-	ns
Address Valid to End of Write	tAW	7	-	8	-	10	-	ns
Write Pulse Width(OE High)	tWP	7	-	8	-	10	-	ns
Write Pulse Width(OE Low)	tWP1	10	-	12	-	15	-	ns
UB, LB Valid to End of Write	tBW	7	-	8 .	-	10	-	ns
Write Recovery Time	tWR	0	-	0	-	0 .	-	ns
Write to Output High-Z	tWHZ	0	5	0	6	0	7	ns
Data to Write Time Overlap	tDW	5	-	6	-	7	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

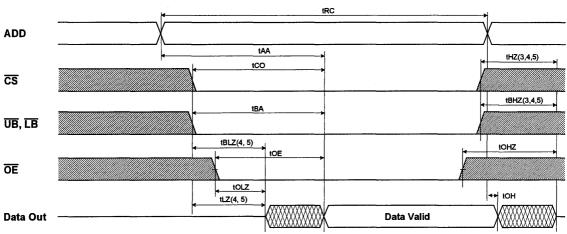
NOTE: Above parameters are also guaranteed at industrial temperature range.

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS} = \overline{OE} = \overline{UB} = \overline{LB} = VIL, \overline{WE} = VIH)$



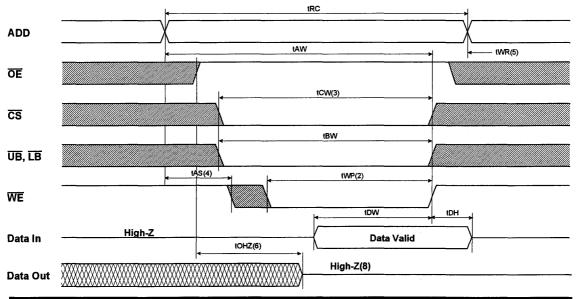
TIMING WAVE FORM OF READ CYCLE(2) (WE=VIH)



NOTES(READ CYCLE)

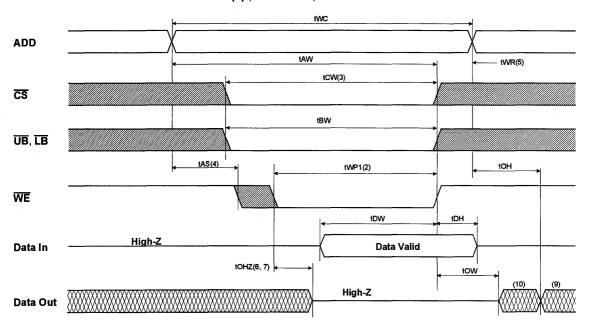
- 1. WE is high for read cycle.
- 2. All read cycle timing is referenced from the last valid address to the first transition address.
- 3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VoH or VoL Levels
- 4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
- 5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
- 6. Device is continuously selected with CS=VIL.
- 7. Address valid prior to coincident with CS transition low.
- 8 For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVE FORM OF WRITE CYCLE(1) (OE=Clock)

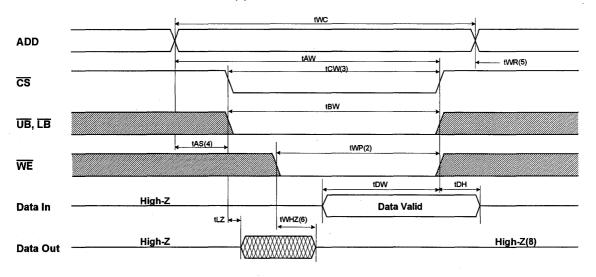




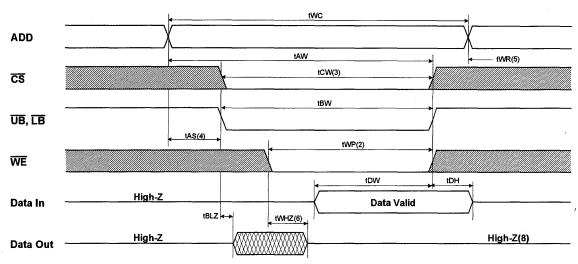




TIMING WAVE FORM OF WRITE CYCLE(3) (CS=Controlled)



TIMING WAVE FORM OF WRITE CYCLE(4) (UB, LB Controlled)



NOTES(WRITE CYCLE)

- 1. All write cycle timing is referenced from the last valid address to the first transition address.
- 2. A write occurs during the overlap of a low \overline{CS} , \overline{WE} , \overline{LB} and \overline{UB} . A write begins at the latest transition \overline{CS} going low and \overline{WE} going low; A write ends at the earliest transition \overline{CS} going high or \overline{WE} going high. tWP is measured from the beginning of write to the end of write.
- 3. tCW is measured from the later of $\overline{\text{CS}}$ going low to end of write.
- 4. tAS is measured from the address valid to the beginning of write.
- 5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as CS, or WE going high.
- 6. If \overline{OE} . \overline{CS} and \overline{WE} are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
- 7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
- 8. If CS goes low simultaneously with WE going or after WE going low, the outputs remain high impedance state.
- 9. Dout is the read data of the new address.
- 10. When $\overline{\text{CS}}$ is low: I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

CS	WE	ŌĒ	LB	UB	Mode	1/0	Pin	Supply Current
- 03	***	UL	LD	06	Wode	1/01~1/08	I/O9~I/O16	Supply Current
Н	Х	X*	Х	Х	Not Select	High-Z		ISB, ISB1
L	Н	Н	Х	X	Output Disable	High-Z	High-Z	lcc
L	Х	Х	Н	Н				
Ĺ	Н	L	L	Н	Read	Dout	High-Z	lcc
	•		Н	L		High-Z	Dout	
			L	L		Dout	Dout	
L	L	Х	L	Н	Write	DIN	High-Z	Icc
l			Н	L		High-Z	Din	
			L	L		DIN	DIN	

^{*} NOTE: X means Don't Care.

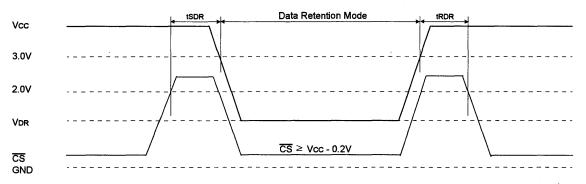


DATA RETENTION CHARACTERISTICS*(TA = 0°C to 70°C)

Parameter	Symbol	Test Condition	Min.	Тур.	Max.	Unit	
Vcc for Data Retention	VDR	CS ≥ Vcc - 0.2V	2.0	-	3.6	_ V	
Data Retention Current	IDR	$Vcc = 3.0V, \overline{CS} \ge Vcc - 0.2V$ $Vin \ge Vcc - 0.2V \text{ or } Vin \le 0.2V$	-	-	0.9	mA	
·		$ \begin{array}{c} \text{Vcc} = 2.0 \text{V, } \overline{\text{CS}} \geq \text{Vcc} - 0.2 \text{V} \\ \text{Vin} \geq \text{Vcc} - 0.2 \text{V or Vin} \leq 0.2 \text{V} \\ \end{array} $	-	-	0.7	1	
Data Retention Set-Up Time tSDR		See Data Retention	0_	-	-	ns	
Recovery Time	tRDR	Wave form(below)	5	-	-	ms	

NOTE: Above parameters are also guaranteed at industrial temperature range.

DATA RETENTION WAVE FORM(CS Controlled)





^{*} L-Ver only.

256K x 16 Bit High-Speed BiCMOS Static RAM(3.3V Operating)

FEATURES

- Fast Access Time 12,13,15 ns (Max.)
- Low Power Dissipation

Standby (TTL) : 60mA(Max.)

(CMOS): 30mA(Max.)

Operating KM616BV4002 - 12: 240mA(Max.)

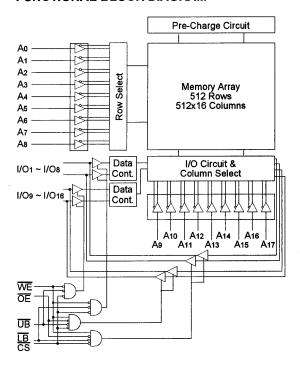
KM616BV4002 - 13: 235mA(Max.)

KM616BV4002 - 15: 230mA(Max.)

- . Single 3.3V+ 10%/-5% Power Supply
- . TTL Compatible Inputs and Outputs
- · Fully Static Operation
- No Clock or Refresh required
- · Three State Outputs
- · Center Power/Ground Pin Configuration
- Data Byte Control : LB : I/O1~ I/O8, UB : I/O9~ I/O16
- · Standard Pin Configuration

KM616BV4002J: 44-SOJ-400

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The KM616BV4002 is a 4,194,304-bit high-speed Static Random Access Memory organized as 262,144 words by 16 bits. The KM616BV4002 uses 16 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. Also it allows that lower and upper byte access by data byte control (UB, LB). The device is fabricated using SAMSUNG's advanced BicMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM616BV4002 is packaged in a 400mil 44-pin plastic SOJ.

PIN CONFIGURATION (Top View)

A0 1 A1 A2 A3 A4 B CS 6 I/O1 7 I/O2 9 I/O4 IIO Vcc III Vcs III V/O5 IIO I/O5 IIO I/O5 IIO IIO IIO IIO IIO IIO IIO IIO IIO I	0	soJ		A15 OE UB LB I/O16 I/O15 I/O14 I/O13 Vss Vcc I/O11 I/O9 I/O9 N.C A14 A13 A12
A9 22			23	
79 KK				, A10

PIN FUNCTION

Pin Name	Pin Function
A0 - A17	Address inputs
WE	Write Enable
CS	Chip Select
ŌĒ	Output Enable
LB	Lower-byte Control(I/O1~I/O8)
UB	Upper-byte Control(I/O9~I/O16)
I/O1 ~ I/O16	Data Inputs/Outputs
Vcc	Power(+3.3V)
Vss	Ground
N.C	No Connection



KM616BV4002 BICMOS SRAM

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	VIN, VOUT	-0.5 to 4.6	V
Voltage on Vcc Supply Relative to Vss	Vcc	-0.5 to 5.5	V
Power Dissipation	Po	1.0	W
Storage Temperature	Тѕтс	-65 to 150	°C
Operating Temperature	TA	0 to 70	°C

^{*} Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(TA = 0 to 70°C)

Parameter	Symbol	Min	Тур	Max	Unit
Supply Voltage	Vcc	3.13	3.3	3.6	V
Ground	Vss	0	0	0	٧.
Input Low Voltage	ViH	2.2	-	Vcc + 0.3**	V
Input Low Voltage	VIL	-0.3*	_	0.8	V

^{*} VIL(Min) = -2.0V a.c(Pulse Width \leq 10ns) for I \leq 20mÅ

DC AND OPERATING CHARACTERISTICS (TA = 0 to 70°C, Vcc= 3.3V+10%/-5%, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Max	Unit	
Input Leakage Current	lu	Vin = Vss to Vcc		-2	2	μA
Output Leakage Current	lLO	CS=ViH or OE=ViH or WE=ViL Vout = Vss to Vcc	-10	10	μA	
Operating Current Icc	Icc	Min. Cycle, 100% Duty	12ns	-	240	mA
		CS=VIL, VIN = VIH or VIL, IOUT=0mA	13ns	-	235	
			15ns	-	230	
Standby Current	ISB	Min. Cycle, CS=Viн		-	60	mA
	ISB1	f=0MHz, $\overline{CS} \ge Vcc-0.2V$, Vin $\ge Vcc-0.2V$ or Vin $\le 0.2V$		-	30	mA
Output Low Voltage Level	Vol	IoL=8mA		-	0.4	V
Output High Voltage Level	Von	IOH=-4mA		2.4	-	٧

CAPACITANCE*(TA =25°C, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	C1/0	VI/O=0V	-	8	pF
Input Capacitance	CIN	Vin=0V	-	7	pF

^{*} NOTE: Capacitance is sampled and not 100% tested.



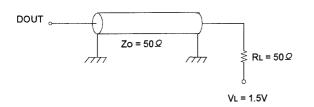
^{**} VIH(Max) = Vcc + 2.0V a.c (Pulse Width \le 10ns) for I \le 20mA

AC CHARACTERISTICS(TA = 0 to 70 °C, Vcc =3.3V +10%/-5%, unless otherwise noted.)

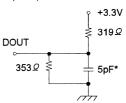
TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below





Output Loads(B) for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

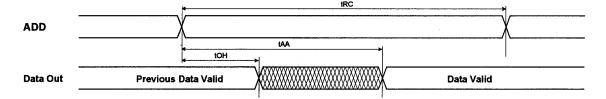
_		KM616BV4002-12		KM616BV4002-13		KM616BV4002 -15		1
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit
Read Cycle Time	tRC	12	-	13	-	15	-	ns
Address Access Time	tAA	-	12	-	13	-	15	ns
Chip Select to Output	tCO	•	12	-	13	-	15	ns
Output Enable to Valid Output	tOE	-	6	-	6	-	7	ns
UB, LB Access Time	tBA	-	6	-	6	-	7	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
UB, LB Enable to Low-Z Output	tBLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	6	0	6	0	7	ns
Output Disable to High-Z Output	tOHZ	0	6	0	6	0	7	ns
UB, LB Disable to High-Z Output	tBHZ	. 0	6	0	6	0	7	ns
Output Hold from Address Change	tOH	3	-	3	_	3	-	ns

WRITE CYCLE

Parameter		KM616BV4002-12		KM616BV4002-13		KM616BV4002-15		T
	Symbol -	Min	Max	Min	Max	Min	Max	- Unit
Write Cycle Time	tWC	12	-	13	-	15	-	ns
Chip Select to End of Write	tCW	9	-	10	-	10	-	ns
Address Set-up Time	tAS	0	-	0	-	0		ns
Address Valid to End of Write	tAW	9	-	10	-	10	-	ns
Write Pulse Width(OE High)	tWP	9	-	10	-	10	-	ns
Write Pulse Width(OE Low)	tWP1	10	-	11	-	12	-	ns
UB, LB Valid to End of Write	tBW	9	-	10	-	10	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	6.5	0	7	0	7.5	ns
Data to Write Time Overlap	tDW	7	-	7	-	8	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

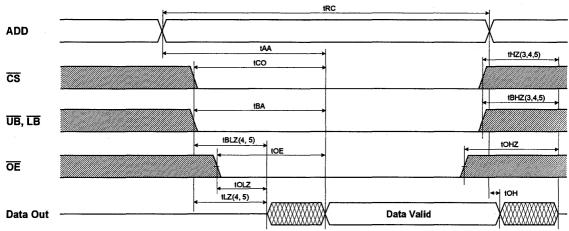
TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, CS=OE=UB=LB=VIL, WE=VIH)





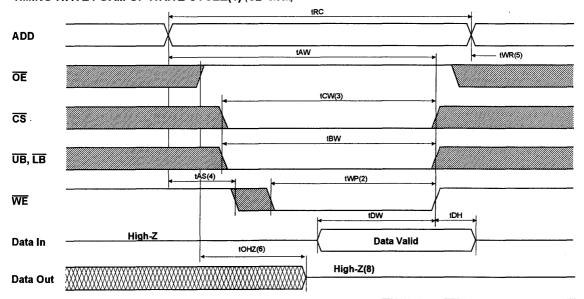
TIMING WAVE FORM OF READ CYCLE(2) (WE=VIH)



NOTES(READ CYCLE)

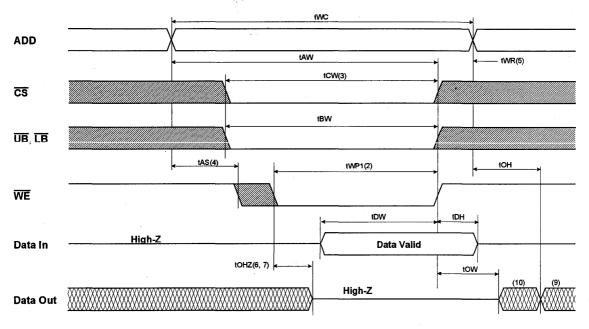
- 1. WE is high for read cycle.
- 2. All read cycle timing is referenced from the last valid address to the first transition address.
- 3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VoH or VoL Levels.
- 4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
- 5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
- 6. Device is continuously selected with CS=VIL.
- 7. Address valid prior to coincident with CS transition low.
- 8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVE FORM OF WRITE CYCLE(1) (OE=Clock)

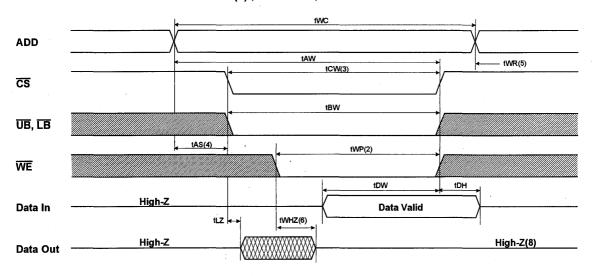




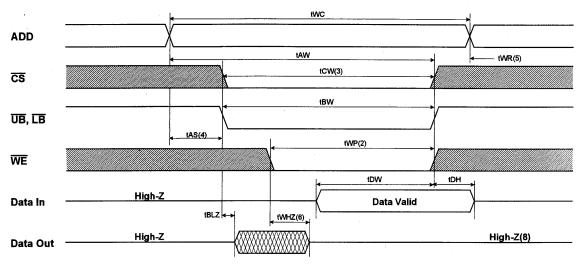
TIMING WAVE FORM OF WRITE CYCLE(2) (OE=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) (CS=Controlled)



TIMING WAVE FORM OF WRITE CYCLE(4) (UB, LB Controlled)



NOTES(WRITE CYCLE)

- 1. All write cycle timing is referenced from the last valid address to the first transition address.
- 2. A write occurs during the overlap of a low \overline{CS} , \overline{WE} , \overline{LB} and \overline{UB} . A write begins at the latest transition \overline{CS} going low and \overline{WE} going low; A write ends at the earliest transition \overline{CS} going high or \overline{WE} going high. tWP is measured from the beginning of write to the end of write.
- 3. tCW is measured from the later of CS going low to end of write.
- 4. tAS is measured from the address valid to the beginning of write.
- 5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as CS, or WE going high.
- 6. If OE. CS and WE are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
- 7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
- 8. If CS goes low simultaneously with WE going or after WE going low, the outputs remain high impedance state.
- 9. Dout is the read data of the new address.
- 10. When $\overline{\text{CS}}$ is low: I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

CS	WE	ŌĒ	ĽΒ	UB	Mode	1/0	Supply Current	
	711	OL.		- OL	mode	I/O1~I/O8	I/O9~I/O16	Supply Surrent
н	Х	X*	· X	X	Not Select	High-Z		ISB, ISB1
· L	Н	Н	Х	Х	Output Disable	High-Z	High-Z	Icc
L	Х	Х	н	Н				
L	н	L	L	H	Read	Dout	High-Z	Icc
			Н	L		High-Z	Dout	
			Ĺ	L		Dout	Dout	
L	L	Х	L	Н	Write	DIN	High-Z	Icc
			Н	L		High-Z	DIN	
			L	L		Din	Din	

^{*} NOTE : X means Don't Care.



256K x 16 Bit High-Speed CMOS Static RAM

FEATURES

- Fast Access Time 15, 17,20 ns (Max.)
- · Low Power Dissipation

Standby (TTL) : 50mA(Max.)

(CMOS): 10mA(Max.)

Operating KM616V4002A - 15: 200mA(Max.)

KM616V4002A - 17: 195mA(Max.)

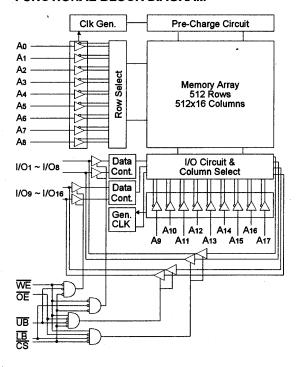
KM616V4002A - 20: 190mA(Max.)

- Single 3.3V ± 0.3V Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
 - No Clock or Refresh required
- · Three State Outputs
- · Center Power/Ground Pin Configuration
- Data Byte Control : LB : I/O1~ I/O8, UB : I/O9~ I/O16

. Standard Pin Configuration

KM616V4002AJ: 44-SOJ-400

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The KM616V4002A is a 4,194,304-bit high-speed Static Random Access Memory organized as 262,144 words by 16 bits. The KM616V4002A uses 16 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. Also it allows that lower and upper byte access by data byte control (UB, LB). The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM616V4002A is packaged in a 400mil 44-pin plastic SOJ.

PIN CONFIGURATION (Top View)

A0 1 2 A1 2 A2 3 A3 4 A4 5 6 B 1/O1 7 1/O2 B 1/O3 9 1/O4 10 1/O5 13 1/O6 14 1/O7 15 1/O8 16 WE 17 A5 18 A6 18 A7 20 A8 21 A9 222	0	soJ	37 36 35 34 33 32 31 30 29 28 27 26 25	A17 A16 A15 OE UB I/O16 I/O15 I/O14 I/O10 I/O9 N.C A14 A13 A12 A11 A10
			 l	

PIN FUNCTION

Pin Name	Pin Function
A0 - A17	Address Inputs
WE '	Write Enable
CS	Chip Select
ŌĒ	Output Enable
LB	Lower-byte Control(I/O1~I/O8)
UB	Upper-byte Control(I/O9~I/O16)
1/01 ~ 1/016	Data Inputs/Outputs
Vcc	Power(+3.3V)
Vss	Ground
N.C	No Connection



ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	VIN, VOUT	-0.5 to 4.6	V
Voltage on Vcc Supply Relative to Vss	Vcc	-0.5 to 4.6	٧
Power Dissipation	Pp	1.0	W
Storage Temperature	Тѕтҫ	-65 to 150	°C
Operating Temperature	TA	0 to 70	C

^{*} Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(TA = 0 to 70°C)

Parameter	Symbol	Min	Тур	Max	Unit
Supply Voltage	Vcc	3.0	3.3	3.6	V
Ground	Vss	0	, 0	0	V
Input Low Voltage	ViH	2.2	-	Vcc + 0.3**	V
Input Low Voltage	VIL	-0.3*	-	0.8	V

^{*} VIL(Min) = -2.0V a.c(Pulse Width≤10ns) for 1 ≤ 20mÅ

DC AND OPERATING CHARACTERISTICS(TA = 0 to 70 °C, Vcc= 3.3V ± 0.3V, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Max	Unit	
Input Leakage Current	ILI	VIN = Vss to Vcc	Vin = Vss to Vcc			
Output Leakage Current	lLO	CS=VIH or OE=VIH or WE=VIL VOUT = Vss to Vcc	-2	2	μA	
Operating Current Icc		Min. Cycle, 100% Duty	15ns	-	200	mA
		CS=VIL, VIN = VIH or VIL, IOUT=0mA	17ns	-	195	
		·	20ns	-	190	
Standby Current	ISB	Min. Cycle, CS=Vін		-	50	mA
	ISB1	f=0MHz, $\overline{CS} \ge Vcc-0.2V$, Vin $\ge Vcc-0.2V$ or Vin $\le 0.2V$		-	10	mA
Output Low Voltage Level	Vol	loL=8mA	-	0.4	٧	
Output High Voltage Level	Voн	IOH=-4mA		2.4	-	٧

CAPACITANCE*(TA =25°C, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	Ci/o	V1/0=0V	•	8	pF
Input Capacitance	CIN	VIN=0V	-	7	pF

^{*} NOTE: Capacitance is sampled and not 100% tested.

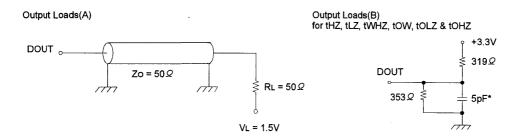


^{**} VIH(Max) = Vcc + 2.0V a.c (Pulse Width \leq 10ns) for I \leq 20mÅ

AC CHARACTERISTICS(TA = 0 to 70 °C, Vcc =3.3V \pm 0.3V, unless otherwise noted.)

TEST CONDITIONS

Parameter	Value
Input Pulse Levels	OV to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below



* Including Scope and Jig Capacitance

READ CYCLE

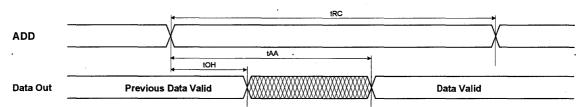
Parameter		KM616V4002A-15		KM616V4002A-17		KM616V4002A-20		T
	Symbol	Min	Max	Min	Max	Min	Max	- Unit
Read Cycle Time	tRC	15	-	17	-	20	-	ns
Address Access Time	tAA	-	15	-	17	-	20	ns
Chip Select to Output	tCO	-	15	-	17	-	20	ns
Output Enable to Valid Output	tOE	_	7	-	8	-	9	ns
UB, LB Access Time	tBA	-	7	-	8	- ,	9	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
UB, LB Enable to Low-Z Output	tBLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	7	0	8	0	9	ns
Output Disable to High-Z Output	tOHZ	0	7	0	8	0	9	ns
UB, LB Disable to High-Z Output	tBHZ	0	7	0	8	0	9	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns

WRITE CYCLE

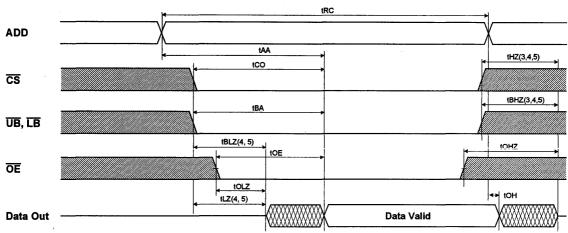
Parameter		KM616V4002A-15		KM616V4002A-17		KM616V4002A-20		T
	Symbol	Min	Max.	Min	Max	Min	Max	- Unit
Write Cycle Time	tWC	15	-	17	-	20	-	ns
Chip Select to End of Write	tCW	12	-	13	-	14	-	ns
Address Set-up Time	tAS	0	-	0.	-	0	-	ns
Address Valid to End of Write	tAW	12	-	13	-	14	-	ns
Write Pulse Width(OE High) tWP		12	-	13	-	14	-	ns
Write Pulse Width(OE Low) tWP1		15		17	-	20	-	ns
UB, LB Valid to End of Write	tBW	12	-	13	-	14	-	ns
Write Recovery Time	tWR	0	·-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	7	0	8	0	9	ns
Data to Write Time Overlap	tDW	8	-	9	-	10		ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{\text{CS}} = \overline{\text{OE}} = \overline{\text{UB}} = \overline{\text{LB}} = \text{VIL}$, $\overline{\text{WE}} = \text{VIH}$)



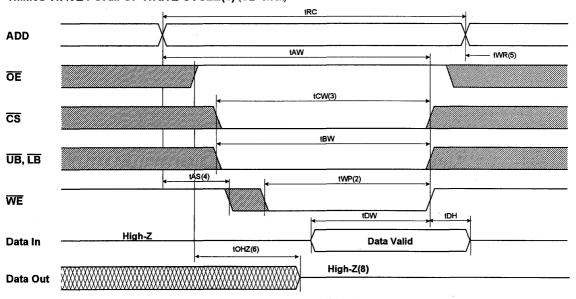
TIMING WAVE FORM OF READ CYCLE(2) (WE=VIH)



NOTES(READ CYCLE)

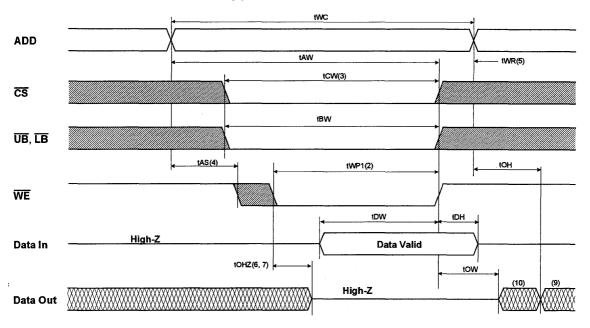
- 1. WE is high for read cycle.
- 2. All read cycle timing is referenced from the last valid address to the first transition address.
- 3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VoH or VoL Levels.
- 4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
- 5. Transition is measured ±200 mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
- 6. Device is continuously selected with CS=VIL.
- 7. Address valid prior to coincident with CS transition low.
- 8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVE FORM OF WRITE CYCLE(1) (OE=Clock)

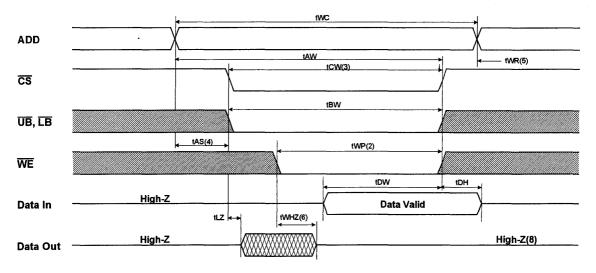




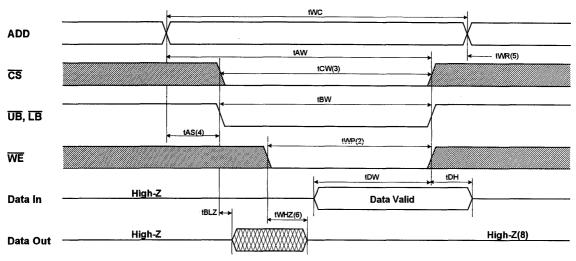
TIMING WAVE FORM OF WRITE CYCLE(2) (OE=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) (CS=Controlled)



TIMING WAVE FORM OF WRITE CYCLE(4) (UB, LB Controlled)



NOTES(WRITE CYCLE)

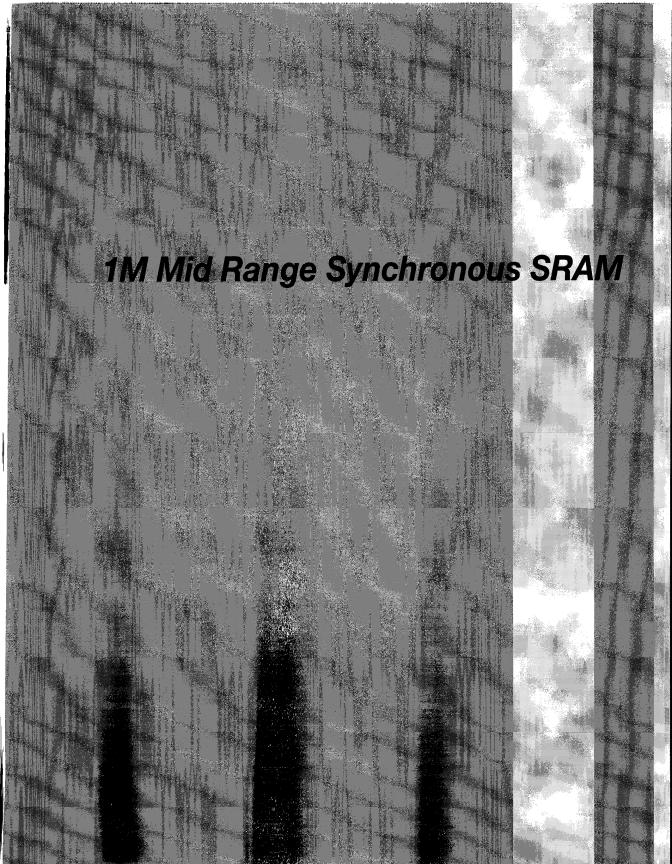
- 1. All write cycle timing is referenced from the last valid address to the first transition address.
- 2. A write occurs during the overlap of a low \overline{CS} , \overline{WE} , \overline{LB} and \overline{UB} . A write begins at the latest transition \overline{CS} going low and \overline{WE} going low; A write ends at the earliest transition \overline{CS} going high or \overline{WE} going high. tWP is measured from the beginning of write to the end of write.
- 3. tCW is measured from the later of CS going low to end of write.
- 4. tAS is measured from the address valid to the beginning of write.
- 5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as CS, or WE going high.
- 6. If \overline{OE} . \overline{CS} and \overline{WE} are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
- 7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
- 8. If CS goes low simultaneously with WE going or after WE going low, the outputs remain high impedance state.
- 9. Dout is the read data of the new address.
- 10. When \overline{CS} is low: I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

CS	WE	ŌĒ	CB	UB	Mode	1/0	I/O Pin		
- 00	WL	OL.	LD	- 00	Mode	I/O1~I/O8	1/09~1/016	Supply Current	
Н	Х	X*	Х	Х	Not Select	High-Z		ISB, ISB1	
L	Н	н	Х	X	Output Disable	High-Z	High-Z	Icc	
L	Х	Х	Н	H,			4		
L	Н	L	L	Н	Read	Dout	High-Z	lcc	
			Н	L		High-Z	Dout		
			L	L		Dout	Dout		
L	L	Х	L	Н	Write	DIN	High-Z	lcc	
			Н	L		High-Z	DIN		
			L	L		DIN	Din		

^{*} NOTE : X means Don't Care.





64Kx18-Bit Synchronous Burst SRAM FEATURES

- · Synchronous Operation.
- · On-Chip Address Counter.
- · Self-Timed Write Cycle.
- · On-Chip Address and Control Registers.
- Single 5V ± 5% Power Supply.
- · Byte Writable Function.
- · Asynchronous Output Enable Control.
- . ADSP, ADSC, ADV Burst Control Pins.
- . TTL-Level Three-State Output.
- · 3.3V I/O Compatible.
- 52-Pin PLCC Package.

FAST ACCESS TIMES

Parameter	Symbol	-8	-9	-10	-12	Unit
Cycle Time	tCYC	15	15	17	20	ns
Clock Access Time	tCD	8	9	10	12	ns
Output Enable Access Time	tOE	5	5	5	6	ns

GENERAL DESCRIPTION

The KM718B86 is a 1,179,648 bits Synchronous Static Random Access Memory designed to support 66MHz of Intel secondary caches.

It is organized as 65,536 words of 18 bits and integrates address and control registers, a 2-bit burst address counter and high output drive circuitry onto a single integrated circuit for reduced components count implementations of high performance cache RAM applications.

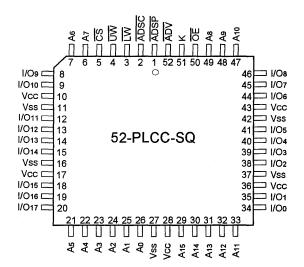
Write cycles are internally self-timed and synchronous.

The self-timed write feature eliminates complex off chip write pulse shaping logic, simplifying the cache design and further reducing the component count.

Burst cycle can be initiated with either the address status processor(ADSP) or address status cache controller(ADSC) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance(ADV) input.

The KM718B86 is implemented with SAMSUNG's high performance BiCMOS technology and is available in a 52pin PLCC package. Multiple power and ground pins are utilized to minimize ground bounce.

PIN CONFIGURATION (TOP VIEW)

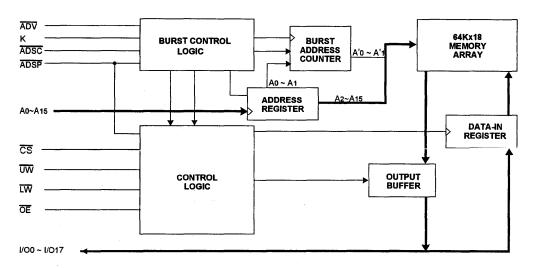


PIN NAME

Pin Name	Pin Function				
A0 - A15	Address Inputs				
К	Clock				
LW, UW	Write Enable				
ĊS	Chip Selects				
ŌĒ	Output Enable				
ĀDV	Burst Address Advance				
ADSP, ADSC	Address Status				
1/00~1/017	Data Inputs/Outputs				
Vcc +5V Power Supple					
Vss Ground					



LOGIC BLOCK DIAGRAM



FUNCTION DESCRIPTION

The KM718B86 is a synchronous SRAM designed to support the burst address accessing sequence of the Power microprocessor. All inputs(with the exception of \overline{OE}) are sampled on rising clock edges. The start and duration of the burst access is controlled by \overline{ADSP} and \overline{ADSC} . The accesses are enabled with the chip select signals and output enable. Wait states are inserted into the access with \overline{ADV} .

Read cycles are initiated with $\overline{\text{ADSP}}$ (regardless of $\overline{\text{LW}}$, $\overline{\text{UW}}$ and $\overline{\text{ADSC}}$) using the new external address clocked into the on-chip address register whenever $\overline{\text{ADSP}}$ is sample low, The chip selects are sampled active, and the output buffer is enabled with $\overline{\text{OE}}$, $\overline{\text{ADV}}$ is ignored on the clock edge that samples $\overline{\text{ADSP}}$ asserted, but is sampled on the next and subsequent clock edges. The address is increased internally for the next access of the burst when $\overline{\text{LW}}$, $\overline{\text{UW}}$ is sampled HIGH and $\overline{\text{ADV}}$ is sampled low.

Write cycles are performed by disabling the output buffers with \overline{OE} and asserting \overline{LW} , \overline{UW} , \overline{LW} , \overline{UW} is ignored on the clock edge that sampled ADSP low, but is sampled on the next and subsequent clock edges. The output buffers are disabled when \overline{LW} , \overline{UW} is sampled low (regardless of \overline{OE}). Data is clocked into the input register when \overline{LW} , \overline{UW} is sampled low. The address increases internally to the next address of burst, if both \overline{LW} , \overline{UW} and \overline{ADV} are sampled Low. Individual byte write cycles are performed sampling low only one byte write enable signals(\overline{LW} or \overline{LW}) and \overline{LW} controls \overline{LW} controls \overline{LW}) \overline{LW} and \overline{LW} controls \overline{LW} 00~ \overline{LW} 077.

Read or write cycles (depending on LW, LU)may also be initiated with ADSC, instead of ADSP. The differences between cycles initiated with ADSC and ADSP are as follows:

ADSP must be sampled high when ADSC is sampled low to initiate a cycle with ADSC. LW, UW is sampled on the same clock edge that sampled ADSC low(and ADSP high).

Addresses are generated for the burst accesses as shown below. The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion.

BURST SEQUENCE TABLE

(Interleaved Burst)

	Case 1		Case 2		Case 3		Case 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
1	0	1	0	0	1	1	1	0
. ↓	1	0	1	1	0	0	0	1
Fourth Address	1	1	1	0	0	1	0	0



TRUTH TABLES

SYNCHRONOUS TRUTH TABLE(See Notes 1 and 2)

ζŚ	ADSP	ADSC	ADV	LW/UW	К	Address Accessed	Operation
Н	L	X	Х	Х	1	N/A	Not Selected
Н	Х	L	Х	Х	1	N/A	Not Selected
L	L	X	Х	Х	1	External Address	Begin Burst Read Cycle
L	Н	L	Х	Н	1	External Address	Begin Burst Read Cycle
Х	Н	Н	L	Н	1	Next Address	Continue Burst Read Cycle
X	Н	H	Н	Н	1	Current Address	Suspend Burst Read Cycle
L	Н	L	Х	L	1	External Address	Begin Burst Write Cycle
Х	Н	Н	L	L	1	Next Address	Continue Burst Write Cycle
Х	Н	Н	Н	L	1	Current Address	Suspend Burst Write Cycle

NOTE1: X means "Don't Care".

NOTE2: The rising edge of clock is symbolized by 1.

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

ŌĒ	Operation
L	Read I/O0~I/O17
Н	Output High-Z
Х	Not Selected, Outputs High-Z

NOTE1: X means "Don't Care".

NOTE2 : For write cycles that following read cycles, the output buffers must be disabled with $\overline{\text{OE}}$, otherwise data bus contention

will occur.

ABSOLUTE MAXIMUM RATING*

Parameter	Symbol	Rating	Unit
Voltage on VDD Supply Relative to Vss	Vcc	-0.5 to 7.0	V
Voltage on Any Other Pin Relative to Vss	Vin	-0.5 to 7.0	V
Power Dissipation	PD	1.2	W
Storage Temperature	Тѕтс	-65 to 150	°C
Operating Temperature	TOPR	0 to 70	°C
Storage Temperature Range Under Bias	TBIAS	-10 to 85	င

*NOTE: Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.



OPERATING CONDITIONS(0 $^{\circ}$ C $^{<}$ TA $^{<}$ 70 $^{\circ}$ C)

Parameter	Symbol	Min	Тур.	Max	Unit
Supply Voltage	Vcc	4.75	5.0	5.25	V
Ground	Vss	0	0	0	V

CAPACITANCE*(TA = 25 °C, f = 1MHz)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	ÇIN	ViN=0V	-	5	pF
Output Capacitance	Соит	Vout=0V	-	8	pF

^{*}NOTE: Sampled not 100% tested.

TEST CONDITIONS(TA = 0 °C to 70 °C, VDD = 5V \pm 5%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time(Measured at 0.3V and 2.7V)	2ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1

DC ELECTRICAL CHARACTERISTICS(TA = 0 $^{\circ}$ to 70 $^{\circ}$, V_{DD} = 3.3V $^{\pm}$ 5%)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current(except ZZ)	lıL.	VDD = Max ; VIN = Vss to VCC	V _{DD} = Max ; V _{IN} = V _{SS} to V _{CC}			μA
Output Leakage Current	loL	Output Disabled	-2	+2	μA	
Operating Current	Icc	Vcc = Max	15ns	-	270	
		IOUT = 0mA	17ns	-	260	mA
		Cycle Time ≥ tCYC min	20ns	-	250	
Standby Current	ISB	Device deselected, louт = 0mA All Inputs= Viн and Vil., Viн ≥3	-	90	mA	
Output Low Voltage	VoL	IOL = 8.0mA		-	0.4	٧
Output High Voltage	Voн	Iон = -4.0mA		2.4	3.3	V
Input Low Voltage	VIL			-0.5*	0.8	V
Input High Voltage	VIH			2.2	Vcc+0.5	V

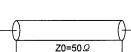
^{*} VIL(min) = -3.0(Pulse Width≤20ns)



AC TIMING CHARACTERISTICS (TA = 0 °C to 70 °C, Vcc = $5V\pm5\%$)

Parameter	Symbol	KM71	8B86-8	KM71	8B86-9	KM718	B86-10	KM718	B86-12	Unit
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	- Oint
Cycle Time	tCYC	15	-	15	-	17	-	20	-	ns
Clock Access Time	tCD	-	8	-	9	-	10	-	12	ns
Output Enable to Data Valid	tOE	-	5	-	5	-	5	-	6	ns
Clock High to Output Low-Z	tLZC	6	-	6	-	6	-	6	-	ns
Output Hold from Clock High	tOH	3	-	3	-	3	-	3	-	ns
Output Enable Low to Output Low-Z	tLZOE	0	-	0	-	0	-	0 .	-	ns
Output Enable High to Output High-Z	tHZOE	2	5	2	5	2	5	2	5	ns
Clock High to Output High-Z	tHZC	-	6	-	6	-	6	-	6	ns
Clock High Pulse Width	tCH	5	-	5	-	5	-	6	-	ns
Clock Low Pulse Width	tCL	5	-	5	-	5	-	6	-	ns
Address Setup to Clock High	tAS	2.5		2.5	-	2.5	-	2.5	-	ns
Address Status Setup to Clock High	tSS	2.5	-	2.5	-	2.5	-	2.5	-	ns
Data Setup to Clock High	tDS	2.5	-	2.5	-	2.5	-	2.5	-	ns
Write Setup to Clock High	tWS	2.5	-	2.5	-	2.5	-	2.5	-	ns
Address/Advance Setup to Clock	tADVS	2.5	-	2.5	-	2.5	-	2.5		ns
Chip Select Setup to Clock High	tCSS	2.5	-	2.5	-	2.5	-	2.5	-	ns
Address Hold from Clock High	tAH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Address Status Hold from Clock High	tSH	0.5	-	0.5	· -	0.5	-	0.5	-	ns
Data Hold from Clock High	tDH	0.5	-	0.5	-	0.5	-	0.5		ns
Write Hold from Clock High	tWH	0.5	-	0.5		0.5	-	0.5	-	ns
Address Advance Hold from Clock	tADVH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	tCSH	0.5	-	0.5	-	0.5	-	0.5	-	ns

NOTE: 1. All address inputs must meet the specified setup and hold times for all rising clock edges whenever ADSC and/or ADSP is sampled low and CS is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected. Both chip selects must be active whenever ADSC or ADSP is sampled low in order for this device to remain enabled.

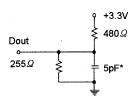


Output Load(A)

* Including Scope and Jig Capacitance

Fig. 1

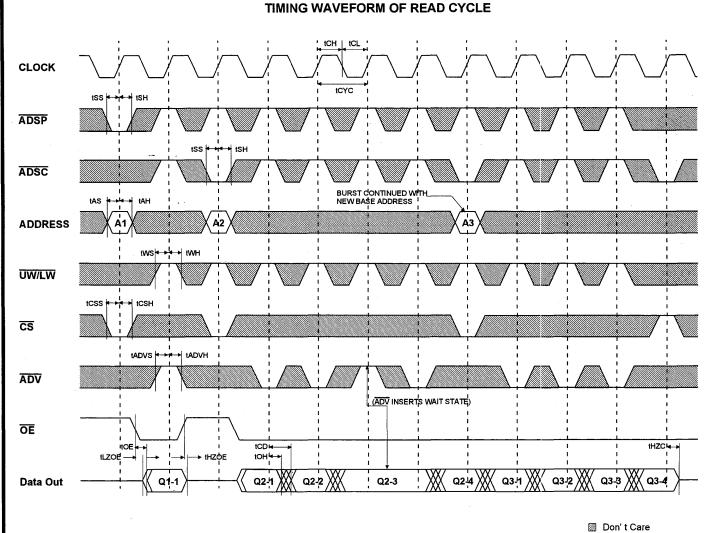
Output Load(B) (for tLZC, tLZOE, tHZOE& tHZC)





Dout

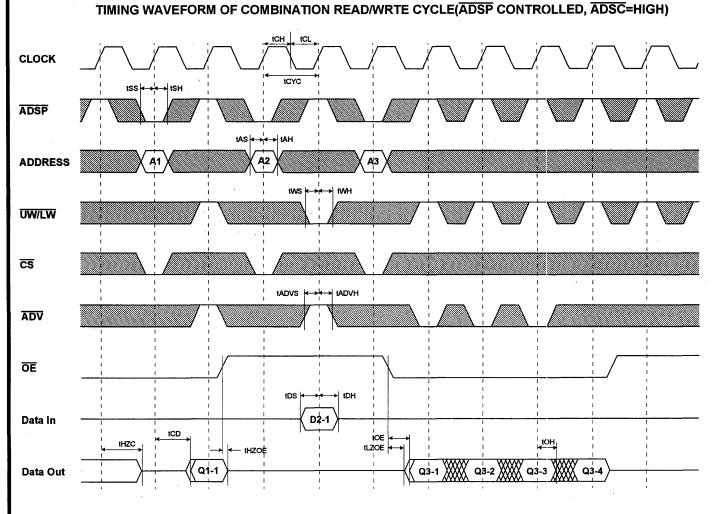
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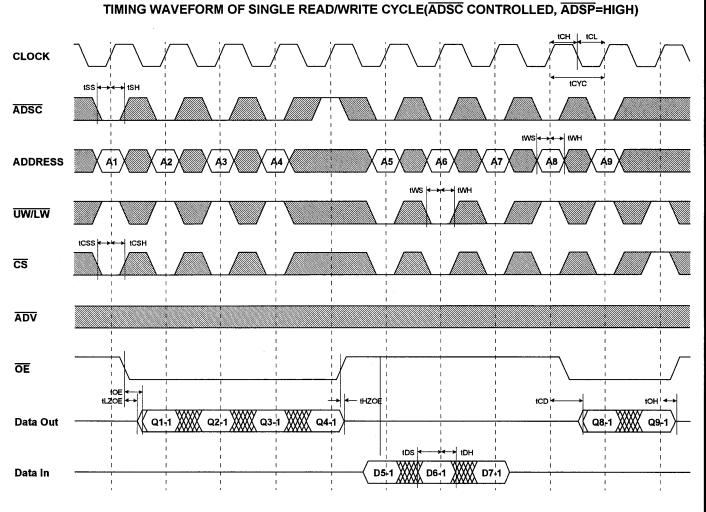


SAMSUNG

ELECTRONICS

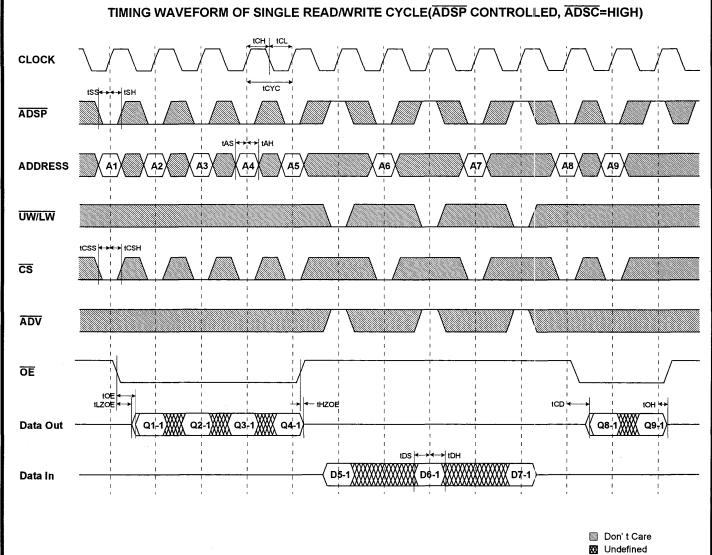


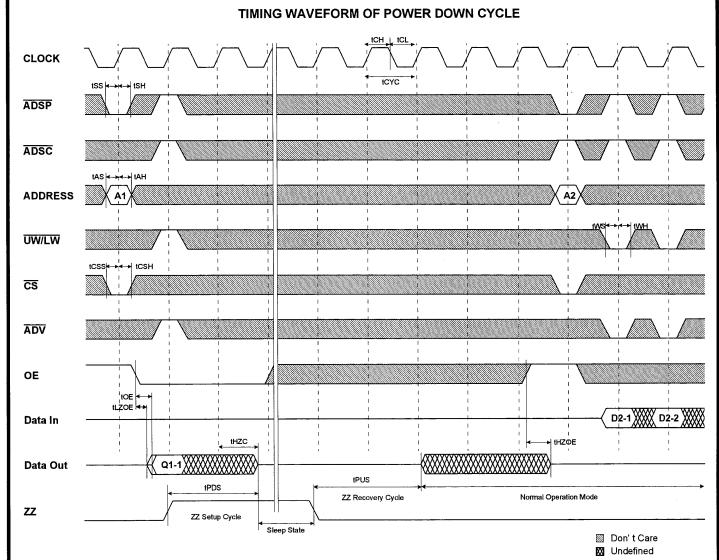




Don't Care

☑ Undefined





64Kx18-Bit Synchronous Burst SRAM FEATURES

- . Synchronous Operation.
- On-Chip Address Counter.
- · Self-Timed Write Cycle.
- · On-Chip Address and Control Registers.
- Single 5V ± 5% Power Supply.
- . Byte Writable Function.
- Asynchronous Output Enable Control.
- ADSP, ADSC, ADV Burst Control Pins.
- . TTL-Level Three-State Output.
- . 3.3V I/O Compatible.
- 52-Pin PLCC Package.

FAST ACCESS TIMES

Parameter	Symbol	-8	-9	-10	-11	Unit
Cycle Time	tCYC	15	15	17	20	ns
Clock Access Time	tCD	8	9	10	11	ns
Output Enable Access Time	tOE	5	5	5	6	ns

GENERAL DESCRIPTION

The KM718B90 is a 1,179,648 bits Synchronous Static Random Access Memory designed to support 66MHz of Intel secondary caches.

It is organized as 65,536 words of 18 bits. And it integrates address and control registers, a 2-bit burst address counter and high output drive circuitry onto a single integrated circuit for reduced components counts implementation of high performance cache RAM applications.

Write cycles are internally self-timed and synchronous.

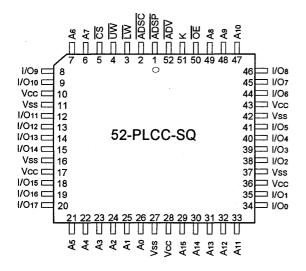
The self-timed write feature eliminates complex off chip write pulse shaping logic, simplifying the cache design and further reducing the component count.

Burst cycle can be initiated with either the address status processor(ADSP) or address status cache controller(ADSC) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance(ADV) input.

ZZ pin controls Power Down State and reduces Stand-by current regardless of CLK.

The KM718B90 is implemented with SAMSUNG's high performance BiCMOS technology and is available in a 52pin PLCC package. Multiple power and ground pins are utilized to minimize ground bounce.

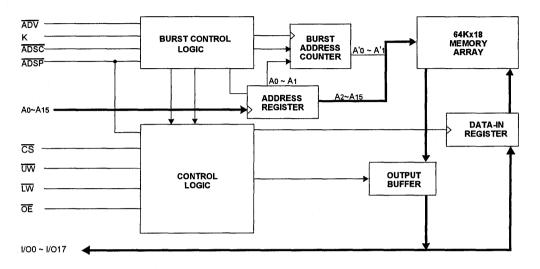
PIN CONFIGURATION(TOP VIEW)



PIN NAME

Pin Name	Pin Function
A0 - A15	Address Inputs
К	Clock
LW, UW	Write Enable
ĊS	Chip Selects
ŌĒ	Output Enable
ADV	Burst Address Advance
ADSP, ADSC	Address Status
1/00~1/017	Data Inputs/Outputs
Vcc	+5V Power Supple
Vss	Ground

LOGIC BLOCK DIAGRAM



FUNCTION DESCRIPTION

The KM718B90 is a synchronous SRAM designed to support the burst address accessing sequence of the Power microprocessor. All inputs(with the exception of \overline{OE}) are sampled on rising clock edges. The start and duration of the burst access is controlled by \overline{ADSP} and \overline{ADSC} . The accesses are enabled with the chip select signals and output enable. Wait states are inserted into the access with \overline{ADV} .

Read cycles are initiated with \overline{ADSP} (regardless of \overline{LW} , \overline{UW} and \overline{ADSC}) using the new external address clocked into the on-chip address register whenever \overline{ADSP} is sample low, The chip selects are sampled active, and the output buffer is enabled with \overline{OE} , \overline{ADSP} is ignored on the clock edge that samples \overline{ADSP} asserted, but is sampled on the next and subsequent clock edges. The address is increased internally for the next access of the burst when \overline{LW} , \overline{UW} is sampled HIGH and \overline{ADV} is sampled low.

Write cycles are performed by disabling the output buffers with \overline{OE} and asserting \overline{LW} , \overline{UW} , \overline{LW} , \overline{UW} is ignored on the clock edge that sampled ADSP low, but is sampled on the next and subsequent clock edges. The output buffers are disabled when \overline{LW} , \overline{UW} is sampled low (regardless of \overline{OE}). Data is clocked into the input register when \overline{LW} , \overline{UW} is sampled low. The address increases internally to the next address of burst, if both \overline{LW} , \overline{UW} and \overline{ADV} are sampled Low. Individual byte write cycles are performed sampling low only one byte write enable signals(\overline{LW} or \overline{LU})and \overline{LW} controls $I/O9 \sim I/O7$ and \overline{UW} controls $I/O8 \sim I/O17$.

Read or write cycles (depending on \overline{LW}, \overline{LU})may also be initiated with \overline{ADSC}, instead of \overline{ADSP}. The differences between cycles initiated with \overline{ADSC} and \overline{ADSP} are as follows;

ADSP must be sampled high when ADSC is sampled low to initiate a cycle with ADSC.

LW, UW is sampled on the same clock edge that sampled ADSC low(and ADSP high).

Addresses are generated for the burst accesses as shown below. The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion.

BURST SEQUENCE TABLE

(Linear Burst)

	Case 1		Case 2		Cas	ie 3	Case 4	
	A1	A0	A1	A0	A1	A0	A1	
First Address	0	0	0	1	1	0	1	1
	0	1	1	0	1	1	0	0
1	1	0	1	1	0	0	0	1
Fourth Address	1	1	0	0	0	1	1	0



TRUTH TABLES

SYNCHRONOUS TRUTH TABLE(See Notes 1 and 2)

CS	ADSP	ADSC	ADV	LW/UW	К	Address Accessed	Operation
Н	L	Х	Х	Х	1	N/A	Not Selected
Н	Х	L	Х	Х	1	N/A	Not Selected
L	L	Х	Х	Х	1	External Address	Begin Burst Read Cycle
Ļ	Н	L	Х	Н	1	External Address	Begin Burst Read Cycle
X	Н	H	L	Н	1	Next Address	Continue Burst Read Cycle
Х	Н	Н	Н	Н	1	Current Address	Suspend Burst Read Cycle
L	Н	L	Х	Н	1	External Address	Begin Burst Write Cycle
Х	Н	Н	L	L	1	Next Address	Continue Burst Write Cycle
Х	Н	Н	Н	L	1	Current Address	Suspend Burst Write Cycle

NOTE1: X means "Don't Care".

NOTE2: The rising edge of clock is symbolized by 1.

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

ŌĒ	Operation
L	Read I/O0~I/O17
Н	Output High-Z
Х	Not Selected, Outputs High-Z

NOTE1: X means "Don't Care".

NOTE2: For write cycles that follow read cycles, the output buffers must be disabled with $\overline{\text{OE}}$, otherwise data bus contention will occur

ABSOLUTE MAXIMUM RATING*

Parameter	Symbol	Rating	Unit
Voltage on Vcc Supply Relative to Vss	Vcc	-0.5 to 7.0	V
Voltage on Any Other Pin Relative to Vss	Vin	-0.5 to 7.0	V
Power Dissipation	PD	1.2	W
Storage Temperature	Тѕтс	-65 to 150	°C
Operating Temperature	Topr	0 to 70	°C
Storage Temperature Range Under Bias	TBIAS	-10 to 85	°C

*NOTE: Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.



OPERATING CONDITIONS(0 $^{\circ}$ C $^{<}$ TA $^{<}$ 70 $^{\circ}$ C)

Parameter	Symbol	Min	Тур.	Max	Unit
Supply Voltage	Vcc	4.75	5.0	5.25	V
Ground	Vss	0	0	0	V

CAPACITANCE*(TA = 25°C, f = 1MHz)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	CIN	Vin=0V	-	5	pF
Output Capacitance	Соит	Vout=0V	-	8	pF

^{*}NOTE: Sampled not 100% tested.

TEST CONDITIONS(TA = 0° to 70° , VDD = $5V \pm 5\%$, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time(Measured at 0.3V and 2.7V)	2ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1

DC ELECTRICAL CHARACTERISTICS(TA = 0°C to 70°C, VDD = 5V±5%)

Parameter	Symbol	Test Conditions	Min	Max	Unit	
Input Leakage Current	lıL	VDD = Max ; VIN = Vss to Vcc		-2	+2	μA
Output Leakage Current	loL	Output Disabled	-2	+2	μA	
Operating Current	lcc	Vcc = Max	15ns	- 270		
		iout = 0mA	17ns	-	260	mΑ
		Cycle Time ≥ tCYC min	20ns	-	250	
Standby Current	IsB	Device deselected, louт = 0mA All Inputs= Viн and Vil, Viн ≥ 3	-	90	mA	
Output Low Voltage	Vol	IoL = 8.0mA		-	0.4	V
Output High Voltage	Voн	Iон = -4.0mA		2.4	3.3	V
Input Low Voltage	VIL			-0.5*	0.8	V
Input High Voltage	ViH			2.2	Vcc+5.5	V

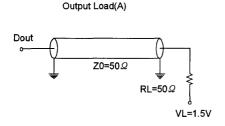
^{*} VIL(min) = -3.0(Pulse Width≤20ns)



AC TIMING CHARACTERISTICS	(TA = 0° to 70° , Vcc = $5V \pm 5\%$)
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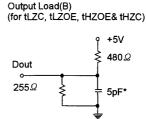
Parameter	Symbol	Symbol KM718B90-8		KM718B90-9		KM718B90-10		KM718B90-11		Unit
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unn
Cycle Time	tCYC	15	-	15	-	17	-	20	-	ns
Clock Access Time	tCD	-	8	-	9	-	10	-	11	ns
Output Enable to Data Valid	tOE	-	5	-	5	-	5	-	6	ns
Clock High to Output Low-Z	tLZC	6	-	6	-	6	-	6	-	ns
Output Hold from Clock High	tOH	3	-	3	-	3	-	3	-	ns
Output Enable Low to Output Low-Z	tLZOE	0	-	0	_	0	-	0	-	ns
Output Enable High to Output High-Z	tHZOE	2	5	2	5	2	5	2	5	ns
Clock High to Output High-Z	tHZC	-	6	-	6	-	6	-	6	ns
Clock High Pulse Width	tCH	5	-	5	-	5	-	6	-	ns
Clock Low Pulse Width	tCL	5	-	5	-	5	-	6	-	ns
Address Setup to Clock High	tAS	2.5	-	2.5	-	2.5	-	2.5	-	ns
Address Status Setup to Clock High	tSS	2.5	-	2.5	-	2.5	-	2.5	-	ns
Data Setup to Clock High	tDS	2.5	-	2.5	-	2.5	-	2.5	-	ns
Write Setup to Clock High	tWS	2.5	-	2.5	-	2.5	-	2.5	-	ns
Address/Advance Setup to Clock	tADVS	2.5	-	2.5		2.5	-	2.5	_	ns
Chip Select Setup to Clock High	tCSS	2.5	-	2.5	-	2.5	-	2.5	-	ns
Address Hold from Clock High	tAH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Address Status Hold from Clock High	tSH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Data Hold from Clock High	tDH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Write Hold from Clock High	tWH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Address Advance Hold from Clock	tADVH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	tCSH	0.5	-	0.5	-	0.5	-	0.5	-	ns

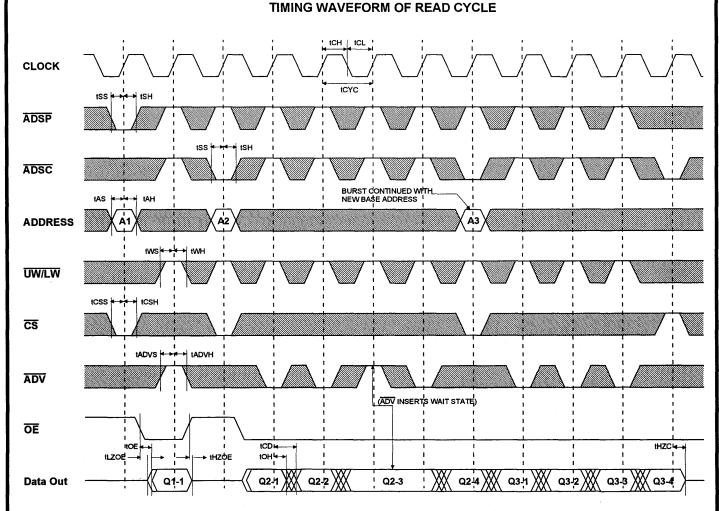
NOTE: 1. All address inputs must meet the specified setup and hold times for all rising clock edges whenever ADSC and/or ADSP is sampled low and CS is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected. Both chip selects must be active whenever ADSC or ADSP is sampled low in order for this device to remain enabled.



^{*} Including Scope and Jig Capacitance

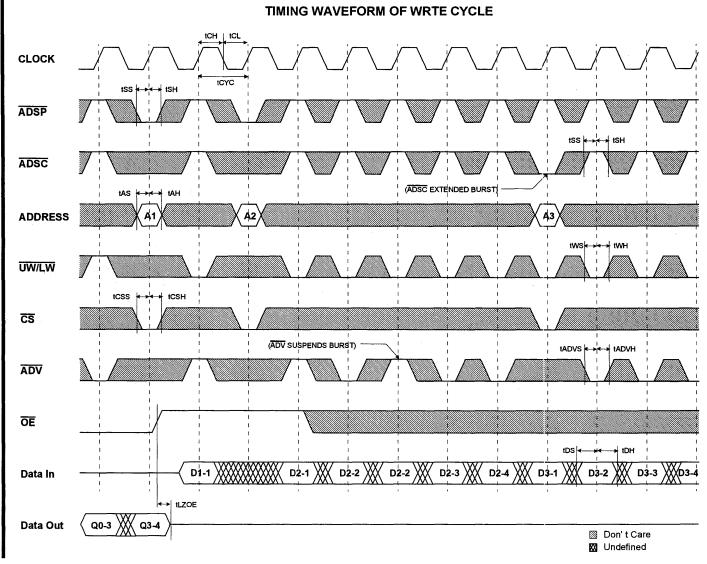
Fig. 1

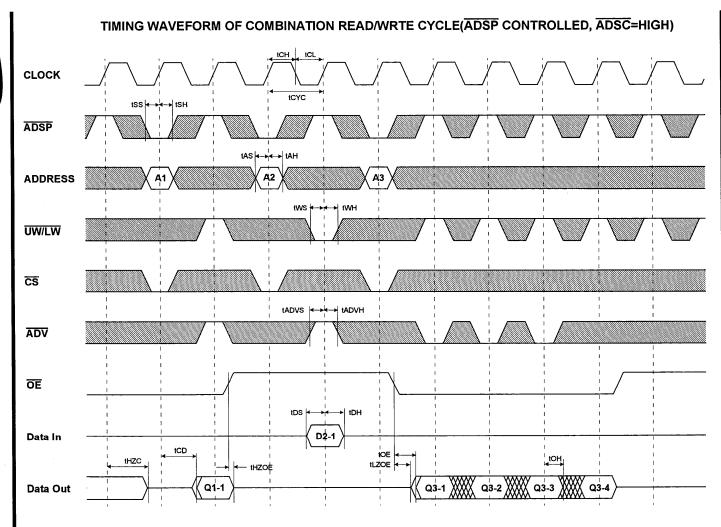




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SUMSUNG

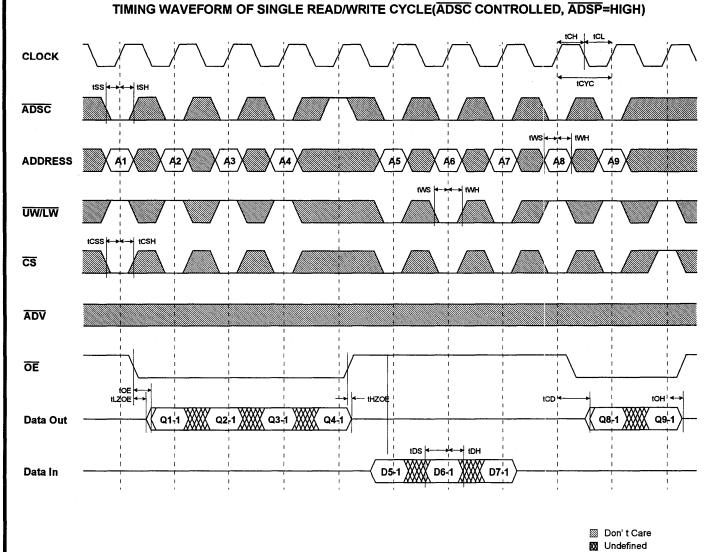




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SUMSUNG

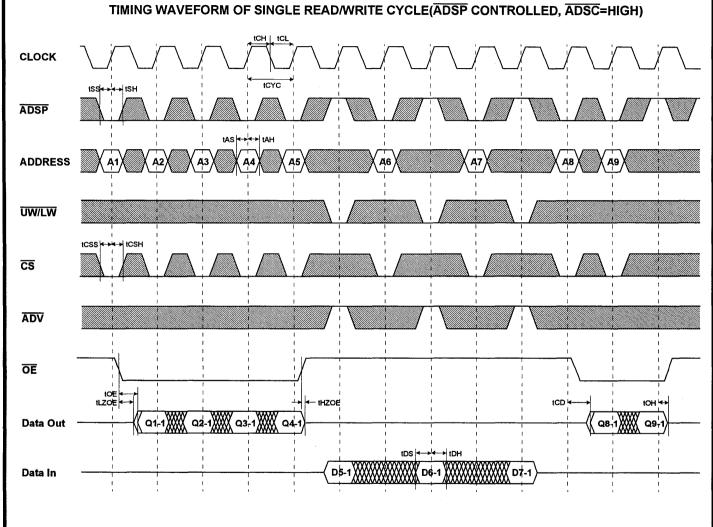
ELECTRONICS



SAMSUNG

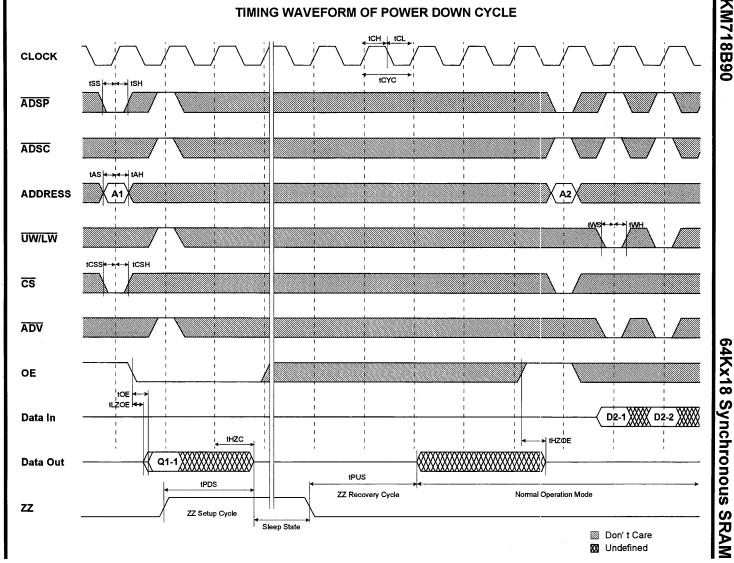
ELECTRONICS

SAMSUNG



Don't Care

⊠ Undefined



64Kx18-Bit Synchronous Burst SRAM FEATURES

- · Synchronous Operation.
- · On-Chip Address Counter.
- Self-Timed Write Cycle.
- · On-Chip Address and Control Registers.
- Single $3.3V \pm 5\%$ Power Supply.
- · Byte Writable Function.
- · Asynchronous Output Enable Control.
- . ADSP, ADSC, ADV Burst Control Pins.
- . TTL-Level Three-State Output.
- . 5V I/O Compatible.
- 52-Pin PLCC Package.

FAST ACCESS TIMES

Parameter	Symbol	-9	-10	-12	Unit
Cycle Time	tCYC	15	17	20	ns
Clock Access Time	tCD	9	10	12	ns
Output Enable Access Time	tOE	5	5	6	ns

GENERAL DESCRIPTION

The KM718BV87 is a 1,179,648 bits Synchronous Static Random Access Memory designed to support zero wait state performance with advanced i486/Pentium address pipelining.

When CS is high, ADSP is blocked to control singles.

It is organized as 65,536 words of 18 bits and integrates address and control registers, a 2-bit burst address counter and high output drive circuitry onto a single integrated circuit for reduced components count implementations of high performance cache RAM applications.

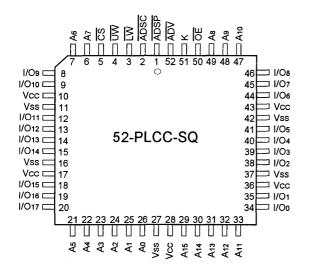
Write cycles are internally self-timed and synchronous.

The self-timed write feature eliminates complex off chip write pulse shaping logic, simplifying the cache design and further reducing the component count.

Burst cycle can be initiated with either the address status processor(\overline{ADSP}) or address status cache controller(\overline{ADSC}) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance(\overline{ADV}) input.

The KM718BV87 is implemented with SAMSUNG's high performance BiCMOS technology and is available in a 52pin PLCC package. Multiple power and ground pins are utilized to minimize ground bounce.

PIN CONFIGURATION (TOP VIEW)

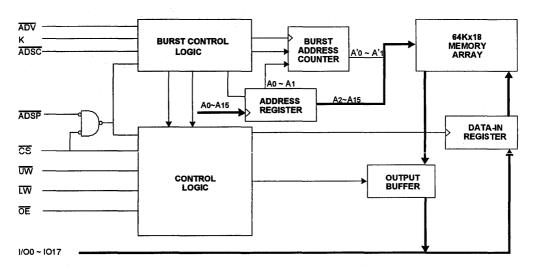


PIN NAME

Pin Name	Pin Function
Ao - A15	Address Inputs
K	Clock
LW, UW	Write Enable
CS	Chip Selects
ŌĒ	Output Enable
ADV	Burst Address Advance
ADSP, ADSC	Address Status
I/O0~I/O17	Data Inputs/Outputs
Vcc	+3.3V Power Supple
Vss	Ground



LOGIC BLOCK DIAGRAM



FUNCTION DESCRIPTION

The KM718BV87 is a synchronous SRAM designed to support the burst address accessing sequence of the i486/586 microprocessor. All inputs(with the exception of \overline{OE}) are sampled on rising clock edges. The start and duration of the burst access is controlled by \overline{ADSC} and \overline{ADSP} . The accesses are enabled with the chip select signals and output enable. Wait states are inserted into the access with \overline{ADV} .

Read cycles are initiated with \overline{ADSP} (regardless of \overline{LW} , \overline{UW} and \overline{ADSC}) using the new external address clocked into the on-chip address register whenever \overline{ADSP} is sample low, The chip selects are sampled active, and the output buffer is enabled with \overline{OE} , \overline{ADV} is ignored on the clock edge that samples \overline{ADSP} asserted, but is sampled on the next and subsequent clock edges. The address is increased internally for the next access of the burst when \overline{LW} , \overline{UW} is sampled HIGH and \overline{ADV} is sampled low. And \overline{ADSP} is blocked to control signals by disabling \overline{CS} .

Write cycles are performed by disabling the output buffers with \overline{OE} and asserting \overline{LW} , \overline{UW} , \overline{LW} , \overline{UW} is ignored on the clock edge that samples \overline{ADSP} low, but is sampled on the next and subsequent clock edges. The output buffers are disabled when \overline{LW} , \overline{UW} is sampled low (regardless of \overline{OE}). Data is clocked into the data input register when \overline{LW} , \overline{UW} is sampled low. The address increases internally to the next address of burst, if both \overline{LW} , \overline{UW} and \overline{ADV} are sampled Low. Individual byte write cycles are performed by sampling low only one byte write enable signals(\overline{LW} or \overline{LU}) and \overline{LW} controls |I/OP| onto |I/OP|. Onto |I/OP|. The differences between cycles initiated

Read or write cycles (depending on LW, LU)may also be initiated with ADSC, instead of ADSP. The differences between cycles initiated with ADSP and ADSC are as follows;

ADSP must be sampled high when ADSC is sampled low to initiate a cycle with ADSC.

LW, UW is sampled on the same clock edge that sampled ADSC loe(and ADSP high).

Addresses are generated for the burst access as shown below, The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion.

BURST SEQUENCE TABLE

(Interleaved Burst)

	Ca	Case 1		Case 2		Case 3		Case 4	
	A1	A0	A1	A0	A1	A0	A1	A0	
First Address	0	0	0	1	1	0	1	1	
	0	1	0	0	1	1	1	0	
↓	1	0	1	1	0	0	0	1	
Fourth Address	1	1	1	0	0	1	0	0	



TRUTH TABLES

SYNCHRONOUS TRUTH TABLE(See Notes 1 and 2)

ĊŚ	ADSP	ADSC	ADV	LW/UW	к	Address Accessed	Operation
L	L	Х	Х	X	1	External Address	Begin Burst Read Cycle
L	Н	L	Х	L	1	External Address	Begin Burst Write Cycle
L	Н	L	Х	H	1	External Address	Begin Burst Read Cycle
Н	X	L	Х	X	1	N/A	Not Selected
Н	X	Н	L	L	1	Next Address	Continue Burst Write Cycle
Н	X	Н	L	Н	1	Next Address	Continue Burst Read Cycle
Н	X	Н	Н	L	1	Current Address	Suspend Burst Write Cycle
Н	Х	Н	Н	Н	1	Current Address	Suspend Burst Read Cycle
X	Н	Н	L	L	1	Next Address	Continue Burst Write Cycle
Х	Н	Н	L	Н	1	Next Address	Continue Burst Read Cycle
Х	Н	Н	Н	L	1	Current Address	Suspend Burst Write Cycle
Х	Н	Н	Н	Н	1	Current Address	Suspend Burst Read Cycle

NOTE1: X means "Don't Care".

NOTE2: The rising edge of clock is symbolized by 1.

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

ŌĒ	Operation
L	Read I/O0~I/O17
Н	Output High-Z
Х	Not Selected, Outputs High-Z

NOTE1: X means "Don't Care".

 $\textbf{NOTE2}: \ \ \text{For write cycles that following read cycles, the output buffers must be disabled with } \overline{\text{OE}}, \ \text{otherwise data bus contention}$

will occur.

ABSOLUTE MAXIMUM RATING*

Parameter	Symbol	Rating	Unit
Voltage on VDD Supply Relative to Vss	Vcc	-0.3 to 4.6	V
Voltage on Any Other Pin Relative to Vss	Vin	-0.3 to 6.0	V
Power Dissipation	Po	1.2	W
Storage Temperature	Тѕтс	-65 to 150	°C
Operating Temperature	Topr	0 to 70	°C
Storage Temperature Range Under Bias	TBIAS	-10 to 85	°C

*NOTE: Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.



OPERATING CONDITIONS($0^{\circ} \le TA \le 70^{\circ}$)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	Vcc	3.13	3.3	3.47	V
Ground	Vss	0	0	0	V

CAPACITANCE*(TA = 25 °C, f = 1MHz)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	Cin	VIN=0V	-	5	pF
Output Capacitance	Соит	∨ουτ=0∨		8	pF

^{*}NOTE: Sampled not 100% tested.

TEST CONDITIONS(TA = 0° C to 70° C, VDD = $3.3V \pm 5\%$, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time(Measured at 0.3V and 2.7V)	2ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1

DC ELECTRICAL CHARACTERISTICS(TA = 0°C to 70°C, VDD = 3.3V±5%)

Parameter	Symbol	Test Conditions	Min	Max	Unit	
Input Leakage Current(except ZZ)	İIL	VDD = Max ; VIN = Vss to Vcc	VDD = Max ; VIN = Vss to Vcc Output Disabled			μA
Output Leakage Current	loL	Output Disabled				μA
Operating Current	lcc	Vcc = Max	15ns	-	270	
	1	IOUT = 0mA	17ns	-	260	mA
		Cycle Time ≥ tCYC min	20ns	-	250	
Standby Current	ISB	CS = VIH, IOUT = 0mA, Min Cyc	ele	-	80	mA
Output Low Voltage	Vol	IoL = 8.0mA		-	0.4	V
Output High Voltage	Voн	Iон = -4.0mA		2.4	-	V
Input Low Voltage	VIL			-0.5*	0.8	V
Input High Voltage	ViH			2.2	+5.5	V

^{*} VIL(min) = -3.0(Pulse Width \le 20ns)

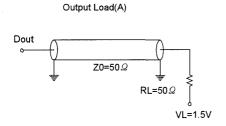


AC TIMING CHARACTERISTICS (TA = 0° to 70°, Vcc = 5V±5%)

7	S	KM718	BV87-9	KM718	KM718BV87-10		BV87-12	Unit
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit
Cycle Time	tCYC	15	-	17	-	20	-	ns
Clock Access Time	tCD	-	9	-	10	-	12	ns
Output Enable to Data Valid	tOE	-	5	-	5	-	6	ns
Clock High to Output Low-Z	tLZC	6	-	6	-	6	-	ns
Output Hold from Clock High	tOH	3	-	3	-	3	-	ns
Output Enable Low to Output Low-Z	tLZOE	0	-	0	-	0	-	ns
Output Enable High to Output High-Z	tHZOE	2	5	2	5	2	5	ns
Clock High to Output High-Z	tHZC	-	6	-	6	-	6	ns
Clock High Pulse Width	tCH	5	-	5	-	6	-	ns
Clock Low Pulse Width	tCL	5	-	5	-	6	-	ns
Address Setup to Clock High	tAS	2.5	-	2.5	-	2.5	-	ns
Address Status Setup to Clock High	tss	2.5	-	2.5	-	2.5	-	ns
Data Setup to Clock High	tDS	2.5	-	2.5	-	2.5	-	ns
Write Setup to Clock High	tWS	2.5	-	2.5	-	2.5	-	ns
Address/Advance Setup to Clock High	tADVS	2.5	-	2.5	-	2.5	-	ns
Chip Select Setup to Clock High	tCSS	2.5	-	2.5	-	2.5	-	ns
Address Hold from Clock High	tAH	0.5	-	0.5	-	0.5	-	ns
Address Status Hold from Clock High	tSH	0.5	-	0.5	-	0.5	-	ns
Data Hold from Clock High	tDH	0.5	-	0.5	-	0.5	-	ns
Write Hold from Clock High	tWH	0.5	-	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	tADVH	0.5	-	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	tCSH	0.5	-	0.5	-	0.5	-	ns

NOTE: 1. All address inputs must meet the specified setup and hold times for all rising clock edges whenever ADSC and/or ADSP is sampled low and CS is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected. Both chip selects must be active whenever ADSC or ADSP is sampled low in order for this device to remain enabled.

Fig. 1

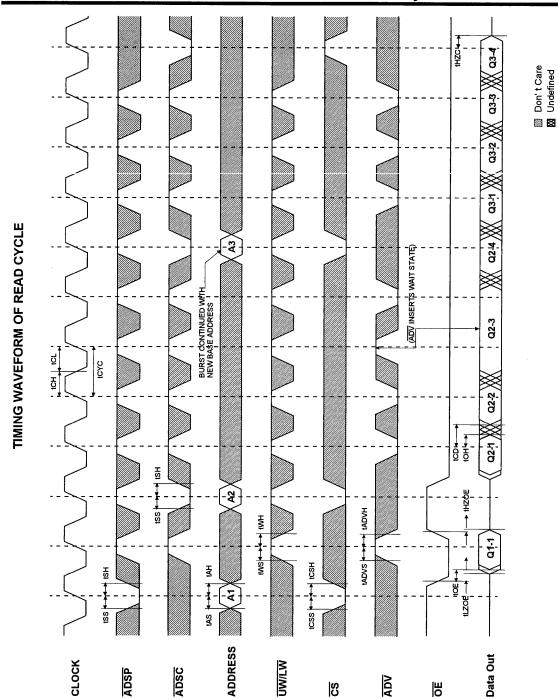


* Including Scope and Jig Capacitance

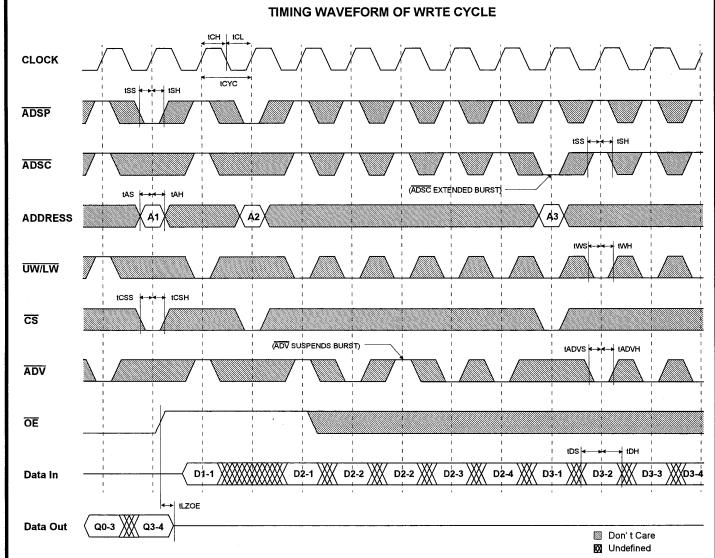
Dout \$ 319\to 2 \$ 353\to 2 \$ 5pF*

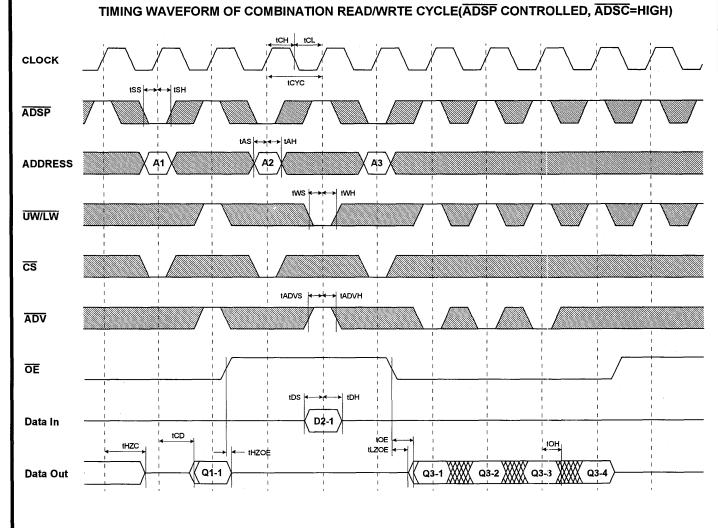
Output Load(B) (for tLZC, tLZOE, tHZOE& tHZC)

+3.3V



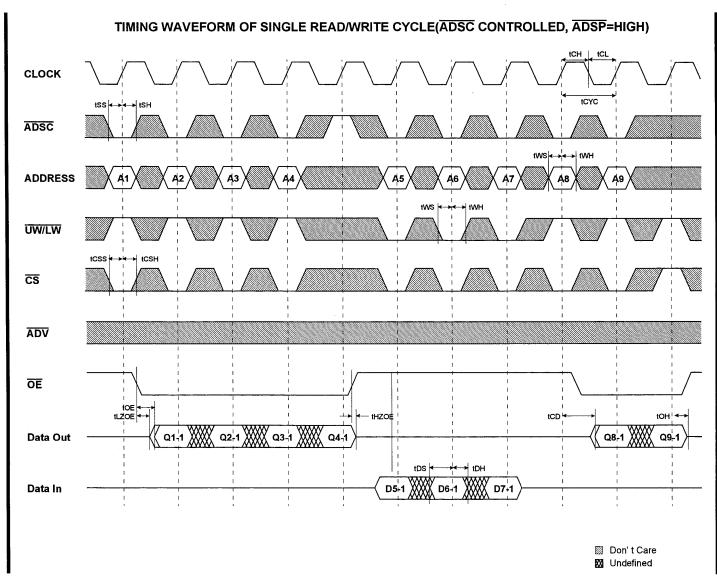




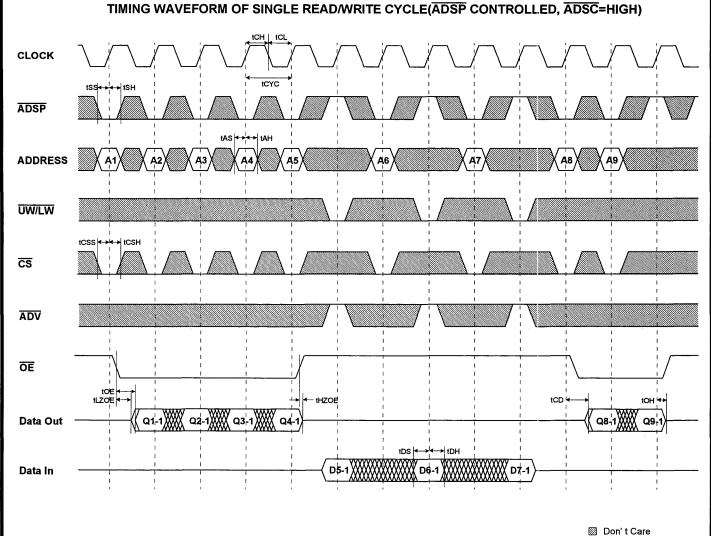


Don't Care

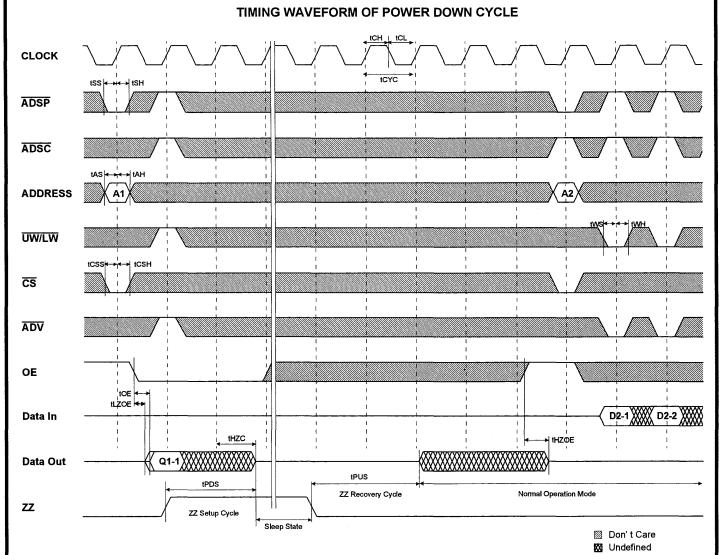
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32Kx32-Bit Synchronous Pipelined Burst SRAM

FEATURES

- · Synchronous Operation.
- . 2 Stage Pipelined operation with 4 Burst.
- · On-Chip Address Counter.
- · Self-Timed Write Cycle.
- · On-Chip Address and Control Registers.
- . Single 3.3V-5%/+10% Power Supply
- 5V Tolerant Inputs except I/O Pins
- . Byte Writable Function.
- . Global Write Enable Controls a full bus-width write.
- · Power Down State via ZZ Signal.
- LBO Pin allows a choice of either a interleaved burst or a linear burst.
- Three Chip Enables for simple depth expansion with No Data Contention; 2 cycle Enable, 1 cycle Disable.
- · Asynchronous Output Enable Control.
- . ADSP, ADSC, ADV Burst Control Pins.
- . TTL-Level Three-State Output.
- . 100-Pin QFP/TQFP Package

FAST ACCESS TIMES

Parameter	Symbol	-13	-15	-17	Unit
Cycle Time	tCYC	13	15	17	ns
Clock Access Time	tCD	7	8	9	ns
Output Enable Access Time	tOE	6	7	8	ns

GENERAL DESCRIPTION

The KM732V589/L is a 1,048,576-bit Synchronous Static Random Access Memory designed for high performance second level cache of i486/Pentium and Power PC based System.

It is organized as 32K words of 32 bits and integrates address and control registers, a 2-bit burst address counter and added some new functions for high performance cache RAM applications: $\overline{\text{GW}}$, $\overline{\text{BW}}$, $\overline{\text{LBO}}$, ZZ.

Write cycles are internally self-timed and synchronous.

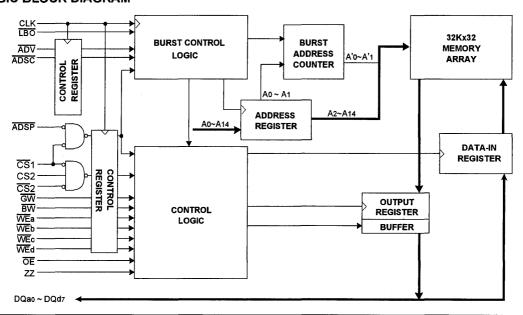
Full bus-width write is done by $\overline{\text{GW}}$, and each byte write is performed by the combination of $\overline{\text{WEx}}$ and $\overline{\text{BW}}$ when $\overline{\text{GW}}$ is high. And with $\overline{\text{CS1}}$ high, $\overline{\text{ADSP}}$ disable to support address pipelining. Burst cycle can be initiated with either the address status processor($\overline{\text{ADSP}}$) or address status cache controller($\overline{\text{ADSC}}$) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance($\overline{\text{ADV}}$) input.

LBO pin is DC operated and determines burst sequence(linear or interleaved).

ZZ pin controls Power Down State and reduces Stand-by current regardless of CLK.

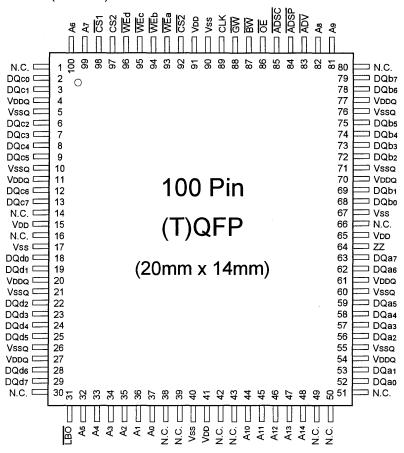
The KM732V589/L is fabricated using SAMSUNG's high performance CMOS technology and is available in a 100pin QFP/TQFP package. Multiple power and ground pins are utilized to minimize ground bounce.

LOGIC BLOCK DIAGRAM





PIN CONFIGURATION (TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A14	Address Inputs	32,33,34,35,36,37,	VDD	Power Supply(+3.3V)	15,41,65,91
	·	44,45,46,47,48,81,	Vss	Ground	17,40,67,90
		82,99,100	N.C.	No Connect	1,14,16,30,38,39,42,43,
ADV	Burst Address Advance	83			49,50,51,66,80
ADSP	Address Status Processor	84	DQa0 ~ a7	Data Inputs/Outputs	52,53,56,57,58,59,62,63
ADSC	Address Status Controller	85	DQb0 ~ b7		68,69,72,73,74,75,78,79
CLK	Clock	89	DQc0 ~ c7		2,3,6,7,8,9,12,13
CS1	Chip Select	98	DQd0 ~ d7		18,19,22,23,24,25,28,29
CS2	Chip Select	97	ĺ	1	
CS2	Chip Select	92	VDDQ	Output Power Supply	4,11,20,27,54,61,70,77
WEx	Byte Write Inputs	93,94,95,96		(+3.3V)	
ŌĒ	Output Enable	86	Vssq	Output Ground	5,10,21,26,55,60,71,76
GW	Global Write Enable	88	1		
BW	Byte Write Enable	87			
ZZ	Power Down Input	64			
LBO	Burst Mode Control	31	1		

FUNCTION DESCRIPTION

The KM732V589/L is a synchronous SRAM designed to support the burst address accessing sequence of the P6 and Power PC based microprocessor. All inputs (with the exception of \overline{OE} and ZZ) are sampled on rising clock edges. The start and duration of the burst access is controlled by $\overline{CS1}$, \overline{ADSC} , \overline{ADSC} and \overline{ADV} . The accesses are enabled with the chip select signals and output enabled signals. Wait states are inserted into the access with \overline{ADV} .

When ZZ is pulled high, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM normally operates after 2 cycles of wake up time.

Read cycles are initiated with $\overline{\text{ADSP}}$ (regardless of $\overline{\text{WEx}}$ and $\overline{\text{ADSC}}$) using the new external address clocked into the on-chip address register whenever $\overline{\text{ADSP}}$ is sampled low, the chip selects are sampled active, and the output buffer is enabled with $\overline{\text{OE}}$. In read operation the data of cell array accessed by the current address, registered in the Data-out registers by the positive edge of CLK, are carried to the Data-out buffer by the next positive edge of CLK. The data, registered in the Data-out buffer, are projected to the output pins. $\overline{\text{ADV}}$ is ignored on the clock edge that samples $\overline{\text{ADSP}}$ asserted, but is sampled on the subsequent clock edges. The address increases intornally for the next access of the burst when $\overline{\text{WEx}}$ are sampled High and $\overline{\text{ADV}}$ is sampled low. And $\overline{\text{ADSP}}$ is blocked to control signals by disabling $\overline{\text{CS}1}$.

All byte write is done by \overline{GW} (regardless of \overline{BW} and \overline{WEx} .), and each byte write is performed by the combination of \overline{BW} and \overline{WEx} when \overline{GW} is high.

Write cycles are performed by disabling the output buffers with \overline{OE} and asserting \overline{WEx} . \overline{WEx} are ignored on the clock edge that samples \overline{ADSP} low, but are sampled on the subsequent clock edges. The output buffers are disabled when \overline{WEx} are sampled Low(regardless of \overline{OE}). Data is clocked into the data input register when \overline{WEx} sampled Low. The address increases internally to the next address of burst, if both \overline{WEx} and \overline{ADV} are sampled Low. Individual byte write cycles are performed by any one or more byte write enable signals(\overline{WEa} , \overline{WEb} , \overline{WEc} or \overline{WEd}) sampled low. The \overline{WEa} controls DQao ~ DQa7, \overline{WEb} controls DQbo ~ DQb7, \overline{WEc} controls DQco ~ DQc7, and \overline{WEd} controls DQdo ~ DQd7. Read or write cycle may also be initiated with \overline{ADSC} , instead of \overline{ADSP} . The differences between cycles initiated with \overline{ADSC} and \overline{ADSP} as are follows;

ADSP must be sampled high when ADSC is sampled low to initiate a cycle with ADSC. WEx are sampled on the same clock edge that sampled ADSC low(and ADSP high).

Addresses are generated for the burst access as shown below, The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the LBO pin. When this pin is Low, linear burst sequence is selected. When this pin is High, Interleaved burst sequence is selected.

BURST SEQUENCE TABLE

(Interleaved Burst)

LBO PIN HIGH	Cas	Case 1		Case 2		se 3	Case 4		
LBOFIN	A1	A0	A1	A0	A1	A0	A1	A0	
First Address	0	0	0	1	1	0	1	. 1	
	0	1	0	0	1	1	1	0	
1	1	0	1	1	0	0	0	1	
Fourth Address	1	1	1	0	0	1	0	0	

(Linear Burst)

LBO PIN LOW	Cas	se 1	Cas	e 2	Cas	se 3	Ca	se 4
LBO FIN LOW	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
	0	1	1	0	1	1	0	0
	1	0	1	1	0	0	0	1 1
Fourth Address	1	1	0	0	0	1	1	0

NOTE: 1. LBO pin must be tied to High or Low, and Floating State must not be allowed.



TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

CS1	CS2	CS2	ADSP	ADSC	ADV	WRITE	CLK	Address Accessed	Operation
Н	Х	Х	Х	L	X	Х	1	N/A	Not Selected
L	L	Х	L	X	Х	Х	1	N/A	Not Selected
L	Х	Н	L	Х	Х	Х	1	N/A	Not Selected
L	L	Х	Х	٦	Х	Х	1	N/A	Not Selected
L	Х	Н	Х	L	Х	Х		N/A	Not Selected
L	Н	L	L	Х	Х	Х	1	External Address	Begin Burst Read Cycle
L	Н	L	Н	L	Х	L	1	External Address	Begin Burst Write Cycle
L	Н	L	Н	Г	X	Н	1	External Address	Begin Burst Read Cycle
Х	Х	Х	Н	Н	L	Н	1	Next Address	Continue Burst Read Cycle
Н	Х	Х	Х	H	L	Н	1	Next Address	Continue Burst Read Cycle
X	Х	Х	Н	Н	L	L	1	Next Address	Continue Burst Write Cycle
Н	Х	Х	Х	Н	L	L	1	Next Address	Continue Burst Write Cycle
Х	Х	Х	Н	Н	Н	Н	1	Current Address	Suspend Burst Read Cycle
Н	Х	Х	X	Н	Η	Н	1	Current Address	Suspend Burst Read Cycle
Х	Х	X	Н	. Н	Н	L	1	Current Address	Suspend Burst Write Cycle
Н	Х	Х	Х	Н	Н	L	1	Current Address	Suspend Burst Write Cycle

NOTE: 1. X means "Don't Care".

- 2. The rising edge of clock is symbolized by \uparrow .
- WRITE = L means Write operation in WRITE TRUTH TABLE.
 WRITE = H means Read operation in WRITE TRUTH TABLE.
- 4. Operation finally depends on status of asynchronous input pins(ZZ and \overline{OE}).

WRITE TRUTH TABLE

GW	BW	WEa	WEb	WEc	WEd	Operation
Н	Н	X	Х	Х	X	READ
Н	L	Н	Н	Н	Н	READ
Н	L	L	Н	Н	Н	WRITE BYTE a
Н	L	Н	L	Н	Н	WRITE BYTE b
Н	L	Н	Н	L	L	WRITE BYTE c and d
Н	L	L	L	L	L	WRITE ALL BYTEs
L	X	Х	Х	Х	Х	WRITE ALL BYTEs

NOTE: 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(\uparrow).

ASYNCHRONOUS TRUTH TABLE

(See Notes 1 and 2):

(000 110100 1			
Operation	ZZ	ŌĒ	I/O Status
Sleep Mode	Н	Х	High-Z
Read	L	L	DQ
Read	L	Н	High-Z
Write	L	X	Din, High-Z
Deselected	L	Х	High-Z

NOTE

- 1. X means "Don't Care".
- 2. ZZ pin is pulled down internally
- 3. For write cycles that following read cycles, the output buffers must be disabled with $\overline{\text{OE}}$, otherwise data bus contention will occur.
- 4. Sleep Mode means power down state of which stand-by current does not depend on cycle time.
- 5. Deselected means power down state of which stand-by current depends on cycle time.

PASS-THROUGH TRUTH TABLE

Previous Cycle		Presen	Present Cycle					
Operation WRITI		Operation	CS1	WRITE	ŌĒ	Next Cycle		
Write Cycle, All bytes Address=An-1, Data=Dn-1		Initiate Read Cycle Address=An Data=Qn-1 for all bytes	L	н	L	Read Cycle Data=Qn		
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=Qn-1 for all bytes H H L		No carryover from previous cycle				
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=High-Z	Н	н	Н	No carryover from previous cycle		
Write Cycle, One byte Address=An-1, Data=Dn-1	One L	Initiate Read Cycle Address=An Data=Qn-1 for one byte	L	Н	L	Read Cycle Data=Qn		
Write Cycle, One byte Address=An-1, Data=Dn-1	One L	No new cycle Data=Qn-1 for one byte	н	н	L	No carryover from previous cycle		

NOTE: 1. This operation makes written data immediately available at output during a read cycle preceded by a write cycle.

2. WEx means WEa ~ WEd.

ABSOLUTE MAXIMUM RATING*

Parameter	Symbol	Rating	Unit
Voltage on VDD Supply Relative to Vss	VDD	-0.3 to 4.6	V
Voltage on VDDQ Supply Relative to Vss	VDDQ	VDD	V
Voltage on Input Pin Relative to Vss	Vin	-0.3 to 6.0	٧
Voltage on I/O Pin Relative to Vss	Vio	-0.3 to VDDQ + 0.5	٧
Power Dissipation	Po	1.2	W
Storage Temperature	Тѕтс	-65 to 150	င
Operating Temperature	Topr	0 to 70	င
Storage Temperature Range Under Bias	TBIAS	-10 to 85	°C

*NOTE: Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS (0°C ≤ TA ≤ 70°C)

Parameter	Symbol	Min	Тур.	Max	Unit
Cumply Valtage	VDD	3.13	3.3	3.6	V
Supply Voltage	VDDQ	3.13	3.3	3.6	٧
Ground	Vss	0	0	0	V

CAPACITANCE*(TA = 25°C, f = 1MHz)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	CIN	VIN=0V	-	5	pF
Output Capacitance	Соит	Vout=0V	-	7	pF

*NOTE: Sampled not 100% tested.



DC ELECTRICAL CHARACTERISTICS

 $(VDD=3.3V-5\%+10\%, TA=0^{\circ}C to 70^{\circ}C)$

Parameter	Symbol	Test Conditions	Min	Max	Unit	
Input Leakage Current	lıL	VDD = Vss to VDD; VIN = Vss to VDD		-2	+2	μA
Output Leakage Current	loL	Output Disabled, Vout = Vss to VDDQ	-2	+2	μA	
Operating Current	Icc	Device Selected, IouT = 0mA, ZZ≤VIL,	-13	-	200	mA
		All Inputs = VIL or VIH	-15	-	180	
		Cycle Time ≥ tCYC min	-17	-	160	
Standby Current	ISB	Device deselected, IouT = 0mA, ZZ ≤ VIL, f = Max, All Inputs ≤ 0.2V or ≥ VDD-0.2V	-	30	mA	
	IsB1	Device deselected, lout = 0mA, ZZ≤0.2V, f = 0,		-	5	mA
	1581	All Inputs=fixed (VDD-0.2V or 0.2V)	L-Ver.	-	1	mA
	IsB2	Device deselected, lout = 0mA, ZZ≥Vpp-0.2V, f = Max,		•	5	mA
	1352	All Inputs ≤ VIL or ≥ VIH	L-Ver.	-	200	μA
Output Low Voltage	VoL	IoL = 8.0mA	-	0.4	V	
Output High Voltage	Vон	IOH = -4.0mA		2.4	-	٧
Input Low Voltage	VIL			-0.5*	0.8	٧
Input High Voltage	ViH			2.2	5.5**	٧

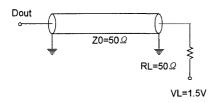
^{*} VIL(min) = -3.0(Pulse Width \le 20ns)

TEST CONDITIONS

(TA = 0°C to 70°C, VDD=3.3V-5%/+10% unless otherwise specified)

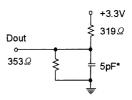
Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time(Measured at 0.3V and 2.7V)	2ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1

Output Load(A)



^{*} Capacitive Load consists of all components of the test environment.

Output Load(B) (for tLZC, tLZOE, tHZOE& tHZC)



* Including Scope and Jig Capacitance

Fig. 1



^{**} In Case of I/O Pins, the Max. VIH = VDDQ + 0.5V

AC TIMING CHARACTERISTICS

(VDD=3.3V-5%/+10%,TA=0% to 70%)

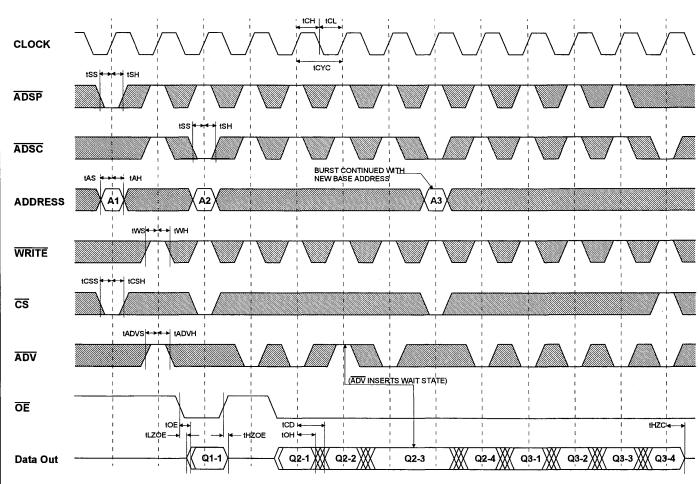
Parameter	Symbol	KM732	V589-13	KM732	V589-15	KM732V589-17		Unit
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit
Cycle Time	tCYC	13	-	15	-	17	-	ns
Clock Access Time	tCD	-	7	-	8	-	9	ns
Output Enable to Data Valid	tOE	-	6	-	7	-	8	ns
Clock High to Output Low-Z	tLZC	6	-	6	-	6	-	ns
Output Hold from Clock High	tOH	2.5	-	2.5	-	2.5	-	ns
Output Enable Low to Output Low-Z	tLZOE	2	-	2	-	2	-	ns
Output Enable High to Output High-Z	tHZOE	2	5	2	6	2	-	ns
Clock High to Output High-Z	tHZC		7		7		7	ns
Clock High Pulse Width	tCH	4.5	-	5.5	-	6	-	ns
Clock Low Pulse Width	tCL	4.5	-	5.5	-	6	-	ns
Address Setup to Clock High	tAS	2.5	-	2.5	-	2.5	-	ns
Address Status Setup to Clock High	tSS	2.5	-	2.5	-	2.5	-	ns
Data Setup to Clock High	tDS	2.5	-	2.5	-	2.5	-	ns
Write Setup to Clock High(GW, BW, WEx)	tWS	2.5	-	2.5	_	2.5	-	ns
Address Advance Setup to Clock High	tADVS	2.5	-	2.5	-	2.5	-	ns
Chip Select Setup to Clock High	tCSS	2.5	-	2.5	-	2.5	-	ns
Address Hold from Clock High	tAH	0.5	-	0.5	-	0.5	-	ns
Address Status Hold from Clock High	tSH	0.5	-	0.5	-	0.5	-	ns
Data Hold from Clock High	tDH	0.5	-	0.5	-	0.5	-	ns
Write Hold from Clock High(GW, BW, WEx)	tWH	0.5	-	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	tADVH	0.5	-	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	tCSH	0.5	-	0.5	-	0.5	-	ns
ZZ High to Power Down	tPDS	2	-	2	-	2	-	cycle
ZZ Low to Power Up	tPUS	2	-	2	-	2	-	cycle

NOTE: 1. All address inputs must meet the specified setup and hold times for all rising clock edges whenever ADSC and/or ADSP is sampled low and CS is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.

2. Both chip selects must be active whenever ADSC or ADSP is sampled low in order for the this device to remain enabled.

3. ADSC or ADSP must not be asserted for at least 2 Clock after leaving ZZ state.

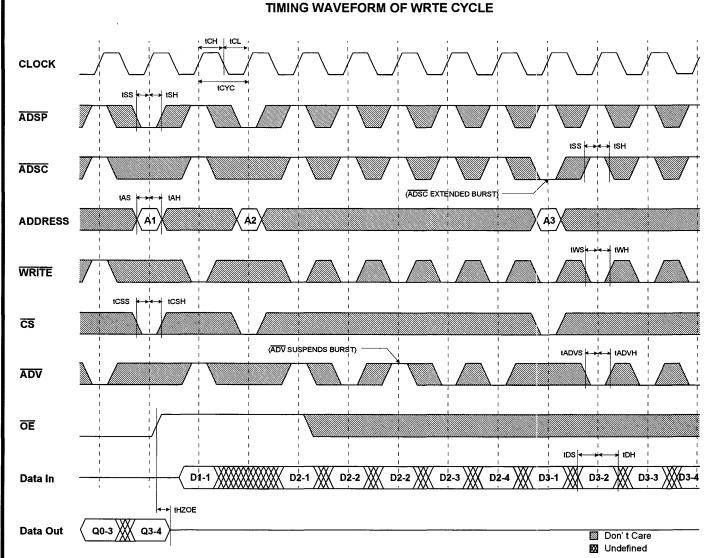
TIMING WAVEFORM OF READ CYCLE



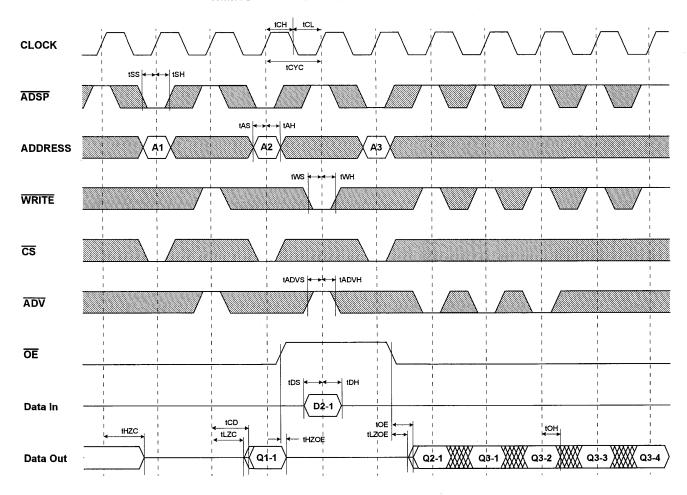
NOTES: $\overline{WRITE} = L$ means $\overline{GW} = L$, or $\overline{GW} = H$, $\overline{BW} = L$, $\overline{WE}x = L$ $\overline{CS} = L$ means $\overline{CS}1 = L$, $\overline{CS}2 = H$ and $\overline{CS}2 = L$ $\overline{CS} = H$ means $\overline{CS}1 = H$, or $\overline{CS}1 = L$ and $\overline{CS}2 = H$, or $\overline{CS}1 = L$, and $\overline{CS}2 = L$

Don't Care

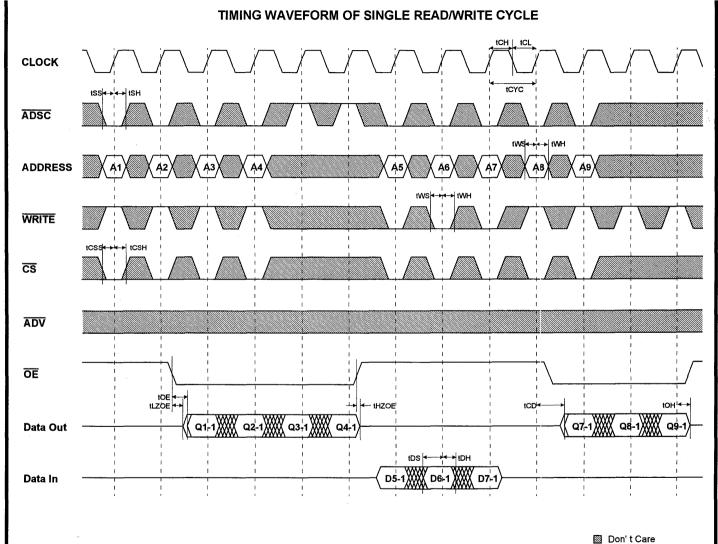
☑ Undefined

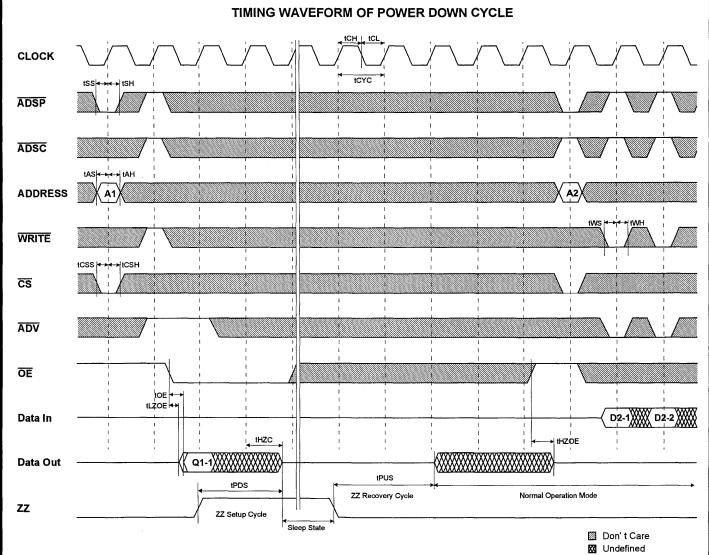


TIMING WAVEFORM OF COMBINATION READ/WRTE CYCLE



Undefined

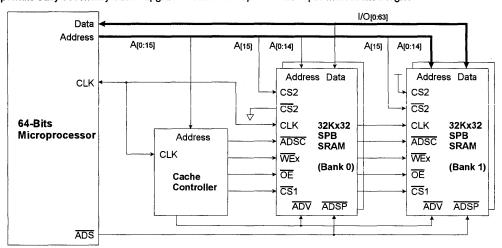




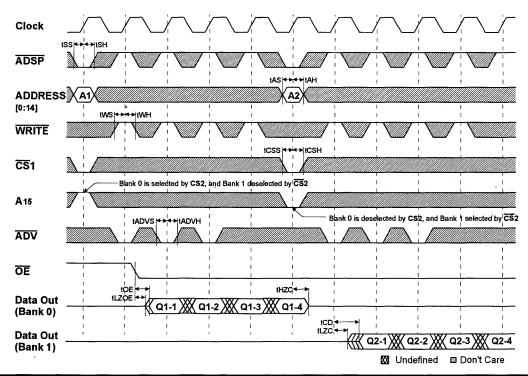
APPLICATION INFORMATION

DEPTH EXPANSION

The Samsung 32Kx32 Synchronous Pipelined Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 32K depth to 64K depth without extra logic.



INTERLEAVE READ TIMING (Refer to non-interleave write timing for interleave write timing)



32Kx32-Bit Synchronous Pipelined Burst SRAM

FEATURES

- · Synchronous Operation.
- . 2 Stage Pipelined operation with 4 Burst.
- · On-Chip Address Counter.
- · Self-Timed Write Cycle.
- · On-Chip Address and Control Registers.
- VDD = 3.3V-5%/+10% Power Supply
- 5V Tolerant Inputs except I/O Pins
- . Byte Writable Function.
- · Global Write Enable Controls a full bus-width write.
- Power Down State via ZZ Signal.
- TBO Pin allows a choice of either a interleaved burst or a linear burst.
- Three Chip Enables for simple depth expansion with No Data Contention; 2 cycle Enable, 1 cycle Disable.
- · Asynchronous Output Enable Control.
- . ADSP, ADSC, ADV Burst Control Pins.
- TTL-Level Three-State Output.
- . 100-Pin QFP/TQFP Package

FAST ACCESS TIMES

Parameter	Symbol	-13	-15	Unit
Cycle Time	tCYC	13	15	ns
Clock Access Time	tCD	7.0	8.0	ns
Output Enable Access Time	tOE	6.0	7.0	ns

GENERAL DESCRIPTION

The KM732V589A/L is a 1,048,576-bit Synchronous Static Random Access Memory designed for high performance second level cache of Pentium and Power PC based System.

It is organized as 32K words of 32 bits and integrates address and control registers, a 2-bit burst address counter and added some new functions for high performance cache RAM applications; $\overline{\text{GW}}$, $\overline{\text{BW}}$, $\overline{\text{LBO}}$, ZZ.

Write cycles are internally self-timed and synchronous.

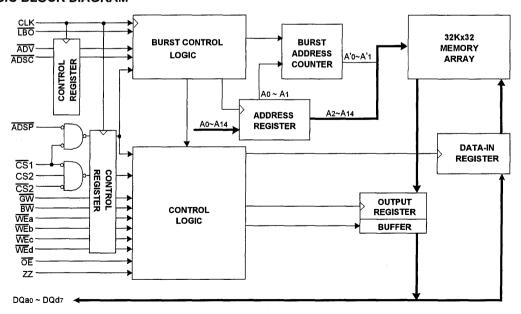
Full bus-width write is done by \overline{GW} , and each byte write is performed by the combination of $\overline{WE}x$ and \overline{BW} when \overline{GW} is high. And with $\overline{CS1}$ high, \overline{ADSP} disable to support address pipelining. Burst cycle can be initiated with either the address status processor(\overline{ADSP}) or address status cache controller(\overline{ADSC}) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance(\overline{ADV}) input.

LBO pin is DC operated and determines burst sequence(linear or interleaved).

ZZ pin controls Power Down State and reduces Stand-by current regardless of CLK.

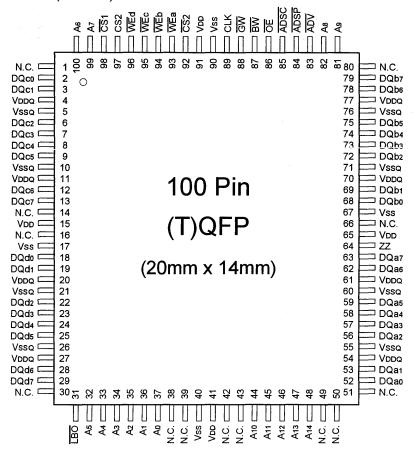
The KM732V589A/L is fabricated using SAMSUNG's high performance CMOS technology and is available in a 100pin QFP/TQFP package. Multiple power and ground pins are utilized to minimize ground bounce.

LOGIC BLOCK DIAGRAM





PIN CONFIGURATION (TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A14	Address Inputs	32,33,34,35,36,37,	VDD	Power Supply(+3.3V)	15,41,65,91
		44,45,46,47,48,81,	Vss	Ground	17,40,67,90
		82,99,100	N.C.	No Connect	1,14,16,30,38,39,42,43,
ADV	Burst Address Advance	83		1	49,50,51,66,80
ADSP	Address Status Processor	84	DQa0 ~ a7	Data inputs/Outputs	52,53,56,57,58,59,62,63
ADSC	Address Status Controller	85	DQb0 ~ b7		68,69,72,73,74,75,78,79
CLK	Clock	89	DQc0 ~ c7		2,3,6,7,8,9,12,13
CS1	Chip Select	98	DQdo ~ d7		18,19,22,23,24,25,28,29
CS2	Chip Select	97		1	
CS2	Chip Select	92	VDDQ	Output Power Supply	4,11,20,27,54,61,70,77
WEx	Byte Write Inputs	93,94,95,96			
ŌĒ	Output Enable	86	Vssq	Output Ground	5,10,21,26,55,60,71,76
Ġ₩	Global Write Enable	88	ľ		
BW	Byte Write Enable	87]]
ZZ	Power Down Input	64		!	
LBO	Burst Mode Control	31		}	



FUNCTION DESCRIPTION

The KM732V589A/L is a synchronous SRAM designed to support the burst address accessing sequence of the P6 and Power PC based microprocessor. All inputs (with the exception of \overline{OE} and ZZ) are sampled on rising clock edges. The start and duration of the burst access is controlled by $\overline{CS1}$, \overline{ADSC} , \overline{ADSC} and \overline{ADV} . The accesses are enabled with the chip select signals and output enabled signals. Wait states are inserted into the access with \overline{ADV} .

When ZZ is pulled high, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM normally operates after 2 cycles of wake up time.

Read cycles are initiated with $\overline{\text{ADSP}}$ (regardless of $\overline{\text{WEx}}$ and $\overline{\text{ADSC}}$) using the new external address clocked into the on-chip address register whenever $\overline{\text{ADSP}}$ is sampled low, the chip selects are sampled active, and the output buffer is enabled with $\overline{\text{OE}}$. In read operation the data of cell array accessed by the current address, registered in the Data-out registers by the positive edge of CLK, are carried to the Data-out buffer by the next positive edge of CLK. The data, registered in the Data-out buffer, are projected to the output pins. $\overline{\text{ADV}}$ is ignored on the clock edge that samples $\overline{\text{ADSP}}$ asserted, but is sampled on the subsequent clock edges. The address increases internally for the next access of the burst when $\overline{\text{WEx}}$ are sampled High and $\overline{\text{ADV}}$ is sampled low. And $\overline{\text{ADSP}}$ is blocked to control signals by disabling $\overline{\text{CS}}$ 1.

All byte write is done by \overline{GW} (regardless of \overline{BW} and $\overline{WE}x$.), and each byte write is performed by the combination of \overline{BW} and $\overline{WE}x$ when \overline{GW} is high.

Write cycles are performed by disabling the output buffers with \overline{OE} and asserting \overline{WEx} . \overline{WEx} are ignored on the clock edge that samples \overline{ADSP} low, but are sampled on the subsequent clock edges. The output buffers are disabled when \overline{WEx} are sampled Low(regardless of \overline{OE}). Data is clocked into the data input register when \overline{WEx} sampled Low. The address increases internally to the next address of burst, if both \overline{WEx} and \overline{ADV} are sampled Low. Individual byte write cycles are performed by any one or more byte write enable signals(\overline{WEa} , \overline{WE}) or \overline{WEd}) sampled low. The \overline{WEa} controls DQao ~ DQa7, \overline{WE} controls DQbo ~ DQb7, \overline{WE} controls DQco ~ DQc7, and \overline{WEd} controls DQdo ~ DQd7. Read or write cycle may also be initiated with \overline{ADSC} and \overline{ADSP} . The differences between cycles initiated with \overline{ADSC} and \overline{ADSP} as are follows;

ADSP must be sampled high when ADSC is sampled low to initiate a cycle with ADSC. WEx are sampled on the same clock edge that sampled ADSC low(and ADSP high).

Addresses are generated for the burst access as shown below, The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the LBO pin. When this pin is Low, linear burst sequence is selected. When this pin is High, Interleaved burst sequence is selected.

BURST SEQUENCE TABLE

(Interleaved Burst)

TBO PIN HIGH	Ca	se 1	Cas	Case 2		se 3	Case 4		
LBO FIN HIGH	A1	A0	A1	A0	A1	A0	A1	A0	
First Address	0	0	0	1	1	0	1	1	
	0	1	0	0	1	1	1 1	0	
↓	1	0	1	1	0	0	0	1	
Fourth Address	1	1	1	0	0	1	0	0	

(Linear Burst)

LBO PIN LOW	Case 1 Case 2			Cas	se 3	Case 4		
CDO FIN COV	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
·	0	1	1 1	0	1	1	0	0
	1	0	1	1	0	0	0	1
Fourth Address	1	1	0	. 0	0	1	1	0

NOTE: 1. LBO pin must be tied to High or Low, and Floating State must not be allowed.



TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

CS1	CS2	CS2	ADSP	ADSC	ADV	WRITE	CLK	Address Accessed	Operation
Н	Х	X	Х	L	X	Х	1	N/A	Not Selected
L	L	Х	L	Х	Х	Х	1	N/A	Not Selected
L	Х	Н	L	Х	X	Х	1	N/A	Not Selected
L	L	Х	Х	L	Х	Х	1	N/A	Not Selected
L	Х	Н	Х	L	Х	Х	1	N/A	Not Selected
L	Н	L	٦	Х	Х	Х	1	External Address	Begin Burst Read Cycle
L	Н	L	Н	L	Х	L	↑	External Address	Begin Burst Write Cycle
L	Н	L	Н	L	Х	Н	1	External Address	Begin Burst Read Cycle
X	Х	Х	Н	Н	L	Н	1	Next Address	Continue Burst Read Cycle
Н	Х	Х	Х	Н	L	Н	1	Next Address	Continue Burst Read Cycle
X	Х	Х	Н	Н	L	٦	1	Next Address	Continue Burst Write Cycle
Н	Х	Х	Х	Н	L	L	1	Next Address	Continue Burst Write Cycle
X	Х	Х	Н	Н	Н	Н	1	Current Address	Suspend Burst Read Cycle
Н	Х	Х	Х	Н	Н	Н	1	Current Address	Suspend Burst Read Cycle
Х	Х	Х	Н	Н	Н	L	1	Current Address	Suspend Burst Write Cycle
Н	Х	Х	Х	Н	Н	L	1	Current Address	Suspend Burst Write Cycle

NOTE: 1. X means "Don't Care".

- 2. The rising edge of clock is symbolized by \uparrow .
- WRITE = L means Write operation in WRITE TRUTH TABLE.
 WRITE = H means Read operation in WRITE TRUTH TABLE.
- 4. Operation finally depends on status of asynchronous input pins(ZZ and \overline{OE}).

WRITE TRUTH TABLE

GW	BW	WEa	WEb	WEc	WEd	Operation
Н	Н	Х	Х	Х	Х	READ
Н	L	Н	H	Н	Н	READ
Н	L	L	Н	Н	Н	WRITE BYTE a
Н	L	Н	L	Н	Н	WRITE BYTE b
Н	L	Н	Н	L	L	WRITE BYTE c and d
Н	L	L	L	L	L	WRITE ALL BYTES
L	Х	Х	Х	Х	Х	WRITE ALL BYTEs

NOTE: 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(1).

ASYNCHRONOUS TRUTH TABLE

(See Notes 1 and 2):

Operation	ZZ	ŌĒ	I/O Status
Sleep Mode	Н	Х	High-Z
Read	L	L	DQ
Read	L	Н	High-Z
Write	L	Х	Din, High-Z
Deselected	L	Х	High-Z

NOTE

- 1. X means "Don't Care".
- 2. ZZ pin is pulled down internally
- 3. For write cycles that following read cycles, the output buffers must be disabled with \overline{OE} , otherwise data bus contention will occur.
- Sleep Mode means power down state of which stand-by current does not depend on cycle time.
- Deselected means power down state of which stand-by current depends on cycle time.



PASS-THROUGH TRUTH TABLE

Previous Cycle Operation WRITE		Presen	Novi Cuala			
		Operation	₹ 5 1	CS1 WRITE		Next Cycle
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	Initiate Read Cycle Address=An Data=Qn-1 for all bytes	L	н	L	Read Cycle Data=Qn
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=Qn-1 for all bytes	Н	н	L	No carryover from previous cycle
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=High-Z	Н	н	Н	No carryover from previous cycle
Write Cycle, One byte Address=An-1, Data=Dn-1	One L	Initiate Read Cycle Address=An Data=Qn-1 for one byte	L	н	L	Read Cycle Data=Qn
Write Cycle, One byte Address=An-1, Data=Dn-1	One L	No new cycle Data=Qn-1 for one byte	Н	Н	L	No carryover from previous cycle

NOTE: 1. This operation makes written data immediately available at output during a read cycle preceded by a write cycle.

2. WEx means WEa ~ WEd.

ABSOLUTE MAXIMUM RATING*

Parameter	Symbol	Rating	Unit
Voltage on VDD Supply Relative to Vss	VDD	-0.3 to 4.6	V
Voltage on VDDQ Supply Relative to Vss	VDDQ	VDD	V
Voltage on Input Pin Relative to Vss	VIN	-0.3 to 6.0	V
Voltage on I/O Pin Relative to Vss	Vio	-0.3 to VDDQ + 0.5	· V
Power Dissipation	Po	1.2	W
Storage Temperature	Тѕтҫ	-65 to 150	°C
Operating Temperature	TOPR	0 to 70	°C
Storage Temperature Range Under Bias	TBIAS	-10 to 85	°C

*NOTE: Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS (0 $^{\circ}$ C $^{\circ}$ TA $^{\leq}$ 70 $^{\circ}$ C)

Parameter	Symbol	Min	Тур.	Max	Unit
Supply Voltage	VDD	3.13	3.3	3.6	V
	VDDQ	3.13	3.3	3.6	V
Ground	Vss	0	0	0	V

CAPACITANCE*(TA = 25°C, f = 1MHz)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	CIN	VIN=0V	-	5	pF
Output Capacitance	Соит	Vout≕0V	-	7	pF

*NOTE: Sampled not 100% tested.



DC ELECTRICAL CHARACTERISTICS

(VDD=3.3V-5%+10%, TA = 0° to 70°)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current(except ZZ)	lıL	VDD = Vss to VDD; VIN = Vss to VDD		-2	+2	μA
Output Leakage Current	loL	Output Disabled, VOUT = Vss to VDDQ	Output Disabled, Vout = Vss to VDDQ			
Operating Current	lcc	Device Selected, Io∪T = 0mA, ZZ≤VIL,	-13	-	200	mA
		All Inputs = VIL or VIH	-15	-	·180	
		Cycle Time ≥ tCYC min				
Standby Current	ISB	Device deselected, lout = 0mA, ZZ≤ViL, f = Max, All Inputs≤0.2V or ≥ VDD-0.2V		-	40	mA
	IsB1	Device deselected, lout = 0mA, IsB1 ZZ≤0.2V, f = 0,		-	5	mA
	.52.	All Inputs=fixed (VDD-0.2V or 0.2V)	L-Ver.	-	1	mA
	IsB2	Device deselected, louт = 0mA, ISB2 ZZ≥VDD-0.2V, f = Max,		•	5	mA
		All Inputs ≤ VIL or ≥ VIH	L-Ver.	-	500	μA
Output Low Voltage	Vol	IoL = 8.0mA		-	0.4	٧
Output High Voltage	Voн	Iон = -4.0mA		2.4	-	V
Input Low Voltage	VIL			-0.5*	0.8	٧
Input High Voltage	ViH			2.2	5.5**	٧

^{*} VIL(min) = -3.0(Pulse Width≤20ns)

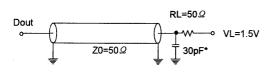
TEST CONDITIONS

(TA = 0 $^{\circ}$ C to 70 $^{\circ}$ C, VDD=3.3V-5%/+10% unless otherwise specified)

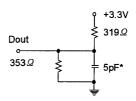
Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time(Measured at 0.3V and 2.7V)	2ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1

Output Load(A)

Output Load(B) (for tLZC, tLZOE, tHZOE& tHZC)



^{*} Capacitive Load consists of all components of the test environment.



* Including Scope and Jig Capacitance

Fig. 1



^{**} In Case of I/O Pins, the Max. VIH = VDDQ + 0.5V

AC TIMING CHARACTERISTICS

(VDD=3.3V-5%/+10%,TA = 0° to 70°)

Parameter	Symbol	KM732V589A-13		KM732V589A-15		Unit
Farameter	Symbol	Min	Max	Min	Max	Unit
Cycle Time	tCYC	13	-	15	-	ns
Clock Access Time	tCD	-	7.0	-	8.0	ns
Output Enable to Data Valid	tOE	-	6.0		7.0	ns
Clock High to Output Low-Z	tLZC	0	_	0	-	ns
Output Hold from Clock High	tOH	2.5	-	2.5	-	ns
Output Enable Low to Output Low-Z	tLZOE	0	-	0	-	ns
Output Enable High to Output High-Z	tHZOE	-	4.0	-	4.0	ns
Clock High to Output High-Z	tHZC	1.5	5.0	2.0	6.0	ns
Clock High Pulse Width	tCH	4.5		6.0	-	ns
Clock Low Pulse Width	tCL	4.5	-	6.0	-	ns
Address Setup to Clock High	tAS	2.5	-	2.5	-	ns
Address Status Setup to Clock High	tSS	2.5	-	2.5	-	ns
Data Setup to Clock High	tDS	2.5	-	2.5	-	ns
Write Setup to Clock High(GW, BW, WEx)	tWS	2.5	-	2.5	-	ns
Address Advance Setup to Clock High	tADVS	2.5	-	2.5	-	ns
Chip Select Setup to Clock High	tCSS	2.5	-	2.5	-	ns
Address Hold from Clock High	tAH	0.5	-	0.5	-	ns
Address Status Hold from Clock High	tSH	0.5	-	0.5	-	ns
Data Hold from Clock High	tDH	0.5	-	0.5	-	ns
Write Hold from Clock High(GW, BW, WEx)	tWH	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	tADVH	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	tCSH	0.5	-	0.5	-	ns
ZZ High to Power Down	tPDS	2	-	2	-	cycle
ZZ Low to Power Up	tPUS	2	-	2	-	cycle

NOTE: 1. All address inputs must meet the specified setup and hold times for all rising clock edges whenever ADSC and/or ADSP is sampled low and CS is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.

2. Both chip selects must be active whenever ADSC or ADSP is sampled low in order for the this device to remain enabled.

3. ADSC or ADSP must not be asserted for at least 2 Clock after leaving ZZ state.

CLOCK tCYC **ADSP ADSC** BURST CONTINUED WITH. NEW BASE ADDRESS tAS + +++ tAH **ADDRESS** A3 WRITE tcss + ++ + tCSH $\overline{\mathsf{cs}}$ tADVS + →+ → tADVH ADV (ADV INSERTS WAIT STATE) ŌĒ tHZC⊌ I tOE ++ tCD ₩ tOH ┕ tLZÓE → - tHZOE Q2-3 **Data Out**

TIMING WAVEFORM OF READ CYCLE

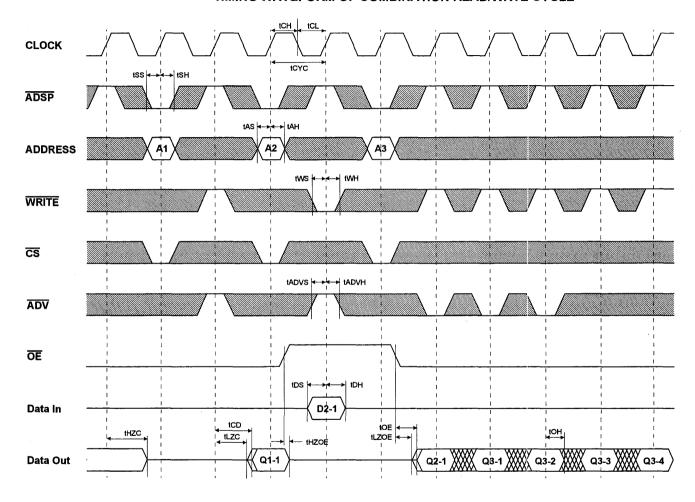
NOTES: WRITE = L means GW = L, or GW = H, BW = L, WEx = L

 \overline{CS} = L means \overline{CS} 1 = L, CS2 = H and \overline{CS} 2 = L \overline{CS} = H means \overline{CS} 1 = H, or \overline{CS} 1 = L and \overline{CS} 2 = H, or \overline{CS} 1 = L, and \overline{CS} 2 = L

Don't Care

TIMING WAVEFORM OF WRTE CYCLE CLOCK tCYC **ADSP** ADSC (ADSC EXTENDED BURST) **ADDRESS** tWS++++ tWH WRITE tCSS tCSH $\overline{\mathsf{cs}}$ (ADV SUSPENDS BURST) tADVS -+ tADVH ADV ŌĒ tDS ◀ + tDH D2-1 XX D2-2 XX Data In < → tHZOE Q0-3 XX Q0-4 **Data Out** Don't Care ☑ Undefined

TIMING WAVEFORM OF COMBINATION READ/WRTE CYCLE



Don't Care

☑ Undefined

ŌĒ

Data Out

Data In

673

tOE ↔

Q1-1 Q2-1 Q3-1 Q3-1

tOH^I

Q7-1 Q8-1 Q8-1

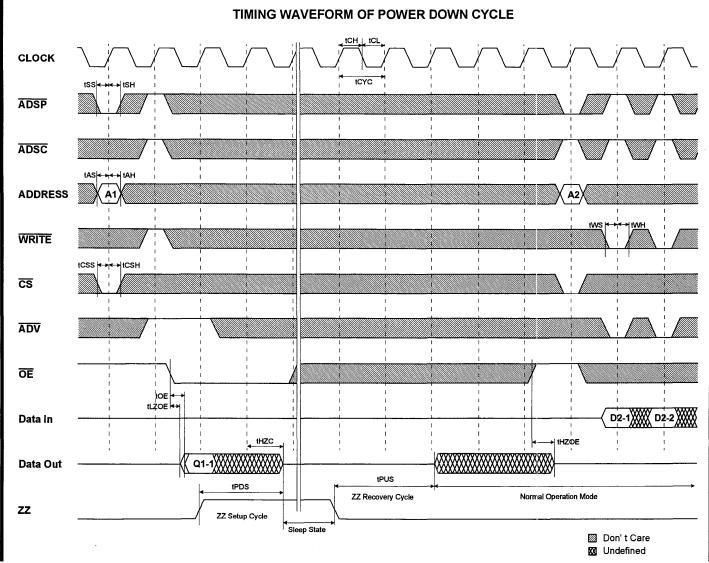
Don't Care

Undefined

KM732V589A/L

tHZOE

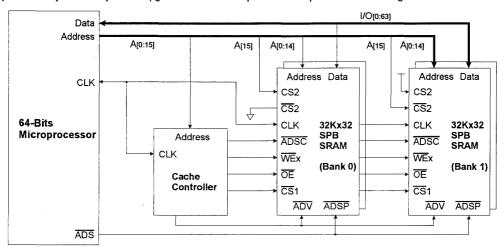




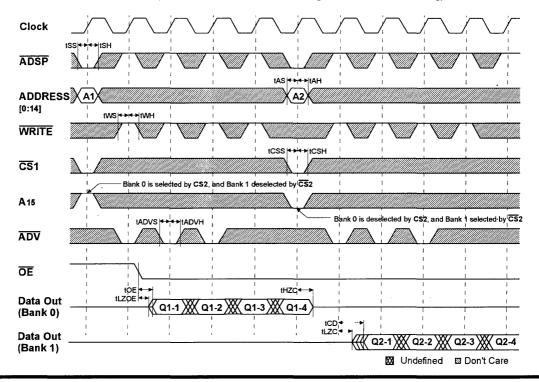
APPLICATION INFORMATION

DEPTH EXPANSION

The Samsung 32Kx32 Synchronous Pipelined Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 32K depth to 64K depth without extra logic.



INTERLEAVE READ TIMING (Refer to non-interleave write timing)



32Kx32-Bit Synchronous Pipelined Burst SRAM

FEATURES

- · Synchronous Operation.
- · 2 Stage Pipelined operation with 4 Burst.
- · On-Chip Address Counter.
- · Write Self-Timed Cycle.
- · On-Chip Address and Control Registers.
- VDD=3.3V-5%/+10% Power Supply for 3.3V I/O.
- VDD=3.3V±5% Power Supply for 2.5V I/O.
- I/O Supply Voltage: 3.3V-5%/+10% for 3.3V I/O or 2.5V+0.4V/-0.13V for 2.5V I/O
- . 5V Tolerant Inputs except I/O Pins.
- Byte Writable Function.
- · Global Write Enable Controls a full bus-width write.
- · Power Down State via ZZ Signal.
- Asynchronous Output Enable Control.
- ADSP, ADSC, ADV Burst Control Pins.
- LBO Pin allows a choice of either a interleaved burst or a linear burst.
- Three Chip Enables for simple depth expansion with No Data Contention; 2 cycle Enable, 1 cycle Disable.
- · TTL-Level Three-State Output.
- 100-Pin TQFP Package

FAST ACCESS TIMES

Parameter	Symbol	-13	-15	Unit
Cycle Time	tCYC	13	15	ns
Clock Access Time	tCD	7	8	ns
Output Enable Access Time	tOE	6	7	ns

GENERAL DESCRIPTION

The KM732V596A/L is a 1,048,576 bit Synchronous Static Random Access Memory designed for high performance second level cache of Pentium and Power PC based Mobile System.

It is organized as 32K words of 32 bits and integrates address and control registers, a 2-bit burst address counter and added some new functions for high performance cache RAM applications; $\overline{\text{GW}}$, $\overline{\text{BW}}$, $\overline{\text{LBO}}$, ZZ.

Write cycles are internally self-timed and synchronous.

Full bus-width write is done by \overline{GW} , and each byte write is performed by the combination of \overline{WEx} and \overline{BW} when \overline{GW} is high. And with $\overline{CS1}$ high, \overline{ADSP} is blocked to control signals.

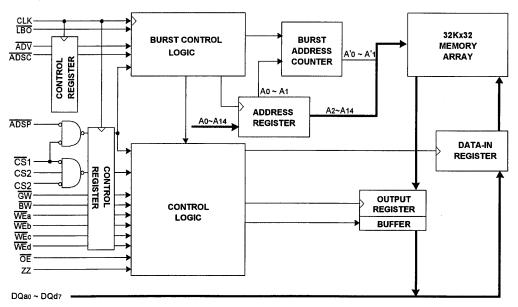
Burst cycle can be initiated with either the address status processor(ADSP) or address status cache controller(ADSC) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance(ADV) input.

<u>IBO</u> pin is DC operated and determines burst sequence(linear or interleaved).

ZZ pin controls Power Down State and reduces Stand-by current regardless of CLK.

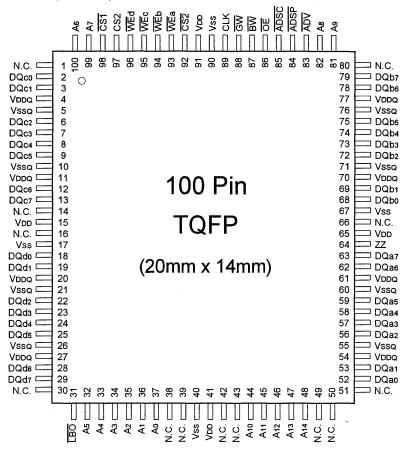
The KM732V596A/L is fabricated using SAMSUNG's high performance CMOS technology and is available in a 100pin TQFP package. Multiple power and ground pins are utilized to minimize ground bounce.

LOGIC BLOCK DIAGRAM





PIN CONFIGURATION (TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A14	Address Inputs	32,33,34,35,36,37,	VDD	Power Supply(+3.3V)	15,41,65,91
		44,45,46,47,48,81,	Vss	Ground	17,40,67,90
		82,99,100	N.C.	No Connect	1,14,16,30,38,39,42,43,
ADV	Burst Address Advance	83			49,50,51,66,80
ADSP	Address Status Processor	84	DQao ~ a7	Data Inputs/Outputs	52,53,56,57,58,59,62,63
ADSC	Address Status Controller	85	DQb0 ~ b7		68,69,72,73,74,75,78,79
CLK	Clock	89	DQc0 ~ c7		2,3,6,7,8,9,12,13
CS1	Chip Select	98	DQd0 ~ d7		18,19,22,23,24,25,28,29
CS2	Chip Select	97		ţ	
CS 2	Chip Select	92	VDDQ	Output Power Supply	4,11,20,27,54,61,70,77
WEx	Byte Write Inputs	93,94,95,96		(2.5V or 3.3V)	1
ŌĒ	Output Enable	86	Vssq	Output Ground	5,10,21,26,55,60,71,76
Ġ₩	Global Write Enable	88			
₿₩	Byte Write Enable	87			
ZZ	Power Down Input	64			
<u>LBO</u>	Burst Mode Control	31	1		

FUNCTION DESCRIPTION

The KM732V596A/L is a synchronous SRAM designed to support the burst address accessing sequence of the Pentium and Power PC based microprocessor. All inputs(with the exception of \overline{OE} and ZZ) are sampled on rising clock edges. The start and duration of the burst access is controlled by \overline{CS} 1, \overline{ADSP} , \overline{ADSC} and \overline{ADV} . The accesses are enabled with the chip select signals and output enabled signals. Wait states are inserted into access with \overline{ADV} .

When ZZ is pulled high, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When ZZ returns to Low, the SRAM normally operates after 2 cycles of wake up time. ZZ pin is pulled down internally.

Read cycles are initiated with $\overline{\text{ADSP}}$ (regardless of $\overline{\text{WEx}}$ and $\overline{\text{ADSC}}$) using the new external address clocked into the on-chip address register whenever $\overline{\text{ADSP}}$ is sampled low, the chip selects are sampled active, and the output buffer is enabled with $\overline{\text{OE}}$. In read operation the data of cell array accessed by the current address, registered in the Data-out registers by the positive edge of CLK, are carried to the Data-out buffer by the next positive edge of CLK. The data, registered in the Data-out buffer, are projected to the output [ins. ADV is ignored on the clock edge that samples ADSP asserted, but is sampled on the subsequent clock edges. The address increases internally for the next access of the burst when $\overline{\text{WEx}}$ are sampled high and $\overline{\text{ADV}}$ is sampled Low. And $\overline{\text{ADSP}}$ is blocked to control signals by disabling $\overline{\text{CS}}1$.

All byte write is done by $\overline{\text{GW}}$ (regardless of $\overline{\text{BW}}$ and $\overline{\text{WEx}}$.), and each byte write is performed by the combination of $\overline{\text{BW}}$ and $\overline{\text{WEx}}$ when $\overline{\text{GW}}$ is High. Write cycles are performed by disabling the output buffers with $\overline{\text{OE}}$ and asserting $\overline{\text{WEx}}$. $\overline{\text{WEx}}$ are ignored on the clock edge that samples $\overline{\text{ADSP}}$ Low, but are sampled on the subsequent clock edges. The output buffers are disabled when $\overline{\text{WEx}}$ are sampled Low(regardless of $\overline{\text{OE}}$). Data is clocked into the data input register when $\overline{\text{WEx}}$ sampled Low. The address increases internally to the next address of burst, if both $\overline{\text{WEx}}$ and $\overline{\text{ADV}}$ are sampled Low. Individual byte write cycles are performed by any one or more byte write enable signals($\overline{\text{WEa}}$), $\overline{\text{WE}}$), $\overline{\text{WE}}$ 0 or $\overline{\text{WE}}$ 0 sampled low. THE $\overline{\text{WE}}$ 1 control DQa0 \sim DQa7, $\overline{\text{WE}}$ 2 control DQc0 \sim DQc7, and $\overline{\text{WE}}$ 3 control DQd0 \sim DQd7. Read or write cycle may also be initiated with $\overline{\text{ADSC}}$ 3, instead of $\overline{\text{ADSP}}$ 5. The differences between cycles initiated with $\overline{\text{ADSC}}$ 3 and $\overline{\text{ADSP}}$ 4 as are follows;

ADSP must be sampled high when ADSC is sampled low to initiate a cycle with ADSC. WEx are sampled on the same clock edge that sampled ADSC low(and ADSP high).

Addresses are generated for the burst access as shown below, The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the LBO pin. When this pin is Low, linear burst sequence is selected. When this pin is High, Interleaved burst sequence is selected.

BURST SEQUENCE TABLE

(Interleaved Burst)

EBO PIN HIGH	Ca	Case 1		Case 2		Case 3		Case 4	
LBO FIN HIGH	A1	A0	A1	A0	A1	A0	A1	A0	
First Address	0	0	0	1	1	0	1	1	
	0	1	0	0	1	1	1	0	
1	1	0	1	1	0	0	0	1	
Fourth Address	1	1	1	0	0	1	0	0	

(Linear Burst)

TBO PIN LOW	Case 1		Case 2		Case 3		Case 4	
LBO FILV	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
	0	1	1	0	1	1	0	0
	1 1	0	1	1	0	0	0	1
Fourth Address	1	1	0	0	0	1	11	0

NOTE: 1. LBO pin must be tied to High or Low, and Floating State must not be allowed.



TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

CS1	CS2	CS2	ADSP	ADSC	ADV	WRITE	CLK	Address Accessed	Operation
Н	Х	Х	Х	اـ	Х	Х	1	N/A	Not Selected
L	L	Х	L	Х	Х	X	1	N/A	Not Selected
L	Х	Н	L	Х	Х	Х	1	N/A	Not Selected
اد	L	Х	Х	L	X	Х	1	N/A	Not Selected
L	Х	Н	Х	L	X	Х	1	N/A	Not Selected
	Н	لـ	L	X	X	Х	1	External Address	Begin Burst Read Cycle
L	Н	L	Н	L	Х	L	1	External Address	Begin Burst Write Cycle
L	Н	L	Н	L	X	H	1	External Address	Begin Burst Read Cycle
X	Х	Х	Н	Н	L	Н	1	Next Address	Continue Burst Read Cycle
Н	Х	Х	Х	Н	L	Н	1	Next Address	Continue Burst Read Cycle
Х	Х	Х	Н	Н	L	L	1	Next Address	Continue Burst Write Cycle
Н	Х	Х	Х	Н	L	L	1	Next Address	Continue Burst Write Cycle
Х	Х	Х	Н	Н	Н	Н	1	Current Address	Suspend Burst Read Cycle
Н	Х	Х	Х	Н	Н	Н	1	Current Address	Suspend Burst Read Cycle
Х	Х	Х	Н	Н	Н	L	1	Current Address	Suspend Burst Write Cycle
Н	Х	Χ	Х	Н	Н	L	1	Current Address	Suspend Burst Write Cycle

NOTE: 1. X means "Don't Care".

- 2. The rising edge of clock is symbolized by 1.
- 3. WRITE = L means Write operation in WRITE TRUTH TABLE.
 WRITE = H means Read operation in WRITE TRUTH TABLE.
- 4. Operation finally depends on status of asynchronous input pins(ZZ and OE).

WRITE TRUTH TABLE

GW	BW	WEa	WEb	WEc	WEd	Operation
Н	H	Х	Х	Х	X	READ
Н	L	н	Н	Н	Н	READ
Н	L	L	Н	Н	Н	WRITE BYTE a
Н	L	Н	L	Н	Н	WRITE BYTE b
Н	L	Н	Н	L	L	WRITE BYTE c and d
Н	L	L	L	L	L	WRITE ALL BYTEs
L	Х	Х	Х	Х	Х	WRITE ALL BYTEs

NOTE: 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(1).

ASYNCHRONOUS TRUTH TABLE

(See Notes 1 and 2):

Operation	ZZ	ŌĒ	I/O Status		
Sleep Mode	Н	Х	High-Z		
Read	L	L	DQ		
Read	L	Н	High-Z		
Write	L	Х	Din, High-Z		
Deselected	L	Х	High-Z		

NOTE

- 1. X means "Don't Care".
- 2. ZZ pin is pulled down internally.
- 3. For write cycles that following read cycles, the output buffers must be disabled with \overline{OE} , otherwise data bus contention will occur.
- Sleep Mode means power down state of which stand-by current does not depend on cycle time.
- Deselected means power down state of which stand-by current depends on cycle time.



PASS-THROUGH TRUTH TABLE

Previous Cycle Operation WRITE		Presen	North Courts			
		Operation CS		WRITE	ŌĒ	Next Cycle
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	Initiate Read Cycle Address=An Data=Qn-1 for all bytes	L	н	L	Read Cycle Data=Qn
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=Qn-1 for all bytes	Н	н	L	No carryover from previous cycle
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=High-Z	н	н	Н	No carryover from previous cycle
Write Cycle, One byte Address=An-1, Data=Dn-1	One L	Initiate Read Cycle Address=An Data=Qn-1 for one byte	L	н	L	Read Cycle Data=Qn
Write Cycle, One byte Address=An-1, Data=Dn-1	One L	No new cycle Data=Qn-1 for one byte	Н	Н	L	No carryover from previous cycle

NOTE: This operation makes written data immediately available at output during a read cycle preceded by a write cycle.

ABSOLUTE MAXIMUM RATING*

Parameter	Symbol	Rating	Unit
Voltage on VDD Supply Relative to Vss	VDD	-0.3 to 4.6	V
Voltage on VDDQ Supply Relative to Vss	VDDQ	VDD	V
Voltage on Input Pin Relative to Vss	Vin	-0.3 to 6.0	V
Voltage on I/O Pin Relative to Vss	Vio	-0.3 to VDDQ + 0.5	V
Power Dissipation	Po	1.2	W
Storage Temperature	Тѕтс	-65 to 150	°C
Operating Temperature	Topr	0 to 70	°C
Storage Temperature Range Under Bias	TBIAS	-10 to 85	°C

^{*}NOTE: Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability

OPERATING CONDITIONS at 3.3V I/O($0^{\circ} \le T_A \le 70^{\circ}$)

Parameter	Symbol	Min	Тур.	Max	Unit
Supply Voltage	VDD	3.13	3.3	3.6	V
Supply Voltage	VDDQ	3.13	3.3	3.6	V
Ground	Vss	0	0	0	V

OPERATING CONDITIONS at 2.5V I/O($0^{\circ} \le TA \le 70^{\circ}$)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	VDD	3.13	3.3	3.47	V
Supply Voltage	VDDQ	2.37	2.5	2.9	٧
Ground	Vss	0	0	0	V



CAPACITANCE*(TA = 25°C, f = 1MHz)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	CIN	VIN=0V	-	5	pF
Output Capacitance	Соит	Vout=0V	-	7	pF

^{*}NOTE: Sampled not 100% tested.

DC ELECTRICAL CHARACTERISTICS

(VDD=3.3V-5%/+10%, VDDQ=3.3V-5%/+10%, or VDD=3.3V±5%, VDDQ=2.5V+0.4V/-0.13V, TA = 0°C to 70°C)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current(except ZZ)	lıL	VDD = Vss to VDD, VIN = Vss to VDD		-2	2	μA
Output Leakage Current	loL	Output Disabled, Vour = Vss to VDD	2	-2	2	μA
Operating Current	Icc	Device Selected, IOUT = 0mA,	-13	-	200	mA
		ZZ≤VIL, All Inputs = VIL or VIH	-15	-	180	
		Cycle Time ≥ tCYC min				
Standby Current	ISB	Device deselected, lout = 0mA, ZZ≤ f = Max, All Inputs≤0.2V or ≥ VDD-0	•	-	40	mΑ
	IsB1	IsB1 Device deselected, IouT = 0mA, ZZ ≤ 0.2V, f = 0,		-	5	mA
	All Inputs = fixed(VDD-0.2V or 0.2V)	L-Ver.	-	1.0	mA	
	IsB2	Device deselected, louт = 0mA, ZZ ≥ Vpp-0.2V, f = Max.		-	5	mA
		All Inputs≤VIL or ≥VIH	L-Ver.	-	500	μA
Output Low Voltage(3.3V I/O)	Vol	IoL = 8.0mA		-	0.4	٧
Output High Voltage(3.3V I/O)	Voн	Iон = -4.0mA		2.4	•	V
Output Low Voltage(2.5V I/O)	Vol	IoL = 1.0mA		-	0.2	V
Output High Voltage(2.5V I/O)	Voн	Iон = -1.0mA		2.0	-	V
Input Low Voltage(3.3V I/O)	VIL			-0.5*	0.8	٧
Input High Voltage(3.3V I/O)	VIH			2.0	5.5**	V
Input Low Voltage(2.5V I/O)	VIL			-0.3*	0.7	٧
Input High Voltage(2.5V I/O)	VIH			1.7	5.5**	V

^{*} VIL(min) = -3.0(Pulse Width ≤ 20ns)

^{**} In Case of I/O Pins, the Max. VIH = VDDQ + 0.5V

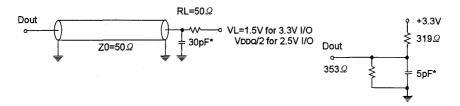
TEST CONDITIONS

(TA = 0 ℃ to 70 ℃, VDD=3.3V-5%/+10%, VDDQ=3.3V-5%/+10%, or VDD=3.3V±5%, VDDQ=2.5V +0.4V/-0.13V)

Parameter	Value
Input Pulse Level (for 3.3V I/O)	0 to 3V
Input Pulse Level (for 2.5V I/O)	0 to 2.5V
Input Rise and Fall Time(Measured at 0.3V and 2.7V for 3.3V I/O)	2ns
Input Rise and Fall Time(Measured at 0.3V and 2.1V for 2.5V I/O)	2ns
Input and Output Timing Reference Levels(for 3.3V I/O)	1.5V
Input and Output Timing Reference Levels(for 2.5V I/O)	VDDQ/2
Output Load	See Fig. 1

Output Load(A)

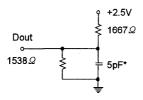
Output Load(B),(3.3V I/O) (for tLZC, tLZOE, tHZOE& tHZC)



* Capacitive Load consists of all components of the test environment.

* Including Scope and Jig Capacitance

Output Load(C),(2.5V I/O) (for tLZC, tLZOE, tHZOE& tHZC)



* Including Scope and Jig Capacitance

Fig. 1

AC TIMING CHARACTERISTICS

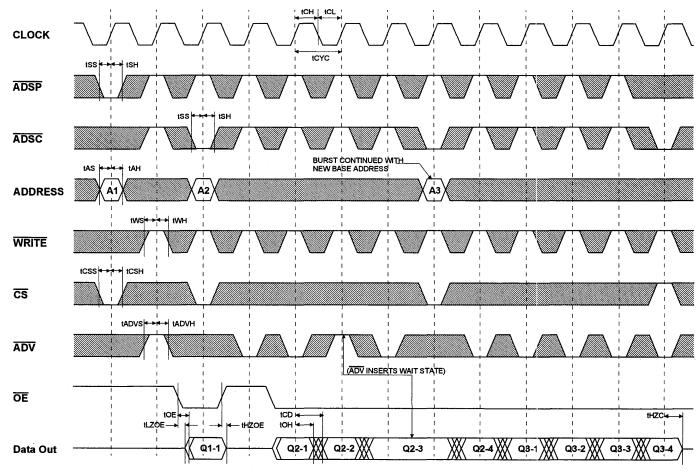
 $(VDD=3.3V-5\%+10\%, VDDQ=3.3V-5\%+10\%, or VDD=3.3V\pm5\%, VDDQ=2.5V+0.4V-0.13V, TA=0°C to 70°C)$

Parameter	Symbol	KM732	V596A-13	KM732	V596A-15	Unit
Faidilletei	Symbol	Min	Max	Min	Max	- Omi
Cycle Time	tCYC	13	-	15	-	ns
Clock Access Time	tCD	-	7.0	T -	8.0	ns
Output Enable to Data Valid	tOE	-	6.0		7.0	ns
Clock High to Output Low-Z	tLZC	0	-	0	-	ns
Output Hold from Clock High	tOH	2.5	-	2.5	-	ns
Output Enable Low to Output Low-Z	tLZOE	0	-	0	-	ns
Output Enable High to Output High-Z	tHZOE	-	4.0	-	4.0	ns
Clock High to Output High-Z	tHZC	1.5	5.0	2.0	6.0	ns
Clock High Pulse Width	tCH	4.5	-	6.0	-	ns
Clock Low Pulse Width	tCL	4.5	-	6.0	-	ns
Address Setup to Clock High	tAS	2.5	-	2.5	-	ns
Address Status Setup to Clock High	tss	2.5	-	2.5	-	ns
Data Setup to Clock High	tDS	2.5	-	2.5	-	ns
Write Setup to Clock High(GW, BW, WEx)	tWS	2.5	-	2.5	-	ns
Address Advance Setup to Clock High	tADVS	2.5	-	2.5	-	ns
Chip Select Setup to Clock High	tCSS	2.5	-	2.5	-	ns
Address Hold from Clock High	tAH	0.5	-	0.5	-	ns
Address Status Hold from Clock High	tSH	0.5	-	0.5	-	ns
Data Hold from Clock High	tDH	0.5	-	0.5	-	ns
Write Hold from Clock High(GW, BW, WEx)	tWH	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	tADVH	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	tCSH	0.5	-	0.5	-	ns
ZZ High to Power Down	tPDS	2	-	2	-	cycle
ZZ Low to Power Up	tPUS	2	-	2	-	cycle

NOTE: 1. All address inputs must meet the specified setup and hold times for all rising clock edges whenever ADSC and/or ADSP is sampled low and CS is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.

- 2. Both chip selects must be active whenever ADSC or ADSP is sampled low in order for the this device to remain enabled.
- 3. ADSC or ADSP must not be asserted for at least 2 Clock after leaving ZZ state.

TIMING WAVEFORM OF READ CYCLE



NOTES: $\overline{WRITE} = L$ means $\overline{GW} = L$, or $\overline{GW} = H$, $\overline{BW} = L$, $\overline{WE}x = L$ $\overline{CS} = L$ means $\overline{CS}1 = L$, $\overline{CS}2 = H$ and $\overline{CS}2 = L$ $\overline{CS} = H$ means $\overline{CS}1 = H$, or $\overline{CS}1 = L$ and $\overline{CS}2 = H$, or $\overline{CS}1 = L$, and $\overline{CS}2 = L$

KM732V596A/L

Data In

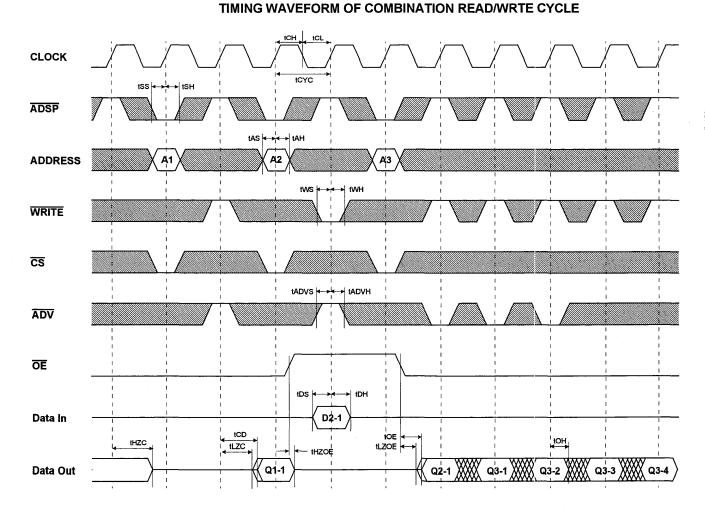
Data Out

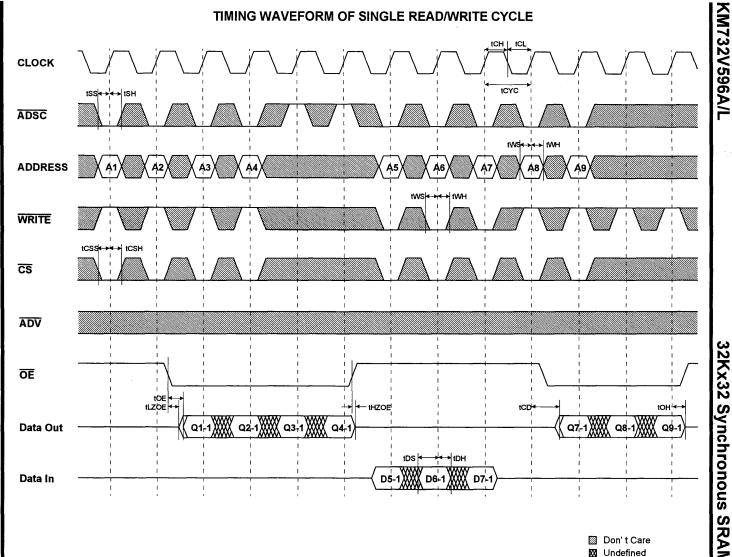
←→ tHZOE

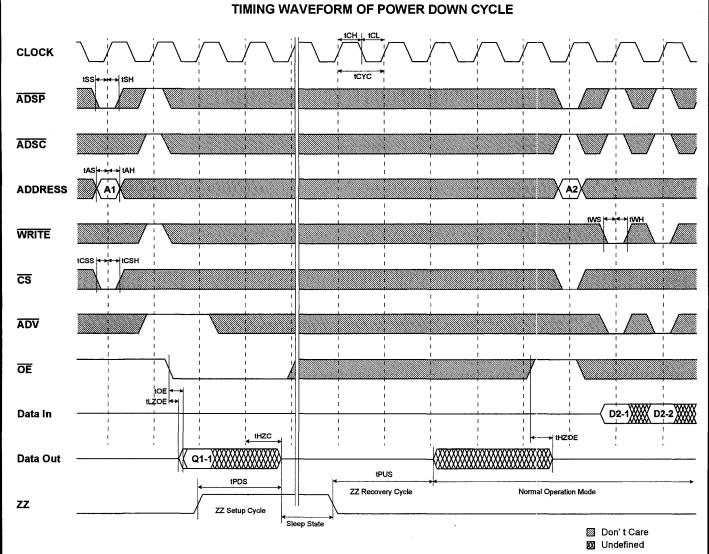
Don't Care

Undefined

SAMSUNG ELECTRONICS



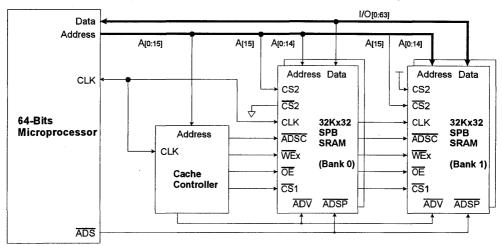




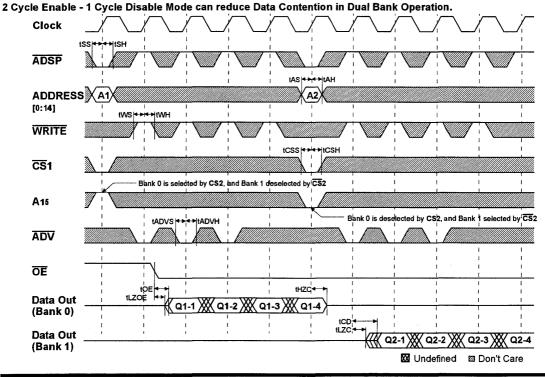
APPLICATION INFORMATION

DEPTH EXPANSION

The Samsung 32Kx32 Synchronous Pipelined Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 32K depth to 64K depth without extra logic.



INTERLEAVE READ TIMING (Refer to non-interleave write timing for interleave write timing)





32Kx32-Bit Synchronous Pipelined Burst SRAM

FEATURES

- · Synchronous Operation.
- 2 Stage Pipelined operation with 4 Burst.
- · On-Chip Address Counter.
- · Self-Timed Write Cycle.
- · On-Chip Address and Control Registers.
- Core Supply Voltage : $3.3V \pm 5\%$
- 5V Tolerant Inputs except I/O Pins
- I/O Supply Voltage: 2.5V+0.4/-0.13V.
- · Byte Writable Function.
- · Global Write Enable Controls a full bus-width write.
- · Power Down State via ZZ Signal.
- LBO Pin allows a choice of either a interleaved burst or a linear burst.
- Three Chip Enables for simple depth expansion with No Data Contention; 2 cycle Enable, 1 cycle Disable.
- · Asynchronous Output Enable Control.
- . ADSP, ADSC, ADV Burst Control Pins.
- . TTL-Level Three-State Output.
- 100-Pin TQFP Package

FAST ACCESS TIMES

Parameter	Symbol	-6	-7	-8	-10	Unit
Cycle Time	tCYC	6.6	7.5	8.6	10	ns
Clock Access Time	tCD	4.4	5.0	5.0	5.5	ns
Output Enable Access Time	tOE	4.8	4.8	5.0	5.5	ns

GENERAL DESCRIPTION

The KM732V595A/L is a 1,048,576 bit Synchronous Static Random Access Memory designed for high performance second level cache of Pentium and Power PC based System.

It is organized as 32K words of 32 bits and integrates address and control registers, a 2-bit burst address counter and added some new functions for high performance cache RAM applications; GW, BW, LBO, ZZ.

Write cycles are internally self-timed and synchronous.

Full bus-width write is done by \overline{GW} , and each byte write is performed by the combination of $\overline{WE}x$ and \overline{BW} when \overline{GW} is high. And with $\overline{CS1}$ high, \overline{ADSP} is blocked to control signals.

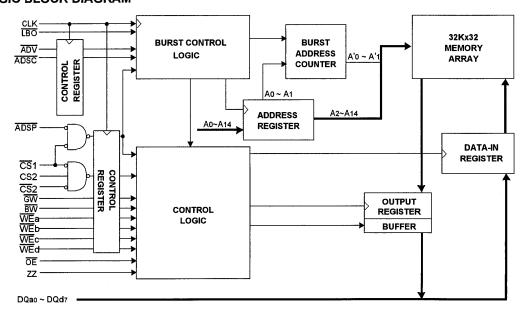
Burst cycle can be initiated with either the address status processor(ADSP) or address status cache controller(ADSC) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance(ADV) input.

LBO pin is DC operated and determines burst sequence (linear or interleaved).

ZZ pin controls Power Down State and reduces Stand-by current regardless of CLK.

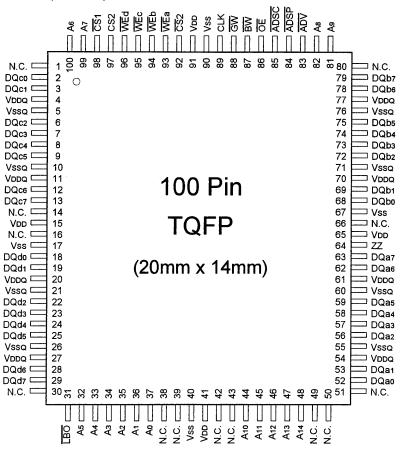
The KM732V595A/L is fabricated using SAMSUNG's high performance CMOS technology and is available in a 100pin TQFP package. Multiple power and ground pins are utilized to minimize ground bounce.

LOGIC BLOCK DIAGRAM





PIN CONFIGURATION (TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A14	Address Inputs	32,33,34,35,36,37,	VDD	Power Supply(+3.3V)	15,41,65,91
	•	44,45,46,47,48,81,	Vss	Ground	17,40,67,90
		82,99,100	N.C.	No Connect	1,14,16,30,38,39,42,43,
ĀDV	Burst Address Advance	83	1		49,50,51,66,80
ADSP	Address Status Processor	84	DQa0 ~ a7	Data Inputs/Outputs	52,53,56,57,58,59,62,63
ADSC	Address Status Controller	85	DQb0 ~ b7		68,69,72,73,74,75,78,79
CLK	Clock	89	DQc0 ~ c7		2,3,6,7,8,9,12,13
CS1	Chip Select	98	DQdo ~ d7		18,19,22,23,24,25,28,29
CS2	Chip Select	97	VDDQ	Output Power Supply	4,11,20,27,54,61,70,77
CS 2	Chip Select	92		(+2.5V)	
WEx	Byte Write Inputs	93,94,95,96	Vssq	Output Ground	5,10,21,26,55,60,71,76
ŌĒ	Output Enable	86			
Ġ₩	Global Write Enable	88			
BW	Byte Write Enable	87			
ZZ	Power Down Input	64	1		
LBO	Burst Mode Control	31			

FUNCTION DESCRIPTION

The KM732V595A/L is a synchronous SRAM designed to support the burst address accessing sequence of the P6 and Power PC based microprocessor. All inputs (with the exception of \overline{OE} and ZZ) are sampled on rising clock edges. The start and duration of the burst access is controlled by $\overline{CS1}$, \overline{ADSC} , \overline{ADSC} and \overline{ADV} .

The accesses are enabled with the chip select signals and output enabled signals. Wait states are inserted into the access with ADV.

When ZZ is pulled high, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM normally operates after 2 cycles of wake up time. ZZ pin is pulled down internally.

Read cycles are initiated with \overline{ADSP} (regardless of \overline{WEx} and \overline{ADSC}) using the new external address clocked into the on-chip address register whenever \overline{ADSP} is sampled low, the chip selects are sampled active, and the output buffer is enabled with \overline{OE} . In read operation the data of cell array accessed by the current address, registered in the Data-out registers by the positive edge of CLK, are carried to the Data-out buffer by the next positive edge of CLK. The data, registered in the Data-out buffer, are projected to the output pins. \overline{ADV} is ignored on the clock edge that samples \overline{ADSP} asserted, but is sampled on the subsequent clock edges. The address increases internally for the next access of the burst when \overline{WEx} are sampled High and \overline{ADV} is sampled low. And \overline{ADSP} is blocked to control signals by disabling $\overline{CS1}$.

All byte write is done by \overline{GW} (regardless of \overline{BW} and \overline{WEx} .), and each byte write is performed by the combination of \overline{BW} and \overline{WEx} when \overline{GW} is high.

Write cycles are performed by disabling the output buffers with \overline{OE} and asserting \overline{WEx} . \overline{WEx} are ignored on the clock edge that samples \overline{ADSP} low, but are sampled on the subsequent clock edges. The output buffers are disabled when \overline{WEx} are sampled Low(regardless of \overline{OE}). Data is clocked into the data input register when \overline{WEx} sampled Low. The address increases internally to the next address of burst, if both \overline{WEx} and \overline{ADV} are sampled Low. Individual byte write cycles are performed by any one or more byte write enable signals(\overline{WEa} , \overline{WEb} , \overline{WEc} or \overline{WEd}) sampled low. The \overline{WEa} controls DQao ~ DQar, \overline{WEb} controls DQbo ~ DQbr, \overline{WEc} controls DQco ~ DQcr, and \overline{WEd} controls DQdo ~ DQdr. Read or write cycle may also be initiated with \overline{ADSC} , instead of \overline{ADSP} . The differences between cycles initiated with \overline{ADSC} and \overline{ADSP} as are follows:

ADSP must be sampled high when ADSC is sampled low to initiate a cycle with ADSC.

WEx are sampled on the same clock edge that sampled ADSC low(and ADSP high).

Addresses are generated for the burst access as shown below, The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the LBO pin. When this pin is Low, linear burst sequence is selected. When this pin is High, Interleaved burst sequence is selected.

BURST SEQUENCE TABLE

(Interleaved Burst)

TRO DIN LIGH	Case 1		Case 2		Case 3		Case 4	
LBO FIN IIIGII	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
ļ .	0	1	0	0	1	1	1	0
1 1	1	0	1	1	0	0	0	1
Fourth Address	1	1	1	0	0	1	0	0

(Linear Burst)

LBO PIN LOW	Cas	Case 1		Case 2		Case 3		Case 4	
LBO FIN LOW	A1	A0	A1	A0	A1	A0	A1	A0	
First Address	0	0	0	1	1	0	1	1	
	0	1	1	0	1	1	0	0	
	1	0	1	1	0	0	0	1.	
Fourth Address	1	1	0	0	0	1	1	0	

NOTE: 1. LBO pin must be tied to High or Low, and Floating State must not be allowed.



TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

CS1	CS2	CS2	ADSP	ADSC	ADV	WRITE	CLK	Address Accessed	Operation
Н	Х	Х	Х	L	X	Х	1	N/A	Not Selected
L	L	Х	L	Х	Χ	X	1	N/A	Not Selected
L	Х	Н	L	Х	X	Х	1	N/A	Not Selected
L	L	Х	X	L	Χ	Х	1	N/A	Not Selected
L	Х	H	Х	L	Х	Х	1	N/A	Not Selected
L	Н	L	· L	Х	Χ	Х	1	External Address	Begin Burst Read Cycle
L	Н	L	Н	٦	Х	L	1	External Address	Begin Burst Write Cycle
L	Н	L	Н	L	X	Н	1	External Address	Begin Burst Read Cycle
Х	Х	Х	Н	H	L	Н	1	Next Address	Continue Burst Read Cycle
Н	Х	Х	Х	Н	L	Н	1	Next Address	Continue Burst Read Cycle
Х	Х	Х	Н	I	L	L	1	Next Address	Continue Burst Write Cycle
Н	Х	Х	Х	Н	L	L	1	Next Address	Continue Burst Write Cycle
Х	Х	Х	Н	Н	Н	Н	1	Current Address	Suspend Burst Read Cycle
Н	Х	Х	Х	Н	Н	Н	1	Current Address	Suspend Burst Read Cycle
Х	Х	Х	Н	Н	Н	L	1	Current Address	Suspend Burst Write Cycle
Н	Х	Х	Х	Н	Н	L	1	Current Address	Suspend Burst Write Cycle

NOTE: 1. X means "Don't Care".

- 2. The rising edge of clock is symbolized by 1.
- WRITE = L means Write operation in WRITE TRUTH TABLE.
 WRITE = H means Read operation in WRITE TRUTH TABLE.
- 4. Operation finally depends on status of asynchronous input pins(ZZ and \overline{OE}).

WRITE TRUTH TABLE

GW	BW	WEa	WEb	WEc	WEd	Operation
Н	Н	Х	Х	Х	Х	READ
Н	L	Н	Н	Н	Н	READ
Н	L	L	Н	Н	Н	WRITE BYTE a
Н	L	Н	L	Н	Н	WRITE BYTE b
Н	L	Н	Н	L	L	WRITE BYTE c and d
Н	L	L	L	L	L	WRITE ALL BYTEs
L	Х	Х	Х	Х	Х	WRITE ALL BYTEs

NOTE: 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(1).

ASYNCHRONOUS TRUTH TABLE

(See Notes 1 and 2):

Operation	ZZ	ŌĒ	I/O Status
Sleep Mode	Н	Х	High-Z
Dood	L	L	DQ
Read	L	Н	High-Z
Write	L	Х	Din, High-Z
Deselected	L	Х	High-Z

NOTE

- 1. X means "Don't Care".
- 2. ZZ pin is pulled down internally
- 3. For write cycles that following read cycles, the output buffers must be disabled with \overline{OE} , otherwise data bus contention will occur.
- Sleep Mode means power down state of which stand-by current does not depend on cycle time.
- Deselected means power down state of which stand-by current depends on cycle time.



PASS-THROUGH TRUTH TABLE

Previous Cycle		Presen	t Cycle			Name Court	
Operation	WRITE	Operation CS		1 WRITE OF		Next Cycle	
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	Initiate Read Cycle Address=An Data=Qn-1 for all bytes	L	н	L	Read Cycle Data=Qn	
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=Qn-1 for all bytes	н	Н	L	No carryover from previous cycle	
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=High-Z	н	н	Н	No carryover from previous cycle	
Write Cycle, One byte Address=An-1, Data=Dn-1	One L	Initiate Read Cycle Address=An Data=Qn-1 for one byte	L	н	L	Read Cycle Data=Qn	
Write Cycle, One byte Address=An-1, Data=Dn-1	One L	No new cycle Data=Qn-1 for one byte	Н	н	L	No carryover from previous cycle	

NOTE: This operation makes written data immediately available at output during a read cycle preceded by a write cycle.

ABSOLUTE MAXIMUM RATING*

Parameter	Symbol	Rating	Unit
Voltage on VDD Supply Relative to Vss	VDD	-0.3 to 4.6	٧
Voltage on VDDQ Supply Relative to Vss	VDDQ	VDD	٧
Voltage on Input Pin Relative to Vss	VIN	-0.3 to 6.0	V
Voltage on I/O Pin Relative to Vss	Vio	-0.3 to VDDQ + 0.5	٧
Power Dissipation	Po	1.2	W
Storage Temperature	Тѕтҫ	-65 to 150	°C
Operating Temperature	Topr	0 to 70	°C
Storage Temperature Range Under Bias	TBIAS	-10 to 85	°C

*NOTE: Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS (0° \leq TA \leq 70°C)

Parameter	Symbol	Min		Max	Unit
Supply Voltage	VDD	3.13	3.3	3.47	V
	VDDQ	2.37	2.5	2.9	٧
Ground	Vss	0	0	0	V

CAPACITANCE*(TA = 25°C, f = 1MHz)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	Cin	VIN=0V	-	5	pF
Output Capacitance	Cout	Vout=0V	-	7	pF

*NOTE: Sampled not 100% tested.



DC ELECTRICAL CHARACTERISTICS

 $(VDD=3.3V\pm5\%, VDDQ=2.5V+0.4V/-0.13V \text{ or TA} = 0^{\circ}C \text{ to } 70^{\circ}C)$

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current(except ZZ)	lıL	VDD = Vss to VDD , VIN = Vss to VD	D	-2	+2	μA
Output Leakage Current	loL	Output Disabled, Vout = Vss to VDD	-2	+2	μA	
		D	-6	-	290	mA
Operating Current	lcc	Device Selected, louт = 0mA, ZZ≤ViL, All Inputs = ViL or ViH	-7	-	270	
Operating Current	ICC	Cycle Time ≥ tCYC min	-8	-	260	
		Cycle Time = 1010 min	-10	•	240	
	Isa	Device deselected, IouT = 0mA, ZZ ≤ ViL, f = Max,	-6	-	70	mA
0	155	All Inputs \leq 0.2V or \geq VDD-0.2V	-7/8/10	-	60	
	IsB1	Device deselected, Iou τ = 0mA, $ZZ \le 0.2V$, f = 0.		-	10	mA
Standby Current	1361	All Inputs=fixed (Vpp-0.2V or 0.2V)	L-Ver.	•	1.0	mA
	IsB2	Device deselected, IouT = 0mA, ZZ≥VDD-0.2V, f = Max,		-	10	mA
	1582	All Inputs≤ViL or ≥ViH	L-Ver.	-	500	μА
Output Low Voltage	Vol	loL = 1.0mA	-	0.4	V	
Output High Voltage	Voн	Iон = -1.0mA	2.0	-	٧	
Input Low Voltage	VIL			-0.3*	0.7	V
Input High Voltage	ViH			1.7	5.5**	V

^{*} VIL(min) = -3.0(Pulse Width \le 20ns)

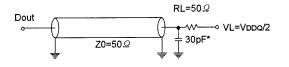
TEST CONDITIONS

(TA = 0°C to 70°C, VDD=3.3V \pm 5%, VDDQ=2.5V+0.4V/-0.13V, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 2.5V
Input Rise and Fall Time(Measured at 0.3V and 2.1V)	2ns
Input and Output Timing Reference Levels	VDDQ/2
Output Load	See Fig. 1

Output Load(A)

Output Load(B) (for tLZC, tLZOE, tHZOE& tHZC)



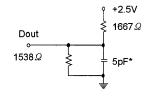


Fig. 1



^{**} In Case of I/O Pins, the Max. VIH = VDDQ + 0.5V

^{*} Capacitive Load consists of all components of the test environment.

^{*} Including Scope and Jig Capacitance

AC TIMING CHARACTERISTICS

(VDD=3.3V \pm 5%, VDDQ=2.5V+0.4V/-0.13V, TA = 0°C to 70°C)

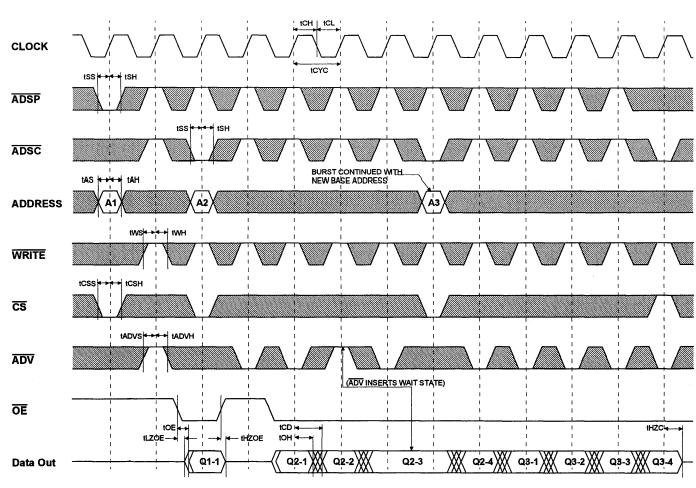
Parameter	Symbol	KM732	V595A-6	KM732\	/696A-7	KM732	/595A-8	KM732V595A-10		Unit
rarameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Cycle Time	tCYC	6.6	-	7.5	-	8.6	-	10	-	ns
Clock Access Time	tCD	-	4.4	-	5.0	-	5.0	-	5.5	ns
Output Enable to Data Valid	tOE	-	4.8	-	4.8	. -	5.0	-	5.5	ns
Clock High to Output Low-Z	tLZC	0	-	0	-	0	-	0	-	ns
Output Hold from Clock High	tOH	1.5	-	1.5	-	1.5	-	2.0	-	ns
Output Enable Low to Output Low-Z	tLZOE	0	-	0	-	0	-	0	-	ns
Output Enable High to Output High-Z	tHZOE	-	4.0	-	4.0	-	4.0	-	4.0	ns
Clock High to Output High-Z	tHZC	1.5	5.0	1.5	5.0	1.5	5.0	1.5	5.0	ns
Clock High Pulse Width	tCH	2.5	-	2.5	-	2.5	-	3.0	-	ns
Clock Low Pulse Width	tCL	2.5	-	2.5	-	2.5	-	3.0	-	ns
Address Setup to Clock High	tAS	2.0	-	2.0	-	2.0	-	2.0	-	ns
Address Status Setup to Clock High	tSS	2.0	-	2.0	-	2.0	-	2.0	-	ns
Data Setup to Clock High	tDS	2.0	-	2.0	-	2.0	-	2.0	-	ns
Write Setup to Clock High (GW, BW, WEx)	tWS	2.0	-	2.0	-	2.0	-	2.0	-	ns
Address Advance Setup to Clock High	tADVS	2.0	-	2.0	-	2.0	-	2.0	-	ns
Chip Select Setup to Clock High	tCSS	2.0	-	2.0	-	2.0	-	2.0	-	ns
Address Hold from Clock High	tAH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Address Status Hold from Clock High	tSH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Data Hold from Clock High	tDH	0.5	-	0.5	-	0.5		0.5	-	ns
Write Hold from Clock High (GW, BW, WEx)	tWH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	tADVH	0.5	-	0.5	-	0.5		0.5	-	ns
Chip Select Hold from Clock High	tCSH	0.5	-	0.5	-	0.5	-	0.5	-	ns
ZZ High to Power Down	tPDS	2	-	2	-	2	-	2	-	cycle
ZZ Low to Power Up	tPUS	2	-	2	-	2	-	2	-	cycle

NOTE: 1. All address inputs must meet the specified setup and hold times for all rising clock edges whenever ADSC and/or ADSP is sampled low and CS is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.

2. Both chip selects must be active whenever ADSC or ADSP is sampled low in order for the this device to remain enabled.

3. ADSC or ADSP must not be asserted for at least 2 Clock after leaving ZZ state.

TIMING WAVEFORM OF READ CYCLE



NOTES: WRITE = L means \overline{GW} = L, or \overline{GW} = H, \overline{BW} = L, \overline{WE} x = L \overline{CS} = L means \overline{CS} 1 = L, \overline{CS} 2 = H and \overline{CS} 2 = L \overline{CS} 5 = H means \overline{CS} 1 = H, or \overline{CS} 1 = L and \overline{CS} 2 = H, or \overline{CS} 1 = L, and \overline{CS} 2 = L

Don't Care Undefined

tDH

Don't Care

☑ Undefined

ŌĒ

Data In

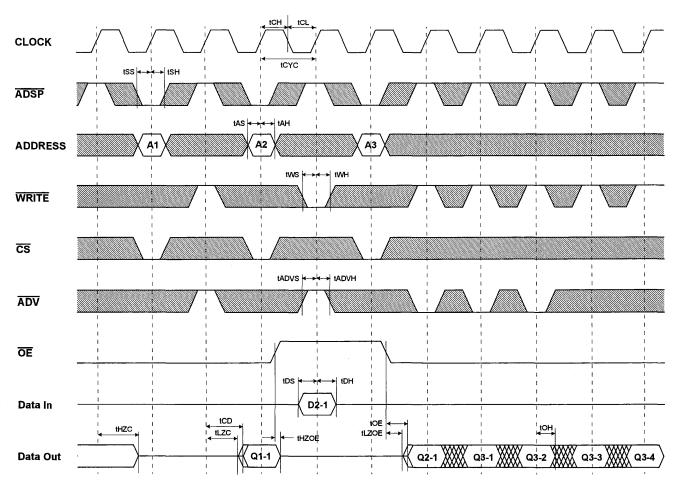
Data Out

←→ tHZOE

Q0-4

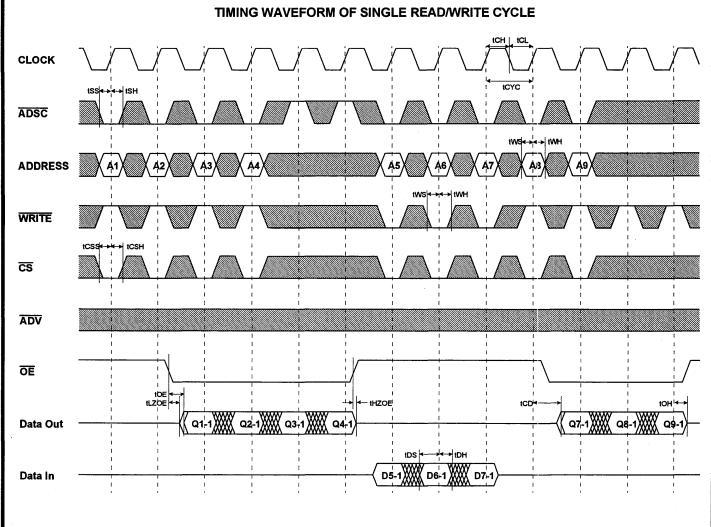
Q0-3

TIMING WAVEFORM OF COMBINATION READ/WRTE CYCLE

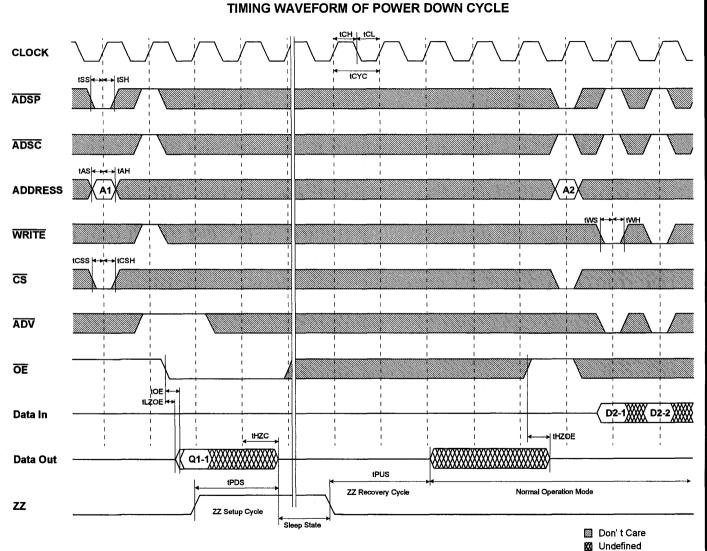


Don't Care Undefined





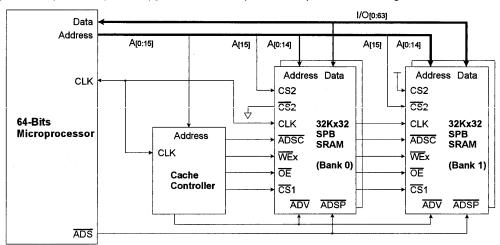
KM732V595A/L



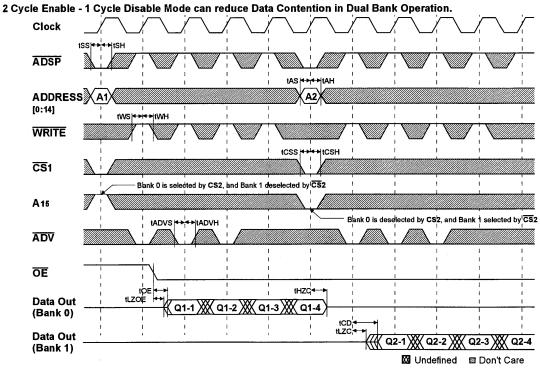
APPLICATION INFORMATION

DEPTH EXPANSION

The Samsung 32Kx32 Synchronous Pipelined Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 32K depth to 64K depth without extra logic.



INTERLEAVE READ TIMING (Refer non-interleave write timing for interleave write timing)



32Kx32-Bit Synchronous Pipelined Burst SRAM

FEATURES

- · Synchronous Operation.
- · 2 Stage Pipelined operation with 4 Burst.
- · On-Chip Address Counter.
- · Self-Timed Write Cycle.
- · On-Chip Address and Control Registers.
- VDD = 3.3V-5%/+10% Power Supply
- . 5V Tolerant Inputs except I/O Pins
- . Byte Writable Function.
- · Global Write Enable Controls a full bus-width write.
- · Power Down State via ZZ Signal.
- TBO Pin allows a choice of either a interleaved burst or a linear burst.
- Three Chip Enables for simple depth expansion with No Data Contention; 2 cycle Enable, 1 cycle Disable.
- · Asynchronous Output Enable Control.
- . ADSP, ADSC, ADV Burst Control Pins.
- . TTL-Level Three-State Output.
- 100-Pin TQFP Package

FAST ACCESS TIMES

Parameter	Symbol	-7	-8	-10	Unit
Cycle Time	tCYC	7.5	8.6	10	ns
Clock Access Time	tCD	4.5	5.0	5.0	ns
Output Enable Access Time	tOE	4.5	5.0	5.0	ns

GENERAL DESCRIPTION

The KM732V599A/L is a 1,048,576-bit Synchronous Static Random Access Memory designed for high performance second level cache of Pentium and Power PC based System.

It is organized as 32K words of 32 bits and integrates address and control registers, a 2-bit burst address counter and added some new functions for high performance cache RAM applications; GW, BW, LBO, ZZ.

Write cycles are internally self-timed and synchronous.

Full bus-width write is done by \overline{GW} , and each byte write is performed by the combination of $\overline{WE}x$ and \overline{BW} when \overline{GW} is high. And with $\overline{CS1}$ high, \overline{ADSP} is blocked to control signals.

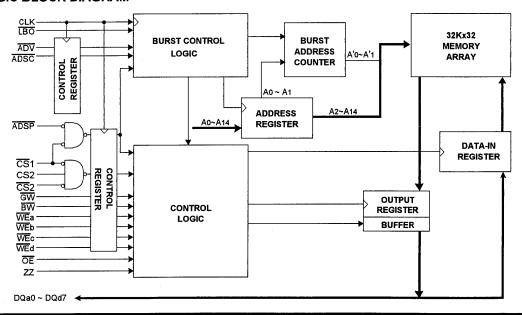
Burst cycle can be initiated with either the address status processor(ADSP) or address status cache controller(ADSC) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance(ADV) input.

LBO pin is DC operated and determines burst sequence(linear or interleaved).

ZZ pin controls Power Down State and reduces Stand-by current regardless of CLK.

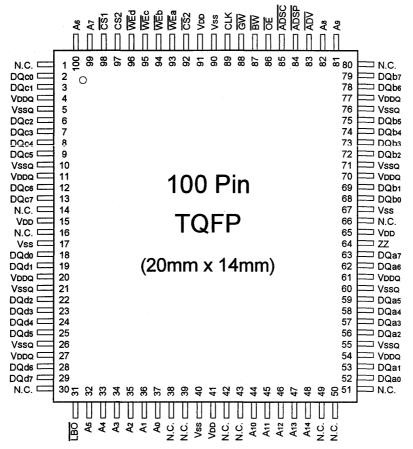
The KM732V599A/L is fabricated using SAMSUNG's high performance CMOS technology and is available in a 100pin TQFP package. Multiple power and ground pins are utilized to minimize ground bounce.

LOGIC BLOCK DIAGRAM





PIN CONFIGURATION(TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A14	Address Inputs	32,33,34,35,36,37,	VDD	Power Supply(+3.3V)	15,41,65,91
		44,45,46,47,48,81,	Vss	Ground	17,40,67,90
		82,99,100	N.C.	No Connect	1,14,16,30,38,39,42,43,
ADV	Burst Address Advance	83	1		49,50,51,66,80
ADSP	Address Status Processor	84	DQa0 ~ a7	Data Inputs/Outputs	52,53,56,57,58,59,62,63
ADSC	Address Status Controller	85	DQb0 ~ b7		68,69,72,73,74,75,78,79
CLK	Clock	89	DQc0 ~ c7	,	2,3,6,7,8,9,12,13
CS1	Chip Select	98	DQd0 ~ d7		18,19,22,23,24,25,28,29
CS2	Chip Select	97			
CS2	Chip Select	92	VDDQ	Output Power Supply	4,11,20,27,54,61,70,77
WEx	Byte Write Inputs	93,94,95,96	į.	(+3.3V)	1
ŌĒ	Output Enable	86	Vssq	Output Ground	5,10,21,26,55,60,71,76
Ġ₩	Global Write Enable	88	1		
BW	Byte Write Enable	87	1		
ZZ	Power Down Input	64			
LBO	Burst Mode Control	31			

FUNCTION DESCRIPTION

The KM732V599A/L is a synchronous SRAM designed to support the burst address accessing sequence of the P6 and Power PC based microprocessor. All inputs (with the exception of \overline{OE} and ZZ) are sampled on rising clock edges. The start and duration of the burst access is controlled by \overline{CS} 1, \overline{ADSC} , \overline{ADSP} and \overline{ADV} . The accesses are enabled with the chip select signals and output enabled signals. Wait states are inserted into the access with \overline{ADV} .

When ZZ is pulled high, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM normally operates after 2 cycles of wake up time. ZZ pin is pulled down internally.

Read cycles are initiated with $\overline{\text{ADSP}}$ (regardless of $\overline{\text{WEx}}$ and $\overline{\text{ADSC}}$) using the new external address clocked into the on-chip address register whenever $\overline{\text{ADSP}}$ is sampled low, the chip selects are sampled active, and the output buffer is enabled with $\overline{\text{OE}}$. In read operation the data of cell array accessed by the current address, registered in the Data-out registers by the positive edge of CLK, are carried to the Data-out buffer by the next positive edge of CLK. The data, registered in the Data-out buffer, are projected to the output pins. $\overline{\text{ADV}}$ is ignored on the clock edge that samples $\overline{\text{ADSP}}$ asserted, but is sampled on the subsequent clock edges. The address increases internally for the next access of the burst when $\overline{\text{WEx}}$ are sampled High and $\overline{\text{ADV}}$ is sampled low. And $\overline{\text{ADSP}}$ is blocked to control signals by disabling $\overline{\text{CS}}1$.

All byte write is done by \overline{GW} (regardless of \overline{BW} and $\overline{WE}x$.), and each byte write is performed by the combination of \overline{BW} and $\overline{WE}x$ when \overline{GW} is high.

Write cycles are performed by disabling the output buffers with \overline{OE} and asserting \overline{WEx} . \overline{WEx} are ignored on the clock edge that samples \overline{ADSP} low, but are sampled on the subsequent clock edges. The output buffers are disabled when \overline{WEx} are sampled Low(regardless of \overline{OE}). Data is clocked into the data input register when \overline{WEx} sampled Low. The address increases internally to the next address of burst, if both \overline{WEx} and \overline{ADV} are sampled Low. Individual byte write cycles are performed by any one or more byte write enable signals(\overline{WEa} , \overline{WEb}), \overline{WEc} or \overline{WEd}) sampled low. The \overline{WEa} controls DQao \sim DQa7, \overline{WEb} controls DQbo \sim DQb7, \overline{WEc} controls DQco \sim DQc7, and \overline{WEd} 0 controls DQdo \sim DQd7. Read or write cycle may also be initiated with \overline{ADSC} , instead of \overline{ADSP} . The differences between cycles initiated with \overline{ADSC} and \overline{ADSP} as are follows;

ADSP must be sampled high when ADSC is sampled low to initiate a cycle with ADSC. WEx are sampled on the same clock edge that sampled ADSC low(and ADSP high).

Addresses are generated for the burst access as shown below, The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the LBO pin. When this pin is Low, linear burst sequence is selected. When this pin is High, Interleaved burst sequence is selected.

BURST SEQUENCE TABLE

(Interleaved Burst)

LBO PIN HIGH	Case 1		Case 2		Ca	se 3	Case 4	
LBO FIN HIGH	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
	0	1	0	0	1	1	1	0
V	1	0	1	1	0	0	0	1
Fourth Address	1	1 1	1	0	0	1	0	0

(Linear Burst)

LBO PIN LOW	Case 1		Case 2		Cas	se 3	Case 4	
EBO FIN LOW	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
	0	1	1	0	1	1	0	0
	1	0	1	1	0	0	0	1
Fourth Address	1	1	0	0	0	1	1	0

NOTE: 1. LBO pin must be tied to High or Low, and Floating State must not be allowed.



TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

CS1	CS2	CS2	ADSP	ADSC	ADV	WRITE	CLK	Address Accessed	Operation
Н	Х	Х	Х	L	Χ	Х	1	N/A	Not Selected
L	L	Х	L	Х	Χ	Х	1	N/A	Not Selected
L	Х	Н	L	Х	Х	Х	1	N/A	Not Selected
L	L	Х	Х	L	Χ	Х	1	N/A	Not Selected
L	Х	Н	Х	L	Χ	Х	1	N/A	Not Selected
L	Н	L	L	Х	Х	Х	1	External Address	Begin Burst Read Cycle
L	Н	L	Н	L	Χ	Г	1	External Address	Begin Burst Write Cycle
L	Н	L	Н	L	Х	Н	1	External Address	Begin Burst Read Cycle
Х	Х	Х	Н	Н	L	Н	1	Next Address	Continue Burst Read Cycle
Н	Х	Х	Х	Н	L	Н	1	Next Address	Continue Burst Read Cycle
Х	Х	Х	Н	Н	L	٦	1	Next Address	Continue Burst Write Cycle
Н	Х	Х	Х	Н	L	L	1	Next Address	Continue Burst Write Cycle
Х	Х	X	Н	Н	Н	H	1	Current Address	Suspend Burst Read Cycle
Н	Х	Χ	Х	Н	Н	H	1	Current Address	Suspend Burst Read Cycle
Х	Х	Х	Н	Н	Н	L	1	Current Address	Suspend Burst Write Cycle
Н	Х	Х	Х	Н	Н	L	1	Current Address	Suspend Burst Write Cycle

NOTE: 1. X means "Don't Care".

2. The rising edge of clock is symbolized by \uparrow .

3. WRITE = L means Write operation in WRITE TRUTH TABLE.

WRITE = H means Read operation in WRITE TRUTH TABLE.

4. Operation finally depends on status of asynchronous input pins(ZZ and $\overline{\text{OE}}$).

WRITE TRUTH TABLE

GW	BW	WEa	WEb	WEc	WEd	Operation
Н	Н	Х	X	X	X	READ
Н	L	Н	Н	Н	Н	READ
Н	L	L	Н	Н	Н	WRITE BYTE a
Н	L	Н	L	Н	Н	WRITE BYTE b
Н	L	Н	Н	L	L	WRITE BYTE c and d
Н	L	L	L	L	L	WRITE ALL BYTEs
L	Х	Х	Х	Х	Х	WRITE ALL BYTEs

NOTE: 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(\uparrow).

ASYNCHRONOUS TRUTH TABLE

(See Notes 1 and 2):

Operation	ZZ	ŌĒ	I/O Status
Sleep Mode	Н	Х	High-Z
· · · · · · · · · · · · · · · · · · ·	L	L	DQ
Read	L	н	High-Z
Write	L	Х	Din, High-Z
Deselected	L	Х	High-Z

NOTE

- 1. X means "Don't Care".
- 2. ZZ pin is pulled down internally
- 3. For write cycles that following read cycles, the output buffers must be disabled with \overline{OE} , otherwise data bus contention will occur.
- Sleep Mode means power down state of which stand-by current does not depend on cycle time.
- Deselected means power down state of which stand-by current depends on cycle time.



PASS-THROUGH TRUTH TABLE

Previous Cycle		Preser	Present Cycle						
Operation WRITE		Operation	CS1	CS1 WRITE		Next Cycle			
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	Initiate Read Cycle Address=An Data=Qn-1 for all bytes	L	Н	L	Read Cycle Data=Qn			
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=Qn-1 for all bytes	н	Н	L	No carryover from previous cycle			
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=High-Z	н	н	Н	No carryover from previous cycle			
Write Cycle, One byte Address=An-1, Data=Dn-1	One L	Initiate Read Cycle Address=An Data=Qn-1 for one byte	L	Н	L	Read Cycle Data=Qn			
Write Cycle, One byte Address=An-1, Data=Dn-1	One L	No new cycle Data=Qn-1 for one byte	Н	Н	L	No carryover from previous cycle			

NOTE: 1. This operation makes written data immediately available at output during a read cycle preceded by a write cycle.

2. WEx means WEa ~ WEd.

ABSOLUTE MAXIMUM RATING*

Parameter	Symbol	Rating	Unit
Voltage on VDD Supply Relative to Vss	VDD	-0.3 to 4.6	V
Voltage on VDDQ Supply Relative to Vss	VDDQ	VDD	V
Voltage on Input Pin Relative to Vss	Vin	-0.3 to 6.0	V
Voltage on I/O Pin Relative to Vss	Vio	-0.3 to VDDQ + 0.5	V
Power Dissipation	PD	1.2	W
Storage Temperature	Тѕтс	-65 to 150	°C
Operating Temperature	Topr	0 to 70	°C
Storage Temperature Range Under Bias	TBIAS	-10 to 85	င

*NOTE: Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS $(0^{\circ} \le TA \le 70^{\circ})$

Parameter	Symbol	Min	Тур.	Max	Unit
Supply Voltage	VDD	3.13	3.3	3.6	V
	VDDQ	3.13	3.3	3.6	V
Ground	Vss	0	0	0	V

CAPACITANCE*(TA = 25°C, f = 1MHz)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	CIN	VIN=0V	-	5	pF
Output Capacitance	Соит	Vout=0V	-	7	pF

*NOTE: Sampled not 100% tested.



DC ELECTRICAL CHARACTERISTICS (VDD=3.3V-5%+10%, TA = 0 $^{\circ}$ to 70 $^{\circ}$)

Parameter	Symbol	Test Conditions		Min	Max	Unit	
Input Leakage Current(except ZZ)	İIL	VDD = Vss to VDD, VIN = Vss to VDD		-2	+2	μA	
Output Leakage Current	loL	Output Disabled, Vout = Vss to VDDQ	-2	+2	μA		
Operating Current	Icc	CC Device Selected, IouT = 0mA, ZZ≤VIL,		-	270		
•		All Inputs = VIL or VIH	-8	-	260	mA	
		Cycle Time ≥ tCYC min	-10	-	240		
Standby Current		Davise decelected lour - 0mA 77<\/i	-7	-	60		
	ISB	Device deselected, IouT = 0mA, $ZZ \le VIL$, f = Max, All Inputs $\le 0.2V$ or $\ge VDD-0.2V$	-8	-	60	mA	
		1 - Wax, All Iliputs - 0.24 of - 455-0.24	-10	-	60		
	IsB1	Device deselected, louт = 0mA, IsB1 ZZ≤0.2V, f = 0,		-	10	mA	
	1581	All Inputs = fixed(VDD-0.2V or 0.2V)	L-Ver.	-	1.0	mA	
	IsB2	Device deselected, louт = 0mA, ZZ≥Vpp-0.2V, f = Max,		-	10	mA	
	1562	All Inputs ≤ VIL or ≥ VIH	L-Ver.	-	500	μA	
Output Low Voltage	Vol	IOL = 8.0mA	-	0.4	٧		
Output High Voltage	Vон .	IOH = -4.0mA	2.4	-	٧		
Input Low Voltage	VIL			-0.5*	0.8	٧	
Input High Voltage	VIH			2.0	5.5**	٧	

^{*} VIL(min) = -3.0(Pulse Width ≤ 20ns)

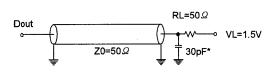
TEST CONDITIONS

(TA = 0 $^{\circ}$ C to 70 $^{\circ}$ C, VDD=3.3V-5%/+10% unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time(Measured at 0.3V and 2.7V)	2ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1

Fig. 1

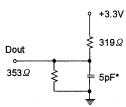




^{*} Capacitive Load consists of all components of the test environment.

(for tLZC, tLZOE, tHZOE& tHZC)

Output Load(B)



^{*} Including Scope and Jig Capacitance



^{**} In Case of I/O Pins, the Max. VIH = VDDQ + 0.5V

AC TIMING CHARACTERISTICS

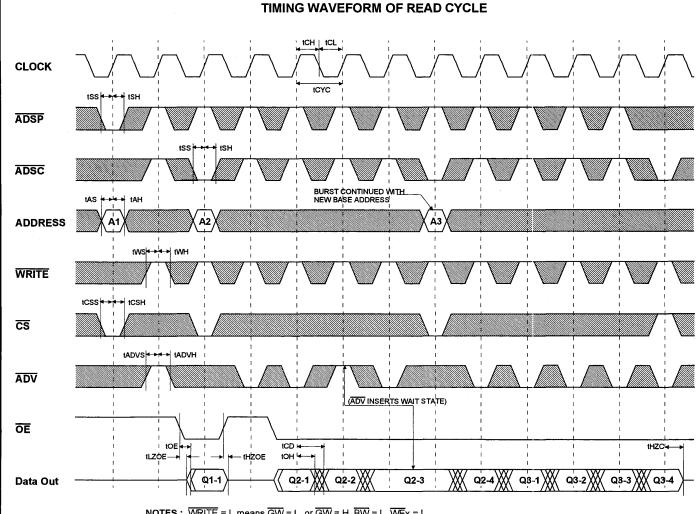
(VDD=3.3V-5%/+10%,TA=0% to 70%)

Parameter	Symbol	KM732	V599A-7	KM732	KM732V599A-8		KM732V599A-10	
Parameter	Эунооі	Min	Max	Min	Max	Min	Max	Unit
Cycle Time	tCYC	7.5	-	8.6	-	10	-	ns
Clock Access Time	tCD	-	4.5	-	5.0	-	5.0	ns
Output Enable to Data Valid	tOE	-	4.5	-	5.0	-	5.0	ns
Clock High to Output Low-Z	tLZC	0	-	0	-	0	-	ns
Output Hold from Clock High	tOH	1.5	-	1.5	-	1.5	-	ns
Output Enable Low to Output Low-Z	tLZOE	0	_	0	-	0	-	ns
Output Enable High to Output High-Z	tHZOE	-	4.0	-	4.0	-	4.0	ns
Clock High to Output High-Z	tHZC	1.5	5.0	1.5	5.0	1.5	5.0	ns
Clock High Pulse Width	tCH	2.5	-	2.5	-	3.0	-	ns
Clock Low Pulse Width	tCL	2.5	-	2.5	-	3.0	-	ns
Address Setup to Clock High	tAS	2.0	-	2.0	-	2.0	-	ns
Address Status Setup to Clock High	tSS	2.0	-	2.0	-	2.0	-	ns
Data Setup to Clock High	tDS	2.0	-	2.0	-	2.0	-	ns
Write Setup to Clock High (GW, BW, WEx)	tWS	2.0	-	2.0	-	2.0	-	ns
Address Advance Setup to Clock High	tADVS	2.0	-	2.0	-	2.0	-	ns
Chip Select Setup to Clock High	tCSS	2.0	-	2.0	-	2.0	-	ns
Address Hold from Clock High	tAH	0.5	-	0.5	-	0.5	-	ns
Address Status Hold from Clock High	tSH	0.5	-	0.5	-	0.5	-	ns
Data Hold from Clock High	tDH	0.5	-	0.5	-	0.5	-	ns
Write Hold from Clock High (GW, BW, WEx)	tWH	0.5	-	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	tADVH	0.5	-	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	tCSH	0.5	-	0.5	-	0.5	-	ns
ZZ High to Power Down	tPDS	2	-	2	-	2	-	cycle
ZZ Low to Power Up	tPUS	2	-	2	-	2	-	cycle

NOTE: 1. All address inputs must meet the specified setup and hold times for all rising clock edges whenever ADSC and/or ADSP is sampled low and CS is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.

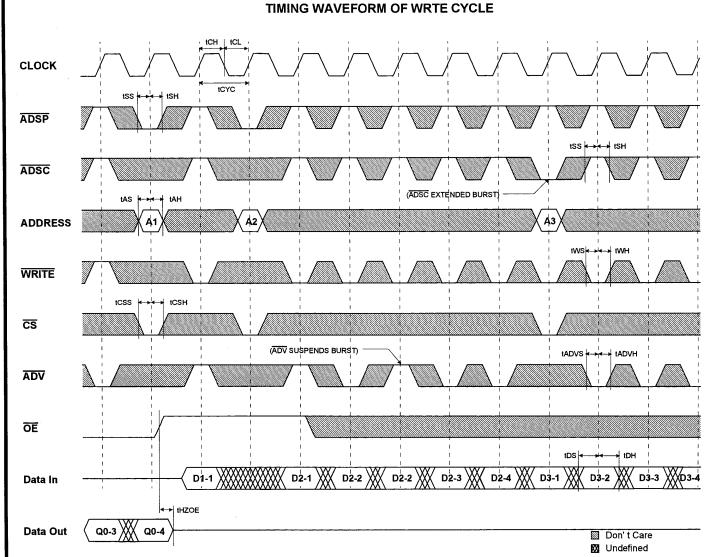
2. Both chip selects must be active whenever $\overline{\text{ADSC}}$ or $\overline{\text{ADSP}}$ is sampled low in order for the this device to remain enabled.

3. ADSC or ADSP must not be asserted for at least 2 Clock after leaving ZZ state.

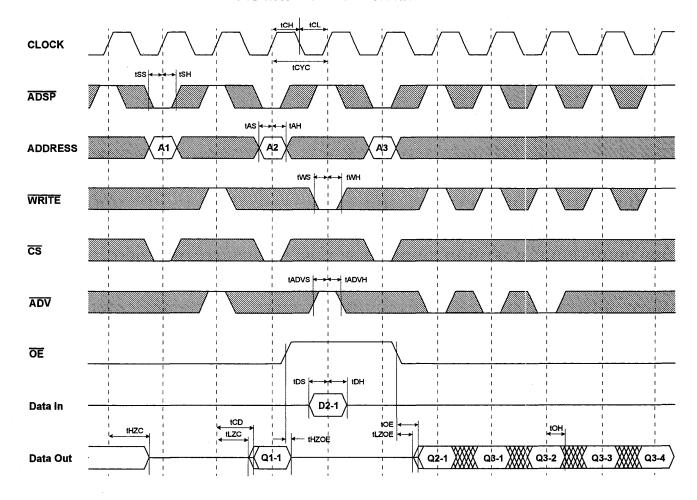


NOTES: $\overline{WRITE} = L$ means $\overline{GW} = L$, or $\overline{GW} = H$, $\overline{BW} = L$, $\overline{WE}x = L$ $\overline{CS} = L$ means $\overline{CS}1 = L$, $\overline{CS}2 = H$ and $\overline{CS}2 = L$ $\overline{CS} = H$ means $\overline{CS}1 = H$, or $\overline{CS}1 = L$ and $\overline{CS}2 = H$, or $\overline{CS}1 = L$, and $\overline{CS}2 = L$

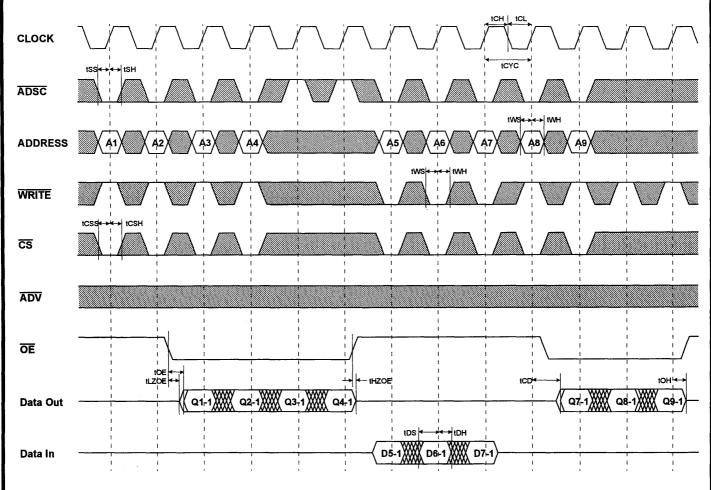
Don't Care ☑ Undefined



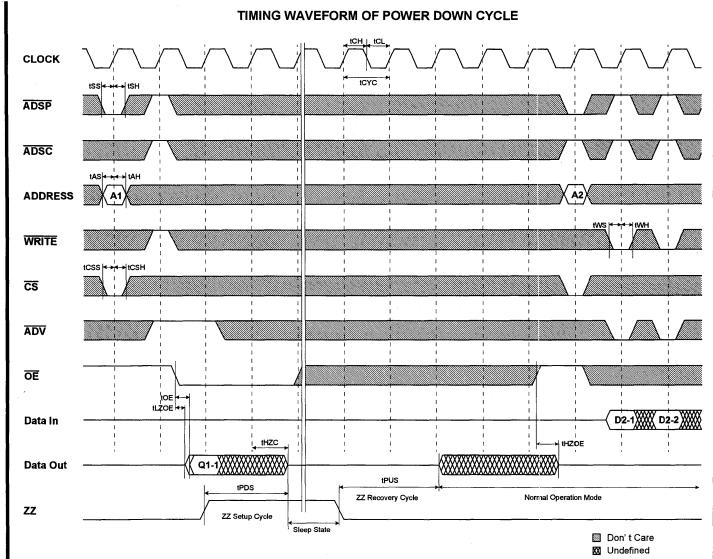
TIMING WAVEFORM OF COMBINATION READ/WRTE CYCLE



TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE



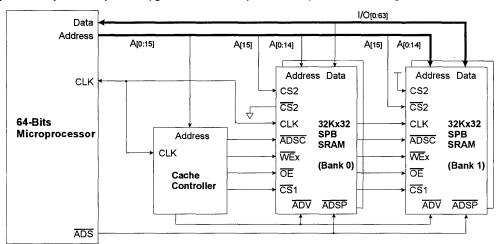
Don't Care



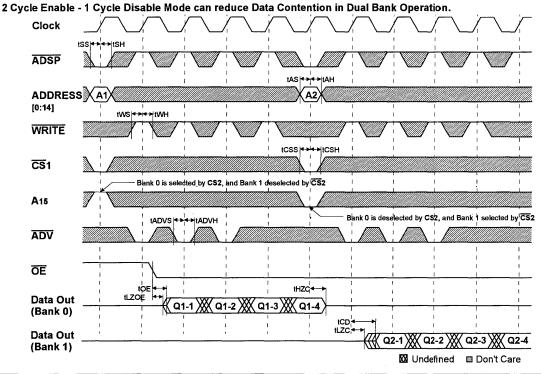
APPLICATION INFORMATION

DEPTH EXPANSION

The Samsung 32Kx32 Synchronous Pipelined Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 32K depth to 64K depth without extra logic.



INTERLEAVE READ TIMING (Refer to non-interleave write timing for interleave write timing)





32Kx36-Bit Synchronous Pipelined Burst SRAM FEATURES GENE

LAIONEO

- · Synchronous Operation.
- 2 Stage Pipelined operation with 4 Burst.
- · On-Chip Address Counter.
- Self-Timed Write Cycle.
- On-Chip Address and Control Registers.
- Core Supply Voltage: 3.3V±5%
- I/O Supply Voltage: 2.5V+0.4/-0.13V.
- . 5V Tolerant Inputs except I/O Pins
- Byte Writable Function.
- · Global Write Enable Controls a full bus-width write.
- Power Down State via ZZ Signal.
- BO Pin allows a choice of either a interleaved burst or a linear burst
- Three Chip Enables for simple depth expansion with No Data Contention: 2 cycle Enable, 1 cycle Disable.
- · Asynchronous Output Enable Control.
- ADSP, ADSC, ADV Burst Control Pins.
- TTL-Level Three-State Output.
- . 100-Pin TQFP Package

FAST ACCESS TIMES

Parameter	Symbol	-6	-7	-8	-10	Unit
Cycle Time	tCYC	6.6	7.5	8.6	10	ns
Clock Access Time	tCD	4.4	5.0	5.0	5.5	ns
Output Enable Access Time	tOE	4.8	4.8	5.0	5.5	ns

GENERAL DESCRIPTION

The KM736V595A/L is a 1,179,648 bit Synchronous Static Random Access Memory designed for high performance second level cache of Pentium and Power PC based System.

It is organized as 32K words of 36bits and integrates address and control registers, a 2-bit burst address counter and added some new functions for high performance cache RAM applications: GW. BW. LBO. ZZ.

Write cycles are internally self-timed and synchronous.

Full bus-width write is done by \overline{GW} , and each byte write is performed by the combination of $\overline{WE}x$ and \overline{BW} when \overline{GW} is high. And with $\overline{CS1}$ high. \overline{ADSP} is blocked to control signals.

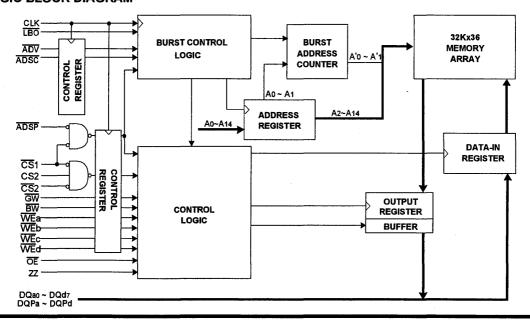
Burst cycle can be initiated with either the address status processor(ADSP) or address status cache controller(ADSC) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance(ADV) input.

LBO pin is DC operated and determines burst sequence(linear or interleaved).

ZZ pin controls Power Down State and reduces Stand-by current regardless of CLK.

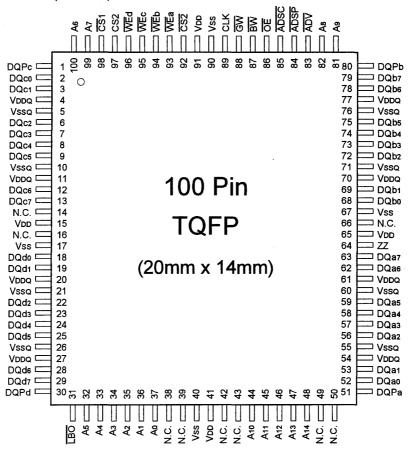
The KM736V595A/L is fabricated using SAMSUNG's high performance CMOS technology and is available in a 100pin TQFP package. Multiple power and ground pins are utilized to minimize ground bounce.

LOGIC BLOCK DIAGRAM





PIN CONFIGURATION (TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A14	Address Inputs	32,33,34,35,36,37,	VDD	Power Supply(+3.3V)	15,41,65,91
	-	44,45,46,47,48,81,	Vss	Ground	17,40,67,90
		82,99,100	N.C.	No Connect	14,16,38,39,42,43,49,50
ĀDV	Burst Address Advance	83	1		66
ADSP	Address Status Processor	84	DQa0 ~ a7	Data Inputs/Outputs	52,53,56,57,58,59,62,63
ADSC	Address Status Controller	85	DQb0 ~ b7		68,69,72,73,74,75,78,79
CLK	Clock	89	DQc0 ~ c7		2,3,6,7,8,9,12,13
CS1	Chip Select	98	DQdo ~ d7		18,19,22,23,24,25,28,29
CS2	Chip Select	97	DQPa~Pd	1	51,80,1,30
CS 2	Chip Select	92	1		
WE x	Byte Write Inputs	93,94,95,96	VDDQ	Output Power Supply	4,11,20,27,54,61,70,77
ŌĒ	Output Enable	86	ſ	(+2.5V)	1
₫₩	Global Write Enable	88	Vssq	Output Ground	5,10,21,26,55,60,71,76
₿₩	Byte Write Enable	87		1	1
ZZ	Power Down Input	64	I		
LBO	Burst Mode Control	31			

FUNCTION DESCRIPTION

The KM736V595A/L is a synchronous SRAM designed to support the burst address accessing sequence of the P6 and Power PC based microprocessor. All inputs (with the exception of \overline{OE} and ZZ) are sampled on rising clock edges. The start and duration of the burst access is controlled by $\overline{CS1}$, \overline{ADSC} , \overline{ADSC} and \overline{ADV} . The accesses are enabled with the chip select signals and output enabled signals. Wait states are inserted into the access with \overline{ADV} .

When ZZ is pulled high, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM normally operates after 2 cycles of wake up time. ZZ pin is pulled down internally.

Read cycles are initiated with \overline{ADSP} (regardless of \overline{WEx} and \overline{ADSC}) using the new external address clocked into the on-chip address register whenever \overline{ADSP} is sampled low, the chip selects are sampled active, and the output buffer is enabled with \overline{OE} . In read operation the data of cell array accessed by the current address, registered in the Data-out registers by the positive edge of CLK, are carried to the Data-out buffer by the next positive edge of CLK. The data, registered in the Data-out buffer, are projected to the output pins. \overline{ADV} is ignored on the clock edge that samples \overline{ADSP} asserted, but is sampled on the subsequent clock edges. The address increases internally for the next access of the burst when \overline{WEx} are sampled High and \overline{ADV} is sampled low. And \overline{ADSP} is blocked to control signals by disabling $\overline{CS1}$.

All byte write is done by \overline{GW} (regardless of \overline{BW} and $\overline{WE}x$.), and each byte write is performed by the combination of \overline{BW} and $\overline{WE}x$ when \overline{GW} is high.

Write cycles are performed by disabling the output buffers with \overline{OE} and asserting \overline{WEx} . \overline{WEx} are ignored on the clock edge that samples \overline{ADSP} low, but are sampled on the subsequent clock edges. The output buffers are disabled when \overline{WEx} are sampled Low(regardless of \overline{OE}). Data is clocked into the data input register when \overline{WEx} sampled Low. The address increases internally to the next address of burst, if both \overline{WEx} and \overline{ADV} are sampled Low. Individual byte write cycles are performed by any one or more byte write anales signals(\overline{WEx}), \overline{WEx}) and \overline{DE} 0 sampled low. The \overline{WEx} controls \overline{DQx} 0 and \overline{DQPx} 0, \overline{WEx} 0 controls \overline{DQx} 0 and \overline{DQPx} 0, and \overline{WEx} 0 controls \overline{DQx} 0 and \overline{DQx} 0. Read or write cycle may also be initiated with \overline{ADSC} 0, instead of \overline{ADSP} 0. The differences between cycles initiated with \overline{ADSC} 0 and \overline{ADSP} 0 as are follows;

ADSP must be sampled high when ADSC is sampled low to initiate a cycle with ADSC. WEx are sampled on the same clock edge that sampled ADSC low(and ADSP high).

Addresses are generated for the burst access as shown below, The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the LBO pin. When this pin is Low, linear burst sequence is selected. When this pin is High, Interleaved burst sequence is selected.

BURST SEQUENCE TABLE

(Interleaved Burst)

LBO PIN HIGH	Cas	Case 1		Case 2		Case 3		Case 4	
LBOFIN HIGH	A1	A0	A1	A0	A1	A0	A1	A0	
First Address	0	0	0	1	1	0	1	1	
	0	1	0	0	1	1	1	0	
1	1	0	1	1	0	0	0	1	
Fourth Address	1	1	1	0	0	1	0	0	

(Linear Burst)

LBO PIN LOW	Case 1		Case 2		Case 3		Case 4	
LBO FIN LOW	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
· ·	0	1	1	0	1	1	0	0
1	1	0	1	1	0	0	0	1
Fourth Address	1	1	0	0	0	1	1	0

NOTE: 1. LBO pin must be tied to High or Low, and Floating State must not be allowed.



TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

CS1	CS2	CS2	ADSP	ADSC	ADV	WRITE	CLK	Address Accessed	Operation
ŲН	Х	Х	Х	٦	X	Х	1	. N/A	Not Selected
L	L	Х	L	Х	Χ	Х	1	N/A	Not Selected
L	Х	Н	L	Х	Χ	Х	1	N/A	Not Selected
L	L	Х	Х	L	Χ	Х	1	N/A	Not Selected
L	Х	Н	Х	L	Х	Х	1	N/A	Not Selected
L	Н	L	L	Х	Χ	Х	1	External Address	Begin Burst Read Cycle
L	Н	L	Н	L	Χ	٦	1	External Address	Begin Burst Write Cycle
L	Н	L	Н	L	Χ	Ξ	1	External Address	Begin Burst Read Cycle
Х	Х	Х	Н	Н	L	Н	1	Next Address	Continue Burst Read Cycle
Н	Х	Х	Х	Н	L	Н	1	Next Address	Continue Burst Read Cycle
Х	Х	Х	Н	Н	L	٦	1	Next Address	Continue Burst Write Cycle
Н	Х	Х	Х	Н	L	L	1	Next Address	Continue Burst Write Cycle
Х	Х	Х	Н	Н	Н	Н	1	Current Address	Suspend Burst Read Cycle
Н	Х	Х	Х	Н	Н	Н	1	Current Address	Suspend Burst Read Cycle
Х	Х	X	Н	Н	Н	L	1	Current Address	Suspend Burst Write Cycle
Н	Х	Х	Х	Н	Н	L	1	Current Address	Suspend Burst Write Cycle

NOTE: 1. X means "Don't Care".

- 2. The rising edge of clock is symbolized by 1.
- 3. WRITE = L means Write operation in WRITE TRUTH TABLE.
 WRITE = H means Read operation in WRITE TRUTH TABLE.
- 4. Operation finally depends on status of asynchronous input pins(ZZ and \overline{OE}).

WRITE TRUTH TABLE

GW	BW	WEa	WEb	WEc	WEd	Operation
Н	Н	Х	X	Х	X	READ
Н	L	Н	. н	Н	Н	READ
Н	L	L	Н	Н	Н	WRITE BYTE a
Н	L	Н	L	Н	Н	WRITE BYTE b
Н	L	Н	Н	L	L	WRITE BYTE c and d
Н	L	L	L	L	L	WRITE ALL BYTEs
L	X	X	Х	Х	X	WRITE ALL BYTEs

NOTE: 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(\uparrow).

ASYNCHRONOUS TRUTH TABLE

(See Notes 1 and 2):

Operation	ZZ	ŌĒ	I/O Status
Sleep Mode	Н	Х	High-Z
Read	L	L	DQ
Read	L	Н	High-Z
Write	L	Х	Din, High-Z
Deselected	L	Х	High-Z

NOTE

- 1. X means "Don't Care".
- 2. ZZ pin is pulled down internally
- For write cycles that following read cycles, the output buffers must be disabled with OE, otherwise data bus contention will occur.
- Sleep Mode means power down state of which stand-by current does not depend on cycle time.
- Deselected means power down state of which stand-by current depends on cycle time.



PASS-THROUGH TRUTH TABLE

Previous Cycle		Presen	Present Cycle					
Operation WRITE		Operation	CS1	CS1 WRITE		Next Cycle		
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	Initiate Read Cycle Address=An Data=Qn-1 for all bytes	L	н	L	Read Cycle Data=Qn		
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=Qn-1 for all bytes	Н	Н	L	No carryover from previous cycle		
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=High-Z	н	н	Н	No carryover from previous cycle		
Write Cycle, One byte Address=An-1, Data=Dn-1	One L	Initiate Read Cycle Address=An Data=Qn-1 for one byte	L	н	L	Read Cycle Data=Qn		
Write Cycle, One byte Address=An-1, Data=Dn-1	One L	No new cycle Data=Qn-1 for one byte	н	н	L	No carryover from previous cycle		

NOTE: This operation makes written data immediately available at output during a read cycle preceded by a write cycle.

ABSOLUTE MAXIMUM RATING*

Parameter	Symbol	Rating	Unit	
Voltage on VDD Supply Relative to Vss	VDD	-0.3 to 4.6	V	
Voltage on VDDQ Supply Relative to Vss	VDDQ	VDD	V	
Voltage on Input Pin Relative to Vss	Vin	-0.3 to 6.0	٧	
Voltage on I/O Pin Relative to Vss	Vio	-0.3 to VDDQ + 0.5	٧	
Power Dissipation	Po	1.2	W	
Storage Temperature	Тѕтс	-65 to 150	င	
Operating Temperature	Topr	0 to 70	င	
Storage Temperature Range Under Bias	TBIAS	-10 to 85	°C	

^{*}NOTE: Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS (0° \leq TA \leq 70°C)

Parameter	Symbol	Min	Typ.	Max	Unit	
Supply Voltage	VDD	3.13	3.3	3.47	V	
	VDDQ	2.37	2.5	2.9	٧	
Ground	Vss	0	0	0	٧	

CAPACITANCE*(TA = 25°C, f = 1MHz)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	CIN	VIN=0V	-	5	pF
Output Capacitance	€out	Vo⊔T=0V	-	7	pF

*NOTE: Sampled not 100% tested.



DC ELECTRICAL CHARACTERISTICS

 $(VDD=3.3V\pm5\%, VDDQ=2.5V+0.4V/-0.13V \text{ or TA} = 0^{\circ}C \text{ to } 70^{\circ}C)$

Parameter	Symbol	Test Conditions	Min	Max	Unit	
Input Leakage Current(except ZZ)	lıL	VDD = Vss to VDD, VIN = Vss to VD	-2	+2	μA	
Output Leakage Current	loL	Output Disabled, Vout = Vss to Vo	QD	-2	+2	μA
		Davisa Salastad Jour - 0-A	-6	-	290	
Operating Current	lcc	Device Selected, lo∪т = 0mA, ZZ≤ViL, All Inputs = ViL or ViH	-7	-	270	mA
operating outlett	100	Cycle Time ≥ tCYC min	-8	-	260	
		Syste Time = 1010 min	-10	-	240	
Standby Current	IsB	Device deselected, louт = 0mA, ZZ≤ViL, f = Max,	-6	•	70	mA
	136	All Inputs $\leq 0.2V$ or $\geq VDD-0.2V$	-7/8/10	•	60	mA
	ISB1	Device deselected, lout = 0mA, ZZ≤0.2V, f = 0,		-	10	mA
	1001	All Inputs=fixed (VDD-0.2V or 0.2V)	L-Ver.	-	1.0	mA
	IsB2	Device deselected, Iouт = 0mA, ZZ ≥ Vpp-0.2V, f = Max,		-	10	mA
	1582	All Inputs ≤ VIL or ≥ VIH	L-Ver.	-	500	μA
Output Low Voltage	Vol	loL = 1.0mA	-	0.4	V	
Output High Voltage	Voн	Iон = -1.0mA		2.0	-	V
Input Low Voltage	VIL			-0.3*	0.7	٧
Input High Voltage	ViH		1.7	5.5**	٧	

^{*} VIL(min) = -3.0(Pulse Width≤20ns)

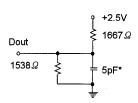
TEST CONDITIONS

(TA = 0°C to 70°C, VDD=3.3V \pm 5%, VDDQ=2.5V+0.4V/-0.13V unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 2.5V
Input Rise and Fall Time(Measured at 0.3V and 2.1V)	2ns
Input and Output Timing Reference Levels	VDDQ/2
Output Load	See Fig. 1

Output Load(A)

Output Load(B) (for tLZC, tLZOE, tHZOE& tHZC)





^{**} In Case of I/O Pins, the Max. VIH = VDDQ + 0.5V

^{*} Capacitive Load consists of all components of the test environment.

Fig. 1

^{*} Including Scope and Jig Capacitance

AC TIMING CHARACTERISTICS

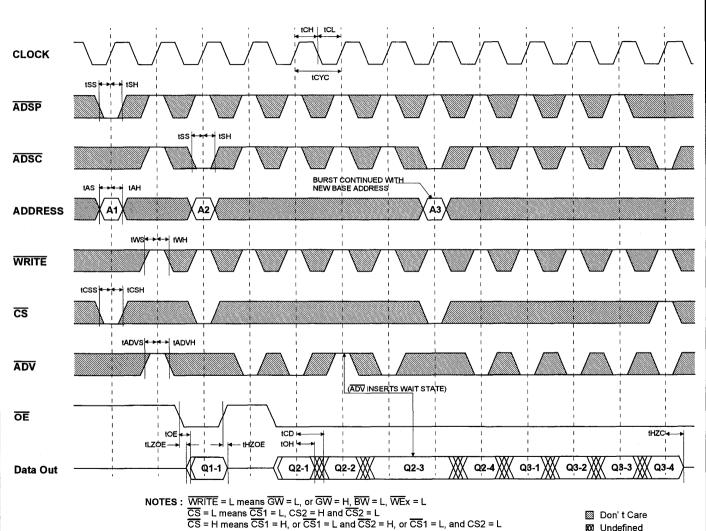
(VDD=3.3V \pm 5%, VDDQ=2.5V+0.4V/-0.13V, TA = 0°C to 70°C)

Parameter	Symbol	KM736V595A-6		KM736V595A-7		KM736V595A-8		KM736V595A-10		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Unit
Cycle Time	tCYC	6.6	-	7.5	-	8.6	-	10	-	ns
Clock Access Time	tCD	-	4.4	-	5.0	-	5.0	-	5.5	ns
Output Enable to Data Valid	tOE	-	4.8	-	4.8	-	5.0	-	5.5	ns
Clock High to Output Low-Z	tLZC	0	-	0	-	0	-	0	-	ns
Output Hold from Clock High	tOH	1.5	-	1.5	-	1.5	-	2.0	-	ns
Output Enable Low to Output Low-Z	tLZOE	0	-	0	-	0	-	0	-	ns
Output Enable High to Output High-Z	tHZOE	-	4.0	-	4.0	-	4.0	-	4.0	ns
Clock High to Output High-Z	tHZC	1.5	5.0	1.5	5.0	1.5	5.0	1.5	5.0	ns
Clock High Pulse Width	tCH	2.5	-	2.5	-	2.5	-	3.0	-	ns
Clock Low Pulse Width	tCL	2.5	-	2.5	-	2.5	-	3.0	-	ns
Address Setup to Clock High	tAS	2.0	-	2.0	-	2.0	-	2.0	-	ns
Address Status Setup to Clock High	tSS	2.0	-	2.0	-	2.0	-	2.0	-	ns
Data Setup to Clock High	tDS	2.0	-	2.0	-	2.0	-	2.0	-	ns
Write Setup to Clock High (GW, BW, WEx)	tWS	2.0	-	2.0	-	2.0	-	2.0	-	ns
Address Advance Setup to Clock High	tADVS	2.0	-	2.0	-	2.0	-	2.0	-	ns
Chip Select Setup to Clock High	tCSS	2.0	-	2.0	-	2.0	-	2.0	-	ns
Address Hold from Clock High	tAH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Address Status Hold from Clock High	tSH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Data Hold from Clock High	tDH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Write Hold from Clock High (GW, BW, WEx)	tWH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	tADVH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	tCSH	0.5	-	0.5	-	0.5	-	0.5	-	ns
ZZ High to Power Down	tPDS	2	-	2	-	2		2	-	cycle
ZZ Low to Power Up	tPUS	2	-	2	-	2	-	2	-	cycle

NOTE: 1. All address inputs must meet the specified setup and hold times for all rising clock edges whenever ADSC and/or ADSP is sampled low and CS is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.

2. Both chip selects must be active whenever ADSC or ADSP is sampled low in order for the this device to remain enabled.

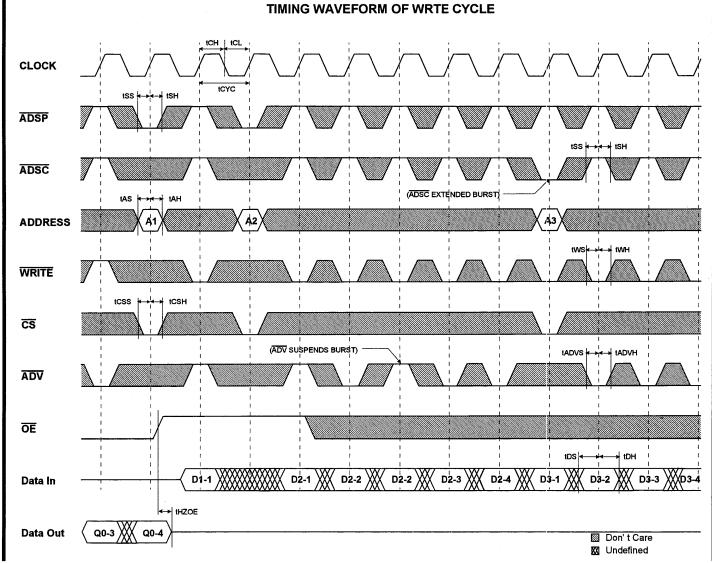
3. ADSC or ADSP must not be asserted for at least 2 Clock after leaving ZZ state.



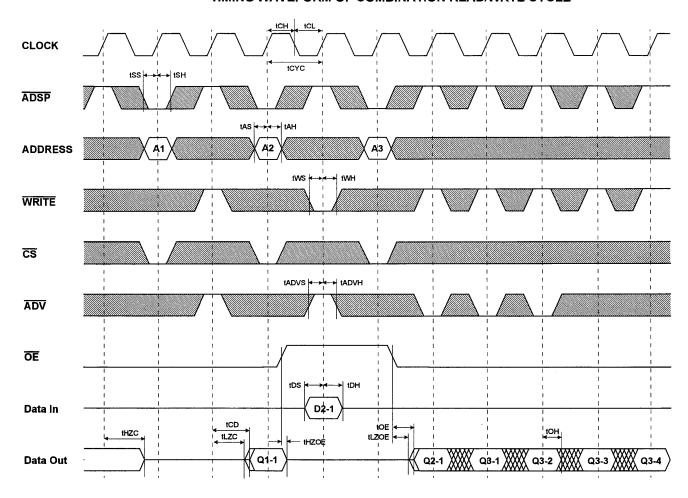
TIMING WAVEFORM OF READ CYCLE

Don't Care

☑ Undefined

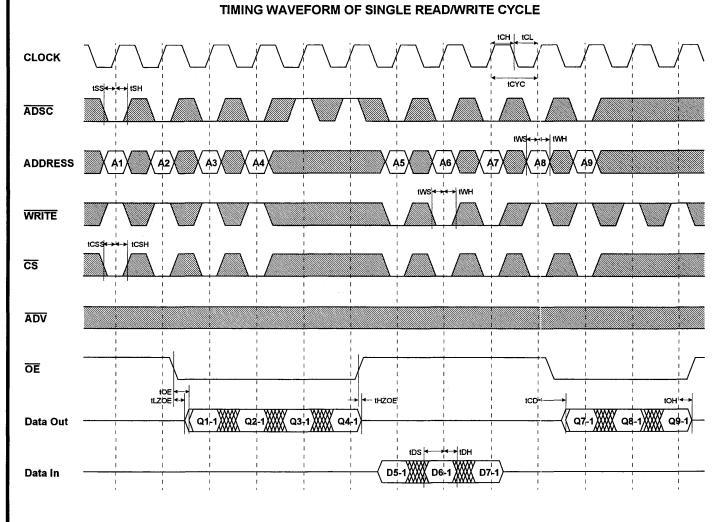


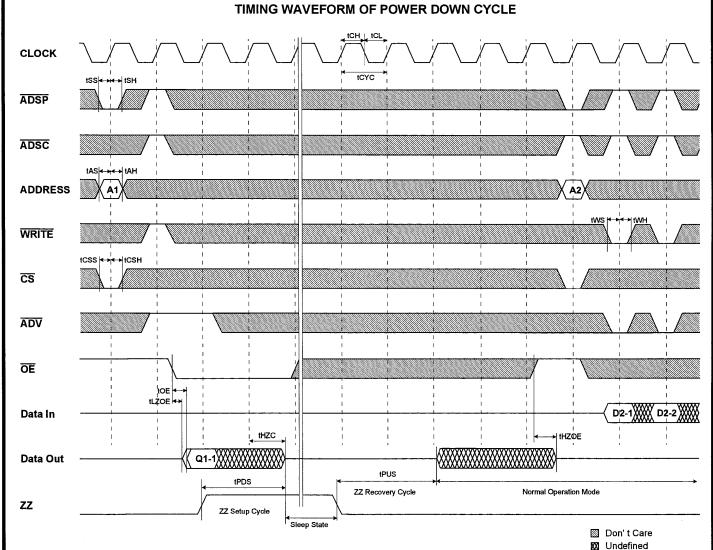
TIMING WAVEFORM OF COMBINATION READ/WRTE CYCLE



Don't Care

Undefined

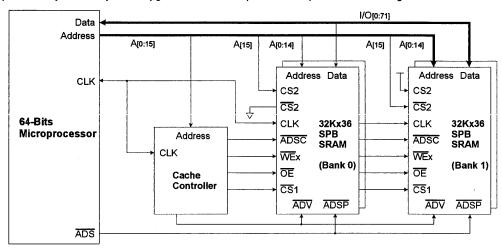




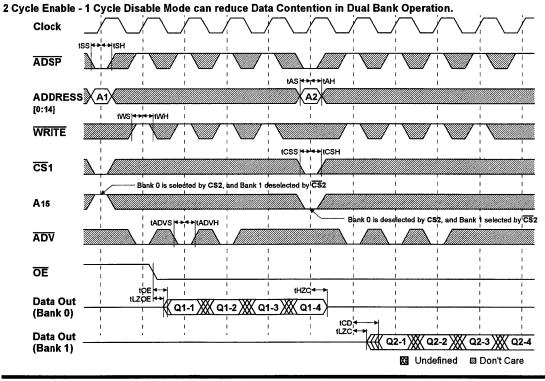
APPLICATION INFORMATION

DEPTH EXPANSION

The Samsung 32Kx36 Synchronous Pipelined Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 32K depth to 64K depth without extra logic.



INTERLEAVE READ TIMING (Refer to non-interleave write timing for interleave write timing)





32Kx36-Bit Synchronous Pipelined Burst SRAM FEATURES GENE

- · Synchronous Operation.
- 2 Stage Pipelined operation with 4 Burst.
- On-Chip Address Counter.
- · Self-Timed Write Cycle.
- · On-Chip Address and Control Registers.
- Add= 3.3V-5%/+10% Power Supply
- . 5V Tolerant Inputs except I/O Pins
- Byte Writable Function.
- · Global Write Enable Controls a full bus-width write.
- · Power Down State via ZZ Signal.
- LBO Pin allows a choice of either a interleaved burst or a linear burst.
- Three Chip Enables for simple depth expansion with No Data Contention; 2 cycle Enable, 1 cycle Disable.
- · Asynchronous Output Enable Control.
- ADSP, ADSC, ADV Burst Control Pins.
- . TTL-Level Three-State Output.
- 100-Pin TQFP Package.

FAST ACCESS TIMES

Parameter	Symbol	-7	-8	-10	Unit
Cycle Time	tCYC	7.5	8.6	10	ns
Clock Access Time	tCD	4.5	5.0	5.0	ns
Output Enable Access Time	tOE	4.5	5.0	5.0	ns

GENERAL DESCRIPTION

The KM736V599A/L is a 1,179,648-bit Synchronous Static Random Access Memory designed for high performance second level cache of P6 and Power PC based System.

It is organized as 32K words of 36bits and integrates address and control registers, a 2-bit burst address counter and added some new functions for high performance cache RAM applications; $\overline{\text{GW}}$, $\overline{\text{BW}}$, $\overline{\text{LBO}}$, ZZ.

Write cycles are internally self-timed and synchronous.

Full bus-width write is done by \overline{GW} , and each byte write is performed by the combination of $\overline{WE}x$ and \overline{BW} when \overline{GW} is high. And with $\overline{CS1}$ high, \overline{ADSP} is blocked to control signals.

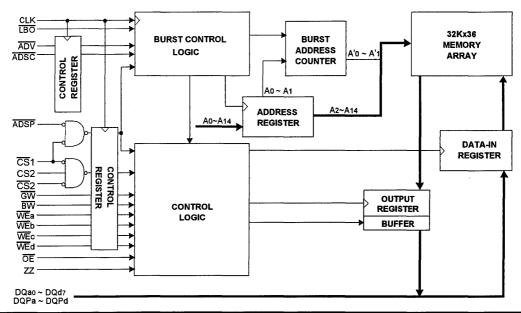
Burst cycle can be initiated with either the address status processor(ADSP) or address status cache controller(ADSC) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance(ADV) input.

LBO pin is DC operated and determines burst sequence(linear or interleaved).

ZZ pin controls Power Down State and reduces Stand-by current regardless of CLK.

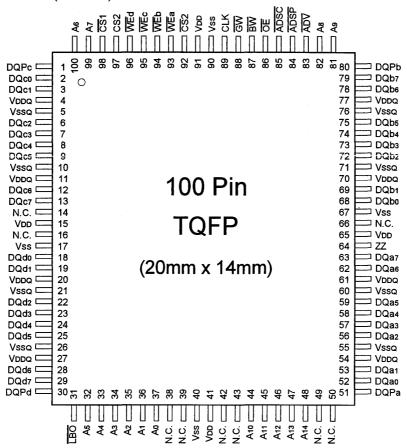
The KM736V599A/L is fabricated using SAMSUNG's high performance CMOS technology and is available in a 100pin TQFP package. Multiple power and ground pins are utilized to minimize ground bounce.

LOGIC BLOCK DIAGRAM





PIN CONFIGURATION(TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A14	Address Inputs	32,33,34,35,36,37,	VDD	Power Supply(+3.3V)	15,41,65,91
		44,45,46,47,48,	Vss	Ground	17,40,67,90
		81,82,99,100	N.C.	No Connect	14,16,38,39,42,43,49,50,
ĀDV	Burst Address Advance	83			66
ADSP	Address Status Processor	84	DQao ~ a7	Data Inputs/Outputs	52,53,56,57,58,59,62,63
ADSC	Address Status Controller	85	DQbo ~ b7		68,69,72,73,74,75,78,79
CLK	Clock	89	DQc0 ~ c7		2,3,6,7,8,9,12,13
CS1	Chip Select	98	DQdo ~ d7	ŀ	18,19,22,23,24,25,28,29
CS2	Chip Select	97	DQPa~Pd	1	51,80,1,30
CS ₂	Chip Select	92			
WEx	Byte Write Inputs	93,94,95,96	VDDQ	Output Power Supply	4,11,20,27,54,61,70,77
ŌĒ	Output Enable	86			
Ġ₩	Global Write Enable	88	VssQ	Output Ground	5,10,21,26,55,60,71,76
BW	Byte Write Enable	87			
ZZ	Power Down Input	64	l		
LBO	Burst Mode Control	31	1	1	



FUNCTION DESCRIPTION

The KM736V599A/L is a synchronous SRAM designed to support the burst address accessing sequence of the P6 and Power PC based microprocessor. All inputs (with the exception of \overline{OE} and ZZ) are sampled on rising clock edges. The start and duration of the burst access is controlled by $\overline{CS1}$, \overline{ADSC} , \overline{ADSP} and \overline{ADV} . The accesses are enabled with the chip select signals and output enabled signals. Wait states are inserted into the access with \overline{ADV} .

When ZZ is pulled high, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM normally operates after 2 cycles of wake up time. ZZ pin is pulled down internally.

Read cycles are initiated with $\overline{\text{ADSP}}$ (regardless of $\overline{\text{WEx}}$ and $\overline{\text{ADSC}}$) using the new external address clocked into the on-chip address register whenever $\overline{\text{ADSP}}$ is sampled low, the chip selects are sampled active, and the output buffer is enabled with $\overline{\text{OE}}$. In read operation the data of cell array accessed by the current address, registered in the Data-out registers by the positive edge of CLK, are carried to the Data-out buffer by the next positive edge of CLK. The data, registered in the Data-out buffer, are projected to the output pins. $\overline{\text{ADV}}$ is ignored on the clock edge that samples $\overline{\text{ADSP}}$ asserted, but is sampled on the subsequent clock edges. The address increases internally for the next access of the burst when $\overline{\text{WEx}}$ are sampled High and $\overline{\text{ADV}}$ is sampled low. And $\overline{\text{ADSP}}$ is blocked to control signals by disabling $\overline{\text{CS}}1$.

All byte write is done by \overline{GW} (regaedless of \overline{BW} and $\overline{WE}x$.), and each byte write is performed by the combination of \overline{BW} and $\overline{WE}x$ when \overline{GW} is high.

Write cycles are performed by disabling the output buffers with \overline{OE} and asserting \overline{WEx} . \overline{WEx} are ignored on the clock edge that samples \overline{ADSP} low, but are sampled on the subsequent clock edges. The output buffers are disabled when \overline{WEx} are sampled Low(regaedless of \overline{OE}). Data is clocked into the data input register when \overline{WEx} sampled Low. The address increases internally to the next address of burst, if both \overline{WEx} and \overline{ADV} are sampled Low. Individual byte write cycles are performed by any one or more byte write enable signals(\overline{WEa}), \overline{WE} 0 or \overline{WEd} 0 sampled low. The \overline{WE} 1 controls DQ00 ~ DQ07 and DQP0, \overline{WE} 2 controls DQ00 ~ DQ07 and DQP0, \overline{WE} 3 controls DQ00 ~ DQ07 and DQP0, and \overline{WE} 4 controls DQ00 ~ DQ07 and DQP0. The differences between cycles initiated with \overline{ADSP} 3 as are follows;

ADSP must be sampled high when ADSC is sampled low to initiate a cycle with ADSC. WEx are sampled on the same clock edge that sampled ADSC low(and ADSP high).

Addresses are generated for the burst access as shown below, The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the LBO pin. When this pin is Low, linear burst sequence is selected. When this pin is High, Interleaved burst sequence is selected.

BURST SEQUENCE TABLE

(Interleaved Burst)

LBO PIN HIGH	Cas	se 1	Case 2		Cas	se 3	Case 4		
EBO FIN	A1	A0	A1	A0	A1	A0	A1	A0	
First Address	0	0	0	1	1	0	1	1	
	0	1	0	0	1	1	1	0.	
↓	1	0	1	1	0	0	0	1	
Fourth Address	1	1	1	0	0	1	0	0	

(Linear Burst)

LBO PIN LOW	Ca	Case 1		Case 2		Case 3		Case 4	
LDO FIN LOW	A1	A0	A1	A0	A1	A0	A1	A0	
First Address	0	0	0	1	1	0	1	1	
	0	1	1	0	1	1	0	0	
	1	0	1	1	0	0	0	1 1	
Fourth Address	1	1	0	0	0	1	1	0	

NOTE: 1. LBO pin must be tied to High or Low, and Floating State must not be allowed.



TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

CS1	CS2	CS2	ADSP	ADSC	ADV	WRITE	CLK	Address Accessed	Operation
Н	Х	Х	Х	٦	X	Х	1	N/A	Not Selected
L	L	Х	L	Х	Х	Х	1	N/A	Not Selected
L	Х	Н	L	Х	Х	Х	1	N/A	Not Selected
L	L	Х	Х	L	Х	Х	1	N/A	Not Selected
L	Х	Н	Х	L	X	X	1	N/A	Not Selected
L	Н	L	L	Х	Х	X	1	External Address	Begin Burst Read Cycle
L	Н	L	Н	L	Х	L	1	External Address	Begin Burst Write Cycle
L	Н	L	Н	L	Х	Н	1	External Address	Begin Burst Read Cycle
X	Х	Х	Н	н	L	Н	1	Next Address	Continue Burst Read Cycle
Н	Х	X	Х	Н	L	Н	î	Next Address	Continue Burst Read Cycle
X	Х	Х	Н	Н	L	L	1	Next Address	Continue Burst Write Cycle
Н	Х	Х	Х	Н	L	L	1	Next Address	Continue Burst Write Cycle
Х	Х	Х	Н	Н	Н	Н	1	Current Address	Suspend Burst Read Cycle
Н	Х	Х	Х	Н.	Н	Н	1	Current Address	Suspend Burst Read Cycle
X	Х	Х	Н	Н	Ŧ	L	1	Current Address	Suspend Burst Write Cycle
Н	Х	Х	X	Н	Ι	L	1	Current Address	Suspend Burst Write Cycle

NOTE: 1. X means "Don't Care".

2. The rising edge of clock is symbolized by 1.

3. WRITE = L means Write operation in WRITE TRUTH TABLE.
WRITE = H means Read operation in WRITE TRUTH TABLE.

4. Operation finally depends on status of asynchronous input pins(ZZ and OE).

WRITE TRUTH TABLE

GW	BW	WEa	WEb	WEc	WEd	Operation
Н	Н	Х	Х	Х	X	READ
Н	L	Н	Н	Н	Н	READ
Н	L	L	Н	Н	Н	WRITE BYTE a
Н	L	Н	L	Н	н	WRITE BYTE b
Н	L	Н	Н	L	L	WRITE BYTE c and d
Н	L	L	L	L	L	WRITE ALL BYTEs
L	Х	X	Х	Х	X	WRITE ALL BYTEs

NOTE: 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(1).

ASYNCHRONOUS TRUTH TABLE

(See Notes 1 and 2):

Operation	ZZ	ŌĒ	I/O Status
Sleep Mode	Н	X	High-Z
David	L	L	DQ
Read	L	Н	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

NOTE

- 1. X means "Don't Care".
- 2. ZZ pin is pulled down internally
- For write cycles that following read cycles, the output buffers must be disabled with OE, otherwise data bus contention will occur.
- 4. Sleep Mode means power down state of which stand-by current does not depend on cycle time.
- Deselected means power down state of which stand-by current depends on cycle time.



PASS-THROUGH TRUTH TABLE

Previous Cycle		Presen	t Cycle			Navi Coola
Operation	WRITE	Operation CS		1 WRITE C		Next Cycle
Write Cycle, All bytes Address=An-1, Data=Dn-1		Initiate Read Cycle Address=An Data=Qn-1 for all bytes		н	L	Read Cycle Data=Qn
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=Qn-1 for all bytes	Н	Н	L	No carryover from previous cycle
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=High-Z	н	н	Н	No carryover from previous cycle
Write Cycle, One byte Address=An-1, Data=Dn-1	One L	Initiate Read Cycle Address=An Data=Qn-1 for one byte	L	н	L	Read Cycle Data=Qn
Write Cycle, One byte Address=An-1, Data=Dn-1	One L	No new cycle Data=Qn-1 for one byte	Н	н	L	No carryover from previous cycle

NOTE: 1. This operation makes written data immediately available at output during a read cycle preceded by a write cycle.

ABSOLUTE MAXIMUM RATING*

Parameter	Symbol	Rating	Unit
Voltage on VDD Supply Relative to Vss	VDD	-0.3 to 4.6	V
Voltage on VDDQ Supply Relative to Vss	VDDQ	VDD	V
Voltage on Input Pin Relative to Vss	Vin	-0.3 to 6.0	V
Voltage on I/O Pin Relative to Vss	Vio	-0.3 to VDDQ + 0.5	V
Power Dissipation	PD	1.2	W
Storage Temperature	Тѕтҫ	-65 to 150	°C
Operating Temperature	Topr	0 to 70	°C
Storage Temperature Range Under Bias	TBIAS	-10 to 85	°C

*NOTE: Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS (0°C ≤ TA ≤ 70°C)

Parameter	Symbol	Min	Тур.	Max	Unit
Supply Voltage	VDD	3.13	3.3	3.6	V
	VDDQ	3.13	3.3	3.6	V
Ground	Vss	0	0	0	V

CAPACITANCE* (TA = 25°C, f = 1MHz)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	CIN	VIN=0V	-	5	pF
Output Capacitance	Cout	Vout=0V	-	7	pF

^{*}NOTE: Sampled not 100% tested.



^{2.} WEx means WEa ~ WEd.

DC ELECTRICAL CHARACTERISTICS

 $(VDD=3.3V-5\%/+10\%, TA = 0^{\circ} to 70^{\circ})$

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current(except ZZ)	lıL .	VDD = Vss to VDD, VIN = Vss to VDD		-2	+2	μA
Output Leakage Current	loL	Output Disabled, Vout = Vss to VDDQ		-2	+2	μA
Operating Current		Device Selected, IouT = 0mA, ZZ≤VIL,	-7	-	270	mA
	Icc	All Inputs = VIL or VIH	-8	-	260	
		Cycle Time ≥ tCYC min	-10	-	240	
Standby Current		Device developed lour - 0mA 77<\/u	-7	-	60	
·	ISB	Device deselected, IouT = 0mA, ZZ≤VIL, f = Max, All Inputs≤0.2V or ≥ VDD-0.2V	-8	-	60	mA
		1 - Wax, All Imputs = 0.27 01 = 700-0.27	-10	-	60	
		Device deselected, Iout = 0mA,		-	10	mA
	ISB1	IsB1		-	1	mA
	10	Device deselected, Iout = 0mA,		-	10	mA
	IsB2	ZZ≥VDD-0.2V, f = Max, All Inputs≤VIL or ≥ViH	L-Ver.	-	500	μA
Output Low Voltage	Vol	IoL = 8mA		-	0.4	٧
Output High Voltage	Voн	Iон = -4mA		2.4	-	V
Input Low Voltage	VIL			-0.5*	0.8	٧
Input High Voltage	VIH			2.0	5.5**	V

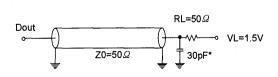
^{*} VIL(min) = -3.0 (Pulse Width $\leq 20ns$)

TEST CONDITIONS

(TA = 0 $^{\circ}$ C to 70 $^{\circ}$ C, VDD=3.3V-5%/+10% unless otherwise specified)

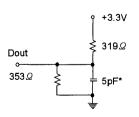
Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time(Measured at 0.3V and 2.7V)	2ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1

Output Load(A)



^{*} Capacitive Load consists of all components of the test environment.

Output Load(B) (for tLZC, tLZOE, tHZOE& tHZC)



^{*} Including Scope and Jig Capacitance





^{**} In Case of I/O Pins, The Max. VIH=VDDQ + 0.5V

AC TIMING CHARACTERISTICS

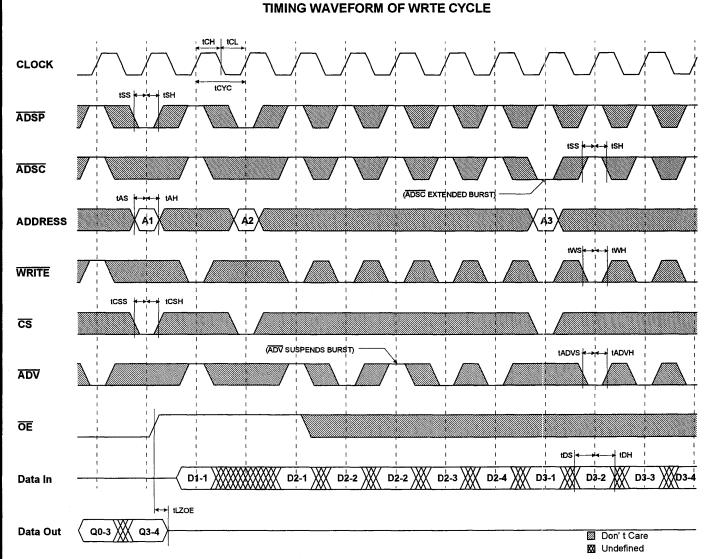
 $(VDD=3.3V-5\%/10\%, TA = 0^{\circ} to 70^{\circ})$

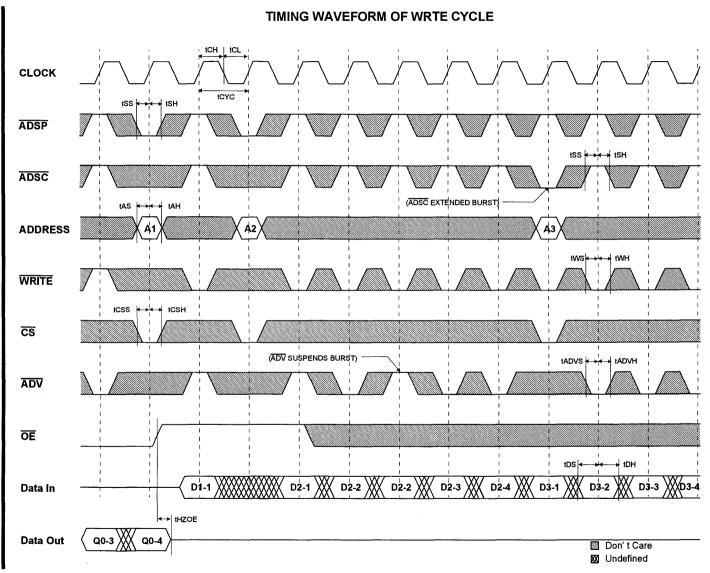
Parameter	Sumbel	KM736	V599A-7	KM736V599A-8		KM736V599A-10		Unit
Parameter	Symbol	Min	Max	Min	Max	Min	Max	- Unit
Cycle Time	tCYC	7.5	-	8.6	-	10	-	ns
Clock Access Time	tCD	-	4.5	-	5.0	-	5.0	ns
Output Enable to Data Valid	tOE	-	4.5	-	5.0	-	5.0	ns
Clock High to Output Low-Z	tLZC	0	-	0	-	0		ns
Output Hold from Clock High	tOH	1.5	-	1.5	-	1.5	-	ns
Output Enable Low to Output Low-Z	tLZOE	0	-	0	-	-0	-	ns
Output Enable High to Output High-Z	tHZOE	-	4.0	-	4.0	-	4.0	ns
Clock High to Output High-Z	tHZC	1.5	5.0	1.5	5.0	1.5	5.0	ns
Clock High Pulse Width	tCH	2.5	-	2.5	-	3.0	-	ns
Clock Low Pulse Width	tCL	2.5	-	2.5	-	3.0	-	ns
Address Setup to Clock High	tAS	2.0	-	2.0	-	2.0	-	ns
Address Status Setup to Clock High	tSS	2.0	-	2.0	-	2.0	-	ns
Data Setup to Clock High	tDS	2.0	-	2.0	-	2.0	-	ns
Write Setup to Clock High (GW, BW, WEx)	tWS	2.0	-	2.0	-	2.0	-	ns
Address Advance Setup to Clock High	tADVS	2.0	-	2.0	-	2.0	-	ns
Chip Select Setup to Clock High	tCSS	2.0	-	2.0	-	2.0	-	ns
Address Hold from Clock High	tAH	0.5	-	0.5	-	0.5	-	ns
Address Status Hold from Clock High	tSH	0.5	-	0.5	-	0.5	-	ns
Data Hold from Clock High	tDH	0.5		0.5	-	0.5	-	ns
Write Hold from Clock High (GW, BW, WEx)	tWH	0.5	-	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	tADVH	0.5	-	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	tCSH	0.5	-	0.5	-	0.5	-	ns
ZZ High to Power Down	tPDS	2	-	2	-	2	-	cycle
ZZ Low to Power Up	tPUS	2	-	2	-	2	-	cycle

NOTE: 1. All address inputs must meet the specified setup and hold times for all rising clock edges whenever ADSC and/or ADSP is sampled low and CS is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.

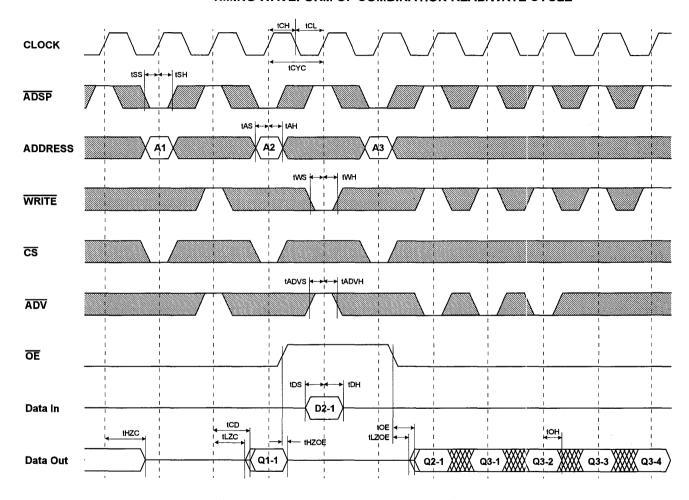
2. Both chip selects must be active whenever ADSC or ADSP is sampled low in order for the this device to remain enabled.

3. ADSC or ADSP must not be asserted for at least 2 Clock after leaving ZZ state.



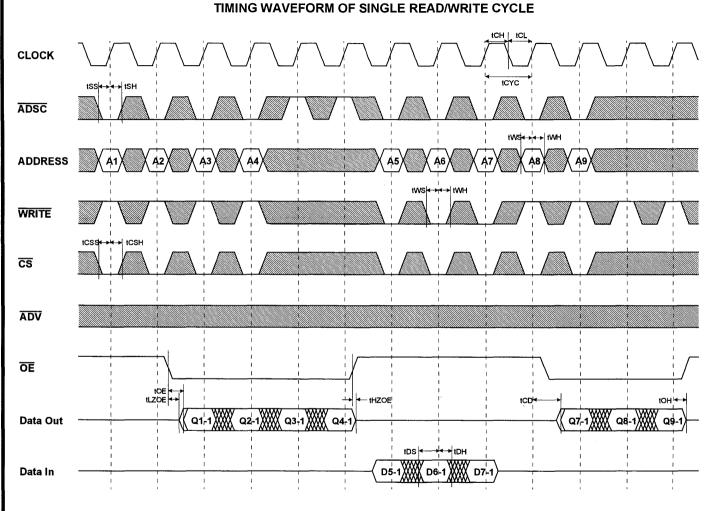


TIMING WAVEFORM OF COMBINATION READ/WRTE CYCLE



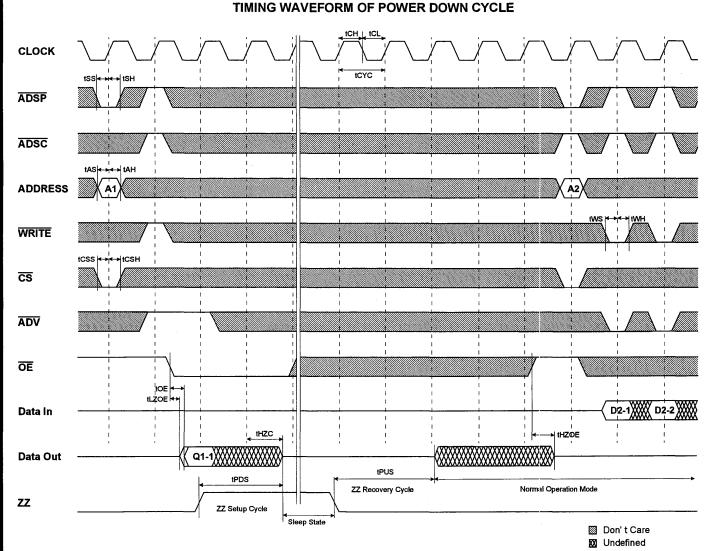
Don't Care

Undefined



Don't Care

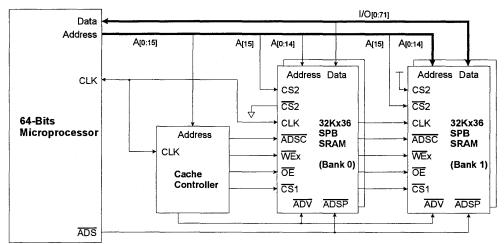
⊠ Undefined



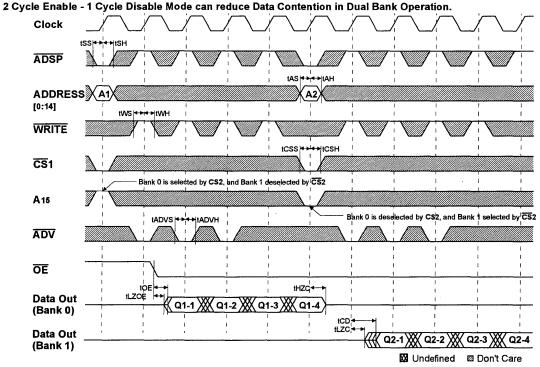
APPLICATION INFORMATION

DEPTH EXPANSION

The Samsung 32Kx36 Synchronous Pipelined Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 32K depth to 64K depth without extra logic.



INTERLEAVE READ TIMING (Refer to non-interleave write timing for interleave write timing)



64Kx18-Bit Synchronous Burst SRAM FEATURES

- . Synchronous Operation.
- · On-Chip Address Counter.
- . Write Self-Timed Cycle.
- . On-Chip Address and Control Registers.
- Single 3.3± 5% Power Supply.
- 5V Tolerant Inputs except I/O Pins.
- . Byte Writable Function.
- . Global Write Enable Controls a full bus-width write.
- . Power Down State via ZZ Signal.
- Asynchronous Output Enable Control.
- . ADSP, ADSC, ADV Burst Control Pins.
- LBO Pin allows a choice of either a interleaved burst or a linear burst.
- Three Chip Enables for simple depth expansion with No Data Contention
- . TTL-Level Three-State Output.
- 100-Pin TQFP Package

FAST ACCESS TIMES

Parameter	Symbol	-8	-9	-10	Unit
Cycle Time	tCYC	12	12	15	ns
Clock Access Time	tCD	8.5	9	10	ns
Output Enable Access Time	tOE	4	4	5	ns

GENERAL DESCRIPTION

The KM718V687 is a 1,179,648 bits Synchronous Static Random Access Memory designed to support zero wait state performance for advanced Pentium and Power PC based system. And with CS1 high, ADSP is blocked to control signal.

It is organized as 64K words of 18 bits. And it integrates address and control registers, a 2-bit burst address counter and high output drive circuitry onto a single integrated circuit for reduced components counts implementation of high performance cache RAM applications.

Write cycles are internally self-timed and synchronous.

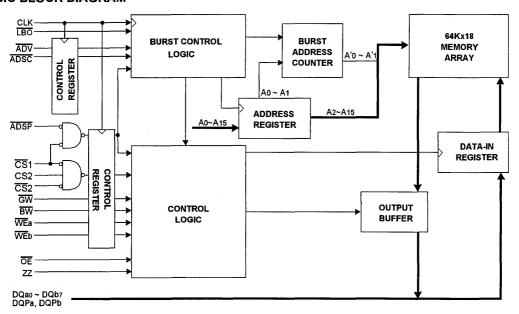
The self-timed write feature eliminates complex off chip write pulse shaping logic, simplifying the cache design and further reducing the component count.

Burst cycle can be initiated with either the address status processor(ADSP) or address status cache controller(ADSC) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance(ADV) input.

ZZ pin controls Power Down State and reduces Stand-by current regardless of CLK.

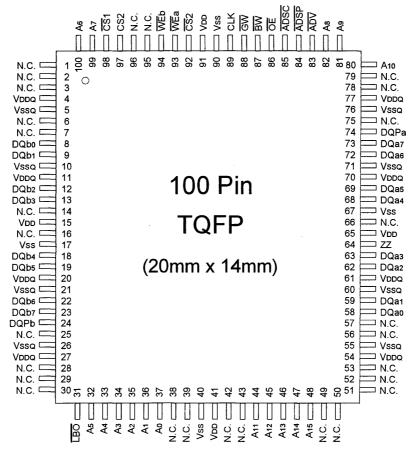
The KM718V687 is implemented with SAMSUNG's high performance CMOS technology and is available in a 100pin TQFP package. Multiple power and ground pins are utilized to minimize ground bounce.

LOGIC BLOCK DIAGRAM





PIN CONFIGURATION (TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A15	Address Inputs	32,33,34,35,36,37,	VDD	Power Supply(+3.3V)	15,41,65,91
		44,45,46,47,48,80,	Vss	Ground	17,40,67,90
	1	81,82,99,100	N.C.	No Connect	1,2,3,6,7,14,16,25,28,29
ADV	Burst Address Advance	83			,30,38,39,42,43,49,50,
ADSP	Address Status Processor	84			51,52,53,56,57,66,75,
ADSC	Address Status Controller	85	1		78,79,95,96
CLK	Clock	89	DQa0 ~ a7	Data Inputs/Outputs	58,59,62,63,68,69,72,73
CS1	Chip Select	98	DQb0 ~ b7		8,9,12,13,18,19,22,23
CS2	Chip Select	97	DQPa, Pb		74,24
CS2	Chip Select	92	VDDQ	Output Power Supply	4,11,20,27,54,61,70,77
WEx	Byte Write Inputs	93,94	ı	(+3.3V)	
ŌĒ	Output Enable	86	Vssq	Output Ground	5,10,21,26,55,60,71,76
Ġ₩	Global Write Enable	88			
₿₩	Byte Write Enable	87	1		
ZZ	Power Down Input	64			
LBO	Burst Mode Control	31			

FUNCTION DESCRIPTION

The KM718V687 is a synchronous SRAM designed to support the burst address accessing sequence of the Pentium and Power PC based microprocessor. All inputs(with the exception of OE, LBO and ZZ) are sampled on rising clock edges.

The start and duration of the burst access is controlled by ADSP, ADSC, ADV and Chip Select pins.

When ZZ is pulled HIGH, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When ZZ returns to LOW, the SRAM normally operates after 2 cycles of wake up time. ZZ pin is pulled down internally.

Read cycles are initiated with \overline{ADSP} (or \overline{ADSC}) using the new external address clocked into the on-chip address register when both \overline{GW} and \overline{BW} are high or when \overline{BW} is low and both \overline{WE} a and \overline{WE} b are high, When \overline{ADSP} is sampled low, the chip selects are sampled active, and the output buffer is enabled with \overline{OE} , the data of cell array accessed by the current address are projected to the output pins.

Write cycles are also initiated with ADSP(or ADSC) and are differentiated into two kinds of operations; All byte write operation and individual byte write operation.

All byte write occurs by enabling \overline{GW} (in dependent of \overline{BW} and \overline{WEx} .), and individual byte write is performed only when \overline{GW} is High and \overline{BW} is Low. In KM718V687, A 64Kx18 organization, \overline{WE} a controls DQa0 ~ DQa7 and DQPa, \overline{WE} b controls DQb0 ~ DQb7 and DQPb.

CS1 is used to enable the device and conditions internal use of ADSP and is sampled only when a new external address is loaded.

 $\overline{\text{ADV}}$ is ignored at the clock edge when $\overline{\text{ADSP}}$ is asserted, but can be sampled on the subsequent clock edges. The address increases internally for the next access of the burst when $\overline{\text{ADV}}$ is sampled low.

Addresses are generated for the burst access as shown below, The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the LBO pin. When this pin is Low, linear burst sequence is selected. And when this pin is High, Interleaved burst sequence is selected.

BURST SEQUENCE TABLE

(Interleaved Burst)

TBO PIN HIGH	Case 1		Case 2		Case 3		Case 4	
LBO FIN HIGH	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
	0	1	0	0	1	1	1	0
↓	1	0	1	1	0	0	0	1
Fourth Address	1	1	1	0	0	1	0	0

(Linear Burst)

TRO DIN LOW	Case 1		Case 2		Case 3		Case 4	
LBO FIN LOW	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
	0	1	1	0	1	1	0	0
	1	0	1	1	0	0	0	1
Fourth Address	1	1	0	0	0	1	1	0

NOTE: 1. LBO pin must be tied to High or Low, and Floating State must not be allowed.

TRUTH TABLES

ASYNCHRONOUS TRUTH TABLE

(See Notes 1 and 2):

Operation	ZZ	ŌĒ	I/O Status
Sleep Mode	Н	Χ	High-Z
Read	L	L	DQ
Reau	L	H	High-Z
Write	L	Х	Din, High-Z
Deselected	L	Х	High-Z

NOTE

- 1. X means "Don't Care".
- 2. ZZ pin is pulled down internally
- 3. For write cycles that following read cycles, the output buffers must be disabled with \overline{OE} , otherwise data bus contention will occur.
- Sleep Mode means power down state of which stand-by current does not depend on cycle time.
- Deselected means power down state of which stand-by current depends on cycle time.



SYNCHRONOUS TRUTH TABLE

CS1	CS2	CS2	ADSP	ADSC	ĀDV	WRITE	CLK	Address Accessed	Operation
Н	Х	Х	Х	L	X	Х	1	N/A	Not Selected
L	L	Х	L	Х	Х	Х	1	N/A	Not Selected
L	X	Н	L	Х	Х	Х	1	N/A	Not Selected
L	L	Х	Х	L	Х	Х	1	N/A	Not Selected
L	X	Н	Х	L	X	Х	1	N/A	Not Selected
L	Н	L	L	Х	Х	Х	1	External Address	Begin Burst Read Cycle
L	Н	L	Н	L	Х	L	1	External Address	Begin Burst Write Cycle
L	Н	L	Н	L	Х	Н	1	External Address	Begin Burst Read Cycle
X	Х	Х	Н	Н	L	Н	1	Next Address	Continue Burst Read Cycle
Н	Х	Х	Х	Н	L	Н	1	Next Address	Continue Burst Read Cycle
X	Х	Х	Н	Н	L	L	1	Next Address	Continue Burst Write Cycle
Н	Х	Х	X	Н	L	L	1	Next Address	Continue Burst Write Cycle
Х	Х	Х	Н	Н	Н	Н	1	Current Address	Suspend Burst Read Cycle
Н	X	Х	X	Н	Н	Н	1	Current Address	Suspend Burst Read Cycle
Х	Х	Х	Н	Н	Н	L	1	Current Address	Suspend Burst Write Cycle
Н	Х	Х	×	Н	Н	L	1	Current Address	Suspend Burst Write Cycle

NOTE: 1. X means "Don't Care".

- 2. The rising edge of clock is symbolized by 1.
- WRITE = L means Write operation in WRITE TRUTH TABLE.
 WRITE = H means Read operation in WRITE TRUTH TABLE.
- 4. Operation finally depends on status of asynchronous input pins(ZZ and OE).

WRITE TRUTH TABLE

GW	BW	WEa	WEb	Operation
Н	Н	Х	X	READ
Н	L	Н	Н	READ
Н	L	L	Н	WRITE BYTE a
Н	L	Н	L	WRITE BYTE b
Н	L	L	L	WRITE ALL BYTEs
L	Х	Х	Х	WRITE ALL BYTEs

NOTE: 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(1).

ABSOLUTE MAXIMUM RATING*

Parameter	Symbol	Rating	Unit
Voltage on VDD Supply Relative to Vss	VDD	-0.3 to 4.6	V
Voltage on VDDQ Supply Relative to Vss	VDDQ	VDD	V
Voltage on Input Pin Relative to Vss	Vin	-0.3 to 6.0	V
Voltage on I/O Pin Relative to Vss	Vio	-0.3 to VDDQ + 0.5	V
Power Dissipation	Po	1.2	W
Storage Temperature	Тѕтс	-65 to 150	°C
Operating Temperature	Topr	0 to 70	°C
Storage Temperature Range Under Bias	TBIAS	-10 to 85	°C

*NOTE: Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.



OPERATING CONDITIONS(0° \leq TA \leq 70°C)

Parameter	Symbol	Min	Тур.	Max	Unit
Supply Voltage	VDD	3.13	3.3	3.47	V
Supply Voltage	VDDQ	3.13	3.3	3.47	V
Ground	Vss	0	0	0	V

CAPACITANCE* (TA = 25°C, f = 1MHz)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	CIN	VIN=0V	-	5	pF
Output Capacitance	Соит	Vout=0V	-	8	pF

^{*}NOTE: Sampled not 100% tested.

TEST CONDITIONS(TA = 0° to 70° , VDD = $3.3V \pm 5\%$, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time(Measured at 0.3V and 2.7V)	2ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1

DC ELECTRICAL CHARACTERISTICS(TA = 0°C to 70°C, VDD = 3.3V±5%)

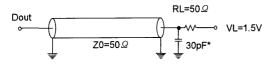
Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current(except ZZ)	liL	VDD = Max , VIN = Vss to VDD	-2	+2	μA	
Output Leakage Current	loL	Output Disabled, Vout = Vss to Vo	Output Disabled, Vout = Vss to VDDQ			
Operating Current	Icc	Device Selected, lout = 0mA,	8ns	-	330	
		ZZ≤VIL, All Inputs = VIL or VIH	9ns	-	330	mA
		Cycle Time ≥ tCYC min	10ns	-	300	1
Standby Current	ISB	Device deselected, IOUT = 0mA,	8ns	-	80	
		ZZ ≤ VIL,f = Max, All Inputs ≤ 0.2V or ≥ VDD-0.2V	9ns	•	80	mA
			10ns	-	60	1
	ISB1	ISB1 Device deselected, IouT = 0mA, $ZZ \le 0.2V$, f = 0, All Inputs = fixed (VDD-0.2V or 0.2V)			10	mA
	ISB2	Device deselected, IouT = 0mA, ZZ≥VoD-0.2V, f = Max, All Inputs≤ViL or ≥ViH		-	10	mA
Output Low Voltage	VoL	IOL = 8.0mA		-	0.4	V
Output High Voltage	Voн	Iон = -4.0mA		2.4	-	V
Input Low Voltage	VIL			-0.5*	0.8	V
Input High Voltage	ViH		2.2	5.5**	V	

^{*} VIL(min) = -3.0(Pulse Width≤20ns)



^{**} In Case of I/O Pins, the Max. VIH = VDDQ + 0.5V

Output Load(A)



Output Load(B) (for tLZC, tLZOE, tHZOE& tHZC)

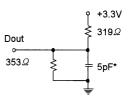


Fig. 1

AC TIMING CHARACTERISTICS (TA = 0 °C to 70 °C, VDD = $3.3V\pm5\%$)

Parameter		KM718	3V687-8	KM718V687-9		KM718V687-10		Unit
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Onit
Cycle Time	tCYC	12	-	12	-	15	-	ns
Clock Access Time	tCD	-	8.5	-	9	-	10	ns
Output Enable to Data Valid	tOE	-	4	-	4	-	5	ns
Clock High to Output Low-Z	tLZC	4	-	4	-	6	-	ns
Output Hold from Clock High	tOH	3	-	3	-	3	-	ns
Output Enable Low to Output Low-Z	tLZOE	0	-	0	-	0		ns
Output Enable High to Output High-Z	tHZOE	2	5	2	5	2	5	ns
Clock High to Output High-Z	tHZC	-	5	-	5	-	6	ns
Clock High Pulse Width	tCH	4	-	4	-	5		ns
Clock Low Pulse Width	tCL	4	-	4	-	5	-	ns
Address Setup to Clock High	tAS	2.5	-	2.5	-	2.5	-	ns
Address Status Setup to Clock High	tSS	2.5	-	2.5	-	2.5	-	ns
Data Setup to Clock High	tDS	2.5	-	2.5	-	2.5	-	ns
Write Setup to Clock High	tWS	2.5	-	2.5	-	2.5	-	ns
Address/Advance Setup to Clock High	tADVS	2.5	-	2.5	-	2.5	-	ns
Chip Select Setup to Clock High	tCSS	2.5	-	2.5	-	2.5	-	ns
Address Hold from Clock High	tAH	0.5	-	0.5	-	0.5	-	ns
Address Status Hold from Clock High	tSH	0.5	-	0.5	-	0.5	-	ns
Data Hold from Clock High	tDH	0.5	-	0.5	-	0.5	-	ns
Write Hold from Clock High	tWH	0.5	-	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	tADVH	0.5	-	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	tCSH	0.5	-	0.5	-	0.5	-	ns
ZZ High to Power Down	tPDS	2	-	2	-	2	-	cycle
ZZ Low to Power Up	tPUS	2	-	2	-	2	-	cycle

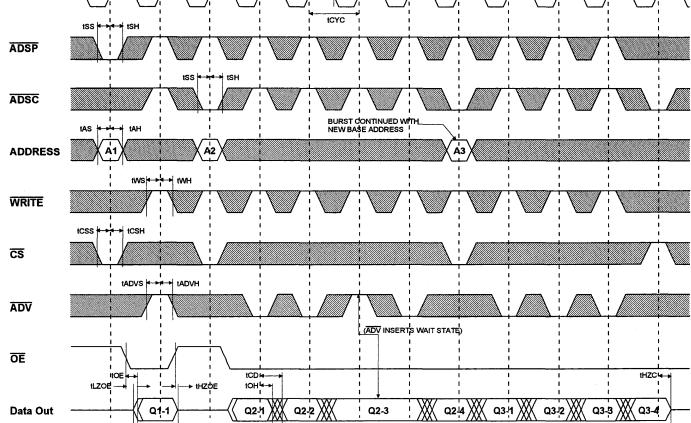
NOTE: 1. All address inputs must meet the specified setup and hold times for all rising clock edges whenever ADSC and/or ADSP is sampled low and CS is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.

- 2. Both chip selects must be active whenever ADSC or ADSP is sampled low in order for the this device to remain enabled.
- 3. ADSC or ADSP must not be asserted for at least 2 Clock after leaving ZZ state.



^{*} Including Scope and Jig Capacitance

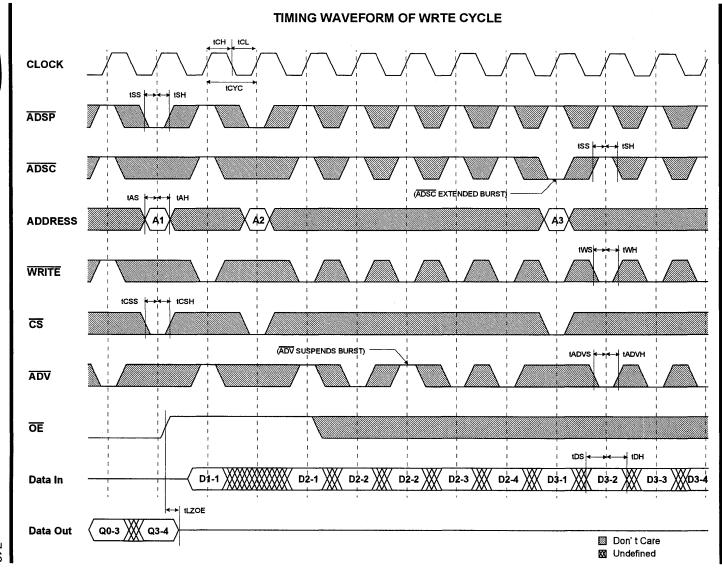
CLOCK tCYC



TIMING WAVEFORM OF READ CYCLE

NOTES: $\overline{WRITE} = L$ means $\overline{GW} = L$, or $\overline{GW} = H$, $\overline{BW} = L$, $\overline{WE}x.= L$ $\overline{CS} = L$ means $\overline{CS}1 = L$, $\overline{CS}2 = H$ and $\overline{CS}2 = L$ $\overline{CS} = H$ means $\overline{CS}1 = H$, or $\overline{CS}1 = L$ and $\overline{CS}2 = H$, or $\overline{CS}1 = L$, and $\overline{CS}2 = L$

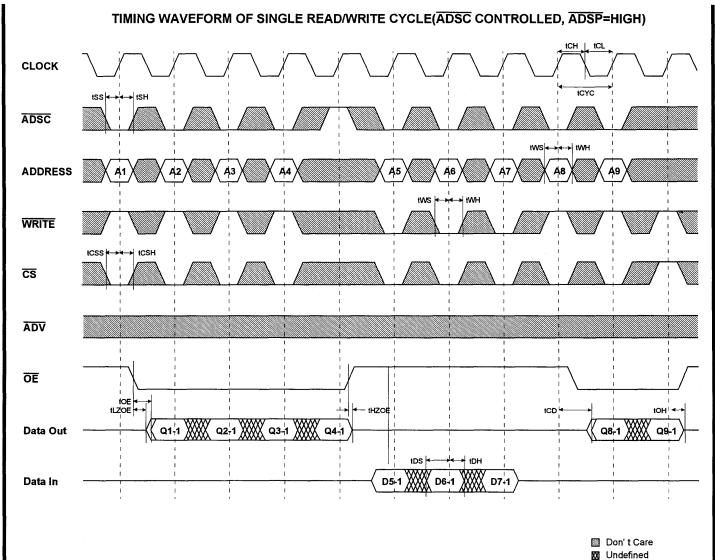
Don't Care

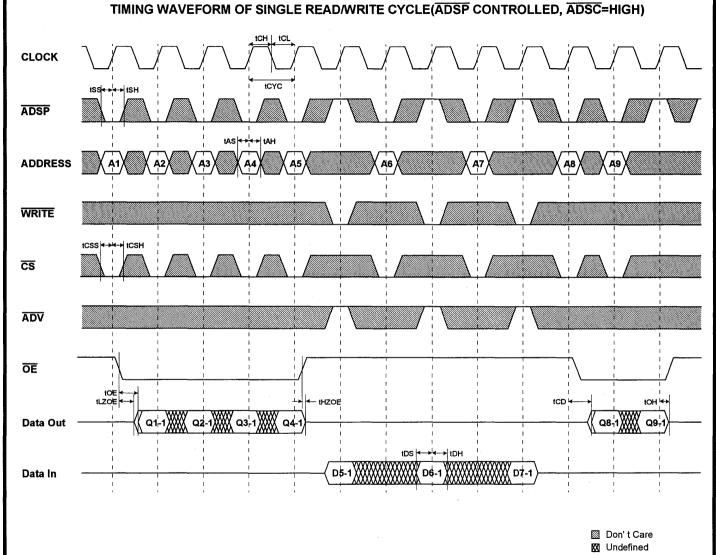


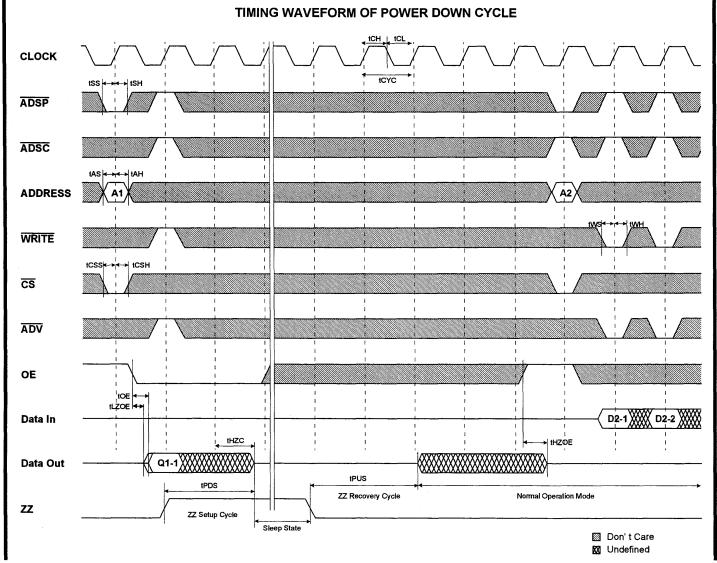
SAMSUNG

ELECTRONICS

TIMING WAVEFORM OF COMBINATION READ/WRTE CYCLE(ADSP CONTROLLED, ADSC=HIGH) CLOCK tCYC ADSP **ADDRESS** Ą1 A3 WRITE cs tADVH tADVS + ++ ADV ŌΕ tDS tDH Data In D2-1 tCD 1OE tHZC tLZIOE + – tHZOĖ Data Out Q1-1







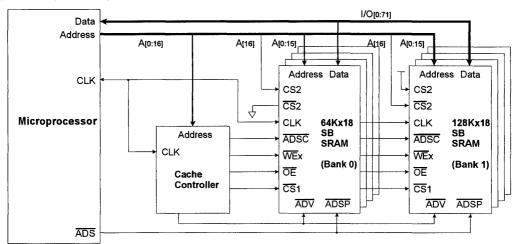
UMSUNG

ELECTRONICS

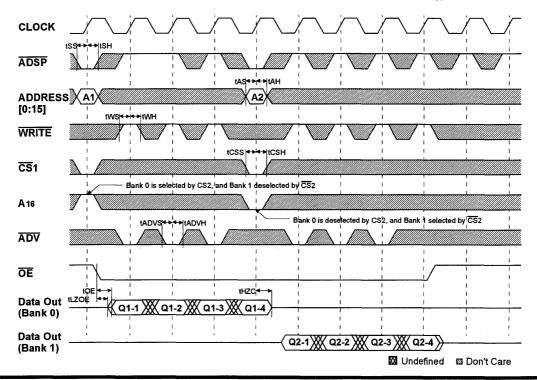
APPLICATION INFORMATION

DEPTH EXPANSION

The Samsung 64Kx18 Synchronous Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 64K depth to 128K depth without extra logic.



INTERLEAVE READ TIMING (Refer to non-interleave write timing for interleave write timing)





32Kx36-Bit Synchronous Burst SRAM FEATURES

- · Synchronous Operation.
- On-Chip Address Counter.
- Write Self-Timed Cycle.
- · On-Chip Address and Control Registers.
- Single 3.3V \pm 5% Power Supply.
- . 5V Tolerant Inputs except I/O Pins.
- · Byte Writable Function.
- · Global Write Enable Controls a full bus-width write.
- · Power Down State via ZZ Signal.
- · Asynchronous Output Enable Control.
- · ADSP, ADSC, ADV Burst Control Pins.
- LBO Pin allows a choice of either a interleaved burst or a linear burst.
- Three Chip Enables for simple depth expansion with No Data Contention.
- . TTL-Level Three-State Output.
- . 100-Pin TQFP Package

FAST ACCESS TIMES

Parameter	Symbol	-8	-9	-10	Unit
Cycle Time	tCYC	12	12	15	ns
Clock Access Time	tCD	8.5	9	10	ns
Output Enable Access Time	tOE	4	4	5	ns

GENERAL DESCRIPTION

The KM736V587 is 1,179,648 bits Synchronous Static Random Access Memory designed to support zero wait state performance for advanced Pentium/Power PC based system. And with $\overline{\text{CS1}}$ high, $\overline{\text{ADSP}}$ is blocked to control signals.

It can be organized as 32K words of 36 bits. And it integrates address and control registers, a 2-bit burst address counter and high output drive circuitry onto a single integrated circuit for reduced components counts implementation of high performance cache RAM applications.

Write cycles are internally self-timed and synchronous.

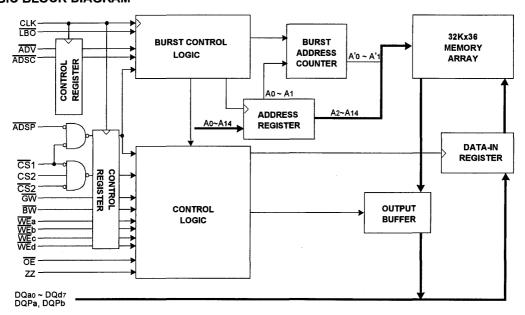
The self-timed write feature eliminates complex off chip write pulse shaping logic, simplifying the cache design and further reducing the component count.

Burst cycle can be initiated with either the address status processor(ADSP) or address status cache controller(ADSC) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance(ADV) input.

ZZ pin controls Power Down State and reduces Stand-by current regardless of CLK.

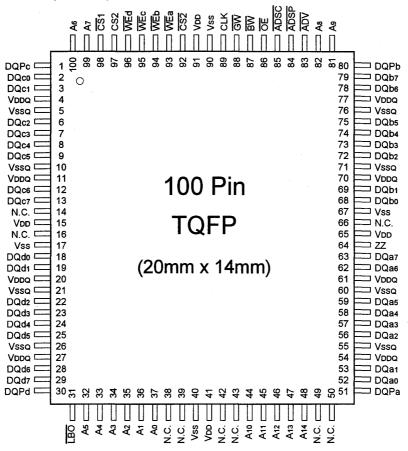
The KM736V587 is implemented with SAMSUNG's high performance CMOS technology and is available in a 100pin TQFP package. Multiple power and ground pins are utilized to minimize ground bounce.

LOGIC BLOCK DIAGRAM





PIN CONFIGURATION (TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A14	Address Inputs	32,33,34,35,36,37,	VDD	Power Supply(+3.3V)	15,41,65,91
		44,45,46,47,48,81,	Vss	Ground	17,40,67,90
		82,99,100	N.C.	No Connect	14,16,38,39,42,43,49,50,
ADV	Burst Address Advance	83			66
ADSP	Address Status Processor	84	DQa0 ~ a7	Data Inputs/Outputs	52,53,56,57,58,59,62,63
ADSC	Address Status Controller	85	DQb0 ~ b7		68,69,72,73,74,75,78,79
CLK	Clock	89	DQc0 ~ c7		2,3,6,7,8,9,12,13
CS1	Chip Select	98	DQdo ~ d7		18,19,22,23,24,25,28,29
CS2	Chip Select	97	DQPa ~ Pd		51,80,1,30
CS 2	Chip Select	92			
WEx	Byte Write Inputs	93,94,95,96	VDDQ	Output Power Supply	4,11,20,27,54,61,70,77
ŌĒ	Output Enable	86	1	(+3.3V)	
Ġ₩	Global Write Enable	88	VssQ	Output Ground	5,10,21,26,55,60,71,76
₿₩	Byte Write Enable	87	1		
ZZ	Power Down Input	64	1		
LBO	Burst Mode Control	31			

FUNCTION DESCRIPTION

The KM736V587 is a synchronous SRAM designed to support the burst address accessing sequence of the Pentium and Power PC based microprocessor. All inputs (with the exception of \overline{OE} , \overline{LBO} and ZZ) are sampled on rising clock edges. The start and duration of the burst access is controlled by \overline{ADSC} , \overline{ADSP} and \overline{ADV} and chip select pins.

When ZZ is pulled high, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM normally operates after 2 cycles of wake up time. ZZ pin is pulled down internally.

Read cycles are initiated with \overline{ADSP} (or \overline{ADSC}) using the new external address clocked into the on-chip address register when both \overline{GW} and \overline{BW} are high or when \overline{BW} is low and \overline{WE} a, \overline{WE} b, \overline{WE} c, and \overline{WE} d are high. When \overline{ADSP} is sampled low, the chip selects are sampled active, and the output buffer is enabled with \overline{OE} . the data of cell array accessed by the current address are projected to the output pins.

Write cycles are also initiated with ADSP(or ADSC) and are differentiated into two kinds of operations; All byte write operation and individual byte write operation.

All byte write occurs by enabling $\overline{\text{GW}}$ (independent of $\overline{\text{BW}}$ and $\overline{\text{WEx.}}$), and individual byte write is performed only when $\overline{\text{GW}}$ is high and $\overline{\text{BW}}$ is low. In KM736V587, a 32Kx36 organization, $\overline{\text{WE}}$ a controls DQa0 ~ DQa7 and DQPa, $\overline{\text{WE}}$ b controls DQb0 ~ DQb7 and DQPb, $\overline{\text{WE}}$ c controls DQc0 ~ DQc7 and DQPc and $\overline{\text{WE}}$ d controls DQd0 ~ DQd7 and DQPd.

CS1 is used to enable the device and conditions internal use of ADSP and is sampled only when a new external address is loaded.

 $\overline{\text{ADV}}$ is ignored at the clock edge when $\overline{\text{ADSP}}$ is asserted, but can be sampled on the subsequent clock edges. The address increases internally for the next access of the burst when $\overline{\text{ADV}}$ is sampled low.

Addresses are generated for the burst access as shown below, The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the LBO pin. When this pin is Low, linear burst sequence is selected. And this pin is High, Interleaved burst sequence is selected.

BURST SEQUENCE TABLE

(Interleaved Burst)

LBO PIN HIGH	Case 1		Case 2		Case 3		Case 4	
LBO FIN HIGH	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
	0	1	0	0	1	1	1	0
1	1	o	1	1	0	0	0	1
Fourth Address	1	1	1	.0	0	1	0	0

(Linear Burst)

LBO PIN LOW	Case 1		Case 2		Case 3		Case 4	
LBO FIN LOW	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
	0	1	1	0	1	1	0	0
1	1	0	1 1	1	0	0	0	1
Fourth Address	1	1	0	0	0	1	1	0

NOTE: 1. LBO pin must be tied to High or Low, and Floating State must not be allowed.

ASYNCHRONOUS TRUTH TABLE

(See Notes 1 and 2):

Operation	ZZ	ŌĒ	I/O Status	
Sleep Mode	Н	Х	High-Z	
Read	L	L	DQ	
Read	L	Н	High-Z	
Write	L	Х	Din, High-Z	
Deselected	L	Х	High-Z	

NOTE

- 1. X means "Don't Care".
- 2. ZZ pin is pulled down internally
- For write cycles that following read cycles, the output buffers must be disabled with OE, otherwise data bus contention will occur.
- Sleep Mode means power down state of which stand-by current does not depend on cycle time.
- Deselected means power down state of which stand-by current depends on cycle time.



SYNCHRONOUS TRUTH TABLE

CS1	CS2	CS2	ADSP	ADSC	ADV	WRITE	CLK	Address Accessed	Operation
Н	Х	Х	Х	L	Х	Х	1	N/A	Not Selected
L	L	Х	L	Х	Χ	Х	1	N/A	Not Selected
L	X	Н	L	Х	Х	Х	Î	N/A	Not Selected
L	L	Х	Х	٦	Х	Х	Î	N/A	Not Selected
L	Х	Н	Х	٦	Х	Х	1	N/A	Not Selected
L	Н	L	L	X	X	X	1	External Address	Begin Burst Read Cycle
L	Н	L	Н	L	X	L	1	External Address	Begin Burst Write Cycle
L	Н	L	Н	L	Х	H	1	External Address	Begin Burst Read Cycle
Х	X	Х	Н	Н	L	H	1	Next Address	Continue Burst Read Cycle
Н	Х	Х	Х	Н	L	Н	1	Next Address	Continue Burst Read Cycle
Х	Х	Х	Н	Н	٦	Г	1	Next Address	Continue Burst Write Cycle
Н	Х	Х	Х	Н	L	L	1	Next Address	Continue Burst Write Cycle
Х	Х	Х	Н	Н	Н	Н	1	Current Address	Suspend Burst Read Cycle
Н	Х	Х	Х	Н	Н	Н	1	Current Address	Suspend Burst Read Cycle
Х	Х	Х	Н	Н	Н	L	1	Current Address	Suspend Burst Write Cycle
Н	Х	Х	Х	Н	I	L	1	Current Address	Suspend Burst Write Cycle

NOTE: 1. X means "Don't Care".

- 2. The rising edge of clock is symbolized by 1.
- 3. WRITE = L means Write operation in WRITE TRUTH TABLE.

WRITE = H means Read operation in WRITE TRUTH TABLE.

4. Operation finally depends on status of asynchronous input pins(ZZ and OE).

WRITE TRUTH TABLE

GW	BW	WEa	WEb	WEc	WEd	Operation
Н	Н	Х	Х	Х	Х	READ
Н	L	Н	Н	Н	Н	READ
Н	L	L	Н	н	Н	WRITE BYTE a
Н	L	Н	L	Н	Н	WRITE BYTE b
н	L	Н	Н	L	L	WRITE BYTE c and d
н	L	L	L	L	L	WRITE ALL BYTEs
L	X	Х	X	X	Х	WRITE ALL BYTEs

NOTE: 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(\uparrow).

ABSOLUTE MAXIMUM RATING*

Parameter	Symbol	Rating	Unit
Voltage on VDD Supply Relative to Vss	VDD	-0.3 to 4.6	٧
Voltage on VDDQ Supply Relative to Vss	VDDQ	VDD	V
Voltage on Input Pin Relative to Vss	Vin	-0.3 to 6.0	V
Voltage on I/O Pin Relative to Vss	Vio	-0.3 to VDDQ + 0.5	٧
Power Dissipation	PD	1.2	W
Storage Temperature	Тѕтс	-65 to 150	င
Operating Temperature	TOPR	0 to 70	°C
Storage Temperature Range Under Bias	TBIAS	-10 to 85	r

*NOTE: Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.



OPERATING CONDITIONS($0^{\circ}C \le TA \le 70^{\circ}C$)

Parameter	Symbol	Min	Тур.	Max	Unit
Supply Voltage	VDD	3.13	3.3	3.47	V
Supply Voltage	VDDQ	3.13	3.3	3.47	V
Ground	Vss	0	0	0	V

CAPACITANCE*(TA = 25°C, f = 1MHz)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	CIN	VIN=0V	-	5	pF
Output Capacitance	Соит	Vout=0V	-	8	pF

^{*}NOTE: Sampled not 100% tested.

TEST CONDITIONS(TA = 0° to 70° , VDD = $3.3V \pm 5\%$, unless otherwise specified)

Parameter	l Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time(Measured at 0.3V and 2.7V)	2ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1

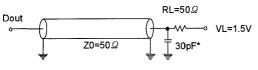
DC ELECTRICAL CHARACTERISTICS(TA = 0 °C to 70 °C, VDD = 3.3V ±5%)

Parameter	Symbol	Test Conditions	Min	Max	Unit	
Input Leakage Current(except ZZ)	lıL	VDD = Max , ViN = Vss to VDD	-2	+2	μA	
Output Leakage Current	loL	Output Disabled, Vout = Vss to Vo	-2	+2	μA	
Operating Current	Icc	Device Selected, lout = 0mA,	-8	-	330	mA
		ZZ≤ViL, All Inputs = ViL or ViH	-9	-	330	
		Cycle Time ≥ tCYC min	-10	-	300	
Standby Current	1	Device deselected, lout = 0mA,	-8	-	80	mA
	IsB	ZZ≤ViL, f = Max, All Inputs≤0.2V or ≥ VDD-0.2V	-9	-	80	
			-10	-	60	
	ISB1	Device deselected, IOUT = 0mA, $ZZ \le 0.2V$, f = 0, All Inputs = fixed (VDD-0.2V or 0.2V	-	10	mA	
	IsB2	Device deselected, IouT = 0mA, ZZ≥ VDD-0.2V, f = Max, All Inputs≤ VIL or ≥ VIH	-	10	mA	
Output Low Voltage	Vol	IOL = 8.0mA		-	0.4	٧
Output High Voltage	Voн	Iон = -4.0mA		2.4	-	٧
Input Low Voltage	VIL			-0.5*	0.8	٧
Input High Voltage	ViH			2.2	5.5**	٧

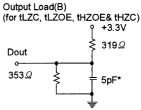
^{*} VIL(min) = -3.0(Pulse Width \leq 20ns)

^{**} In Case of I/O Pins, the Max. VIH = VDDQ + 0.5V





^{*} Including Scope and Jig Capacitance





AC TIMING CHARACTERISTICS (TA = 0° to 70° , VDD = $3.3V \pm 5\%$)

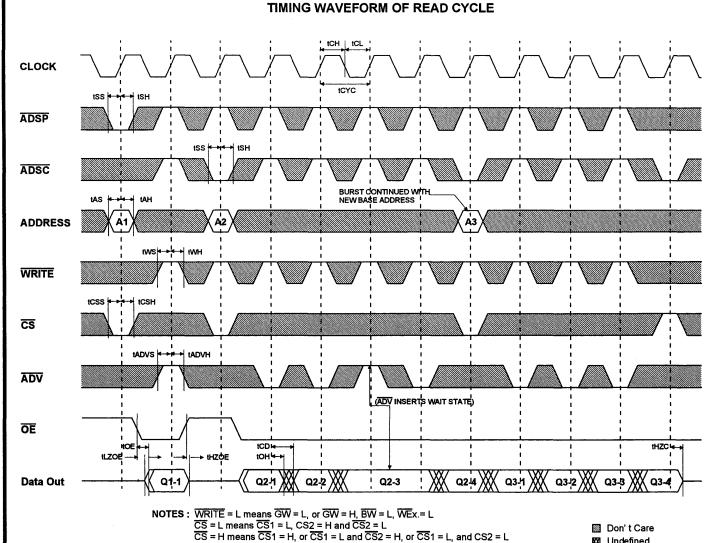
Parameter	Symbol	KM736V587-8		KM736V587-9		KM736V587-10		Unit
		Min	Max	Min	Max	Min	Max	Unit
Cycle Time	tCYC	12	-	12	-	15	-	ns
Clock Access Time	tCD	-	8.5	-	9	-	10	ns
Output Enable to Data Valid	tOE	-	4	-	4	-	5	ns
Clock High to Output Low-Z	tLZC	4	-	4	-	6	-	ns
Output Hold from Clock High	tOH	3	-	3	-	3	-	ns
Output Enable Low to Output Low-Z	tLZOE	0	-	0	-	0	-	ns
Output Enable High to Output High-Z	tHZOE	2	5	2	5	2	5	ns
Clock High to Output High-Z	tHZC	-	5	-	5	-	6	ns
Clock High Pulse Width	tCH	4	-	4	-	5		ns
Clock Low Pulse Width	tCL	4	-	4	-	5	-	ns
Address Setup to Clock High	tAS	2.5	-	2.5	-	2.5	-	ns
Address Status Setup to Clock High	tSS	2.5	-	2.5	-	2.5	-	ns
Data Setup to Clock High	tDS	2.5	-	2.5	•	2.5	-	ns
Write Setup to Clock High	tWS	2.5		2.5	-	2.5	-	ns
Address/Advance Setup to Clock High	tADVS	2.5	-	2.5	-	2.5	-	ns
Chip Select Setup to Clock High	tCSS	2.5	-	2.5	-	2.5	-	ns
Address Hold from Clock High	tAH	0.5	- ,	0.5	-	0.5	-	ns
Address Status Hold from Clock High	tSH	0.5	-	0.5	-	0.5	-	ns
Data Hold from Clock High	tDH	0.5	-	0.5	-	0.5	-	ns
Write Hold from Clock High	tWH	0.5	-	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	tADVH	0.5	-	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	tCSH	0.5	-	0.5	-	0.5	-	ns
ZZ High to Power Down	tPDS	2	-	2	-	2	-	cycle
ZZ Low to Power Up	tPUS	2	-	2	-	2	-	cycle

NOTE: 1. All address inputs must meet the specified setup and hold times for all rising clock edges whenever ADSC and/or ADSP is sampled low and CS is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.

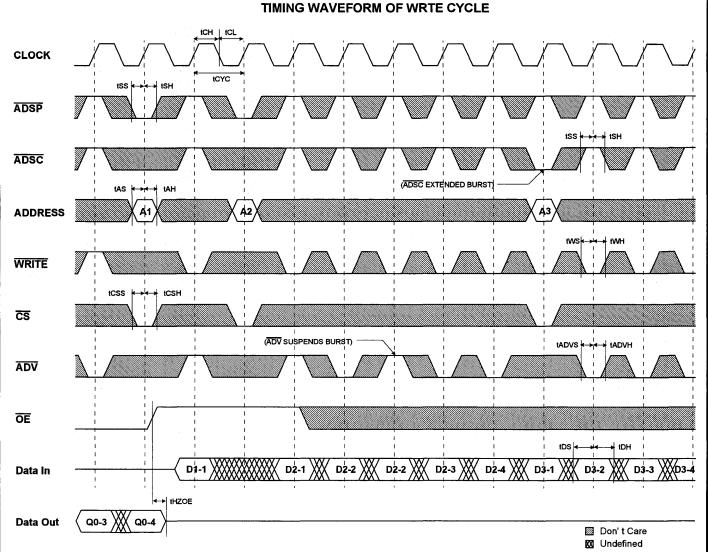
2. Both chip selects must be active whenever ADSC or ADSP is sampled low in order for the this device to remain enabled.

3. ADSC or ADSP must not be asserted for at least 2 Clock after leaving ZZ state.

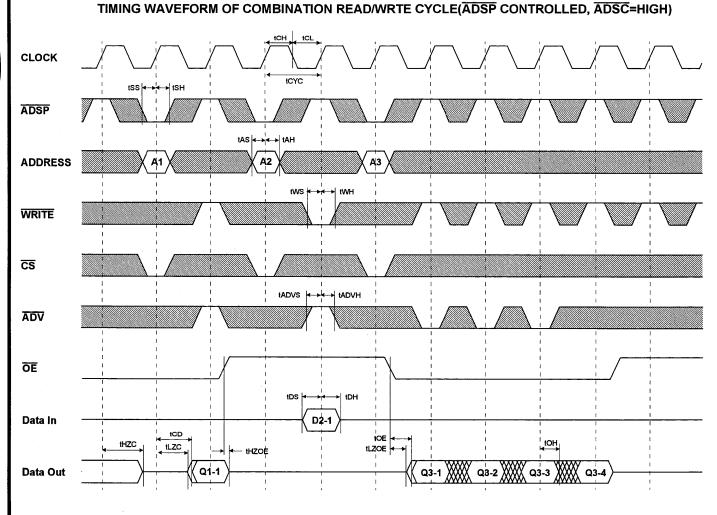


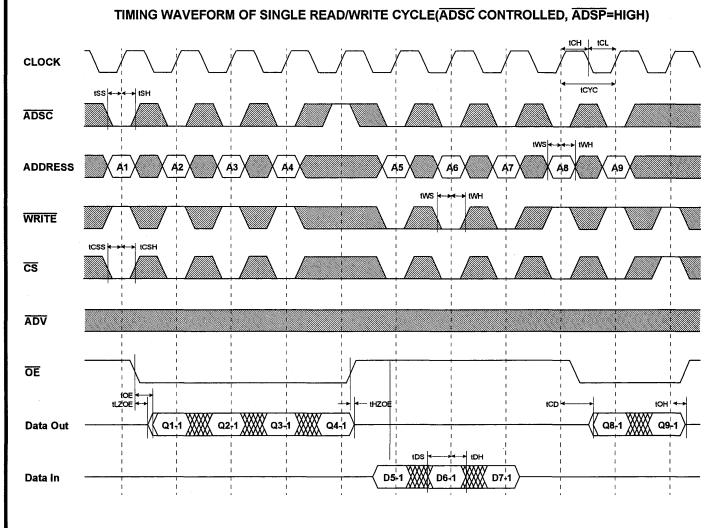


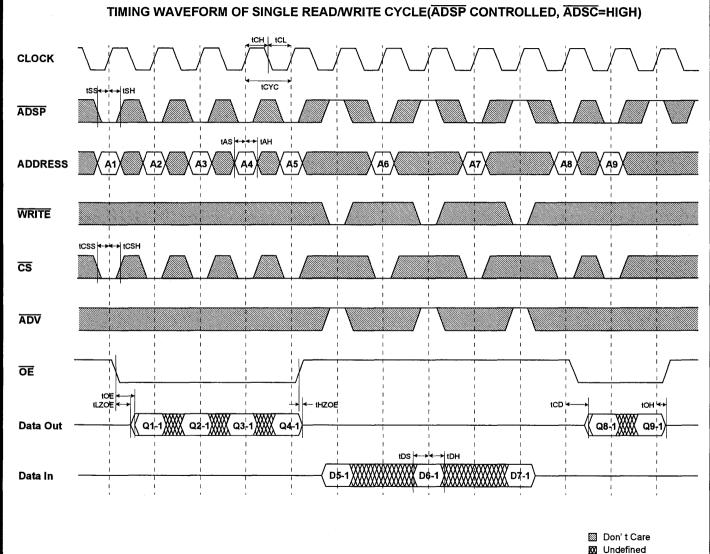
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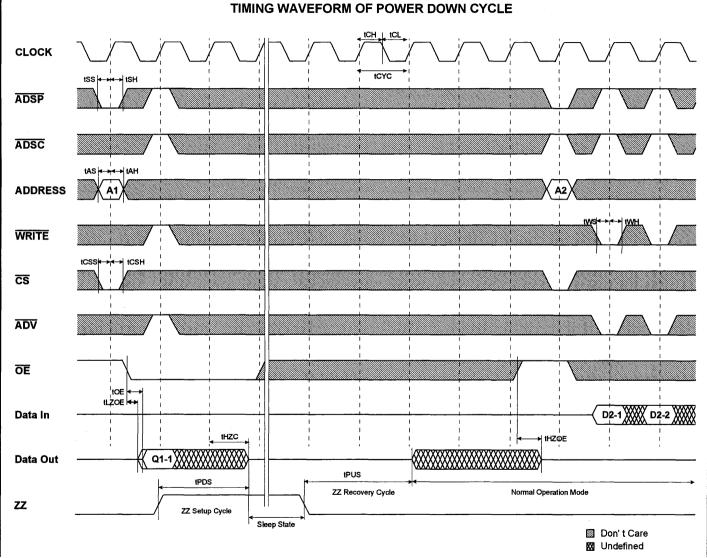




SAMSUNG

ELECTRONICS

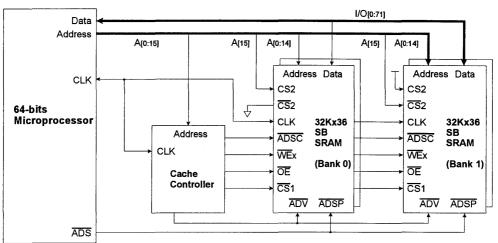
SAMSUNG



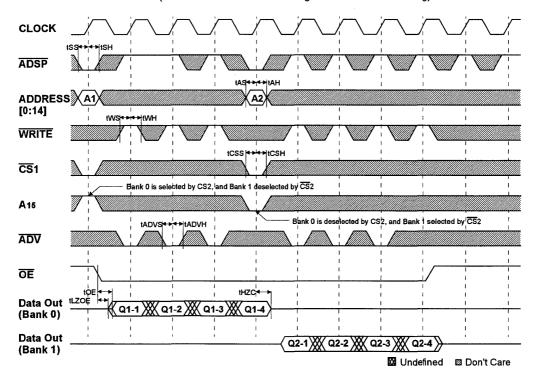
APPLICATION INFORMATION

DEPTH EXPANSION

The Samsung 32Kx36 Synchronous Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 32K depth to 64K depth without extra logic.



INTERLEAVE READ TIMING (Refer non-interleave write timing for interleave write timing)



2M Mid Range Synchronous SRAM

64Kx32-Bit Synchronous Pipelined Burst SRAM

FEATURES

- · Synchronous Operation.
- 2 Stage Pipelined operation with 4 Burst.
- · On-Chip Address Counter.
- · Self-Timed Write Cycle.
- · On-Chip Address and Control Registers.
- VDD=3.3V-5%/+10% Power Supply
- I/O Supply Voltage: 3.3V-5%/+10%
- . 5V Tolerant Inputs except I/O Pins.
- · Byte Writable Function.
- · Global Write Enable Controls a full bus-width write.
- · Power Down State via ZZ Signal.
- · Asynchronous Output Enable Control.
- ADSP, ADSC, ADV Burst Control Pins.
- LBO Pin allows a choice of either a interleaved burst or a linear burst.
- Three Chip Enables for simple depth expansion with No Data Contention; 2 cycle Enable, 1 cycle Disable.
- . TTL-Level Three-State Output.
- . 100-Pin QFP/TQFP Package

FAST ACCESS TIMES

Parameter	Symbol	-13	-15	Unit
Cycle Time	tCYC	13	15	ns
Clock Access Time	tCD	7	8	ns
Output Enable Access Time	tOE	6	7	ns

GENERAL DESCRIPTION

The KM732V688/L is a 2,097,152 bit Synchronous Static Random Access Memory designed for high performance second level cache of Pentium and Power PC based System.

It is organized as 64K words of 32 bits and integrates address and control registers, a 2-bit burst address counter and added some new functions for high performance cache RAM applications; $\overline{\text{GW}}$, $\overline{\text{BW}}$, $\overline{\text{LBO}}$, ZZ.

Write cycles are internally self-timed and synchronous.

Full bus-width write is done by \overline{GW} , and each byte write is performed by the combination of $\overline{WE}x$ and \overline{BW} when \overline{GW} is high. And with $\overline{CS1}$ high, \overline{ADSP} is blocked to control signals.

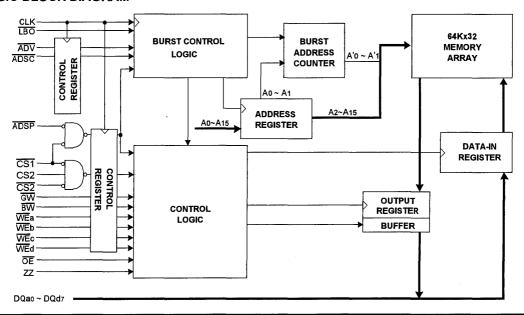
Burst cycle can be initiated with either the address status processor(ADSP) or address status cache controller(ADSC) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance(ADV) input.

LBO pin is DC operated and determines burst sequence(linear or interleaved).

ZZ pin controls Power Down State and reduces Stand-by current regardless of CLK.

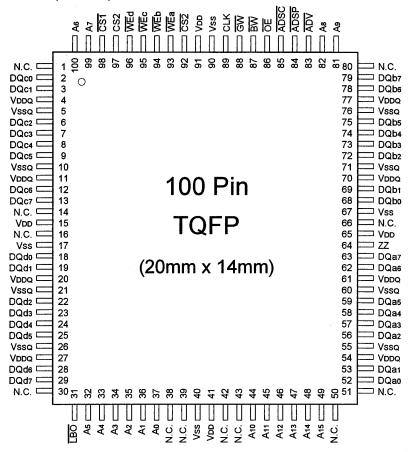
The KM732V688/L is fabricated using SAMSUNG's high performance CMOS technology and is available in a 100pin QFP/TQFP package. Multiple power and ground pins are utilized to minimize ground bounce.

LOGIC BLOCK DIAGRAM





PIN CONFIGURATION (TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A15	Address Inputs	32,33,34,35,36,37,	VDD	Power Supply(+3.3V)	15,41,65,91
		44,45,46,47,48,49,	Vss	Ground	17,40,67,90
		81,82,99,100	N.C.	No Connect	1,14,16,30,38,39,42,43,
ADV	Burst Address Advance	83			50,51,66,80
ADSP	Address Status Processor	84	DQa0 ~ a7	Data Inputs/Outputs	52,53,56,57,58,59,62,63
ADSC	Address Status Controller	85	DQb0 ~ b7		68,69,72,73,74,75,78,79
CLK	Clock	89	DQc0 ~ c7		2,3,6,7,8,9,12,13
CS1	Chip Select	98	DQdo ~ d7		18,19,22,23,24,25,28,29
CS2	Chip Select	97	VDDQ	Output Power Supply	4,11,20,27,54,61,70,77
CS2	Chip Select	92	1	(+3.3V)	
WE x	Byte Write Inputs	93,94,95,96	VssQ	Output Ground	5,10,21,26,55,60,71,76
ŌĒ	Output Enable	86	1	· ·	
Ġ₩	Global Write Enable	88	1		
BW	Byte Write Enable	87			
ZZ	Power Down Input	64			
LBO	Burst Mode Control	31			



FUNCTION DESCRIPTION

The KM732V688/L is a synchronous SRAM designed to support the burst address accessing sequence of the CISC and RISC microprocessor. All inputs(with the exception of OE, LBO and ZZ) are sampled on rising clock edges. The start and duration of the burst access is controlled by ADSC, ADSP and ADV and chip select pins.

The accesses are enabled with the chip select signals and output enabled signals. Wait states are inserted into the access with ADV.

When ZZ is pulled high, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM normally operates after 2 cycles of wake up time. ZZ pin is pulled down internally.

Read cycles are initiated with $\overline{\text{ADSP}}$ (regardless of $\overline{\text{WEx}}$ and $\overline{\text{ADSC}}$) using the new external address clocked into the on-chip address register whenever $\overline{\text{ADSP}}$ is sampled low, the chip selects are sampled active, and the output buffer is enabled with $\overline{\text{OE}}$. In read operation the data of cell array accessed by the current address, registered in the Data-out registers by the positive edge of CLK, are carried to the Data-out buffer by the next positive edge of CLK. The data, registered in the Data-out buffer, are projected to the output pins. $\overline{\text{ADV}}$ is ignored on the clock edge that samples $\overline{\text{ADSP}}$ asserted, but is sampled on the subsequent clock edges. The address increases internally for the next access of the burst when $\overline{\text{WEx}}$ are sampled High and $\overline{\text{ADV}}$ is sampled Low. And $\overline{\text{ADSP}}$ is blocked to control signals by disabling $\overline{\text{CS}}$ 1.

All byte write is done by \overline{GW} (regardless of \overline{BW} and $\overline{WE}x$.), and each byte write is performed by the combination of \overline{BW} and $\overline{WE}x$ when \overline{GW} is High.

Write cycles are performed by disabling the output buffers with \overline{OE} and asserting $\overline{WE}x$. $\overline{WE}x$ are ignored on the clock edge that samples \overline{ADSP} Low, but are sampled on the subsequent clock edges. The output buffers are disabled when $\overline{WE}x$ are sampled Low(regardless of \overline{OE}). Data is clocked into the data input register when $\overline{WE}x$ sampled Low. The address increases internally to the next address of burst, if both $\overline{WE}x$ and \overline{ADV} are sampled Low. Individual byte write cycles are performed by any one or more byte write enable signals($\overline{WE}a$, $\overline{WE}b$, $\overline{WE}c$ or $\overline{WE}b$) sampled low. The $\overline{WE}a$ controls DQa0 ~ DQa7, $\overline{WE}b$ controls DQb0 ~ DQb7, $\overline{WE}c$ control DQc0 ~ DQc7, and $\overline{WE}d$ controls DQd0 ~ DQd7. Read or write cycle may also be initiated with \overline{ADSC} , instead of \overline{ADSP} . The differences between cycles initiated with \overline{ADSC} and \overline{ADSP} as are follows:

ADSP must be sampled high when ADSC is sampled low to initiate a cycle with ADSC. WEx are sampled on the same clock edge that sampled ADSC low(and ADSP high).

Addresses are generated for the burst access as shown below, The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the BO pin. When this pin is Low, linear burst sequence is selected. When this pin is High, Interleaved burst sequence is selected.

BURST SEQUENCE TABLE

(Interleaved Burst)

EBO PIN HIGH	Case 1		Case 2		Ca	se 3	Case 4		
	A1	A0	A1	A0	A1	A0	A1	A0	
First Address	0	0	0	1	1	0	1	1	
	0	1	0	0	1	1	1	0	
√	1 1	0	1	1	0	0	0	1	
Fourth Address	1 1	1	1	0	0	1	0	0	

(Linear Burst)

LBO PIN LOW	Case 1 Case 2			Cas	se 3	Case 4		
EBOT III	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
	0	[1	1	0	1	1	0	0
	1	0	1	1	0	0	l 0	1
Fourth Address	1	1	0	0	0	1	1	0

NOTE: 1. LBO pin must be tied to High or Low, and Floating State must not be allowed.



TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

CS1	CS2	CS2	ADSP	ADSC	ADV	WRITE	CLK	Address Accessed	Operation
Н	X	Х	Х	L	Х	Х	1	N/A	Not Selected
L	L	Х	L	Х	X	Х	1	N/A	Not Selected
L	Х	Н	L	Х	Х	Х	1	N/A	Not Selected
L	L	Х	Х	L	Х	Х	1	N/A	Not Selected
L	X	Н	Х	Г	Х	Х	1	N/A	Not Selected
L	Н	L	· L	Х	Х	Х	1	External Address	Begin Burst Read Cycle
L	Н	L	Н	L	Х	١	1	External Address	Begin Burst Write Cycle
L	н	L	Н	٦	Х	Н	1	External Address	Begin Burst Read Cycle
Х	Х	Х	Н	Н	L	Н	1	Next Address	Continue Burst Read Cycle
Н	X	Х	Х	Н	L	Н	1	Next Address	Continue Burst Read Cycle
Х	Х	Х	Н	Н	L	L	1	Next Address	Continue Burst Write Cycle
Н	Х	Х	Х	Н	L	L	1	Next Address	Continue Burst Write Cycle
Х	Х	Х	Н	Н	Н	H	1	Current Address	Suspend Burst Read Cycle
Н	Х	Х	X	Н	Н	Н	1	Current Address	Suspend Burst Read Cycle
Х	Х	Х	Н	Н	Н	L	1	Current Address	Suspend Burst Write Cycle
Н	Х	Х	Х	Н	Н	L	1	Current Address	Suspend Burst Write Cycle

NOTE: 1. X means "Don't Care".

- 2. The rising edge of clock is symbolized by 1.
- 3. WRITE = L means Write operation in WRITE TRUTH TABLE.
 - WRITE = H means Read operation in WRITE TRUTH TABLE.
- 4. Operation finally depends on status of asynchronous input pins(ZZ and OE).

WRITE TRUTH TABLE

GW	BW	WEa	WEb	WEc	WEd	Operation
Н	Н	Х	Х	Х	Х	READ
Н	L	H	Н	Н	Н	READ
Н	L	L	H	Н	Н	WRITE BYTE a
н	L	Н	الـ	Н	Н	WRITE BYTE b
Н	L	Н	Н	L	L	WRITE BYTE c and d
Н	L	Ł	L	L	L	WRITE ALL BYTEs
L	Х	Х	Х	X	Х	WRITE ALL BYTES

NOTE: 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(1).

ASYNCHRONOUS TRUTH TABLE

(See Notes 1 and 2):

Operation	ZZ	ŌĒ	I/O Status
Sleep Mode	Н	Х	High-Z
Read	L	L	DQ
Read	L	Н	High-Z
Write	L	Х	Din, High-Z
Deselected	L	×	High-Z

NOTE

- 1. X means "Don't Care".
- 2. ZZ pin is pulled down internally
- 3. For write cycles that following read cycles, the output buffers must be disabled with \overline{OE} , otherwise data bus contention will occur.
- Sleep Mode means power down state of which stand-by current does not depend on cycle time.
- Deselected means power down state of which stand-by current depends on cycle time.



PASS-THROUGH TRUTH TABLE

Previous Cycle		Presen	t Cycle			New Code	
Operation	WRITE	Operation		CS1 WRITE		Next Cycle	
Write Cycle, All bytes Address=An-1, Data=Dn-1		Initiate Read Cycle Address=An Data=Qn-1 for all bytes	L	Н	L	Read Cycle Data=Qn	
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=Qn-1 for all bytes	Н	н	L	No carryover from previous cycle	
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=High-Z	Н	н	Н	No carryover from previous cycle	
Write Cycle, One byte Address=An-1, Data=Dn-1	One L	Initiate Read Cycle Address=An Data=Qn-1 for one byte	L	Н	L	Read Cycle Data=Qn	
Write Cycle, One byte Address=An-1, Data=Dn-1	One L	No new cycle Data=Qn-1 for one byte	Н	н	L	No carryover from previous cycle	

NOTE: This operation makes written data immediately available at output during a read cycle preceded by a write cycle.

ABSOLUTE MAXIMUM RATING*

Parameter	Symbol	Rating	Unit
Voltage on VDD Supply Relative to Vss	VDD	-0.3 to 4.6	V
Voltage on VDDQ Supply Relative to Vss	VDDQ	VDD	٧
Voltage on Input Pin Relative to Vss	Vin	-0.3 to 6.0	V
Voltage on I/O Pin Relative to Vss	Vio	-0.3 to VDDQ+ 0.5	V
Power Dissipation	PD	1.2	W
Storage Temperature	Тѕтс	-65 to 150	°C
Operating Temperature	Topr	0 to 70	°C
Storage Temperature Range Under Bias	TBIAS	-10 to 85	°C

*NOTE: Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS (0°C ≤ TA ≤ 70°C)

Parameter	Symbol	Min	Тур.	Max	Unit
Supply Voltage	VDD	3.13	3.3	3.6	V
	VDDQ	3.13	3.3	3.6	٧
Ground	Vss	0	0	0	V

CAPACITANCE*(TA = 25°C, f = 1MHz)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	CIN	VIN=0V		5	pF
Output Capacitance	Соит	Vout=0V	-	7	pF

^{*}NOTE: Sampled not 100% tested.

DC ELECTRICAL CHARACTERISTICS

 $(VDD=3.3V-5\%/+10\%, VDDQ=3.3V-5\%/+10\%, TA = 0 \degree to 70 \degree)$

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current(except ZZ)	liL	VDD = Vss to VDD, VIN = Vss to VDD		-2	+2	μA
Output Leakage Current	loL	Output Disabled, Vout = Vss to VDD	2	-2	+2	μA
Operating Current	lcc	Device Selected, Iout = 0mA,	-13	-	250	mA
		ZZ≤ViŁ, All Inputs = ViL or ViH	-15	-	220	
		Cycle Time ≥ tCYC min				
Standby Current	ISB	Device deselected, lout = 0mA, ZZ≤	VIL,		60	mA
		f = Max, All Inputs ≤ 0.2V or ≥ VDD-0	_		1111/4	
		Device deselected, IOUT = 0mA,		-	10	mA
	ISB1	$ZZ \leq 0.2V$, $f = 0$,			, ,	
		All Inputs = fixed(VDD-0.2V or 0.2V)	L-Ver.	-	2.0	mA
		Device deselected, Iout = 0mA,		_	10	mA
	IsB2	ZZ≥VDD-0.2V, f = Max,				
		All Inputs≤VIL or ≥VIH	L-Ver.		1	mΑ
Output Low Voltage	Vol	IOL = 8.0mA		-	0.4	V
Output High Voltage	Voн	IOH = -4.0mA		2.4	-	V
Input Low Voltage	VIL			-0.5*	0.8	V
Input High Voltage	VIH		2.0	5.5**	V	

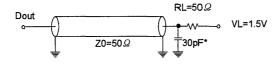
^{*} VIL(min) = -3.0(Pulse Width ≤ 20ns)
** In Case of I/O Pins, the Max. VIH = VDDQ + 0.5V

TEST CONDITIONS

(TA = 0 $^{\circ}$ C to 70 $^{\circ}$ C, VDD=3.3V-5%/+10%, VDDQ=3.3V-5%/+10%, unless otherwise specified)

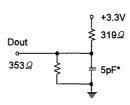
Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time(Measured at 0.3V and 2.7V)	2ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1

Output Load(A)



* Capacitive Load consists of all components of the test environment.

Output Load(B) (for tLZC, tLZOE, tHZOE& tHZC)



* Including Scope and Jig Capacitance

Fig. 1

AC TIMING CHARACTERISTICS

(VDD=3.3V-5%/+10%, TA = 0% to 70%)

Parameter	Symbol	KM732	V688-13	KM732V688-15		Unit
Parameter	Symbol	Min	Max	Min	Max	Unit
Cycle Time	tCYC	13	-	15	-	ns
Clock Access Time	tCD	-	7	-	8	ns
Output Enable to Data Valid	tOE	-	6	-	7	ns
Clock High to Output Low-Z	tLZC	0	-	0	-	ns
Output Hold from Clock High	tOH	2.0	-	2.0	-	ns
Output Enable Low to Output Low-Z	tLZOE	0	-	0	-	ns
Output Enable High to Output High-Z	tHZOE	-	4.0	-	4.0	ns
Clock High to Output High-Z	tHZC	1.5	5.0	1.5	5.0	ns
Clock High Pulse Width	tCH	4.5	-	5.5	-	ns
Clock Low Pulse Width	tCL	4.5	-	5.5	-	ns
Address Setup to Clock High	tAS	2.5	-	2.5	-	ns
Address Status Setup to Clock High	tSS	2.5	-	2.5	-	ns
Data Setup to Clock High	tDS	2.5	-	2.5	-	ns
Write Setup to Clock High(GW, BW, WEx)	tWS	2.5	-	2.5	-	ns
Address Advance Setup to Clock High	tADVS	2.5	-	2.5	-	ns
Chip Select Setup to Clock High	tCSS	2.5	-	2.5	-	ns
Address Hold from Clock High	tAH	0.5	-	0.5	-	ns
Address Status Hold from Clock High	tSH	0.5	-	0.5	-	ns
Data Hold from Clock High	tDH	0.5	-	0.5	-	ns
Write Hold from Clock High(GW, BW, WEx)	tWH	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	tADVH	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	tCSH	0.5	-	0.5	-	ns
ZZ High to Power Down	tPDS	2	-	2	-	cycle
ZZ Low to Power Up	tPUS	2	-	2	-	cycle

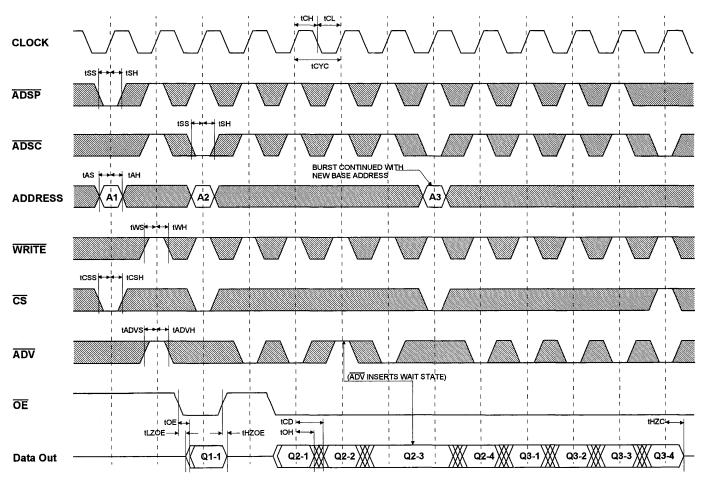
NOTE: 1. All address inputs must meet the specified setup and hold times for all rising clock edges whenever ADSC and/or ADSP is sampled low and CS is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.

2. Both chip selects must be active whenever ADSC or ADSP is sampled low in order for the this device to remain enabled.

3. ADSC or ADSP must not be asserted for at least 2 Clock after leaving ZZ state.



TIMING WAVEFORM OF READ CYCLE



NOTES: WRITE = L means GW = L, or GW = H, BW = L, WEx = L

 $\overline{\text{CS}}$ = L means $\overline{\text{CS}}$ 1 = L, CS2 = H and $\overline{\text{CS}}$ 2 = L

 \overline{CS} = H means \overline{CS} 1 = H, or \overline{CS} 1 = L and \overline{CS} 2 = H, or \overline{CS} 1 = L, and \overline{CS} 2 = L

Don't Care Undefined

VMSUNG

ELECTRONICS

D2-2 XX

tDS -

→ tDH

Don't Care

☑ Undefined

ADV

ŌĒ

Data In

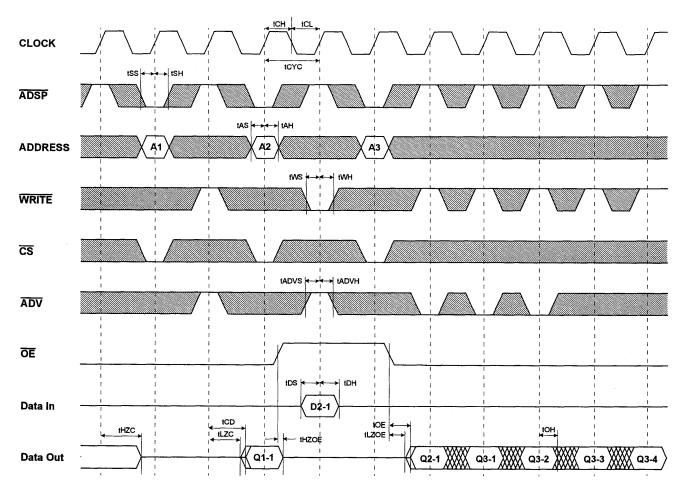
Data Out

←→ tHZOE

Q0-4

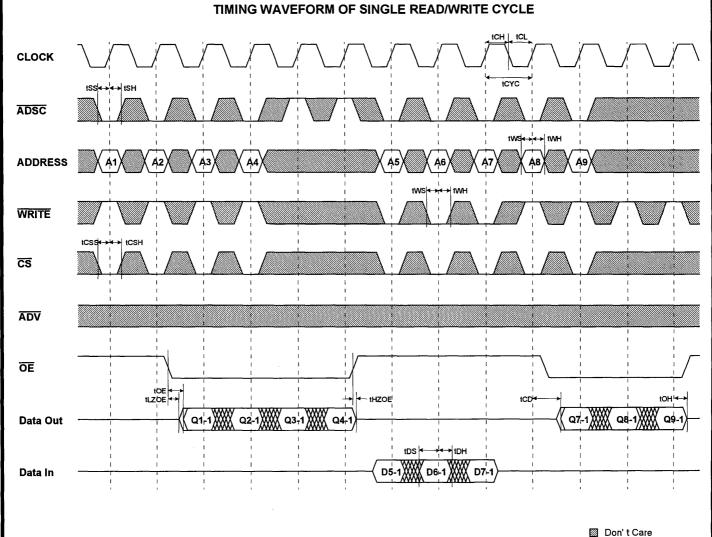
Q0-3 XX

TIMING WAVEFORM OF COMBINATION READ/WRTE CYCLE



Don't Care ☑ Undefined

☑ Undefined



tPUS

ZZ Recovery Cycle

D2-1 D2-2 D2-2

Don't Care

Undefined

KM732V688/L

Data in

Data Out

ZZ

ILZOE **

Q1-1

tPDS

ZZ Setup Cycle

Sleep State

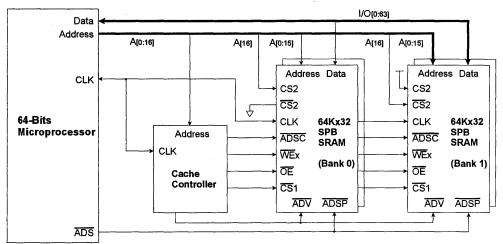
+ tHZOE

Normal Operation Mode

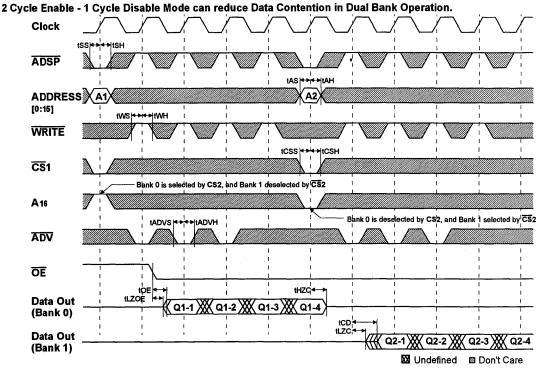
APPLICATION INFORMATION

DEPTH EXPANSION

The Samsung 64Kx32 Synchronous Pipelined Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 64K depth to 128K depth without extra logic.



INTERLEAVE READ TIMING (Refer non-interleave write timing for interleave write timing)





64Kx32-Bit Synchronous Pipelined Burst SRAM FEATURES GENE

- · Synchronous Operation.
- 2 Stage Pipelined operation with 4 Burst.
- · On-Chip Address Counter.
- · Self-Timed Write Cycle.
- On-Chip Address and Control Registers.
- VDD=3.3V-5%/+10% Power Supply for 3.3V I/O
- VDD=3.3V±5% Power Supply for 2.5V I/O
- I/O Supply Voltage: 3.3V-5%/+10% for 3.3V I/O or 2.5V+0.4V/-0.13V for 2.5V I/O
- 5V Tolerant Inputs except I/O Pins.
- · Byte Writable Function.
- . Global Write Enable Controls a full bus-width write.
- · Power Down State via ZZ Signal.
- LBO Pin allows a choice of either a interleaved burst or a linear burst.
- Three Chip Enables for simple depth expansion with No Data Contention; 2 cycle Enable, 1 cycle Disable.
- · Asynchronous Output Enable Control.
- ADSP, ADSC, ADV Burst Control Pins.
- . TTL-Level Three-State Output.
- 100-Pin TQFP Package

FAST ACCESS TIMES

Parameter	Symbol	-13	-15	Unit
Cycle Time	tCYC	13	15	ns
Clock Access Time	tCD	7	8	ns
Output Enable Access Time	tOE	6	7	ns

GENERAL DESCRIPTION

The KM732V696/L is a 2,097,152 bit Synchronous Static Random Access Memory designed for high performance second level cache of Pentium and Power PC based System.

It is organized as 64K words of 32 bits and integrates address and control registers, a 2-bit burst address counter and added some new functions for high performance cache RAM applications; $\overline{\text{GW}}$, $\overline{\text{BW}}$, $\overline{\text{LBO}}$, ZZ. Write cycles are internally self-timed and synchronous.

Full bus-width write is done by \overline{GW} , and each byte write is performed by the combination of $\overline{WE}x$ and \overline{BW} when \overline{GW} is high. And with $\overline{CS1}$ high, \overline{ADSP} is blocked to control signals.

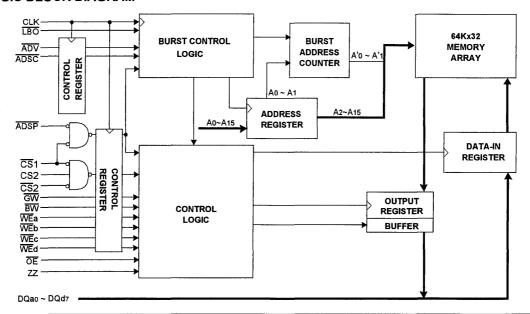
Burst cycle can be initiated with either the address status processor(ADSP) or address status cache controller(ADSC) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance(ADV) input.

LBO pin is DC operated and determines burst sequence(linear or interleaved).

ZZ pin controls Power Down State and reduces Stand-by current regardless of CLK.

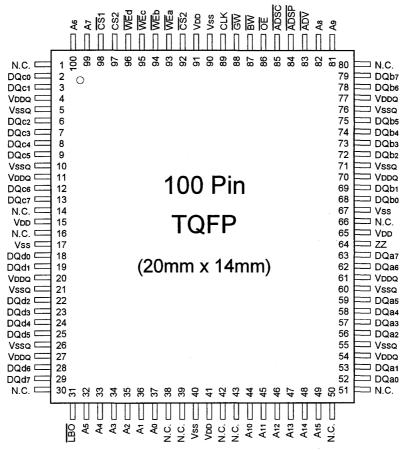
The KM732V696/L is fabricated using SAMSUNG's high performance CMOS technology and is available in a 100pin TQFP package. Multiple power and ground pins are utilized to minimize ground bounce.

LOGIC BLOCK DIAGRAM





PIN CONFIGURATION (TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A15	Address Inputs	32,33,34,35,36,37,	VDD	Power Supply(+3.3V)	15,41,65,91
	·	44,45,46,47,48,49,	Vss	Ground	17,40,67,90
		81,82,99,100	N.C.	No Connect	1,14,16,30,38,39,42,43,
ADV	Burst Address Advance	83			50,51,66,80
ADSP	Address Status Processor	84	DQa0 ~ a7	Data Inputs/Outputs	52,53,56,57,58,59,62,63
ADSC	Address Status Controller	85	DQb0 ~ b7		68,69,72,73,74,75,78,79
CLK	Clock	89	DQc0 ~ c7	·	2,3,6,7,8,9,12,13
CS1	Chip Select	98	DQd0 ~ d7		18,19,22,23,24,25,28,29
CS2	Chip Select	97		1	
CS2	Chip Select	92	VDDQ	Output Power Supply	4,11,20,27,54,61,70,77
WEx	Byte Write Inputs	93,94,95,96		(2.5V or 3.3V)	ļ
ŌĒ	Output Enable	86	Vssq	Output Ground	5,10,21,26,55,60,71,76
Ġ₩	Global Write Enable	88	ı		
BW	Byte Write Enable	87	1		
ZZ	Power Down Input	64	ŀ		
<u>LBO</u>	Burst Mode Control	31	ŀ		



FUNCTION DESCRIPTION

The KM732V696/L is a synchronous SRAM designed to support the burst address accessing sequence of the CISC and RISC microprocessor. All inputs(with the exception of OE, LBO and ZZ) are sampled on rising clock edges. The start and duration of the burst access is controlled by ADSC, ADSP and ADV and chip select pins.

The accesses are enabled with the chip select signals and output enabled signals. Wait states are inserted into the access with ADV.

When ZZ is pulled high, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM normally operates after 2 cycles of wake up time. ZZ pin is pulled down internally.

Read cycles are initiated with $\overline{\text{ADSP}}$ (regardless of $\overline{\text{WEx}}$ and $\overline{\text{ADSC}}$) using the new external address clocked into the on-chip address register whenever $\overline{\text{ADSP}}$ is sampled low, the chip selects are sampled active, and the output buffer is enabled with $\overline{\text{OE}}$. In read operation the data of cell array accessed by the current address, registered in the Data-out registers by the positive edge of CLK, are carried to the Data-out buffer by the next positive edge of CLK. The data, registered in the Data-out buffer, are projected to the output pins. $\overline{\text{ADV}}$ is ignored on the clock edge that samples $\overline{\text{ADSP}}$ asserted, but is sampled on the subsequent clock edges. The address increases internally for the next access of the burst when $\overline{\text{WEx}}$ are sampled High and $\overline{\text{ADV}}$ is sampled Low. And $\overline{\text{ADSP}}$ is blocked to control signals by disabling $\overline{\text{CS}1}$.

All byte write is done by \overline{GW} (regardless of \overline{BW} and \overline{WEx} .), and each byte write is performed by the combination of \overline{BW} and \overline{WEx} when \overline{GW} is High.

Write cycles are performed by disabling the output buffers with \overline{OE} and asserting \overline{WEx} . \overline{WEx} are ignored on the clock edge that samples \overline{ADSP} Low, but are sampled on the subsequent clock edges. The output buffers are disabled when \overline{WEx} are sampled Low(regardless of \overline{OE}). Data is clocked into the data input register when \overline{WEx} sampled Low. The address increases internally to the next address of burst, if both \overline{WEx} and \overline{ADV} are sampled Low. Individual byte write cycles are performed by any one or more byte write enable signals(\overline{WEx}), \overline{WEx}) and \overline{ADV} are sampled low. The \overline{WEx} controls $\overline{DQao} \sim \overline{DQao}$, \overline{WEx}) controls $\overline{DQao} \sim \overline{DQao}$, \overline{WEx} controls $\overline{DQao} \sim \overline{DQao}$. Read or write cycle may also be initiated with \overline{ADSO} , instead of \overline{ADSO} . The differences between cycles initiated with \overline{ADSO} and \overline{ADSO} as are follows:

ADSP must be sampled high when ADSC is sampled low to initiate a cycle with ADSC. WEx are sampled on the same clock edge that sampled ADSC low(and ADSP high).

Addresses are generated for the burst access as shown below, The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the LBO pin. When this pin is Low, linear burst sequence is selected. When this pin is High, Interleaved burst sequence is selected.

BURST SEQUENCE TABLE

(Interleaved Burst)

LBO PIN HIGH	IGU Case 1			se 2	Cas	se 3	Case 4	
LDO FIN HIGH	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
	0	1	0	0	1	1	1	0
\downarrow	1 1	0	1	1	0	0	0	1
Fourth Address	1 1	1	1	0	0	1	0	0

(Linear Burst)

LBO PIN LOW	Case 1		Case 2		Ca	se 3	Case 4	
LDO I III	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
	0	1	1	0	1	1	0	0
	1	0	1	1	0	0	0	1
Fourth Address	1	1	0	0	0	1	1	0

NOTE: 1. LBO pin must be tied to High or Low, and Floating State must not be allowed.



TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

CS1	CS2	CS2	ADSP	ADSC	ADV	WRITE	CLK	Address Accessed	Operation
H	Х	Х	X	L	Х	Х	1	N/A	Not Selected
L	L	Х	L	X	Х	Х	1	N/A	Not Selected
L	Х	H	L	Х	Х	Х	1	N/A	Not Selected
L	L	Х	Х	L	Х	Х	1	N/A	Not Selected
L	Х	Τ	Х	L	Х	Х	1	N/A	Not Selected
L	Н	L	L	Х	Χ	Х	1	External Address	Begin Burst Read Cycle
L	Н	L	Н	L	Х	٦	1	External Address	Begin Burst Write Cycle
L	Н	L	Н	L	Χ	Н	1	External Address	Begin Burst Read Cycle
Х	Х	Х	Н	Н	L	Н	1	Next Address	Continue Burst Read Cycle
Н	Х	Х	Х	Н	L	Н	1	Next Address	Continue Burst Read Cycle
Х	Х	Х	Н	Н	L	L	1	Next Address	Continue Burst Write Cycle
Н	Х	Х	X	Н	L	L	1	Next Address	Continue Burst Write Cycle
Х	Х	Х	Н	Н	Н	Н	1	Current Address	Suspend Burst Read Cycle
Н	Х	X	Х	Н	H	Н	1	Current Address	Suspend Burst Read Cycle
Х	Х	Χ	Н	Н	Н	L	1	Current Address	Suspend Burst Write Cycle
Н	Х	Х	Х	Н	Н	L	1	Current Address	Suspend Burst Write Cycle

NOTE: 1. X means "Don't Care".

- 2. The rising edge of clock is symbolized by 1.
- 3. WRITE = L means Write operation in WRITE TRUTH TABLE.
 WRITE = H means Read operation in WRITE TRUTH TABLE.
- 4. Operation finally depends on status of asynchronous input pins(ZZ and OE).

WRITE TRUTH TABLE

GW	BW	WEa	WEb	WEc	WEd	Operation
Н	Н	Х	Х	X	Х	READ
Н	L	Н	Н	Н	Н	READ
Н	L	L	Н	Н	Н	WRITE BYTE a
Н	L	Н	L	Н	Н	WRITE BYTE b
Н	L	Н	Н	L	L	WRITE BYTE c and d
Н	L	L	L	L	L	WRITE ALL BYTEs
L	Х	X	X	X	Х	WRITE ALL BYTEs

NOTE: 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(\uparrow).

ASYNCHRONOUS TRUTH TABLE

(See Notes 1 and 2):

Operation	ZZ	ŌĒ	I/O Status
Sleep Mode	Н	Х	High-Z
Dand	L	L	DQ
Read	L	Н	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

NOTE

- 1. X means "Don't Care".
- 2. ZZ pin is pulled down internally
- 3. For write cycles that following read cycles, the output buffers must be disabled with $\overline{\text{OE}}$, otherwise data bus contention will occur.
- Sleep Mode means power down state of which stand-by current does not depend on cycle time.
- Deselected means power down state of which stand-by current depends on cycle time.



PASS-THROUGH TRUTH TABLE

Previous Cycle Operation WRITE		Present	Cycle			W
		Operation CS		CS1 WRITE		Next Cycle
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	Initiate Read Cycle Address=An Data=Qn-1 for all bytes	L	н	L	Read Cycle Data=Qn
Write Cycle, All bytes Address=An-1, Data=Dn-1		No new cycle Data=Qn-1 for all bytes	н	Н	L	No carryover from previous cycle
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=High-Z	Н	н	Н	No carryover from previous cycle
Write Cycle, One byte Address=An-1, Data=Dn-1		Initiate Read Cycle Address=An Data=Qn-1 for one byte	L	Н	L	Read Cycle Data=Qn
Write Cycle, One byte Address=An-1, Data=Dn-1	One L	No new cycle Data=Qn-1 for one byte	Н	н	L	No carryover from previous cycle

NOTE: This operation makes written data immediately available at output during a read cycle preceded by a write cycle.

ABSOLUTE MAXIMUM RATING*

Parameter	Symbol	Rating	Unit
Voltage on VDD Supply Relative to Vss	VDD	-0.3 to 4.6	V
Voltage on VDDQ Supply Relative to Vss	VDDQ	VDD	V
Voltage on Input Pin Relative to Vss	Vin	-0.3 to 6.0	V
Voltage on I/O Pin Relative to Vss	Vio	-0.3 to VDDQ + 0.5	V
Power Dissipation	PD	1.2	W
Storage Temperature	Тѕтс	-65 to 150	°C
Operating Temperature	Topr	0 to 70	°C
Storage Temperature Range Under Bias	TBIAS	-10 to 85	°C

*NOTE: Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS at 3.3V I/O(0°C ≤ TA ≤ 70°C)

Parameter	Symbol	Min		Max	Unit
Supply Voltage	VDD	3.13	3.3	3.6	V
Supply Voltage	VDDQ	3.13	3.3	3.6	٧
Ground	Vss	0	0	0	V

OPERATING CONDITIONS at 2.5V I/O(0 $^{\circ}$ C $^{\circ}$ TA $^{\circ}$ 70 $^{\circ}$)

Parameter	Symbol	Min	Тур.	Max	Unit
Supply Voltage	VDD	3.13	3.3	3.47	V
	VDDQ	2.37	2.5	2.9	V
Ground	Vss	0	0	0	V



CAPACITANCE*(TA = 25°C, f = 1MHz)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	CIN	VIN=0V	-	5	pF
Output Capacitance	Соит	Vout=0V	-	7	pF

^{*}NOTE: Sampled not 100% tested.

DC ELECTRICAL CHARACTERISTICS

 $(VDD=3.3V-5\%/+10\%, VDDQ=3.3V-5\%/+10\%, or\ VDD=3.3V\pm5\%, VDDQ=2.5V+0.4V/-0.13V,\ TA=0\ ^{\circ}\ to\ 70\ ^{\circ})$

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current(except ZZ)	lıL	VDD = Vss to VDD, VIN = Vss to VDD		-2	+2	μA
Output Leakage Current	loL	Output Disabled, Vout = Vss to VDDQ	-2	+2	μA	
Operating Current	lcc	Device Selected, IOUT = 0mA,	-13	-	250	mA
		ZZ≤ViL, All Inputs = ViL or ViH	-15	-	220	
		Cycle Time ≥ tCYC min				
Standby Current	ISB	Device deselected, IOUT = 0mA, ZZ \le f = Max, All Inputs \le 0.2V or \ge VDD-0.			60	mA
	ISB1	Device deselected, Iouт = 0mA, ZZ≤0.2V, f = 0,		-	10	mA
		All Inputs = fixed (VDD-0.2V or 0.2V)	L-Ver.	-	2.0	mA
		Device deselected, lout = 0mA,		_	10	mA
	ISB2	ZZ≥VDD-0.2V, f = Max, All Inputs≤VIL or ≥VIH	L-Ver.	-	1.0	mA
Output Low Voltage(3.3V I/O)	Vol	IoL = 8.0mA		-	0.4	٧
Output High Voltage(3.3V I/O)	Voн	IOH = -4.0mA		2.4	-	٧
Output Low Voltage(2.5V I/O)	Vol	IoL = 1mA		-	0.2	٧
Output High Voltage(2.5V I/O)	Voн	Iон = -1mA		2.0	-	٧
input Low Voltage(3.3V I/O)	VIL			-0.5*	0.8	٧
Input High Voltage(3.3V I/O)	ViH			2.0	5.5**	٧
Input Low Voltage(2.5V I/O)	VIL			-0.3*	0.7	V
Input High Voltage(2.5V I/O)	VIH			1.7	5.5**	٧

^{*} VIL(min) = -3.0(Pulse Width≤20ns)



^{**} In Case of I/O Pins, the Max. VIH = VDDQ + 0.5V

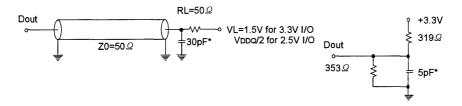
TEST CONDITIONS

(TA = 0 °C to 70 °C, VDD=3.3V-5%/+10%, VDDQ=3.3V-5%/+10%, or VDD=3.3V±5%, VDDQ=2.5V +0.4V/-0.13V)

Parameter	Value
Input Pulse Level (for 3.3V I/O)	0 to 3V
Input Pulse Level (for 2.5V I/O)	0 to 2.5V
Input Rise and Fall Time(Measured at 0.3V and 2.7V for 3.3V I/O)	2ns
Input Rise and Fall Time(Measured at 0.3V and 2.1V for 2.5V I/O)	2ns
Input and Output Timing Reference Levels(for 3.3V I/O)	1.5V
Input and Output Timing Reference Levels(for 2.5V I/O)	VDDQ/2
Output Load	See Fig. 1

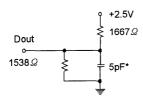
Output Load(A)

Output Load(B), (3.3V I/O) (for tLZC, tLZOE, tHZOE & tHZC)



^{*} Capacitive Load consists of all components of the test environment.

Output Load(C), (2.5V I/O) (for tLZC, tLZOE, tHZOE & tHZC)



* Including Scope and Jig Capacitance

Fig. 1

^{*} Including Scope and Jig Capacitance

AC TIMING CHARACTERISTICS

(TA = 0 °C to 70 °C, VDD=3.3V-5%/+10%, VDDQ=3.3V-5%/+10%, or VDD=3.3V \pm 5%, VDDQ=2.5V +0.4V/-0.13V, unless otherwise specified)

Parameter	Symbol	KM732V696-13		KM732V696-15		11-34
raidilielei		Min	Max	Min	Max	Unit
Cycle Time	tCYC	13	-	15	-	ns
Clock Access Time	tCD	-	7	-	8	ns
Output Enable to Data Valid	tOE	-	6	-	7	ns
Clock High to Output Low-Z	tLZC	. 0	-	0	-	ns
Output Hold from Clock High	tOH	2.0	-	2.0	-	ns
Output Enable Low to Output Low-Z	tLZOE	0	-	0	-	ns
Output Enable High to Output High-Z	tHZOE	-	4.0	-	4.0	ns
Clock High to Output High-Z	tHZC	1.5	5.0	1.5	5.0	ns
Clock High Pulse Width	tCH	4.5	-	5.5	-	ns
Clock Low Pulse Width	tCL	4.5	-	5.5	-	ns
Address Setup to Clock High	tAS	2.5	-	2.5	-	ns
Address Status Setup to Clock High	tSS	2.5	-	2.5	-	ns
Data Setup to Clock High	tDS	2.5	-	2.5	-	ns
Write Setup to Clock High(GW , BW , WE x)	tWS	2.5	-	2.5	-	ns
Address Advance Setup to Clock High	tADVS	2.5	-	2.5	-	ns
Chip Select Setup to Clock High	tCSS	2.5	-	2.5	-	ns
Address Hold from Clock High	tAH	0.5	-	0.5	-	ns
Address Status Hold from Clock High	tSH	0.5	•	0.5	-	ns
Data Hold from Clock High	tDH	0.5	-	0.5	-	ns
Write Hold from Clock High(GW, BW, WEx)	tWH	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	tADVH	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	tCSH	0.5	-	0.5	-	ns
ZZ High to Power Down	tPDS	2	-	2	-	cycle
ZZ Low to Power Up	tPUS	2	-	2	-	cycle

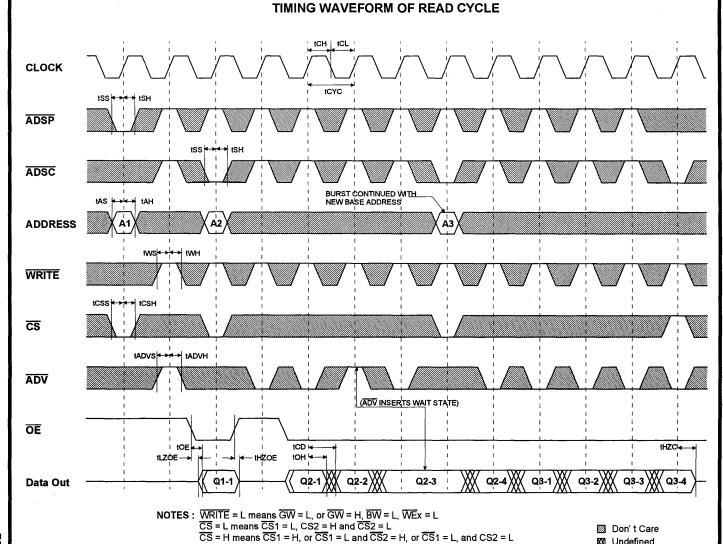
NOTE: 1. All address inputs must meet the specified setup and hold times for all rising clock edges whenever ADSC and/or ADSP is sampled low and CS is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.

2. Both chip selects must be active whenever ADSC or ADSP is sampled low in order for the this device to remain enabled.

3. ADSC or ADSP must not be asserted for at least 2 Clock after leaving ZZ state.



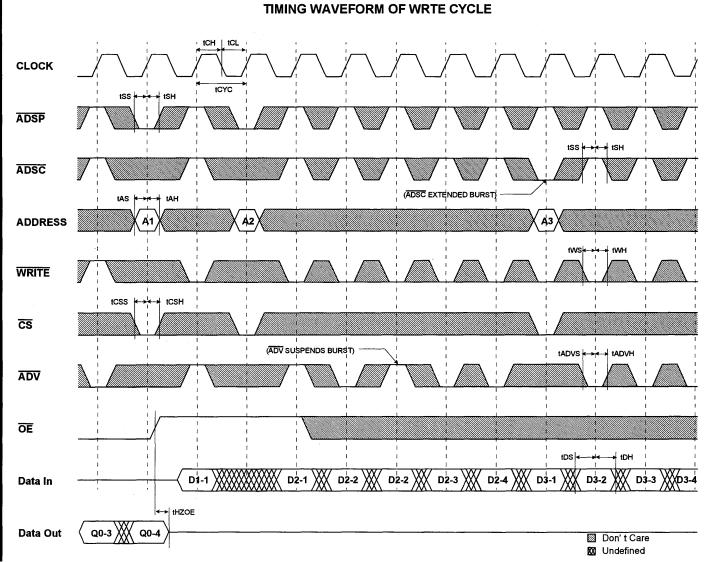
SUMSANG ELECTRONICS



Don't Care

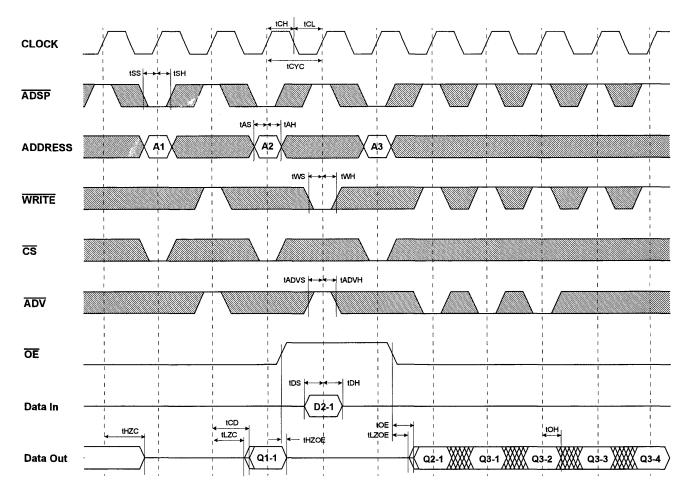
Undefined





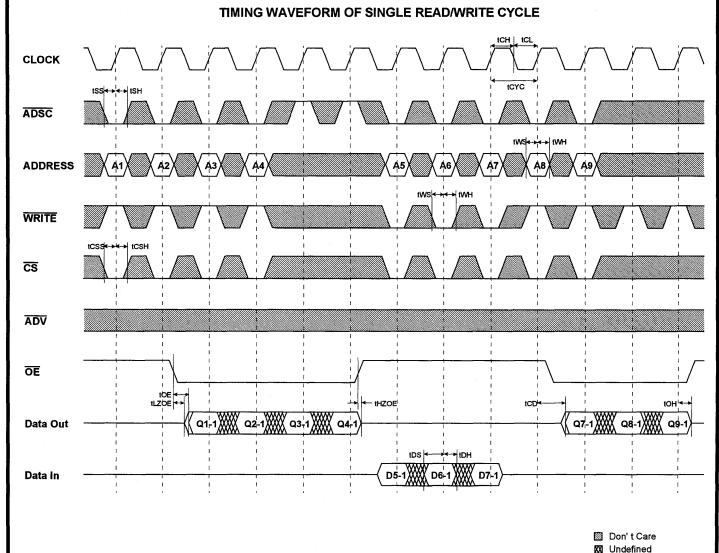
SAMSUNG ELECTRONICS

TIMING WAVEFORM OF COMBINATION READ/WRTE CYCLE



Don't Care

□ Undefined



tPUS

ZZ Recovery Cycle

D2-1 D2-2 D2-2

Don't Care

☑ Undefined

Data In

Data Out

ZZ

tOE ←

ZZ Setup Cycle

Sleep State

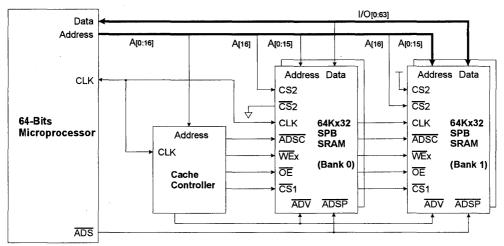
H tHZOE

Normal Operation Mode

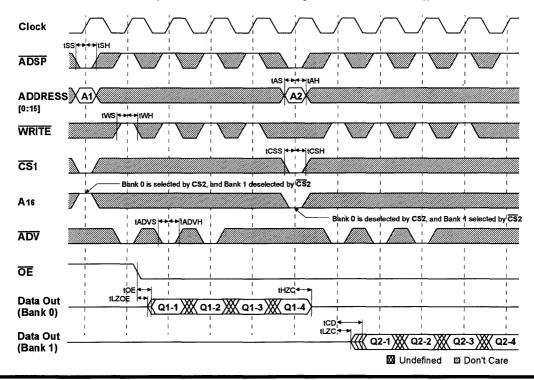
APPLICATION INFORMATION

DEPTH EXPANSION

The Samsung 64Kx32 Synchronous Pipelined Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 64K depth to 128K depth without extra logic.



INTERLEAVE READ TIMING (Refer non-interleave write timing for interleave write timing)





128Kx18-Bit Synchronous Pipelined Burst SRAM

FEATURES

- Synchronous Operation.
- · 2 Stage Pipelined Operation With 4 Burst
- · On-Chip Address Counter.
- Self-Timed Write Cycle.
- On-Chip Address and Control Registers.
- VDD = 3.3V-5%/+10% Power Supply.
- 5V Tolerant Inputs except I/O Pins.
- Byte Writable Function.
- Global Write Enable Controls a full bus-width write.
- Power Down State via ZZ Signal.
- LBO Pin allows a choice of either a interleaved burst or a
- . Three Chip Enables for simple depth expansion with No Data Contention; 2 cycle Enable, 1 cycle Disable.
- · Asynchronous Output Enable Control.
- ADSP, ADSC, ADV Burst Control Pins.
- · TTL-Level Three-State Output.
- . 100-Pin TQFP Package

FAST ACCESS TIMES

Parameter	Symbol	-7	-8	-10	-11	Unit
Cycle Time	tCYC	7.5	8.6	10	11	ns
Clock Access Time	tCD	4.5	5.0	5.0	6.0	ns
Output Enable Access Time	tOE	4.5	5.0	5.0	6.0	ns

GENERAL DESCRIPTION

The KM718V789/L is a 2,359,296 bits Synchronous Static Random Access Memory designed for high performance second level cache of pentium and Power PC based system.

It is organized as 128K words of 18 bits. And it integrates address and control registers, a 2-bit burst address counter and added some new functions for high performance cache RAM applications; GW, BW, LBO, ZZ.

Write cycles are internally self-timed and synchronous.

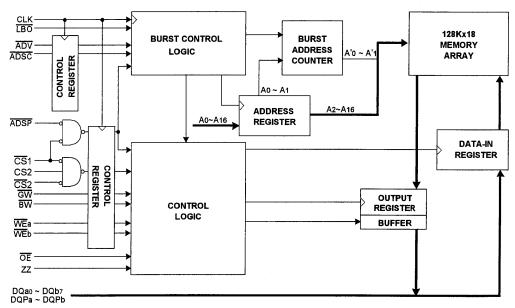
Full bus-width write is done by GW, and each byte write is performed by the combination of WEx and BW when GW is high. And with CS1 high, ADSP disable to support address pipelining. Burst cycle can be initiated with either the address status processor(ADSP) or address status cache controller(ADSC) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance(ADV) input.

LBO pin is DC operated and determines burst sequence (linear or interleaved).

ZZ pin controls Power Down State and reduces Stand-by current regardless of CLK.

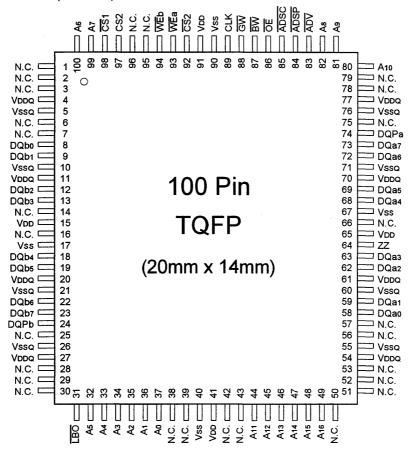
The KM718V789/L is fabricated using SAMSUNG's high performance CMOS technology and is available in a 100pin TQFP. Multiple power and ground pins are utilized to minimize ground bounce

LOGIC BLOCK DIAGRAM





PIN CONFIGURATION (TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A16	Address Inputs	32,33,34,35,36,37,	VDD	Power Supply(+3.3V)	15,41,65,91
		44,45,46,47,48,49,	Vss	Ground	17,40,67,90
		80,81,82,99,100	N.C.	No Connect	1,2,3,6,7,14,16,25,28,29
ADV	Burst Address Advance	83			,30,38,39,42,43,50,
ADSP	Address Status Processor	84			51,52,53,56,57,66,75,
ADSC	Address Status Controller	85	1		78,79,95,96
CLK	Clock	89	DQa0 ~ a7	Data Inputs/Outputs	58,59,62,63,68,69,72,73
CS1	Chip Select	98	DQb0 ~ b7		8,9,12,13,18,19,22,23
CS2	Chip Select	97	DQPa, Pb		74,24
CS2	Chip Select	92	VDDQ	Output Power Supply	4,11,20,27,54,61,70,77
WEx	Byte Write Inputs	93,94		(+3.3V)	
ŌĒ	Output Enable	86	Vssq	Output Ground	5,10,21,26,55,60,71,76
Ġ₩	Global Write Enable	88			
BW	Byte Write Enable	87			
ZZ	Power Down Input	64	1		
LBO	Burst Mode Control	31	ł		

FUNCTION DESCRIPTION

The KM718V789 is a synchronous SRAM designed to support the burst address accessing sequence of the Pentium and Power PC based microprocessor. All inputs(with the exception of \overline{OE} , \overline{LBO} and ZZ) are sampled on rising clock edges. The start and duration of the burst access is controlled by \overline{ADSP} , \overline{ADSC} , \overline{ADV} and Chip Select pins.

The accesses are enabled with the chip select signals and output enabled signals. Wait states are inserted into the access with ADV.

When ZZ is pulled high, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM normally operates after 2 cycles of wake up time. ZZ pin is pulled down internally.

Read cycles are initiated with $\overline{\text{ADSP}}$ (regardless of $\overline{\text{WE}}x$ and $\overline{\text{ADSC}}$) using the new external address clocked into the on-chip address register whenever $\overline{\text{ADSP}}$ is sampled low, the chip selects are sampled active, and the output buffer is enabled with $\overline{\text{OE}}$. In read operation the data of cell array accessed by the current address, registered in the Data-out registers by the positive edge of CLK, are carried to the Data-out buffer by the next positive edge of CLK. The data, registered in the Data-out buffer, are projected to the output pins. $\overline{\text{ADV}}$ is ignored on the clock edge that samples $\overline{\text{ADSP}}$ asserted, but is sampled on the subsequent clock edges. The address increases internally for the next access of the burst when $\overline{\text{WE}}x$ are sampled High and $\overline{\text{ADV}}$ is sampled Low. And $\overline{\text{ADSP}}$ is blocked to control signals by disabling $\overline{\text{CS}}1$.

All byte write is done by \overline{GW} (regardless of \overline{BW} and $\overline{WE}x$.), and each byte write is performed by the combination of \overline{BW} and $\overline{WE}x$ when \overline{GW} is High.

Write cycles are performed by disabling the output buffers with \overline{OE} and asserting \overline{WEx} . \overline{WEx} are ignored on the clock edge that samples \overline{ADSP} Low, but are sampled on the subsequent clock edges. The output buffers are disabled when \overline{WEx} are sampled Low(regaedless of \overline{OE}). Data is clocked into the data input register when \overline{WEx} sampled Low. The address increases internally to the next address of burst, if both \overline{WEx} and \overline{ADV} are sampled Low. Individual byte write cycles are performed by any one or more byte write enable signals(\overline{WEx} or \overline{WEx}) sampled low. The \overline{WEx} controls DQao ~ DQa7 and DQPa, \overline{WEx} controls DQbo ~ DQb7 and DQPb. Read or write cycle may also be initiated with \overline{ADSC} , instead of \overline{ADSP} . The differences between cycles initiated with \overline{ADSC} and \overline{ADSP} as are follows:

ADSP must be sampled high when ADSC is sampled low to initiate a cycle with ADSC. WEx are sampled on the same clock edge that sampled ADSC low(and ADSP high).

Addresses are generated for the burst access as shown below, The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the LBO pin. When this pin is Low, linear burst sequence is selected. And when this pin is High, Interleaved burst sequence is selected.

BURST SEQUENCE TABLE

(Interleaved Burst)

LBO PIN HIGH	Case 1		Case 2		Case 3		Case 4	
LBOTTIN THOS	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
	0	1	0	0	1	1	1	0
	1	0	1	1 1	0	0	0	1
Fourth Address	1	1	1	0	0	1	0	0

(Linear Burst)

LBO PIN LOW	Case 1		Case 2		Case 3		Case 4	
LEGO FIN	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
	0	1	1	0	1	1	0	0
	1	0	1	1	0	0	0	1
Fourth Address	1	1	0	0	0	1	1	0

NOTE: 1. LBO pin must be tied to High or Low, and Floating State must not be allowed.



TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

CS1	CS2	CS2	ADSP	ADSC	ADV	WRITE	CLK	Address Accessed	Operation
Н	Х	Х	Х	L	Χ	Х	1	N/A	Not Selected
L	L	X	L	Х	Χ	Х	1	N/A	Not Selected
L	Х	Н	L	Х	Х	Х	1	N/A	Not Selected
L	L	Х	Х	L	Х	Х	<u> </u>	N/A	Not Selected
L	Х	Н	Х	L	Χ	Х	1	N/A	Not Selected
L	Н	L	L	Х	Χ	Х	1	External Address	Begin Burst Read Cycle
L	Н	L	Н	L	Χ	L	1	External Address	Begin Burst Write Cycle
L	Н	L	Н	Г	Χ	Н	1	External Address	Begin Burst Read Cycle
Х	Х	Х	Н	H	L	Н	1	Next Address	Continue Burst Read Cycle
Н	Х	Х	Х	Н	L	Н	1	Next Address	Continue Burst Read Cycle
Х	Х	Х	Н	Н	L	L	1	Next Address	Continue Burst Write Cycle
Н	Х	Х	Х	H	L	L	1	Next Address	Continue Burst Write Cycle
Х	Х	Х	Н	Н	Н	Н	1	Current Address	Suspend Burst Read Cycle
Н	Х	Х	Х	Н	Н	Н	1	Current Address	Suspend Burst Read Cycle
X	Х	Х	Н	Н	Н	L	1	Current Address	Suspend Burst Write Cycle
Н	Х	Χ	Х	Н	Н	L	1	Current Address	Suspend Burst Write Cycle

NOTE: 1. X means "Don't Care".

- 2. The rising edge of clock is symbolized by 1.
- 3. WRITE = L means Write operation in WRITE TRUTH TABLE.
 WRITE = H means Read operation in WRITE TRUTH TABLE.
- 4. Operation finally depends on status of asynchronous input pins(ZZ and \overline{OE}).

WRITE TRUTH TABLE

GW	BW	WEa	WEb	Operation
Н	Н	Х	Х	READ
Н	L	Н	Н	READ
Н	L	L	н	WRITE BYTE a
Н	L	Н	L	WRITE BYTE b
Н	L	L	L	WRITE ALL BYTEs
L	X	Х	Х	WRITE ALL BYTEs

NOTE: 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(\uparrow).

ASYNCHRONOUS TRUTH TABLE

(See Notes 1 and 2):

Operation	ZZ	ŌĒ	I/O Status
Sleep Mode	Н	X	High-Z
Read	L	L	DQ
Read	L	Н	High-Z
Write	L	Х	Din, High-Z
Deselected	L	Х	High-Z

NOTE

- 1. X means "Don't Care".
- 2. ZZ pin is pulled down internally
- For write cycles that following read cycles, the output buffers must be disabled with OE, otherwise data bus contention will occur.
- 4. Sleep Mode means power down state of which stand-by current does not depend on cycle time.
- Deselected means power down state of which stand-by current depends on cycle time.



PASS-THROUGH TRUTH TABLE

Previous Cycle		Present Cycle				New Courts	
Operation WRITE		Operation CS1 V		WRITE	ŌĒ	Next Cycle	
Write Cycle, All bytes Address=An-1, Data=Dn-1		Initiate Read Cycle Address=An Data=Qn-1 for all bytes	L	Н	L	Read Cycle Data=Qn	
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=Qn-1 for all bytes		Н	L	No carryover from previous cycle	
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=High-Z	Н	Н	Н	No carryover from previous cycle	
Write Cycle, One byte Address=An-1, Data=Dn-1 One L		Initiate Read Cycle Address=An Data=Qn-1 for one byte	L	Н	L	Read Cycle Data=Qn	
Write Cycle, One byte Address=An-1, Data=Dn-1 One L.		No new cycle Data=Qn-1 for one byte	Н	Н	L	No carryover from previous cycle	

NOTE: 1. This operation makes written data immediately available at output during a read cycle preceded by a write cycle.

2. WEx means WEa ~ WEd.

ABSOLUTE MAXIMUM RATING*

Parameter	Symbol	Rating	Unit
Voltage on VDD Supply Relative to Vss	VDD	-0.3 to 4.6	V
Voltage on VDDQ Supply Relative to Vss	VDDQ	VDD	٧
Voltage on Input Pin Relative to Vss	VIN	-0.3 to 6.0	V
Voltage on I/O Pin Relative to Vss	Vio	-0.3 to VDDQ + 0.5	٧
Power Dissipation	PD	1.2	W
Storage Temperature	Тѕтс	-65 to 150	°C
Operating Temperature	Topr	0 to 70	°C
Storage Temperature Range Under Bias	TBIAS	-10 to 85	°C

*NOTE: Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS(0 $^{\circ}$ C $^{\leq}$ TA $^{\leq}$ 70 $^{\circ}$ C)

Parameter	Symbol	Min	Тур.	Max	Unit
Supply Voltage	VDD	3.13	3.3	3.6	· V
Supply Voltage	VDDQ	3.13	3.3	3.6	V
Ground	Vss	0	0	0	V

CAPACITANCE*(TA = 25°C, f = 1MHz)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	Cin	VIN=0V	-	5	pF
Output Capacitance	Соит	Vout=0V	-	7	pF

*NOTE: Sampled not 100% tested.



DC ELECTRICAL CHARACTERISTICS(TA = 0°C to 70°C, VDD = 3.3V±5%)

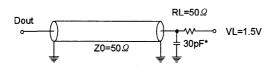
Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current(except ZZ)	lıL	VDD = Vss to VDD ; VIN = Vss to VDD		-2	+2	μA
Output Leakage Current	loL	Output Disabled, Vour=Vss to VDDQ		-2	+2	μA
Operating Current	Icc	Device Selected Java - On A	-7	-	395	
·	,	Device Selected, lout = 0mA, ZZ≤ViL, All Inputs = ViL or ViH	-8	-	360	1
		Cycle Time ≥ tCYC min	-10	-	320	mA .
		Sydic Time = 1010 min	-11	-	320	}
Standby Current			-7	-	100	
	IsB	Device deselected, lout = 0mA,	-8	-	90	mA
		$ZZ \le VIL$, $f = Max$, All Inputs $\le 0.2V$ or $\ge VDD-0.2V$	-10	-	80	
		All Imputs = 0.24 of = 400-0.24	-11	-	80	
	ISB1	Device deselected, lout = 0mA, ZZ≤0.2V, f = 0,		-	10	mA
	1561	All Inputs=fixed (VDD-0.2V or 0.2V)	L-Ver	-	5.0	mA
	IsB2	Device deselected, louт = 0mA, ZZ≥Vpp-0.2V, f = Max.		-	10	mA
	1362	All Inputs ≤ VIL or ≥ VIH	L-Ver	-	1.0	mA
Output Low Voltage	Vol	IoL = 8.0mA		-	0.4	V
Output High Voltage	Voн	Iон = -4.0mA		2.4	-	V
Input Low Voltage	VIL			-0.5*	0.8	V
Input High Voltage	ViH			2.0	5.5**	V

^{*} VIL(min) = -3.0(Pulse Width≤20ns)

TEST CONDITIONS (TA = 0°C to 70°C, VDD = 3.3V-5%/+10%, unless otherwise specified)

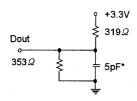
Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time(Measured at 0.3V and 2.7V)	2ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1

Output Load(A)



^{*} Capacitive Load consists of all components of the test environment.

Output Load(B) (for tLZC, tLZOE, tHZOE& tHZC)



^{*} Including Scope and Jig Capacitance

Fig. 1



^{**} In Case of I/O Pins, the Max. VIH = VDDQ + 0.5V

AC TIMING CHARACTERISTICS

(VDD=3.3V-5%/+10%, TA = 0° to 70°)

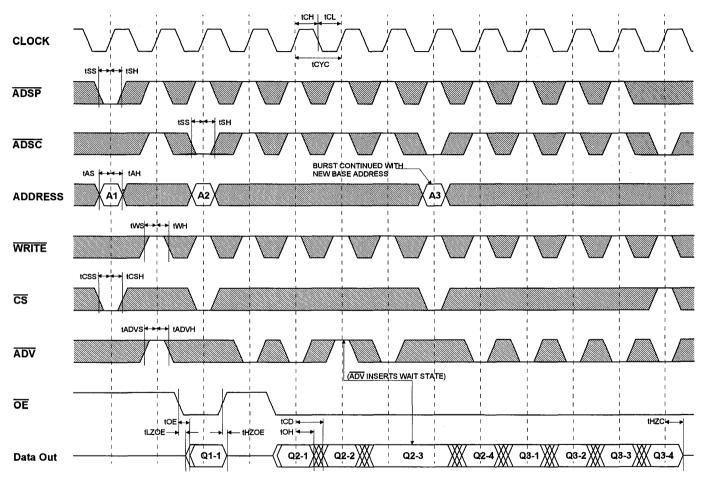
Parameter	Symbol		7	-8		-	10	-11		Unit
Farameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Cycle Time	tCYC	7.5	-	8.6	-	10	-	11	-	ns
Clock Access Time	tCD	-	4.5	-	5.0	-	5.0	-	6.0	ns
Output Enable to Data Valid	tOE	-	4.5	-	5.0	-	5.0	-	6.0	ns
Clock High to Output Low-Z	tLZC	0	-	0	-	0		0		ns
Output Hold from Clock High	tOH	1.5	-	1.5	-	1.5	-	1.5	-	ns
Output Enable Low to Output Low-Z	tLZOE	0	-	0	-	0	-	0	-	ns
Output Enable High to Output High-Z	tHZOE	-	4.0	-	4.0	-	4.0	-	4.0	ns
Clock High to Output High-Z	tHZC	1.5	5.0	1.5	5.0	1.5	5.0	1.5	5.0	ns
Clock High Pulse Width	tCH	3.0	-	3.5	-	4.0	-	4.0	-	ns
Clock Low Pulse Width	tCL	3.0	-	3.5	-	4.0	-	4.0	-	ns
Address Setup to Clock High	tAS	2.0	-	2.0	-	2.0	-	2.0	-	ns
Address Status Setup to Clock High	tSS	2.0	-	2.0	-	2.0	-	2.0	-	ns
Data Setup to Clock High	tDS	2.0	-	2.0	-	2.5	-	2.5	-	ns
Write Setup to Clock High (GW, BW, WEx)	tWS	2.0	-	2.0	-	2.0	-	2.0		ns
Address Advance Setup to Clock High	tADVS	2.0	-	2.0	-	2.0	-	2.0	-	ns
Chip Select Setup to Clock High	tCSS	2.0	-	2.0	-	2.0	-	2.0	-	ns
Address Hold from Clock High	tAH	0.5	-	0.5	-	0.5		0.5	-	ns
Address Status Hold from Clock High	tSH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Data Hold from Clock High	tDH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Write Hold from Clock High (GW, BW, WEx)	tWH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	tADVH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	tCSH	0.5	-	0.5	-	0.5	-	0.5	-	ns
ZZ High to Power Down	tPDS	2	-	2	-	2	-	2	-	cycl
ZZ Low to Power Up	tPUS	2	-	2	-	2	-	2	-	cycl

NOTE: 1. All address inputs must meet the specified setup and hold times for all rising clock edges whenever ADSC and/or ADSP is sampled low and CS is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.

2. Both chip selects must be active whenever ADSC or ADSP is sampled low in order for the this device to remain enabled.

3. ADSC or ADSP must not be asserted for at least 2 Clock after leaving ZZ state.

TIMING WAVEFORM OF READ CYCLE



NOTES: WRITE = L means \overline{GW} = L, or \overline{GW} = H, \overline{BW} = L, \overline{WE} x = L

 \overline{CS} = L means \overline{CS} 1 = L, CS2 = H and \overline{CS} 2 = L \overline{CS} = H means \overline{CS} 1 = H, or \overline{CS} 1 = L and \overline{CS} 2 = H, or \overline{CS} 1 = L, and \overline{CS} 2 = L

□ Don't Care
 □ Undefined

KM718V789/L

ŌĒ

Data In

Data Out

+→ tHZOE

Q0-3 XX Q0-4

tDS -

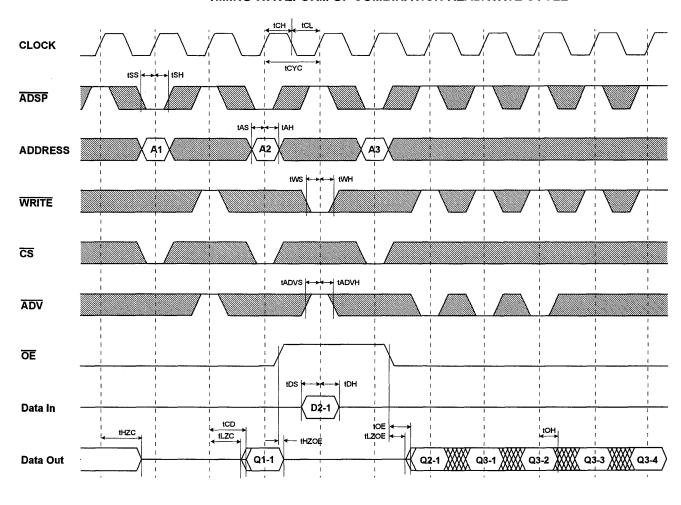
D3-2

→ tDH

Don't Care

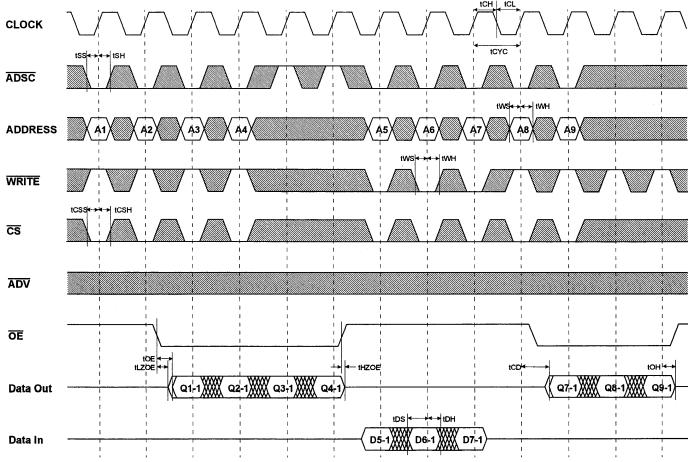
☑ Undefined

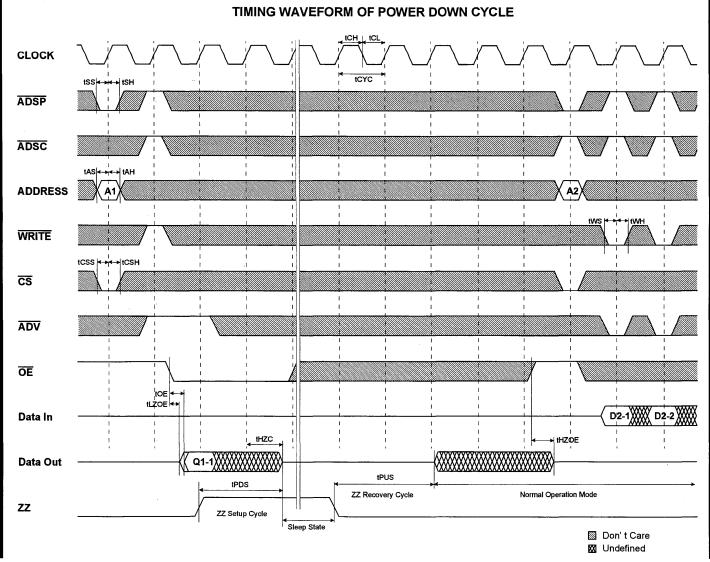
TIMING WAVEFORM OF COMBINATION READ/WRTE CYCLE





TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE

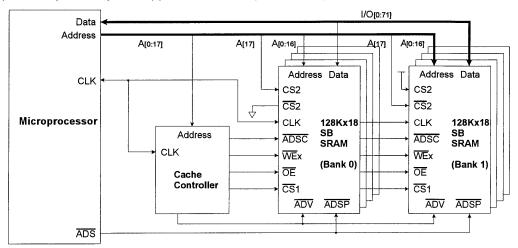




APPLICATION INFORMATION

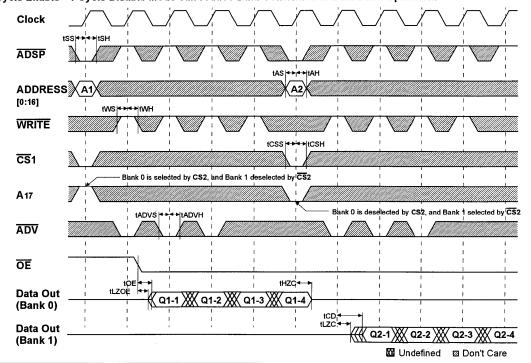
DEPTH EXPANSION

The Samsung 128Kx18 Synchronous Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 128K depth to 256K depth without extra logic.



INTERLEAVE READ TIMING (Refer to non-interleave write timing for interleave write timing)

2 Cycle Enable - 1 Cycle Disable Mode can reduce Data Contention in Dual Bank Operation.



64Kx36-Bit Synchronous Pipelined Burst SRAM **FEATURES**

· Synchronous Operation.

- . 2 Stage Pipelined operation with 4 Burst.
- On-Chip Address Counter.
- Self-Timed Write Cycle.
- On-Chip Address and Control Registers.
- VDD= 3.3V-5%/+10% Power Supple
- 5V Tolerant Inputs Except I/O Pins.
- Byte Writable Function.
- Global Write Enable Controls a full bus-width write.
- Power Down State via ZZ Signal.
- LBO Pin allows a choice of either a interleaved burst or a
- . Three Chip Enables for simple depth expansion with No Data Contention; 2 cycle Enable, 1 cycle Disable.
- Asynchronous Output Enable Control.
 ADSP, ADSC, ADV Burst Control Pins.
- TTL-Level Three-State Output.
- . 100-Pin TQFP Package

FAST ACCESS TIMES

Parameter	Symbol	-7	-8	-10	-11	Unit
Cycle Time	tCYC	7.5	8.6	10	11	ns
Clock Access Time	tCD	4.5	5.0	5.0	6.0	ns
Output Enable Access Time	tOE	4.5	5.0	5.0	6.0	ns

GENERAL DESCRIPTION

The KM736V689/L is a 2,359,296-bit Synchronous Static Random Access Memory designed for high performance second level cache of Pentium and Power PC based System.

It is organized as 64K words of 36bits and integrates address and control registers, a 2-bit burst address counter and added some new functions for high performance cache RAM applications; GW, BW, LBO, ZZ. Write cycles are internally self-timed and synchronous.

Full bus-width write is done by GW, and each byte write is performed by the combination of WEx and BW when GW is high. And with CS1 high, ADSP is blocked to control signals.

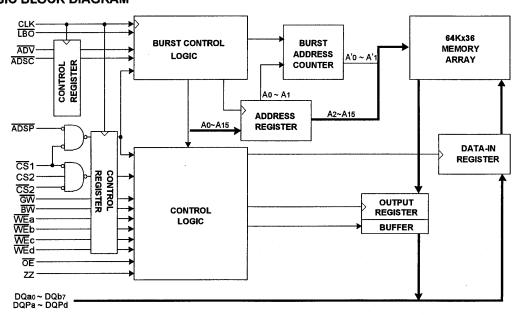
Burst cycle can be initiated with either the address status processor(ADSP) or address status cache controller(ADSC) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance(ADV) input.

LBO pin is DC operated and determines burst sequence(linear or interleaved).

ZZ pin controls Power Down State and reduces Stand-by current regardless of CLK.

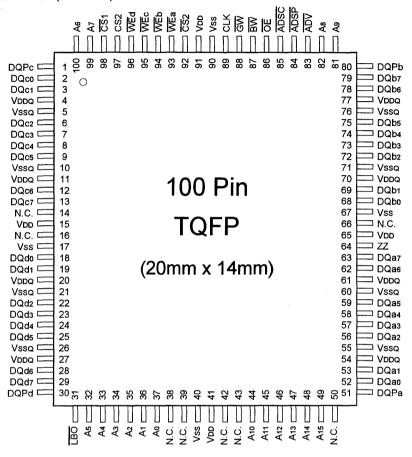
The KM736V689/L is fabricated using SAMSUNG's high performance CMOS technology and is available in a 100pin TQFP package. Multiple power and ground pins are utilized to minimize ground bounce.

LOGIC BLOCK DIAGRAM





PIN CONFIGURATION (TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A15	Address Inputs	32,33,34,35,36,37,	VDD	Power Supply(+3.3V)	15,41,65,91
	-	44,45,46,47,48,49,	Vss	Ground	17,40,67,90
		81,82,99,100	N.C.	No Connect	14,16,38,39,42,43,50,66
ĀDV	Burst Address Advance	83	1		
ADSP	Address Status Processor	84	DQa0 ~ a7	Data Inputs/Outputs	52,53,56,57,58,59,62,63
ADSC	Address Status Controller	85	DQb0 ~ b7		68,69,72,73,74,75,78,79
CLK	Clock	89	DQc0 ~ c7		2,3,6,7,8,9,12,13
CS1	Chip Select	98	DQdo ~ d7	i	18,19,22,23,24,25,28,29
CS2	Chip Select	97	DQPa~Pd	<u> </u>	51,70,1,20
CS2	Chip Select	92	VDDQ	Output Power Supply	4,11,20,27,54,61,70,77
WEx	Byte Write Inputs	93,94,95,96	1	(+3.3V)	
ŌĒ	Output Enable	86	VssQ	Output Ground	5,10,21,26,55,60,71,76
Ġ₩	Global Write Enable	88			
BW	Byte Write Enable	87			
ZZ	Power Down Input	64	1		
<u>LBO</u>	Burst Mode Control	31	1		

FUNCTION DESCRIPTION

The KM736V689/L is a synchronous SRAM designed to support the burst address accessing sequence of the P6 and Power PC based microprocessor. All inputs (with the exception of \overline{OE} , \overline{LBO} and ZZ) are sampled on rising clock edges. The start and duration of the burst access is controlled by \overline{ADSC} , \overline{ADSP} and \overline{ADV} and chip select pins.

The accesses are enabled with the chip select signals and output enabled signals. Wait states are inserted into the access with ADV.

When ZZ is pulled high, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM normally operates after 2 cycles of wake up time. ZZ pin is pulled down internally.

Read cycles are initiated with $\overline{\text{ADSP}}$ (regardless of $\overline{\text{WEx}}$ and $\overline{\text{ADSC}}$) using the new external address clocked into the on-chip address register whenever $\overline{\text{ADSP}}$ is sampled low, the chip selects are sampled active, and the output buffer is enabled with $\overline{\text{OE}}$. In read operation the data of cell array accessed by the current address, registered in the Data-out registers by the positive edge of CLK, are carried to the Data-out buffer by the next positive edge of CLK. The data, registered in the Data-out buffer, are projected to the output pins. $\overline{\text{ADV}}$ is ignored on the clock edge that samples $\overline{\text{ADSP}}$ asserted, but is sampled on the subsequent clock edges. The address increases internally for the next access of the burst when $\overline{\text{WEx}}$ are sampled High and $\overline{\text{ADV}}$ is sampled low. And $\overline{\text{ADSP}}$ is blocked to control signals by disabling $\overline{\text{CS}}1$.

All byte write is done by \overline{GW} (regaedless of \overline{BW} and $\overline{WE}x$.), and each byte write is performed by the combination of \overline{BW} and $\overline{WE}x$ when \overline{GW} is high.

Write cycles are performed by disabling the output buffers with \overline{OE} and asserting \overline{WEx} . \overline{WEx} are ignored on the clock edge that samples \overline{ADSP} low, but are sampled on the subsequent clock edges. The output buffers are disabled when \overline{WEx} are sampled Low(regaedless of \overline{OE}). Data is clocked into the data input register when \overline{WEx} sampled Low. The address increases internally to the next address of burst, if both \overline{WEx} and \overline{ADV} are sampled Low. Individual byte write cycles are performed by any one or more byte write enable signals(\overline{WEa} , \overline{WEb} , \overline{WEc} or \overline{WEd}) sampled low. The \overline{WE} control DQao ~ DQar and DQPa, \overline{WEb} controls DQbo ~ DQbr and DQPb, \overline{WEc} controls DQco ~ DQcr and DQPc, and \overline{WEd} control DQdo ~ DQdr and DQPd. Read or write cycle may also be initiated with \overline{ADSC} , instead of \overline{ADSP} . The differences between cycles initiated with \overline{ADSC} and \overline{ADSP} as are follows;

ADSP must be sampled high when ADSC is sampled low to initiate a cycle with ADSC.

WEx are sampled on the same clock edge that sampled ADSC low(and ADSP high).

Addresses are generated for the burst access as shown below, The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the LBO pin. When this pin is Low, linear burst sequence is selected. When this pin is High, Interleaved burst sequence is selected.

BURST SEQUENCE TABLE

(Interleaved Burst)

LBO PIN HIGH	Case 1		Case 2		Case 3		Case 4	
LDO FIN	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
	0	1	0	0	1	1	1	0
	1	0	1	1	0	0	0	1
Fourth Address	1	_1	1	0	0	11	0	0

(Linear Burst)

LBO PIN LOW	Cas	se 1	Case 2 Case 3				Cas	Case 4	
LEG FIN	A1	A0	A1	A0	A1	A0	A1	A0	
First Address	0	0	0	1	1	0	1	1	
	0	1	1	0	1	1	l o	0	
	1	0	1	1	0	0	0	1 1	
Fourth Address	1	1	0	0	0	1	1	0	

NOTE: 1. LBO pin must be tied to High or Low, and Floating State must not be allowed.



TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

CS1	CS2	CS2	ADSP	ADSC	ADV	WRIT	CLK	Address Accessed	Operation
Н	X	Х	X	L	X	Х	↑	N/A	Not Selected
L	L	Х	L	Х	X	Х	1	N/A	Not Selected
L	Х	Н	L	Х	Х	X	1	N/A	Not Selected
L	L	Х	Х	L	X	Х	1	N/A	Not Selected
L	Х	Н	Х	L	Х	Х	1	N/A	Not Selected
L	Н	L	L_	Х	X	Х	1	External Address	Begin Burst Read Cycle
L	Н	L	Н	L	X	L	1	External Address	Begin Burst Write Cycle
L	Н	L	Н	L	X	Н	1	External Address	Begin Burst Read Cycle
Χ	Х	Х	Н	H	L	Н	1	Next Address	Continue Burst Read Cycle
Н	Х	Х	Х	Н	L	Н	1	Next Address	Continue Burst Read Cycle
Х	Х	Х	Н	Н	L	L	1	Next Address	Continue Burst Write Cycle
Н	Х	Х	Х	H	L	L	1	Next Address	Continue Burst Write Cycle
X	Х	Х	Н	Н	Н	Н	1	Current Address	Suspend Burst Read Cycle
Н	Х	Х	Х	Н	Н	Н	1	Current Address	Suspend Burst Read Cycle
Х	Х	Х	Н	Н	Н	L	1	Current Address	Suspend Burst Write Cycle
Н	Х	Х	Х	Н	Н	L	1	Current Address	Suspend Burst Write Cycle

NOTE: 1. X means "Don't Care".

- 2. The rising edge of clock is symbolized by 1.
- WRITE = L means Write operation in WRITE TRUTH TABLE.
 WRITE = H means Read operation in WRITE TRUTH TABLE.
- 4. Operation finally depends on status of asynchronous input pins(ZZ and \overline{OE}).

WRITE TRUTH TABLE

GW	BW	WEa	WEb	WEc	WEd	Operation
Н	Н	Х	Х	Х	X	READ
Н	L	H	H	Н	Н	READ
Н	L	L	Н	Н	Н	WRITE BYTE a
Н	L	Н	L	Н	Н	WRITE BYTE b
Н	L	Н	Н	L	L	WRITE BYTE c and d
Н	L	L	L	L	L	WRITE ALL BYTEs
L	Х	Х	Х	X	X	WRITE ALL BYTEs

NOTE: 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(1).

ASYNCHRONOUS TRUTH TABLE

(See Notes 1 and 2):

Operation	ZZ	ŌĒ	I/O Status
Sleep Mode	Н	Х	High-Z
Read	L	L	DQ
r Read	L	Н	High-Z
Write	L	Х	Din, High-Z
Deselected	L	Х	High-Z

NOTE

- 1. X means "Don't Care".
- 2. ZZ pin is pulled down internally
- 3. For write cycles that following read cycles, the output buffers must be disabled with \overline{OE} , otherwise data bus contention will occur.
- 4. Sleep Mode means power down state of which stand-by current does not depend on cycle time.
- Deselected means power down state of which stand-by current depends on cycle time.



PASS-THROUGH TRUTH TABLE

Previous Cycle		Preser	t Cycle			
Operation WRITE		Operation	CS1	CS1 WRITE		Next Cycle
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	Initiate Read Cycle Address=An Data=Qn-1 for all bytes	L	Н	L	Read Cycle Data=Qn
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=Qn-1 for all bytes	Н	Н	L	No carryover from previous cycle
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=High-Z	н	Н	Н	No carryover from previous cycle
Write Cycle, One byte Address=An-1, Data=Dn-1	One L	Initiate Read Cycle Address=An Data=Qn-1 for one byte	L	Н	L	Read Cycle Data=Qn
Write Cycle, One byte Address=An-1, Data=Dn-1	One L	No new cycle Data=Qn-1 for one byte	н	Н	L	No carryover from previous cycle

NOTE: 1. This operation makes written data immediately available at output during a read cycle preceded by a write cycle.

2. WEx means WEa ~ WEd.

ABSOLUTE MAXIMUM RATING*

Parameter	Symbol	Rating	Unit
Voltage on VDD Supply Relative to Vss	VDD	-0.3 to 4.6	V
Voltage on VDDQ Supply Relative to Vss	VDDQ	VDD	V
Voltage on Input Pin Relative to Vss	Vin	-0.3 to 6.0	٧
Voltage on I/O Pin Relative to Vss	Vio	-0.3 to VDDQ + 0.5	٧
Power Dissipation	Pb	1.2	W
Storage Temperature	Тѕтс	-65 to 150	°C
Operating Temperature	TOPR	0 to 70	°C
Storage Temperature Range Under Bias	TBIAS	-10 to 85	Ů

*NOTE: Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS (0°C ≤ TA ≤ 70°C)

Parameter	CONTRACTOR OF THE PROPERTY OF		Тур.	Max	Unit
Supply Voltage	VDD	3.13	3.3	3.6	V
	VDDQ	3.13	3.3	3.6	V
Ground	Vss	0	0	0	V

CAPACITANCE*(TA = 25°C, f = 1MHz)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	CIN	VIN=0V	-	5	pF
Output Capacitance	Соит	Vout=0V	-	7	pF

*NOTE: Sampled not 100% tested.



DC ELECTRICAL CHARACTERISTICS(TA = 0° to 70°, VDD = 3.3V ± 5%)

Parameter	Symbol	Test Conditions	Min	Max	Unit	
Input Leakage Current(except ZZ)	lıL	VDD = Vss to VDD ; VIN = Vss to VDD	-2	+2	μA	
Output Leakage Current	loL	Output Disabled, Vout=Vss to VDDC	-2	+2	μA	
Operating Current	lcc	Device Colored Java Co. A	-7	-	395	
		Device Selected, lout = 0mA, ZZ≤VIL, All Inputs = VIL or VIH	-8	-	360	mA
		Cycle Time ≥ tCYC min	-10	-	320	1111/4
		Syste Time = 1010 IIIII	-11	-	320	1
			-7	-	100	
Standby Current	lan.	Device deselected, IouT = 0mA,	-8	-	90	mA
	ISB	$ZZ \le V_{IL}$, $f = Max$, All Inputs $\le 0.2V$ or $\ge V_{DD}-0.2V$	-10	-	80	
		All Inputs = 0.20 of = 000-0.20	-11	-	80	
	1	Device deselected, louт = 0mA, ZZ≤0.2V, f = 0,		-	10	mA
	1581	All Inputs=fixed (VDD-0.2V or 0.2V)	L-Ver	-	5.0	mA
	IsB2	Device deselected, lout = 0mA, ZZ≥Vpp-0.2V, f = Max,		-	10	mA
	1582	All Inputs ≤ ViL or ≥ ViH	L-Ver	-	1.0	mA
Output Low Voltage	Vol	IoL = 8.0mA		-	0.4	V
Output High Voltage	Voн	Iон = -4.0mA		2.4	-	٧
Input Low Voltage	VIL			-0.5*	0.8	V
Input High Voltage	ViH			2.0	5.5**	V

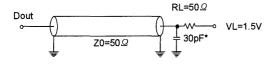
^{*} VIL(min) = -3.0(Pulse Width≤20ns)

TEST CONDITIONS

(TA = 0 $^{\circ}$ to 70 $^{\circ}$, VDD=3.3V-5%/+10%,unless otherwise specified)

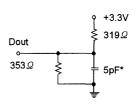
Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time(Measured at 0.3V and 2.7V)	2ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1





* Capacitive Load consists of all components of the test environment.

Output Load(B),(3.3V I/O) (for tLZC, tLZOE, tHZOE& tHZC)



* Including Scope and Jig Capacitance

Fig. 1



^{**} In Case of I/O Pins, the Max. VIH = VDDQ + 0.5V

AC TIMING CHARACTERISTICS

(VDD=3.3V-5%/+10%, TA = 0° to 70°)

Parameter	Symbol		7		8	-	10	-	11	
Faiameter	Syllibol	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Cycle Time	tCYC	7.5	-	8.6	-	10	-	11	-	ns
Clock Access Time	tCD	-	4.5	-	5.0	-	5.0	-	6.0	ns
Output Enable to Data Valid	tOE	-	4.5	-	5.0	-	5.0	-	6.0	ns
Clock High to Output Low-Z	tLZC	. 0	-	0	-	0	-	0	-	ns
Output Hold from Clock High	tOH	1.5	-	1.5	-	1.5	-	1.5	-	ns
Output Enable Low to Output Low-Z	tLZOE	0	-	0	-	0	-	0	-	ns
Output Enable High to Output High-Z	tHZOE	-	4.0	-	4.0	-	4.0	-	4.0	ns
Clock High to Output High-Z	tHZC	1.5	5.0	1.5	5.0	1.5	5.0	1.5	5.0	ns
Clock High Pulse Width	tCH	3.0	-	3.5	-	4.0	-	4.0	-	ns
Clock Low Pulse Width	tCL	3.0	-	3.5	-	4.0	-	4.0	-	ns
Address Setup to Clock High	tAS	2.0	-	2.0	-	2.0	-	2.0	-	ns
Address Status Setup to Clock High	tSS	2.0	-	2.0	-	2.0	-	2.0	-	ns
Data Setup to Clock High	tDS	2.0	-	2.0	-	2.5	-	2.5	-	ns
Write Setup to Clock High (GW, BW, WEx)	tWS	2.0	-	2.0	-	2.0	-	2.0	-	ns
Address Advance Setup to Clock High	tADVS	2.0	-	2.0	-	2.0	-	2.0	-	ns
Chip Select Setup to Clock High	tCSS	2.0	-	2.0	-	2.0	-	2.0	-	ns
Address Hold from Clock High	tAH	0.5	-	0.5	-	0.5	-	0.5		ns
Address Status Hold from Clock High	tSH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Data Hold from Clock High	tDH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Write Hold from Clock High (GW, BW, WEx)	tWH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	tADVH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	tCSH	0.5	-	0.5	-	0.5	-	0.5	-	ns
ZZ High to Power Down	tPDS	2	-	2	-	2	-	2	-	cycl
ZZ Low to Power Up	tPUS	2	-	2		2	-	2	-	cycl

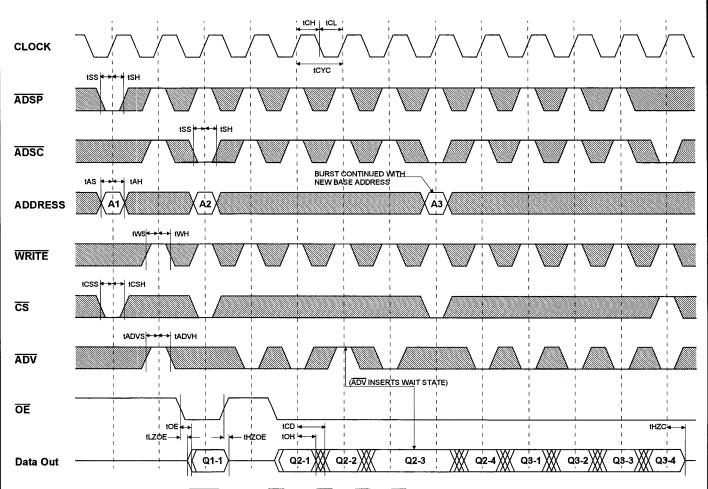
NOTE: 1. All address inputs must meet the specified setup and hold times for all rising clock edges whenever ADSC and/or ADSP is sampled low and CS is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.

2. Both chip selects must be active whenever ADSC or ADSP is sampled low in order for the this device to remain enabled.

3. ADSC or ADSP must not be asserted for at least 2 Clock after leaving ZZ state.



TIMING WAVEFORM OF READ CYCLE



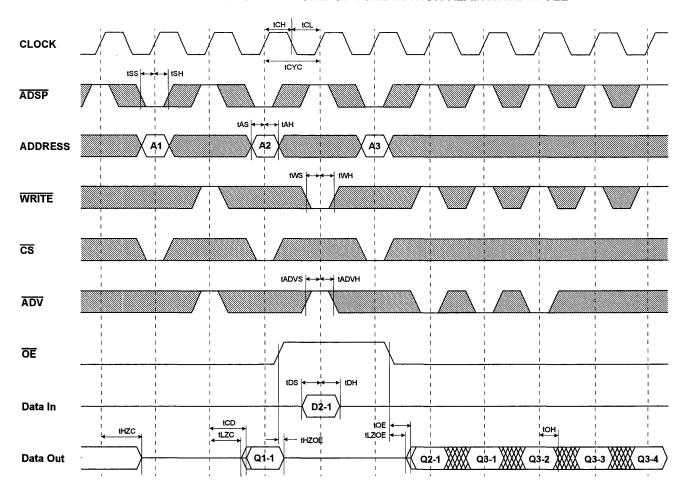
NOTES: $\overline{WR1TE} = L$ means $\overline{GW} = L$, or $\overline{GW} = H$, $\overline{BW} = L$, $\overline{WE}x = L$ $\overline{CS} = L$ means $\overline{CS}1 = L$, CS2 = H and $\overline{CS}2 = L$ $\overline{CS} = H$ means $\overline{CS}1 = H$, or $\overline{CS}1 = L$ and $\overline{CS}2 = H$, or $\overline{CS}1 = L$, and CS2 = L

Don't Care

☑ Undefined

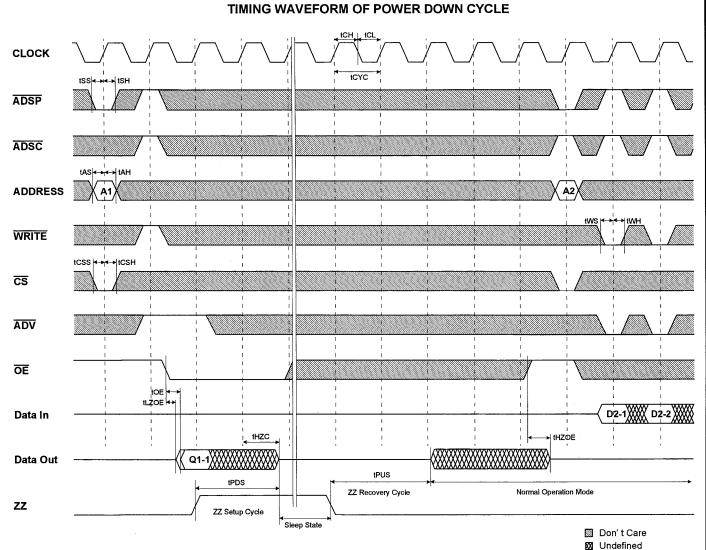
TIMING WAVEFORM OF WRTE CYCLE CLOCK tCYC **ADSP** tSS ADSC (ADSC EXTENDED BURST) tAH **ADDRESS** WRITE tCSS tCSH cs (ADV SUSPENDS BURST) tADVH tADVS | ADV ŌĒ tDS -Data In **←→** tHZOE Data Out Q0-3 Don't Care ☑ Undefined

TIMING WAVEFORM OF COMBINATION READ/WRTE CYCLE



Don't Care

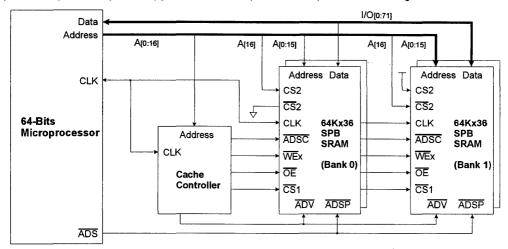
TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE **CLOCK** tCYC **ADSC** tWS←→ tWH **ADDRESS** tWS ← → → tWH WRITE $\overline{\mathsf{cs}}$ ADV ŌĒ tOE ↔ ++ tHZOE tCD⁴ tOH^I◆ **Data Out** -₩tDH tDS -D7-1 Data In Don't Care



APPLICATION INFORMATION

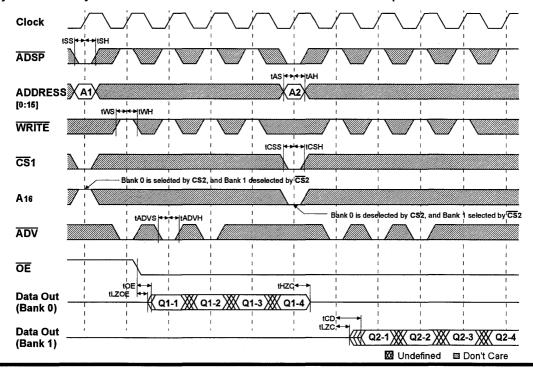
DEPTH EXPANSION

The Samsung 64Kx36 Synchronous Pipelined Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 64K depth to 128K depth without extra logic.



INTERLEAVE READ TIMING (Refer to non-interleave write timing for interleave write timing)

2 Cycle Enable - 1 Cycle Disable Mode can reduce Data Contention in Dual Bank Operation.





128Kx18-Bit Synchronous Burst SRAM FEATURES

- . Synchronous Operation.
- · On-Chip Address Counter.
- · Write Self-Timed Cycle.
- · On-Chip Address and Control Registers.
- Single 3.3 ± 5% Power Supply.
- . 5V Tolerant Inputs except I/O Pins.
- · Byte Writable Function.
- · Global Write Enable Controls a full bus-width write.
- Power Down State via ZZ Signal.
- · Asynchronous Output Enable Control.
- . ADSP, ADSC, ADV Burst Control Pins.
- LBO Pin allows a choice of either a interleaved burst or a linear burst.
- Three Chip Enables for simple depth expansion with No Data Contention.
- . TTL-Level Three-State Output.
- . 100-Pin TQFP Package

FAST ACCESS TIMES

Parameter	Symbol	-8	-9	-10	Unit
Cycle Time	tCYC	12	12	15	ns
Clock Access Time	tCD	8.5	9	10	ns
Output Enable Access Time	tOE	4	4	5	ns

GENERAL DESCRIPTION

The KM718V787 is a 2,359,296 bit Synchronous Static Random Access Memory designed for support zero wait state performance for advanced Pentium/Power PC address pipelining. And with CS1 high, ADSP is blocked to control signal.

It is organized as 128K words of 18 bits and integrates address and control registers, a 2-bit burst address counter and high output drive circuitry onto a single integrated circuit for reduced components count implementation of high performance cache RAM applications.

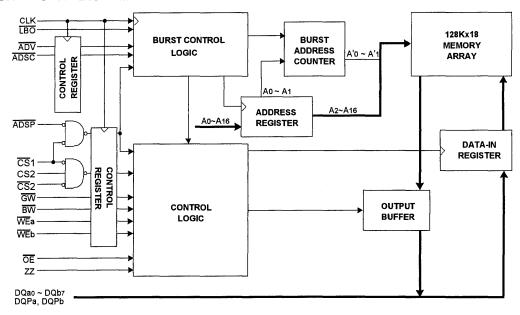
Write cycles are internally self-timed and synchronous.

The self-timed write feature eliminates complex off chip write pulse shaping logic, simplifying the cache design and further reducing the component count.

Burst cycle can be initiated with either the address status processor(ADSP) or address status cache controller(ADSC) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance(ADV) input. ZZ pin controls Power Down State and reduces Stand-by current regardless of CLK.

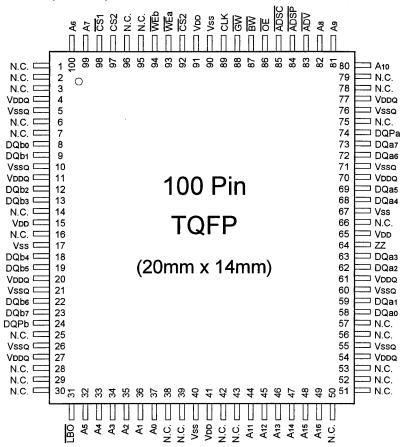
The KM718V787 is implemented in SAMSUNG's high performance CMOS technology and is available in a 100pin TQFP package. Multiple power and ground pins are utilized to minimize ground bounce.

LOGIC BLOCK DIAGRAM





PIN CONFIGURATION(TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A16	Address Inputs	32,33,34,35,36,37,	VDD	Power Supply(+3.3V)	15,41,65,91
	-	44,45,46,47,48,49,	Vss	Ground	17,40,67,90
		80,81,82,99,100	N.C.	No Connect	1,2,3,6,7,14,16,25,28,
ADV	Burst Address Advance	83			29,30,38,39,42,43,50,
ADSP	Address Status Processor	84			51,52,53,56,57,66,75,
ADSC	Address Status Controller	85	1		78,79,95,96
CLK	Clock	89	DQa0 ~ a7	Data Inputs/Outputs	58,59,62,63,68,69,72,73
CS1	Chip Select	98	DQb0 ~ b7		8,9,12,13,18,19,22,23
CS2	Chip Select	97	DQPa, Pb		74,24
CS2	Chip Select	92	VDDQ	Output Power Supply	4,11,20,27,54,61,70,77
WEx	Byte Write Inputs	93,94		(+3.3V)	
ŌĒ	Output Enable	86	Vssq	Output Ground	5,10,21,26,55,60,71,76
Ġ₩	Global Write Enable	88			
BW	Byte Write Enable	87			
ZZ	Power Down Input	64			
LBO	Burst Mode Control	31			



FUNCTION DESCRIPTION

The KM718V787 is a synchronous SRAM designed to support the burst address accessing sequence of the Pentium and Power PC based microprocessor. All inputs(with the exception of \overline{OE} , \overline{LBO} and ZZ) are sampled on rising clock edges. The start and duration of the burst access is controlled by \overline{ADSP} , \overline{ADSO} , \overline{ADV} and Chip Select pins.

When ZZ is pulled HIGH, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM normally operates after 2 cycles of wake up time. ZZ pin is pulled down internally.

Read cycles are initiated with \overline{ADSP} (or \overline{ADSC}) using the new external address clocked into the on-chip address register when both \overline{GW} and \overline{BW} are high or when \overline{BW} is low and both \overline{WE} a and \overline{WE} b are high, When \overline{ADSP} is sampled low, the chip selects are sampled active, and the output buffer is enabled with \overline{OE} , the data of cell array accessed by the current address are projected to the output pins.

Write cycles are also initiated with \overline{ADSP} (or \overline{ADSC}) and are differentiated into two kinds of operations; All byte write operation and individual byte write operation. All byte write occurs by enabling \overline{GW} (in dependent of \overline{BW} and \overline{WE} x.), and individual byte write is performed only when \overline{GW} is High and \overline{BW} is Low. \overline{WE} a controls DQa0 ~ DQa7 and DQPa, \overline{WE} b controls DQb0 ~ DQb7 and DQPb.

CS1 is used to enable the device and conditions internal use of ADSP and is sampled only when a new external address is loaded.

 $\overline{\text{ADV}}$ is ignored at the clock edge when $\overline{\text{ADSP}}$ is asserted, but can be sampled on the subsequent clock edges. The address increases internally for the next access of the burst when $\overline{\text{ADV}}$ is sampled low.

Addresses are generated for the burst access as shown below, The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the LBO pin. When this pin is low, linear burst sequence is selected. And when this pin is High, Interleaved burst sequence is selected.

BURST SEQUENCE TABLE

(Interleaved Burst)

LBO PIN HIGH	Case 1		Case 2		Cas	se 3 Case 4		
LDOTTN	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
	0	1	0	0	1	1	1	0
1	1	0	1	1	0	0	0	1
Fourth Address	1	1	1	0	0	1	0	0

(Linear Burst)

LBO PIN LOW	Case 1 Case 2			Ca	se 3	Case 4		
LBO FIN	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
1	0	1	1	0	1 1	1	0	0
J.	1	0	1	1	0	0	0	1
Fourth Address	1	1	0	0	0	1	1	0

NOTE: 1. LBO pin must be tied to High or Low, and Floating State must not be allowed.

TRUTH TABLES

ASYNCHRONOUS TRUTH TABLE

(See Notes 1 and 2):

Operation	ZZ	ŌĒ	I/O Status
Sleep Mode	Н	X	High-Z
Read	L	L	DQ
Read	L	Н	High-Z
Write	L	X	Din, High-Z
Deselected	L	Х	High-Z

NOTE

- 1. X means "Don't Care"
- 2. ZZ pin is pulled down internally
- 3. For write cycles that following read cycles, the output buffers must be disabled with \overline{OE} , otherwise data bus contention will occur.
- 4. Sleep Mode means power down state of which stand-by current does not depend on cycle time.
- Deselected means power down state of which stand-by current depends on cycle time.

SYNCHRONOUS TRUTH TABLE

CS1	CS2	CS2	ADSP	ADSC	ADV	WRITE	CLK	Address Accessed	Operation
Н	Х	Х	Х	L	Х	Х	1	None	Not Selected
L	L	Х	L	Х	Х	Х	1	None	Not Selected
L	Х	Н	L	Х	Х	Х	1	None	Not Selected
L	L	Х	Х	L	Х	Х	1	None	Not Selected
L	Х	Н	Х	L	Х	Х	1	None	Not Selected
L	Н	L	L	Х	Х	Х	1	External Address	Begin Burst Read Cycle
L	Н	L	Н	L	Х	L	1	External Address	Begin Burst Write Cycle
L	Н	L	Н	L	Х	Н	1	External Address	Begin Burst Read Cycle
Х	Х	Х	Н	Н	L	Н	1	Next Address	Continue Burst Read Cycle
Н	Х	Х	Х	Н	L	Н	1	Next Address	Continue Burst Read Cycle
Х	Х	Х	Н	Н	L	L	1	Next Address	Continue Burst Write Cycle
Н	Х	Х	Х	Н	L	L	1	Next Address	Continue Burst Write Cycle
Х	Х	Х	Н	Н	Н	Н	1	Current Address	Suspend Burst Read Cycle
Н	Х	Х	Х	Н	Н	Н	1	Current Address	Suspend Burst Read Cycle
Х	Х	Х	Н	Н	Н	. L	1	Current Address	Suspend Burst Write Cycle
Н	Х	X	Х	Н	Н	L	1	Current Address	Suspend Burst Write Cycle

NOTE: 1. X means "Don't Care".

- 2. The rising edge of clock is symbolized by \uparrow .
- 3. WRITE = L means Write operation in WRITE TRUTH TABLE.
 WRITE = H means Read operation in WRITE TRUTH TABLE.
- 4. Operation finally depends on status of asynchronous input pins(ZZ and OE).

WRITE TRUTH TABLE

GW	BW	WEa	WEb	Operation
Н	Н	Х	X	READ
Н	L	Н	Н	READ
Н	L	L	Н	WRITE BYTE a
Н	L	Н	L	WRITE BYTE b
Н	L	L	L	WRITE ALL BYTEs
L	Х	Х	Х	WRITE ALL BYTEs

NOTE: 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(\uparrow).

ABSOLUTE MAXIMUM RATING*

Parameter	Symbol	Rating	Unit
Voltage on VDD Supply Relative to Vss	VDD	-0.3 to 4.6	V
Voltage on VDDQ Supply Relative to Vss	VDDQ	VDD	V
Voltage on Input Pin Relative to Vss	VIN	-0.3 to 6.0	V
Voltage on I/O Pin Relative to Vss	Vio	-0.3 to VDDQ + 0.5	٧
Power Dissipation	Po	1.2	W
Storage Temperature	Тѕтс	-65 to 150	°C
Operating Temperature	Topr	0 to 70	င
Storage Temperature Range Under Bias	TBIAS	-10 to 85	°C

*NOTE: Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.



OPERATING CONDITIONS($0^{\circ} \le TA \le 70^{\circ}$)

Parameter	Symbol	Min	Тур.	Max	Unit
Supply Voltage	VDD	3.13	3.3	3.47	٧
	VDDQ	3.13	3.3	3.47	V
Ground	Vss	0	0	0	٧

CAPACITANCE*(TA = 25°C, f = 1MHz)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	CIN	VIN=0V	-	5	рF
Output Capacitance	Cout	Vout=0V	-	8	pF

^{*}NOTE: Sampled not 100% tested.

TEST CONDITIONS(TA = 0°C to 70°C, VDD = $3.3V\pm5\%$, unless otherwise specified)

Parameter	Value				
Input Pulse Level	0 to 3V				
Input Rise and Fall Time(Measured at 0.3V and 2.7V)	2ns				
Input and Output Timing Reference Levels	1.5V				
Output Load	See Fig. 1				

DC ELECTRICAL CHARACTERISTICS (TA = 0°C to 70°C, VDD = 3.3V±5%)

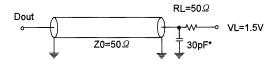
Parameter	Symbol	Test Conditions	Min	Max	Unit	
Input Leakage Current(except ZZ)	lıL	VDD = Max ; VIN = Vss to VDD	-2	2	μA	
Output Leakage Current	loL	Output Disabled, Vout = Vss to Vo	-2	2	μA	
Operating Current	Icc	Device Selected, IOUT = 0mA,	-8	-	330	
		ZZ≤ViL, All Inputs = ViL or ViH	-9	-	330	mA
		Cycle Time ≥ tCYC min	-10	-	300	
Standby Current	ISB	Device deselected, lout = 0mA,	-8	-	80	mA
		ZZ≤VIL, f = Max, All Inputs≤0.2V or ≥ VDD-0.2V	-9	-	80	
			-10	-	60	1
	IsB1	Device deselected, IouT = 0mA, ZZ f = 0, All Inputs = fixed (VDD-0.2V	_	10	mA	
	Is82	Device deselected, IouT = 0mA, ZZ≥Vpp-0.2V, f = Max, All Inputs≤ViL or ≥ViH	-	10	mA	
Output Low Voltage	Vol	IOL = 8.0mA	-	0.4	V	
Output High Voltage	Voн	Iон = -4.0mA		2.4	-	V
Input Low Voltage	VIL			-0.5*	0.8	V
Input High Voltage	ViH			2.2	5.5**	V

^{*} VIL(min) = -3.0(Pulse Width \le 20ns)

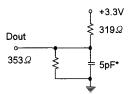


^{**} In Case of I/O Pins, the Max. VIH = VDDQ + 0.5V

Output Load(A)



Output Load(B) (for tLZC, tLZOE, tHZOE& tHZC)



* Including Scope and Jig Capacitance

Fig. 1

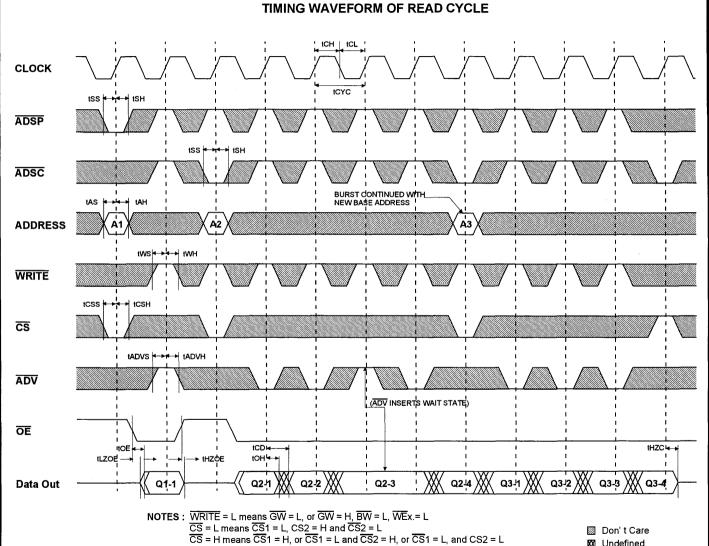
AC TIMING CHARACTERISTICS (TA = 0 $^{\circ}$ to 70 $^{\circ}$, VDD = 3.3V $^{\pm}$ 5%)

Parameter	Symbol	KM718V787-8		KM718V787-9		KM718V787-10		Unit
Parameter		Min	Max	Min	Max	Min	Max) Uiiii
Cycle Time	tCYC	12	-	12	-	15	-	ns
Clock Access Time	tCD	-	8.5	-	9	-	10	ns
Output Enable to Data Valid	tOE	-	4	-	4	-	5	ns
Clock High to Output Low-Z	tLZC	4	-	4	-	6	-	ns
Output Hold from Clock High	tOH	3	-	3	-	3	-	ns
Output Enable Low to Output Low-Z	tLZOE	0	-	0	-	0	-	ns
Output Enable High to Output High-Z	tHZOE	2	5	2	5	2	5	ns
Clock High to Output High-Z	tHZC	-	5	-	5	-	6	ns
Clock High Pulse Width	tCH	4	-	4	-	5	-	ns
Clock Low Pulse Width	tCL	4	-	4	-	5	-	ns
Address Setup to Clock High	tAS	2.5	-	2.5	-	2.5	-	ns
Address Status Setup to Clock High	tSS	2.5	-	2.5	-	2.5	-	ns
Data Setup to Clock High	tDS	2.5	-	2.5	-	2.5	-	ns
Write Setup to Clock High	tWS	2.5	-	2.5	-	2.5	-	ns
Address Advance Setup to Clock High	tADVS	2.5	-	2.5	-	2.5	-	ns
Chip Select Setup to Clock High	tCSS	2.5	-	2.5]	2.5	-	ns
Address Hold from Clock High	tAH	0.5		0.5	-	0.5	-	ns
Address Status Hold from Clock High	tSH	0.5	-	0.5	-	0.5		ns
Data Hold from Clock High	tDH	0.5	-	0.5	-	0.5	-	ns
Write Hold from Clock High(GW, BW, WEx)	tWH	0.5	-	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	tADVH	0.5	-	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	tCSH	0.5	-	0.5	-	0.5	-	ns
ZZ High to Power Down	tPDS	2	-	2	-	2	-	cycle
ZZ Low to Power Up	tPUS	2	-	2		2	-	cycle

NOTE: 1. All address inputs must meet the specified setup and hold times for all rising clock edges whenever ADSC and/or ADSP is sampled low and CS is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.

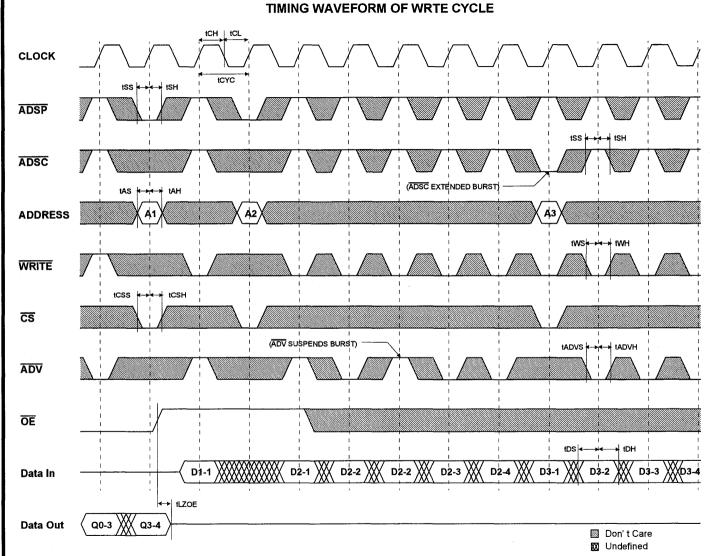
- 2. Both chip selects must be active whenever ADSC or ADSP is sampled low in order for the this device to remain enabled.
- 3. ADSC or ADSP must not be asserted for at least 2 Clock after leaving ZZ state.

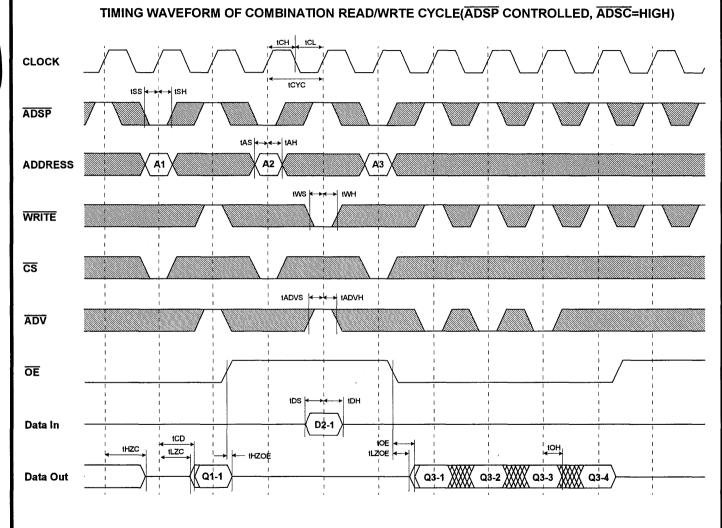




Don't Care

₩ Undefined





UMSUNG

ELECTRONICS

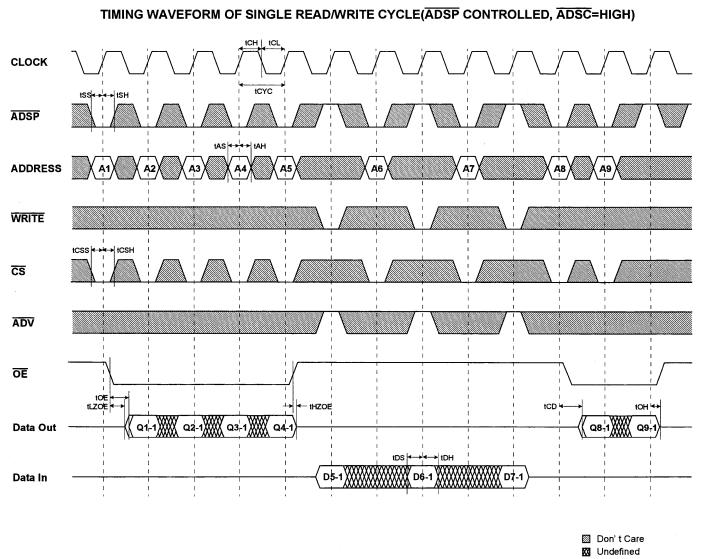
Don't Care

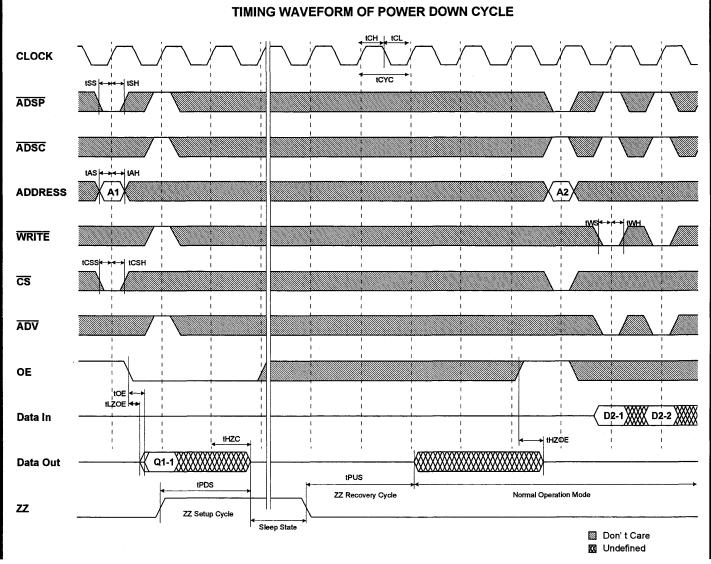
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TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE(ADSC CONTROLLED, ADSP=HIGH) CLOCK tCYC **ADSC** tWS ← → tWH **ADDRESS** tWS < →< → tWH WRITE tCSS ¥ →+→ tCSH CS ADV ŌĒ tOE ←→ tHZOE tOH ¹ ◀ tCD 4 Data Out tDS | Data in Don't Care

SUMSUNG

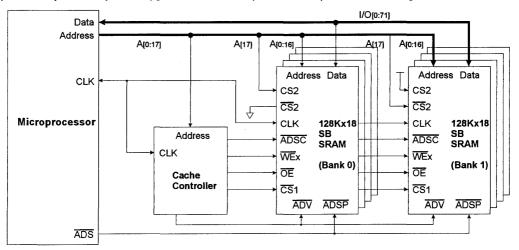




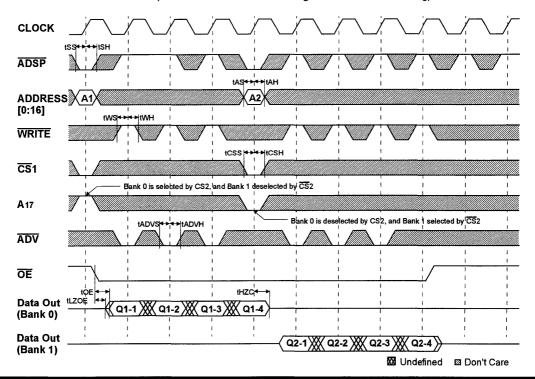
APPLICATION INFORMATION

DEPTH EXPANSION

The Samsung 128Kx18 Synchronous Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 128K depth to 256K depth without extra logic.



INTERLEAVE READ TIMING (Refer non-interleave write timing for interleave write timing)



64Kx36-Bit Synchronous Burst SRAM FEATURES

- · Synchronous Operation.
- · On-Chip Address Counter.
- Write Self-Timed Cycle.
- · On-Chip Address and Control Registers.
- Single 3.3V ± 5% Power Supply.
- . 5V Tolerant Inputs except I/O Pins.
- · Byte Writable Function.
- · Global Write Enable Controls a full bus-width write.
- · Power Down State via ZZ Signal.
- Asynchronous Output Enable Control.
- . ADSP, ADSC, ADV Burst Control Pins.
- LBO Pin allows a choice of either a interleaved burst or a linear burst.
- Three Chip Enables for simple depth expansion with No Data Contention.
- . TTL-Level Three-State Output.
- 100-Pin TQFP Package

FAST ACCESS TIMES

Parameter	Symbol	-8	-9	-10	Unit
Cycle Time	tCYC	12	12	15	ns
Clock Access Time	tCD	8.5	9	10	ns
Output Enable Access Time	tOE	4	4	5	ns

GENERAL DESCRIPTION

The KM736V687 is 2,359,296 bits Synchronous Static Random Access Memory designed to support zero wait state performance for advanced Pentium/Power PC based system. And with $\overline{\text{CS}}1$ high, $\overline{\text{ADSP}}$ is blocked to control signals.

It can be organized as 64K words of 36 bits. And it integrates address and control registers, a 2-bit burst address counter and high output drive circuitry onto a single integrated circuit for reduced components counts implementation of high performance cache RAM applications.

Write cycles are internally self-timed and synchronous.

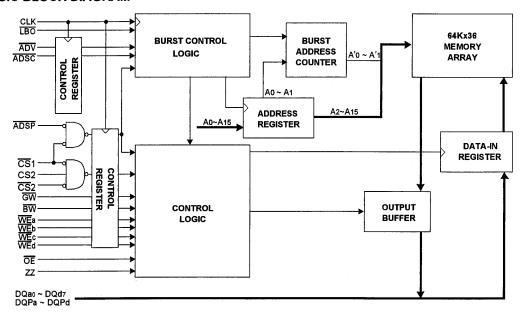
The self-timed write feature eliminates complex off chip write pulse shaping logic, simplifying the cache design and further reducing the component count.

Burst cycle can be initiated with either the address status processor(ADSP) or address status cache controller(ADSC) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance(ADV) input.

ZZ pin controls Power Down State and reduces Stand-by current regardless of CLK.

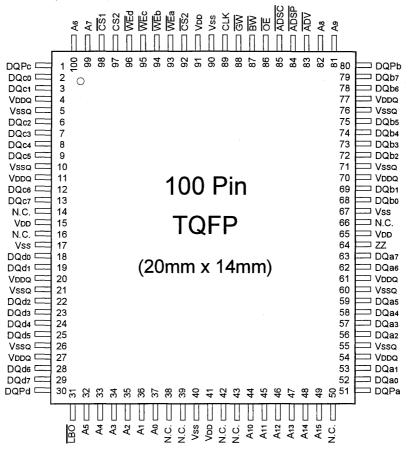
The KM736V687 is implemented with SAMSUNG's high performance CMOS technology and is available in a 100pin TQFP package. Multiple power and ground pins are utilized to minimize ground bounce.

LOGIC BLOCK DIAGRAM





PIN CONFIGURATION (TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A15	Address Inputs	32,33,34,35,36,37,	VDD	Power Supply(+3.3V)	15,41,65,91
		44,45,46,47,48,49,	Vss	Ground	17,40,67,90
	İ	81,82,99,100	N.C.	No Connect	14,16,38,39,42,43,50,66
ĀDV	Burst Address Advance	83		ł	
ADSP	Address Status Processor	84	DQa0 ~ a7	Data Inputs/Outputs	52,53,56,57,58,59,62,63
ADSC	Address Status Controller	85	DQb0 ~ b7	1	68,69,72,73,74,75,78,79
CLK	Clock	89	DQc0 ~ c7		2,3,6,7,8,9,12,13
CS1	Chip Select	98	DQdo ~ d7		18,19,22,23,24,25,28,29
CS2	Chip Select	97	DQPa~Pd	1	51,80,1,30
CS2	Chip Select	92			
WEx	Byte Write Inputs	93,94,95,96	VDDQ	Output Power Supply	4,11,20,27,54,61,70,77
ŌĒ	Output Enable	86		(+3.3V)	
Ġ₩	Global Write Enable	88	VssQ	Output Ground	5,10,21,26,55,60,71,76
₿₩	Byte Write Enable	87			
ZZ	Power Down Input	64			
LBO	Burst Mode Control	31			

FUNCTION DESCRIPTIONThe KM736V687 is a synchronous SRAM designed to <u>support</u> the burst address accessing sequence of the Pentium and Power PC based microprocessor. All inputs (with the exception of OE, LBO and ZZ) are sampled on rising clock edges. The start and duration of the burst access is controlled by ADSC, ADSP and ADV and chip select pins.

When ZZ is pulled high, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM normally operates after 2 cycles of wake up time. ZZ pin is pulled down internally.

Read cycles are initiated with ADSP(or ADSC) using the new external address clocked into the on-chip address register when both GW and BW are high or when BW is low and WEa, WEb, WEc, and WEd are high. When ADSP is sampled low, the chip selects are sampled active, and the output buffer is enabled with OE. the data of cell array accessed by the current address are projected to the output

Write cycles are also initiated with ADSP(or ADSC) and are differentiated into two kinds of operations; All byte write operation and individual byte write operation.

All byte write occurs by enabling GW(independent of BW and WEx.), and individual byte write is performed only when GW is high and BW is low. In KM736V687, a 64Kx36 organization, WEa controls DQa0 ~ DQa7 and DQPa, WEb controls DQb0 ~ DQb7 and DQPb, WEc controls DQc0 ~ DQc7 and DQPc and WEd controls DQd0 ~ DQd7 and DQPd.

CS1 is used to enable the device and conditions internal use of ADSP and is sampled only when a new external address is loaded.

ADV is ignored at the clock edge when ADSP is asserted, but can be sampled on the subsequent clock edges. The address increases internally for the next access of the burst when ADV is sampled low.

Addresses are generated for the burst access as shown below. The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the LBO pin. When this pin is Low, linear burst sequence is selected. And this pin is High, Interleaved burst sequence is selected.

BURST SEQUENCE TABLE

(Interleaved Burst)

LBO PIN HIGH	Cas	se 1	Case 2		Case 3		Case 4	
LBO FIN	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
	0	1	0	0	1	1	1	0
↓	1	0	1	1	0	0	0	1
Fourth Address	1	1	1	0	0	1	0	0

(Linear Burst)

EBO PIN LOW	Cas	se 1	Cas	se 2	Cas	se 3	Ca	se 4
LDO FIN LOW	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
	0	1	1	0	1	1	0 .	0
	1	0	1	1	0	0	l 0	1
Fourth Address	1	1	0	0	0	1	1	0

NOTE: 1. LBO pin must be tied to high or low, and floating state must not be allowed.

ASYNCHRONOUS TRUTH TABLE

(See Notes 1 and 2):

Operation	ZZ	ŌĒ	I/O Status
Sleep Mode	Н	Х	High-Z
Read	L	L	DQ
Read	L	Н	High-Z
Write	L	Х	Din, High-Z
Deselected	L	Х	High-Z

NOTE

- 1. X means "Don't Care".
- 2. ZZ pin is pulled down internally
- 3. For write cycles that following read cycles, the output buffers must be disabled with OE, otherwise data bus contention will occur.
- 4. Sleep Mode means power down state of which stand-by current does not depend on cycle time.
- 5. Deselected means power down state of which stand-by current depends on cycle time.



SYNCHRONOUS TRUTH TABLE

CS1	CS2	CS2	ADSP	ADSC	ADV	WRITE	CLK	Address Accessed	Operation
Н	Х	Х	X	L	Х	Х	1	N/A	Not Selected
L	L	Х	L	Х	Х	Х	1	N/A	Not Selected
L	Х	Н	L	Х	Х	Х	1	N/A	Not Selected
L	L	Х	Х	L	Х	Х	1	N/A	Not Selected
L	Х	Н	Х	L	Χ	Х	1	N/A	Not Selected
L	Н	L	L	Х	Х	Х	1	External Address	Begin Burst Read Cycle
L	Н	L	Н	L	Х	L	1	External Address	Begin Burst Write Cycle
L	Н	L	Н	L	Χ	Н	1	External Address	Begin Burst Read Cycle
Х	Х	Х	Н	Н	L	Н	1	Next Address	Continue Burst Read Cycle
Н	Х	Х	X	Н	L	Н	1	Next Address	Continue Burst Read Cycle
Х	Х	Х	Н	Н	L	L	1	Next Address	Continue Burst Write Cycle
Н	X	Х	×	Н	L	٦	1	Next Address	Continue Burst Write Cycle
Х	Х	Х	Н	Н	Н	Н	1	Current Address	Suspend Burst Read Cycle
Н	Х	Х	Х	Н	Η	Н	1	Current Address	Suspend Burst Read Cycle
Х	Х	Х	Н	Н	Н	L	1	Current Address	Suspend Burst Write Cycle
Н	Х	Χ	Х	Н	Ξ	L	1	Current Address	Suspend Burst Write Cycle

NOTE: 1. X means "Don't Care".

- 2. The rising edge of clock is symbolized by 1.
- 3. WRITE = L means Write operation in WRITE TRUTH TABLE.
 WRITE = H means Read operation in WRITE TRUTH TABLE.
- 4. Operation finally depends on status of asynchronous input pins(ZZ and OE).

WRITE TRUTH TABLE

GW	BW	WEa	WEb	WEc	WEd	Operation
Н	Н	Х	Х	X	Х	READ
Н	L	Н	Н	Н	Н	READ
H	L	L	Н	Н	Н	WRITE BYTE a
Н	L	Н	L	Н	Н	WRITE BYTE b
Н	L	н	Н	L	L	WRITE BYTE c and d
Н	L	L	L	L	L	WRITE ALL BYTEs
L	X	Х	Х	Х	X	WRITE ALL BYTEs

NOTE: 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(\uparrow).

ABSOLUTE MAXIMUM RATING*

Parameter	Symbol	Rating	Unit
Voltage on VDD Supply Relative to Vss	VDD	-0.3 to 4.6	٧
Voltage on VDDQ Supply Relative to Vss	VDDQ	VDD	V
Voltage on Input Pin Relative to Vss	Vin	-0.3 to 6.0	V
Voltage on I/O Pin Relative to Vss	Vio	-0.3 to VDDQ + 0.5	٧
Power Dissipation	PD	1.2	W
Storage Temperature	Тѕтс	-65 to 150	°C
Operating Temperature	Topr	0 to 70	°C
Storage Temperature Range Under Bias	TBIAS	-10 to 85	°C

*NOTE: Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.



OPERATING CONDITIONS(0°C \leq TA \leq 70°C)

Parameter		Min	Тур.	Max	Unit
	VDD	3.13	3.3	3.47	٧
Supply Voltage	VDDQ	3.13	3.3	3.47	٧
Ground	Vss	0	0	0	V

CAPACITANCE*(TA = 25°C, f = 1MHz)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	CIN	VIN=0V	-	5	pF
Output Capacitance	Соит	Vout=0V	-	8	pF

*NOTE: Sampled not 100% tested.

TEST CONDITIONS(TA = 0 °C to 70 °C, VDD = 3.3V ±5%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time(Measured at 0.3V and 2.7V)	2ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1

DC ELECTRICAL CHARACTERISTICS(TA = 0° to 70° , VDD = $3.3V \pm 5\%$)

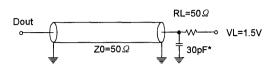
Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current(except ZZ)	lıL	VDD = Max , VIN = Vss to VDD		-2	+2	μA
Output Leakage Current	loL	Output Disabled, Vout = Vss to Vo	DQ	-2	+2	μA
Operating Current	Icc	Icc Device Selected, IouT = 0mA, -8		-	330	
		ZZ≤VIL, All Inputs = VIL or VIH	-9	-	330	mA
		Cycle Time ≥ tCYC min	-10	-	300	
Standby Current		Device deselected, lout = 0mA,	-8	-	80	
	ZZ≤VIL, f = Max,	-9	-	80	mA	
		All Inputs $\leq 0.2V$ or $\geq VDD-0.2V$	-10	-	60	1
	IsB1	ZZ ≤ 0.2V, f = 0, All Inputs = fixed (VDD-0.2V or 0.2V)		-	10	mA
	Iss2			-	10	mA
Output Low Voltage	Vol	IoL = 8.0mA		-	0.4	V
Output High Voltage	Voн	Iон = -4.0mA		2.4	-	V
Input Low Voltage	VIL			-0.5*	0.8	V
Input High Voltage	VIH			2.2	5.5**	٧

^{*} VIL(min) = -3.0(Pulse Width≤20ns)

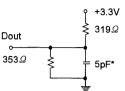


^{**} In Case of I/O Pins, the Max. VIH = VDDQ + 0.5V

Output Load(A)



Output Load(B) (for tLZC, tLZOE, tHZOE& tHZC)



* Including Scope and Jig Capacitance

Fig. 1

AC TIMING CHARACTERISTICS (TA = 0° to 70° , VDD = $3.3V \pm 5\%$)

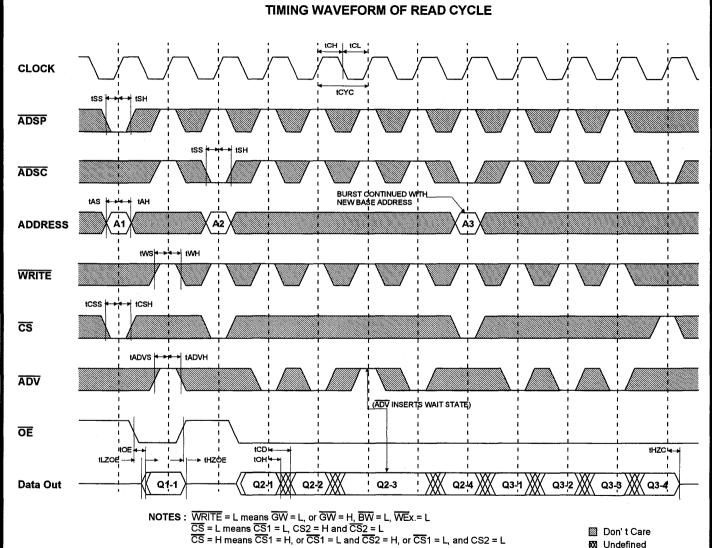
Parameter	Symbol	KM736V687-8		KM736V687-9		KM736V687-10		Unit
Falallictei	Symbol	Min	Max	Min	Max	Min	Max	Unit
Cycle Time	tCYC	12	-	12	-	15	-	ns
Clock Access Time	tCD	-	8.5	-	9	-	10	ns
Output Enable to Data Valid	tOE	-	4	-	4	-	5	ns
Clock High to Output Low-Z	tLZC	4	-	4	-	6	-	ns
Output Hold from Clock High	tOH	3	-	3	-	3	-	ns
Output Enable Low to Output Low-Z	tLZOE	0	-	0	-	0	-	ns
Output Enable High to Output High-Z	tHZOE	2	5	2	5	2	5	ns
Clock High to Output High-Z	tHZC	-	5	-	5	-	6	ns
Clock High Pulse Width	tCH	4	-	4	-	5	-	ns
Clock Low Pulse Width	tCL	4	-	4	-	5	-	ns
Address Setup to Clock High	tAS	2.5	-	2.5	-	2.5	-	ns
Address Status Setup to Clock High	tSS	2.5	-	2.5	-	2.5	-	ns
Data Setup to Clock High	tDS	2.5	-	2.5	-	2.5	-	ns
Write Setup to Clock High	tWS	2.5	-	2.5	-	2.5	-	ns
Address/Advance Setup to Clock High	tADVS	2.5	-	2.5	-	2.5	-	ns
Chip Select Setup to Clock High	tCSS	2.5	-	2.5	-	2.5	-	ns
Address Hold from Clock High	tAH	0.5	-	0.5	-	0.5	-	ns
Address Status Hold from Clock High	tSH	0.5	-	0.5	-	0.5	-	ns
Data Hold from Clock High	tDH	0.5	-	0.5	-	0.5	-	ns
Write Hold from Clock High	tWH	0.5	-	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	tADVH	0.5	-	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	tCSH	0.5	-	0.5	-	0.5	-	ns
ZZ High to Power Down	tPDS	2	-	2	-	2	-	cycle
ZZ Low to Power Up	tPUS	2	-	2	-	2	-	cycle

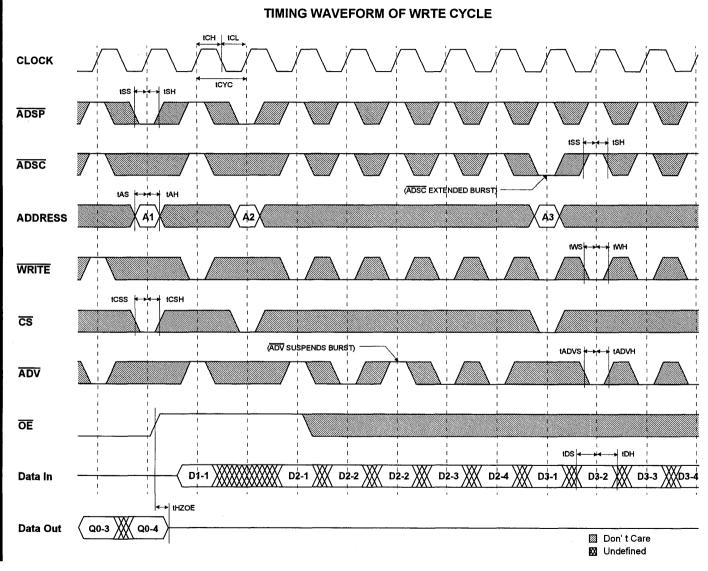
NOTE: 1. All address inputs must meet the specified setup and hold times for all rising clock edges whenever ADSC and/or ADSP is sampled low and CS is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.

2. Both chip selects must be active whenever ADSC or ADSP is sampled low in order for the this device to remain enabled.

3. ADSC or ADSP must not be asserted for at least 2 Clock after leaving ZZ state.







SAMSUNG

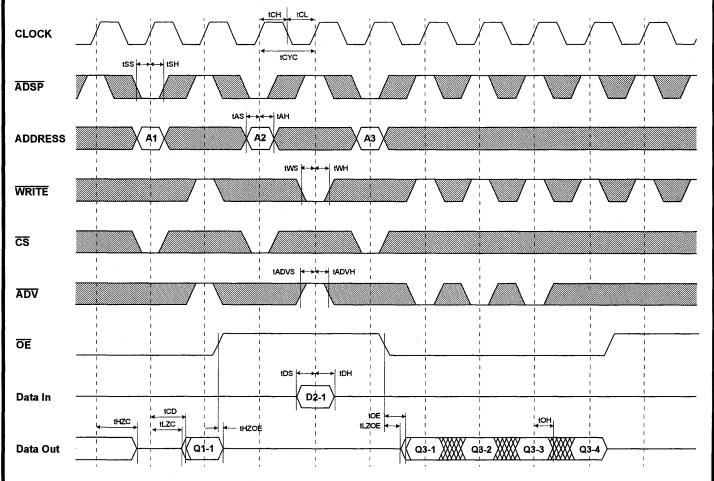
ELECTRONICS

SAMSUNG

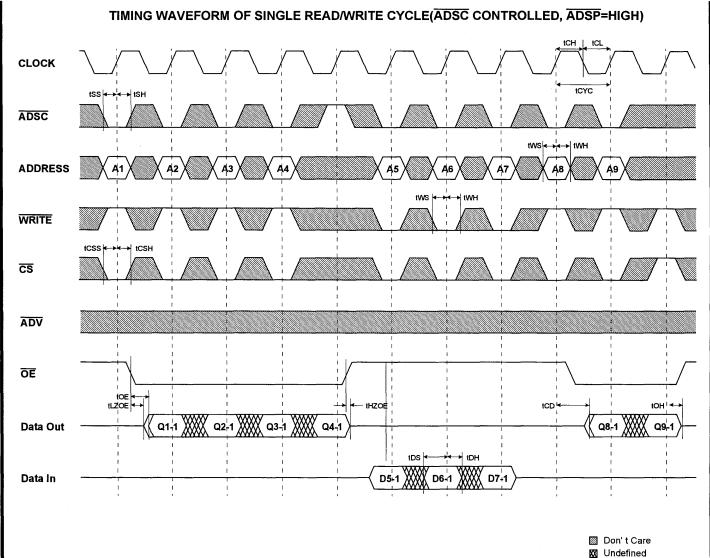
- 9 -

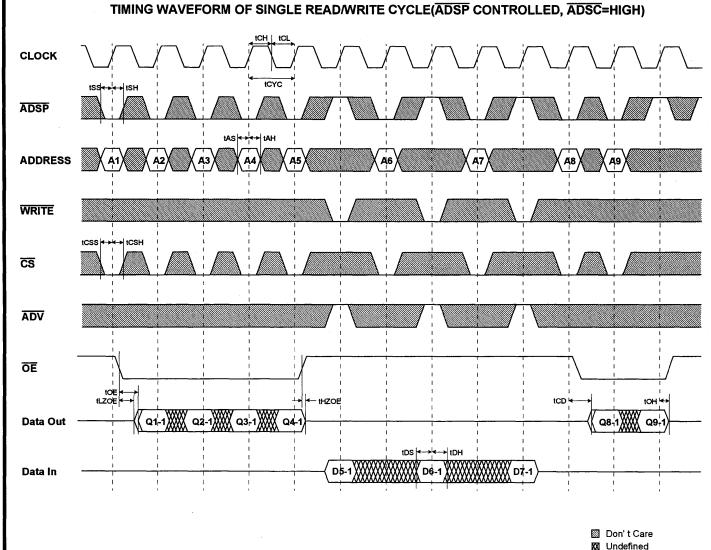
Don't Care

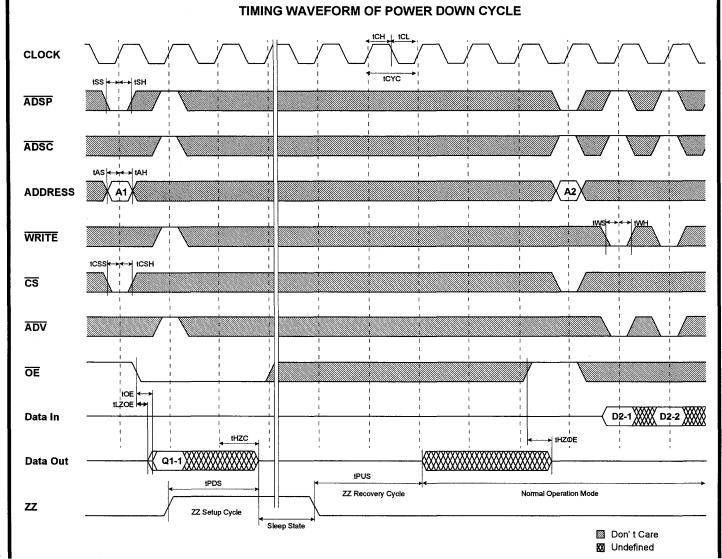
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TIMING WAVEFORM OF COMBINATION READ/WRTE CYCLE(ADSP CONTROLLED, ADSC=HIGH)



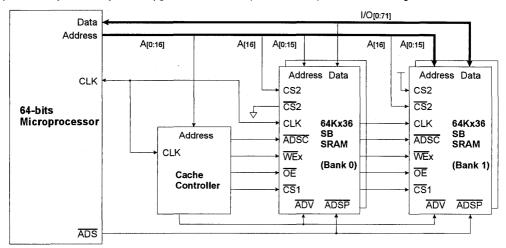




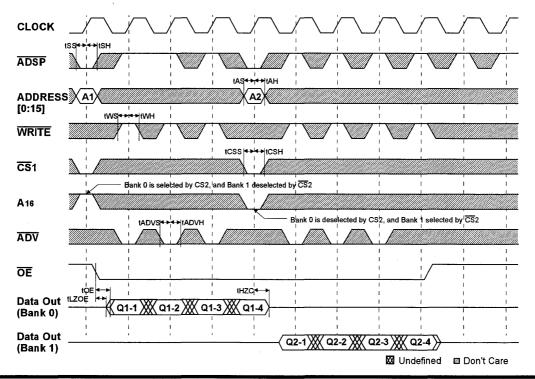
APPLICATION INFORMATION

DEPTH EXPANSION

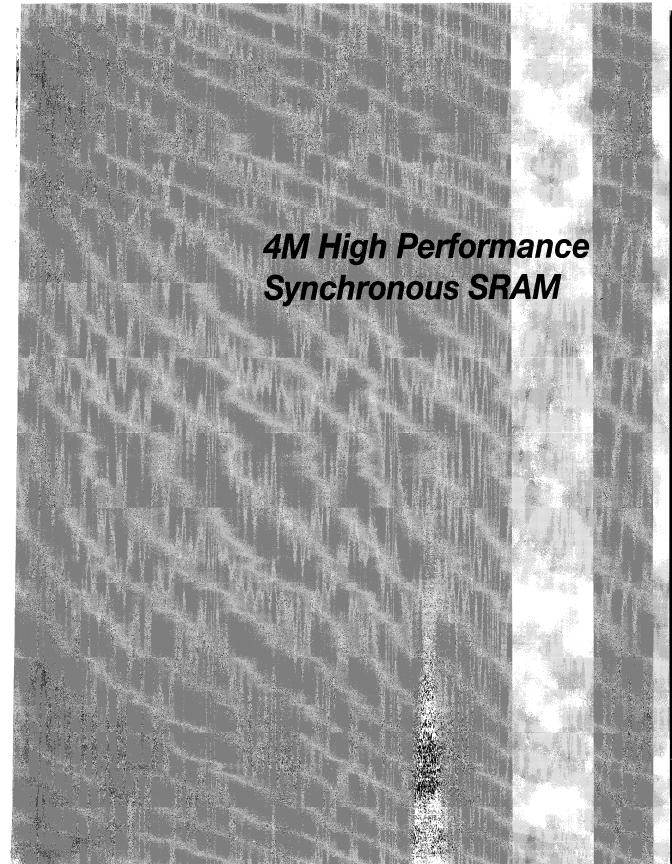
The Samsung 64Kx36 Synchronous Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 64K depth to 128K depth without extra logic.



INTERLEAVE READ TIMING (Refer non-interleave write timing for interleave write timing)







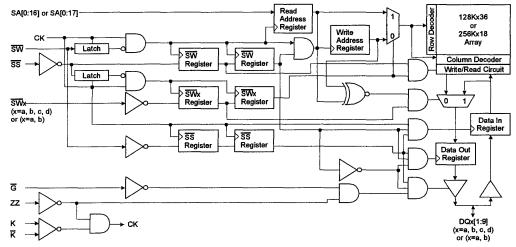
128Kx36 & 256Kx18 Synchronous Pipelined SRAM FEATURES

- . 128Kx36 or 256Kx18 Organizations.
- 3.3V Core/1.5V Output Power Supply.
- . HSTL Input and Output Levels.
- Differential, HSTL Clock Inputs K, K.
- . Synchronous Read and Write Operation
- · Registered Input and Registered Output
- . Internal Pipeline Latches to Support Late Write.
- Byte Write Capability(four byte write selects, one for each 9 bits)
- · Synchronous or Asynchronous Output Enable.
- Power Down Mode via ZZ Signal.
- Programmable Impedance Output Drivers.

- . JTAG 1149.1 Compatible Test Access port.
- 119(7x17) Pin Ball Grid Array Package(14mm x 22mm).

Organization	Part Number	Cycle Time	Access Time
	KM736FV4011H-5	5	2.5
128Kx36	KM736FV4011H-6	6	3.0
	KM736FV4011H-7	7	3.5
	KM718FV4011H-5	5	2.5
256Kx18	KM718FV4011H-6	6	3.0
	KM718FV4011H-7	7	3.5

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

Pin Name	Pin Description	Pin Name	Pin Description
κ, ₹	Differential Clocks	c, c	Differential Output Clocks
SAn	Synchronous Address Input	M1, M2	Read Protocol Mode Pins
DQn	Bi-directional Data Bus	ਫ	Asynchronous Output Enable
≅₩	Synchronous Grobal Write Enable	<u> इड</u>	Synchronous Select
SWa	Synchronous Byte a Write Enable	TCK	JTAG Test Clock
SWb	Synchronous Byte b Write Enable	TMS	JTAG Test Mode Select
SWc	Synchronous Byte c Write Enable	TDI	JTAG Test Data Input
S₩d	Synchronous Byte d Write Enable	TDO	JTAG Test Data Output
ZZ	Asynchronous Power Down	ZQ	Output Driver Impedance Control Input HSTL Level
VDD	Core Power Supply	Vss	GND
VDDQ	Output Power Supply	NC	No Connection
VREF	HSTL Input Reference Voltage		

NOTE: 1. This SRAM only supports single clock, register-register read protocol and have fixed impedance output driver.

Therefore the following inputs must be set with power up and must not change during SRAM operation;

C=VDD, C=Vss, M1=Vss, M2=VDD. But they are also designed to operate being left floating.



PACKAGE PIN CONFIGURATIONS (TOP VIEW)

KM736FV4011(128Kx36)

	1	2	3	4	5	6	7
Α	VDDQ	SA13	SA10	NC	SA7	SA4	VDDQ
В	NC	NC	SA9	NC	SA8	NC	NC
С	NC	SA12	SA11	VDD	SA6	SA5	NC
D	DQc8	DQc9	Vss	ZQ	Vss	DQb9	DQb8
E	DQc6	DQc7	Vss	<u>ss</u>	Vss	DQb7	DQb6
F	VDDQ	DQc5	Vss	<u></u>	Vss	DQb5	VDDQ
G	DQc3	DQc4	≅₩c	ਟ	SWb	DQb4	DQb3
Н	DQc1	DQc2	Vss	С	Vss	DQb2	DQb1
J	VDDQ	VDD	VREF	VDD	VREF	VDD	VDDQ
K	DQd1	DQd2	Vss	K	Vss	DQa2	DQa1
L	DQd3	DQd4	SWd	ĸ	SWa	DQa4	DQa3
M	VDDQ	DQd5	Vss	SW	Vss	DQa5	VDDQ
N	DQd6	DQd7	Vss	SA16	Vss	DQa7	DQa6
Р	DQd8	DQd9	Vss	SA ₀	Vss	DQa9	DQa8
R	NC	SA15	M1	VDD	M2	SA ₂	NC
T	NC	NC	SA14	SA1	SA ₃	NC	ZZ
U	VDDQ	TMS	TDI	TCK	TDO	NC	VDDQ

KM718FV4011(256Kx18)

	1	2	3	4	5	6	7
Α	VDDQ	SA13	SA10	NC	SA7	SA4	VDDQ
В	NC	NC	SA9	NC	SA8	NC	NC
С	NC	SA12	SA11	VDD	SA6	SA5	NC
D	DQb1	NC	Vss	ZQ	Vss	DQa9	NC
E	NC	DQb2	Vss	SS	Vss	NC	DQa8
F	VDDQ	NC	Vss	<u>G</u>	Vss	DQa7	VDDQ
G	NC	DQb3	SWb	፳	Vss	NC	DQa6
Н	DQb4	NC	Vss	С	Vss	DQa5	NC
J	VDDQ	VDD	VREF	VDD	VREF	VDD	VDDQ
K	NC	DQb5	Vss	K	Vss	NC	DQa4
L	DQb6	NC	Vss	ĸ	SWa	DQa3	NC
М	VDDQ	DQb7	Vss	SW	Vss	NC	VDDQ
N	DQb8	NC	Vss	SA16	Vss	DQa2	NC
Р	NC	DQb9	Vss	SA1	Vss	NC	DQa1
R	NC	SA15	M1	VDD	M2	SA ₂	NC
Т	NC	SA17	SA14	NC	SАз	SAo	ZZ
U	VDDQ	TMS	TDI	TCK	TDO	NC	VDDQ

FUNCTION DESCRIPTION

The KM736FV4011 and KM718FV4011 are 4,718,592 bit Synchronous Pipeline Mode SRAM. It is organized as 131,072 words of 36 bits(or 262, 144 words of 18 bits) and is implemented in SAMSUNG's advanced CMOS technology.

Single differential HSTL level K clocks are used to initiate the read/write operation and all internal operations are self-timed. At the rising edge of K clock, All addresses, Write Enables, Synchronous Select and Data Ins are registered internally. Data outs are updated from output registers edge of the next rising edge of the K clock. An internal write data buffer allows write data to follow one cycle after addresses and controls. The package is 119(7x17) Ball Grid Array with balls on a 1.27mm pitch.

Read Operation

During reads, the address is registered during the frist clock edge, the internal array is read between this first edge and the second edge, and data is captured in the output register and driven to the CPU during the second clock edge. SS is driven low during this cycle, signaling that the SRAM should drive out the data.

During consecutive read cycles where the address is the same, the data output must be held constant without any glitches. This characteristic is because the SRAM will be read by devices that will operate slower than the SRAM frequency and will require multiple SRAM cycles to perform a single read operation.

Write(Store) Operation

All addresses and \overline{SW} are sampled on the clock rising edge. \overline{SW} is low on the rising clock. Write data is sampled on the rising clock, one cycle after write address and \overline{SW} have been sampled by the SRAM. \overline{SS} will be driven low during the same cycle that the Address, \overline{SW} and \overline{SW} [a:d] are valid to signal that a valid operation is on the Address and Control Input.

Pipelined write are supported. This is done by using write data buffers on the SRAM that capture the write addresses on one write cycle, and write the array on the next write cycle. The "next write cycle" can actually be many cycles away, broken by a series of read cycles. Byte writes are supported. The byte write signals $\overline{SW}[a:d]$ signal which 9-bit bytes will be writen. Timing of $\overline{SW}[a:d]$ is the same as the \overline{SW} signal.

Bypass Read Operation

Since write data is not fully written into the array on first write cycle, there is a need to sense the address in case a future read is to be done from the location that has not been written yet. For this case, the address comparator check to see if the new read address is the same as the contents of the stored write address Latch. If the contents match, the read data must be supplied from the stored write data latch with standard read timing. If there is no match, the read data comes from the SRAM array. The bypassing of the SRAM array occurs on a byte by byte basis. If one byte is written and the other bytes are not, read data from the last written will have new byte data from the write data buffer and the other bytes from the SRAM array.

Low Power Dissipation Mode

During normal operation, asynchronous signal ZZ must be pulled low. Low Power Mode is enabled by switching ZZ high. When the SRAM is in Power Down Mode, the outputs will go to a Hi-Z state and the SRAM will draw standby current. SRAM data will be preserved and a recovery time(tZZR) is required before the SRAM resumes to normal operation.

TRUTH TABLE

К	ZZ	Ğ	SS	SW	SWa	SWb	SWc	SWd	DQa	DQb	DQc	DQd	Operation
Х	Н	Χ	Χ	Х	Х	Х	Χ	Х	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Power Down Mode. No Operation
Х	L	Н	Χ	Х	Х	Χ	Χ	Χ	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Output Disabled.
1	L	L	Н	Х	Χ	Χ	X	Χ	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Output Disabled. No Operation
1	L	L	L	Н	Χ	Х	Χ	Х	Dout	Dout	Dout	Dout	Read Cycle
1	L	L	L	L	Н	Н	H	Н	Hi-Z	Hi-Z	Hi-Z	Hi-Z	No Bytes Written
1	L	L	L	L	L	Н	Н	Н	Din	Hi-Z	Hi-Z	Hi-Z	Write first byte
1	L	L	L	L	Н	L	H	Н	Hi-Z	Din	Hi-Z	Hi-Z	Write second byte
1	٦	L	L	L	Н	Н	L	Н	Hi-Z	Hi-Z	Din	Hi-Z	Write third byte
1	L	L	L	L	H	Н	Н	L	Hi-Z	Hi-Z	Hi-Z	DIN	Write fourth byte
1	L	L	L	L		L	L	L	Din	Din	Din	Din	Write all byte



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Core Supply Voltage Relative to Vss	VDD	-0.5 to 4.6	V
Output Supply Voltage Relative to Vss	VDDQ	-0.5 to 4.6	V
Voltage on any I/O pin Relative to Vss	VTERM	-0.5 to VDDQ+0.5	V
Maximum Power Dissipation	PD	2.5	W
Output Short-Circuit Current	lout	25	mA
Operating Temperature	Topr	0 to 70	°C
Storage Temperature	Тѕтс	-65 to 125	°C

NOTE: Stresses greater than those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Тур	Max	Unit	Note
Core Power Supply Voltage	VDD	3.15	3.3	3.45	٧	
Output Power Supply Voltage	VDDQ	1.4	1.5	1.6	V	
Input High Level	ViH	VREF+0.1	-	VDDQ + 0.3	V	1, 2
Input Low Level	VIL	-0.3		VREF - 0.1	٧	1, 3
Input Reference Voltage	VREF	VDDQ/2	-	2Vppq/3	٧	1
Clock Input Signal Voltage	VIN-CLK	-0.3	-	VDDQ + 0.3	٧	1
Clock Input Differential Voltage	VDIF-CLK	0.1	-	VDDQ + 0.6	٧	1
Clock Input Common Mode Voltage	Vcm-CLK	VDDQ/2	-	2Vppq/3	٧	1
Operating Junction Temperature	TJ	10	-	110	င	4

- NOTE:1. These are DC VIH/VIH spec. The AC VIH/VIL levels are defined separately for measuring timing parameters.
 - 2. VIH (Max)DC = VDD+0.3V, VIH (Max)AC = VDD+1.5V(pulse width ≤ 5ns).
 - 3. VIL (Min)DC = -0.3V, VIL (Min)AC =-1.5V(pulse width \leq 5ns).
 - 4. Junction temperature is a function of on-chip power dissipation, package thermal impedance, mounting site temperature and mounting site thermal impedance. TJ = TA + PD x THETA_JA

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit	Note
Average Power Supply Operating Current-x36 (VIN=VIH or VIL, ZZ & SS=VIL)	ldd	-	700	mA	1
Average Power Supply Operating Current-x18 (VIN=VIH or VIL, ZZ & SS=VIL)	loo	-	650	mA	1
Power Supply Standby Current (VIN=VIH or VIL, ZZ =VIH)	ISB	-	100	mA	1
Input Leakage Current (VIN=Vss or VDD)	lu	-1	1	μА	
Output Leakage Current (Vout=Vss or Vdd, ZZ =ViH)	llo	-5	5	μА	
Output High Voltage(IoH=-2mA)	Voн	VDDQ/2+0.3	VDDQ	V	
Output Low Voltage(IoL=2mA)	Vol	Vss	VDDQ/2+0.3	٧	

NOTE: 1. Minimum cycle. IOUT=0mA.



PIN CAPACITANCE

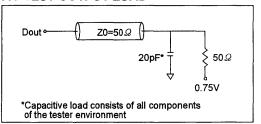
Parameter	Symbol	Pin Name	Min	Тур	Max	Unit
Input Capacitance	Cin	K, K, SS, SW, G, ZZ SWx, ZQ, M1, M2, SAn, TCK, TMS, TDI	3	4	5	pF
Output Capacitance	Cout	DQn, TDO	5	6	7	pF

NOTE: Periodically sampled and 100% tested.(dV=0V, f=1MHz)

AC TEST CONDITIONS

Paramete r	Symbol	Value	Unit
Input High/Low Level	VIH/VIL	1.5/0.0	٧
Input Reference Level	VREF	0.75	٧
Input Rise/Fall Time	TR/TF	1.0/1.0	ns
Output Rise/Fall Time	TR/TF	0.5~1.0	ns
Input and Out Timing Reference Level		0.75	٧
Clock Input Timing Reference Level	1	Cross Point	٧

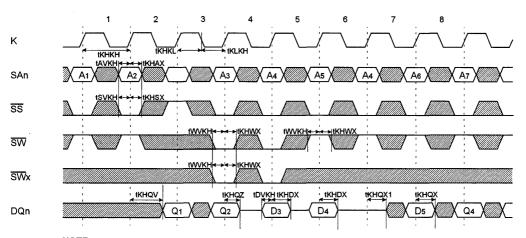
AC TEST OUTPUT LOAD



AC CHARACTERISTICS

Parameter	Symbol		-5		6	-7		Unit	Note
rarameter	Symbol	Min	Max	Min	Max	Min	Max		Note
Clock Cycle Time	tKHKH	5.0	-	6.0	-	7.0	-	ns	
Clock High Pulse Width	tKHKL	2.0	-	2.4	-	2.8	-	ns	
Clock Low Pulse Width	tKLKH	2.0	-	2.4	-	2.8	-	ns	
Clock High to Output Valid	tKHQV	-	2.5	-	3.0		3.5	ns	
Clock High to Output Hold	tKHQX	1.0	-	1.0	-	1.0	-	ns	
Address Setup Time	tAVKH	0.5	-	0.5	-	0.5	-	ns	
Address Hold Time	tKHAX	1.0	-	1.0	-	1.0	-	ns	
Write Data Setup Time	tDVKH	0.5	-	0.5	-	0.5	-	ns	
Write Data Hold Time	tKHDX	1.0	-	1.0	-	1.0	-	ns	
SW, SW[a:d] Setup Time	tWVKH	0.5	-	0.5	-	0.5	-	ns	
SW, SW[a:d] Hold Time	tKHWX	1.0	-	1.0	-	1.0	-	ns	
SS Setup Time	tsvkh	0.5	-	0.5	-	0.5	-	ns	
SS Hold Time	tKHSX	1.0	-	1.0	-	1.0	-	ns	
Clock High to Output Hi-Z	tKHQZ	-	2.5	-	3.0	-	3.5	ns	
Clock High to Output Low-Z	tKHQX1	1.0	-	1.0	-	1.0	-	ns	
G High to Output High-Z	tGHQZ	-	2.5	-	3.0	-	3.5	ns	
G Low to Output Low-Z	tGLQX	0.5		0.5	_	0.5		ns	
G Low to Output Valid	tGLQV	-	2.5	-	3.0	_	3.5	ns	
ZZ High to Power Down(Sleep Time)	tZZE	-	5.0	-	6.0		7.0	ns	
ZZ Low to Recovery(Wake-up Time)	tZZR	-	5.0	-	6.0	-	7.0	ns	

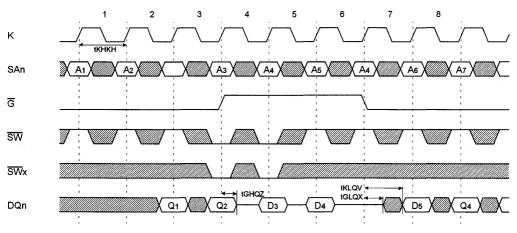
TIMING WAVEFORMS OF NORMAL ACTIVE CYCLES(SS Controlled, G=Low)



NOTE:

- 1. D3 is the input data written in memory location A3.
- Q4 is the output data read from the write data buffer(not from the cell array), as a result of address A4 being a match from the last write cycle address.

TIMING WAVEFORMS OF NORMAL ACTIVE CYCLES(G Controlled, SS=Low)

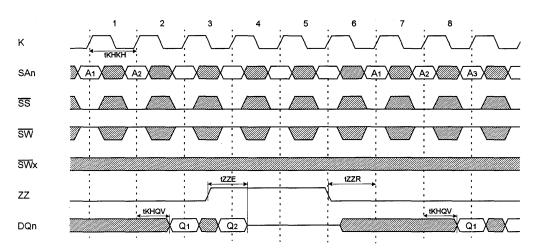


NOTE:

- 1. D3 is the input data written in memory location A3.
- Q4 is the output data read from the write data buffer(not from the cell array), as a result of address A4 being a match from the last write cycle address.



TIMING WAVEFORMS OF STANDBY CYCLES



PROGRAMMABLE IMPEDANCE OUTPUT BUFFER OPERATION

The designer can program the SRAM's output buffer impedance by terminating the ZQ pin to Vss through a precision resistor(RQ). The value of RQ is five times the output impedance desired. For example, $250\mathcal{Q}$ resistor will give an output impedance of $50\mathcal{Q}$. The allowable range of RQ to guarantee impedance matching with a tolerance of 7.5% is between $175\mathcal{Q}$ and $350\mathcal{Q}$. Impedance updates occur early in cycles that do not activate the outputs, such as deselect cycles. They may also occur in cycles initiated with \overline{G} high. In all cases impedance updates are transparent to the user and do not produce access time "push-outs" or other anomalous behavior in the SRAM. Periodic readjustment is necessary as the impedance is greatly affected by drifts in supply voltage and temperature. Impedance updates occur no more often than every 32 clock cycles. Clock cycles are counted whether the SRAM is selected or not and proceed regardless of the type of cycle being executed. Therefore, the user can be assured that after 33 continuous read cycles have occurred, an impedance update will occur the next time \overline{SS} or \overline{G} are high at a rising edge of the K clock. There are no power up requirements for the SRAM. However, to guarantee optimum output driver impedance after power up, the SRAM needs 1024 non-read cycles.

DC Electrical Characteristics

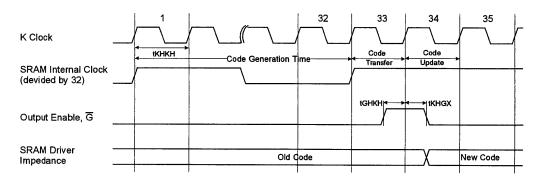
Parameter	Symbol	Min	Тур	Max	Unit	Note
Impedance Control Resistor Range	RQ	175	250	350	Ω	-
Driver Impedance	ZD	RQ/5-7.5%	-	RQ/5+7.5%	Ω	1

NOTE: 1. Measured at VouT=VDDq/2. louT=(VDDq/2)/(RQ/5) ± 7.5% @VouT=VDDq/2.

AC Electrical Characteristics

Parameter	Symbol	Min	Тур	Max	Unit	Note
Output Impedance Update G Setup Time	tGHKH	0.5	-	•	ns	-
Output Impedance Update G Hold Time	tKHGX	1.0	-	-	ns	-

TIMING WAVEFORMS OF Driver Impedance Update Control

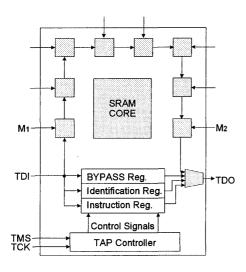




IEEE 1149.1 TEST ACCESS PORT AND BOUNDARY SCAN-JTAG

This part contains an IEEE standard 1149.1 Compatible Teat Access Port(TAP). The package pads are monitored by the Serial Scan circuitry when in test mode. This is to support connectivity testing during manufacturing and system diagnostics. Internal data is not driven out of the SRAM under JTAG control. In conformance with IEEE 1149.1, the SRAM contains a TAP controller, Instruction Register, Bypass Register and ID register. The TAP controller has a standard 16-state machine that resets internally upon power-up, therefore, TRST signal is not required. It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfacing with normal operation of the SRAM, TCK must be tied to Vss to preclude mid level input. TMS and TDI are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to Vpb through a resistor. TDO should be left unconnected.

JTAG Block Diagram



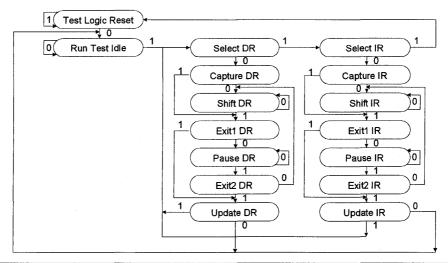
JTAG Instruction Coding

IR2	IR1	IRO	Instruction	TDO Output	Notes
0	0	0	SAMPLE-Z	Boundary Scan Register	1
0	0	1	IDCODE	Identification Register	2
0	1	0	SAMPLE-Z	Boundary Scan Register	1
0	1	1	BYPASS	Bypass Register	3
1	0	0	SAMPLE	Boundary Scan Register	4
1	0	1	BYPASS	Bypass Register	3
1	1	0	BYPASS	Bypass Register	3
1	1	1	BYPASS	Bypass Register	3

NOTE:

- Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs.
- TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
- Bypass register is initiated to Vss when BYPASS instruction is invoked. The Bypass Register also holds serially loaded TDI when exiting the Shift DR states.
- 4. SAMPLE instruction dose not places DQs in Hi-Z.

TAP Controller State Diagram





SCAN REGISTER DEFINITION

Part	Instruction Register	Bypass Register	ID Register	Boundary Scan
128Kx36	3 bits	1 bits	32 bits	70 bits
256Kx18	3 bits	1 bits	32 bits	51 bits

ID REGISTER DEFINITION

Part	Revision Number (31:28)	Part Configuration (27:18)	Vendor Definition (17:12)	Samsung JEDEC Code (11: 1)	Start Bit(0)
128Kx36	0000	00101 00100	000000	00001001110	1
256Kx18	0000	00110 00011	000000	00001001110	1

BOUN	DARY	SCAN	EXIT (ORDER	k(x36)	
36	3B	SA9		SA8	5B	35
37	2B	NC		NC	6B	34
38	3A	SA10		SA7	5A	33
39	3C	SA ₁₁		SA6	5C	32
40	2C	SA12		SA ₅	6C	31
41	2A	SA13		SA4	6A	30
42	2D	DQc9		DQb9	6D	29
43	1D	DQc8		DQb8	7D	28
44	2E	DQc7		DQb7	6E	27
45	1E	DQc6		DQb6	7E	26
46	2F	DQc5		DQb5	6F	25
47	2G	DQc4		DQb4	6G	24
48	1G	DQc3		DQb3	7G	23
49	2H	DQc2		DQb2	6H	22
50	1H	DQc1		DQb1	7H	21
51	3G	SWc		SWb	5G	20
52	4D	ZQ		G	4F	19
53	4E	SS		К	4K	18
54	4G	<u>c</u>		ĸ	4L	17
55	4H	С		SWa	5L	16
56	4M	SW		DQa1	7K	15
57	3L	SWd		DQa2	6K	14
58	1K	DQd1		DQa3	7L	13
59	2K	DQd2		DQa4	6L	12
60	1L	DQd3		DQa5	6M	11
61	2L	DQd4		DQa6	_7N	10
62	2 M	DQd5		DQa7	6N	9
63	1N	DQd6		DQa8	7P	8
64	2N	DQd7		DQa9	6P	7
65	1P	DQd8		ZZ	7T	6
66	2P	DQd9		SA3	5T	5
67	3T	SA14		SA ₂	6R	4
68	2R	SA15		SA1	4T	3
69	4N	SA16		SA ₀	4P	2
70	3R	M1		M2	5R	1

BOUNDARY SCAN EXIT ORDER(x18)

26 3B SA9 SA8 5B 27 2B NC NC 6B 28 3A SA10 SA7 5A 29 3C SA11 SA6 5C 30 2C SA12 SA5 6C 31 2A SA13 SA4 6A DQa9 6D DQa9 6D 32 1D DQb1 DQa8 7E DQa7 6F DQa7 6F	25 24 23 22 21 20 19 18 17
28 3A SA10 SA7 5A 29 3C SA11 SA6 5C 30 2C SA12 SA5 6C 31 2A SA13 SA4 6A DQa9 6D 32 1D DQb1 33 2E DQb2 DQa7 6F	23 22 21 20 19 18 17
29 3C SA11 SA6 5C 30 2C SA12 SA5 6C 31 2A SA13 SA4 6A DQa9 6D 32 1D DQb1 33 2E DQb2 DQa8 7E DQa7 6F	22 21 20 19 18 17
30 2C SA12 SA5 6C 31 2A SA13 SA4 6A DQa9 6D 32 1D DQb1 33 2E DQb2 DQa8 7E DQa7 6F	21 20 19 18 17
31 2A SA13 SA4 6A DQa9 6D 32 1D DQb1 33 2E DQb2 DQa8 7E DQa7 6F	20 19 18 17
DQa9 6D	19 18 17
32 1D DQb1 33 2E DQb2 DQa8 7E DQa7 6F	18 17
33 2E DQb2 DQa8 7E DQa7 6F	17 16
DQa8 7E DQa7 6F	17 16
DQa7 6F	17 16
	16
34 2G DQb3	
DQa6 7G	
DQa5 6H	15
35 1H DQb4	
36 3G SWb	
37 4D ZQ G 4F	14
38 4E SS K 4K	13
39 4G C K 4L	12
40 4H C SWa 5L	11
41 4M SW DQa4 7K	10
42 2K DQb5 DQa3 6L	9
43 1L DQb6	
44 2M DQb7 DQa2 6N	8
45 1N DQb8 DQa1 7P	7
ZZ 7T	6
46 2P DQb9 SA3 5T	5
47 3T SA14 SA2 6R	4
48 2R SA15	
49 4N SA16 SA1 4P	3
50 2T SA17 SA0 6T	2
51 3R M1 M2 5R	1

NOTE: 1. Pins 6B and 2B are no connection pin to internal chip. These pins are place holders for 16M part and the scanned data are fixed to "0" for this 4M parts.



JTAG DC OPERATING CONDITIONS

Parameter	Symbol	Min	Тур	Max	Unit	Note
Power Supply Voltage	VDD	3.15	3.3	3.45	V	
Input High Level	ViH	2.0	-	Vpp+0.3	V	
Input Low Level	VIL	-0.3	-	0.8	V	
Output High Voltage(IoH=-2mA)	Voн	2.4	-	VDD	V	
Output Low Voltage(IoL=2mA)	Vol	Vss	-	0.4	V	

NOTE: 1. The input level of SRAM pin is to follow the SRAM DC specification.

JTAG AC TEST CONDITIONS

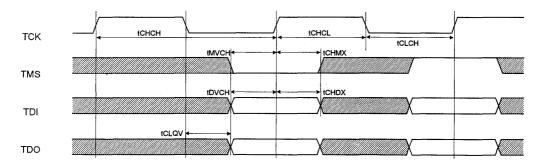
Parameter	Symbol	Min	Unit	Note
Input High/Low Level	VIH/VIL	3.0/0.0	V	
Input Rise/Fall Time	TR/TF	2.0/2.0	ns	
Input and Output Timing Reference Level		1.5	V	1

NOTE: 1. See SRAM AC test output load on page 5.

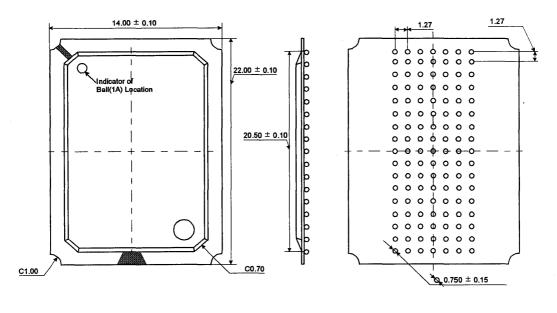
JTAG AC Characteristics

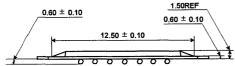
Parameter	Symbol	Mîn	Max	Unit	Note
TCK Cycle Time	tCHCH	50	-	ns	
TCK High Pulse Width	tCHCL	20	-	ns	
TCK Low Pulse Width	tCLCH	20	-	ns	
TMS Input Setup Time	tMVCH	5	-	ns	
TMS Input Hold Time	tCHMX	5	-	ns	
TDI Input Setup Time	tDVCH	5	-	ns	
TDI Input Hold Time	tCHDX	5	-	ns	
Clock Low to Output Valid	tCLQV	0	10	ns	

JTAG TIMING DIAGRAM



119 BGA PACKAGE DIMENSIONS





NOTE:

- 1. All Dimensions are in Millimeters.
- 2. Solder Ball to PCB Offset: 0.10 MAX.
- 3. PCB to Cavity Offset: 0.10 MAX.

119 BGA PACKAGE THERMAL CHARACTERISTICS

Parameter	Symbol	Min	Тур	Max	Unit	Note
Junction to Ambient(at still air)	Theta_JA	-	-	50	°€W	
Junction to Ambient(at air flow of 100 LFPM)	Theta_JA	-	-	40	°CW0	
Junction to Case	Theta_JC	-	-	8	°CW	
Junction to Solder Ball	Theta_JB	-	-	10	.cw	

NOTE: 1. Junction temperature can be calculated by: TJ = TA + PD x Theta_JA.



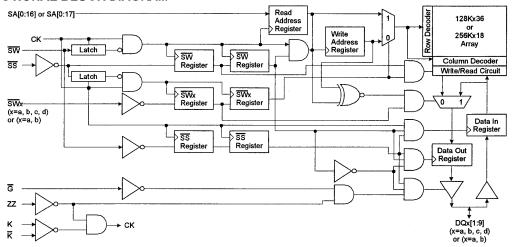
128Kx36 & 256Kx18 Synchronous Pipelined SRAM FEATURES

- 128Kx36 or 256Kx18 Organizations.
- . 3.3V Core/ Output Power Supply.
- LVTTL 3.3V Input and Output Levels.
- Differential, PECL Clock Inputs K, K.
- . Synchronous Read and Write Operation
- · Registered Input and Registered Output
- Internal Pipeline Latches to Support Late Write.
- Byte Write Capability(four byte write selects, one for each 9 bits)
- . Synchronous or Asynchronous Output Enable.
- · Power Down Mode via ZZ Signal.

- JTAG 1149.1 Compatible Test Access port.
- 119(7x17) Pin Ball Grid Array Package(14mm x 22mm).

Organization	Part Number	Cycle Time	Access Time
	KM736FV4021H-5	5	2.5
128Kx36	KM736FV4021H-6	6	3.0
	KM736FV4021H-7	7	3.5
256Kx18	KM718FV4021H-5	5	2.5
	KM718FV4021H-6	6	3.0
	KM718FV4021H-7	7	3.5

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

Pin Name	Pin Description	Pin Name	Pin Description
K, K	Differential Clocks	c, c	Differential Output Clocks
SAn	Synchronous Address Input	M1, M2	Read Protocol Mode Pins
DQn	Bi-directional Data Bus	G	Asynchronous Output Enable
SW	Synchronous Grobal Write Enable	SS	Synchronous Select
SWa	Synchronous Byte a Write Enable	тск	JTAG Test Clock
≅₩b	Synchronous Byte b Write Enable	TMS	JTAG Test Mode Select
S₩c	Synchronous Byte c Write Enable	TDI	JTAG Test Data Input
≅Wd	Synchronous Byte d Write Enable	TDO	JTAG Test Data Output
ZZ	Asynchronous Power Down	ZQ	Output Driver Impedance Control Input HSTL Level
VDD	Core Power Supply	Vss	GND
VDDQ	Output Power Supply	NC	No Connection
VREF	HSTL Input Reference Voltage		

NOTE: 1. This SRAM only supports single clock, register-register read protocol and have fixed impedance output driver.

Therefore the following inputs must be set with power up and must not change during SRAM operation;

C=VDD, C=Vss, M1=Vss, M2=VDD, ZQ=VDD and VREF=VDD. But they are also designed to operate being left floating.



PACKAGE PIN CONFIGURATIONS (TOP VIEW)

KM736FV4021(128Kx36)

	1	2	3	4	5	6	7
Α	VDDQ	SA13	SA10	NC	SA7	SA4	VDDQ
В	NC	NC	SA9	NC	SA8	NC	NC
С	NC	SA12	SA11	VDD	SA6	SA5	NC
D	DQc8	DQc9	Vss	ZQ	Vss	DQb9	DQb8
E	DQc6	DQc7	Vss	SS	Vss	DQb7	DQb6
F	VDDQ	DQc5	Vss	ĪG	Vss	DQb5	VDDQ
G	DQc3	DQc4	SWc	ਟ	≅₩b	DQb4	DQb3
Н	DQc1	DQc2	Vss	С	Vss	DQb2	DQb1
J	VDDQ	VDD	VREF	Voo	VREF	VDD	VDDQ
K	DQd1	DQd2	Vss	K	Vss	DQa2	DQa1
L	DQd3	DQd4	SWd	ĸ	SWa	DQa4	DQa3
М	VDDQ	DQd5	Vss	SW	Vss	DQa5	VDDQ
N	DQd6	DQd7	Vss	SA16	Vss	DQa7	DQa6
Р	DQd8	DQd9	Vss	SAo	Vss	DQa9	DQa8
R	NC	SA15	M1	VDD	M2	SA2	NC
Т	NC	NC	SA14	SA ₁	SA ₃	NCNC	ZZ
U	VDDQ	TMS	TDI	TCK	TDO	NC	VDDQ

KM718FV4021(256Kx18)

	1	2	3	4	5	6	7
Α	VDDQ	SA13	SA10	NC	SA7	SA4	VDDQ
В	NC	NC	SA9	NC	SA8	NC	NC
С	NC	SA12	SA11	VDD	SA ₆	SA5	NC
D	DQb1	NC	Vss	ZQ	Vss	DQa9	NC
E	NC	DQb2	Vss	SS	Vss	NC	DQa8
F	VDDQ	NC	Vss	Ğ	Vss	DQa7	VDDQ
G	NC	DQb3	SWb	ਟ	Vss	NC	DQa6
Н	DQb4	NC	Vss	С	Vss	DQa5	NC
J	VDDQ	VDD	VREF	VDĐ	VREF	VDD	VDDQ
K	NC	DQb5	Vss	K	Vss	NC	DQa4
LL	DQb6	NC	Vss	₹	SWa	DQa3	NC
М	VDDQ	DQb7	Vss	SW	Vss	NC	VDDQ
N	DQb8	NC	Vss	SA16	Vss	DQa2	NC
Р	NC	DQb9	Vss	SA1	Vss	NC	DQa1
R	NC	SA15	M1	DaV	M2	SA2	NC
Т	NC	SA17	SA14	NC	SA3	SA ₀	ZZ
U	VDDQ	TMS	TDI	TCK	TDO	NC	VDDQ

FUNCTION DESCRIPTION

The KM736FV4021 and KM718FV4011 are 4,718,592 bit Synchronous Pipeline Mode SRAM. It is organized as 131,072 words of 36 bits(or 262, 144 words of 18 bits) and is implemented in SAMSUNG's advanced CMOS technology.

Single differential PECL level K clocks are used to initiate the read/write operation and all internal operations are self-timed. At the rising edge of K clock, All addresses, Write Enables, Synchronous Select and Data Ins are registered internally. Data outs are updated from output registers edge of the next rising edge of the K clock. An internal write data buffer allows write data to follow one cycle after addresses and controls. The package is 119(7x17) Ball Grid Array with balls on a 1.27mm pitch.

Read Operation

During reads, the address is registered during the frist clock edge, the internal array is read between this first edge and the second edge, and data is captured in the output register and driven to the CPU during the second clock edge. SS is driven low during this cycle, signaling that the SRAM should drive out the data.

During consecutive read cycles where the address is the same, the data output must be held constant without any glitches. This characteristic is because the SRAM will be read by devices that will operate slower than the SRAM frequency and will require multiple SRAM cycles to perform a single read operation.

Write(Store) Operation

All addresses and \overline{SW} are sampled on the clock rising edge. \overline{SW} is low on the rising clock. Write data is sampled on the rising clock, one cycle after write address and \overline{SW} have been sampled by the SRAM. \overline{SS} will be driven low during the same cycle that the Address, \overline{SW} and \overline{SW} [a:d] are valid to signal that a valid operation is on the Address and Control Input.

Pipelined write are supported. This is done by using write data buffers on the SRAM that capture the write addresses on one write cycle, and write the array on the next write cycle. The "next write cycle" can actually be many cycles away, broken by a series of read cycles. Byte writes are supported. The byte write signals $\overline{SW}[a:d]$ signal which 9-bit bytes will be writen. Timing of $\overline{SW}[a:d]$ is the same as the \overline{SW} signal.

Bypass Read Operation

Since write data is not fully written into the array on first write cycle, there is a need to sense the address in case a future read is to be done from the location that has not been written yet. For this case, the address comparator check to see if the new read address is the same as the contents of the stored write address Latch. If the contents match, the read data must be supplied from the stored write data latch with standard read timing. If there is no match, the read data comes from the SRAM array. The bypassing of the SRAM array occurs on a byte by byte basis. If one byte is written and the other bytes are not, read data from the last written will have new byte data from the write data buffer and the other bytes from the SRAM array.

Low Power Dissipation Mode

During normal operation, asynchronous signal ZZ must be pulled low. Low Power Mode is enabled by switching ZZ high. When the SRAM is in Power Down Mode, the outputs will go to a Hi-Z state and the SRAM will draw standby current. SRAM data will be preserved and a recovery time(tZZR) is required before the SRAM resumes to normal operation.

TRUTH TABLE

К	ZZ	Ğ	SS	sw	SWa	SWb	SWc	SWd	DQa	DQb	DQc	DQd	Operation
Χ	Н.	Х	Х	Х	Х	Х	Х	Х	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Power Down Mode. No Operation
Χ	L	Н	Х	Х	Х	Х	Х	Х	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Output Disabled.
1	L	L	Н	Х	Х	Χ	Х	Х	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Output Disabled. No Operation
1	L	L	L	Н	Х	Х	Х	Х	Dout	Dout	Dout	Dout	Read Cycle
1	L	L	L	L	Н	Н	Н	Н	Hi-Z	Hi-Z	Hi-Z	Hi-Z	No Bytes Written
1	L	L	L	L	L	Н	Н	Ĥ	DIN	Hi-Z	Hi-Z	Hi-Z	Write first byte
1	L	L	L.	L	Н	L	Н	Н	Hi-Z	Din	Hi-Z	Hi-Z	Write second byte
1	L	L	L	L	Н	Н	L	Η	Hi-Z	Hi-Z	Din	Hi-Z	Write third byte
1	L	L	L	L	Н	Н	Η	L	Hi-Z	Hi-Z	Hi-Z	Din	Write fourth byte
1	L	L	L	L	L	L	L	L	Din	Din	Din	Din	Write all byte



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Core Supply Voltage Relative to Vss	VDD	-0.5 to 4.6	V
Output Supply Voltage Relative to Vss	VDDQ	-0.5 to 4.6	V
Voltage on any I/O pin Relative to Vss	VTERM	-0.5 to VDDQ+0.5	٧
Maximum Power Dissipation	PD	2.5	W
Output Short-Circuit Current	lout	25	mA
Operating Temperature	TOPR	0 to 70	C
Storage Temperature	Тѕтҫ	-65 to 125	°C

NOTE: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Тур	Max	Unit	Note
Core Power Supply Voltage	VDD	3.15	3.3	3.45	٧	
Output Power Supply Voltage	VDDQ	3.15	3.3	3.45	٧	
Input High Level	ViH	2.0	-	VDD + 0.3	V	1, 2
Input Low Level	VIL	-0.3	-	0.8	V	1, 3
PECL Clock Input High Level	VIH-PECL	2.135	-	2.420	V	1
PECL Clock Input Low Level	VIL-PECL	1.490	-	1.825	٧	.1
Operating Junction Temperature	TJ	10	-	110	°C	4

- NOTE: 1. These are DC VIH/VIH spec. The AC VIH/VIL levels are defined separately for measuring timing parameters.
 - 2. VIH (Max)DC = VDD+0.3V, VIH (Max)AC = VDD+1.5V(pulse width ≤ 5ns).
 - 3. VIL (Min)DC = -0.3V, VIL (Min)AC =-1.5V(pulse width \leq 5ns).
 - 4. Junction temperature is a function of on-chip power dissipation, package thermal impedance, mounting site temperature and mounting site thermal impedance. TJ = TA + PD x THETA_JA

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit	Note
Average Power Supply Operating Current-x36 (VIN=VIH or VIL, ZZ & SS=VIL)	IDD	-	700	mA	1
Average Power Supply Operating Current-x18 (VIN=VIH or VIL, ZZ & SS=VIL)	IDD	-	650	mÄ	1
Power Supply Standby Current (VIN=VIH or VIL, ZZ =VIH)	ISB		100	mA	1,
Input Leakage Current (VIN=Vss or VDD)	lu	-1	1	μА	
Output Leakage Current (Vouт=Vss or Vpd, ZZ =Viн)	ILO	-5	5	μА	
Output High Voltage(IOH=-2mA)	Voн	2.4	VDDQ	V	
Output Low Voltage(IoL=2mA)	VoL	Vss	0.4	V	

NOTE: 1. Minimum cycle. IOUT=0mA.



PIN CAPACITANCE

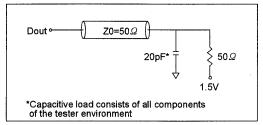
Parameter	Symbol	Pin Name	Min	Тур	Max	Unit
Input Capacitance	CIN	K, \overline{K} , \overline{SS} , \overline{SW} , \overline{G} , ZZ \overline{SW} x, ZQ, M1, M2, SAn, TCK, TMS, TDI	3	4	5	рF
Output Capacitance	Соит	DQn, TDO	5	6	7	рF

NOTE: Periodically sampled and 100% tested.(dV=0V, f=1MHz)

AC TEST CONDITIONS

Parameter	Symbol	Value	Unit
Input High/Low Level	VIH/VIL	3.0/0.0	>
Clock Input High/Low Level(PECL)	VIH/VIL	2.4/1.5	٧
Input Rise/Fall Time	TR/TF	1.0/1.0	ns
Clock Input Rise/Fall Time(PECL)	TR/TF	0.5/0.5	ns
Output Rise/Fall Time	TR/TF	0.5~1.0	ns
Input and Out Timing Reference Level		1.5	>
Clock Input Timing Reference Level		Cross Point	>

AC TEST OUTPUT LOAD

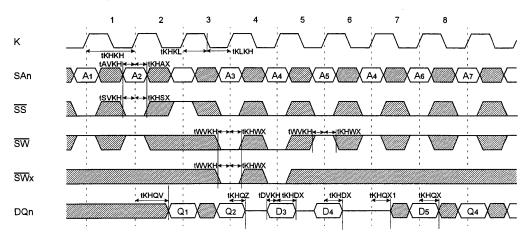


AC CHARACTERISTICS

Parameter	Symbol	-5		-6			-7	Unit	Note
raiailletei	Symbol	Min	Max	Min	Max	Min	Max	Onic	Note
Clock Cycle Time	tKHKH	5.0	-	6.0	-	7.0	-	ns	
Clock High Pulse Width	tKHKL	2.0	-	2.4	-	2.8	-	ns	
Clock Low Pulse Width	tKLKH	2.0	-	2.4	-	2.8	-	ns	
Clock High to Output Valid	tKHQV	-	2.5	-	3.0	-	3.5	ns	
Clock High to Output Hold	tKHQX	1.0	-	1.0	-	1.0	-	ns	
Address Setup Time	tAVKH	0.5	_	0.5	-	0.5	-	ns	
Address Hold Time	tKHAX	1.0	-	1.0	-	1.0	-	ns	
Write Data Setup Time	tDVKH	0.5	-	0.5	-	0.5	-	ns	
Write Data Hold Time	tKHDX	1.0	-	1.0	-	1.0	-	ns	
SW, SW[a:d] Setup Time	tWVKH	0.5	-	0.5	-	0.5	-	ns	
SW, SW[a:d] Hold Time	tKHWX	1.0	-	1.0	-	1.0	-	ns	
SS Setup Time	tSVKH	0.5	-	0.5	-	0.5	-	ns	
SS Hold Time	tKHSX	1.0	-	1.0	-	1.0	-	ns	
Clock High to Output Hi-Z	tKHQZ	-	2.5	-	3.0	-	3.5	ns	
Clock High to Output Low-Z	tKHQX1	1.0	-	1.0	-	1.0	-	ns	
G High to Output High-Z	tGHQZ	-	2.5	-	3.0	-	3.5	ns	
G Low to Output Low-Z	tGLQX	0.5	-	0.5	-	0.5	-	ns	
G Low to Output Valid	tGLQV	-	2.5	-	3.0	-	3.5	ns	
ZZ High to Power Down(Sleep Time)	tZZE	-	5.0	-	6.0	-	7.0	ns	
ZZ Low to Recovery(Wake-up Time)	tZZR	-	5.0	-	6.0	-	7.0	ns	



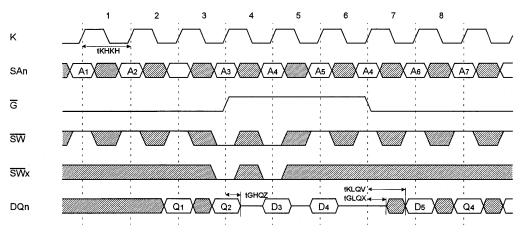
TIMING WAVEFORMS OF NORMAL ACTIVE CYCLES(\$\overline{SS}\$ Controlled, \$\overline{G}=Low\$)



NOTE:

- 1. D3 is the input data written in memory location A3.
- Q4 is the output data read from the write data buffer(not from the cell array), as a result of address A4 being a match from the last write cycle address.

TIMING WAVEFORMS OF NORMAL ACTIVE CYCLES(G Controlled, SS=Low)

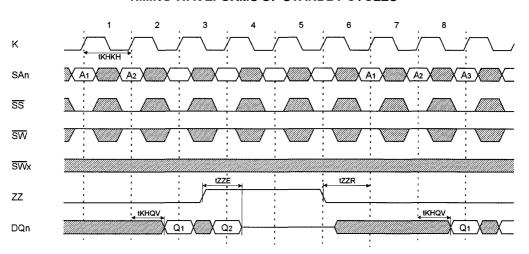


NOTE:

- 1. D3 is the input data written in memory location A3.
- Q4 is the output data read from the write data buffer(not from the cell array), as a result of address A4 being a match from the last write cycle address.



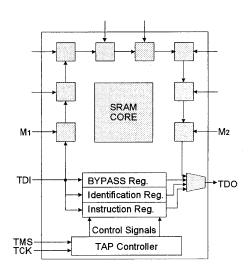
TIMING WAVEFORMS OF STANDBY CYCLES



IEEE 1149.1 TEST ACCESS PORT AND BOUNDARY SCAN-JTAG

This part contains an IEEE standard 1149.1 Compatible Teat Access Port(TAP). The package pads are monitored by the Serial Scan circuitry when in test mode. This is to support connectivity testing during manufacturing and system diagnostics. Internal data is not driven out of the SRAM under JTAG control. In conformance with IEEE 1149.1, the SRAM contains a TAP controller, Instruction Register, Bypass Register and ID register. The TAP controller has a standard 16-state machine that resets internally upon power-up, therefore, TRST signal is not required. It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfacing with normal operation of the SRAM, TCK must be tied to Vss to preclude mid level input. TMS and TDI are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to Vpp through a resistor. TDO should be left unconnected.

JTAG Block Diagram



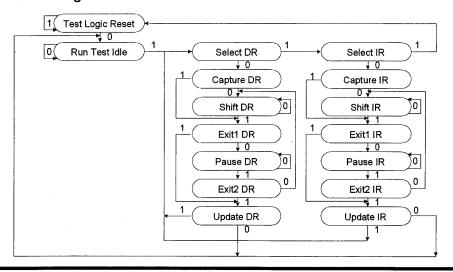
JTAG Instruction Coding

IR2	IR1	IR0	Instruction	TDO Output	Notes
0	0	0	SAMPLE-Z	Boundary Scan Register	1
0	0	1	IDCODE	OCODE Identification Register	
0	1	0	SAMPLE-Z	E-Z Boundary Scan Register	
0	1	1	BYPASS	Bypass Register	3
1	0	0	SAMPLE	Boundary Scan Register	4
1	0	1	BYPASS	Bypass Register	3
1	1	0	BYPASS	Bypass Register	3
1	1	1	BYPASS	Bypass Register	3

NOTE:

- Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs.
- TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
- Bypass register is initiated to Vss when BYPASS instruction is invoked. The Bypass Register also holds serially loaded TDI when exiting the Shift DR states.
- 4. SAMPLE instruction dose not places DQs in Hi-Z.

TAP Controller State Diagram





SCAN REGISTER DEFINITION

Part	Instruction Register	Bypass Register	ID Register	Boundary Scan
128Kx36	3 bits	1 bits	32 bits	70 bits
256Kx18	3 bits	1 bits	32 bits	51 bits

ID REGISTER DEFINITION

Part	Revision Number (31:28)	Part Configuration (27:18)	Vendor Definition (17:12)	Samsung JEDEC Code (11: 1)	Start Bit(0)
128Kx36	0000	00101 00100	000000	00001001110	1
256Kx18	0000	00110 00011	000000	00001001110	11

BOUNDARY SCAN EXIT ORDER(x36)

BOUNDARY SCAN EXIT ORDER(x36)						
36	3B	SA9		SAs	5B	35
37	2B	NC		NC	6B	34
38	3A	SA10		SA ₇	5A	33
39	_3C	SA11		SA ₆	5C	32
40	2C	SA12		SA ₅	6C	31
41	2A	SA13		SA4	6A	30
42	2D	DQc9		DQb9	6D	29
43	1D	DQc8		DQb8	7D	28
44	2E	DQc7		DQb7	6E	27
45	1E	DQc6		DQb6	7E	26
46	2F	DQc5		DQb5	6F	25
47	2G	DQc4		DQb4	6G	24
48	1G	DQc3		DQb3	7G	23
49	2H	DQc2		DQb2	6H	22
50	1H	DQc1		DQb1	7H	21
51	3G	SWc		SWb	5G	20
52	4D	ZQ		G	4F	19
53	4E	SS		K	4K	18
54	4G	C		ĸ	4L	17
55	4H	С		SWa	5L	16
56	4M	SW		DQa1	7K	15
57	3L	SWd		DQa2	6K	14
58	1K	DQd1		DQa3	7L	13
59	2K	DQd2		DQa4	6L	12
60	1L	DQd3		DQa5	6M	11
61	2L	DQd4		DQa6	7N	10
62	2M	DQd5		DQa7	6N	9
63	1N	DQd6		DQa8	7P	8
64	2N	DQd7		DQa9	6P	7
65	1P	DQd8		ZZ	7T	6
66	2P	DQd9		SA ₃	5T	5 .
67	3T	SA14		SA ₂	6R	4
68	2R	SA15		SA1	4T	3
69	4N	SA16		SA ₀	4P	2
70	3R	M1		M2	<u>5</u> R	1

BOUNDARY SCAN EXIT ORDER(x18)

DOUN	DANI	JUAN	LAII	JULL	(XIO)	
26	3B	SA ₉		SA8	5B	25
27	2B	NC		NC	6B	24
28	ЗА	SA10		SA7	5A	23
29	3C	SA11		SA6	5C	22
30	2C	SA12		SA ₅	6C	21
31	2A	SA13		SA4	6A	20
				DQa9	6D	19
32	1D	DQb1				
33	2E	DQb2				
				DQa8	7E	18
				DQa7	6F	17
34	2G	DQb3				
				DQa6	7G	16
				DQa5	6H	. 15
35	1H	DQb4				
36	3G	SWb				
37	4D	ZQ		G	4F	14
38	4E	SS		K	4K	13
39	4G	ō		ĸ	4L	12
40	4H	С		SWa	5L	11
41	4M	SW		DQa4	7K	10
42	2K	DQb5		DQa3	6L	9
43	1L	DQb6				
44	2M	DQb7		DQa2	6N	8
45	1N	DQb8		DQa1	7P	7
				ZZ	7T	6
46	2P	DQb9		SАз	5T_	5
47	3T_	SA14		SA ₂	6R	4
48	2R	SA ₁₅				
49	4N	SA16		SA1	4P	3
50	2T	SA17		SAo	6T	2
51	3R	M ₁		M2	5R	1
pins are	place ho	Iders for 1	6M part a	and the s	canned d	ata are

NOTE: 1. Pins 6B and 2B are no connection pin to internal chip. These pins are place holders for 16M part and the scanned data are fixed to "0" for this 4M parts.



JTAG DC OPERATING CONDITIONS

Parameter	Symbol	Min	Тур	Max	Unit	Note
Power Supply Voltage	VDD	3.15	3.3	3.45	٧	
Input High Level	ViH	2.0	-	VDD+0.3	٧	
Input Low Level	VIL	-0.3	-	0.8	V	
Output High Voltage(IoH=-2mA)	Voн	2.4	-	VDD	٧	
Output Low Voltage(IoL=2mA)	Vol	Vss	-	0.4	٧	

NOTE: 1. The input level of SRAM pin is to follow the SRAM DC specification.

JTAG AC TEST CONDITIONS

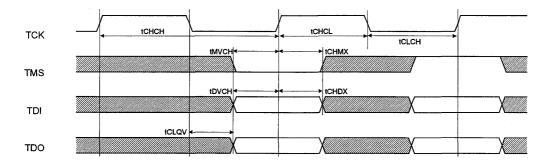
Parameter	Symbol	Min	Unit	Note
Input High/Low Level	VIH/VIL	3.0/0.0	V	
Input Rise/Fall Time	TR/TF	2.0/2.0	ns	
Input and Output Timing Reference Level		1.5	٧	1

NOTE: 1. See SRAM AC test output load on page 5.

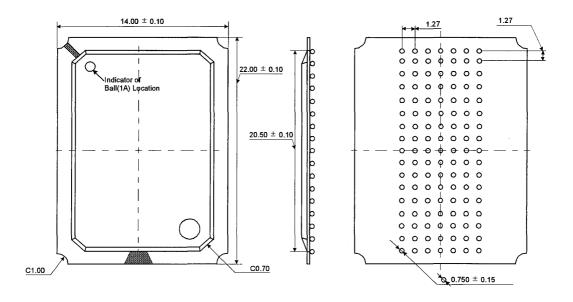
JTAG AC Characteristics

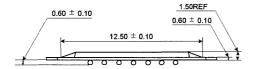
Parameter	Symbol	Min	Max	Unit	Note
TCK Cycle Time	tCHCH	50	-	ns	
TCK High Pulse Width	tCHCL	20	-	ns	
TCK Low Pulse Width	tCLCH	20	-	ns	
TMS Input Setup Time	tMVCH	5	-	ns	
TMS Input Hold Time	tCHMX	5	-	ns	
TDI Input Setup Time	tDVCH	5	-	ns	
TDI Input Hold Time	tCHDX	5	-	ns	
Clock Low to Output Valid	tCLQV	0	10	ns	

JTAG TIMING DIAGRAM



119 BGA PACKAGE DIMENSIONS





NOTE:

- All Dimensions are in Millimeters.
 Solder Ball to PCB Offset: 0.10 MAX.
- 3. PCB to Cavity Offset: 0.10 MAX.

119 BGA PACKAGE THERMAL CHARACTERISTICS

Parameter	Symbol	Min	Тур	Max	Unit	Note
Junction to Ambient(at still air)	Theta_JA	-	-	50	°CW ℃	
Junction to Ambient(at air flow of 100 LFPM)	Theta_JA	-	-	40	.cw	
Junction to Case	Theta_JC	-	-	8	ςw	
Junction to Solder Ball	Theta_JB	-	-	10	сw	

NOTE: 1. Junction temperature can be calculated by: TJ = TA + PD x Theta_JA.

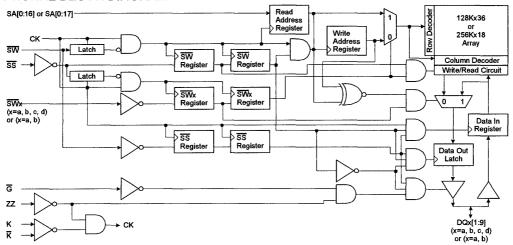
128Kx36 & 256Kx18 Synchronous Pipelined SRAM

FEATURES

- 128Kx36 or 256Kx18 Organizations.
- 3.3V Core/2.5V Output Power Supply.
- . LVCMOS Input and Output Levels.
- Differential, PECL Clock Inputs K, K
- . Synchronous Read and Write Operation
- Registered Input and Latched Output
- Internal Pipeline Latches to Support Late Write.
- Byte Write Capability(four byte write selects, one for each 9 bits)
- · Synchronous or Asynchronous Output Enable.
- · Power Down Mode via ZZ Signal.
- JTAG 1149.1 Compatible Test Access port.
- 119(7x17) Pin Ball Grid Array Package(14mm x 22mm).

Organization	Part Number	Cycle Time	Access Time
	KM736FV4002H-8	8	7.0
128Kx36	KM736FV4002H-9	9	8.0
	KM736FV4002H-10	8 9 10 8 9	9.0
	KM718FV4002H-8	8	7.0
256Kx18	KM718FV4002H-9	9	8.0
	KM718FV4002H-10	10	9.0

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

Pin Name	Pin Description	Pin Name	Pin Description
к, ₹	Differential Clocks(PECL Level)	c, c	Differential Output Clocks
SAn	Synchronous Address Input	M1, M2	Read Protocol Mode Pins
DQn	Bi-directional Data Bus	G	Asynchronous Output Enable
SW	Synchronous Grobal Write Enable	SS	Synchronous Select
SWa	Synchronous Byte a Write Enable	тск	JTAG Test Clock
SWb	Synchronous Byte b Write Enable	TMS	JTAG Test Mode Select
≅₩c	Synchronous Byte c Write Enable	TDI	JTAG Test Data Input
S₩d	Synchronous Byte d Write Enable	TDO	JTAG Test Data Output
ZZ	Asynchronous Power Down	ZQ	Output Driver Impedance Control Input HSTL Level
VDD	Core Power Supply	Vss	GND
VDDQ	Output Power Supply	NC	No Connection
VREF	HSTL Input Reference Voltage		

NOTE: 1. This SRAM only supports single clock, register-latch read protocol and have fixed impedance output driver.

Therefore the following inputs must be set with power up and must not change during SRAM operation;

C=VDD, C=Vss, M1=VDD, M2=Vss, ZQ=VDD and VREF=VDD. But they are also designed to operate being left floating.



PACKAGE PIN CONFIGURATIONS (TOP VIEW)

KM736FV4002(128Kx36)

	1	2	3	4	5	6	7
Α	VDDQ	SA13	SA10	NC	SA7	SA4	VDDQ
В	NC	NC	SA9	NC	SA8	NC	NC
С	NC	SA12	SA11	VDD	SA6	SA ₅	NC
D	DQc8	DQc9	Vss	ZQ	Vss	DQb9	DQb8
E	DQc6	DQc7	Vss	SS	Vss	DQb7	DQb6
F	VDDQ	DQc5	Vss	ਫ	Vss	DQb5	VDDQ
G	DQc3	DQc4	SWc	ਟ	SWb	DQb4	DQb3
Н	DQc1	DQc2	Vss	С	Vss	DQb2	DQb1
J	VDDQ	VDD	VREF	VDD	VREF	VDD	VDDQ
K	DQd1	DQd2	Vss	K	Vss	DQa2	DQa1
L	DQd3	DQd4	<u>S</u> ₩d	ĸ	SWa	DQa4	DQa3
М	VDDQ	DQd5	Vss	<u>sw</u>	Vss	DQa5	VDDQ
N	DQd6	DQd7	Vss	SA16	Vss	DQa7	DQa6
Р	DQd8	DQd9	Vss	SA ₀	Vss	DQa9	DQa8
R	NC	SA15	M 1	VDD	M2	SA ₂	NC
Т	NC	NC	SA14	SA1	SАз	NC	ZZ
U	VDDQ	TMS	TDI	TCK	TDO	NC NC	VDDQ

KM718FV4002(256Kx18)

	1	2	3	4	5	6	7
Α	VDDQ	SA13	SA10	NC	SA7	SA4	VDDQ
В	NC	NC	SA9	NC	SA8	NC	NC
С	NC	SA12	SA11	DaV	SA6	SA5	NC
D	DQb1	NC	Vss	ZQ	Vss	DQa9	NC _
E	NC	DQb2	Vss	SS	Vss	NC	DQa8
F	VDDQ	NC	Vss	G	Vss	DQa7	VDDQ
G	NC	DQb3	SWb	C	Vss	NC	DQa6
Н	DQb4	NC	Vss	С	Vss	DQa5	NC
J	VDDQ	VDD	VREF	VDD	VREF	VDD	VDDQ
K	NC	DQb5	Vss	K	Vss	NC	DQa4
L	DQb6	NC	Vss	ҡ	≅Wa	DQa3	NC
M	VDDQ	DQb7	Vss	SW	Vss	NC	VDDQ
N	DQb8	NC	Vss	SA16	Vss	DQa2	NC
Р	NC	DQb9	Vss	SA ₁	Vss	NC	DQa1
R	NC	SA15	M1	VDD	M2	SA ₂	NC
ТТ	NC	SA17	SA14	NC	SАз	SA ₀	ZZ
U	VDDQ	TMS	TDI	TCK	TDO	NC	VDDQ

FUNCTION DESCRIPTION

The KM736FV4002 and KM718FV4002 are 4,718,592 bit Synchronous SRAM. It is organized as 131,072 words of 36 bits(or 262, 144 words of 18 bits) and is implemented in SAMSUNG's advanced CMOS technology.

Single differential PECL level K clocks are used to initiate the read/write operation and all internal operations are self-timed. At the rising edge of K clock, all addresses, Write Enables, Synchronous Select and Data Ins are registered internally. Data outputs are updated from output latches of the falling edge of the K clock. An internal write data buffer allows write data to follow one cycle after addresses and controls. The package is 119(7x17) Ball Grid Array with balls on a 1.27mm pitch.

Read Operation

During reads, the address is registered during the clock rising edge and the internal array is read. The data is driven to the CPU in the following cycle. SS is driven low during this cycle, signaling that the SRAM should drive out the data.

During consecutive read cycles where the address is the same, the data output must be held constantly without any glitches. This characteristic is because the SRAM will be read by devices that will operate slower than the SRAM frequency and will require multiple SRAM cycles to perform a single read operation.

Write(Store) Operation

All addresses and \overline{SW} are both sampled on the clock rising edge. \overline{SW} is low on the rising clock. Write data is sampled on the rising clock, one cycle after write address and \overline{SW} have been sampled by the SRAM. \overline{SS} will be driven low during the same cycle that the Address, \overline{SW} and \overline{SWa} : are valid to signal that a valid operations is on the Address and Control Input.

Pipelined write are supported. This is done by using write data buffers on the SRAM that capture the write addresses on one write cycle, and write the array on the next write cycle. The "next write cycle" can actually be many cycles away, broken by a series of read cycles. Byte writes are supported. The byte write signals $\overline{SW}[a:d]$ signal which 9-bit bytes will be writen. Timing of $\overline{SW}[a:d]$ is the same as the \overline{SW} signal.

Bypass Read Operation

Since write data is not fully written into the array on first write cycle, there is a need to sense the address in case a future read is to be done from the location that has not been written yet. For this case, the address comparator check to see if the new read address is the same as the contents of the stored write address Latch. If the contents match, the read data must be supplied from the stored write data latch with standard read timing. If there is no match, the read data comes from the SRAM array. The bypassing of the SRAM array occurs on a byte by byte basis. If one byte is written and the other bytes are not, read data from the last written will have new byte data from the write data buffer and the other bytes from the SRAM array.

Low Power Dissipation Mode

During normal operation, asynchronous signal ZZ must be pulled low. Low Power Mode is enabled by switching ZZ high. When the SRAM is in Power Down Mode, the outputs will go to a Hi-Z state and the SRAM will draw standby current. SRAM data will be preserved and a recovery time(tZZR) is required before the SRAM resumes to normal operation.

TRUTH TABLE

K	ZZ	Ğ	55	SW	SWa	SWb	SWc	SWd	DQa	DQb	DQc	DQd	Operation	
Х	H	Х	Χ	Χ	Χ	Х	Χ	Χ	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Power Down Mode. No Operation	
Х	L	H	Χ	Χ	Χ	Х	Χ	Х	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Output Disabled. No Operation	
1	L	L	Н	Χ	Χ	Χ	Χ	Χ	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Output Disabled. No Operation	
1	L	L	L	Η	Х	Х	Χ	Χ	Dout	Dout	Dout	Dout	Read Cycle	
1		L	L	L	Η	Н	Ξ	Н	Hi-Z	Hi-Z	Hi-Z	Hi-Z	No Bytes Written	
. 1	L	L	L	L	L	Н	Н	Η	Din	Hi-Z	Hi-Z	Hi-Z	Write first byte	
1	L	L	Г	L	Н	L	Н	Н	Hi-Z	Din	Hi-Z	Hi-Z	Write second byte	
1	L	L	L	L	H	Н	L	H	Hi-Z	Hi-Z	DIN	Hi-Z	Write third byte	
1	L	L	L	L	Н	Н	Н	L	Hi-Z	Hi-Z	Hi-Z	DIN	Write fourth byte	
<u></u>	L	L	L	L	L	L	L	L	Din	DIN	Din	DIN	Write all byte	



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Core Supply Voltage Relative to Vss	VDD	-0.5 to 4.6	V
Output Supply Voltage Relative to Vss	VDDQ	-0.5 to 4.6	V
Voltage on any I/O pin Relative to Vss	VTERM	-0.5 to VDDQ+0.5	V
Maximum Power Dissipation	PD	2.5	W
Output Short-Circuit Current	lout	25	mA
Operating Temperature	Topr	0 to 70	°C
Storage Temperature	Тѕтс	-55 to 125	°C

NOTE: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Тур	Max	Unit	Note
Core Power Supply Voltage	VDD	3.15	3.3	3.45	V	
Output Power Supply Voltage	VDDQ	2.4	2.5	2.6	٧	
Input High Level	ViH	1.7	-	VDD + 0.3	٧	1, 2
Input Low Level	VIL	-0.3	-	0.7	٧	1, 3
PECL Clock Input High Level	VIH-PECL	2.135	-	2.420	٧	1
PECL Clock Input Low Level	VIL-PECL	1.490	-	1.825	٧	1
Operating Junction Temperature	TJ	10	-	110	°C	4

- NOTE: 1. These are DC VIH/VIH spec. The AC VIH/VIL levels are defined separately for measuring timing parameters.
 - 2. ViH (Max)DC = VDD+0.3V, ViH (Max)AC = VDD+1.5V(pulse width≤5ns).
 - 3. VIL (Min)DC = -0.3V, VIL (Min)AC =-1.5V(pulse width \leq 5ns).
 - 4. Junction temperature is a function of on-chip power dissipation, package thermal impedance, mounting site temperature and mounting site thermal impedance. TJ = TA + PD x THETA_JA

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit	Note
Average Power Supply Operating Current-x36 (VIN=VIH or VIL, ZZ & \overline{SS} =VIL)	IDD	-	450	mA	1
Average Power Supply Operating Current-x18 (VIN=VIH or VIL, ZZ & SS=VIL)	IDD	-	400	mA	1
Power Supply Standby Current (VIN=VIH or VIL, ZZ =VIH)	IsB	-	100	mA	1
Input Leakage Current (VIN=Vss or VDD)	lu	-1	1	μА	
Output Leakage Current (Vout=Vss or Vdd, ZZ =ViH)	lLO	-5	5	μA	
Output High Voltage(IoH=-2mA)	Voн	2.0	VDDQ	٧	
Output Low Voltage(IoL=2mA)	Vol	Vss	0.4	V	

NOTE: 1. Minimum cycle. IouT=0mA.



PIN CAPACITANCE

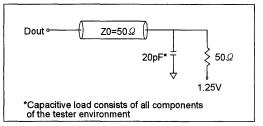
Parameter	Symbol	Pin Name	Min	Тур	Max	Unit
Input Capacitance	Cin	K, \overline{K} , \overline{SS} , \overline{SW} , \overline{G} , ZZ \overline{SW} x, ZQ, M1, M2, SAn, TCK, TMS, TDI	3	4	5	рF
Output Capacitance	Соит	DQn, TDO	5	6	7	pF

NOTE: Periodically sampled and 100% tested.(dV=0V, f=1MHz)

AC TEST CONDITIONS

Parameter	Symbol	Value	Unit
Input High/Low Level	VIH/VIL	2.5/0.0	٧
Clock Input High/Low Level(PECL)	VIH/VIL	2.4/1.5	٧
Input Rise/Fall Time	TR/TF	1.0/1.0	ns
Clock Input Rise/Fall Time(PECL)	TR/TF	0.5/0.5	ns
Output Rise/Fall Time	TR/TF	0.5~1.0	ns
Input and Out Timing Reference Level		1.25	٧
Clock Input Timing Reference Level		Cross Point	٧

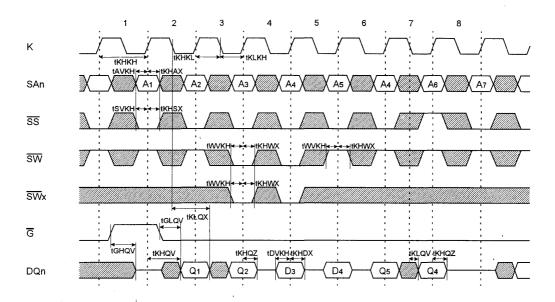
AC TEST OUTPUT LOAD



AC CHARACTERISTICS

Parameter	Symbol	-	8		9		10	Unit	Note
raiametei	Symbol	Min	Max	Min	Max	Min	Max	Unit	Note
Clock Cycle Time	tKHKH	8.0	-	9.0	-	10.0	-	ns	
Clock High Pulse Width	tKHKL	3.2	-	3.6	-	4.0	-	ns	
Clock Low Pulse Width	tKLKH	3.2	-	3.6	-	4.0	-	ns	
Clock High to Output Valid	tKHQV	-	7.0	-	8.0	-	9.0	ns	
Clock Low to Output Valid	tKLQV	-	2.5	-	3.0	-	3.5	ns	
Clock Low to Output Hold	tKLQX	1.0	-	1.0	-	1.0	-	ns	
Address Setup Time	tAVKH	0.5	-	0.5	-	0.1	-	ns	
Address Hold Time	tKHAX	1.0	-	1.0	-	1.0	-	ns	
Write Data Setup Time	tDVKH	0.5	-	0.5	-	0.5	-	ns	
Write Data Hold Time	tKHDX	1.0	-	1.0	-	1.0	-	ns	
SW, SW[a:d] Setup Time	t₩VKH	0.5	-	0.5	-	0.5	-	ns	
SW, SW[a:d] Hold Time	tKHWX	1.0	-	1.0	-	1.0	-	ns	
SS Setup Time	tSVKH	0.5	-	0.5	-	0.5	-	ns	
SS Hold Time	tKHSX	1.0	-	1.0	-	1.0	-	ns	
Clock High to Output Hi-Z	tKHQZ	-	2.5	-	3.0	-	3.5	ns	
Clock Low to Output Low-Z	tKHQX1	1.0	-	1.0	-	1.0	-	ns	
G High to Output High-Z	tGHQZ	-	2.5	-	3.0	-	3.5	ns	
উ Low to Output Low-Z	tGLQX	0.5	-	0.5	-	0.5	-	ns	
G Low to Output Valid	tGLQV	-	2.5		3.0	-	3.5	ns	
ZZ High to Power Down(Sleep Time)	tZZE	-	8.0	-	9.0	-	10.0	ns	
ZZ Low to Recovery(Wake-up Time)	tZZR	-	8.0	_	9.0	-	10.0	ns	

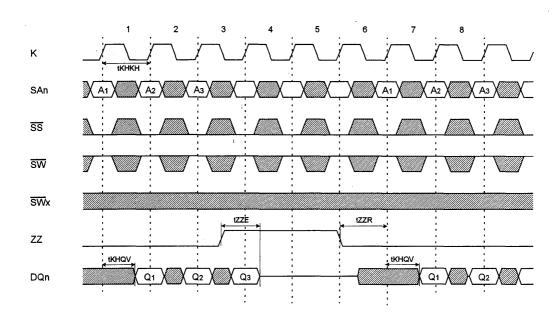
TIMING WAVEFORMS OF NORMAL ACTIVE CYCLES



NOTE:

- 1. D3 is the input data written in memory location A3.
- Q4 is the output data read from the write data buffer(not from the cell array), as a result of address A4 being a match from the last write cycle address.
- 3. Data is valid at the output at the later of tKHQV following the rising clock edge, or tKLQV following the fallowing clock edge.
- 4. When SS is sampled high or SW is sampled low on the rising edge of clock, the outputs go into Hi-Z state no later than tKHQZ following the rising clock edge.
- 5. When SS is low and SW is high on the rising edge of clock, the outputs go into Low-Z state(being driven) no earlier than tKHQX following the next falling edge of clock.
- 6. When the SRAM is deselected, the output goes Hi-Z at tKHQZ following the rising clock edge. On the next read cycle, note that the SRAM output do not leave the Hi-Z state until tKLQX after the falling clock edge.

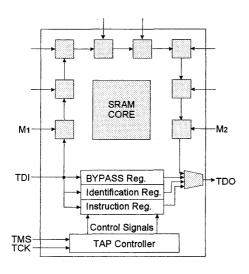
TIMING WAVEFORMS OF STANDBY CYCLES



IEEE 1149.1 TEST ACCESS PORT AND BOUNDARY SCAN-JTAG

This part contains an IEEE standard 1149.1 Compatible Teat Access Port(TAP). The package pads are monitored by the Serial Scan circuitry when in test mode. This is to support connectivity testing during manufacturing and system diagnostics. Internal data is not driven out of the SRAM under JTAG control. In conformance with IEEE 1149.1, the SRAM contains a TAP controller, Instruction Register, Bypass Register and ID register. The TAP controller has a standard 16-state machine that resets internally upon power-up, therefore, TRST signal is not required. It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfacing with normal operation of the SRAM, TCK must be tied to Vss to preclude mid level input. TMS and TDI are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to VDD through a resistor. TDO should be left unconnected.

JTAG Block Diagram



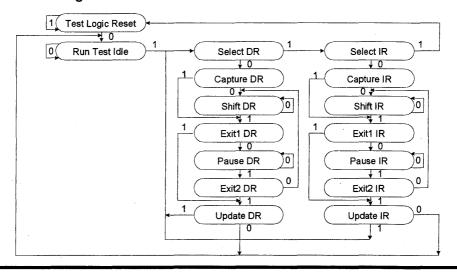
JTAG Instruction Coding

IR2	IR1	IR0	Instruction	TDO Output	Notes
0	0	0	SAMPLE-Z	Boundary Scan Register	1
0	0	1	IDCODE	Identification Register	2
0	1	0	SAMPLE-Z	Boundary Scan Register	1
0	1	1	BYPASS	Bypass Register	3
1	0	0	SAMPLE	Boundary Scan Register	4
1	0	1	BYPASS	Bypass Register	3_
1	1	0	BYPASS	Bypass Register	3_
1	1	1	BYPASS	Bypass Register	3

NOTE:

- Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs.
- TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
- Bypass register is initiated to Vss when BYPASS instruction is invoked. The Bypass Register also holds serially loaded TDI when exiting the Shift DR states.
- 4. SAMPLE instruction dose not places DQs in Hi-Z.

TAP Controller State Diagram





SCAN REGISTER DEFINITION

Part	Instruction Register	Bypass Register	ID Register	Boundary Scan
128Kx36	3 bits	1 bits	32 bits	70 bits
256Kx18	3 bits	1 bits	32 bits	51 bits

ID REGISTER DEFINITION

Part	Revision Number (31:28)	Part Configuration (27:18)	Vendor Definition (17:12)	Samsung JEDEC Code (11: 1)	Start Bit(0)
128Kx36	0000	00101 00100	000000	00001001110	1
256Kx18	0000	00110 00011	000000	00001001110	. 1

BOUNDARY SCAN EXIT ORDER(x36)

BOUN	DARY	SCAN	EXIT (ORDER	k(x36)	
36	3B	SA9		SA8	5B	35
37	2B	NC		NC	6B	34
38	3A	SA10		SA7	5A	33
39	3C	SA11		SA6	5C	32
40	2C	SA12		SA ₅	6C	31
41	2A	SA13		SA4	6A	30
42	2D	DQc9		DQb9	6D	29
43	1D	DQc8		DQb8	7D	28
44	2E	DQc7		DQb7	6E	27
45	1E	DQc6		DQb6	7E	26
46	2F	DQc5		DQb5	6F	25
47	2G	DQc4		DQb4	6G	24
48	1G	DQc3		DQb3	7G	23
49	2H	DQc2		DQb2	6H	22
50	1H	DQc1		DQb1	7H	21
51	3G	SWc	1	SWb	5G	20
52	4D	ZQ		G.	4F	19
53	4E	SS	1	K	4K	18
54	4G	ਟ		ĸ,	4L	17
[,] 55	4H	С		SWa	5L	16
56	4M	sw		DQa1	7K	15
57	3L	SWd		DQa2	_6K	14
58	1K	DQd1		DQa3	7L	13
59	2K	DQd2		DQa4	6L	12
60	1L	DQd3		DQa5	6M	11
61	2L	DQd4		DQa6	7N	10
62	2M	DQd5		DQa7	6N	9
63	1N	DQd6		DQa8	7P	8
64	2N	DQd7		DQa9	6P	7
65	1P	DQd8		ZZ	7T	6
66	2P	DQd9		SA ₃	5T	5
67	3T	SA14		SA2	6R	4
68	2R	SA15		SA1	4T	3
69	4N	SA16		SAo	4P	2
70	3R	M ₁		M2	5R	1

BOUNDARY SCAN EXIT ORDER(x18)

26 3B SA9 SA8 5B 25 27 2B NC NC 6B 24 28 3A SA10 SA7 5A 23 29 3C SA11 SA6 5C 22 30 2C SA12 SA5 6C 21 31 2A SA13 SA4 6A 20 DQa9 6D 19 32 1D DQb1 1 19 32 1D DQb1 1 19 19 32 1D DQb1 1 19 19 19 19 32 1D DQb1 1 19	DOUN	DAIL	JUAN	LAII	ONDER	(
28 3A SA10 SA7 5A 23 29 3C SA11 SA6 5C 22 30 2C SA12 SA5 6C 21 31 2A SA13 SA4 6A 20 DQa9 6D 19 32 1D DQb1 19 32 1D DQb1 19 32 1D DQb1 19 32 1D DQb2 19 32 1D DQb2 19 DQa8 7E 18 DQa7 6F 17 34 2G DQb3 16 DQa6 7G 16 DQa5 6H 15 35 1H DQb4 36 3G 3G \$\overline{Wb} \$\overline{Wb} 37 4D ZQ \$\overline{G} 4F 14 38 4E \$\overline{SS} <t< th=""><th>26</th><th>3B</th><th>SA₉</th><th></th><th>SA8</th><th>5B</th><th>25</th></t<>	26	3B	SA ₉		SA8	5B	25
29 3C SA11 SA6 5C 22 30 2C SA12 SA5 6C 21 31 2A SA13 SA4 6A 20 DQa9 6D 19 32 1D DQb1 DQa9 6D 19 32 1D DQb2 DQa8 7E 18 DQa7 6F 17 17 18 17 18 17 18 11 18 18 18 18 18 18 18 18 18 18 14 14 18 18 18 18	27	2B	NC		NC	6B	24
30 2C SA12 SA5 6C 21 31 2A SA13 SA4 6A 20 DQa9 6D 19 32 1D DQb1 19 33 2E DQb2 19 DQa8 7E 18 18 DQa7 6F 17 34 2G DQb3 16 DQa6 7G 16 DQa5 6H 15 35 1H DQb4 15 36 3G \$\overline{SWb}\$ \$\overline{G}\$ 4F 14 38 4E \$\overline{SS}\$ K 4K 13 14 14 12 40 4H C \$\overline{Ww}\$ \$\overline{L}\$ 11 1 41 4M \$\overline{Ww}\$ \$\overline{DQa4}\$ 7K 10 42 2K \$\overline{DQb5}\$ \$\overline{DQa2}\$ 6N 8 43 <	28	3A_	SA10		SA7	5A	23
31 2A SA13 SA4 6A 20 32 1D DQb1 DQa8 6D 19 33 2E DQb2 DQa8 7E 18 DQa7 6F 17 6F 17 34 2G DQb3 DQa6 7G 16 DQa5 6H 15 DQa5 6H 15 35 1H DQb4 DQa5 6H 15 36 3G SWb SW SW 14 38 4E SS K 4K 13 39 4G C K 4L 12 40 4H C SWa 5L 11 41 4M SW DQa4 7K 10 42 2K DQb5 DQa3 6L 9 43 1L DQb6 DQa1 7P 7 46 2P DQb9 SA3<	29	3C	SA11		SA6	5C	22
DQa9 6D 19 32 1D DQb1	30	2C	SA12		SA ₅	6C	21
32 1D DQb1 DQa8 7E 18 33 2E DQb2 DQa7 6F 17 34 2G DQb3 DQa6 7G 16 34 2G DQb4 DQa5 6H 15 35 1H DQb4 DQa5 6H 15 36 3G SWb SWb SW SW SW 14 14 14 14 14 14 14 14 14 14 13 14 14 14 12 14 14 14 12 14 14 14 12 14 14 14 12 14 14 14 12 14 14 12 14 14 12 14 14 12 14 14 14 14 12 14 14 14 14 14 14 14 14 14 14 14 14 14 14 <td>31</td> <td>2A</td> <td>SA13</td> <td></td> <td>SA4</td> <td>6A</td> <td>20</td>	31	2A	SA13		SA4	6A	20
DQa8 TE 18 DQa7 6F 17					DQa9	6D	19
DQa8 7E 18 DQa7 6F 17 34 2G DQb3 DQa6 7G 16 DQa5 6H 15 35 1H DQb4 36 3G SWb 37 4D ZQ G 4F 14 13 39 4G C K 4L 12 40 4H C SWa 5L 11 41 4M SW DQa4 7K 10 34 1L DQb6 34 45 1N DQb6 37 40 40 40 40 40 40 40 4	32	1D	DQb1				
DQa7 6F 17 34 2G DQb3 DQa6 7G 16 DQa5 6H 15 35 1H DQb4 36 3G SWb 37 4D ZQ G 4F 14 13 39 4G C K 4L 12 40 4H C SWa 5L 11 41 4M SW DQa4 7K 10 34 1L DQb6 34 45 1N DQb8 DQa1 7P 7 7 46 2P DQb9 SA3 5T 5 47 3T SA14 SA2 6R 4 49 4N SA16 SA1 4P 3 50 2T SA17 SA0 6T 2	33	2E	DQb2				
34 2G DQb3 DQa6 7G 16 35 1H DQb4 DQa5 6H 15 36 3G SWb					DQa8	7E	18
DQa6 7G 16 DQa5 6H 15 35					DQa7	6F	17
DQa5 6H 15 15 35 1H DQb4	34	2G	DQb3				
35 1H DQb4					DQa6	7G_	16
36 3G SWb G 4F 14 37 4D ZQ G 4F 14 38 4E SS K 4K 13 39 4G C K 4L 12 40 4H C SWa 5L 11 41 4M SW DQa4 7K 10 41 4M SW DQa4 7K 10 42 2K DQb5 DQa3 6L 9 43 1L DQb6 DQa3 6L 9 43 1L DQb6 DQa2 6N 8 45 1N DQb8 DQa1 7P 7 45 1N DQb8 DQa1 7P 7 46 2P DQb9 SA3 5T 5 47 3T SA14 SA2 6R 4 48 2R SA15					DQa5	6H	15
37 4D ZQ G 4F 14 38 4E SS K 4K 13 39 4G C K 4L 12 40 4H C SWa 5L 11 41 4M SW DQa4 7K 10 41 4M SW DQa4 7K 10 42 2K DQb5 DQa3 6L 9 43 1L DQb6 DQa3 6L 9 43 1L DQb6 DQa1 7P 7 45 1N DQb8 DQa1 7P 7 45 1N DQb8 DQa1 7P 7 46 2P DQb9 SA3 5T 5 47 3T SA14 SA2 6R 4 48 2R SA15 SA1 4P 3 49 4N SA16	35	1H_	DQb4				
38 4E \$\overline{SS}\$ K 4K 13 39 4G \$\overline{C}\$ \$\overline{K}\$ 4L 12 40 4H \$C \$\overline{SW}\$ 5L 11 41 4M \$\overline{SW}\$ DQa4 7K 10 42 2K DQb5 DQa3 6L 9 43 1L DQb6 DQa3 6L 9 44 2M DQb7 DQa2 6N 8 45 1N DQb8 DQa1 7P 7 45 1N DQb8 DQa1 7P 7 46 2P DQb9 SA3 5T 5 47 3T SA14 SA2 6R 4 48 2R SA15 SA1 4P 3 49 4N SA16 SA1 4P 3 50 2T SA17 SA0 6T 2	36	3G	SWb				
39 4G C K 4L 12 40 4H C \$\overline{\mathbb{SW}}\$ & 5L 11 41 4M \$\overline{\mathbb{SW}}\$ & DQa4 7K 10 42 2K DQb5 DQa3 6L 9 43 1L DQb6 DQa3 6L 9 44 2M DQb7 DQa2 6N 8 45 1N DQb8 DQa1 7P 7 45 1N DQb8 DQa1 7P 7 46 2P DQb9 SA3 5T 5 47 3T SA14 SA2 6R 4 48 2R SA15 SA1 4P 3 49 4N SA16 SA1 4P 3 50 2T SA17 SA0 6T 2	37	4D	ZQ		G	4F	14
40 4H C SWa 5L 11 41 4M SW DQa4 7K 10 42 2K DQb5 DQa3 6L 9 43 1L DQb6 SA3 5L 11 44 2M DQb7 DQa2 6N 8 45 1N DQb8 DQa1 7P 7 ZZ 7T 6 46 2P DQb9 SA3 5T 5 47 3T SA14 SA2 6R 4 48 2R SA15 49 4N SA16 SA1 4P 3 50 2T SA17 SA0 6T 2	38	4E	SS		K	4K	13
41 4M \$\overline{\text{SW}}\$ DQa4 7K 10 42 2K DQb5 DQa3 6L 9 43 1L DQb6 DQa2 6N 8 44 2M DQb7 DQa2 6N 8 45 1N DQb8 DQa1 7P 7 2Z 7T 6 46 2P DQb9 SA3 5T 5 47 3T SA14 SA2 6R 4 48 2R SA15 49 4N SA16 SA1 4P 3 50 2T SA17 SA0 6T 2	. 39	4G	<u>c</u>		R	4L	12
42 2K DQb5 DQa3 6L 9 43 1L DQb6 44 2M DQb7 DQa2 6N 8 45 1N DQb8 DQa1 7P 7 ZZ 7T 6 46 2P DQb9 SA3 5T 5 47 3T SA14 SA2 6R 4 48 2R SA15 49 4N SA16 SA1 4P 3 50 2T SA17 SA0 6T 2	40	4H	С		SWa	5L	11
43 1L DQb6 44 2M DQb7 DQa2 6N 8 45 1N DQb8 DQa1 7P 7 2Z 7T 6 46 2P DQb9 SA3 5T 5 47 3T SA14 SA2 6R 4 48 2R SA15 49 4N SA16 SA1 4P 3 50 2T SA17 SA0 6T 2	41	4M	SW		DQa4	7K	10
43 1L DQb6 44 2M DQb7 DQa2 6N 8 45 1N DQb8 DQa1 7P 7 2Z 7T 6 46 2P DQb9 SA3 5T 5 47 3T SA14 SA2 6R 4 48 2R SA15 49 4N SA16 SA1 4P 3 50 2T SA17 SA0 6T 2							
43 1L DQb6 44 2M DQb7 DQa2 6N 8 45 1N DQb8 DQa1 7P 7 2Z 7T 6 46 2P DQb9 SA3 5T 5 47 3T SA14 SA2 6R 4 48 2R SA15 49 4N SA16 SA1 4P 3 50 2T SA17 SA0 6T 2							
44 2M DQb7 DQa2 6N 8 45 1N DQb8 DQa1 7P 7 ZZ 7T 6 46 2P DQb9 SA3 5T 5 47 3T SA14 SA2 6R 4 48 2R SA15 49 4N SA16 SA1 4P 3 50 2T SA17 SA0 6T 2	42	2K	DQb5		DQa3	6L	9
45 1N DQb8 DQa1 7P 7 2Z 7T 6 46 2P DQb9 SA3 5T 5 47 3T SA14 SA2 6R 4 48 2R SA15 49 4N SA16 SA1 4P 3 50 2T SA17 SA0 6T 2	43	1L	DQb6				
45 1N DQb8 DQa1 7P 7 2Z 7T 6 46 2P DQb9 SA3 5T 5 47 3T SA14 SA2 6R 4 48 2R SA15 49 4N SA16 SA1 4P 3 50 2T SA17 SA0 6T 2							
ZZ 7T 6	44	2M	DQb7		DQa2	6N	8
46 2P DQb9 SA3 5T 5 47 3T SA14 SA2 6R 4 48 2R SA15 SA1 4P 3 49 4N SA16 SA1 4P 3 50 2T SA17 SA0 6T 2	45	1N	DQb8		DQa1	7P	7
46 2P DQb9 SA3 5T 5 47 3T SA14 SA2 6R 4 48 2R SA15 SA1 4P 3 49 4N SA16 SA1 4P 3 50 2T SA17 SA0 6T 2	- 1						
47 3T SA14 SA2 6R 4 48 2R SA15 SA1 4P 3 49 4N SA16 SA1 4P 3 50 2T SA17 SA0 6T 2					ZZ	7T	6
48 2R SA15 49 4N SA16 SA1 4P 3 50 2T SA17 SA0 6T 2	46	2P	DQb9		SA ₃	5T	5
49 4N SA16 SA1 4P 3 50 2T SA17 SA0 6T 2	47	3T	SA14		SA ₂	6R	4
50 2T SA17 SA0 6T 2	48	2R	SA15				
	-	4N	SA16		SA1	4P	3
51 3R M1 M2 5R 1		2T	SA17		SA ₀	6T	
	51	3R	M1		M2	5R	1

NOTE: 1. Pins 6B and 2B are no connection pin to internal chip. These pins are place holders for 16M part and the scanned data are fixed to "0" for this 4M parts.



JTAG DC OPERATING CONDITIONS

Parameter	Symbol	Min	Тур	Max	Unit	Note
Power Supply Voltage	VDD	3.15	3.3	3.45	٧	
Input High Level	VIH	2.0	-	VDD+0.3	V	
Input Low Level	VIL	-0.3	-	0.8	٧	
Output High Voltage(IOH=-2mA)	Voн	2.4	-	VDD	V	
Output Low Voltage(IoL=2mA)	Vol	Vss ·	-	0.4	V	

NOTE: 1. The input level of SRAM pin is to follow the SRAM DC specification.

JTAG AC TEST CONDITIONS

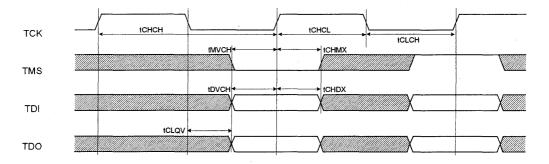
Parameter	Symbol	Min	Unit	Note
Input High/Low Level	VIH/VIL	3.0/0.0	V	
Input Rise/Fall Time	TR/TF	2.0/2.0	ns	
Input and Output Timing Reference Level		1.5	V	1

NOTE: 1. See SRAM AC test output load on page 5.

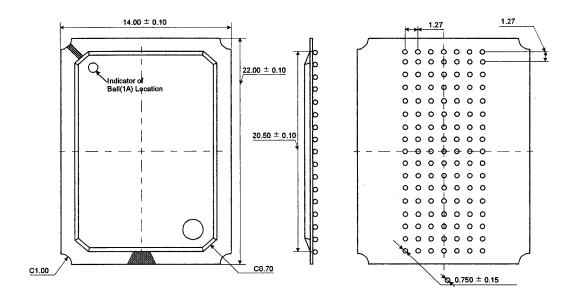
JTAG AC Characteristics

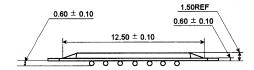
Parameter	Symbol	Min	Max	Unit	Note
TCK Cycle Time	tCHCH	50	-	ns	
TCK High Pulse Width	tCHCL	20	-	ns	
TCK Low Pulse Width	tCLCH	20	-	ns	
TMS Input Setup Time	tMVCH	5	-	ns	
TMS Input Hold Time	tCHMX	5	-	ns	
TDI Input Setup Time	tDVCH	5	-	ns	
TDI Input Hold Time	tCHDX	5	-	ns	
Clock Low to Output Valid	tCLQV	0	10	ns	

JTAG TIMING DIAGRAM



119 BGA PACKAGE DIMENSIONS





NOTE:

- All Dimensions are in Millimeters.
 Solder Ball to PCB Offset: 0.10 MAX.
- 3. PCB to Cavity Offset: 0.10 MAX.

119 BGA PACKAGE THERMAL CHARACTERISTICS

Parameter	Symbol	Min	Тур	Max	Unit	Note
Junction to Ambient(at still air)	Theta_JA	-	-	50	€W	
Junction to Ambient(at air flow of 100 LFPM)	Theta_JA	-	-	40	€W	
Junction to Case	Theta_JC	-	-	8	€W	
Junction to Solder Ball	Theta_JB	-	-	10	ςw	

NOTE: 1. Junction temperature can be calculated by: TJ = TA + PD x Theta_JA.

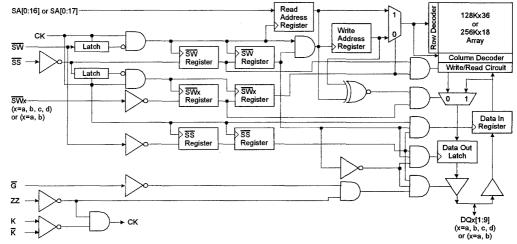


128Kx36 & 256Kx18 Synchronous Pipelined SRAM FEATURES

- 128Kx36 or 256Kx18 Organizations.
- 3.3V Core/ Output Power Supply.
- . LVTTL 3.3V Input and Output Levels.
- Differential, PECL Clock Inputs K, K.
- . Synchronous Read and Write Operation
- Registered Input and Latched Output
- Internal Pipeline Latches to Support Late Write.
- Byte Write Capability(four byte write selects, one for each 9 bits)
- Synchronous or Asynchronous Output Enable.
- Power Down Mode via ZZ Signal.
- JTAG 1149.1 Compatible Test Access port.
- 119(7x17) Pin Ball Grid Array Package(14mm x 22mm).

Organization	Part Number	Cycle Time	Access Time
	KM736FV4022H-8	8	7.0
128Kx36	KM736FV4022H-9	9	8.0
	KM736FV4022H-10	10	9.0
	KM718FV4022H-8	8	7.0
256Kx18	KM718FV4022H-9	9	8.0
	KM718FV4022H-10	10	9.0

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

Pin Name	Pin Description	Pin Name	Pin Description
K, K̈̃	Differential Clocks(PECL Level)	c, c	Differential Output Clocks
SAn	Synchronous Address Input	M1, M2	Read Protocol Mode Pins
DQn	Bi-directional Data Bus	G	Asynchronous Output Enable
SW	Synchronous Grobal Write Enable	<u>\$\$</u>	Synchronous Select
SWa	Synchronous Byte a Write Enable	TCK	JTAG Test Clock
≅Wb	Synchronous Byte b Write Enable	TMS	JTAG Test Mode Select
≅Wc	Synchronous Byte c Write Enable	TDI	JTAG Test Data Input
SWd	Synchronous Byte d Write Enable	TDO	JTAG Test Data Output
ZZ	Asynchronous Power Down	ZQ	Output Driver Impedance Control Input HSTL Level
VDD	Core Power Supply	Vss	GND
VDDQ	Output Power Supply	NC	No Connection
VREF	HSTL Input Reference Voltage		

NOTE: 1. This SRAM only supports single clock, register-latch read protocol and have fixed impedance output driver.

Therefore the following inputs must be set with power up and must not change during SRAM operation;

C=VDD, C=Vss, M1=VDD, M2=Vss, ZQ=VDD and VREF=VDD. But they are also designed to operate being left floating.



PACKAGE PIN CONFIGURATIONS (TOP VIEW)

KM736FV4022(128Kx36)

	1	2	3	4	5	6	7
Α	VDDQ	SA13	SA10	NC	SA7	SA4	VDDQ
В	NC	NC	SA ₉	. NC	SA8	NC	NC
С	NC	SA12	SA11	VDD	SA6	SA ₅	NC
D	DQc8	DQc9	Vss	ZQ	Vss	DQb9	DQb8
E	DQc6	DQc7	Vss	SS	Vss	DQb7	DQb6
F	VDDQ	DQc5	Vss	Ğ	Vss	DQb5	VDDQ
G	DQc3	DQc4	<u>S</u> ₩c	ੋ	SWb	DQb4	DQb3
Н	DQc1	DQc2	Vss	С	Vss	DQb2	DQb1
J	VDDQ	VDD	VREF	VDD	VREF	VDD	VDDQ
K	DQd1	DQd2	Vss	К	Vss	DQa2	DQa1
L	DQd3	DQd4	SWd	ĸ	SWa	DQa4	DQa3
М	VDDQ	DQd5	Vss	SW	Vss	DQa5	VDDQ
N	DQd6	DQd7	Vss	SA16	Vss	DQa7	DQa6
Р	DQd8	DQd9	Vss	SA ₀	Vss	DQa9	DQa8
R	NC	SA15	M1	VDD	M2	SA2	NC
Т	NC	NC	SA14	SA1	SA ₃	NC	ZZ
U	VDDQ	TMS	TDI	TCK	TDO	NC	VDDQ

KM718FV4022(256Kx18)

	1	2	3	4	5	6	7
Α	VDDQ	SA13	SA10	NC	SA7	SA4	VDDQ
В	NC	NC	SA9	NC	SA8	NC	NC
С	NC	SA12	SA11	VDD	SA6	SA5	NC
D	DQb1	NC	Vss	ZQ	Vss	DQa9	NC
E	NC	DQb2	Vss	SS	Vss	NC	DQa8
F	VDDQ	NC	Vss ·	G	Vss	DQa7	VDDQ
G ·	NC	DQb3	SWb	ਟ	Vss	NC	DQa6
Н	DQb4	NC	Vss	С	Vss	DQa5	NC
J	VDDQ	VDD	VREF	VDD.	VREF	VDD	VDDQ
K	NC	DQb5	Vss	K	Vss	NC	DQa4
L	DQb6	NC	Vss	ĸ	SWa	DQa3	NC
M	VDDQ	DQb7	Vss	SW	Vss .	NC	VDDQ
N	DQb8	NC	Vss	SA16	Vss	DQa2	NC
P	NC	DQb9	Vss	SA ₁	Vss	NC	DQa1
R	NC	SA15	M1	VDD	M2	SA ₂	NC
Т	NC	SA17	SA14	NC ·	SA3	SA ₀	ZZ
U	VDDQ	TMS	TDI	TCK	TDO	NC	VDDQ

FUNCTION DESCRIPTION

The KM736FV4022 and KM718FV4022 are 4,718,592 bit Synchronous SRAM. It is organized as 131,072 words of 36 bits(or 262, 144 words of 18 bits) and is implemented in SAMSUNG's advanced CMOS technology.

Single differential PECL level K clocks are used to initiate the read/write operation and all internal operations are self-timed. At the rising edge of K clock, all addresses, Write Enables, Synchronous Select and Data Ins are registered internally. Data outputs are updated from output latches of the falling edge of the K clock. An internal write data buffer allows write data to follow one cycle after addresses and controls. The package is 119(7x17) Ball Grid Array with balls on a 1.27mm pitch.

Read Operation

During reads, the address is registered during the clock rising edge and the internal array is read. The data is driven to the CPU in the following cycle. SS is driven low during this cycle, signaling that the SRAM should drive out the data.

During consecutive read cycles where the address is the same, the data output must be held constantly without any glitches. This characteristic is because the SRAM will be read by devices that will operate slower than the SRAM frequency and will require multiple SRAM cycles to perform a single read operation.

Write(Store) Operation

All addresses and \overline{SW} are both sampled on the clock rising edge. \overline{SW} is low on the rising clock. Write data is sampled on the rising clock, one cycle after write address and \overline{SW} have been sampled by the SRAM. \overline{SS} will be driven low during the same cycle that the Address, \overline{SW} and \overline{SW} [a:d] are valid to signal that a valid operations is on the Address and Control Input.

Pipelined write are supported. This is done by using write data buffers on the SRAM that capture the write addresses on one write cycle, and write the array on the next write cycle. The "next write cycle" can actually be many cycles away, broken by a series of read cycles. Byte writes are supported. The byte write signals $\overline{SW}[a:d]$ signal which 9-bit bytes will be writen. Timing of $\overline{SW}[a:d]$ is the same as the \overline{SW} signal.

Bypass Read Operation

Since write data is not fully written into the array on first write cycle, there is a need to sense the address in case a future read is to be done from the location that has not been written yet. For this case, the address comparator check to see if the new read address is the same as the contents of the stored write address Latch. If the contents match, the read data must be supplied from the stored write data latch with standard read timing. If there is no match, the read data comes from the SRAM array. The bypassing of the SRAM array occurs on a byte by byte basis. If one byte is written and the other bytes are not, read data from the last written will have new byte data from the write data buffer and the other bytes from the SRAM array.

Low Power Dissipation Mode

During normal operation, asynchronous signal ZZ must be pulled low. Low Power Mode is enabled by switching ZZ high. When the SRAM is in Power Down Mode, the outputs will go to a Hi-Z state and the SRAM will draw standby current. SRAM data will be preserved and a recovery time(tZZR) is required before the SRAM resumes to normal operation.

TRUTH TABLE

K	ZZ	Ğ	SS	sw	SWa	SWb	SWc	SWd	DQa	DQb	DQc	DQd	Operation
X	Н	Х	Χ	Х	Х	Х	Х	Х	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Power Down Mode. No Operation
Х	L	Н	Х	Х	Х	Х	Х	Х	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Output Disabled. No Operation
1	L	L	Н	Х	Х	Х	Х	Х	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Output Disabled. No Operation
1	L	L	L	Н	Х	Х	Х	X	Dout	Dout	Dout	Dout	Read Cycle
1	L	L	L	L	Н	Н	Н	Н	Hi-Z	Hi-Z	Hi-Z	Hi-Z	No Bytes Written
Î	L	L	L	L	L	Н	Н	Н	DIN	Hi-Z	Hi-Z	Hi-Z	Write first byte
1	L	L	L	L	Н	L	.H	Н	Hi-Z	DIN	Hi-Z	Hi-Z	Write second byte
1	L	L	L	L	Н	Н	L	Н	Hi-Z	Hi-Z	Din	Hi-Z	Write third byte
1	L	L	L	L	Н	Н	Н	L	Hi-Z	Hi-Z	Hi-Z	DIN	Write fourth byte
1	L	L	L	L	L	L	L	L	DIN	Din	Din	Din	Write all byte



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Core Supply Voltage Relative to Vss	VDD	-0.5 to 4.6	V
Output Supply Voltage Relative to Vss	VDDQ	-0.5 to 4.6	V
Voltage on any I/O pin Relative to Vss	VTERM	-0.5 to VDDQ+0.5	V
Maximum Power Dissipation	PD	2.5	W
Output Short-Circuit Current	lout	25	mA
Operating Temperature	Topr	0 to 70	င
Storage Temperature	Тѕтҫ	-55 to 125	°C

NOTE: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Тур	Max	Unit	Note
Core Power Supply Voltage	VDD	3.15	3.3	3.45	٧	
Output Power Supply Voltage	VDDQ	3.15	3.3	3.45	V	
Input High Level	VIH	2.0	-	VDD + 0.3	V	1, 2
Input Low Level	VIL	-0.3	-	0.8	٧	1, 3
PECL Clock Input High Level	VIH-PECL	2.135	-	2.420	V	1
PECL Clock Input Low Level	VIL-PECL	1.490		1.825	٧	1
Operating Junction Temperature	TJ	10	-	110	°C	4

- NOTE: 1. These are DC VIH/VIH spec. The AC VIH/VIL levels are defined separately for measuring timing parameters.
 - 2. ViH (Max)DC = VDD+0.3V, ViH (Max)AC = VDD+1.5V(pulse width \leq 5ns).
 - 3. VIL (Min)DC = -0.3V, VIL (Min)AC =-1.5V(pulse width≤5ns).
 - 4. Junction temperature is a function of on-chip power dissipation, package thermal impedance, mounting site temperature and mounting site thermal impedance. TJ = TA + PD x THETA_JA

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit	Note
Average Power Supply Operating Current-x36 (VIN=VIH or VIL, ZZ & SS=VIL)	IDD	-	450	mA	1
Average Power Supply Operating Current-x18 (VIN=VIH or VIL, ZZ & SS=VIL)	IDD	-	400	mA	1
Power Supply Standby Current (VIN=VIH or VIL, ZZ =VIH)	ISB	-	100	mA	1
Input Leakage Current (VIN=Vss or VDD)	lu	-1	1	μA	
Output Leakage Current (Vouт=Vss or Vpp, ZZ =Viн)	lLO	-5	5	μA	
Output High Voltage(IOH=-2mA)	Voн	2.4	VDDQ	V	
Output Low Voltage(IoL=2mA)	Vol	Vss	0.4	٧	

NOTE: 1. Minimum cycle. Iout=0mA.



PIN CAPACITANCE

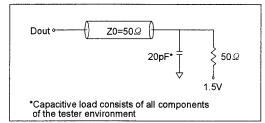
Parameter	Symbol	Pin Name	Min	Тур	Max	Unit
Input Capacitance	Cin	K, K, SS, SW, G, ZZ SWx, ZQ, M1, M2, SAn, TCK, TMS, TDI	3	4	5	pF
Output Capacitance	Соит	DQn, TDO	5	6	7	pF

NOTE: Periodically sampled and 100% tested.(dV=0V, f=1MHz)

AC TEST CONDITIONS

Parameter	Symbol	Value	Unit
Input High/Low Level	VIH/VIL	3.0/0.0	٧
Clock Input High/Low Level(PECL)	VIH/VIL	2.4/1.5	٧
Input Rise/Fall Time	TR/TF	1.0/1.0	ns
Clock Input Rise/Fall Time(PECL)	TR/TF	0.5/0.5	ns
Output Rise/Fall Time	TR/TF	0.5~1.0	ns
Input and Out Timing Reference Level		1.5	٧
Clock Input Timing Reference Level		Cross Point	V

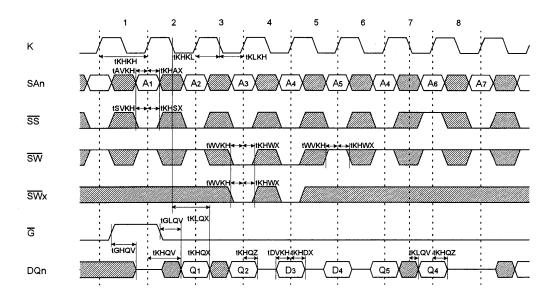
AC TEST OUTPUT LOAD



AC CHARACTERISTICS

Parameter	Symbol		8	-9		-10		Unit	Note
Falailletei	Symbol	Min	Max	Min	Max	Min	Max	Onic	Note
Clock Cycle Time	tKHKH	8.0	-	9.0	-	10.0	-	ns	
Clock High Pulse Width	tKHKL	3.2	-	3.6	-	4.0	-	ns	
Clock Low Pulse Width	tKLKH	3.2	-	3.6	-	4.0	-	ns	
Clock High to Output Valid	tKHQV	-	7.0	-	8.0	-	9.0	ns	
Clock Low to Output Valid	tKLQV	-	2.5	-	3.0	-	3.5	ns	
Clock Low to Output Hold	tKLQX	1.0	-	1.0	-	1.0	-	ns	
Address Setup Time	tAVKH	0.5	-	0.5	-	0.1	-	ns	
Address Hold Time	tKHAX	1.0	-	1.0	-	1.0	-	ns	
Write Data Setup Time	tDVKH	0.5	-	0.5	-	0.5	-	ns	
Write Data Hold Time	tKHDX	1.0	-	1.0	-	1.0	-	ns	
SW, SW[a:d] Setup Time	tWVKH	0.5	-	0.5	-	0.5	-	ns	
SW, SW[a:d] Hold Time	tKHWX	1.0	-	1.0	-	1.0	-	ns	
SS Setup Time	tSVKH	0.5	-	0.5	-	0.5	-	ns	
SS Hold Time	tKHSX	1.0	-	1.0	-	1.0	-	ns	
Clock High to Output Hi-Z	tKHQZ	-	2.5	-	3.0	-	3.5	ns	
Clock Low to Output Low-Z	tKHQX1	1.0	-	1.0	-	1.0	-	ns	
G High to Output High-Z	tGHQZ	-	2.5	_	3.0	-	3.5	ns	
G Low to Output Low-Z	tGLQX	0.5	-	0.5	-	0.5	-	ns	
G Low to Output Valid	tGLQV	-	2.5	-	3.0	-	3.5	ns	
ZZ High to Power Down(Sleep Time)	tZZE	-	8.0	-	9.0	-	10.0	ns	
ZZ Low to Recovery(Wake-up Time)	tZZR	-	8.0	-	9.0	-	10.0	ns	

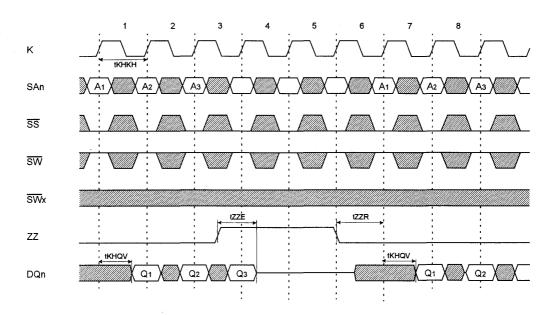
TIMING WAVEFORMS OF NORMAL ACTIVE CYCLES



NOTE:

- 1. D3 is the input data written in memory location A3.
- Q4 is the output data read from the write data buffer(not from the cell array), as a result of address A4 being a match from the last write cycle address.
- 3. Data is valid at the output at the later of tKHQV following the rising clock edge, or tKLQV following the fallowing clock edge.
- 4. When SS is sampled high or SW is sampled low on the rising edge of clock, the outputs go into Hi-Z state no later than tKHQZ following the rising clock edge.
- 5. When SS is low and SW is high on the rising edge of clock, the outputs go into Low-Z state(being driven) no earlier than tKHQX following the next falling edge of clock.
- When the SRAM is deselected, the output goes Hi-Z at tKHQZ following the rising clock edge. On the next read cycle, note that the SRAM output do not leave the Hi-Z state until tKLQX after the falling clock edge.

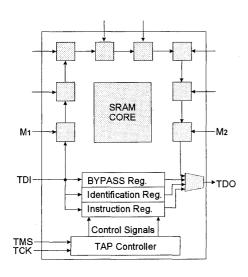
TIMING WAVEFORMS OF STANDBY CYCLES



IEEE 1149.1 TEST ACCESS PORT AND BOUNDARY SCAN-JTAG

This part contains an IEEE standard 1149.1 Compatible Teat Access Port(TAP). The package pads are monitored by the Serial Scan circuitry when in test mode. This is to support connectivity testing during manufacturing and system diagnostics. Internal data is not driven out of the SRAM under JTAG control. In conformance with IEEE 1149.1, the SRAM contains a TAP controller, Instruction Register, Bypass Register and ID register. The TAP controller has a standard 16-state machine that resets internally upon power-up, therefore, TRST signal is not required. It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfacing with normal operation of the SRAM, TCK must be tied to Vss to preclude mid level input. TMS and TDI are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to Vpp through a resistor. TDO should be left unconnected.

JTAG Block Diagram



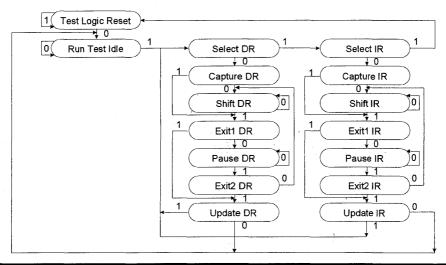
JTAG Instruction Coding

IR2	IR1	IR0	Instruction	TDO Output	Notes
0	0	0	SAMPLE-Z	Boundary Scan Register	1
0	0	1	IDCODE	Identification Register	2
0	1	0	SAMPLE-Z	Boundary Scan Register	1
0	1	1	BYPASS	Bypass Register	3
1	0	0	SAMPLE	Boundary Scan Register	4
1	0	1	BYPASS	Bypass Register	3
1	1	0	BYPASS	Bypass Register	3
1	1	1	BYPASS	Bypass Register	3

NOTE:

- Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs.
- TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
- Bypass register is initiated to Vss when BYPASS instruction is invoked. The Bypass Register also holds serially loaded TDI when exiting the Shift DR states.
- 4. SAMPLE instruction dose not places DQs in Hi-Z.

TAP Controller State Diagram





SCAN REGISTER DEFINITION

Part	Instruction Register	Bypass Register	ID Register	Boundary Scan
128Kx36	3 bits	1 bits	32 bits	70 bits
256Kx18	3 bits	1 bits	32 bits	51 bits

ID REGISTER DEFINITION

Part	Revision Number (31:28)	Part Configuration (27:18)	Vendor Definition (17:12)	Samsung JEDEC Code (11: 1)	Start Bit(0)
128Kx36	0000	00101 00100	000000	00001001110	1
256Kx18	0000 .	00110 00011	000000	00001001110	1

BOUN	DARY	SCAN	EXIT (ORDER	R(x36)	
36 *	3B	SA9		SA8	5B	35
37	2B	NC		NC	6B	34
38	ЗА	SA10		SA7	5A	33
39	3C	SA11		SA ₆	5C	32
40	2C	SA12		SA ₅	6C	31
41	2A	SA13		SA4	6A	30
42	2D	DQc9		DQb9	6D	29
43	1D	DQc8		DQb8	7D	28
44	2E	DQc7		DQb7	6E	27
45	1E	DQc6		DQb6	7E	26
46	2F	DQc5		DQb5	6F	25
47	2G	DQc4		DQb4	6G	24
48	1G	DQc3		DQb3	7G	23
49	2H	DQc2		DQb2	6H	22
50	1H	DQc1		DQb1	7H	21
51	3G	SWc		SWb	5G	20
52	4D	ZQ		G	4F	19
53	4E	SS		K	4K	18
54	4G	C		ĸ	4L	17
55	4H	С		SWa	5L	16
56	4M	SW		DQa1	7K	15
57	3L	SWd		DQa2	6K	14
58	1K	DQd1		DQa3	7L	13
59	2K	DQd2		DQa4	6L	12
60	1L	DQd3		DQa5	6M	11
61	2L	DQd4		DQa6	7N	10
62	2M	DQd5		DQa7	6N	9
63	1N	DQd6		DQa8	7P	8
64	2N	DQd7		DQa9	6P	7
65	1P	DQd8		ZZ	7T	6
66	2P	DQd9		SАз	5T	5
67	3T	SA14		SA2	6R	4
68	2R	SA15		SA1	4T	3
69	4N	SA16		SA ₀	4P	2
70	3R	M ₁		M2	5R	1

BOUNDARY SCAN EXIT ORDER(x18)

			 	(אוט)	
26	3B	SA9	SA8	5B	25
27	2B	NC	NC	6B	24
28	3A	SA10	SA7	5A	23
29	3C	SA11	SA6	5C	22
30	2C	SA12	SA ₅	6C	21
31	2A	SA13	SA4	6A	20
			DQa9	6D	19
32	1D	DQb1			
33	2E	DQb2			
			DQa8	7E	18
			DQa7	6F	17
34	2G	DQb3			
			DQa6	7G	16
			DQa5	6H	15
35	1H	DQb4			
36	3G	SWb			
37	4D	ZQ	JO	4F	14
38	4E	SS	K	4K	13
39	4G	C	K	4L	12
40	4H	С	SWa	5L	11
41	4M	SW	DQa4	7K	10
42	2K	DQb5	DQa3	6L	9
43	1L	DQb6			
44	2M	DQb7	DQa2	6N	8
45	1N	DQb8	DQa1	7P	7
L					
			ZZ	7T	6
46	2P	DQb9	SA3	5T	5
47	ЗТ	SA14	SA ₂	6R	4
48	2R	SA15			
49	4N	SA16	SA ₁	4P	3
50	2T	SA17	SA ₀	6T	2
51	3R	M1	M2	5R	1

NOTE: 1. Pins 6B and 2B are no connection pin to internal chip. These pins are place holders for 16M part and the scanned data are fixed to "0" for this 4M parts.



JTAG DC OPERATING CONDITIONS

Parameter	Symbol	Min	Тур	Max	Unit	Note
Power Supply Voltage	VDD	3.15	3.3	3.45	٧	
Input High Level	ViH	2.0	-	Vpp+0.3	V	
Input Low Level	ViL	-0.3	-	0.8	V	
Output High Voltage(IoH=-2mA)	Voн	2.4	-	VDD	٧	
Output Low Voltage(IoL=2mA)	Vol	Vss	-	0.4	V	

NOTE: 1. The input level of SRAM pin is to follow the SRAM DC specification.

JTAG AC TEST CONDITIONS

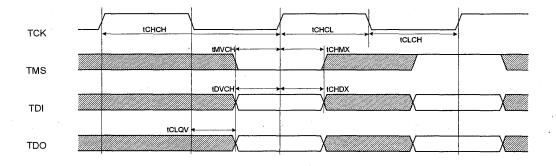
Parameter	Symbol	Min	Unit	Note
Input High/Low Level	VIH/VIL	3.0/0.0	V	
Input Rise/Fall Time	TR/TF	2.0/2.0	ns	
Input and Output Timing Reference Level		1.5	V	1

NOTE: 1. See SRAM AC test output load on page 5.

JTAG AC Characteristics

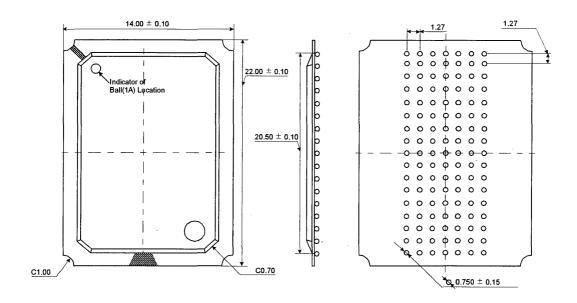
Parameter	Symbol	Min	Max	Unit	Note
TCK Cycle Time	tCHCH	50	-	ns	
TCK High Pulse Width	tCHCL	20	-	ns	
TCK Low Pulse Width	tCLCH	20	-	ns	
TMS Input Setup Time	tMVCH	5	-	ns	
TMS Input Hold Time	tCHMX	5	-	ns	
TDI Input Setup Time	tDVCH	5	-	ns	
TDI Input Hold Time	tCHDX	5	-	ns	
Clock Low to Output Valid	tCLQV	0	10	ns	

JTAG TIMING DIAGRAM





119 BGA PACKAGE DIMENSIONS





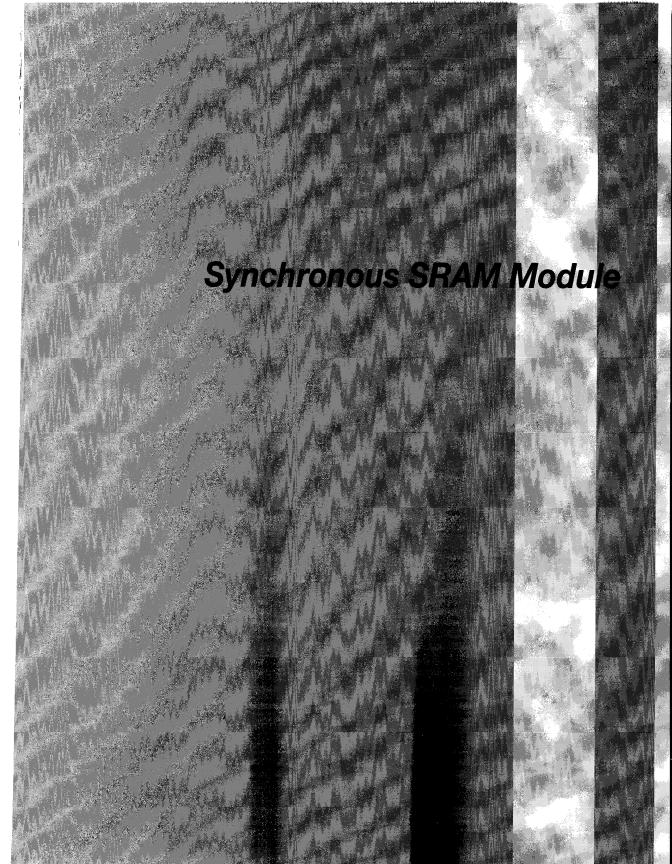
NOTE:

- 1. All Dimensions are in Millimeters.
- 2. Solder Ball to PCB Offset: 0.10 MAX.
- 3. PCB to Cavity Offset: 0.10 MAX.

119 BGA PACKAGE THERMAL CHARACTERISTICS

Parameter	Symbol	Min	Тур	Max	Unit	Note
Junction to Ambient(at still air)	Theta_JA	-	-	50	€W	
Junction to Ambient(at air flow of 100 LFPM)	Theta_JA	-	v-	40	°CW °	
Junction to Case	Theta_JC	-	-	8	°CW	
Junction to Solder Ball	Theta_JB	-	-	10	°CW\	

NOTE: 1. Junction temperature can be calculated by: TJ = TA + PD x Theta_JA.



256KB Synchronous Pipelined Burst SRAM Module

FEATURES

- . Implemented based on COAST 3.1
- . Supports Interleave Burst and Linear Burst Mode
- · Zero-wait-state operation at 75/66MHz
- . TTL compatible inputs/outputs
- Multiple ground pins and decoupling capacitors for maximum noise immunity
- . 160-pin DIMM with gold plated Tap
- PCB : Height (1130mil)
- Product Family: KMM764V41AG2-13/15

GENERAL DESCRIPTION

The KMM764V41AG2 is 256K byte high-frequency Synchronous Pipelined Burst Static Random Access Memory module organized as 32K words by 64 bits. The module is designed specially to function as the secondary cache in Pentium, K5, M1, and Power PC-based systems and using SAMSUNG's PCB design tool. The device for this module is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology.

PIN NAMES

Pin Name	Pin Function
CLK[1:0]	Clock Inputs
A[18:3]	Cache RAM Address Inputs
D[63:0]	Cache RAM Data Inputs/Outputs
TIO[7:0]	Tag RAM Data Inputs/Outputs
TWE	Tag RAM Write Enable Input
ECS[2:1]	Chip Select Inputs for Depth Expansion
ccs	Chip Select Input
<u>CWE</u> [7:0]	Write Enable Inputs
COE	Output Enable Input
ADSP	Address Status Processor
CADS	Address Status Controller
CADV	Burst Address Advance
BWE	Byte Write Enable Input
GWE	Grobal Write Enable Input
LBO	Burst Mode Control
Vcc5	Power Supply(5V)
Vccз	Power Supply(3.3V)
Vss	Ground
N.C	No Connection

PD PIN INFORMATION

N.C	Vss	N.C	N.C	KMM764V41AG2
PD3	PD2	PD1	PD ₀	
	PD Pin /	Allocation		Module Part No

PIN CONFIGURATION(Top View)

Vss	81	1	Vss	D57	122	42	D56
TIO ₁	82	2	TIO₀		i		l
TIO7	83	3	TIO ₂		İ		
TIO5	84	4	TIO ₆	Vss	123	43	Vss
TIO ₃	85	5	TIO ₄	D55	124	44	D54
N.C	86	6	N.C	D53	125	45	D52
Vccs	87	7	Vccs	D51	126	46	D50
N.C	88	8	TWE	D49	127	47	D48
CADV	89	9	CADS	Vss	128	48	Vss
Vss	90	10	Vss	D47	129	49	D46
COE	91	11	CWE₄	D45	130	50	D44
CWE ₅	92	12	CWE ₆	D43	131	51	D42
CWE ₇	93	13	CWE₀	Vcc5	132	52	Vccs
CWE ₁	94	14	CWE ₂	D41	133	53	D40
Vcc5	95	15	Vccs	D39	134	54	D38
	96	16	CCS	D37	135	55	D36
N.C	97	17	GWE(3)	Vss	136	56	Vss
N.C	98	18	BWE(3)	D35	137	57	D34
Vss	99	19	Vss	D33	138	58	D32
N.C	100	20	Аз	D31	139	59	D30
A4	101	21	A7	Vcc5	140	60	Vccs
A6	102	22	A5	D29	141	61	D28
As	103	23	A11	D27	142	62	D26
A10	104	24	A16	D25	143	63	D24
Vcc5	105	25	Vccs	Vss	144	64	Vss
A17	106	26	A18(1)	D23	145	65	D22
Vss	107	27	Vss	D21	146	66	D20
As	108	28	A12	D19	147	67	D18
A14	109	29	A13	Vccs	148	68	Vccs
A15	110	30	ADSP	D17	149	69	D16
N.C	111	31	ECS ₁	D15	150	70	D14
PD₀	112	32	ECS ₂	D13	151	71	D12
PD2	113	33	PD ₁	Vss	152	72	Vss
LBO(2)	114	34	PD3	D11	153	73	D10
Vss	115	35	Vss	D9	154	74	D8
CLK ₀	116	36	CLK1(1)	D7	155	75	D6
Vss	117	37	Vss	Vcc5	156	76	Vccs
D63	118	38	D62	D ₅	157	77	D4
Vcc5	119	39	Vccs	D3	158	78	D ₂
D61	120	30	D60	D ₁	159	79	D ₀
D59	121	41	D58	Vss	160	80	Vss
				- 1			

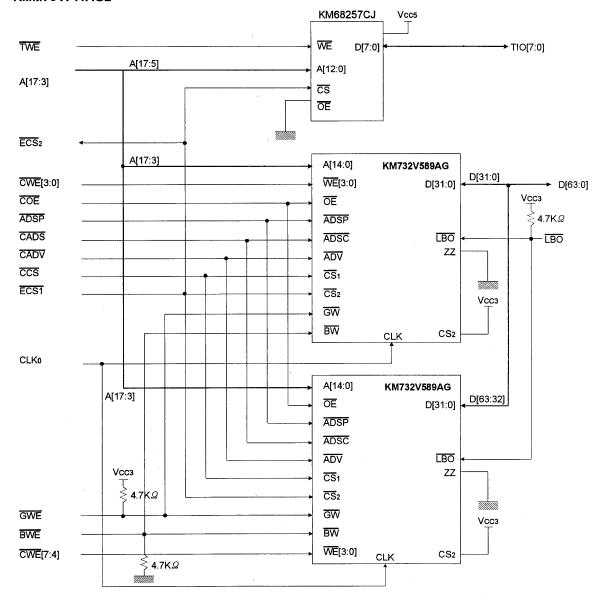
NOTE

- These pins are used for 512KB module only and they should be no connect for this module.
- Default is no connect for Intel processor based designs becouse this pin pulled up with 4.7Kohm resistor on the module.
- When these pins are no connect, all byte write should be controlled by all CWEx pins.



FUNCTIONAL BLOCK DIAGRAM

KMM764V41AG2



NOTE

- 1. ZZ pin is internally connected to Vss and not pinout on the module.
- 2. LBO is pulled up with 4.7Kohm resistor.
- 3. GWE is pulled up with 4.7Kohm resistor and BWE is pulled down with 4.7Kohm resistor.



A-1. SYNCHRONOUS PIPELINE BURST TRUTH TABLE(Data field)

CCS	ECS	ADSP	CADS	CADV	WRITE	K	Address Accessed	Operation
Н	X*	Х	L	Х	Х	1	N/A	Not Selected
L	Х	L	Х	Х	Х	1	N/A	Not Selected
L	Н	L	Х	Х	Х	1	N/A	Not Selected
L	Х	X	L	Х	Х	1	N/A	Not Selected
L	Н	Х	L	Х	Х	. 1	N/A	Not Selected
L	L	L	Х	Х	Х	1	External Address	Begin Burst Read Cycle
L	L	Н	L	Х	L	1	External Address	Begin Burst Read Cycle
L	L	Н	L	Х	Н	1	External Address	Begin Burst Read Cycle
Х	Х	Н	Н	L	Н	1	Next Address	Continue Burst Read Cycle
Н	Х	Х	Н	L	Н	1	Next Address	Continue Burst Read Cycle
Х	Х	Н	Н	L	L	1	Next Address	Continue Burst Read Cycle
Н	Х	Х	Н	L	L	1	Next Address	Continue Burst Read Cycle
Х	Х	Н	Н	H	Н	1	Current Address	Suspend Burst Read Cycle
Н	Х	Х	Н	Н	Н	1	Current Address	Suspend Burst Read Cycle
Х	Х	Н	Н	Н	L	1	Current Address	Suspend Burst Read Cycle
Н	Х	Х	Н	Н	L	1	Current Address	Suspend Burst Read Cycle

NOTE:

- 1. X means "Don't Care"
- 2. ECS = ECS1 and ECS2
- 3. The rising edge of clock is symbolized by 1
- 4. WRITE=L means Write operation in A-2. Synchronous Pipeline Butst Write Truth Table
 WRITE=H means Read operation in A-2. Synchronous Pipeline Butst Write Truth Table
- 5. Operation finally depends on status of asynchronous input pin (COE)

A-2. SYNCHRONOUS PIPELINE BURST WRITE TRUTH TABLE(Data field)

GWE	BWE	CWE[1:0]	CWE[3:2]	CWE[5:4]	CWE[7:6]	Operation
Н	Н	Х	Х	Х	Х	Read
Н	L	Н	Н	Н	Н	Read
Н	L	L	Н	Н	Н	Write Byte D[15:0]
Н	L	Н	L	н	Н	Write Byte D[31:16]
Н	L	Н	н	L	L	Write Byte D[63:32]
Н	L	L	L	L	L	Write All Bytes
L	Х	X	Х	Х	Х	Write All Bytes

NOTE:

- 1. X means "Don't Care"
- 2. All input in this table must meet setup and hold time around the rising edge of CLK(\uparrow).

B-1. ASYNCHRONOUS TRUTH TABLE(Tag field)

ECS	TWE	Mode	I/O Pin	Supply Current
Н	X*	Not Selest	HIGH-Z	ISB,ISB1
L	Н	Read	Dout	Icc
L	L	Write	Din	lcc

NOTE: X means "Don't Care"



C. BURST SEQUENCE

Addresses are generated for the burst access as shown below. The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the LBO pin. When this pin is Low, linear burst sequence is selected. When this pin is High, Interleaved burst sequence is selected.

INTERLEAVE BURST SEQUENCE TABLE

Pin 114 Pin state		Cas	se 1	Cas	se 2	Cas	se 3	Case 4 A1 A0 1 1 0 0 11	
*LBO	High	A1	A0	A1	A0	A1	A0	A1	A0
First Addres	s	0	0	0	1	1	0	1	1
Second Add	Iress	0	1	0	0	1	1	1	0
Third Addres	ss	1	0	1	1	0	0	0	1
Fouth Addre	ess	1	1	1	0	0	1	0	0

NOTE:

- 1. When this pin is no connects, LBO should be high.
- 2. Dafault is no connect for Intel processor based designs.

LINEAR BURST SEQUENCE TABLE

Pin 114 Pin state		Cas	ie 1	Cas	se 2	Ca	Case 3 Case 4		se 4
*LBO Low	Low	A1	A0	A1	A0	A1	A0	A1	A0
First Address	s	0	0	0	1	1	0	1	1
Second Add	ress	0	1	1	0	1	1	0	0
Third Addres	ss	1	0	1	1	0	0	0	1
Fouth Addre	ess	1	1	0	0	0	1	1	0

NOTE : $\overline{\text{LBO}}$ must be tied to low because this pin is pulled up with 4.7K \varOmega on the module.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Vcc3 Supply Relative to Vss	Vccз	-0.3 to 4.6	V
Voltage on Vcc5 Supply Relative to Vss	Vcc5	-0.3 to 6.0	V
Voltage on Any Other Pin Relative to Vss	Vin	-0.3 to 6.0	V
Storage Temperature	Тѕтс	-65 to 150	°C
Operating Temperature	TA	0 to 70	°C
Storage Temperature Range Under Bias	TBIAS	-10 to 85	°C

^{*} Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any outher conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.



OPERATING CONDITIONS (TA =0 to 70°C)

Parameter	Symbol	Min	Тур.	Max	Unit
Supply Voltage	Vccз	3.13	3.3	3.6	V
	VCC5	4.75	5.0	5.25	V
Ground	Vss	0	0	0	V
Input Low Voltage	VIL*	-0.3	-	0.8	V
Input High Voltage	ViH**	2.2	-	Vcc***+0.3	V

^{*} VIL3(min) = -1.4 (Pulse width ≤ 10ns), VIL5(min) = -2.0 (Pulse Width ≤ 10ns)

DC ELECTRICAL CHARACTERISTICS*(TA =0 to 70 °C, Vcc3=3.3V+10%/-5%)

Parameter	Symbol	Test Condition	S	Min	Max	Unit
Input Leakage current	iu**	Vcc3=Max, Vin=Vss to Vcc3	2.00	-5	5	μΑ
Output Leakage Current	ILO	Output Disable, VouT=Vss to Vcc	3	-5	5	μΑ
Operating Current	lcc	f=Max, 100% Duty	75MHz	-	400	mA
	100	VIN=VIH or VIL, IOUT=0mA	66MHz	-	360] "
Chandle Coment	1s _B	f=Max, 100% Duty, Device desele Vin=Vih or Vil., lout=0mA	-	80	mA	
Standby Current	ISB1	f=0MHz, Device deselected, Vin≥Vcc3-0.2V or ViL, Vin ≤ 0.2	V, Iout=0mA	-	10	mA
Output Low Voltage	Vol	IoL=8mA	-	0.4	V	
Output High Voltage	Voн	IOH=-4mA	2.4	-	V	

^{*} Excludes Tag field.

CAPACITANCE*(f=1MHz,TA=25°C)

Item	Symbol	Test Condition	Min.	Max.	Unit
Address, ECS Input Capacitance	CIN1	Vin=0V	-	35	pF
TWE, CWE, CLK Input Capacitance	CIN2	VIN=0V	-	20	pF
COE, ADSP, CADS, CADV, CCS GWE, BWE Input Capacitance	Сімз	Vin=0V	-	20	pF
Data and Tag Input/Output Capacitance	CI/O1	V1/0=0V	-	15	рF

^{*} NOTE: Capacitance is sampled and not 100% tested.



^{**} Vin3(max) = 5.0V (Pulse Width ≤ 10ns); In case of I/O pins, the maximum Vin3(max) = 4.1V (Pulse Width ≤ 10ns) Vin5(max) = 7.0V (Pulse Width ≤ 10ns)

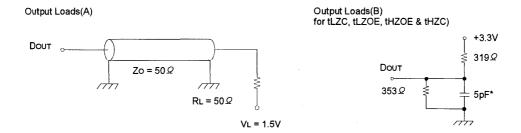
^{***} Vcc =Vcc3 or Vcc5

^{**} ILI for LBO, GWE, TIO(8,9,10) and BWE is ±1mA(Max.)

AC CHARACTERISTICS

TEST CONDITIONS ON DATA RAM (TA =0 to 70°C, Vcc3=3.3V+10%/-5%, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time (Measured at 0.3V and 2.7V)	2ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig 1

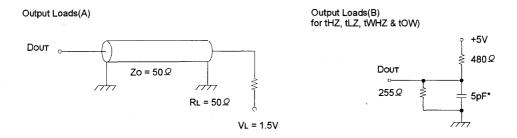


* Including Scope and Jig Capacitance

Fig. 1

TEST CONDITIONS ON TAG RAM (TA =0 to 70 °C, Vcc5=5.0V ± 5%, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time (Measured at 0.3V and 2.7V)	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig 1



* Including Scope and Jig Capacitance

Fig. 2



AC TIMING CHARACTERISTICS ON DATA RAM (TA =0 to 70°C, VCC3=3.3V+10%/-5%)

Refers to the individual components, not the whole module

Parameter	Symbol	KMM764V41AG2-13		KMM764V41AG2-15		
		Min	Max	Min	Max	Unit
Cycle Time	tCYC	13	-	15	-	ns
Clock Access Time	tCD	-	7	-	7	ns
Output Enable to Data Valid	tOE	-	6	-	6	ns
Clock High to Output Low-Z	tLZC	0	-	0	-	ns
Output Hold from Clock High	tOH	2.5	-	2.5	-	ns
Output Enable Low to Output Low-Z	tLZOE	0	-	0		ns
Output Enable High to Output High-Z	tHZOE	-	4	-	4	ns
Clock High to Output High-Z	tHZC	1.5	5	2.0	6	ns
Clock High Pulse Width	tCH	4.5	-	5.5	-	ns
Clock Low Pulse Width	tCL	4.5	-	5.5	-	ns
Address Setup to Clock High	tAS	2.5	-	2.5	-	ns
Address Status Setup to Cock High	tSS	2.5	-	2.5	-	ns
Data Setup to Cock High	tDS	2.5	-	2.5	-	ns
Write Setup to Clock High(GWE, BWE, CWEX)	tWS	2.5	-	2.5	-	ns
Address Advance Setup to Clock High	tADVS	2.5	-	2.5	-	ns
Chip Select Setup to Clock High	tCSS	2.5	-	2.5	-	ns
Address Hold from Clock High	tAH	0.5	-	0.5	-	ns
Address Status Hold from Clock High	tSH	0.5	-	0.5	-	ns
Data Hold from Clock High	tDH	0.5	-	0.5	-	ns
Write Hold from Clock High(GWE, BWE, CWEx)	tWH	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	tADVH	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	tCSH	0.5	-	0.5	-	ns
ZZ High to Power Down	tPDS	2	-	2	-	cycle
ZZ Low to Power Up	tPUS	2	-	2	-	cycle

NOTE

^{1.} All address inputs must meet the specified setup and hold times for all rising clock(Clk) edges whenever CADS and/or ADSP is sampled low and this device is chip selected.

All other synchronous inputs must meet the specified sample and hold times whenever this device is chip selected.

^{2.} Both chip selects must be active whenever CADS or ADSP is sampled low in order to the this device remained at enable.

^{3.} CADS or ADSP must not be asserted for at least 2 Clocks after leaving ZZ state.

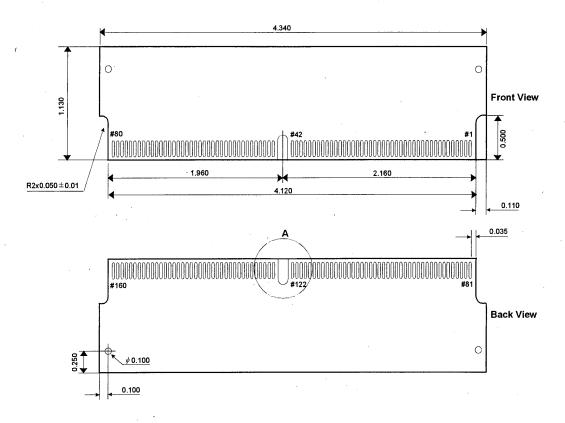
AC TIMING CHARACTERISTICS ON TAG RAM (TA =0 to 70 $^{\circ}$, Vcc5=5.0V \pm 5%)

Refers to the individual components, not the whole module

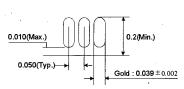
Parameter	Symbol	KMM764V41AG2-13		KMM764V41AG2-15		11
	Symbol	Min	Max	Min	Max	Unit
Read Cycle Time	tRC	12	-	15	-	ns
Address Access Time	tAA	-	12	-	15	ns
Chip Select to Output	tCO	-	12	-	15	ns
Chip Select to Low-Z Output	tLZ	3	-	3	-	ns
Chip Disable to High-Z Output	tHZ	0	6	0	7	ns
Output Hold from Address Change	tOH	3	-	3	-	ns
Write cycle Time	tWC	12	-	15	-	ns
Chip Select to End of Write	tCW	9	-	11	-	ns
Address Set-up Time	tAS	0	-	0	-	ns
Address Valid to End of Write	tAW	9	•	12	-	ns
Write Pulse Width	tWP	12	-	15	-	ns
Write Recovery Time	tWR	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	6	0	8	ns
Data to Write Time Overlap	tDW	7	-	8	-	ns
Data Hold from Write Time	tDH	0	-	0	-	ns
End Write to Output Low-Z	tOW	0	-	0	-	ns

PACKAGE DIMENSIONS

Units : Inches

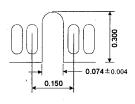


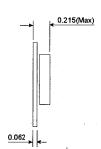




Tolerances: ± 0.005 unless otherwise specified

Detail of A





256KB Synchronous Pipelined Burst SRAM Module

FEATURES

- . Implemented based on COAST 3.1
- · Supports Interleave Burst and Linear Burst Mode
- Zero-wait-state operation at 75/66MHz
- · TTL compatible inputs/outputs
- Multiple ground pins and decoupling capacitors for maximum noise immunity
- · 160-pin DIMM with gold plated Tap
- · Series 22 ohm resistors for niose immunity
- Product Family: KMM764V41AG7-13/15

GENERAL DESCRIPTION

The KMM764V41AG7 is 256K byte high-frequency Synchronous Pipelined Burst Static Random Access Memory module organized as 32K words by 64 bits. The module is designed specially to function as the secondary cache in Pentium and Power PC-based systems. The device for this module is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. The module uses two of SAMSUNG's KM732V589AG and one KM68257C for 8bits tag ROM

PIN NAMES

Pin Name	Pin Function
CLK[1:0]	Clock Inputs
A[18:3]	Cache RAM Address Inputs
D[63:0]	Cache RAM Data Inputs/Outputs
TIO[7:0]	Tag RAM Data Inputs/Outputs
TWE	Tag RAM Write Enable Input
ECS[2:1]	Chip Select Inputs for Depth Expansion
CCS	Chip Select Input
CWE[7:0]	Write Enable Inputs
COE	Output Enable Input
ADSP	Address Status Processor
CADS	Address Status Controller
CADV	Burst Address Advance
BWE	Byte Write Enable Input
GWE	Grobal Write Enable Input
LBO	Burst Mode Control
VCC5	Power Supply(5V)
Vccз	Power Supply(3.3V)
Vss	Ground
N.C	No Connection

PD PIN INFORMATION

	PD Pin A	llocation		Module Part No
PD3	PD2	PD1	PD ₀	module (art 100
N.C	Vss	N.C	N.C	KMM764V41AG7

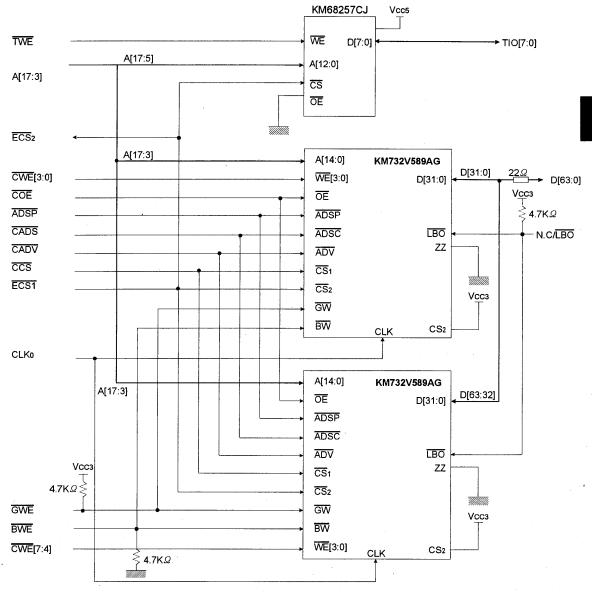
PIN CONFIGURATION(Top View)

			ı		,		
Vss	81	1	Vss	D57	122	42	D56
TIO ₁	82	2	TIO ₀				
TIO7	83	3	TIO ₂				
TIO5	84	4	TIO ₆	Vss	123	43	Vss
TIO3	85	5	TIO ₄	D55	124	44	D54
N.C	86	6	N.C	D53	125	45	D52
Vcc5	87	7	Vcc3	D51	126	46	D50
N.C	88	8	TWE	D49	127	47	D48
CADV	89	9	CADS	Vss	128	48	Vss
Vss	90	10	Vss	D47	129	49	D46
COE	91	11	CWE₄	D45	130	50	D44
CWE ₅	92	12	CWE ₆	D43	131	51	D42
CWE ₇	93	13	CWE₀	Vcc5	132	52	Vccs
CWE ₁	94	14	CWE₂	D41	133	53	D40
Vcc5	95	15	Vcc3	D39	134	54	Dзв
CWE ₃	96	16	ccs	D37	135	55	D36
N.C	97	17	GWE(3)	Vss	136	56	Vss
N.C	98	18	BWE(3)	D35	137	57	D34
Vss	99	19	Vss	D33	138	58	D32
N.C	100	20	Аз	D31	139	59	D30
A4	101	21	A 7	Vcc5	140	60	Vccs
A6	102	22	A5	D29	141	61	D28
, Aa	103	23	A11	D27	142	62	D26
A10	104	24	A16	D ₂₅	143	63	D24
Vcc5	105	25	Vcc3	Vss	144	64	Vss
A17	106	26	A18(1)	D23	145	65	D22
Vss	107	27	Vss	D21	146	66	D20
A9	108	28	A12	D19	147	67	D18
A14	109	29	A13	Vccs	148	68	Vccs
A15	110	30	ADSP	D17	149	69	D16
N.C	111	31	ECS ₁	D15	150	70	D14
PD₀	112	32	ECS ₂	D13	151	71	D12
PD2	113	33	PD ₁	Vss	152	72	Vss
LBO(2)	114	34	PD3	D11	153	73	D10
Vss	115	35	Vss	D₃	154	74	Dθ
CLK₀	116	36	CLK ₁ (1)	D7	155	75	D ₆
Vss	117	37	Vss	Vcc5	156	76	Vccs
D63	118	38	D62	D5	157	77	D4
Vcc5	119	39	Vccs	D₃	158	78	D2
D61	120	30	D60	D1	159	79	D ₀
D59	121	41	D58	Vss	160	80	Vss

- These pins are used for 512KB module only and they should be no connect for this module.
- 2. Default is no connect for Intel processor based designs becouse this pin pulled up with 4.7Kohm resistor on the module.
- When these pins are no connect, all byte write should be controlled by all CWEx pins.

FUNCTIONAL BLOCK DIAGRAM

KMM764V41AG7



NOTE

- 1. ZZ pin is internally connected to Vss and not pinout on the module.
- 2. LBO is pulled up with 4.7Kohm resistor.
- 3. GWE is pulled up with 4.7Kohm resistor and BWE is pulled down with 4.7Kohm resistor.



A-1. SYNCHRONOUS PIPELINE BURST TRUTH TABLE(Data field)

CCS	ECS	ADSP	CADS	CADV	WRITE	К	Address Accessed	Operation
Н	X*	Х	L	Х	Х	1	N/A	Not Selected
L	Х	L	Х	Х	Х	1	N/A	Not Selected
L	Н	L	Х	Х	Х	1	N/A	Not Selected
L	X	Х	L	Х	Х	1	N/A	Not Selected
L	Н	Х	L	Х	Х	1	N/A	Not Selected
L	L	L	Х	Х	Х	1	External Address	Begin Burst Read Cycle
L	L	Н	L	Х	L	1	External Address	Begin Burst Read Cycle
L	L	Н	L	Х	Н	1	External Address	Begin Burst Read Cycle
X	Х	Н	Н	L	Н	1	Next Address	Continue Burst Read Cycle
Н	Х	Х	Н	L	Н	1	Next Address	Continue Burst Read Cycle
Х	Х	Н	Н	L	L	1	Next Address	Continue Burst Read Cycle
Н	Х	Х	Н	L	L	1	Next Address	Continue Burst Read Cycle
Х	Х	Н	Н	Н	Н	1	Current Address	Suspend Burst Read Cycle
Н	Х	Х	Н	Н	Н	1	Current Address	Suspend Burst Read Cycle
Х	Х	Н	Н	Н	L	1	Current Address	Suspend Burst Read Cycle
Н	Х	Х	Н	Н	L	1	Current Address	Suspend Burst Read Cycle

NOTE:

- 1. X means "Don't Care"
- 2. ECS = ECS1 and ECS2
- WRITE=L means Write operation in A-2. Synchronous Pipeline Butst Write Truth Table WRITE=H means Read operation in A-2. Synchronous Pipeline Butst Write Truth Table
- 5. Operation finally depends on status of asynchronous input pin $(\overline{\text{COE}})$

A-2. SYNCHRONOUS PIPELINE BURST WRITE TRUTH TABLE(Data field)

GWE	BWE	CWE[1:0]	CWE[3:2]	CWE[5:4]	CWE[7:6]	Operation
Н	Н	Х	Х	Х	Х	Read
Н	L	Н	Н	н	н	Read
Н	L	L	Н	Н	Н	Write Byte D[15:0]
Н	L	Н	L.	Н	Н	Write Byte D[31:16]
Н	L	Н	Н	L	L	Write Byte D[63:32]
Н	L	L	L	L	L	Write All Bytes
L	Х	Х	Х	Х	Х	Write All Bytes

NOTE:

- 1. X means "Don't Care"
- 2. All input in this table must meet setup and hold time around the rising edge of CLK(\uparrow).

B-1. ASYNCHRONOUS TRUTH TABLE(Tag field)

ECS	TWE	Mode	I/O Pin	Supply Current
н	X*	Not Selest	HIGH-Z	ISB,ISB1
L	Н	Read	Dout	lcc
L	L	Write	DIN	lcc ·

NOTE: X means "Don't Care"



C. BURST SEQUENCE

Addresses are generated for the burst access as shown below. The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the $\overline{\text{LBO}}$ pin. When this pin is Low, linear burst sequence is selected. When this pin is High, Interleaved burst sequence is selected.

INTERLEAVE BURST SEQUENCE TABLE

Pin 114	Pin state	Cas	ie 1	Cas	ie 2	Cas	se 3	Ca	se 4
*LBO	High	A1	A0	A1	A0	A1	A0	A1	A0
First Addres	S	0	0	0	1	1	0	1	1
Second Add	ress	0	1	0	0	1	1	1	0
Third Addres	ss	1	0	1	1	0	0	0	1
Fouth Addre	ss	1	1	1	0	0	1	0	0

NOTE:

- 1. When this pin is no connects, LBO should be high.
- 2. Dafault is no connect for Intel processor based designs.

LINEAR BURST SEQUENCE TABLE

Pin 114	Pin state	Cas	se 1	Cas	se 2	Cas	se 3	Ca	se 4
*LBO	Low	A1	A0	A1	A0	A1	A0	A1	A0
First Address Second Addr Third Addres Fouth Addres	ess s	0 0 1 1	0 1 0 1	0 1 1 0	1 0 1 0	1 1 0 0	0 1 0 1	1 0 0 1	1 0 1 0

NOTE : $\overline{\text{LBO}}$ must be tied to low because this pin is pulled up with 4.7K Ω on the module.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Vcc3 Supply Relative to Vss	Vccз	-0.3 to 4.6	V
Voltage on Vccs Supply Relative to Vss	Vcc5	-0.3 to 6.0	٧
Voltage on Any Other Pin Relative to Vss	Vin	-0.3 to 6.0	V :
Storage Temperature	Тѕтв	-65 to 150	°C
Operating Temperature	TA	0 to 70	°
Storage Temperature Range Under Bias	TBIAS	-10 to 85	°C

^{*} Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any outher conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.



OPERATING CONDITIONS (TA =0 to 70°C)

Parameter	Symbol	Min	Тур.	Max	Unit
Supply Voltage	Vccз	3.13	3.3	3.6	V
	Vcc5	4.75 ⁻	5.0	5.25	٧
Ground	Vss	0	0	0	V
Input Low Voltage	VIL*	-0.3	-	0.8	V
Input High Voltage	ViH**	2.2	-	Vcc***+0.3	V

^{*} VIL3(min) = -1.4 (Pulse width ≤ 10ns), VIL5(min) = -2.0 (Pulse Width ≤ 10ns)

DC ELECTRICAL CHARACTERISTICS*(TA =0 to 70°, Vcc3=3.3V+10%/-5%)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage current	lu**	Vcc3=Max, Vin=Vss to Vcc3	-5	5	μΑ	
Output Leakage Current	ILO	Output Disable, VouT=Vss to Vcc3		-5	5	μΑ
		f=Max, 100% Duty	75MHz	-	400	mA
Operating Current	lcc	VIN=VIH or VIL, IOUT=0mA	66MHz	-	360	"'
İSB		f=Max, 100% Duty, Device deseled VIN=VIH or VIL, IOUT=0mA	-	80	mA	
Standby Current	ISB1	f=0MHz, Device deselected, Vin≥Vcc3 -0.2V or ViL, Vin ≤ 0.2V	-	10	mA	
Output Low Voltage	Vol	IoL=8mA	-	0.4	V	
Output High Voltage	Voн	IOH=-4mA		2.4	-	V

^{*} Excludes Tag field.

CAPACITANCE*(f=1MHz,TA=25°C)

Item	Symbol	Test Condition	Min.	Max.	Unit
Address, ECS Input Capacitance	CIN1	VIN=0V	-	35	pF
TWE, CWE, CLK Input Capacitance	CIN2	Vin=0V	-	20	pF
COE, ADSP, CADS, CADV, CCS GWE, BWE Input Capacitance	Сімз	VIN=0V	-	20	pF
Data and Tag Input/Output Capacitance	CI/01	VI/0=0V	-	15	pF

^{*} NOTE : Capacitance is sampled and not 100% tested.



^{**} VIH3(max) = 5.0V (Pulse Width \leq 10ns); In case of I/O pins, the maximum VIH3(max) = 4.1V (Pulse Width \leq 10ns)

V_{IH5}(max) = 7.0V (Pulse Width ≤ 10ns)

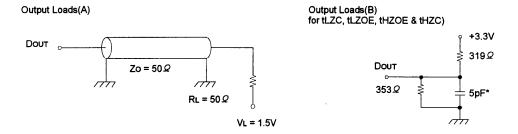
^{***} Vcc =Vcc3 or Vcc5

^{**} ILI for LBO, GWE and BWE is ±1mA(Max.)

AC CHARACTERISTICS

TEST CONDITIONS ON DATA RAM (TA =0 to 70°C,Vcc3=3.3V+10%/-5%, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time (Measured at 0.3V and 2.7V)	2ns .
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig 1

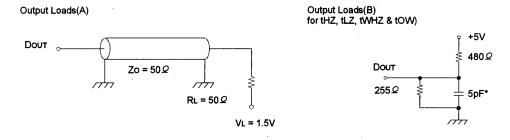


* Including Scope and Jig Capacitance

Fig. 1

TEST CONDITIONS ON TAG RAM (TA =0 to 70 $^{\circ}$ C,Vcc5=5.0V $^{\pm}$ 5%, unless otherwise specified.)

Parameter .	¹ Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time (Measured at 0.3V and 2.7V)	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig 1



* Including Scope and Jig Capacitance

Fig. 2



AC TIMING CHARACTERISTICS ON DATA RAM (TA =0 to 70°, VCC3=3.3V+10%/-5%)

Refers to the individual components, not the whole module

Parameter	Sumbel	KMM764	/41AG7-13	KMM764\	/41AG7-15	Unit
Parameter	Symbol	Min	Max	Min	Max	Unit
Cycle Time	tCYC	13	-	15	-	ns
Clock Access Time	tCD	-	7	-	7	ns
Output Enable to Data Valid	tOE	-	6	-	6	ns
Clock High to Output Low-Z	tLZC	0	-	0	-	ns
Output Hold from Clock High	tOH	2.5	-	2.5	-	ns
Output Enable Low to Output Low-Z	tLZOE	0	-	0	-	ns
Output Enable High to Output High-Z	tHZOE	-	4	-	4	ns
Clock High to Output High-Z	tHZC	1.5	5	2.0	6	ns
Clock High Pulse Width	tCH	4.5	-	5.5	-	ns
Clock Low Pulse Width	tCL	4.5	-	5.5	-	ns
Address Setup to Clock High	tAS	2.5	-	2.5	-	ns
Address Status Setup to Cock High	tSS	2.5	-	2.5	-	ns
Data Setup to Cock High	tDS	2.5	-	2.5	- 1	ns
Write Setup to Clock High(GWE, BWE, CWEx)	tWS	2.5	-	2.5	-	ns
Address Advance Setup to Clock High	tADVS	2.5	-	2.5	-	ns
Chip Select Setup to Clock High	tCSS	2.5	-	2.5	-	ns
Address Hold from Clock High	tAH	0.5	-	0.5	-	ns
Address Status Hold from Clock High	tSH	0.5	-	0.5	-	ns
Data Hold from Clock High	tDH	0.5	-	0.5	-	ns
Write Hold from Clock High(GWE, BWE, CWEx)	tWH	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	tADVH	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	tCSH	0.5	_	0.5	-	ns
ZZ High to Power Down	tPDS	2		2	-	cycle
ZZ Low to Power Up	tPUS	2	-	2	-	cycle

^{1.} All address inputs must meet the specified setup and hold times for all rising clock(Clk) edges whenever CADS and/or ADSP is sampled low and this device is chip selected.

All other synchronous inputs must meet the specified sample and hold times whenever this device is chip selected.

^{2.} Both chip selects must be active whenever CADS or ADSP is sampled low in order to the this device remained at enable.

^{3.} CADS or ADSP must not be asserted for at least 2 Clocks after leaving ZZ state.

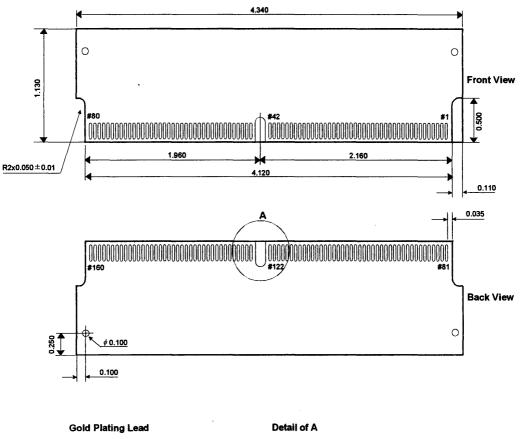
AC TIMING CHARACTERISTICS ON TAG RAM (TA =0 to 70 $^{\circ}$, Vcc5=5.0V $^{\pm}$ 5%)

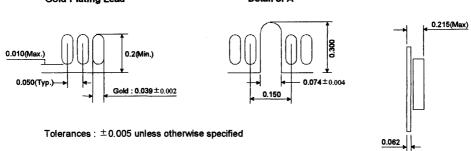
Refers to the individual components, not the whole module

Parameter	Symbol	KMM764\	/41AG7-13	KMM764\	/41AG7-15	Unit
Parameter	Symbol	Min	Max	Min	Max	Unit
Read Cycle Time	tRC	12	-	15	-	ns
Address Access Time	tAA	-	12	-	15	ns
Chip Select to Output	tCO	-	12	-	15	ns
Chip Select to Low-Z Output	tLZ	3	-	3	-	ns
Chip Disable to High-Z Output	tHZ	0	6	0	7	ns
Output Hold from Address Change	tOH	3	-	3	-	ns
Write cycle Time	tWC	12	-	15	-	ns
Chip Select to End of Write	tCW	9	-	11	-	ns
Address Set-up Time	tAS	0	-	0	-	ns
Address Valid to End of Write	tAW	9	-	12	- 1	ns
Write Pulse Width	tWP	12	-	15	-	ns
Write Recovery Time	tWR	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	6	0	8	ns
Data to Write Time Overlap	tDW	7	-	8	-	ns
Data Hold from Write Time	tDH	0	-	0	-	ns
End Write to Output Low-Z	tOW	0	-	0	-	ns

PACKAGE DIMENSIONS

Units: Inches





256KB Synchronous Pipelined Burst SRAM Module

FEATURES

- . Implemented based on COAST 3.1
- . Supports Interleave Burst and Linear Burst Mode
- · Zero-wait-state operation at 75/66MHz
- . TTL compatible inputs/outputs
- Multiple ground pins and decoupling capacitors for maximum noise immunity
- . 160-pin DIMM with gold plated Tap
- · Series 22 ohm resistors for niose immunity
- Product Family: KMM764V45AG-13/15

GENERAL DESCRIPTION

The KMM764V45AG7 is 256K byte high-frequency Synchronous Pipelined Burst Static Random Access Memory module organized as 32K words by 64 bits. The module is designed specially to function as the secondary cache in Pentium and Power PC-based systems. The component on this module is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. The module uses two of SAMSUNG's KM732V589AG and one KM68257C for 11bits tag RAM.

PIN NAMES

Pin Name	Pin Function
CLK[1:0]	Clock inputs
A[18:3]	Cache RAM Address Inputs
D[63:0]	Cache RAM Data Inputs/Outputs
TIO[7:0]	Tag RAM Data Inputs/Outputs
TWE	Tag RAM Write Enable Input
ECS[2:1]	Chip Select Inputs for Depth Expansion
CCS	Chip Select Input
CWE[7:0]	Write Enable Inputs
COE	Output Enable Input
ADSP	Address Status Processor
CADS	Address Status Controller
CADV	Burst Address Advance
BWE	Byte Write Enable Input
GWE	Grobal Write Enable Input
LBO	Burst Mode Control
Vcc5	Power Supply(5V)
Vccз	Power Supply(3.3V)
Vss	Ground
N.C	No Connection

PD PIN INFORMATION

	PD Pin A	Allocation	1	Module Part No
PD3	PD2	PD1	PD ₀	Module Fait No
N.C	Vss	N.C	N.C	KMM764V45AG

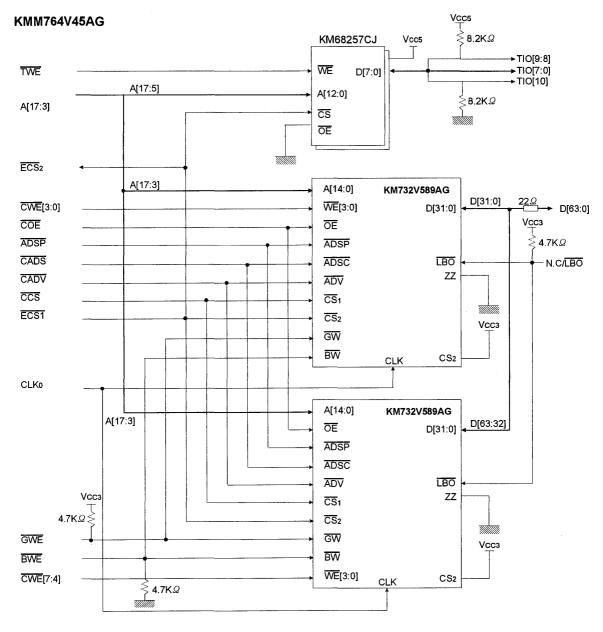
PIN CONFIGURATION(Top View)

			,				•
Vss	81	1	Vss	D57	122	42	D56
TIO ₁	82	2	TIO₀				
TIO ₇	83	3	TIO ₂		l		
TIO₅	84	4	TIO ₆	Vss	123	43	Vss
TIO ₃	85	5	TIO ₄	D55	124	44	D54
TIOs	86	6	TIOs	D53	125	45	D52
Vcc5	87	7	Vccs	D51	126	46	D50
TIO ₁₀	88	8	TWE	D49	127	47	D48
CADV	89	9	CADS	Vss	128	48	Vss
Vss	90	10	Vss	D47	129	49	D46
COE	91	11	CWE₄	D45	130	50	D44
CWE ₅	92	12	CWE ₆	D43	131	51	D42
CWE ₇	93	13	CWE₀	Vcc5	132	52	Vcc3
CWE ₁	94	14	CWE ₂	D41	133	53	D40
Vcc5	95	15	Vccs	D39	134	54	D38
CWE ₃	96	16	CCS	D37	135	55	D36
N.C	97	17	GWE(3)	Vss	136	56	Vss
N.C	98	18	BWE(3)	D35	137	57	D34
Vss	99	19	Vss	D33	138	58	D32
N.C	100	20	Аз	D31	139	59	D30
A4	101	21	A7	Vcc5	140	60	Vccs
A6	102	22	A ₅	D29	141	61	D28
Ав	103	23	A11	D27	142	62	D26
A10	104	24	A16	D25	143	63	D24
Vcc5	105	25	Vccs	Vss	144	64	Vss
A17	106	26	A18(1)	D23	145	65	D22
Vss	107	27	Vss	D21	146	66	D20
Ae	108	28	A12	D19	147	67	D18
A14	109	29	A13	Vcc5	148	68	Vccs
A15	110	30	ADSP	D17	149	69	D16
N.C	111	31	ECS ₁	D15	150	70	D14
PD₀	112	32	ECS₂	D13	151	71	D12
PD₂	113	33	PD ₁	Vss	152	72	Vss
LBO(2)	114	34	PD ₃	D11	153	73	D10
Vss	115	35	Vss	D∍	154	74	Ds
CLK₀	116	36	CLK ₁ (1)	D7	155	75	De
Vss	117	37	Vss	Vcc5	156	76	Vcc3
D63	118	38	D62	D5	157	77	D ₄
Vcc5	119	39	Vccs	Dз	158	78	D ₂
D61	120	30	D60	D1	159	79	D ₀
D59	121	41	D58	Vss	160	80	Vss
				1			

- These pins are used for 256KB module only and they should be no connect for this module.
- Default is no connect for Intel processor based designs becouse this pin pulled up with 4.7Kohm resistor on the module.
- When these pins are no connect, all byte write should be controlled by all CWEx pins.



FUNCTIONAL BLOCK DIAGRAM



- 1. ZZ pin is internally connected to Vss and not pinout on the module.
- 2. LBO is pulled up with 4.7Kohm resistor.
- 3. $\overline{\text{GWE}}$ is pulled up with 4.7Kohm resistor and $\overline{\text{BWE}}$ is pulled down with 4.7Kohm resistor.



A-1. SYNCHRONOUS PIPELINE BURST TRUTH TABLE(Data field)

ccs	ECS	ADSP	CADS	CADV	WRITE	K	Address Accessed	Operation
Н	X*	Х	L	Х	Х	1	N/A	Not Selected
L	Х	L	Х	Х	Х	1	N/A Not Selected	
L	Н	L	X	Х	Х	1	N/A	Not Selected
L	Х	X	L	Х	Х	1	N/A	Not Selected
L	Н	Х	L	Х	Х	1	N/A	Not Selected
L	L	L	Х	Х	Х	1	External Address	Begin Burst Read Cycle
L	L	Н	L	Х	L	1	External Address	Begin Burst Read Cycle
L	L	H	L	Х	Н	1	External Address	Begin Burst Read Cycle
X	Х	Н	Н	L	Н	1	Next Address	Continue Burst Read Cycle
Н	Х	Х	Н	L	Н	1	Next Address	Continue Burst Read Cycle
Х	Х	Н	Н	L	L	1	Next Address	Continue Burst Read Cycle
Н	Х	Х	Н	L	L	1	Next Address	Continue Burst Read Cycle
Х	Х	Н	Н	Н	Н	1	Current Address	Suspend Burst Read Cycle
Н	Х	X	Н	Н	Н	1	Current Address	Suspend Burst Read Cycle
X	Х	Н	Н	Н	L	1	Current Address	Suspend Burst Read Cycle
Н	Х	Х	Н	Н	L	1	Current Address	Suspend Burst Read Cycle

NOTE:

- 1. X means "Don't Care"
- 2. ECS = ECS1 and ECS2
- 3. The rising edge of clock is symbolized by 1
- WRITE=L means Write operation in A-2. Synchronous Pipeline Butst Write Truth Table WRITE=H means Read operation in A-2. Synchronous Pipeline Butst Write Truth Table
- 5. Operation finally depends on status of asynchronous input pin (COE)

A-2. SYNCHRONOUS PIPELINE BURST WRITE TRUTH TABLE(Data field)

GWE	BWE	CWE[1:0]	CWE[3:2]	CWE[5:4]	CWE[7:6]	Operation
Н	Н	X	Х	Х	X	Read
Н	L	Н	Н	Н	Н	Read
Н	L	L	Н	Н	Н	Write Byte D[15:0]
Н	L	Н	L	Н	Н	Write Byte D[31:16]
Н	L	Н	Н	L	L	Write Byte D[63:32]
Н	L	L	L	L	L	Write All Bytes
L	Х	X	Х	Х	Х	Write All Bytes

NOTE:

- 1. X means "Don't Care"
- 2. All input in this table must meet setup and hold time around the rising edge of CLK(\uparrow).

B-1. ASYNCHRONOUS TRUTH TABLE(Tag field)

ECS	TWE	Mode	I/O Pin	Supply Current
Н	X*	Not Selest	HIGH-Z	ISB,ISB1
L	Н	Read	Dout	Icc
L	L	Write	DIN	Icc

NOTE: X means "Don't Care"



KMM764V45AG

C. BURST SEQUENCE

Addresses are generated for the burst access as shown below. The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the $\overline{\text{LBO}}$ pin. When this pin is Low, linear burst sequence is selected. When this pin is High, Interleaved burst sequence is selected.

INTERLEAVE BURST SEQUENCE TABLE

Pin 114	Pin state	Cas	se 1	Cas	se 2	Cas	se 3	Cas	ie 4
*LBO	High	. A1	A0	A1	A0	A1	A0	A1	A0
First Address Second Address Third Address Fouth Address	ress s	0 0 1 1	0 1 0 1	0 0 1 1	1 0 1 0	1 1 0	0 1 0 1	1 1 0 0	1 0 1 0

NOTE:

- 1. When this pin is no connects, LBO should be high.
- 2. Dafault is no connect for Intel processor based designs.

LINEAR BURST SEQUENCE TABLE

Pin 114	Pin state	Cas	ie 1	Cas	se 2	Cas	se 3	Cas	se 4
* LBO	Low	A1	A0	A1	A0	A1	A0	A1	A0
First Address Second Address Third Address Fouth Addres	ess S	0 0 1 1	0 1 0 1	0 1 1 0	1 0 1 0	1 1 0	0 1 0 1	1 0 0 1	1 0 1 0

NOTE: $\overline{\text{LBO}}$ must be tied to low because this pin is pulled up with 4.7K Ω on the module.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Vcc3 Supply Relative to Vss	Vccз	-0.3 to 4.6	V
Voltage on Vcc5 Supply Relative to Vss	Vcc5	-0.3 to 6.0	V
Voltage on Any Other Pin Relative to Vss	Vin	-0.3 to 6.0	V
Storage Temperature	Тѕтс	-65 to 150	°C
Operating Temperature	TA	0 to 70	°C
Storage Temperature Range Under Bias	TBIAS	-10 to 85	°C

^{*} Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any outher conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.



OPERATING CONDITIONS (TA =0 to 70°C)

Parameter	Symbol	Min	Тур.	Max	Unit
Supply Voltage	Vcc3	3.13	3.3	3.6	V
	Vcc5	4.75	5.0	5.25	V
Ground	Vss	0	0	0	V
Input Low Voltage	VIL*	-0.3	_	0.8	V
Input High Voltage	VIH**	2.2	-	Vcc***+0.3	V

^{*} $V_{IL3}(min) = -1.4$ (Pulse width ≤ 10 ns), $V_{IL5}(min) = -2.0$ (Pulse Width ≤ 10 ns)

DC ELECTRICAL CHARACTERISTICS*(TA =0 to 70 °C,Vcc3=3.3V+10%/-5%)

Parameter	Symbol	Test Condition	S	Min	Max	Unit
Input Leakage current	l⊔**	Vcc3=Max, Vin=Vss to Vcc3		-5	5	μΑ
Output Leakage Current	ILO	Output Disable, Vour=Vss to Vcc	3	-5	5	μΑ
0		f=Max, 100% Duty	75MHz	-	400	mA
Operating Current	lcc	VIN=VIH or VIL, IOUT=0mA	66MHz	-	360	mA
Ctandhy Current	IsB f=Max, 100% Duty, Device deselected, Vin=Vin or Vil, Iout=0mA		ected,	-	80	mA
Standby Current Ise		f=0MHz, Device deselected, Vin≥Vcc3 -0.2V or ViL, Vin ≤ 0.2	-	10	mA	
Output Low Voltage	Vol	IoL=8mA	-	0.4	V	
Output High Voltage	Voн	loн=-4mA	2.4	-	V	

^{*} Excludes Tag field.

CAPACITANCE*(f=1MHz,TA=25°C)

Item	Symbol	Test Condition	Min.	Max.	Unit
Address, ECS Input Capacitance	CIN1	Vin=0V	-	35	pF
TWE, CWE, CLK Input Capacitance	CIN2	Vin=0V	-	20	pF
COE, ADSP, CADS, CADV, CCS GWE, BWE Input Capacitance	Сінз	V0=nIV	-	20	pF
Data and Tag Input/Output Capacitance	CI/O1	VI/O=0V	-	15	pF

^{*} NOTE : Capacitance is sampled and not 100% tested.



^{**} VH3(max) = 5.0V (Pulse Width \leq 10ns); In case of I/O pins, the maximum VH3(max) = 4.1V (Pulse Width \leq 10ns) VH3(max) = 7.0V (Pulse Width \leq 10ns)

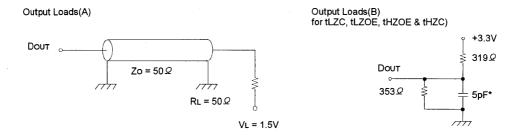
^{***} Vcc =Vcc3 or Vcc5

^{**} ILI for LBO, GWE and BWE is ±1mA(Max.)

AC CHARACTERISTICS

TEST CONDITIONS ON DATA RAM (TA =0 to 70°C, Vcc3=3.3V+10%/-5%, unless otherwise specified.)

	· · · · · · · · · · · · · · · · · · ·
Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time (Measured at 0.3V and 2.7V)	2ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig 1

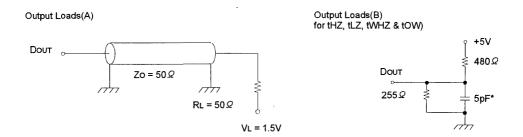


* Including Scope and Jig Capacitance

Fig. 1

TEST CONDITIONS ON TAG RAM (TA =0 to 70 °C, Vcc5=5.0V ± 5%, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time (Measured at 0.3V and 2.7V)	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig 1



* Including Scope and Jig Capacitance

Fig. 2



AC TIMING CHARACTERISTICS ON DATA RAM (TA =0 to 70°C, VCC3=3.3V+10%/-5%)

Refers to the individual components, not the whole module

Parameter	Symbol	KMM764V41AG7-13		KMM764V41AG7-15		Unit
Farameter	Symbol	Min	Max	Min	Max	Unit
Cycle Time	tCYC	13	-	15	-	ns
Clock Access Time	tCD	-	7	-	7	ns
Output Enable to Data Valid	tOE	-	6	-	6	ns
Clock High to Output Low-Z	tLZC	0	-	0	-	ns
Output Hold from Clock High	tOH	2.5	-	2.5	-	ns
Output Enable Low to Output Low-Z	tLZOE	0	-	0	· <u>-</u>	ns
Output Enable High to Output High-Z	tHZOE	-	4	-	4	ns
Clock High to Output High-Z	tHZC	1.5	5	2.0	6	ns
Clock High Pulse Width	tCH	4.5	-	5.5	-	ns
Clock Low Pulse Width	tCL	4.5	-	5.5	-	ns
Address Setup to Clock High	tAS	2.5	-	2.5	-	ns
Address Status Setup to Cock High	tSS	2.5	-	2.5	-	ns
Data Setup to Cock High	tDS	2.5	-	2.5	-	ns
Write Setup to Clock High(GWE, BWE, CWEx)	tWS	2.5	-	2.5	-	ns
Address Advance Setup to Clock High	tADVS	2.5	-	2.5	-	ns
Chip Select Setup to Clock High	tCSS	2.5	-	2.5	-	ns
Address Hold from Clock High	tAH	0.5	-	0.5	-	ns
Address Status Hold from Clock High	tSH	0.5	-	0.5	-	ns
Data Hold from Clock High	tDH	0.5	-	0.5	-	ns
Write Hold from Clock High(GWE, BWE, CWEx)	tWH	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	tADVH	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	tCSH	0.5	-	0.5	-	ns
ZZ High to Power Down	tPDS	2	-	2	-	cycle
ZZ Low to Power Up	tPUS	2	-	2	-	cycle

NOTE

^{1.} All address inputs must meet the specified setup and hold times for all rising clock(Clk) edges whenever CADS and/or ADSP is sampled low and this device is chip selected.

All other synchronous inputs must meet the specified sample and hold times whenever this device is chip selected.

^{2.} Both chip selects must be active whenever CADS or ADSP is sampled low in order to the device remained at enable.

^{3.} CADS or ADSP must not be asserted for at least 2 Clocks after leaving ZZ state.

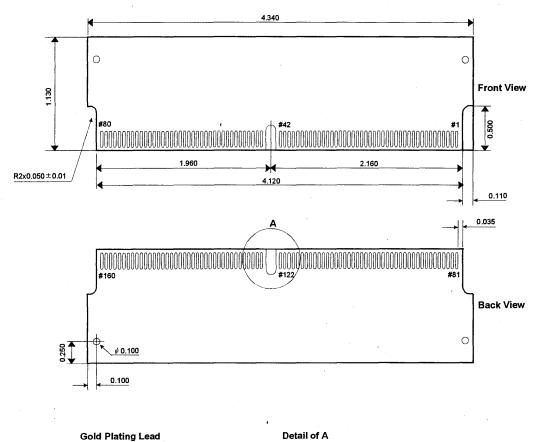
AC TIMING CHARACTERISTICS ON TAG RAM (TA =0 to 70 $^{\circ}\text{C,Vcc5=5.0V} \pm 5\%)$

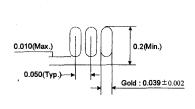
Refers to the individual components, not the whole module

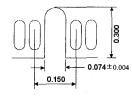
Parameter	Symbol	KMM764\	/41AG7-13	KMM764V41AG7-15		
Parameter	Symbol	Min	Max	Min	Max	Unit
Read Cycle Time	tRC	12	-	15		ns
Address Access Time	tAA	-	12	-	15	ns
Chip Select to Output	tCO	-	12	-	15	ns
Chip Select to Low-Z Output	tLZ	3	-	3	-	ns
Chip Disable to High-Z Output	tHZ	0	6	0	7	ns
Output Hold from Address Change	tOH	3	-	3	- 1	ns
Write cycle Time	tWC	12	-	15	-	ns
Chip Select to End of Write	tCW	9	-	11	-	ns
Address Set-up Time	tAS	0	-	0	-	ns
Address Valid to End of Write	tAW	9	-	12	-	ns
Write Pulse Width	tWP	12	-	15	-	ns
Write Recovery Time	tWR	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	6	0	8	ns
Data to Write Time Overlap	tDW	7	-	8	-	ns
Data Hold from Write Time	tDH	0	-	0	-	ns
End Write to Output Low-Z	tOW	0	-	0	-	ns

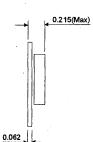
PACKAGE DIMENSIONS

Units: Inches









Tolerances : ± 0.005 unless otherwise specified

512KB SPB SRAM Module (Single Bank Operation)

FEATURES

- . Implemented based on COAST 1.4
- · Supports Interleave Burst and Linear Burst Mode
- · Single Bank Operation
- · Zero-wait-state operation at 75/66MHz
- · TTL compatible inputs/outputs
- Multiple ground pins and decoupling capacitors for maximum noise immunity
- · 160-pin DIMM with gold plated Tap
- · PCB: Height (1130mil)
- Product Family: KMM764V72G2-13/15

GENERAL DESCRIPTION

The KMM764V72G2 is 512K byte high-frequency Synchronous Pipelined Burst Static Randomd Access Memory module organized as 64K words by 64 bits. The module is designed specially to function as the secondary cache in Pentium, K5,M1, and Power PC-based systems and using SAMSUNG's PCB design tool. The device for this module is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology.

PIN NAMES

Pin Name	Pin Function
CLK[1:0]	Clock Inputs
A[18:3]	Cache RAM Address Inputs
D[63:0]	Cache RAM Data Inputs/Outputs
TIO[7:0]	Tag RAM Data Inputs/Outputs
TWE	Tag RAM Write Enable Input
ECS[2:1]	Chip Select Inputs for Depth Expansion
ccs	Chip Select Input
CWE [7:0]	Write Enable Inputs
COE	Output Enable Input
ADSP	Address Status Processor
CADS	Address Status Controller
CADV	Burst Address Advance
BWE	Byte Write Enable Input
GWE	Grobal Write Enable Input
LBO	Burst Mode Control
VCC5	Power Supply(5V)
Vccз	Power Supply(3.3V)
Vss	Ground
N.C	No Connections

PD PIN INFORMATION

	PD Pin A	llocation		Module Part No
PD3	PD2	PD1	PD0	module rait no
Vss	N.C	N.C	N.C	KMM764V72G2

PIN CONFIGURATION(Top View)

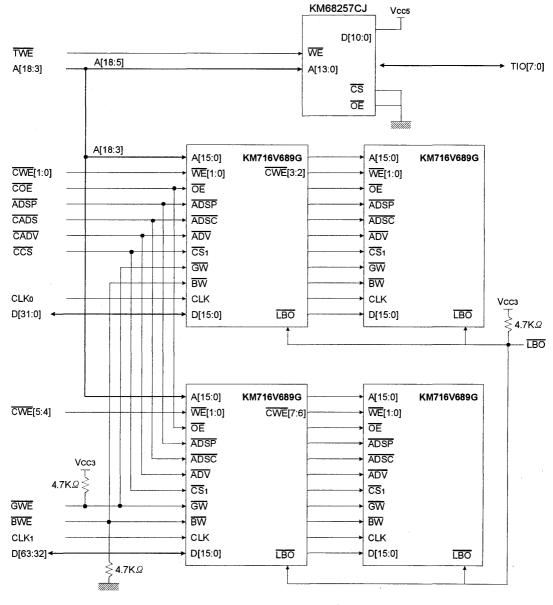
Vss	81	1	Vss	D57	122	42	D56
TIO ₁	82	2	TIO ₀				
TIO ₇	83	3	TIO ₂				
TIO ₅	84	4	TIOs	Vss	123	43	Vss
TiO ₃	85	5	TIO4	D55	124	44	D54
N.C	86	6	N.C	D53	125	45	D52
Vcc5	87	7	Vccs	D51	126	46	D50
N.C	88	8	TWE	D49	127	47	D48
CADV	89	9	CADS	Vss	128	48	Vss
Vss	90	10	Vss	D47	129	49	D46
COE	91	11	CWE₄	D45	130	50	D44
CWE ₅	92	12	CWE ₆	D43	131	51	D42
CWE ₇	93	13	CWE ₀	Vcc5	132	52	Vccs
CWE ₁	94	14	CWE2	D41	133	53	D40
Vcc5	95	15	Vcc3	D39	134	54	D38
CWE ₃	96	16	ccs	D37	135	55	D36
N.C	97	17	GWE(3)	Vss	136	56	Vss
N.C	98	18	BWE(3)	D35	137	57	D34
Vss	99	19	Vss	D33	138	58	D32
N.C	100	20	Аз	D31	139	59	D30
A4	101	21	A7	Vcc5	140	60	Vcc3
A ₆	102	22	A5	D29	141	61	D28
Ав	103	23	A11	D27	142	62	D26
A10	104	24	A16	D25	143	63	D24
Vcc5	105	25	Vccs	Vss	144	64	Vss
A17	106	26	A18	D ₂₃	145	65	D22
Vss	107	27	Vss	D21	146	66	D20
A9	108	28	A12	D19	147	67	D18
A14	109	29	A13	Vcc5	148	68	Vcc3
A15	110	30	ADSP	D17	149	69	D16
N.C	111	31	ECS ₁ (1)	D15	150	70	D14
PD ₀	112	32	ECS ₂ (1)	D13	151	71	D12
PD ₂	113	33	PD ₁	Vss	152	72	Vss
LBO(2)	114	34	PD ₃	D11	153	73	D10
Vss	115	35	Vss	D9	154	74	Dв
CLK₀	116	36	CLK1	D7	155	75	Dε
Vss	117	37	Vss	Vcc5	156	76	Vccз
D63	118	38	D62	D ₅	157	77	D4
Vcc5	119	39	Vcc3	D3	158	78	D2
D61	120	30	D60	D1	159	79	Do
D59	121	41	D58	Vss	160	80	Vss
	L		ŀ		Щ.		l

- 1. These pins are used for 256KB module only and they should be no connect for
- Default is no connect for Intel processor based designs becouse this pin pulled up with 4.7Kohm resistor on the module.
- When these pins are no connect, all byte write should be controlled by all CWEx pins.



FUNCTIONAL BLOCK DIAGRAM

KMM764V72G2



- 1. ZZ pin is internally connected to Vss and not pinout on the module.
- 2. LBO is pulled up with 4.7Kohm resistor.
- 3. GWE is pulled up with 4.7Kohm resistor and BWE is pulled down with 4.7Kohm resistor.



A-1. SYNCHRONOUS PIPELINE BURST TRUTH TABLE(Data field)

ccs	ADSP	CADS	CADV	WRITE	K	Address Accessed	Operation
Н	Х	L	Х	Х	1	N/A	Not Selected
L	L	Х	Х	Х	1	N/A	Not Selected
L	Х	L	Х	Х	1	N/A	Not Selected
L	L	Х	Х	Х	1	External Address	Begin Burst Read Cycle
L	Н	L	Х	L	1	External Address	Begin Burst Read Cycle
L	Н	L	Х	Н	1	External Address	Begin Burst Read Cycle
Х	Н	Н	L	Н	1	Next Address	Continue Burst Read Cycle
Н	Х	Н	L	Н	1	Next Address	Continue Burst Read Cycle
Х	Н	Н	L	L	1	Next Address	Continue Burst Read Cycle
Н	Х	H	L	L	1	Next Address	Continue Burst Read Cycle
Х	Н	Н	Н	Н	1	Current Address	Suspend Burst Read Cycle
Н	Х	Н	Н	Н	1	Current Address	Suspend Burst Read Cycle
Х	Н	Н	Н	L	1	Current Address	Suspend Burst Read Cycle
Н	Х	Н	Н	L	1	Current Address	Suspend Burst Read Cycle

NOTE:

1. X means "Don't Care"

2. The rising edge of clock is symbolized by $\,\,{\uparrow}$

3. WRITE=L means Write operation in A-2. Synchronous Pipeline Butst Write Truth Table
WRITE=H means Read operation in A-2. Synchronous Pipeline Butst Write Truth Table

4. Operation finally depends on status of asynchronous input pin (COE)

A-2. SYNCHRONOUS PIPELINE BURST WRITE TRUTH TABLE(Data field)

GWE	BWE	CWE[1:0]	CWE[3:2]	CWE[5:4]	CWE[7:6]	Operation
Н	Н	X	Х	Х	Х	Read
Н	L	Н	Н	Н	Н	Read
Н	L	L	Н	Н	Н	Write Byte D[15:0]
Н	L	Н	L	Н	Н	Write Byte D[31:16]
Н	L	Н	Н	L	L	Write Byte D[63:32]
Н	. L	L	L	L	L	Write All Bytes
L	Х	X	Х	Х	Х	Write All Bytes

NOTE:

1. X means "Don't Care"

2. All input in this table must meet setup and hold time around the rising edge of CLK(\uparrow).

B-1. ASYNCHRONOUS TRUTH TABLE(Tag field)

TWE	Mode	I/O Pin	Supply Current
H	Read	Dout	lcc
L	. Write	DIN	Icc

NOTE: X means "Don't Care"



C. BURST SEQUENCE

Addresses are generated for the burst access as shown below. The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the LBO# pin. When this pin is Low, linear burst sequence is selected. When this pin is High, Interleaved burst sequence is selected.

INTERLEAVE BURST SEQUENCE TABLE

Pin 114	Pin state	Cas	ie 1	Cas	se 2	Ca	se 3	Cas	se 4
* LBO	High	A1	A0	A1	A0	A1	A0	A1	A0
First Address		0	0	0	1	1	0	1	1
Second Addr	ess	0	1	0	0	1	1	1) 0
Third Address	s	1	0	1	1	0	0	0	1
Fouth Addres	ss	1	1	1	0	0	1	0	0

NOTE:

- 1. When this pin is no connects, LBO should be high.
- 2. Dafault is no connect for Intel processor based designs.

LINEAR BURST SEQUENCE TABLE

Pin 114	Pin state	Cas	se 1	Cas	se 2	Cas	se 3	Cas	se 4
*LBO	Low	A1	A0	A1	A0	A1	A0	A1	A0
First Address		0	0	0	1	1	0	1	1
Second Addr	ess	0	1	1	0	1	1	0	0
Third Address	s	1	0	1	1	0	0	0	1
Fouth Addres	ss	1	1	0	0	0	1	1	0

NOTE: $\overline{\text{LBO}}$ must be tied to low because this pin is pulled up with 4.7K Ω on the module.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Vcc3 Supply Relative to Vss	Vccз	-0.3 to 4.6	V
Voltage on Vccs Supply Relative to Vss	Vcc5	-0.3 to 6.0	V
Voltage on Any Other Pin Relative to Vss	Vin	-0.3 to 6.0	V
Storage Temperature	Тѕтс	-65 to 150	°C
Operating Temperature	TA	0 to 70	°C
Storage Temperature Range Under Bias	TBIAS	-10 to 85	°C

^{*} Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any outher conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.



OPERATING CONDITIONS (TA = 0 to 70°C)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	Vccз	3.13	3.3	3.6	V
	Vcc5	4.75	5.0	5.25	V
Ground	Vss	0	0	0	V
Input Low Voltage	ViL*	-0.3	-	0.8	V
Input High Voltage	ViH*	2.2	-	Vcc***+0.3	V

^{*} VIL3(min) = -1.4 (Pulse Width ≤ 10ns), VIL5(min) = -2.0 (Pulse Width ≤ 10ns)

DC ELECTRICAL CHARACTERISTICS*(TA =0 to 70°C, Vcc3=3.3V+10%/-5%)

Parameter	Symbol	Test Conditions	S	Min	Max	Unit
Input Leakage current	lu**	Vcc3=Max, Vin=Vss to Vcc3		-5	5	μΑ
Output Leakage Current	ILO	Output Disable, Vour=Vss to Vcc	3	-5	5	μΑ
	100	f=MAX, 100% Duty	75MHz	-	800	mA
Operating Current	lcc	VIN=VIH or VIL, IOUT=0mA	66MHz	-	720	1 11114
Chandle Coverant	ISB	f=MAX, 100% Duty, Device desele	ected,	-	120	mA
		f=MAX, 100% Duty, Device desele Vin≥Vcc3-0.2V or ViL, Vin ≤ 0.2V		-	20	mA
Output Low Voltage	Vol	IoL=8mA		-	0.4	V
Output High Voltage	Vон	IOH=-4mA		2.4	-	V

^{*} Excludes Tag field.

CAPACITANCE*(f=1MHz,TA=25°C)

Item	Symbol	Test Condition	Min.	Max.	Unit
Address, ECS Input Capacitance	CIN1	VIN=0V	-	40	pF
TWE, CWE, CLK Input Capacitance	CIN2	VIN=0V	-	20	pF
COE, ADSP, CADS, CADV, CCS GWE, BWE Input Capacitance	Сімз	VIN=0V	-	30	pF
Data and Tag Input/Output Capacitance	CI/01	V1/0=0V	-	15	pF

^{*} NOTE : Capacitance is sampled and not 100% tested.



^{**} V_{IH3}(max) = 5.0V (Pulse Width \leq 10ns); In case of I/O pins, the maximum V_{H3}(max) = 4.1V (Pulse Width \leq 10ns) V_{IH5}(max) = 7.0V (Pulse width \leq 10ns)

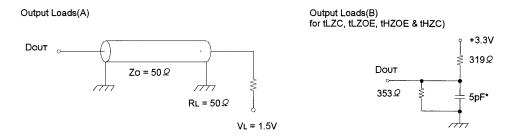
^{***} Vcc =Vcc3 or Vcc5

^{**} ILI for $\overline{LBO}(pin\ 114)$, $\overline{GWE}(pin\ 17)$ and $\overline{BWE}(pin\ 18)$ is $\pm\ 1mA(Max.)$

AC CHARACTERISTICS

TEST CONDITIONS ON DATA RAM (TA =0 to 70°, Vcc3=3.3V+10%/-5%, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time (Measured at 0.3V and 2.7V)	2ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig 1

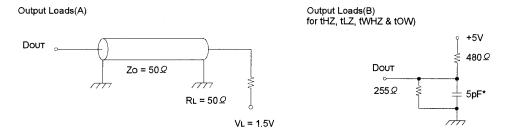


* Including Scope and Jig Capacitance

Fig. 1

TEST CONDITIONS ON TAG RAM (TA =0 to 70 °C, Vcc5=5.0V ±5%, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time (Measured at 0.3V and 2.7V)	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig 1



* Including Scope and Jig Capacitance

Fig. 2



AC TIMING CHARACTERISTICS ON DATA RAM (TA =0 to 70°C,Vcc3=3.3V+10%/-5%)

Refers to the individual components, not the whole module

Parameter	Symbol	KMM764	V72G2-13	KMM764	V72G2-15	11-14
Parameter	Symbol	Min	Max	Min	Max	Unit
Cycle Time	tCYC	13	-	15	-	ns
Clock Access Time	tCD	-	7	-	8	ns
Output Enable to Data Valid	tOE	-	6	-	7	ns
Clock High to Output Low-Z	tLZC	6	-	6	-	ns
Output Hold from Clock High	tOH	3	-	3	-	ns
Output Enable Low to Output Low-Z	tLZOE	2	-	2	-	ns
Output Enable High to Output High-Z	tHZOE	2	5	2	. 6	ns
Clock High to Output High-Z	tHZC	-	7	-	7	ns
Clock High Pulse Width	tCH	4.5	-	5.5	-	ns
Clock Low Pulse Width	tCL	4.5	-	5.5	-	ns
Address Setup to Clock High	tAS	2.5	-	2.5	•	ns
Address Status Setup to Cock High	tSS	2.5	-	2.5	-	ns
Data Setup to Cock High	tDS	2.5	-	2.5		ns
Write Setup to Clock High(GWE, BWE, CWEx)	tWS	2.5	-	2.5	-	ns
Address Advance Setup to Clock High	tADVS	2.5	-	2.5	-	ns
Chip Select Setup to Clock High	tCSS	2.5	-	2.5	-	ns
Address Hold from Clock High	tAH	0.5	-	0.5	-	ns
Address Status Hold from Clock High	tSH	0.5	-	0.5	-	ns
Data Hold from Clock High	tDH	0.5	-	0.5	-	ns
Write Hold from Clock High(GWE, BWE, CWEx)	tWH	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	tADVH	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	tCSH	0.5	-	0.5	-	ns
ZZ High to Power Down	tPDS	2	-	2	-	cycle
ZZ Low to Power Up	tPUS	2	-	2	-	cycle

^{1.} All address inputs must meet the specified setup and hold times for all rising clock(Clk) edges whenever CADS and/or ADSP is sampled low and this device is chip selected.

All other synchronous inputs must meet the specified sample and hold times whenever this device is chip selected.

^{2.} Both chip selects must be active whenever CADS or ADSP is sampled low in order for the this device to remain enabled.

^{3.} CADS or ADSP must not be asserted for at least 2 Clocks after leaving ZZ state.

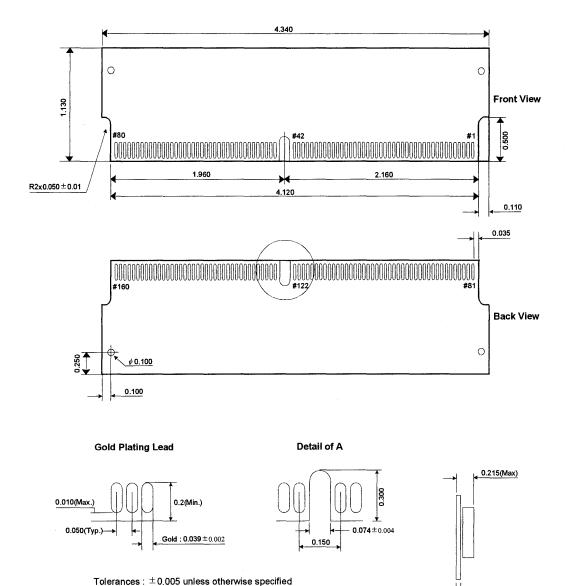
AC TIMING CHARACTERISTICS ON TAG RAM (TA =0 to 70 $^{\circ}\text{C,Vcc5=5.0V} \pm 5\%)$

Refers to the individual components, not the whole module

Parameter	Symbol	KMM764	V72G2-13	KMM764	Unit	
Parameter	Symbol	Min	Max	Min	Max	Unit
Read Cycle Time	tRC	12	-	15	•	ns
Address Access Time	tAA	-	12	-	15	ns
Chip Select to Low-Z Output	tLZ	3	-	3	-	ns
Output Hold from Address Change	tOH	3	-	3	-	ns
Write cycle Time	tWC	12	-	15	-	ns
Address Set-up Time	tAS	0	-	0	-	ns
Address Valid to End of Write	tAW	9	-	12	-	ns
Write Pulse Width	tWP	12	-	15	-	ns
Write Recovery Time	tWR	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	6	0	8	ns
Data to Write Time Overlap	tDW	7	-	8	-	ns
Data Hold from Write Time	tDH	0		0	-	ns
End Write to Output Low-Z	tOW	0	-	0	-	ns

PACKAGE DIMENSIONS

Units: Inches



0.062

512KB SPB SRAM Module (Single Bank Operation)

FEATURES

- . Implemented based on COAST 1.4
- · Supports Interleave Burst and Linear Burst Mode
- · Single Bank Operation
- · Zero-wait-state operation at 75/66MHz
- . TTL compatible inputs/outputs
- Multiple ground pins and decoupling capacitors for maximum noise immunity
- . 160-pin DIMM with gold plated Tap
- · Series 22 ohm resistors for nuose immunity
- · Product Family: KMM764V72G7-13/15

GENERAL DESCRIPTION

The KMM764V72G7 is 512K byte high-frequency Synchronous Pipelined Burst Static Randomd Access Memory module organized as 64K words by 64 bits. The module is designed specially to function as the secondary cache in Pentium and Power PC-based systems. The device for this module is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. The module uses four SAMSUNG's KM716V689G and KM68257C for 8-bits tag RAM.

PIN NAMES

Pin Name	Pin Function
CLK[1:0]	Clock Inputs
A[18:3]	Cache RAM Address Inputs
D[63:0]	Cache RAM Data Inputs/Outputs
TIO[10:0]	Tag RAM Data Inputs/Outputs
TWE	Tag RAM Write Enable Input
ECS[2:1]	Chip Select Inputs for Depth Expansion
ccs	Chip Select Input
CWE[7:0]	Write Enable Inputs
COE	Output Enable Input
ADSP	Address Status Processor
CADS	Address Status Controller
CADV	Burst Address Advance
BWE	Byte Write Enable Input
GWE	Grobal Write Enable Input
LBO	Burst Mode Control
Vcc5	Power Supply(5V)
Vccз	Power Supply(3.3V)
Vss	Ground
N.C	No Connections

PD PIN INFORMATION

	PD Pin A	llocation		Module Part No
PD3	PD2	PD1	PD ₀	Wodule Fait 140
Vss	N.C	N.C	N.C	KMM764V72G7

PIN CONFIGURATION(Top View)

Vss	81	1	Vss	D57	122	42	D56
TIO ₁	82	2	TIO₀		ĺ		
TIO7	83	3	TIO ₂				
TIO ₅	84	4	TIO6	Vss	123	43	Vss
TIO ₃	85	5	TIO4	D55	124	44	D54
N.C	86	6	N.C	D53	125	45	D52
Vcc5	87	7	Vccs	D51	126	46	D50
N.C	88	8	TWE	D49	127	47	D48
CADV	89	9	CADS	Vss	128	48	Vss
Vss	90	10	Vss	D47	129	49	D46
COE	91	11	CWE₄	D45	130	50	D44
CWE ₅	92	12	CWE ₆	D43	131	51	D42
CWE ₇	93	13	CWE₀	Vcc5	132	52	Vccs
CWE ₁	94	14	CWE₂	D41	133	53	D40
Vcc5	95	15	Vccs	D39	134	54	D38
CWE₃	96	16	CCS	D37	135	55	D36
N.C	97	17	GWE (3)	Vss	136	56	Vss
N.C	98	18	BWE(3)	D35	137	57	D34
Vss	99	19	Vss	Daa	138	58	D32
N.C	100	20	A3	D31	139	59	D30
A4	101	21	A7	Vcc5	140	60	Vccs
A ₆	102	22	A ₅	D29	141	61	Dze
Aa	103	23	A11	D27	142	62	D26
A10	104	24	A16	D25	143	63	D24
Vcc5	105	25	Vccs	Vss	144	64	Vss
A 17	106	26	A18	D ₂₃	145	65	D22
Vss	107	27	Vss	D21	146	66	D20
A9	108	28	A12	D19	147	67	D18
A14	109	29	Ata	Vcc5	148	68	Vcc3
A15	110	30	ADSP	D17	149	69	D16
N.C	111	31	ECS1(1)	D15	150	70	D14
PD₀	112	32	ECS ₂ (1)	D13	151	71	D12
PD ₂	113	33	PD ₁	Vss	152	72	Vss
LBO(2)	114	34	PD ₃	D11	153	73	D10
Vss	115	35	Vss	De	154	74	Dв
CLK₀	116	36	CLK ₁	D7	155	75	D6
Vss	117	37	Vss	Vcc5	156	76	Vccs
D63	118	38	D62	D5	157	77	D4
Vcc5	119	39	Vcc3	D3	158	78	D ₂
D61	120	30	D60	D1	159	79	D ₀
D59	121	41	D58	Vss	160	80	Vss

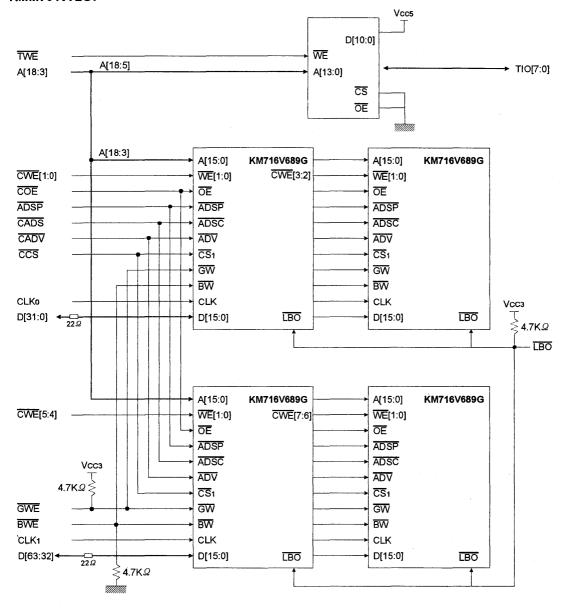
NOTE

- These pins are used for 256KB module only and they should be no connect for this module.
- Default is no connect for Intel processor based designs becouse this pin pulled up with 4.7Kohm resistor on the module.
- When these pins are no connect, all byte write should be controlled by all CWEx pins.



FUNCTIONAL BLOCK DIAGRAM

KMM764V72G7



- 1. ZZ pin is internally connected to Vss and not pinout on the module.
- 2. LBO is pulled up with 4.7Kohm resistor.
- 3. GWE is pulled up with 4.7Kohm resistor and BWE is pulled down with 4.7Kohm resistor.



A-1. SYNCHRONOUS PIPELINE BURST TRUTH TABLE(Data field)

ccs	ADSP	CADS	CADV	WRITE	K	Address Accessed	Operation
Н	Х	L	Х	Х	1	N/A	Not Selected
L	L	Х	Х	Х	1	N/A	Not Selected
L	Х	L	Х	Х	1	N/A	Not Selected
L	L	· X	Х	Х	1	External Address	Begin Burst Read Cycle
L	Н	L	Х	L	1	External Address	Begin Burst Read Cycle
L	Н	L	Х	Н	1	External Address	Begin Burst Read Cycle
Х	Н	Н	L	Н	1	Next Address	Continue Burst Read Cycle
Н	Х	Н	L	Н	1	Next Address	Continue Burst Read Cycle
Х	Н	Н	L	L	1	Next Address	Continue Burst Read Cycle
Н	Х	Н	L	L	1	Next Address	Continue Burst Read Cycle
Х	Н	Н	Н	Н	1	Current Address	Suspend Burst Read Cycle
Н	Х	Н	Н	Н	1	Current Address	Suspend Burst Read Cycle
Х	Н	Н	Н	L	1	Current Address	Suspend Burst Read Cycle
Н	Х	Н	Н	L	1	Current Address	Suspend Burst Read Cycle

NOTE

- 1. X means "Don't Care"
- 2. The rising edge of clock is symbolized by 1
- 3. WRITE=L means Write operation in A-2. Synchronous Pipeline Butst Write Truth Table
 WRITE=H means Read operation in A-2. Synchronous Pipeline Butst Write Truth Table
- 4. Operation finally depends on status of asynchronous input pin (COE)

A-2. SYNCHRONOUS PIPELINE BURST WRITE TRUTH TABLE(Data field)

GWE	BWE	CWE[1:0]	CWE[3:2]	CWE[5:4]	CWE[7:6]	Operation
Н	Н	X	Х	Х	X	Read
Н	L	Н	Н	Н	Н	Read
Н	L	L	Н	Н	Н	Write Byte D[15:0]
Н	L	Н	L	Н	Н	Write Byte D[31:16]
Н	L	Н	Н	L	L	Write Byte D[63:32]
Н	L	L	L	L	L	Write All Bytes
L	X	Х	Х	Х	Х	Write All Bytes

NOTE:

- 1. X means "Don't Care"
- 2. All input in this table must meet setup and hold time around the rising edge of CLK(\uparrow).

B-1. ASYNCHRONOUS TRUTH TABLE(Tag field)

TWE	Made	I/O Pin	Supply Current
Н	Read	Dout	lcc
L	Write	DIN	lcc

NOTE: X means "Don't Care"



C. BURST SEQUENCE

Addresses are generated for the burst access as shown below. The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the LBO# pin. When this pin is Low, linear burst sequence is selected. When this pin is High, Interleaved burst sequence is selected.

INTERLEAVE BURST SEQUENCE TABLE

Pin 114	Pin state	Cas	ie1	Ca	se 2	Ca	se 3	Ca	se 4
*LBO	High	A1	A0	A1	A0	A1	A0	A1	A0
First Address		0	0	0	1	1	0	1	1
Second Addr	ess	0	1	0	0	1	1	1	0
Third Address	s	1	0	1	1 1	0	0	0	1
Fouth Addres	s	1	1	1	0	0	1	0	0

NOTE:

- 1. When this pin is no connects, LBO should be high.
- 2. Dafault is no connect for Intel processor based designs.

LINEAR BURST SEQUENCE TABLE

Pin 114	Pin state	Cas	ie 1	Ca	se 2	Ca	se 3	Ca	se 4
*LBO	Low	A1	A0	A1	A0	A1	A0	A1	A0
First Address		0	0	0	1	1	0	1	1
Second Addr	ess	0	1	1	0	1	1	0	0
Third Address	s	1	0	1	1	0	0	0	1
Fouth Addres	ss	1	1	0	0	0	1	1	0
				1	i		ł		

NOTE: $\overline{\text{LBO}}$ must be tied to low because this pin is pulled up with 4.7K Ω on the module.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Vcc3 Supply Relative to Vss	Vccз	-0.3 to 4.6	V
Voltage on Vcc5 Supply Relative to Vss	Vcc5	-0.3 to 6.0	V
Voltage on Any Other Pin Relative to Vss	Vin	-0.3 to 6.0	V
Storage Temperature	Тѕтс	-65 to 150	°C
Operating Temperature	ТА	0 to 70	Ĉ
Storage Temperature Range Under Bias	TBIAS	-10 to 85	°C

^{*} Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any outher conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.



· OPERATING CONDITIONS (TA =0 to 70°C)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	Vcc3	3.13	3.3	3.6	V
	Vcc5	4.75	5.0	5.25	V
Ground	Vss	0	0	0	V
Input Low Voltage	VIL*	-0.3	-	0.8	V
Input High Voltage	ViH*	2.2	-	Vcc***+0.3	V

^{*} VIL3(min) = -1.4 (Pulse Width \leq 10ns), VIL5(min) \approx -2.0 (Pulse Width \leq 10ns)

DC ELECTRICAL CHARACTERISTICS*(TA = 0 to 70°, Vcc3=3.3V+10%/-5%)

Parameter	Symbol	Test Condition	S	Min	Max	Unit
Input Leakage current	lu**	Vcc3=Max, ViN=Vss to Vcc3		-5	5	μΑ
Output Leakage Current	ILO	Output Disable, VouT=Vss to Vcc	3	-5	5	μΑ
On anating Commant	lcc	f=MAX, 100% Duty	=MAX, 100% Duty 75MHz		800	mA
Operating Current	licc	VIN=VIH or VIL, IOUT=0mA 66MHz		-	720	1 1114
Standby Coment	ISB	f=MAX, 100% Duty, Device desele	f=MAX, 100% Duty, Device deselected, VIN=VIH or VIL, IOUT=0mA		120	mA
Standby Current f=MAX, 100% Duty, Device deselected, VIN≥Vcc3-0.2V or VIL, VIN ≤ 0.2V, IOUT=0m			-	20	mA	
Output Low Voltage	Vol	IoL=8mA	-	0.4	V	
Output High Voltage	Vон	Iон=-4mA		2.4	-	V

^{*} Excludes Tag field.

CAPACITANCE*(f=1MHz,TA=25°C)

ltem .	Symbol	Test Condition	Min.	Max.	Unit
Address, ECS Input Capacitance	CIN1	VIN=0V	-	45	pF
TWE, CWE, CLK Input Capacitance	CIN2	VIN=0V	-	20	pF
COE, ADSP, CADS, CADV, CCS GWE, BWE Input Capacitance	Сімз	VIN=0V	-	30	pF
Data and Tag Input/Output Capacitance	CI/O1	VI/0=0V	-	15	pF

^{*} NOTE : Capacitance is sampled and not 100% tested.



^{**} VH3(max) = 5.0V (Pulse Width \leq 10ns); In case of I/O pins, the maximum VH3(max) = 4.1V (Pulse Width \leq 10ns) VH3(max) = 7.0V (Pulse width \leq 10ns)

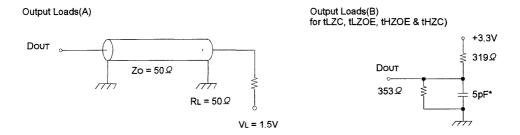
^{***} Vcc =Vcc3 or Vcc5

^{**} ILI for LBO, GWE and BWE is ±1mA (Max.)

AC CHARACTERISTICS

TEST CONDITIONS ON DATA RAM (TA = 0 to 70 °C, Vcc3=3.3V+10%/-5%, unless otherwise specified.)

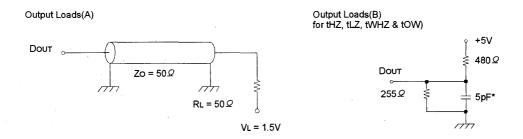
Parameter	
Input Pulse Level	0 to 3V
Input Rise and Fall Time (Measured at 0.3V and 2.7V)	2ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig 1



* Including Scope and Jig Capacitance Fig. 1

TEST CONDITIONS ON TAG RAM (TA =0 to 70 °C, Vcc5=5.0V ±5%, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time (Measured at 0.3V and 2.7V)	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig 1



* Including Scope and Jig Capacitance

Fig. 2



AC TIMING CHARACTERISTICS ON DATA RAM (TA = 0 to 70 °C, VCC3=3.3V+10%/-5%)

Refers to the individual components, not the whole module

Parameter	Symbol	KMM764V72G7-13		KMM764V72G7-15		
		Min	Max	Min	Max	Unit
Cycle Time	tCYC	13	-	15	-	ns
Clock Access Time	tCD	•	. 7	-	8	ns
Output Enable to Data Valid	tOE	-	6	-	7	ns
Clock High to Output Low-Z	tLZC	6	-	6	-	ns
Output Hold from Clock High	tOH	3	-	3	-	ns
Output Enable Low to Output Low-Z	tLZOE	2	-	- 2	-	ns
Output Enable High to Output High-Z	tHZOE	2	5	2	6	ns
Clock High to Output High-Z	tHZC	-	7	-	7	ns
Clock High Pulse Width	tCH	4.5	-	5.5	-	ns
Clock Low Pulse Width	tCL	4.5	-	5.5	-	ns
Address Setup to Clock High	tAS	2.5	-	2.5	-	ns
Address Status Setup to Cock High	tSS	2.5	-	2.5	-	ns
Data Setup to Cock High	tDS	2.5	-	2.5	-	ns
Write Setup to Clock High(GWE, BWE, CWEX)	tWS	2.5	-	2.5	-	ns
Address Advance Setup to Clock High	tADVS	2.5	-	2.5	-	ns
Chip Select Setup to Clock High	tCSS	2.5	-	2.5	-	ns
Address Hold from Clock High	tAH	0.5	-	0.5	-	ns
Address Status Hold from Clock High	tSH	0.5	-	0.5	-	ns
Data Hold from Clock High	tDH	0.5	-	0.5	-	ns
Write Hold from Clock High(GWE, BWE, CWEx)	tWH	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	tADVH	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	tCSH	0.5	-	0.5	-	ns
ZZ High to Power Down	tPDS	2	-	2	-	cycle
ZZ Low to Power Up	tPUS	2	-	2	-	cycle

^{1.} All address inputs must meet the specified setup and hold times for all rising clock(Clk) edges whenever CADS and/or ADSP is sampled low and this device is chip selected.

All other synchronous inputs must meet the specified sample and hold times whenever this device is chip selected.

^{2.} Both chip selects must be active whenever CADS or ADSP is sampled low in order to the device remained at enable.

^{3.} CADS or ADSP must not be asserted for at least 2 Clocks after leaving ZZ state.

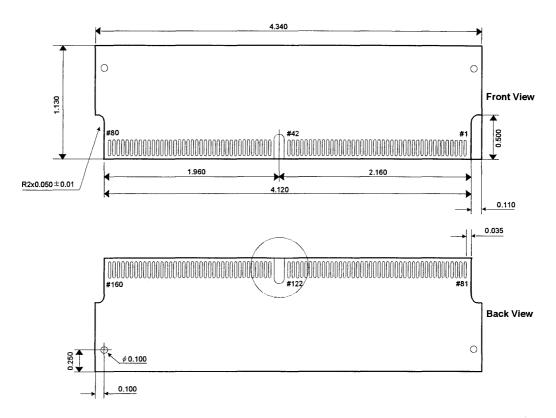
AC TIMING CHARACTERISTICS ON TAG RAM (TA =0 to 70 °C, VCC5=5.0V±5%)

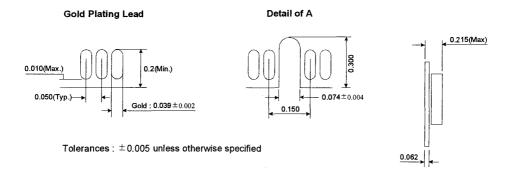
Refers to the individual components, not the whole module

Parameter	Court at	KMM764V72G7-13		KMM764V72G7-15		
	Symbol	Min	Max	Min	Max	Unit
Read Cycle Time	tRC	12	-	15	-	ns
Address Access Time	tAA	-	12	-	15	ns
Chip Select to Low-Z Output	tLZ	3	-	3	-	ns
Output Hold from Address Change	tOH	3	-	3	-	ns
Write cycle Time	tWC	12	-	15	-	ns
Address Set-up Time	tAS	0	-	0	•	ns
Address Valid to End of Write	tAW	9	-	12	-	ns
Write Pulse Width	tWP	12	-	15	-	ns
Write Recovery Time	tWR	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	6	0	8	ns
Data to Write Time Overlap	tDW	7	-	8	-	ns
Data Hold from Write Time	tDH	0	-	0	-	ns
End Write to Output Low-Z	tOW	0	-	0	-	ns

PACKAGE DIMENSIONS

Units: Inches





512KB SPB SRAM Module (Single Bank Operation)

FEATURES

- . Implemented based on COAST 3.1
- . Supports Interleave Burst and Linear Burst Mode
- · Single Bank Operation
- · Zero-wait-state operation at 75/66MHz
- . TTL compatible inputs/outputs
- Multiple ground pins and decoupling capacitors for maximum noise immunity
- 160-pin DIMM with gold plated Tap
- Series 22 ohm resistors for nuose immunity
- Product Family: KMM764V75G-13/15

GENERAL DESCRIPTION

The KMM764V75G is 512K byte high-frequency Synchronous Pipelined Burst Static Randomd Access Memory module organized as 64K words by 64 bits. The module is designed specially to function as the secondary cache in Pentium and Power PC-based systems. The device for this module is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. The module uses four SAMSUNG's KM716V689G and KM68257C for 11-bits tag RAM.

PIN NAMES

Pin Name	Pin Function
CLK[1:0]	Clock Inputs
A[18:3]	Cache RAM Address Inputs
D[63:0]	Cache RAM Data Inputs/Outputs
TIO[10:0]	Tag RAM Data Inputs/Outputs
TWE	Tag RAM Write Enable Input
ECS[2:1]	Chip Select Inputs for Depth Expansion
ccs	Chip Select Input
CWE[7:0]	Write Enable Inputs
COE	Output Enable Input
ADSP	Address Status Processor
CADS	Address Status Controller
CADV	Burst Address Advance
BWE	Byte Write Enable Input
GWE	Grobal Write Enable Input
LBO	Burst Mode Control
Vcc5	Power Supply(5V)
Vccз	Power Supply(3.3V)
Vss	Ground
N.C	No Connections

PD PIN INFORMATION

	PD Pin A	llocation	1	Module Part No
PD3	PD2	PD1	PD0	Module Fait No
Vss	N.C	N.C	N.C	KMM764V75G

PIN CONFIGURATION(Top View)

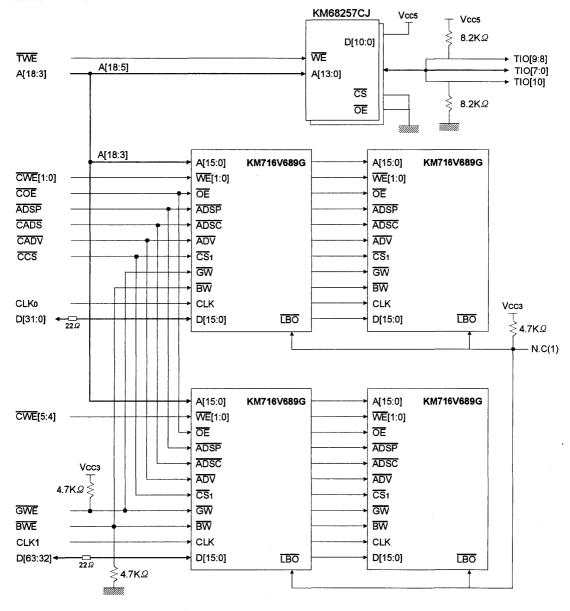
Vss	81	1	Vss	D57	122	42	D58
TIOs	82	2	TIO₀				
TIO7	83	3	TIO ₂				
TIO ₅	84	4	TIO ₆	Vss	123	43	Vss
TIO ₃	85	5	TiO ₄	D55	124	44	D54
TIOs	86	6	TIO ₈	D53	125	45	D52
Vcc5	87	7	Vccs	D51	126	46	D50
TIO ₁₀	88	8	TWE	D49	127	47	D48
CADV	89	9	CADS	Vss	128	48	Vss
Vss	90	10	Vss	D47	129	49	D46
COE	91	11	CWE₄	D45	130	50	D44
CWE ₅	92	12	CWE ₆	D43	131	51	D42
CWE ₇	93	13	CWE₀	Vcc5	132	52	Vccs
CWE ₁	94	14	CWE ₂	D41	133	53	D40
Vcc5	95	15	Vccs	D39	134	54	D38
CWE ₃	96	16	CCS	D37	135	55	D36
N.C	97	17	GWE(3)	Vss	136	56	Vss
N.C	98	18	BWE(3)	D35	137	57	D34
Vss	99	19	Vss	D33	138	58	D32
N.C	100	20	Аз	D31	139	59	D30
A4	101	21	A 7	Vcc5	140	60	Vccs
As	102	22	A 5	D29	141	61	D28
As	103	23	A11	D27	142	62	D26
A10	104	24	A16	D25	143	63	D24
Vcc5	105	25	Vccs	Vss	144	64	Vss
A17	106	26	A18	D ₂₃	145	65	D22
Vss	107	27	Vss	D21	146	66	D20
Аş	108	28	A12	D19	147	67	D18
A14	109	29	A13	Vcc5	148	68	Vccs
A15	110	30	ADSP	D17	149	69	D16
N.C	111	31	ECS ₁ (1)	D15	150	70	D14
PD ₀	112	32	<u>ECS</u> 2(1)	D13	151	71	D12
PD ₂	113	33	PD ₁	Vss	152	72	Vss
LBO(2)	114	34	PD ₃	D11	153	73	D10
Vss	115	35	Vss	D9	154	74	Dŧ
CLK₀	116	36	CLK1	D7	155	75	D6
Vss	117	37	Vss	Vcc5	156	76	Vccs
D63	118	38	D62	D ₅	157	77	D4
Vcc5	119	39	Vccs	D3	158	78	D ₂
D61	120	30	D60	D ₁	159	79	D ₀
D59	121	41	D58	Vss	160	80	Vss

NOTE

- These pins are used for 256KB module only and they should be no connect for this module.
- Default is no connect for Intel processor based designs becouse this pin pulled up with 4.7Kohm resistor on the module.
- When these pins are no connect, all byte write should be controlled by all CWEX pins.

FUNCTIONAL BLOCK DIAGRAM

KMM764V75G



NOTE

- 1. $\underline{\textbf{ZZ}}$ pin is internally connected to Vss and not pinout on the module.
- 2. LBO is pulled up with 4.7Kohm resistor.
- 3. GWE is pulled up with 4.7Kohm resistor and BWE is pulled down with 4.7Kohm resistor.



A-1. SYNCHRONOUS PIPELINE BURST TRUTH TABLE(Data field)

CCS	ADSP	CADS	CADV	WRITE	K	Address Accessed	Operation
Н	Х	L	Х	Х	1	N/A	Not Selected
L	L	Х	Х	Х	1	N/A	Not Selected
L	Х	L	Х	Х	1	N/A	Not Selected
L	L	Х	Х	Х	1	External Address	Begin Burst Read Cycle
L	Н	L	Х	L	1	External Address	Begin Burst Read Cycle
L	Н	L	Х	Н	1	External Address	Begin Burst Read Cycle
Х	Н	Н	L	Н	1	Next Address	Continue Burst Read Cycle
Н	Х	Н	L	Н	1	Next Address	Continue Burst Read Cycle
Х	Н	Н	L	L	1	Next Address	Continue Burst Read Cycle
Н	Х	Н	L	L	1	Next Address	Continue Burst Read Cycle
Х	H	Н	Н	Н	1	Current Address	Suspend Burst Read Cycle
Н	Х	Н	Н	Н	1	Current Address	Suspend Burst Read Cycle
Х	Н	Н	Н	L	1	Current Address	Suspend Burst Read Cycle
Н	Х	Н	Н	L	1	Current Address	Suspend Burst Read Cycle

NOTE:

- 1. X means "Don't Care"
- 2. The rising edge of clock is symbolized by 1
- 3. WRITE=L means Write operation in A-2. Synchronous Pipeline Butst Write Truth Table
 WRITE=H means Read operation in A-2. Synchronous Pipeline Butst Write Truth Table
- 4. Operation finally depends on status of asynchronous input pin (COE)

A-2. SYNCHRONOUS PIPELINE BURST WRITE TRUTH TABLE(Data field)

GWE	BWE	CWE[1:0]	CWE[3:2]	CWE[5:4]	CWE[7:6]	Operation
Н	Н	Х	Х	X	X	Read
Н	L	Н	Н	Н	Н	Read
Н	L	L	Н	Н	Н	Write Byte D[15:0]
Н	L	Н	L	Н	Н	Write Byte D[31:16]
Н	L	Н	Н	L	L	Write Byte D[63:32]
Н	L	L	L	L	L	Write All Bytes
L	Х	Х	Х	X	X	Write All Bytes

NOTE

- 1. X means "Don't Care"
- 2. All input in this table must meet setup and hold time around the rising edge of CLK(1).

B-1. ASYNCHRONOUS TRUTH TABLE(Tag field)

TWE		I/O Pin	Supply Current
Н	Read	Dout	Icc
L	Write	Din	Icc

NOTE: X means "Don't Care"



C. BURST SEQUENCE

Addresses are generated for the burst access as shown below. The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the LBO# pin. When this pin is Low, linear burst sequence is selected. When this pin is High, Interleaved burst sequence is selected.

INTERLEAVE BURST SEQUENCE TABLE

Pin 114	Pin state	Cas	se 1	Са	se 2	Ca	se 3	Ca	se 4
*LBO	High	A1	A0	A1	A0	A1	A0	A1	A0
First Address		0	0	0	1	1	0	1	1
Second Add		0	1	0	0	1	1	1	0
Third Addres	ss	1	0	1	1	0	0	0	1
Fouth Addre	ss	1	1	1	0	0	1	0	0

NOTE:

- 1. When this pin is no connects, LBO should be high.
- 2. Dafault is no connect for Intel processor based designs.

LINEAR BURST SEQUENCE TABLE

Pin 114	Pin state	Cas	se 1	Cas	se 2	Ca	se 3	Cas	se 4
*LBO	Low	A1	A0	A1	A0	A1	A0	A1	A0
First Address	S	0	0	0	1	1	0	1	1
Second Add	ress	0	1	1	0	1	1	0	0
Third Addres	ss	1 1	0	1	1	0	0	0	1
Fouth Addre	ss	1	1	0	0	0	1	1	0

NOTE: $\overline{\text{LBO}}$ must be tied to low because this pin is pulled up with 4.7K Ω on the module.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Vcc3 Supply Relative to Vss	Vccз	-0.3 to 4.6	V
Voltage on Vccs Supply Relative to Vss	Vcc5	-0.3 to 6.0	V
Voltage on Any Other Pin Relative to Vss	Vin	-0.3 to 6.0	V
Storage Temperature	Тѕтс	-65 to 150	C
Operating Temperature	TA	0 to 70	°C
Storage Temperature Range Under Bias	TBIAS	-10 to 85	°C

^{*} Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any outher conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.



OPERATING CONDITIONS (TA =0 to 70°C)

Parameter	Symbol	Min	Тур.	Max	Unit
Supply Voltage	Vccз	3.13	3.3	3.6	٧
	Vcc5	4.75	5.0	5.25	٧
Ground	Vss	0	0	0	٧
Input Low Voltage	VIL*	-0.3	-	0.8	V
Input High Voltage	VIH*	2.2	-	Vcc***+0.3	٧

^{*} $V_{L3}(min) = -1.4$ (Pulse Width ≤ 10 ns), $V_{L5}(min) = -2.0$ (Pulse Width ≤ 10 ns)

DC ELECTRICAL CHARACTERISTICS*(TA = 0 to 70°C, Vcc3=3.3V+10%/-5%)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage current	ILI**	Vcc3=Max, Vin=Vss to Vcc3		-5	5	μΑ
Output Leakage Current	ILO	Output Disable, Vout=Vss to Vcc3		-5	5	μΑ
Operating Current	Icc	f=MAX, 100% Duty	75MHz		800	mA
		VIN=VIH or VIL, IOUT=0mA	66MHz	-	720	1 1114
Ohan dhu Oumant	ISB	f=MAX, 100% Duty, Device deselected, Vin=Vih or Vil, Iout=0mA	-	120	mA	
Standby Current ISB1		f=MAX, 100% Duty, Device deselected, Vin=Vih or Vil., Iout=0mA		-	20	mA
Output Low Voltage	Vol	IoL=8mA		-	0.4	V
Output High Voltage	Vон	IOH=-4mA		2.4	•	V

^{*} Excludes Tag field.

CAPACITANCE*(f=1MHz,Ta=25°C)

Item	Symbol	Test Condition	Min.	Max.	Unit
Address, ECS Input Capacitance	CIN1	Vin=0V	-	45	pF
TWE, CWE, CLK Input Capacitance	CIN2	VIN=0V	-	20	pF
COE, ADSP, CADS, CADV, CCS GWE, BWE Input Capacitance	Сімз	VIN=0V	-	30	pF
Data and Tag Input/Output Capacitance	CI/01	V1/0=0V	-	15	pF

^{*} NOTE : Capacitance is sampled and not 100% tested.



^{**} V_{H3}(max) = 5.0V (Pulse Width \leq 10ns); In case of I/O pins, the maximum V_{H3}(max) = 4.1V (Pulse Width \leq 10ns) V_{H5}(max) = 7.0V (Pulse width \leq 10ns)

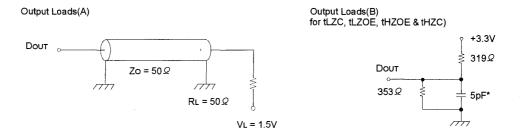
^{***} Vcc =Vccs or Vccs

^{**} ILI for LBO, GWE, TIO(8,9,10) and BWE is ±1mA(Max.)

AC CHARACTERISTICS

TEST CONDITIONS ON DATA RAM (TA =0 to 70 °C, Vcc3=3.3V+10%/-5%, unless otherwise specified.)

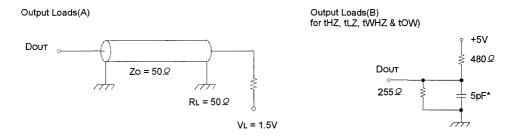
Parameter Value			
Input Pulse Level	0 to 3V		
Input Rise and Fall Time (Measured at 0.3V and 2.7V)	2ns		
Input and Output Timing Reference Levels	1.5V		
Output Load	See Fig 1		



* Including Scope and Jig Capacitance Fig. 1

TEST CONDITIONS ON TAG RAM (TA =0 to 70 °C, Vcc5=5.0V ±5%, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time (Measured at 0.3V and 2.7V)	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig 1



* Including Scope and Jig Capacitance

Fig. 2



AC TIMING CHARACTERISTICS ON DATA RAM (TA = 0 to 70°, VCc3=3.3V+10%/-5%)

Refers to the individual components, not the whole module

Parameter	Symbol	KMM76	4V75G-13	KMM764	V75G-15	11
Parameter	Symbol	Min	Max	Min	Max	Unit
Cycle Time	tCYC	13	-	15	-	ns
Clock Access Time	tCD	-	7	-	8	ns
Output Enable to Data Valid	tOE	-	6	-	7	ns
Clock High to Output Low-Z	tLZC	6	-	6	-	ns
Output Hold from Clock High	tOH	3	-	3	-	ns
Output Enable Low to Output Low-Z	tLZOE	2	-	2	-	ns
Output Enable High to Output High-Z	tHZOE	2	5	2	6	ns
Clock High to Output High-Z	tHZC	-	7	-	7	ns
Clock High Pulse Width	tCH	4.5	-	5.5	-	ns
Clock Low Pulse Width	tCL	4.5	-	5.5	-	ns
Address Setup to Clock High	tAS	2.5	-	2.5	-	ns
Address Status Setup to Cock High	tSS	2.5	-	2.5	-	ns
Data Setup to Cock High	tDS	2.5	-	2.5	-	ns
Write Setup to Clock High(GWE, BWE, CWEx)	tWS	2.5	-	2.5	_	ns
Address Advance Setup to Clock High	tADVS	2.5	-	2.5	-	ns
Chip Select Setup to Clock High	tCSS	2.5	-	2.5	-	ns
Address Hold from Clock High	tAH	0.5	-	0.5	-	ns
Address Status Hold from Clock High	tSH	0.5	-	0.5	-	ns
Data Hold from Clock High	tDH	0.5	-	0.5	-	ns
Write Hold from Clock High(GWE, BWE, CWEx)	tWH	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	tADVH	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	tCSH	0.5	-	0.5	-	ns
ZZ High to Power Down	tPDS	2	-	2	-	cycle
ZZ Low to Power Up	tPUS	2	-	2	-	cycle

NOTE:

^{1.} All address inputs must meet the specified setup and hold times for all rising clock(Clk) edges whenever CADS and/or ADSP is sampled low and this device is chip selected.

All other synchronous inputs must meet the specified sample and hold times whenever this device is chip selected.

^{2.} Both chip selects must be active whenever CADS or ADSP is sampled low in order to the device remained at enable.

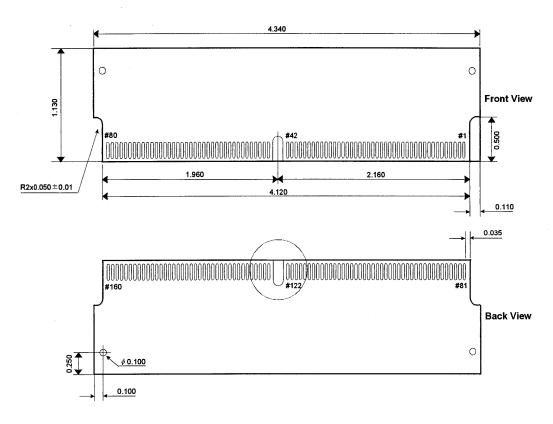
^{3.} CADS or ADSP must not be asserted for at least 2 Clocks after leaving ZZ state.

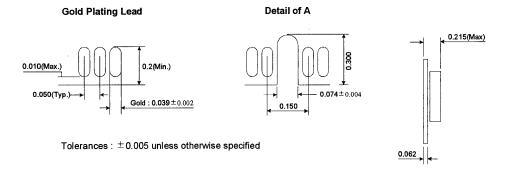
AC TIMING CHARACTERISTICS ON TAG RAM (TA =0 to 70 $^{\circ}$ C,Vcc5=5.0V $^{\pm}$ 5%)

Refers to the individual components, not the whole module

P	-m.t		Sumbol KMM764V75G-13		IV75G-13	KMM764V75G-15		
Parameter	Symbol	Min	Max	Min	Max	Unit		
Read Cycle Time	tRC	12	-	15	•	ns		
Address Access Time	tAA	-	12	-	15	ns		
Chip Select to Low-Z Output	tLZ	3	-	3	-	ns		
Output Hold from Address Change	tOH	3	-	3	-	ns		
Write cycle Time	tWC	12	-	15	-	ns		
Address Set-up Time	tAS	0	-	0	-	ns		
Address Valid to End of Write	tAW	9	-	12	-	ns		
Write Pulse Width	tWP	12	-	15	-	ns		
Write Recovery Time	tWR	0	-	0	-	ns		
Write to Output High-Z	tWHZ	0	6	0	8	ns		
Data to Write Time Overlap	tDW	7	-	8	-	ns		
Data Hold from Write Time	tDH	0	-	0	-	ns		
End Write to Output Low-Z	tOW	0	-	0	-	ns		

Units: Inches

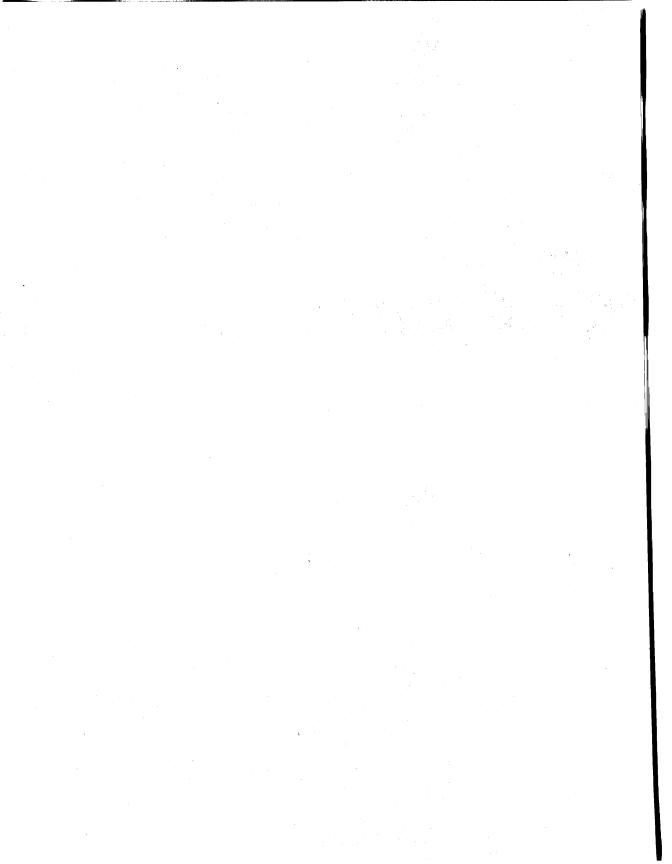


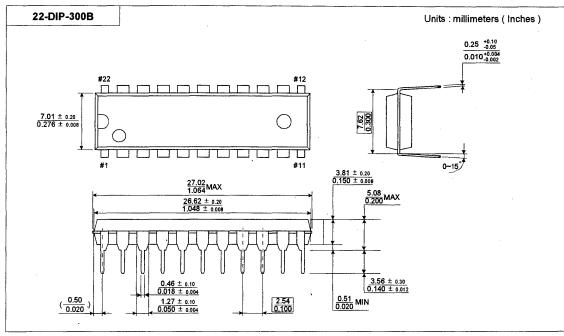


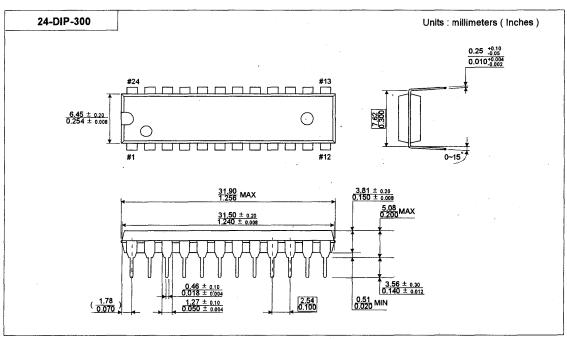


Package Dimensions 3

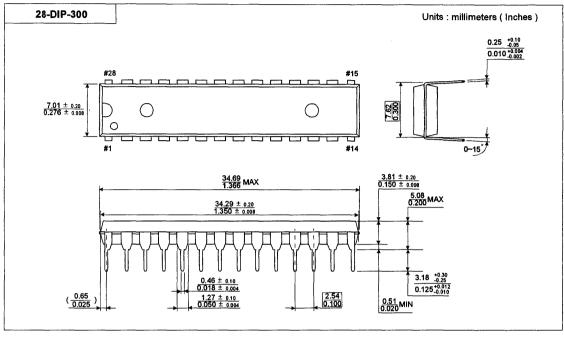


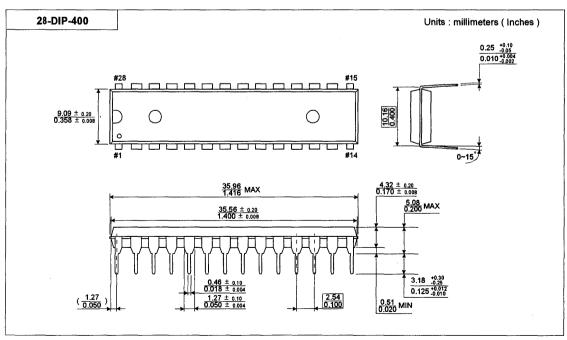




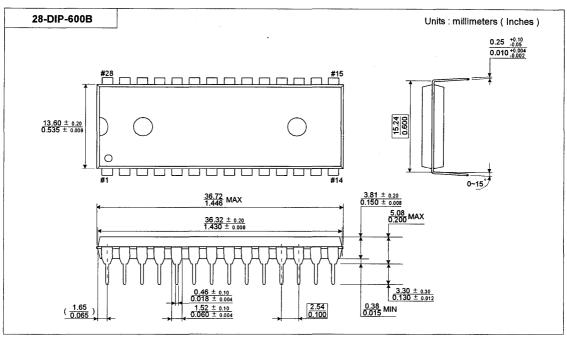


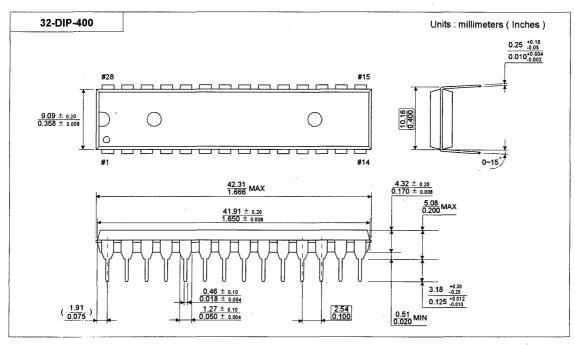




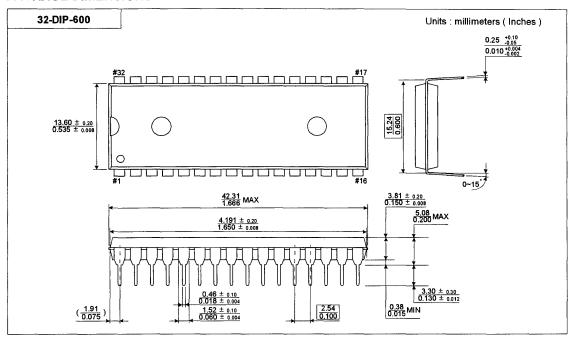


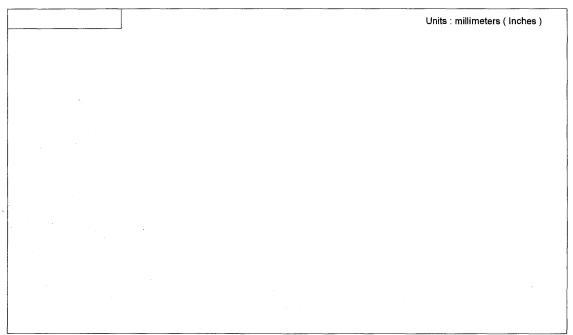




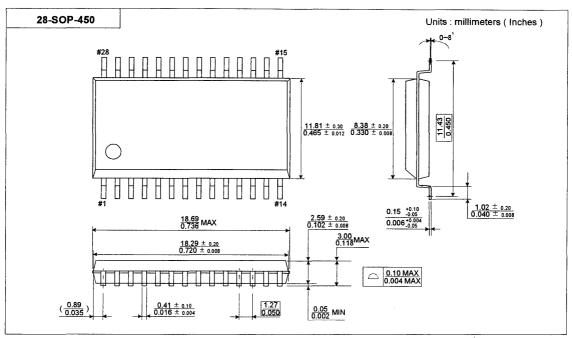


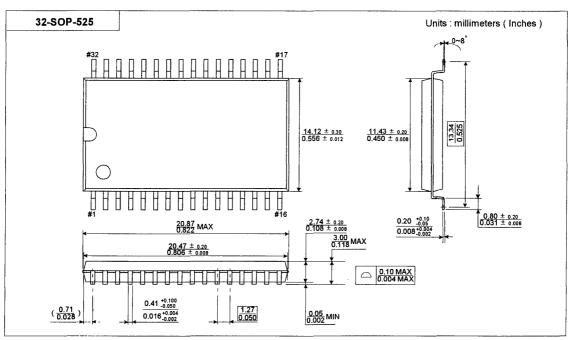


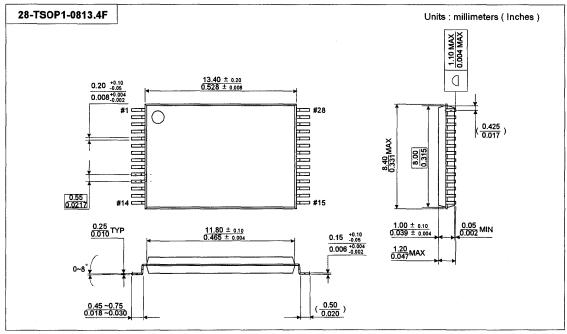


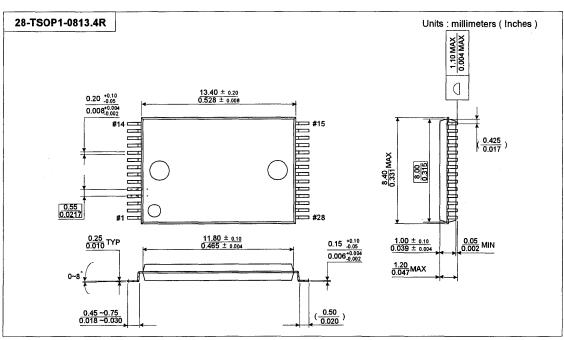




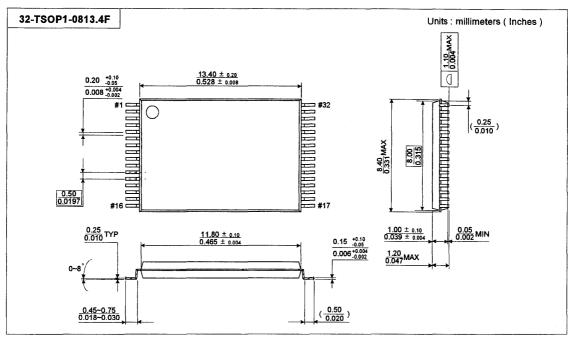


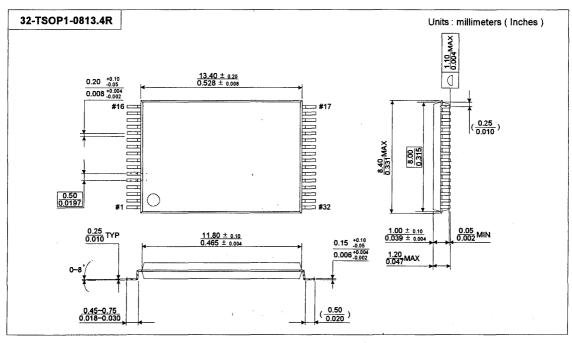


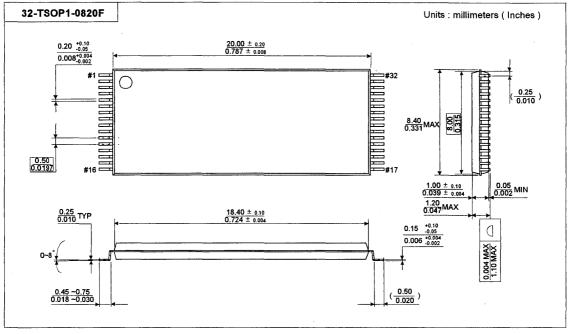


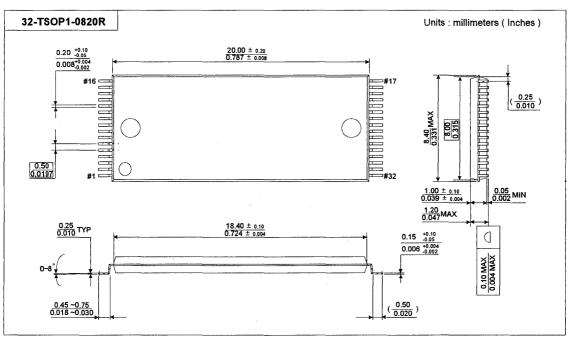




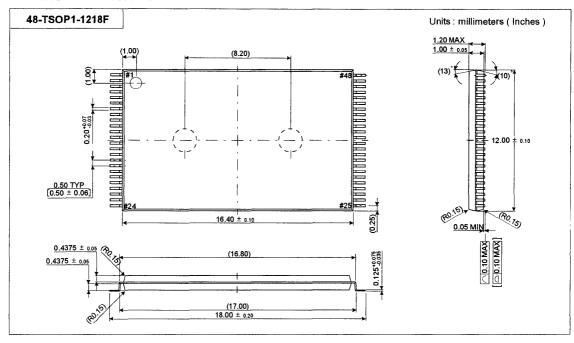


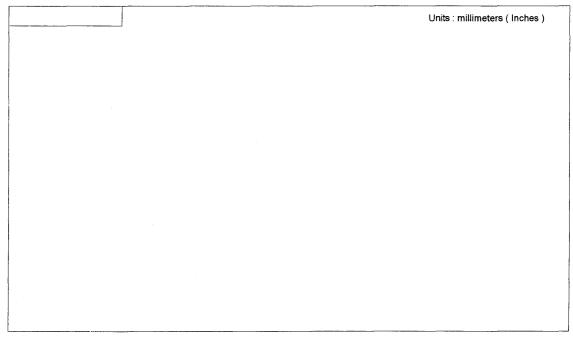


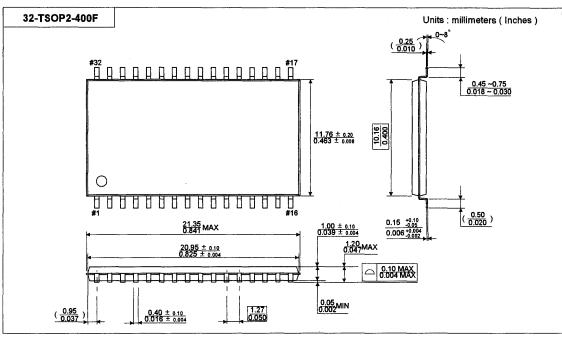


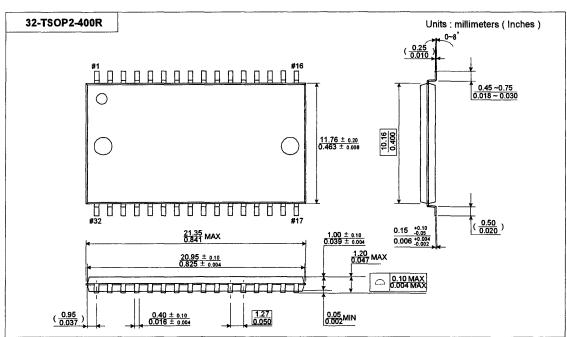




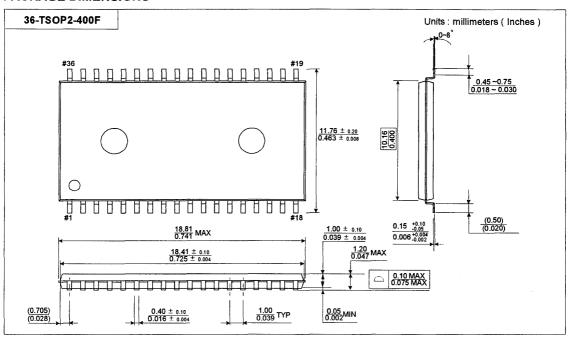




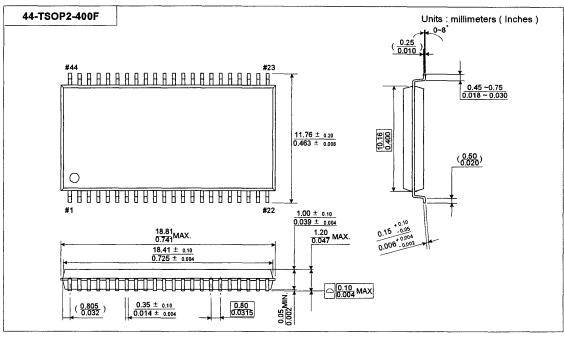


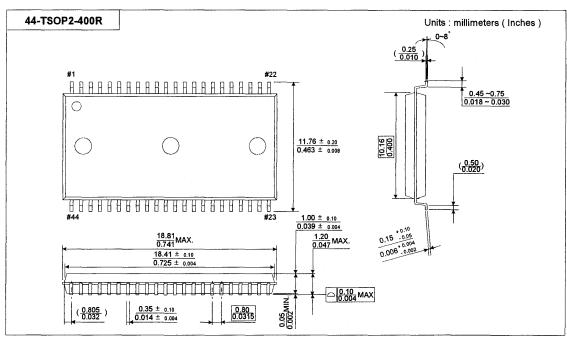




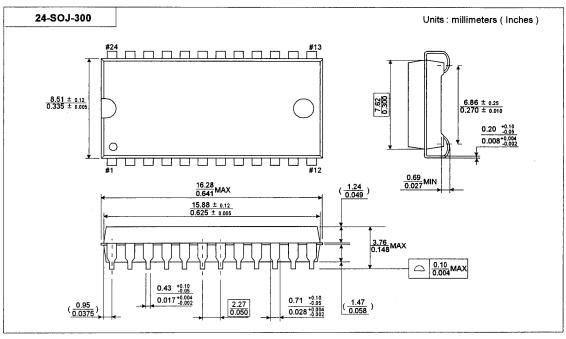


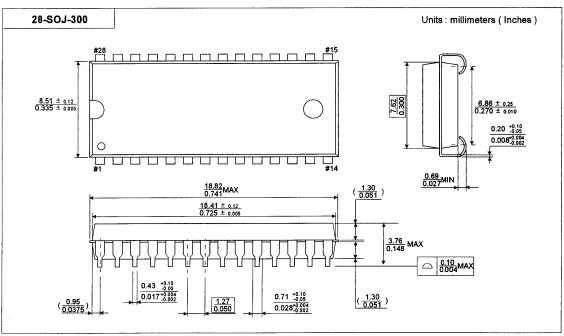
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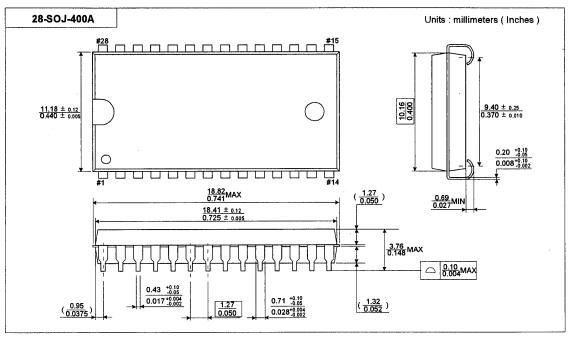


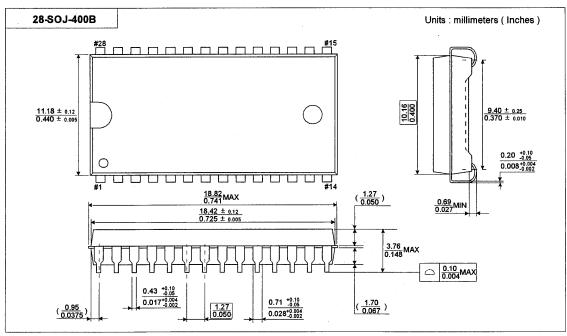




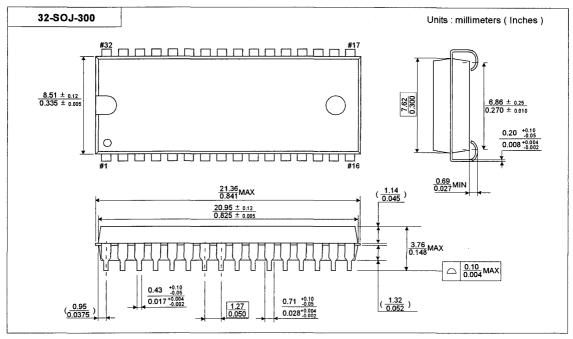


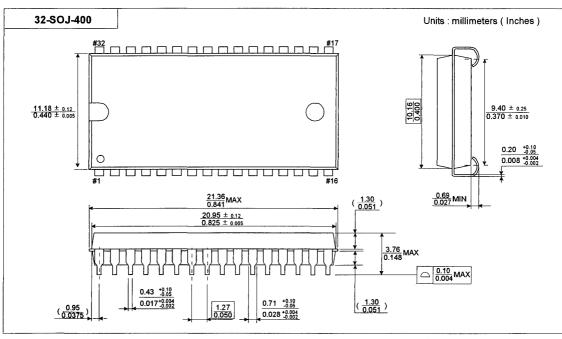




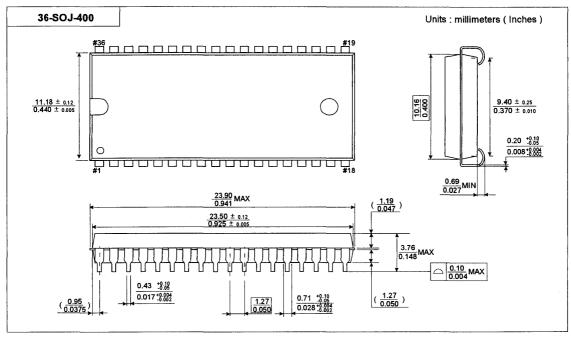


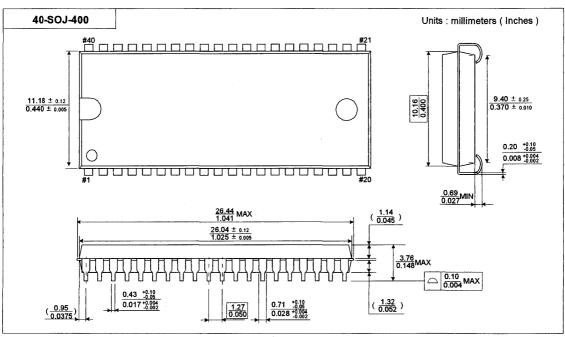




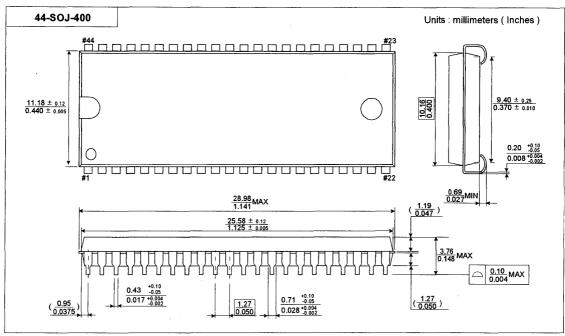


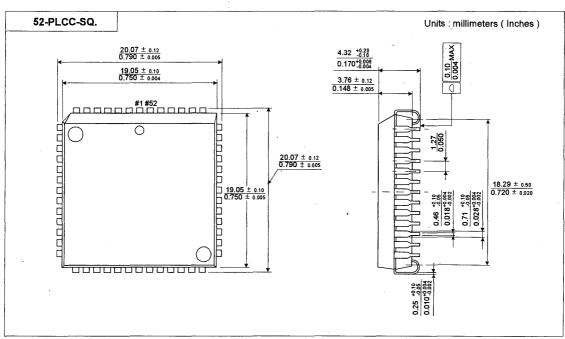




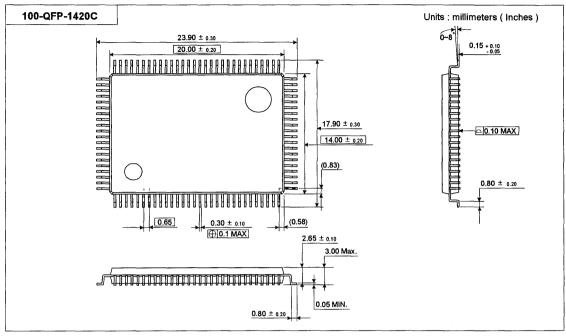


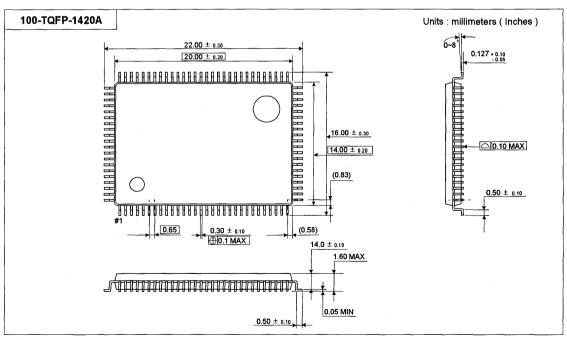


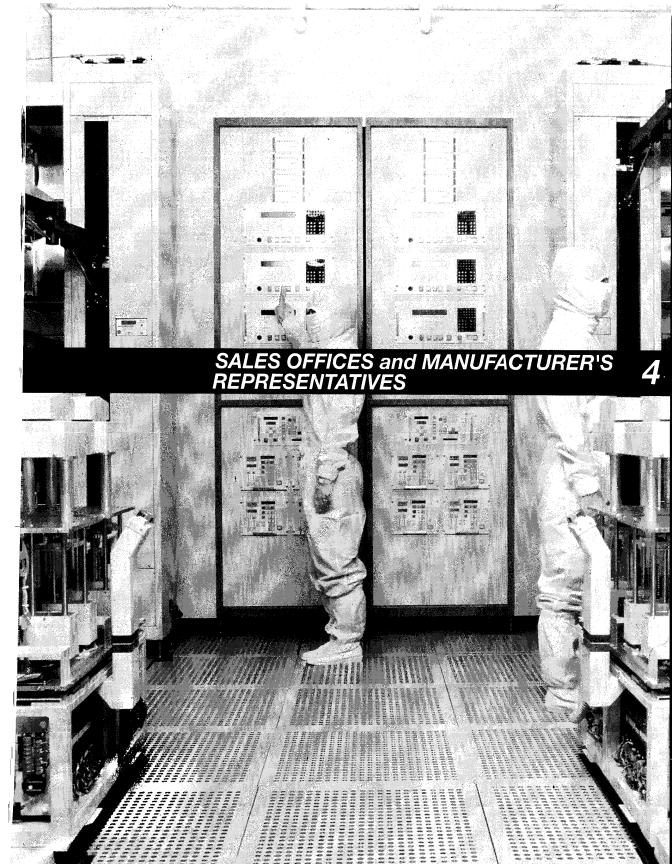












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ALL AMERICAN	TEL: 818-878-0555 FAX: 818-878-0533	Irvine, CA 92718 MILGRAY 6835 Flanders DR., STE #300	FAX: 714-753-1682 TEL: 619-457-7545
ALL AMERICAN 26010 Mureau RD., #120	FAX: 818-878-0533	Irvine, CA 92718 MILGRAY	FAX: 714-753-1682
ALL AMERICAN 26010 Mureau RD., #120 Calabasas, CA 91302 ALL AMERICAN 10805 Holder ST., #100	FAX: 818-878-0533 TEL: 714-229-8600	Irvine, CA 92718 MILGRAY 6835 Flanders DR., STE #300 San Diego, CA 92121	FAX: 714-753-1682 TEL: 619-457-7545
ALL AMERICAN 26010 Mureau RD., #120 Calabasas, CA 91302 ALL AMERICAN 10805 Holder ST., #100 Cypress, CA 90630	FAX: 818-878-0533	Irvine, CA 92718 MILGRAY 6835 Flanders DR., STE #300 San Diego, CA 92121 CANADA	FAX: 714-753-1682 TEL: 619-457-7545
ALL AMERICAN 26010 Mureau RD., #120 Calabasas, CA 91302 ALL AMERICAN 10805 Holder ST., #100 Cypress, CA 90630 ALL AMERICAN	FAX: 818-878-0533 TEL: 714-229-8600 FAX: 714-229-8603	Irvine, CA 92718 MILGRAY 6835 Flanders DR., STE #300 San Diego, CA 92121 CANADA ALL AMERICAN	FAX: 714-753-1682 TEL: 619-457-7545 FAX: 619-457-9750
ALL AMERICAN 26010 Mureau RD., #120 Calabasas, CA 91302 ALL AMERICAN 10805 Holder ST., #100 Cypress, CA 90630 ALL AMERICAN 6390 Greenwich DR., #170	FAX: 818-878-0533 TEL: 714-229-8600 FAX: 714-229-8603 TEL: 619-658-0200	Irvine, CA 92718 MILGRAY 6835 Flanders DR., STE #300 San Diego, CA 92121 CANADA ALL AMERICAN 6375 Dixie RD., Units 4,5 & 6	FAX: 714-753-1682 TEL: 619-457-7545 FAX: 619-457-9750 TEL: 905-670-5946
ALL AMERICAN 26010 Mureau RD., #120 Calabasas, CA 91302 ALL AMERICAN 10805 Holder ST., #100 Cypress, CA 90630 ALL AMERICAN 6390 Greenwich DR., #170 San Diego, CA 92122	FAX: 818-878-0533 TEL: 714-229-8600 FAX: 714-229-8603	Irvine, CA 92718 MILGRAY 6835 Flanders DR., STE #300 San Diego, CA 92121 CANADA ALL AMERICAN 6375 Dixie RD., Units 4,5 & 6 Mississauga, ON L5T2E7	FAX: 714-753-1682 TEL: 619-457-7545 FAX: 619-457-9750
ALL AMERICAN 26010 Mureau RD., #120 Calabasas, CA 91302 ALL AMERICAN 10805 Holder ST., #100 Cypress, CA 90630 ALL AMERICAN 6390 Greenwich DR., #170 San Diego, CA 92122 ALL AMERICAN	FAX: 818-878-0533 TEL: 714-229-8600 FAX: 714-229-8603 TEL: 619-658-0200 FAX: 619-658-0201	Irvine, CA 92718 MILGRAY 6835 Flanders DR., STE #300 San Diego, CA 92121 CANADA ALL AMERICAN 6375 Dixie RD., Units 4,5 & 6 Mississauga, ON L5T2E7 MILGRAY	FAX: 714-753-1682 TEL: 619-457-7545 FAX: 619-457-9750 TEL: 905-670-5946 FAX: 905-670-5947
ALL AMERICAN 26010 Mureau RD., #120 Calabasas, CA 91302 ALL AMERICAN 10805 Holder ST., #100 Cypress, CA 90630 ALL AMERICAN 6390 Greenwich DR., #170 San Diego, CA 92122 ALL AMERICAN 230 Devcon DR.,	FAX: 818-878-0533 TEL: 714-229-8600 FAX: 714-229-8603 TEL: 619-658-0200 FAX: 619-658-0201 TEL: 408-441-1300	Irvine, CA 92718 MILGRAY 6835 Flanders DR., STE #300 San Diego, CA 92121 CANADA ALL AMERICAN 6375 Dixie RD., Units 4,5 & 6 Mississauga, ON L5T2E7 MILGRAY 4185 Still Creek DR., STE #B201	FAX: 714-753-1682 TEL: 619-457-7545 FAX: 619-457-9750 TEL: 905-670-5946 FAX: 905-670-5947 TEL: 604-291-0044
ALL AMERICAN 26010 Mureau RD., #120 Calabasas, CA 91302 ALL AMERICAN 10805 Holder ST., #100 Cypress, CA 90630 ALL AMERICAN 6390 Greenwich DR., #170 San Diego, CA 92122 ALL AMERICAN 230 Devcon DR., San Jose, CA 95112	FAX: 818-878-0533 TEL: 714-229-8600 FAX: 714-229-8603 TEL: 619-658-0200 FAX: 619-658-0201	Irvine, CA 92718 MILGRAY 6835 Flanders DR., STE #300 San Diego, CA 92121 CANADA ALL AMERICAN 6375 Dixie RD., Units 4,5 & 6 Mississauga, ON L5T2E7 MILGRAY 4185 Still Creek DR., STE #B201 Burnaby, B.C. V5C6G9, CN	FAX: 714-753-1682 TEL: 619-457-7545 FAX: 619-457-9750 TEL: 905-670-5946 FAX: 905-670-5947
ALL AMERICAN 26010 Mureau RD., #120 Calabasas, CA 91302 ALL AMERICAN 10805 Holder ST., #100 Cypress, CA 90630 ALL AMERICAN 6390 Greenwich DR., #170 San Diego, CA 92122 ALL AMERICAN 230 Devcon DR., San Jose, CA 95112 ALL AMERICAN	FAX: 818-878-0533 TEL: 714-229-8600 FAX: 714-229-8603 TEL: 619-658-0200 FAX: 619-658-0201 TEL: 408-441-1300 FAX: 408-437-8970	Irvine, CA 92718 MILGRAY 6835 Flanders DR., STE #300 San Diego, CA 92121 CANADA ALL AMERICAN 6375 Dixie RD., Units 4,5 & 6 Mississauga, ON L5T2E7 MILGRAY 4185 Still Creek DR., STE #B201 Burnaby, B.C. V5C6G9, CN MILGRAY	FAX: 714-753-1682 TEL: 619-457-7545 FAX: 619-457-9750 TEL: 905-670-5946 FAX: 905-670-5947 TEL: 604-291-0044 FAX: 604-291-9939
ALL AMERICAN 26010 Mureau RD., #120 Calabasas, CA 91302 ALL AMERICAN 10805 Holder ST., #100 Cypress, CA 90630 ALL AMERICAN 6390 Greenwich DR., #170 San Diego, CA 92122 ALL AMERICAN 230 Devcon DR., San Jose, CA 95112 ALL AMERICAN 14192 Chambers RD.	FAX: 818-878-0533 TEL: 714-229-8600 FAX: 714-229-8603 TEL: 619-658-0200 FAX: 619-658-0201 TEL: 408-441-1300 FAX: 408-437-8970 TEL: 714-573-5000	Irvine, CA 92718 MILGRAY 6835 Flanders DR., STE #300 San Diego, CA 92121 CANADA ALL AMERICAN 6375 Dixie RD., Units 4,5 & 6 Mississauga, ON L5T2E7 MILGRAY 4185 Still Creek DR., STE #B201 Burnaby, B.C. V5C6G9, CN MILGRAY 6600 Trans Canada HWY. Suite #209	FAX: 714-753-1682 TEL: 619-457-7545 FAX: 619-457-9750 TEL: 905-670-5946 FAX: 905-670-5947 TEL: 604-291-0044 FAX: 604-291-9939 TEL: 514-426-5900
ALL AMERICAN 26010 Mureau RD., #120 Calabasas, CA 91302 ALL AMERICAN 10805 Holder ST., #100 Cypress, CA 90630 ALL AMERICAN 6390 Greenwich DR., #170 San Diego, CA 92122 ALL AMERICAN 230 Devcon DR., San Jose, CA 95112 ALL AMERICAN 14192 Chambers RD. Tustin, CA 92780	FAX: 818-878-0533 TEL: 714-229-8600 FAX: 714-229-8603 TEL: 619-658-0200 FAX: 619-658-0201 TEL: 408-441-1300 FAX: 408-437-8970	Irvine, CA 92718 MILGRAY 6835 Flanders DR., STE #300 San Diego, CA 92121 CANADA ALL AMERICAN 6375 Dixie RD., Units 4,5 & 6 Mississauga, ON L5T2E7 MILGRAY 4185 Still Creek DR., STE #B201 Burnaby, B.C. V5C6G9, CN MILGRAY 6600 Trans Canada HWY. Suite #209 Pointe Claire, Quebec, CN H9R4S2	FAX: 714-753-1682 TEL: 619-457-7545 FAX: 619-457-9750 TEL: 905-670-5946 FAX: 905-670-5947 TEL: 604-291-0044 FAX: 604-291-9939
ALL AMERICAN 26010 Mureau RD., #120 Calabasas, CA 91302 ALL AMERICAN 10805 Holder ST., #100 Cypress, CA 90630 ALL AMERICAN 6390 Greenwich DR., #170 San Diego, CA 92122 ALL AMERICAN 230 Devcon DR., San Jose, CA 95112 ALL AMERICAN 14192 Chambers RD. Tustin, CA 92780 ALL AMERICAN	FAX: 818-878-0533 TEL: 714-229-8600 FAX: 714-229-8603 TEL: 619-658-0200 FAX: 619-658-0201 TEL: 408-441-1300 FAX: 408-437-8970 TEL: 714-573-5000 FAX: 714-573-5050	Irvine, CA 92718 MILGRAY 6835 Flanders DR., STE #300 San Diego, CA 92121 CANADA ALL AMERICAN 6375 Dixie RD., Units 4,5 & 6 Mississauga, ON L5T2E7 MILGRAY 4185 Still Creek DR., STE #B201 Burnaby, B.C. V5C6G9, CN MILGRAY 6600 Trans Canada HWY. Suite #209 Pointe Claire, Quebec, CN H9R4S2 MILGRAY	FAX: 714-753-1682 TEL: 619-457-7545 FAX: 619-457-9750 TEL: 905-670-5946 FAX: 905-670-5947 TEL: 604-291-0044 FAX: 604-291-9339 TEL: 514-426-5900 FAX: 514-426-5836
ALL AMERICAN 26010 Mureau RD., #120 Calabasas, CA 91302 ALL AMERICAN 10805 Holder ST., #100 Cypress, CA 90630 ALL AMERICAN 6390 Greenwich DR., #170 San Diego, CA 92122 ALL AMERICAN 230 Devcon DR., San Jose, CA 95112 ALL AMERICAN 14192 Chambers RD. Tustin, CA 92780 ALL AMERICAN 111. S. Court ST., #104	FAX: 818-878-0533 TEL: 714-229-8600 FAX: 714-229-8603 TEL: 619-658-0200 FAX: 619-658-0201 TEL: 408-441-1300 FAX: 408-437-8970 TEL: 714-573-5000 FAX: 714-573-5050 TEL: 209-734-8861	Irvine, CA 92718 MILGRAY 6835 Flanders DR., STE #300 San Diego, CA 92121 CANADA ALL AMERICAN 6375 Dixie RD., Units 4,5 & 6 Mississauga, ON L5T2E7 MILGRAY 4185 Still Creek DR., STE #B201 Burnaby, B.C. V5C6G9, CN MILGRAY 6600 Trans Canada HWY. Suite #209 Pointe Claire, Quebec, CN H9R4S2 MILGRAY 2783 Thamesgate DR.,	TEL: 619-457-7545 FAX: 619-457-9750 TEL: 905-670-5946 FAX: 905-670-5947 TEL: 604-291-0044 FAX: 604-291-9939 TEL: 514-426-5900 FAX: 514-426-5836 TEL: 905-678-0958
ALL AMERICAN 26010 Mureau RD., #120 Calabasas, CA 91302 ALL AMERICAN 10805 Holder ST., #100 Cypress, CA 90630 ALL AMERICAN 6390 Greenwich DR., #170 San Diego, CA 92122 ALL AMERICAN 230 Devcon DR., San Jose, CA 95112 ALL AMERICAN 14192 Chambers RD. Tustin, CA 92780 ALL AMERICAN 111. S. Court ST., #104 Visalia, CA 93291	FAX: 818-878-0533 TEL: 714-229-8600 FAX: 714-229-8603 TEL: 619-658-0200 FAX: 619-658-0201 TEL: 408-441-1300 FAX: 408-437-8970 TEL: 714-573-5000 FAX: 714-573-5050	Irvine, CA 92718 MILGRAY 6835 Flanders DR., STE #300 San Diego, CA 92121 CANADA ALL AMERICAN 6375 Dixie RD., Units 4,5 & 6 Mississauga, ON L5T2E7 MILGRAY 4185 Still Creek DR., STE #B201 Burnaby, B.C. V5C6G9, CN MILGRAY 6600 Trans Canada HWY. Suite #209 Pointe Claire, Quebec, CN H9R4S2 MILGRAY	FAX: 714-753-1682 TEL: 619-457-7545 FAX: 619-457-9750 TEL: 905-670-5946 FAX: 905-670-5947 TEL: 604-291-0044 FAX: 604-291-9339 TEL: 514-426-5900 FAX: 514-426-5836
ALL AMERICAN 26010 Mureau RD., #120 Calabasas, CA 91302 ALL AMERICAN 10805 Holder ST., #100 Cypress, CA 90630 ALL AMERICAN 6390 Greenwich DR., #170 San Diego, CA 92122 ALL AMERICAN 230 Devcon DR., San Jose, CA 95112 ALL AMERICAN 14192 Chambers RD. Tustin, CA 92780 ALL AMERICAN 111. S. Court ST., #104 Visalia, CA 93291 BELL INDUSTRIES	FAX: 818-878-0533 TEL: 714-229-8600 FAX: 714-229-8603 TEL: 619-658-0200 FAX: 619-658-0201 TEL: 408-441-1300 FAX: 408-437-8970 TEL: 714-573-5000 FAX: 714-573-5050 TEL: 209-734-8861 FAX: 209-734-8865	Irvine, CA 92718 MILGRAY 6835 Flanders DR., STE #300 San Diego, CA 92121 CANADA ALL AMERICAN 6375 Dixie RD., Units 4,5 & 6 Mississauga, ON L5T2E7 MILGRAY 4185 Still Creek DR., STE #B201 Burnaby, B.C. V5C6G9, CN MILGRAY 6600 Trans Canada HWY. Suite #209 Pointe Claire, Quebec, CN H9R4S2 MILGRAY 2783 Tharnesgate DR., Mississauga, Ontario, CN L4T1G5	TEL: 619-457-7545 FAX: 619-457-9750 TEL: 905-670-5946 FAX: 905-670-5947 TEL: 604-291-0044 FAX: 604-291-9939 TEL: 514-426-5900 FAX: 514-426-5836 TEL: 905-678-0958
ALL AMERICAN 26010 Mureau RD., #120 Calabasas, CA 91302 ALL AMERICAN 10805 Holder ST., #100 Cypress, CA 90630 ALL AMERICAN 6390 Greenwich DR., #170 San Diego, CA 92122 ALL AMERICAN 230 Devcon DR., San Jose, CA 95112 ALL AMERICAN 14192 Chambers RD. Tustin, CA 92780 ALL AMERICAN 111. S. Court ST., #104 Visalia, CA 93291 BELL INDUSTRIES 11812 San Vicente BLVD., STE. 300	FAX: 818-878-0533 TEL: 714-229-8600 FAX: 714-229-8603 TEL: 619-658-0200 FAX: 619-658-0201 TEL: 408-441-1300 FAX: 408-437-8970 TEL: 714-573-5000 FAX: 714-573-5050 TEL: 209-734-8861 FAX: 209-734-8865 TEL: 310-447-6312	Irvine, CA 92718 MILGRAY 6835 Flanders DR., STE #300 San Diego, CA 92121 CANADA ALL AMERICAN 6375 Dixie RD., Units 4,5 & 6 Mississauga, ON L5T2E7 MILGRAY 4185 Still Creek DR., STE #B201 Burnaby, B.C. V5C6G9, CN MILGRAY 6600 Trans Canada HWY. Suite #209 Pointe Claire, Quebec, CN H9R4S2 MILGRAY 2783 Tharnesgate DR., Mississauga, Ontario, CN L4T1G5	TEL: 619-457-7545 FAX: 619-457-9750 TEL: 905-670-5946 FAX: 905-670-5947 TEL: 604-291-0044 FAX: 604-291-9939 TEL: 514-426-5900 FAX: 514-426-5836 TEL: 905-678-0958
ALL AMERICAN 26010 Mureau RD., #120 Calabasas, CA 91302 ALL AMERICAN 10805 Holder ST., #100 Cypress, CA 90630 ALL AMERICAN 6390 Greenwich DR., #170 San Diego, CA 92122 ALL AMERICAN 230 Devcon DR., San Jose, CA 95112 ALL AMERICAN 14192 Chambers RD. Tustin, CA 92780 ALL AMERICAN 111. S. Court ST., #104 Visalia, CA 93291 BELL INDUSTRIES 11812 San Vicente BLVD., STE. 300 Los Angeles, CA 90049	FAX: 818-878-0533 TEL: 714-229-8600 FAX: 714-229-8603 TEL: 619-658-0200 FAX: 619-658-0201 TEL: 408-441-1300 FAX: 408-437-8970 TEL: 714-573-5000 FAX: 714-573-5050 TEL: 209-734-8861 FAX: 209-734-8865	Irvine, CA 92718 MILGRAY 6835 Flanders DR., STE #300 San Diego, CA 92121 CANADA ALL AMERICAN 6375 Dixie RD., Units 4,5 & 6 Mississauga, ON L5T2E7 MILGRAY 4185 Still Creek DR., STE #B201 Burnaby, B.C. V5C6G9, CN MILGRAY 6600 Trans Canada HWY. Suite #209 Pointe Claire, Quebec, CN H9R4S2 MILGRAY 2783 Tharnesgate DR., Mississauga, Ontario, CN L4T1G5 COLORADO ALL AMERICAN	FAX: 714-753-1682 TEL: 619-457-7545 FAX: 619-457-9750 TEL: 905-670-5946 FAX: 905-670-5947 TEL: 604-291-0044 FAX: 604-291-9939 TEL: 514-426-5900 FAX: 514-426-5836 TEL: 905-678-0958 FAX: 905-678-1213
ALL AMERICAN 26010 Mureau RD., #120 Calabasas, CA 91302 ALL AMERICAN 10805 Holder ST., #100 Cypress, CA 90630 ALL AMERICAN 6390 Greenwich DR., #170 San Diego, CA 92122 ALL AMERICAN 230 Devcon DR., San Jose, CA 95112 ALL AMERICAN 14192 Chambers RD. Tustin, CA 92780 ALL AMERICAN 111. S. Court ST., #104 Visalia, CA 93291 BELL INDUSTRIES 11812 San Vicente BLVD., STE. 300 Los Angeles, CA 90049 BELL INDUSTRIES	FAX: 818-878-0533 TEL: 714-229-8600 FAX: 714-229-8603 TEL: 619-658-0200 FAX: 619-658-0201 TEL: 408-441-1300 FAX: 408-437-8970 TEL: 714-573-5000 FAX: 714-573-5050 TEL: 209-734-8861 FAX: 209-734-8865 TEL: 310-447-6312 FAX: 310-826-1534	Irvine, CA 92718 MILGRAY 6835 Flanders DR., STE #300 San Diego, CA 92121 CANADA ALL AMERICAN 6375 Dixie RD., Units 4,5 & 6 Mississauga, ON L5T2E7 MILGRAY 4185 Still Creek DR., STE #B201 Burnaby, B.C. V5C6G9, CN MILGRAY 6600 Trans Canada HWY. Suite #209 Pointe Claire, Quebec, CN H9R4S2 MILGRAY 2783 Thamesgate DR., Mississauga, Ontario, CN L4T1G5 COLORADO ALL AMERICAN 4090 Youngfield ST.,	FAX: 714-753-1682 TEL: 619-457-7545 FAX: 619-457-9750 TEL: 905-670-5946 FAX: 905-670-5947 TEL: 604-291-0044 FAX: 604-291-9939 TEL: 514-426-5836 TEL: 905-678-0958 FAX: 905-678-1213
ALL AMERICAN 26010 Mureau RD., #120 Calabasas, CA 91302 ALL AMERICAN 10805 Holder ST., #100 Cypress, CA 90630 ALL AMERICAN 6390 Greenwich DR., #170 San Diego, CA 92122 ALL AMERICAN 230 Devcon DR., San Jose, CA 95112 ALL AMERICAN 14192 Chambers RD. Tustin, CA 92780 ALL AMERICAN 111. S. Court ST., #104 Visalia, CA 93291 BELL INDUSTRIES 11812 San Vicente BLVD., STE. 300 Los Angeles, CA 90049 BELL INDUSTRIES 220 Technology DR., STE. 100	FAX: 818-878-0533 TEL: 714-229-8600 FAX: 714-229-8603 TEL: 619-658-0200 FAX: 619-658-0201 TEL: 408-441-1300 FAX: 408-437-8970 TEL: 714-573-5000 FAX: 714-573-5050 TEL: 209-734-8861 FAX: 209-734-8865 TEL: 310-447-6312 FAX: 310-826-1534 TEL: 714-727-4500	Irvine, CA 92718 MILGRAY 6835 Flanders DR., STE #300 San Diego, CA 92121 CANADA ALL AMERICAN 6375 Dixie RD., Units 4,5 & 6 Mississauga, ON L5T2E7 MILGRAY 4185 Still Creek DR., STE #B201 Burnaby, B.C. V5C6G9, CN MILGRAY 6600 Trans Canada HWY. Suite #209 Pointe Claire, Quebec, CN H9R4S2 MILGRAY 2783 Thamesgate DR., Mississauga, Ontario, CN L4T1G5 COLORADO ALL AMERICAN 4090 Youngfield ST., Wheatridge, CO 80033	FAX: 714-753-1682 TEL: 619-457-7545 FAX: 619-457-9750 TEL: 905-670-5946 FAX: 905-670-5947 TEL: 604-291-0044 FAX: 604-291-9939 TEL: 514-426-5900 FAX: 514-426-5836 TEL: 905-678-0958 FAX: 905-678-1213
ALL AMERICAN 26010 Mureau RD., #120 Calabasas, CA 91302 ALL AMERICAN 10805 Holder ST., #100 Cypress, CA 90630 ALL AMERICAN 6390 Greenwich DR., #170 San Diego, CA 92122 ALL AMERICAN 230 Devcon DR., San Jose, CA 95112 ALL AMERICAN 14192 Chambers RD. Tustin, CA 92780 ALL AMERICAN 111. S. Court ST., #104 Visalia, CA 93291 BELL INDUSTRIES 11812 San Vicente BLVD., STE. 300 Los Angeles, CA 90049 BELL INDUSTRIES 220 Technology DR., STE. 100 Irvine, CA 92718	FAX: 818-878-0533 TEL: 714-229-8600 FAX: 714-229-8603 TEL: 619-658-0200 FAX: 619-658-0201 TEL: 408-441-1300 FAX: 408-437-8970 TEL: 714-573-5000 FAX: 714-573-5050 TEL: 209-734-8861 FAX: 209-734-8865 TEL: 310-447-6312 FAX: 310-826-1534	Irvine, CA 92718 MILGRAY 6835 Flanders DR., STE #300 San Diego, CA 92121 CANADA ALL AMERICAN 6375 Dixie RD., Units 4,5 & 6 Mississauga, ON L5T2E7 MILGRAY 4185 Still Creek DR., STE #B201 Burnaby, B.C. V5C6G9, CN MILGRAY 6600 Trans Canada HWY. Suite #209 Pointe Claire, Quebec, CN H9R4S2 MILGRAY 2783 Thamesgate DR., Mississauga, Ontario, CN L4T1G5 COLORADO ALL AMERICAN 4090 Youngfield ST., Wheatridge, CO 80033 BELL INDUSTRIES	FAX: 714-753-1682 TEL: 619-457-7545 FAX: 619-457-9750 TEL: 905-670-5946 FAX: 905-670-5947 TEL: 604-291-0044 FAX: 604-291-9939 TEL: 514-426-5900 FAX: 514-426-5836 TEL: 905-678-0958 FAX: 905-678-1213
ALL AMERICAN 26010 Mureau RD., #120 Calabasas, CA 91302 ALL AMERICAN 10805 Holder ST., #100 Cypress, CA 90630 ALL AMERICAN 6390 Greenwich DR., #170 San Diego, CA 92122 ALL AMERICAN 230 Devcon DR., San Jose, CA 95112 ALL AMERICAN 14192 Chambers RD. Tustin, CA 92780 ALL AMERICAN 111. S. Court ST., #104 Visalia, CA 93291 BELL INDUSTRIES 11812 San Vicente BLVD., STE. 300 Los Angeles, CA 90049 BELL INDUSTRIES 220 Technology DR., STE. 100 Ivine, CA 92718 BELL INDUSTRIES	FAX: 818-878-0533 TEL: 714-229-8600 FAX: 714-229-8603 TEL: 619-658-0200 FAX: 619-658-0201 TEL: 408-441-1300 FAX: 408-437-8970 TEL: 714-573-5050 TEL: 209-734-8861 FAX: 209-734-8865 TEL: 310-447-6312 FAX: 310-826-1534 TEL: 714-727-4500 FAX: 714-453-4610	Irvine, CA 92718 MILGRAY 6835 Flanders DR., STE #300 San Diego, CA 92121 CANADA ALL AMERICAN 6375 Dixie RD., Units 4,5 & 6 Mississauga, ON L5T2E7 MILGRAY 4185 Still Creek DR., STE #B201 Burnaby, B.C. V5C6G9, CN MILGRAY 6600 Trans Canada HWY. Suite #209 Pointe Claire, Quebec, CN H9R4S2 MILGRAY 2783 Tharnesgate DR., Mississauga, Ontario, CN L4T1G5 COLORADO ALL AMERICAN 4090 Youngfield ST., Wheatridge, CO 80033 BELL INDUSTRIES 9351 Grant Street, STE. 460	TEL: 905-670-5946 FAX: 905-670-5946 FAX: 905-670-5947 TEL: 604-291-0044 FAX: 604-291-9939 TEL: 514-426-5900 FAX: 514-426-5836 TEL: 905-678-0958 FAX: 905-678-1213 TEL: 303-422-1701 FAX: 303-422-2529 TEL: 303-280-1115
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8787 Tumpike DR., STE #160	TEL: 303-657-2750	Schaumburg, IL 60173	FAX: 847-303-1996
Westminster, CO 80030	FAX: 303-657-2952	BELL INDUSTRIES	1744.047-000-1990
recommendation, and added	17017000 007 2002	175 W. Central RD.,	TEL: 847-202-6400
CONNECTICUT		Schaumburg, IL 60195	FAX: 847-202-5850
ALL AMERICAN		IEC	
100 Mill Plain RD., #360	TEL: 203-791-3816	2401 W.Hassell RD., Suite #1505	TEL: 847-843-2040
Danbury, CT 6811	FAX: 203-791-3801	Hoffman Estates, IL 60915	FAX: 847-843-2320
BELL INDUSTRIES		JACO	
1064 East Main ST.,	TEL: 203-639-6000	101 E. Commerce DR.,	TEL: 847-884-6620
Meridian, CT 1801	FAX: 203-639-6005	Schaumburg, IL 60173	FAX: 847-884-7573
MILGRAY	TEL . 000 070 5500	MILGRAY	TEL - 0.47 000 1000
326 W. MAIN ST.,	TEL: 203-878-5538 FAX: 203-878-6970	1530 E. Dundee RD.,	TEL: 847-202-1900 FAX: 847-202-1985
Milford, CT 6460	FAX: 203-8/8-09/0	Palatine, IL 60067	FAX: 847-202-1985
FLORIDA		INDIANA	
ADVENT		ADVENT	
111 North Palm AVE.,	TEL: 407-952-8669	8446 Moller RD.,	TEL: 317-872-4910
Indialantic, FL 32903	FAX: 407-984-2487	Indianapolis, IN 46268	FAX: 317-872-9987
ADVENT		BELL INDUSTRIES	
10500 NW 50th ST., #101	TEL: 954-748-9781	6982 Hillsdale Court	TEL: 317-842-4244
Sunrise, FL 33351	FAX: 954-748-9784	Indianapolis, IN 46250	FAX: 317-570-1344
ALL AMERICAN	*	BELL INDUSTRIES	
16115 N.W. 52nd AVE.,	TEL: 305-620-7831	525 Airport No. Office Park	TEL: 219-490-2100
Miami, FL 33014	FAX: 305-620-7831	Fort Wayne, IN 46825 MILGRAY	FAX: 219-490-2104
ALL AMERICAN 14450 46th ST., #116	TEL: 813-532-9800	5226 Elmwood AVE.,	FAX: 317-781-9997
Clearwater, FL 34622	FAX: 813-538-5567	Indianapolis, IN 46203	FAX: 317-718-6970
ALL AMERICAN	174.010 000 0001	11 Gianapolio, 114 40200	1700.017 110 0070
1400 E. Newport CTR. DR. #205	TEL: 954-429-2800	IOWA	
Deerfield Beach, FL 33442	FAX: 954-429-0391	ADVENT	
ALL AMERICAN		682 58TH AVE. CT. SW	TEL: 319-363-0221
16115 NW 52nd AVE.,	TEL: 305-621-8282	Cedar Rapids, IA 52404	FAX: 319-363-4514
Miami(Headquarters), FL 33014			
BELL INDUSTRIES		KANSAS	
650 S. Northlake BLVD., #400	TEL: 407-339-0078	ADVENT	
Altamonte Springs, FL 32701	FAX: 407-339-0139	9521 Mission RD.,	TEL: 913-381-9003
CHIP SUPPLY	TEL: 407-298-7100	Overland, KS 66206	FAX: 913-381-0866
7725 N. Orange Blossom Trail Corlando, FL 32810	FAX: 407-290-0164	MILGRAY	TEL: 913-236-8800
JACO	1700.407 250 0104	6400 Glenwood, STE #313 Overland Park, KS 66202	FAX: 913-384-6825
9900 West Sample RD., #404	TEL: 305-341-8280	Overland Park, NO 00202	174.910-304-0023
Coral Springs, FL 33065	FAX: 305-341-7848	MASSACHUSETTS	
MILGRAY		ALL AMERICAN	
755 Rinehart RD., STE #100	TEL: 407-321-2555	19C Crosby DR.,	TEL: 617-275-8888
Lakemary, FL 32746	FAX: 407-322-4225	Bedford, MA 1730	FAX: 617-275-1982
		BELL INDUSTRIES	
GEORGIA		100 Burtt RD., #G01	TEL: 508-623-3200
BELL INDUSTRIES		Andover, MA 1810	FAX: 508-474-8902
3850 Holcomb Bridge RD. Suite #110	TEL: 770-446-2333		



JACO		523 Fellowship Rd., STE #275	TEL: 609-778-1300
1053 East ST.,	TEL: 508-640-0010	MT. Laurel., NJ 8054	FAX: 609-778-7669
Tewksbury, MA 1876	FAX: 508-640-0755	MILGRAY	
MILGRAY	TEL - 500 057 5000	3799 Route 46 East Suite #303	TEL: 201-335-1766
187 Ballardvale ST. Wilmington, MA 1887	TEL: 508-657-5900 FAX: 508-658-7989	Parsippany, NJ 7054	FAX: 201-335-2110
Willington, WA 1887	FAX . 500-050-7-909	NEW YORK	
MARYLAND		ALL AMERICAN	
ALL AMERICAN		275B Marcus BLVD.	TEL: 516-434-9000
14636 Rothgeb DR.,	TEL: 301-251-1205	Hauppauge, NY 11788	FAX: 516-434-9394
Rockville, MD 20850	FAX: 301-251-8574	ALL AMERICAN	
		333 Metro Park	TEL: 716-292-6700
BELL INDUSTRIES		Rochester, NY 14623	FAX: 716-292-6755
8945 Guilford, RD., STE. 130	TEL: 410-290-5100	BELL INDUSTRIES	
Columbia, MD 21046	FAX: 410-290-8006	300 Vanderbilt Motor PKWY,	TEL: 516-435-8910
JACO 10260 Old Columbia RD	TEL: 410-995-6620	Suite #217, Hauppauge, NY 11788	FAX: 516-435-8913
Columbia, MD 21046	FAX: 410-995-6032	145 Oser AVE.	TEL: 516-273-5500
MILGRAY	1747.410-330-0002	Hauppauge, NY 11788	FAX: 516-273-5799
6460 Dobbin RD., STE #D	TEL: 410-730-6119	MILGRAY	1740.010 210 0100
Columbia, MD 21045	FAX: 410-730-8940	77 Schmitt BLVD.,	TEL: 516-391-3000
,		Farmingdale, NY 11735	FAX: 516-420-0685
MICHIGAN		MILGRAY	
ADVENT		1170 Pittsford-Victor RD., Suite #200	TEL: 716-381-9700
24713 Crestview CT.,	TEL: 810-477-1650	Pittsford, NY 14534	FAX: 716-381-9495
Farmington Hills, MI 48335	FAX: 313-477-2630	NORTH CAROLINA	
ALL AMERICAN	TEL . 040 404 0000	BELL INDUSTRIES	
39201 Schoolcraft RD., #B20 Livonia, Mi 48150	TEL: 313-464-2202 FAX: 313-464-2433	3100 Smoketree Court, STE, 800	TEL: 919-874-0011
LIVOHIA, IVII 46 150	FAX: 313-404-2433	Raleigh, NC 27604	FAX: 919-874-0013
MINESOTA		JACO	
MINESOTA ALL AMERICAN		JACO 5206 Greens Dairy RD.,	TEL: 919-876-7767
	TEL: 612-944-2151	JACO	TEL: 919-876-7767 FAX: 919-876-6964
ALL AMERICAN	TEL: 612-944-2151 FAX: 612-944-9803	JACO 5206 Greens Dairy RD., Raleigh, NC 27604	
ALL AMERICAN 7716 Golden Triangle DR., Eden Prarie, MN 55344 BELL INDUSTRIES	FAX: 612-944-9803	JACO 5206 Greens Dairy RD., Raleigh, NC 27604 OHIO	
ALL AMERICAN 7716 Golden Triangle DR., Eden Prarie, MN 55344 BELL INDUSTRIES 9401 James Avenue south, #142	FAX : 612-944-9803 TEL : 612-888-7747	JACO 5206 Greens Dairy RD., Raleigh, NC 27604	
ALL AMERICAN 7716 Golden Triangle DR., Eden Prarie, MN 55344 BELL INDUSTRIES 9401 James Avenue south, #142 Bloomington, MN 55431	FAX: 612-944-9803	JACO 5206 Greens Dairy RD., Raleigh, NC 27604 OHIO ALL AMERICAN	FAX: 919-876-6964
ALL AMERICAN 7716 Golden Triangle DR., Eden Prarie, MN 55344 BELL INDUSTRIES 9401 James Avenue south, #142 Bloomington, MN 55431 JACO	FAX: 612-944-9803 TEL: 612-888-7747 FAX: 612-888-7757	JACO 5206 Greens Dairy RD., Raleigh, NC 27604 OHIO ALL AMERICAN 26650 Renaissance PKWY. Warrenville Heights, OH 44128 BELL INDUSTRIES	FAX: 919-876-6964 TEL: 216-514-0625 FAX: 216-514-0822
ALL AMERICAN 7716 Golden Triangle DR., Eden Prarie, MN 55344 BELL INDUSTRIES 9401 James Avenue south, #142 Bloomington, MN 55431 JACO 10340 Viking DR., Suite #115	FAX: 612-944-9803 TEL: 612-888-7747 FAX: 612-888-7757 TEL: 612-941-2757	JACO 5206 Greens Dairy RD., Raleigh, NC 27604 OHIO ALL AMERICAN 26650 Renaissance PKWY. Warrenville Heights, OH 44128 BELL INDUSTRIES 31200 Solon RD., Suite 12	FAX: 919-876-6964 TEL: 216-514-0625 FAX: 216-514-0822 TEL: 216-498-2002
ALL AMERICAN 7716 Golden Triangle DR., Eden Prarie, MN 55344 BELL INDUSTRIES 9401 James Avenue south, #142 Bloomington, MN 55431 JACO	FAX: 612-944-9803 TEL: 612-888-7747 FAX: 612-888-7757	JACO 5206 Greens Dairy RD., Raleigh, NC 27604 OHIO ALL AMERICAN 26650 Renaissance PKWY. Warrenville Heights, OH 44128 BELL INDUSTRIES 31200 Solon RD., Suite 12 Solon, OH 44139	FAX: 919-876-6964 TEL: 216-514-0625 FAX: 216-514-0822
ALL AMERICAN 7716 Golden Triangle DR., Eden Prarie, MN 55344 BELL INDUSTRIES 9401 James Avenue south, #142 Bloomington, MN 55431 JACO 10340 Viking DR., Suite #115 Eden Prarie, MN 55344	FAX: 612-944-9803 TEL: 612-888-7747 FAX: 612-888-7757 TEL: 612-941-2757	JACO 5206 Greens Dairy RD., Raleigh, NC 27604 OHIO ALL AMERICAN 26650 Renaissance PKWY. Warrenville Heights, OH 44128 BELL INDUSTRIES 31200 Solon RD., Suite 12 Solon, OH 44139 BELL INDUSTRIES	FAX: 919-876-6964 TEL: 216-514-0625 FAX: 216-514-0822 TEL: 216-498-2002 FAX: 216-498-2006
ALL AMERICAN 7716 Golden Triangle DR., Eden Prarie, MN 55344 BELL INDUSTRIES 9401 James Avenue south, #142 Bloomington, MN 55431 JACO 10340 Viking DR., Suite #115	FAX: 612-944-9803 TEL: 612-888-7747 FAX: 612-888-7757 TEL: 612-941-2757	JACO 5206 Greens Dairy RD., Raleigh, NC 27604 OHIO ALL AMERICAN 26650 Renaissance PKWY. Warrenville Heights, OH 44128 BELL INDUSTRIES 31200 Solon RD., Suite 12 Solon, OH 44139 BELL INDUSTRIES 444 Windsor Park DR.,	TEL: 216-514-0625 FAX: 216-514-0822 TEL: 216-498-2002 FAX: 216-498-2006 TEL: 513-435-5922
ALL AMERICAN 7716 Golden Triangle DR., Eden Prarie, MN 55344 BELL INDUSTRIES 9401 James Avenue south, #142 Bloomington, MN 55431 JACO 10340 Viking DR., Suite #115 Eden Prarie, MN 55344	FAX: 612-944-9803 TEL: 612-888-7747 FAX: 612-888-7757 TEL: 612-941-2757	JACO 5206 Greens Dairy RD., Raleigh, NC 27604 OHIO ALL AMERICAN 26650 Renaissance PKWY. Warrenville Heights, OH 44128 BELL INDUSTRIES 31200 Solon RD., Suite 12 Solon, OH 44139 BELL INDUSTRIES 444 Windsor Park DR., Dayton, OH 45459	FAX: 919-876-6964 TEL: 216-514-0625 FAX: 216-514-0822 TEL: 216-498-2002 FAX: 216-498-2006
ALL AMERICAN 7716 Golden Triangle DR., Eden Prarie, MN 55344 BELL INDUSTRIES 9401 James Avenue south, #142 Bloomington, MN 55431 JACO 10340 Viking DR., Suite #115 Eden Prarie, MN 55344 MISSOURI ADVENT	FAX: 612-944-9803 TEL: 612-888-7747 FAX: 612-888-7757 TEL: 612-941-2757 FAX: 612-941-1989	JACO 5206 Greens Dairy RD., Raleigh, NC 27604 OHIO ALL AMERICAN 26650 Renaissance PKWY. Warrenville Heights, OH 44128 BELL INDUSTRIES 31200 Solon RD., Suite 12 Solon, OH 44139 BELL INDUSTRIES 444 Windsor Park DR., Dayton, OH 45459 BELL INDUSTRIES	TEL: 216-514-0625 FAX: 216-514-0822 TEL: 216-498-2002 FAX: 216-498-2006 TEL: 513-435-5922 FAX: 513-435-3122
ALL AMERICAN 7716 Golden Triangle DR., Eden Prarie, MN 55344 BELL INDUSTRIES 9401 James Avenue south, #142 Bloomington, MN 55431 JACO 10340 Viking DR., Suite #115 Eden Prarie, MN 55344 MISSOURI ADVENT 1029 East Terra Lane O'Fallon, MO 63366	FAX: 612-944-9803 TEL: 612-888-7747 FAX: 612-888-7757 TEL: 612-941-2757 FAX: 612-941-1989 TEL: 314-272-4281	JACO 5206 Greens Dairy RD., Raleigh, NC 27604 OHIO ALL AMERICAN 26650 Renaissance PKWY. Warrenville Heights, OH 44128 BELL INDUSTRIES 31200 Solon RD., Suite 12 Solon, OH 44139 BELL INDUSTRIES 444 Windsor Park DR., Dayton, OH 45459	TEL: 216-514-0625 FAX: 216-514-0822 TEL: 216-498-2002 FAX: 216-498-2006 TEL: 513-435-5922
ALL AMERICAN 7716 Golden Triangle DR., Eden Prarie, MN 55344 BELL INDUSTRIES 9401 James Avenue south, #142 Bloomington, MN 55431 JACO 10340 Viking DR., Suite #115 Eden Prarie, MN 55344 MISSOURI ADVENT 1029 East Terra Lane O'Fallon, MO 63366 NEW JERSEY	FAX: 612-944-9803 TEL: 612-888-7747 FAX: 612-888-7757 TEL: 612-941-2757 FAX: 612-941-1989 TEL: 314-272-4281	JACO 5206 Greens Dairy RD., Raleigh, NC 27604 OHIO ALL AMERICAN 26650 Renaissance PKWY. Warrenville Heights, OH 44128 BELL INDUSTRIES 31200 Solon RD., Suite 12 Solon, OH 44139 BELL INDUSTRIES 444 Windsor Park DR., Dayton, OH 45459 BELL INDUSTRIES 446 Windsor Park DR.,	TEL: 216-514-0625 FAX: 216-514-0822 TEL: 216-498-2002 FAX: 216-498-2006 TEL: 513-435-5922 FAX: 513-435-3122 TEL: 513-434-8231
ALL AMERICAN 7716 Golden Triangle DR., Eden Prarie, MN 55344 BELL INDUSTRIES 9401 James Avenue south, #142 Bloomington, MN 55431 JACO 10340 Viking DR., Suite #115 Eden Prarie, MN 55344 MISSOURI ADVENT 1029 East Terra Lane O'Fallon, MO 63366 NEW JERSEY ADVENT	FAX: 612-944-9803 TEL: 612-888-7747 FAX: 612-888-7757 TEL: 612-941-2757 FAX: 612-941-1989 TEL: 314-272-4281 FAX: 314-272-2950	JACO 5206 Greens Dairy RD., Raleigh, NC 27604 OHIO ALL AMERICAN 26650 Renaissance PKWY. Warrenville Heights, OH 44128 BELL INDUSTRIES 31200 Solon RD., Suite 12 Solon, OH 44139 BELL INDUSTRIES 444 Windsor Park DR., Dayton, OH 45459 BELL INDUSTRIES 446 Windsor Park DR., Dayton, OH 45459 BELL INDUSTRIES 446 Windsor Park DR., Dayton, OH 45459 MILGRAY 6155 Rockside RD., STE #206	TEL: 216-514-0625 FAX: 216-514-0822 TEL: 216-498-2002 FAX: 216-498-2006 TEL: 513-435-5922 FAX: 513-435-3122 TEL: 513-434-8231 FAX: 513-434-8103 TEL: 216-447-1520
ALL AMERICAN 7716 Golden Triangle DR., Eden Prarie, MN 55344 BELL INDUSTRIES 9401 James Avenue south, #142 Bioomington, MN 55431 JACO 10340 Viking DR., Suite #115 Eden Prarie, MN 55344 MISSOURI ADVENT 1029 East Terra Lane O'Fallon, MO 63366 NEW JERSEY ADVENT 600 Penn ST.,	FAX: 612-944-9803 TEL: 612-888-7747 FAX: 612-888-7757 TEL: 612-941-2757 FAX: 612-941-1989 TEL: 314-272-4281 FAX: 314-272-2950 TEL: 609-964-8560	JACO 5206 Greens Dairy RD., Raleigh, NC 27604 OHIO ALL AMERICAN 26650 Renaissance PKWY. Warrenville Heights, OH 44128 BELL INDUSTRIES 31200 Solon RD., Suite 12 Solon, OH 44139 BELL INDUSTRIES 444 Windsor Park DR., Dayton, OH 45459 BELL INDUSTRIES 446 Windsor Park DR., Dayton, OH 45459 MILGRAY	FAX: 919-876-6964 TEL: 216-514-0625 FAX: 216-514-0822 TEL: 216-498-2006 TEL: 513-435-5922 FAX: 513-435-3122 TEL: 513-434-8231 FAX: 513-434-8103
ALL AMERICAN 7716 Golden Triangle DR., Eden Prarie, MN 55344 BELL INDUSTRIES 9401 James Avenue south, #142 Bioornington, MN 55431 JACO 10340 Viking DR., Suite #115 Eden Prarie, MN 55344 MISSOURI ADVENT 1029 East Terra Lane O'Fallon, MO 63366 NEW JERSEY ADVENT 600 Penn ST., Camden, NJ 8102	FAX: 612-944-9803 TEL: 612-888-7747 FAX: 612-888-7757 TEL: 612-941-2757 FAX: 612-941-1989 TEL: 314-272-4281 FAX: 314-272-2950	JACO 5206 Greens Dairy RD., Raleigh, NC 27604 OHIO ALL AMERICAN 26650 Renaissance PKWY. Warrenville Heights, OH 44128 BELL INDUSTRIES 31200 Solon RD., Suite 12 Solon, OH 44139 BELL INDUSTRIES 444 Windsor Park DR., Dayton, OH 45459 BELL INDUSTRIES 446 Windsor Park DR., Dayton, OH 45459 MILGRAY 6155 Rockside RD., STE #206 Cleveland, OH 44131	TEL: 216-514-0625 FAX: 216-514-0822 TEL: 216-498-2002 FAX: 216-498-2006 TEL: 513-435-5922 FAX: 513-435-3122 TEL: 513-434-8231 FAX: 513-434-8103 TEL: 216-447-1520
ALL AMERICAN 7716 Golden Triangle DR., Eden Prarie, MN 55344 BELL INDUSTRIES 9401 James Avenue south, #142 Bloomington, MN 55431 JACO 10340 Viking DR., Suite #115 Eden Prarie, MN 55344 MISSOURI ADVENT 1029 East Terra Lane O'Fallon, MO 63366 NEW JERSEY ADVENT 600 Penn ST., Camden, NJ 8102 ALL AMERICAN	FAX: 612-944-9803 TEL: 612-888-7747 FAX: 612-888-7757 TEL: 612-941-2757 FAX: 612-941-1989 TEL: 314-272-4281 FAX: 314-272-2950 TEL: 609-964-8560 FAX: 609-964-0423	JACO 5206 Greens Dairy RD., Raleigh, NC 27604 OHIO ALL AMERICAN 26650 Renaissance PKWY. Warrenville Heights, OH 44128 BELL INDUSTRIES 31200 Solon RD., Suite 12 Solon, OH 44139 BELL INDUSTRIES 444 Windsor Park DR., Dayton, OH 45459 BELL INDUSTRIES 446 Windsor Park DR., Dayton, OH 45459 MILGRAY 6155 Rockside RD., STE #206 Cleveland, OH 44131 OREGON	TEL: 216-514-0625 FAX: 216-514-0822 TEL: 216-498-2002 FAX: 216-498-2006 TEL: 513-435-5922 FAX: 513-435-3122 TEL: 513-434-8231 FAX: 513-434-8103 TEL: 216-447-1520
ALL AMERICAN 7716 Golden Triangle DR., Eden Prarie, MN 55344 BELL INDUSTRIES 9401 James Avenue south, #142 Bioornington, MN 55431 JACO 10340 Viking DR., Suite #115 Eden Prarie, MN 55344 MISSOURI ADVENT 1029 East Terra Lane O'Fallon, MO 63366 NEW JERSEY ADVENT 600 Penn ST., Camden, NJ 8102	FAX: 612-944-9803 TEL: 612-888-7747 FAX: 612-888-7757 TEL: 612-941-2757 FAX: 612-941-1989 TEL: 314-272-4281 FAX: 314-272-2950 TEL: 609-964-8560	JACO 5206 Greens Dairy RD., Raleigh, NC 27604 OHIO ALL AMERICAN 26650 Renaissance PKWY. Warrenville Heights, OH 44128 BELL INDUSTRIES 31200 Solon RD., Suite 12 Solon, OH 44139 BELL INDUSTRIES 444 Windsor Park DR., Dayton, OH 45459 BELL INDUSTRIES 446 Windsor Park DR., Dayton, OH 45459 MILGRAY 6155 Rockside RD., STE #206 Cleveland, OH 44131	TEL: 216-514-0625 FAX: 216-514-0822 TEL: 216-498-2002 FAX: 216-498-2006 TEL: 513-435-5922 FAX: 513-435-3122 TEL: 513-434-8231 FAX: 513-434-8103 TEL: 216-447-1520
ALL AMERICAN 7716 Golden Triangle DR., Eden Prarie, MN 55344 BELL INDUSTRIES 9401 James Avenue south, #142 Bloomington, MN 55431 JACO 10340 Viking DR., Suite #115 Eden Prarie, MN 55344 MISSOURI ADVENT 1029 East Terra Lane O'Fallon, MO 63366 NEW JERSEY ADVENT 600 Penn ST., Camden, NJ 8102 ALL AMERICAN 8. E. Stow RD., #100	FAX: 612-944-9803 TEL: 612-888-7747 FAX: 612-888-7757 TEL: 612-941-2757 FAX: 612-941-1989 TEL: 314-272-4281 FAX: 314-272-2950 TEL: 609-964-8560 FAX: 609-964-0423 TEL: 609-596-6666	JACO 5206 Greens Dairy RD., Raleigh, NC 27604 OHIO ALL AMERICAN 26650 Renaissance PKWY. Warrenville Heights, OH 44128 BELL INDUSTRIES 31200 Solon RD., Suite 12 Solon, OH 44139 BELL INDUSTRIES 444 Windsor Park DR., Dayton, OH 45459 BELL INDUSTRIES 446 Windsor Park DR., Dayton, OH 45459 BELL INDUSTRIES 446 Windsor Park DR., Dayton, OH 45459 MILGRAY 6155 Rockside RD., STE #206 Cleveland, OH 44131 OREGON ALL AMERICAN	FAX: 919-876-6964 TEL: 216-514-0625 FAX: 216-514-0822 TEL: 216-498-2006 TEL: 513-435-5922 FAX: 513-435-3122 TEL: 513-434-8231 FAX: 513-434-8103 TEL: 216-447-1520 FAX: 216-447-1761
ALL AMERICAN 7716 Golden Triangle DR., Eden Prarie, MN 55344 BELL INDUSTRIES 9401 James Avenue south, #142 Bloomington, MN 55431 JACO 10340 Viking DR., Suite #115 Eden Prarie, MN 55344 MISSOURI ADVENT 1029 East Terra Lane O'Fallon, MO 63366 NEW JERSEY ADVENT 600 Penn ST., Camden, NJ 8102 ALL AMERICAN 8. E. Stow RD., #100 Martton, NJ 8053	FAX: 612-944-9803 TEL: 612-888-7747 FAX: 612-888-7757 TEL: 612-941-2757 FAX: 612-941-1989 TEL: 314-272-4281 FAX: 314-272-2950 TEL: 609-964-8560 FAX: 609-964-0423 TEL: 609-596-6666 FAX: 609-797-1700	JACO 5206 Greens Dairy RD., Raleigh, NC 27604 OHIO ALL AMERICAN 26650 Renaissance PKWY. Warrenville Heights, OH 44128 BELL INDUSTRIES 31200 Solon RD., Suite 12 Solon, OH 44139 BELL INDUSTRIES 444 Windsor Park DR., Dayton, OH 45459 BELL INDUSTRIES 446 Windsor Park DR., Dayton, OH 45459 MILGRAY 6155 Rockside RD., STE #206 Cleveland, OH 44131 OREGON ALL AMERICAN 1815 NW 169th PL., Suite #6025	FAX: 919-876-6964 TEL: 216-514-0625 FAX: 216-514-0822 TEL: 216-498-2002 FAX: 216-498-2006 TEL: 513-435-5922 FAX: 513-435-3122 TEL: 513-434-8231 FAX: 513-434-8103 TEL: 216-447-1520 FAX: 216-447-1761
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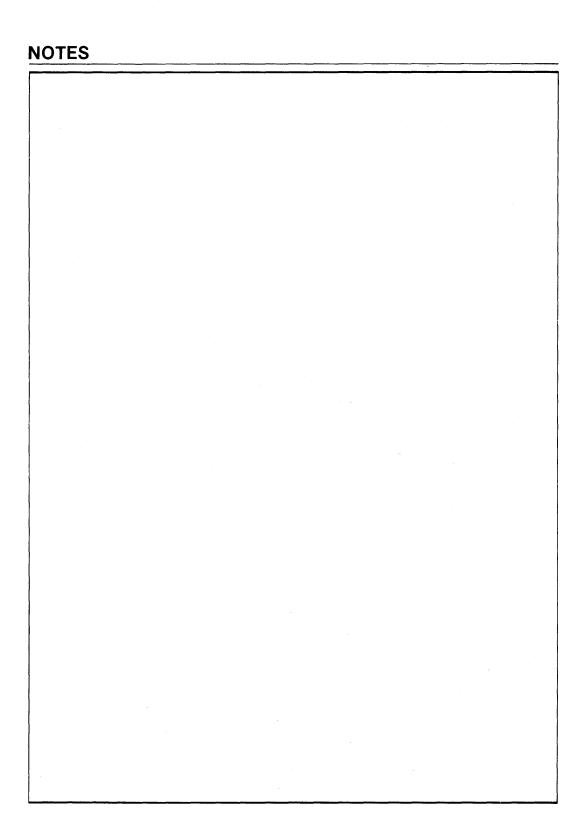
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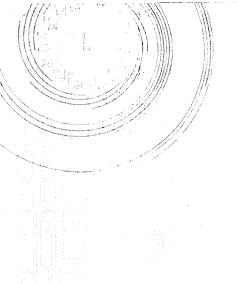
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