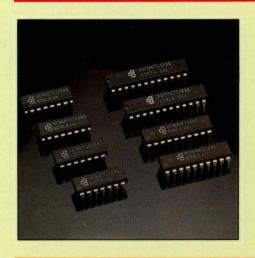


# High Performance CMOS Logic Data Book



1988

#### INTRODUCTION

Samsung Semiconductor is a broad-line manufacturer of semiconductors that range from VLSI circuits such as memories (DRAM, SRAM, EPROM and EEPROM), microprocessors, gate arrays and programmable logic to transistors, linear circuits and telecommunications products.

The KS54/74AHCT and the KS54/74HCTLS high-performance CMOS logic families are Samsung's entry into the general purpose digital logic area.

The KS54/74AHCT advanced high-speed CMOS family is designed to provide performance equivalent to or better than that of the bipolar 54/74ALS (Advanced Low-power Scholttky) family with the additional CMOS advantages of low power dissipation and high noise immunity. The AHCT parts can therefore be used as direct plug-in replacements for their ALS counterparts (and in most applications for FAST and Schottky) and improve the system performance.

The 54/74HCTLS high-speed CMOS family offers similar benefits as a replacement for industry-standard 54/74LS (Low-power Schottky), 54/74HCT and 54/74HC. While meeting all of the HCT electrical specifications, it also provides improved speed and drive capability, so that LS parts can be replaced with no performance degradation.

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## High Performance CMOS Logic Data Book

KS54/74AHCT
Advanced High-Speed CMOS

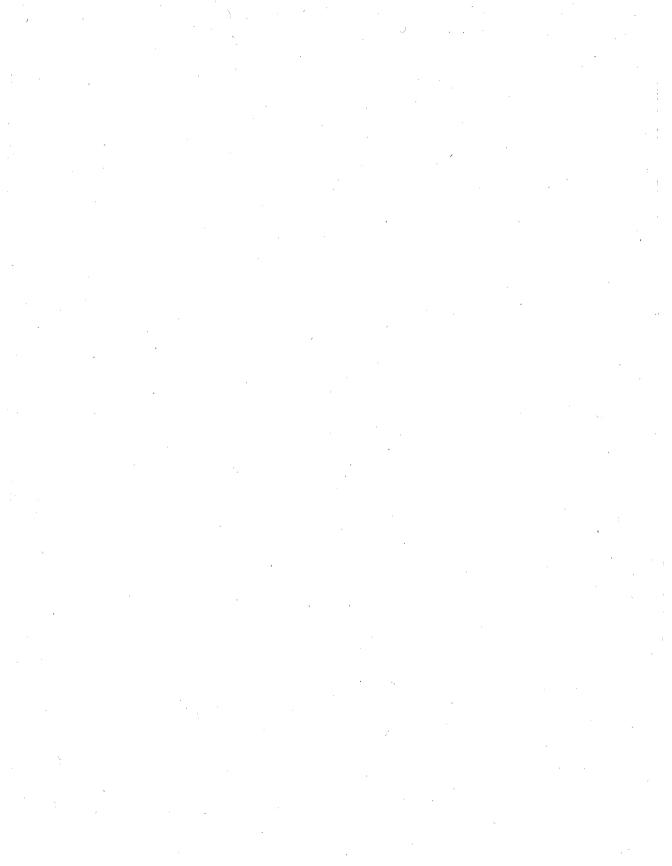
KS54/74HCTLS High-Speed CMOS

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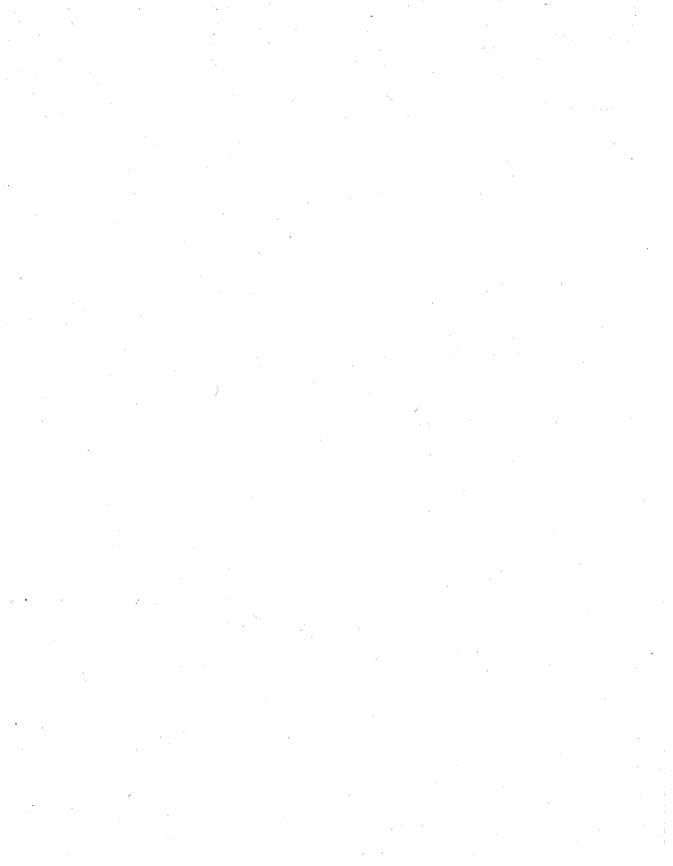
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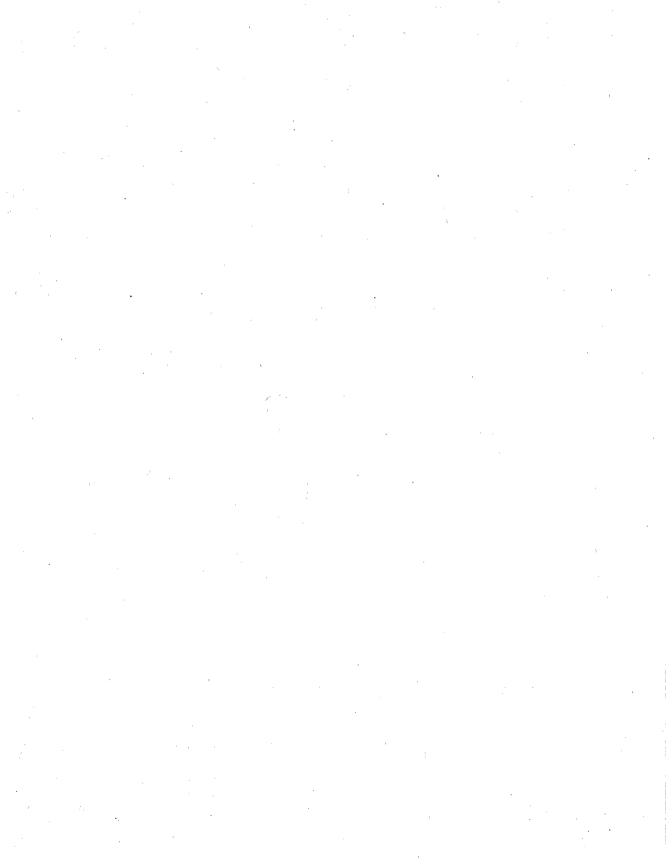
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S54/74HCTLS595	8-Bit Shift Registers with Output Latches	702
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S54/74HCTLS640	Octal Bus Transceivers with 3-State Outputs	709
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S54/74HCTLS645	Octal Bus Transceivers with 3-State Outputs	709
(S54/74HCTLS646	Octal 3-State Transceivers with Registers	712
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S54/74HCTLS658	Octal Bus Transceivers with Parity	720
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S54/74HCTLS664	Octal Bus Transceivers with Parity	724
(S54/74HCTLS665	Octal Bus Transceivers with Parity	724
(S54/74HCTLS670	4-By-4 Register Files with 3-State Outputs	728
(S54/74HCTLS679	12-Bit Address Comparators	732
(S54/74HCTLS680	12-Bit Address Comparators	732
(S54/74HCTLS682	8-Bit Magnitude Comparators	737
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S54/74HCTLS794	10-Bit Bus Interface Registers with 3-State Outputs	749
(S54/74HCTLS821	10-Bit Bus Interface Registers with 3-State Outputs	749
(S54/74HCTLS823	9-Bit Bus Interface Registers with 3-State Outputs	753
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	9-Bit Bus Interface Registers with 3-State Outputs	757
S54/74HCLTS825	8-Bit Bus Interface Registers with 3-State Outputs	757
(S54/74HCTLS826	8-Bit Bus Interface Registers with 3-State Outputs	761
(S54/74HCTLS841	10-Bit Bus Interface Registers with 3-State Outputs	761
(S54/74HCTLS842	10-Bit Bus Interface Registers with 3-State Outputs	
(S54/74HCTLS843	9-Bit Bus Interface Registers with 3-State Outputs	765 765
(S54/74HCTLS844	9-Bit Bus Interface Registers with 3-State Outputs	769
(S54/74HCTLS845	8-Bit Bus Interface Registers with 3-State Outputs	
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(S54/74HCTLS4049	Hex inverting Logic level Down Converters	773
KS54/74HCTLS4050	Hex Logic Level Down Converters	773



## 2. Functional Selection Guide

Function	Part Number KS54/74AHCT KS54/74HCTLS	Description	Package
Gates and	00	Quad 2-Input NAND Gates	14 DIP
Inverters	01	Quad 2-Input NAND Gates with Open-Drain Outputs	14 DIP
	02	Quad 2-Input NOR Gates	14 DIP
	03	Quad 2-Input NAND Gates with Open-Drain Outputs	14 DIP
	04	Hex Inverters	14 DIP
	05	Hex Inverters with Open-Drain Outputs	14 DIP
	08	Quad 2-Input AND Gates	14 DIP
	09	Quad 2-Input AND Gates with Open-Drain Outputs	- 14 DIP
	10	Triple 3-Input NAND Gates	14 DIP
	11	Triple 3-Input AND Gates	14 DIP
	12	Triple 3-Input NAND Gates with Open-Drain Outputs	14 DIP
•	14	Hex Schmitt-Trigger Inverters	14 DIP
	20	Dual 4-Input NAND Gates	14 DIP
	. 21	Dual 4-Input AND Gates	14 DIP
	22	Dual 4-Input NAND Gates with Open-Drain Outputs	14 DIP
	27	Triple 3-Input NOR Gates	14 DIP
	30	8-Input NAND Gate	14 DIP
	32	Quad 2-Input OR Gates	14 DIP
	51	Dual AND-OR-Invert Gates	14 DIP
	58	Dual AND-OR Gates	14 DIP
	86	Quad 2-Input Exclusive-OR Gates	14 DIP
	132	Quad 2-Input NAND Gates with Schmitt-Trigger Inputs	14 DIP
	133	13-Input NAND Gates	16 DIP
	266	Quad Exclusive-NOR Gates with Open Drain Outputs	14 DIP
Buffers	125	Quad Buffers with 3-State Outputs	14 DIP
and	126	Quad Buffers with 3-State Outputs	14 DIP
Line	210	Octal Buffers and Line Drivers with 3-State Outputs	20 DIP
Drivers	240	Octal Buffers and Line Drivers with 3-State Outputs	20 DIP
	241	Octal Buffers and Line Drivers with 3-State Outputs	20 DIP
	244	Octal Buffers and Line Drivers with 3-State Outputs	20 DIP
	365	Hex Bus-Drivers with 3-State Outputs	16 DIP
	366	Hex Bus-Drivers with 3-State Outputs	16 DIP
	367	Hex Bus-Drivers with 3-State Outputs	16 DIP
	368	Hex Bus-Drivers with 3-State Outputs	16 DIP
	465	Octal Buffers and Line Drivers with 3-State Outputs	20 DIP
	466	Octal Buffers and Line Drivers with 3-State Outputs	20 DIP
	467	Octal Buffers and Line Drivers with 3-State Outputs	20 DIP
	468	Octal Buffers and Line Drivers with 3-State Outputs	20 DIP
	540	Octal Buffers and Line Drivers with 3-State Outputs	20 DIP
	541	Octal Buffers and Line Drivers with 3-State Outputs	20 DIP
Level	4049	Hex Inverting Logic level Down Converters	16 DIP
Shifters	4050	Hex Logic level Down Converters	16 DIP
Flip-Flops	73	Dual J-K Negative-Edge-Triggered Flip-Flops with Clear	14 DIP
	74	Dual D-Type Positive-Edge-Triggered Flip-Flops with Preset and Clear	14 DIP
	76	Dual J-K Negative-Edge-Triggered Flip-Flops with Preset and Clear	16 DIP
·	78	Dual J-K Negative-Edge-Triggered Flip-Flops with Preset, Common Clear	
		and Common Clock	14 DIP
	107	Dual J-K Negative-Edge-Triggered Flip-Flops with Clear	14 DIP
	109	Dual J-K Positive-Edge-Triggered Flip-Flops with Preset and Clear	16 DIP

## Functional Selection Guide (continued)

Function	Part Number KS54/74AHCT KS54/74HCTLS	Description	Package
	112	Dual J-K Negative-Edge-Triggered Flip-Flops with Preset and Clear	16 DIP
	173	4-Bit D-Type Registers with 3-State Outputs	16 DIP
	174	Hex D-Type Flip-Flops with Clear	16 DIP
	175	Quad D-Type Flip-Flops with Clear	16 DIP
	273	Octal D-Type Flip-Flops with Clear	20 DIP
	374	Octal D-Type Flip-Flops with 3-State Outputs	20 DIP
	377	Octal D-Type Flip-Flops with Clock Enable	20 DIP
	399	Quad 2-Port Registers	16 DIP
	534	Octal D-Type Flip-Flops with 3-State	20 DIP
	564	Octal D-Type Flip-Flops with 3-State	20 DIP
•	574	Octal D-Type Flip-Flops with 3-State	20 DIP
	670	4-By-4-Register Files with 3-State Outputs	16 DIP
	794	Octal Register with Readback	20 DIP
	821	10 Bit BUS Interface Registers with 3-State Outputs	24 DIP
:	822	10 Bit BUS Interface Registers with 3-State Outputs	24 DIP
	823	9-Bit BUS Interface Registers with 3-State Outputs	24 DIP
,	824	9-Bit BUS Interface Registers with 3-State Outputs	24 DIP
	825	8-Bit BUS Interface Registers with 3-State Outputs	24 DIP
	826	8-Bit BUS Interface Registers with 3-State Outputs	24 DIP
	75	Quad Bistable Transparent Latches	16° DIP
	77	Quad D-Type Latches	14 DIP
Latches	.259	8-Bit Addressable Latches	16 DIP
	373	Octal D-Type Transparent Latches with 3-State Outputs	20 DIP
	533	Octal D-Type Transparent Latches with 3-State Outputs	20 DIP
	563	Octal D-Type Transparent Latches with 3-State Outputs	20 DIP
	573	Octal D-Type Transparent Latches with 3-State Outputs	20 DIP
	793	Octal D-Type Transparent Latches with Readback	20 DIP
	841	10-Bit Bus Interface D-Type latches with 3-State Outputs	24 DIP
	842	10-Bit Bus Interface D-Type latches with 3-State Outputs	24 DIP
	843	9-Bit Bus Interface D-Type latches with 3-State Outputs	24 DIP
	844	9-Bit Bus Interface D-Type latches with 3-State Outputs	24 DIP
	845	8-Bit Bus Interface D-Type latches with 3-State Outputs	24 DIP
	846	8-Bit Bus Interface D-Type latches with 3-State Outputs	24 DIP
Multiplexers	151	1 of 8 Data Selectors/Multiplexers	16 DIP
	153	Dual 1 of 4 Data Selectors/Multiplexers	16 DIP
	157	Quad 2-Line to 1-Line Data Selectors/Multiplexers	16 DIP
	158	Quad 2-Line to 1-Line Data Selectors/Multiplexers	16 DIP
	251	1-of-4 Data Selectors/Multiplexers with 3-State Outputs	16 DIP
	253	Dual 1-of-4 Data Selectors/Multiplexers with 3-State Outputs	16 DIP
	257	Quad 2-Line to 1-Line Data Selectors/Multiplexers with 3-State Outputs	16 DIP
	258	Quad 2-Line to 1-Line Data Selectors/Multiplexers with 3-State Outputs	16 DIP
	352	Dual 1-of-4 Data Selectors/Multiplexers	16 DIP
,	353	1-of-4 Data Selectors/Multiplexers with 3-State Outputs	16 DIP
Shift	164	8-Bit Serial-In/Parallel-Out Sift Registers	14 DIP
Registers	165	8-Bit Parallel-IN/Serial-Out Shift Registers	16 DIP
	166	8-Bit Parallel-IN/Serial-Out Shift Registers	16 DIP
	194	4-Bit Bidirectional Universal Shift Registers	16 DIP
	195	4-Bit Bidirectional Universal Shift Registers	16 DIP
	299	8-Bit Universal Shift/Storage Registers with 3-State Outputs	20 DIP



## Functional Selection Gude (continued)

Function	Part Number KS54/74AHCT KS54/74HCTLS	Description	Package
Gates and	595	8-Bit Shift Registers with Output Latches	16 DIP
	596	8-Bit Shift Registers with Output Latches	16 DIP
	597	8-Bit Shift Registers with Input Latches	16 DIP
Transceivers/	242	Quad Bus Transceivers with 3-State Outputs	14 DIP
	243	Quad Bus Transceivers with 3-State Outputs	14 DIP
	245	Ouad Bus Transceivers with 3-State Outputs	20 DIP
	640	Ouad Bus Transceivers with 3-State Outputs	20 DIP
	643	Ouad Bus Transceivers with 3-State Outputs	20 DIP
	645	Ouad Bus Transceivers with 3-State Outputs	20 DIP
	646	Octal 3-State Bus Transceivers with Registers	24 DIP
	648	Octal 3-State Bus Transceivers with Registers	24 DIP
	651	Octal 3-State Bus Transceivers with Registers	24 DIP
	652	Octal 3-State Bus Transceivers with Registers	24 DIP 24 DIP
	658	Octal Bus Transceivers with Parity	24 DIP
	659 664	Octal Bus Transceivers with Parity	24 DIP
	665	Octal Bus Transceivers with Parity Octal Bus Transceivers with Parity	24 DIP
Counters	160	Synchronous 4-Bit Decade Counters	16 DIP
	161	Synchronous 4-Bit Binary Counters	16 DIP
	162	Synchronous 4-Bit Decade Counters	16 DIP
	163	Synchronous 4-Bit Binary Counters	16 DIP
	168	Synchronous 4-Bit Up/Down Decade Counters	16 DIP
	169	Synchronous 4-Bit Up/Down Binary Counters	16 DIP
	190 191	Presettable Synchronous BCD Decade Up/Down Counter	16 DIP 16 DIP
	192	Synchronous 4-Bit Up/Down Binary Counters Synchronous 4-Bit Up/Down Binary Counters	16 DIP
	193	Synchronous 4-Bit Up/Down Binary Counters with Dual Clock	16 DIP
	390	Dual 4-Bit Decade Counters	16 DIP
	393	Dual 4-Bit Binary Counters	16 DIP
	590	8-Bit Binary Counters with 3-State Output Register	16 DIP
	591	8-Bit Binary Counters with 3-State Output Register	16 DIP
	592	8-Bit Binary Counters with Input Register	16 DIP
	593	8-Bit Binary Counters with Bidirectional Input Register/Counter Output	20 DIP
Decocers	42	BCD-to-Decimal Decoder	16 DIP
Encoders	138	3-Line to 8-Line Decoders/Demultiplexers	16 DIP
Liloddeid	139	Dual 1-of-4 Decoders/Demultiplexers	16 DIP
	148	8-Line to 3-Line Priority Encoders	16 DIP
	154	4-Line to 16-Line Decoders/Demultiplexers	24 DIP
	155	Dual 2-to-4 Line Decoders/Demultiplexers	16 DIP
	238	3-Line to 8-Line Decoders/Demultiplexers	16 DIP
	239	Dual 1-of-4 Decoders/Demultiplexers	16 DIP
Multivibrators	121	Monostable Multivibrators with Schmit-Trigger Inputs	14 DIP
Maniviolators	123	Dual Retriggerable Monostable Multivibrators	16 DIP
	423	Dual Retriggerable Monostable Multivibrators	16 DIP
Arithmetic	181	4-Bit Arithmetic Logic Unit	24 DIP
Circuits	182	Look-Ahead Carry Generator	16 DIP
OiiCuito	183	Dual High Speed Adder	14 DIP
	280	9-Bit Parity Generators/Checkers	14 DIP



## PRODUCT GUIDE

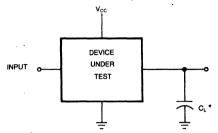
## Functional Selection Guide (contnued)

Function	Pant Namber KS54/74AHCT KS54/74HCTLS	Description -	Package
	518	8-Bit Identity Comparators	20 DIP
	519	8-Bit Identity Comparators	20 DIP
,	520	8-Bit Identity Comparators	20 DIP
	521	8-Bit Identity Comparators	20 DIP
	522	8-Bit Identity Comparators	20 DIP
	679	12-Bit Address Comparators	20 DIP
	680	12-Bit Address Comparators	20 DIP
	682	8-Bit Magnitude Comparators	20 DIP
	684	8-Bit Magnitude Comparators	20 DIP
	686	8-Bit Magnitude Comparators	20 DIP
	688	8-Bit Magnitude Comparators	20 DIP
	689	8-Bit Identity Comparators with Open-Drain Outputs	20 DIP

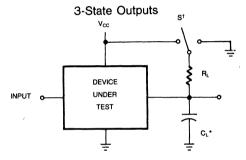


## **AC SWITCHING TEST CIRCUITS**

#### **Totem-Pole Outputs**

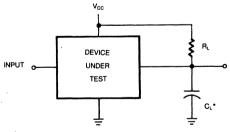


\*C<sub>L</sub> includes load and test jig capacitance



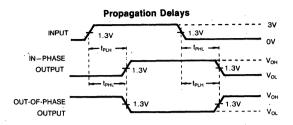
 $^{\star}C_L$  includes load and test jig capacitance  $S^{\dagger}=V_{CC}$  for  $t_{PZL}$  and  $t_{PLZ}$  measurements S=GND for  $t_{PZH}$  and  $t_{PHZ}$  measurements.

#### Open-Drain Outputs

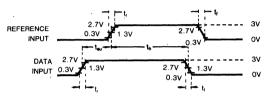


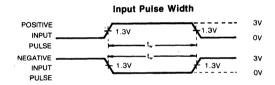
\*C<sub>L</sub> includes load and test jig capacitance

#### **TIMING WAVEFORMS**

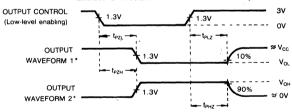


#### Setup & Hold Times, Input Rise & Fall Times





#### **Enable & Disable Time for 3-State Outputs**



- \* Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. This waveform is applicable to both 3-state and open-drain outputs.
- \* Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

#### **DEFINITIONS OF TERMS & SYMBOLS**

#### **FUNCTION TABLE SYMBOLS**

- H = Steady state high level
- L = Steady state low level
- ↑ = Transition from low to high level
- ↓ = Transition from high to low level
- X = Don't care (high, low states or transitions)
- Z = High-impedance state of a 3-state output
- a..h = The level of steady-state inputs at inputs A thru H, respectively
- Q<sub>0</sub> = Level of Q before the indicated steady-state input conditions were established
- $\overline{Q}_0$  = Complement of  $Q_0$  or level of  $\overline{Q}$  before the indicated steady-state conditions were established
- Q<sub>n</sub> = Level of Q before the most recent active transition indicated by \(^1\) or \(^1\)
- $\Pi$  = One high-level pulse
- ☐ ☐ = One low-level pulse

TOGGLE = each output changes to the complement of its previous level on each active transition indicated by  $\uparrow$  or  $\downarrow$  If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with  $\uparrow$  and/or  $\downarrow$ , this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as level (H, L,  $Q_0$ , or  $\bar{Q}_0$ ), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output. (If the output is shown as pulse,  $\prod$  or  $\prod$ , the pulse follows the indicated input transition and persists for an interval dependent on the circuit)

#### **DC Characteristics Terms**

#### VIH High-Level input voltage

An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables. A minimum is specified that is the least-positive value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.

#### V<sub>IL</sub> Low-Level input voltage

An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables. A maximum is specified that is the most-postive value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

#### V<sub>OH</sub> High-Level output voltage

The voltage at an output terminal with input conditions applied that, according to product specification, will establish a high level at the output.

#### Vol Low-Level output voltage

The voltage at an output terminal with input conditions applied that, according to product specification, will establish a low level at the output.

#### V<sub>T+</sub> Positive-Going threshold level

The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage,  $V_{T-}$ .



#### V<sub>T</sub>\_ Negative-Going threshold level

The voltage at a transition-operated input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage,  $V_{T+}$ .

#### Io Output Current

The current into\* an output with input conditions applied that, according to the product specification, will establish a high or a low level at the output.

#### I<sub>IN</sub> Input Curent

The current into\* an input when a high or a low level voltage is applied to that input.

#### Ioz Off-State (high-impedance-state) output current (of a three-state output)

The current flowing into \* an output having three-state capability with input conditions established that, according to the product specification, will establish the high-impedance state at the output level voltage applied to the output.

This parameter is measured with other input conditions established that would cause the output to be at a low-voltage level (if it were enabled) when the externally applied voltage is high; or high-voltage level when the externally applied voltage is low.

#### I<sub>CC</sub> Supply current

The current into\* the V<sub>CC</sub> supply terminal of an integrated circuit.

#### **AC CHARACTERISTICS TERMS**

#### t<sub>r</sub> Rise time

The time interval between two reference points (10% and 90% unless otherwise specified) on a waveform that is changing from the defined low level to the high level.

#### t<sub>f</sub> Fall time

The time interval between two reference points (90% and 10% unless otherwise specified) on a waveform that is changing from the defined high level to the defined low level.

#### f<sub>max</sub> Maximum clock frequency

The highest rate at which the cock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of a logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification.

#### t<sub>PLH</sub> Propagation delay time, low-to-high-level output

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.

#### tрнь Propagation delay time, high-to-low-level output

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.

#### t<sub>PZH</sub> Enable time (of a three-state output) to high level

The time interval between the specified reference points on the input and output voltage waveforms with the threestate outputs changing from a high-impedance (off) state to the defined high level.

#### tpzL Enable time (of a three-state output) to low level

The time interval between the specified reference points on the input and output voltage waveforms with the threestate outputs changing from a high-impedance (off) state to the defined low level.



<sup>\*</sup>Current out of a terminal is given as negative value.

#### t<sub>PHZ</sub> Disable time (of a three-state output) from high level

The time interval between the specified reference points on the input and output voltage waveforms with the three-state outputs changing from the defined high level to high-impedance (off) state.

#### tpl7 Disable time (of a three-state output) from low level

The time interval between the specified reference points on the input and output voltage waveforms with the threestate outputs changing from the defined high level to high-impedance (off) state.

#### tw Pulse width

The time interval between specified reference points on the leading and trailing edges of the pulse waveform.

#### t<sub>su</sub> Setup time

The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal.

- NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.
  - The setup time may have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is guaranteed.

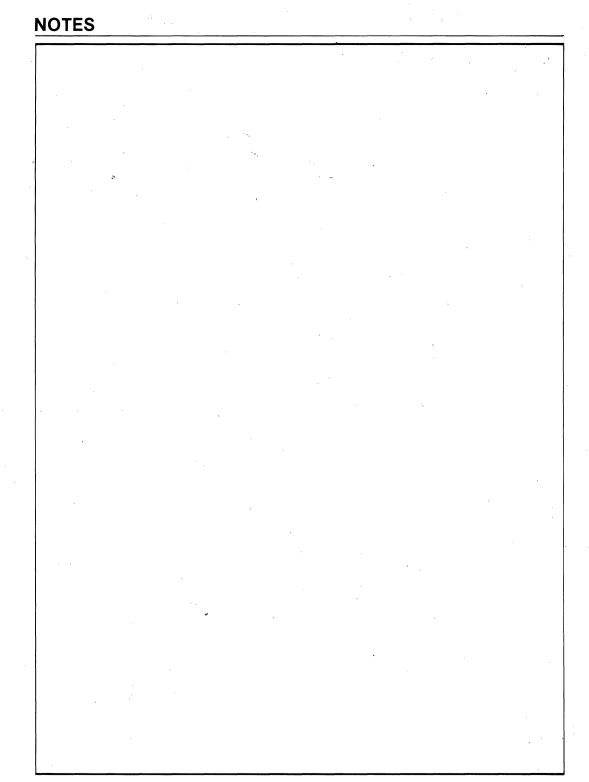
#### th Hold time

The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.

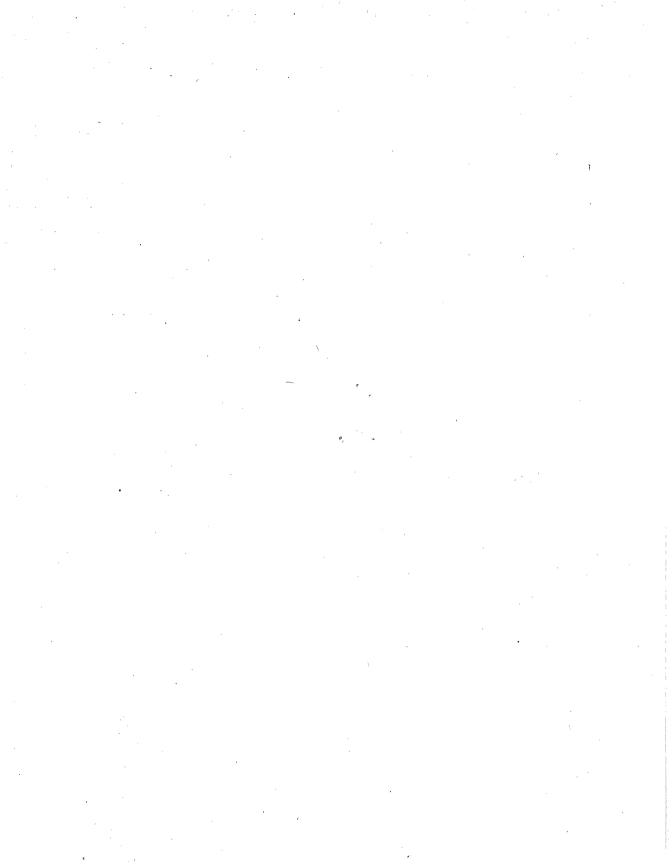
- NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.
  - The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is guaranteed.

#### C<sub>PD</sub> Power dissipation capacitance

Used to determine the no-load dynamic power dissipation per logic function (see individual circuit pages):  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .



# TECHNICAL OVERVIEW 3



#### INTRODUCTION

The 54/74AHCT Advanced High-Speed CMOS and the 54/74HCTLS High-Speed CMOS logic families were designed to offer the most desirable features of their CMOS and bipolar predecessors. They have the low power dissipation, superior noise immunity, wide voltage and temperature ranges and the very low input currents of the other high-speed CMOS logic families, in addition to the high speed and drive capability of LS and ALS bipolar logic.

The AHCT family is an exact equivalent of the bipolar ALS and can readily replace ALS in existing applications to reduce power dissipation. In many applications, AHCT parts can also be used as replacements for FAST<sup>TM</sup> and S (Schottky).

The HCTLS parts, on the other hand, meet and exceed all of industry-standard LS and HCT specifications, and can be used as replacements to these to lower the power dissipation and improve performance. Figure 1 shows how AHCT and HCTLS families rank with the other bipolar technologies in terms of speed and power dissipation.

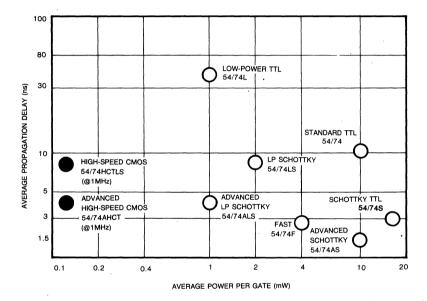


FIGURE 1. Power dissipation vs gate dely characteristics for a two-input NAND gate (74XXX00) implemented in various bipolar and CMOS technologies

Both families feature TTL input voltage levels which enable them to interface with all TTL, NMOS or CMOS outputs without any external components. All AHCT and HCTLS parts are fully characterized and specified over the 4.5 to 5.5V voltage range, and the industrial (-4Q to 85°C) and military (-55 to 125°C) temperature ranges. This is a significant improvement over the older biploar logic families, where, for example LS would specify DC specs over 4.75V to 5.25V and AC specs only at 5V and room temperature. (ALS is specified over 4.5 to 5.5V and 0 to 70°C). A comparison of the key characteristics for an octal buffer illustrates these improvements clearly in Figure 2. The DC characteristics common to all AHCT and HCTLS parts are listed in Figure 3.

FAST is a trademark of Fairchild camera and Instrument





		TTL			SAMSUN	G CMOS	OTHER	CMOS
	,	74LS244	74ALS244	74F244	74HCTLS244	74AHCT244	74HC244	74HCT244
Operating Voltage Range (Commercial)		4.75V to 5.25V	4.5V to 5.5V	4.75V to 5.25V	4.5V to 5.5V	4.5V to 5.5V	2V to 6 V	4.5V to 5.5V
Operating Temperature Range (Commercial)		0°C to 70°C	0°C to 70°C	0°C to 70°C	-40°C to +85°C	-40°C to +85°C	-40°C to +85°C	-40°C to +85°C
Maximum Propagation Delay (C <sub>L</sub> = 50 pF)		18 ns (V <sub>CC</sub> = 5V, T <sub>a</sub> = 25°C)	10 ns (Over Operating Conditions)	6.5 ns (Over Operating Conditions)	18 ns $(V_{CC} = 5V, T_a = 25^{\circ}C)$	. 10 ns (Over Operating Conditions)	20 ns $(V_{CC} = 5V, T_a = 25^{\circ}C)$	18 ns $(V_{CC} = 5V, T_a = 25^{\circ}C)$
Maximum Quiescent Current		54 mA	27 mA	90 mA	0.08 mA	0.08 mA	0.08 mA	0.08 mA
Typical Power Dissipation	Static	120 mW	70 mW	260 mW	0.004 mW	0.004 mW	0.004 mW	0.004 mW
	At 100 kHz (All inputs toggling)	120 mW	70 mW	260 mW	0.6 mW	0.6 mW	1.0 mW	1.8 mW
Output Drive Currents	Іон	-3  mA (V <sub>OH</sub> = 2.4V) -15  mA (V <sub>OH</sub> = 2.0V)	$-3 \text{ mA}$ $(V_{OH} = 2.4V)$ $-15 \text{ mA}$ $(V_{OH} = 2.0V)$	- 15 mA (V <sub>OH</sub> 2.0V)	-6 mA (V <sub>OH</sub> = 3.84V)	-6  mA (V <sub>OH</sub> = 3.84V)	-6 mA (V <sub>OH</sub> = 3.84V)	-6 mA (V <sub>OH</sub> = 3.84V)
	loL	12 mA $(V_{OL} = 0.4V)$ 24 mA $(V_{OL} = 0.5V)$	12 mA (V <sub>OL</sub> = 0.4V) 24 mA (V <sub>OL</sub> = 0.5V)	64 mA (V <sub>OL</sub> = 0.55V)	12 mA (V <sub>OL</sub> = 0.4V) 24 mA (V <sub>OL</sub> = 0.5V)	12 mA $(V_{OL} = 0.4V)$ 24 mA $(V_{OL} = 0.5V)$	6 mA (V <sub>OL</sub> = 0.33V)	6 mA (V <sub>OL</sub> = 0.33V)
Input Threshold Voltages	V <sub>IL</sub>	0.8V	0.8V	0.8V	0.8V	0.8V	0.9V (V <sub>CC</sub> = 4.5V)	0.8V
	V <sub>IH</sub>	2.0V	2.0V	2.0V	2.0V	2.0V	3.15V (V <sub>CC</sub> = 4.5V)	2.0V
Input Currents	lı∟	-0.2  mA (V <sub>I</sub> = 0.4V)	-0.1  mA (V <sub>I</sub> = 0.4V)	-1.6  mA (V <sub>I</sub> = 0.5V)	-1.0 μA	-1.0 μA	-1.0 μΑ	-1.0 μΑ
	I <sub>IH</sub>	20 μA (V <sub>I</sub> = 2.7V)	20 μA (V <sub>I</sub> = 2.7V)	20 μA (V <sub>I</sub> = 2.7V)	. , 1.0 μΑ	1.0 μΑ	1.0 μΑ	1.0 μΑ

FIGURE 2. Key performance characteristics for 74XXXX244 octal buffer

## **TECHNICAL OVERVIEW**

The Samsung CMOS logic families include a comprehensive set of buffers, registers, latches and transceivers that are offered in 8, 9 and 10-bit versions. A wide variety of gates, flip-flops, multiplexers, shift registers, encoder/decoders, schmitt triggers and multivibrators complete the family of 157 part types. Each function is available in both AHCT and HCTLS version.

Characteristic	: Symbol	Conditions		T <sub>a</sub> = 25°C		Commercial T <sub>a</sub> = -40°C to +85°C	Military T <sub>a</sub> = -55°C to +125°C	Unit
				Тур		Guaranteed Li	mits	
Minimum High-Level Input Voltage	V <sub>IH</sub>				2.0	2.0	2.0	V
Minimum Low-Level Input Voltage	V <sub>IL</sub>				0.8	0.8	0.8	V
Minimum	V <sub>ОН</sub>	P.	CMOS loads I <sub>OH</sub> =-20µA	Vcc	V <sub>CC</sub> -0.1	V <sub>CC</sub> -0.1	V <sub>CC</sub> -0.1	V
High-Level Output Voltage			Standard Outputs I <sub>OH</sub> =-4 mA	4.2	3.98	3.84	3.7	
,			Bus-Driver Outputs I <sub>OH</sub> =-6 mA	4.2	3.98	3.84	3.7	
		$V_{IN}$ = $V_{IH}$ or $V_{IL}$	CMOS loads I <sub>OL</sub> =20 μA	0.1	0.1	0.1	0.1	V
Minimum Low-Level Output Voltage	V <sub>OL</sub>		Standard Outputs I <sub>OL</sub> =4 mA I <sub>OL</sub> =8 mA	0.2 0.3	0.26 0.39	0.33 0.5	0.4	
			Bus-Driver Outputs I <sub>OL</sub> =12 mA I <sub>OL</sub> =24 mA	0.2 0.3	0.26 0.39	0.33 0.5	0.4	v
Maximum Input Leakage Current	l <sub>l</sub>	V <sub>CC</sub> =Max, V <sub>IN</sub> =V <sub>CC</sub> or GND			±0.1	±1.0	1.0	, μA
Maximum 3-State Leakage Current	loz	V <sub>CC</sub> =Max, Enable=V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND			±0.5	±5.0	±10.0	μА
		V <sub>CC</sub> =Max V <sub>IN</sub> =V <sub>CC</sub> or GND	SSI Circuits		2.0	20.0	40.0	μΑ
Maximum Quiescent	Icc		Dual and Quad Flip-Flops & Latches		4.0	40.0	80.0	
Supply Current		All Outputs Open	MSI Circuits & Circuits with High-Current Outputs		8.0	80.0	160.0	

FIGURE 3. DC characteristics of the 54/74AHCT and 54/74 HCTLS Families ( $V_{CC} = 5.0V \pm 10\%$ )

#### PROCESS TECHNOLOGY

The high performance of the AHCT and HCTLS is a result of a unique self-aligned metal-gate CMOS process technology that features 1.2 $\mu$ m effective gate lengths and double metallization. The following table compares the general characteristics of this process with other existing CMOS and bipolar technologies used for logic circuits:

	SAMSUNG CMOS	INDUSTRY CMOS (HC & HCT)	INDUSTRY ALS
Number of Masking Steps	8	12-14	13
Number of Metal Layers	2	1	2
Minimum Feature Size (drawn)	2 μm	3-4 μm	4 μm
Interconnections	All Metal	Poly & Metal	All Metal
Relative Die Size	1X	2.5-5X	1.5-2X
Manufacturing Equipment	Standard	Standard	Standard

Samsung's CMOS process was designed from the ground up to be a scaled two-layer metal CMOS process (see *Figure 4* for a cross section). The goal was to make the process as simple as possible, and be able to readily control gate length and gate dielectric thickness. The process uses 8 masking steps. Other semiconductor manufactures, in trying to go to two-layer metal short-channel processes have generally embellished pre-existing silicon-gate processes and have wound up with 12-14 masking steps. More masking steps, of course, make wafers more costly, but most importantly, reduce yield because of more chances for random defects.

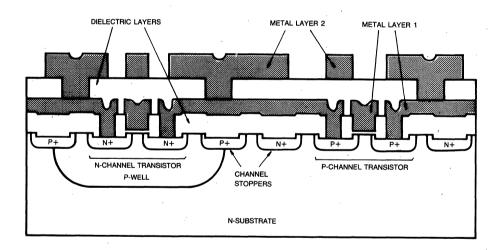
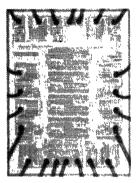


FIGURE 4. Samsung CMOS process cross section for an inverter stage

The Samsung process, with the short 2  $\mu$ m channel lengths (1.2  $\mu$ m effective), yields gate delays as fast as those of the bipolar LS and ALS processes, and the same short channel lengths allow high-current output drivers to occupy a modest silicon area. Generally, the AHCT and HCTLS logic chips are much smaller than their CMOS and bipolar equivalents (see *Figure 5*). In achieving this small size, two-layer metal is as important as having short channels. For example, in the on-chip busing of ground and  $V_{CC}$  to the output drivers, very wide metal lines have to be used that take considerable area. In this case, if these lines are in Metal 2, no extra area is wasted since the circuitry can be placed underneath.

2.57X



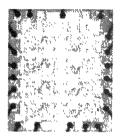
MM74HC240 National Semiconductor

1.42X



74F240 Fairchild

1.57X



SN74ALS240 Texas Instruments

1 X



KS74AHCT240 KS74HCTLS240 Samsung

FIGURE 5. Die size comparison for a 74XXX244 from various technologies.

## INPUT CHARACTERISITICS

The input stage of an AHCT or HCTLS circuit is illustrated in *Figure 6*. It consists of a diode protection network and a CMOS inverter stage that has very high input impedance. The ultra-low input current specified in the data sheets ( $1\mu$ A maximum) is due to the reverse leakage currents of the diodes and is not used for "driving" the CMOS transistors i.e. the inputs are voltage-driven. This makes AHCT and HCTLS inputs very easy to drive and results in a very high fan-in capability.

TTL-compatible input threshold voltages of 0.8V V<sub>IL</sub> and 2.0V V<sub>IH</sub> are accomplished by properly sizing the p- and n-channel transistors of the CMOS inverter stage. The actual logic transition takes place mid-way between these values, at 1.4V, and is very sharp compared to TTL logic due to the very high gain of the first inverter stage. This is illustrated in *Figure 7* for a two-input NAND gate. Note that the input threshold for CMOS is much more stable with temperature than that for LS.

While the AHCT and HCTLS parts are recommended as direct replacements for ALS and LS, one needs to pay attention to not leaving any inputs floating, i.e. unconnected. Since the inputs have very high impedance, they can easily pick up external noise which can result in random switching of the device and high power consumption. Therefore, all unused inputs must be terminated to either  $V_{CC}$  or ground.



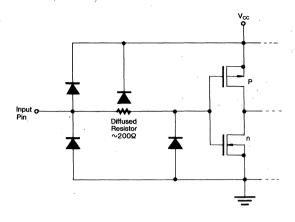


FIGURE 6. The input circuit of AHCT and HCTLS parts.

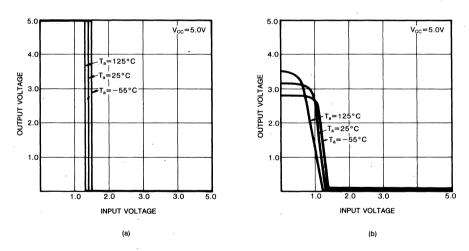


FIGURE 7. Input-Output transfer characteristics for (a) AHCT/HCTLS00, (b) LS00.

#### **OUTPUT CHARACTERISTICS**

A typical output stage of an AHCT or HCTLS part consists of a complementary pair of transistors and a diode protection network (see *Figure 8*). Unlike the bipolar outputs, the voltage swing is rail-to-rail, which is responsible for the improved noise margine of AHCT/HCTLS systems. The drive capability of these outputs is similar to the bipolar parts, i.e. 24mA or 8mA  $|_{OL}$  (at  $0.5\text{V V}_{OL}$ ) for bus-driver and standard outputs, respectively. This means that AHCT and HCTLS parts can drive as many loads or as large bus capacitances as their ALS and LS counterparts. *Figure 9* shows a comparison of the output drive capabilities of AHCT/HCTLS and LS/ALS outputs. *Figure 10* illustrates the variations of  $|_{OL}$  and  $|_{OH}$  with supply voltage and temperature for a standard output ('00) and a bus driver ('244).

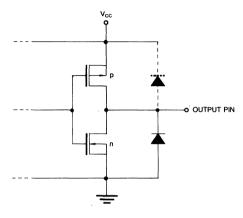
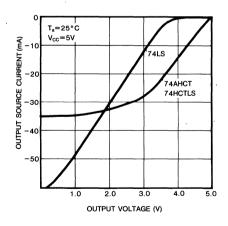


FIGURE 8. A typical output circuit of an AHCT or HCTLS part.

The upper diode is parasitic and embedded in the p-channel transistor.



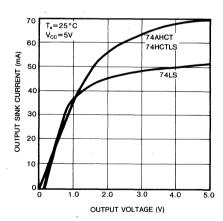
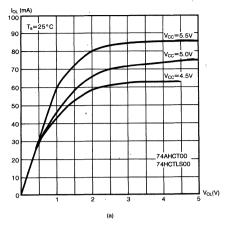
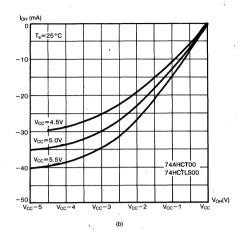
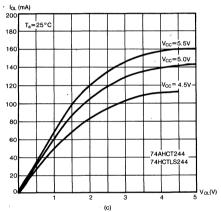


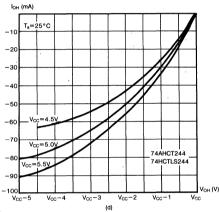
FIGURE 9. Comparison of standard AHCT/HCTLS and standard LS output (a) Source, and (b) sink currents.

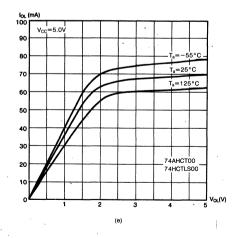
## **TECHNICAL OVERVIEW**

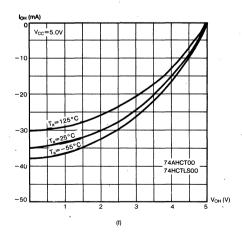


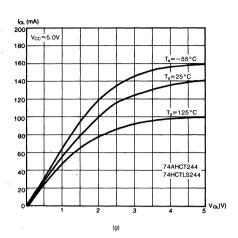












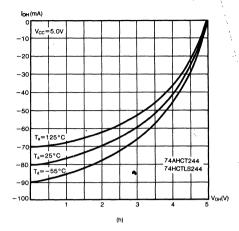


FIGURE 10. Output current variations with supply voltage and temperature for standard [(a), (b), (e) (f)] and bus driver [(c), (d), (g), (h)] outputs.

#### **NOISE IMMUNITY & NOISE MARGINS**

The term "noise" in the context of digital circuits and systems means unwanted transient variations of voltages and currents at logic nodes. Typically noise is transferred to logic nodes or interconnecting lines by unwanted capacitive or inductive coupling, as illustrated in *Figure 11*.

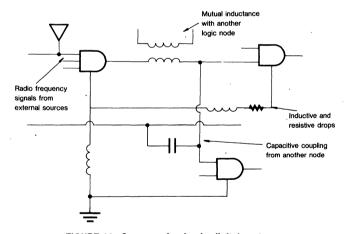
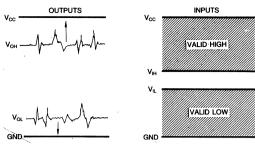


FIGURE 11. Sources of noise in digital systems.

Noise becomes a particularly critical issue in high-speed systems where fast voltage transitions accentuate these parasitic capacitances and inductances. Also, higher speeds allow the device to respond more quickly to noise transients. Therefore, special board layout and decoupling techniques have to be employed to confine noise to an "acceptable range". Obviously, the wider this range, the easier it is to design a clean system. This range is dictated by the input and output characteristics of the ICs in the system, as illustrated in Figure 12, and is measured in terms of "noise margins".

## **TECHNICAL OVERVIEW**

The output signals should be as close to the supply rails as possible. This allows more margin for noise to distort the output signal without violating the logic level requirements of the driven inputs.



The voltage range for each logic level should be as wide as possible. This relaxes the requirements for the cleanliness of incoming signals.

FIGURE 12. Requirements for good noise immunity.

Noise margins specify the maximum amplitude noise pulse that will not change the state of a driven stage, assuming the driving stage presents a worst-case logic level to the driven stage. Specifically, the high-level and the low-level noise margins (NM<sub>H</sub> and NM<sub>L</sub>) are defined as:

$$NM_H = V_{OH} - V_{IH}$$
,  
 $NM_L = V_{IL} - V_{OL}$ 

where the voltage values are the guaranteed worst-case extremes for each case. Figure 13 shows the noise margins for several different interfaces.

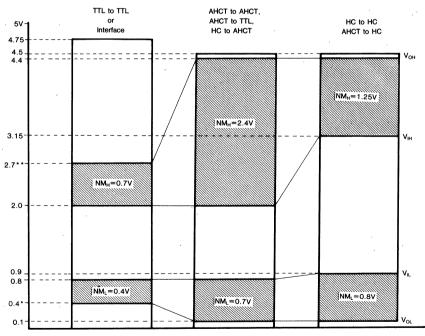


FIGURE 13. Noise margins for various interfaces. Noise margins for HCTLS are the same as those for AHCT.

- \* When an AHCT output drives TTL loads the V<sub>OH</sub> level will be dependent on how many loads are driven. For example if an AHCT244 drives 60LS loads, the V<sub>OH</sub> will rise to 0.4V
- \*\* For some, TTL parts, VOH is 2.4V; instead of 2.7V

## TECHNICAL OVERVIEW

It is immediately obvious that the TTL-to-TTL interfaces have the poorest noise immunity and those driven by CMOS have the best. This is due to the rail-to-rail voltage swings of CMOS outputs.

Note the HC logic has almost symmetrical noise margins while AHCT (or HCTLS) has a very large noise margin for high level and a smaller low-level one. This is due to the fact that AHCT (or HCTLS) inputs are designed for direct interface with TTL and NMOS outputs as well as other CMOS. Notice, however, that the low-level noise margin (NM<sub>L</sub>) for AHCT is only 0.1V less than that for HC, which means that it provides nearly as much immunity to ground noise. In addition, since AHCT drive capability is two to four times better than HC, it is less susceptible to noise currents coupled to its outputs. That is, lower stray voltages are induced for a given amount of current coupling than for HC:

#### **ESD PROTECTION**

Historically, MOS devices have always been considered to be more susceptible to damages due to electrostatic discharges (ESD), which can occur during handling and assembly procedures. However, the new protection circuitry, design, and special processing used for AHCT and HCTLS have improved the ESD immunity for these devices where it is now much better than that of bipolar logic.

Figure 6 and 8 show the input and output ESD protection circuitry employed. All AHCT and HCTLS pins are protected to ESD levels typically greater than ±2kV, the tests are conducted using the "human-body" model that is shown in Figure 14.

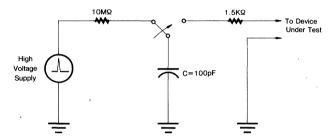


FIGURE 14. Test circuit used to measure ESD damage in AHCT and HCTLS circuits.

#### LATCHUP CHARACTERISTICS

SCR iatchup is an undesirable parasitic phenomenon which is inherent in circuits fabricated using bulk CMOS technology. A parasitic four-layer (P-N-P-N) SCR structure that appears between V<sub>CC</sub> and ground can be triggered when voltages greater than V<sub>CC</sub> or less than ground are applied to inputs or outputs. When this happens, V<sub>CC</sub> gets effectively shorted to ground, and the only way to get the device off the latchup mode is to shut off the power supply. If large currents are allowed to flow through the chip, it may be destroyed. Samsung CMOS logic parts have been designed and processed to virtually eliminate this possibility in real-life situations where voltages out of the supply range many appear at the input or output pins (overshoots, undershoots, power-up & power-down situations).

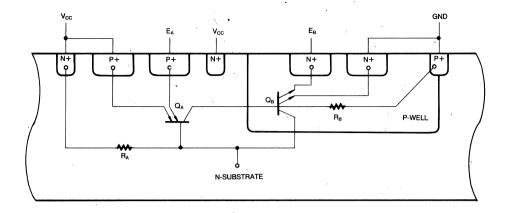


FIGURE 15. Simplified cross section of a CMOS inverter

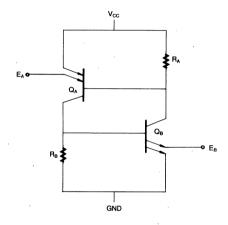


FIGURE 16. CMOS SCR structure

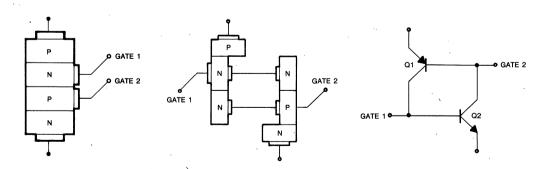


FIGURE 17. Simplified four layer SCR structure

The parasitic SCR structure in a CMOS inverter cross section is illustrated in *Figure 15*, where vertical and lateral NPN and PNP transistors are formed back-to-back by the N and P diffusions.  $R_A$  and  $R_B$  are the P-well and the N-substrate power supply connections. *Figure 16* is a schematic representation of this parasitic structure that looks like a cross-coupled transistor model of an SCR (*Figure 17*). The exceptions are the  $R_A$  and  $R_B$  resistors and the fact that the real SCR is triggered at the gates, while the CMOS parasitic SCR is triggered at its emitters. This happens when either the  $E_A$  is raised above  $V_{CC}$  enough to turn on  $Q_A$ , or  $E_B$  is lowered below ground enough to turn on  $Q_B$ . When  $E_A$  is brought above  $V_{CC}$ , current is injected from the emitter of  $Q_A$  and is swept to its collector. This current, in turn, will increase the voltage at the  $Q_B$  gate and once it is above 0.7V,  $Q_B$  will turn on and feed current from its collector back into  $R_A$  and into  $Q_A$ . When 0.7V drop appears across  $R_A$ ,  $Q_A$  will turn on even more.

If the two transistors have enough gain and enough current is provided by the supply to sustain the SCR, it will turn on and remain on even after E<sub>A</sub> and E<sub>B</sub> are returned to the rail voltages. Notice that low resistor values effectively reduce the gain of the transistors by stealing current away from their bases. Therefore, transistors should actually have much higher gains in order to have an overall SCR loop gain greater than one and enable SCR to trigger.

Samsung CMOS logic parts are designed and processed to have very low R<sub>A</sub>, R<sub>B</sub> values and low gains for the parasitic transistors. In addition, large diodes exist between each signal pin and the supply rails to shunt out voltages above V<sub>CC</sub> and below ground. In fact, traditionally, one refers to the current that flows through these diodes as the element that triggers latchup, i.e. we talk of "latchup trigger currents", not voltages.

Measured on a static basis, i.e. by applying DC voltages above V<sub>CC</sub> and below ground, Samsung parts can withstand currents typically well above 200mA-even under the worst-case conditions of 7V V<sub>CC</sub> and +125°C operation. *Figure 18* illustrates the test set-up used for static latchup tests.

A common occurence of voltages above V<sub>CC</sub> and below ground in systems is overshoots and undershoots that are caused by signal line ringing and power supply transients. In this case, unlike the static operation, only short pulses cause forward-bias diode currents and hence possible latch-up. It turns out, fortunately, that the parasitic SCR has extremely slow response time to transients, i.e. very poor frequency characteristics. *Figure 19* shows the increased peak currents required to latch an AHCT or HCTLS device up when the pulse width is decreased. For pulse widths in the range of several tens of nanoseconds, it is virtually impossible to latch the device up.

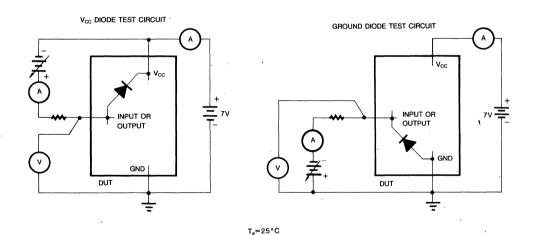


FIGURE 18. Test setup for measuring DC latch-up

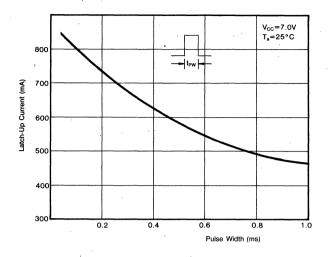


FIGURE 19. Pulsed latch-up characteristics

#### **POWER DISSIPATION**

Low power dissipation is by far the most important advantage of CMOS over any other technology. Particularly in the quiescent state, the AHCT and HCTLS circuits consume up to seven orders of magnitude less power than the equivalent TTL functions. This makes them ideal for battery-operated or ultra-low power systems where the system may be put to "sleep" by shutting off the system clock.

The dynamic power dissipation, however, depends on:

- 1. Cross-over currents of the internal CMOS transistors,
- 2. Internal load capacitances,
- 3. External load capacitances, and
- 4. Input voltage levels.

All of the above add up every time there is a logic transition and dynamic power dissipation is the sum of these contributions averaged at a given operating frequency. A practical formula is developed to calculate the dynamic power dissipation (P<sub>D</sub>) resulting from the first three items: (input voltage transitions are rail-to-rail)

$$P_D = (C_L + C_{PD}) V_{CC}^2 f$$
,

where  $C_L$  is the load capacitance;  $C_{PD}$  is the "internal power dissipation capacitance",  $V_{CC}$  is the supply voltage and f is the operating frequency. The  $C_{PD}$  value, as specified in each data sheet, sums up the contributions of the first two factors (crossover currents and internal load capacitances) as a capacitance value for purposes of this calculation. The equation indicates that the dynamic power dissipation is directly proportional to frequency.

The contribution of the fourth factor listed above, the input voltage levels, can also be significant when AHCT or HCTLS inputs are driven by TTL outputs. Figure 20 shows the typical crossover currents generated at the input inverer stage as the input voltage swings from O to  $V_{CC}$ . This is because both the n-channel and the p-channel transistors turn on partially and provide a low-resistance current path between  $V_{CC}$  and ground when the input voltage is near the threshold voltage of the complementary pair. At 2.7V, which is the worst case  $V_{OH}$  for TTL parts, the  $I_{CC}$  can be as high as 0.5mA per input. This has to be taken into account when calculating the worst-case power dissipation of an AHCT or HCTLS part operating in a TTL environment.

## **TECHNICAL OVERVIEW**

Figure 21 shows the internal power dissipation for an AHCT244 (same for HCTLS244) and compares it with the dynamic power dissipation for LS, ALS and F244. It can be seen that the curves for the bipolar parts are essentially flat for frequencies up to 1 MHz where the quiescent currents mask out the dynamic effects. However, as the frequency goes up, the currents that charge the internal capacitances start adding to the quiescent currents and increase the overall power dissipation. The AHCT244 driven by worst-case TTL voltage levels (all inputs, 50% duty cycle) displays a similar trend but still dissipates an order of magnitude less power than the lowest-power TTL. When CMOS input voltage levels are used, however, the power dissipation is directly proportional to frequency as predicted by the above mentioned formula, and is less than those for the TTL parts, Although the power dissipation becomes comparable to ALS levels at around 10MHz, a crossover does not happen below 50MHz, which is already beyond the maximum clock frequencies of most systems. This behaviour is pretty much the same for all parts in the AHCT and HCTLS families.

In calculating the power dissipation of a system, however, note that only a small percentage of the devices operate at the maximum clock frequency while others operate at a fraction of that. Therefore the average operating frequency tends to be much lower where CMOS has a clear advantage.

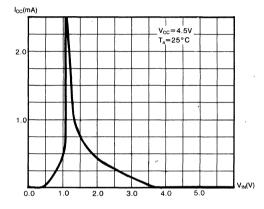


FIGURE 20. Typical crossover current of an AHCT or HCTLS input.

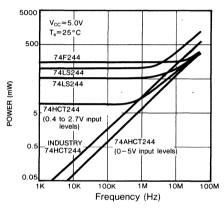


FIGURE 21. Typical dynamic power consumption`
(no-load) of the 74XXX240 octal buffer
with all inputs toggling.

#### **AC CHARACTERISTICS**

All AHCT and HCTLS parts are designed to meet or exceed the ALS and LS propagation delay specifications, respectively. Coupled with the equivalent drive capability, this makes them ideal replacements for the ALS and LS in existing designs. In addition the AC specifications for AHCT and HCTLS parts are improved to reflect more realistic design situations. First of all, unlike LS, the AHCT & HCTLS propagation delays are specified with a 50pF load for all part types and guaranteed over the entire voltage and temperature ranges (5V±10%, -40°C to +85°C). Standard LS propagation delays are specified with a 15pF load and guaranteed only at room temperature and 5V V<sub>CC</sub>. In addition, all bus drivers specify the propagation delays with a 150pF load capacitance to enable the designer to predict a worst-case maximum speed degradation due to capacitive loading.

The effect of the supply voltage variations on propagation delay is illustrated in *Figure 22* for a bus-driver (AHCT244). It can be seen that the parts are functional over a very wide range of voltages and that they slow down as V<sub>CC</sub> goes down. However, propagation delays are specified and guaranteed only over the 4.5 to 5.5V range.

Figure 23 shows the effect of temperature on the propagation delays for the same part. As for all CMOS circuits, AHCT and HCTLS parts slow down as temperature goes up. Typically speeds derate linearly from 25°C at about 0.02 ns/°C. The propagation delay at any temperature (between -55°C and +125°C) can therefore be calculated using the following formula:

 $t_{PD}(T)=t_{PD}(25^{\circ}C)+k_{T}(T-25^{\circ}C)$ 

#### where:

tpp (T)=Propagation delay at the desired T temperature,

tpD (25°C)=Propagation delay at 25°C,

k<sub>T</sub>=Temperature derating factor=0.02 ns/°C

The effect of capacitive loading of the outputs on the propagation delay is illustrated in *Figure 24*: the higher the load capacitance, the slower the propagation delay gets. To determine the maximum limit for propagation delay at any value of capacitive loading up to 500pF, the following equation is used:

 $t_{PD} (C_L) = t_{PD} (50pF) + k_C (C_L - 50pF)$ 

#### where:

tpD (CL)=Maximum propagation delay at the desired CL,

tpD (50pF)=Maximum propagation delay from device data sheet,

k<sub>C</sub>=Maximum multiplicative factor (ns/pF):

- . 0.04 for standard outputs, and
- . 0.02 for bus-drivers.

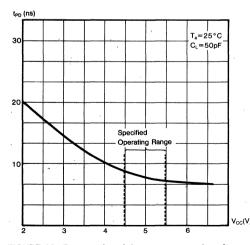


FIGURE 22. Propagation delay versus supply voltage for an AHCT244.

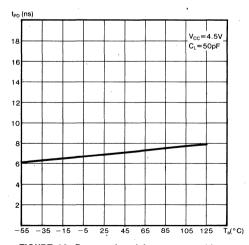
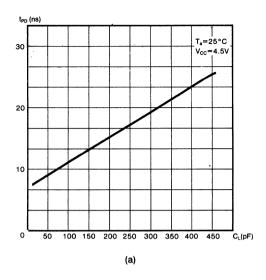


FIGURE 23. Propagation delay versus ambient temperature for an AHCT244.



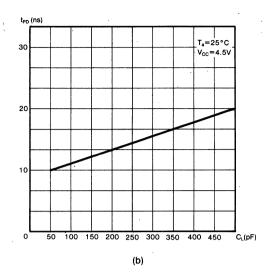


FIGURE 24. Propagation delay versus capacitive load for a (a) standard output (HCTLS00), (b) bus-driver output (HCTLS374)

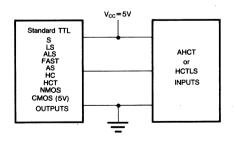
## INTERFACING 54/74AHCT AND 54/74HCTLS WITH OTHER LOGIC FAMILIES AND LOADS

Speed and power, while paramount in the initial choice of a logic family, are not the only basis of decision. Another very important factor is the interface flexibility: the inherent capacity of a family to interface with other types of logic and to drive various loads. The Samsung CMOS logic families have this very attractive feature that they can easily be interfaced to all other kinds of digital logic with minimal or no external components.

AHCT and HCTLS parts can be coupled directly with all other TTL, NMOS and CMOS parts if they operate from the same supply voltage. The list includes Standard TTL, Schottky(S), Low-Power Schottky(LS), Advanced Low-Power Schottky(ALS), Advanced Schottky (AS and FAST); all industry-standard CMOS logic families (HC, HCT, CD4000, 14000); all bipolar, NMOS and CMOS microprocessors, microcontrollers, peripherals and memory circuits (see figure 25). This is due to the TTL-compatible input voltage levels coupled with CMOS (rail-to-rail) output voltage swings.

Interface with ECL logic, however, requires external components as shown in Figure 26.

Methods of interfacing with standard CMOS logic families (4000 and 14000), when supply voltages are different, are illustrated in Figure 27 and 28.



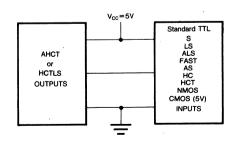


FIGURE 25. Interfacing with TTL, NMOS and other CMOS logic. No extra components are needed.

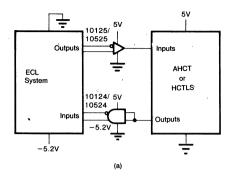
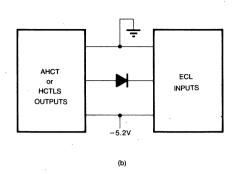
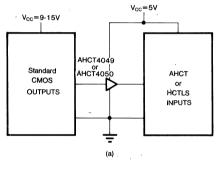
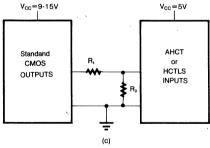


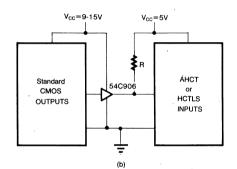
FIGURE 26. (a) General ECL interface



(b) Driving ECL from same power supply.







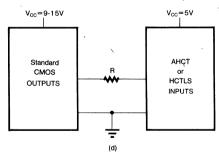


FIGURE 27. Methods of interfacing standard CMOS (4000 and 14000 series) outputs with AHCT and HCTLS inputs when supply voltages are different.

- (a) Using logic down converters,
- (b) Using Open-drain CMOS
- (b) Using resistor divider  $(V_{OH} \cdot R_2/(R_1 + R_2) \le 5V)$
- (d) Using series resistor

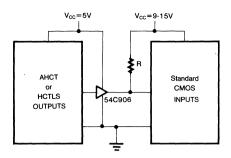


FIGURE 28. Interfacing AHCT and HCTLS outputs with standard CMOS (4000 and 14000) using an open-drain CMOS circuit.

## High Voltage and Industrial Control Interfaces

Interfacing with high voltage industrial control circuitry where 4000 or 14000-type of CMOS logic is used has been described in *Figure 27* and *28*. In rugged industrial and automotive environments, more care may be required to prevent large transients from harming AHCT and HCTLS logic. *Figure 29* shows a typical connection that utilizes external diode clamps for input and output protection. The values of R<sub>1</sub> and R<sub>2</sub> depend on the output voltage of the driving circuit and C depends on the noise level and speed. The values of R<sub>3</sub> and R<sub>4</sub> depend on supply voltage and transistor type.

#### **Driving Relays**

The high-drive of AHCT and HCTLS outputs enable direct interface with relays, but additional isolation is recommended. Clamp diodes can be used to prevent spikes generated by the relay from harming the circuit. For higher current drive, an external transistor may be employed (*Figures 30* (a) and (b)). Alternatively, multiple gates may be connected in parallel to increase the current sinking and sourcing capability.

## **Driving LED's**

Any AHCT or HCTLS output can be used to drive light-emitting diodes (LED's) directly. Figure 31 shows two methods of doing this. The resistor performs the founction of current limiter. The luminous intensity of the LED depends on the amount of forward current.

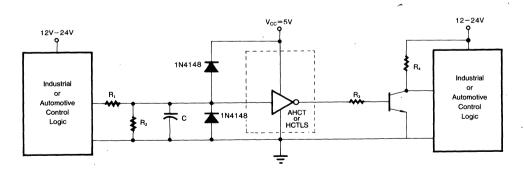


FIGURE 29. Interfacing between AHCT/HCTLS logic and high-voltage industrial and automotive circuitry in rugged environments.

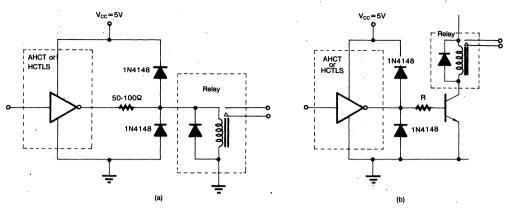


FIGURE 30. Methods of driving relays. (a) Direct and (b) Through a transistor for higher drive  $(R = V_{CC} - 0.7)/I_C/\beta)$ ).

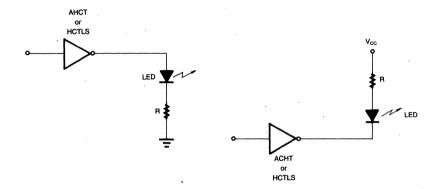


FIGURE 31. Methods of driving LED's

#### **Design Tips**

Although the AHCT and HCTLS families are functionally equivalent to the ALS and LS families, some conditions have to be satisfied in order to be able to simply replace them in existing designs. The AHCT and HCTLS families essentially integrate TTL and CMOS characteristics into one family. Therefore, in general, the do's and don'ts of both families apply to the AHCT and HCTLS.

- Don't leave any AHCT or HCTLS input floating. This is frequency overlooked problem with bipolar devices although it is discouraged by every bipolar manufacturer. CMOS inputs have extremely high input impedance and if left unterminated, can pick up noise that causes excursions through the threshold. The result is random switching of the device and high power consumption which can be excessive, especially if the inputs stay very close to the device threshold. Prolonged exposure to these conditions can damage the device. The thing to do is to simply tie the unused inputs to V<sub>CC</sub> or ground (or they can be tied to nearest operational pin although this may cause more power consumption).
- Don't power up inputs before both V<sub>CC</sub> and ground are connected, and don't plug boards into or out of powered connectors unless input currents are limited to the absolute maximum ratings specified for the device, and are short-lived. Both conditions can forward bias the input and output ESD protection diodes, resulting in excessive diode currents (see *Figure 32*). If these conditions cannot be avoided, one of the following methods should be used to prevent damage to the AHCT/HCTLS circuits:
- Use connectors that apply power before signals.
- Add series resistors at each input to limit currents to the absolute maximum ratings (Figure 33a).
- Add logic to board interfaces that forces all outputs to either ground or high-impedance state when they are connected
  to unpowered devices (Figure 33b).
- Add logic to board inputs to prevent direct interface with unpowered HCTLS inputs (Figure 33c). Circuits designed for this purpose are 74AHCT4049 (Hex Inverting Logic Level Down Converter) and 74AHCT4050 (Hex Logic Level Down Converter). These parts have a modified input protection structure that enables them to be used as logic level translators which convert high-level logic to low-level logic while operating from the low logic supply. In this case, since the low logic supply is zero (unpowered), the outputs of the 4049 and 4050 will always be zero regardless of the inputs.

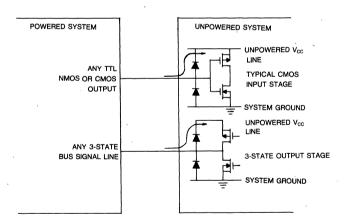


FIGURE 32. Direct interface to unpowered CMOS\ICs presents a dangerous situation where high-level signals forward-bias input and output protection diodes and try to "power-up" the Vcc line.

Excessive currents at such an interface can cause damage to the circuitry.

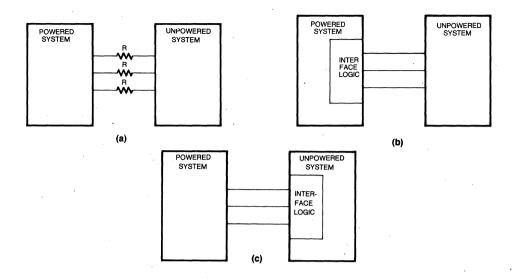
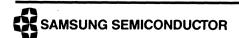


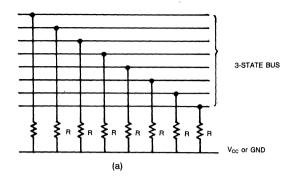
FIGURE 33. Methods of protection in power-down situations: (a) Use of series resistors to limit input currents to absolute maximum ratings, (b) Interface logic circuitry that forces all outputs to either ground or high-impedance state, (c) Interface circuitry at board inputs that acts as buffer between powered and unpowered devices; ideal components for this purpose are the 74AHCT4049 and 74AHCT 4050 Hex Logic Level Down Converters that lack the V<sub>CC</sub> diode in their protection circuitry.

- In bus-oriented systems, don't allow the bus to stay in high-impedance state for extended periods of time if it is not terminated, because this will have the same effect as leaving inputs open. Two simple ways of terminating the bus are illustrated in Figure 34. Most microprocessor-based systems, however, do not keep the bus in 3-state for long periods, in which case, the bus capacitance can maintain valid logic levels. In these cases, pull-up or pull-down circuitry may not be necessary.
- •The edge-rates of the AHCT and HCTLS part are similar to the very high-speed TTL parts. Therefore, system grounding and supply-decoupling techniques normally employed in high-speed TTL designs should be duplicated in AHCT/HCTLS designs to ensure proper operation. A good rule of thumb to reduce the affects of PC board trace inductance is to place 0.01 to 0.1 µF RF-grade capacitors every two-to-five ICs (octal flip-flops and buffers may require more decoupling). This, of course, has to be accompanied by careful pc board layout to minimize these inductances.
- The testing problems encountered in ALS, LS and FAST apply also to AHCT and HCTLS. Most of these problems result from the noise produced by the interactions of the device being tested and the test system. Typical test fixtures have lead inductances several times that of a PC board socket. This inductance, especially in the device ground path is the source of these problems.

The outputs, for example, can cause transient currents in the 50 to 200 mA range within a couple of nanoseconds while changing state. These appear as changes in the voltage drop across the device ground lead. The test system's input and output reference voltages are set with respect to tester ground and are not affected by these transients. Consequently the effective input voltages to the device will vary. If the ground pin goes up 1 volt, all the inputs effectively go down 1 volt. This must be considered in selecting input and output voltage levels. In functional tests, for example, solid input logic levels should be applied, instead of 0.8 and 2.0 volts.

Furthermore, if TTL test programs are to be used, one must be particularly careful not to apply voltages to inputs and outputs that are below ground or above V<sub>CC</sub> in excess of the absolute maximum limits specified in the data sheets.





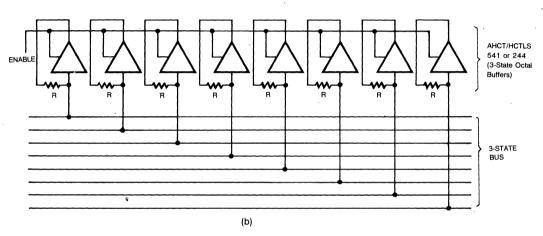


FIGURE 34. Methods of terminating 3-state buses; (a) Pullup or pulldown resistors (b) Use of 3-state buffers. The latter approach terminates the bus to the last active logic level and dissipates no static power.

## NOTES

# KS54/74AHCT DATA SHEETS 4



## KS54AHCT 00

#### **FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- . Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
  - $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

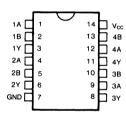
## **DESCRIPTION**

These devices contain four independent 2-input NAND gates that perform the Boolean functions  $Y = \overline{A \bullet B}$  or  $Y = \overline{A} + \overline{B}$ 

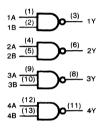
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{\text{CC}}$  and ground.

#### PIN CONFIGURATION



#### LOGIC DIAGRAM



#### **FUNCTION TABLE**

(Each Gate)

Inp	uts	Output
Α	В	Y
Н	Н	L
L	Χ	H
Χ	L	н

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±35 mA
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . . . . . . . . . 4.5V to 5.5V DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . OV to  $V_{CC}$  Operating Temperature

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . Max 500 ns

 Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

#### DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	ymbol Test Conditions		= 25°C	KS74AHCT $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit	
,			Тур		Guaranteed Limits			
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	٧	
Maximum Low-Level Input Voltage	VįL			0.8	0.8	0.8	v	
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	v	
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0,1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v	
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ	
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.0	20.0	40.0	μΑ	
Additional Worst Case Supply Current	Δlcc	per input pin $V_I=2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA	

## AC ELECTRICAL CHARACTERISTICS (Input tr., tres 2 ns), AHCTOO

Characteristic	Symbol	Conditions†	$T_a = 25^{\circ}C$ $V_{CC} = 5.0V$ $Typ$			KS54AHCT T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%		Unit
				Min	Max	Min	Max	
Propagation Delay	t <sub>PLH</sub>	C <sub>L</sub> =50pF	7		11		14	ns
Topagation Delay	t <sub>PHL</sub>		7		11		14	"
Input Capacitance	CIN		5					рF
Power Dissipation Capacitance*	C <sub>PD</sub>	(per gate)	15					pF

<sup>\*</sup> CPD determines the no-load dynamic power dissipation: PD=CPD VCC2 f + ICC VCC.

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.



#### **FEATURES**

- . Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
  - $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5V$
- . Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

• Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

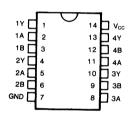
#### DESCRIPTION

These devices contain four independent 2-input NAND gates with open-drain outputs. Using a suitable pull-up resistor, these outputs may be connected to other opendrain outputs to implement wired-AND functions.

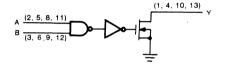
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V<sub>CC</sub> and ground.

#### PIN CONFIGURATION



#### LOGIC DIAGRAM



#### **FUNCTION TABLE**

(Each Gate)

Inp	uts	Output
Α	В	γ.
Н	Н	L
L	Χ	'H
Х	L	н

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur

These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Supply Voltage, V <sub>CC</sub>	4.5V to 5.5V
DC Input & Output Voltages*, VIN, VOUT	
Operating Temperature	

Range KS74AHCT: -40°C to +85°C
KS54AHCT: -55°C to +125°C
Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . Max 500 ns

 Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

#### DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	bol Test Conditions	ns T <sub>a</sub> = 25°C		KS74AHCT KS54AHCT T <sub>a</sub> = -40°C to +85°C T <sub>a</sub> = -55°C to +12		Unit
			Тур	,	Guaranteed Lim	its	
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	v
Maximum Low-Level Input Voltage	VIL	,		0.8	0.8	0.8	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	l <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Output Leakage Current	loz	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> =V <sub>CC</sub>		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	ΔΙσ	per input pin $V_{I}{=}2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}{=}0\mu\text{A}$		2.7	2.9	3.0	mA

### AC ELECTRICAL CHARACTERISTICS (Input tr. tr <2 ns), AHCT01

Characteristic	Symbol Co	Conditions <sup>†</sup>	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	KS74AHCT T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%		KS54AHCT T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> =5.0V ± 10%		Unit
			Тур	Min	Max	Min	Max	
Propagation Delay	t <sub>PLH</sub>	C <sub>L</sub> =50pF	. 17		25		29	ns
	t <sub>PHL</sub>	$R_L=1k\Omega$	10		16		19	113
Input Capacitance	CIN		5					рF
Power Dissipation Capacitance*	C <sub>PD</sub>	(per gate)	15					pF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.



#### 4

#### **FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
  - $I_{OL}$  =8 mA @  $V_{OL}$  =0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

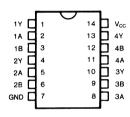
#### **DESCRIPTION**

These devices contain four independent 2-input NOR gates that perform the Boolean functions  $Y = \overline{A} + \overline{B}$  or  $Y = \overline{A} \bullet \overline{B}$ .

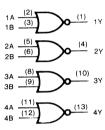
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and around.

#### PIN CONFIGURATION



## LOGIC DIAGRAM



#### **FUNCTION TABLE**

(Each Gate)

Inp	uts	Output
Α	В	Y
Н	Х	L
Х	Н	L
L	L	н

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V)$ ±20 mA
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
Vcc or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-

posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Supply Voltage,	Vcc	4.5	V to 5.5V
DC Input & Outp	out Voltages*, V <sub>IN</sub> ,	Vout	OV to Vcc
Operating Temp	erature		
Range	KS74AHCT:	-40°C t	o +85°C
	MOE ANDOT		

KS54AHCT: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T <sub>a</sub> = 25°C		$KS74AHCT$ $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54AHCT $T_a = -55$ °C to $+125$ °C	Unit
			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	v
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	V <sub>CC</sub> 4.2	V <sub>CC</sub> −0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> = 0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> =20µA I <sub>O</sub> =4mA I <sub>O</sub> =8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	IIN	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0 .	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.0	20.0	40.0	μА
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

## AC ELECTRICAL CHARACTERISTICS (Input tr, tres 2 ns), AHCT02

Characteristic	Symbol	Conditions <sup>†</sup>	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	$T_a = -40^{\circ}$	AHCT C to +85°C OV ± 10%	$T_a = -55$ °C	AHCT to +125°C V ± 10%	Unit
			Тур	Min	Max	Min	Max	]
Propagation Delay	t <sub>PLH</sub>	C <sub>L</sub> =50pF	7		12		14	ns
Topagation Bolay	t <sub>PHL</sub>		7		12		14	] '''
Input Capacitance	CIN		5					pF
Power Dissipation Capacitance*	C <sub>PD</sub>	(per gate)	15					pF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.



#### **FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
   I<sub>OL</sub> = 8 mA @ V<sub>OL</sub> = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

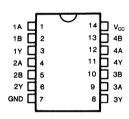
#### DESCRIPTION

These devices contain four independent 2-input NAND gates with open-drain outputs. Using a suitable pull-up resistor, these outputs may be connected to other open-drain outputs to implement wired-AND functions.

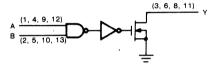
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### PIN CONFIGURATION



#### LOGIC DIAGRAM



#### **FUNCTION TABLE**

(Each Gate)

Inp	uts	Output
Α	В	Y
Н	Н	L
L	Χ	н
Х	L	н

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . Max 500 ns

 Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

### DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Symbol Test Conditions		= 25°C	KS74AHCT T <sub>a</sub> = -40°C to +85°C	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	0.8	٧
Maximum Low-Level Output Voltage	VoL	$V_{IN}$ = $V_{IH}$ or $V_{IL}$ $I_{O}$ =20 $\mu$ A $I_{O}$ =4mA $I_{O}$ =8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	l <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Output Leakage Current	loz	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> =V <sub>CC</sub>		±0.5	±5.0	±10.0	μА
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin $V_l=2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

#### AC ELECTRICAL CHARACTERISTICS (Input tr, tr≤2 ns), AHCTO3

Characteristic	Symbol	Conditions <sup>†</sup>	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	$KS74$ $T_a = -40^{\circ}$ $V_{CC} = 5$ .	AHCT C to +85°C 0V ± 10%	$KS54$ $T_a = -55°C$ $V_{CC} = 5.0$	1AHCT C to +125°C 0V ± 10%	Unit
			Тур	Min	Max	Min	Max	
Propagation Delay	t <sub>PLH</sub>	C <sub>L</sub> =50pF	17		25		29	ns
Topagation Belay	t <sub>PHL</sub>	$R_L=1k\Omega$	10		16		19	7 113
Input Capacitance	CIN		5		,			рF
Power Dissipation Capacitance*	C <sub>PD</sub>	(per gate)	15					pF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.



## KS54AHCT **04**

#### **FEATURES**

- · Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
  - $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5 \text{V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- · Characterized for operation over industrial and military temperature ranges: KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

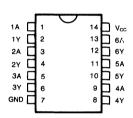
### **DESCRIPTION**

These devices contain six independent inverters. They perform the Boolean function  $Y = \overline{A}$ .

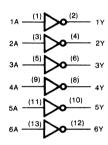
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and vet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V<sub>CC</sub> and ground.

#### PIN CONFIGURATION



#### LOGIC DIAGRAM



#### **FUNCTION TABLE**

#### (Each Inverter)

Input	Output
A	Y
Н	L
L	Н

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Supply Voltage,	V <sub>CC</sub>	4.5V to 5.5V
DC Input & Outp	out Voltages*, V <sub>IN</sub> ,	Vout . OV to Voc
Operating Temper	erature	*
Range	KS74AHCT:	-40°C to +85°C

\* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

#### DC ELECTRICAL CHARACTERISTICS (Vcc=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	a = 25°C	KS74AHCT $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54AHCT $\Gamma_a = -55$ °C to $+125$ °C	Unit
			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	V <sub>CC</sub> 4.2	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> -0.1 3.84	V <sub>CC</sub> -0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	lin	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.0	20.0	40.0	μА
Additional Worst Case Supply Current	Δlcc	per input pin  V <sub>I</sub> =2.4V  other Inputs:  at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0µA		2.7	2.9	. 3.0	mA

## AC ELECTRICAL CHARACTERISTICS (Input tr, ti-2 ns), AHCT04

Characteristic	Symbol Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	$T_a = -40^{\circ}$			to +125°C	Unit	
			Тур	Min	Max	Min	Max	
Propagation Delay	t <sub>PLH</sub>	C <sub>L</sub> =50pF	7		11		14	ns
Propagation Delay	t <sub>PHL</sub>		7		11		14	
Input Capacitance	CIN		5					pF
Power Dissipation Capacitance*	C <sub>PD</sub>	(per gate)	15					pF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

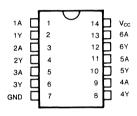
<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.



#### **FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
  - IOL = 8 mA @ VOL = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
   KS74AHCT: -40°C to +85°C
- KS54AHCT: -55°C to +125°C
   Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

## PIN CONFIGURATION



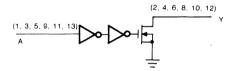
#### **DESCRIPTION**

These devices contain six independent inverters with opendrain outputs. Using a suitable pull-up resistor, these outputs may be connected to other open-drain outputs to implement wired-AND functions.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### LOGIC DIAGRAM



#### **FUNCTION TABLE**

(Each Inverter)

	<u>.</u>
Input	Output
A	Y
Н	L
L	н

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Supply Voltage, V <sub>CC</sub>	4.5V to 5.5V
DC Input & Output Voltages*, VIN, VOUT	OV to Vcc
Operating Temperature	

Range KS74AHCT: -40°C to +85°C
KS54AHCT: -55°C to +125°C
Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

#### DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic Syml		Test Conditions	T <sub>a</sub> = 25°C		KS74AHCT $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54AHCT $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$	Unit
		·	Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			∞0.8	0.8	0.8	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Output Leakage Current	loz	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> =V <sub>CC</sub>		±0.5	±5.0	·±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA	7	2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin $V_1=2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

#### AC ELECTRICAL CHARACTERISTICS (Input tr., tr 42 ns), AHCT05

Characteristic	Symbol	Conditions†	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	KS74AHCT T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%		KS54AHCT $T_a = -55^{\circ}\text{C to } +125^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit
			Тур	Min	Max	Min	Max	]	
Propagation Delay	t <sub>PLH</sub>	C <sub>L</sub> =50pF	17		25		29	ns	
	t <sub>PHL</sub>	$R_L=1k\Omega$	8		14	*	33		
Input Capacitance	CIN		5					pF	
Power Dissipation Capacitance*	C <sub>PD</sub>	(per inverter)	15					pF	

C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.



#### **FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
   I<sub>OL</sub> = 8 mA @ V<sub>OL</sub> = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

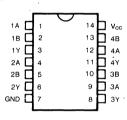
#### DESCRIPTION

These devices contain four independent 2-input AND gates. They perform the Boolean functions  $Y = A \bullet B$  or  $Y = \overline{A + B}$ .

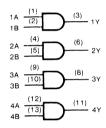
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### PIN CONFIGURATION



#### LOGIC DIAGRAM



#### **FUNCTION TABLE**

#### (Each Gate)

Inp	uts	Output
A	В	Y
Н	Н	Н ′
L	Χ	L
Χ	L	L

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IoK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, $P_d^{\dagger}$ 500 mW
* Absolute Maximum Patings are those values beyond

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Supply Voltage, V<sub>CC</sub> . . . . . . . . . . . . . . . . . 4.5V to 5.5V DC Input & Output Voltages\*, V<sub>IN</sub>, V<sub>OUT</sub> . . OV to V<sub>CC</sub> Operating Temperature

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

#### DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T <sub>a</sub> = 25°C		KS74AHCT T <sub>a</sub> = -40°C to +85°C	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH} \text{ or } V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-4\text{mA}$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> -0.1	V <sub>CC</sub> -0.1 3.7	. <b>V</b>
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	l <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

## AC ELECTRICAL CHARACTERISTICS (Input tr, tr≤2 ns), AHCT08

Characteristic	Symbol	Conditions <sup>†</sup>	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	$T_a = -40^{\circ}$	AHCT C to +85°C DV ±10%	$T_a = -55$ °C	AHCT to +125°C V ± 10%	Unit
			Тур	Min	Max	Min	Max	
Propagation Delay	t <sub>PLH</sub>	C <sub>L</sub> =50pF	8		14		17	ns
	t <sub>PHL</sub>		8		14		17	
Input Capacitance	CIN		5			•		pF
Power Dissipation Capacitance*	C <sub>PD</sub>	(per gate)	15					pF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.



These devices contain four independent 2-input AND gates

with open-drain outputs. Using a suitable pull-up resistor,

these outputs may be connected to other open-drain out-

These devices provide speeds and drive capability

equivalent to their ALSTTL counterparts and vet maintain

CMOS power levels. The input and output voltage levels

allow direct interface with TTL, NMOS and CMOS devices

All inputs and outputs are protected from damage due to

static discharge by internal diode clamps to V<sub>CC</sub> and

puts to implement wired-AND functions.

without any external components.

#### **FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
  - $I_{OL} = 8 \text{ mA } @ V_{OL} = 0.5 \text{V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

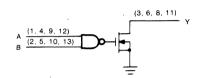
KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

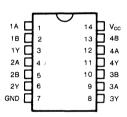
## LOGIC DIAGRAM

ground.

**DESCRIPTION** 



#### PIN CONFIGURATION



#### **FUNCTION TABLE**

#### (Each Gate)

Inp	uts	Output
Α	В	Y
Н	Н	Н
L	Χ	L
Χ	L	L.

Supply Voltage Range  $V_{CC}$ , -0.5V to  $\pm 7V$  DC Input Diode Current,  $I_{IK}$   $(V_I < -0.5V \text{ or } V_I > V_{CC} +0.5V)$   $\pm 20 \text{ mA}$  DC Output Diode Current,  $I_{OK}$   $(V_O < -0.5V \text{ or } V_O > V_{CC} +0.5V)$   $\pm 20 \text{ mA}$  Continuous Output Current Per Pin,  $I_O$   $(-0.5V < V_O < V_{CC} +0.5V)$   $\pm 35 \text{ mA}$  Continuous Current Through  $V_{CC}$  or GND pins  $\pm 125 \text{ mA}$  Storage Temperature Range,  $T_{stg}$   $-65^{\circ}C$  to  $\pm 150^{\circ}C$  Power Dissipation Per Package,  $P_{ctg}$   $\pm 125 \text{ mA}$ 

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

### **Recommended Operating Conditions**

Supply Voltage, V<sub>CC</sub> . . . . . . . . . . 4.5V to 5.5V DC Input & Output Voltages\*, V<sub>IN</sub>, V<sub>OUT</sub> . . OV to V<sub>CC</sub> Operating Temperature

Range KS74AHCT:  $-40^{\circ}$ C to  $+85^{\circ}$ C KS54AHCT:  $-55^{\circ}$ C to  $+125^{\circ}$ C Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns

\* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

### DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	symbol Test Conditions		= 25°C	KS74AHCT $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	iits	
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	0.8	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	О	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	liN	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Output Leakage Current	loz	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> =V <sub>CC</sub>		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin $V_I$ =2.4V other inputs: at $V_{CC}$ or GND $I_{OUT}$ =0 $\mu$ A		2.7	2.9	3.0	mA

#### AC ELECTRICAL CHARACTERISTICS (Input t<sub>r</sub>, t<sub>f</sub>≤2 ns), AHCT09

Characteristic	Symbol	Conditions† V <sub>C</sub>	$T_a = 25^{\circ}C$ $V_{CC} = 5.0V$	$KS74AHCT$ $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55^{\circ}\text{C to } + 125^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit
'			Тур	Min	Max	Min	Max	
Propagation Delay	t <sub>PLH</sub>	C <sub>L</sub> =50pF	18		27		31	ns
Propagation Delay	t <sub>PHL</sub>	$R_L=1k\Omega$	9		15		18	
Input Capacitance	CIN		5					pF
Power Dissipation Capacitance*	C <sub>PD</sub>	(per gate)	15					pF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.



- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs: I<sub>OL</sub> = 8 mA @ V<sub>OL</sub> = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

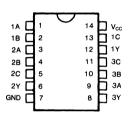
### **DESCRIPTION**

These devices contain three independent 3-input NAND gates. They perform the Boolean functions  $Y = \overline{A \bullet B \bullet C}$  or  $Y = \overline{A} + \overline{B} + \overline{C}$ .

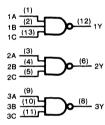
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{\text{CC}}$  and ground.

#### PIN CONFIGURATION



#### LOGIC DIAGRAM



#### **FUNCTION TABLE**

#### (Each Gate)

	Inputs	Output	
A	В.	С	Y
Н	Н	Н	L
L	Х	X	н
Х	L	Х	н
Х	Χ	L	Н

## .

### **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW
* Absolute Maximum Ratings are those values beyond

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

### **Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..., 4.5V to 5.5V DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  .. 0V to  $V_{CC}$  Operating Temperature

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

Input Rise & Fall Times,  $t_r$ ,  $t_f$  ......... Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

### DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

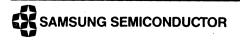
Characteristic	Symbol	Test Conditions	T,	= 25°C	$KS74AHCT$ $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54AHCT $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$	Unit
		Typ Guaranteed Limits					
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> -0.1	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	lin	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin  V <sub>I</sub> =2.4V  other inputs: at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

### AC ELECTRICAL CHARACTERISTICS (Input tr, tie2 ns), AHCT10

Characteristic	Symbol Conditions†		T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		to +125°C	Unit	
			Тур	Min	Max	Min	Max	
Propagation Delay	t <sub>PLH</sub>	C <sub>I</sub> = 50pF	9		15		18	ns
Tropagation Bolay	t <sub>PHL</sub>	оц-оорі	9		15		18	113
Input Capacitance	CIN		5					pF
Power Dissipation Capacitance*	C <sub>PD</sub>	(per gate)	15					pF

<sup>\*</sup> CPD determines the no-load dynamic power dissipation: PD=CPD VCC2 f + ICC VCC.

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.



- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
  - IOL = 8 mA @ VOL = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

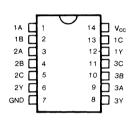
#### **DESCRIPTION**

These devices contain three independent 3-input AND gates. They perform the Boolean functions  $Y = A \cdot B \cdot C$  or  $Y = \overline{A} + \overline{B} + \overline{C}$ .

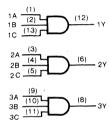
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{\text{CC}}$  and ground.

#### PIN CONFIGURATION



#### LOGIC DIAGRAM



#### **FUNCTION TABLE**

(Each Gate)

	Inputs	Output	
A	В	С	Y
Н	Н	Η	. H
L	X	Х	L
Χ	L	Х	L
Х	Х	L	L

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_{I} < -0.5V \text{ or } V_{I} > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, I <sub>OK</sub>
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 35 \text{ mA}$
Continuous Current Through
Vcc or GND pins ±125 mA
Storage Temperature Range, $T_{stg} \dots -65^{\circ}C$ to $+150^{\circ}C$
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW
* Absolute Maximum Ratings are those values howard

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

### **Recommended Operating Conditions**

Supply Voltage, V <sub>CC</sub>		4.5V to 5.5V
DC Input & Output Voltages*,	V <sub>IN</sub> , V <sub>OUT</sub>	OV to Vcc
Operating Temperature		

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . Max 500 ns

### DC ELECTRICAL CHARACTERISTICS (Vcc=5V±10% Unless Otherwise Specified)

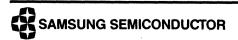
Characteristic	Symbol	mbol Test Conditions		ymbol Test Conditions		= 25°C	KS74AHCT T <sub>a</sub> = -40°C to +85°C	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
			Тур	Guaranteed Limits					
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	٧		
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	0.8	٧		
Minimum High-Level Output Voltage	VoH	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1	v		
Maximum Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> =20µA I <sub>O</sub> =4mA I <sub>O</sub> =8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v		
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		,±0.1	±1.0	±1.0	μΑ		
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.0	20.0	40.0	μΑ		
Additional Worst Case Supply Current	Δlcc	per input pin  V <sub>I</sub> =2.4V  other Inputs: at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0µA		2.7	2.9	3.0	mA		

#### AC ELECTRICAL CHARACTERISTICS (Input tr, tr≤2 ns), AHCT11

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	$T_a = -40^{\circ}$	AHCT C to +85°C 0V±10%	$T_a = -55$ °C	IAHCT C to +125°C DV ± 10%	Unit
	1	,	Тур	Min	Max	Min	Max	]
Propagation Delay	t <sub>PLH</sub>	C <sub>L</sub> =50pF	9		15		18	ns
r Topagation Delay	t <sub>PHL</sub>	$R_L=1k\Omega$	9		15		18	1113
Input Capacitance	CiN		5			,		pF
Power Dissipation Capacitance*	C <sub>PD</sub>	(per gate)	15					pF

<sup>\*</sup> CPD determines the no-load dynamic power dissipation: PD=CPD VCC2 f + ICC VCC.

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.



Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

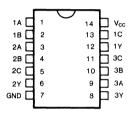
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
  - $I_{OL} = 8 \text{ mA } @ V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

### **PIN CONFIGURATION**



#### DESCRIPTION

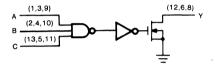
These devices contain three independent 3-input NAND gates with open-drain outputs. They perform the Boolean functions  $Y = \overline{A} \bullet B \bullet \overline{C}$  or  $Y = \overline{A} + \overline{B} + \overline{C}$ .

Using a suitable pull-up resistor, these outputs may be connected to other open-drain outputs to implement wired-AND functions.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### LOGIC DIAGRAM



#### **FUNCTION TABLE**

(Each Gate)

	Inputs	Output	
Α	В	C	Y
Н	Н	Н	L
L	Х	Х	Н
Χ	L	X	Н
Χ	X	L	Н

• • • • • • • • • • • • • • • • • • • •
Supply Voltage Range $V_{CC}$ , $-0.5V$ to $+7V$
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW

Storage Temperature Range, T<sub>stg</sub>...-65°C to +150°C Power Dissipation Per Package, P<sub>d</sub>†.......500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation

of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

### **Recommended Operating Conditions**

Range KS74AHCT:  $-40^{\circ}$ C to  $+85^{\circ}$ C KS54AHCT:  $-55^{\circ}$ C to  $+125^{\circ}$ C Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . . Max 500 ns

 Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

### DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	t Conditions T <sub>a</sub> = 25°C		KS74AHCT KS54AHCT $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $T_a = -55^{\circ}\text{C to } +12^{\circ}$		Unit
	}		Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	v
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	0.8	v
Maximum Low-Level Output Voltage	Vol	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	О	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	. I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Output Leakage Current	loz	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> =V <sub>CC</sub>		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin $V_1$ =2.4V other inputs: at $V_{CC}$ or GND $I_{OUT}$ =0 $\mu$ A		2.7	2.9	3.0	mA

### AC ELECTRICAL CHARACTERISTICS (Input tr, tr <2 ns), AHCT12

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	$KS74AHCT$ $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$ $V_{CC} = 5.0V \pm 10^{\circ}$		KS54AHCT $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Тур	Min	Max	Min	Max	
Propagation Delay	tplH	C <sub>L</sub> =50pF	19		27,		31	ns
Topagation Bolay	t <sub>PHL</sub>		11		18		22	113
Input Capacitance	CIN		5					pF
Power Dissipation Capacitance*	C <sub>PD</sub>	(per gate)	15					рF

<sup>\*</sup> CPD determines the no-load dynamic power dissipation: PD=CPD VCC2 f + ICC VCC.

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.



#### 4

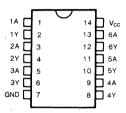
#### **FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs: I<sub>OL</sub> = 8 mA @ V<sub>OL</sub> = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

### PIN CONFIGURATION



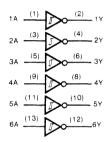
#### DESCRIPTION

These Schmitt-trigger devices contain six independent inverters. They perform the Boolean function  $Y = \overline{A}$ .

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### LOGIC DIAGRAM



#### **FUNCTION TABLE**

#### (Each Inverter)

(22011 111101101)					
Input	Output				
Α	Y				
Н	L				
L	н				

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, $P_d^{\dagger}$ 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.
These are stress ratings only and functional operation
3 ,
of the device at or beyond them is not implied. Long ex-
posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

### **Recommended Operating Conditions**

Supply Voltage, \	Vcc	4.5V to 5.5V
DC Input & Outpo	ut Voltages*, V <sub>IN</sub> ,	Vout OV to Vcc
Operating Tempe	rature	
Range	KS74AHCT:	-40°C to +85°C

KS74AHCT: -40°C to +65°C KS54AHCT: -55°C to +125°C

 Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

### DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T <sub>a</sub> = 25°C		K\$74AHCT T <sub>a</sub> = -40°C to +85°C	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN} = V_{IH}$ or $V_{IL}$ $I_{O} = -20\mu A$ $I_{O} = -4mA$	V <sub>C</sub> C 4.2	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> -0.11	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.0	20.0	40.0	μА
Additional Worst Case Supply Current	Δlcc	per input pin  V <sub>I</sub> =2.4V  other inputs: at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

### DC ELECTRICAL CHARACTERISTICS

Characteristic		Symbol	Symbol Test Conditions		25°C	KS74AHCT T <sub>a</sub> = -40°C to +85°C		KS54AHCT T <sub>a=-55°C</sub> to +125°C		Unit
		Oyboi	rest conditions	Min	Max	Min	Max	Min	Max	
	Positive-Going ·	V <sub>T+</sub>	V <sub>CC</sub> =4.5V	1.2	1.9	1.2	1.9	1.2	1.9	V
	Threshold Voltage	VI+	V <sub>CC</sub> =5.5V	1.4	2.1	1.4	2,1	1.4	2.1	
	Negative-Going	V <sub>T</sub> _	V <sub>CC</sub> =4.5V	0.5	1.2	0.5	1.2	0.5	1.2	v
	Threshold Voltage	•1-	$V_{CC}=5.5V$	0.6	1.4	0.6	1.4	0.6	1.4	] [
	Hysteresis	VH	V <sub>CC</sub> =4.5V	0.4	1.4	0.4	1.4	0.4	1.4	v
	(V <sub>T+</sub> -V <sub>T-</sub> )	VH	V <sub>CC</sub> =5.5V	0.4	1.5	0.4	1.5	0.4	1.5	•

### AC ELECTRICAL CHARACTERISTICS (Input tr, tre2 ns), AHCT14

Characteristic	Symbol	Conditions <sup>†</sup>	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	$KS74AHCT \\ T_a = -40 ^{\circ}C \text{ to } +85 ^{\circ}C \\ V_{CC} = 5.0V \pm 10 \%$		KS54AHCT T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> =5.0V ± 10%		Unit
			Тур	Min	Max	Min	Max	
Propagation Delay	t <sub>PLH</sub>	C <sub>L</sub> =50pF	8		14		17	ns
Topagation Delay	tehl		8		15		19	
Input Capacitance	CIN		5					pF
Power Dissipation Capacitance*	C <sub>PD</sub>	(per gate)	15					pF

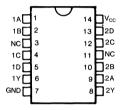
<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} \ V_{CC}^2 \ f + I_{CC} \ V_{CC}$ .
† For AC switching test circuits and timing waveforms see section 2.

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
   I<sub>OL</sub> = 8 mA @ V<sub>OL</sub> = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATION



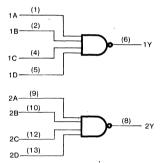
#### DESCRIPTION

These devices contain two independent 4-input NAND gates. They perform the Boolean functions  $Y = \overline{A \cdot B \cdot C \cdot D}$  or  $Y = \overline{A + B} + \overline{C} + \overline{D}$  in positive logic.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground

#### **LOGIC DIAGRAM**



#### **FUNCTION TABLE**

(Each gate)

, , , , , , , , , , , , , , , , , , ,									
	INP	OUTPUT							
Α	В	С	D	Y					
Н	Н	Н	.H	L					
L	Χ	Χ	Χ	Н					
X	L	Χ	Χ	Н					
X	X	L	Χ	Н					
X	Х	Χ	L	н					

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±35 mA
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.

These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

### **Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . . . . . . 4.5V to 5.5V DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . 0V to  $V_{CC}$  Operating Temperature

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . Max 500 ns

\* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

#### DC ELECTRICAL CHARACTERISTICS (Vcc=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	a = 25°C	$KS74AHCT$ $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	$KS54AHCT$ $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$	Unit
			Тур		its		
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	v
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> −0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	o	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin  V <sub>I</sub> =2.4V  other Inputs: at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

### AC ELECTRICAL CHARACTERISTICS (Input tr, tr <2 ns), AHCT20

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V Typ	$KS74AHCT$ $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Min	Max	Min	Max	
Propagation Delay,	tpLH	C <sub>L</sub> =50pF	7		11		13	ns
Any input to Y	t <sub>PHL</sub>	оц-зорі	7		11		13	113
Input Capacitance	CIN		5					рF
Power Dissipation Capacitance*	C <sub>PD</sub>	(per gate)						pF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

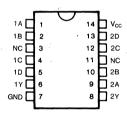


- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs: I<sub>OL</sub> = 8 mA @ V<sub>OL</sub> = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

### PIN CONFIGURATION



#### **FUNCTION TABLE**

#### (Each gate)

	INP	OUTPUT		
A	В	С	D	Y
Н	Н	Н	٠Η	н
L	Χ	Χ	Х	L
×	L	Χ	Х	L
X	Χ	L	Х	L
X	Х	Χ	L	L

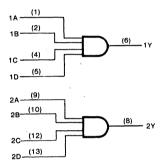
### **DESCRIPTION**

These devices contain two independent 4-input AND gates. They perform the Boolean functions  $Y=A \bullet B \bullet C \bullet D$  or  $Y=\overline{A}+\overline{B}+\overline{C}+\overline{D}$  in positive logic.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{\text{CC}}$  and ground.

#### LOGIC DIAGRAM



Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V)$ . , $\pm 20 \text{ mA}$
DC Output Diode Current, I <sub>OK</sub>
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±35 mA
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-
posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

### **Recommended Operating Conditions**

Supply Voltage, V <sub>CC</sub>	4.5V to 5.5V
DC Input & Output Voltages*, VIN, VOUT	OV to $V_{CC}$
Operating Temperature	

Range KS74AHCT:  $-40\,^{\circ}$ C to  $+85\,^{\circ}$ C KS54AHCT:  $-55\,^{\circ}$ C to  $+125\,^{\circ}$ C Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . . . Max 500 ns

 Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

#### DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	ymbol Test Conditions		= 25°C	KS74AHCT T <sub>a</sub> = -40°C to +85°C	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
		-	Тур		Guaranteed Lim	its ,	
Minimum High-Level Input Voltage	V <sub>IH</sub>	·		2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	Icc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin  V <sub>1</sub> =2.4V  other Inputs: at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0µA		2.7	2.9	3.0	mA

### AC ELECTRICAL CHARACTERISTICS (Input tr, tr <2 ns), AHCT21

Characteristic	Symbol Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	$KS74AHCT \\ T_a = -40^{\circ}C \text{ to } +85^{\circ}C \\ V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$		Unit	
			Тур	Min	Max	Min	Max	1
Propagation Delay, Any input to Y	t <sub>PLH</sub>	C <sub>L</sub> =50pF	8		14		17•	ns
	t <sub>PHL</sub>		8		14		17 -	,,,,
Input Capacitance	CIN		5					рF
Power Dissipation Capacitance*	C <sub>PD</sub>	(per gate)						pF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.



- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs: I<sub>OL</sub> = 8 mA @ V<sub>OL</sub> = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
   KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

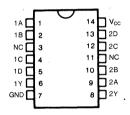
#### DESCRIPTION

These devices contain two independent 4-input NAND gates. These gates perform the Boolean functions  $Y = \overline{A} + \overline{B} + \overline{C} + \overline{D}$  or  $Y = \overline{A} + \overline{B} + \overline{C} + \overline{D}$  in positive logic. The open-drain outputs require pull-up resistors to perform correctly. They may be connected to other open-drain outputs to implement active low wired-OR or active high wired-AND functions.

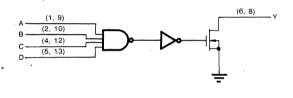
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### PIN CONFIGURATION



#### **LOGIC DIAGRAM**



#### **FUNCTION TABLE**

(Each Gate)

	INP	OUTPUT		
Α	В	С	D	Υ ,
Н	Н	Н	Н	L
L	Χ	Χ	Χ	Н
X	Ļ	Χ	Χ	H
X	Χ	L	Χ	H
X	Х	Х	L	Ĥ

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation

of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

### **Recommended Operating Conditions**

Supply Voltage, \	/cc	4.5V to 5.5V
DC Input & Output	ut Voltages*, V <sub>IN</sub> ,	Vout OV to Vcc
Operating Tempe	rature	
Range	KS74AHCT:	-40°C to +85°C

KS54AHCT: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . . Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

#### DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T <sub>a</sub> = 25°C		KS74AHCT $T_{a=-40}^{\circ}\text{C to } +85^{\circ}\text{C}$	KS54AHCT $T_{a} = -55$ °C to +125°C	Unit
_					Guaranteed Limits		
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	٧
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Output Leakage Current	loz	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> =V <sub>CC</sub>		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

### AC ELECTRICAL CHARACTERISTICS (Input tr, ti <2 ns), AHCT22

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	$T_a = -40^\circ$	AHCT C to +85°C 0V ±10%	KS54AHCT T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> =5.0V± 10%		Unit
			Тур	Min	Max	Min	Max	]
Propagation Delay, Any input to Y	t <sub>PLH</sub>	C <sub>L</sub> =50pF	19		29		34	ns
	t <sub>PHL</sub>	R <sub>L</sub> =1kΩ	11		18		22	] ""
Input Capacitance	CIN		5					pF
Power Dissipation Capacitance*	C <sub>PD</sub>	(per gate)						pF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.



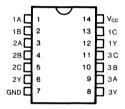
<sup>†</sup> Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
   I<sub>OL</sub> = 8 mA @ V<sub>OL</sub> = 0.5V
- Inputs and outputs interfacé directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATION



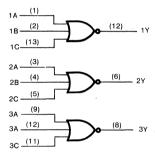
#### **DESCRIPTION**

These devices contain two independent 3-input NOR gates. They perform the Boolean functions  $Y = \overline{A} + \overline{B} + \overline{C}$  or  $Y = \overline{A} \bullet \overline{B} \bullet \overline{C}$  in positive logic.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### LOGIC DIAGRAM



#### **FUNCTION TABLE**

(Each Gate)

11	NPUT	OUTPUT	
Α	В	C.	Y
Н	Х	Х	L
X	Н	Х	L
Х	Χ	Н	L '
L	L	L	, Н ,

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, I <sub>OK</sub>
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

### **Recommended Operating Conditions**

Supply Voltage, Vcc			4.5V to	5.5V
DC Input & Output \	/oltages*, V <sub>II</sub>	N, Vout	OV to	V <sub>CC</sub>
Operating Temperati	ure			

Operating Temperature

Range KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

### DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic S	Symbol	Test Conditions	Т	a = 25°C	KS74AHCT T <sub>a = -40°C</sub> to +85°C	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	ViH	,		2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> -0.1 3.84	V <sub>CC</sub> -0.1	v
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.0	20.0	40.0	μА
Additional Worst Case Supply Current	ΔΙσο	per input pin $V_I$ =2.4V other Inputs: at $V_{CC}$ or GND $I_{OUT}$ =0 $\mu$ A		2.7	2.9	3.0	mA

#### AC ELECTRICAL CHARACTERISTICS (Input tr, tr <2 ns), AHCT27

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	$T_a = -40^\circ$	IAHCT C to +85°C 0V±10%	$KS54$ $T_a = -55°($ $V_{CC} = 5.6$	Unit	
			Тур	Min	Max	Min	Max	1
Propagation Delay, Any input to Y	t <sub>PLH</sub>	C <sub>L</sub> =50pF	8		14		17	ns
	t <sub>PHL</sub>		10		16		20	
Input Capacitance	CIN		5					pF
Power Dissipation Capacitance*	C <sub>PD</sub>	(per gate)						pF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
   I<sub>OL</sub> = 8mA @ V<sub>OL</sub> = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### **DESCRIPTION**

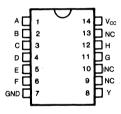
The '30 contains a single 8-input NAND gate. It performs the boolean functions (in positive logic):

 $Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H}$   $Y = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} + \overline{F} + \overline{G} + \overline{H}$ 

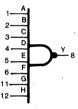
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### PIN CONFIGURATION



#### LOGIC DIAGRAM



#### **FUNCTION TABLE**

Inputs A Through	Н	Output Y		
All Inputs	Н	L		
One or more inputs	L	Н		

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, IIK
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V)$ ±20 mA
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

### **Recommended Operating Conditions**

Supply Voltage, V<sub>CC</sub> . . . . . . . . . . . . . . . . . 4.5V to 5.5V DC Input & Output Voltages\*, V<sub>IN</sub>, V<sub>OUT</sub> . . . OV to V<sub>CC</sub> Operating Temperature

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

#### DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic			т	a = 25°C	KS74AHCT	KS54AHCT		
	Symbol	Test Conditions		a-25 C	$T_a = -40$ °C to $+85$ °C	$T_a = -55^{\circ}C \text{ to } +125^{\circ}C$	Unit	
			Тур		Guaranteed Limits			
Minimum High-Level Input Voltage	V <sub>IH</sub>	,		2.0	2.0	2.0	v	
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v	
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4m A$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	v	
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$		0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v	
Maximum Input Current	liN	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ	
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.0	20.0	40.0	μΑ	
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA <sub>.</sub>	

#### AC ELECTRICAL CHARACTERISTICS (Input tr., tr <2 ns), AHCT30

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	KS74AHCT T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%		KS54AHCT T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%		Unit
			Тур	Min	Max	Min	Max	
Propagation Delay	t <sub>PLH</sub>	C <sub>L</sub> =50pF	6		11	0	14	ns
	t <sub>PHL</sub>		6		11		14	
Input Capacitance	CIN		5					рF
Power Dissipation Capacitance*	C <sub>PD</sub>		15				],	pF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.



- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
   I<sub>OL</sub> = 8 mA @ V<sub>OL</sub> = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

   CONTAINED. 1000 to 1000

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

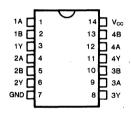
#### DESCRIPTION

These devices contain four independent 2-input OR gates. They perform the Boolean functions Y=A+B or Y=A•B.

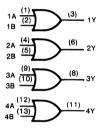
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL. NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damaged due to static discharge by internal diode clamps to  $V_{\rm cc}$  and ground.

#### PIN CONFIGURATION



#### LOGIC DIAGRAM



#### **FUNCTION TABLE**

(Each Gate)

Inputs		Outputs
Α	В	Y
Н	Х	н
X	Н	н
L	L	L

•
Supply Voltage Range $V_{CC}$ , $-0.5V$ to $+7V$
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, $P_d^{\dagger}$ 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-

posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

### **Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . . . . . . 4.5V to 5.5V DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . OV to  $V_{CC}$  Operating Temperature

Range KS74AHCT:  $-40^{\circ}$ C to  $+85^{\circ}$ C KS54AHCT:  $-55^{\circ}$ C to  $+125^{\circ}$ C Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . . Max 500 ns

 Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

### DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic S	Symbol	mbol Test Conditions		a = 25°C	KS74AHCT T <sub>a</sub> = -40°C to +85°C	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
			Тур	,	Guaranteed Limits		
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> -0.1 3.7	V
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0:39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	l <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μА
Maximum Quiescent Supply Current	loc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin  V <sub>1</sub> =2.4V  other Inputs:  at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0µA		2.7	2.9	3.0	mA

### AC ELECTRICAL CHARACTERISTICS (Input tr., tres 2 ns), AHCT32

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V Typ	$KS74AHCT$ $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Min	Max	Min	Max	
Propagation Delay	t <sub>PLH</sub>	C <sub>L</sub> =50pF	8		14		17	ns
Propagation Delay	t <sub>PHL</sub>		8		14		17	
Input Capacitance	CIN		5					pF
Power Dissipation Capacitance*	C <sub>PD</sub>	(per gate)	15	,				pF

<sup>\*</sup> CPD determines the no-load dynamic power dissipation: PD=CPD VCC2 f + ICC VCC.

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.



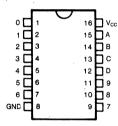
- Full decoding of Input Logic
- All outputs are High for Invalid BCD Conditions
- Also for application as 3-Line to 8-Line Decoders
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs: I<sub>OL</sub> = 8 mA @ V<sub>OL</sub> = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATION



#### **FUNCTION TABLE**

No.		Inp	uts					C	Out	put	s			
NO.	D	С	В	Α	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н
1	L	L	L	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н
2	L	L	Н	L	Н	Н	L	Н	Н	Н	Н	Н	Н	Н
3	L	L	Н	Н	Н	Н	Н	L	Н	Н	Н	Н	Η	Н
· 4	L	Н	L	L	Н	Н	Н	Н	L	Н	Н	Н	Н	Н
5	L	Н	L	Н	Н	Н	Н	Н	Н	L	Н	Н	Н	Н
6	L	Н	Н	L	Н	Н	Н	Н	Н	Н	L	Н	Н	Н
7	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	Н	Н
8	Н	L	L	L	Н	Н	Н	н	Н	Н	Н	Н	L	Н
9	Н	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L
	Н	L	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
INVALID	Н	Н	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
INVALID	Н	Н	L	Н	Н	Н	Н	н	Н	Н	Н	Н	Н	Н
	н	Н	Н	L	Н	Н	н	н	н	Н	Н	Н	Н	Н
	н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	н	Н	Н

#### **DESCRIPTION**

The '42 decoder accepts for active-high BCD inputs and provides 10 mutually exclusive active-low outputs, as shown by logic symbol or diagram. The active-low outputs facilitate addressing other MSI units with active low input enables.

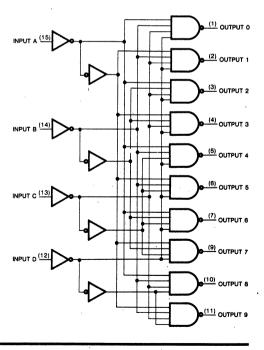
The logic design of the '42 ensures that all outputs are high when binary codes greater than nine are applied to the inputs.

The most significant input, D, produces a useful inhibit function when the '42 is used as a 1-of-8 decoder. The D input can also be used as the Data input in an 8-output demultiplexer application.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### LOGIC DIAGRAM



\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

### **Recommended Operating Conditions**

Supply Voltage, V <sub>CC</sub>	4.5V to 5.5V
DC Input & Output Voltages*, VIN, VOUT	OV to Vcc
Operating Temperature	

Operating Temperature

Range

KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . Max 500 ns

\* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

#### DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol Test Condition		T,	a = 25°C	KS74AHCT T <sub>a</sub> = -40°C to +85°C	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit	
y			Тур		Guaranteed Limits			
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	٧	
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	0.8	٧	
Minimum High-Level Output Voltage	Voh	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> -0.1	v	
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	ķ	
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ	
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ	
Additional Worst Case Supply Current	Δlcc	per input pin $V_{l}{=}2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}{=}0\mu\text{A}$		2.7	2.9	3.0	mA	

### AC ELECTRICAL CHARACTERISTICS (Input tr, tr <2 ns), AHCT42

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	KS74 $T_a = -40$ °C $V_{CC} = 5.0$	to +85°C	$T_a = -55$ °C	AHCT to +125°C )V ± 10%	Unit
			Тур	Min	Max	Min	Max	
Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pF	11		18		22	ns
Any input to Y	t <sub>PHL</sub>	OL-30pi	11		18		22	5
Input Capacitance	CIN		5					pF
Power Dissipation Capacitance*	C <sub>PD</sub>	(per gate)						рF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.



- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:

 $I_{OL} = 8$  mA @  $V_{OL} = 0.5$ V

- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
   KSZANHOT: -40°C to 1.85°C

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### DESCRIPTION

The '51 performs the following Boolean functions:  $1Y = (1\overline{A} \circ 1B \circ 1C) + (1\overline{D} \circ 1E \circ 1F)$  $2Y = (2\overline{A} \circ 2B) + (2\overline{C} \circ 2D)$ 

The '58 performs: 1Y=(1A•1B•1C)+(1D•1E•1F) 2Y=(2A•2B)+(2C•2D)

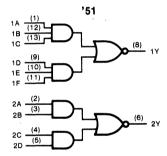
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### PIN CONFIGURATION



#### LOGIC DIAGRAMS

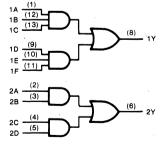


#### **FUNCTION TABLES**

		Output 1Y					
1A	1B	1C	1D	1E	1F	'51	'58
Н	Н	Н	Х	Х	Х	L	Н
Χ	Х	Х	Н	. н	н	L	Н
	Any	other o	ombina	ation		H	L

	Inp	Outp	ut 2Y		
2A	2B	2C	2D	'51	'58
Н	Н	X	χ.	L	Н
Χ	X	Н	Н	L	Н
An	y other c	combination	on	ŀН	L

#### '58



Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_I < -0.5V \text{ or } V_I > V_{CC} +0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_0 < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

### **Recommended Operating Conditions**

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

### DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	= 25°C	KS74AHCT $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	<b>v</b> .
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

### AC ELECTRICAL CHARACTERISTICS (Input tr, tr≤2 ns), AHCT51, AHCT58

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	$T_a = -40^{\circ}$	AHCT C to +85°C OV ± 10%	$T_a = -55^{\circ}$	IAHCT C to +125°C DV ± 10%	Unit
			Тур	Min	Max	Min	Max *	
Propagation Delay	t <sub>PLH</sub>	C <sub>L</sub> =50pF	9		15		18	ns
Topagation Delay	tpHL	J CL JODI	9		15		18	] 113
Input Capacitance	Cin	-	5					рF
Power Dissipation Capacitance*	C <sub>PD</sub>	(per gate)	15					рF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.



- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
   I<sub>OL</sub> = 8 mA @ V<sub>OL</sub> = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### **DESCRIPTION**

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at  $\overline{\text{CLR}}$  input resets the outputs regardless of the levels of the other inputs. When  $\overline{\text{CLR}}$  is inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

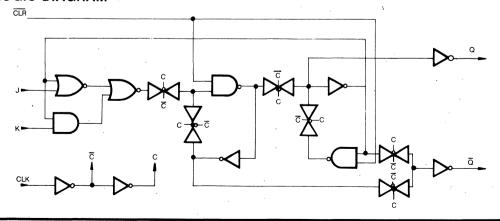
#### PIN CONFIGURATION

#### 

#### **FUNCTION TABLE**

	Input	s		Outp	outs
CLR	CLK	J	K	Q	ā
L	X	×	Х	L	Н
H	<b>↓</b>	L	L	Q <sub>o</sub>	$\overline{Q}_{o}$
Н	↓ .	Н	L	н	L
н	<b>↓</b>	L	Н	L	Н
Н	<b>↓</b>	Н	н	TOG	GLE_
Н	Н	Х	Х	Q <sub>o</sub>	$\bar{Q}_{\scriptscriptstyle{0}}$

#### LOGIC DIAGRAM





Supply Voltage Range $V_{CC}$ , $-0.5V$ to $+7V$
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW

Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

### **Recommended Operating Conditions**

Supply Voltage, Vcc .			4.5V	to 5	5.5V
DC Input & Output Volt	ages*, V <sub>IN</sub> ,	$V_{\text{OUT}}$	0	√ to	$v_{cc}$
Operating Temperature					

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . Max 500 ns

 Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

#### DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Symbol Test Conditions		ymbol Test Conditions		a = 25°C	KS74AHCT $T_{a} = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		its				
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	v		
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧		
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-4m A$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> -0.1 3.7	v		
Maximum Low-Level Output Voltage	1 '	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v		
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ		
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		4.0	40.0	80.0	μΑ		
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA		

### AC ELECTRICAL CHARACTERISTICS (Input tr, tr <2 ns), AHCT73

Characteristic		Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	-		KS54. T <sub>a</sub> = -55°C V <sub>CC</sub> = 5.0	to +125°C	Unit
				Тур	· Min	Max	Min	Max	
Maximum Clock Fr	equency	f <sub>max</sub>		45	30		25		MHz
Propagation Delay,		tpLH		10		17		20	ns
CLK to Q or Q		t <sub>PHL</sub>	C <sub>L</sub> =50pF	10		17		20	"
Propagation Delay,		tpLH		, 10		17		20	ns
CLR to Q or Q	*	t <sub>PHL</sub>		10		17		20	113
Setup Time	J or K	t <sub>su</sub>		8	13		15		ns
before CLK↓	CLR Inactive	เรน		- 8	13		15		113
Hold Time, J or K	after CLK↓	th		3	0		0		ns
Pulse Width	CLK High or Low	t <sub>w</sub>		8	13		15		ns
Puise Width	CLR Low	'w		8	13		15		113
Input Capacitance		CIN		5	}				рF
Power Dissipation	Capacitance*	C <sub>PD</sub>	(per flip-flop)	40				4	рF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} \ V_{CC}^2 \ f + I_{CC} \ V_{CC}$ .
† For AC switching test circuits and timing waveforms see section 2.

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
   I<sub>OL</sub> = 8 mA @ V<sub>OL</sub> = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

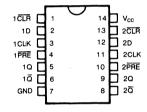
### **DESCRIPTION**

These devices contain two independent positive-edge-triggered D-type flip-flops. Each flip-flop has its own data, clock, preset and clear inputs and complementary Q and  $\overline{Q}$  outputs. The preset and clear inputs are active-low and operate independently of the clock. Data at the D input is transferred to the Q outputs on the positive transition of the clock, provided setup requirements have been met.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{\text{CC}}$  and ground.

#### PIN CONFIGURATION

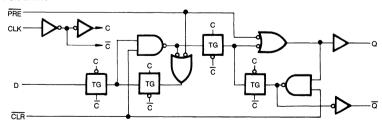


#### **FUNCTION TABLE**

	Inpu	its		Ou	tputs
PRE	CLR	CLK	D	Q	ā
Ŀ	Н	X	Х	Н	L
Н	L	Х	Х	L	Н
L	L	Χ	X	Н*	H*
Н	Н	<b>↑</b>	н	Н	L
· H	Н	<b>↑</b>	L	L	Н
Н	Н	L	Х	No C	hange
Н	Н	Н	X	No CI	hange
Н	Η,	<b>↓</b>	Х	No Cl	hange

\*Both outputs will remain high as long as PRE and CLR are low, but the output states are unpredictable if PRE and CLR go high simultaneously.

### LOGIC DIAGRAM



# Dual D-Type Positive-Edge-Triggered Flip-Flops with Preset and Clear

### **Absolute Maximum Ratings\***

Supply Voltage Range $V_{CC}, \ldots, -0.5V$ to $+7V$
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5 \text{V.or } V_1 > V_{CC} + 0.5 \text{V}) + \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_0 < V_{CC} + 0.5V) + \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> /65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.

These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

### **Recommended Operating Conditions**

Supply Voltage, V <sub>CC</sub>	4.5V	to 5.5\
DC Input & Output Voltages*, VIN, VOUT	0\	to Vcc
Operating Temperature		

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . Max 500 ns

 Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

### DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	a = 25°C	KS74AHCT T <sub>a</sub> = -40°C to +85°C	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	<b>v</b>
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> -0.1 3.84	V <sub>CC</sub> -0.1	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input . Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		4.0	40.0	80.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

### AC ELECTRICAL CHARACTERISTICS (Input tr, tre2 ns), AHCT74

Characteristic		1 ' 1 ;		T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	= = ADYC TO + 85YC		KS54AHCT T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> =5.0V ± 10%		Unit
				Тур	Min	Max	Min	Max	
Maximum Clock I	Frequency	f <sub>max</sub>		55	34		30		MHz
Propagation Dela	у,	tpLH		10		17		20	ns
CLK to Q or Q		t <sub>PHL</sub>	C <sub>L</sub> =50pF	10		17		20	ns
Propagation Delay,		t <sub>PLH</sub>		9		15		18	
PRE or CLR to C		t <sub>PHL</sub>		9		15		18	] " 3
Setup Time	Data	t <sub>su</sub>		7	12		15		ns
before CLK1	PRE or CLR Inactive	<sup>L</sup> Su		5	8		10		113
Hold Time, Data	after CLK1	th		-3	0		0		ns
Pulse Width	CLK High or Low		,	9	15		17		
Puise Width	PRE or CLR Low	tw		9	15		17		ns
Input Capacitance		CIN		5					pF
Power Dissipation	n Capacitance*	C <sub>PD</sub>							pF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
   I<sub>OL</sub> = 8mA @ V<sub>OL</sub> = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
   (C744) (C744)

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### DESCRIPTION

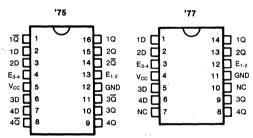
The '75 and '77 consist of 4 high-speed D-type latches that can be used as temporary storage for binary information between processing units. The '75 features complementary Q and  $\overline{Q}$  output while the '77 features single nail output. These devices are ideal for high component density application.

The latches are transparent: when the enable (E) is high, the Q output will follow the data input. When the enable goes low, the output latches at the level that was set up at the D-input.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### PIN CONFIGURATION

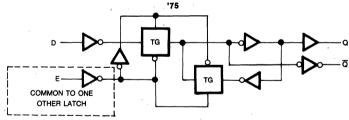


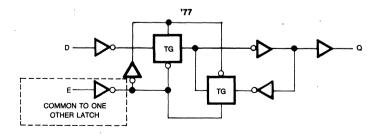
#### **FUNCTION TABLE**

Inputs		Outputs			
D	E	α	Q*		
L	Н	L	Н		
Н	Н	Н	L		
X	L	Qo	$\overline{\overline{\mathbf{Q}}}_{0}$		

\*Q: '75 only

### LOGIC DIAGRAM





Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_0 < V_{CC} + 0.5V)$ ±35 mA
Continuous Current Through
Vcc or GND pins ±125 mA
Storage Temperature Range, $T_{stg} \dots -65$ °C to $+150$ °C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Patings are those values beyond

<sup>\*</sup> Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

### **Recommended Operating Conditions**

	•	- ,	
Supply Voltage, V <sub>CC</sub>			4.5V to 5.5V
DC Input & Output V	oltages*, V <sub>IN</sub>	, V <sub>OUT</sub>	OV to V <sub>CC</sub>
Operating Temperatu	re ·		

Range KS74AHCT: -40°C to +85°C
KS54AHCT: -55°C to +125°C
Input Rise & Fall Times, t<sub>r</sub>, t<sub>t</sub> . . . . . . . . Max 500 ns

 Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

### DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	Т,	<sub>a</sub> = 25°C	KS74AHCT T <sub>a</sub> = -40°C to +85°C	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	, V
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-4m A$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> -0.1 3.84	V <sub>CC</sub> −0.1 . 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input in V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

### AC ELECTRICAL CHARACTERISTICS (Input tr. tres 2 ns), AHCT75

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V			KS54AHCT T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%		Unit
			Тур	Min	Max	Min	Max	
Propagation Delay	tpLH	C <sub>I</sub> = 50pF	10		16		20	ns
E to Q or Q	t <sub>PHL</sub>	OL OOD!	10		. 16		20	
Propagation Delay	tpLH	C <sub>L</sub> =50pF	9		15		18	ns
D to Q or Q	tpHL		9		15		18	
Data Set up Time D to Enable	tsu		6	10		12		ns
Data Hold Time Enable to D	th		3		5		6	ns
Input Capacitance	CiN		5					рF
Power disipation Capacitance*	C <sub>PD</sub>						1	рF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

### AC ELECTRICAL CHARACTERISTICS (Input tr. tr 2 ns), AHCT77

Characteristic	Symbol	Conditions <sup>†</sup>	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V			KS54AHCT $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Тур	Min	Max	Min	Max	
Propagation Delay	t <sub>PLH</sub>	C <sub>1</sub> = 50pF	8		14		17	ns
E to Q	t <sub>PHL</sub>	OL COP!	8		14		17	
Propagation Delay	tpLH	C <sub>L</sub> =50pF	8		13		15	ns
D to Q	tpHL	OL-30bi	8		13		15	
Data Set up Time D to Enable	tsu		6	10		12		ns
Data Hold Time Enable to D	th		3		5		6	ns
Input Capacitance	CIN		5					pF
Power disipation Capacitance*	C <sub>PD</sub>							pF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

For AC switching test circuits and timing waveforms see section 2.

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs: I<sub>OL</sub> = 8 mA @ V<sub>OL</sub> = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

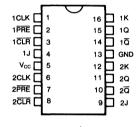
#### DESCRIPTION

These parts consist of two negative-edge-triggered J-K flip-flops with independent J, K, preset, clear and clock inputs and complementary outputs. The J-K inputs at each flip-flop are enabled when the clock goes high. The input data are transferred to the outputs on the negative-going edge of the clock pulse, provided the setup requirements have been met.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{\text{CC}}$  and ground.

#### PIN CONFIGURATION

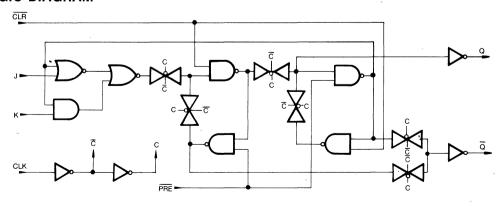


#### **FUNCTION TABLE**

	Inputs					Outputs		
PRE	CLR	CLK	J	K	Q	ā		
L	Н	Х	Х	Х	Н	L		
Н	L	X	Х	Х	L	Н		
L	L	Х	Х	Х	Н*	Н*		
н	н	<b>↓</b>	L	L	Q <sub>o</sub>	$\overline{Q}_{o}$		
Н	н	<b>↓</b>	н	L	н	L		
н	н	<b>↓</b>	L	н	L	Н		
н	н	<b>↓</b>	Н	н	TOGGLE			
н	Н	Н	X	Х	Q <sub>o</sub>	Q₀		

<sup>\*</sup>Both outputs will remain high as long as preset and clear are low, but the output states are unpredictable if preset and clear go high simultaneously.

#### LOGIC DIAGRAM



<sup>\*</sup> Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Supply Voltage, V<sub>CC</sub> . . . . . . . . . . . . . . . . . 4.5V to 5.5V DC Input & Output Voltages\*, V<sub>IN</sub>, V<sub>OUT</sub> . . OV to V<sub>CC</sub> Operating Temperature

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . Max 500 ns

 Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

Characteristic	Symbol	Test Conditions	T <sub>a</sub> = 25°C		KS74AHCT T <sub>a</sub> = -40°C to +85°C	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-4m A$	Vcc 4.2	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> -0.1	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND	,	±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		4.0	40.0	80.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin  V <sub>I</sub> =2.4V  other Inputs: at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0µA		2.7	2.9	3.0	mA

# KS54AHCT **76**

# AC ELECTRICAL CHARACTERISTICS (Input tr, tr<2 ns), AHCT76

Characteristic		Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	$ T_a = 25^{\circ}C \\ V_{CC} = 5.0V \\ T_a = -40^{\circ}C \text{ to } +85^{\circ}C \\ V_{CC} = 5.0V \pm 10^{\circ} $		KS54 T <sub>a</sub> = -55°C V <sub>CC</sub> = 5.0	Unit	
				Тур	Min	Max	Min	Max	
Maximum Clock F	requency	f <sub>max</sub>		45	30		25		MHz
Propagation Delay	',	tpLH		10		17		20	ns
CLK to Q or Q		t <sub>PHL</sub>	C <sub>L</sub> =50pF	10		17		20	'''
Propagation Delay,		tpLH		10		17		20	ns
PRE or CLR to Q		t <sub>PHL</sub>		10	17		20		113
Setup Time	J or K	t <sub>su</sub>		10	.17		20		ns
before CLK↓	PRE or CLR Inactive	'su		10	17		20		1115
Hold Time, Data a	fter CLK↓	th		-3	0		0		ns
Pulse Width	CLK High or Low			8	13		15		
ruise width	PRE or CLR Low	tw		8	13		15		ns
Input Capacitance		CiN		5			,		pF
Power Dissipation Capacitance*		C <sub>PD</sub>	(per flip-flop)	40					pF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

# Dual J-K Flip-Flops with Preset, Common Clear & Common Clock

#### **FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
- I<sub>OL</sub> = 8 mA @ V<sub>OL</sub> = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges: KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

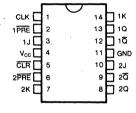
#### **DESCRIPTION**

These parts consist of two negative-edge-triggered J-K flip-flops with independent J, K and preset inputs and complementary outputs. The clear and clock inputs are common to both flip-flops. The J-K inputs are enabled when the clock goes high. The input data are transferred to the outputs on the negative-going edge of the clock pulse, provided the setup requirements have been met.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### PIN CONFIGURATION

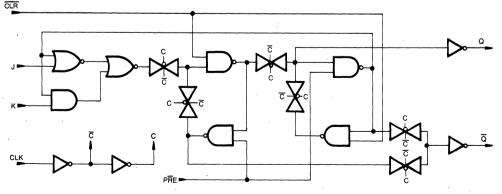


#### **FUNCTION TABLE**

	11	nputs			Outp	outs
PRE	CLR	CLK	J	K	Q	Q
L	Н	Х	X	Х	Н	L
Н	L	Х	X	X	L	н
L	L	Χ	X	X	H*	H*
E H	н	<b>↓</b>	L	L	. Oº	Ō₀
Н	н	į.	н	L	н	L
Н	н	<b>↓</b>	L	Н	L	Н
Н	Н	<b>↓</b>	Н	Н	TOG	GLE
Н	н	н	Χ	Χ	Q <sub>o</sub>	Q₀

\*Both outputs will remain high as long as preset and clear are low, but the output states are unpredictable if preset and clear go high simultaneously.

# LOGIC DIAGRAM



Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_0 < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Supply Voltage, V<sub>CC</sub> . . . . . . . . . . . . . . . . 4.5V to 5.5V DC Input & Output Voltages\*, V<sub>IN</sub>, V<sub>OUT</sub> . . OV to V<sub>CC</sub> Operating Temperature

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . Max 500 ns

 Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

Characteristic	Symbol	Test Conditions	Т,	<sub>a</sub> = 25°C	KS74AHCT T <sub>a</sub> = -40°C to +85°C	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V <sub>ОН</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> -0.1 3.84	V <sub>CC</sub> -0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> =20µA I <sub>O</sub> =4mA I <sub>O</sub> =8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		4.0	40.0	80.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin  V <sub>I</sub> =2.4V  other Inputs:  at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0µA		2.7	2.9	3.0	mA

# AC ELECTRICAL CHARACTERISTICS (Input tr, ti-2 ns), AHCT78

Characteristic		Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V			KS54 T <sub>a</sub> = -55°C V <sub>CC</sub> = 5.0	Unit	
				Тур	Min	Max	.Min	Max	
Maximum Clock F	requency	f <sub>max</sub>		45	30		25		MHz
Propagation Delay	,	tpLH		10		17		20	ns
CLK to Q or Q		t <sub>PHL</sub>	C <sub>L</sub> =50pF	10		17		20	113
Propagation Delay,		tPLH		10		. 17		20	ns
PRE or CLR to Q	or Q	tenl		10		17		20	113
Setup Time	J or K	t <sub>su</sub>		10	17		20		ns
before CLK↓	PRE or CLR Inactive			10	17		20		115
Hold Time, J or K	after CLK↓	th		-3	0		0		ns
Pulse Width	CLK High or Low			8	13		15		ns
Fuise Width	PRE or CLR Low	tw		8	13		15		
Input Capacitance		CiN		5					pF
Power Dissipation	Capacitance*	C <sub>PD</sub>	(per flip-flop)	40					рF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

For AC switching test circuits and timing waveforms see section 2.

#### **FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:

and CMOS devices

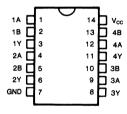
- I<sub>OL</sub> = 8 mA @ V<sub>OL</sub> = 0.5V
   Inputs and outputs interface directly with TTL, NMOS
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATION



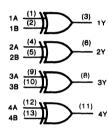
#### DESCRIPTION

These devices contain four independent 2-input Exclusive-OR gates. They perform the Boolean functions Y=A@B or Y=AB+AB.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{\rm CC}$  and ground.

#### LOGIC DIAGRAM



#### **FUNCTION TABLE**

(Each Gate)

Inp	uts	Output
A	В	Y
L	L	L
L	Н	Н
Н	L	н
Н	Н	L

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, IIK
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, I <sub>OK</sub>
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±35 mA
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW

<sup>\*</sup> Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Supply Voltage, \	/cc	4.	5V to 5.5V
DC Input & Output	ut Voltages*, V <sub>IN</sub> ,	V <sub>OUT</sub>	OV to Vcc
Operating Tempe	rature		
Range	KS74AHCT:	-40°C	to +85°C

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . . Max 500 ns

Characteristic	Symbol	Test Conditions	T,	a = 25°C	KS74AHCT T <sub>a</sub> = -40°C to +85°C	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
3.12.23.13.13	,		Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	v
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	V
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	О	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	l <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

 <sup>\*</sup> Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

# AC ELECTRICAL CHARACTERISTICS (Input tr, tr 42 ns), AHCT86

Characteristic	Symbol	Conditions <sup>†</sup>	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	KS74AHCT  T <sub>a</sub> = -40°C to +85°C  V <sub>CC</sub> = 5.0V ± 10%		$KS54AHCT$ $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$		Unit
	3		Тур	Min	Max	Min	Max	
Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pF	10 1		16		19	ns
A or B to Y (Other Input Low)	t <sub>PHL</sub>		10		16		19	
Propagation Delay, A or B to Y (Other Input High)	t <sub>PLH</sub>		12		20		24	
	t <sub>PHL</sub>		12		20		24	118
Input Capacitance	CiN		5					pF
Power Dissipation Capacitance*	C <sub>PD</sub>	(per flip-flop)	15					рF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

# Dual J-K Negative-Edge-Triggered Flip-Flops with Clear

#### **FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
   I<sub>OL</sub> = 8 mA @ V<sub>OL</sub> = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
   KS74AHCT: -40°C to +85°C
   KS54AHCT: -55°C to +125°C
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

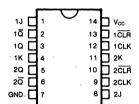
#### DESCRIPTION

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the  $\overline{\text{CLR}}$  input resets the outputs regardless of the levels of the other inputs. When  $\overline{\text{CLR}}$  is inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clarrips to  $V_{CC}$  and ground.

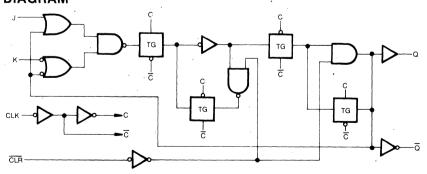
#### PIN CONFIGURATION



#### **FUNCTION TABLE**

	Input	Outp	outs		
CLR	CLK	J	K	Q	ā
L	Х	Х	Х	L	Н
Н	<b>↓</b>	L	L	Q,	죠。
Н	<b>1</b>	Н	L	H	L
Н	<b>↓</b>	L	Н	L	.H
Н	<b>+</b>	Н	Н	TOG	GLE
Н	Н	Х	Х	Qo	<b>Q</b> ₀

#### LOGIC DIAGRAM



Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20_{\text{L}} \text{mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissination Per Package Put 500 mW

# **Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . . . . . . 4.5V to 5.5V DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . OV to  $V_{CC}$  Operating Temperature

Range KS74AHCT:  $-40^{\circ}$ C to  $+85^{\circ}$ C KS54AHCT:  $-55^{\circ}$ C to  $+125^{\circ}$ C Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . . Max 500 ns

Characteristic	Symbol	Test Conditions	T,	a = 25°C	KS74AHCT T <sub>a</sub> = -40°C to +85°C	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	v
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> -0.1	v
Maximum Low-Level Output Voltage	VoL	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> =20µA I <sub>O</sub> =4mA I <sub>O</sub> =8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	l <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		4.0	40.0	80.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	.3.0	mA

<sup>†</sup> Power Dissipation temperature derating: Fiastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

 <sup>\*</sup> Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

# Dual J-K Negative-Edge-Triggered Flip-Flops with Clear

# AC ELECTRICAL CHARACTERISTICS (Input t<sub>r</sub>, t<sub>f</sub>≤2 ns), AHCT107

Characteristic		Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	Ta = -40°C	AHCT c to +85°C 0V±10%	Ta = -55°C	AHCT to +125°C V± 10%	Unit	
				Тур	Min	Max	Min -	Max .		
Maximum Clock F	equency	f <sub>max</sub>		45 🔉	30	30	25		MHz	
Propagation Delay	,	tpLH		10	-	17		20	ns	
CLK to Q or Q		tpHL	C <sub>L</sub> =50pF	10	-	17		20	ns	
Propagation Delay,		tplH		10		17		20		
CLR to Q or Q		tpHL		10		17		20	110	
Setup Time	J or K	tsu	10	17		20		ns		
before CLK↓	CLR Inactive	'su		10	17	.,	20		] ''3	
Hold Time, J or K after CLK↓		th		-3	0		0		ns	
Pulse Width CLK High or Low				8	13		15			
ruise width	CLR Low	tw		8	13		15		ns	
Input Capacitance		CiN		. 5					pF	
Power Dissipation	Capacitance*	CPD	(per flip-flop)	40					pF	

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

#### **FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
  - I<sub>OL</sub> = 8 mA @ V<sub>OL</sub> = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

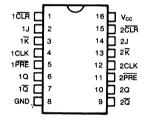
#### DESCRIPTION

These devices contain two positive-edge-triggered  $J\cdot\overline{K}$  flipflops with independent preset and clear inputs and complementary Q and  $\overline{Q}$  outputs. The present and clear inputs are active-low and operate independently of the clock Data at the J and  $\overline{K}$  inputs are transferred to the ouptuts on the positive transition of the clock provided setup requirements have been met. These versatile flip-flops can perform as toggel flip-flops by grounding K and tying J high. They can also perform as D-type flops if J and  $\overline{K}$  are tied together.

These devices provide speeds and drive capability equivalent to their ALST, '- counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### PIN CONFIGURATION

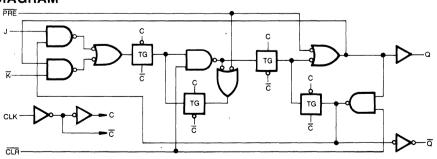


#### **FUNCTION TABLE**

	Inputs							
PRE	CLR	CLK	J	ĸ	Q	ā		
L	Ĥ	Х	Х	Х	Н	L		
Н	L	X	Х	Х	L	Н		
L	. L 1	Х	Χ	Χ	H*	Н*		
H	Н	<b>†</b>	L	L	L	Н		
H	Н	<b>†</b>	Н	L	TOG	GLE		
Н	Н	<b>†</b>	L	Н	Q <sub>o</sub>	ā,		
Н	Н	<b>†</b>	Н	Н	Н	L		
Н	Н	L	Χ	Χ	Q <sub>o</sub>	ā₀		

\*Both outputs will remain high as long as  $\overrightarrow{PRE}$  and  $\overrightarrow{CLR}$  are low, but the output states are unpredictable if  $\overrightarrow{PRE}$  and  $\overrightarrow{CLR}$  go high simultaneously.

#### LOGIC DIAGRAM



Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, I <sub>OK</sub>
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-
posure to these conditions may affect device reliability

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Supply Voltage,	V <sub>CC</sub>	4.	5V to 5.5V
DC Input & Outp	ut Voltages*, V <sub>IN</sub> ,	Vout	OV to Vcc
Operating Tempe	erature		
Range	KS74AHCT:	-40°C	to +85°C

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

Characteristic	Symbol	Test Conditions		a = 25°C	KS74AHCT T <sub>a</sub> = -40°C to +85°C	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	v
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	IIN	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		4.0	40.0	80.0	μА
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0µA		2.7	2.9	3.0	mA

# AC ELECTRICAL CHARACTERISTICS (Input tr., tr <2 ns), AHCT109

Characteristic		Symbol Conditions		T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	Ta = -40°0	AHCT C to +85°C DV ±10%	Ta = - 55°C	AHCT to +125°C V ± 10%	Unit
				Тур	. Min	Max	Min	Max	
Maximum Clock	Frequency	f <sub>max</sub>		55	34	34	30		MHz
Propagation Dela	у,	tpLH		10		17		20	ns
CLK to Q or Q		t <sub>PHL</sub>	C <sub>L</sub> =50pF	10		17		20	
Propagation Delay,		tplH		10		17		20	ns
PRE or CLR to C	or Q	t <sub>PHL</sub>		10		17		20	
Setup Time	Data	t <sub>su</sub>		7	12		15		ns
before CLK1	PRE or CLR Inactive			5	8		10		1115
Hold Time, Data	after CLK†	th		-3	0		0	1	ns
Pulse Width	CLK High or Low			9	15		17	1	ns
ruise Width	PRE or CLR Low	tw		9	15		17		1115
Input Capacitance		C <sub>IN</sub>		5					pF
Power Dissipation	n Capacitance*	C <sub>PD</sub>							pF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

#### **FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  $I_{OL} = 8$  mA @  $V_{OL} = 0.5$ V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
   KS74AHCT: -40°C to +85°C
   KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

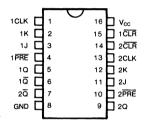
#### DESCRIPTION

These parts consist of two negative-edge-triggered J-K flipflops with independent J, K, preset, clear and clock inputs and complementary outputs. The J-K inputs at each flipflop are enabled when the clock goes high. The input data are transferred to the outputs on the negative-going edge of the clock pulse, provided the setup requirements have been met.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground

#### PIN CONFIGURATION

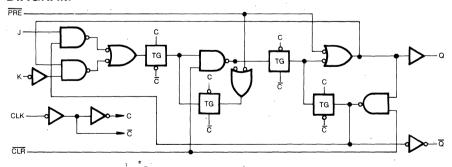


#### **FUNCTION TABLE**

	Out	outs				
PRE	CLR	CLK	J	K	Q	ā
L	Н	X	Х	Х	Н	L
Н	L	Χ	Х	Х	L	Н
L	Ľ	Х	Х	Х	H*	H*
н	н	1	`L	L	Q <sub>o</sub>	Q.
н	Н	<b>↓</b>	Н	L	н	L
н	н	<b>↓</b>	L	н	L	Н
Н	Н	<b>↓</b>	A	Н	TOG	GLE ·
Н	Н	Н	X	Χ	Q <sub>o</sub>	<b>Q</b> ₀

\*Both outputs will remain high as long as  $\overline{PRE}$  and  $\overline{CLR}$  are low, but the output states are unpredictable if  $\overline{PRE}$  and  $\overline{CLR}$  go high simultaneously.

#### LOGIC DIAGRAM



posure to these conditions may affect device reliability.

# **Recommended Operating Conditions**

Supply Voltage, V <sub>CC</sub>	4.5V to 5.5V
DC Input & Output Voltages*, V <sub>IN</sub> , V <sub>OUT</sub>	OV to V <sub>CC</sub>
Operating Temperature	

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . . Max 500 ns

 Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

Characteristic	Symbol	Test Conditions	Т	a = 25°C	KS74AHCT T <sub>a</sub> = -40°C to +85°C	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit	
			Тур		Guaranteed Lim	its	1	
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	<	
Maximum Low-Level Input Voltage	VIL	·		0.8	0.8	0.8	٧	
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> -0.1 3.7	<b>v</b>	
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1	v	
Maximum Input Current	l <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ	
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		4.0	40.0	80.0	μΑ	
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA	

<sup>†</sup> Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# AC ELECTRICAL CHARACTERISTICS (Input tr, tr <2 ns), AHCT112

Characteristic		Symbol	Conditions <sup>†</sup>	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	$T_a = -40^{\circ}$	AHCT C to +85°C DV ± 10%	KS54 T <sub>a</sub> = - 55°C V <sub>CC</sub> = 5.0	Unit	
			+	Тур	Min	Max	Min	Max.	
Maximum Clock F	requency	f <sub>max</sub>		50 ·	30		25	,	MHz
Propagation Delay	/,	tpLH		10		17		20	ns
CLK to Q or Q		t <sub>PHL</sub>	C <sub>L</sub> =50pF	10	7	17		20	113
Propagation Delay,		tpLH		10		17		20	ns
PRE or CLR to Q	or Q	t <sub>PHL</sub>		10		17		20	7 113
Setup Time	J or K	tsu		10	17		20		ns
before CLK↓	PRE or CLR Inactive	I ISU		-10	17		20		113
Hold Time, Data a	after CLK↓	th		-3	0		0		ns
Pulse Width	CLK High or Low	_		10	17		20		ns
Puise Width	PRE or CLR Low	t <sub>w</sub>	٠.	6	10		15		118
Input Capacitance		CiN		5					pF
Power Dissipation Capacitance*		C <sub>PD</sub>	(per flip-flop)	40					pF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation:  $P_D = C_{PD} \ V_{CC}^2 \ f + I_{CC} \ V_{CC}$ .
† For AC switching test circuits and timing waveforms see section 2.

# KS54AHCT **121** KS74AHCT

# Monostable Multibrators with Schmitt-Trigger Inputs

**Preliminary Specifications** 

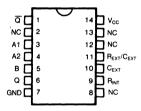
#### **FEATURES**

- Schmitt-trigger for slow Input transitions
- Internal timing resistor
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs: io. = 8 mA @ Vol = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range; 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATION



#### **FUNCTION TABLE**

	Inputs	Outputs			
A1	A2	В	Q	ā	
L	Х	X	L	H	
×	L	Н	L	Н	
×	X	L	L	Н	
Н	Н	X	L	Н	
Н	\ ↓	Н	Л.	L	
↓ ↓	Н	Н	$\int$	L L	
- 1	1	Н	л	. T	
L	×	1	Л	T.	
X	L	1	л	L	

H= HIGH Voltage level

L= LOW voltage level

X= Don't care

↑= LOW-to-HIGH transition

↓= HIGH-to-LOW transition

□ = one LOW level output pulse

#### DESCRIPTION

These multivibrators feature dual negative-transitiontriggered inputs and a single positive-transition-triggered input which can be used as an inhibit input. Complementary output pulses are provided.

Pulse triggering occurs at particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry for the B input allows jitterfree triggering from inputs with transition rates as slow as 1 volt/second, providing the circuit with excellent noise immunity.

Once fired, the outputs are independent of further transitions of the inputs and are a function only of the timing components. Input pulses may be of any duration relative to the output pulse. Output pulse length may be varied from 40 nanoseconds to 28 seconds by choosing appropriate timing components. With no external timing components (i.e., R<sub>INT</sub> connected to V<sub>CC</sub>, C<sub>EXT</sub> and C<sub>EXT</sub>/C<sub>EXT</sub> open), an output pulse of typically 30 or 35 nanoseconds is achieved which may be used as a d-c triggered reset signal.

Pulse width stability is achieved through internal compensation and is virtually independent of V<sub>CC</sub> and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

Jitter-free operation is maintained over the full temperature and  $V_{CC}$  ranges for more than six decades of timing capacitance (10 pF to  $10\mu F)$  and more than one decade of timing resistance (2 k $\Omega$  to 40 k $\Omega)$ . Throughout these ranges, pulse width is defined by the relationship  $t_{w(out)} = C_{EXT}R_{EXT}\ ln = 0.7\ C_{EXT}\ R_{EXT}$ . In circuits where pulse cutoff is not critical, timing capacitance up to  $1000\mu F$  and timing resistance as low as  $1.4\ k\Omega$  may be used. Also, the range of jitter-free output pulse widths is extended if  $V_{CC}$  is held to 5 volts and free-air temperature is  $25^{\circ}$  C. Duty cycles as high as 90% are achieved when using maximum recommended  $R_{EXT}$ . Higher duty cycles are available if a certain amount of pulse-width jitter is allowed.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts any yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

# Monostable Multibrators with Schmitt-Trigger Inputs

# A1 (4) (5) (6) Q (1). Q

- Notes: 1. An external capacitor may be connected between CEXT (positive) and REXT/CEXT.
  - To use the internal timing resistor, connect R<sub>INT</sub> to V<sub>CC</sub>. For Improved pulse width accuracy and repeatability connect on external resistor between R<sub>EXT</sub>/C<sub>EXT</sub> V<sub>CC</sub> with R<sub>INT</sub> opencircuited.

Range

# **Absolute Maximum Ratings\***

† Power Dissipation temperature derating: Plastic Package(N): -12mW/°C from 65°C to 85°C Ceramic Package(J): -12mW/°Cfrom100°C to 125°C

# **Recommended Operating Conditions**

Supply Voltage, Vcc	4.5V	to 5.5V
DC Input & Output Voltages*, VIN, VOUT	۰۰۰۰ ۵۱	√ to V <sub>CC</sub>
Operating Temperature		

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

Characteristic	Symbol	Test Conditions	Т	<sub>a</sub> = 25°C	KS74AHCT $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	liN	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	Icc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	-80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input in V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA



# AC ELECTRICAL CHARACTERISTICS (Input tr., tr 42 ns), AHCT121

Characteristic	Symbol	Conditions <sup>†</sup>	$T_a = 25^{\circ}C$ $V_{CC} = 5.0V$		KS74AHCT T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%		KS54AHCT  T <sub>8</sub> = -55°C to +125°C  V <sub>CC</sub> = 5.0V ± 10%		
			Тур	Min	Max	Min	Max		
Propagation Delay	t <sub>PLH</sub>	C <sub>1</sub> = 50pF	40		54		65	ns	
A, B to Q, Q	t <sub>PHL</sub>	C <sub>ext</sub> =80pF	40		54		65		
Propagation Delay	t <sub>PLH</sub>	R <sub>int</sub> to V <sub>CC</sub>	30		43		51	ns	
B to Q & Q output	t <sub>PHL</sub>		30		43		51	""	
Minimum Output pulse width	t <sub>w</sub>	C <sub>ext</sub> =0pF R <sub>int</sub> to V <sub>CC</sub>	35		52		52	ns	
		C <sub>ext</sub> =80pF R <sub>int</sub> to V <sub>CC</sub>	110	67	156	67	156	ns	
Output pulse width	tw	C <sub>ext</sub> =100pF R <sub>ext</sub> =10kΩ	700	602	798	595	805	ns	
		$C_{\text{ext}} = 1 \mu F$ $R_{\text{ext}} = 10 k \Omega$	7	6	8	5.9	8.1	ms	
Minimum input pulse width to trigger	t <sub>w</sub>			40		40		ns	
External timing tesistor range	R <sub>ext</sub>		. 10	1.4	40	1.4	40	kΩ	
External timing capacitance range	C <sub>ext</sub>			0	1,000	0	1,000	μF	
Output Duty cycle		$R_{ext} = 2k\Omega$			67		67	%	
Catput Daty Cycle		R <sub>ext</sub> =R <sub>ext(max)</sub>			90		90	%	
Input Capacitance	Cin								
Power dissipation Capacitance	C <sub>PD</sub>								

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

# Dual Retriggerable Monostable Multivibrator with Clear

Preliminary Specifications

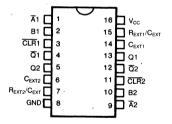
#### **FEATURES**

- Simple pulse width formula tw = 0.45RC
- . DC triggered from active HIGH or active Low inputs
- Retriggerable for very long output pulses up to 100% duty cycle
- . Overriding clear terminates output pulse
- Schmitt trigger A & B inputs allow infinite rise and fall times on these inputs
- Functions, pin-out, speed and drive compativility with 54/74ALS logic family
- . Low power consumption characteristic of CMOS
- High drive current outputs: I<sub>OL</sub> = 8mA @ V<sub>OL</sub> = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range; 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATION



#### **DESCRIPTION**

The '123 contains dual retriggerable monostable multivibrators with output pulse width control by three methods.

The basic pulse time is programmed by selection of an external resistor (Rext) and capacitor (Cext). The external resistor and capacitor are normally connected as shown timing component.

Once triggered, the basic output pulse width may be extended by retriggering the gated active Low going edge input (Ai) or the active HIGH going edge input (Bi). By repeating this process, the output pulse period (nQ=HIGH, nQ=LOW) can be made as long as desired. Alternatively an output delay can be terminated at any time by a Lowgoing edge on input CLR, which also inhibits the triggering. An internal connection from CLR to the input gates makes it possible to trigger the circuit by a positive-going signal at input CLR as shown in the function table when CEXT>10nF, the typical output pulse width is defined as; tw=0.45×REXT $\times$ CEXT(typ).

Where  $t_w$  is in seconds. R is in ohm. and C is in fards. All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### **FUNCTION TABLE**

	Inputs	Outputs			
CLR	Ā	В	Q	ā	
L	Х	Х	L	Н	
X	Н	X	L	Н	
X	X	L	L'	Н	
Н	L	1	Л	U	
Н	↓	Н	Л	L	
1	L	Н	л	ĹŢ	

H= HIGH voltage level

L= LOW voltage level

X= don't care

↑= LOW to HIGH transition

↓= HIGH to LOW transition

Π= one HIGH level output pulse

□ one LOW level output pulse

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
(V <sub>1</sub> <-0.5V or V <sub>4</sub> >V <sub>CC</sub> +0.5V) ±20 mA
DC Output Diode Current, I <sub>Ok</sub>
(V <sub>O</sub> <-0.5V or V <sub>O</sub> >V <sub>CC</sub> +0.5V) ±20 mA
Continuous OUtput Current Per Pin, Io
(−0.5V <v<sub>0<v<sub>CC+0.5V) ±35 mA</v<sub></v<sub>
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> -65°C to +150°C
Power Dissipation Per Package, Pa† 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-
posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package(N): -12mW/°C from 65°C to 85°C Ceramic Package(J): -12mW/°Cfrom100°C to 125°C

# **Recommended Operating Conditions**

	e, V <sub>CC</sub>
Range	KS74AHCT: -40°C to +85°C
	KSEAAHOT -55°C to +125°C

Characteristic	Symbol	Test Conditions	1	a=25°C	KS74AHCT T <sub>a</sub> = -40°C to +85°C	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	VIH			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	VıL			0.8	0.B	0.8	v
Minimum High-Level Output Voltage	V <sub>OH</sub>	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> =-20µA I <sub>O</sub> =-4mA	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC,</sub> =0.1 3.7	v
Maximum Low-Level Output Voltage		V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> =20µA I <sub>O</sub> =4mA I <sub>O</sub> =8mA	o	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	In	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	icc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0µA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input in  V <sub>1</sub> =2.4V other tnputs: at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0 <sub>µ</sub> A		2.7	2.9	3.0	mA

# AC ELECTRICAL CHARACTERISTICS (Input tr, tre2 ns), AHCT123

Characteristic	Symbol	Conditions <sup>†</sup>	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	Ta = -40°	AHCT C to +85°C 0V±10%	KS54 T <sub>a</sub> = -55°C V <sub>CC</sub> = 5.0	Unit		
			Тур	Min	Max	Min	Max		
Propagation Delay	t <sub>PLH</sub>		18		33		39	ns	
A, B to Q, Q	t <sub>PHL</sub>	C <sub>L</sub> =50pF	18		33		39		
Propagation Delay	t <sub>PLH</sub>	C <sub>ext</sub> =0,	16		27		32	ns	
CLR to Q, Q	t <sub>PHL</sub>	$R_{ext} = 5k\Omega$	16		27		32	'''	
Output Pulse Width 1	twQ1		116		207		209	ns	
Output Pulse Width 2	t <sub>WQ2</sub>	$C_L$ =50pF $C_{ext}$ =1000pF $R_{ext}$ =10k $\Omega$	4.5	3.8	5.2	3.8	5.2	μS	
Trigger Pulse Width	t <sub>w</sub>	C <sub>L</sub> =50pF A <sub>i</sub> =LOW	5		16		20	ns	
Trigger Pulse Width	t <sub>w</sub>	C <sub>L</sub> =50pF B <sub>i</sub> =High	5		16		20	ns	
Clear Pulse Width	t <sub>w</sub>	C <sub>L</sub> =50pF CLR <sub>i</sub> =LOW	6		16		20	ns	
External Timing Resistance	R <sub>ext</sub>	,		2	1,000	. 2	1,000	kΩ	
External Timing Capacitance Cext				no restriction					
Input Capacitance	Cin		5					рF	
Power Dissipation Capacitance	C <sub>PD</sub>							рF	

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

# **Application Information**

The basic output pulse width is determined by the value of external capacitance and timing resistance. For output pulse widths greater than  $100\mu s$  or external capacitance greater than 1000pF the following equation should be used.

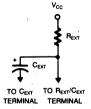
$$t_w = k \cdot R_{ext} \cdot C_{ext}$$

Where

 $t_W$  is in second K is the multiplying factor and is approximately 0.45 for  $C_{ext} \ge 1000 pF$   $C_{ext}$  is in F

For best results, system ground should be applied to the  $C_{\text{ext}}$  terminal. These devices do not require a switching diode in series with the  $R_{\text{ext}}/C_{\text{ext}}$  terminal (as required by some other monostable multivibrators)

#### **TIMING COMPONENT**



<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

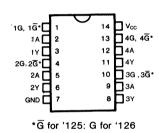
#### **FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- · 3-State outputs with drive current
- $(I_{OL} = 24 \text{ mA} Q V_{OL} = 0.5 \text{V})$  for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges: KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATION



#### **FUNCTION TABLES**

Output
Y
Н
L
Z

'126

Int	outs	Output							
A	G	Υ							
Н	Н	Н							
L	Н	L							
X	L	Z							

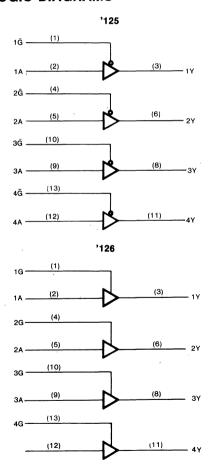
#### DESCRIPTION

These bus buffers feature four independent line drivers with 3-state outputs. The output enable functions for the '125 buffers are active-low, while those for '126 are active high.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{\text{CC}}$  and ground.

#### LOGIC DIAGRAMS



Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IoK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_0 < V_{CC} + 0.5V)$ ±70 mA
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, $T_{sig} \dots -65^{\circ}\text{C}$ to $+150^{\circ}\text{C}$
Power Dissipation Per Package, $P_d{}^\dagger$ 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-
posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Supply Voltage, V <sub>CC</sub>	4.5V to 5.5V
DC Input & Output Voltages*, VIN, VOUT	OV to Vcc
Operating Temperature	

 Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

Characteristic Symb		Symbol Test Conditions		a=25°C	KS74AHCT T <sub>a</sub> = -40°C to +85°C	KS54AHCT T <sub>a</sub> = -55°C to +125°C	
			Тур		Guaranteed Lim	its	1
Minimum High-Level Input Voltage	V#H			2.0	2.0	2.0	v
Maximum Low-Level Input Voltage	VIL			0.8	0.6	0.8	V
Minimum High-Level Output Voltage	V <sub>OH</sub>	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> =-20µA I <sub>O</sub> =-6mA	Vcc 4.2	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> =0.1 3.84	V <sub>CC</sub> −'0.1 3.7	v
Maximum Low-Level Output Voltage	1	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> =20µA I <sub>O</sub> =12mA I <sub>O</sub> =24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	4m	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>fH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μА
Maximum Quiescent Supply Current	icc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =OµA		8.0	80.0	160.0	μА
Additional Worst Case Supply Current		per input pin V <sub>I</sub> =2.4V other inputs: at V <sub>CC</sub> or GND tour=0µA		2.7	2.9	3.0	mΑ

# AC ELECTRICAL CHARACTERISTICS (Input tr, tr≤2 ns), AHCT125, AHCT126

Characteristic	Symbol	, Con	ditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	$T_a = -40^{\circ}$	AHCT C to +85°C OV±10%	KS54 T <sub>a</sub> = -55°C V <sub>CC</sub> =5.0	Unit	
					Min	Max	Min	Max	
Propagation Delay,	t <sub>PLH</sub>		C <sub>L</sub> =50pF C <sub>L</sub> =150pF			10 15		12 18	ns
A to Y	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150p		6 9		10 15		12 18	115
Output Enable Time	t <sub>PZH</sub>	Rı=1kΩ	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	11 14		18 23		22 28	ns
Enable to Y	t <sub>PZL</sub>		C <sub>L</sub> =50pF C <sub>L</sub> =150pF	11 14		18 23		22 28	113
Output Disable Time,	t <sub>PHZ</sub>	$R_L=1k\Omega$		13		18		22	ns
Enable to Y	tPLZ	C <sub>L</sub> =50pF	•	13		18		22	
Input Capacitance	CIN								рF
Output Capacitance	Cout	Output di	Output disabled						рF
Power Dissipation Capacitance* (per stage)	C <sub>PD</sub>	G or G=\ G.or G=0		5 30					pF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} \ V_{CC}^2 \ f + I_{CC} \ V_{CC}$ .

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

Preliminary Specifications

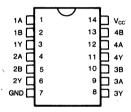
#### **FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
  - IoL = 8 mA @ VoL = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
   KEZANICT: 6090 Apr. 18590

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATION



#### DESCRIPTION

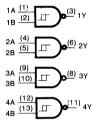
These Schmitt-trigger devices contain four independent NAND gates. They perform the Boolean function  $Y = \overline{A} \bullet \overline{B} = \overline{A} + \overline{B}$  in positive logic.

The input threshold levels are temperature compensated and can be triggered from the slowest of input ranges and still give jitter-free output signals.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### LOGIC DIAGRAM



#### **FUNCTION TABLE**

(Each Gate)

INP	UTS	OUTPUTS
A	В	. <b>Y</b>
L	L	Н
L	Н	Н
H	L	Н
Н	Η .	L

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

# DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T <sub>a</sub> = 25°C		KS74AHCT T <sub>a</sub> = -40°C to +85°C	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit		
			Typ Guaranteed Limits						
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-4mA$	VCC 4.2	V <sub>CC</sub> −0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> -0.11 3.7	v		
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 ' 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v		
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0 '	μΑ		
Maximum Quiescent Supply Current	1 Icc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.0	20.0	40.0	μΑ		
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA		

# DC ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions	T <sub>a</sub> =	25°C	KS74 T <sub>a</sub> = -40°	AHCT C to +85°C	KS54	IAHCT to +125°C	Uni
	- Cyllibor	1 est conditions	Min	Max	Min	Max	Min	Max	
Positive-Going	V <sub>T+</sub>	V <sub>CC</sub> =4.5V	1.2	1.9	1.2	1.9	1.2	1.9	V
Threshold Voltage	VI+	V <sub>CC</sub> =5.5V	1.4	2.1	1.4	2.1	1.4	2.1	1
Negative-Going	V <sub>T</sub> _	V <sub>CC</sub> =4.5V	0.5	1.2	0.5	1.2	0.5	1.2	v
Threshold Voltage		V <sub>CC</sub> =5.5V	0.6	1.4	0.6	1.4	0.6	1.4	1
Hysteresis .	VH	V <sub>CC</sub> =4.5V	0.4	1.4	0.4	1.4	0.4	1.4	v
$(V_{T+}-V_{T-})$	\ \frac{1}{2}	V <sub>CC</sub> =5.5V	0.4	1.5	0.4	1.5	0.4	1.5	1

# AC ELECTRICAL CHARACTERISTICS (Input tr, tre2 ns), AHCT132

Characteristic	Symbol	Conditions <sup>†</sup>	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	$T_a = -40^{\circ}$	AHCT C to +85°C DV ± 10%	$T_a = -55$ °C	IAHCT C to +125°C DV ± 10%	Unit
			Тур	Min	Max	Min	Max	
Propagation Delay,	t <sub>PLH</sub>	Cı =50pF	8		14		17	ns
Any input to Y	t <sub>PHL</sub>	OL-30bi	8		14		17	113
Input Capacitance	CIN		5					pF
Power Dissipation Capacitance*	C <sub>PD</sub>	(per gate)	15					рF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

#### 4

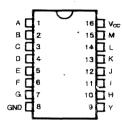
#### **FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- · Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
  - $I_{OL} = 8 \text{ mA } \textcircled{O} \text{ V}_{OL} = 0.5 \text{V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

# PIN CONFIGURATION



#### **FUNCTION TABLE**

INPUTS A THRU M	,	OUTPUT Y
All inputs	H	Ļ
One or more inputs	L	H

#### DESCRIPTION

The '133 contains a single 13-input NAND gate. It performs the boolean functions (in positive logic):

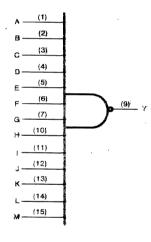
 $Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H \cdot I \cdot J \cdot K \cdot L \cdot M}$ 

 $Y = \tilde{A} + \tilde{B} + \tilde{C} + \tilde{D} + \tilde{E} + \tilde{F} + \tilde{G} + \tilde{H} + \tilde{I} + \tilde{J} + \tilde{K} + \tilde{L} + \tilde{M}$ 

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### LOGIC DIAGRAM



Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> −65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.

These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

# **Recommended Operating Conditions**

Supply Voltage,	Vcc	4	1.5V to 5.5V
DC Input & Outp	out Voltages*, V <sub>IN</sub> ,	Vout .	. OV to Vcc
Operating Temp	erature	j	
Pongo	KC74AHCT	-400	C to 185°C

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . Max 500 ns

\* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	mbol Test Conditions		bol Test Conditions		a = 25°C	$KS74AHCT$ $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
N		,	Тур		Guaranteed Lim	its			
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	v		
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v		
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1	V <sub>CC</sub> −0.1 3.7	v		
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v		
Maximum Input Current	lin	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ		
Maximum Quiescent Supply Current	Icc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.0	20.0	40.0	μΑ		
Additional Worst Case Supply Current	ΔΙςς	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA		

# AC ELECTRICAL CHARACTERISTICS (Input $t_r$ , $t_i \le 2$ ns), AHCT133

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	$T_a = -40^\circ$	AHCT C to +85°C 0V ± 10%	$T_a = -55$ °C	AHCT to +125°C V ± 10%	Unit
			Тур	Min	Max	Min	Max	7
Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pF	11		18		22-	ns
Any input to Y	tPHL		11		18		22	] "3
Input Capacitance	CIN		5					pF
Power Dissipation Capacitance*	C <sub>PD</sub>		·					pF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.



<sup>†</sup> Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

#### **FEATURES**

- Designed specifically for high-speed memory decoders and data transmission systems
- Incorporates 3 enable inputs to simplify cascading and/or data reception
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:

IoL = 8 mA @ VoL = 0.5V

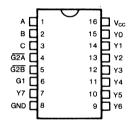
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATION



#### **FUNCTION TABLE**

	able outs	_	ele pu		Outputs							
G1	<u>G2</u> *	С	В	A	Y0	Y1	Y2	Υ3	Y4	<b>Y</b> 5	Y6	<b>Y7</b>
Х	Н	Х	Х	Х	Н	Н	Н	Н	Н	Н	Н	Н
L	Х	X	Х	Х	н	Н	Н	Н	Н	Н	Н	Н
Н	L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н
Н	L	L	L	Н	Н	L	Н	Н	Н	Н	Н	Н
Н	L	L	Н	L	Н	Н	L	Н	Н	Н	Н	Н
H	L	L	Н	Н	Н	Н	Н	L	Н	Н	Н	Н
Н	L	Н	L	L	Н	Н	Н	Н	L	Н	Н	Н
Н	L	Н	L	Н	Н	Н	Н	Н	Н	L	Н	Н
Н	L	н	Н	L	Н	Н	Н	Н	Н	н	L	Н
Н	L	н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L

\*G2=G2A+G2B

#### **DESCRIPTION**

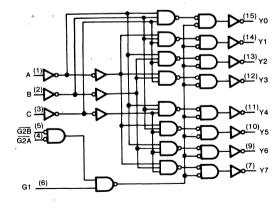
These devices are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can be used to minimize the effects of system decoding. When used with high-speed memories utilizing a fast-enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The conditions at the binary select inputs and the three enable inputs select one of eight input lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### **LOGIC DIAGRAM**



Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_i < -0.5V \text{ or } V_i > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
(-0.5V < Vo < Vcc +0.5V) ±35 mA
Continuous Current Through
Vcc or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, $P_d{}^\dagger$ 500 mW
* Absolute Maximum Ratings are those values beyond

Power Dissipation Per Package, Pd<sup>†</sup> . . . . . 500 mW
\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature denating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Supply Voltage, Vcc	4.5V to 5.5V
DC input & Output Voltages*, Vin., Vout	OV to Vcc
Operating Temperature	

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

# DC ELECTRICAL CHARACTERISTICS (Vcc=5V±10% Unless Otherwise Specified)

Characteristic Sy	Symbol	Test Conditions	T	=25°C	KS74AHCT Ta = -40°C to +85°C	KS54AHCT T <sub>a</sub> =-55°C to +125°C	Unit
			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	v
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	VoH	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>Q</sub> =-20µA I <sub>Q</sub> =-4mA	Vcc 4.2	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> -0.1 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	Vol	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> =20µA I <sub>O</sub> =4mA I <sub>O</sub> =8mA	o	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	line	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μА
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =O <sub>M</sub> A		8.0	80.0	160.0	μА
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>1</sub> =2.4V other inputs: at V <sub>CC</sub> or GND lout=0µA		2.7	2.9	3.0	mA



# AC ELECTRICAL CHARACTERISTICS (Input tr. tr 42 ns), AHCT138

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	$T_a = -40^{\circ}$	AHCT C to +85°C DV ± 10%	Ta=-55°C	AHCT to +125°C V ± 10%	Unit
			Тур	Min	Max	Min	Max	
Propagation Delay, A, B, C or any Y	t <sub>PLH</sub>		12		20		24	ns
	t <sub>PHL</sub>		12		20		24	113
Propagation Delay,	t <sub>PLH</sub>		10		17		20	ns
G1 to any Y	t <sub>PHL</sub>	C <sub>L</sub> =50pF	10		17		20	113
Propagation Delay,	t <sub>PLH</sub>		10		17		20	ns
G2A or G2B to any Y	t <sub>PHL</sub>		10		17		20	1113
Input Capacitance	CIN		5					pF
Power Dissipation Capacitance*	C <sub>PD</sub>		50					рF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

#### **FEATURES**

- Designed specifically for high-speed memory decoders and data transmission systems
- Incorporates 2 enable inputs to simplify cascading and/or data reception
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
   I<sub>OL</sub> = 8 mA @ V<sub>OL</sub> = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### **DESCRIPTION**

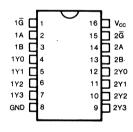
These devices are designed to be used in highperformance memory-decoding or data-routing applications requiring very short propagation delay times. In highperformance memory systems, these decoders can be used to minimize the effects of system decoding. When used with high-speed memories utilizing a fast-enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory, this means that the effective system delay introduced by the decoder is negligible.

The '139 consists of two individual two-line to four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

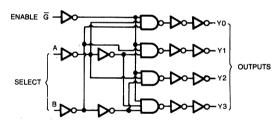
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### PIN CONFIGURATION



#### **LOGIC DIAGRAM**

#### (Each Decoder/Demultiplexer)



#### **FUNCTION TABLE**

In	puts					
Enable G	Sel B	lect A	YO	Y1	Y2	Y3
Н	Х	Х	Н	Н	Н	Н
L	L	L	L	Н	Н	Н
L	L	Н	Н	L	Н	Н
L	Н	L	Н	Н	L	Н
L	н	Н	Н	Н	Н	L

Supply Voltage Hange $V_{CC}$ ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-
posure to these conditions may affect device reliability.

<sup>†</sup> Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

Characteristic	Symbol	Test Conditions	Т,	a = 25°C	KS74AHCT T <sub>a</sub> = -40°C to +85°C	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> =20µA I <sub>O</sub> =4mA I <sub>O</sub> =8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

# AC ELECTRICAL CHARACTERISTICS (Input t, t <2 ns), AHCT139

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	Ta = -40°	4AHCT C to +85°C .0V±10%	KS54AHCT T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%		Unit
			Typ Min Max	Max	Min	Max		
Propagation Delay, A or B to Y	tpLH	C <sub>L</sub> =50pF	. 11		17		20	ns - ns
	tPHL		11		17		20	
Propagation Delay,	t <sub>PL:H</sub>		11		18		21	
G to any Y	t <sub>PHL</sub>		11		18		21	113
Input Capacitance	CIN		5					рF
Power Dissipation Capacitance*	C <sub>PD</sub>		50					рF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

# KS54AHCT 148 KS74AHCT

### Preliminary Specifications

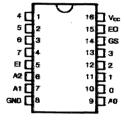
### **FEATURES**

- · Encodes eight data lines in priority
- · Provides 3-bit binary priority code
- · Input enable capability
- Easily cascadable
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
  - los =8 mA @ Vol =0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices:
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

## PIN CONFIGURATION



### DESCRIPTION

The '148 provides three bits of binary coded output representing the position of the highest order active input, along with an output indicating the presence of any active input. It is easily expanded via input and output enables to provide priority encoding over many bits.

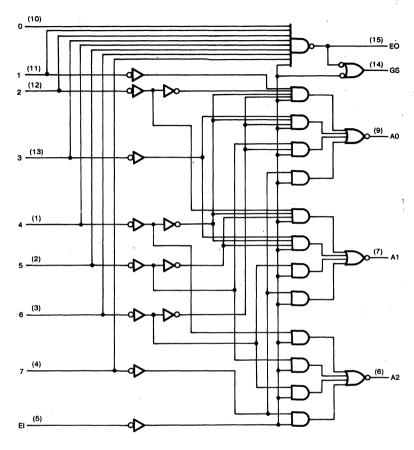
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

### **FUNCTION TABLE**

	Inputs									C	)utpc	ıts	
E	0	1	2	3	4	5	6	7	A2	Af	AG	GS	EO
Н	X	X	X	х	X	X	Х	Х	н	Н	H	Н	Н
L	Н	н	н	Н	Н	Н	H	Н	H	н	H	H	L
L	Х	X	X	X	Х	X	Х	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	Х	Х	Х	X	L	Н	Н	L	H	L	L	H
L	Х	X	Х	X	L	Н	Н	н	L	H	Н	L	H
L	X	X	X	L	н	Н	Н	Н	H	L	L	L	H
L	X	X	L	Н	Н	Н	Н	Н	H	L	H	L	H
L	Ж	L	н	н	Ħ	H	H	H	Н	H	L	L	Н
L	L	H	H	H	Н	Н	H	Н	H	H	H	L	H

# **LOGIC DIAGRAM**



# **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

Input Rise & Fall Times, tr, tf . . . . . . . Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

# DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	ymbol Test Conditions		= 25°C	KS74AHCT T <sub>a</sub> =-40°C to +85°C	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
3			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	v
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> -0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	lin	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin  V <sub>I</sub> =2.4V  other Inputs:  at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0µA		2.7	2.9	3.0	mA

# AC ELECTRICAL CHARACTERISTICS (Input tr., tr <2 ns), AHCT148

Characteristic	Symbol	Conditions†	$ \begin{array}{c c} & & & KS74AHCT \\ \hline & T_a = 25 ^{\circ}C \\ V_{CC} = 5.0V \\ \hline \end{array} \begin{array}{c} & KS74AHCT \\ \hline & T_a = -40 ^{\circ}C \ to \ +85 \\ \hline & V_{CC} = 5.0V \pm 10 \% \\ \end{array} $		C to +85°C	T <sub>a</sub> = -55°C	AHCT C to +125°C OV ± 10%	Unit
			Тур	Min	Max	Min	Max	
Propagation Delay,	tPLH		10		17		20	ns
1-7 to AO, A1 or A2	t <sub>PHL</sub>		10		17		20	113
Propagation Delay,	tpLH		11		18		22	ns ns ns
0-7 to EO	t <sub>PHL</sub>	C <sub>L</sub> =50pF	11		18		22	
Propagation Delay,	tplH		14		24		29	
0-7 to GS	t <sub>PHL</sub>		14		24		29	
Propagation Delay,	t <sub>PLH</sub>		10		16		19	
El to AO, A1 or A2	t <sub>PHL</sub>		10		16		19	
Propagation Delay,	tpLH		10		17		20	
El to GS	t <sub>PHL</sub>		10		17		20	
Propagation Delay,	t <sub>PLH</sub>		11		18		22	
EI to EO	t <sub>PHL</sub>		11		18		22	ns
Input Capacitance	Cin		5			·		рF
Power Dissipation Capacitance*	C <sub>PD</sub>		50			./		pF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

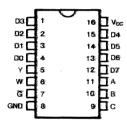
### **FEATURES**

- Can perform as:
   Boolean Function Generators
   Parallel-to-Serial Converters
   Data Source Selectors
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High drive currents outputs
- ( $I_{OL} = 24 \text{ mA} @ V_{OL} = 0.5V$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices.
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

### PIN CONFIGURATION



### **Absolute Maximum Ratings\***

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

### DESCRIPTION

These monolithic data selectors/multiplexers provide full binary decoding to select one of eight data sources. The strobe input  $(\widehat{\mathbf{G}})$  must be at a low logic level to enable the inputs. A high level at the strobe terminal forces the W output high and the Y output low.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

### **FUNCTION TABLE**

		OUTI	PUTS			
S	ELEC	т	STROBE			
C	3	A	G	Y	₩	
х	х	Х	H	L	Н	
L	L	L	L	סם	DO	
L	L	H	L	D1	<u> 1</u>	
L	1+	L	L	02	D2	
L	H	Н	. L	D3	<b>D3</b>	
H	1_	L	L	D4	<b>D4</b>	
H	L	H	L	05	D5	
H	H	L	L	D6	06	
Ħ	H	H	L	07	<del>07</del>	

H = high levet, L = low levet, X = irretevantD0, D1 ... D7 = the levet of the D respective input

Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

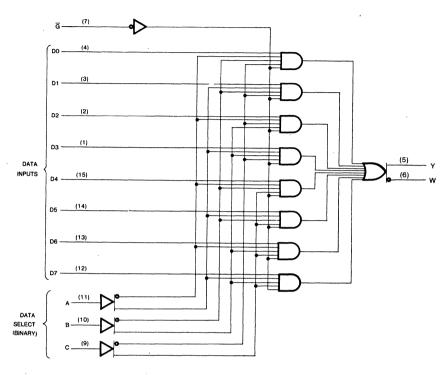
Hange KS74AHCT: −40°C to +85°C KS54AHCT: −55°C to +125°C

Input Rise & Fall Times, tr, tr . . . . . . Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)



# **LOGIC DIAGRAM**



DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T <sub>a</sub> = 25°C		KS74AHCT $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V <sub>ОН</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-6$ mA	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> -0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	IIN	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0 ·	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μА
Additional Worst Case Supply Current	ΔΙσς	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

# AC ELECTRICAL CHARACTERISTICS (Input tr, tr≤2 ns), AHCT151

Characteristic	Symbol	Conditions <sup>†</sup>	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	Ta = -40°0	AHCT C to +85°C DV±10%		AHCT to +125°C V± 10%	Unit
	l		Тур	Min	Max	Min .	Max	1
Propagation Delay, A, B or C to Y	tpLH	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	13 16		21 26		25 31	
	tpHL	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	13 16		21 26		25 31	ns
Propagation Delay, A, B or C to W	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	15 18		24 29		27 33	ns
	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	15 18		<b>24</b> 29		27 33	118
Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	9 12		15 20		18 24	ns
Any D to Y	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	9 12		15 20		18 24	
Propagation Delay	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	8 11		15 20		· 18	ns
Any D to W	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	8 11		15 20		18 24	113
Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	12 15		19 24		23 29	ns
G to Y	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	12 15		19 24		23 29	113
Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	13 16		21 26		25 31	ns
G to W	, t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	13 16		21 26		25 31	113
Input Capacitance	CIN		5					pF
Power Dissipation Capacitance*	C <sub>PD</sub>							pF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

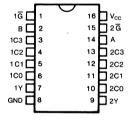
### **FEATURES**

- . Allows Multiplexing from N Lines to 1 Line
- Performs Parallel-to-Serial Conversion
- Strobe (Enable) Line Provided for Cascading (N lines to n lines)
- '253 is the 3-State Version of this part
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High drive currents Outputs
  - ( $I_{OL}$  = 24 mA @  $V_{OL}$  = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

### PIN CONFIGURATION



### DESCRIPTION

Each of these data selectors/multiplexers contains inverters and drives to supply full binary decoding data selection to the AND-OR gates. Separate strobe inputs (G) are provided for each of the two four-line sections.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

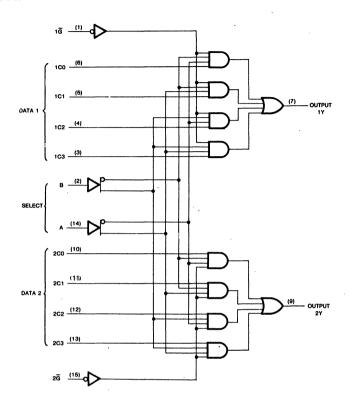
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground

## **FUNCTION TABLE**

	ECT UTS	DA	TA	INPU	TS	STROBE	ОИТРИТ
В	Α	CO.	C1	C2	C3	Ğ	Y
Х	Х	Х	Х	Х	X	Н	L
L	L	L	Х	Χ	Х	L	L
L	L	Н	Х	Χ	Х	L	Н
L	Н	Х	L	Χ	Χ	L	L
L	Н	Х	Н	Χ	Х	L	Н
Н	L	Х	Χ	L	Х	L	L
Н	L	Х	Х	Н	Χ	L	Н
Н	Н	Х	Х	Χ	L	L	L
Н	Н	Х	Χ	Χ	Н	L	Н

Select inputs A and B are common to both sections.

### **LOGIC DIAGRAM**



# **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 70 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-

posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . . Max 500 ns

\* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

# 4

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	mbol Test Conditions		=25°C	KS74AHCT T <sub>a</sub> = -40°C to +65°C	KS54AHCT T <sub>e</sub> =-55°C to +125°C	Uni
			Туф		Gueranteed Limits		
Minimum High-Level Input Voltage	Veri			2.0	2.0	2.0	v
Maximum Low-Level Input Voltage	ViL			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V <sub>OH</sub>	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> $i_O = -20\mu A$ $i_O = -6mA$	Vcc 4.2	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	VOL	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> to=20µA to=12mA to=24mA	o	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	in	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μА
Maximum Quiescent Supply Current	i in	V <sub>IN</sub> =V <sub>CC</sub> or GND IOUT=OµA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	_~~	per input pin V <sub>1</sub> =2.4V other inputs: at V <sub>CC</sub> or GND lour=0µA		2.7	2.9	3.0	mA

### AC ELECTRICAL CHARACTERISTICS (Input & tel 2 ns), AHCT153

Characteristic	Symbol	Conditions <sup>†</sup>	T.=25°C Vcc=5.0V	$T_{e} = -40^{\circ}$	V <sub>CC</sub> =5.0V±10%		KS54AHCT T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> =5.0V± 10%		
			Тур	Min	Max	Min	Mex		
		C <sub>L</sub> =50pF	13		21		25		
Propagation Delay, A or B to Y	<b>I</b> PLH	CL=150pF	16		26		31	ns	
	4	C <sub>L</sub> =50pF	13		21		25		
	<b>IPHL</b>	C <sub>L</sub> =150pF	16		26		31		
	t <sub>PLH</sub>	C <sub>L</sub> =50pF	9		15		18	l	
Propagation Delay,		C <sub>L</sub> =150pF	12		20		24	ns	
Data (Any C) to Y		C <sub>L</sub> =50pF	9		15		18		
	\$PHL	C_=150pF	12	1	20		24		
		Ct = 50pF	11		18		22		
Propagation Delay,	İPLH	C_=150pF	14		23		28	ns	
G to Y		C <sub>1</sub> =50pF	11		18		22	1.2	
	\$PHL	C_=150pF	14		23		28		
Input Capacitance	CIN		5					pF	
Power Dissipation Capacitance*	CPD	(per package)						pF	

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

 $<sup>^{\</sup>dagger}$  For AC switching test circuits and timing waveforms see section 2.

### **FEATURES**

- Decodes 4 Binary-Coded Inputs into One of 16 Mutually Exclusive Outputs
- Performs the Demultiplexing Function by Distributing Data From One Input to Any One of 16 Outputs
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
   I<sub>OL</sub> = 8 mA @ V<sub>OL</sub> = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

# DESCRIPTION These monolithic, 4-lin

These monolithic, 4-line to 16-line decoders decode four binary-coded inputs into one of sixteen mutually exclusive outputs when both the strobe inputs. G1 and G2, are low. The demultiplexing function is performed by using the 4 input lines to address the output line, passing data from one of the strobe inputs with the other strobe input low. When either strobe input is high, all outputs are high. These demultiplexers are idenally suited for implementing high-performance memory decoders.

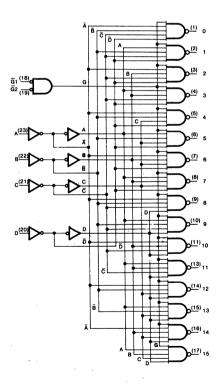
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

### PIN CONFIGURATION

1	$\neg \sim$		ì
ο¤	1	24	D Vcc
10	2	23	ΠA
20	3	22	В
3.□	4	21	<b>b</b> c
40	5	20	D D
5₫	6	19	Ğ2
6口	7	18	₫1
70	8	17	15
8 <b>d</b>	9 `	16	14
9.	10	15	13
10	11 ,	14	<b>5</b> 12
GND d	12	13	511

### LOGIC DIAGRAM



### **FUNCTION TABLE**

		Inputs	;				Outputs														
Ğ1	Ğ2	D	С	В	Α	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
L	L	L	L	L	Н	н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
L	L	L	L	Н	L	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
L	L	L	L	Н	Н	Н	Н	Н	Ĺ	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
L	L	L	н	L	L	н	Н	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
L	L	L	H	L	Н	Н	Н	Н	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
L	L	L	Н	Н	L	Н	Н	Н	Н	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н
L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н
L	L	• н	L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	L	Н	Н	Н	Н	Н	Н	Н
L	L	н	L	L	Н	Н	Н	Н	Н	Н	Н	H	Н	н	L	Н	Н	н	Н	Н	Н
. L	L	Н	L	Н	L '	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	Н	Н	Н	Н	Н
L	L	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	Н	Н	H	Н
L	L	Н	Н	L.	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	Н	Н	Н
L	L	Н	Н	L	Н	Н	Н	Ή	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	Н	Н
L	L	Н	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	н
L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L
L	Н	Х	Х	Χ	Χ	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
н	L	Х	Х	Х	Χ	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	H	Н	Н
Н	Н	Х	X	Х	Χ	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н

# **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> , −0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_l < -0.5V \text{ or } V_l > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pat 500 mW

<sup>\*</sup> Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	Τ.	a=25°C	KS74AHCT T <sub>a</sub> = -40°C to +85°C	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit			
			Тур	p Guaranteed Limits						
Minimum High-Level Input Voltage	VaH			2.0	2.0	2.0	٧			
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	0.8	٧			
Minimum High-Level Output Voltage	VoH	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> =-20µA I <sub>O</sub> =-8mA	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> -0.1	٧			
Maximum Low-Level Output Voltage	1	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> =20µA I <sub>O</sub> =4mA I <sub>O</sub> =8mA	O	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	٧			
Maximum Input Current	Im	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μА			
Maximum Quiescent Supply Current	łcc	V <sub>IN</sub> =V <sub>CC</sub> or GND L <sub>OUT</sub> =O <sub>M</sub> A		8.0	80.0	160.0	μА			
Additional Worst Case Supply Current	Δlcc	per input pin  V <sub>i</sub> =2.4V  other inputs: at V <sub>CC</sub> or GND  lout=0µA		2.7	2.9	3.0	mA			

## AC ELECTRICAL CHARACTERISTICS (Input tr, tr≤2 ns), AHCT154

Characteristic	Symbol	Conditions <sup>†</sup>	T <sub>a</sub> =25°C V <sub>CC</sub> =5.0V	1 -	AHCT C to +85°C 3V±10%	KS54 T <sub>s</sub> = -55°C V <sub>CC</sub> =5.1	Unit		
			Тур	Min	Max	Min	Max		
Propagation Delay,	ФРЦН		12		20		24	ns	
A, B, C, D to Any Output	tenu	C <sub>L</sub> =50pF	C SONE	12		20		24	110
Propagation Delay,	<b>t</b> PLH		12		20		24	ns	
G1 or G2 to Any Output	tent		12		20		24	шъ	
Input Capacitance	CiN	·	5					рF	
Power Dissipation Capacitance*	CPD	,	50					рF	

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

### **FEATURES**

- Typical applications:
   Dual 2-to-4 line decoder
   Dual 1-to-4 line demultiplexer
   3-to-8 line decoder
   1-to-8 line demultiplexer
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
- $I_{OL} = 8 \text{ mA } @ V_{OL} = 0.5 \text{V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
   KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

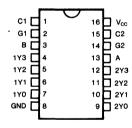
### DESCRIPTION

The '155 consists of two 1-to-4 line demultiplexers with independent strobes and common binary address inputs. When both sections are enabled by the strobes, the common address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired. Data applied to input C1 is inverted at its outputs and data applied to C2 is true through its outputs. The inverter following the C1 data input permits use as a 3-to-8 line decoder, or 1-to-8 line demultiplexer, without gating.

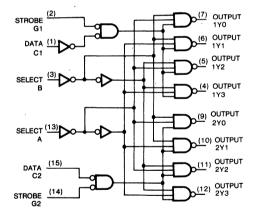
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

### PIN CONFIGURATION



### LOGIC DIAGRAM



### **FUNCTION TABLES**

2-to-4 Line Decoder or 1-to-4 Line Demultiplexer

		Inputs		0							
Sel	ect	Strobe	Data	Outputs							
В	A	G1	C1	1Y0	1Y1	1Y2	1Y3				
Х	Х	Н	X	н	Н	н	Н				
L	L	L	Н	L	Н	Н	Н				
L	Н	L	Н	Н	L	н	н				
Н	L	L	н	Н	Н	L	Н				
Н	Н	L	Н	Н	н	н	L				
Х	Χ	Х	L	Н	H	н	Н				

		Inputs		Outnite								
Sel	ect	Strobe	Data		Outputs							
В	A	G2	C2	2Y0	2Y1	2Y2	2Y3					
Х	Х	Н	Х	Н	Н	Н	Н					
L	L	L	L	L	Н	Н	Н					
L	Н	L	L	Н	L	Н	Н					
Н	L	L	L	Н	Н	L	H					
Н	Н	L	L	Н	Н	Н	L.					
X	Χ	X	Н	Н	Н	Н	Н					

3-to-8 Line Decoder or 1-to-8 Line Demultiplexer

int	outs		Outputs										
Select	Strobe or Data	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)				
ICB A	IG	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3				
XXX	Н	Н	Н	Н	Н	Н	Н	Н	Н				
LLL	L	L	Н	Н	. <b>H</b>	Н	Н	Н	Н				
LLH	L	Н	L	Н	Н	Н	Н	Н	Н				
LHL	L	Н	Н	L	Н	Н	Н	Н	Н				
LHH	L	Н	Н	Н	L	Н	Н	Н	Н				
HLL	L	Н	Н	Н	Н	L	Н	Н	Н				
HLH	L	Н	н	н	Н	Н	L	Н	Н				
HHL	L	Н	Н	Н	Н	Н	Н	L	Н				
ннн	L	Н	· H	Н	Н	Н	Н	Н	Ŀ				

IC = Inputs C1 and C2 connected together IG = Inputs G1 and G2 connected together

### **Absolute Maximum Ratings\***

Supply Voltage Range $V_{CC}$ , $-0.5V$ to $+7V$
DC Input Diode Current, I <sub>IK</sub>
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
A Abrahata Adamiana Daliana and Abraha salung bernand

<sup>\*</sup> Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Supply Voltage, V<sub>CC</sub> . . . . . . . . . . . . . . . . . 4.5V to 5.5V DC Input & Output Voltages\*, V<sub>IN</sub>, V<sub>OUT</sub> . . OV to V<sub>CC</sub> Operating Temperature

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either Vcc or GND)

# DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	= 25°C	KS74AHCT Ta = -40°C to +85°C	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit			
			Тур	Guaranteed Limits						
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	٧			
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	0.8	٧			
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-4m A$	V <sub>CC</sub>	V <sub>CC</sub> -0.1	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> -0.1	v			
Maximum Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> =20µA I <sub>O</sub> =4mA I <sub>O</sub> =8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v			
Maximum Input Current	l <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ			
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ			
Additional Worst Case Supply Current	Δlcc	per input pin  V <sub>i</sub> =2.4V  other inputs:  at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0µA		. 2.7	2.9	3.0	mΆ			

# AC ELECTRICAL CHARACTERISTICS (Input tr., tres 2 ns), AHCT155

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	Ta = -40°	AHCT C to +85°C 0V±10%	T <sub>a</sub> = -55°C	AHCT C to +125°C OV± 10%	Unit
			Тур	Min	Max	Min	Max	
Maximum Propagation Delay,	t <sub>PLH</sub>		12		20		24	ns
A, B, C2, G1 or G2 to any Output (2 levels of logic)	t <sub>PHL</sub>		12		20		24	
Maximum Propagation Delay,	t <sub>PLH</sub>	- C <sub>L</sub> =50pF	14		23		28	ns
A or B to any Y (3 levels of logic)	t <sub>PHL</sub>		OL COD!	14		23		28
Maximum Propagation Delay,	t <sub>PLH</sub>		13		22		26	ns
C1 to any Y	t <sub>PHL</sub>		13		22		/ 26	"
Maximum Input Capacitance	CIN		5					pF
Power Dissipation Capacitance*	C <sub>PD</sub>							pF

<sup>\*</sup> CPD determines the no-load dynamic power dissipation: PD=CPD VCC2 f + ICC VCC.

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

### **FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:

 $I_{OL} = 8$  mA @  $V_{OL} = 0.5$ V

- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

## DESCRIPTION

These are data selectors multiplexers which select a 4-bit word from one of two sources via the control of a common select input  $(\overline{A}/B)$ . A separate strobe input  $(\overline{G})$  is provided. The '157 presents true data whereas the '158 presents inverted data at the outputs.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

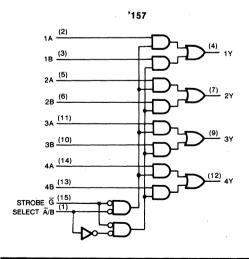
# PIN CONFIGURATION

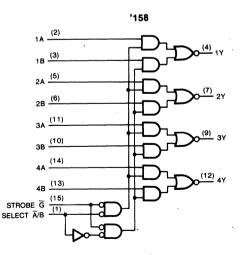
Ā/B	16 V <sub>CC</sub> 15 G 14 AA 13 AB 12 AY
1Y 🛮 4	13 <b>5</b> 4B
GND 8	9 3Y

### **FUNCTION TABLE**

	Inputs	Output Y				
Strobe	Select	Da		14.50		
Ğ	Ā/B	Α	В	'157	'158	
Н	Х	Х	Х	L	Н	
L	L	L	Х	L	H	
L	L	Н	Х	Н	L	
L	Н	X	L	L	Н	
L	н	X	н	н	L	

### LOGIC DIAGRAMS





# **Absolute Maximum Ratings\***

Supply Voltage Range V<sub>CC</sub>, . . . . . . −0.5V to +7V

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Supply Voltage, V <sub>CC</sub>	4.5V to 5.5V
DC Input & Output Voltages*, VIN, VOUT	OV to Vcc
Operating Temperature	,

Range KS74AHCT:  $-40^{\circ}$ C to  $+85^{\circ}$ C KS54AHCT:  $-55^{\circ}$ C to  $+125^{\circ}$ C Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . . . Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

# DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	= 25°C	KS74AHCT $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit	
			Тур		Guaranteed Limits			
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	٧	
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v	
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> -0.1 3.84	V <sub>CC</sub> -0.1 3.7	v	
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1	v	
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ	
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μA	
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>1</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0µA		2.7	2.9	3.0	mA	

# AC ELECTRICAL CHARACTERISTICS (Input tr, tr≤2 ns), AHCT157, AHCT158

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	$KS74AHCT$ $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$		$KS54AHCT$ $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Тур	Min	Max	Min	Max	
Propagation Delay.	tpLH		. 9		14		18	ns
A or B to Y	t <sub>PHL</sub>		9		14		18	113
Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pF	13		22		26	ns
Ā/B to Y	t <sub>PHL</sub>		13		22		26	115
Propagation Delay,	t <sub>PLH</sub>		12		19		23	ns
G to Y	t <sub>PHL</sub>		12		19		23	110
Input Capacitance	C <sub>IN</sub>		5					pF
Power Dissipation Capacitance*	C <sub>PD</sub>	(per gate)						pF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} \ V_{CC}^2 \ f + I_{CC} \ V_{CC}$ .

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

# KS54AHCT **160/161** KS74AHCT **162/163**

# Synchronous 4-Bit Decade and Binary Counters

### **FEATURES**

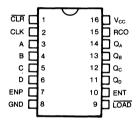
- Internal Look Ahead for Fast Counting
- Carry Output for n-bit cascading
- Synchronous Counting
- Synchronously Programmable
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
- loL = 8 mA @ Vol = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

### PIN CONFIGURATION



### **FUNCTION TABLES**

'160, '161

	CLK	CLR	ENP	ENT	LOAD	Function			
	Х	L	Х	X	Х	Clear			
	Х	Н	Н	L	н	Count & RC disabled			
	Х	Н	L	Н	н	Count disabled			
١	Χ	Н	L	L	Н	Count & RC disabled			
-	Ť	Н	Х	Х	L	Load			
	<b>†</b>	Н	Н	Н	Н	Increment Counter			

'162, '163

CLK	CLR	ENP	ENT	LOAD	Function		
1	L	Х	Х	Х	Clear		
Х	Н	Н	L	Н	Count & RC disabled		
Х	н	L	н	Н	Count disabled		
X	Н	L	L	н	Count & RC disabled		
1	Н	Х	Х	L	Load		
<u>†</u>	Н	H	Н	Н	Increment counter		

### DESCRIPTION

These are synchronous, presettable 4-bit binary counters featuring internal carry-look-ahead for high-speed counting. The '160 and '162 are decade counters, and the '161 and '163 are 4-bit binary counters. The buffered clock input triggers all flip-flops simultaneously on the rising edge of the input waveform. This eliminates the output counting spikes normally associated with asynchronous counters.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs.

The clear function for the '160 and '161 is asynchronous and a low level at the clear input sets all four of the flipflop outputs low regardless of the levels of the clock, load or enable inputs.

The clear function for the '162 and 163 is synchronous and a low level at the clear input sets all four of the flipflop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter.

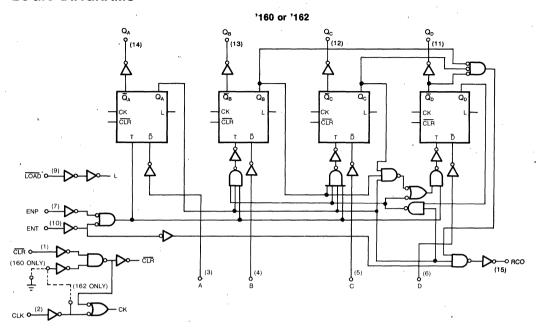
Two enable inputs and a ripple carry output allow easy cascading of the counters. Both count-enable inputs (ENP and ENT) must be high to count, and ENT is fed forward to enable the ripple carry output. The ripple carry output (RCO) thus enabled will produce a high-level pulse while the count is maximum (9 or 15 with Q<sub>A</sub> high). This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. Transitions at the ENP or ENT are allowed regardless of the level of the clock input.

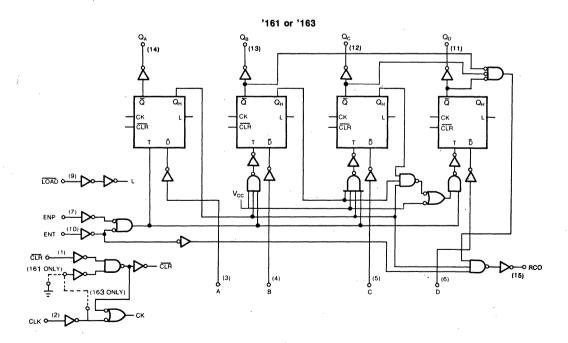
These counters feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, or  $\overline{\text{LOAD}}$ ) that will modify the operating model have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{\text{cc}}$  and ground.

# **LOGIC DIAGRAMS**

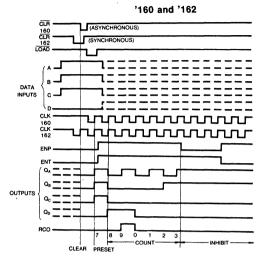




# KS54AHCT 160/161 KS74AHCT 162/163

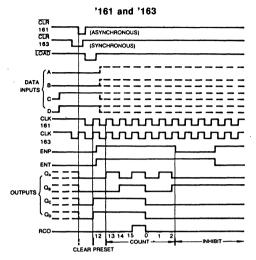
# Synchronous 4-Bit Decade and Binary Counters

### Typical Clear, Preset, Count and Inhibit Sequences



#### Sequence:

- (1) Clear outputs to zero
- (2) Preset to BCD seven
- (3) Count to eight, nine, zero, one, two, and three
- (4) Inhibit



#### Sequence:

- (1) Clear outputs to zero
- (2) Preset to binary twelve
- (3) Count to thirteen, fourteen, fifteen, zero, one and two
- (4) Inhibit

# Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$ , -0.5V to  $\pm 7V$  DC Input Diode Current,  $I_{IK}$   $(V_I < -0.5V$  or  $V_I > V_{CC} \pm 0.5V)$   $\pm 20$  mA DC Output Diode Current,  $I_{OK}$   $(V_O < -0.5V$  or  $V_O > V_{CC} \pm 0.5V)$   $\pm 20$  mA Continuous Output Current Per Pin,  $I_O$   $(-0.5V < V_O < V_{CC} \pm 0.5V)$   $\pm 35$  mA Continuous Current Through  $V_{CC}$  or GND pins  $\pm 125$  mA Storage Temperature Range,  $T_{stg}$   $\pm -65^{\circ}C$  to  $\pm 150^{\circ}C$  Power Dissipation Per Package,  $P_d^{\dagger}$  500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Supply Voltage, V<sub>CC</sub> . . . . . . . . . . . . . . . . . 4.5V to 5.5V DC Input & Output Voltages\*, V<sub>IN</sub>, V<sub>OUT</sub> . . . OV to V<sub>CC</sub> Operating Temperature

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . . Max 500 ns

\* Unused inputs must always be tied to an appropriate logic

 Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

# Synchronous 4-Bit Decade and Binary Counters

# DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	a = 25°C	KS74AHCT $T_{a} = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	v
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

# AC ELECTRICAL CHARACTERISTICS (Input t<sub>r</sub>, t<sub>f</sub>≤2 ns), AHCT160, AHCT161

Characteristic		Symbol	Conditions <sup>†</sup>	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	$T_a = -40^{\circ}$	AHCT C to +85°C DV ± 10%	$T_a = -55$ °C	AHCT to +125°C V± 10%	Unit	
				Тур	Min	Max	Min	Max		
Maximum Cloc	k Frequency	f <sub>max</sub>		50	40		35		MHz	
Propagation De	elay,	t <sub>PLH</sub>		15		20		24	ns	
CLK to RCO		t <sub>PHL</sub>		15		20		24	110	
Propagation De	elay,	tpLH		10		16	- 1	19	ns	
CLK to any Q		t <sub>PHL</sub>	C <sub>L</sub> =50pF	10		16		19	110	
Propagation De	elay,	t <sub>PLH</sub>	OL-30pi	8		13		16	ns	
ENT to RCO	-	t <sub>PHL</sub>		8		13		16	110	
Propagation De	Propagation Delay, CLR to any Q				15		24		29	ns
Propagation De	elay,	t <sub>PHL</sub>		17		23		33	ns	
Pulse Width	CLK High or Low	tw		10	15		20	;	ns	
l disc Width	CLR Low	l w		10	15		20		] "	
	A, B, C, D			10	15		20			
Setup Time	LOAD	t <sub>su</sub>		10	15		20		ns	
Setup Time before CLK1	ENP, ENT	- su	ĺ	10	15		20		113	
	CLR inactive	]		6	10		· 10			
Hold time, All Synchronous Inputs after CLK†		t <sub>h</sub>		-3	0		0		ns	
Input Capacitar	Input Capacitance			5					pF	
Power Dissipat	tion Capacitance*	C <sub>PD</sub>		80					pF	

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} \ V_{CC}^2 \ f \ + \ I_{CC} \ V_{CC}$ .

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.



# KS54AHCT 160/161 KS74AHCT 162/163

# Synchronous 4-Bit Decade and Binary Counters

# AC ELECTRICAL CHARACTERISTICS (Input tr, tr≤2 ns), AHCT162, AHCT163

Characteristic		Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	T <sub>a</sub> = -40°C	AHCT C to +85°C OV ±10%	$T_a = -55$ °C	AHCT to +125°C V± 10%	Unit
				Тур	Min	Max	Min	Max	
Maximum Clo	ck Frequency	f <sub>max</sub>		50	40		35		MHz
Propagation D	elay,	t <sub>PLH</sub>		15		20		24	ns
CLK to RCO		t <sub>PHL</sub>		15		20		24	110
Propagation D	elay,	tpLH	C <sub>L</sub> =50pF	10		16		20	ns
CLK to any Q		t <sub>PHL</sub>		10		16		20	113
Propagation D	elay,	tpLH		9		15		18	ns
ENT to RCO		t <sub>PHL</sub>	· ·	9		15		18	113
Pulse Width, CLK High or I	_ow	t <sub>w</sub>		8	12.5		20		ns
	A, B, C, D			10	15		20		
Setup Time	LOAD	t <sub>su</sub>		10	15		20		ns
Setup Time before CLK1	ENP, ENT	- Lsu		15	15		20		1115
	CLR inactive			6	10		10		1
	CLR Low			6	15		20		
Hold time, All Synchronous Inputs after CLK↑		t <sub>h</sub>		<b>–3</b>	0		0		ns
Input Capacita	Input Capacitance			5					pF
Power Dissipa	ation Capacitance*	C <sub>PD</sub>		80					pF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

- AND—Gated (enable/disable) serial inputs
- · Fully buffered clock and serial inputs
- Direct clear
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:

 $I_{OL} = 8$  mA @  $V_{OL} = 0.5$ V

- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

· Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

### DESCRIPTION

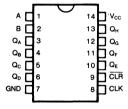
These are high-speed 8-bit registers with AND-gated serial inputs and an asynchronous clear. Data is entered serially through either one of the two inputs, A and B. A high on one input enables the other one, which will then determine the state of the first flip-flop. A low at either or both inputs inhibits data entry and resets the first flip-flop to a low level at the next positive clock transition.

Data at the serial inputs may be changed while the clock is high or low, provided the minimum setup time requirements are met. Clocking occurs on the low-to-highlevel transition of their clock input.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V<sub>CC</sub> and

### PIN CONFIGURATION



### **FUNCTION TABLE**

	Inputs		Outputs	3		
CLR	CLK	QA	Q <sub>B</sub> .	Q <sub>H</sub>		
L	Х	Х	Х	L	L	L
Н	L	Х	Χ	QAO	Q <sub>B0</sub>	$Q_{HO}$
Н	. 1	Н	Н	н	$Q_{An}$	$Q_{Gn}$
H	1	L	Χ	L	$Q_{An}$	$Q_{Gn}$
Н	. ↓	· X	L	L	$Q_{An}$	$Q_{Gn}$

H = high level (steady state), L = low level (steady state)

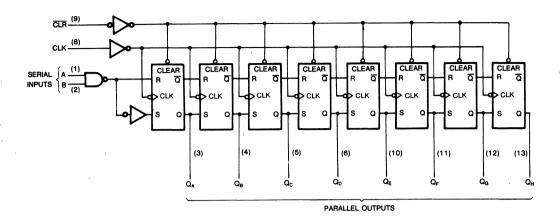
X = irrelevant (any input, including transitions)

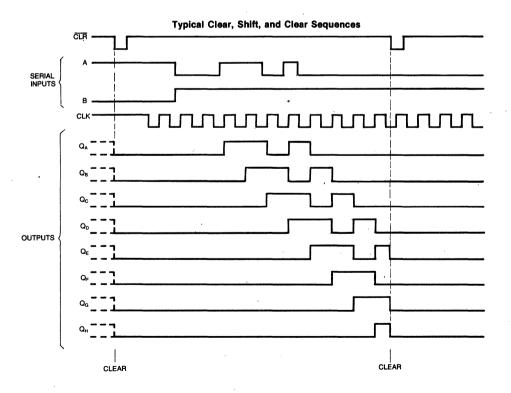
t = transition from low to high level.

Q<sub>A0</sub>, Q<sub>B0</sub>, Q<sub>H0</sub>=the level of Q<sub>A</sub>, Q<sub>B</sub> or Q<sub>H</sub>, respectively, before the indicate steadystate input conditions were established.

Q<sub>An</sub>, Q<sub>Gn</sub> = the level of Q<sub>A</sub> or Q<sub>G</sub> before the most-recent † transition of the clock; indicates a one-bit shift.

## **LOGIC DIAGRAMS**





### **Absolute Maximum Ratings\***

Supply Voltage Range $V_{CC}$ , $-0.5V$ to $+7V$
DC Input Diode Current, I <sub>IK</sub>
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + 2.5 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissination Per Package Put 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

	-	_	
Supply Voltage, Vo	с		4.5V to 5.5V
DC Input & Output	Voltages*, V <sub>IN</sub> ,	Vout	OV to V <sub>CC</sub>
Operating Tempera			,

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . Max 500 ns

 Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

# DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	a = 25°C	KS74AHCT T <sub>a</sub> = -40°C to +85°C	KS54AHCT T <sub>a=-55°C</sub> to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> -0.1	v
Maximum Low-Level Output Voltage.	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	ő	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin  V <sub>I</sub> =2.4V  other Inputs: at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0µA		2.7	2.9	3.0	mA <sup>-</sup>

# AC ELECTRICAL CHARACTERISTICS (Input tr, tr≤2 ns), AHCT164

Characteristic		Symbol	Conditions <sup>†</sup>	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	KS74 T <sub>a</sub> = -40°C V <sub>CC</sub> =5.0	to +85°C	KS54, $T_a = -55$ °C $V_{CC} = 5.0$	to +125°C	Unit
				Тур	Min	Max	Min	Max	
Maximum Clock Fro	equency	f <sub>max</sub>		60	36		30		MHz
Propagation Delay, CLR to any Q		t <sub>PHL</sub>	C <sub>L</sub> =50pF	12		20		24	ns
Propagation Delay,		t <sub>PLH</sub>	OL COP.	11		18		21	ns
CLK to any Q		tPHL		11		18		21	
Pulse Width	CLR Low	- t <sub>w</sub>		8	12		15		ns
I disc Width	CLK High or Low			8	12		15		] '''
Setup	Data			8	12		15		ns
Time before CLK↑ CLR Inactive		- t <sub>su</sub>		8	12		15		1 115
Hold Time Data after CLK1		t <sub>h</sub>		1	4		5	6	ns
Input Capacitance		C <sub>IN</sub>		5					рF
Power Dissipation	Capacitance*	C <sub>PD</sub>	(per package)	120					pF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

### **FEATURES**

- Complementary outputs
- Direct overriding load (data) inputs
- · Gated clock inputs
- · Parallel-to-Serial data conversion
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
   I<sub>OL</sub> = 8 mA @ V<sub>OL</sub> = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

### DESCRIPTION

These are high-speed 8-bit parallel-load or serial-in shift registers with complementary serial outputs available from the last stage. Parallel-in access is asynchronous and is enabled by pulling the SH/LD input low. When SH/LD is high, data is entered serially at the SER input and shifted one place to the right with each positive clock transition.

Clocking is accomplished through a 2-input NOR gate which permits one of the clocks to be used as a clock inhibit function. Holding either clock input high inhibits clocking. Either clock input is enabled by holding the other clock input low while the  $SH/\overline{LD}$  input is high.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

### PIN CONFIGURATION

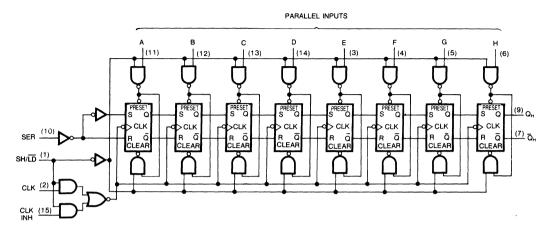
SH/LD 1	16	/cc
CLK 🗖 2	15 0	CLK INH
E <b>□</b> 3	14 🗖 🗈	)
F 🗖 4	13 🗖 C	; '
G <b>□</b> 5	12 B	l
н □6	11 🗖 A	
QH 🗖 7	10 🗖 S	ER
GND 🔲 8	9 🗖 0	)H
<u> </u>		

### **FUNCTION TABLE**

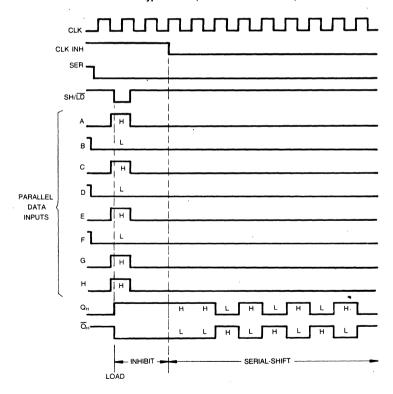
		Inputs		
	SH/LD	CLK	CLK INH	Function
	L	Х	Х	PARALLEL LOAD
-	н	Н	X	NO CHANGE
	н	X	Н	NO CHANGE
1	Н	L	1	SHIFT*
	Н	1	L	SHIFT*

<sup>\*</sup>Content of each internal register shifts toward output Q<sub>H</sub>. Data at serial input is shifted into first register.

### **LOGIC DIAGRAMS**



Typical Shift, Load and Inhibit Sequences



# **Absolute Maximum Ratings\***

Supply Voltage Range $V_{CC}$ , $-0.5V$ to $+7V$
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V)$ or $V_1 > V_{CC} + 0.5V) \dots \pm 20$ mA
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW
* Absolute Maximum Ratings are those values beyond

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . Max 500 ns

\* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

# DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	τ	a = 25°C	KS74AHCT T <sub>a</sub> = -40°C to +85°C	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	>
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-4m A$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> -0.1 3.84	V <sub>CC</sub> −0.1	٧
Maximum Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> =20µA I <sub>O</sub> =4mA I <sub>O</sub> =8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin  V <sub>I</sub> =2.4V  other Inputs:  at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0µA		2.7	2.9	3.0	mA

# AC ELECTRICAL CHARACTERISTICS (Input tr., tr <2 ns), AHCT165

Characteristic		Symbol	Conditions <sup>†</sup>	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	$T_a = -40^{\circ}C$	AHCT C to +85°C DV ± 10%	T <sub>a</sub> = - 55°C	IAHCT C to +125°C DV ± 10%	Unit
		. '		Тур	Min	Max	Min	Max	
Maximum Clo	ock Frequency	f <sub>max</sub>		50	30		25		MHz
Propagation [	Delay,	t <sub>PLH</sub>		15	,	25		30	ns
SH/LD to Q <sub>H</sub>	or Q <sub>H</sub>	t <sub>PHL</sub>		15		25		30	
Propagation (		t <sub>PLH</sub>	C <sub>L</sub> =50pF	19		31		37	ns
CLK to Q <sub>H</sub> or	r Q <sub>H</sub>	t <sub>PHL</sub>		19		31		37	
Propagation (	Delay,	t <sub>PLH</sub>		12		20		24	ns
H to Q <sub>H</sub> or $\overline{Q}$	Н	t <sub>PHL</sub>		12		20		24.	
Pulse Width	SH/LD Low	tw		8	12		15		ns
T GIOG TTTGTT	CLK High or Low			8	12		15		
	SH/LD High before CLK1			7	15		20	,	
	SER before CLK1			8	12	1	15		
Setup Time	CLK INH Low before CLK1	tsu		7	15		20		ns
	CLK INH High before CLK↓			7	15		20		
	Data before SH/LD↑			5	8		10		
Hold Time	SER Data after CLK1	th		-3	0		0		ns
TIOIG TITLE	PAR Data after SH/LD1			-3	0		0		
Input Capacit	ance	CIN		5					рF
Power Dissip	ation Capacitance*	C <sub>PD</sub>		100					pF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} \ V_{CC}^2 \ f + I_{CC} \ V_{CC}$ .
† For AC switching test circuits and timing waveforms see section 2.

### **FEATURES**

- Synchronous load
- Direct overriding clear
- Parallel to serial conversion
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
  - $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5 \text{V}$
- . Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- · Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

Package options include plastic "small outline"

packages, standard plastic and ceramic 300-mil DIPs

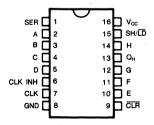
### DESCRIPTION

These devices feature parallel-in or serial-in, serial-out registers, gated clock inputs and an overriding clear input. The paralled-in or serial-in modes are established by the shift/load input. When high, the input enables the serial data input and couples the eight fill-flops for serial shifting with each clock pulse. When low, the paralled data inputs are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high edge of the clock pulse through a two-input positive NOR gate permitting one input to be used as a clock-enable or clock-inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. This allows the system clock to be free-running and the register can be stopped on command with the clock input. The clock-inhibit input should be changed to the high level only when the clock input is high. A buffered direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to Vcc and

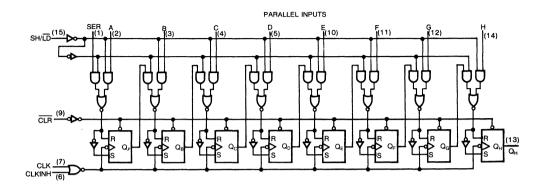
### PIN CONFIGURATION



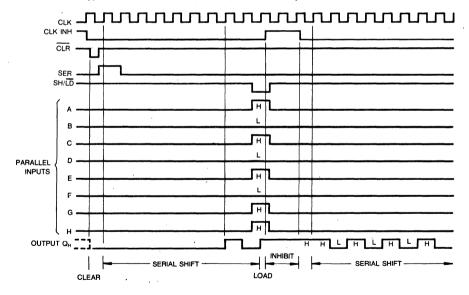
### **FUNCTION TABLE**

		Inte	rnal	Output				
CLR	SH/LD	CLK	01.1/	050		Outputs		
CLK	9H/LU	INH	CLK	SER	A H	QA	QB	
L	Х	Х	X	Х	Х	L	L	L.
Н	X	L	L	Х	X	QAO	Q <sub>B0</sub>	Q <sub>H0</sub>
Н	L	L	<b>↑</b>	X	a h	а	b	h
Н	Н	L	1	Н	X	Н	$Q_{\text{An}}$	Q <sub>Gn</sub>
н	н	L	1	L	X	L	$Q_{An}$	
Н	X	н	1	Х	X	GAO	$Q_{B0}$	Q <sub>H0</sub>

# **LOGIC DIAGRAM**



Typical Clear, Shift, Load, Inhibit, and Shift Sequences



# **Absolute Maximum Ratings\***

Supply Voltage Range $V_{CC}$ ,0.5V to +7V DC Input Diode Current, $I_{IK}$
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

		•	•	
Supp	ply Voltage, V <sub>CC</sub>	:	4.5V to	5.5V
DC I	Input & Output \	/oltages*, V <sub>IN</sub> ,	Vout OV to	V <sub>CC</sub>
Ope	rating Temperati	ure		
F	Range	KS74AHCT:	-40°C to +8	35°C
		KS54AHCT:	-55°C to +12	25°C

Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . Max 500 ns \* Unused inputs must always be tied to an appropriate logic

voltage level (either V<sub>CC</sub> or GND)

# DC ELECTRICAL CHARACTERISTICS (Vcc=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T <sub>a</sub> = 25°C		KS74AHCT T <sub>a</sub> = -40°C to +85°C	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
			Тур	Guaranteed Limits			
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL	,		0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> -0.1	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

# AC ELECTRICAL CHARACTERISTICS (Input t<sub>r</sub>, t<sub>f</sub>≤2 ns), AHCT166

Characteristic		Symbol	Conditions <sup>†</sup>	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	KS74AHCT $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%		Unit
				Тур	Min	Max	Min	Max	
Maximum Clock Frequency		f <sub>max</sub>		60	36		30		MHz
Propagation Delay, CLR to Q <sub>H</sub>		t <sub>PHL</sub>	C <sub>L</sub> =50pF	10		17		20	ns
Propagation Delay, CLK to Q <sub>H</sub>		tpLH	OL-30bi	13		21		25	ns
		t <sub>PHL</sub>		13		21		25	
Pulse Width	CLR Low			8	12		15		ns
	CLK High or Low	tw		8	12		15		
Setup Time	SH/LD High before CLK1			.8	12		15		
	SER before CLK1	1.		8	12		15		
	CLK INH before before CLK1	t <sub>su</sub>		8	12		15 ·		ns
	Data before SH/LD1	1		8	12		15		
	CLR Inactive before CLK			8	12		15		
Hold Time	SH/LD High after CLK1			5	8		10		
	SER after CLK1			5	8		10		
	CLK INH after CLK1	th		5	8		10		ns
	Data after SH/LD↑			5	8		10		
	CLR Active after CLK†			5	. 8		10		
Input Capacitance		CIN		5					pF
Power Dissipation Capacitance*		C <sub>PD</sub>							pF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

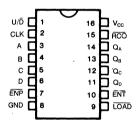
<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

- Fully Synchronous Operation for Counting and Programming
- Internal Look Ahead for Fast Counting
- · Carry Output for N-bit Cascading
- Fully Independent Clock Circuit
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
  - $I_{OL} = 8$  mA @  $V_{OL} = 0.5$ V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V' to 5.5V
- Characterized for operation over industrial and military temperature ranges: KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATION



#### DESCRIPTION

These synchronous presettable counters feature an internal carry look-ahead for cascading in high-speed counting applications. The '168 is a decade counter and the '169 is a 4-bit binary counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (rip-ple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock waveform.

These counters are fully programmable; that is, the outputs may each be preset to either level. The load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

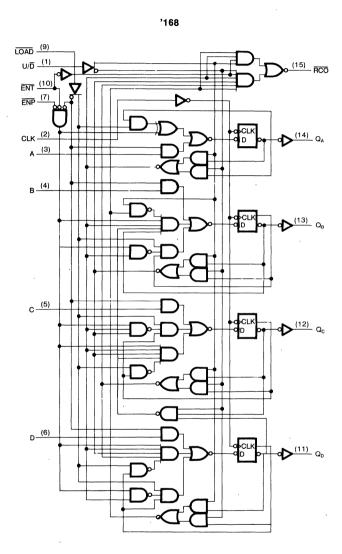
The carry look-ahead circuitry provides for cascading counters for n-bit synchronous application without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count enable inputs ( $\overline{\text{ENP}}$  and  $\overline{\text{ENT}}$ ) must be low to count. The direction of the count is determined by the level of the  $U/\overline{D}$  input. When  $U/\overline{D}$  is high, the counter counts up; when low, it counts down. Input  $\overline{\text{ENT}}$  is fed forward to enable the carry output. The ripple carry output ( $\overline{\text{RCO}}$ ) thus enabled will produce a low-level pulse while the count is zero (all inputs low) counting down or maximum (9 or 15) counting up. This low-level overflow carry pulse can be used to enable successive cascaded stages. Transition at  $\overline{\text{ENP}}$  or  $\overline{\text{ENT}}$  are allowed regardless of the level of the clock input.

These counters feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, LOAD, U/D) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

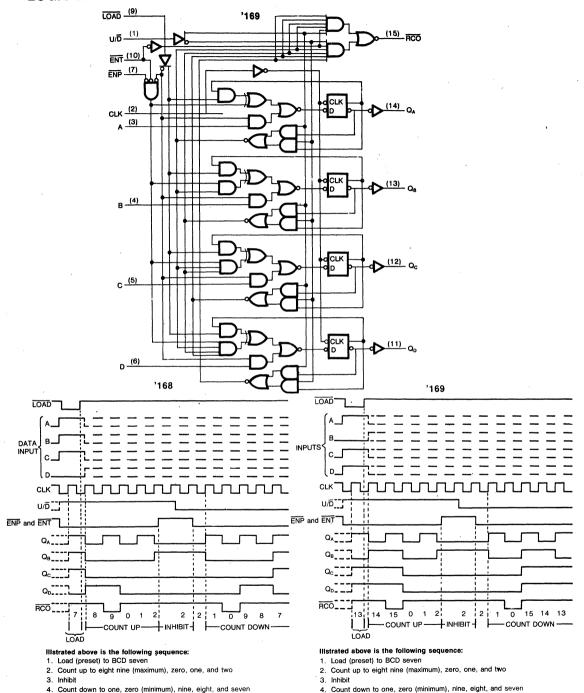
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

## **LOGIC DIAGRAMS**



## LOGIC DIAGRAMS (continued)



#### **FUNCTION TABLE**

OPERATING MODE			INP	OUTPUTS				
	CLK	U/D	ENP	ENT	LOAD	Dn	Qn	RCO
Parallel Load	1	Х	Х	Х	ı	i	L	(1)
	1	X	X	Х	i	h	Н	(1)
Count Up	1	h	ı	1	h	Х	Count Up	(1)
Count Down	1	ı	ı	i	h	Х	Count Down	(1)
Hold	1	Х	h	Х	h	X	Qn	(1,)
	1	X	Х	h	h	Х	q <sub>n</sub>	Н

H=HIGH voltage level steady state

h=HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition

L=LOW voltage level steady state

I=LOW voltage level one setup time prior to the LOW-to-HIGH clock transition

X=Don't care

q=Lower case letters indicate the state of the referenced output prior to the LOW-to-HIGH clock transition

↑=LOW-to-HIGH clock transition

#### NOTE:

1. The RCO is LOW when ENT is LOW and the counter is at Terminal Count Terminal Count Up is (HHHH) and Terminal Count Down is (LLLL) for '169.

The RCO is LOW when ENT is LOW and the counter is at Terminal Count. Terminal Count Up is (HLLH) and Terminal Count Down is (LLLL) for '168.

## Absolute Maximum Ratings\*

DC Input Diode Current, I <sub>IK</sub>
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_0 < V_{CC} + 0.5\dot{V}) + \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW

Supply Voltage Range V<sub>CC</sub>, . . . . . . . −0.5V to +7V

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

 Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

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## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	Т	<sub>a</sub> = 25°C	KS74AHCT T <sub>a</sub> = -40°C to +85°C	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
		•	Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3,84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	l <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	l lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.Ò	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin  V <sub>I</sub> =2.4V  other Inputs:  at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0µA		2.7	2.9	3.0	mA

## AC ELECTRICAL CHARACTERISTICS (Input tr, tr <2 ns), AHCT168, AHCT169

Characteristic		Symbol	Conditions <sup>†</sup>	$\begin{array}{c c} T_a = 25^{\circ}C \\ V_{CC} = 5.0V \end{array}$		KS74AHCT $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 10^{\circ}\text{M}$		KS54AHCT $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$	
				Тур	Min	Max	Min	Max	
Maximum Operating Fr	equency	f <sub>max</sub>		50	30		25		MHz
Propagation Delay,		t <sub>PLH</sub>		19		28		32	ns
CLK to RCO		t <sub>PHL</sub>		19		·28		32	115
Propagation Delay,		t <sub>PLH</sub>		12		18		22	no
CLK to Any Q	*	t <sub>PHL</sub>	C <sub>1</sub> = 50pF	12		18		22	ns
Propagation Delay,		tpLH	CL=50pr	10		16		19	
ENT to RCO		t <sub>PHL</sub>		10		16		19	ns
Propagation Delay,		t <sub>PLH</sub>		14		23		25	
U/D to RCO		tPHL		14		23		25	ns
Pulse Duration, CLK high or low		t <sub>w</sub> .		10	16		20	,	ns
Setup Time, A,	B, C or D	c#		9	15		20		
Before CLK1 EN	NP or ENT			12	20		. 25		
· LC	DAD			9	15		20		ns
U/	Ď			9	15		. 20 '		
Hold Time, Data after CLK†		th		-3	0		0		ns
Input Capacitance		C <sub>IN</sub>		5					pF
Power Dissipation Capa	acitance*	C <sub>PD</sub>							pF

<sup>\*</sup> CPD determines the no-load dynamic power dissipation: PD=CPD VCC2 f + ICC VCC.

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.



- Gated output control lines for enabling or disabling the outputs
- Fully independent clock for operation in parallel-load or hold modes
- · For application as bus buffer registers
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
  - $I_{OL}$  = 24 mA @  $V_{OL}$  = 0.5V for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### DESCRIPTION

These 4-bit registers contain D-type flip-flops with 3-state outputs, capable of driving highly-capacitive or low-impedance loads. This provides the device with the capability of being connected directly to and driving the bus lines in a busorganized system without need for interface or pull-up components.

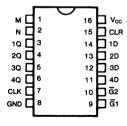
Gated enable inputs are provided for controlling the entry of data into the flip-flops. When both data-enable inputs are low, data at the D inputs are loaded into their respective flip-flops on the next positive transition of the buffered clock input. Gated output control inputs are also provided. When both are low, the normal logic states of the four outputs are available for driving the loads or bus lines. The outputs are disabled independently from the level of the clock by a high logic level at either output control input. The outputs then present a high impedance and neither load nor drive the bus line. Detailed operation is given in the function table.

To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable times are shorter than the average output enable times.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

## PIN CONFIGURATION

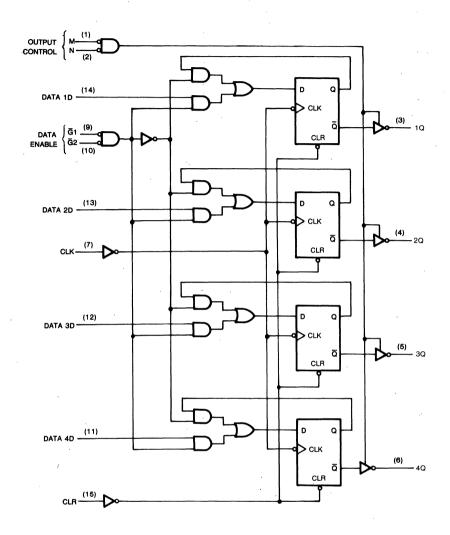


#### **FUNCTION TABLE**

	Input										
CLR	CLK	Data !	Enable	Data	Output						
OLII	J.K	Ğ1	G1 G2								
Н	Х	X	Х	/ <b>X</b>	L						
L	L	X	Χ	Х	Q <sub>0</sub> Q <sub>0</sub> Q <sub>0</sub>						
L	1	H	Х	. X	Qo						
L	1	×	Н	X	Q <sub>0</sub>						
L	<b>†</b>	L	L	L	L						
L	1	L	L	Н	Н						

When either M or N (or both) is (are) high the output is disabled to the high-impedance state; however sequential operation of the flip-flops is not affected.

## \* LOGIC DIAGRAM



## **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> , −0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 70 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-
posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	a = 25°C	KS74AHCT T <sub>a</sub> = -40°C to +85°C	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-6mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	ΔΙςς	per input pin V <sub>1</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

## AC ELECTRICAL CHARACTERISTICS (Input tr, tr <2 ns), AHCT173

Characteristic		Symbol	Cond	itions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	$T_a = -40^{\circ}C$	AHCT C to +85°C OV ± 10%	KS54A T <sub>a</sub> = -55°C t V <sub>CC</sub> = 5.0V	to +125°C	Unit	
					Тур	Min	Max	Min	Max		
Maximum Cloc	k Frequency	f <sub>max</sub>	,		50	30		25		MHz	
Propagation Delay, CLK to any Q		t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF		13 16		21 26		25 31	ns	
		t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF				21 26		25 31	1115	
Propagation D CLR to any Q		t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF		15 18		25 30		30 36	ns	
Output Enable Time, M or N to any Q		t <sub>PZH</sub>	$R_L = 1 k\Omega$	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	12 15	/	20 25		24 30		
W OF N 10 arry	· ·	t <sub>PZL</sub>	UL— 1711	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	12 15		20 25		24 30	ns	
Output Disable	e Time,	t <sub>PHZ</sub>	$R_L = 1 k\Omega$ , C	=50nF	10		17		20	ns	
M or N to any	Q	t <sub>PLZ</sub>	11, 11, 11		10		17		ຸ20	113	
Pulse Width	CLK High or Low	.tw			7	12		15		ns	
Taise Watt	CLR High				7	12		15		113	
	G1 and G2			,	8	15		20			
Setup Time,	Data	t <sub>su</sub>			′ 7	12		15		ns	
before CLK1	CLR Inactive	130			7	12		15			
Hold Time	G1 and G2	th			-3	0		0		ns	
After CLK1	Data	L'n			-3	0		0		113	
Input Capacita	nce	CiN		· ·	5 .					рF	
Output Cipacit	ance	Cout	Output Disa	bled	10					рF	
Power Dissipation Capacitance*		C <sub>PD</sub>								рF	

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.-

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
- $I_{OL} = 8 \text{ mA } @ V_{OL} = 0.5 \text{V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### **DESCRIPTION**

The '174 contains six, and the '175 contains four D-type filp-flops all sharing a common clock and a common clear. The '174 features single nail outputs for every flip-flops whereas the '175 has complementary outputs.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### PIN CONFIGURATIONS

#### 174 CLR [ □ v<sub>cc</sub> 10 [ **□** 60 15 1D 🗀 14 🗖 6D 3 13 5D 2D [ 2Q 🗌 12 5Q зр 🗌 6 11 ☐ 4D 10 40 3Q 🗌 GND [ CLK

#### 175 CLR [ 16 Vcc 1Q [ 15 4Q 1Q 🗆 <u>|</u> 4ā 3 14 1D 🗀 1 4D 13 2D 🗀 I зъ 12 □ 3ā 2Q 🗀 6 11 □ 3Q 2Q [ 10 GND [ CLK

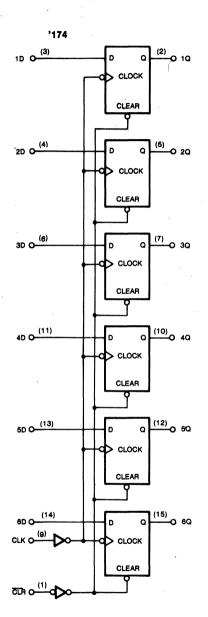
#### **FUNCTION TABLE**

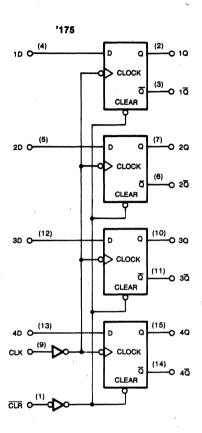
#### (Each Flip-Flop)

ı	nputs	Outputs			
CLR	CLK	D	Q	Q٢	
L	Х	Х	L	I	
Н	^↑	Н	н	L	
Н	<b>↑</b>	L	L	Н	
Н	L	Χ	Qo	Q₀	

† '175 only

## **LOGIC DIAGRAMS**





## **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V)$ ±20 mA
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±35 mA
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, $P_d{}^{\dagger}$ 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-
posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Range KS74AHCT:  $-40^{\circ}$ C to  $+85^{\circ}$ C KS54AHCT:  $-55^{\circ}$ C to  $+125^{\circ}$ C Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . . . Max 500 ns

 Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

## DC ELECTRICAL CHARACTERISTICS (Vcc=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T	a = 25°C	KS74AHCT $T_{a} = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0:8	0.8	٧
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> =20µA I <sub>O</sub> =4mA I <sub>O</sub> =8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μА
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin  V <sub>I</sub> =2.4V  other Inputs: at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0µA		2.7	2.9	3.0	mA

## AC ELECTRICAL CHARACTERISTICS (Input tr, tr≤2 ns), AHCT174, AHCT175

Characteristic		Symbol	Conditions†	T <sub>A</sub> = 25°C V <sub>CC</sub> = 5.0V	KS74AHCT  T <sub>A</sub> = -40°C to +85°C  V <sub>CC</sub> = 5.0V ± 10%		KS54 T <sub>A</sub> = -55°C V <sub>CC</sub> = 5.0	Unit		
				Тур	Min	Max	Min	Max		
Maximum Clock Fr	equency	f <sub>max</sub>		70	50		40		MHz	
Propagation Delay,	•	t <sub>PLH</sub>		11		17₄		20	ns	
CLK to Q or Q		t <sub>PHL</sub>	C <sub>L</sub> =50pF	11		17		20	"	
Propagation Delay,		tpLH		12		21		25	ns	
CLR to Q or Q		t <sub>PHL</sub>		12		21		25	113	
Setup	Data			6	10		15		ns	
Time before CLK1	CLR Inactive	t <sub>su</sub>		4	6		8		113	
Hold Time, Data after CLK1		th		-3	0		0		ns	
Pulse	CLK High or Low	tw		6	10		15		ns	
Width CLR Low		ıw		6	10		15		115	
Input Capacitace		CiN		5					pF	
Power Dissipation	Capacitance*	C <sub>PD</sub>							рF	

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} \ V_{CC}^2 \ f + I_{CC} \ V_{CC}$ .
† For AC switching test circuits and timing waveforms see section 2.

Arithmetic Logic Unit/

## KS54AHCT 181 KS74AHCT

# Preliminary Specifications FEATURES

Arithmetic operating modes:

Addition Subtraction

Shift operand A one position

Magnitude comparison

Plus 12 other arithmetic operations

• Logic function modes:

Exclusive-OR

Comparator

AND, NAND, OR, NOR

Plus 10 other logic operations

- Full look-ahead for high-speed operations on long words
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current Outputs:

 $I_{OL} = 8mA @ V_{OL} = 0.5V$ 

- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATION

Бo	Н	, ~	24	H	V <sub>CC</sub>
ÃO	-		23		
S3			22		
·S2	d	4			Ā2
S1	d	5			<b>B</b> 2
S0	d	6	19	Ь	ĀЗ
C"	d	7	18	Ь	ĒЗ
М	_	_			G
FC	_	-	16	Þ	C,+4
F1	-		15	~	P
·F2			14	Þ	A=B
GND	9	12	13	Р	F3

#### DESCRIPTION

The '181 is an Arithmetic Logic Unit (ALU)/Function Generator that performs 16 binary arithmetic operations on two 4-bit words as shown in table 1 and 2. These operations are selected by the four functions select lines (S0. S1, S2, S3) and include addition, subtraction, decrement and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low level voltage to the mode control input(M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means of 2 cascadeoutputs  $(\overline{P} \text{ and } \overline{G})$  for the 4-bits in the package. When used in conjunction with AHCT182, high-speed arithmetic operation can be performed. The typical addition times shown in table below illustrates how little is required for addition of longer words when full carry look-ahead is employed.

If high speed is not important, a ripple-carry input  $(C_n)$  and a ripple-carry output  $(C_n+4)$  are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small lengths can be performed without external circuitry.

The '181 will accommodate active-high or active-low data, if the pin designations are interpreted as shown below.

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A-B-1, which requires and end-around or forced carry to provide A-B.

The '181 can also be utilized as a comparator. The A=B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of the equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A=B). The ALU should be in the subtract mode with  $C_n$ =H when performing the comparison. The A=B output is open-drain so that it can be wire-AND connected to give a comparison for more than four bits. The carry output  $(C_{n+4})$  can also be used to supply relative magnitude information. Again, the ALU should be placed in the subract mode by placing the function select input S3, S2, S1, S0 at L,H,H,L respectively.

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two boolean variables without the use of external circuitry. These logical functions are selected by use of the four function select inputs (S0, S1, S2, S3) with the mode control input (M) at a high level to disable the internal carry.

The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, OR and NOR functions.

Pin number	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-Low Data (Table1)	$\bar{A}_0$	Βo	Ā <sub>1</sub>	₿₁	A <sub>2</sub>	<b>B</b> ₂	<b>A</b> 3	<b>B</b> ₃	Fo	F <sub>1</sub>	<b>F</b> ₂	F <sub>3</sub>	Cn	C <sub>n</sub> +4	P	Ğ
Active-High Data (Table 2)	A <sub>0</sub>	B <sub>0</sub>	A <sub>1</sub>	B <sub>1</sub>	<b>A</b> <sub>2</sub>	B <sub>2</sub>	<b>A</b> <sub>3</sub>	Вз	F <sub>0</sub>	F <sub>1</sub>	F <sub>2</sub>	Fз	$\overline{\mathbf{C}}_{n}$	$\overline{C}_n + 4$	Х	Υ

## **ALU SIGNAL DESIGNATION**

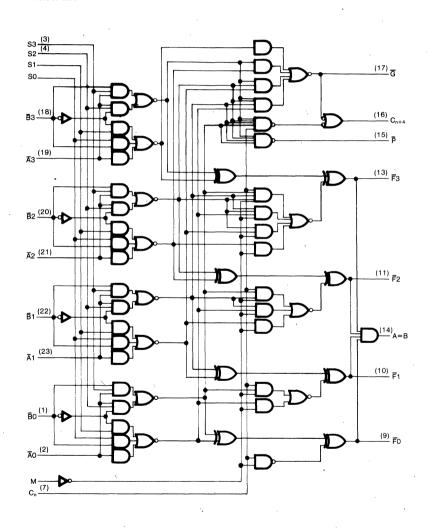
The '181 can be used with the signal designations. The logic functions and arithmetic operations obtained with signal designations as in Table 1.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels

allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{\text{CC}}$  and ground.

## LOGIC DIAGRAM





## O Table 1

	Sala	ction			Active	-Low Data
				M = H	M = L; Arith	metic Operations
S3	S2	<b>S</b> 1	S0	Logic Functions	C <sub>n</sub> =L (no carry)	C <sub>n</sub> =H (with carry)
, L	L	L	L	F=Ā	F=A Minus 1	F=A
L	L	L	Н	F=ĀB	F=AB Minus 1	F=AB
L	L	н	L	F=⊼ + B	F=AB Minus 1	F=AB
L	L	Н	н	F=1	F=Minus 1 (2's Comp)	F=Zero
L	Н	L	L	F=A + B	F=A Plus (A + B)	F=A Plus (A + B) Plus 1
L	н	L	Н	F=B	F=AB Plus (A + B)	F=AB Plus (A + B) Plus 1
L	Н	н	L	F=Ā⊕B	F=A Minus B Minus 1	F=A Minus B
L	Н	Н	Н	F=A + B	F=A + B	F=(A + B) Plus 1
н	L	L	L	F=ĀB	F=A Plus (A + B)	F=A Plus (A + B) Plus 1
Н	L	L	Н	F=A⊕B	F=A Plus B	F=A Plus B Plus 1
н	L	н	L	F=B	F=AB Plus (A + B)	F=AB Plus (A + B) Plus 1
н	L	н	н	F=A + B	F=(A + B)	F=(A + B) Plus 1
н	Н	L	L	F=0	F=A Plus A*	F=A Plus A Plus 1
Н	Н	L	Н	F=AB	F=AB Plus A	F=AB Plus A Plus 1
Н	Н	Н	L	F=AB	F=AB Plus A	F=AB Plus A Plus 1
Н	Н	Н	Н	F=A	F=A	F=A Plus 1

#### O Table 2

	مام؟	ction			Active-High Data					
	0010	Clion		M = H	M = L; Arith	metic Operations				
<b>S</b> 3	S2	S1	S0	Logic Functions	C <sub>n</sub> =L (no carry)	C <sub>n</sub> =H (with carry)				
L	L	L	L	F=Ā	F=A	F=A Plus 1				
L	L	L	Н	$F = \overline{A + B}$	F=A + B	F=(A + B) Plus 1				
L	L	Н	L	F=ĀB	F=A + B	F=(A + B) Plus 1				
L	L	Н	Н	F=0	F=Minus 1 (2's Comp)	F=Zero				
L	Н	L	L	F=AB	F=A Plus AB	F=A Plus AB Plus 1				
L	Н	L	Η.	F=B	F=(A + B) Plus AB	F=(A + B) Plus AB Plus 1				
L	Н	Н	L	F=A⊕B	F=A Minus B Minus 1	F=A Minus B				
L	H.	Н	Н	F=AB	F=AB Minus 1	F=AB				
Н	L	L	L	F=A + B	F=A Plus AB	F=A Plus AB Plus 1				
Н	L	L	Н	F=A⊕B	F=A Plus B	F=A Plus B Plus 1				
Н	L	Н	L	F=B	F=(A + B) Plus AB	F=(A + B) Plus AB Plus 1				
Н	L	. Н	Н	F=AB	F=AB Minus 1	F=AB				
Н	Н	L	L	F=1	F=A Plus A*	F=A Plus A Plus 1				
Н	Н	L	′ <b>H</b>	$F=A + \overline{B}$	F=(A + B) Plus A	A=(A + B) Plus A Plus 1				
н	Н	Н	L	F=A + B	F=(A + B) Plus A	F=(A + B) Plus A Plus 1				
Н	Н	Н	Н	F=A	F=A Minus 1	F=A				

<sup>\*</sup> Each bit is shifted to the next more significant position

## **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, $P_d^{\dagger}$ 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

	ion obeimmi 2 communication
Supply Voltage, Vo	cc 4.5V to 5.5V
DC Input & Output	t Voltages*, V <sub>IN</sub> , V <sub>OUT</sub> OV to V <sub>CC</sub>
Operating Tempera	
Range	KS74AHCT: -40°C to +85°C
	KS54AHCT: -55°C to +125°C
Input Rise & Fall T	imes, t <sub>r</sub> , t <sub>f</sub> Max 500 ns

 Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

## DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V\pm10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	= 25°C	KS74AHCT T <sub>a</sub> =-40°C to +85°C	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
,			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	٧
Maximum Low-Level Input .Voltage	VIL	1		0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> -0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> =20µA I <sub>O</sub> =4mA I <sub>O</sub> =8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μА
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> ⇒V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input in  V <sub>I</sub> =2.4V  other inputs: at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0µA		2.7	2.9	3.0	mA

# INPUT PAIRS HIGH/NOT HIGH TEST TABLE FUNCTION INPUTS: S2 = M = 4.5 V, S0 = S1 = S3 = 0 V

PARAMETER	INPUT UNDER	OTHER INPUT SAME BIT		OTHER DA	TA INPUTS	OUTPUT UNDER	OUTPUT WAVEFORM	
	TEST	APPLY 4.5 V	APPLY GND	APPLY 4.5 V APPLY GND		TEST		
t <sub>PLH</sub>	Αi	Bi	None	Remaining	Remaining	P	In-Phase	
t <sub>PHL</sub>	] ^	ы	None	Ā, C <sub>n</sub>	B		III-Filase	
tpLH	Bi	Āi	None	Remaining	Remaining	P	In-Phase	
t <sub>PHL</sub>	ы	AI .	None	B̄, C <sub>n</sub>	Ā	P	iii-Filase	
t <sub>PHL</sub>	Āi	Bi	None	Remaining	Remaining	C +4	Out of Phase	
t <sub>PHL</sub>	1 ^1	ы	None	Ā, C <sub>n</sub>	B	C <sub>n</sub> +4	Out-of-Phase	
tpLH	- B:	Ā:	None	Remaining	Remaining	C 14	Out-of-Phase	
t <sub>PHL</sub>	Bi Āi		None	B̄, C <sub>n</sub>	Ā	C <sub>n</sub> +4	Out-of-Phase	

#### PARAMETER MEASUREMENT INFORMATION

# $\overline{\text{SUM}} \text{ MODE TEST TABLE} \\ \text{FUNCTION INPUTS: } S0 = S3 = 4.5 \text{ V}, S1 = S2 = M = 0 \text{ V}$

PARAMETER	INPUT UNDER	OTHER INPUT SAME BIT  APPLY 4.5 V APPLY GND		OTHER DA	TA INPUTS	OUTPUT UNDER	OUTPUT WAVEFORM	
	TEST			APPLY 4.5 V	APPLY GND	TEST		
t <sub>PLH</sub>	Āi	Bi	None	Remaining	Cn	Fi	In-Phase	
t <sub>PHL</sub>	<b>A</b>	В	None	A and B	On .		III-F IIase	
t <sub>PLH</sub>	Bi	Āi	None	Remaining		Fi	In-Phase	
t <sub>PHL</sub> .	ы	^'	None	A and B	C <sub>n</sub>	''	in-Friase	
t <sub>PLH</sub>	Āi	Bi	None	None	Remaining	P	In-Phase	
t <sub>PHL</sub>	^	ы	None	None	A and B, C <sub>n</sub>	F	in-Friase	
t <sub>PLH</sub>	Bi	Αi	None	None	Remaining	Ē	In-Phase	
t <sub>PHL</sub>	ы	^'	None	None	$\overline{A}$ and $\overline{B}$ , $C_n$	F		
t <sub>PLH</sub>	Āi	None	Bi	Remaining	Remaining	G	In-Phone	
t <sub>PHL</sub>		None	ы	B	Ā, Cn	G		
t <sub>PLH</sub>	Bi	None	Āi	Remaining	Remaining	G	In-Phase	
t <sub>PHL</sub>	ы	None	Al	B	A, C <sub>n</sub>	G	in-Phase	
t <sub>PLH</sub>	_	None	None	All	All	Any ₹	In-Phase	
t <sub>PHL</sub>	C <sub>n</sub>	None	None	Ā	B	or C <sub>n</sub> +4	III-F Hase	
tpLH	Āi	None	Bi	Remaining	Remaining	Cn+4	Out-of-Phase	
tphL	"	None	ы	B ₁	Ā, C <sub>n</sub>	Un <sup>™4</sup>	Out-of-Filase	
tpLH	Bi	None	Āi	Remaining	Remaining	Cn+4	Out-of-Phase	
t <sub>PHL</sub>	ы	None	Al	B	Ā, C <sub>n</sub>	Un <sup>∓4</sup>	Out-of-Phase	

## AC ELECTRICAL CHARACTERISTICS (Input t<sub>r</sub>, t<sub>i</sub>≤2 ns), AHCT181

Characteristic	Symbol	Conditions <sup>†</sup>	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V			T <sub>a</sub> = -55°C	AHCT to +125°C V± 10%	Unit
		C <sub>L</sub> = 50pF	Тур	Min	Max	Min	Max	
Propagation Delay,	t <sub>PLH</sub>	M=0V,	8		14		17	ns
C <sub>n</sub> to C <sub>n</sub> +4	tpHL	Sum or Diff Mode	8	,	14		. 17	,,,,
Propagation Delay,	tpLH	M=S1=S2=0V	16		24		29	ns
Ā or B̄ to C <sub>n</sub> +4	t <sub>PHL</sub>	S0=S3=4.5V	16		24		29	
Propagation Delay,	T <sub>PLH</sub>	M=S0=S3=0V	17		25		30	ns
A or B to C <sub>n</sub> +4	t <sub>PHL</sub>	S1=S2=4.5V	17		25		30	113
Propagation Delay	tpLH	M=S1=S2=0V	17		25		30	ns
A or B to G	tpHL	S0=S3=4.5V	17		25		30	113
Propagation Delay	tpLH	M=S0=S3=0V	17		25		30	ns
A or B to G	tpHL	S1=S2=4.5V	17		25		30	113
Propagation Delay	tpLH	M=S0=S3=0V	15		23		27	ns
Ā or B to P	tpHL	S1=S2=4.5V	15		23		27	113
Propagation Delay	tpLH	M=S1=S2=0V	16		24		29	ns
Ā or B to P	tpHL	S0=S3=4.5V	16		24		29	113
Propagation Delay	t <sub>PLH</sub>	M=S1=S2=0V	20		29		35	ns
Ā or B to Fi	tpHL	S0=S3=4.5V	20		29		35	113
Propagation Delay	tpLH	M=S0=S3=0V	19		27		32	ns
A or B to Fi	tpHL	S1=S2=4.5V	19		27		32	113
Propagation Delay	tpLH	M=4.5V	16		24		29	ns
Ā or B to F;	tpHL	W=4.5V	16		24		29	115
Propagation Delay	tpLZ	M=S0=S3=0V	19		27		32	ns
A or B to A=B	t <sub>PZL</sub>	S1=S2=4.5V	16		24		29	118
Propagation Delay	tpLH		15		23		24	
C <sub>n</sub> to any F	t <sub>PHL</sub>		15		23		27	ns
Input Capacitance	Cin		5					pF
Power Dissipation Capacitance*	<del> </del>							pF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

#### PARAMETER MEASUREMENT INFORMATION

LOGIC MODE TEST TABLE FUNCTION INPUTS: S1 = S2 = M = 4.5 V, S0 = S3 = 0 V

PARAMETER	INPUT UNDER	OTHER INPUT SAME BIT		OTHER DA	TA INPUTS	OUTPUT UNDER	OUTPUT WAVEFORM	
	TEST APPLY 4.5 V APPLY GNI		APPLY GND	APPLY 4.5 V	APPLY GND	TEST		
tpLH	Āi	- Bi	None	None	Remaining	Fi	Out-of-Phase	
t <sub>PHL</sub>	7"	J 5			A and B, C <sub>n</sub>			
t <sub>PLH</sub>	Bi	Āi	None	None	Remaining	Fi	Out-of-Phase	
t <sub>PHL</sub>			None	None	$\overline{A}$ and $\overline{B}$ , $C_n$	''	Out-of-Friase	

# INPUT BITS EQUAL/NOT EQUAL TEST TABLE FUNCTION INPUTS: $S0=S3=M=4.5\ V,\ S1=S2=0\ V$

PARAMETER	INPUT UNDER	OTHER INPUT SAME BIT		OTHER DA	TA INPUTS	OUTPUT	OUTPUT WAVEFORM	
	TEST	APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND	TEST		
t <sub>PLH</sub>	Āi	Bi	None	Remaining	None	Ē	Out-of-Phase	
t <sub>PHL</sub>	A	5,	140/16	$\overline{A}$ and $\overline{B}$ , $C_n$	None	'	Out of I flase	
tpLH	Bi	Āi	None	Remaining	None	P	Out-of-Phase	
t <sub>PHL</sub>	اب	<u> </u>	None	Ā and B, C <sub>n</sub>	None		Out-or-Friase	
tpLH	Āi	None	Bi	Remaining	None	Ē	In-Phase	
t <sub>PHL</sub>	Λ'	None	Б,	Ā and B, C <sub>n</sub>	None		III TRACC	
tpLH	Bi	Bi None Āi Remaining None		None	P	In-Phase		
t <sub>PHL</sub>	ы	None	Λ'	$\overline{A}$ and $\overline{B}$ , $C_n$	None		11,1,1100	
tpLH	Āi	Bi	None	Remaining	None	Cn+4	In-Phase	
t <sub>PHL</sub>	^'	ы	None	$\overline{A}$ and $\overline{B}$ , $C_n$	140116	On 14	III Hase	
tpLH	Bi	Āi	None	Remaining	None	C <sub>n</sub> +4	In-Phase	
t <sub>PHL</sub>	Di.	^'	None	Ā and B, C <sub>n</sub>	140/16	On 1 4	iiii iiase	
tрын	Āi	None	Bi	Remaining	None	Cn+4	Out-of-Phase	
t <sub>PHL</sub>		NOILE	ы	Ā and Ē, C <sub>n</sub>	INOHE	On 1 7	Out-oi-i iidəe	
tplH	Bi	None	Āi	Remaining	None	C <sub>n</sub> +4	Out-of Phase	
t <sub>PHL</sub>	Di	None	^'	$\overline{A}$ and $\overline{B}$ , $C_n$	None	Un <sup>∓</sup> ∓		

#### $\overline{\text{DIFF}}$ MODE TEST TABLE FUNCTION INPUTS: S1 = S2 = 4.5 V, S0 = S3 = M = 0 V

PARAMETER	INPUT UNDER	NDER SAME BIT		OTHER DA	TA INPUTS	OUTPUT UNDER	OUTPUT WAVEFORM	
	TEST			APPLY 4.5 V APPLY GND		TEST		
t <sub>PLH</sub>	Āi	None	Bi	Remaining	Remaining	Fi	In-Phase	
t <sub>PHL</sub>	Α'	None	Di	Ā	B, C <sub>n</sub>		III-FIIdoe	
t <sub>PLH</sub>	Bi	Āi	None	Remaining	Remaining	Fi	Out-of-Phase	
t <sub>PHL</sub>	Di .	^'	None	Ā	B, C <sub>n</sub>	11	Out-or-mase	
<b>t</b> PLH	Āi	None	Bi	None	Remaining	P	In-Phase	
t <sub>PHL</sub>	Δ'	None	Di	None	$\overline{A}$ and $\overline{B}$ , $C_n$		in-Phase	
t <sub>PLH</sub>	Bi	Āi	None	None	Remaining	P	Out-of-Phase	
t <sub>PHL</sub>	ы	<u></u>	None	None	$\overline{A}$ and $\overline{B}$ , $C_n$		Jul 31 / Habi	
t <sub>PLH</sub>	Āi	Bi	None	None	Remaining	G	In-Phase	
t <sub>PHL</sub>	Λ'	, ,	None	None	$\overline{A}$ and $\overline{B}$ , $C_n$	_ u	111111111111111111111111111111111111111	
t <sub>PLH</sub> ·	Bi	None	Āi	None	Remaining	G	Out-of-Phas	
t <sub>PHL</sub>	Di	None	Λ'	None	$\overline{A}$ and $\overline{B}$ , $C_n$	<u> </u>	Jul Of Fila	
t <sub>PLH</sub>	Āi	None	Bi	Remaining	Remaining	A=B	In-Phase	
t <sub>PHL</sub>	^'	None	Di	Ā	B, C <sub>n</sub>	A-B	III-I IIaoc	
t <sub>PLH</sub>	Bi	Āi	None	Remaining	Remaining	A=B	Out-of-Phase	
t <sub>PHL</sub>	Di	^'	None	Ā	B, C <sub>n</sub>	A-B	Out-of-Phase	
t <sub>PLH</sub>	Cn	None	None	All	None	C <sub>n</sub> +4	In-Phase	
t <sub>PHL</sub>	On .	,,,,,,,	110110	$\overline{A}$ and $\overline{B}$	110110	or any F	iii i ilaac	
t <sub>PLH</sub>	Āi	Bi	None	None	Remaining	C <sub>n</sub> +4	Out-of-Phase	
t <sub>PHL</sub>	AI .	Di	NOHE	INOLIG	A, B, C <sub>n</sub>	On 1 4	Out-or-rilase	
t <sub>PLH</sub>	Bi	None	Āì	None	Remaining	Cn+4	In-Phase	
ten		1	1	1	A. B. Cn	-"		





- Compatible Carry Functions for direct ALU connection
- Cascadable to perform look-ahead across n-bit adders.
- High output current drive: I<sub>OL</sub> = 8mA @ V<sub>OL</sub> = 0.5V
- Low power consumption characteristic of CMOS
- Direct interface capability to TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATION



#### DESCRIPTION

The '182 is a high-speed, look-ahead carry generator, capable of anticipating a carry across four binary adders or group of adders. These devices can be cascaded to perform full look-ahead across n-bit adders. Carry, generate-carry, and propagate-carry functions are provided as shown in the pin designation table.

When used in conjuction with the AHCT181 arithmetic logic unit, these generators provide high-speed carry look-ahead capability for any word length. Each 182 generates the look-ahead (anticipated carry) across a group of four ALUs and, in addition, other carry look-ahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to n-bits. The method of cascading circuits to perform multi-level look-ahead is illustrated under typical application data.

Carry input and output of the ALU's are in their true from, and the carry propagate (P) and carry generate (G) are in negated form; therefore, the carry functions (inputs, outputs, generate, and propagate) of the look-ahead generators are implemented in the compatible forms for direct connection to the ALU. Reinterpretations of carry functions, as explained on the 181 data sheet are also applicable to and compatible with the look-ahead generator. Logic equations for the 182 are:

Cn+x=G0 + P0 Cn Cn+y=G1 + P1 G0 + P1 P0 Cn Cn+z=G2 + P2 G1 + P2 P1 G0 + P2 P1 P0 Cn G=G3 + P3 G2 + P3 P2 G1 + P3 P2 P1 G0 P=P3 P2 P1 P0

#### PIN DESIGNATIONS

Designation Pin No		Function			
<u>G0,G1,G2,G</u> 3 3,1,14,5		Active Low Carry Generate Inputs			
PO,P1,P2,P3 4,2,15,6		Active Low Carry Propagate Inputs			
Cn 13		Carry Input, Active HIGH			
Cn+x, Cn+y, Cn+z	12,11,9	Carry Outputs			
· G	10	Active Low Carry Generate Output			
P	7	Active Low Carry Propagae Output			
· Vcc	16	Supply Voltage			
GND	8	Ground			

## **FUNCTION TABLES**

#### FOR G OUTPUT

	OUTPUT								
ĞЗ	G2	<b>G</b> 1	ĞΘ	P3	P̄2	₽1	Ğ		
L	X	Х	Х	Х	X	×	L		
X	L	Χ	Χ	L	Χ	Х	L		
X	Χ	L	Χ	L	L	Х	L		
X	Χ	X	L	۱ L	L	L	L		
	All other combinations								

FOR	Ρ(	JUT	PU	T

	• .
. INPUTS	OUTPUT
P3 P2 P1 P0	P
LLLL	L
All other combinations	н

FOR	C <sub>n</sub> +	X	OUTPUT	

IN	IPUT	OUTPUT			
G0	PO C <sub>n</sub>		C <sub>n</sub> +,x		
L	хх		·H		
Х	L	Н	н		
1	l othe binat	L			

Cn+y OUTPUT

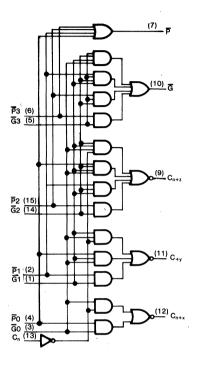
	OUTPUT				
G1	<del>G</del> 0	₽1	P0	Cn	C <sub>n+y</sub>
L	Х	Х	X	Х	н
X	L	. L	Х	Х	н
X	Х	L	L	Н	н
	L				

· Cn+z OUTPUT

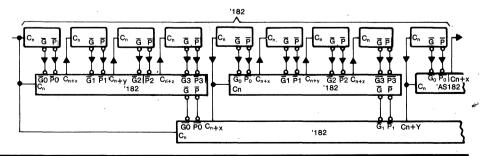
	OUTPUT						
Ğ2	G1 GO P2 P1 PO Cn					C <sub>n</sub> +z	
L	Х	Х	Х	Х	х	Х	Н
X	L	Х	L	Х	Χ	Х	Н
X	Х	L	L	L	Х	Χ	н
X	XXXLLL					Н	Н
L	All other combinations						

H = high-level, L = low level, X = don't careAny inputs not shown in a given table are don't care with respect to that output.

## **LOGIC DIAGRAM**



#### Figure; THE '182 IN A 64-BIT LOOK-AHEAD CARRY CIRCUIT



## **Absolute Maximum Ratings\***

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	Ta	= 25°C	KS74AHCT T <sub>a = -40°C</sub> to +85°C	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	d Limits	
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	V <sub>CC</sub> 4.2	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> -0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

## AC ELECTRICAL CHARACTERISTICS (Input tr, tr<2 ns), AHCT182

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	KS74AHCT T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> =5.0V±10%		KS54AHCT  T <sub>a</sub> = -55°C to +125°C  V <sub>CC</sub> =5.0V ± 10%		Unit
			Тур	Min	Max	Min	Max	
Propagation Delay,	tpLH	C <sub>L</sub> =50pF	12		20		24	ns
Pi or Gi to C <sub>n+x</sub> C <sub>n+y</sub> , C <sub>n+z</sub>	t <sub>PHL</sub>	OL-30bi	12		20		24	113
Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pF	.12		20		24	ns
Pi or Gi to G	tPHL		12		20		24	
Propagation Delay,	tplH	C <sub>L</sub> =50pF	15		21		26	ns
C <sub>n</sub> to C <sub>n+x</sub> , C <sub>n+y</sub> , C <sub>n+z</sub>	tPHL	OL-30pi	15		21		26	
Propagation Delay	t <sub>PLH</sub>	C <sub>L</sub> =50pF	11		18		21	ns
Pi to P	tpHL	OL-30pi	11		18		21	
Input Capacitance	CiN		5					pF
Power Dissipation Capacitance*	C <sub>PD</sub>							рF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} \ V_{CC}^2 \ f + I_{CC} \ V_{CC}$ .
† For AC switching test circuits and timing waveforms see section 2.

- · For use in high-speed wallace-tree summing
- · Fast addition operation
- Low power consumption characteristic of CMOS
- High output current drive: I<sub>OL</sub> = 8mA @ V<sub>OL</sub> = 0.5V
- Direct interface capability with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to + 85°C KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

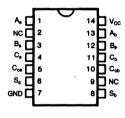
#### DESCRIPTION

The '183 is a dual full adder features an individual carry output from each bit for use in multiple-input, carry-save techniques to produce the true sum and true carry outputs with no more than 2 gate delays.

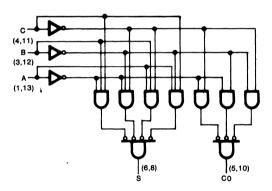
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### PIN CONFIGURATION



#### **LOGIC DIAGRAM**



#### **FUNCTION TABLE**

(Each Half)

	Inputs		Out	put
Α	В	С	S	C <sub>o</sub>
L	L	L	L	L
Н	L	L	Н	L
L	н	L	Н	L
L	L	н	Н	L
н	н	L	L	н
н	L	н	L	н
L	н	Н	L	н
н	н	н	l H	н

## **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 70 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation

of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:

Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Supply Voltage, V<sub>CC</sub> . . . . . . . . . . . 4.5V to 5.5V DC Input & Output Voltages\*, V<sub>IN</sub>, V<sub>OUT</sub> . . OV to V<sub>CC</sub> Operating Temperature

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . Max 500 ns

 Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

#### DC ELECTRICAL CHARACTERISTICS (Voc=5V+10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	τ,	= 25°C	KS74AHCT T <sub>a</sub> = -40°C to +85°C	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
,		Ĺ	Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-4m A$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> -0.1 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> =20µA I <sub>O</sub> =4mA I <sub>O</sub> =8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	lin	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input in  V <sub>I</sub> =2.4V  other inputs: at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0µA		2.7	2.9	3.0	mA

## AC ELECTRICAL CHARACTERISTICS (Input tr., tr46 ns), AHCT183

Characteristic	Symbol C	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	KS74AHCT T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%		KS54AHCT T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> =5.0V ± 10%		Unit	
			Тур	Min	Max	Min	Max		
Propagation Delay	tpLH	C <sub>L</sub> =50pF	10		15		18	ns	
. ropagation Dojay	tpHL	OL-COP!	13		20		24	]	
Input Capacitance	CIN		5					pF	
Power dissipation Capacitance*	CPD							pF	

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} \ V_{CC}^2 \ f \ + \ I_{CC} \ V_{CC}$ .

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

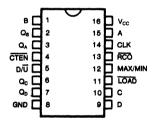


- · Single down/up count control line
- Look-ahead circuit enhances speed of cascaded counters
- Fully synchronous in count modes
- Asynchronously presettable with load control
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- **High-Drive-Current outputs:**
- IOL = 8 mA @ VOL = 0.5V
- . Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- · Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

## PIN CONFIGURATION



#### **FUNCTION TABLE**

OPERATING MODE		INPUTS								
OPERATING MODE	LOAD	D/Ū	CTEN	CLK	Input	On				
parallel load	L L	×	X	X X	L H	L H				
count up	Н	L	1	†	X	count up				
count down	Н	Н	1	†	х	count dow				
hold (do nothing)	Н	Х	Н	Х	×	no change				

RCO AND MAX/MIN FUNCTION TABLE

	INPUTS		TERI	MINAL C	OUTPUTS			
D/Ū	CTEN	CLK	QA	QB	Qc	Qp	MAX/MIN	RCO
н	Н	х	н	×	х	Н	L	н
L	H	X	н	x	'x	н	Н 1	н
L	L	T	н	X	X	н	1 7	ਪ
L	н	х	L	L	L	L	L	н
н	н	х	L	L	L	L	н	н
н	L	J.	L	L	L	l L	1 7	ਪ

- H = HIGH voltage leve
- LOW voltage level
- LOW voltage level one setup time prior to the LOW-to-HIGH CLK transition
- = Don't care = LOW-to-HIGH CLK transition
- T = one LOW level puls
- L = MAX/MIN goes LOW ON A LOW-to-HIGH CLK transition

#### DESCRIPTION

These are high-speed synchronous reversible 4-bit decade counters. Synchronous counting operation is provided by having all flip-flops clocked simultaneously so that the outputs change with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered on a low-tohigh-level transition of the clock input if the enable input (CTEN) is low. A high at CTEN inhibits counting. The direction of the count is determined by the level of the down/up  $(D/\overline{U})$  input. When  $D/\overline{U}$  is low, the counter counts up and when D/U is high, it counts down.

These counters feature a fully independent clock circuit. Changes at the control inputs ( $\overline{CTEN}$  and  $D/\overline{U}$ ) that will modify the operating mode have no affect on the contents of the counter until clocking occurs. The function of the counter will be dictated solely by the condition meeting the stable setup and hold times.

These counters are fully programmable; that is, the outputs may each be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

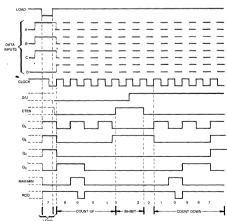
Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock while the count is zero (all outputs low) counting down or maximum (9 or 15) counting up. The ripple clock output produces a low-level output pulse under those same conditions but only while the clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V<sub>CC</sub> and

# LOGIC DIAGRAM (12) <u>CO</u> (13) BO UP (4) DOWN LOAD

#### Typical load, count, and inhibit sequences



#### Sequence;

- (1) Load (preset) to BCD seven.
- (2) Count up to eight, mine(maximum) zero, one, and two.
- (3) Inhibit
- (4) Count down to one, zero (minimum), nine, egiht, and seven

NOTE A: Clear overrides load data, and count inputs.

Note B:When count up, count-down input must be high;
when counting down, countup intput must be high.

## **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_{I} < -0.5V \text{ or } V_{I} > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW

<sup>\*</sup> Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . Max 500 ns

\* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	Ta	= 25°C	KS74AHCT $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧.
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> -0.1	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	\ \
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

## AC ELECTRICAL CHARACTERISTICS (Input t<sub>r</sub>, t<sub>f</sub>≤2 ns), AHCT190

Chi	aracteristic	Symbol	Conditions <sup>†</sup>	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	Į.	AHCT C to +85°C OV±10%	KS54A T <sub>a</sub> = -55°C V <sub>CC</sub> = 5.0°	to +125°C	Unit
	,	:		Тур	Min	Max	Min	Max	
Maximum Clo	ck Frequency	f <sub>max</sub>		50	30		25		MHz
Propagation D	Delay,	t <sub>PLH</sub> .		18		30		36	ns
LOAD to any	Q	t <sub>PHL</sub>		18		30		36	
Propagation D	Delay,	tplH		13		21		25	ns
A,B,C, D to a	ny Q	t <sub>PHL</sub>	,	13		21		25	110
Propagation D	Delay,	tpLH		12		20		24	ns
CLK to RCO		t <sub>PHL</sub>		12		20		24	110
Propagation D	Delay,	t <sub>PLH</sub>		11		18		22	ns
CLK to any Q	) ·	t <sub>PHL</sub>	C <sub>L</sub> =50pF	11.		18		22	110
Propagation D			CL-50PF	19		31		37	ns
CLK to MAX/I	MIN	t <sub>PHL</sub>	L	19		31		37	
Propagation D	n Delay,			19		32		38	ns.
D/Ū to RCO		tpHL	PHL	19		32		38	116.
Propagation D	Delay,			15		25 `		30	
D/U to MAX/N		t <sub>PHL</sub>		15		25		30	1
Propagation D	Delay,	t <sub>PLH</sub>		11		18		22	200
CTEN to RCC		t <sub>PHL</sub>		11		18		22	ns
Pulse Width	CLK High or Low			10		17		20	ns
ruise Widti	LOAD Low	t <sub>w</sub>		12		20		25	115
	Data before LOAD1		1	10	17	,	20		
Setup Time	CTEN before CLK1	t <sub>su</sub>		10	17		20		ns
Getup Time	D/Ū before CLK↑	Lsu		10	17		20		1115
	LOAD Inactive before CLK1			10	17		20		
	Data after LOAD1			2	4		5		
Hold Time	CTEN after CLK1	th		-3	0		0 ,		ns
	D/Ū after CLK↑			-3	0		0		]
Input Capacita	ance	C <sub>IN</sub>		5					pF
Power Dissipa	ation Capacitance*	C <sub>PD</sub>		80					рF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} \ V_{CC}^2 \ f + I_{CC} \ V_{CC}$ .

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

- Single down/up count control line
- Look-ahead circultry enhances speed of cascaded counters
- · Fully synchronous in count modes
- Asynchronously presettable with load control
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:

IoL = 8 mA @ VoL = 0.5V

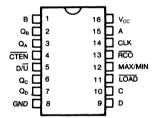
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATION



#### **FUNCTION TABLE**

OPERATING MODE		INPUTS								
OFENATING MODE	LOAD	D/Ū	CTEN	CLK	Input	On				
parallel load	L L	X X	X	X X	L . H	L H				
count up	Н	L	1	t	Х	count up				
count down	н	н		†	Х	count down				
hold (do nothing)	н	X	н	Х	X	no change				

RCO AND MAXIMIN FUNCTION TABLE

	INPUTS		TER	MINAL C	OUTPUTS			
D/Ū	CTEN	CLK	QA	QB	Qc	QD	MAX/MIN	RCO
н	Н	Х	Н	X	X	Н	L	Н
L	н	X	н	х	X	Н	/ H	н
L	L	T	н	X	X	Н	T.	T
L	Н	X	L	L	L	L	L	н
н	Н	Х	L	L	L	L	н	н
н	L	T	L	L	L	L	1 7	T

- H. = HIGH voltage level
- L = LOW voltage level
- I = LOW voltage level one setup time prior to the LOW-to-HIGH CLK transition
- X = Don't care
- ↑ = LOW-to-HIGH CLK transition
- ∪ = one LOW level pulse
- T.= MAX/MIN goes LOW ON A LOW-to-HIGH CLK transition

#### DESCRIPTION

These are high-speed synchronous, reversible 4-bit binary counters. Synchronous counting operation is provided by having all flip-flops clocked simultaneously so that the outputs change with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered on a low-to-high-level transition of the clock input if the enable input  $(\overline{CTEN})$  is low. A high at  $\overline{CTEN}$  inhibits counting. The direction of the count is determined by the level of the down/up  $(D/\overline{U})$  input. When  $D/\overline{U}$  is low, the counter counts up and when  $D/\overline{U}$  is high, it counts down.

These counters feature a fully independent clock circuit. Changes at the control inputs  $(\overline{CTEN})$  and  $D/\overline{U}$  that will modify the operating mode have no affect on the contents of the counter until clocking occurs. The function of the counter will be dictated solely by the condition meeting the stable setup and hold times.

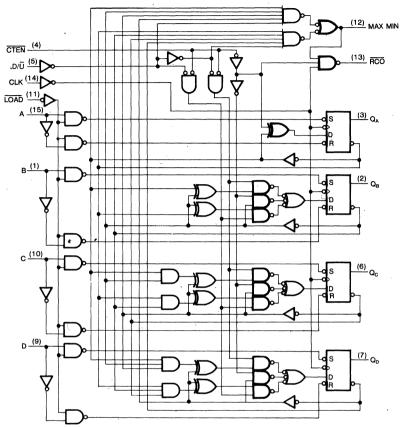
These counters are fully programmable; that is, the outputs may each be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock while the count is zero (all outputs low) counting down or maximum (9 or 15) counting up. The nipple clock output produces a low-level output pulse under those same conditions but only while the clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

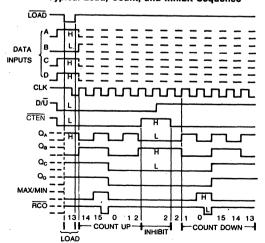
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

## **LOGIC DIAGRAM**



Typical Load, Count, and Inhibit Sequence



#### Sequence:

- (1) Load (preset) to binary thirteen
- (2) Count up to fourteen, fifteen, zero, one, and two
- (3) Inhibit
- (4) Count down to one, zero, fifteen, fourteen, and thirteen

## **Absolute Maximum Ratings\***

Supply Voltage Range $V_{CC}$ , $-0.5V$ to $+7V$
DC Input Diode Current, I <sub>IK</sub>
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Gutput Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V)$ ±20 mA
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW
* Absolute Maximum Ratings are those values beyond

which permanent damage to the device may occur.

These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

## **Recommended Operating Conditions**

Supply Voltage,	V <sub>CC</sub> 4	.5V to 5.5V				
DC Input & Outp	out Voltages*, V <sub>IN</sub> , V <sub>OUT</sub>	. OV to Vcc				
Operating Temperature						
Range	KS74AHCT: -40°C	C to +85°C				
	KS54AHCT: -55°C	to +125°C				
Input Rise & Fall	Times, $t_r$ , $t_f$	Max 500 ns				

Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T <sub>a</sub> = 25°C		KS74AHCT T <sub>a</sub> = -40°C to +85°C	KS54AHCT $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$	Unit
			Тур	Guaranteed Limits			
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	VIL			0:8	0.8	0.8	V
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> -0.1 3.84	V <sub>CC</sub> -0.1 3.7	V
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin  V <sub>I</sub> =2.4V  other lħputs:  at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

<sup>†</sup> Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## AC ELECTRICAL CHARACTERISTICS (Input tr, tr≤2 ns), AHCT191

Characteristic		Symbol	Conditions <sup>†</sup>	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	KS74AHCT $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Тур	Min	Max ·	Min	Max	
Maximum Clock Frequency		f <sub>max</sub>		50	30		25		MHz
Propagation Delay, LOAD to any Q		t <sub>PLH</sub>		18		30		36	ns
		t <sub>PHL</sub>		18		30	·	36	
Propagation Delay,		tpLH	t <sub>PLH</sub>	13		21		25	ns
A,B,C, D to a	ny Q	t <sub>PHL</sub>		13		21		25	"
Propagation Delay, CLK to RCO		tplH		12		20		24	ns
		t <sub>PHL</sub>		12		20		24	
Propagation Delay,	tplH		11		18		22	ns	
CLK to any Q		t <sub>PHL</sub>	C <sub>L</sub> =50pF	11		18		22	110
Propagation Delay, CLK to MAX/MIN		t <sub>PLH</sub>		19		31		37	ns
		t <sub>PHL</sub>		19		31		37	1115
Propagation Delay,	t <sub>PLH</sub>		19		32		38	ns	
D/Ū to RCO			t <sub>PHL</sub>	19		32			- 38
Propagation D	Delay,	t <sub>PLH</sub>		15		25		30	
D/Ū to MAX/MIN	t <sub>PHL</sub>		15		25		30		
Propagation Delay.	t <sub>PLH</sub>		· 11		18		22	ne	
CTEN to RCC	)	t <sub>PHL</sub>		11		18		22	ns
Pulse Width	CLK High or Low	t <sub>w</sub>		10		17		20	ns
T dise (Width	LOAD Low			12		20		25	
Setup Time	Data before LOAD1			10	17		20		- ns
	CTEN before CLK1	tsu		10	17		20	,	
	D/Ū before CLK1			10	17		20		
	LOAD Inactive before CLK1			10	17		20		
Hold Time	Data after LOAD↑	th		2	4		5		
	CTEN after CLK1			-3	0		0		ns
	D/Ū after CLK↑			-3	0		0		
Input Capacitance		CIN		5					pF
Power Dissipation Capacitance*		C <sub>PD</sub>		80					pF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

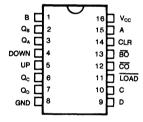
<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

- Look-ahead circuit enhances cascaded counters
- Fully synchronous in count modes
- Parallel asynchronous load for modulo-N count lenaths
- Asynchronous clear
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
  - IOL = 8 mA @ VOL = 0.5V
- . Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- · Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATION



#### **FUNCTION TABLE**

**OPERATING MODE** 

reset (clear)

paraiel load

count up

#### L Н 1 Н Н count down

LOAD

Х

Χ

L

L

L

L

CLR

Н

н

L

L

1

1

\* CO=Up at terminal count up (HHHH) \*\* BO=Down at terminal count down (LLLL)

H = HIGH voltage level

Х L = LOW voltage level

X = don't care

INPUTS

DOWN

Н

L

Н

Х

Х

Α В C D Q۵

Х

Х Х Х Х

L L L L L

L L L L L

Н

Н Х Х Н

Х Х Х Х

Х

Х Х

Х Χ Н Α

UP

Х

Х

Х

Х

ı

Н

↑ = LOW to HIGH clock transition

Χ

#### DESCRIPTION

These are high-speed synchronous reversible 4-bit decade counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered by a low-tohigh-level transition of either count (clock) input (Up or Down). The direction of counting is determined by which count input is pulsed while the other count input is high.

All four counters are fully programmable; that is, each output may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided that forces all outputs to the low level when a high level is applied. The clear function is independent of the count and the load inputs.

These counters were designed to be cascaded without the need for external circuitry. The borrow output (BO) produces a low-level pulse while the count is zero (all outputs low) and the count-down input is low. Similarly, the carry output (CO) produces a low-level pulse while the count is maximum (9 or 15) and the count-up input is low. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and countup inputs, respectively, of the succeeding counter.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V<sub>CC</sub> and ground.

**OUTPUTS** 

Qc

L

L

L

L

С

 $Q_D$ 

L

L

D

D

 $Q_B$ 

L

L

L

L

В

В

count up

count down

L

CO

Н

Н

Н

١

Н

H\*

BO

L

Н

L

Н

Н

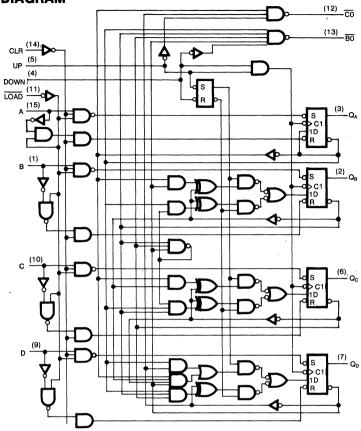
Н

Н

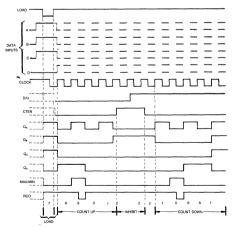
H\*\*



## **LOGIC DIAGRAM**



#### Typical load, count, and inhibit sequences



#### Sequence;

- (1) Load (preset) to BCD seven.
- (2) Count up to eight, mine(maximum) zero, one, and two.
- (3) Inhibit
- (4) Count down to one, zero (minimum), nine, egiht, and seven

NOTE A: Clear overrides load data, and count inputs.

Note B:When count up, count-down input must be high;
when counting down, countup intput must be high.

## **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
(-0.5V < V <sub>O</sub> < V <sub>CC</sub> +0.5V) ±35 mA
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW
* Absolute Maximum Ratings are those values beyond

Storage Temperature Range, T<sub>stg</sub>...-65°C to +150°C Power Dissipation Per Package, P<sub>d</sub>†.......500 mW \* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): -12mW/°C from 65°C to 85°C
Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

## DC ELECTRICAL CHARACTERISTICS (Vcc=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	Т	a = 25°C	KS74AHCT T <sub>a</sub> = -40°C to +85°C	<b>KS54AHCT</b> T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V <sub>OH</sub>	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> =-20μA I <sub>O</sub> =-4mA	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> -0.1 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	VOL	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> =20µA I <sub>O</sub> =4mA I <sub>O</sub> =8mA	o	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	IN	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μА
Maximum Quiescent Supply Current	loc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0µA		8.0	80.0	160.0	μА
Additional Worst Case Supply Current	ΔΙος	per input in V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND lout=0µA		2.7	2.9	3.0	mA

## AC ELECTRICAL CHARACTERISTICS (Input tr, tr≤2 ns), AHCT192

(	Characteristic	Symbol	Conditions <sup>†</sup>	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	Ta = -40°	AHCT C to +85°C DV±10%	Ta = -55°C	AHCT to +125°C 0V ± 10%	Unit
				Тур	Min	Max	Min	Max	
Maximum Cl	ock Frequency	f <sub>max</sub>		50	30		25		MHz
Propagation	Delay,	t <sub>PLH</sub>		11		18		22	ns
UP to CO	,	t <sub>PHL</sub>	,	11		18		22	
Propagation	Delay,	t <sub>PLH</sub>		11		18		22	ns
DOWN to an		t <sub>PHL</sub>	C <sub>L</sub> =50pF	11		18		22	110
Propagation	Delay,	t <sub>PLH</sub>		11		19	,	23	ns
UP or DOW	or DOWN to any Q			11		19		23	
Propagation	Delay,	t <sub>PLH</sub>		17		29	,	35	ns
LOAD to any	DAD to any Q			17		29		35	113
Propagation CLR to any		t <sub>PLH</sub>		10		17		20	ns
	CLR High			6	10		15		
	LOAD Low	tw		10	17		20		ns
Pulse Width	UP or DOWN High or Low			10	17		20		
	Data before LOAD1			10	17		29		
,	CLR Inactive before UP1 or DOWN1			· 10	17		20		
Setup Time	LOAD Inactive before UP1 or DOWN1	t <sub>su</sub>		10	17		20		ns
	UP high before DOWNt			10	17		17		
	Down high before UP1	1		8	15		15		
	Data after LOAD1			-3	0		0		
Hold Time	UP High after DOWN1	th		-3	0		0		ns
	DOWN High after UP			3	8		6		1
nput Capacitance		CIN		5			,		рF
Power Dissip	ation Capacitance*	CPD		80					рF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

#### **FEATURES**

- · Look-ahead circuitry enhances cascaded counters
- · Fully synchronous in count modes
- Parallel asynchronous load for modulo-N count lengths
- Asynchronous clear
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:

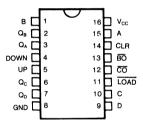
I<sub>OL</sub> = 8 mA @ V<sub>OL</sub> = 0.5V

- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### **PIN CONFIGURATION**



#### **FUNCTION TABLE**

#### **DESCRIPTION**

These are high-speed synchronous reversible 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered by a low-tohigh-level transition of either count (clock) input (Up or Down). The direction of counting is determined by which count input is pulsed while the other count input is high.

All four counters are fully programmable; that is, each output may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided that forces all outputs to the low level when a high level is applied. The clear function is independent of the count and the load inputs.

These counters were designed to be cascaded without the need for external circuitry. The borrow output  $(\overline{BO})$  produces a low-level pulse while the count is zero (all outputs low) and the count-down input is low. Similarly, the carry output  $(\overline{CO})$  produces a low-level pulse while the count is maximum (9 or 15) and the count-up input is low. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and countup inputs, respectively, of the succeeding counter.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{\text{CC}}$  and ground.

OPERATING MODE				INPUTS							OUT	PUTS		
OF ENATING MODE	CLR	LOAD	UP	DOWN	Α	В	С	D	QA	QB	Qc	QD	CO	BO
	Н	Х	Х	L	X	Х	Х	Х	L	L	L	L	Н	L
reset (clear)	Н	Х	Х	Н	X	X	Х	X	L	L	L	L	Н	Н
	L	L	Х	L	L	L	L	L	L	L	L	L	Н	L
a and that the aid	L	L	X	H	L	L	L	L	L	L	L	L	Н	Н
parailel load	L	L	L	X	Н	Н	Н	Н	Н	Н	Н	Н	L	н
	L	L	Н	Х	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
count up	L	Н	1	. Н	Х	Х	Х	Х		cou	nt up		H*	. Н
count down	L	Н	Н	1	Х	Х	Х			count	down		Н	H**

H= HIGH voltage level

↑= LOW-to-HIGH clock transition

L= LOW voltage lovel

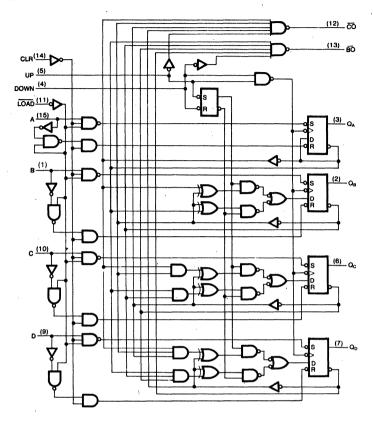
\* CO = UP at terminal count up (HHHH)

X= don't care

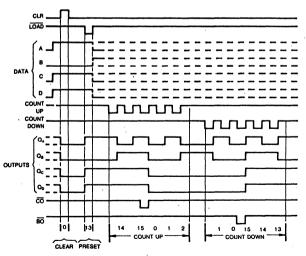
\*\* BO = DOWN at terminal count down (LLLL)



## **LOGIC DIAGRAM**



Typical Clear, Load, and Count Sequences



#### Sequence:

- (1) Clear outputs to zero.
- (2) Load (preset) to binary thirteen.
- (3) Count up to fourteen, fifteen, carry, zero, one and two.
- (4) Count down to one, zero, borrow, fifteen, fourteen, and thirteen.

Note A: Clear overrides load data, and count inputs.

Note B: When counting up, count-down input must be high; when counting down, count-up input must be high.

## **Absolute Maximum Ratings\***

Supply Voltage Range $V_{CC}$ , $-0.5V$ to $+7V$
DC Input Diode Current, I <sub>IK</sub>
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V)$ ±20 mA
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±35 mA
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation

of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Supply Voltage, V<sub>CC</sub> . . . . . . . . . 4.5V to 5.5V DC Input & Output Voltages\*, V<sub>IN</sub>, V<sub>OUT</sub> . . . OV to V<sub>CC</sub> Operating Temperature

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . Max 500 ns

\* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	, = 25°C	KS74AHCT $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Uni			
			Тур		Guaranteed Limits					
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	٧			
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧			
Minimum High-Level Output Voltage	Voh	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> -0.1	V <sub>CC</sub> −0.1 3.7	v			
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V			
Maximum Input Current	liN	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ			
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ			
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA			

## AC ELECTRICAL CHARACTERISTICS (Input t<sub>r</sub>, t<sub>i</sub>≤2 ns), AHCT193

	Characteristic	Symbol	Conditions <sup>†</sup>	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	Ta = - 40°0	AHCT C to +85°C DV ± 10%	T <sub>a</sub> = -55°C	AHCT to +125°C V± 10%	Unit
				Тур	Min	Max	Min	Max	
Maximum Cl	ock Frequency	f <sub>max</sub>		50	30		25		MHz
Propagation	Delay,	t <sub>PLH</sub>		11		18		22	ns
UP to CO		t <sub>PHL</sub>	ľ	11		18	,	22	
Propagation		tpLH		11		18		22	ns
DOWN to an	y Q	tpHL	C <sub>L</sub> =50pF	11		18		22	
Propagation		tpLH		11		19		23	ns
UP or DOW	N to any Q	t <sub>PHL</sub>		11		19		23	
Propagation		tpLH		17		29		35	ns
LOAD#to any	, Q	t <sub>PHL</sub>		17		29		35	
Propagation CLR to any		t <sub>PLH</sub>		10		17	,	20	ns
	CLR High			6	10		15		
	LOAD Low	tw		10	17		20		'ns
Pulse Width	UP or DOWN High or Low			10	17		20		
	Data before LOAD1			10	17		29		
	CLR Inactive before UP1 or DOWN1			10	17		20		
Setup Time	LOAD Inactive before UP1 or DOWN1	t <sub>su</sub>		10	17		20		ns
	UP high before DOWN1			10	17		17		
	Down high before UP1	1		8	15		15		
	Data after LOAD↑			-3	0		0		
Hold Time	UP High after DOWN1	th		-3	0		0		ns
	DOWN High after UP1			3	8		6		
Input Capaci	tance	CIN		5					pF
Power Dissip	pation Capacitance*	C <sub>PD</sub>		80					pF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

#### **FEATURES**

- Parallel-to-Serial, Serial-to-Parallel Conversions
- · Left or Right Shifts
- Parallel Synchronous Loading
- Direct Overriding Clear
- Temporary Data Latching Capability
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
  - IOL = 8 mA @ VOL = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### DESCRIPTION

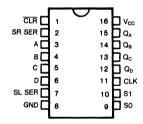
These bidirectional shift registers feature parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation:

- Inhibit clock (temporary data latch/do nothing)
- Shift-right (in the direction QA toward QD)
- Shift-left (in the direction QD toward QA)
- Parallel (broadside) load

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, SO and S1, high. The data is loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift-right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial inputs. Clocking of the flip-flop is inhibited when both mode control inputs are low.

#### PIN CONFIGURATION



#### **FUNCTION TABLE**

			INP	UTS							OUTP	UTS	
CLR	МС	DE	01.4	SE	RIAL	P	\R/	<b>ALL</b>	EL	0.	0-	0-	0-
CLR	S1	SO	CLK	LEFT	RIGHT	A	В	С	D	QA	QB	Qc	QD
L	Х	Х	X	X	Х	Х	Х	Х	Х	L	L	L	L
Н	Х	Х	L	X	Χ	X	Χ	Х	Х	Q <sub>AO</sub>	$Q_{B0}$	$Q_{C0}$	$Q_{D0}$
Н	Н	н	<b>↑</b>	X	Χ	a	b	С	d	а	b	С	d
Н	L	н	<b>↑</b>	X	Н	X	Х	Χ	Х	H	$Q_{An}$	$Q_{Bn}$	Q <sub>Cn</sub>
Н	L	н	<b>†</b>	X	L	Х	Х	Х	Х	L	$Q_{An}$	$Q_{Bn}$	Q <sub>Cn</sub>
Н	Н	L	<b>↑</b>	Н	Χ	X	Х	Χ	Х	Q <sub>Bn</sub>	$\mathbf{Q}_{\text{Cn}}$	$Q_{DN}$	Н
Н	Н	L	<b>↑</b>	L	Χ	X	Х	Χ	Х	Q <sub>Bn</sub>	Q <sub>Cn</sub>	$Q_{Dn}$	L
н	L	L	Х	Х	Х	X	Χ	Х	Х	QAO	$Q_{B0}$	$Q_{C0}$	$Q_{D0}$

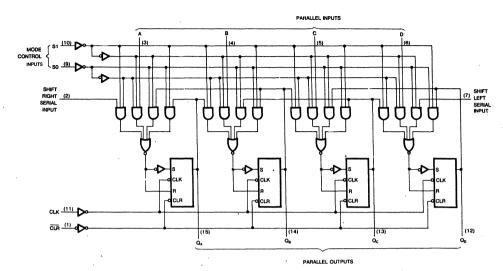
H=high level (steady state) L=low level (steady state)

X=irrelevant (any input, including transitions)

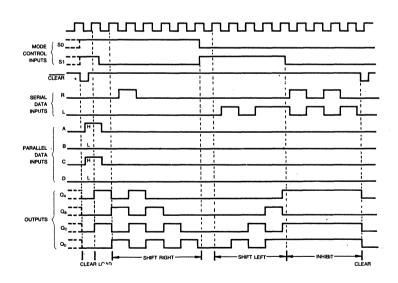
↑=transition from low to high level a,b,c,d=the level of steady-state input at inputs A,B,C, or D, respectively.

Q<sub>A0</sub>, Q<sub>B0</sub>, Q<sub>C0</sub>, Q<sub>D0</sub>=the level of Q<sub>A</sub>, Q<sub>B</sub>, Q<sub>C</sub>, or Q<sub>D</sub>, respectively, before the indicated steady-state input conditions were established.

Q<sub>An</sub>, Q<sub>Bn</sub>, Q<sub>Cn</sub>, Q<sub>Dn</sub>=the level of Q<sub>A</sub>, Q<sub>B</sub>, Q<sub>C</sub>, respectively, before the most-recent ↑ transition of the clock.



typical clear, load, right-shift, inhibit, and clear sequences



## **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> , −0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW
* Absolute Maximum Ratings are those values beyond

which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Supply Voltage, V<sub>CC</sub> . . . . . . . . . . 4.5V to 5.5V DC Input & Output Voltages\*, VIN, VOUT ... OV to VCC Operating Temperature

KS74AHCT: -40°C to +85°C Range KS54AHCT: -55°C to +125°C Input Rise & Fall Times, tr, tf . . . . . . . Max 500 ns

\* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

## DC ELECTRICAL CHARACTERISTICS (VCC=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	Ta	= 25°C	KS74AHCT T <sub>a</sub> = -40°C to +85°C	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	. VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> -0.1	v
Maximum Low-Level Output Voltage		$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	Q	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

## AC ELECTRICAL CHARACTERISTICS (Input t<sub>r</sub>, t<sub>i</sub>≤2 ns), AHCT194

Cha	racteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	$T_a = -40^\circ$	IAHCT C to +85°C OV±10%	T <sub>a</sub> = -55°C	AHCT to +125°C IV ± 10%	Unit
	A second			Тур	Min	Max	Min	Max	
Maximum Clo	ck Frequency	f <sub>max</sub>		60	35		30		MHz
Propagation [	Delay,	tpLH	]	10		17		20	ns
CLK to Q <sub>H</sub>	•	t <sub>PHL</sub>	C <sub>L</sub> =50pF	10		17		20	113
Propagation I	Delay,	t <sub>PHL</sub>	,	11		19		22	ns
Pulse Width	CLR LOW	tw		10	17		20		ns
ruise Width	CLK High or LOW	l w		10	17		20		. 113
Setup Time, Any Input bet	ore CLKf	ts		10	17		20		ns
Hold Time, Data after CL	K†	ts		-3	0		0		ns
Input Capacit	ance	CIN		5					pF
Power Dissip	ation Capacitance*	C <sub>PD</sub>		80					pF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

#### **FEATURES**

- Parallel-to-Serial, Serial-to-Parallel Conversions
- · Parallel Synchronous Loading
- J and K Inputs to First Stage
- Right-shift Only with Complementary Outputs on Last Stage
- Direct Overriding Clear
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:

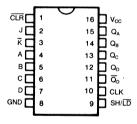
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5 \text{V}$ 

- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATION



#### DESCRIPTION

These 4-bit rigisters feature parallel inputs, parallel outputs, J- $\overline{K}$  serial inputs, shift/load control input, and a direct overriding clear. The registers have two modes of operation:

Parallel (broadside) load

Shift (in the direction AA toward QD)

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data are loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading serial data flow is inhibited.

Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-K inputs. These inputs permit the first stage to perform as a J-K, D-, or T-type flip-flop as shown in the function table.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### **FUNCTION TABLE**

		INPUTS								OUTF	OUT	s	
CLR	SH/LD	CLK	SEF	RIAL	PA	R/	۱LL	.EL	QA	QB	Qc	Qn	$\overline{\mathbf{Q}}_{\mathbf{D}}$
CEN	SI1/LD	CLK	J	ĸ	A	В	С	D	U <sub>A</sub>	αB	СС	Uр	uр
L	Х	Х	Х	Х	Х	Х	Х	Х	L	L	L	L	Н
Н	L	1	Х	Х	a	b	С	d	а	b	С	d	d
Н	Н	L	X	Χ	X	Χ	Х	Χ	Q <sub>AO</sub>	$Q_{B0}$	$Q_{C0}$	$Q_{D0}$	$\overline{Q}_{DO}$
н	Н	1	L	Н	Х	Х	Х	Х	Q <sub>AO</sub>	$Q_{AO}$	$Q_{Bn}$	Qcn	$\overline{Q}_{Cn}$
Н	Н	1	L	L	X	Х	Х	Х	L	$Q_{An}$	$Q_{Bn}$	Qcn	$\overline{Q}_{Cn}$
Н	Н	↑	Н	Н	X	Х	Х	Х	Н	$Q_{An}$	$Q_{Bn}$	Qcn	$\overline{\mathbb{Q}}_{Cn}$
Н	Н	1	Н	L	X	Χ	Χ	Х	Q <sub>An</sub>	$Q_{\text{An}}$	$\mathbf{Q}_{\text{Bn}}$	$\mathbf{Q}_{\text{Cn}}$	$\overline{\mathbf{Q}}_{Cn}$

H=high level (steady state)

L=low level (steady state)
X=irrelevant (any input, in

X=irrelevant (any input, including transitions)

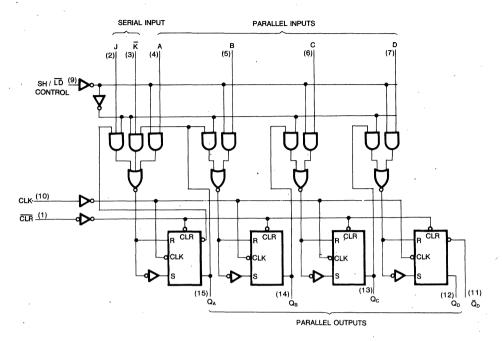
1=transition from low to high level

a,b,c,d=the level of steady-state input at A,B,C, or D, respectively.

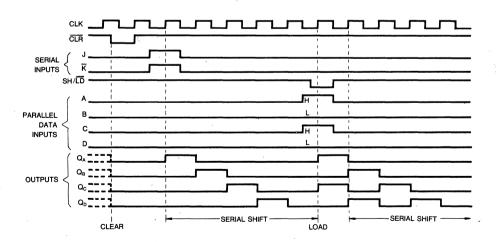
Q<sub>A0</sub>, Q<sub>B0</sub>, Q<sub>C0</sub>, Q<sub>D0</sub>=the level of Q<sub>A</sub>, Q<sub>B</sub>, Q<sub>C</sub>, or Q<sub>D</sub>, respectively, before the indicated steady-state input conditions were established.

Q<sub>An</sub>, Q<sub>Bn</sub>, Q<sub>Cn</sub>=the level of Q<sub>A</sub>, Q<sub>B</sub> or Q<sub>C</sub>, respectively, before the mostrecent transition of the clock.

## **LOGIC DIAGRAMS**



typical clear, shift, and load sequences



## **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±35 mA
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, $T_{stg} \dots -65^{\circ}C$ to $+150^{\circ}C$
Power Dissipation Per Package, $P_d^{\dagger}$ 500 mW
<ul> <li>Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.</li> </ul>
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-
posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Supply Voltage, V <sub>CC</sub>	4.5V to 5.5V
DC Input & Output Voltages	", VIN, VOUT UV TO VCC
Operating Temperature	

Range KS74AHCT:  $-40\,^{\circ}\text{C}$  to  $+85\,^{\circ}\text{C}$  KS54AHCT:  $-55\,^{\circ}\text{C}$  to  $+125\,^{\circ}\text{C}$  Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . . . Max 500 ns

 Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	= 25°C	KS74AHCT T <sub>a</sub> = -40°C to +85°C	KS54AHCT T <sub>a=</sub> -55°C to +125°C	Unit
	,		Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	Voh	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	V <sub>CC</sub> 4.2	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> -0.1 3.84	V <sub>CC</sub> -0.1 3.7	v
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin  V <sub>I</sub> =2.4V  other Inputs: at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0µA		2.7	2.9	3.0	mA

## AC ELECTRICAL CHARACTERISTICS (Input tr, tr<2 ns), AHCT195

Characteristic		Symbol	Conditions <sup>†</sup>	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	$T_a = -40^{\circ}$	AHCT C to +85°C DV ±10%	$T_a = -55$ °C	AHCT to +125°C V± 10%	Unit
	•			Тур	Min	Max	Min	Max	
Maximum Clo	ck Frequency	f <sub>max</sub>		60	35		30		MHz
Propagation [	Delay,	tpLH		10	,	17		20	ns
CLK to Q <sub>H</sub>		t <sub>PHL</sub>	C <sub>L</sub> =50pF	10		17		20	113
Propagation Delay, CLR to Q <sub>H</sub>		t <sub>PHL</sub>		. 11		19		22	ns
Pulse Width	CLR Low	tw		10	17		20		ns
ruise Width	CLK High or Low	·w		10	17		20		113
Satura Time	SH/LD High			10	17		20		
Setup Time before CLK1	Serial or Parallel Data •	t <sub>su</sub>		10	17		20		ns
	CLR inactive	1		10	17		20		
Hold Time	SH/LD High			-3	0		0		ns
after CLK1	Serial or Parallel Data			-3	0		0		
Input Capacita	ance	CIN		5					рF
Power Dissipa	ation Capacitance*	C <sub>PD</sub>							рF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} \ V_{CC}^2 \ f \ + \ I_{CC} \ V_{CC}$ .

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

#### **FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
   The Address of - I<sub>OL</sub> = 24 mA @ V<sub>OL</sub> = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
- KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

## **DESCRIPTION**

These high-speed octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The designer has the choice of combinations of inverting non-inverting outputs and symmetrical complementary input control (both active-low, or one active-low, the other active-high).

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

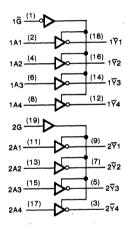
#### **PIN CONFIGURATION**



#### **FUNCTION TABLE**

in	out	Output
G	Α	Υ
L	L	Н
L	Н	L
Н	Х	Z

#### **LOGIC DIAGRAM**



## **Absolute Maximum Ratings\***

Supply Voltage Range $V_{CC}$ , $-0.5V$ to $+7V$
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 70 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-

posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Supply Voltage, V <sub>CC</sub>	4.5V to 5.5V
DC Input & Output Voltages*, VIN, VOUT	OV to Vcc
Operating Temperature	

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>t</sub> . . . . . . . . . . Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	a = 25°C	KS74AHCT $T_{a=}-40^{\circ}\text{C to }+85^{\circ}\text{C}$	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
		/	Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}^{\bullet}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-6mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=12mA$ $I_{O}=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ





## AC ELECTRICAL CHARACTERISTICS (Input tr, tres 2 ns), AHCT210

Characteristic	Symbol	Conditions <sup>†</sup>		ol Conditions†		T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	Ta = -40°0	AHCT C to +85°C OV±10%	Ta = -55°C	AHCT to +125°C V ± 10%	Unit
				Тур	Min	Max	Min	Max			
Propagation Delay,	t <sub>PLH</sub>		C <sub>L</sub> =50pF C <sub>L</sub> =150pF			10 15		12 18			
A to Y	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF		7 11		10 16		12 19	ns		
Output Enable Time, Enable to $\overrightarrow{Y}$	t <sub>PZH</sub>	R <sub>L</sub> =1kΩ	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	12 15		20 25	,	24 30	ns		
	tpzL		TIL-TRU		TIE-TRE	C <sub>L</sub> =50pF C <sub>L</sub> =150pF			20 25		24 30
Output Disable Time,	t <sub>PHZ</sub>	R <sub>L</sub> =1kΩ		13		18		22	ns		
Enable to ₹	tpLZ	C <sub>L</sub> =50pF	=	13		18		22	113		
Input Capacitance	CIN			5					рF		
Output Capacitance	Cout	Output D	isabled	10					рF		
Power Dissipation Capacitance*	C <sub>PD</sub> *	Output Di Output Ei		5 30					рF		

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} \ V_{CC}^2 \ f + I_{CC} \ V_{CC}$ .
† For AC switching test circuits and timing waveforms see section 2.

#### **FEATURES**

- Designed specifically for high-speed memory decoders and data transmission systems.
- Incorporates 2 enable inputs to simplify cascading and/or data reception
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
  - IoL = 8 mA @ VoL = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### DESCRIPTION

These devices are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can be used with high-speed memories utilizing a fast enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

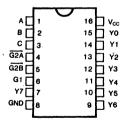
This conditions at the binary select inputs and the three enable inputs select one of eight input lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding.

A 24-line decoder can be implemented without external inverters and a 31-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{\text{CC}}$  and ground.

#### PIN CONFIGURATION



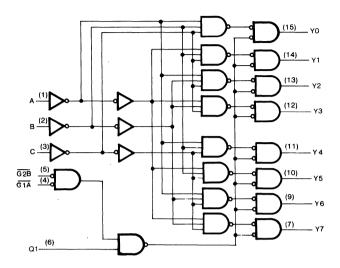
#### **FUNCTION TABLE**

Enable Inputs		1 -	ele		Outputs							
G1	G2*	С	В	A	YO	Y1	Y2	Y3	Y4	Y5	Y6	<b>Y7</b>
Х	Н	X	Х	Х	L	L	L	L	L	L	L	L
L	Х	X	Х	Х	Ŀ	L	L	L	L	L	L	L
Н	L	L	L	L	Н	L	L	L	L	L	L	L
Н	L	L	L	Н	L	Н	L	L	L	L	L	L
Н	L	L	н	L	L	L	Н	L	L	L	L	L
Н	L	Н	L	L	L	L	L	Н	L	L	L	L
Н	L	Н	L	L	L	L	, L	L	Н	L	L	L
Н	L	Н	L	Н	L	L	L	L	L	Н	L	L
н	L	Н	н	L	L	L	L	L	L	L	Н	L
Н	L	Н	Н	Н	· L	L	L	L	L	L	L	Н

\* G2=G2A+G2B



#### LOGIC DIAGRAM



## **Absolute Maximum Ratings\***

•
Supply Voltage Range V <sub>CC</sub> , −0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . . . . Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	A = 25°C	KS74AHCT T <sub>A</sub> = -40°C to +85°C	KS54AHCT T <sub>A</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	v
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	Vон	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	VoL	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> =20µA I <sub>O</sub> =4mA I <sub>O</sub> =8mA	0	0.1 0.26 0.39	0.1 0.33 . 0.5	0.1 0.4	v
Maximum Input Current	l <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

## AC ELECTRICAL CHARACTERISTICS (Input tr, tre2 ns), AHCT238

Characteristic	Symbol	Conditions†	T <sub>A</sub> = 25°C V <sub>CC</sub> = 5.0V	KS74AHCT  T <sub>A</sub> = -40°C to +85°C  V <sub>CC</sub> = 5.0V ± 10%		KS54AHCT  T <sub>A</sub> = -55°C to +125°C  V <sub>CC</sub> = 5.0V ± 10%		Unit
			Тур	Min	Max	Min	Max	
Propagation Delay,	t <sub>PLH</sub>		12		20		24	ns
A, B, C or Y	t <sub>PHL</sub>		12		20		24	113
Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pF	· 10		17		20	ns
G1 to any Y	t <sub>PHL</sub>		10		17		20	
Propagation Delay,	t <sub>PLH</sub>	,	10		17		20	ne
G2A or G2B to any Y	tPHL		10		17		20	ns
Input Capacitance	CIN		5					рF
Power Dissipation Capacitance*	C <sub>PD</sub>		50					рF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} \ V_{CC}^2 \ f + I_{CC} \ V_{CC}$ .

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

#### **FEATURES**

- Designed specifically for high-speed memory decoders and data transmission systems
- Incorporates 2 enable inputs to simplify cascading and/or data reception
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
  - IOL = 8 mA @ VOL = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### DESCRIPTION

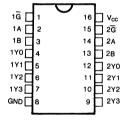
These devices are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times in high-performance memory systems, these decoders can be used to minimize the effects of system decoding. When used with high-speed memories utilizing a fast-enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory.

This means that the effective system delay introduced by the decoder is negligible.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{\text{CC}}$  and ground.

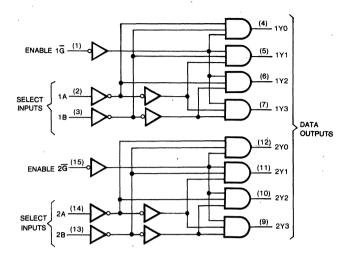
#### PIN CONFIGURATION



#### **FUNCTION TABLE**

In	puts			Out	puts	
Enable	Se	lect	YO	Y1	Y2	Y3
Ğ	В	Α	10	11	12	13
Н	Х	Х	L	L	L	L
L	L	L.	Н	L	L	L.
L	L	Н	L	Н	L	L
L	Н	L	L	L	Н	L
L	Н	Н	L	L	L	Н

## **LOGIC DIAGRAM**



## **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_0 < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> −65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Input Rise & Fall Times,  $t_{r},\ t_{f}$  . . . . . . . . Max 500 ns

 Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	Т,	a = 25°C	KS74AHCT T <sub>a</sub> = -40°C to +85°C	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit	
			Тур	Guaranteed Limits				
Minimum High-Level Input Voltage	VIH			2.0	2.0	2.0	٧	
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧	
Minimum High-Level Output Voltage	V <sub>ОН</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> -0.1 3.7	٧	
Maximum Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> =20µA I <sub>O</sub> =4mA I <sub>O</sub> =8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v	
Maximum Input Current	liN	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ	
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA	1	8.0	80.0	160.0	μΑ	
Additional Worst Case Supply Current	Δlcc	per input pin  V <sub>I</sub> =2.4V  other Inputs: at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0µA		2.7	2.9	3.0	mA	

## AC ELECTRICAL CHARACTERISTICS (Input tr, tr <2 ns), AHCT239

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	KS74AHCT T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%		KS54AHCT $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Тур	Min	Max	Min	Max	
Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pF	12		20		24	ns
A or B to any Y	t <sub>PHL</sub>		12		20		24	
Propagation Delay,	t <sub>PLH</sub>		10		17		20	
G to any Y	t <sub>PHL</sub>		10		17		20	
Input Capacitance	CIN		5					pF
Power Dissipation Capacitance*	C <sub>PD</sub>		50					pF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} \ V_{CC}^2 \ f + I_{CC} \ V_{CC}$ .

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

## KS54AHCT **240/241/244** Octal Buffers and Line Drivers KS74AHCT with 3-State Outputs

#### **FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with drive current (loL = 24 mA @ VoL = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### DESCRIPTION

These high-speed octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

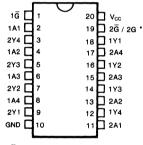
The designer has the choice of combinations of inverting/ non-inverting outputs and symmetrical complementary input control (both active-low, or one active-low, the other active-high).

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

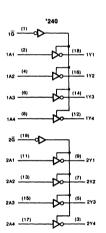
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{\text{CC}}$  and ground.

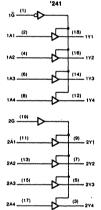
#### PIN CONFIGURATION

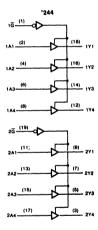
## LOGIC DIAGRAMS



\*2G for '240 and '244 2G for '241







#### **FUNCTION TABLE**

			'241, '244	'240	
Input			Output	Output	
G	G	A	Y	Y	
Н	L	L	L	Н	
Н	L	н	Н	L	
L	Н	X	Z	Z	

# KS54AHCT **240/241/244** Octal Buffers and Line Drivers KS74AHCT with 3-State Outputs

## **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 70 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW
* Absolute Maximum Patings are those values beyond

<sup>\*</sup> Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . . Max 500 ns

 Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	a = 25°C	KS74AHCT $T_{a=-40^{\circ}\text{C to }+85^{\circ}\text{C}$	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Uni	
			Тур		Guaranteed Limits			
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	v	
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧	
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-6mA$	V <sub>CC</sub> 4.2	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> -0.1 3.7	v	
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=12mA$ $I_{O}=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v	
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ	
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	. ±10.0	μΑ	
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ	



# KS54AHCT **240/241/244**Octal Buffers and Line Drivers KS74AHCT with 3-State Outputs

## AC ELECTRICAL CHARACTERISTICS (Input tr, tr≤2 ns), AHCT240, AHCT241, AHCT244

Characteristic	Symbol	Conditions†		Conditions <sup>†</sup>		T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	$T_a = -40^\circ$	AHCT C to +85°C 0V±10%	KS54. T <sub>a</sub> = -55°C V <sub>CC</sub> = 5.0	to +125°C	Unit
				Тур	Min	Max	Min	Max			
	tpLH	C <sub>L</sub> =50pF C <sub>L</sub> =150r	C <sub>L</sub> =50pF			10 15		12 18			
Propagation Delay, A to Y		C <sub>L</sub> =50pF C <sub>L</sub> =150pF		9 6 9		10		12 18	ns		
Output Enable Time,	t <sub>PZH</sub>	R <sub>L</sub> =1kΩ	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	12 15		20 25		24 30	ns		
Enable to Y	t <sub>PZL</sub>		C <sub>L</sub> =50pF C <sub>L</sub> =150pF	12 15		20 25		24 30			
Output Disable Time.	t <sub>PHZ</sub>	R <sub>L</sub> =1kΩ		13		18		22	ns		
Enable to Y	tPLZ	C <sub>L</sub> =50pF		13		18		22	113		
Input Capacitance	CiN		,						рF		
Output Capacitance	Cout	Output D	Output Disabled						рF		
Power Dissipation Capacitance*	C <sub>PD</sub>		Output Disabled Output Enabled						pF		

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

#### 4

## **FEATURES**

- 2-Way Asynchronous Communication Between Data Buses
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current
- ( $I_{OL} = 24 \text{ mA}$  @  $V_{OL} = 0.5 \text{V}$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

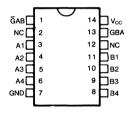
KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

Package ontions include plastic '

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

## PIN CONFIGURATION



#### DESCRIPTION

These four-data line transceivers are designed for asynchronous two-way communications between data buses.

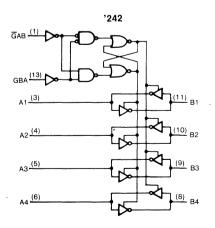
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

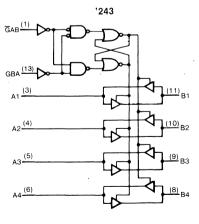
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### **FUNCTION TABLE**

INPUTS		1040			
ĞАВ	GBA	'242	'243		
L	L	Ā to B	A to B		
Н	Н	B to A	B to A		
Н	L	Isolation	Isolation		
L	Н	Isolation	Isolation		

#### LOGIC DIAGRAMS





## **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 70 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW
* Absolute Maximum Ratings are those values beyond

Storage lemperature Range, T<sub>stg</sub>... -65°C to +150°C Power Dissipation Per Package, P<sub>d</sub>†........ 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

DC Input & Ou		4.5V to 5.5V $\ensuremath{\text{V}_{\text{OUT}}}$ 0V to $\ensuremath{\text{V}_{\text{CC}}}$
Operating Tem	perature	
Range	KS74AHCT:	-40°C to +85°C
	MOTALIOT.	EE00 4- 140E00

Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T <sub>a</sub> = 25°C		KS74AHCT T <sub>a</sub> = -40°C to +85°C	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-6mA$	V <sub>CC</sub> 4.2	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

## AC ELECTRICAL CHARACTERISTICS (Input tr., tr <2 ns), AHCT242, AHCT243

Characteristic	Symbol					KS54 T <sub>a</sub> = -55°C V <sub>CC</sub> = 5.0	Unit		
				Тур	Min	Max	Min	Max	
Propagation Delay, A to B or B to A	tpLH	C <sub>L</sub> =50pF C <sub>L</sub> =150pF C <sub>L</sub> =50pF C <sub>L</sub> =150pF		7 10		11 16		15 21	ns
	t <sub>PHL</sub>			7 10		11 16		15 21	115
Output Enable Time	tpzH	R <sub>L</sub> =1kΩ	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	12 15		20 25		25 21	ns
GAB to B, GBA to A	t <sub>PZL</sub>		C <sub>L</sub> =50pF C <sub>L</sub> =150pF	12   15		20 25		25 21	
Output Disable Time,	tpHZ	$R_L = 1 k\Omega$		12		20		25	ns
GAB to B, GBA to A	tPLZ	C <sub>L</sub> =50pF		12		20		25	IIS
Input Capacitance	CIN			5					pF
Output Capacitance	Соит	Output D	Output Disabled						pF
Power Dissipation Capacitance*(per stage)	C <sub>PD</sub>	1 -	Output Enabled Output Disabled						рF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

## Octal Bus Transceivers with 3-State Outputs

#### **FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current
   (I<sub>OL</sub> = 24 mA @ V<sub>OL</sub> = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### DESCRIPTION

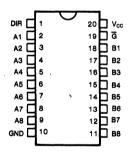
These high-speed octal bus transceivers are designed for synchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction control (DIR) input. The enable input  $(\overline{G})$  can be used to disable the device so that the buses are effectively isolated.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

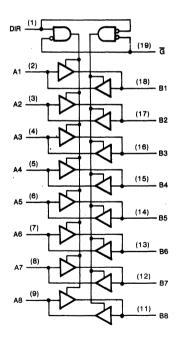
#### PIN CONFIGURATION



#### **FUNCTION TABLE**

Inputs		Operation					
Ğ	DIR	Operation					
L	L	Bus B Data to Bus A					
L	Н	Bus A Data to Bus B					
Н	Х	Isolation					

## **LOGIC DIAGRAM**



## **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, IIK
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 70 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Supply Voltage, V<sub>CC</sub> . . . . . . . . . . . . 4.5V to 5.5V DC Input & Output Voltages\*, V<sub>IN</sub>, V<sub>OUT</sub> . . OV to V<sub>CC</sub> Operating Temperature

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C Input Rise & Fall Times,  $t_r, t_f$  . . . . . . Max 500 ns

 Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

#### DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T <sub>a</sub> = 25°C		KS74AHCT Ta = -40°C to +85°C	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V <sub>IH</sub>	_		2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-6mA$	V <sub>CC</sub> 4.2	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> -0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=12mA$ $I_{O}=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

## AC ELECTRICAL CHARACTERISTICS (Input tr, tr <2 ns), AHCT245

Characteristic	1 1		T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	KS74AHCT T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%		KS54 T <sub>a</sub> = -55°C V <sub>CC</sub> = 5.0	Unit		
				Тур	Min	Max	Min	Max	
Propagation Delay,	tpLH		C <sub>L</sub> =50pF C <sub>L</sub> =150pF			10 15		14 20	ns
A to B or B to A	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF		6 9		10 15		14 20	ris
Output Enable Time	tpzH	-R <sub>L</sub> =1kΩ	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	12 15		20 25		25 31	ns
G to A or B	t <sub>PZL</sub>	וונ – ואש	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	12 17		20 25		25 31	
Output Disable Time,	t <sub>PHZ</sub>	R <sub>L</sub> =1kΩ		13		18		22	ns
G to A or B	tPLZ	C <sub>L</sub> =50pF	•	13		18		22	""
Input Capacitance	CIN			5					pF
Output Capacitance	Cout	Output Di	Output Disabled						pF
Power Dissipation Capacitance*	C <sub>PD</sub>	G=V <sub>CC</sub> G=GND	(per stage)	5 30					рF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} \ V_{CC}^2 \ f \ + \ I_{CC} \ V_{CC}$ .

 $<sup>^{\</sup>dagger}$  For AC switching test circuits and timing waveforms see section 2.

#### **FEATURES**

- Three-State Version of '151
- Three-State Outputs Interface Directly with System Bus
- · Performs Parallel-to-Serial Conversion
- Complementary Outputs Provide True and Inverted Data
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current
   (I<sub>OL</sub> = 24 mA @ V<sub>OL</sub> = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### DESCRIPTION

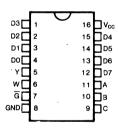
These data selectors/multiplexers contain full binary decoding to select one-of-eight data sources and feature strobe-controlled complementary three-state outputs.

The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state), the low-impedance of the single enabled output will drive the bus line to a high or low logic level. Both outputs are controlled by the strobe ( $\overline{G}$ ). The outputs are disabled when  $\overline{G}$  is high.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{\text{CC}}$  and ground.

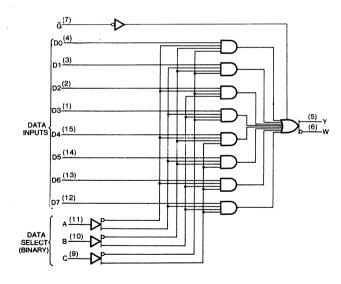
#### PIN CONFIGURATION



#### **FUNCTION TABLE**

		INP	UTS	OUTI	PUTS
SE	LEC	CT	STROBE	ν.	w
С	В	A	Ğ	•	•••
Х	Х	Х	н	Z	Z
L	L	L	L	DO	DO
L	L	Н	L	D1	D1
L	Н	L	L	D2	D2
L	Н	Н	L	DЗ	D3
Н	L	L	L	D4	D4
Н	L	Н	L	D5	D5
Н	Н	L	L	D6	D6
Н	Н	Н	L	D7	D7

#### **LOGIC DIAGRAM**



# 1-of-8 Data Selectors/Multiplexers with 3-State Outputs

## **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, I <sub>OK</sub>
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 70 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-
posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . . . . . . . 4.5V to 5.5V DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . OV to  $V_{CC}$  Operating Temperature

Range KS74AHCT:  $-40\,^{\circ}$ C to  $+85\,^{\circ}$ C KS54AHCT:  $-55\,^{\circ}$ C to  $+125\,^{\circ}$ C Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . . . Max 500 ns

\* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T <sub>a</sub> = 25°C		KS74AHCT $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-6mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> = 0.1	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	٧
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	Icc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA	,	2.7	2.9	3.0	mA

## AC ELECTRICAL CHARACTERISTICS (Input tr, tres 2 ns), AHCT251

Characteristic	Symbol	Conditions <sup>†</sup>		T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	Ta = -40°0	AHCT C to +85°C 0V±10%	KS54. T <sub>a</sub> = -55°C V <sub>CC</sub> = 5.0	Unit	
				Тур	Min	Max	Min	Max	
Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF		13 16		21 26		25 31	
A, B or C to Y	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150p		13 16		21 26		25 31	ns
Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pf C <sub>L</sub> =150p		15 18		24 29		27 33	ne
A, B or C to W	t <sub>PHL</sub>	C <sub>L</sub> =50pl C <sub>L</sub> =150pl		15 18		24 29		27 33	ns
Propagation Delay, Any D to Y	t <sub>PLH</sub>	C <sub>L</sub> =50pF\ C <sub>L</sub> =150pF		9 12		15 20		18 24	ns
	t <sub>PHL</sub>	C <sub>L</sub> =50pl		9 12		15 20		18 24	113
Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF C <sub>L</sub> =50pF C <sub>L</sub> =150pF		- 8 11		15 20		18 24	ns
Any D to W	t <sub>PHL</sub>			8 11		15 20		18 24	
Output Enable Time,	t <sub>PZH</sub>	$R_1 = 1 k\Omega$	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	11 14		18 23		22 28	ns
G to Y or W	t <sub>PZL</sub>	111_1143	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	11 14		18 23		22 <b>28</b>	
Output Disable Time,	t <sub>PHZ</sub>	R <sub>L</sub> =1kΩ		13		18		22	ns
G to Y or W	tpLZ	C <sub>L</sub> =50pl	F	13		18		22 ·	
Input Capacitance	CIN			5					pF
Output Capacitance	Соит	Output D	isabled	10					pF
Power Dissipation Capacitance*	C <sub>PD</sub>								pF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

# Dual 1-of-4 Data Selectors/Multiplexers with 3-State Outputs

#### **FEATURES**

- Three-State Version of '153
- Permits Multiplexing from N Lines to 1 Line
- Performs Parallel-to-Serial Conversion
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current
  - $(I_{OL} = 24 \text{ mA} @ V_{OL} = 0.5 \text{V})$  for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
   KS74AHCT: -40°C to +85°C
- KS54AHCT: -55°C to +125°C
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### DESCRIPTION

Each of these data selectors/multiplexers contains inverters and drivers to supply full binary decoding data selection to the AND-OR gates. Separate output control inputs are provided for each of the two four-line sections.

The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the low-impedance of the single enabled output will drive the bus line to a high or low logic level. Each output has its own strobe  $(\overline{G})$ . The output is disabled when its strobe is high.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### PIN CONFIGURATION

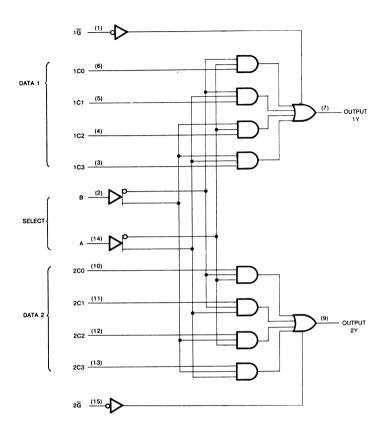
1Ğ[	1	16	Vcc
в	2	15	2Ğ
1C3 🗀	з.	14	] A
1C2	4	13	2C3
101	5	12	]2C2
1C0	6	11	2C1
17 🗆	7	10	2C0
GND	8	9	2Y

#### **FUNCTION TABLE**

SEL	SELECT		DATA INPUTS		OUTPUT CONTROL	ОИТРИТ	
В	A	CO	C1	C2	СЗ	, <b>G</b>	Y
X	Х	X	Х	Х	X	Н	Z
L	L	L	Х	Х	Χ	L	L
L	L	Н	Х	Х	Χ	L	Н
L	Н	X	L	Х	Х	L	L
L	Н	Х	Н	Х	Х	L	Н
Н	L	Х	Х	L	Х	L	L
Н	L	Х	Х	Н	Χ	L	Н
Н	Н	Х	Х	Х	L	L	L
Н	Н	X	Χ	Χ	Н	L	Н

Address inputs A and B are common to both sections.

#### LOGIC DIAGRAM



# Absolute Maximum Ratings\*

Supply Voltage Range V <sub>CC</sub> ,0.5V	to +7V
DC Input Diode Current, I <sub>IK</sub>	
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V)$	±20 mA

DC Output Diode Current,  $I_{OK}$  (V<sub>O</sub> < -0.5V or V<sub>O</sub> > V<sub>CC</sub> +0.5V) . . . .  $\pm$ 20 mA

Continuous Output Current Per Pin,  $I_0$ (-0.5V <  $V_0$  <  $V_{CC}$  +0.5V) . . . . . . .  $\pm$ 70 mA

Storage Temperature Range, T $_{stg}$ ...-65°C to +150°C Power Dissipation Per Package, P $_{d}$ † ...... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

Input Rise & Fall Times,  $t_r, \; t_f \; \ldots \; \ldots \; \ldots \;$  Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

# DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	= 25°C	KS74AHCT Ta = -40°C to +85°C	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit	
			Тур	Α	Guaranteed Limits			
Minimum High-Level Input Voltage	V <sub>IH</sub>	,		2.0	2.0	2.0	<b>~</b>	
Maximum Low-Level Input Voltage	ViL			0.8	0.8	0.8	٧	
Minimum High-Level Output Voltage	V <sub>ОН</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-6m A$	V <sub>CC</sub> 4.2	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> -0.1 3.84	V <sub>CC</sub> -0.1 3.7	v	
Maximum Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> =20μΑ I <sub>O</sub> =12mA I <sub>O</sub> =24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v	
Maximum Input Current	l <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ	
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μА	
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ	
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA	

# AC ELECTRICAL CHARACTERISTICS (Input tr, tre2 ns), AHCT253

Characteristic	Symbol	1		T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	Ta = -40°C	AHCT C to +85°C OV ± 10%	Ta = -55°C	AHCT to +125°C 0V ± 10%	Unit
				Тур	Min	Max	Min	Max	
Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150p		13 16		21 26		25 31	ns
A or B to any Y	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150p		13 16		21 26		25 31	113
Propagation Delay, Data (any C) to any Y	t <sub>PLH</sub>		C <sub>L</sub> =50pF C <sub>L</sub> =150pF			15 20		18 34	ns
	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF		9 12		15 20		18 34	
Output Enable Time	t <sub>PZH</sub>	R <sub>L</sub> =1kΩ	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	10 13		16 · 21		19 35	ns
G to Y	t <sub>PZL</sub>	UL— 1K7	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	10 13		16 21		19 35	115
Output Disable Time,	tpHZ	$R_L = 1 k\Omega$		13		18		22	ns
G to Y	tpLZ	C <sub>L</sub> =50pf	=	13		18		22	113
Input Capacitance	CIN			5		,			pF
Output Capacitance	Cour	Output D	isabled	10					pF
Power Dissipation Capacitance*	C <sub>PD</sub>								pF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} \ V_{CC}^2 \ f \ + \ I_{CC} \ V_{CC}$ .

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.



#### KS54AHCT **257/258** Quad 2-Line to 1-Line Data Selector/ KS74AHCT **257/258** Quad 2-Line to 1-Line Data Selector/ Multiplexers with 3-State Outputs

#### **FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current (I<sub>OL</sub> = 24 mA @ V<sub>OL</sub> = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges: KS74AHCT: -40°C to +85°C
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### **DESCRIPTION**

The '257 and '258 multiplex signals from for-bit data sources to four-output data lines in bus organized systems. The data presented at the outputs is non-inverted for the '257, and inverted for the '258.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V<sub>CC</sub> and ground.

#### PIN CONFIGURATION

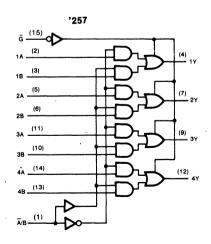
KS54AHCT: -55°C to +125°C

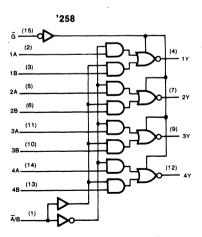
Ã/B 🗖 1	$\cup$	16 Vcc
1A 🗖 2		15 🗖 Ğ
1B 🔲 3		14 🗖 4A
1Y 🗖 4		13 🔲 4B
2A 🗖 5		12 4Y
2B 🗖 6		11 3A
2Y 🗖 7		10 🔲 ЗВ
GND 🔲 8		9 🗖 3Y
L		

#### **FUNCTION TABLE**

	Inputs	Outp	out Y			
Output Control	Select	Select Data		'257	'258	
Ğ.	Ã/B	Α	В			
Н	Х	X.	Х	Z	Z	
L	L	L	X	L	н	
L	L	Н	X	Н	L	
L	Н	X	L	L	Н	
L	Н	X	Н	н	L	

# LOGIC DIAGRAMS





Supply Voltage Range $V_{CC},\ \dots \ -0.5V$ to $+7V$
DC Input Diode Current, I <sub>IK</sub>
$(V_{I} < -0.5V \text{ or } V_{I} > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + 1.5V$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, $P_d{}^{\dagger}$ 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.

These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Supply Voltage, V <sub>CC</sub> 4.5	V to s	5.5V
DC Input & Output Voltages*, VIN, VOUT	OV to	Vcc
Operating Temperature		

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

# DC ELECTRICAL CHARACTERISTICS (Vcc=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	Ta	= 25°C	KS74AHCT $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
,			Тур	Guaranteed Limits			
Minimum High-Level Input Voltage	, V <sub>IH</sub>			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-6mA$	V <sub>CC</sub> 4.2	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin  V <sub>I</sub> =2.4V  other Inputs: at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0µA		2.7	2.9	3.0	mA



#### KS54AHCT **257/258** Quad 2-Line to 1-Line Data Selector/ KS74AHCT **257/258** Quad 2-Line to 1-Line Data Selector/ Multiplexers with 3-State Outputs

# AC ELECTRICAL CHARACTERISTICS (Input tr, tr <2 ns), AHCT257

Characteristic	Symból	Con	ditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	-	AHCT C to +85°C OV±10%	T, = -55°C	AHCT to +125°C )V ± 10%	Unit
				Тур	Min	Max	Min	Max	
Propagation Delay, A or B to any Y	t <sub>PLH</sub>	C <sub>L</sub> =50pl C <sub>L</sub> =150pl		7 10		12 17		14 20	ns
	t <sub>PHL</sub>	C <sub>L</sub> =50pl C <sub>L</sub> =150pl		7 10		12 17		14 20	113
Propagation Delay, Ā/B to any Y	tpLH	C <sub>L</sub> =50pF C <sub>L=150pF</sub>		12 15		20 25		24 30	
	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150p		12 15		20 25		24 30	ns
Output Enable Time,	t <sub>PZH</sub>	$R_1 = 1 k\Omega$	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	13 16		18 23		22 28	ns
G to any Y	tpzL	11[-1142	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	13 16	ı.	18 23		22 28	113
Output Disable Time,	tPHZ	$R_L = 1k\Omega$		13		18		22	ns
G to any Y	t <sub>PLZ</sub>	C <sub>L</sub> =50pF	=	13		18		22	ijs
Input Capacitance	CIN			5					pF
Output Capacitance	Cout	Output D	isabled	10		,			рF
Power Dissipation Capacitance*	C <sub>PD</sub>		4						рF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

# AC ELECTRICAL CHARACTERISTICS (Input tr, tr <2 ns), AHCT258

Characteristic	Symbol	Conditions <sup>†</sup>		T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	Ta = -40°	AHCT C to +85°C 0V±10%	Ta = -55°C	AHCT to +125°C V± 10%	Unit
				Тур	Min	Max	Min	Max	
Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pf C <sub>L</sub> =150p		7 10		12 17		14 20	ns
A or B to any Y	tphL	C <sub>L</sub> =50pF C <sub>L</sub> =150p		9 12		14 19		16 22	110
Propagation Delay, Ā/B to any Y	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF		14 17		23 28		28 34	
	tpHL	C <sub>L</sub> =50pF C <sub>L</sub> =150p	-	14 17		23 28		28 34	ns
Output Enable Time,	<b>t</b> PZH	$R_i = 1 k\Omega$	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	11 14		18 23		22 28	ns
G to any Y	tpzL	112 1142	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	11 14		18 23		22 28	
Output Disable Time,	t <sub>PHZ</sub>	R <sub>L</sub> =1kΩ		13		18		22	ns
G to any Y	tPLZ	C <sub>L</sub> =50pF	:	13		18		22	
Input Capacitance	CIN			5					рF
Output Capacitance	Соит	Output Di	sabled	10					pF
Power Dissipation Capacitance*	C <sub>PD</sub>								pF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC^2} f + I_{CC} V_{CC}$ .

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.



<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

- 8-Bit parallel-out storage register performs serial-toparallel conversion with storage
- · Asynchronous parallel clear
- · Active high decoder
- Enable/Disable input simplifies expansion
- Expandable for N-bit applications
- · Four distinct functional modes
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:

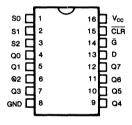
 $I_{OL} = 8 \text{ mA } @ V_{OL} = 0.5 \text{V}$ 

- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATION



# **FUNCTION TABLE**

Inpu	nputs Output of Addressed		Each Other	Function
CLR	G	Latch	Output	Function
Н	L	D	Qio	Addressable Latch
Н	Н	Qio	QiO	Memory
L	L	. D	L	8-Line Demultiplexer
L	Н	L	L	Clear

D = the level at the data input.  $Q_{i0}$  = the level of  $Q_{i0}$  (i = Q, 1, ... 7, as appropriate) before the indicated steady-state input conditions were established.

#### DESCRIPTION

The '259 is a high-speed addressable latch designed for general purpose storage applications in digital systems. It can be used for implementing working registers, serial-holding registers and active-high decoders or demultiplexers.

The '259 has four distinct modes of operation that are selected via the clear ( $\overline{\text{CLR}}$ ) and enable ( $\overline{\text{G}}$ ) inputs: 1) addressable latch; 2) memory; 3) active-high eight-channel demultiplexer; and 4) clear.

In the addressable latch mode, data on the data input (D) is written into the addressed latch. In this mode, data will be written into the addressed latch with all non-addressed latches remaining in their previous states.

In the memory mode, all latches remain in their previous state and are unaffected by the data of address inputs.

In the demultiplexing mode, addressed outputs will follow the state of the D input and all other outputs will remain low.

In the clear mode, all outputs are low and unaffected by the address and data inputs.

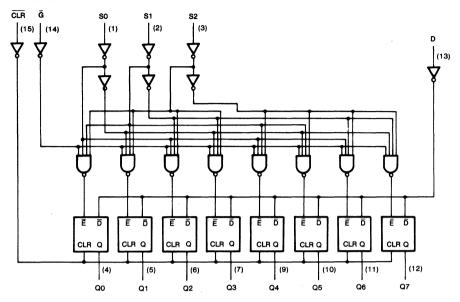
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### LATCH SELECTION TABLE

Sel	ect Inp	outs	Latch
S2	S1	SO	Addressed
L	L	L	. 0
L	L	Н	1 '
L	Н	L	2
L	` H	Н	3
Н	L	L	4
Н	L	Н	5
н	Н	L	6
Ĥ	Н	Н	7

#### LOGIC DIAGRAM



# **Absolute Maximum Ratings\***

Supply Voltage Range $V_{CC}$ , $-0.5V$ to $+7V$
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Datings are those values beyond

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Supply Voltage, V<sub>CC</sub> . . . . . . . . . . . 4.5V to 5.5V DC Input & Output Voltages\*, V<sub>IN</sub>, V<sub>OUT</sub> . . OV to V<sub>CC</sub> Operating Temperature

Range

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . Max 500 ns

 Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

# DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol Test Conditions		T <sub>a</sub> = 25°C		KS74AHCT T <sub>a</sub> = -40°C to +85°C	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
		,	Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	v
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> -0.1	V <sub>CC</sub> -0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	l <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μА
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

# AC ELECTRICAL CHARACTERISTICS (Input tr, tre2 ns), AHCT259

Characteristic		Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	KS74AHCT T <sub>a</sub> = -40°C to +85°C' V <sub>CC</sub> = 5.0V ± 10%		KS54AHCT $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Тур	Min	Max	Min	Max	
Propagation Delay CLR to any Q		t <sub>PHL</sub>		9		15		18	ns
Propagation Delay,		t <sub>PLH</sub>		-12		19		23	ns
Data to any Q		t <sub>PHL</sub>	C <sub>L</sub> =50pF	12	1	19		23	ns
Propagation Delay, Address to any Q		t <sub>PLH</sub>		13		22		27	
		tPHL		13		22		27	
Propagation Delay,		t <sub>PLH</sub>		12		20		24	ns
G to any Q		t <sub>PHL</sub>		12		20		24	
Pulse Width	CLR Low			6	10		10		ns
i dise widii	G Low	t <sub>w</sub>		9	15		20		
Setup Time Data or Address before Gt		t <sub>su</sub>		10	15		20		ns
Hold Time, Data or Address before Gt		th		-3	0		0		ns
Input Capacitance		C <sub>IN</sub>	,	5					pF
Power Dissipation Ca	apacitance*	C <sub>PD</sub>	`	,80					рF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
  - $I_{OL} = 8 \text{ mA } @ \dot{V}_{OL} = 0.5 \text{V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

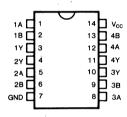
#### **DESCRIPTION**

These devices contain four independent exclusive-NOR gates with open-drain outputs. Using a suitable pull-up resistor, these outputs may be connected to other open-drain outputs to implement wired-AND functions.

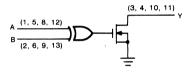
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

# PIN CONFIGURATION



### LOGIC DIAGRAM



#### **FUNCTION TABLE**

inp	uts	Output
Α	В	Y
L	L	Н
L	Н	L
Н	L	L
Н	Н	н

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stq</sub> 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Supply Voltage, V<sub>CC</sub> . . . . . . . . . . . . . . . . . 4.5V to 5.5V DC Input & Output Voltages\*, V<sub>IN</sub>, V<sub>OUT</sub> . . OV to V<sub>CC</sub> Operating Temperature

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . . Max 500 ns

 Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

# DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T <sub>a</sub> = 25°C		KS74AHCT T <sub>a</sub> = -40°C to +85°C	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit	
		,	Тур	p Guaranteed Limits				
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	v	
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v	
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v	
Maximum Input Current	l <sub>IN</sub> .	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ	
Maximum Output Leakage Current	loz	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> · V <sub>OUT</sub> =V <sub>CC</sub>		±0.5	±5.0	±10.0	μΑ	
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.0	20.0	40.0	μΑ	
Additional Worst Case Supply Current	Δlcc	per input pin  V <sub>I</sub> =2.4V  other Inputs: at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0µA		2.7	2.9	3.0	mA	

# AC ELECTRICAL CHARACTERISTICS (Input tr, ties 2 ns), AHCT266

Characteristic	Symbo	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	25°C KS74AHCT T <sub>a</sub> = -40°C to +85° V <sub>CC</sub> = 5.0V ± 10%		KS54AHCT C T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%		Unit
	\ \		Тур	Min	Max	Min	Max	1
Propagation Delay	t <sub>PLH</sub>	C <sub>L</sub> =50pF	19		29		35	ns
- ropuguion Doia,	$t_{PHL}$ $R_L = 1 k\Omega$	11		18		22	1115	
Input Capacitance	CIN		5					pF
Power Dissipation Capacitance*	C <sub>PD</sub>	(per gate)	15			,		pF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.



- Eight positive-edge-triggered D-type flip-flops with single-rail outputs
- Buffered common clock and asynchronous clear
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
   I<sub>OL</sub> = 24mA @ V<sub>OL</sub> = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### **DESCRIPTION**

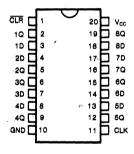
These devices are high-speed octal registers. They consist of eight positive-edge-triggered D-type flip-flops with individual D inputs and Q outputs. All flip flops are loaded and cleared simultaneously by the common buffered clock (CLK) and clear (CLR) inputs.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

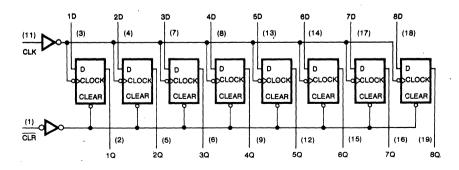
#### PIN CONFIGURATION



# **FUNCTION TABLE**

(Each Flip-Flop) Inputs Output CLR CLK D Q Х Х L н Ť н н Н Ť L L Н Х Qo

#### LOGIC DIAGRAM



Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, IIK
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V)$ ±20 mA
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±70 mA
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.

These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Supply Voltage, V <sub>CC</sub>	4.5V to 5.5V
DC Input & Output Voltages*, VIN, VOUT	OV to Vcc
Operating Temperature	

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . . Max 500 ns

\* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

# DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol Test Conditions		T,	a = 25°C	KS74AHCT $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54AHCT $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$	Unit
			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	VoH	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-6mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> -0.1 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}$ = $V_{IH}$ or $V_{IL}$ $I_{O}$ =20 $\mu$ A $I_{O}$ =12 $\mu$ A $I_{O}$ =24 $\mu$ A	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 * 0.4	٧.
Maximum Input Current	lin	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>1</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

# AC ELECTRICAL CHARACTERISTICS (Input t<sub>r</sub>, t<sub>f</sub>≤2 ns), AHCT273

Characteristic		Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	KS74AHCT $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$ $V_{CC} = 5.0V \pm 10^{\circ}$		KS54AHCT $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$		Unit	
				Тур	Min	Max	Min	Max		
Maximum Clo	ck Frequency	f <sub>max</sub>	C <sub>L</sub> =50pF	50	35		30		MHz	
Propagation Delay, CLK to any Q  Propagation Delay, CLR to any Q		t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	12 13		16 20 .		19 34	ns	
		t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	12 13		16 20		19 34	113	
		t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	11 14		18 23		22 28	ns	
Pulse Width	CLR Low	tw		8	14		17		ns	
ruise Width	CLK High or Low			8	14		17		1113	
Setup Time	Data	tsu		6	10		10		ns	
before CLKt	Clear inactive State	\ \tsu	•	9	15		15		118	
Hold time, Data after CLK†		th		-3	0		0		ns	
Input Capacitance		CIN		5					pF	
Power Dissipation Capacitance*		C <sub>PD</sub>	(per package)	150					pF	

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

- Generates Odd or Even Parity for Nine Data Lines
- · Cascadable for N-Bits Parity
- Can be used to Upgrade Existing Systems using MSI Parity Circuits
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
- (I<sub>OL</sub> = 24 mA @ V<sub>OL</sub> = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
   KS74HCTLS: -40°C to +85°C
- KS54HCTLS: -55°C to +125°C
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### DESCRIPTION

These universal, nine-bit parity generators/checkers feature odd and even outputs to facilitate operation of either odd or even parity application. The word-length capability is easily expanded by cascading.

The devices can be used to upgrade the performance of most systems utilizing the '180 parity generator/checker, Although the '280 is implemented without expander inputs, the corresponding function is provided by the availability of an input at pin 4 and the absence of any internal connection at pin 3. This permits the '280 to be substituted for the '180 in existing designs to produce an identical function even if the devices are mixed with existing '180's.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

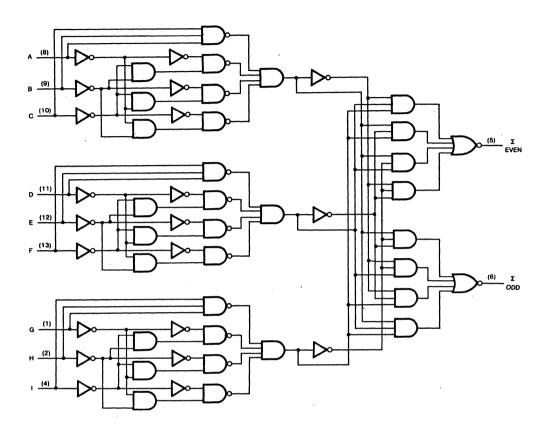
#### PIN CONFIGURATION

G	14 13 12 11 10 9	V F E D C B
_		

#### **FUNCTION TABLE**

NUMBER OF INPUTS A	OUTF	PUTS
THRU I THAT ARE HIGH	Σ EVEN	Σ ODD
0,2,4,6,8	H	L
1,3,5,7,9	L	Н

#### **LOGIC DIAGRAM**



# **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V	V
DC Input Diode Current, IIK	
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ m/s}$	Ą
DC Output Diode Current, IOK	
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ m/s}$	٩
Continuous Output Current Per Pin, Io	
$(-0.5V < V_O < V_{CC} + 0.5V) + 0.5V$	Ą
Continuous Current Through	
V <sub>CC</sub> or GND pins ±250 m/	4
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C	2
Power Dissipation Per Package, Pd† 500 mV	۷

<sup>\*</sup> Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . . . . . . . 4.5V to 5.5V DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . 0V to  $V_{CC}$  Operating Temperature

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)



# DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T <sub>a</sub> = 25°C		KS74AHCT Ta = -40°C to +85°C	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL	/		0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	VoH	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-6mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> -0.1 3.84	V <sub>CC</sub> -0.1	v
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	IIN	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μА
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μА
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>1</sub> =2.4V' other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0µA		2.7	2.9	3.0	mA

# AC ELECTRICAL CHARACTERISTICS (Input tr. tr 42 ns), AHCT280

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	I <sub>2</sub> = -40°C to +85°C		KS54 T <sub>a</sub> = -55°C V <sub>CC</sub> = 5.0	Unit		
			Тур	Min	Max	Min	Max		
Propagation Delay	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	12 15		20 25		24 30		
Any input to Σ Even	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	12 15		20 25		24 30	ns	
Propagation Delay.	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	13 16		22 27		26 32	200	
Any input to Σ Odd	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	13 16		22 27		26 32	ns	
Input Capacitance	CIN		5					рF	
Power Dissipation Capacitance*	C <sub>PD</sub>							рF	

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

- . Multiplexed I/O ports provides improved bit density
- Four modes of operation: hold (store), shift right, shift left, and load data
- . Operates with outputs enabled or at high impedance
- . Can be cascaded for N-bit word lengths
- . Direct overriding clear
- Application:
  - Stacked or push-down registers, buffer storage, and accumulator registers
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- · 3-State outputs with drive current
- ( $I_{OL} = 24 \text{ mA } @ V_{OL} = 0.5 \text{V}$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### DESCRIPTION

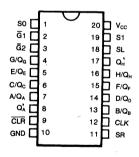
These eight-bit universal registers feature multiplexed I/O ports to achieve full eight-bit data handling. Two function-select inputs and two output-control inputs can be used to choose the modes of operation listed in the function table.

Synchronous parallel loading is accomplished by taking both function-select lines SO and S1 high. This places the three-state outputs in a high-impedance state and permits data that is applied on the I/O ports to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. Clearing occurs asynchronously when  $\overline{\text{CLR}}$  is low. Pulling either of the output controls,  $\overline{\text{G1}}$  or  $\overline{\text{G2}}$ , high disables the outputs but this has no effect on clearing, shifting, or storage of data

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

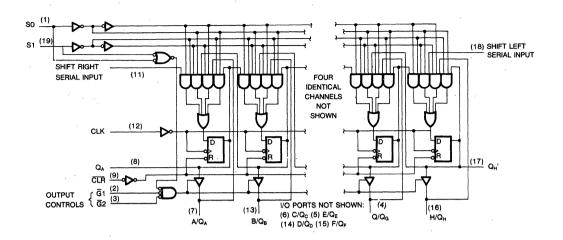
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### PIN CONFIGURATION



# 8-Bit Universal Shift/Storage Registers with 3-State Outputs

### **LOGIC DIAGRAM**



#### **FUNCTION TABLE**

				Inp	uts							1/0 F	orts				Out	puts
Mode	CLR	S1	SO	1 '	tput ntroi <b>G</b> 2	CLK	SL	SR	A/Q <sub>A</sub>	B/Q <sub>B</sub>	C/Qc	D/Q <sub>D</sub>	E/Q <sub>E</sub>	F/Q <sub>F</sub>	G/Q <sub>G</sub>	H/Q <sub>H</sub>	Q <sub>A</sub> '	Q <sub>H</sub> '
Clear	L L	X L H	L X H	L L X	L L X	X X X	×××	X X X	L L X	L L X	L X	L L X	L X	L L X	L X	L L X	LLL	L L
Hold	H. H	L	L	L	L L	X L	X	X	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>C0</sub>	Q <sub>D0</sub>	Q <sub>E0</sub>	Q <sub>F0</sub>	Q <sub>G0</sub>	Q <sub>H0</sub>	Q <sub>A0</sub>	Q <sub>H0</sub>
Shift Right	H	L	Н	L	L	† . †	X	H	H	Q <sub>An</sub> Q <sub>An</sub>	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Dn</sub> Q <sub>Dn</sub>	Q <sub>En</sub>	Q <sub>Fn</sub> Q <sub>Fn</sub>	Q <sub>Gn</sub> Q <sub>Gn</sub>	H	Q <sub>Gn</sub> Q <sub>Gn</sub>
Shift Left	H	H	L	L	L	<b>†</b>	HL	X	Q <sub>Bn</sub> Q <sub>Bn</sub>	Q <sub>Cn</sub> Q <sub>Cn</sub>	Q <sub>Dn</sub> Q <sub>Dn</sub>	Q <sub>En</sub> Q <sub>En</sub>	Q <sub>Fn</sub> Q <sub>Fn</sub>	Q <sub>Gn</sub> Q <sub>Gn</sub>	Q <sub>Hn</sub> Q <sub>Hn</sub>	H	Q <sub>Bn</sub> Q <sub>Bn</sub>	H
Load	н	Н	Н	Х	X	1	Х	Х	а	b	С	d	е	f	g	h	а	h

When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

•
Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 70 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pat 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . Max 500 ns

 Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

# DC ELECTRICAL CHARACTERISTICS (Vcc=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	Ta	=25°C	KS74AHCT $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$	$KS54AHCT$ $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$	Unit
			Тур		Guaranteed Limi	ts	
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	0.8	V
Minimum High-		V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> =-20μA Q' <sub>A</sub> and Q' <sub>H</sub> outputs:		V <sub>CC</sub> -0.1	V <sub>CC</sub> -0.1	V <sub>CC</sub> -0.1	
Level Output Voltage	Voн	I <sub>O</sub> = -4mA Q <sub>A</sub> thru Q <sub>H</sub> outputs: I <sub>O</sub> = -6mA	4.2	3.98	3.84	3.7	V
Miximum		V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> =20μA Q' <sub>A</sub> and Q' <sub>H</sub> outputs:	0	0.1	0.1	0.1	
Low-Level Output Voltage	VoL	I <sub>O</sub> =4mA I <sub>O</sub> =8mA Q <sub>A</sub> thru Q <sub>H</sub> outputs:		0.26 0.39	0.33 0.5	0.4	V
		I <sub>O</sub> =12mA I <sub>O</sub> =24mA		0.26 0.39	0.33 0.5	0.4	
Maximum Input Current	lin	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable = V <sub>IN</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	.μA
Maximum Quiescent Supply Current	loc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	ΔΙας	per input pin  V <sub>I</sub> =2.4V  other Inputs: at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0µA		2.7	2.9	3.0	mA

# AC ELECTRICAL CHARACTERISTICS (Input tr., tr <2 ns), AHCT299

Cha	racteristic	Symbol	Conditions <sup>†</sup>	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	$T_a = -40^\circ$	IAHCT C to +85°C 0V±10%	$T_a = -55^{\circ}C$	AHCT to +125°C DV ± 10%	Unit
				Тур	Min	Max	Min	Max	
Maximum Clo	ock Frequency	f <sub>max</sub>		50	30		25		MHz
Propagation	Delav.	tpLH		10		17		20	ns
CLK to Q'A		t <sub>PHL</sub>	C <sub>L</sub> =50pF	10		17		20	
Propagation CLR to Q'A (		t <sub>PHL</sub>		13	-	22		26	ns
Propagation	Delav	t <sub>PLH</sub>	$C_L=50pF$ $C_L=150pF$	10 13		16 21		19 25	ns
	Propagation Delay, CLK to Q <sub>A</sub> thru Q <sub>H</sub>		C <sub>L</sub> =50pF C <sub>L</sub> =150pF	10 13		16 21		19 25	115
Propagation CLR to Q <sub>A</sub> th	• '	t <sub>PHL</sub>	$C_L=50pF$ $C_L=150pF$	13 16		22 27		26 31	ns
Output Enab	le Time.	t <sub>PZH</sub>	$C_L = 50p$ $C_L = 150$			19 24	,	23 29	ns
G  1, G  2, to 0			C <sub>L</sub> =50p C <sub>L</sub> =150	1		19 24		23 29	
Output Disab	le Time,	t <sub>PHZ</sub>	$R_L = 1 k\Omega$	11		18		22	ns
G  1, G  2 to C	A thru QH	tPLZ	C <sub>L</sub> =50pF	11		18		22	
Pulse Width	CLK High or Low	tw		9	15		20		ns
	CLR Low			5	8		10		
	S0 and S1			12	20		10		
Setup time	High-Level Inputs	t <sub>su</sub>		. 8	13		15		ns
before CLK1	Low-Level Inputs			8	13		15		
	CLR Inactive			8	13		15		
Hold Time				0	0		0	1	ns
after CLK†				0		1			
Input Capaci	tance	CIN		5					pF
Output Capa	citance	Соит	Output Disable	10				1	pF
Power Dissip	ation Capacitance*	CPD							pF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

- Inverting Version of '153
- Permits Multiplexing from N Lines to 1 Line
- Performs Parallel-to-Serial Conversion
- Strobe (Enable) Line Provided for Cascading (N Lines to n Lines)
- · Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- · High drive current outputs
  - $(I_{OL} = 24 \text{ mA} @ V_{OL} = 0.5 \text{V})$  for direct bus interface
- . Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C

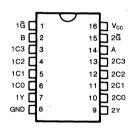
KS54AHCT: -55°C to +125°C

· Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs Each of these data selectors/multiplexers contains inverters and drivers to supply fully complementary binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs (G) are provided for each of the two four-line sections.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels. allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V<sub>CC</sub> and ground.

#### PIN CONFIGURATION



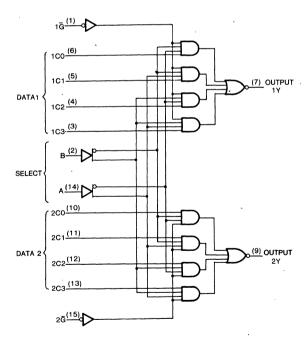
#### **FUNCTION TABLE**

	ECT UTS	DA	TA	INPL	ITS	STROBE	ОИТРИТ
В	A	CO	C1	C2	СЗ	Ğ	Y
Х	Х	Х	Х	Х	Х	Н	Η.
L	L	L	Х	Х	Х	L	Н
L	L	Н	Χ	Х	- X	L	L
L	Н	. X	L	X	Х	L	Н
L	Н	Х	Н	Χ	Х	L	L
Н	L	Х	Χ	L	Χ	L	н
Н	L	Х	Χ	Н	Х	L	L
Н	Н	Х	Х	Х	L	L	н
Н	Н	Х	Х	Χ	Н	L	L

Select inputs A and B are common to both sections.

### LOGIC DIAGRAM

DESCRIPTION



# Dual 4-Line to 1-Line Data Selectors/Multiplexers

# **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V)$ ±20 mA
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 70 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-
posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

neconfillended Operating Conditions
Supply Voltage, V <sub>CC</sub> 4.5V to 5.5V
DC Input & Output Voltages*, VIN, VOUT 0V to VCC
Operating Temperature
Range KS74AHCT: -40°C to +85°C
KS54AHCT: -55°C to +125°C
Input Rise & Fall Times, $t_r,  t_f  \ldots  \ldots  Max  500  ns$

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

# DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	a = 25°C	KS74AHCT $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
1			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-6mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=12mA$ $I_{O}=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	IIN	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0 ,	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin  V <sub>I</sub> =2.4V  other Inputs: at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0µA		2.7	2.9	3.0	mA

# AC ELECTRICAL CHARACTERISTICS (Input tr, tr≤2 ns), AHCT352

Characteristic	Symbol	Conditions†	bol Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	T. = -40°	IAHCT C to +85°C 0V±10%	T <sub>a</sub> = -55°C	AHCT to +125°C V± 10%	Unit
			Тур	Min	Max	Min	Max		
Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	14 17		23 28		28 34	ns	
A or B to Y	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	14 17		23 28		28 34	115	
Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	11 14		18 23		21 27	ns	
Data (Any C) to Y	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	11 · 14		18 23		21 27	113	
Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	12 15		20 25		24 30	ns	
G to Y	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	12 15		20 25		24 30	113	
Input Capacitance	CIN		5					pF	
Power Dissipation Capacitance*	C <sub>PD</sub>							рF	

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

- Inverting Version of '253
- Permits Multiplexing from N lines to 1 line
- Performs Parallel-to-Serial Conversion
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- · 3-State outputs with high drive current ( $I_{OL} = 24 \text{ mA} @ V_{OL} = 0.5 \text{V}$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS
- and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- · Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

• Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

# DESCRIPTION

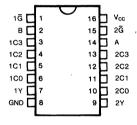
Each of these data selectors/multiplexers contains inverters and drivers to supply full binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs (G) are provided for each of the two four-line sections.

The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the lowimpedance of the single enabled output will drive the bus line to a high or low logic level. Each output has its own strobe  $(\overline{G})$ . The output is disabled when its strobe is high.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V<sub>CC</sub> and around.

### PIN CONFIGURATION

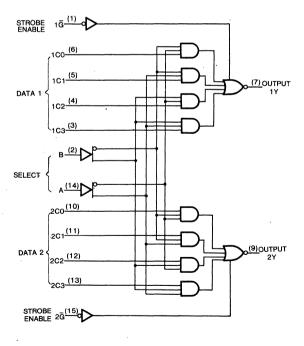


# **FUNCTION TABLE**

SELECT INPUTS		DA	TA	INPL	ITS	OUTPUT	ОИТРИТ	
В	A	CO	C1	C2	C3	Ğ	Y	
Х	X	Х	Х	Х	Х	Н	Z	
L	L	L	Х	Х	Х	L	Н	
L	L	Н	Χ	Х	Χ	L	L	
L	Н	Х	L	Х	Χ	L	н	
L	Н	Х	Н	Х	Χ	L	L	
Н	L	Х	Х	L	Х	L	Н	
Н	L	X	Х	Н	Χ	L	L	
Н	Н	Х	Х	Х	L	L	Н	
Н	Н	Х	Х	Χ	Н	L	L	

Select inputs A and B are common to both sections.

### LOGIC DIAGRAM



Supply Voltage Range $V_{CC}$ , $-0.5V$ to $+7V$
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 70 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissination Per Package Pd <sup>†</sup> 500 mW

<sup>\*</sup> Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

# **Recommended Operating Conditions**

Supply Voltage, V <sub>CC</sub>	4.5V to 5.5V
DC Input & Output Voltages*, VIN, VOUT	OV to V <sub>CC</sub>
Operating Temperature	

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . . Max 500 ns

# DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T <sub>a</sub> = 25°C		KS74AHCT T <sub>a</sub> = -40°C to +85°C	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit		
			Тур		Guaranteed Limits				
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	٧		
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧		
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-6mA$	V <sub>CC</sub> 4.2	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> -0.1 3.84	V <sub>CC</sub> −0.1 3.7	٧		
Maximum Low-Level Output Voltage	Vor	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V		
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ		
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μΑ		
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ		
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA		

<sup>†</sup> Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

<sup>\*</sup> Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

# Dual 1-of-4 Data Selectors/Multiplexers with 3-State Outputs

# AC ELECTRICAL CHARACTERISTICS (Input tr, tre2 ns), AHCT353

Characteristic	Symbol	Conditions†		1		T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	Ta = -40°	AHCT C to +85°C 0V±10%	Ta = -55°C	IAHCT C to +125°C IV ± 10%	Unit
				Тур	Min	Max	Min	Max			
Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pf C <sub>L</sub> =150p		14 17		24 29		28 34	ns		
A or B to any Y	t <sub>PHL</sub>		C <sub>L</sub> =50pF C <sub>L</sub> =150pF			24 29		28 34	113		
Propagation Delay, Data (Any C) to Any Y	t <sub>PLH</sub>	C <sub>L</sub> =50pl C <sub>L=150l</sub>		10 13		18 23		21 27			
	tpHL	C <sub>L</sub> =50pF C <sub>L</sub> =150pF		10 13		18 23		21 27	ns		
Output Enable Time,	tpzH	R <sub>L</sub> =1kΩ	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	10 13		16 21		19 25	ns		
G to Y	t <sub>PZL</sub>		C <sub>L</sub> =50pF C <sub>L</sub> =150pF	10 13		16 21		19 25			
Output Disable Time,	t <sub>PHZ</sub>	$R_L=1k\Omega$		10		18		22	ns		
G to Y	tpLZ	C <sub>L</sub> =50pl	=	10		18		22			
Input Capacitance	CIN			5					pF		
Output Capacitance	Cout	Output D	isabled	10					pF		
Power Dissipation Capacitance*	C <sub>PD</sub>								pF		

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current
   (I<sub>OL</sub> = 24 mA @ V<sub>OL</sub> = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### DESCRIPTION

These high-speed Hex bus drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus oriented receivers and transmitters.

The '365 and '366 have two output enables ( $\overline{G}1$  and  $\overline{G}2$ ) NOR'ed together to control all six gates. The '367 and '368 have two output enables which are configured so that one enable ( $\overline{G}1$ ) controls four gates and the other ( $\overline{G}2$ ) controls the remaining two gates. The '366 and '368 have inverting data paths. The '365 and '367 have noninverting data paths.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### PIN CONFIGURATION

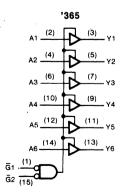
#### Ğ1 [ ☐ V<sub>cc</sub> A1 [ ☐ Ğ2 Y1 [ ☐ A6 A2 [ ☐ Y6 Y2 7 A5 ☐ Y5 АЗ 6 үз Г □ A4 GND [

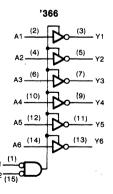
#### **FUNCTION TABLES**

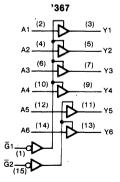
	365 810 356									
lr	puts	;	Y Outputs							
Ğ1	Ğ2	A	'365	'366						
L	L	L	L.	Н						
L	L	Н	Н	L						
Н	Х	Х	Z	Z						
Х	Н	Х	Z	Z T						

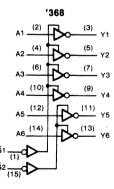
307 and 308								
Inputs	Y Outputs							
G1 & G2	A	'367	'368					
L	L	L	Н					
L	Н	н	L					
Н	Х	Z	Z					

#### **LOGIC DIAGRAMS**









Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 70 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Ratings are those values beyond

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . . . . . . . 4.5V to 5.5V DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . OV to  $V_{CC}$  Operating Temperature

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . Max 500 ns
\* Unused inputs must always be tied to an appropriate logic

voltage level (either V<sub>CC</sub> or GND)

#### DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T <sub>a</sub> = 25°C		KS74AHCT T <sub>a</sub> = -40°C to +85°C	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit		
·			Тур		Guaranteed Lim	its			
Minimum High-Level Input Voltage	VIH			2.0	2.0	2.0	٧		
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧		
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-6mA$	V <sub>CC</sub> 4.2	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	v		
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=12mA$ $I_{O}=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v		
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ		
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μΑ		
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ		
Additional Worst Case Supply Current	Δlcc	per input pin  V <sub>I</sub> =2.4V  other Inputs: at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0µA		2.7	2.9	3.0	mA		

# AC ELECTRICAL CHARACTERISTICS (Input t, t < 2 ns), AHCT367, AHCT368

Characteristic	Symbol	Conditions†				T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	KS74AHCT T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%		KS54 T <sub>a</sub> = -55°C V <sub>CC</sub> = 5.0	Unit
				Тур	Min	Max	Min	Max		
Propagation Delay,	t <sub>PLH</sub>		C <sub>L</sub> = 50pF C <sub>L</sub> =150pF			14 19		17 33	ns	
A to Y,	t <sub>PHL</sub>	C <sub>L</sub> = 50pF C <sub>L</sub> =150pF		8 11		14 19		17 33		
Output Enable Time, G to Y	tpzH		C <sub>L</sub> = 50pF C <sub>L</sub> =150pF			23 28		28 34	- ns	
	tpzL		C <sub>L</sub> = 50pF C <sub>L</sub> =150pF	14 17		23 28		28 34		
Output Disable Time,	t <sub>PHZ</sub>	R <sub>L</sub> =1kΩ		15		20		22	ns	
G to Y	tpLZ	C <sub>L</sub> =50pF		15		20		22	113	
Input Capacitance	CIN			5					pF	
Output Capacitance	Соит	Output D	Output Disabled						рF	
Power Dissipation Capacitance* (per driver)	C <sub>PD</sub>	$\overline{G} = V_{CC}$ $\overline{G} = GND$		5					pF	

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

# Octal D-Type Transparent Latches with 3-State Outputs

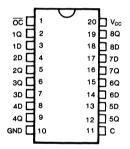
#### **FEATURES**

- 8 latches in a single package
- · Full parallel access for loading
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ( $I_{OL}=24$  mA @  $V_{OL}=0.5V$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATION



#### DESCRIPTION

The '373 consists of 8 high-speed D-type latches coupled to 3-state output buffers with high drive current capability. It can be used in implementing buffer registers, I/O ports, bidirectional bus drivers and working registers.

The latches are transparent: when the enable (C) is high, the Q outputs follow the data (D) inputs. When the enable is low, the outputs latch at the levels that were set up at the D inputs.

The output buffers are controlled by a common signal ( $\overline{OC}$ ) which places the outputs at a high-impedance state when it is taken high. The  $\overline{OC}$  signal does not affect the internal operations of the latches. Old data can be retained or new data can be entered while outputs are off.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

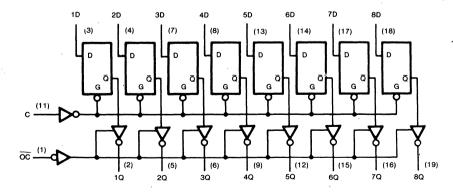
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### **FUNCTION TABLE**

(Each Latch)

	Inputs		Output
ŏc	Enable C	D	Q
L	Н	Н	Н
L	Н	L	L
L	L ·	Х	$Q_0$
Н	Χ	X	Z

#### **LOGIC DIAGRAM**



<sup>\*</sup> Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

\* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

#### DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	Ta = 25°C		KS74AHCT T <sub>a</sub> = -40°C to +85°C	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit	
			Тур		Guaranteed Limits			
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	v	
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v	
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-6mA$	V <sub>CC</sub> 4.2	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	v	
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v	
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ	
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μΑ	
Maximum Quiescent Supply Current	lcc	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μΑ	
Additional Worst Case Supply Current	ΔΙ <sub>CC</sub>	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA	L	2.7	2.9	3.0	mA	

1. W. A.

# Octal D-Type Transparent Latches with 3-State Outputs

# AC ELECTRICAL CHARACTERISTICS (Input tr, tr≤2 ns), AHCT373

Characteristic Symb		1 1		T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	Ta = -40°C	AHCT C to +85°C OV ±10%	KS54AHCT $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Тур	Min	Max	Min	Max	
Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> = 50pl C <sub>L</sub> =150pl		.8 11		14 19		17 23	ns
D to Q	t <sub>PHL</sub>	C <sub>L</sub> = 50pl C <sub>L</sub> =150pl		8 11		14 19		17 23	113
Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> = 50pl C <sub>L</sub> =150pl		14 17		23 28		27 33	ns
C to Q	t <sub>PHL</sub>	C <sub>L</sub> = 50pl C <sub>L</sub> =150pl		14 17		23 28		27 33	
Output Enable Time,	t <sub>PZH</sub>	-R <sub>L</sub> =1kΩ	C <sub>L</sub> = 50pF C <sub>L</sub> =150pF	12 15		20 25	,	24 30	
	t <sub>PZL</sub>		C <sub>L</sub> = 50pF C <sub>L</sub> =150pF	12 15		20 25		24 30	ns
Output Disable Time,	t <sub>PHZ</sub>	$R_L=1k\Omega$		13		18		22	ns
OC to any Q	t <sub>PLZ</sub>	C <sub>L</sub> =50pF		13	1	18		22	113
Pulse Width, C High	tw			9	15		18		ns
Setup Time, D before C↓	tsu			6	10		10		ns
Hold Time, D after C↓	t <sub>h</sub>			3	<b>.</b> 5		7		ns
Input Capacitance	CIN			5					рF
Output Capacitance	Cout	Output Disabled		10					pF
Power Dissipation Capacitance* (per latch)	C <sub>PD</sub>	OC=V <sub>CC</sub> OC=GND		5 30					pF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

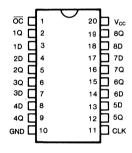
<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current (I<sub>OL</sub> = 24 mA @ V<sub>OL</sub> = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATION



#### LOGIC DIAGRAM

# flip-flops coupled to 3-state output buffers with high drive current capability. It can be used in implementing buffer registers, I/O ports, bidirectional bus driver and working registers. The flip-flops are edge-triggered on the positive transition

The '374 consists of 8 high-speed D-type edge-triggered

The flip-flops are edge-triggered on the positive transition of the clock. The Q outputs are set to the logic levels that were set up at the D inputs.

The output buffers are controlled by a common signal  $(\overline{OC})$  which places the outputs at a high-impedance state when it is taken high. The OC signal does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while outputs are off.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

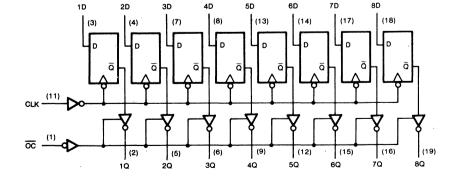
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{\text{CC}}$  and ground.

#### **FUNCTION TABLE**

DESCRIPTION

(Each Flip-Flop)

I	nputs	Output	
ОC	CLK	D	Q
L	1	Н	Н
L	1	L	L
L	L	Х	$Q_0$
Н	Х	Х	Z



Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_0 < V_{CC} + 0.5V) \dots \pm 70 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long ex-
nosure to these conditions may affect device reliability

Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Hullions
.5V to 5.5V
OV to Vcc
to +85°C
to +125°C
Max 500 ns

 Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

# DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	= 25°C	KS74AHCT $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
		,	Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-6mA$	V <sub>CC</sub> 4.2	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 ° 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	· V
Maximum Input Current	liN	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

# AC ELECTRICAL CHARACTERISTICS (Input tr., tr <2 ns), AHCT374

Characteristic	Symbol	Conditions†		T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	Ta = -40°	AHCT C to +85°C OV ± 10%	o +85°C T <sub>a</sub> = -55°C to +125°C		Unit
				Тур	Min	Max	Min	Max	
Maximum Operating Frequency	f <sub>max</sub>			50	35		30		MHz
Propagation Delay,	tpLH	C <sub>L</sub> = 50pF C <sub>L</sub> =150pF		8 11		14 19		17 23	ns
CLK to any Q	t <sub>PHL</sub>	C <sub>L</sub> = 50p C <sub>L</sub> =150p		. 11		14 19		17 23	113
Octo any O	t <sub>PZH</sub>	- R <sub>L</sub> =1kΩ	C <sub>L</sub> = 50pF C <sub>L</sub> =150pF	11 14		18 23		22 28	ns .
	t <sub>PZL</sub>		C <sub>L</sub> = 50pF C <sub>L</sub> =150pF	11 14		18 23		22 28	
Output Disable Time,	tpHZ	$R_L=1k\Omega$		13		18		22	ns
OC to any Q	tPLZ	C <sub>L</sub> =50pF		13		18		22	
Pulse Width, CLK High or Low	t <sub>w</sub>			7	15		18		ns
Setup Time, D before CLK†	t <sub>su</sub>			9	. 14		13		ns
Hold Time, D after CLKf	t'n			-3	0		0		ns
Input Capacitance	CIN			5					pF
Output Capacitance	Cout	Output Disabled		10					pF
Power Dissipation Capacitance*		OC=V <sub>CC</sub> OC=GND	(per stage)	5 30					

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

- · Can be used for implementing
  - Buffer/Storage Registers
  - Shift Registers
  - Pattern Generators
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:

IOL = 8 mA @ VOL = 0.5V

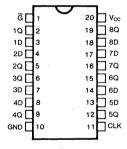
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

   CTANIOT. 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000 | 1000

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATION



#### DESCRIPTION

The '377 contains eight positive-edge-triggered D-type flipflops with an enable ihput. This part is similar to '273 but features a latched clock enable  $(\overline{G})$  instead of a common clear.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse if  $\overline{G}$  is low. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output. The circuits are designed to prevent false clocking by transitioins at the  $\overline{G}$  input.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

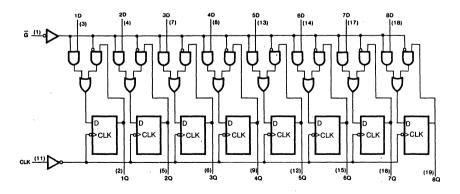
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### **FUNCTION TABLE**

(EACH FLIP-FLOP)

	INPU	OUTPUT	
Ğ	CLK	DATA	Q
Н	Х	Х	Q <sub>0</sub>
L	<b>↑</b>	Н	н
L	ì	L	L
Х	L	Х	$Q_0$

#### LOGIC DIAGRAM



# **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Supply Voltage, V <sub>CC</sub>	4.5V to 5.5V
DC Input & Output Voltages*, VIN, VOUT	OV to Vcc
Operating Temperature	

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . . Max 500 ns

\* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

Characteristic	Symbol	ymbol Test Conditions		<sub>a</sub> = 25°C	KS74AHCT T <sub>a</sub> = -40°C to +85°C	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	v
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-4m A$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μА
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	ΔΙσο	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

# AC ELECTRICAL CHARACTERISTICS (Input tr., tr <2 ns), AHCT377

Characteristic		Symbol Conditions†		T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	$KS74AHCT$ $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> =5.0V ± 10%		Unit	
				Тур	Min	Max	Min	Max		
Maximum Clock	Frequency	f <sub>max</sub>		50	35		30		MHz	
Propagation Delay, CLK to any Q		t <sub>PLH</sub>				16		19		
		t <sub>PHL</sub> C <sub>L</sub> =50pl		10	16		19		ns	
Pulse	G Low	tw		8	14		17			
Width	CLK High or Low	·w		8	14		17		ns	
Setup time	Data			6	10		10			
before CLK1	G High or Low	t <sub>su</sub>		9	15		15		ns	
Hold Time, Data after CLK↑		th		-3	0		0		ns	
Input Capacitan	Input Capacitance			5					рF	
Power Dissipation	on Capacitance*	C <sub>PD</sub>	per package	50					рF	

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

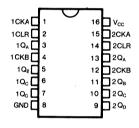
- Individual clock for A and B flip-flops provide dual ÷2 and ÷5 counters
- · Direct clear for each 4-bit counter
- Significant improvement in system density through reduced counter package count.
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs: (IoL = 8 mA @ VoL = 0.5V)
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

## PIN CONFIGURATION



#### DESCRIPTION

These devices incorporate dual divide-by-two and divide-five counters, which can be used to implement cycle lengths equal to any whole and/or cumulative multiple of 2 and/or 5 up to divide-by-100. When connected as a biquinary counter, the separate divide-by-two circuit can be used to provide symmetry (a square ware) at the final outpur stage. The '390 incorporates dual divide-by-two and divide-by-five counters, which can be used to implement cycle lengths equal to any whole and/or cumulative multiples of 2 and/or 5 up to divide-by-100. When connected as a bi-quinary counter, the separate divide-by-tow circuit can be used to provide symmetry (a square wave) at the final outpur stage. The '390 has parallel outputs from each counter stage so that any submultiple of the input count frequency is available for system-timing signals.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### **FUNCTION TABLES**

BCD COUNT SEQUENCE (EACH COUNTER) (See Note A)

COUNT		OUTPUT						
	QD	Qc	QB	QA				
0	L	L	L	L				
1	L	L.	L	Н				
2	L	L	Н	L				
3	L	L	Н	Н				
4	L	Н	L	L				
5	L	Н	L	Н				
6	L	Н	Н	L				
7	L	Н	Н	Н				
8	Н	L	L	L				
9	Н	L	L	Н				

BIQUINARY (5-2) (EACH COUNTER) (See Note B)

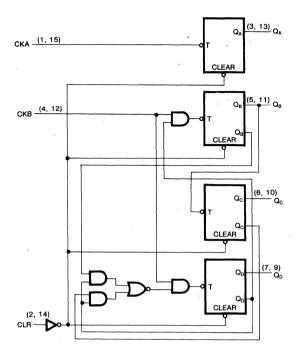
COUNT		OUTPUT						
	QD	Qc	QB	$Q_{A}$				
0	L	L	L	L				
1	L	L	L	Н				
2	L	L.	Н	L				
3	L	L	Н	Н				
4	L	Н	L	L				
5	Н	L	L	L				
6	Н	L	L	Н				
7	Н	L	Н	L				
8	Н	L	Н	Н				
9	Н	н	L	L				

NOTES A. Output QA is connected to input CKB for BCD count.

B. Output QD is connected to input CKA for biquinary count.



## **LOGIC DIAGRAM**



# **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> , -0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.

These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

† Power Dissipation temperature derating:

# **Recommended Operating Conditions**

Supply Voltage, V<sub>CC</sub> . . . . . . . . . . . . 4.5V to 5.5V DC Input & Output Voltages\*, VIN, VOUT ... OV to Vcc Operating Temperature

KS74AHCT: -40°C to +85°C Range KS54AHCT: -55°C to +125°C

Input Rise & Fall Times, tr, tf ..... Max 500 ns

\* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)



# DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T	a = 25°C	KS74AHCT T <sub>a</sub> = -40°C to +85°C	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
			Тур	Typ Guaranteed Limits			
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH} \text{ or } V_{IL}$ $I_{O}=-20\mu\text{A}$ $I_{O}=-4\text{mA}$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> -0.1	٧
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	٧
Maximum Input Current	lin	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current		per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

# AC ELECTRICAL CHARACTERISTICS (Input tr, tr<2 ns), AHCT390

Characteristic		Symbol	Conditions <sup>†</sup>	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	$KS74AHCT$ $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT  T <sub>a</sub> = -55°C to +125°C  V <sub>CC</sub> = 5.0V ± 10%		Unit
				Тур	Min	Max	Min	Max	
Propagation Delay, CKA to Q <sub>A</sub> or CKB to	Q <sub>B</sub>	f <sub>max</sub>		50	30		25		MHz
Propagation Delay,		tpLH		9		15		18	ns
CKA to Q <sub>A</sub>		tehl		9		15		18	ns
Propagation Delay,		t <sub>PLH</sub>		24		40		48	ns
CKA to Q <sub>C</sub>		tpHL		24		40		48	ns
Propagation Delay, CKB to Q <sub>B</sub>		t <sub>PLH</sub>	C <sub>L</sub> =50pF	10		17		21	ns
		tpHL		10		17		21	ns
Propagation Delay,	•	tpLH		16		27		33	ns
CKB to Q <sub>C</sub>		t <sub>PHL</sub>		16		27		33	ns
Propagation Delay,		tpLH		10		17		21	ns
CKB to Q <sub>D</sub>		tpHL		10		17		21	ns
Propagation Delay, CLR to Any Q		t <sub>PHL</sub>		14		24		29	ns
Pulse Width	CKA or CKB High or Low	t <sub>w</sub>		7	12		15	,	ns
T dise Width	CLR High			7	12		15		
Minimum Setup Time, CLR inactive before CKA or CKB		tsu		5	8		10		ns
Input Capacitance		CIN		5					pF
Power Dissipation Ca	oocitance	C <sub>PD</sub>							pF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} \ V_{CC}^2 \ f \ + \ I_{CC} \ V_{CC}$ .

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.



- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
  - IOL = 8 mA @ VOL = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

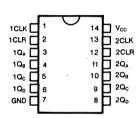
# DESCRIPTION

The '393 consists of two independent 4-bit binary counters each with its own clear and clock inputs. N-bit binary counters can be implemented with each package providing the capability of divide-by-256. parallel outputs from each counter stage provided any submultiple of the input count frequency for system timing signals.

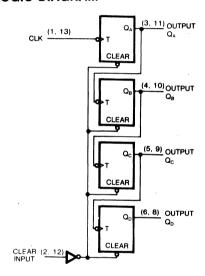
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{\text{CC}}$  and ground.

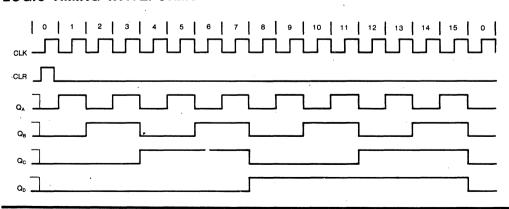
#### PIN CONFIGURATION



#### LOGIC DIAGRAM



#### LOGIC TIMING WAVEFORMS



# **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, $T_{stg} \dots -65$ °C to $+150$ °C
Power Dissipation Per Package, $P_d{}^\dagger$ 500 mW

Power Dissipation Per Package, Pd<sup>†</sup> . . . . . . 500 mW
 Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Supply Voltage, V<sub>CC</sub> . . . . . . . . . . . 4.5V to 5.5V DC Input & Output Voltages\*, V<sub>IN</sub>, V<sub>OUT</sub> . . OV to V<sub>CC</sub> Operating Temperature

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

Characteristic	Symbol	Test Conditions	Ta	= 25°C	KS74AHCT $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
	<u> </u>		Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	<b>V</b>
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> -0.1 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	VoL	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> =20µA I <sub>O</sub> =4mA I <sub>O</sub> =8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	l <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	loc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μÁ
Additional Worst Case Supply Current	Δlcc	per input pin  V <sub>I</sub> =2.4V  other inputs: at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0µA		2.7	2.9	3.0	mA

# AC ELECTRICAL CHARACTERISTICS (Input t<sub>r</sub>, t<sub>i</sub>≤2 ns), AHCT393

Characteristic		Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	T <sub>a</sub> = -40°	AHCT C to +85°C 0V±10%	KS54AHCT  T <sub>a</sub> = -55°C to +125°C  V <sub>CC</sub> = 5.0V ± 10%		Unit
				Тур	Min	Max	Min	Max	
Maximum Cloc	k Frequency	f <sub>max</sub>		50	30		25		MHz
Propagation De	elay,	t <sub>PLH</sub>		14		22		26	ne
A to Q <sub>A</sub>		t <sub>PHL</sub>		14		22		26	ns
Propagation De	elay,	t <sub>PLH</sub>		18		27		32	ns
A to Q <sub>B</sub>		t <sub>PHL</sub>	C <sub>L</sub> =50pF	18		27		32	113
Propagation Dealy,		t <sub>PLH</sub>		20		33		40	ns
A to Q <sub>C</sub>	•	t <sub>PHL</sub>		20		33		40	113
Propagation De	elay,	tpLH	*	26		40		48	ns
A to Q <sub>D</sub>	•	t <sub>PHL</sub>		26		40		48	113
Propagation Dealy, CLR to any Q		t <sub>PHL</sub>		15		25		30	ns
Pulse A Input High or Low Width CLR High				7	12		15		ns
		t <sub>w</sub>		7	12		15		
Setup Time, CLR Inactive before A		t <sub>su</sub>		, 5	8		10		ns
Input Capacitar	nce	CIN		. 5					рF
Power Dissipation Capacitance*		C <sub>PD</sub>	(per counter)	40					pF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:

 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5 \text{V}$ 

- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

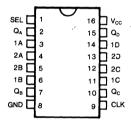
## **DESCRIPTION**

These are high-speed quad 2-port registers. They are the logical equivalent of a quad 2-input multiplexer followed by a quad 4-bit edge-triggered register. A common select input (SEL) selects between two 4-bit input ports. The selected data is transferred to the output register on the low-to-high transition of the clock input.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### PIN CONFIGURATION



#### **FUNCTION TABLE**

	Inputs						
SEL	Port 1	Port 2	Q				
ı	ı	Х	L				
l	h	Х	Н				
h	Х	ı	L				
h	Х	h	Н				

- I = Low Voltage Level one setup time prior to the low-to-high clock transition
- h = High Voltage Level one setup time prior to the low-to-high clock transition

# 1A (3) SEL (11) 2A (4) 1B (6) 2B (5) 1C (11) 2C (12) 1D (14) 2D (13) CLK R (10) CLK R (11) CLK R (15) 
# **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V)$ ±20 mA
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . Max 500 ns \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

# DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T	a = 25°C	KS74AHCT T <sub>a</sub> = -40°C to +85°C	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> -0.1	v
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0µA		2.7	2.9	3.0	mA

# AC ELECTRICAL CHARACTERISTICS (Input tr, tr <2 ns), AHCT399

Characteristic		1 1		T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	KS74AHCT $T_a = -40$ °C to +85°C $V_{CC} = 5.0V \pm 10$ %		KS54AHCT  T <sub>a</sub> = -55°C to +125°C  V <sub>CC</sub> = 5.0V ± 10%		Unit
			:	Тур	Min	Max	Min	Max	
Propagation Delay, CLK to Q		tpLH	C <sub>L</sub> =50pF	12		19		23	ns
		t <sub>PHL</sub>		12		19		23	
Pulse Width, CLK High or Low		tw		6	10		15		ns
Time	Time Data		į	6	10		15		ns
before CLK1 Word Select		t <sub>su</sub>		. 6	, 10		15		
Hold Time, Data after CLK1		t <sub>h</sub>		-3	0		0		ns
Input Capacitance		CiN		5					pF
Power Dissipation	Capacitance*	C <sub>PD</sub>							pF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

# Dual Retriggerable Monostable Multivibrator with Clear

Preliminary Specifications

#### **FEATURES**

- Simple pulse width formula tw = 0.45RC
- . DC triggered from active HIGH or active Low inputs
- Retriggerable for very long output pulses up to 100% duty cycle
- · Overriding clear terminates output pulse
- Schmitt trigger A & B inputs allow infinite rise and fall times on these inputs
- Functions, pin-out, speed and drive compativility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High drive current outputs:
  - $I_{OL} = 8mA @ V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range; 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

# **DESCRIPTION**

The '423 contains dual retriggerable monostable multivibrators with output pulsewidth control by two methods. The basic pulse time is programmed by selection of an external resistor (R<sub>EXT</sub>) and capacitor (C<sub>EXT</sub>). The external resistor and capacitor are normally connected as shown timing component.

Once triggered, the basic output pulse width may be extended by retriggering the gated active Low-going edge input (Ai) or the active High-going edge input (Bi). By repeating this process, the output pulse period (nQ=HIGH,  $n\overline{Q}$ =LOW) can be made as long as desired.

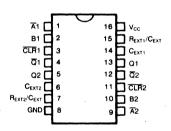
Pulse width stability over a wide range of temperature and supply is achieved using linear CMOS techniques.

The output pulse equation is simply;

 $t_W=0.45\times(R_{EXT})$  (C<sub>EXT</sub>)

Where  $t_w$  is in seconds. R is in ohm. and C is in fards. All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{\text{CC}}$  and ground.

#### PIN CONFIGURATION



#### **FUNCTION TABLE**

	Inputs	Outputs			
CLR	Ā	В	Q	ā	
L	Х	X	L	Н	
X	`H	X	L.	Н	
X	X	L	L	Н	
Н	L	<b>†</b>	л	T	
Н	<b>+</b>	Н	J.	l T	

H= HIGH voltage level

L= LOW voltage level

X= don't care

↑= LOW to HIGH transition

↓= HIGH to LOW transition

'L'= one LOW level output pulse

# **Absolute Maximum Ratings\***

Supply Voltage Range $V_{CC}$ ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, Iok
(Vo<-0.5V or Vo>Vcc+0.5V) ±20 mA
Continuous OUtput Current Per Pin, Io
(-0.5V <vo<v<sub>CC+0.5V) ±35 mA</vo<v<sub>
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> -65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-
posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package(N): -12mW/°C from 65°C to 85°C Ceramic Package(J): -12mW/°Cfrom100°C to 125°C

# **Recommended Operating Conditions**

Supply Voltage,	V <sub>CC</sub> 4.5V to 5.5V
DC Input & Out	out Voltages*, V <sub>IN</sub> , V <sub>OUT</sub> 0V to V <sub>CC</sub>
Operating Temp	erature
Range	KS74AHCT: -40°C to +85°C
	KS54AHCT: -55°C to +125°C
Input Rise & Fa	Il Times, t <sub>r</sub> , t <sub>f</sub> Max 500 ns
* Unused inputs	must always be tied to an appropriate logic

voltage level (either V<sub>CC</sub> or GND)

Characteristic	Symbol Test Conditions		T <sub>a</sub> = 25°C		$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		
			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	Voh	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 . 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	l <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current		per input in V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

# AC ELECTRICAL CHARACTERISTICS (Input tr. tr≤2 ns), AHCT 423

Characteristic	Symbol	Conditionel Voc. = 5 NV		Ta = -40°	KS74AHCT T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%		KS54AHCT T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> =5.0V ± 10%	
			Тур	Min	Max	Min	Max	
Propagation Delay	tpLH		18		33		40	ns
Ā, B to Q, Q	tpHL	C <sub>L</sub> =50pF	18		33	,	40	113
Propagation Delay	tplH	C <sub>ext</sub> =0,	16		27		33	ns
CLR to Q, Q	tpHL	$R_{ext} = 5k\Omega$	16		27		33	113
Output Pulse Width 1	twQ1		116		207		209	ns
Output Pulse Width 2	t <sub>WQ2</sub>	$C_L$ =50pF $C_{ext}$ =1000pF $R_{ext}$ =10k $\Omega$	4.5	3.8	5.2	3.8	5.2	μS
Trigger Pulse Width	t <sub>w</sub>	C <sub>L</sub> =50pF A <sub>i</sub> =LOW	5		16		20	ns
Trigger Pulse Width	t <sub>w</sub>	C <sub>L</sub> =50pF B <sub>i</sub> =High	5		16		20	ns
Clear Pulse Width	t <sub>w</sub>	C <sub>L</sub> =50pF CLR <sub>i</sub> =LOW	6		16		20	ns
External Timing Resistance	R <sub>ext</sub>			2	1,000	2	1,000	kΩ
External Timing Capacitance	Cin			1	no restri	ction		
Input Capacitance	Cin		5					pF
Power Dissipation Capacitance	C <sub>PD</sub>							pF

<sup>\*</sup> CPD determines the no-load dynamic power dissipation: PD=CPD Vcc² f + Icc Vcc.

# **Application Information**

The basic output pulse width is determined by the value of external capacitance and timing resistance. For output pulse widths greater than  $100\mu s$  or external capacitance greater than 1000pF the following equation should be used.

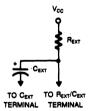
$$t_w = k \cdot R_{ext} \cdot C_{ext}$$

Where

t<sub>w</sub> is in second K is the multiplying factor and is approximately 0.45 for C<sub>ext</sub>≥1000pF C<sub>ext</sub> is in F

For best results, system ground should be applied to the  $C_{\text{ext}}$  terminal. These devices do not require a switching diode in series with the  $R_{\text{ext}}/C_{\text{ext}}$  terminal (as required by some other monostable multivibrators)

# **TIMING COMPONENT**



<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current
   (I<sub>OL</sub> = 24 mA @ V<sub>OL</sub> = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

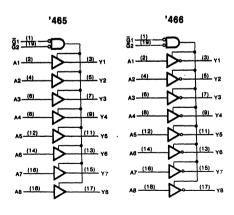
KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

# **PIN CONFIGURATIONS**

'467 and '468 '465 and '466 Ğ1 🔲 1Ğ 🗆 20 Vcc 20 ] Vcc A1 ☐ 2 2 19 🗖 2Ğ 19 7 <u>G</u>2 1A1[ 18 🔲 A8 1Y1 [ 18 2A4 Y1 3 17 2Y4 17 □ Y8 1A2 🔲 A2 4 Y2 1 5 16 A7 1Y2 🗍 16 🔲 2A3 A3 🗆 6 15 🔲 Y7 1 A 3 🗖 15 🗖 2Y3 Y3 🛛 7 14 A6 1Y3 🗖 14 T 2A2 13 Y6 184 🗖 13 1 272 A4 174 12 2A1 12 🔲 A5 11 F 2Y1 GND 11 Y5 GND [

#### LOGIC DIAGRAMS



#### DESCRIPTION

These high-speed octal buffers and drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and busoriented receivers and transmitters. The designer has the choice of inverting/ noninverting outputs and various types of output controls.

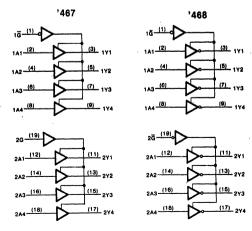
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### **FUNCTION TABLE**

	Input	Output		
Ğ,	Ğ₂	Α	'465	'466
L	L	L	L	Н
L	L	. н	н	L
Н	x	Χ	Z	Z
X	Н	Х	Z	Z

	Input	Output		
G	G	Α	'467	'468
Н	L	L	L	Н
Н	L	Н	H	L
L	Н	Х	·Z	Z



# KS54AHCT 465/466 KS74AHCT 467/468

# Octal Buffers and Line Drivers with 3-State Outputs

# Absolute Maximum Ratings\*

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + 1.00 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.

These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability

† Power Dissipation temperature derating:

# Recommended Operating Conditions Supply Voltage, Vcc 4.5V to 5.5V

DC Input & Output Voltages\*, V<sub>IN</sub>, V<sub>OUT</sub> . . . OV to V<sub>CC</sub>
Operating Temperature

Rance

KS74AHCT: -40°C to +85°C

KS54AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

Characteristic	Symbol	Test Conditions	T,	= 25°C	KS74AHCT T <sub>a</sub> = -40°C to +85°C	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
,			Тур		Guaranteed Lim	its	1
Minimum High-Level Input Voltage	V <sub>IH</sub>	·		2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	V <sub>IL</sub> .			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-6mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# KS54AHCT 465/466 KS74AHCT 467/468

# Octal Buffers and Line Drivers with 3-State Outputs

AC ELECTRICAL CHARACTERISTICS (Input tr., tr<2 ns), AHCT465, AHCT468

Parameter	Symbol	Symbol Conditions $\begin{array}{c} C_L = 50 pF \\ C_L = 150 pF \end{array}$		Symbol Cond	$T_a = 25 ^{\circ} \text{C}$ Note that the conditions $T_c = 25 ^{\circ} \text{C}$		KS74AHCT $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 5.0V \pm 10^{\circ}$		54AHCT T <sub>a</sub> = +55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%		Unit
				Тур	Min	Max	Min	Max			
Propagation Delay,	t <sub>PLH</sub>					12 17		14 20			
A to Y	t <sub>PHL</sub>	C <sub>L</sub> =50pl C <sub>L</sub> =150		7 10		12 17		14 20	ns		
Output Enable Time, Enable to Y	t <sub>PZH</sub>	$R_L = 1 k\Omega$	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	12 15		20 25		24 30	ns		
	t <sub>PZL</sub>		C <sub>L</sub> =50pF C <sub>L</sub> =150pF	12 15		20 25		24 30			
Output Disable Time,	t <sub>PHZ</sub>	$R_L = 1 k\Omega$		13		18		22	ns		
Enable to Y	tpLZ	C <sub>L</sub> =50pl	=	13		18		22			
Input Capacitance	CIN			5					рF		
Output Capacitance	Cout	Output Disabled		10					pF		
Power Dissipation Capacitance* (per stage)	C <sub>PD</sub>		Output Disabled Output Enabled						рF		

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} \ V_{CC}^2 \ f + I_{CC} \ V_{CC}$ . For AC switching test circuits and timing waveforms see section 2.

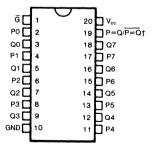
- Compares two 8-bit words
- '518, '520 and 522 have 20kΩ pull-up Resistors on Q Inputs

TYPE	INPUT PULL-UP RESISTOR	OUTPUT FUNCTION AND CONFIGURATION
'518	Yes	P=Q Open-Drain
'519	No	P=Q Open-Drain
'520	Yes	P=Q Totem-Pole
'521	No	P=Q Totem-Pole
'522	Yes	P=Q Open-Drain

† '521 is identical to '688

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- · 3-State outputs with high drive current
- ( $I_{OL} = 24$  mA @  $V_{OL} = 0.5$ V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
   KS74AHCT: -40°C to +85°C
   KS54AHCT: -55°C to +125°C
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATION



† P=Q for '518 and '519; P=Q for '520, '521, '522.

# **DESCRIPTION**

These identity comparators perform comparisons on two eight-bit binary or BCD words. The '518 and '519 provide  $P\!=\!Q$  outputs, while the '520, 521, and '522 provide  $\overline{P}\!=\!\overline{Q}$  outputs. The '518, '519, and '522 have open-drain outputs. The '518, '520, and '522 feature 20-k $\Omega$  inputs for analog or switch data.

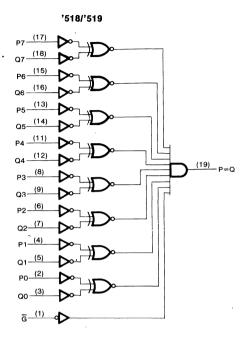
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

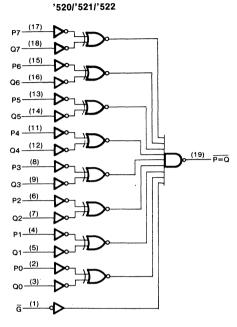
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{\text{CC}}$  and ground.

## **FUNCTION TABLE**

IN	PUTS	OUTPUTS		
DATA P, Q	ENABLE Ğ	P=Q	P=Q	
P=Q	L	Н	L	
P>Q	L.	L	Н	
P <q< td=""><td>L</td><td>L</td><td>Н</td></q<>	L	L	Н	
Х	Н	L	Н	

# LOGIC DIAGRAMS





# Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$ , -0.5V to  $\pm 7V$  DC Input Diode Current,  $I_{IK}$   $(V_I < -0.5V \text{ or } V_I > V_{CC} \pm 0.5V)$   $\pm 20 \text{ mA}$  DC Output Diode Current,  $I_{OK}$   $(V_O < -0.5V \text{ or } V_O > V_{CC} \pm 0.5V)$   $\pm 20 \text{ mA}$  Continuous Output Current Per Pin,  $I_O$   $(-0.5V < V_O < V_{CC} \pm 0.5V)$   $\pm 70 \text{ mA}$  Continuous Current Through  $V_{CC}$  or GND pins  $\pm 250 \text{ mA}$  Storage Temperature Range,  $T_{stg}$   $-65^{\circ}C$  to  $\pm 150^{\circ}C$  Power Dissipation Per Package,  $P_{d}^{\dagger}$  500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Supply Voltage, V<sub>CC</sub> . . . . . . . . . . . 4.5V to 5.5V DC Input & Output Voltages\*, V<sub>IN</sub>, V<sub>OUT</sub> . . OV to V<sub>CC</sub> Operating Temperature

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

Input Rise & Fall Times, tr, tf ..... Max 500 ns

 Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

Parameter	Symbol	Test Conditions	ons T <sub>a</sub> = 25°C		KS74AHCT T <sub>A</sub> = -40°C to +85°C	54AHCT T <sub>a</sub> = -55°C to +125°C	Únit
			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	V
Minimum High-Level Output Voltage (Totem-pole Outputs)	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-6mA$	V <sub>CC</sub> 4.2		V <sub>CC</sub> -0.1 3.84	V <sub>CC</sub> −0.1 3.7	V
Maximum Low-Level Output Voltage (All Outputs)	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current, ('518, '520 and '522 Q input)		V <sub>CC</sub> =Max V <sub>IN</sub> =2.7V V <sub>IN</sub> =0.4V		<del>-</del> 0.2 -0.6 .	-0.2 -0.6	-0.2 -0.6	mA
Maximum Input Current (All other Inputs)	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μА
Maximum Output Leakage Current (Open-Drain Outputs)	loz	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> =V <sub>CC</sub>		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent	lcc	For '518, '520 and '522:  V <sub>IN</sub> =GND (Q0-Q7)  V <sub>IN</sub> =V <sub>CC</sub> or GND (all other inputs)		3.5	3.5	3.5	mA
Supply Current		For '519 and '521: V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μА
Additional Worst Case Supply Current	Δlcc	per input pin Vi=2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0µA		2.7	2.9	3.0	mA

# AC ELECTRICAL CHARACTERISTICS (Input tr. tr <2 ns), AHCT518, AHCT519

Characteristic	Symbol	mbol Conditions	54/74ACHT T <sub>a</sub> = 25°C V <sub>CC</sub> = 5V	$KS74AHCT$ $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$ $V_{CC} = 5V \pm 10^{\circ}$		54AHCT  T <sub>a</sub> = -55°C to +125°C  V <sub>CC</sub> =5.0V ± 10%		Unit
			Typical	Min	Max	Min	Max	
Propagation Delay, P or Q to P=Q	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	20 23		30 35		35 41	
	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	15 18		25 30		30 <sup>-</sup> 36	ns
Propagation Delay,	t <sub>PLH</sub>	C=50pF C <sub>L</sub> =150pF	16 19		23 28		27 33	
G to P=Q	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	11 14		18 23		22 28	ns
Input Capacitance	CiN	,	5					pF
Power Dissipation Capacitance*	C <sub>PD</sub>							pF

# AC ELECTRICAL CHARACTERISTICS (Input tr. tr≤2 ns), AHCT520, AHCT521

Characteristic	Symbol	Conditions	54/74ACHT T <sub>A</sub> = 25°C V <sub>CC</sub> = 5V		$KS74AHCT$ $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$ $V_{CC} = 5V \pm 10^{\circ}$		$54AHCT$ $T_{a = -55^{\circ}C}$ to +125°C $V_{CC} = 5.0V \pm 10\%$	
	F		Typical	Min	Max	Min	Max	
Propagation Delay, P or Q to P=Q	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	12 15		19 24		23 29	
	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	12 15		19 24		23 29	ns
Propagation Delay,	t <sub>PLH</sub>	C=50pF C <sub>L</sub> =150pF	11 14		17 22		20 26	200
G to P=Q	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	11		17 22		20 26	ns
Input Capacitance	Cin		5					pF
Power Dissipation Capacitance*	C <sub>PD</sub>							pF

# AC ELECTRICAL CHARACTERISTICS (Input tr, tr 42 ns), AHC522

Characteristic	Symbol	nbol Conditions	Conditions	$KS74AHCT$ $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$ $V_{CC} = 5V \pm 10^{\circ}$		$54AHCT$ $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Typical	Min	Max	Min	Max	
Propagation Delay, P or Q to P=Q	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	19 22		28 33		33 39	
	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	14 17		23 28		28 34	ns
Propagation Delay,	tpuH	C=50pF C <sub>L</sub> =150pF	16 19		23 28		27 33	
G to P=Q	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	11 14		18 27		22 33	ns
Input Capacitance	CIN		5					pF
Power Dissipation Capacitance*	C <sub>PD</sub>							рF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

# Octal D-Type Transparent Latches with 3-State Outputs

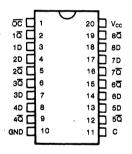
#### **FEATURES**

- 8 latches in a single package
- · Full parallel access for loading
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ( $I_{OL}=24$  mA @  $V_{OL}=0.5V$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATION



#### DESCRIPTION

The '533 consists of 8 high-speed D-type latches coupled to 3-state output buffers with high drive current capability. It can be used in implementing buffer registers, I/O ports, bidirectional bus drivers and working registers.

The latches are transparent: when the enable (C) is high, the  $\overline{Q}$  outputs follow the complements of the data (D) inputs. When the enable is low, the outputs latch at the levels that were set up at the D inputs.

The output buffers are controlled by a common signal  $(\overline{OC})$  which places the outputs at high-impedance state when it is taken high. The  $\overline{OC}$  signal does not affect the internal operations of the latches. Old data can be retained or new data can be entered while outputs are off.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

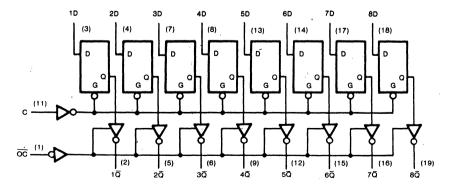
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{\text{CC}}$  and ground.

#### **FUNCTION TABLE**

(Each Latch)

	Output		
<u>oc</u>	Enable C	D	ā
L	Н	Н	L
, L	Н	L	н
L	L	X	۵o
н	, <b>X</b>	Х	Z

#### LOGIC DIAGRAM



# Absolute Maximum Ratings\*

Supply Voltage Range $V_{CC}$ , $-0.5V$ to $+.7V$
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, IO
$(-0.5V < V_O < V_{CC} + 0.5V) + 2.5V$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, $P_d{}^{\dagger}$ 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation

of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Cerarhic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Supply Voltage, V <sub>CC</sub>	4.5V to 5.5V
DC Input & Output Voltages*, VIN, VOUT	OV to Vcc
Operating Temperature	

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . . . Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

Characteristic	Symbol	Test Conditions	Ta	= 25°C	KS74AHCT T <sub>a</sub> = -40°C to +85°C	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-6mA$	V <sub>CC</sub> 4.2	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> - 0.1	V
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	lin	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μА
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	∆lcc	per input pin V <sub>1</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

# Octal D-Type Transparent Latches with 3-State Outputs

# AC ELECTRICAL CHARACTERISTICS (Input tr, tr<2 ns), AHCT533

Characteristic	Symbol	mbol Conditions†		T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	Ta = -40°0	AHCT C to +85°C DV ± 10%	Ta = -55°C	AHCT to +125°C V± 10%	Unit
,				Тур	Min	Max	Min	Max	
Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pl C <sub>L</sub> =150		10 13	ı	16 21		19 25	
D to Q	t <sub>PHL</sub>	C <sub>L</sub> =50pl C <sub>L</sub> =150		10 13		16 21		19 25	ns
Propagation Delay,	t <sub>PLH</sub>	C=50pF C <sub>L</sub> =150		13 16		21 26		25 31	
C to Q	t <sub>PHL</sub>		C <sub>L</sub> =50pF C <sub>L</sub> =150pF			21 26		25 31	ns
Output Enable Time, OC to any Q	t <sub>PZH</sub>	R <sub>L</sub> =1kΩ	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	11 14		18 23		22 28	ns
	tpzL		C <sub>L</sub> =50pF C <sub>L</sub> =150pF	11 14		18 23		22 28	
Output Disable Time,	t <sub>PHZ</sub>	$R_L = 1 k\Omega$		13		18		22	
OC to any Q	t <sub>PLZ</sub>	C <sub>L</sub> =50p	F	13		18		22	ns
Pulse Width, C High	tw			9	15		18		ns
Setup Time, D before C↓	t <sub>su</sub>			9	. 15		18		ns
Hold Time, D after C↓	th			3	5		7.		ns
Input Capacitance	CIN			5					pF
Output Capacitance	Cout	Output [	Disabled	10		,			pF
Power Dissipation Capacitance* (per stage)	C <sub>PD</sub>	ŌC=V <sub>CC</sub> ŌC=GN	; D	5 30					pF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

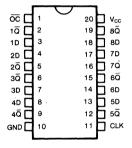
<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- · 3-State outputs with high drive current
- $(I_{OL} = 24 \text{ mA } @ V_{OL} = 0.5 \text{V})$  for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATION



#### DESCRIPTION

The '534 consists of 8 high-speed D-type edge-triggered flip-flops coupled to 3-state output buffers with high drive current capability. It can be used in implementing buffer registers, I/O ports, bidirectional bus driver and working registers.

The flip-flops are edge-triggered on the positive transition of the clock: the  $\bar{\mathbb{Q}}$  outputs are set to the complement of the logic levels that were set up at the D inputs.

The output buffers are controlled by a common signal ( $\overline{OC}$ ) which places the outputs in high-impedance state when it is taken high, the OC signal does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while outputs are off.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

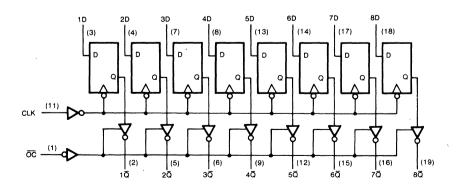
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### **FUNCTION TABLE**

(Each Latch)

I	nputs	Output	
ŌĊ	CLK	D	Q
L	<b>†</b>	Н	L
L	<b>†</b>	L	Н
L	L	Χ	$\bar{\mathbf{Q}}_{0}$
Н	Х	Х	Z

# **LOGIC DIAGRAM**



# **Absolute Maximum Ratings\***

of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

# **Recommended Operating Conditions**

Supply Voltage, V <sub>CC</sub>	4.5V to 5.5V
DC Input & Output Voltages*, VIN, VOUT	0V to $V_{CC}$
Operating Temperature	

Range KS74AHCT:  $-40^{\circ}$ C to  $+85^{\circ}$ C KS54AHCT:  $-55^{\circ}$ C to  $+125^{\circ}$ C Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . . Max 500 ns

\* Unused inputs must always be tied to an appropriate logic voltage level (either Vcc or GND)

Characteristic	Symbol	Test Conditions	Ta	= 25°C	KS74AHCT $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-6mA$	V <sub>CC</sub> 4.2	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μА
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin  V <sub>I</sub> =2.4V  other Inputs: at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0µA		2.7	2.9	3.0	mA

<sup>†</sup> Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# AC ELECTRICAL CHARACTERISTICS (Input tr, tr 42 ns), AHCT534

Characteristic	Symbol	Conditions†		T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	Ta = -40°	AHCT C to +85°C 0V±10%	$T_a = -55$ °C	NAHCT C to +125°C DV ± 10%	Unit
,				Тур	Min	Max	Min	Max	
Maximum Operating Frequency	f <sub>max</sub>	C <sub>L</sub> =50pl	F	50	35		30		MHz
Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pl C <sub>L</sub> =150		8 11		14 19		17 23	
CLK to any Q	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF		8 11		14 19		17 23	ns
Output Enable Time,	t <sub>PZH</sub>	$R_L = 1 k\Omega$	$C_L = 50pF$ $C_L = 150pF$	11 14		18 23		22 28	
	t <sub>PZL</sub>		C <sub>L</sub> =50pF C <sub>L</sub> =150pF	11 14		18 23		22 28	ns
Output Disable Time,	t <sub>PHZ</sub>	$R_L = 1 k \Omega$	13		18		22		
OC to any Q	t <sub>PLZ</sub>	C <sub>L</sub> =50pl	F ,	13		18		22	ns
Pulse Width, CLK High or Low	tw			9	15		18		ns
Setup Time, D before CLKt	t <sub>su</sub>			9	14		17		ns
Hold Time, D after CLK1	th			-3	0		0		ns
Input Capacitance	Cin			5					pF
Output Capacitance	Соит	Output D	isabled	10					pF
Power Dissipation Capacitance* (per stage)	C <sub>PD</sub>	OC=V <sub>CC</sub> OC=GNI		5 30					pF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

# Octal Buffers and Line Drivers with 3-State Outputs

#### **FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current (IoL = 24 mA @ VoL = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### DESCRIPTION

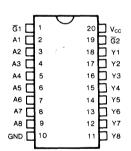
The '540 and '541 are general purpose high-speed octal line drivers/buffers with 3-state outputs. The inputs and outputs are located on opposite sides of the 20-pin package, thus improving circuit board density. The '540 provides inverted data and the '541 provides true data at the outputs.

The three-state control gate is a 2-input NOR such that if either  $\bar{G}1$  or  $\bar{G}2$  is high, all eight outputs are in the high impedance state.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

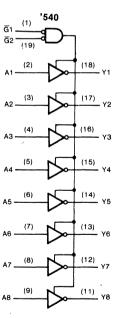
#### PIN CONFIGURATION

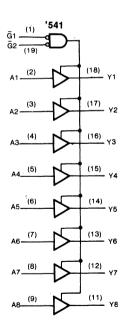


## **FUNCTION TABLE**

	Input	Output			
G,	Ğ₂	Α	'540	'541	
L	L	L	Н	L	
L	L	Н	L	• Н	
Н	×	Х	Z	Z	
X	Н	X	Z	Z	

#### LOGIC DIAGRAMS





# KS54AHCT **540/541** KS74AHCT

# Octal Buffers and Line Drivers with 3-State Outputs

#### Absolute Maximum Ratings\*

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 70 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW

Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Supply Voltage, V<sub>CC</sub> . . . . . . . . . . . 4.5V to 5.5V DC Input & Output Voltages\*, V<sub>IN</sub>, V<sub>OUT</sub> . . . OV to V<sub>CC</sub> Operating Temperature

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . Max 500 ns

 Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

					VEZAAUCT	KS54AHCT	
Characteristic	Symbol	mbol Test Conditions		a = 25°C	KS74AHCT T <sub>a</sub> = -40°C to +85°C	T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	v
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-6mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> -0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=12mA$ $I_{O}=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	l <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ



# AC ELECTRICAL CHARACTERISTICS (Input tr., tr≤2 ns), AHCT540, AHCT541

Characteristic	Symbol			T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	KS74AHCT $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 5.0V \pm 10\%$		$KS54AHCT$ $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Тур	Min	Max	Min	Max	
Propagation Delay,	t <sub>PLH</sub>		C <sub>L</sub> = 50pF C <sub>L</sub> =150pF			12 17		14 20	
A to Y	t <sub>PHL</sub>	C <sub>L</sub> = 50; C <sub>L</sub> =150;		7 10		12 17		14 20	ns
Output Enable Time,	t <sub>PZH</sub>	$R_1 = 1 k\Omega$	C <sub>L</sub> = 50pF C <sub>L</sub> =150pF	12 15		20 25		24 30	ns
G to Y	t <sub>PZL</sub>	U[- 1K12	C <sub>L</sub> =50pF C <sub>L</sub> =50pF	12 15		20 25		24 30	
Output Disable Time	t <sub>PHZ</sub>	$R_L = 1 k\Omega$		14		19		23	1
G to Y t <sub>PLZ</sub>		C <sub>L</sub> =50pF		14		19		23	ns
Input Capacitance	CiN								pF
Output Capacitance	Соит	Output D	isabled	10					pF
Power Dissipation Capacitance* (per stage)	C <sub>PD</sub>	Ā=V <sub>CC</sub> Ā=GND	ā=V <sub>CC</sub>						pF

<sup>\*\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

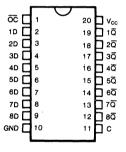
- 8 latches in a single package
- · Full parallel access for loading
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current (I<sub>OL</sub> = 24mA @ V<sub>OL</sub> = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to + 85°C

KS54AHCT: -55°C to + 125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

# PIN CONFIGURATION



#### **DESCRIPTION**

The '563 consists of 8 high-speed D-type latches coupled to 3-state output buffers with high drive current capability. It can be used in implementing buffer register, I/O ports, bidirectional bus drivers and working registers.

The latches are transparent: when the enable (C) is high, the Q outputs follow complements of the data (D) inputs. When the enable is low, the outputs latch at the levels that were set up at the D inputs.

The output buffers are controlled by a common signal (OC) which places the outputs at a high-impedance stage when it is taken high. The OC signal does not affect the internal operations of the latches. Old data can be retained or new data can be entered while outputs are off.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

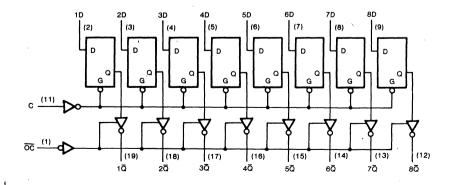
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### **FUNCTION TABLE**

(Each Latch)

	Inputs							
ŌĊ	Enable C	D	Q					
L	Н	Н	L					
L	н	L	н					
L	L	Х	$\widetilde{Q}_{o}$					
• н	X	Х	. <b>Z</b>					

#### LOGIC DIAGRAM



# Octal D-Type Transparent Latches with 3-State Outputs

# **Absolute Maximum Ratings\***

· · · · · · · · · · · · · · · · · · ·
Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_{O} < -0.5V \text{ or } V_{O} > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 70 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.

These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability:

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

	•	_	
Supply Voltage, V	cc	4.5V to	5.5V
DC Input & Outpu	it Voltages*, V <sub>IN</sub> ,	V <sub>OUT</sub> 0V	to V <sub>CC</sub>
Operating Temper	ature		*
Range	KS74AHCT:	-40°C to +	-85°C

KS54AHCT: -40°C to +65°C
KS54AHCT: -55°C to +125°C
Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . Max 500 ns

Characteristic S	Symbol	bol Test Conditions		= 25°C	KS74AHCT T <sub>a</sub> = -40°C to +85°C	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-6mA$	V <sub>CC</sub> 4.2	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> -0.1 . 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=12mA$ $I_{O}=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	ΔΙσο	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA



<sup>\*</sup> Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

# AC ELECTRICAL CHARACTERISTICS (Input tr., tr<2 ns), AHCT563

Characteristic	Symbol	nbol Conditions†		T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	KS74AHCT T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%		KS54AHCT T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> =5.0V ± 10%		Unit	
				Тур	Min	Max	Min	Max		
Propagation Delay,	t <sub>PLH</sub> .	C <sub>L</sub> = 50 C <sub>L</sub> =150		12 15		18 23		22 28		
D to Q	t <sub>PHL</sub>		C <sub>L</sub> = 50pF C <sub>L</sub> =150pF			18 23		22 28	ns	
Propagation Delay, C to Q	t <sub>PLH</sub>	C= 50p C <sub>L</sub> =150		14 17		22 27		27 33		
	t <sub>PHL</sub>	C <sub>L</sub> = 50 C <sub>L</sub> =150		14 17		22 27		27 33	ns	
Output Enable Time, OC to any Q	t <sub>PZH</sub>	$R_L=1k\Omega$	C <sub>L</sub> = 50pF C <sub>L</sub> =150pF	11 14		18 23		22 28		
	tpzL		C <sub>L</sub> = 50pF C <sub>L</sub> =150pF	11 14		18 23		22 28	ns	
Output Disable Time,	t <sub>PHZ</sub>	$R_L=1k\Omega$		13		19		22		
OC to any Q	tpLZ	C <sub>L</sub> =50pF	F	13		19		22	ns	
Pulse Width, C High	t <sub>w</sub>			9	15		18		ns	
Setup Time, D before C↓	t <sub>su</sub>			6	10		10		ns	
Hold Time, D after C↓	th			3	5		7	7.	ns	
Input Capacitance	Cin	·		5					pF	
Output Capacitance	Соит	Output D	isabled	10					pF	
Power Dissipation Capacitance* (per stage)	C <sub>PD</sub>		OC=V <sub>CC</sub> OC=GND					V	pF	

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

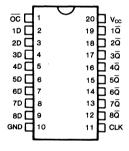
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current (I<sub>OL</sub> = 24mA @ V<sub>OL</sub> = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C + 85°C

KS54HACT: -55°C + 125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATION



#### **DESCRIPTION**

The '564 consists of 8 high-speed D-type edge-triggered flip-flops coupled to 3-state output buffers with high drive current capability. It can be used in implementing buffer registers, I/O ports, bidirectional bus driver and working registers.

The flip-flops are edge-triggered: on the positive transition of the clock, the  $\bar{Q}$  outputs are set to the complement of the logic levels that were set up at the D inputs.

The output buffers are controlled by a common signal ( $\overline{OC}$ ) which places the outputs at high impedance stat when it is taken high. The OC signal does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while outputs are off.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

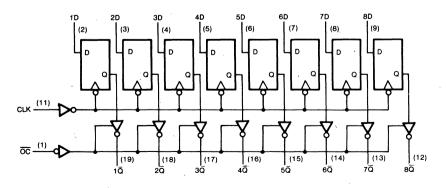
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground

#### **FUNCTION TABLE**

(Each Flip-Flop)

Inputs			Output
ŌĊ	CLK	D	Q
L	<b>†</b>	Н	L
L	<b>↑</b>	L	Н
L	L	Χ	$\tilde{\mathbf{Q}}_{0}$
Н	Х	Х	Z

#### LOGIC DIAGRAM



# **Absolute Maximum Ratings\***

Supply Voltage Range $V_{CC}$ , $-0.5V$ to $+7V$
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 70 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.

These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Supply Voltage, V <sub>CC</sub>	4.5V to 5.5V
DC Input & Output Voltages*, VIN, VOUT	OV to $\ensuremath{\text{V}_{\text{CC}}}$
Operating Temperature	

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . . Max 500 ns

 Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

Characteristic	Symbol	mbol Test Conditions		=25°C	KS74AHCT $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
· ·			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	v
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-6mA$	V <sub>CC</sub> 4.2	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> -0.1 3.84	V <sub>CC</sub> = 0.1	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μА
Maximum Quiescent Supply Current	lcc	$V_{IN}=V_{CC}$ or GND $I_{OUT}=O\mu A$		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	ΔΙ <sub>СС</sub>	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

# AC ELECTRICAL CHARACTERISTICS (Input tr, tr<2 ns), AHCT564

Characteristic	Symbol	Conditions <sup>†</sup>		symbol Conditions†		T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	Ta = -40°0	AHCT C to +85°C DV ±10%	Ta = -55°C	AHCT to +125°C V± 10%	Unit
1.		:		Тур	Min	Max	Min	Max			
Maximum Operating Frequency	f <sub>max</sub>	C <sub>L</sub> = 50	pF	50	35		30		MHz		
Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> = 50 C <sub>L</sub> =150		8 11		14 19		17 23	,		
CLK to any Q	t <sub>PHL</sub>	C <sub>L</sub> = 50pF C <sub>I</sub> =150pF		8 11	,	14 19		17 23	ns		
Output Enable Time,	tpzH	-R <sub>L</sub> =1kΩ	C <sub>L</sub> = 50pF C <sub>L</sub> =150pF	11 14		18 23		<b>22</b> 28	ns		
	t <sub>PZL</sub>		C <sub>L</sub> = 50pF C <sub>L</sub> =150pF	1·1 1·4		18 23		22 28			
Output Disable Time,	t <sub>PHZ</sub>	R <sub>L</sub> =1kΩ C <sub>L</sub> =50pl	R <sub>L</sub> =1kΩ			19 19		22 28	ns		
Pulse Width, CLK High or Low	tw			9	15		18		ns		
Setup Time, D before CLK†	t <sub>su</sub>	٠		9	14		17		ns		
Hold Time, D after CLK†	th		1	-3	0		0		ns		
Input Capacitance	Cin		,	5					pF		
Output Capacitance	Cout	Output Disabled		10					pF		
Power Dissipation Capacitance* (per stage)	C <sub>PD</sub>	OC=V <sub>CC</sub>	ŌC=V <sub>CC</sub>						рF		

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.



<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

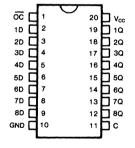
#### **FEATURES**

- 8 latches in a single package
- · Full parallel access for loading
- Function, pin-out, speed and drive compability with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current
   (I<sub>OL</sub> = 24 mA @ V<sub>OL</sub> = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to + 85°C KS54HACT: -40°C to + 125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATION



#### **DESCRIPTION**

The '573 consists of 8 high-speed D-type latches coupled to 3-state output buffers with high drive current capability. It can be used in implementing bufer registers, I/O ports, bidirectional bus drivers and working registers.

The latches are transparent: when the enable (C) is high, the Q outputs follow the data (D) inputs. When the enable is low, the outputs latch at the levels that were set up at the D inputs.

The output buffers are controlled by a common signal (OC) which places the outputs at a high-impedance state when it is taken high. The  $\overline{OC}$  signal does not affect the internal operations of the latches. Old data can be retained or new data can be entered while outputs are off.

There devices provide speeds and drive capability equivalent of their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

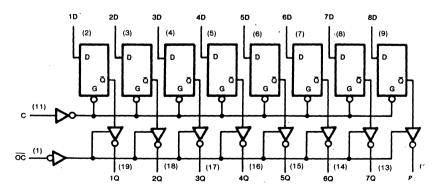
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### **FUNCTION TABLE**

(Each Latch)

	Inputs							
ōc	Enable C	D	Q					
L	Н	Н	н					
L	н	L	L					
L	·L	Х	Q <sub>0</sub>					
н	X	X	Z					

## **LOGIC DIAGRAM**





# Octal D-Type Transparent Latches with 3-State Outputs



Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, Iok
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 70 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.
These are stress fatings only and functional operation
of the device at or beyond them is not implied. Long ex-
posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Supply Voltage, V <sub>CC</sub>	4.5V to 5.5V
DC Input & Output Voltages*, VIN, VOUT	OV to Vcc
Operating Temperature	

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . Max 500 ns

 Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	est Conditions T <sub>a</sub> = 25°		KS74AHCT T <sub>a</sub> = -40°C to +85°C	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
	,		Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	Von	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-6mA$	V <sub>CC</sub> 4.2	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> -0.1 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage		$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=12mA$ $I_{O}=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	<b>&gt;</b>
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μА
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA



# AC ELECTRICAL CHARACTERISTICS (Input tr. tres 2 ns), AHCT573

Characteristic	Symbol	Conditions†		mbol Conditions†		T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	$T_a = -40^\circ$	IAHCT C to +85°C 0V±10%	Ta = -55°C	AHCT to +125°C V± 10%	Unit
				Тур	Min	Max	Mig	Max			
Propagation Delay,	tpLH	C <sub>L</sub> = 50 C <sub>L</sub> =150		9 12		14 19		17 23			
D to Q	t <sub>PHL</sub>	C <sub>L</sub> = 50 C <sub>L</sub> =150		9 12		14 19		17 23	ns		
Propagation Delay,	t <sub>PLH</sub>	C=50pF C <sub>L</sub> =150		12 15		20 25	,	24 30			
C to Q	t <sub>PHL</sub>	C <sub>L</sub> = 50pF C <sub>L</sub> =150pF		12 15		20 25		24 30	ns		
Output Enable Time	t <sub>PZH</sub>	PZH R <sub>L</sub> =1kΩ	C <sub>L</sub> = 50pF C <sub>L</sub> =150pF	11 14		18 23		22 28	ns		
OC to any Q	t <sub>PZL</sub>		C <sub>L</sub> = 50pF C <sub>L</sub> =150pF	11 14		18 23		22 28			
Output Disable Time	t <sub>PHZ</sub>	$R_L=1k\Omega$		13		19		22			
OC to any Q	t <sub>PLZ</sub>	C <sub>L</sub> =50pl	=	13		19		22	ns		
Pulse Width, C High	t <sub>w</sub>			9	15		18		ns		
Setup Time, D before C↓	t <sub>su</sub>			6	10		12		ns		
Hold Time, D after C↓	t <sub>h</sub>			4	7		9		ns		
Input Capacitance	CIN			5					pF		
Output Capacitance	Соит	Output D	isabled	10					pF		
Power Dissipation Capacitance* (per stage)	C <sub>PD</sub>	OC=V <sub>CC</sub>		5 30					pF		

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

#### **FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current
- ( $I_{OL}$  = 24 mA @  $V_{OL}$  = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
   KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### DESCRIPTION

The '574 consists of 8 high-speed D-type edge-triggered flip-flops coupled to 3-state output buffers with high drive current capability. It can be used in implementing buffer registers, I/O ports, bidirectional bus drivers and working registers.

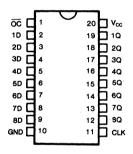
The flip-flops are edge-triggered on the positive transition of the clock. The Q outputs are set to the logic levels that were set up at the D inputs.

The output buffers are controlled by a common signal  $(\overline{OC})$  which places the outputs at a high-impedance state when it is taken high. The  $\overline{OC}$  signal does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while outputs are off.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### PIN CONFIGURATION

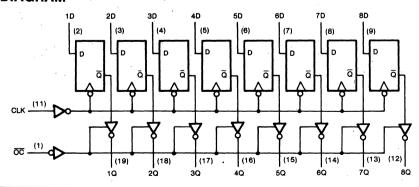


#### **FUNCTION TABLE**

(Each Flip-Flop)

1	nputs	Output	
ŌĊ	CLK	D	Q
L	<b>†</b>	Н	Н
L	<b>्</b> ↑	L.	L.
L	L	Х	$Q_0$
Н	X	Χ	Z

## **LOGIC DIAGRAM**



## **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 70 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW

<sup>\*</sup> Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Supply Voltage, V <sub>CC</sub>			4.5V	to 5	5.5V
DC Input & Output Voltage	s*, V <sub>IN</sub> , V	/оит	0	V to	Vcc
Operating Temperature					
- 140-	ALIOT	40			

 Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	characteristic Symbol Test Conditions		T <sub>a</sub> = 25°C		KS74AHCT $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit	
			Тур		Guaranteed Limits			
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	٧	
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	0.8	v	
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-6mA$	V <sub>CC</sub> 4.2	V <sub>CC</sub> −0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	v	
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v	
Maximum Input Current	lin	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μА	
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μΑ	
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ	
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA	

## AC ELECTRICAL CHARACTERISTICS (Input t<sub>r</sub>, t<sub>i</sub>≤2 ns), AHCT574

Characteristic	Symbol	Conditions <sup>†</sup>		1 +		T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	Ta = -40°	AHCT C to +85°C DV±10%	T. = -55°C	IAHCT C to +125°C DV ± 10%	Unit
				Тур	Min	Max	Min	Max			
Maximum Operating Frequency	f <sub>max</sub>	C <sub>L</sub> = 50	ρF	50	35		30		MHz		
Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> = 50 C <sub>L</sub> =150		8 11		14 19		17 23			
CLK to any Q	t <sub>PHL</sub>		C <sub>L</sub> = 50pF C <sub>L</sub> =150pF			14 19		17 23	ns		
Output Enable Time,	t <sub>PZH</sub>	R <sub>L</sub> =1kΩ	C <sub>L</sub> = 50pF C <sub>L</sub> =150pF	11 14		18 23		22 28			
	t <sub>PZL</sub>		C <sub>L</sub> = 50pF C <sub>L</sub> =150pF	11 14		18 23		22 28	ns		
Output Disable Time,	t <sub>PHZ</sub>	$R_L=1k\Omega$		13		18		22	ns		
OC to any Q	t <sub>PLZ</sub>	C <sub>L</sub> =50pl	=	13		18		22			
Pulse Width, CLK High or Low	t <sub>w</sub>			9	15		18		ns		
Setup Time, D before CLKt	t <sub>su</sub>			9	14		17		ns		
Hold Time, D after CLK1	t <sub>h</sub>			-3	0		o		ns		
Input Capacitance	CiN			5					рF		
Output Capacitance	Cout	Output Disabled		10					pF		
Power Dissipation Capacitance* (per stage)	C <sub>PD</sub>	OC=V <sub>CC</sub>		. 5 30					рF		

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} \ V_{CC}^2 \ f + I_{CC} \ V_{CC}$ .
† For AC switching test circuits and timing waveforms see section 2.

# KS54AHCT 590/591 KS74AHCT

# 8-Bit Binary Counters with Output Registers

Preliminary Specifications

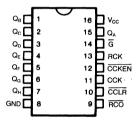
#### **FEATURES**

- Choice of 3-State ('590) and Open-Drain ('591) Outputs
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current
   (I<sub>OL</sub> = 24 mA @ V<sub>OL</sub> = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
   KSZAANCT: \_\_ARCC to\_\_LRESC.

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATION



#### DESCRIPTION

These devices each consist of an 8-bit binary counter which feeds an 8-bit register. The counter is incremented on the rising edge of the CCK input, provided that clock enable,  $\overline{\text{CCKEN}}$ , is low. When the counter increments to the all ones condition, ripple carry out,  $\overline{\text{RCO}}$ , will go low. This enables either synchronous cascading of the counters by connecting the  $\overline{\text{RCO}}$  of the first stage to the  $\overline{\text{CCKEN}}$  of the second, or clocking both circuits in parallel. Ripple cascading is accomplished by connecting the  $\overline{\text{RCO}}$  of the first to the CCK of the second stage. A clear input is also provided which will reset the counter to the all zeros state.

The output register is loaded with the contents of the counter on the rising edge of the register clock, RCK. The outputs of this register feed the outputs which are enabled when the enable input,  $\overline{G}$ , is taken low. This enables connection of this part to a system bus. The Q outputs of the '590 are 3-State and those for '591 are Open-drain.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{\text{CC}}$  and ground.

#### **FUNCTION TABLE**

		INPUTS			FUNCTION			
G	RCK	CCLR	CCKEN	ССК	FONCTION			
Н	х	Х	X	Х	Q Outputs disable			
L	Х	Х	X	Х	Q Outputs enable			
L		Х	Х	Х	Counter data is stored into register			
L	Z	Х	X	Х	Register state is not changed			
L	Х	L	х	Х	Counter clear			
L	Х	Н	L	7	Advance one count			
L	X	Н	L	7	No count			
L	Х	Н	Н	X	No count .			

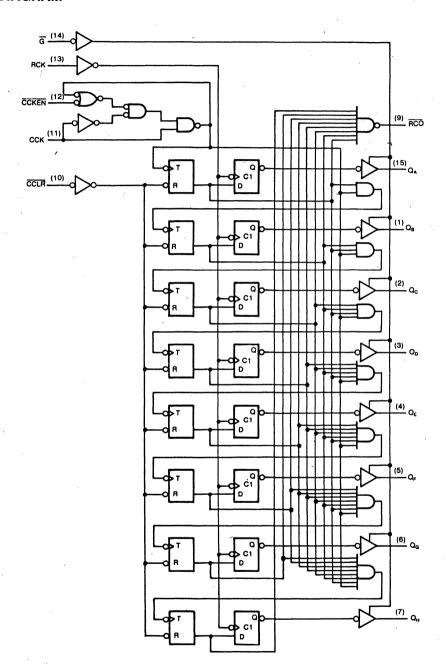
X: Don't care

RCO =  $Q_A' \cdot Q_B' Q_C' \cdot Q_D' Q_E' \cdot Q_F' Q_G' \cdot Q_H'$ 

(Q<sub>A</sub>' ∼ Q<sub>H</sub>': Internal outputs of the counter)



## **LOGIC DIAGRAM**



#### **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 70 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, P <sub>d</sub> <sup>†</sup> 500 mW

<sup>\*</sup> Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . . Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	Tį	= 25°C	KS74AHCT $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit	
			Тур		Guaranteed Limits			
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	٧	
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧	
Minimum High-Level Output Voltage (All '590 Outputs and '591 RCO Output)	VoH	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-6mA$	V <sub>CC</sub> 4.2	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> -0.1	V <sub>CC</sub> −0.1 3.7	v	
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}$ = $V_{IH}$ or $V_{IL}$ $I_{O}$ =20 $\mu$ A $I_{O}$ =12 $\mu$ A $I_{O}$ =24 $\mu$ A	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v	
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ	
Maximum Output Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub>		±0.5	±5.0	±10.0	μΑ	
Maximum Quiescent Supply Current	lcc	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μΑ	
Additional Worst Case Supply Current	ΔΙσο	per input pin V <sub>1</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA	

180

# AC ELECTRICAL CHARACTERISTICS (Input tr, tr <2 ns), AHCT590

Characteristic		Symbol	Conditions <sup>†</sup>	54/74ACHT T <sub>a</sub> = 25°C V <sub>CC</sub> = 5V	Ta = -40°0	AHCT C to +85°C V±10%	Ta = -55°C	HCT to +125°C V± 10%	Unit
				Typical	Min	Max	Min Max		1
Maximum Cl	ock Frequency	f <sub>max</sub>		50	30		25	` .	ņs
Propagation	Delay,	t <sub>PLH</sub>		15		25		29	
CCK↑ to RC	<u> </u>	t <sub>PHL</sub>		15		25		29	ns
Propagation CCLR↓ to R		t <sub>PHL</sub>	C <sub>L</sub> =50pF	17		28	,	33	ns
Propagation	Delay,	tpLH		10		16		19	
RCK1 to Q		t <sub>PHL</sub>		10		16		19	ns
Output Enab	le Time,	tpzH		13		18		22	
G√ to Q		t <sub>PZL</sub>	C <sub>L</sub> =50pF	13		18		22	ns
Output Disat	ole Time,	t <sub>PHZ</sub>	R <sub>L</sub> =1KΩ	13		18		22	
Gn to Q		tpLZ		13		18		22	ns
Pulse Duration	CCK or RCK High or Low	t <sub>w</sub>		10	15		20		ns
Duration	CCLR Low			10	15		20		
	CCKEN↓ before	,		10	15		20	,	
Setup Time	CCLRt before .	t <sub>su</sub>		6	10		10		ns
•	CCK† to RCK†††			15	20		25		
Input Capacitance		CiN		5					рF
Output Capacitance (Q Outputs)		Соит	Output Disabled	10					рF
Power Dissip	oation Capacitance*	C <sub>PD</sub>							pF

CPD determines the no-load dynamic power dissipation: PD=CPD VCC2 f + ICC VCC.

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

<sup>††</sup> This setup time ensures the register will see stable data from the counter outputs. The clocks may be tied together in which case the register state will be one clock pulse behind the counter.

# AC ELECTRICAL CHARACTERISTICS (Input t<sub>r</sub>, t<sub>f</sub>≤2 ns), AHCT591

Characteristic		Symbol	Conditions†	54/74ACHT T <sub>a</sub> = 25°C V <sub>CC</sub> = 5V	Ta = -40°	AHCT C to +85°C V±10%	$T_a = -55^{\circ}C$	HCT to +125°C V ± 10%	Unit	
				Typical	Min	Max	Min	Max	1	
Maximum Clo	ock Frequency	f <sub>max</sub>		50	30		25		MHz	
Propagation		t <sub>PLH</sub>		15		25		29	ns	
CCK1 to RC	5	t <sub>PHL</sub>		15		25		29	115	
Propagation CCLR↓ to RC		t <sub>PHL</sub>	$C_L=50pF$ $R_I=1k\Omega$	17		28		33	ns	
Propagation	Delay,	tplH	110-1732	18		31		37	1	
RCK1 to Q		tPHL		10		16		19	ns	
Propagation Delay, G↓ to Q		t <sub>PHL</sub>		14		20		24	ns	
Propagation G1 to Q	Delay,	t <sub>PLH</sub>		14		20		24	ns	
Pulse Duration	CCK or RCK High or Low	t <sub>w</sub>		10	15		20		ns	
Duration	CCLR Low			10	15		20			
	CCKEN↓ Low to CCK↑			10	15		20			
Setup Time	CCLR† High to	t <sub>su-</sub>		6	10		10		ns	
CCK† to RCK†††				15	20		25			
Input Capa	citance	CIN		5					pF	
Power Dissip	oation Capacitance*	CPD							pF	

<sup>\*</sup> CPD determines the no-load dynamic power dissipation: PD=CPD VCC2 f + ICC VCC.

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

<sup>††</sup> This setup time ensures the register will see stable data from the counter outputs. The clocks may be tied together in which case the register state will be one clock pulse behind the counter.

Preliminary Specifications

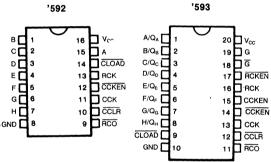
#### **FEATURES**

- Parallel Register Inputs ('592)
- Parallel 3-State I/O: Register Inputs/Counter Outputs ('593)
- Counter Has Direct Overriding Load and Clear
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current
   (I<sub>OL</sub> = 24 mA @ V<sub>OL</sub> = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATIONS



## **DESCRIPTION**

The '592 and '593 both contain an 8-bit register which feeds an 8-bit binary counter. The counter is incremented on the rising edge of the CCK input, provided that clock enable, CCKEN, is low. When the counter increments to the all ones condition, ripple carry out, RCO, will go low. This enables either synchronous cascading of the counters by connecting the RCO or the first stage to the CCKEN of the second, or clocking both circuits in parallel. Ripple cascading is accomplished by connecting the RCO of the first to the CCK of the second stage. A clear input is also provided which will reset the counter to the all zeros state.

The input register is loaded on the rising edge of the register clock, RCK. The outputs of this register feed the counter. The counter is loaded with the register's contents when the clock load, CLOAD, input is taken low.

The '592 differs from the '593 in that the latter device has bidirectional I input/output pins. The 3-state outputs of the counter can be enabled and are active when enable input,  $\overline{G}$ , is taken low and input G is taken high. The outputs of the counter then appear on the register inputs. This enables connection of this part to a system bus. The '593 also has a second clock enable pin,  $\overline{CCKEN}$ , which is active high and it also has an active low register clock enable,  $\overline{RCKEN}$ .

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### **FUNCTION TABLE**

		INPUTS			FUNCTION
RCK	CLOAD	CCLR	CCKEN	сск	ronomon
Х	L	н	Х	Х	Register data is loaded into counter
Х	Н	L	Х	х	Counter clear
	Н	н .	x	х	The data of a thru H inputs is stored into register
-	Н	н	·X	х	Register state is not changed
X	Н	Н	L		Counter advances the count
Х	Н	Н	L	T_	No count
X	Н	Н	Н	Х	No count

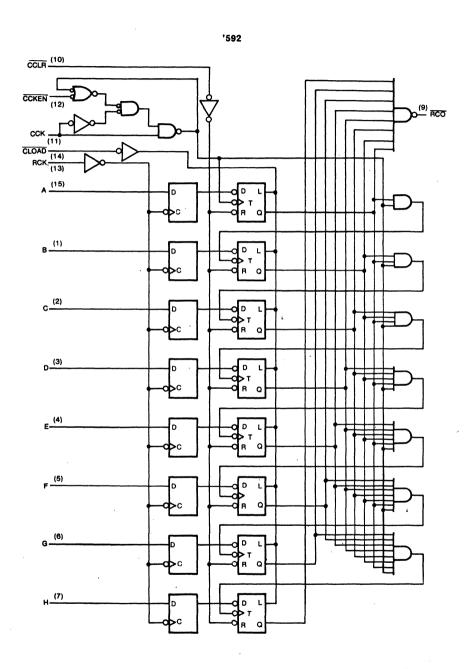
X: Don't care

 $RCO = Q_A' \cdot Q_B' Q_C' \cdot Q_D' Q_E' \cdot Q_F' Q_G' \cdot Q_H'$ 

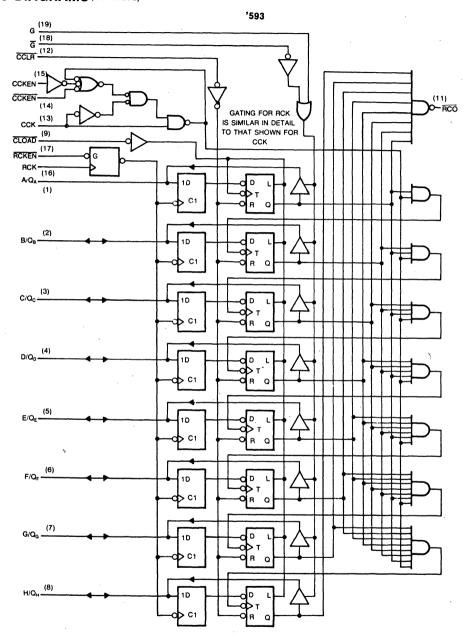
(Q<sub>A</sub>' ∼ Q<sub>H</sub>': Internal outputs of the counter)



## **LOGIC DIAGRAMS**



## LOGIC DIAGRAMS (Continued)



## **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 70 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, P <sub>d</sub> † 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-
posure to these conditions may affect device reliability

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . . . Max 500 ns

 Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

# DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T <sub>a</sub> = 25°C		KS74AHCT T <sub>a</sub> = -40°C to +85°C	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	v
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-6mA$	V <sub>CC</sub> 4.2	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	l <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

## AC ELECTRICAL CHARACTERISTICS (Input tr., tr <2 ns), AHCT592

Characteristic		Symbol	Conditions <sup>†</sup>			C to +85°C	KS54AHCT $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$		
,				Тур	Min	Max	Min	Max	
Maximum Cl	ock Frequency	f <sub>max</sub>		50	30		25		MHz
Propagation	Delay,	t <sub>PLH</sub>		15		25		29	
CCK1 to RC	Ō	tpHL		15		25		29	ns
Propagation	Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pF	15		25		29	
CLOAD↓ to I	RCO	t <sub>PHL</sub>	ο <sub>ε</sub> σορ.	15		25		29	ns
Propagation CCLR		t <sub>PHL</sub>		15	,	25		29	ns
Propagation	Delay,	tpLH	C <sub>L</sub> =50pF	18		30		36	
RCK1 to RC	Ō	t <sub>PHL</sub>	CLOAD=GND	18		30		36	ns
Pulse Width	CCK or RCK High or Low			10	15		20		
width	CCLR Low	t <sub>w</sub>		10	15		20		ns
	CLOAD Low			10	15		20		1
	CCKEN↓ before		4	10	15		20		
Setup Time	CCLRt before	t <sub>su</sub>		6	10		10		ns
	RCK1 before			10	15		20		
	Data A-H1 before RCK1			10	15		20		
Hold Time		th		-3	0		0		ns
Input Capaci	tance	CIN		5					рF
Power Dissip	pation Capacitance*	C <sub>PD</sub>							pF

 $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

<sup>††</sup> The RCK† to CCK† setup time ensures that the counter will see stable data from the register output.

# AC ELECTRICAL CHARACTERISTICS (Input tr, tr <2 ns), AHCT593

Characteristic		Symbol	Condition	s†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	T. = - 40°C		KS54 T <sub>a</sub> = -55°C	to +125°C	Unit
		Cymbol Conditions			100-0.01		)V ± 10%	V <sub>CC</sub> = 5.0V ± 10%		-
						Min	Max	Min	Max	
Maximum (	Clock Frequency	f <sub>max</sub>			50	30		25		MH
Propagation	n Delay.	t <sub>PLH</sub>	C <sub>L</sub> =50pl		15 18		25 30		29 35	
CCK1 to Q	• ·	tpHL	C <sub>L</sub> =50p	F	15		25 30		29	ns
			C <sub>L</sub> =150	pr	18				35	-
Propagation		tPLH	C <sub>L</sub> =50pl	F	15 15		25 25		29 29	ns
			C <sub>L</sub> =50pl	=	15		25		29	
Propagation		tpLH	C <sub>L</sub> =150		18		30		35	ns
CLOAD↓ to	Q	t <sub>PHL</sub>	C <sub>L</sub> =50pl C <sub>L</sub> =150		15 18		25 30		29 35	113
Propagation	n Delay	t <sub>PLH</sub>			15		25		29	t
CLOAD↓ to		tPHL	C <sub>L</sub> =50pl	F	15		25		29	ns
Propagation	n Delay,	tpLH	C <sub>L</sub> =50pl	F	18		30		36	
RCK1 to R		t <sub>PHL</sub>	CLOAD=		18		30			ns
Propagation Delay, CCLR↓ to Q		t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF		15 18		25 30		29 35	ns
Propagation Delay, CCLRI to RCO		t <sub>PLH</sub>	C <sub>L</sub> =50pF		15		25		29	ns
Enable_Tim		t <sub>PZH</sub>	$R_L = 1 k\Omega$	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	13 16	,	20 25		24 30	
G† or Ğ∔ to	Q	t <sub>PZL</sub>	TIL TRAS	$C_L=50pF$ $C_L=150pF$	13 16		20 25		24 30	ns
Disable Tim	ne,	t <sub>PHZ</sub>	$R_L = 1k\Omega$		13		20		24	
Ğ∔ or G† to	à	t <sub>PLZ</sub>	C <sub>L</sub> =50pF		13		20		24	ns
Pulse	CCK or RCK High or Low				10	15		20		
Width	CCLR Low	tw			10	15		20		ns
	CLOAD Low				10	15		20		
	CCKEN↓ before			,	10	15		20		
Setup	RCKEN↓ to				10	15		20		
Time	CCLR↓ before CCKt	ț <sub>su</sub>			6	10		10 .		ns .
	RCK1 before CCK111				10	15		20		
Data A-H before RCKf					10	15		20		
Hold Time		th			-3	0		0		ns
Input Capac	citance	CiN			5					рF
Output Cap	acitance	Cout	Output D	isabled	10					рF
Power Diss Capacitance	•	C <sub>PD</sub>								pF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>††</sup> The RCKf to CCKf setup time ensures that the counter will see stable data from the register output.



<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

#### **FEATURES**

- 8-Bit Serial-In, Parallel-Out Shift Registers With Storage.
- Choice of 3-State ('595) or Open-Drain ('596) Parallel Outputs.
- Shift Register Has Direct Clear.
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- . 3-State outputs with high drive current
- (I<sub>OL</sub> = 24 mA @ V<sub>OL</sub> = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges: KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### DESCRIPTION

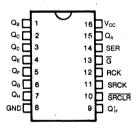
These devices each contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state ('595) or opendrain ('596) outputs. Separate clocks are provided for both the shift register and the storage register. The shift register has a direct-overriding clear, serial input, and serial output pins for cascading.

Both the shift register and storage register clocks are positive-edge triggered. If the user wishes to connect both clocks together, the shift register state will always be one clock pulse ahead of the storage register.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### PIN CONFIGURATION



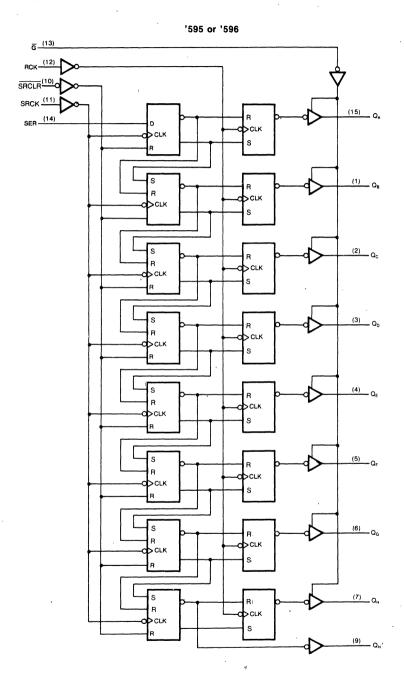
#### **FUNCTION TABLE**

INPUTS					FUNCTION
SER	SRCK	SRCLR	RCK	Ğ	FUNCTION
X	Х	Х	Х	Н	Q <sub>A</sub> thru Q <sub>H</sub> outputs disable
Х	Х	Х	X	L	Q <sub>A</sub> thru Q <sub>H</sub> outputs enable
Х	Х	L	Х	Х	Shift register is cleared.
L	5	Н	Х	x	First stage of S.R. becomes "L". Other stages store the data of previous stage, respectively.
Н		Н	х	х.	First stage of S.R. becomes "H". Other stages store the data of previous stage, respectively.
Х	17L	Н	×	х	State of S.R. is not changed.
Χ	Х	X		X ·	S.R. data is stored into storage register.
X	X	Х	ī	Х	Storage register state is not changed.

X: DON'T CARE



## **LOGIC DIAGRAM**



## 8-Bit Shift Registers with Output Registers

## **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 70 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, $P_d{}^{\dagger}$ 500 mW
$^{\star}$ Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-

posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Supply Voltage, V <sub>CC</sub>	4.5V to 5.5V
DC Input & Output Voltages*, VIN, VOUT	OV to Vcc
Operating Temperature	

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . Max 500 ns
\* Unused inputs must always be tied to an appropriate logic

voltage level (either V<sub>CC</sub> or GND)

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T <sub>a</sub> = 25°C		KS74AHCT T <sub>a</sub> = -40°C to +85°C	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage (All '595 Outputs and '596 Q <sub>H</sub> ' Output)	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{C}=-6mA$	V <sub>CC</sub> 4.2	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> -0.1 3.84	V <sub>CC</sub> −0.1 3.7	٧
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable · =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	ΔΙσο	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA



## AC ELECTRICAL CHARACTERISTICS (Input tr, tr<2 ns), AHCT595, AHCT596

Characteristic		Symbol	Condition	s <sup>†</sup>	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	Ta = - 40°0	AHCT C to +85°C 0V±10%	T. = -55°C	AHCT to +125°C V± 10%	Unit
					Тур	Min	Max	Min	to +125°C	
Propagation		tpLH	C <sub>L</sub> =50pF		9		25		18	ns
SRCK† to	Q' <sub>H</sub>	tpHL	OL-30p.		9		15		18	113
Propagation		t <sub>PLH</sub>	C <sub>L</sub> =50pl C <sub>L</sub> =150		11 14		16 21			ns
RCKf to (	Q <sub>A</sub> thru Q <sub>H</sub>	t <sub>PHL</sub>	C <sub>L</sub> =50pl		11 14	}	17 22			115
Output Enable Time,		t <sub>PZH</sub>	5	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	14 17		20 25			
Ğł to Q <sub>A</sub> thru Q <sub>H</sub> ('595 only)	t <sub>PZL</sub>	R <sub>L</sub> =1kΩ	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	14 17		20 25		1	ns	
	sable Time,	t <sub>PHZ</sub>	$z R_L = 1 k\Omega$		14		20		24	
Gt to Q <sub>A</sub> thru Q <sub>H</sub> ('595 only)		tPLZ	C <sub>L</sub> =50pF		14		20		24	ns
Propagation of to QA ('596 only	thru Q <sub>H</sub>	t <sub>PLH</sub>	C <sub>L</sub> =50pl C <sub>L</sub> =150	L=50pF L=150pF			20 25			ns
Propagation G↓ to Q <sub>A</sub> ('596 only	thru Q <sub>H</sub>	t <sub>PHL</sub>	C <sub>L</sub> =50pl C <sub>L</sub> =150		14 17		20 25			ns
Pulse	SRCK or RCK	t <sub>w</sub>			10	15		20		
Width	SRCLR Low				10	15.		20		ns
Setup	SRCLRt to SRCKt				6	10		12		
Time	SER to SRCK†	t <sub>su</sub>			10	15		20		ns
	SRCK† to RCK††				15	20		25		
Hold Time,		th			-3	0		0		ns
Input Cap	acitance	CiN			. 5		r			pF
Output Ca	pacitance	Cout	Output D	isabled	10					pF
Power Dis Capacitan		C <sub>PD</sub>								рF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} \ V_{CC}^2 \ f + I_{CC} \ V_{CC}$ .

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

The RCK1 to CCK1 setup time ensures that the counter will see stable data from the register output.

#### **FEATURES**

- 8-Bit Parallel Storage Register Inputs
- shift Register has Direct Overiding Load and Clear.
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
   I<sub>OL</sub> = 8 mA @ V<sub>OL</sub> = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
   (2022)

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

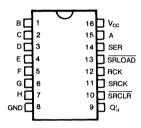
#### DESCRIPTION

The '597 consists of an 8-bit storage latch feeding a parallel-in, serial-out 8-bit shift register. Both the storage register and the shift register have positive-edge triggered clocks. The shift register also has direct load (from storage) and clear inputs.

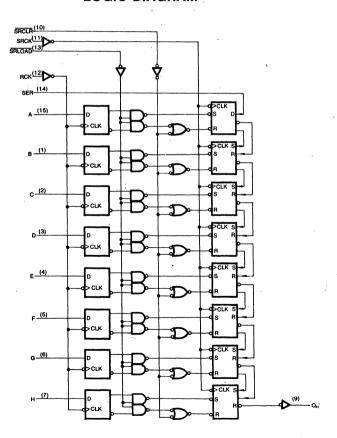
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### PIN CONFIGURATION



#### LOGIC DIAGRAM



#### **FUNCTION TABLE**

		INPUTS			FUNCTION
SER	SRCK	SRCLR	SRLOAD	RCK	FONCTION
Х	Х	L	Н	X	S.R. is cleared to "L"
Х	X	Н	J	х	Input register data is stored into S.R.
L		н	Н	х	First stage of S.R. becomes "L". Other stages store the data of previous stage, respectively.
Н		Н	Н	x	First stage of S.R. becomes "H". Other stages stores the data of previous stage, respectively.
Х	х	X	Х		State of S.R. is not changed.
х	х	Х	Х	- 5	Input data on A∼H line is stored into input register
Χ.	X	X	Х	ī	Storage register state is not changed.

## **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_I < -0.5V \text{ or } V_I > V_{CC} +0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V)$ ±20 mA
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . Max 500 ns

\* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

#### DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	Ta	= 25°C	KS74AHCT T <sub>a</sub> = -40°C to +85°C	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
			its				
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	v
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	V
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=4$ mA $I_O=8$ mA	О	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	ΔΙσς	per input pin V <sub>1</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0µA		2.7	2.9	3.0	mA

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## AC ELECTRICAL CHARACTERISTICS (Input t<sub>r</sub>, t<sub>i</sub>≤2 ns), AHCT597

Characteristic		Symbol	Conditions <sup>†</sup>	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	$T_a = -40^{\circ}$	AHCT C to +85°C 0V±10%	KS54 T <sub>a</sub> = -55°C V <sub>CC</sub> = 5.0	to +125°C	Unit
,				Тур	Min	Max	Min	Max	,
Maximum Clock Frequency		f <sub>max</sub>		50	30		25		MHz
Propagation	Delay,	t <sub>PLH</sub>		9	·	15		18	
SRCK1 to Q'H		t <sub>PHL</sub>		9		15	,	18	ns
Propagation	Delay,	t <sub>PLH</sub>	$C_L = 50pF$	14		20		24	
SRLOAD↓ to	Q' <sub>H</sub>	t <sub>PHL</sub>		14	14	20		24	ns
Propagation Delay, SRCLR↓ to Q' <sub>H</sub>		t <sub>PHL</sub>		11		18		21	ns
Propagation Delay, RCK1 to Q'H		t <sub>PLH</sub>	C <sub>L</sub> =50pF	15		25		29	Ī
		t <sub>PHL</sub>	SLOAD=Low	15		25		29	ns
Pulse	RCK or SRCK High or Low		•	10	15			20	
Width	SRCLR or SRLOAD Low	t <sub>w</sub>	,	10	15		20		ns
	SRCLR1 before SRCK1			6	10 .		12		
Setup Time	RCK† before SRCK†††	t <sub>su</sub>		15	20		25		ns
	SER before SRCK1			10	15		20		
	A thru H before RCK1			10	15		20	J	
Hold Time		th		-3	0		0		ns
Input Capaci	tance	CIN		5					рF
Power Dissip	ation Capacitance*	C <sub>PD</sub>	•						pF

<sup>\*</sup> CPD determines the no-load dynamic power dissipation: PD=CPD VCC2 f + ICC VCC.

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

<sup>††</sup> The RCK† to CCK† setup time ensures that the counter will see stable data from the register output.

#### **FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current (I<sub>OL</sub> = 24 mA @ V<sub>OL</sub> = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
   KS74AHCT: -40°C to +85°C
   KS54AHCT: -55°C to +125°C
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### **DESCRIPTION**

These high-speed octal/bus transceivers are designed for asynchronous two-way communication between data buses. A direction control input (DIR) controls the flow direction of data. When DIR is high, data flows from the A inputs to the B outputs. When DIR is low, data flows from B to A. The '643 transfers inverted data from the A bus to the B bus and non-inverted data from the B bus to the A bus. The '640 transfers inverted data in both directions.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

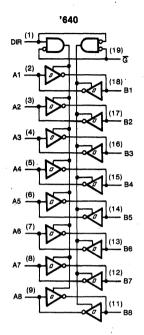
#### PIN CONFIGURATION

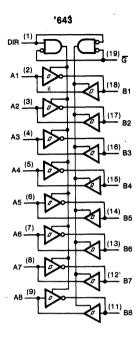
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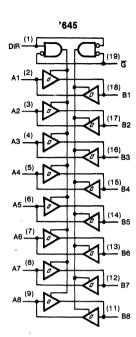
#### **FUNCTION TABLE**

1	ntrol puts	Operation					
Ğ	DIR	'640	'643	'645			
L	L	Inverted data transmitted from Bus B to Bus A	Data transmitted from Bus B to Bus A	Data transmitted from Bus B to Bus A			
L	Н	Inverted data transmitted from Bus A to Bus B	Inverted data transmitted from Bus A to Bus B	Data transmitted from Bus A to Bus B			
Н	x	Buses isolated (High-impedance state)	Buses isolated (High-impedance state)	Buses isolated (High-impedance state)			

## LOGIC DIAGRAMS







# **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_{I} < -0.5V \text{ or } V_{I} > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + 2.5V$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long-exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Supply Voltage, Vo	oc	4.5V to 5.5V
DC Input & Output	: Voltages*, V <sub>IN</sub> , V	OUT OV to Vcc
Operating Tempera	ature	
Range	KS74AHCT:	-40°C to +85°C
	KS54AHCT: -	55°C to +125°C

Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . Max 500 ns

\* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T <sub>a</sub> = 25°C		KS74AHCT T <sub>a</sub> = -40°C to +85°C	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
			Тур	,	Guaranteed Lim	its	
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-6m A$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> =0.1	v
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	lin	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	ΔΙοσ	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

# AC ELECTRICAL CHARACTERISTICS (Input tr, tr≤2 ns), AHCT640, AHCT643

Characteristic	Symbol	Conditions†		T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V			to +125°C	Unit	
				Тур	Min	Max	Min	Max	
,	tpLH	C <sub>L</sub> =50pF	=	7		12		14	
Propagation Delay, A to B, or B to A	UPLH .	C <sub>L</sub> =150	oF	10		17		20	ns
		C <sub>L</sub> =50pF 7		12		14			
	tpHL	CL=150	οF	10		17		20	
		R <sub>L</sub> =1kΩ	C <sub>L</sub> =50pF	12		20		25	
Output Enable Time,	tpzH		C <sub>L</sub> =150pF	15		25		31	ns
G to A or B			C <sub>L</sub> =50pF	12		20		25	
	tpzL		$C_L = 150pF$	15		25		31	
Output Disable Time,	t <sub>PHZ</sub>	R <sub>L</sub> =1kΩ		13		18		22	ns
G to A or B	tpLZ	C <sub>L</sub> =50pF	•	13		18		22	115
Input Capacitance	CIN			5					pF
Output Capacitance	Cout	Output D	Output Disabled						рF
Power Dissipation	C <sub>PD</sub> *	G=V <sub>CC</sub>							рF
Capacitance*	CPD	G=GND	(per stage)	30					PF.

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} \ V_{CC}^2 \ f \ + \ I_{CC} \ V_{CC}$ .

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

# AC ELECTRICAL CHARACTERISTICS (Input t<sub>r</sub>, t<sub>f</sub>≤2 ns), AHCT645

Characteristic	Symbol	,		T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	a = - 40°C; to +85°C;     = -55°C; to +125°C		to +125°C	Unit	
				Тур	Min	Max	Min	Max	
Propagation Delay,	t <sub>PLH</sub>		C <sub>L</sub> =50pF C <sub>L</sub> =150pF C <sub>L</sub> =50pF C <sub>L</sub> =150pF			10 19		14 25	ns
A to B, or B to A	t <sub>PHL</sub>					10 19	,	14 25	
Output Enable Time	tрźн	R <sub>L</sub> =1kΩ	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	12 18	,	20 29		25 36	ns
G to A or B	tpzŁ		C <sub>L</sub> =50pF C <sub>L</sub> =150pF	12 18		20 29	,	25 36	
Output Disable Time,	t <sub>PHZ</sub>	$R_L = 1 k\Omega$		13		18		22	ns
G to A or B	tpLZ	C <sub>L</sub> =50pF	=	13		18		22	115
Input Capacitance	CIN			5					pF
Output Capacitance	Соит	Output Di	Output Disabled						pF
Power Dissipation Capacitance*	C <sub>PD</sub> *	Ğ=V <sub>CC</sub> Ğ=GND	(per stage)	5 30		14			pF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

#### **FEATURES**

- · 8 bi-directional data paths
- · Transmits direct or stored data in either direction
- 24-pin slim DIP package
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current
- $(I_{OL} = 24 \text{ mA } @ V_{OL} = 0.5 \text{V})$  for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
   KS74AHCT: -40°C to + 85°C

KS54HACT: -55°C to + 125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATION

CAB	1	24	□v∞
SAB	2	23	СВА
DIR 🗆	3	22	SBA
A1	4	21	ΒĜ
A2	5	20	<b>B</b> 1
A3 🗆	6	19	B2 □
A4	7	18	<b>□</b> B3
A5 🗆	8	17	B4 □
A6 🗆	9	16	B5
A7 🗆	10	15	<b>□</b> B6
A8 🗖	11	14	В7
GND	12	13	<b>□</b> B8

#### DESCRIPTION

The '646 and '648 are bi-directional bus transceivers with D-type flip-flops and control circuitry to facilitate high speed multiplexed data transmission. The '646 transmits true data and the '648 transmits inverted data.

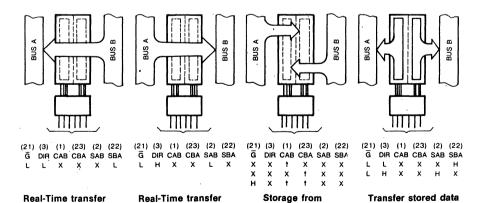
Data can be transmitted directly from one port to the other in either direction. It also can be stored in the flip-flops from either or both ports for subsequent transmission to the opposite port. Six control inputs govern the data flow:

- G (output enable) when high, all outputs are disabled, isolating the A and B ports. When low, one port is enabled at a time as determined by the DIR pin.
- DIR (direction control) disables A or B outputs permitting the pins to be used as inputs thus determining the direction of a data flow. When DIR=high, data flows from A to B
- SAB,SBA (data source AB and BA) determines whether data transmitted is from the data inputs or the registers associated with those inputs.
- CAB,CBA (Clock AB and BA) clocks data from the A inputs and the B inputs, respectively, into their associated registers. Since the clocks are not gated with the G and DIR pins, data at the A and B pins can be clocked into the flip-flops at any time.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

to A AND/OR B



A AND/OR B

bus A to bus B

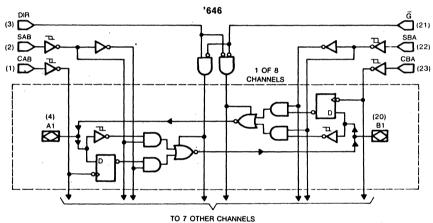
bus B to bus A

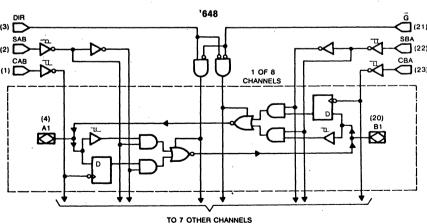
## **FUNCTION TABLE**

Inputs						Data I/O*		Operation or Function			
Ğ	DIR	CAB	CBA	SAB	SBA	A1 thru A8	B1 thru B8	'646	'648		
X X		† X	X ↑	X X	X .	input Not specified	input¹ Not specified	Store A, B unspecified Store B, A unspecified	Store A, B unspecified Store B, A unspecified		
H	X	↑ H or L	↑ HorL	X	X	Input	Input	Store A and B data Isolation, hold storage	Store A and B data isolation, hold storage		
L	L L	X	X H or L	X	L H	Output	Input	Real-Time B data to A bus Stored B data to A bus	Real-Time B data to A bus Stored B data to A bus		
L	Н	X H or L	X X	L H	X	Input	Output	Real-Time A data to B bus Stored A data to B bus	Real-Time Ā data to B bus Stored Ā data to B bus		

<sup>\*</sup>The data output functions may be enabled or disabled by various signals at the  $\overline{G}$  and DIR inputs. Data input functions are always enabled, ie., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

## **LOGIC DIAGRAMS**







## **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 70 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, $T_{stg} \dots -65$ °C to $+150$ °C
Power Dissipation Per Package, $P_d{}^\dagger$ 500 mW
* Absolute Maximum Ratings are those values beyond

which permanent damage to the device may occur.

These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

## **Recommended Operating Conditions**

Supply Voltage, V	'cc	4.5V to 5.5V
DC Input & Output	it Voltages*, V <sub>IN</sub> ,	$V_{\text{OUT}}$ OV to $V_{\text{CO}}$
Operating Temper	ature	
Range	KS74AHCT:	-40°C to +85°C

KS54AHCT: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T <sub>a</sub> = 25°C		KS74AHCT T <sub>a</sub> = -40°C to +85°C	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit		
			Тур		Guaranteed Limits				
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	v		
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧		
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-6m A$	V <sub>CC</sub> 4.2	V <sub>CC</sub> −0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	v		
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v		
Maximum Input Current	lin	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ		
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μΑ		
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ		
Additional Worst Case Supply Current		per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA		

<sup>†</sup> Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# AC ELECTRICAL CHARACTERISTICS (Input tr, tr≤2 ns), AHCT646, AHCT648

Characteristic	Symbol	Con	ditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		AHCT C to +85°C OV±10%	KS54 T <sub>a</sub> = -55°C V <sub>CC</sub> = 5.0	Unit		
				Тур	Min	Max	Min	Max		
Maximum Frequency	f <sub>max</sub>	C <sub>L</sub> =50pF	:	45		30		25	MHz	
Propagation Delay,	tpLH	C <sub>L</sub> =50pf C <sub>L</sub> =150p		11 14		18 23		22 28	ns	
A or B Input to B or A Output	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150p		11 14		18 23		22 28		
Propagation Delay,	tpLH	C <sub>L</sub> =50pf C <sub>L</sub> =150p		15 18		25 30		30 36	ns	
CBA or CAB Input to A or B Output	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150r		15 18		25 30		30 36	ns	
Propagation Delay,†† SBA or SAB Input to	t <sub>PLH</sub>	C <sub>L</sub> =50pf C <sub>L</sub> =150p		16 19	ı	27 33		32 38		
A or B Output (with A or High)	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF		16 19		27 33		32 38	ns	
Propagation Delay,†† SBA or SAB Input to	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF		15 18		25 30		30 36		
A or B Output (with A or Low)	t <sub>PHL</sub>		C <sub>L</sub> =50pF C <sub>l</sub> =150pF			25 30		30 36	ns	
Out Enable Time,	t <sub>PZH</sub>	$R_i = 1k\Omega$	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	14 17		22 27		26 32		
G or DIR Input to A or B Output		HL- IKW	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	14 17		22 27		26 32	ns	
Output Disable Time,	t <sub>PHZ</sub>	$R_L = 1 k\Omega$		13		22		26		
G or DIR Input to A or B Output	t <sub>PLZ</sub>	C <sub>L</sub> =50pF	÷ ·	13		22		26	ns	
Pulse Duration, Clocks High or low	t <sub>w</sub>			8	12		15		ns	
Set up Time, A before CABt or B before CBAt	t <sub>su</sub>				12		15		ns	
Hold Time, A after CAB† or B after CBA†	t <sub>h</sub>		,		0		0		ns	
Input Capacitance	Cin								pF	
Output Capacitance	Cout	Output Di	sabled	10					pF	
Power Dissipation Capacitance*	C <sub>PD</sub>	,	1				-	,	pF	

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.



<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

<sup>††</sup> These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

# KS54AHCT 651/652 KS74AHCT

# Octal 3-State Bus Transceivers with Registers

Preliminary Specifications

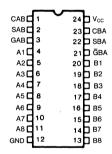
#### **FEATURES**

- Independent Registers and Enables for A and B Buses
- Multiplexed Real-Time and Stored-Data
- . Choice of Time and Inverting Data Paths
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current (I<sub>OL</sub> = 24 mA @ V<sub>OL</sub> = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATION



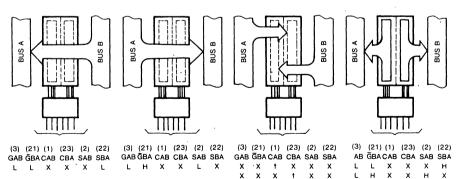
#### DESCRIPTION

These devices consist of bus transceiver circuits. D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Enable GAB and GBA are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether real-time or stored data is transferred. A low input level selects real-time data, and a high selects stored data. The following examples demonstrate the four fundamental busmanagement functions that can be performed with the octal bus transceivers and registers.

Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and GBA. In this configuration each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{\text{CC}}$  and ground.



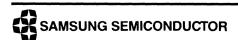
Real-Time transfer bus B to bus A

Real-Time transfer bus A to bus B

Storage from A AND/OR B

н х

Transfer stored data

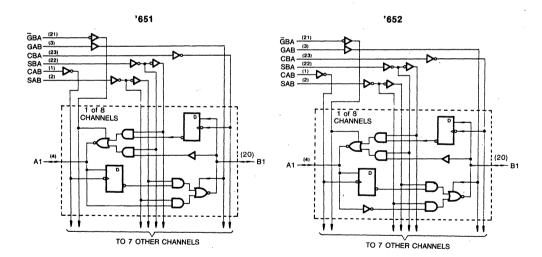


## **FUNCTION TABLE**

,		INP	UTS			DATA	1/0*	OPERATION OR FUNCTION				
GAB	ĞΒΑ	CAB	СВА	SAB	SBA	A1 THRU A8	B1 THRU B8	'651	'652			
. L L	H	H or L ↑	.H or L	×	X	Input	Input	Isolation Store A and B Data	Isolation Store A and B Data			
X	Н	† †	H or L	X X**	X X	Input Input	Not specified Output*	Store A, Hold B Store A in both registers	Store A Hold B Store A in both registers			
L	X L	H or L	. ↑ . ↑	X	X X**	Not specified Output*	Input Input	Hold A, Store B Store B in both registers	Hold A, Store B Store B in both registers			
L	L L	X X	X H or L	X	L	Output	Input	Real-Time B Data to A Bus Stored B Data to A Bus	Real-Time B Data to a Bus Stored B Data to A Bus			
Н	H	X H or L	. X	L H	X	Input	Output	Real-Time A Data to B Bus Stored A Data to Bus	Real-Time A Data to B Bus Stored A Data to B Bus			
Н	L	H or L	. H or L	Н	н	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus	Stored A Data to B Bus and Stored B Data to A Bus			

<sup>\*</sup> The data output functions may be enabled or disabled by various signals at the GAB and GBA inputs. Data input functions are always enabled, ie., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

## **LOGIC DIAGRAMS**



<sup>\*\*</sup> Select control=L: clocks can occur simultaneously
Select control=H: clocks must be staggered in order to load both registers

## **Absolute Maximum Ratings\***

•
Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + 0.5V$
Continuous Current Through
Vcc or GND pins ±250 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . . . . . . . . 4.5V to 5.5V DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . OV to  $V_{CC}$  Operating Temperature

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . Max 500 ns

 Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

#### DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	Ta	=25°C	KS74AHCT $T_a = -40$ °C to +85°C	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-6mA$	V <sub>CC</sub> 4.2	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	o <sup>-</sup>	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	l <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μА
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin .V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

## AC ELECTRICAL CHARACTERISTICS (Input tr, tres 2 ns), AHCT651, AHCT652

Characteristic	Symbol	Con	ditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	Ta = -40°	AHCT C to +85°C 0V±10%	T. = -55°C	AHCT to +125°C V± 10%	Unit
•				Тур	Min	Max	. Min	Max	
Clock Frequency	f <sub>max</sub>	C <sub>L</sub> =50pl	F	45	30		25		MHz
Propagation Delay, A or B Input to	t <sub>PLH</sub>	C <sub>L</sub> =50pl C <sub>L</sub> =150		11 14	,	18 . 23		22 28	
B or A Ouput	t <sub>PHL</sub>	C <sub>L</sub> =50pl		11 14		18 23		22 28	ns
Propagation Delay,	tpLH	C <sub>L</sub> =50pl C <sub>L</sub> =150	F	15 18		25 30		30 36	
CBA or CAB Input to A or B Output	t <sub>PHL</sub>	C <sub>L</sub> =50pl C <sub>L</sub> =150		15 18		25 30		30 36	ns
Propagation Delay, SBA or SAB Input to	t <sub>PLH</sub>	C <sub>L</sub> =50pl C <sub>L</sub> =150		16 19		27 32	,	32 38	
A or B Output (with A or B High)	t <sub>PHL</sub>	C <sub>L</sub> =50pl C <sub>L</sub> =150		16 19		27 32		32 38	ns
Propagation Delay, SBA or SAB Input to	t <sub>PLH</sub>	C <sub>L</sub> =50pl C <sub>L</sub> =150		15 18		25 30		30 36	
A or B Output (with A or B Low)	t <sub>PHL</sub>	C <sub>L</sub> =50pl		15 18		25 30		30 36	ns
Output Enable Time, GBA to A or	tpZL		C <sub>L</sub> =50pF C <sub>L</sub> =150pF	19 22		32 37		38 44	
GAB to B	tpzH	R <sub>L</sub> =1kΩ	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	19 22		32 37		38 44	ns
Output Disable Time,	t <sub>PHZ</sub>	R <sub>L</sub> =1kΩ		13		22		26	
GBA to A or GAB to B	tPLZ	C <sub>L</sub> =50pl	F	13		22		26	ns
Pulse Width Clocks High or Low	tw			8	12		15		ns
Setup Time, A before CAB† or B before CBA†	t <sub>su</sub>			8	12		15	,	ns
Hold Time, A after CAB† or B after CBA†	t <sub>h</sub>			-3	0		0		ns
Maximum Input Capacitance	CIN		,	5					рF
maximum Output Capacitance	Cout	Output D	isabled	10					pF
Power Dissipation Capacitance*	C <sub>PD</sub>								pF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .



<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

# KS54AHCT 658/659 KS74AHCT

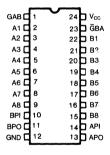
Octal Bus Transceivers with Parity

**Preliminary Specifications** 

## **FEATURES**

- Bus Transceivers with Inverting Outputs ('658) or True Outputs ('659)
- . Generates a Parity Bit for A Bus and B Bus
- Easily Cascadable
- Internal Active Pull-Ups and Pull-Downs
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current
- (I<sub>OL</sub> = 24 mA @ V<sub>OL</sub> = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
   KS74AHCT: -40°C to +85°C
   KS54AHCT: -55°C to +125°C
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATION



#### DESCRIPTION

These octal bus transceivers are designed for asynchronous, bidirectional communication between data buses. The devices transmit data from the A Bus to the B Bus, or from the B Bus to the A Bus, depending on the levels at the direction control inputs, GAB and  $\overline{G}BA$ . These devices also generate parity outputs. APO and BPO, which reflect the number of high levels at the A Bus and B Bus, respectively, taking into account the parity inputs API and BPI.

The bidirectional I/O ports feature active circuits on the input stage that, when the output shared by that pin is disabled, will maintain the input in the last state taken by the output. This state will be maintained until changed by activity on the bus. The advantage of this arrangement is that when all outputs on the bus are disabled, the inputs will be prevented from floating, resulting in minimum power dissipation and minimum susceptibility to noise. This eliminates any need for external pull-up or pull-down resistors. The parity inputs API and BPI have similar circuits.

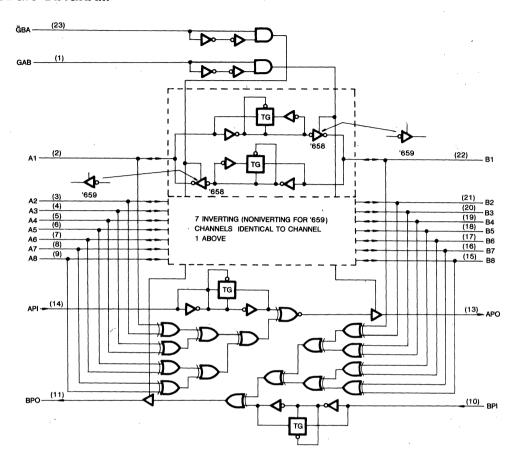
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### **FUNCTION TABLE**

	TROL UTS	NUMBER OF HIGH INPUTS ON	NUMBER OF HIGH INPUTS ON	OUTPUTS		OPERATION		
ĞВА	GAB	A BUS AND API	B BUS AND BPI	APO	вро	'658	'659	
L	L	X	0, 2, 4, 6, 8	Z	Н	B Data to A Bus	B Data to A Bus	
	_	X	1, 3, 5, 7, 9	Z	L	b Data to A Bus	b Data to A Bus	
Н	н	0, 2, 4, 6, 8	x	Н	Z	à Data to B Bus	A Data to B Bus	
''	11	1., 3, 5, 7, 9	Х	L	Z	A Data to B Bus	A Data to B bus	
Н	L	х	Х	Z	Z	Isolation	Isolation	
		Х	0, 2, 4, 6, 8		Н			
	н	X	1, 3, 5, 7, 9		L	B Data to A Bus,	B Data to A Bus,	
-	"	0, 2, 4, 6, 8	х	Н		Ā Data to B Bus	A Data to B Bus	
		1, 3, 5, 7, 9	X	L				

#### **LOGIC DIAGRAM**



# **Absolute Maximum Ratings\***

Supply Voltage Range $V_{CC}$ , $-0.5V$ to $+7V$
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V)$ ±20 mA
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 70 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, P <sub>d</sub> † 500 mW
* Absolute Maximum Patings are those values havend

Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

KS54AHCT: -55°C to +125°C

Input Rise & Fall Times,  $t_r, \, t_f \, \ldots \, \ldots \, Max \, 500 \, ns$ 

 Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

# KS54AHCT **658/659** KS74AHCT

# DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

						· ·	
Characteristic	Symbol	Test Conditions	T,	= 25°C	KS74AHCT T <sub>a</sub> = -40°C to +85°C	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Uni
			Тур		Guaranteed Lim		1 1
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	v
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-6mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_0=20\mu A$ $I_0=12mA$ $I_0=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	ΔΙσο	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

# AC ELECTRICAL CHARACTERISTICS (Input tr., tr <2 ns), AHCT658, AHCT659

Characteristic	Symbol	1 1		T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	Ta = -40°	IAHCT C to +85°C 0V±10%	KS54/ T <sub>a</sub> = -55°C V <sub>CC</sub> = 5.0°	to +125°C	Unit
				Тур	Min	Max	Min	Max	
Propagation Delay,	tpLH	C <sub>L</sub> =50p C <sub>L</sub> =150		11 14		. 18 23		22 28	ns -
A or B to B or A	t <sub>PHL</sub>	C <sub>L</sub> =50p C <sub>L</sub> =150		11 14		18 23		22 28	115 -
Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pl C <sub>L</sub> =150	F	16 19		27 32		32 38	ns -
A or B to APO or BPO	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF		16 19		27 32		32 38	- IIS -
Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pl C <sub>L</sub> =150		11 14		18 23		22 28	ns-
API or BPI to APO or BPO	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF		11 14		18 23		22 28	113
Enable Time, GAB or	t <sub>PZH</sub>	$R_L = 1 k\Omega$	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	16 19		27 32		32 38	ns
GBA to APO or BPO	t <sub>PZL</sub>	UL— IKW	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	16 19		27 32		32 38	113
Disable Time, GAB or	t <sub>PLZ</sub>	$R_L = 1 k\Omega$		16		27		32	ns
GBA to APO or BPO	t <sub>PHZ</sub>	C <sub>L</sub> =50pl	=	16		27		32	
Input Capacitance	CIN			5					рF
Output Capacitance	Соит						,		рF
Power Dissipation Capacitance*	C <sub>PD</sub>								pF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.



## Preliminary Specifications

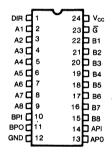
#### **FEATURES**

- Bus Transceivers with Inverting Outputs ('664) or True Outputs ('665)
- . Generates a Parity Bit for A Bus and B Bus
- Easily Cascadable
- Internal Active Pull-Ups and Pull-Downs
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current
   (loL = 24 mA @ VoL = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges: KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

### PIN CONFIGURATION



## DESCRIPTION

These octal bus transceivers are designed for asynchronous, bidirectional communication between data buses. The devices transmit data from the A Bus to the B Bus or from the B Bus to the A Bus, depending on the level at the direction control input, DIR. The enable input,  $\overline{G}$ , can be used to disable the device so that the buses are isolated. These devices will also generate parity outputs, APO and BPO, which reflect the number of high levels at the A Bus and B Bus, respectively, taking into account the parity inputs API and BPI.

The bidirectional I/O ports feature active circuitry on the input stage that, when the output shared by that pin is disabled, will maintain the input in the last state taken by the output. This state will be maintained until changed by the activity on the bus. The advantage of this arrangement is tht when all outputs on the bus are disabled, the inputs will be prevented from floating, resulting in minimum power dissipation and minimum susceptibility to noise. This eliminates any need for external pull-up or pull-down resistors. The parity inputs API and BPI have similar circuitry.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

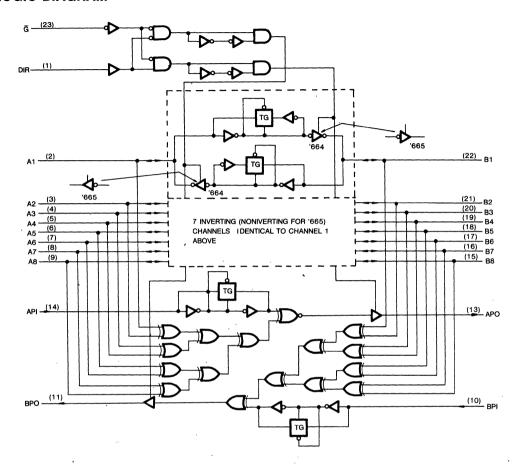
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### **FUNCTION TABLE**

1	NTROL PUTS	NUMBER OF HIGH INPUTS ON	NUMBER OF HIGH INPUTS ON	OUT	PUTS	OPERATION		
Ğ	DIR	A BUS AND API	B BUS AND BPI	APO	вро	'664	'665	
		x	0, 2, 4, 6, 8	Z H	B Data to A Bus	B Data to A Bus		
-		x	1, 3, 5, 7, 9	Z	L	b bala to A bus	B Bata to A Bas	B Bala to A Bao
	н	0, 2, 4, 6, 8	X	Н	Z	Ā Data to B Bus	A Data to B Bus	
-		1, 3, 5, 7, 9	. ×	L	Z	A Data to B Bus	A Data to B Bus	
Н	Х	X	X	ż	Z	Isolation	Isolation	



## LOGIC DIAGRAM



# **Absolute Maximum Ratings\***

Supply Voltage Range $V_{CC}$ , $-0.5V$ to $+7V$
DC Input Diode Current, IIK
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 70 \text{ m/s}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW

<sup>\*</sup> Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Supply Voltage, Vcc . . . . . . . . 4.5V to 5.5V DC Input & Output Voltages\*, V<sub>IN</sub>, V<sub>OUT</sub> . . OV to Vcc Operating Temperature

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

Input Rise & Fall Times,  $t_r,\,t_f$  . . . . . . . . Max 500 ns

 Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

# Octal Bus Transceivers with Parity

# DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	Ta	= 25°C	KS74AHCT T <sub>a</sub> = -40°C to +85°C	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
,			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	Vон	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-6mA$	V <sub>CC</sub> 4.2	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> = 0.1	v
Maximum Low-Level Output Voltage	VoL	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> =20μA I <sub>O</sub> =12mA I <sub>O</sub> =24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

## AC ELECTRICAL CHARACTERISTICS (Input tr, tr≤2 ns), AHCT664, AHCT665

Characteristic	Symbol	Conditions†		T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	T. = -40°0	AHCT C to +85°C DV±10%	KS54AHCT  T <sub>a</sub> = -55°C to +125°C  V <sub>CC</sub> = 5.0V ± 10%		Unit
				Тур	Min	Max	Min	Max	
Propagation Delay,	tpLH	C <sub>L</sub> =50pl C <sub>L</sub> =150		11 14		18 23		22 28	ns
A or B to B or A	t <sub>PHL</sub>	C <sub>L</sub> =50pl C <sub>L</sub> =150		11 14		18 23		22 28	ns
Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pl C <sub>L</sub> =150		16 19		27 32		32 38	ns
A or B to APO or BPO	t <sub>PHL</sub>	C <sub>L</sub> =50pl C <sub>L</sub> =150		16 19		27 32		32 38	ns
Propagation Delay,	t <sub>PLH</sub>		C <sub>L</sub> =50pF C <sub>L</sub> =150pF			18 23		22 28	ns
API or BPI to APO or BPO	t <sub>PHL</sub>		C <sub>L</sub> =50pF C <sub>L</sub> =150pF			18 23	∌.	22 28	ns
Output Enable Time,	t <sub>PZH</sub>	Rı = 1kΩ	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	16 19		27 32		32 38	ns
Ğ to A or B	tpzL	UF-1 K7	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	16 19		27 32		32 38	ns
Output Disable Time,	tpHZ	$R_L=1k\Omega$		16		27		32	ns
G to A or B	tpLZ	C <sub>L</sub> =50pl	=	16		27		32	ns
Output Enable Time,	t <sub>PZH</sub>	R <sub>L</sub> =1kΩ	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	16 19		27 32		32 38	ns
DIR to A or B	tpzL	HL-174	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	16 19		27 32		32 38	ns
Output Disable Time,	tpHZ	$R_L=1k\Omega$		16		27		32	ns
DIR to A or B	tpLZ	C <sub>L</sub> =50pl	=	16		27		32	ns
Input Capacitance	CIN			5					рF
Output Capacitance	Соит	Output D	isabled						pF
Power Dissipation Capacitance*	C <sub>PD</sub>								pF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

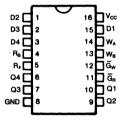
#### **FEATURES**

- Seperate Read Write
   Addressing Permits Simultaneous Reading and
   Writing
- Expandable to 512 Words of 7-bits
- For use as:
  - Scratch pad memory
  - Buffer Storage between processors
  - Bit storage in fast multiplication designs
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with drive current
   (loL = 24 mA @ VoL = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage∉range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

### PIN CONFIGURATION



#### **FUNCTION TABLES**

#### WRITE MODE SELECT TABLE

OPERATING	INPL	JTS	INTERNAL	
MODE	Ğw	Dn	LATCHES(a)	
Write Data	L	L H	L H	
Data Latched	н	х	no change	

#### NOTE:

a. The Write Address (W<sub>A</sub> and  $\overline{W}_B$ ) to the "Internal latches" must be stable while  $\overline{G}_W$  is LOW for conventional operation.

#### DESCRIPTION

The '670 is a 16-bit 3-State Register File organized as 4 words of 4 bits each. Separate Read and Write Address and enable inputs are available, permitting simultaneous writing into one word location and reading from another location. The 4-bit word to be stored is presented to four Data inputs. The Write Address inputs ( $W_A$  and  $W_B$ ) determine the location of the stored word. When the Write Enable ( $\overline{G}_W$ ) input is LOW, the data is entered into the addressed location. The addressed location remains transparent to the data while the  $\overline{G}_W$  is LOW. Data supplied at the inputs will be read out in true (non-inverting) form from the 3-State outputs. Data and Write Address inputs are inhibited when  $\overline{G}_W$  is HIGH.

Direct acquisition of data stored in any of the four registers is made possible by individual Read Address inputs (R<sub>A</sub> and R<sub>B</sub>). The addressed word appears at the four outputs when the Read Enable ( $\overline{G}_R$ ) is LOW. Data outputs are in the HIGH impedance "off" state when the read enable input is HIGH. This permits outputs to be tied together to increase the word capacity to very large numbers.

Up to 128 devices can be stacked to increase the word size to 512 locations by tying the 3-State outputs together. Since the limiting factor for expansion is the output HIGH current, further stacking is possible by tying pull-up resistors to the outputs to increase the l<sub>OH</sub> current available. Design of the read enable signals for the stacked devices must ensure that there is no overlap in the LOW levels which would cause more than one output to be active at the same time. Parallel expansion to generate n-bit words is accomplished by driving the enable and address inputs of each device in parallel.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

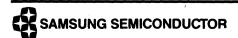
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### **READ MODE SELECT TABLE**

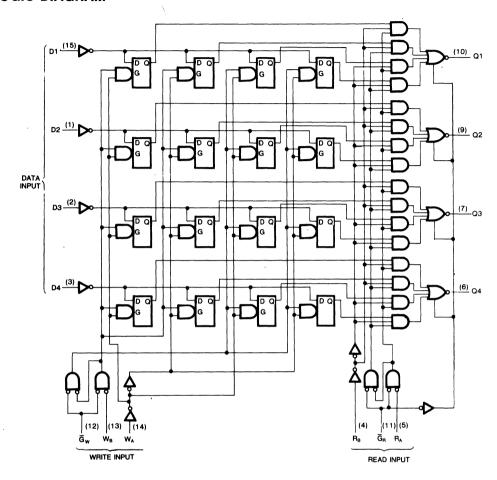
ODEDATING	1	NPUTS	OUTDUT
OPERATING MODE	GR INTERNAL LATCHES(b)		OUTPUT Q <sub>n</sub>
Read	L L	L H	L H
Disabled	Н	. н	(Z)

#### NOTE:

b. The selection of the "internal latches" by Read Address  $(\overline{R}_A$  and  $R_B)$  are not constrained by  $\overline{G}_W$  or  $\overline{G}_R$  operation.



## **LOGIC DIAGRAM**



# **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_{I} < -0.5V \text{ or } V_{I} > V_{CC} +0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 70 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Patings are those values havend

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

KS54AHCT: -40°C to +85°C
KS54AHCT: -55°C to +125°C
Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . Max 500 ns

 Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)



# DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T <sub>a</sub> = 25°C		KS74AHCT T <sub>a</sub> = -40°C to +85°C	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Uni
			Тур		Guaranteed Lim	its	1
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	v
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-6mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 " 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	IIN	V <sub>IN</sub> =V <sub>CC</sub> or GND	,	±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔΙσς	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

# AC ELECTRICAL CHARACTERISTICS (Input tr, tr <2 ns), AHCT670

Characteristic	Symbol	Conditions <sup>†</sup>		T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	KS74AHCT T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%		KS54AHCT  T <sub>a</sub> = -55°C to +125°C  V <sub>CC</sub> = 5.0V ± 10%		Unit
	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Min	Max						
Maximum Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =150pF C <sub>L</sub> =50pF					,	28 34	ns
R <sub>A</sub> or R <sub>B</sub> to Output	t <sub>PHL</sub>			1		1		28 34	113
Propagation Delay,				-				30 36	ns
Gw to Output	t <sub>PHL</sub>							30 36	
Propagation Delay.	t <sub>PLH</sub>	C <sub>L</sub> =150pF C <sub>L</sub> =50pF						28 34	- ns
Data to Output	t <sub>PHL</sub>							28 34	
Output Enable Time	tpzH	$R_i = 1 k\Omega$	0 -450-5	1				25 31	ns
G <sub>R</sub> to Output	tpzL		C <sub>L</sub> =50pF	1				25 31	
Output Disable Time	tpHZ	$R_L = 1k\Omega$		17		28		34	ns
GR to Output	tpLZ	C <sub>L</sub> =150	pF	17		- 28		39	
Input Capacitance	CiN								рF
Output Capacitance	Cout	Output D	isabled	10					рF
Power Dissipation Capacitance*	C <sub>PD</sub>				* *				pF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} \ V_{CC}^2 \ f + I_{CC} \ V_{CC}$ . † For AC switching test circuits and timing waveforms see section 2.



## Preliminary Specifications

#### **FEATURES**

- '679: 12-bit to 4-bit comparator with enable
- '680: 12-bit to 4-bit comparator with latch
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
- $(I_{OL} = 24 \text{ mA} @ V_{OL} = 0.5 \text{V})$  for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### DESCRIPTION

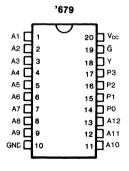
The '679 and '680 address comparators simplify addressing of memory boards and/or other peripheral devices. The four P inputs are normally hard wired with a preprogrammed address. An internal decoder determines what input information applied to the 12 A inputs must be low or high to cause a low state at the output (Y). For example, a positive-logic bit combination of 0111 (decimal 7) at the P input determines that inputs A1 through A7 must be low and that inputs A8 through A12 must be high to cause the output to go low. Equality of the address applied at the A inputs to the preprogrammed address is indicated by the output being low.

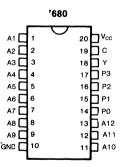
The '679 features an enable inpu  $(\overline{G})$ . When  $\overline{G}$  is low, the device is enabled. When  $\overline{G}$  is high, the device is disabled and the output is high regardless of the A and P inputs. The '680 features a transparent latch and a latch enable input (C). When C is high, the device is in the transparent mode. When C is low, the previous logical state of Y is latched.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### PIN CONFIGURATIONS

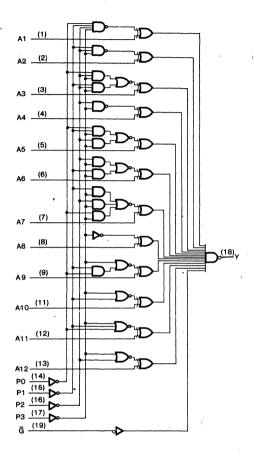


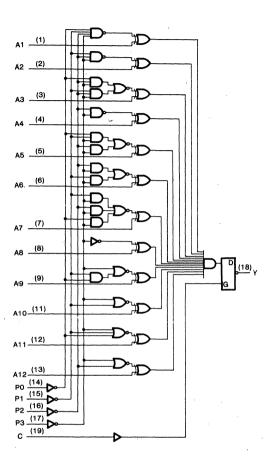


## **LOGIC DIAGRAMS**

'679

'680





## **FUNCTION TABLE**

'679	'680					INI	PUTS	CON	MON	I TO	'679	AND	'680					OUTPUT
Ğ	С	Р3	P2	P1	PO	A1 .	A2	А3	<b>A</b> 4	<b>A</b> 5	A6	<b>A</b> 7	A8	A9	A10	A11	A12	Y
L	Н	L	L	L	L	Н	Н	Н	Н	Н	Н	H.	Н	Н	Н	Н	Н	L
L	Н	L	L	L	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L
L	Н	L	L	Н	L	L	L	Н	Н	Н	Н	Н	Н	Н	` Н	Н	Н	L
L	Н	L	L	Н	Н	L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	L
L	Н	L	Н	L	L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н	н	L
L	Н	L	H,	L	Н	L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н	L
L	Н	L	Н	Н	L	L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н	L
L	Н	L	Н	Н	Н	L	L	L	L	L	L	L	Н	Н	Н	Н	ŀН	L
F,	Н	Н	L	L	L	L	L	L	L	L	L	L	L	Н	Н	Н	Н	L
L	Н	Н	L	L	Н	L	L	L	L	L	L	L	L	L	Н	Н	Н	L
L	Н	Н	L	Н	L	L	L	L	L	L	L	L	L	L	L	Н	Н	L
L	Н	Н	L	Н	Н	L	L	L	L	L	L	L	L	L	L	L	Н	· L
L	Н	Н	Н	L	L	L	L	L	L	L	L	L	Ł	Н	Н	Н	L	L*
L	Н	Н	Н	L	Н	L	L	L	L	L	L	L	L	L	Н	Н	L	L*
L	Н	Н	Н	Н	L	L	L	L	L	L	L	L	L	L	L	Н	L	L*
L	Н	Н	Н	Н	Н	L	L	L	L	L	L	L	L	L	L	L	L	L
L	Н							All o	ther o	combi	inatio	ns						Н
Н								'679	: Any	com	binati	on						Н
	L							'680	: Any	com	binati	on						Latched

<sup>\*</sup> These three rows of the function table show combinations that would normally not be used in address comparator applications. The logic symbols above are not valid for all combinations in which P=12, 13 and 14. If symbols valid for all combinations are required, starting with the fourth Exclusive-OR from the bottom, change P≥9 to P=9 ... 11/13... 15, P≥10 to P=10/11/14/15, and P≥11 to P=11/15.

# **Absolute Maximum Ratings\***

Supply Voltage Hange $V_{CC}$ ,0.5V to +/V
DC Input Diode Current, I <sub>IK</sub>
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 70 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW

<sup>\*</sup> Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

	•	_	
Supply Voltage, V <sub>CC</sub>			
DC Input & Output V	oltages*, V <sub>IN</sub> ,	Vout	. OV to Vcc
Operating Temperatu			
Range	KS74AHCT:	-40°	C to +85°C
	KS54AHCT:	-55°C	to +125°C
Input Rise & Fall Time	es, t <sub>r</sub> , t <sub>f</sub>		Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

# DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	= 25°C	KS74AHCT T <sub>a</sub> = -40°C to +85°C	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-6mA$	V <sub>CC</sub> 4.2	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> -0.1 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	l <sub>IN</sub> .	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μА
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	, ±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3,0	mA

# AC ELECTRICAL CHARACTERISTICS (Input t<sub>r</sub>, t<sub>i</sub>≤2 ns), AHCT679

Characteristic	Symbol	Conditions <sup>†</sup>	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	Ta = -40°	AHCT C to +85°C 0V±10%	KS54AHCT  T <sub>a</sub> = -55°C to +125°C  V <sub>CC</sub> =5.0V± 10%		Unit
			Тур	Min	Max	Min	Max	1 1
Propagation Delay, Any P to Y	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	18 21		30 35		36 42	ns
	tpHL	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	18 27		30 35		36 42	
Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	16 19		26 31		31 37	ns
Any A to Y	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	16 19		26 31		31 37	7 113
Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	12 15		19 24		23 29	ns
G to Y	gation belay,		23 29	113				
Input Capacitance	CIN		- 5					pF
Power Dissipation Capacitance*	C <sub>PD</sub>							рF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC²</sub> f + I<sub>CC</sub> V<sub>CC</sub>.



<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

#### 4

# AC ELECTRICAL CHARACTERISTICS (Input tr, tr <2 ns), AHCT680

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	Ta = -40°0	AHCT C to +85°C DV ± 10%	KS54AHCT  T <sub>a</sub> = -55°C to +125°C  V <sub>CC</sub> = 5.0V ± 10%		Unit
			Тур	Min	Max	Min	Max	
Propagation Delay, Any P to Y	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	21 24		35 40		42 48	ns
	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	21 24		35 40		42 48	113
Propagation Delay,	tpLH	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	18 21		30 35		36 42	ns
Any A to Y	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	18 21		30 35		36 <b>42</b>	113
Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	13 16		21 26		25 31	ns
C to Y	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	13 16		21 26		25 31	,13
Input Capacitance	CIN		5					pF
Power Dissipation Capacitance*	C <sub>PD</sub>							pF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC^2} f + I_{CC} V_{CC}$ .

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

#### **FEATURES**

- Compares Two 8-Bit Words
- '682 has  $20k\Omega$  pullup Resistors on the Q Inputs
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
  - ( $I_{OL}$  = 24 mA @  $V_{OL}$  = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL. NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- · Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

## DESCRIPTION

These magnitude comparators perform comparisons of two eight-bit binary or BCD words. All types provide  $\overline{P} = \overline{Q}$  and P>Q outputs. The '682 features 20-kΩ pullup termination resistors on the Q inputs for analog or switch data.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V<sub>CC</sub> and ground.

## PIN CONFIGURATIONS

Q3 🗌

P>Q [ 20 Vcc PO C P=Q 19 Q0 [ 18 **Q**7 \_\_\_ P7 Q6 **□** P6 Q5 **□** P5

Q4 12

'682 and '684

#### '686 ē>ā d 24 V<sub>CC</sub> 23 G2 Ĝ1 🗖 P0 d 3 22 P=Q 21 07 ᅃᆸ 20 P7 Q1 [ 19 NC NC [ 18 🗖 Q6 P2 **d** 17 🗖 P6 16 🗖 Q5 Q2 РЗ □ 10 15 P5

NC-No internal connection

14 Q4

13 **□** P4

Q3 [

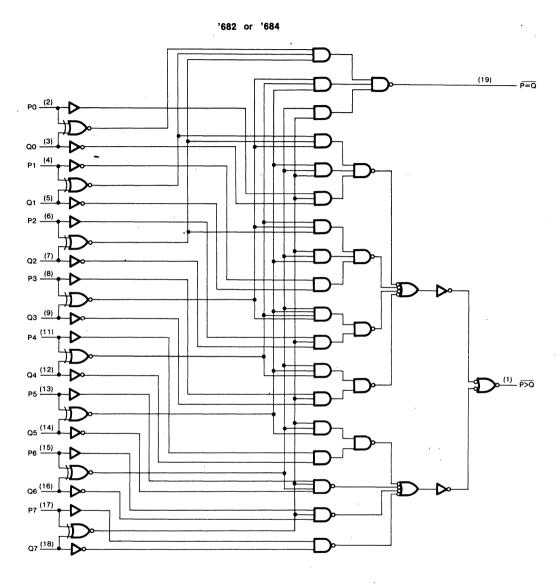
GND [

## **FUNCTION TABLE**

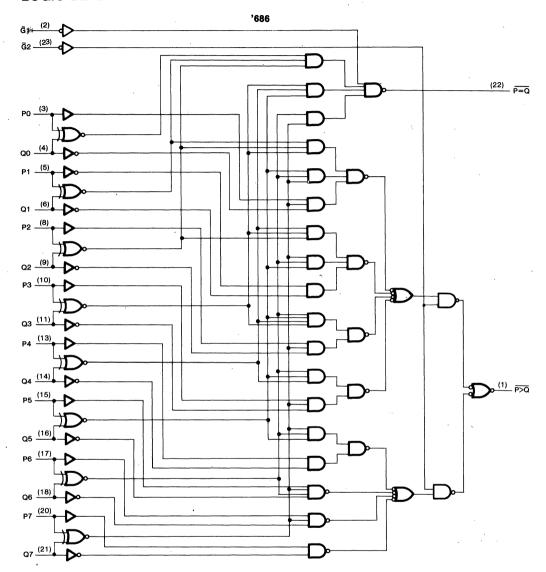
II	NPUTS		OUTF	PITS		
DATA	ENA	G1         G2           L         X           X         L           X         X           H         X           X         H		0017013		
P, Q	Ğ1	Ğ2	P=Q	P>Q		
P=Q	L	X	L	Н		
P>Q	Х	L	Н	L		
P <q< td=""><td>Х</td><td>Χ</td><td>Н</td><td>Н</td></q<>	Х	Χ	Н	Н		
P=Q	Н	Χ	Н	Н		
P>Q	X	Н	Н	Н		
Х	Н	Н	Н	Н		

- NOTES: 1. The last 3 lines of the function table apply only to the device having enable inputs, i.e., '686.
  - 2. The P<Q function can be generated by applying the  $\overline{P}=\overline{Q}$  and  $\overline{P}>\overline{Q}$  outputs to a 2-input NAND gate.

## LOGIC DIAGRAMS



## LOGIC DIAGRAMS (continued)



# **Absolute Maximum Ratings\***

Supply Voltage Range $V_{CC}$ , $-0.5V$ to $+7V$
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IoK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-
posure to these conditions may affect device reliability.

<sup>†</sup> Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

	-	_	
Supply Voltage, V <sub>CC</sub>		4.5	5V to 5.5V
DC Input & Output V	/oltages*, V <sub>IN</sub> ,	Vout	OV to V <sub>CC</sub>
Operating Temperatu	ıre		
Range	KS74AHCT:	-40°C	to +85°C
	KS54AHCT:	-55°C to	+125°C
Input Rise & Fall Tim	ee t. t.	M	lay 500 ne

 <sup>\*</sup> Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Parameter	Symbol	Test Conditions	Т	a = 25°C	KS74AHCT T <sub>a</sub> = -40°C to +85°C	54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Limit		
Minimum High-Level Input Voltage	VIH			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	0.8	v
Minimum High-Level Output Voltage (Totem-pole Outputs)	V <sub>ОН</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-6m A$	V <sub>CC</sub> 4.2	V <sub>CC</sub> -0.1 3.93	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3:7	v
Maximum Low-Level Output Voltage (All Outputs)	V <sub>Q</sub> L	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current, ('682 Q Inputs)		V <sub>CC</sub> =Max V <sub>IN</sub> =2.7V V <sub>IN</sub> =0.4V		-0.2 -0.4	-0.2 -0.4	-0.2 -0.4	mA
Maximum Input Current (All other Inputs)	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent	lcc	For '682: V <sub>IN</sub> =GND (Q0-Q7) V <sub>IN</sub> =V <sub>CC</sub> or GND (all other inputs)		3.5	. 3.5	3.5	mA
Supply Current		For '684 and '688 V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0µA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin  V <sub>I</sub> =2.4V  other Inputs: at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0µA		2.7	2.9	3.0	mA



## AC ELECTRICAL CHARACTERISTICS (Input tr, tres 2 ns), AHCT682, AHCT684, AHCT686

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	Ta = -40°	AHCT C to +85°C 0V±10%	Ta = -55°C	AHCT to +125°C V ± 10%	Unit
			Тур	Min	Max	Min	Max	
Maximum Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	13 16		22 27		27 33	ns
P or Q to P=Q	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	13 16		22 27		27 33	113
Propagation Delay,	tpLH	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	16 19		27 32		32 38	ns
P or Q to P>Q	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	16 19		27 32		32 38	113
Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	10 13		16 21		19 25	ns
G1 to P=Q ('686 Only)	tpHL	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	10 13	4	16 21		19 25	113
Propagation Delay,	t <sub>PLH</sub>	C=50pF C <sub>L</sub> =150pF	11 14		19 24		23 29	ns
G2 to P <q ('686="" only)<="" td=""><td>t<sub>PHL</sub></td><td>C<sub>L</sub>=50pF C<sub>L</sub>=150pF</td><td>11 14</td><td></td><td>19 24</td><td></td><td>23 29</td><td>113</td></q>	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	11 14		19 24		23 29	113
Input Capacitance	CIN		5					рF
Power Dissipation Capacitance*	C <sub>PD</sub>							рF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

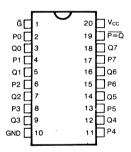
#### **FEATURES**

- Compares Two 8-Bit Words
- Choice of Totem-pole ('688) and open-drain ('689) outputs ('688 is identical to '521)
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- · High output drive
- ( $I_{OL} = 24 \text{ mA} @ V_{OL} = 0.5V$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

## PIN CONFIGURATION



## **FUNCTION TABLE**

IN	PUTS	ОИТРИТ		
DATA P, Q	P=Q			
P=Q	L ·	L		
P>Q	L .	Н		
P <q< td=""><td>L</td><td>Н</td></q<>	L	Н		
Х	Н	Н		

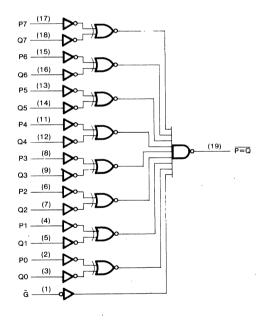
#### DESCRIPTION

These identity comparators perform comparisons of two 8-bit binary or BCD words. The outputs of the '688 are totempole, while '688's are open-drain.

These devices provide speeus and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### LOGIC DIAGRAM



## **Absolute Maximum Ratings\***

Supply Voltage Range $V_{CC}$ , $-0.5V$ to $+7V$
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 70 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, $T_{stg} \dots -65$ °C to $+150$ °C
Power Dissipation Per Package, $P_{d}{}^{\dagger}$ 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Supply Voltage, V <sub>CC</sub>	4.5V to 5.5V
DC Input & Output Voltages*, VIN, VOUT	OV to Vcc
Operating Temperature	

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	= 25°C	KS74AHCT T <sub>a</sub> = -40°C to +85°C	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	1
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v
Minimum High-Level Output Voltage ('688 only)	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-6mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	V
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=12mA$ $I_{O}=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	٧
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Output Leakage Current ('689 only)	loz	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lçc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0µA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin  V <sub>I</sub> =2.4V  other Inputs: at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0µA		2.7	2.9	3.0	mA

# AC ELECTRICAL CHARACTERISTICS (Input tr, tr≤2 ns), AHCT688

Characteristic	Symbol	ymbol Conditions†	$\begin{array}{ccc} T_a = 25^{\circ}C \\ V_{CC} = 5.0V \end{array}$		KS74AHCT T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%		KS54AHCT T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> =5.0V ± 10%	
			Тур	Min	Max	Min	Max	
Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	12 15		19 24		23 29	ns
	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	12 15		19 24		23 29	113
Propagation Delay,	tpLH	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	12 15		19 24		23 29	ns
Q to P=Q	tpHL	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	12 15		19 28		23 29	113
Propagation Delay.	tpLH	C <sub>1</sub> =50pF	11 14		17 22	,	20 26	ns
G to P=Q	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	11 14		17 22		20 26	113
Input Capacitance	CIN		5					pF
Power Dissipation Capacitance*	C <sub>PD</sub>							pF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

# AC ELECTRICAL CHARACTERISTICS (Input tr, tr < 2 ns), AHCT689

Characteristic	Symbol	Conditions†	$T_a = 25^{\circ}C$ Inditions $V_{CC} = 5.0V$		KS74AHCT T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%		KS54AHCT T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> =5.0V± 10%	
			Тур	Min	Max	Min	Max	
Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	19 22		28 33		33 <b>39</b>	ns
P to P=Q	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	14 17		23 <b>28</b>	,	28 <b>34</b>	113
Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	19 22		28 33		33 <b>39</b>	ns
Q to P=Q	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	14 17		<b>23</b> 28		28 <b>34</b>	
Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	16 19	-	23 <b>28</b>		27 33	ns
G to P=Q	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	11 16		18 23		22 <b>28</b>	,,,,
Input Capacitance	CIN		5					рF
Power Dissipation Capacitance*	C <sub>PD</sub>							рF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

## Preliminary Specifications

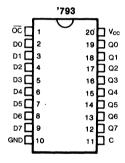
#### **FEATURES**

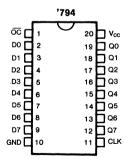
- I/O port configuration enables output data back onto input bus
- · Latch ('793) and and Register ('794) options
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with drive current
  - (IoL = 24 mA @ VoL = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATIONS





## **DESCRIPTION**

These are 8-bit latches/registers that allow temporary storage and retrievel of data on a bus. This operation is important in control algorithms which make decisions based on the previous status of output controls. Rather than storing a redundant copy of the output data in memory, simply reading the register as an I/O port allows the data to be retrieved from where it has been stored in a '793 or '794, for verification and/or updating.

The Data is loaded in the registers on the positive-edge of the clock (CLK) for the '794. The data is passed through the '793 when C is high, and it is latched when C goes low. The output control ( $\overline{OC}$ ) is used to erable data on the D0-D7 pins. when  $\overline{OC}$  is low the output of the latches/registers is enabled on D0-D7, enabling D as an output bus so that the host can perform a read operation. When  $\overline{OC}$  is high, D0-D7 are inputs to the latches/registors configuring D as an input bus.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### **FUNCTION TABLES**

'793

С	ŌĊ	Q	D
L	L	Q <sub>0</sub> ** Q <sub>0</sub> ** D*	Output, Q
L	Н	Q <sub>0</sub> **	Input
H†	L	D*	Output, Q*
Н	• н	D	Input

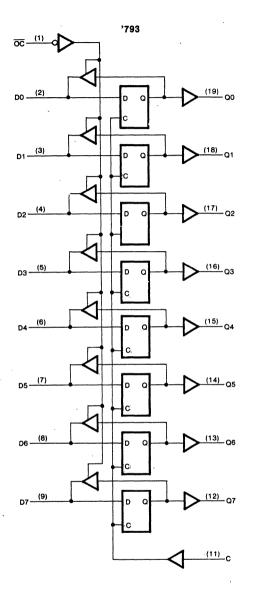
- \* In this case the output of the latch feeds the input, and a "race" condition results.
- \*\* Q<sub>0</sub> represents the previous "latched" state.
- † This transition is not a normal mode of operation and may produce hazards.

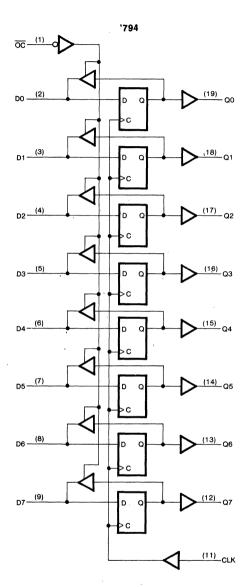
'794

CLK	ŌĊ	Q	D
L or H or ↓	L	Qo	Output, Q
LorHor↓	н	Qo	Input
1	L	Qo	Output, Q*
<b>†</b>	Н	D	Input

 In this case the output of the register is clocked to the inputs and the overall Q output is unchanged at Qo.

## LOGIC DIAGRAMS





# **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 70 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Patings are those values become

<sup>\*</sup> Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Supply Voltage, V<sub>CC</sub> . . . . . . 4.5V to 5.5V DC Input & Output Voltages\*, V<sub>IN</sub>, V<sub>OUT</sub> . . OV to V<sub>CC</sub> Operating Temperature

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . Max 500.ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol Test Conditions		Ta	= 25°C	KS74AHCT T <sub>a</sub> = -40°C to +85°C	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit		
			Тур	p Guaranteed Limits					
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	٧		
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	V		
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-6m A$	V <sub>CC</sub>	V <sub>CC</sub> -0.1	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> = 0.1 3.7	v		
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v		
Maximum Input Current	liN	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μА		
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μΑ		
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ		
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA		



# AC ELECTRICAL CHARACTERISTICS (!::put tr, tr≤2 ns), AHCT793, AHCT794

Characteristic		Symbol	Con			Conditions† \		$T_a = -40^{\circ}$	AHCT C to +85°C OV ± 10%	KS54/ T <sub>a</sub> = - 55°C V <sub>CC</sub> = 5.0	to +125°C	Unit
					Тур	Min	Max	Min	Max			
Maximum ( ('794 only)	Operating Frequency	t <sub>max</sub>	C <sub>L</sub> =50pl	=	60	40		35		MHz		
Propagation	n Delage		C <sub>L</sub> =50pl C <sub>L</sub> =150pl		10 13		16 21		19 25	ns		
Propagation Delage D to Any Q ('793 only)		*	C <sub>L</sub> =50pl C <sub>L</sub> =150pl		10 13		16 21		19 25	IIS		
Propagation Delage CLK/C to Any Q			C <sub>L</sub> =50pl C <sub>L</sub> =150pl		12 15		20 25		24 30			
		t-	C <sub>L</sub> =50pF C <sub>L</sub> =150pF		12 15		20 25		24 30	ns		
Enable Time.		tрzн	R <sub>L</sub> =1kΩ (C=Low	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	11 14		18 23		22 28	ns		
OC to D	`	t <sub>PZL</sub>	for '793)	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	11 13		18 23		22 28	1115		
Disable Tim	ie ,		$R_L = 1 K\Omega$		11		18		22			
OC to D			C <sub>L</sub> =50pF (C=Low for '793)		11		18		22	ns		
Pulse Widtl CLK/C High	•	tw			9	14		19		ns		
Setup time	D before C↓ ('793)	t <sub>su</sub>			6	10		12		ns		
octup time	D before CLKt('794)				10	15		20	1	113		
Hold Time	D after C↓ ('793)	th			9	10		12		ns		
D after CLK† ('794)		un l		-3	0		0					
Input Capci	tance	CiN			5		.,			pF		
Output Cap	acitance	Соит	OC=GND	)	10					рF		
Power Diss	ipation Capacitance*	CPD								ns		

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

 $<sup>^{\</sup>dagger}$  For AC switching test circuits and timing waveforms see section 2.

#### **FEATURES**

- Functionally Equivalent to AMD's Am29821 and Am29822
- Provides Extra Data Width Necessary for Wider Address/Data Paths or Buses with Parity
- Power-Up-High-Impedance State
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current (loL = 24 mA @ VoL = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
   KS74AHCT: -40°C to +85°C

KS54AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATIONS

		'821			
οc (	1	<u>,                                    </u>	24	Ь	Vcc
1D (	<b>1</b> 2		23	b	1Q
2D (	<b>1</b> 3		22	þ	2Q
3D (	<b>1</b> ⁴		21	þ	3Q
4D (	<b></b>		20	Þ	4Q
5D (	<b>1</b> 6		19	Þ	5Q
6D (	<b>1</b> 7		18	Ь	6Q
7D [	<b>∃</b> 8		17	Þ	7Q
8D [	<b>4</b> 9		16	Ь	8Q
9D [	10		15	Ь	9Q
10D (	<b> </b>  11		14	þ	10Q
GND [	12		13	þ	CLK

V <sub>cc</sub> 1Q 2Q
-
20
عد
3Q
4Q
5Q
6Q
7Q
BQ
9Q
OQ
CLK

#### DESCRIPTION

These 10-bit bus-interface flip-flops feature three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. They are suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

All of the flip-flops are edge-triggered and D-type. On the positive transition of the clock the Q outputs on the '821 will be true, and on the '822 will be complementary to the data input.

A buffered output-control input can be used to place the ten outputs in either a normal logic state (high or low levels) or a high-impedance state. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output control  $(\overline{OC})$  does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

## **FUNCTION TABLES**

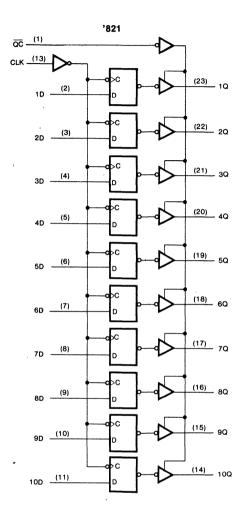
(Each Flip-Flop) '821

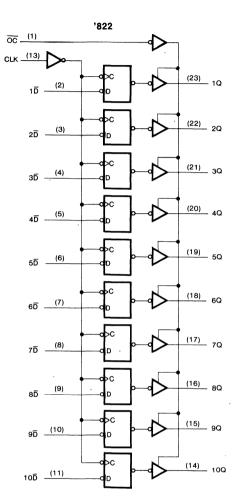
	Inputs	Output		
oc	OC CLK D			
L	<b>†</b>	Н	Н	
L	<b>↑</b>	L	L	
L	L	Х	$Q_0$	
L	Н	X	$Q_0$	
Н	Х	Х	Z	

'822

	Inputs	Output	
ŌĊ	CLK	Q	
L	†	Н	L
L	<b>†</b>	L	Н
L	L	Х	Q <sub>0</sub> Q <sub>0</sub>
L	н	Х	Qo
H	X	Χ	Z

## LOGIC DIAGRAMS





# 10-Bit Bus Interface Flip-Flops with 3-State Outputs

## **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_{I} < -0.5V \text{ or } V_{I} > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_0 < -0.5V)$ or $V_0 > V_{CC} + 0.5V) \dots \pm 20$ mA
Continuous Output Current Per Pin, Io
$(-0.5V < V_0 < V_{CC} + 0.5V) \dots \pm 70 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.
These are stress ratings only and functional operation of the device at or beyond them is not implied. Long ex-
posure to these conditions may affect device reliability.

<sup>†</sup> Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Supply Voltage, \	/cc	4.	5V to 5.5V
DC Input & Outpu	ıt Voltages*, V <sub>IN</sub> ,	Vout	OV to Vcc
Operating Temper	rature		
Range	KS74AHCT:	-40°C	to +85°C

KS54AHCT: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

# DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	Ta	=25°C	KS74AHCT T <sub>a</sub> = -40°C to +85°C	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	<
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	<
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-6mA$	V <sub>CC</sub> 4.2	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> -0.1	٧
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1	٧
Maximum Input Current	I <sub>IN</sub> .	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μА
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μА
Maximum Quiescent Supply Current	Icc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

# AC ELECTRICAL CHARACTERISTICS (Input tr., tr<2 ns), AHCT821, AHCT822

Characteristic	Symbol	Conditions†		T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	T. = - 40°C to 485°C		KS54AHCT  T <sub>a</sub> = -55°C to +125°C  V <sub>CC</sub> = 5.0V ± 10%		Unit
				Тур	Min Max		Min Max		
Maximum Operating Frequency	fmax	C <sub>L</sub> =50p	F	50	35		30		MHz
Propagation Delay		C <sub>L</sub> =50p C <sub>L</sub> =150		8 11		14 19		17 23	ns
CLK to any Q		C <sub>L</sub> =50p C <sub>L</sub> =150		8 11		14 19		17 23	113
Output Enable Time, OC to any Q	tpzL	B. = 1k0	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	11 14		18 23		22 28	ns
	tpzL	-n 1 KW	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	111		18 23		22 28	113
Output Disable Time,	tpHZ	R <sub>L</sub> =1kΩ C <sub>L</sub> =50pF		13		18		22	ns
OC to any Q	tpLZ			13		18		22	
Pulse Width, CLK High or Low	t <sub>w</sub>			9	15		18		ns
Setup Time, Data before CLK†	t <sub>su</sub>			9	14		17	7.	ns
Hold Time, Data after CLK†	th			-3	0		0		ns
Input Capacitance	Cin			5					pF
Output Capacitance	Cour	Output D	isabled	10					pF
Power Dissipation Capacitance* (per stage)	C <sub>PD</sub>	ŌC=V <sub>CC</sub> ŌC=GN		5 30					pF pF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

## Preliminary Specifications

#### **FEATURES**

- Functionally Equivalent to AMD's Am29823 and Am29824
- Provides Extra Data Width Necessary for Wider Address/Data Paths or Buses with Parity
- Power-Up-High-Impedance State
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current
- (I<sub>OL</sub> = 24 mA @  $V_{OL}$  = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
   KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

## PIN CONFIGURATIONS

'823

<u>∞</u> c	1	24	vcc
100	2	23	1Q
2D 🗖	3	22	<b>1</b> 2Q
3D□	4	21	<b>3</b> Q
4D	5	20	<b>1</b> 4Q
, 5D <b>□</b>	6	19	<b>□</b> 5Q
6D	7	18	<b>□</b> 6Q
7D <b>C</b>	8	17	<b>7</b> 0
8D.C	9	16	<b>□</b> 8Q
9D 🗖	10	15	<b>□</b> 9Q
CLR C	11	14	CLKEN
GND	12	13	CLK

'824

$\overline{c}d$	1	24	b v <sub>cc</sub>
1DQ	2	23	<b>1</b> 10
2D	3	22	<b>1</b> 2Q
3DC	4	21	<b>3</b> 0
4Đ	5	20	<b>1</b> 4Q
5DC	6	19	<b>⊃</b> 5Q
6D 🗖	7	18	6Q
7 <b>5</b>	8	17	7Q
85 C	9	16	<b>□</b> 8Q
9 <u>D</u> 🗖	10	15	]9Q
CLR	11	14	CLKEN
GND 🗖	12 -	13	CLK

#### DESCRIPTION

These 9-bit bus interface flip-flops feature three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. They are suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers, parity bus interfacing and working registers.

With the clock enable ( $\overline{\text{CLKEN}}$ ) low, the D-type edge-triggered flip-flops enter data on the low-to-high transitions of the clock. Taking  $\overline{\text{CLKEN}}$  high will disable the clock buffer, thus latching the outputs. The '823 has noninverting D inputs and the '824 has inverting  $\overline{\text{D}}$  inputs. Taking the  $\overline{\text{CLR}}$  input low causes the nine Q outputs to go low independently of the clock.

A buffered output-control input ( $\overline{OC}$ ) can be used to place the ten outputs in either a normal logic state (high or low levels) or a high-impedance state. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output control does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground

#### FUNCTION TABLES

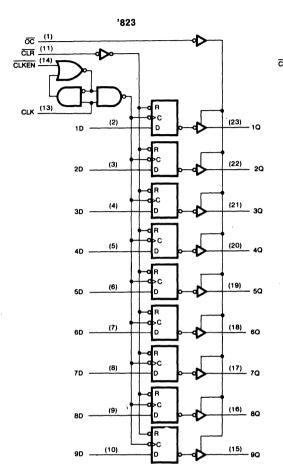
'823

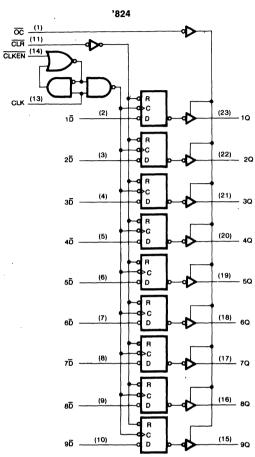
		INPUT			OUTPUT
ŌĊ	CLR	CLKEN	CLK	D	Q
L	L	X	X	Х	L
L	Н	L	<b>↑</b>	Н	н
L	. <b>н</b>	L	1	L	L
L	Н	Н	X	Χ	$\mathbf{Q}_0$
Н	Х	Х	Х	Х	Z

'824

	INPUTS					
ŌĊ	CLR	CLKEN	CLK	D	Q	
L	L	X	X	Х	L	
L	Н	L	<b>↑</b>	Н	н	
L	Н	L	1	L	L	
L	Н	Н	Χ	Х	$Q_0$	
Н	Х	Χ.	X	Χ	Z	

## **LOGIC DIAGRAMS**





## **Absolute Maximum Ratings\***

Supply Voltage Range $V_{CC}$ , $-0.5V$ to $+7V$
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 70 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Ratings are those values beyond

which permanent damage to the device may occur.

These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

# **Recommended Operating Conditions**

Supply Voltage, V <sub>CC</sub>	4.5V to 5.5V
DC Input & Output Voltages*, VIN, VOUT	OV to $V_{CC}$
Operating Temperature	

Range KS74AHCT: -40°C to +85°C
KS54AHCT: -55°C to +125°C
Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T <sub>a</sub> = 25°C		KS74AHCT $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit			
			Тур		Guaranteed Limits					
Minimum High-Level Input Voltage	V <sub>IH</sub>	·		2.0	2.0	2.0	٧			
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	V			
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-6mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> -0.1 3.84	V <sub>CC</sub> −0.1 3.7	v			
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=12mA$ $I_{O}=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v			
Maximum Input Current	l <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ			
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μΑ			
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ			
Additional Worst Case Supply Current	Δία	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA			



<sup>†</sup> Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# AC ELECTRICAL CHARACTERISTICS (Input t, t, <2 ns), AHCT823, AHCT824

Characteristic		Symbol	Conditions <sup>†</sup>		T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	KS74AHCT T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%		KS54AHCT T <sub>e</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%		Unit	
					Тур	Min	Max	Min	Max		
Maximum Op	erating Frequency	f <sub>max</sub>	C <sub>L</sub> =50pl	C <sub>L</sub> =50pF		35		30		MHz	
Propagation Delay CLK to any Q		t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF		8 11		14 19		17 23	ns	
		t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF		8 11		14 19		17 23	lis	
	Propagation Delay, CLR to Any Q		C <sub>L</sub> =50pF C <sub>L</sub> =150pF		10 13		17 22		21 27	ns	
Output Enable Time, OC to any Q		t <sub>PZH</sub>	$R_L = 1 k\Omega$	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	11 14		18 23		22 28	ns	
		t <sub>PZL</sub>		$C_L=50pF$ $C_L=150pF$	11 14		18 23		22 28		
Output Disable Time, OC to any Q		t <sub>PHZ</sub>	$R_L = 1k\Omega$ $C_L = 50pF$		13		18		22	ns	
		tpLZ			13		18		22		
Pulse Width	CLR low	tw			9	15		18		ns	
ruise Width	CLK high or low				9	15		18			
Setup Time before CLKf	CLR inactive	t <sub>su</sub>		•	9	14		17			
	Data				9	14		17		ns	
	CLKEN high or low				9	14		17			
Hold Time, CLKEN or data after CLK†		t <sub>h</sub>			-3	0		. 0		ns	
Input Capacitance		Cin			5					pF	
Output Capacitance		Cour	Output Disabled		10					pF	
Power Dissipation Capacitance* (per stage)		C <sub>PD</sub>	OC=V <sub>CC</sub> OC=GNI		5 30					pF pF	

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

Preliminary Specifications

#### **FEATURES**

- Functionally Equivalent to AMD's Am29825 and Am29826
- Improved I<sub>OH</sub> Specifications
- Multiple Output Enables Allow Multiuser Control of the Interface
- Power-Up High-Impedance State
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current (I<sub>OL</sub> = 24 mA @ V<sub>OL</sub> = 0.5V) for direct bus interface
- 'naputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges: KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATIONS

'825

<u>oc</u> ₁ ⊏	1	24	Vcc
ŌC2 □	2	23	ОCЗ
1D 🗆	3	22	1Q
2D 🗆	4	21	2Q
3D 🗆	5	20	3Q
4D 🗆	6	19	4Q
5D 🗖	7	18	5Q
6D 🗖	8	17	6Q
7D 🗖	9	16	7Q
8D 🗖	10	15	8Q
CLR	11	14	CLKEN
GND 🗆	12	13	CLK

'826

_			
<u>∞</u> ₁₫	1	24	] V <sub>cc</sub>
ŌC2 ☐	2	23	ОСЗ
10 C	3	22	1Q
	4	21	<b>2</b> Q
зБ 🗖		20	<b>]</b> 3Q
40 C		19	<b>]</b> 4Q
5D 🗖	7	18	<b>]</b> 5Q
6 <u>D</u> 🗖	8	17	] 6Q
7Ď 🗖	9	16	<b>]</b> 7Q
8D 🗖	10	15	] 8Q
CLR	11	14	CLKEN
GND [	12	13	CLK

#### DESCRIPTION

These 8-bit flip-flops feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are suitable for implementing multi-user buffer registers, I/O ports, bus drivers and working registers.

With the clock enable (CLKEN) low, all D-type edge-triggered flip-flops enter data on the low-to-high transition of the clock. Taking CLKEN high will disable the clock buffer, thus latching the outputs. The '825 has non-inverting D inputs and the '826 has inverting D inputs. Taking the CLR inputs low causes the eight Q outputs to go low independently of the clock.

Multiuser buffered output-control inputs ( $\overline{OC}$ 1,  $\overline{OC}$ 2, and  $\overline{OC}$ 3) can be used to place the eight outputs in either a normal logic state (high or low level) or a high-impedance state. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output controls do not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### **FUNCTION TABLES**

'825

	Inputs								
OC*	CLR	CLKEN	CLK	D	Output Q				
L	L	Х	X	X	L				
L	Н	L	<b>↑</b>	Н	Н				
L	Н	L	<b>↑</b>	L	L				
L	Н	Н	Χ	X	Qo				
Н	Х	Χ	Х	X	Z				

<sup>\*</sup>  $\overline{OC}$  = H if any of  $\overline{OC}1$ ,  $\overline{OC}2$ , or  $\overline{OC}3$  are high.  $\overline{OC}$  = L if all of  $\overline{OC}1$ ,  $\overline{OC}2$ , and  $\overline{OC}3$  are low.

'826

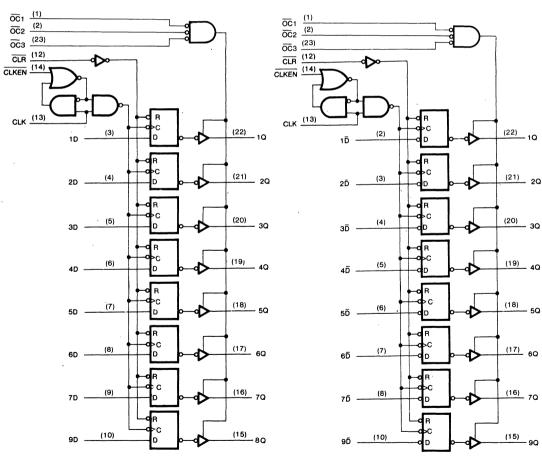
	Inputs								
ŌĊ*	CLR	CLKEN	CLK	D	Q				
L	L	Х	Х	Х	L				
L	Н	L	<b>↑</b>	Н	L				
L	Н	L	<b>↑</b>	L	Н				
L	Н	Н	Χ	X	$Q_0$				
н	. X	Χ	Χ	X	Z				

 $\overrightarrow{OC}$  = H if any of  $\overrightarrow{OC}1$ ,  $\overrightarrow{OC}2$ , or  $\overrightarrow{OC}3$  are high.  $\overrightarrow{OC}$  = L if all of  $\overrightarrow{OC}1$ ,  $\overrightarrow{OC}2$ , and  $\overrightarrow{OC}3$  are low.

#### LOGIC DIAGRAMS

'825

'826



# 8-Bit Bus Interface Flip-Flops with 3-State Outputs

# **Absolute Maximum Ratings\***

These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . . . Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

#### DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Symbol Test Conditions		= 25°C	KS74AHCT $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-6mA$	V <sub>CC</sub> 4.2	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	l <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Outprit Enable =VIH VOUT=VCC or GND		±0.5	±5.0	±10.0	μА
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA.

# AC ELECTRICAL CHARACTERISTICS (Input tr, tr<2 ns), AHCT825, AHCT826

Characteristic		Symbol	Conditions†		T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	T. = -40°	AHCT C to +85°C 0V±10%	Ta = -55°C	AHCT to +125°C OV ± 10%	Unit
						Min	Max	Min	Max	
Maximum Op	erating Frequency	f <sub>max</sub>	C <sub>L</sub> =50p	F	50	35		30		MHz
Propagation Delay CLK to any Q		t <sub>PLH</sub>	C <sub>L</sub> =50p C <sub>L</sub> =150		8 11		14 19		17 23	ns
		t <sub>PHL</sub>	C <sub>L</sub> =50p C <sub>L</sub> =150		8 11		14 19		17 23	113
Propagation CLR to Any		t <sub>PHL</sub>	C <sub>L</sub> =50pl C <sub>L</sub> =150		10 13		17 22		21 27	ns
Output Enable Time, OC to any Q		tpzH	R <sub>i</sub> = 1 kΩ	C <sub>L</sub> =50pF G <sub>L</sub> =150pF	11 14		18 23		22 28	ns
		tpzL	112	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	11 14		18 23		22 28	113
Output Disab			$R_L=1k\Omega$ $C_L=50pF$		13		18		22	ns
OO to any Q	CLR low	tPLZ	CL-50pi		13 9	15	18	18	22	}
Pulse Width	CLK high or low	tw			9	15		18		ns
	CLR ingri or low		:		9	14		17		$\vdash$
Setup	Data	tsu			9	14	<del> </del>	17	<del>                                     </del>	ns
Time before CLKt CLKEN high or low					9	14		17		1
Hold Time, CLKEN or da	ita after CLKf	th			-3	0		0		ns
Input Capacit	acitance C <sub>IN</sub>			5					pF	
Output Capad	citance	Cout	Output D	isabled	10					pF
Power Dissip Capacitance*		C <sub>PD</sub>	OC=V <sub>CC</sub> OC=GNI		5 30					pF pF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} \ V_{CC}^2 \ f \ + \ I_{CC} \ V_{CC}$ .

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

Preliminary Specifications

#### **FEATURES**

- Bus-Structured Pinout
- Provides Extra Bus Driving Latches
- Necessary for Wider Address/Data Paths or Buses with Parity
- Power-Up High-Impedance State
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current
- ( $I_{OL}$  = 24 mA @  $V_{OL}$  = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATIONS

		'841			
ōc I	4	~	24	Ь	Vcc
1D	1 2		23	Б	1Q
2D (	3		.22	Ь	2Q
3D [	₫4		21	Ь	3Q
4D (	5		20	ь	4Q
5D (	<b></b>		19	Ь	5Q
6D (	<b>1</b> 7		18	Ь	6Q
7D (	<b>∃</b> 8		17	Ь	7Q
8D (	19		16	Ь	8Q
9D [	10		15	Ь	9Q
10D [	<b>1</b> 11		14	Ь	10Q
GND [	12		13	h	С

ı	•	^

oc C	1	24	Ь	Vcc
1Ď 🗀	2	23	Ь	1Q
2D 🗀	1	22	þ	2Q
3Ď ┏		21	Ь	3Q
4Ď 🔼		20	Þ	4Q
5Ď 🔼	6	19	Ь	5Q
6Ď □	7	18	Ь	6Q
7Ď 🗀	8			7Q
8D □	9	16	Ь	8Q
9D 🗀	10	15	Ь	9Q
10D 🕻	11	14		10Q
GND 🗀	12	13	Ь	С

#### DESCRIPTION

These 10-bit bus interface latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The ten latches are transparent D-type. The '841 has noninverting data (D) inputs and the '842 has inverting  $(\overline{D})$  inputs.

A buffered output control  $(\overline{OC})$  input can be used to place the ten outputs in either a normal logic state (high or low levels) or a high-impedance state. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are off.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### **FUNCTION TABLES**

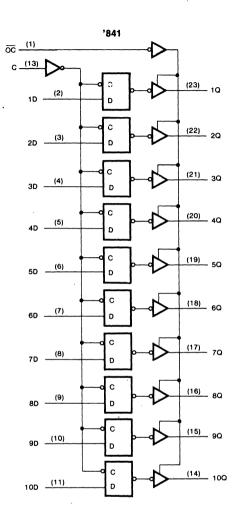
'84

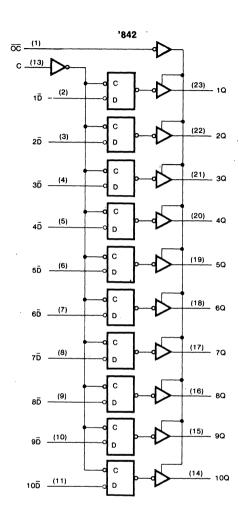
			041	
	lr	nputs	,	Output
	ŌĊ	С	D	Q
	L	Н	Н	Н
	L	Н	L	L
ı	L	L	X	$Q_0$
	Н	Х	Х	Z

'842

li	nputs	Output	
ŌĊ	С	D	Q
L	Н	Н	L
L	Н	L	H
L	L	Χ	$Q_0$
Н	Х	X	Z

# **LOGIC DIAGRAMS**





# KS54AHCT **841/842** KS74AHCT

# 10-Bit Bus Interface D-Type Latches with 3-State Outputs

# **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$\cdot (V_{I} < -0.5V \text{ or } V_{I} > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 70 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW

<sup>\*</sup> Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

# **Recommended Operating Conditions**

Supply Voltage, V <sub>CC</sub>	4.5V to 5.5V
DC Input & Output Voltages*, Vin, Vout	OV to Vcc
Operating Temperature	

Operating	remperature
Range	KS74AHCT: -40°C to +85°C
	KS54AHCT: -55°C to +125°C
nput Rise	& Fall Times, t <sub>r</sub> , t <sub>f</sub> Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

# DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T <sub>a</sub> = 25°C		KS74AHCT Ta = -40°C to +85°C	KS54AHCT T <sub>a = -55°C</sub> to +125°C	Unit
			Тур		Guaranteed Lim	its	1
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-6mA$	V <sub>CC</sub> 4.2	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> =0.1	V <sub>CC</sub> -0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	ΔΙσο	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA



<sup>†</sup> Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# AC ELECTRICAL CHARACTERISTICS (Input tr, tr≤2 ns), AHCT841, AHCT842

Characteristic	Symbol	Conditions <sup>†</sup>		Conditions <sup>†</sup>		T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	Ta = -40°0	AHCT C to +85°C DV ± 10%	$T_a = -55$ °C	AHCT to +125°C	Unit
				Тур	Min	Max	Min	Max			
Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pl C <sub>L</sub> =150		10 13		16 21		19 25	ns		
Data to Q	t <sub>PHL</sub>	C <sub>L</sub> =50pl C <sub>L</sub> =150		10 13		16 21	İ	19 25			
Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pl C <sub>L</sub> =150		15 18		24 29		29 35	ns		
C to any Q	t <sub>PHL</sub>		C <sub>L</sub> =50pF C <sub>L</sub> =150pF			24 29		29 35	113		
Output Enable Time,	t <sub>PZH</sub>	$R_L = 1 k\Omega$	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	13 16		18 23		22 28	ns		
OC to any Q	tpzL	H[- 1K12	$C_L = 50pF$ $C_L = 150pF$	13 16		18 23	,	22 28	115		
Output Disable Time,	t <sub>PHZ</sub>	$R_L = 1 k\Omega$ $C_L = 50 pl$	=	13 13		18 18		22	ns		
Pulse Width, C High	tw			12	20		25		ns		
Setup Time, Data before C↓	t <sub>su</sub>			6	10		12	,	ns		
Hold Time, Data after C↓	th			3	5		7		ns		
Input Capcitance	C <sub>IN</sub>			5 .					pF		
Output Capacitance	Cout	Output D	isabled	10					pF		
Power Dissipation Capacitance* (per stage)	C <sub>PD</sub>	ŌC=V <sub>CC</sub> ŌC=GNI		5 30					pF pF		

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC<sup>2</sup></sub> f + I<sub>CC</sub> V<sub>CC</sub>,

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

- Bus-Structured Pinout
- Provide Extra Bus Driving Latches
   Necessary for Wider Address/Data Paths or Buses
   with Parity
- . Power-Up High Impedance
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current
- ( $I_{OL}$  = 24 mA @  $V_{OL}$  = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

# PIN CONFIGURATIONS

	'843			
<u>oc</u> [	1	24	Ь	Vcc
1D 🗆	2	23	Ь	1Q
2D 🗖	3	22	Þ	2Q
3D 🗆	4	21	Þ	ЗQ
4D 🗆	5	20	Þ	4Q
5Ď 🗖	6	19	Ь	5Q
6D 🗆	7	18	Þ	6Q
7Ď 🗖	8	17	Þ	7Q
8D 🗖	9	16	Þ	8Q
9D 🗆	10	15	Þ	9Q
CLR [	11	14	Þ	PRE
GND 🗆	12	13	Þ	С

		'844			
ÖČ	4	1	24	Ь	Vcc
1Ď	d	2	23	Ь	1Q
2Ď	d	3	22	þ	2Q
ЗĎ	d	4	21	Ь	3Q
4Ď	d	5	20	Þ	4Q
5Ď	d	6	19	Þ	5Q
6Ď	d	7	18	þ	6Q
7Ď		8	17	þ	7Q
8Ď	d	9	16	ь	8Q
9Ď	d	10	15	Ь	9Q
CLR	d	11	14	þ	PRE
GND	d	12	13	þ	c Ì

#### DESCRIPTION

These 9-bit bus interface latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers and working registers.

The nine latches are transparent D-type. The '843 has noninverting data (D) inputs and the '844 has inverting  $\overline{D}$  inputs.

A buffered output control ( $\overline{OC}$ ) input can be used to place the nine outputs in either a normal logic state (high or low levels) or a high-impedance state. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control  $(\overline{OC})$  does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are off.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### **FUNCTION TABLES**

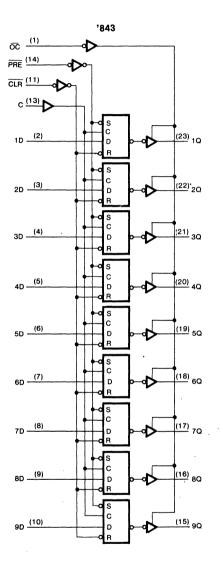
'843

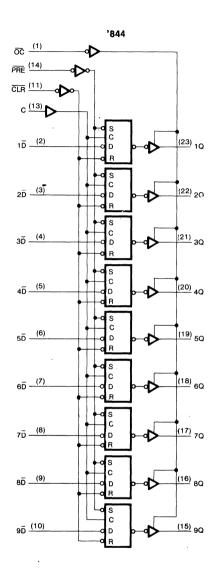
	IN		ОИТРИТ		
PRE	CLR	ŌĊ	С	D	Q
L	Х	L	Х	Х	Н
Н	L	L	Χ	Χ	L
Η.	н	L	Н	L	L
Н	Н	L	Н	Н	Н
Н	ŀН	L	L	Χ	$Q_0$
Х	Х	Н	Х	Х	Z

844

	IN		OUTPUT		
PRE	CLR	ŌĊ	С	D	Q
L	Х	L	Х	X	Н
Н	L	L	Χ	Χ	L
Н	н	L	Н	L	Н
Н	Н	L	Н	Н	. L
Н	Н	L	L	Χ	$Q_0$
X	X	Н	Х	Χ	Z

#### LOGIC DIAGRAMS





Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_0 < V_{CC} + 0.5V) \dots \pm 70 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.

These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Supply Voltage	, V <sub>CC</sub>		4.5V	to .5	.5۷
DC Input & Out	tput Voltages*, V <sub>IN</sub> ,	$V_{\text{OUT}}$	0\	∕ to ˈ	Vcc
Operating Temp	perature				
Range	KS74AHCT:	-40	°C to	+85	٥°C

Range KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . Max 500 ns

\* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

#### DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	Ta	= 25°C	KS74AHCT T <sub>a = -40°C</sub> to +85°C	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	1.
Minimum High-Level Input Voltage	V <sub>IH</sub>		`	2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-6mA$	V <sub>CC</sub> 4.2	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> -0.1	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 > 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

# AC ELECTRICAL CHARACTERISTICS (Input tr, tr≤2 ns), AHCT843, AHCT844

Characteristic	ic Symbol		conditions†		$ T_a = 25^{\circ}C \\ V_{CC} = 5.0V \\ T_a = -40^{\circ}C \text{ to } +85^{\circ}C \\ V_{CC} = 5.0V \pm 10^{\circ}K $		KS54 T <sub>a</sub> = -55°C V <sub>CC</sub> = 5.0	Unit	
·				Тур	Min	Max	Min	Max	
Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pl C <sub>L</sub> =150		13 16		18 23		22 28	ns
Data to Q	t <sub>PHL</sub>	C <sub>L</sub> = 50p C <sub>L</sub> =150		13 16		18 23		22 28	113
Propagation Delay.	t <sub>PLH</sub>	C <sub>L</sub> =50pl C <sub>L</sub> =150		16 19		26 31		31 37	ns
C to any Q	t <sub>PHL</sub>	C <sub>L</sub> =50pl C <sub>L</sub> =150		16 19		26 31		31 37	r 113
Propagation Delay, PRE to Q	tpLH		C <sub>L</sub> =50pF C <sub>L</sub> =150pF			27 32		32 38	ns
Propagation Delay, CLR to Q	t <sub>PHL</sub>		C <sub>L</sub> =50pF C <sub>L</sub> =150pF			27 32		32 38	ns
Output Enable Time,	tpzL	- R <sub>L</sub> =1kΩ	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	11 14		18 23		22 28	ns
OC to any Q	t <sub>PZL</sub>		C <sub>L</sub> =50pF C <sub>L</sub> =150pF	11 14		18 23		22 28	113
Output Disable Time,	tpHZ	$R_L = 1.k\Omega$		13		18		22	ns
OC to any Q	tPLZ	C <sub>L</sub> =50pl	C <sub>L</sub> =50pF			18		22	110
Pulse Width, C High	t <sub>w</sub>			12	20	,	25		ns
Setup Time, Data before C↓	tsu			8	10		12		ns
Hold Time, Data after C↓	th			3	5		7		ns
Input Capacitance	CIN			, 5					pF
Output Capacitance	Cout	Output D	isabled	10					pF
Power Dissipation Capacitance* (per stage)	C <sub>PD</sub>	ŌC=V <sub>CC</sub> ŌC=GNI		5 30				,	pF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

# KS54AHCT **845/846** KS74AHCT

# 8-Bit Bus Interface D-Type Latches with 3-State Outputs

#### **Preliminary Specifications**

#### FEATURE

- 3-state buffer-type outputs drive bus-lines directly
- · Bus-structured pinout
- Provides extra bus driving latches necessary for wider address/data paths or buses with parity
- Low power consumption characteristic of CMOS devices
- 3-state outputs with high drive current (I<sub>OL</sub> = 24mA
   V<sub>OL</sub> = 0.5V) for direct bus interface
- Direct interface capability with TTL, NMOS and CMOS devices
- Wide operating volage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to 125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

# **PIN CONFIGURATIONS**

	′845		
ŌC1 d	1	24	Ь v
OC2	2	23	<b>⊃</b> <del>oc</del> 3
1D 🗖	3	22	<b>1</b> 0
2D 🗖	4	21	2Q
3D 🗖	5	20	] 3Q
4D 🗆	6	19	<b>4</b> Q
5D 🗖	7	18	5Q
6D 🗖	8	17	<b>6</b> Q
<i>3</i> ₽ d	9	16	7Q
8D 🗖	10	15	<b>3</b> 8Q
CLR C	11	14	PRE
GND 🗖	12	13	bс

		_			
<u>oc</u> ₁ ⊏	1	$\sim$	24	Ь	Vcc
ŌC2 □	2		23	Ь	<del>ос</del> з
1 D C	3		22	þ	1Q
20 🕻	4		21	þ	2Q
3D 🗖		ø	20	Þ	3Q
40 🗆	-		19	b	4Q
5 <u>D</u> C			18	Ь	5Q
6 <u>D</u> ☐	8		17	Þ	6Q
7₫ 🗖			16	Ь	7Q
8D 🗖			15	Ь	8Q
CLR C	11		14	þ	PRE
GND [	12		13	Þ	С

#### DESCRIPTION

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches are transparent D-type. The '845 has noninverting data(D) inputs. The '846 has inverting D inputs. Since CLR and PRE are independent of the clock, taking the CLR input low will cause the eight Q outputs to go low. Taking the PRE input low will cause the eight Q outputs to go high. When both PRE and CLR are taken low, the outputs will follow the preset condition.

The buffered output control inputs ( $\overline{OC}1$ ,  $\overline{OC}2$ , and  $\overline{OC}3$ ) can be used to place the eight outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impendance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output controls do not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

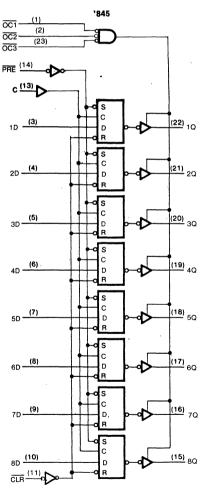
# FUNCTION TABLE,845

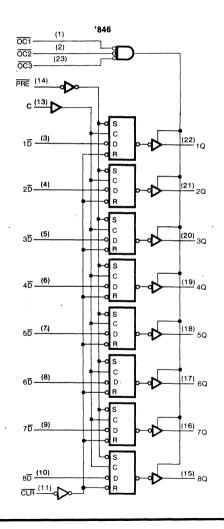
		IN	PUTS				OUTPUT
PRE	CLR	OC1	OC2	OC3	С	D	Q
L	Н	L	L	L	Χ	Χ	Н
Н	L	L	L	L	Χ	Х	L,
L	L	L	L	L	X.	Х	H
Н	Н	L	L	L	Н	L	L
н	н	L	L	L	Н	Н	Н
Н	Н	L	L	L	L	Х	$Q_0$
Х	Х	Х	Х	н	Х	Х	Z
Х	Х	Х	Н	Х	Х	Х	Z
Χ	Х	Н	Х	Х	Х	Х	Z

			•	40			
	,	IN	PUTS				OUTPUT
PRE	CLR	OC1	ŌC2	OC3	С	D	Q ·
L	Н	L	L	L	Х	Х	Н
Н	L	L	L	L	Х	Х	L
L	Ĺ	L	L	L	Х	Х	Н
Н	Н	L	L	L	Н	L	Н
Н	Н	L	L	L	Н	Н	L
Н	Н	L	L	L	L	Х	$Q_0$
Х	Х	Х	Х	H	Х	Х	Z
Χ	Х	Х	Н	Х	Χ	Х	Z
Х	Х	Н	Х	Χ	Х	Х	Z

,046

# **LOGIC DIAGRAMS**





# 8-Bit Bus Interface D-Type Latches with 3-State Outputs

# **Absolute Maximum Ratings\***

Supply Voltage Range $V_{CC}$ , $-0.5V$ to $+7V$ DC Input Diode Current, lik
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + 0.5V$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, $P_d{}^\dagger$ 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Range KS74AHCT: -40°C to +85°C
KS54AHCT: -55°C to +125°C
Input Rise & Fall Times, t<sub>r</sub>, t<sub>t</sub> . . . . . . . Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

#### DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	Т	<sub>a</sub> = 25°C	KS74AHCT T <sub>a</sub> = -40°C to +85°C	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	ViH			2.0	2.0	^ 2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	Voh	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	· V
Maximum Input Current	liN	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input in  V <sub>I</sub> =2.4V  other Inputs:  at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0µA		2.7	2.9	3.0	mA

# KS54AHCT **845/846** KS74AHCT

# 8-Bit Bus Interface D-Type Latches with 3-State Outputs

#### AC ELECTRICAL CHARACTERISTICS (Input tr., tr≤2 ns), AHCT845

Characteristic	Symbol Conditions†	$T_a = 25^{\circ}C$ $V_{CC} = 5.0V$			T <sub>a</sub> = -55°C	AHCT to +125°C V± 10%	Unit	
			Тур	Min	Max	Min	Max	
Propagation Delay	t <sub>PLH</sub>		13		22		26	ns
Clk to Q	t <sub>PHL</sub>		13		22		26	
Propagation Delay	t <sub>PLH</sub>		8		15		20	ns
D to Q	t <sub>PHL</sub>		8		15		20	113
Propagation Delay	tpLH		16		26		31	ns
CLR to Q	tpHL		16		26		31	
Propagation Delay	t <sub>PLH</sub>	PLH	16		26		31	ns
PRE to Q	t <sub>PHL</sub>		16		26		31	
Propagation Delay	t <sub>PZH</sub>		12		20		24	ns
OC to Q	t <sub>PZL</sub>		12		20		24	
Propagation Delay	t <sub>PHZ</sub>		12		20		24	ns
OC to Q	t <sub>PLZ</sub>		12		20		24	113
Input Capacitance	CIN		5					pF
Power dissipation Capacitance*	C <sub>PD</sub>							рF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

# AC ELECTRICAL CHARACTERISTICS (Input t<sub>r</sub>, t<sub>f</sub>≤2 ns), AHCT846

Characteristic	Symbol	rmbol Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	KS74AHCT $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> =5.0V ± 10%		Unit
			Тур	Min	Max	Min	Max	
Propagation Delay	t <sub>PLH</sub>		14		24		32	ns
Clk to Q	t <sub>PHL</sub>		14		24		32	1.0
Propagation Delay	t <sub>PLH</sub>		10		17		22	ns
D to Q	t <sub>PHL</sub>		10		17		22	113
Propagation Delay	t <sub>PLH</sub>		13		22		26	ns
CLR to Q	tpHL		13		22		26	
Propagation Delay	t <sub>PLH</sub>		13		22		26	ns
PRE to Q	t <sub>PHL</sub>		13		22		26	'5
Propagation Delay	t <sub>PZH</sub>		12		20		24	ns
OC to Q	t <sub>PZL</sub>		12		20		24	
Propagation Delay	t <sub>PHZ</sub>		12		20		24	ńs
OC to Q	·tpLZ		12		20		24	
Input Capacitance	CIN		5					pF
Power dissipation Capacitance*	C <sub>PD</sub>							pF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

- Modified input structure allows voltages up to 15V
- High-Drive-current Outputs:
   IOL = 8mA @ VOL = 0.5V
- Low power consumption characteristic of CMOS
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

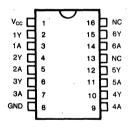
# **DESCRIPTION**

The '4049 and '4050 have a modified input protection structure that enable them to be used as logic level translators which will convert high level logic to a low level logic while operating from the low logic supply. For example, 0-15V logic can be corverted to 0-5V logic when using a 5V supply. The modified input protection has no diode connected to  $V_{\rm cc}$ , thus allowing the input voltage to exceed the supply. The lower zener diode protects the input from both positive and negative static voltages. In addition the '4049 and '4050 can be used as simple buffers or inverters without level translation.

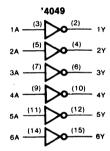
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

## PIN CONFIGURATION



#### LOGIC DIAGRAMS



# 1A (3) (2) 1Y 2A (5) (4) 2Y 3A (7) (6) 3Y 4A (9) (10) 4Y 5A (11) (12) 5Y 6A (14) (15) 6Y

4050

## **FUNCTION TABLE**

Input	Outp	out Y
A	'4049	'4050
Н	L,	Н
L	н '	L

Supply Voltage Range $V_{CC}$ , $-0.5V$ to $+7V$
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > +15.5V)$ ±20 mA
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±35 mA
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-
posure to these conditions may affect device reliability.
posdie to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Supply Voltage, Vo	c	4.5V to 5.5V
DC Input & Output	Voltages*, V <sub>IN</sub> ,	Vout OV to Voc
Operating Tempera	ature	
Range	KS74AHCT:	-40°C to +85°C
	KS54AHCT:	-55°C to +125°C
Input Rise & Fall T	imae t. t.	May 500 ns

 Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

# DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	ool Test Conditions		= 25°C	$KS74AHCT$ $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54AHCT T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	٧
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND V <sub>IN</sub> =15V		±0.1	±1.0 ±10.0	±1.0 ±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	ΔΙσ	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

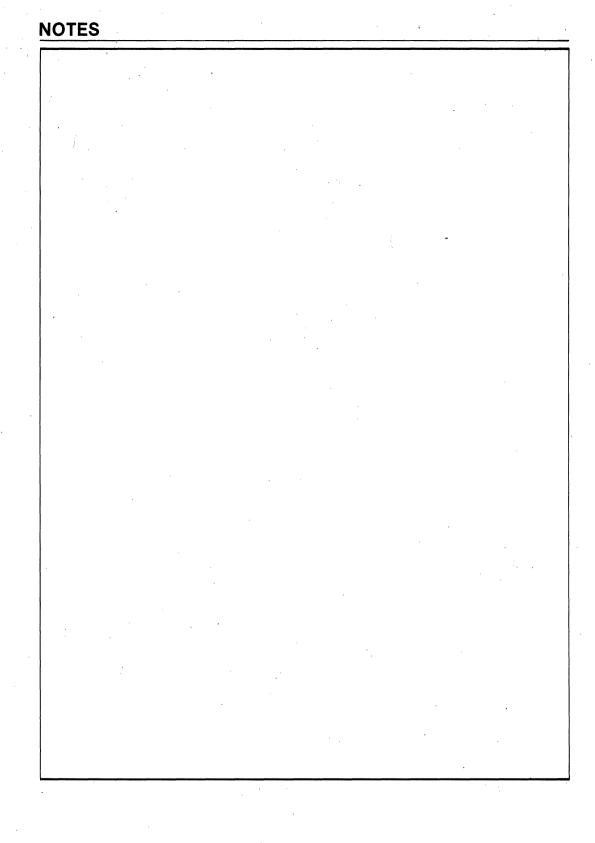
# AC ELECTRICAL CHARACTERISTICS (Input t<sub>r</sub>, t<sub>f</sub> < 2 ns), AHCT4049, AHCT4050

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V	$KS74AHCT$ $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> =5.0V ± 10%		Unit
			Тур	Min	Max	Min	Max	
Propagation Delay	tpLH	C <sub>L</sub> =50pF	7		12		14	ns
Propagation belay	t <sub>PHL</sub>		7		12		14	
Input Capacitance	CiN		5					pF
Power Dissipation Capacitance*	C <sub>PD</sub>	(per gate)	15					pF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ 

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.









- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
   I<sub>OL</sub> = 8mA @ V<sub>OL</sub> = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
   KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

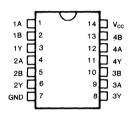
#### DESCRIPTION

These devices contain four independent 2-input NAND gates that perform the Boolean functions  $Y = \overline{A \cdot B}$  or  $Y = \overline{A} + \overline{B}$ .

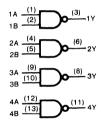
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### PIN CONFIGURATION



#### LOGIC DIAGRAM



#### **FUNCTION TABLE**

#### (Each Gate)

	Inp	uts	Output
	A	В	Υ
Г	Н	Н	L
	L	Χ	н
	Х	L	Н

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissination Per Package D.t 500 mW

Power Dissipation Per Package, Pdf ....... 500 mW
\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . . Max 500 ns

 Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

#### DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T <sub>a</sub> = 25°C		KS74HCTLS T <sub>a</sub> = -40°C to +85°C	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	<b>2.0</b>	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> -0.1 3.84	V <sub>CC</sub> −0.1 3.7	V
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin $V_I$ =2.4V other inputs: at $V_{CC}$ or GND $I_{OUT}$ =0 $\mu$ A		2.7	2.9	3.0	mA

# AC ELECTRICAL CHARACTERISTICS (Input tr, tr 66 ns), HCTLS00

					* **		
Characteristic	Symbol Co	Conditions <sup>†</sup>	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74 HCTLS T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%	KS54HCTLS $T_a = -55^{\circ}\text{C to } + 125^{\circ}\text{C}$ $V_{\text{CC}} = 5.0\text{V} \pm 10\%$	Unit
			Тур		Guaranteed Limits		
Maximum Propagation Delay	tpLH	t <sub>PLH</sub> C <sub>L</sub> =50pF	10	15	18	22	ns
Waximum Fropagation Delay			10	15	18	22	113
Maximum Input Capacitance	C <sub>IN</sub>		5				pF
Power Dissipation Capacitance*	C <sub>PD</sub>	(per gate)	15			,	pF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.



- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
  - IoL = 8mA @ VoL = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
   (2021) (2022) (2022) (2022)

KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

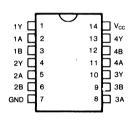
#### **DESCRIPTION**

These devices contain four independent 2-input NAND gates with open-drain outputs. Using a suitable pull-up resistor, these outputs may be connected to other open-drain outputs to implement wired-AND functions.

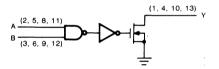
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground

#### PIN CONFIGURATION



#### LOGIC DIAGRAM



#### **FUNCTION TABLE**

(Each Gate)

Inp	uts	Output
Α	В	Y
Н	Н	L
Ľ	X	н
Х	L	Н

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±35 mA
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> −65°C to +150°C
Power Dissipation Per Package Pat 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

#### DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	√T <sub>a</sub> = 25°C		KS74HCTLS T <sub>a</sub> = -40°C to +85°C	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	v
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	0.8	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μА
Maximum Output Leakage Current	loz .	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> =V <sub>CC</sub>		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	Icc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA	,	2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin  V <sub>I</sub> =2.4V  other Inputs: at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0µA		2.7	2.9	3.0	mA

# AC ELECTRICAL CHARACTERISTICS (Input tr., tre6 ns), HCTLS01

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74HCTLS $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	KS54HCTLS $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$	Unit
			Тур		Guaranteed Limits		
Maximum Propagation Delay	t <sub>PLH</sub>	$C_L=50pF$ $R_L=1k\Omega$	24	30	36	43	ns
Maximum Propagation Delay	t <sub>PHL</sub>		15	20	25	30	
Maximum Input Capacitance	CIN		5				pF
Power Dissipation Capacitance*	C <sub>PD</sub>	(per gate)	15				pF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.



- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
- $I_{OL} = 8mA @ V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
   KS74HCTLS: -40°C to +85°C

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

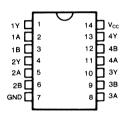
#### **DESCRIPTION**

These devices contain four independent 2-input NOR gates that perform the Boolean functions  $Y = \overline{A} + \overline{B}$  or  $Y = \overline{A} \bullet \overline{B}$ .

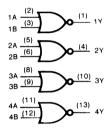
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

# PIN CONFIGURATION



#### LOGIC DIAGRAM



#### **FUNCTION TABLE**

(Each Gate)

Inp	uts	Output
Α	В	Y
Н	Х	L
X	H	L
L	L	H.

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±35 mA
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, $T_{stg} \dots -65^{\circ}C$ to $+150^{\circ}C$
Power Dissipation Per Package, $P_d{}^\dagger$ 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-
posure to these conditions may affect device reliability.
poddio to those conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

#### **Recommended Operating Conditions**

Supply Voltage, V <sub>CC</sub>	4.5V to 5.5V
DC Input & Output Voltages*, VIN, VOUT	OV to Vcc
Operating Temperature	

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . . Max 500 ns

 Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

# DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	ymbol Test Conditions	T <sub>a</sub> = 25°C		KS74HCTLS T <sub>a</sub> = -40°C to +85°C	KS54HCTLS $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin  V <sub>I</sub> =2.4V  other Inputs: at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0µA		2.7	2.9	3.0	mA

# AC ELECTRICAL CHARACTERISTICS (Input tr, ties 6 ns), HCTLS02

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74HCTLS T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%	KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	Unit	
			Тур		Guaranteed	l Limits		
Maximum Propagation Delay	t <sub>PLH</sub>	t <sub>PLH</sub>	t <sub>PLH</sub> C <sub>L</sub> =50pF	9	15	18	22	ns
Waximum Propagation Delay	t <sub>PHL</sub>	OL-30bi	10	15	18	22	115	
Maximum Input Capacitance	CiN		5				pF	
Power Dissipation Capacitance*	C <sub>PD</sub>	(per gate)	15				рF	

<sup>\*</sup> CPD determines the no-load dynamic power dissipation: PD=CPD VCC2 f + ICC VCC

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.



- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current Outputs: I<sub>OL</sub> = 8mA @ V<sub>OL</sub> = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
   KS74HCTLS: -40°C to +85°C
   KS54HCTLS: -55°C to +125°C
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

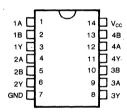
#### DESCRIPTION

These devices contain four independent 2-input NAND gates with open-drain outputs. Using a suitable pull-up resistor, these outputs may be connected to other open-drain outputs to implement wired-AND functions.

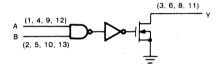
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### PIN CONFIGURATION



# LOGIC DIAGRAM



#### **FUNCTION TABLE**

(Each Gate)

Inputs		Output
Α	B	Y
Н	Н	L
L	Х	Н
Х	L	Н

Supply Voltage Range $V_{CC}$ , $-0.5V$ to $+7V$
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, I <sub>OK</sub>
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±35 mA
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-

posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Supply Voltage,	. V <sub>CC</sub> 4.5V to 5.5V
DC Input & Out	put Voltages*, VIN, VOUT OV to VCC
Operating Temp	perature
Range	KS74HCTLS: -40°C to +85°C
	KS54HCTLS: -55°C to +125°C

Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . . Max 500 ns

\* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

#### DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T <sub>a</sub> = 25°C		KS74HCTLS KS54HCTLS $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $T_a = -55^{\circ}\text{C to } +$		Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	v
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Output Leakage Current	loz	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> =V <sub>CC</sub>		±0.5	±5.0	±10.0	μА
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin  V <sub>I</sub> =2.4V  other Inputs: at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0µA		2.7	2.9	3.0	mA

# AC ELECTRICAL CHARACTERISTICS (Input tr, tres ns), HCTLS03

Characteristic	Symbol	Symbol Conditions! $V_{co} = 5.0V$ $T_a = -40^{\circ}C$ to $+85^{\circ}C$ $T_a = -55^{\circ}$		Conditions $\begin{vmatrix} T_a = 25^{\circ}C \\ V_{co} = 5 \text{ OV} \end{vmatrix}$ $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$		KS54HCTLS  T <sub>a</sub> = -55°C to +125°C  V <sub>CC</sub> = 5.0V ± 10%	Unit
			Тур		Guaranteed	Limits	
Maximum Propagation Delay	t <sub>PLH</sub>	C <sub>L</sub> =50pF	24	30	36	43	ns
Maximum Fropagation Delay	t <sub>PHL</sub>	$R_L=1k\Omega$	15	20	25	30	113
Maximum Input Capacitance	C <sub>IN</sub>	·	5				pF
Power Dissipation Capacitance*	C <sub>PD</sub>	(per gate)	15				pF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} \ V_{CC}^2 \ f \ + \ I_{CC} \ V_{CC}$ .

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.



- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- · High-Drive-Current outputs:
  - $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5 \text{V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

   (C7410710: 4000 to 4000)

   (C7410710: 4000 to 4000)

   (C7410710: 4000 to 4000)

   (C7410710: 4000 to 4000 to 4000)

   (C7410710: 4000 to 4000

KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

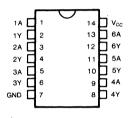
#### DESCRIPTION

These devices contain six independent inverters. They perform the Boolean function Y=  $\overline{A}$  .

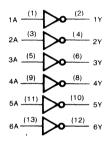
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

# **PIN CONFIGURATION**



# LOGIC DIAGRAM



#### **FUNCTION TABLE**

#### (Each Inverter)

Input	Output
A	Y
Н	L
L	Н

Supply Voltage Range $V_{CC}$ , $-0.5V$ to $+7V$
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, I <sub>OK</sub>
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW
* Absolute Maximum Ratings are those values beyond

which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

# **Recommended Operating Conditions**

Supply Voltage, Vo	c 4.5V to 5.5V
DC Input & Output	Voltages*, $V_{\text{IN}}$ , $V_{\text{OUT}}$ OV to $V_{\text{CC}}$
Operating Tempera	ture
Range	KS74HCTLS: -40°C to +85°C
	KS54HCTLS: -55°C to +125°C

Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . Max 500 ns

\* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

# DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T <sub>a</sub> = 25°C		KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS $T_a = -55$ °C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V <sub>IH</sub>	,		2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH} \text{ or } V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-4\text{mA}$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> -0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> =20µA I <sub>O</sub> =4mA I <sub>O</sub> =8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μА
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0µA		2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	Δłcc	per input pin  V <sub>I</sub> =2.4V  other Inputs: at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0µA		2.7	2.9	3.0	mA

### AC ELECTRICAL CHARACTERISTICS (Input tr, tre6 ns), HCTLS04

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74HCTLS T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%	KS54 HCTLS  T <sub>a</sub> = -55°C to +125°C  V <sub>CC</sub> =5.0V ± 10%	Unit
1			Тур	Typ Guaranteed Limits			
Maximum Propagation Delay	t <sub>PLH</sub>	C <sub>L</sub> =50pF	9	15	. 18	22	ns
Waximaiii i Topagation Belay	tpHL		10	15	18 ·	22	
Maximum Input Capacitance	C <sub>IN</sub>		5				pF
Power Dissipation Capacitance*	C <sub>PD</sub>	(per gate)	15				pF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.



<sup>†</sup> Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

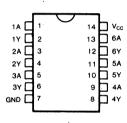
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
  - $I_{OL} = 8$  mA @  $V_{OL} = 0.5$ V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
   (2741071.5: 4090.45 + 8590.5)

KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

# PIN CONFIGURATION



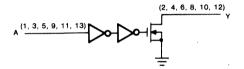
#### DESCRIPTION

These devices contain six independent inverters with opendrain outputs. Using a suitable pull-up resistor, these outputs may be connected to other open-drain outputs to implement wired-AND functions.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### LOGIC DIAGRAM



#### **FUNCTION TABLE**

#### (Each Inverter)

•	
Input	Output
A	Y
Н	L
L	н

Supply Voltage Range V <sub>CC</sub> ,
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
( $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ ) $\pm 20$ mA
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, P <sub>d</sub> <sup>†</sup> 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . . Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

#### DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

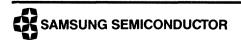
Characteristic S	Symbol	Test Conditions	T <sub>a</sub> = 25°C		KS74HCTLS T <sub>a</sub> = -40°C to +85°C	KS54HCTLS C T <sub>a</sub> = -55°C to +125°C	
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Output Leakage Current	loz	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> =V <sub>CC</sub>		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin  V <sub>I</sub> =2.4V  other Inputs:  at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0µA		2.7	2.9	3.0	mA

#### AC ELECTRICAL CHARACTERISTICS (Input tr. tr 46 ns), HCTLS05

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74HCTLS $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 10^{\circ}\text{M}$	KS54 HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> =5.0V ± 10%	Unit
			Тур	p Guaranteed Limits			
Maximum Propagation Delay	t <sub>PLH</sub>	C <sub>L</sub> =50pF	.24	30	36	43	ns
Waximum Fropagation Delay	t <sub>PHL</sub> R <sub>L</sub> =	$R_L=1k\Omega$	16	22	28	33	113
Maximum Input Capacitance	CIN		5				pF
Power Dissipation Capacitance*	C <sub>PD</sub>	(per gate)	15				pF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.



- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
   I<sub>OL</sub> = 8 mA @ V<sub>OL</sub> = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### **DESCRIPTION**

These devices contain four independent 2-input AND gates. They perform the Boolean functions  $Y = A \bullet B$  or  $Y = \overline{A + B}$ .

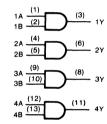
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### PIN CONFIGURATION



# LOGIC DIAGRAM



#### **FUNCTION TABLE**

(Each Gate)

Inp	uts	Output
A	В	Y
Н	Н	Н
L	Χ	L
_ X	L	L

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_0 < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-

posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

#### **Recommended Operating Conditions**

Supply Voltage, V <sub>CC</sub>	4.5V to 5.5V
DC Input & Output Voltages*, VIN, VOUT	OV to $V_{CC}$
Operating Temperature	

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

#### DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

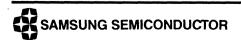
Characteristic	Symbol	bol Test Conditions	T <sub>a</sub> = 25°C		KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS $T_a = -55$ °C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> −0.1 3.98	V <sub>CC</sub> -0.1	V <sub>CC</sub> −0.1 3.7	٧
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μĄ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	00	per input pin  V <sub>I</sub> =2.4V  other Inputs: at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

#### AC ELECTRICAL CHARACTERISTICS (Input tr. tres 6 ns), HCTLS08

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74 HCTLS $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 10^{\circ}\text{M}$	KS54HCTLS $T_a = -55^{\circ}\text{C to } + 125^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	Unit
			Typ Guaranteed Limits			1	
Maximum Propagation Delay	t <sub>PLH</sub>	C <sub>L</sub> =50pF	10	15	18	22	ns
· · · · · · · · · · · · · · · · · · ·	t <sub>PHL</sub>		10	20	25	30	
Maximum Input Capacitance	C <sub>IN</sub>		5		,		pF
Power Dissipation Capacitance*	C <sub>PD</sub>	(per gate)	15				pF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.



# 5

#### **FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
  - IOL = 8 mA @ VOL = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### DESCRIPTION

These devices contain four independent 2-input AND gates with open-drain outputs. Using a suitable pull-up resistor, these outputs may be connected to other open-drain outputs to implement wired-AND functions.

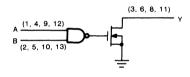
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### PIN CONFIGURATION

#### 

#### LOGIC DIAGRAM



#### **FUNCTION TABLE**

(Each Gate)

Inp	uts	Output
A	В	Y
Н	Н	Н
L	Χ	L
Х	L	L

Supply Voltage Range $V_{CC}$ ,0.5V to +7V DC Input Diode Current, $I_{IK}$
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
, $(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±35 mA
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-
posure to these conditions may affect device reliability.
posure to triese conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Supp	oly Voltage, Vo	x	4.5	V to 5.5V
DC I	nput & Output	Voltages*, V <sub>IN</sub> ,	V <sub>OUT</sub>	OV to Vcc
Oper	rating Tempera	ture		
R	lange	KS74HCTLS:	-40°C	to +85°C
		KS54HCTLS:	-55°C to	+125°C

Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . Max 500 ns \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

# DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T <sub>a</sub> = 25°C		KS74HCTLS T <sub>a</sub> = -40°C to +85°C	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit
		,	Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	.0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Output Leakage Current	loz	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> =V <sub>CC</sub>		±0.5	±5,0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	ΔΙσο	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		. 2.7.	2.9	3.0	mA

# AC ELECTRICAL CHARACTERISTICS (Input tr, tre6 ns), HCTLS09

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74HCTLS T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%	KS54HCTLS $T_a = -55$ °C to +125°C $V_{CC} = 5.0V \pm 10\%$	Unit
			Тур		Guaranteed	Limits	
Maximum Propagation Delay	t <sub>PLH</sub>	$C_L=50pF$ $R_L=1k\Omega$	26	32	38	45	ns
Maximum Propagation Delay	t <sub>PHL</sub>		16	22	28	33	113
Maximum Input Capacitance	CIN		5		•		pF
Power Dissipation Capacitance*	C <sub>PD</sub>	(per gate)	15				рF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.



- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
   I<sub>OL</sub> = 8 mA @ V<sub>OL</sub> = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
   KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

## **DESCRIPTION**

These devices contain three independent 3-input NAND gates. They perform the Boolean functions  $Y = \overline{A} \bullet B \bullet \overline{C}$  or  $Y = \overline{A} + \overline{B} + \overline{C}$ .

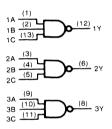
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{\text{CC}}$  and ground.

#### PIN CONFIGURATION



## LOGIC DIAGRAM



#### **FUNCTION TABLE**

(Each Gate)

	Inputs	Output	
A	В	С	Υ
Н	Н	Н	L
L	X	X	н
X	L	Х	н
Х	Х	L	Н

DC Input Diode Current, $I_{IK}$ ( $V_I < -0.5V$ or $V_I > V_{CC} +0.5V$ ) $\pm 20$ mA
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V)$ +20 mA
(1) 1 0.01 0. 1/2 100 10.01/ 220 11
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±35 mA
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> −65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Range KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

#### DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T <sub>a</sub> = 25°C		KS74HCTLS KS54HCTLS $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $T_a = -55^{\circ}\text{C to } +85^{\circ}\text{C}$		Unit
			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	У
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	liN	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	. ±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>i</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

#### AC ELECTRICAL CHARACTERISTICS (Input tr, tre6 ns), HCTLS10

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74 HCTLS T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%	KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	Unit
			Тур		Guaranteed Limits		
Maximum Propagation Delay	t <sub>PLH</sub>	C <sub>L</sub> =50pF	.11	15	19	23	ns
Waximum Fropagation Belay	t <sub>PHL</sub>		11	15	19	23	'''
Maximum Input Capacitance	C <sub>IN</sub>		5		,		pF
Power Dissipation Capacitance*	C <sub>PD</sub>	(per gate)	15				pF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.



#### 3

#### **FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs: I<sub>OL</sub> = 8 mA @ V<sub>OL</sub> = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
   KS74HCTLS: -40°C to +85°C
   KS54HCTLS: -55°C to +125°C
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

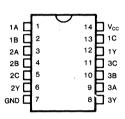
#### **DESCRIPTION**

These devices contain three independent 3-input AND gates. They perform the Boolean functions  $Y = A \cdot B \cdot C$  or  $Y = \overline{A + B + C}$ .

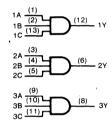
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground

## PIN CONFIGURATION



#### LOGIC DIAGRAM



#### **FUNCTION TABLE**

(Each Gate)

	Inputs	Output	
Α	В	С	Y
Н	Н	Н	Н
L	Х	Х	L
X	L	Х	L
Х	Χ	L	L

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IoK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package Pat 500 mW

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Supply Voltage, V<sub>CC</sub> . . . . . . . . . . . . . . . . . 4.5V to 5.5V DC Input & Output Voltages\*, V<sub>IN</sub>, V<sub>OUT</sub> . . . OV to V<sub>CC</sub> Operating Temperature

Range KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . . Max 500 ns

\* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions		<sub>a</sub> = 25°C	KS74HCTLS $T_{a} = -40$ °C to +85°C	KS54HCTLS $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

# AC ELECTRICAL CHARACTERISTICS (Input tr, tr 66 ns), HCTLS11

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74HCTLS T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> =5.0V±10%	KS54 HCTLS  T <sub>a</sub> = -55°C to +125°C  V <sub>CC</sub> = 5.0V ± 10%	Unit
			Тур		Guaranteed Limits		
Maximum Propagation Delay	t <sub>PLH</sub>	C <sub>1</sub> = 50pF	13	18	22	. 26	ns
The state of the s	t <sub>PHL</sub>	OL COPI	13	18	22	26	113
Maximum Input Capacitance	C <sub>IN</sub>		5				рF
Power Dissipation Capacitance*	C <sub>PD</sub>	(per gate)	15				pF

 $<sup>^{\</sup>prime}$  C<sub>PD</sub> determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ 

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.



- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
  - IOL = 8 mA @ VOL = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### **DESCRIPTION**

These devices contain three independent 3-input NAND gates with open-drain outputs. They perform the Boolean functions  $Y = \overline{A} \bullet \overline{B} \bullet \overline{C}$  or  $Y = \overline{A} + \overline{B} + \overline{C}$ .

Using a suitable pull-up resistor, these outputs may be connected to other open-drain outputs to implement wired-AND functions.

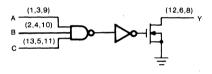
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### PIN CONFIGURATION



#### LOGIC DIAGRAM



#### **FUNCTION TABLE**

(Each Gate)

	Inputs	Output	
A	В	С	Υ
Н	Н	Н	L
L	Х	X	н
X	L	Х	н
Х	X	L	Н

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, IIK
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW
* Abashda Mariarias Delinas are Massa colore barrand

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Range KS74HCTLS:  $-40^{\circ}$ C to  $+85^{\circ}$ C KS54HCTLS:  $-55^{\circ}$ C to  $+125^{\circ}$ C Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . . . Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

#### DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	ol Test Conditions	, T <sub>a</sub> = 25°C		KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V <sub>IH</sub>	,		2.0	2.0	2.0	٧
Maximum Low-∟evel Input Voltage	, V <sub>IL</sub>			0.8	0.8	0.8	٧
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1	v
Maximum Input Current	l <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Output Leakage Current	loz	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> =V <sub>CC</sub>		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

#### AC ELECTRICAL CHARACTERISTICS (Input tr. tie6 ns), HCTLS12

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74 HCTLS $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> =5.0V ± 10%	Unit
			Тур		Guaranteed Limits		
Maximum Propagation Delay	tpLH	C <sub>L</sub> =50pF	26	32	38	45	ns
Waximum Topagation Delay	t <sub>PHL</sub>	$R_L=1k\Omega$	16	22	28	33	
Maximum Input Capacitance	CIN		5				рF
Power Dissipation Capacitance*	C <sub>PD</sub>	(per gate)	15				pF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.



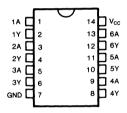
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
   I<sub>OL</sub> = 8 mA @ V<sub>OL</sub> = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
   KSZANCTI St. 409C to 1.959C

KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATION



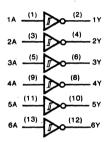
#### **DESCRIPTION**

These Schmitt-trigger devices contain six independent inverters. They perform the Boolean function  $Y = \overline{A}$ .

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### LOGIC DIAGRAM



## **FUNCTION TABLE**

#### (Each Inverter)

Input	Output
mpat	·
A	Y
Н	L
L	н

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stq</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

# DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T <sub>a</sub> =25°C		KS74HCTLS T <sub>a</sub> = -40°C to +85°C	KS54HCTLS $T_{a} = -55^{\circ}\text{C to } +125^{\circ}\text{C}$	Unit
			Тур	yp Guaranteed Limits			
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-4mA$	Vcc 4.2	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC (</sub> -0.11	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0,33 0.5	0.1 0.4	v
Maximum Input Current	l <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin  V <sub>I</sub> =2.4V  other inputs: at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

## DC ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions	Ta=25°C		KS74HCTLS T <sub>a</sub> = -40°C to +85°C		KS54HCTLS T <sub>a</sub> = -55°C to +125°C		Unit
Characteristic	Cymbol	Test Conditions	Min	Max	Min	Max	Min	Max	
Positive-Going	V <sub>T+</sub>	V <sub>CC</sub> =4.5V	1.2	1.9	1.2	1.9	1.2	1.9	V
Threshold Voltage	V 1 +	V <sub>CC</sub> =5.5V	1.4	2.1	1.4	2.1	1.4	2.1	
Negative-Going	V <sub>T</sub> _	$V_{CC}=4.5V$	0.5	1.2	0.5	1.2	0.5	1.2	· v
Threshold Voltage	V 1 -	V <sub>CC</sub> =5.5V	0.6	1.4	0.6	1.4	0.6	1.4	
Hysteresis	VH	V <sub>CC</sub> =4.5V	0.4	1.4	0.4	1.4	0.4	1.4	ν
(V <sub>T+</sub> -V <sub>T-</sub> )	VH.	V <sub>CC</sub> =5.5V	0.4	1.5	0.4	1.5	0.4	1.5	

# AC ELECTRICAL CHARACTERISTICS (Input tr, tr≤6 ns), HCTLS14

Characteristic	Symbol	Conditions <sup>†</sup>	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74 HCTLS $T_a = -40^{\circ}\text{C}$ to +85°C $V_{CC} = 5.0\text{V} \pm 10\%$	KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	Unit
			Тур		Guaranteed Limits		
Maximum Propagation Delay	t <sub>PLH</sub>	C <sub>L</sub> =50pF	15	20	25	30	ns
Waximum Fropagation Belay	t <sub>PHL</sub>		16	22	28	33	
Maximum Input Capacitance	CIN		5				pF
Power Dissipation Capacitance*	C <sub>PD</sub>	(per gate)	15				pF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} \, V_{CC^2} \, f + I_{CC} \, V_{CC}$ .
† For AC switching test circuits and timing waveforms see section 2.

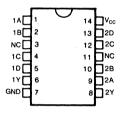
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
   I<sub>OL</sub> = 8 mA @ V<sub>OL</sub> = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

  KETANOTIC: 4000 to 10000

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATION



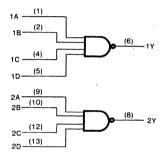
#### **DESCRIPTION**

These devices contain two independent 4-input NAND gates. They perform the Boolean functions  $Y = \overline{A \cdot B \cdot C \cdot D}$  or  $Y = \overline{A} + \overline{B} + \overline{C} + \overline{D}$  in positive logic.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### LOGIC DIAGRAM



#### **FUNCTION TABLE**

(Each gate)

	(								
	INP	OUTPUT							
Α	В	C	D	Y					
Н	Н	Н	Н	Ŀ					
L	Χ	Χ	Χ	н					
×	L	Χ	Χ	Н					
Х	Χ	L	Χ	н					
X	· X	Х	L	н					

Supply Voltage Range $V_{CC}$ , $-0.5V$ to $+7V$ DC Input Diode Current. IIK
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V)$ $\pm 20 \text{ mA}$
DC Output Diode Current, $I_{OK}$ ( $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ ) $\pm 20$ mA
Continuous Output Current Per Pin, $I_0$ (-0.5V < $V_0$ < $V_{CC}$ +0.5V) ±70 mA
Continuous Current Through VCC or GND pins ±250 mA
Storage Temperature Range, $T_{stg}$ 65°C to +150°C Power Dissipation Per Package, $P_d$ <sup>†</sup> 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . . . . . . . . 4.5V to 5.5V DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . 0V to  $V_{CC}$  Operating Temperature

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . . Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T <sub>a</sub> = 25°C		KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit		
			Тур		Guaranteed Lim	its			
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	٧		
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	V		
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-4mA$	V <sub>CC</sub> 4.2	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> -0.1	V <sub>CC</sub> −0.1 3.7	v		
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v		
Maximum Input Current	l <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ		
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.0	20.0	40.0	μΑ		
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V. other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA <sub>.</sub>		

## AC ELECTRICAL CHARACTERISTICS (Input tr, tr 46 ns), HCTLS20

Characteristic	Symbol	Conditions <sup>†</sup>	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		$KS74HCTLS$ $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$	KS54 HCTLS $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$	Unit
,			Тур		Guaranteed Limits		
Maximum Propagation Delay Any Input to Y	t <sub>PLH</sub>	- CL=50pr	11	15	19	23	ns
	t <sub>PHL</sub>		11	15	19	23	
Maximum Input Capacitance	CIN		5				pF
Power Dissipation Capacitance*	C <sub>PD</sub>	(per gate)					pF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

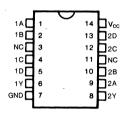


- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
   I<sub>OL</sub> = 8 mA @ V<sub>OL</sub> = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATION



#### **FUNCTION TABLE**

(Each gate)

	INP	OUTPUT		
A	В	С	D	Y
Н	Н	Н	H	Н
L	Х	X	Х	L
Х	L	X	Х	L
Х	Х	L	Х	L
Х	Х	X	L	L

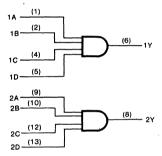
#### DESCRIPTION

These devices contain two independent 4-input AND gates. They perform the Boolean functions  $Y=A \cdot B \cdot C \cdot D$  or  $Y=\overline{A}+\overline{B}+\overline{C}+\overline{D}$  in positive logic.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### LOGIC DIAGRAM



Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V DC Input Diode Current, I <sub>IK</sub>
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, $P_d{}^{\dagger}$ 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . . . . . . . 4.5V to 5.5V DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . 0V to  $V_{CC}$  Operating Temperature

Range KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . . . Max 500 ns

\* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

#### DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	a = 25°C	KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit
	ĺ		Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> -0.1 3.7	v
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	. ±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

# AC ELECTRICAL CHARACTERISTICS (Input tr, tré6 ns), HCTLS21

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$	KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	Unit	
			Тур		Guaranteed	Guaranteed Limits		
Maximum Propagation Delay	t <sub>PLH</sub>	CL=50PF	12	18	22	27	ns	
Any Input to Y	t <sub>PHL</sub>		12	18	22	27		
Maximum Input Capacitance	CIN		5				рF	
Power Dissipation Capacitance*	C <sub>PD</sub>	(per gate)					pF	

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.



- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
   I<sub>OL</sub> = 8 mA @ V<sub>OL</sub> = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

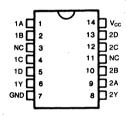
#### **DESCRIPTION**

These devices contain two independent 3-input NOR gates. gates. These gates perform the Boolean fucntions  $Y = \overline{A} + \overline{B} + \overline{C} + \overline{D}$  in positive logic. The open-drain outputs require pull-up resistors to perform correctly. They many be connected to other open-drain outputs to implement active low wired-OR or active high wired-AND functions.

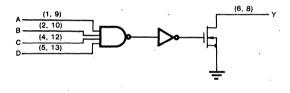
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### PIN CONFIGURATION



## LOGIC DIAGRAM



#### **FUNCTION TABLE**

(Each gate)

		, <b>J</b> ,									
	INP	UTS	OUTPUT								
A	В	С	D	Y							
Н	Н	Н	Н	L							
L	Х	Χ	Χ	н							
Х	L	Χ	Х	н							
X	Х	L	Χ.	Н							
Х	Χ	Х	L	н							

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_{I} < -0.5V \text{ or } V_{I} > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

<sup>†</sup> Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Supply Voltage, V<sub>CC</sub> . . . . . . . . . . . . 4.5V to 5.5V DC Input & Output Voltages\*, V<sub>IN</sub>, V<sub>OUT</sub> . . OV to V<sub>CC</sub> Operating Temperature

Range KS74HCTLS:  $-46^{\circ}$ C to  $+85^{\circ}$ C KS54HCTLS:  $-55^{\circ}$ C to  $+125^{\circ}$ C Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . . Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol Test Conditions		T <sub>a</sub> = 25°C		KS74HCTLS T <sub>a</sub> = -40°C to +85°C	KS54HCTLS $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	l <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Output Leakage Current	loz	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> =V <sub>CC</sub>		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

#### AC ELECTRICAL CHARACTERISTICS (Input tr. tr 46 ns), HCTLS22

Characteristic	Symbol	nbol Conditions†		25°C 5.0V	KS74 HCTLS $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	KS54 HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	Unit
			Тур		Guaranteed	Limits	
Maximum Propagation Delay	t <sub>PLH</sub>	C <sub>L</sub> =50pF	26	33	40	47	ns
Any Input to Y	t <sub>PHL</sub>		15	20	25	.30	
Maximum Input Capacitance	CIN		. 5				рF
Power Dissipation Capacitance*	C <sub>PD</sub>	(per gate)					pF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

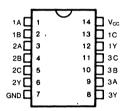


- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
  - $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5 \text{V}$
- . Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges: KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

• Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATION



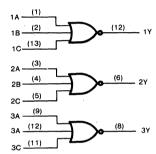
#### DESCRIPTION

These devices contain two independent 3-input NOR gates. They perform the Boolean functions  $\overline{Y=A+B+C}$  or  $Y = \overline{A} \bullet \overline{B} \bullet \overline{C}$  in positive logic.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to Vcc and ground.

#### LOGIC DIAGRAM



#### **FUNCTION TABLE**

(Each Gate)

INPUTS			OUTPUT
Α	A B C		Y
Н	Х	Х	L
X	Н	X	L
X	Χ	Н	L
L	L	L	Н

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V DC Input Diode Current, lik
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

Input Rise & Fall Times, tr, tf ..... Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

#### DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Symbol Test Conditions		a=25°C	KS74HCTLS $T_8 = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> -0.1 3.84	V <sub>CC</sub> -0.1	V
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	l <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

# AC ELECTRICAL CHARACTERISTICS (Input tr, tie6 ns), HCTLS27

Characteristic	Symbol	Conditions <sup>†</sup>	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74HCTLS T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%	KS54 HCTLS $T_a = -55$ °C to +125°C $V_{CC} = 5.0V \pm 10\%$	Unit
			Тур		Guaranteed	Limits	
Maximum Propagation Delay	t <sub>PLH</sub>	C <sub>L</sub> =50pF	11	15	19	23	ns
Any Input to Y	t <sub>PHL</sub>		13	17	22	26	113
Maximum Input Capacitance	CIN		5			-	рF
Power Dissipation Capacitance*	C <sub>PD</sub>	(per gate)					рF

<sup>\*</sup> CPD determines the no-load dynamic power dissipation: PD=CPD VCC2 f + ICC VCC.

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.



- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
  - IoL = 8 mA @ VoL = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### DESCRIPTION

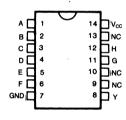
The '30 contains a single 8-input NAND gate. It performs the boolean functions (in positive logic):

 $Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H}$  $Y = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} + \overline{F} + \overline{G} + \overline{H}$ 

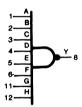
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and around.

#### PIN CONFIGURATION



#### LOGIC DIAGRAM



#### **FUNCTION TABLE**

Inputs A Through	Н	Output Y
All Inputs	Н	L
One or more inputs	L	Н

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> −65°C to +150°C
Power Dissipation Per Package, $P_d^{\dagger}$ 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Supply Voltage, V<sub>CC</sub> . . . . . . . . . . . . . . . . . 4.5V to 5.5V DC Input & Output Voltages\*, V<sub>IN</sub>, V<sub>OUT</sub> . . OV to V<sub>CC</sub> Operating Temperature

Range

KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . Max 500 ns

 Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

#### DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T <sub>a</sub> = 25°C		KS74HCTLS T <sub>a</sub> = -40°C to +85°C	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit			
			Тур		Guaranteed Limits					
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	v			
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	ý			
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> -0.1	v			
Maximum Low-Level Output Voltage	V <sub>O</sub> L	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$		0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v			
Maximum Input Current	liN	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μА			
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.0	20.0	40.0	μΑ			
Additional Worst Case Supply Current	Δlcc	per input pin  V <sub>I</sub> =2.4V  other Inputs: at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0µA		2.7	2.9	3.0	mA			

## AC ELECTRICAL CHARACTERISTICS (Input tr, tre6 ns), HCTLS30

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74HCTLS T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%	KS54HCTLS  T <sub>a</sub> = -55°C to +125°C  V <sub>CC</sub> = 5.0V ± 10%	Unit	
			Тур		Guaranteed Limits			
Propagation Delay	t <sub>PLH</sub>	C <sub>L</sub> =50pF	11	15	19	22 .	ns	
Tropagation Bolay	t <sub>PHL</sub>		11	15	19	22	]	
Input Capacitance	CIN		5				pF	
Power Dissipation Capacitance*	C <sub>PD</sub>		15				pF	

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

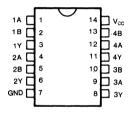


- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
   I<sub>OL</sub> = 8 mA @ V<sub>OL</sub> = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

## PIN CONFIGURATION



#### **FUNCTION TABLE**

(Each Gate)

inp	uts	Output
. А	В	Y
• Н	Х	Н
X	Н	н
L	L	L

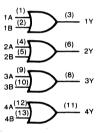
#### DESCRIPTION

These devices contain four independent 2-input OR gates. They perform the Boolean functions Y=A+B or  $Y=\overline{\overline{A}\bullet\overline{B}}$ .

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL. NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damaged due to static discharge by internal diode clamps to  $V_{\text{CC}}$  and ground.

#### LOGIC DIAGRAM



Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

	V <sub>CC</sub> 4.5V to 5.5' ut Voltages*, V <sub>IN</sub> , V <sub>OUT</sub> OV to V <sub>C</sub>	
Operating Temp	•	•
Range	KS74HCTLS: -40°C to +85°C	С
	KS54HCTLS: -55°C to +125°C	C

## DC ELECTRICAL CHARACTERISTICS (Vcc=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T <sub>a</sub> = 25°C		KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$	Unit		
			Тур		Guaranteed Limits				
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	v		
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	V.		
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH} \text{ or } V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-4\text{mA}$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> -0.1 3.84	V <sub>CC</sub> -0.1	v		
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1	V		
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> ≔V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ		
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.0	20.0	40.0	μΑ		
Additional Worst Case Supply Current	Δlcc	per input pin  V <sub>I</sub> =2.4V  other Inputs: at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA		

## AC ELECTRICAL CHARACTERISTICS (Input tr, tr 6 ns), HCTLS32

Characteristic	Symbol	mbol Conditions†		25°C KS74HCTLS $T_a = -40$ °C to +85°C $V_{CC} = 5.0V \pm 10\%$		KS54 HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	Unit		
			Тур		Guaranteed Limits				
Maximum Propagation Delay	t <sub>PLH</sub>	C <sub>L</sub> =50pF	13	17	22	26	ns		
Waximani i ropagation Belay	t <sub>PHL</sub>		13	17	22	26	113		
Maximum Input Capacitance	CIN		5				pF		
Power Dissipation Capacitance*	C <sub>PD</sub>	(per gate)	15				рF		

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.



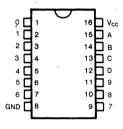
- Full decoding of Input Logic
- All outputs are High for Invalid BCD Conditions
- Also for application as 3-Line to 8-Line Decoders
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
  - IoL = 8 mA @ VoL = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- · Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATION



#### **FUNCTION TABLE**

No	Inputs					Outputs								
No.	D	С	В	Α	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н
1 1	L	L	L	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н
. 2	L	L	Н	L	Н	Н	L	Н	Н	Н	Н	Н	Н	н
3	L	L	Н	Н	Н	Н	Н	L	Н	Н	Н	Н	Н	Н
4	L	Н	L	L	Н	Н	Н	Н	L	Н	Н	Н	Н	Н
5	L	Н	L	Н	Н	Н	Н	Н	Н	L	Н	Н	Н	Н
6	L	Н	Н	L	Н	Н	Н	Н	Н	н	L	Н	Н	Н
7	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	Н	Н
- 8	Н	L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	L	Н
9	Н	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L
	Н	L	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
INVALID	Н	Н	Ļ	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
INVALID	н	٠Н	Н	L	Н	Н	Н	Η,	Н	Н	Н	Н	Η.	Н
	Н	Н	. Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н

#### DESCRIPTION

The '42 decoder accepts for active-high BCD inputs and provides 10 mutually exclusive active-low outputs, as shown by logic symbol or diagram. The active-low outputs facilitate addressing other MSI units with active-low input enables.

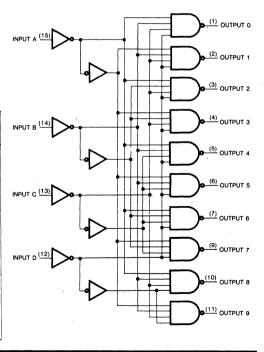
The logic design of the '42 ensures that all outputs are high when binary codes greater than nine are applied to the inputs.

The most significant input, D, produces a useful inhibit function when the '42 is used as a 1-of-8 decoder. The D input can also be used as the Data input in an 8-output demultiplexer application.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V<sub>CC</sub> and around.

#### LOGIC DIAGRAM



Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, P <sub>d</sub> <sup>†</sup> 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

\* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

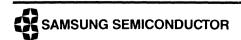
Characteristic	Symbol	Test Conditions	T	a = 25°C	KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit	
			Тур	Guaranteed Limits				
Minimum High-Level Input Voltage	· V <sub>IH</sub>			2.0	2.0	2.0	V	
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧	
Minimum High-Level Output Voltage	V <sub>QH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> -0.1	v	
Maximum Low-Level Output Voltage	Vol	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v	
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ	
Maximum Quiescent Supply Current	lcc	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μΑ	
Additional Worst Case Supply Current	Δlcc	per input pin $V_I$ =2.4V other Inputs: at $V_{CC}$ or GND $I_{OUT}$ =0 $\mu$ A		2.7	2.9	3.0	mA	

# AC ELECTRICAL CHARACTERISTICS (Input tr, tr 6 ns), HCTLS42

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74 HCTLS $T_a = -40 ^{\circ}\text{C to } +85 ^{\circ}\text{C}$ $V_{CC} = 5.0 \text{V} \pm 10 \%$	KS54 HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	Unit
			Тур	Guaranteed Limits			7 .
Maximum Propagation Delay	t <sub>PLH</sub>	C <sub>1</sub> = 50pF	19	25	32	38	ns
Any Input to Y	t <sub>PHL</sub>	OL-30pi	19	25	32	38	113
Maximum Input Capacitance	CIN		5				рF
Power Dissipation Capacitance*	C <sub>PD</sub>	(per gate)					рF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.



- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
   I<sub>OL</sub> = 8 mA @ V<sub>OL</sub> = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
   KS74HCTLS: -40°C to +85°C

KS54HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

## **DESCRIPTION**

The '51 performs the following Boolean functions:  $1Y = (1A \bullet 1B \bullet 1C) + (1D \bullet 1E \bullet 1F)$  $2Y = (2A \bullet 2B) + (2C \bullet 2D)$ 

The '58 performs:

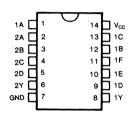
1Y=(1A•1B•1C)+(1D•1E•1F)

2Y=(2A•2B)+(2C•2D)

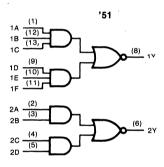
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### PIN CONFIGURATION



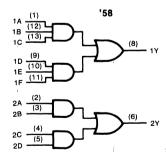
## LOGIC DIAGRAMS



#### **FUNCTION TABLES**

		Outp	ut 1Y				
1A	1B	1C	1D	1E	1F	'51	'58
Н	Н	Н	X	Х	X	L	Н
Χ	Χ,	Х	Н	н	Н	L	Н
	Any o	ther co	ombina	tion		н	L

	Inp	Outp	ut 2Y		
2A	2B	. 2C	2D	'51	'58
Н	Н	Х	Х	L	н
Χ	Х	Н	Н	L	Н
An	y other	combinati	ion	Н	L





Supply Voltage Range $V_{CC}$ , $-0.5V$ to $+7V$
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.

These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Supply Voltage, V <sub>CC</sub>	4.5V to 5.5V
DC Input & Output Voltages*, VIN, VOUT	OV to $V_{CC}$
Operating Temperature	

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . . . . Max 500 ns

#### DC ELECTRICAL CHARACTERISTICS (Vcc=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T <sub>a</sub> = 25°C		$KS74HCTLS$ $T_a = -40°C to +85°C$	KS54HCTLS $T_a = -55$ °C to +125°C	Unii	
			Тур		Guaranteed Lim	its	1	
Minimum High-Level Input Voltage	ViH			2.0	2.0	2:0	٧	
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	0.8	٧	
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	V	
Maximum Low-Level Output Voltage	V <sub>OL</sub> ^	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v	
Maximum Input Current	liN	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ	
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.0	20.0	40.0	μΑ	
Additional Worst Case Supply Current	Δlcc	per input pin  V <sub>I</sub> =2.4V  other Inputs: at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0µA		2.7	2.9	3.0	mA	

# AC ELECTRICAL CHARACTERISTICS (Input tr, tre6 ns), HCTLS51, HCTLS58

Characteristic	Symbol	bol Conditions†		25°C 5.0V	$KS74HCTLS$ $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$	KS54 HCTLS $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$	Unit
		Typ Guaranteed Limits			Limits		
Maximum Propagation Delay	t <sub>PLH</sub>	C <sub>1</sub> =50pF	13	18	23	27	ns
	t <sub>PHL</sub>	_	13	18	23	27	
Maximum Input Capacitance	C <sub>IN</sub>		5				рF
Power Dissipation Capacitance*	C <sub>PD</sub>	(per gate)	15				pF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.



 <sup>\*</sup> Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
  - $I_{OL} = 8 \text{ mA } @ V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

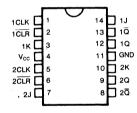
#### **DESCRIPTION**

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at  $\overline{\text{CLR}}$  input resets the outputs regardless of the levels of the other inputs. When  $\overline{\text{CLR}}$  is inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle filp-flops by tying J and K high.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

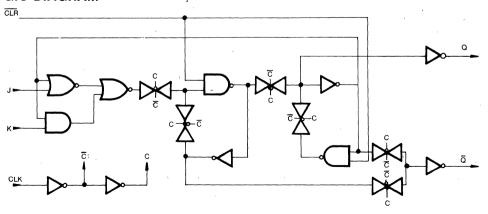
## PIN CONFIGURATION



#### **FUNCTION TABLE**

	Input	Outp	outs		
CLR	CLK	J	K	Q	Q
L.	Х	X	Х	L	. Н
Н	<b>↓</b>	L	L	Q <sub>o</sub>	Ō₀
Н	<b>↓</b>	Н	L	н	L
Н	<b>↓</b>	L	Н	L	Н
Н	<b>↓</b>	ļΗ	Н	TOG	GLE
Н	Н	X	Х	Q,	Q̄₀

#### LOGIC DIAGRAM





which permanent damage to the device may occur.

These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

## **Recommended Operating Conditions**

Supply Voltage, V <sub>CC</sub>	4.5V to 5.5V
DC Input & Output Voltages*, VIN, VOUT	OV to Vcc
Operating Temperature	

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>t</sub> . . . . . . . . . . . Max 500 ns

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	rmbol Test Conditions		<sub>a</sub> = 25°C	KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$	Uni	
			Тур		Guaranteed Lim	its		
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	v	
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	0.8	v	
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> -0.1	v	
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v	
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ	
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		4.0	40.0	80.0	μΑ	
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA	

<sup>†</sup> Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

 <sup>\*</sup> Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

# AC ELECTRICAL CHARACTERISTICS (Input tr, tr 6 ns), HCTLS73A

Characteristic		Symbol Conditions		bol Conditions $T_a = 25^{\circ}$ $V_{CC} = 5.0$		KS74HCTLS  T <sub>a</sub> = -40°C to +85°C  V <sub>CC</sub> = 5.0V ± 10%	KS54HCTLS $T_a = -55^{\circ}\text{C to } + 125^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	Unit
				Тур		Guaranteed Li	mits	
Maximum Clock Fr	equency	f <sub>max</sub>		40	30	25	21	MHz
Maximum Propagat	tion Delay,	tpLH		15	20	25	30	ns
CLK to Q or Q		tPHL	C <sub>L</sub> =50pF	15	20	25	30	""
Maximum Propagat	Maximum Propagation Delay,			15	20	25	30	ns
CLR to Q or Q	•	tpHL	PHL	15	20	25	30	113
Minimum Setup	J or K			10	13	17	20	ns
Time before CLK↓	CLR Inactive	t <sub>su</sub>		10	13	17	20	113
Minimum Hold Tim J or K after CLK↓	e,	th		-3	0	0	O,	ns
Minimum Pulse	CLK High of Low	tw		10	13	17	20	ns
Width	CLR Low	·w		10	13	17	20	'''3
Maximum Input Capacitance		CiN		5				pF
Power Dissipation	Capacitance*	C <sub>PD</sub>	(per flip-flop)	40		,		рF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
  - IOL = 8 mA @ VOL = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
   KS74HCTLS: -40°C to +85°C
   KS54HCTLS: -55°C to +125°C
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

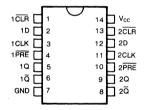
#### DESCRIPTION

These devices contain two independent positive-edge-triggered D-type flip-flops. Each flip-flop has its own data, clock, preset and clear inputs and complementary Q and  $\overline{Q}$  outputs. The preset and clear inputs are active-low and operate independently of the clock. Data at the D input is transferred to the Q outputs on the positive transition of the clock, provided setup requirements have been met.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### PIN CONFIGURATION

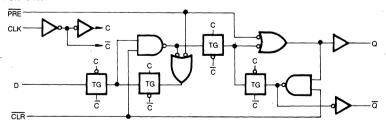


## **FUNCTION TABLE**

	inpu	-	Outputs			
PRE	CLR	CLK	D	Q	Q	
L	Н	X	X	Н	L	
Н	L	Χ	X	L	Н	
Ĺ	L	Χ	Χ	Н*	H*	
Н	Н	<b>↑</b>	Н	Н	L	
Н 1	Н	<b>↑</b>	L	L	Н	
Н	Н	L	X	No Ch	nange	
Н	Н	Н	Х	No Ch	nange	
Н	н .	<b>↓</b>	Х	No Ch	nange	

\*Both outputs will remain high as long as PRE and CLR are low, but the output states are unpredictable if PRE and CLR go high simultaneously.

## **LOGIC DIAGRAM**



# Dual D-Type Positive-Edge-Triggered Flip-Flops with Preset and Clear

## **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ m/s}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ m/s}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW

<sup>\*</sup> Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

## **Recommended Operating Conditions**

		-		
Supply Voltage, Vo	<b>c</b>	4	1.5V to \$	5.5V
DC Input & Output	Voitages*, V <sub>IN</sub> ,	$V_{\text{OUT}}$ .	. 0V to	Vcc
Operating Temperat	ture			
Range	KS74HCTLS:	-40°	C to +8	5°C

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . Max 500 ns

# DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	<sub>a</sub> = 25°C	KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS $T_a = -55$ °C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1	v
Maximum Input Current	l <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		4.0	40.0	80.0	μΑ
Additional Worst Case Supply Current	ΔÍcc	per input pin $V_1=2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

<sup>†</sup> Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

# AC ELECTRICAL CHARACTERISTICS (Input tr, tre6 ns), HCTLS74A

Characteristic						T <sub>a</sub> = -40°C to +85°C	KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> =5.0V± 10%	Unit
				Тур		Guaranteed Li	mits	
Maximum Clock Fr	equency	f <sub>max</sub>		40	30	25	20	MHz
Maximum Propagat	tion Delay,	tpLH		18	25	31	37	ns
CLK to Q or Q		tpHL	PHL CL=50pF		40	50	60	113
Maximum Propagation Delay,		t <sub>PLH</sub>		18	25	31	37	ns
PRE or CLR to Q	or Q	t <sub>PHL</sub>	1	30	40	50	60	113
Minimum Setup	Data	t <sub>su</sub>		10	13	17	20	ns
Time before CLK↑	PRE or CLR Inactive	<sup>L</sup> Su		10	13	17	20	113
Minimum Hold Time, J or K after CLK↓		t <sub>h</sub>		-3	0	0	0	ns
Minimum Pulse CLK High or Low		tw		8	15	20	25	ns
Width	PRE or CLR Low	-tw		8	15	20	25	113
Maximum Input Capacitance		CIN		5				pF
Power Dissipation Capacitance*		C <sub>PD</sub>	(per flip-flop)	40				pF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

- . Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  $I_{OL} = 8mA @ V_{OL} = 0.5V$
- . Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges: KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

## DESCRIPTION

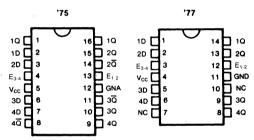
The '75 and '77 consist of 4 high-speed D-type latches that can be used as temporary storage for binary information between processing units. The '75 features complementary Q and Q output while the '77 features single nail output. These devices are ideal for high component density application.

The latches are transparent: when the enable (E) is high. the Q output will follow the data input. When the enable goes low, the output latches at the level that was set up at the D-input.

These device provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V<sub>CC</sub> and around.

#### PIN CONFIGURATION

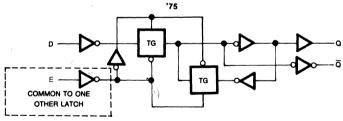


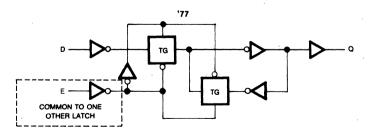
#### **FUNCTION TABLE**

Inp	uts	Outputs		
D	Ε	a	۵٠	
L	Н	L	Н	
н	Н	н	L,	
Х	L	Qo	$\overline{\mathbf{Q}}_{0}$	

\*Q: '75 only

# LOGIC DIAGRAM





Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_0 < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW

<sup>\*</sup> Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Supply Voltage, V<sub>CC</sub> . . . . . . . . . . . . . . . . . 4.5V to 5.5V DC Input & Output Voltages\*, V<sub>IN</sub>, V<sub>OUT</sub> . . OV to V<sub>CC</sub> Operating Temperature

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . Max 500 ns \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	a = 25°C	KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$	Unit
			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8 .	0.8	v
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH} \text{ or } V_{IL}$ $I_{O}=-20\mu\text{A}$ $I_{O}=-4\text{mA}$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> -0.1	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	lın	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input in  V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

## AC ELECTRICAL CHARACTERISTICS (Input tr, tre6 ns), HCTLS75

Characteristic	Symbol			25°C 5.0V	KS74HCTLS T <sub>s</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%	KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> =5.0V± 10%	Unit
			Тур		Guaranteed	Limits	
Propagation Delay,	tpLH	C <sub>1</sub> = 50pF	19	25	31	38	ns
E to Q or Q	t <sub>PHL</sub>	OL-30pi	19	25	31	38	
Propagation Delay,	t <sub>PLH</sub>	C <sub>1</sub> = 50pF	13	21	26	32	ns
D to Q or Q	t <sub>PHL</sub>	CL-20bi	13	21	26	32	
Data Set up Time D to E	tsu		15	20	25	30	ns
Data Hold Time E to D	th		4	5	6	. 8	ns
Input Capacitance	CIN		5			,	pF
Power Dissipation Capacitance*	C <sub>PD</sub>						pF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

## AC ELECTRICAL CHARACTERISTICS (Input tr, tres ns), HCTLS77

Characteristic	Symbol	mbol Conditions†		25°C 5.0V	$KS74HCTLS$ $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$	KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	Unit
			Тур		Guaranteed	Limits	
Propagation Delay,	tpLH	C <sub>1</sub> = 50pF	13	18	23	27	ns
E to Q	tpHL	OL-30bi	13	18	23	27	
Propagation Delay,	ŧ <sub>PLH</sub>	C <sub>1</sub> = 50pF	13	18	23	27	ńs
D to Q or Q	t <sub>PHL</sub>	CL-30bi	13	18	25	27	113
Data Set up Time D to E	tsu		15	20	25	30	ns
Data Hold Time E to D	th		4	5	6	. 8	ns
Input Capacitance	CiN		5				pF
Power Dissipation Capacitance*	C <sub>PD</sub>				,		pF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
   I<sub>OL</sub> = 8 mA @ V<sub>OL</sub> = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
   KS74HCTLS: -40°C to +85°C
   KS54HCTLS: -55°C to +125°C
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### **DESCRIPTION**

These parts consist of two negative-edge-triggered J-K flip-flops with independent J, K, preset, clear and clock inputs and complementary outputs. The J-K inputs at each flip-flop are enabled when the clock goes high. The input data are transferred to the outputs on the negative-going edge of the clock pulse, provided the setup requirements have been met.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### PIN CONFIGURATION

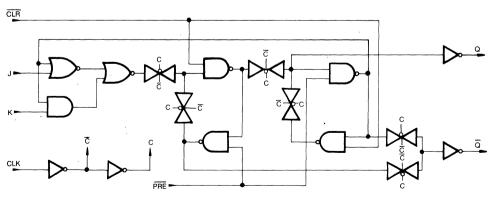
		<del>\ \ \</del>			
1CLK	1	$\overline{}$	16		1K
1PRE	2		15		1Q
1CLR	3.		14		1Q
1J 🗀	4	*	13		GND
V <sub>cc</sub>	5		12		2K
2CLK	6		11		2Q
2PRE	7		10		2Q
2CLR	8		9	口	2J
	L			i	

## **FUNCTION TABLE**

Inputs					Outputs		
PRE	CLR	CLK	J	K	Q	ā	
L	Н	Χ	Х	Х	Н	L	
Н	L	X	Χ	Χ	L	Н	
L	L	X	Χ	Χ	H*	Н٠	
H	Н	<b>↓</b>	L	L	$Q_0$	$\overline{Q}_0$	
Н	Н	<b>↓</b>	Н	L	Н	L	
H	Н	<b>↓</b>	L	Н	L	Η·	
Н	Н	<b>↓</b>	Н	Н	TOG	TOGGLE	
Н	Н	Н	Χ	Χ	Q <sub>0</sub>	$\overline{Q}_{0}$	

\*Both outputs will remain high as long as preset and clear are low, but the output states are unpredictable if preset and clear go high simultaneously.

## LOGIC DIAGRAM



Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
Vcc or GND pins ±125 mA
Storage Temperature Range, $T_{stg}\ldots -65^{\circ}\text{C}$ to $+150^{\circ}\text{C}$
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.

These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

## **Recommended Operating Conditions**

Supply Voltage	, V <sub>CC</sub> 4.5V to 5.5V
DC Input & Ou	tput Voltages*, $V_{IN},\ V_{OUT}$ $OV$ to $V_{CC}$
Operating Temp	perature
Range	KS74HCTLS: -40°C to +85°C
	KS54HCTLS: -55°C to +125°C

Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . . Max 500 ns

\* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

Characteristic	Symbol	Test Conditions	T <sub>a</sub> = 25°C		KS74HCTLS T <sub>a</sub> = -40°C to +85°C	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit
,			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	v
Maximum Low-Level Input Voltage	VIL			0.8	0.8	. 0.8	V
Minimum High-Level Output Voltage	V <sub>OH</sub>	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> =-20μA I <sub>O</sub> =-4mA	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	l <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μА
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		4.0	40.0	80.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

<sup>†</sup> Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## AC ELECTRICAL CHARACTERISTICS (Input tr, tre6 ns), HCTLS76A

Characteristic		Symbol	Conditions <sup>†</sup>	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		$KS74HCTLS$ $T_a = -40 °C to +85 °C$ $V_{CC} = 5.0V \pm 10 %$	KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> =5.0V ± 10%	Unit
				Тур	yp Guaranteed Limits			
Maximum Clock Fr	equency	f <sub>max</sub>		40	30	25	21	MHz
Maximum Propagat	ion Delay,	tpLH		15	20	25 .	30	ns
CLK to Q or Q		t <sub>PHL</sub>	C <sub>L</sub> =50pF	15	20	25	30	115
Maximum Propagat	Maximum Propagation Delay,			15	20	25	30	ns
PRE or CLR to Q	or Q	t <sub>PHL</sub>		15	20	25	30	1113
Minimum Setup	Data	t <sub>su</sub> '		10	13	17	20	ns
Time before CLK↓	PRE or CLR Inactive	Lsu e		10	13	17	20	1 IIS
Minimum Hold Time, J or K after CLK↓		t <sub>h</sub>		-3	0	0	0	ns
Minimum Pulse	CLK High or Low	+		10	13	17	20	ns
Width	PRE or CLR Low	t <sub>w</sub>		10	13	17	20	115
Maximum Input Capacitance		CIN		5				pF
Power Dissipation	Capacitance*	C <sub>PD</sub>	(per flip-flop)	40				pF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} \ V_{CC}^2 \ f + I_{CC} \ V_{CC}$ .
† For AC switching test circuits and timing waveforms see section 2.

- . Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
- IOL = 8 mA @ VOL = 0.5V
- . Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- · Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

• Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

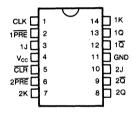
#### DESCRIPTION

These parts consist of two negative-edge-triggered J-K flipflops with independent J, K and preset inputs and complementary outputs. The clear and clock inputs are common to both flip-flops. The J-K inputs are enabled when the clock goes high. The input data are transferred to the outputs on the negative-going edge of the clock pulse, provided the setup requirements have been met.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V<sub>CC</sub> and ground.

#### PIN CONFIGURATION

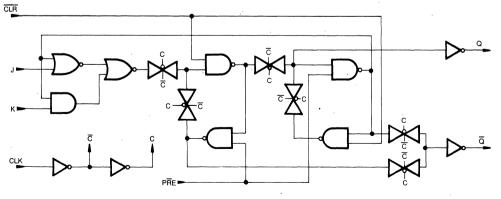


#### **FUNCTION TABLE**

	Ír		Out	puts		
PRE	CLR	ÇLK	J	K	Q	ā
L	Н	Х	Х	Х	Н	L
Н	L	Χ	Χ	X	L	Н
L	L	Х	Χ	Х	H•	Н٠
н	н	<b>+</b>	L	L	Qo	$\overline{Q}_{o}$
Н	Н	<b>↓</b>	Н	L.	Н	L
Н	Н	1	L	н	L	Н
Н	Н	<b>↓</b>	Н	Н	TOG	GLE
Н	Н	Н	Χ	Х	Qo	$\overline{Q}_{0}$

\*Both outputs will remain high as long as preset and clear are low, but the output states are unpredictable if preset and clear go high simultaneously.

#### LOGIC DIAGRAM



Supply Voltage Range $V_{CC}$ , $-0.5V$ to $+7V$
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur

These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C Input Rise & Fall Times,  $t_r, t_f$  . . . . . . Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

Characteristic	Symbol	Symbol Test Conditions		a = 25°C	KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	Vıн			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		4.0	40.0	80.0	μΑ
Additional Worst Case Supply Current		per input pin $V_1=2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

## AC ELECTRICAL CHARACTERISTICS (Input tr., tre6 ns), HCTLS78A

Characteristic		Symbol	Conditions <sup>†</sup>	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74HCTLS $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 5.0V \pm 10\%$	KS54HCTLS $T_a = -55^{\circ}\text{C to } + 125^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	Unit
				Тур	Guaranteed Limits			
Maximum Clock F	requency	f <sub>max</sub>		40	30	25	21	MHz
Maximum Propaga	Maximum Propagation Delay,			15	20	25	30	ns
CLK to Q or Q		t <sub>PHL</sub>	C <sub>L</sub> =50pF	15	20	25	30	ns
Maximum Propagation Delay,		tpLH		15	20	25	30 .	
PRE or CLR to Q	or Q	t <sub>PHL</sub>		15	20	25	30	115
Minimum Setup	J or K	t <sub>su</sub>		10	13	17	20	ns
Time before CLK↓	PRE or CLR Inactive			10	13	17	· 20	113
Minimum Hold Time, J or K after CLK↓		th		-3	0	0	0	ns
Minimum Pulse	CLK High or Low	tw		10	13	17	20	ne
Width	PRE or CLR Low	· w		10	13	17	20	ns
Maximum Input Capacitance		CIN		5			,	рF
Power Dissipation	Capacitance*	C <sub>PD</sub>	(per flip-flop)	40				рF

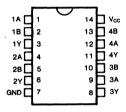
<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} \ V_{CC}^2 \ f + I_{CC} \ V_{CC}$ .
† For AC switching test circuits and timing waveforms see section 2.

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs: I<sub>OL</sub> = 8 mA @ V<sub>OL</sub> = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
   KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATION



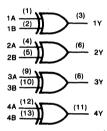
#### **DESCRIPTION**

These devices contain four independent 2-input Exclusive-OR gates. They perform the Boolean functions  $Y = A \oplus B$  or  $Y = \overline{A}B + A \overline{B}$ .

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### LOGIC DIAGRAM



#### **FUNCTION TABLE**

#### (Each Gate)

Inp	uts	Output
A	В	Y
L	L	L
L	Н	` Н
Н	L	н
Н	Н	L

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(\neg 0.5V < V_0 < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
Vcc or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW
* Absolute Maximum Ratings are those values beyond

<sup>\*</sup> Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Supply Voltage,	Vcc	4	.5V to 5.5V
DC Input & Out	put Voltages*, V <sub>IN</sub> ,	Vout .	. OV to Vcc
Operating Temp	erature		
Range	KS74HCTLS:	-40°0	to +85°C

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . Max 500 ns

Characteristic	Symbol	bol Test Conditions		= 25°C	KS74HCTLS T <sub>a</sub> = -40°C to +85°C	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	v
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> -0.1 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	lin	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

## AC ELECTRICAL CHARACTERISTICS (Input tr, tre6 ns), HCTLS86

Characteristic	Symbol	Conditions <sup>†</sup>	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74 HCTLS $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	KS54 HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	Unit
			Тур	Limits			
Maximum Propagation Delay,	tpLH	C <sub>L</sub> =50pF	15	20	25	30	ns ns
A or B to Y (Other Input Low)	t <sub>PHL</sub>		15	20	25	30	
Maximum Propagation Delay,	t <sub>PLH</sub>		18	25	31	37	
A or B to Y (Other Input High)	t <sub>PHL</sub>		18	25	31	37	
Maximum Input Capacitance	CiN		5				pF
Power Dissipation Capacitance*	C <sub>PD</sub>	(per gate)	15				pF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current Outputs: IoL = 8mA @ Vol = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
   KS74HCTLS: -40°C to +85°C
   KS54HCTLS: -55°C to +125°C
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

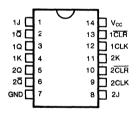
#### DESCRIPTION

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the  $\overline{\text{CLR}}$  input resets the outputs regardless of the levels of the other inputs. When  $\overline{\text{CLR}}$  is inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

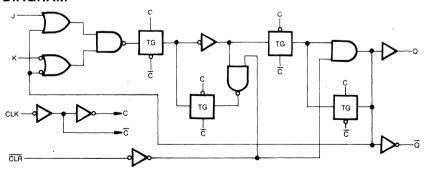
#### PIN CONFIGURATION



#### **FUNCTION TABLE**

	Input	Out	outs		
CLR	CLK	J	K	Q	ā
L	Х	Х	·X	L	Н
Н	<b>↓</b>	L	L	$Q_o$	<b>Q</b> ₀
Н -	<b>↓</b>	Н	L	Н	L.
Н	<b>↓</b>	Ļ	Н	L	. H -
H	<b>↓</b>	Н	H,	TOG	GLE
Н	Н	X	x	Q <sub>o</sub>	Q₀

#### LOGIC DIAGRAM



## KS54HCTLS 107A KS74HCTLS

# Dual J-K Negative-Edge-Triggered Flip-Flops with Clear

## **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pat 500 mW

<sup>\*</sup> Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

		•
Supply Voltage, 1	<b>√</b> cc	4.5V to 5.5V
DC Input & Outp	ut Voltages*, V <sub>IN</sub> ,	$V_{OUT}$ OV to $V_{CC}$
Operating Tempe	rature	
Range	KS74HCTLS:	-40°C to +85°C
	KS54HCTLS:	-55°C to +125°C
Input Rise & Fall	Times, t <sub>r</sub> , t <sub>f</sub>	Max 500 ns

 <sup>\*</sup> Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

Characteristic	Symbol	Test Conditions	T <sub>a</sub> = 25°C		KS74HCTLS KS54HCTLS T <sub>a</sub> = -40°C to +85°C T <sub>a</sub> = -55°C to +125°		
			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		4.0	40.0	80.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

## AC ELECTRICAL CHARACTERISTICS (Input tr., tre6 ns), HCTLS107A

Characteristic		Symbol	mbol Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74HCTLS $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 10^{\circ}\text{M}$	to +85°C T <sub>a</sub> = -55°C to +125°C		
				Тур		Guaranteed Li	mits		
Maximum Clock Fr	equency	f <sub>max</sub>	,	40	30	25	21 .	MHz	
Maximum Propaga	tion Delay,	tpLH		15	20	25	30		
CLK to Q or Q		tpHL	C <sub>L</sub> =50pF	15	20	25	30	ns	
Maximum Propagation Delay,		tpLH		15	20	25	30	ns	
CLR to Q or Q				15	20	25	30	113	
Minimum Setup	Minimum Setup J or K			10	13	17	20	ns	
Time before CLK↓	CLR Inactive	t <sub>su</sub>		10	13	17	. 20	113	
Minimum Hold Time, J or K after CLK↓		t <sub>h</sub>		-3	0	. 0	0	ns	
Minimum Pulse CLK High or Low		tw		10	13	17	20	ns	
Width	CLR Low	·w		10	13	17	20	115	
Maximum Input Capacitance		CIN		5				рF	
Power Dissipation	Capacitance*	CPD	(per flip-flop)	40				pF∙	

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current Outputs: lo = 8mA @ Vo = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

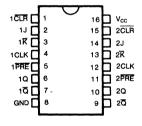
#### DESCRIPTION

These devices contain two positive-edge-triggered J- $\overline{K}$  flipflops with independent preset and clear inputs and complementary Q and  $\overline{Q}$  outputs. The present and clear inputs are active-low and operate independently of the clock Data at the J and  $\overline{K}$  inputs are transferred to the ouptuts on the positive transition of the clock provided setup requirements have been met. These versatile flip-flops can perform as toggel flip-flops by grounding  $\overline{K}$  and tying J high. They can also perform as D-type flops if J and  $\overline{K}$  are tied together.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

## PIN CONFIGURATION

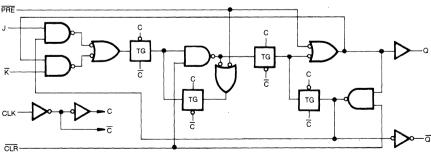


#### **FUNCTION TABLE**

	li	nputs			Outputs		
PRE	CLR	CLK	J	ĸ	Q	Q	
L	Н	Х	Х	Х	Н	L	
Н	L	Х	Х	Х	L	Н	
L	L	Χ	Х	Х	H*	H*	
Н	Н	<b>†</b>	L	L	L	Н	
н	Н	<b>†</b>	Н	L	TOG	GLE	
H	Н	<b>†</b>	Ľ	Н	Q <sub>o</sub>	ā.	
н	н	<b>↑</b>	Н	Н	Н	L	
Н	Н	L	X	Х	Q <sub>o</sub>	ā,	

\*Both outputs will remain high as long as <u>PRE</u> and <u>CLR</u> are low, but the output states are unpredictable if <u>PRE</u> and <u>CLR</u> go high simultaneously.

#### LOGIC DIAGRAM



# Dual J-K Positive Edge-Triggered Flip-Flops with Preset and Clear

## **Absolute Maximum Ratings\***

Supply voltage Hange $V_{CC}$ ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pdf 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Supply Voltage, V <sub>CC</sub>	4.5V to 5.5V
DC Input & Output Voltages*, V <sub>IN</sub> , V <sub>OUT</sub>	
Operating Temperature	00 10 000
Operating reinperature	•

 \*/Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

Characteristic	Symbol	Test Conditions	T,	<sub>a</sub> = 25°C	KS74HCTLS T <sub>a</sub> = -40°C to +85°C	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VıL			0.8	0:8	0.8	٧
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> -0.1	v
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		4.0	40.0	80.0	μΑ
Additional Worst Case Supply Current	ΔΙσο	per input pin  V <sub>I</sub> =2.4V  other Inputs: at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0µA		2.7	2.9	3.0	mA ·



## AC ELECTRICAL CHARACTERISTICS (Input tr, tr 66 ns), HCTLS109A

Characteristic		Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74HCTLS $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 5.0V \pm 10\%$	KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> =5.0V ± 10%	Unit	
				Тур		Guaranteed Li	mits		
Maximum Clock Fr	equency	f <sub>max</sub>		40	30	25	20	MHz	
Maximum Propaga	tion Delay,	tplH		18	25	31	37	ns	
CLK to Q or Q		t <sub>PHL</sub>	C <sub>L</sub> =50pF	30	40	50	60	1115	
Maximum Propaga	Maximum Propagation Delay,			18	25	31	37	ns	
PRE or CLR to Q	or Q	t <sub>PHL</sub>		30	40	50	60	113	
Minimum Setup	Minimum Setup Data		,	10	13	17	20	ns	
	PRE or CLR Inactive	t <sub>su</sub>		10	13	17	20	1115	
Minimum Hold Time, Data after CLK↓		th		-3	0	0	.0	ns	
Minimum Pulse CLK High or Low PRE or CLR Low		tw		8	15	20	25	ns	
		] •w		8	15	20	25		
Maximum Input Capacitance		'C <sub>IN</sub>		5				pF	
Power Dissipation Capacitance*		C <sub>PD</sub>	(per flip-flop)	40				pF	

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} \ V_{CC}^2 \ f + I_{CC} \ V_{CC}$ .
† For AC switching test circuits and timing waveforms see section 2.

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current Outputs:
   IoL = 8mA @ Vol = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
   KS74HCTLS: -40°C to +85°C

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

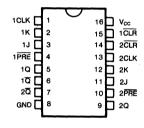
#### **DESCRIPTION**

These parts consist of two negative-edge-triggered J-K flipflops with independent J, K, preset, clear and clock inputs and complementary outputs. The J-K inputs at each flipflop are enabled when the clock goes high. The input data are transferred to the outputs on the negative-going edge of the clock pulse, provided the setup requirements have been met.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### PIN CONFIGURATION

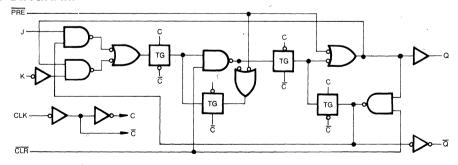


#### **FUNCTION TABLE**

	li		Out	outs		
PRE	PRE CLR		J	K	a	Q
L	Н	X	X	Х	Н	L
Н	L	Χ	Х	X	L	н
L	L	ΧÍ	X	X	H*	H*
Н	Η.	<b>↓</b>	L	L	Q <sub>o</sub>	H* Q₀
Н	Н	<b>↓</b>	Н	L	н	L
н	Н	<b>↓</b>	L	H	L	Н
Н	Η '	<b>↓</b>	Н	Н	TOG	GLE
Н	, H	н	Х	Х	Q <sub>o</sub>	$\overline{Q}_{o}$

\*Both outputs will remain high as long as  $\overline{PRE}$  and  $\overline{CLR}$  are low, but the output states are unpredictable if  $\overline{PRE}$  and  $\overline{CLR}$  go high simultaneously.

#### LOGIC DIAGRAM



Supply Voltage Range $V_{CC}$ , $-0.5V$ to $+7V$
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, $T_{stg}\ldots$ $-65^{\circ}\text{C}$ to $+150^{\circ}\text{C}$
Power Dissipation Per Package, $P_d{}^\dagger$ 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-
posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . . . . . . . 4.5V to 5.5V DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . OV to  $V_{CC}$  Operating Temperature

Page KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

Characteristic	Symbol	Test Conditions	Т,	<sub>a</sub> = 25°C	KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	V
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	l <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		4.0	40.0	80.0	μΑ
Additional Worst Case Supply Current	Δl <sub>CC</sub>	per input pin V <sub>i</sub> =2.4V other inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

## AC ELECTRICAL CHARACTERISTICS (Input tr, tres 6 ns), HCTLS112A

Characteristic		Symbol	Conditions <sup>†</sup> /	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74HCTLS $T_a = -40$ °C to +85°C $V_{CC} = 5.0V \pm 10$ %	KS54HCTLS T <sub>e</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	Unit
				Тур		Guaranteed	Limits	
Maximum Clock Fr	equency	f <sub>max</sub>		40	30	25	21	MHz
Maximum Propaga	tion Delay,	t <sub>PLH</sub>		15	20	25	30	
CLK to Q or Q		t <sub>PHL</sub>	C <sub>L</sub> =50pF	15	20	25	30	ns
Maximum Propaga	Maximum Propagation Delay, CLR to Q or Q			15	20	25	30	ns
CLR to Q or Q				15	20	25	30	"
Minimum Setup	J or K	tsu		10	13	17	20	ns
Time before CLK↓	CLR Inactive	'Su		10	13	17	20	113
Minimum Hold Time,		t <sub>h</sub>	,	-3	0	0	0	ns
Minimum Pulse	CLK High or Low	tw		10	13	17	20	ns
Width	PRE or CLR Low	·w		10	13	17	20	113
Maximum Input Ca	Maximum Input Capacitance			5				pF
Power Dissipation	Capacitance*	C <sub>PD</sub>	(per flip-flop)	40				рF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

# KS54HCTLS 121 KS74HCTLS

Monostable Multibrators with Schmitt-Trigger Inputs

**Preliminary Specifications** 

#### **FEATURES**

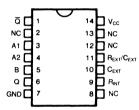
- · Schmitt-trigger for slow Input transitions
- Internal timing resistor
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
  - Ioi = 8 mA @ Voi = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range; 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

## PIN CONFIGURATION



#### **FUNCTION TABLE**

	Inputs		Out	puts
<b>A</b> 1	A2	В	Q	ā
L	Х	Х	L	Н
X	L	Н	L	Н
· X	X	L	L	Н
Н	Н	X	L	Н
н	↓ ↓	Н	7	T
. ↓	н	Н	J	L
↓	↓ ↓	Н	Λ.	L
L	×	1	V	Ъ
X	L	1	T	工

H= HIGH Voltage level

L= LOW voltage level

X= Don't care

↑= LOW-to-HIGH transition

↓= HIGH-to-LOW transition

#### DESCRIPTION

These multivibrators feature dual negative-transitiontriggered inputs and a single positive-transition-triggered input which can be used as an inhibit input. Complementary output pulses are provided.

Pulse triggering occurs at particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry for the B input allows jitterfree triggering from inputs with transition rates as slow as 1 volt/second, providing the circuit with excellent noise immunity.

Once fired, the outputs are independent of further transitions of the inputs and are a function only of the timing components. Input pulses may be of any duration relative to the output pulse. Output pulse length may be varied from 40 nanoseconds to 28 seconds by choosing appropriate timing components. With no external timing components (i.e., R<sub>INT</sub> connected to V<sub>CC</sub>, C<sub>EXT</sub> and C<sub>EXT</sub>/C<sub>EXT</sub> open), an output pulse of typically 30 or 35 nanoseconds is achieved which may be used as a d-c triggered reset signal.

Pulse width stability is achieved through internal compensation and is virtually independent of  $\dot{V}_{CC}$  and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

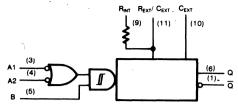
Jitter-free operation is maintained over the full temperature and  $V_{CC}$  ranges for more than six decades of timing capacitance (10 pF to  $10\mu F)$  and more than one decade of timing resistance (2 k $\Omega$  to 40 k $\Omega$ ). Throughout these ranges, pulse width is defined by the relationship  $t_{w(out)} = C_{EXT}R_{EXT} \ In2 = 0.7 \ C_{EXT} \ R_{EXT}.$  In circuits where pulse cutoff is not critical, timing capacitance up to  $1000\mu F$  and timing resistance as low as  $1.4\ k\Omega$  may be used. Also, the range of jitter-free output pulse widths is extended if  $V_{CC}$  is held to 5 volts and free-air temperature is  $25^{\circ}$  C. Duty cycles as high as 90% are achieved when using maximum recommended  $R_{EXT}.$  Higher duty cycles are available if a certain amount of pulse-width jitter is allowed.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts any yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{\text{CC}}$  and ground.

# Monostable Multibrators with Schmitt-Trigger Inputs

#### LOGIC DIAGRAM



- Notes: 1. An external capacitor may be connected between CEXT (positive) and REXT/CEXT.
  - To use the internal timing resistor, connect R<sub>INT</sub> to V<sub>CC</sub>. For Improved pulse width accuracy and repeatability connect on external resistor between R<sub>EXT</sub>/C<sub>EXT</sub> V<sub>CC</sub> with R<sub>INT</sub> opencircuited.

## **Absolute Maximum Ratings\***

† Power Dissipation temperature derating: Plastic Package(N): -12mW/°C from 65°C to 85°C Ceramic Package(J): -12mW/°Cfrom100°C to 125°C

## **Recommended Operating Conditions**

Supply Voltage	, V <sub>CC</sub> 4.5V to 5.5V
DC Input & Out	put Voltages*, VIN, VOUT OV to VCC
Operating Temp	
Range	KS74HCTLS: -40°C to +85°C
	KS54HCTLS: -55°C to +125°C

Characteristic	Symbol	Test Conditions	T,	a = 25°C	KS74HCTLS T <sub>a</sub> = -40°C to +85°C	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	VIL '			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	V
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	lin	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	Icc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	. 160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input in V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

## AC ELECTRICAL CHARACTERISTICS (Input tr., tr≤6 ns), HCTLS121

Characteristic	Symbol	Conditions†	_	25°C = 5.0V	Ta = -40°0	HCTLS C to +85°C DV ±10%	T <sub>a</sub> = -55°C	HCTLS to +125°C IV ± 10%	Unit
		$C_L = 50pF$	Min	Max	Min	Max	Min	Max	
Propagation Delay	t <sub>PLH</sub>	C <sub>L</sub> =50pF		70		87		105	ns
A, B to Q, Q	t <sub>PHL</sub>	C <sub>ext</sub> =80pF		70		87		105	
Propagation Delay	t <sub>PLH</sub>	R <sub>int</sub> to V <sub>CC</sub>		55		68		82	ns
B to Q & Q output	t <sub>PHL</sub>			55		68		82	110
Minimum Output pulse width	t <sub>w</sub>	C <sub>ext</sub> =0pF R <sub>int</sub> to V <sub>CC</sub>	20	50		52		52	ns
		C <sub>ext</sub> =80pF R <sub>int</sub> to V <sub>CC</sub>	70	150		156		156	ns
Output pulse width	t <sub>w</sub>	C <sub>ext</sub> =100pF R <sub>ext</sub> =10k <b>Ω</b>	630	770	602	798	595	805	ns
		$C_{\text{ext}} = 1 \mu F$ $R_{\text{ext}} = 10 k \Omega$	6.3	7.7	6.0	8	5.9	8.1	ns
Minimum input pulse width to trigger	t <sub>w</sub>		50		63		75		ns
External timing tesistor range	R <sub>ext</sub>		1.4	40	1.4	40	1.4	40	kΩ
External timing capacitance range	C <sub>ext</sub>		0	1,000	0	1,000	0	1,000	μF
Output Duty cycle		$R_{ext}=2k\Omega$		67		67		67	%
		R <sub>ext</sub> =R <sub>ext(max)</sub>		90		90		90	%
Input Capacitance	Cin								рF
Power dissipation Capacitance	C <sub>PD</sub>			1					

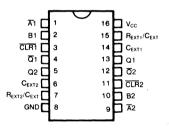
<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} \ V_{CC}^2 \ f + I_{CC} \ V_{CC}$ .
† For AC switching test circuits and timing waveforms see section 2.

- Simple pulse width formula tw = 0.45RC
- . DC triggered from active HIGH or active Low inputs
- Retriggerable for very long output pulses up to 100% duty cycle
- . Overriding clear terminates output pulse
- Schmitt trigger A & B inputs allow infinite rise and fall times on these inputs
- Functions, pin-out, speed and drive compativility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High drive current outputs: I<sub>OL</sub> = 8mA @ V<sub>OL</sub> = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATION



#### **DESCRIPTION**

The '123 contains dual retriggerable monostable multivibrators with output pulse width control by three methods.

The basic pulse time is programmed by selection of an external resistor (Rext) and capacitor (Cext). The external resistor and capacitor are normally connected as shown timing component.

Once triggered, the basic output pulse width may be extended by retriggering the gated active Low going edge input (Ai) or the active HIGH going edge input (Bi). By repeating this process, the output pulse period (nQ=HIGH, n $\overline{\rm Q}$ =LOW) can be made as long as desired. Alternatively an output delay can be terminated at any time by a Lowgoing edge on input CLR, which also inhibits the triggering. An internal connection from CLR to the input gates makes it possible to trigger the circuit by a positive-going signal at input CLR as shown in the function table when CEXT>10nF, the typical output pulse width is defined as; tw=0.45×REXT $\times$ CEXT(typ).

Where  $t_w$  is in seconds. R is in ohm. and C is in fards. All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### **FUNCTION TABLE**

		Inputs	Out	puts	
	CLR	Ā	В	Q	Q
	L	Х	Х	L	Н
1	Х	н	Х	L	н
l	X	Х	L	L	н
١	Н	L	1	Л	U
1	Н	. ↓	Н	Л	T
1	<b>↑</b>	L	Н	J.	T

H= HIGH voltage level

L= LOW voltage level

X= don't care

↑= LOW to HIGH transition

↓= HIGH to LOW transition

\_\_= one HIGH level output pulse

T= one LOW level output pulse



Supply Voltage Range $V_{CC}, \dots -0.5V$ to $+7V$ DC Input Diode Current, $I_{IK}$
(V <sub>I</sub> <-0.5V or V <sub>I</sub> >V <sub>CC</sub> +0.5V) ±20 mA
DC Output Diode Current, IOk
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous OUtput Current Per Pin, Io
(-0.5V <v<sub>0<v<sub>CC+0.5V) ±35 mA</v<sub></v<sub>
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> -65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.
posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package(N): -12mW/°C from 65°C to 85°C Ceramic Package(J): -12mW/°Cfrom100°C to 125°C

## **Recommended Operating Conditions**

Supply Voltage, V	'cc	4.5V to 5.5V
		Vour OV to Vcc
Operating Temper	ature	
Range	KS74HCTLS: -	-40°C to +85°C
	KS54HCTLS: -	-55°C to +125°C
Input Rise & Fall 1	Fimes, $t_r$ , $t_f$	Max 500 ns
* Unused inputs m	ust always be tied	to an appropriate logic
voltage level (ei	ther V <sub>CC</sub> or GND)	)

Characteristic	Symbol	Symbol Test Conditions		<sub>a</sub> = 25°C	KS74HCTLS T <sub>a</sub> = -40°C to +85°C	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	Voh	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	.· V <sub>CC</sub> =0.1 3.7	v
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	liÑ	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	. ±1.0	μΑ
Maximum Quiescent Supply Current	Icc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0,	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input in  V <sub>I</sub> =2.4V  other Inputs: at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0μA		2.7	2.9	. 3.0	mA



#### AC ELECTRICAL CHARACTERISTICS (Input tr., tre6 ns), HCTLS123

Characteristic Symbol Con-				KS74HCTLS $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 10^{\circ}\text{M}$	KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> =5.0V ± 10%	Unit	
			Тур		Guaranteed	Limits	1
Propagation Delay	t <sub>PLH</sub>		23	33	41	50	ns
$\overline{A},B$ to Q, $\overline{Q}$	tpHL	C <sub>L</sub> =50pF	23	33	41	50	113
Propagation Delay	t <sub>PLH</sub>	C <sub>ext</sub> =0,	20	27	34	41	ns
CLR to Q, Q	tpHL	R <sub>ext</sub> =5kΩ	20	27	34.	41	,
Output Pulse Width 1	twq1		116	200	207	209	ns
Output Pulse Width 2	t <sub>WQ2</sub>	$C_L$ =50pF $C_{ext}$ =1000pF $R_{ext}$ =10k $\Omega$	4.5	4.0 5.0	3.8(min) 5.2(max)	3.8 (min) 5.2(max)	μs
Trigger Pulse Width	t <sub>w</sub>	C <sub>L</sub> =50pF A <sub>i</sub> =LOW	7	20	25	30	ns
Trigger Pulse Width	t <sub>w</sub>	C <sub>L</sub> =50pF B <sub>i</sub> =High	7	20	25	30	ns
Clear Pulse Width	tw	C <sub>L</sub> =50pF CLR <sub>i</sub> =LOW	8	20	25	30	ns
External Timing Resistance	Rext			2 1000	2(min) 1000(max)	2(min) 1000(max)	kΩ
External Timing Capacitance	Cin			+	no restriction	n	
Input Capacitance	Cin		5				pF
Power Dissipation Capacitance	C <sub>PD</sub>						pF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

## **Application Information**

The basic output pulse width is determined by the value of external capacitance and timing resistance. For output pulse widths greater than  $100\mu$ s or external capacitance greater than 1000pF the following equation should be used.

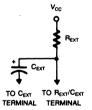
$$t_w = k \cdot R_{ext} \cdot C_{ext}$$

Where

tw is in second
K is the multiplying factor
and is approximately 0.45 for
Cext≥1000pF
Cext is in F

For best results, system ground should be applied to the  $C_{\text{ext}}$  terminal. These devices do not require a switching diode in series with the  $R_{\text{ext}}/C_{\text{ext}}$  terminal (as required by some other monostable multivibrators)

## TIMING COMPONENT



<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current
- (I<sub>OL</sub> = 24 mA @ V<sub>OL</sub> = 0.5V) for direct bus interface ■ Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

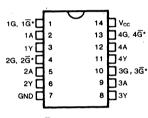
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KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATION



\* G for '125; G for '126

#### **FUNCTION TABLES**

'125							
ir	puts	Output					
A	Ğ	Y					
н	L	Н					
L	L	L					
X	Н	Z					

126

120								
li	nputs	Output						
Α	G	Υ						
Н	Н	Н						
L	н	L						
Х	L	Z						

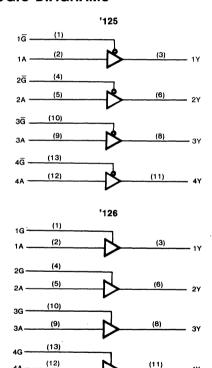
#### **DESCRIPTION**

These bus buffers feature four independent line drivers with 3-state outputs. The output enable functions for the '125 buffers are active-low, while those for '126 are active high.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### LOGIC DIAGRAMS



Supply Voltage Range Vcc,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 70 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . . . . . . . 4.5V to 5.5V DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . OV to  $V_{CC}$  Operating Temperature

Range KS74HCTLS:  $-40^{\circ}$ C to  $+85^{\circ}$ C KS54HCTLS:  $-55^{\circ}$ C to  $+125^{\circ}$ C Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . . . . . . Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

Characteristic	Symbol	ol Test Conditions		Symbol Test Conditions		ymbol Test Conditions		nbol Test Conditions		nbol Test Conditions		nbol Test Conditions $T_a = 25^{\circ}C$ KS74HCTLS $T_a = -40^{\circ}C$ to $+85^{\circ}$				KS54HCTLS $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$	
			Тур		Guaranteed Lim	its											
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	٧										
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧										
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-6m A$	V <sub>CC</sub> 4.2	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> -0.1 3.84	V <sub>CC</sub> −0.1 · 3.7	٧										
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	٧										
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μА										
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μА										
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ										
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA										



#### 5

## AC ELECTRICAL CHARACTERISTICS (Input tr., tr 66 ns), HCTLS125, HCTLS126

Characteristic	Symbol	Conditions†		1		T <sub>a</sub> = 25°0 V <sub>CC</sub> = 5.0°		KS74HCTLS T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%	KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> =5.0V ± 10%	Unit
				Тур		d Limits				
	•	C <sub>L</sub> =50pf	=	13	18	22	27			
Maximum Propagation Delay,	tPLH	C <sub>L</sub> =150	ρF	16	21	27	33	ns		
A to Y		C <sub>L</sub> =50pl	=	13	18	22	27			
	tPHL	C <sub>L</sub> =150pF		16	21	27	33			
	tpzH	R <sub>L</sub> =1kΩ	C <sub>L</sub> =50pF	17	23	29	34	ns		
Maximum Output Enable			C <sub>L</sub> =150pF	20	26	34	40			
Time, Enable to Y			C <sub>L</sub> =50pF	17	23	29	34			
	tpzL		C <sub>L</sub> =150pF	20	26	34	40			
Maximum Output Disable	t <sub>PHZ</sub>	$R_L=1k\Omega$		16		26	32	ns		
Time, Enable to Y	tPLZ	C <sub>L</sub> =50pF		16		26	32	1113		
Maximum Input Capacitance	CIN			5				рF		
Maximum Output Capacitance	Cout	Output D	isabled	10				рF		
Power Dissipation Capacitance* (per stage)	C <sub>PD</sub> *	Output Disabled Output Enabled		5 30		~		pF		

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

**Preliminary Specifications** 

#### **FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
   I<sub>OL</sub> = 8 mA @ V<sub>OL</sub> = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### DESCRIPTION

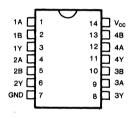
These Schmitt-trigger devices contain four independent NAND gates. They perform the Boolean function  $Y = \overline{A \bullet B} = \overline{A + B}$  in positive logic.

The input threshold levels are temperature compensated and can be triggered from the slowest of input ranges and still give litter-free output signals.

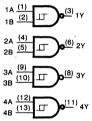
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V<sub>CC</sub> and ground.

#### PIN CONFIGURATION



#### LOGIC DIAGRAM



#### **FUNCTION TABLE**

IN	PUTS	OUTPUTS
Α	В	Υ
L	L	Н
L	н	н
Н	L	н
Н	H,	L

Supply Voltage Hange $V_{CC}$ ,0.5V to +/V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_0 < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . . . . . . . . 4.5V to 5.5V DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . OV to  $V_{CC}$  Operating Temperature

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	т	<sub>a</sub> =25°C	KS74HCTLS T <sub>a</sub> = -40°C to +85°C	KS54HCTLS $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$	Unit
			Тур		its		
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-4mA$	VCC 4.2	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> -0.11	>
Maximum Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> =20μA I <sub>O</sub> =4mA I <sub>O</sub> =8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	٧
Maximum Input Current	lin	V <sub>IN</sub> ≐V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	100	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin  V <sub>I</sub> =2.4V  other inputs: at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0µA		2.7	2.9	3.0	mA

#### DC ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Symbol Test Conditions		25°C	KS74F T <sub>a</sub> = - 40°C	HCTLS to +85°C	KS54 T <sub>a</sub> = - 55°C	HCTLS to +125°C	Unit
O I la la Cito i la Lic	Symbol	1831 Conditions	Min	Max	Min	Max	Min	Max	
Positive-Going	V <sub>T+</sub>	V <sub>CC</sub> =4.5V	1.2	1.9	1.2	1.9	1.2	1.9	v
Threshold Voltage	V 1 +	V <sub>CC</sub> =5.5V	1.4	2.1	1.4	2.1	1.4	2.1	
Negative-Going	V <sub>T</sub> _	V <sub>CC</sub> =4.5V	0.5	1.2	0.5	1.2	0.5	1.2	v
Threshold Voltage	"	V <sub>CC</sub> =5.5V 0.6	1.4	0.6	1.4	0.6	1.4		
Hysteresis	VH	V <sub>CC</sub> =4.5V	0.4	1.4	0.4	1.4	0.4	1.4	v
(V <sub>T+</sub> -V <sub>T-</sub> )	VH	V <sub>CC</sub> =5.5V	0.4	1.5	0.4	1.5	0.4	1.5	

## AC ELECTRICAL CHARACTERISTICS (Input tr., tie6 ns), HCTLS132

Characteristic	Symbol	Conditions <sup>†</sup>	$T_a = 25^{\circ}C$ $V_{CC} = 5.0V$		KS74 HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$	KS54 HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	Unit
			Тур		Guaranteed	Limits	
Maximum Propagation Delay	t <sub>PLH</sub>	C <sub>L</sub> =50pF	17	22	28	33	ns
Any Input to Y	t <sub>PHL</sub>		17	22	28	33 .	113
Maximum Input Capacitance	CIN		5				рF
Power Dissipation Capacitance*	C <sub>PD</sub>	(per gate)					pF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

## 5

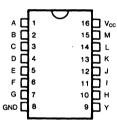
#### **FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
  - IoL = 8 mA @ VoL = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATION



#### **FUNCTION TABLE**

INPUTS A THRU M	OUTPUT Y
All inputs H	L ·
One or more inputs L	н

#### DESCRIPTION

The '133 contains a single 13-input NAND gate. It performs the Boolean functions (in positive logic):

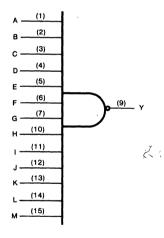
 $Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H \cdot I \cdot J \cdot K \cdot L \cdot M}$ 

 $Y = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} + \overline{F} + \overline{G} + \overline{H} + \overline{I} + \overline{J} + \overline{K} + \overline{L} + \overline{M}$ 

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode olamps to  $V_{CC}$  and ground.

#### **LOGIC DIAGRAM**



<del>_</del>
Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, lo
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW

<sup>\*</sup> Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Supply Voltage, V <sub>CC</sub>	4.5V to 5.5V
DC Input & Output Voltages*, VIN, VOUT	OV to V <sub>CC</sub>
Operating Temperature	

#### DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	bol Test Conditions	T <sub>a</sub> = 25°C		KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 <sub>.</sub> 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

## AC ELECTRICAL CHARACTERISTICS (Input tr. tr. 6 ns), HCTLS133

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 2 V <sub>CC</sub> =		KS74HCTLS $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	Unit
			Тур		Guaranteed	Limits	
Maximum Propagation Delay	tPLH	C <sub>1</sub> = 50pF	18	24	30	36	ns
Any Input to Y	t <sub>PHL</sub>	OL-30pi	18	25	30	36	113
Maximum Input Capacitance	CIN	,	5				pF
Power Dissipation Capacitance*	C <sub>PD</sub>	(per gate)					pF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.



Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

- Designed specifically for high-speed memory decoders and data transmission systems
- Incorporates 3 enable inputs to simplify cascading and/or data reception
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:

 $I_{OL} = 8 \text{ mA } @ V_{OL} = 0.5 \text{V}$ 

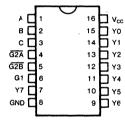
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: ~40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATION



#### **FUNCTION TABLE**

En Inj	1 -	Select Inputs			Outputs							
G1	G2*	С	В	A	YO	Y1	Y2	<b>Y3</b>	<b>Y4</b>	Y5	Y6	<b>Y7</b>
х	Н	х	Х	х	Н	Н	Н	Н	н	Н	Н	н
L	Х	X	Х	Х	Н	Н	Н	Н	Н	Н	Н	Н
Н	L	L	L	L	L	Н	Н	н	Н	Н	Н	Н
Н	L	L	L	Н	Н	L	Н	Н	Н	н	Н	Н
Н	L.	L	Н	L	Н	Н	L	Н	н	Н	Н	Н
Н	L	L	н	н	Н	Н	Н	L	Н	H	Н	н
Н	L	Н	L	L	н	Н	Н	Н	L	Н	Н	Н
Н	L	Н	L	Н	н	Н	Н	н	Н	L	Н	Н
Н	L	Н	Н	L	н	Н	н	Н	Н	н	L	Н
н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L

<sup>•</sup>G2=G2A+G2B

#### DESCRIPTION

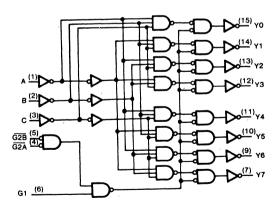
These devices are designed to be used in high-performance memory-decoding or data-routing applications requiring verv short propagation delay times. In high-performance nemory systems, these decoders can be used to minimize the effects of system decoding. When used with high-speed memories utilizing a fast-enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The conditions at the binary select inputs and the three e table inputs select one of eight input lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### LOGIC DIAGRAM



# 3-Line to 8-Line Decoders/Demultiplexers

## **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW

 Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.
 These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . . . . . . 4.5V to 5.5V DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . OV to  $V_{CC}$  Operating Temperature

Range KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . . . Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

Characteristic	Symbol	ol Test Conditions		=25°C	KS74HCTLS T <sub>a</sub> = -40°C to +85°C	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit	
			Тур		Guaranteed Lim	its		
Minimum High-Level Input Voltage	VIH			2.0	2.0	2.0	٧	
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v	
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> -0.1 3.84	. V <sub>CC</sub> -0.1	v	
Maximum Low-Level Output Voltage		$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1	v	
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ	
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ	
Additional Worst Case Supply Current	Δlcc	per input pin  V <sub>I</sub> =2.4V  other Inputs: at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0µA		2.7	2.9	3.0	mA	

## AC ELECTRICAL CHARACTERISTICS (Input tr, tr 6 ns), HCTLS138

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 2 V <sub>CC</sub> =		KS74 HCTLS $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	KS54 HCTLS  T <sub>a</sub> = -55°C to +125°C  V <sub>CC</sub> = 5.0V ± 10%	Unit
			Тур		Guaranteed	Limits	,
Maximum Propagation Delay,	t <sub>PLH</sub>		22	30	37	45	ns
A or B to Y	t <sub>PHL</sub>	C <sub>L</sub> =50pF	22	30	37	45	113
Maximum Propagation Delay,	tpLH	OL-30pi	24	32	40	48	ns
G1 to any Y	t <sub>PHL</sub>		24	32	40	48	115
Maximum Propagation Delay,	t <sub>PLH</sub>		18	25	31	37	ns
G2A or G2B to any Y	t <sub>PHL</sub>		18	25	31	37	115
Maximum Input Capacitance	CIN		5				pF
Power Dissipation Capacitance*	C <sub>PD</sub>	(د	50				pF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

- Designed specifically for high-speed memory decoders and data transmission systems
- Incorporates 2 enable inputs to simplify cascading and/or data reception
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:

IOL = 8 mA @ VOL = 0.5V

- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### DESCRIPTION

These devices are designed to be used in high-performance memory-decoding or data-routing applications requiriring very short propagation delay times. In high-performance memory systems, these decoders can be used to minimize the effects of system decoding. When used with high-speed memories utilizing a fast-enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is nealigible.

The '139 consists of two individual two-line to four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications.

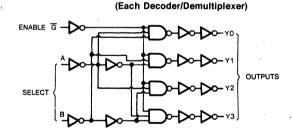
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### PIN CONFIGURATION

#### 

#### LOGIC DIAGRAM



#### **FUNCTION TABLE**

Inputs			Outputs				
Enable G	Sel B	ect A	YO	Y1	Y2	Y3	
Н	Х	X	Н	Н	Н	Н	
L	L	L	L	н	н	н	
L	L	Н	Н.	L	н	Н	
L	Н	L	н	Н	L	. н	
L	Н	Н	Н	Н	Н	L	

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Supply Voltage, Vcc	; 4.5V to 5.5V
DC Input & Output	Voltages*, V <sub>IN</sub> , V <sub>OUT</sub> OV to V <sub>CC</sub>
Operating Temperat	ure
Range	KS74HCTLS: -40°C to +85°C
	KS54HCTLS: -55°C to +125°C
Input Rise & Fall Tir	nes, $t_r$ , $t_f$ Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

Characteristic	Symbol	Test Conditions	T	a = 25°C	KS74HCTLS T <sub>a</sub> = -40°C to +85°C	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	<b>~</b>
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> -0.1 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	l <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin  V <sub>I</sub> =2.4V  other Inputs: at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0µA		2.7	2.9	3.0	mA

# AC ELECTRICAL CHARACTERISTICS (Input tr. tre6 ns), HCTLS139

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 1	25°C 5.0V	KS74 HCTLS $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	Unit	
,			Тур	Typ Guaranteed Limits				
Maximum Propagation Delay,	t <sub>PLH</sub>		22	30	37	45	ns	
A or B to Y	t <sub>PHL</sub>	C <sub>L</sub> =50pF	22	30	37	45		
Maximum Propagation Delay,	t <sub>PLH</sub>	OL-30hi	21	28	35	42	ns	
G to any Y	t <sub>PHL</sub>		21	28	35	42	113	
Maximum Input Capacitance	C <sub>IN</sub>	•	5				pF	
Power Dissipation Capacitance*	C <sub>PD</sub>		50				pF	

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} \ V_{CC}^2 \ f + I_{CC} \ V_{CC}$ .
† For AC switching test circuits and timing waveforms see section 2.

- · Encodes eight data lines in priority
- · Provides 3-bit binary priority code
- · Input enable capability
- Easily cascadable
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
   IoL = 8 mA @ Vol. = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

Package options include plastic "small

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

# DESCRIPTION

The '148 provides three bits of binary coded output representing the position of the highest order active input, along with an output indicating the presence of any active input. It is easily expanded via input and output enables to provide priority encoding over many bits.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

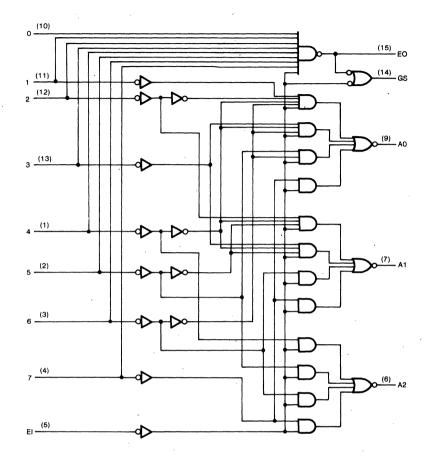
### **PIN CONFIGURATION**

4	1 2 3 4 5 6	16 15 14 13 12	V <sub>cc</sub> EO GS 3 2
			2 1 0 A0

### **FUNCTION TABLE**

			Inj	out	S					(	Outpu	ıts	
EI	0	1	2	3	4	5	6	7	A2	<b>A</b> 1	A0	GS	EO
Н	Х	Х	Х	Х	Х	Х	Х	Χ	Н	Н	Н	Н	Н
L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	н	L
L	Х	Х	Х	Х	Х	Х	Х	L	L	L	L	L	Н
L	Х	Х	Х	Х	Х	Х	L	Н	L	L	Н	L	Н
L	Х	Х	Х	Х	Х	L	Н	Н	L	Н	L	L	Н
L	Х	Х	Х	Х	L	Ή	Н	Н	L	Н	Н	L	Н
L	X	`X	Х	L	Н	н	Н	Н	Н	L	L	L	Н
L	Х	Х	L	Н	Н	Н	Н	Н	Н	L	Н	L	Н
L	Х	L	Н	Н	Н	Н	Н	Н	Н	Н	L	L	н
L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	Н

### LOGIC DIAGRAM



# **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or, } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW
* Absolute Maximum Ratings are those values beyond

These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Range KS74HCTLS:  $-40^{\circ}$ C to  $+85^{\circ}$ C KS54HCTLS:  $-55^{\circ}$ C to  $+125^{\circ}$ C Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . . . . Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)



# DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	Т,	a = 25°C	KS74HCTLS T <sub>a</sub> = -40°C to +85°C	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	v
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	Vон	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	l <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	Icc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

# AC ELECTRICAL CHARACTERISTICS (Input t<sub>r</sub>, t<sub>f</sub>≤6 ns), HCTLS148

Characteristic	Symbol	nbol Conditions†		25°C 5.0V	KS74HCTLS T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%	KS54 HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	Unit
			Тур		Guaranteed	Limits	
Maximum Propagation Delay,	t <sub>PLH</sub>		20	27	34	41	ns
1-7 to A0, A1 or A2	t <sub>PHL</sub>		20	27	34	41	113
Maximum Propagation Delay,	tpLH		22	29	36	44	ns
0-7 to EO	t <sub>PHL</sub>		22	29	36	44	113
Maximum Propagation Delay,	tpLH	C <sub>L</sub> =50pF	28	38	47	57	ns
0-7 to GS	t <sub>PHL</sub>		28	38	47	57	113
Maximum Propagation Delay,	t <sub>PLH</sub>		19	25	31 `	38	ns
El to AO, A1 or A2	t <sub>PHL</sub>		19	25	31	38	ns
Maximum Propagation Delay,	tpLH		20	26	33	39	
El to GS	tent		20	26	33	39	
Maximum Propagation Delay,	tpLH		21	28	35	42	ns
El to EO	t <sub>PHL</sub>		21	28	35	42	113
Maximum Input Capacitance	C <sub>IN</sub>		5				pF
Power Dissipation Capacitance*	C <sub>PD</sub>	(per gate)	50				рF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} \ V_{CC}^2 \ f + I_{CC} \ V_{CC}$ .

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

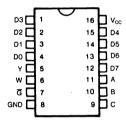
- Can perform as:
   Boolean Function Generators

   Parallel-to-Serial Converters
   Data Source Selectors
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
- (I<sub>OL</sub> = 24 mA @ V<sub>OL</sub> = 0.5V) for direct bus interface ■ Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

### PIN CONFIGURATION



# **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) + \pm 20 \text{ mA}$
DC Output Diode Current, I <sub>OK</sub>
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 70 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Detings are those values become

Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

### DESCRIPTION

These monolithic data selectors/multiplexers provide full binary decoding to select one of eight data sources. The strobe input  $(\overline{G})$  must be at a low logic level to enable the inputs. A high level at the strobe terminal forces the W output high and the Y output low.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

### **FUNCTION TABLE**

		INPUT	rs	OUTPUTS			
S	SELECT STROBE						
С	В	Α	Ğ	Y W			
Х	Х	Х	Н	L	н		
L	L	L	L	DO	$\overline{DO}$		
L	L	H	L	D1	D1		
L	Н	L	L .	D2	D2		
L	Н	н	L	D3	D3		
Н	L	L	L	D4	D4		
Н	L	н	L	Ð5	D5		
Н	Н	, L	, L	D6	D6		
Н	Н	H	L	D7	D7		

H = high level, L = low level, X = irrelevant D0, D1 ... D7 = the level of the D respective input

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

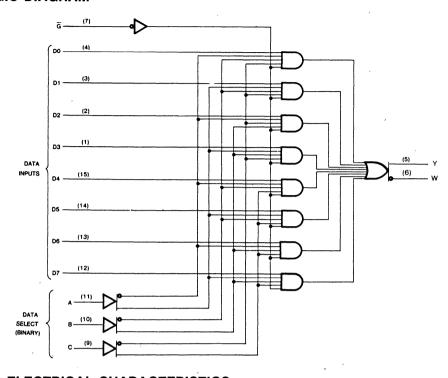
Supply Voltage, V<sub>CC</sub> . . . . . . . . . 4.5V to 5.5V DC Input & Output Voltages\*, V<sub>IN</sub>, V<sub>OUT</sub> . . OV to V<sub>CC</sub> Operating Temperature

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

Input Rise & Fall Times,  $t_r, \ t_f \dots \dots$  Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

# LOGIC DIAGRAM



DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	= 25°C	KS74HCTLS T <sub>a</sub> = -40°C to +85°C	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit
1			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-6mA$ .	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> -0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	Icc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin $V_{l}{=}2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}{=}0\mu A$		2.7	2.9	3.0	mA

# AC ELECTRICAL CHARACTERISTICS (Input tr, tre6 ns), HCTLS151

Characteristic	Symbol	Conditions†	T <sub>a</sub> = : V <sub>CC</sub> =		KS74HCTLS $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	Unit
			Тур		Guaranteed	Limits	
Maximum Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	24 27	32 35	40 <b>4</b> 5	48 54	ns
A, B or C to Y	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	24 27	32 35	40 <b>45</b>	48 54	113
Maximum Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	27 30	36 <b>39</b>	45 50	54 60	ns
A, B or C to W	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	27 30	36 39	45 50	54 60	113
Maximum Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	20 23	26 29	33 38	39 45	ns
Any D to Y	t <sub>PHL</sub>	$C_L=50pF$ $C_L=150pF$	20 23	26 29	33 38	39 <b>45</b>	,,,
Maximum Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	16 19	21 24	26 31	32 38	ns
Any D to W	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	16 19	21 24	26 31	32 38	113
Maximum Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	20 23	26 29	33 38	39 45	ns
G to Y	t <sub>PHL</sub>	$C_L=50pF$ $C_L=150pF$	20 23	26 29	33 38	39 45	
Maximum Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	20 23	26 29	33 38	39 45	ns
G to W	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	20 23	26 29	33 38	. 39 45	113
Maximum Input Capacitance	CIN		5				рF
Power Dissipation Capacitance*	C <sub>PD</sub>				,		рF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

- . Allows Multiplexing from N Lines to 1 Line
- Performs Parallel-to-Serial Conversion
- Strobe (Enable) Line Provided for Cascading (N lines to n lines)
- · '253 is the 3-State Version of this port
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
  - ( $I_{OL} = 24 \text{ mA } @ V_{OL} = 0.5 \text{V}$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
   KS74HCTLS: -40°C to +85°C
   KS54HCTLS: -55°C to +125°C
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

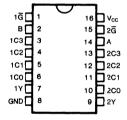
### DESCRIPTION

Each of these data selectors/multiplexers contains inverters and drivers to supply full binary decoding data selection to the AND-OR gates. Separate strobe inputs  $(\bar{G})$  are provided for each of the two four-line sections.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

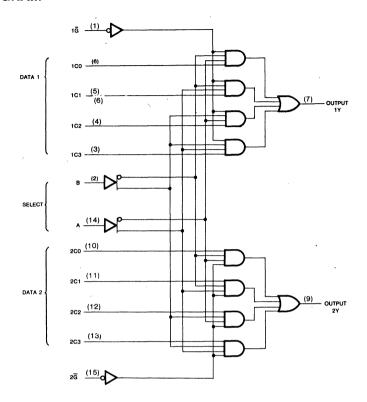
### PIN CONFIGURATION



### **FUNCTION TABLE**

	SELECT INPUTS		ATA	INPU	TS	STROBE	ОИТРИТ
В	A	CO	C1	C2	СЗ	G	Y
Х	Х	Х	Х	Х	Х	Н	L
L	L	L	Χ	Χ	Х	L	L
L	L	Н	Х	Х	Χ	L	Н
L	Н	Х	L	Χ	Х	L	L
L	Н	Х	Н	Χ	Х	L	н
Н	L	Х	Х	L	Х	L	L
Н	L	Х	Х	н	Х	L	н
Н	Н	Х	Х	Х	L	L	L
Н	H	Х	Χ	Х	Н	L	н

### LOGIC DIAGRAM



# **Absolute Maximum Ratings\***

DC Input Diode Current, IIK

$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + 2.5V$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, T <sub>stg</sub> −65 °C to +150 °C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW

Supply Voltage Range  $V_{CC_1}$  ..... -0.5V to +7V

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Range KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . . Max 500 ns

 Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

# DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T	= 25°C	KS74HCTLS T <sub>a</sub> = -40°C to +85°C	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	0.8	v.
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-6mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> -0.1	v
Maximum Low-Level Output Voltage	Vol	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> =20µA I <sub>O</sub> =12mA I <sub>O</sub> =24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	liN	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

# AC ELECTRICAL CHARACTERISTICS (Input tr, tr≤6 ns), HCTLS153

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74HCTLS T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%	KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	Unit
			Тур		Guaranteed	Limits	
Maximum Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	23 26	30 33	38 43	45 51	ns
A or B to Y	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	23 26	30 33	38 43	45 51	113
Maximum Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	15 18	20 23	25 30	30 36	ns
Data (Any C) to Y	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	15 18	20 23	25 30	30 . 36	
Maximum Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	21 24	28 31	35 40	42 48	ns
G to Y	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	21 .24	28 31	35 40	42 48	113
Maximum Input Capacitance	CIN		5				рF
Power Dissipation Capacitance*	C <sub>PD</sub>						pF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

- Decodes 4 Binary-Coded Inputs into One of 16 Mutually Exclusive Outputs
- Performs the Demultiplexing Function by Distributing Data From One Input to Any One of 16 Outputs
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
- $I_{OL} = 8 \text{ mA } @ V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
   (274) 71 5 4090 45 4 5590

KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

### **DESCRIPTION**

These monolithic, 4-line to 16-line decoders decode four binary-coded inputs into one of sixteen mutually exclusive outputs when both the strobe inputs.  $\overline{G}1$  and  $\overline{G}2$ , are low. The demultiplexing function is performed by using the 4 input lines to address the output line, passing data from one of the strobe inputs with the other strobe input low. When either strobe input is high, all outputs are high. These demultiplexers are ideally suited. If or implementing high-performance memory decoders.

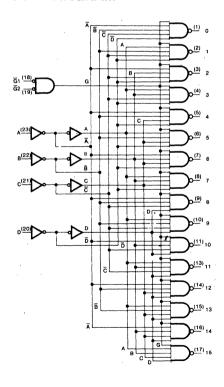
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

### PIN CONFIGURATION

001	24 V <sub>cc</sub>
1 🗖 2	23 🗖 A
2 🗖 3	22 🗖 B
3 🗖 ⁴	21 🗖 C
4 🗖 5	20 🗖 D
5 🗖 6	19 🗖 🛱 2
6 <b>口</b> 7	18 🗖 🛱 1
7 🗖 8	17 🗖 15
8 <b>口</b> 9	16 14
9월10	15 🗖 13
10011	14 12
GND ☐ 12	13 11

### LOGIC DIAGRAM



### **FUNCTION TABLE**

		Inputs	3										O	utpu	ıts						
Ğ1	G2	D	С	В	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	Ļ	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
L	L	L	L	L	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
L	L	L	L	Н	L	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
L	L	L	L	Н	Н	Н	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
L	L	L	Н	L	L	Н	Н	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
L	L	L	Н	L	Н	H	Н	Н	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
L	L	L	Н	Н	L	Н	Н	Н	Н	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н
L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н
L	L	Н	L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	L	Н	Н	Н	` Н	Н	Н	Н
L	L	н	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	Н	Н	Н	Н	Н	Н
L	· L	Н	L	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	Н	Н	Н	Н	Н
L	L	н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	Н	Н	Н	Н
L	L	Н	Н	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	Н	Н	Н
L	L	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	. Н	Н	L	Н	Н
L	L	Н	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	Н
L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L
L	Н	Х	Χ	Χ	Χ	Н	Н	H	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
н	L	Х	Х	Χ	Χ	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
н	Н	X	Χ	Χ	Χ	Н	·H	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н

### **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, I <sub>OK</sub>
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW

<sup>\*</sup> Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Range KS74HCTLS:  $-40^{\circ}$ C to  $+85^{\circ}$ C KS54HCTLS:  $-55^{\circ}$ C to  $+125^{\circ}$ C Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns

\* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

# DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	1		a = 25°C	KS74HCTLS T <sub>a</sub> = -40°C to +85°C	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit			
			Тур		Guaranteed Lim	its	1			
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	v			
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	0.8	v			
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> -0.1 3.84	V <sub>CC</sub> −0.1 3.7	v			
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v			
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ			
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ			
Additional Worst Case Supply Current	Δlcc	per input pin  V <sub>I</sub> =2.4V  other Inputs: at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0µA		2.7	2.9	3.0	mA			

# AC ELECTRICAL CHARACTERISTICS (Input tr, tr 66 ns), HCTLS154

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74 HCTLS T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%	KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	Unit		
			Тур	Typ Guaranteed Limits					
Maximum Propagation Delay,	t <sub>PLH</sub>		21	28	35	42	ns		
A, B, C or D to Any Output	tpHL	C <sub>L</sub> =50pF	21	28	35	42			
Maximum Propagation Delay,	tpLH	OL-3001	2,1	28	35	42	ns		
G1 or G2 to Any Output	t <sub>PHL</sub>		21	28	35	42	115		
Maximum Input Capacitance	CIN		5				рF		
Power Dissipation Capacitance*	C <sub>PD</sub>						рF		

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .



<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

- Typical applications:
   Dual 2-to-4 line decoder
   Dual 1-to-4 line demultiplexer
   3-to-8 line decoder
   1-to-8 line demultiplexer
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
  - $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5 \text{V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges: KS74HCTLS: -40°C to +85°C
  - KS54HCTLS: -55°C to +125°C
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

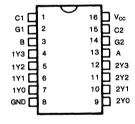
### DESCRIPTION

The '155 consists of two 1-to-4 line demultiplexers with independent strobes and common binary address inputs. When both sections are enabled by the strobes, the common address inputs sequentially select and route associated input data to the appropriate output of each secton. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired. Data applied to input C1 is inverted at its outputs and data applied to C2 is true through its outputs. The inverter following the C1 data input permits use as a 3-to-8 line decoder, or 1-to-8 line demultiplexer, without gating.

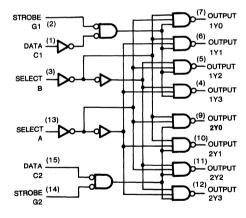
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

### PIN CONFIGURATION



### LOGIC DIAGRAM



### **FUNCTION TABLES**

2-to-4 Line Decoder or 1-to-4 Line Demultiplexer

		inputs		Outputo					
Sel	ect	Strobe	Data	Outputs					
В	A	G1	C1	1Y0	1Y1	1Y2	1Y3		
X	Х	н	X	Н	Н	Н	Н		
L	L	L	н	L	Н	Н	Н		
L	Н	L	Н	H	L	Н	Н		
Н	L	L	Н	Н	Н	L	Н		
Н	Н	L	Н	Н	Н	Н	L,		
X	X	X	L	Н	Н	Н	Н		

		Inputs		0					
Sel	ect	Strobe	Data	Outputs					
В	A	G2	C2	2Y0	2Y1	2Y2	2Y3		
Х	Х	н	Х	Н	Н	Н	Н		
L	L	L	L	L	Н	н	Н		
L	Н	L	L	н	L	н	н		
Н	L	L	L	н	н	L	Н		
. Н	Н	L	L	н	Н	н	L		
Х	Χ	Х	н	Н	Н	Н	Н		

3-to-8 Line Decoder or 1-to-8 Line Demultiplexer

in	outs				Out	puts			
Select	Strobe or Data	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
IC B A	IG .	2Y0	2Y1	2Y2	2Y3	1Y0	1Y <u>1</u>	1Y2	1Y3
XXX	Н	Н	Н	Н	Н	Н	Н	Н	Н
LLL	L	L	Н	Н	Н	Н	Н	Н	Н
LLH	L	Н	L	Н	Н	Н	Н	Н	Н
LHL	L	Н	٠н	L	Н	Н	Н	Н	н
LHH	L	Н	Н	Н	L	Н	Н	Н	Н
HLL	L	Н	Н	Н	Н	L	Н	Н	Н
HLH	L.	Н	Н	Н	Н	Н	L	Н	Н
HHL	L	Н	Н	Н	Н	Н	Н	L	Н
HHH	L	Н	Н	Н	Н	Н	Н	Н	L

IC = Inputs C1 and C2 connected together IG = Inputs G1 and G2 connected together

# **Absolute Maximum Ratings\***

Supply Voltage Range $V_{CC}$ , $-0.5V$ to $+7V$
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW

<sup>\*</sup> Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . . . . . . . . 4.5V to 5.5V DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . OV to  $V_{CC}$  Operating Temperature

Range KS74HCTLS:  $-40^{\circ}$ C to  $+85^{\circ}$ C KS54HCTLS:  $-55^{\circ}$ C to  $+125^{\circ}$ C Input Rise & Fall Times,  $t_r$ ,  $t_t$  . . . . . . Max 500 ns

 Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

### DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	a = 25°C	KS74HCTLS T <sub>a</sub> = -40°C to +85°C	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH} \text{ or } V_{IL}$ $I_{O}=-20\mu\text{A}$ $I_{O}=-4\text{mA}$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> -0.1	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	l <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	Icc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin  V <sub>I</sub> =2.4V  other Inputs:  at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0µA		2.7	2.9	3.0	mA

# AC ELECTRICAL CHARACTERISTICS (Input tr, tre6 ns), HCTLS155

Characteristic	Symbol	Conditions†	T <sub>a</sub> = :		KS74 HCTLS $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	KS54 HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	Unit	
			Тур		Guaranteed	l Limits		
Maximum Propagation Delay, A, B, C2, G1 or G2 to any Output	t <sub>PLH</sub>		17	23	29	35	ns	
(2 levels of logic)	t <sub>PHL</sub>		17	23	29	35		
Maximum Propagation Delay, A or B to any Y	t <sub>PLH</sub>	CL=50pF	21	28	35	42	ns	
(3 levels of logic)	t <sub>PHL</sub>	CL=30pr	, J	21	28	35	42	
Maximum Propagation Delay,	t <sub>PHL</sub>		20	27	34	41	ns	
C1 to any Y	t <sub>PHL</sub>		20	27	34	41	113	
Maximum Input Capacitance	Cin		5				pF	
Power Dissipation Capacitance*	C <sub>PD</sub>						pF	

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

# Quad 2-Line to 1-Line Data Selectors/Multiplexers

### **FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
  - $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

### DESCRIPTION

These are data selectors/multiplexers which select a 4-bit word from one of two sources via the control of a common select input  $(\overline{A}/B)$ . A separate strobe input  $(\overline{G})$  is provided. The '157 presents true data whereas the '158 presents inverted data at the outputs.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

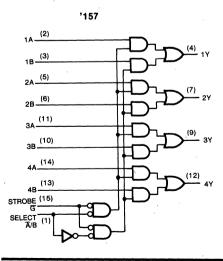
### PIN CONFIGURATION

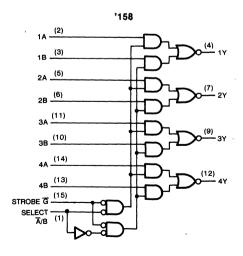
1		<del></del>
Ā/B □	1	16 🗖 V <sub>cc</sub>
1A 🗆	2	15 🗖 Ğ
1B 🛚	3	14 🗖 4A
· 1Y 🛚	4	13 🗖 4B
2A 🗌	5	12 🗖 4Y
2B 🗆	6	11 🗖 3A
2Y 🗆	7	10 🗖 3B
GND [	8 .	9 🗖 3Y
	L	

### **FUNCTION TABLE**

	Inputs	Output Y				
Strobe	Select	Da	ıta	'157		
Ğ	Ã/B	A	В	157	'158	
Н	Х	Х	Х	L	Н	
L,	L	L	Х	L	н	
L	L	Н	Х	н	L	
L.	н	X	L	L	н	
L	н	X	Н	н	L	

### LOGIC DIAGRAMS







# KS54HCTLS **157/158** KS74HCTLS

# Quad 2-Line to 1-Line Data Selectors/Multiplexers

### **Absolute Maximum Ratings\***

Supply Voltage Range $V_{CC}$ , $-0.5V$ to $+7V$
DC Input Diode Current, I <sub>IK</sub>
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, $P_d{}^\dagger$ 500 mW

 Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . . . . . . . . 4.5V to 5.5V DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . OV to  $V_{CC}$  Operating Temperature

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . . . Max 500 ns

 Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

# DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	= 25°C	KS74HCTLS T <sub>a</sub> = -40°C to +85°C	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	V <sub>IL</sub>		,	0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH} \text{ or } V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-4\text{mA}$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> -0.1 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	Icc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin  V <sub>I</sub> =2.4V  other Inputs:  at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0µA		2.7	2.9	3.0	mA



# AC ELECTRICAL CHARACTERISTICS (Input tr, tr 6 ns), HCTLS157, HCTLS158

Characteristic	Symbol	Conditions†	T <sub>a</sub> = :		KS74HCTLS $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	KS54 HCTLS  T <sub>a</sub> = -55°C to +125°C  V <sub>CC</sub> = 5.0V ± 10%	Unit
			Тур		Guaranteed	Limits	
Maximum Propagation Delay, A or B to Y	t <sub>PLH</sub>		11	15	19	22	ns
	t <sub>PHL</sub>		11	15	19	22	113
Maximum Propagation Delay,	t <sub>PLH</sub>	,	17	23	29	34	ns
Ā/B to Y	t <sub>PHL</sub>		17	23	29	34	113
Maximum Propagation Delay,	t <sub>PLH</sub>		15	20	25	30	ns
G to Y	t <sub>PHL</sub>		15	20	25	30	113
Maximum Input Capacitance	CIN		5				pF
Power Dissipation Capacitance*	C <sub>PD</sub>	(per gate)					pF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

# KS54HCTLS 16UA/161A KS74HCTLS 162A/163A

# Synchronous 4-Bit Decade and Binary Counters

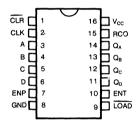
### **FEATURES**

- Internal Look Ahead for Fast Counting
- · Carry Output for n-bit cascading
- Synchronous Counting
- Synchronously Programmable
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
  - IOL = 8 mA @ VOL = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

### PIN CONFIGURATION



#### **FUNCTION TABLES**

'160, '161

CLK	CLR	ENP	ENT	LOAD	Function
Х	L	Х	Х	Х	Clear
X	Н	н	L	Н	Count & RC disabled
X	Н	L	Н	н	Count disabled
X	Н	L	L	н	Count & RC disabled
1	Н	X	Х	L	Load
1	Н	н	Н	Н	Increment Counter

'162, '163

CLK	CLR	ENP	ENT	LOAD	Function
1	L	Х	Х	Х	Clear
X	H	Н	L	Н	Count & RC disabled
X	Н	L	Н	н	Count disabled
X	Н	L	L	н	Count & RC disabled
1	Н	Х	Х	L	Load
1	Н	Н	Н	Н	Increment Counter

### DESCRIPTION

These are synchronous, presettable 4-bit binary counters featuring internal carry-look-ahead for high-speed counting. The '160 and '162 are decade counters, and the '161 and '163 are 4-bit binary counters. The buffered clock input triggers all flip-flops simultaneously on the rising edge of the input waveform. This eliminates the output counting spikes normally associated with asynchronous counters.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs.

The clear function for the '160 and '161 is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of the clock, load or enable inputs.

The clear function for the '162 and 163 is synchronous and a low level at the clear input sets all four of the flipflop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter.

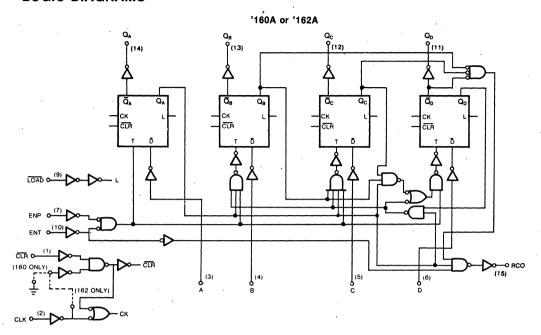
Two enable inputs and a ripple carry output allow easy cascading of the counters. Both count-enable inputs (ENP and ENT) must be high to count, and ENT is fed forward to enable the ripple carry output. The ripple carry output (RCO) thus enabled will produce a high-level pulse while the count is maximum (9 or 15 with QA high). This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. Transitions at the ENP or ENT are allowed regardless of the level of the clock input.

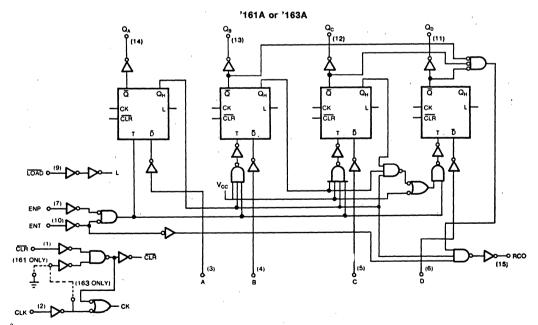
These counters feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, or  $\overline{\text{LOAD}}$ ) that will modify the operating model have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{\text{cc}}$  and ground.

# **LOGIC DIAGRAMS**



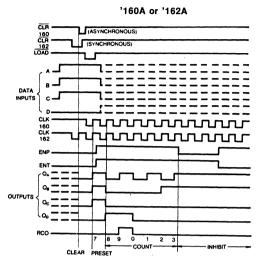


# KS54HCTLS 16UA/161A KS74HCTLS 162A/163A

# Synchronous 4-Bit Decade and Binary Counters

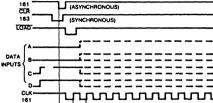
'161A or '163A

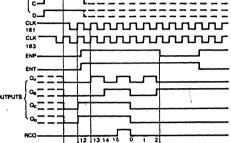
### Typical Clear, Preset, Count and Inhibit Sequences



#### Sequence:

- (1) Clear outputs to zero
- (2) Preset to BCD seven
- (3) Count to eight, nine, zero, one, two, and three
- (4) Inhibit





#### Sequence:

- (1) Clear outputs to zero
- (2) Preset to binary twelve
- (3) Count to thirteen, fourteen, fifteen, zero, one and two
  - (4) Inhibit

### **Absolute Maximum Ratings\***

Supply Voltage Range $V_{CC}$ , $-0.5V$ to $+7V$
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . . . . . . . . . . . . . . 4.5V to 5.5V DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . OV to  $V_{CC}$  Operating Temperature

Range KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  Input Rise & Fall Times,  $t_r$ ,  $t_t$  Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

# KS54HCTLS 160A/161A KS74HCTLS 162A/163A

# Synchronous 4-Bit Decade and Binary Counters

# DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	= 25°C	KS74HCTLS T <sub>a</sub> = -40°C to +85°C	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	v
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -4\text{mA}$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

# AC ELECTRICAL CHARACTERISTICS (Input tr, tre6 ns), HCTLS160A, HCTLS161A

Characteristic		Symbol	Conditions	-	25°C = 5.0V	KS74HCTLS $T_a = -40 ^{\circ}\text{C to } +85 ^{\circ}\text{C}$ $V_{\text{CC}} = 5.0 \text{V} \pm 10 \%$	KS54HCTLS $T_a = -55^{\circ}\text{C to } + 125^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	Unit
			,	Тур		Guaranteed	l Limits	
Maximum Clock	Frequency	f <sub>max</sub>		40	30	25	20	MHz
Maximum Propag	gation Delay,	t <sub>PLH</sub>		26	35	44	53	ns
CLK to RCO		t <sub>PHL</sub>		26	35	44	53	
Maximum Propag	gation Delay,	t <sub>PLH</sub>		20	26	. 33	39	ns
CLK to any Q		t <sub>PHL</sub>	C <sub>1</sub> = 50pF	20	26	33	39	
Maximum Propag	gation Delay,	tpLH	OL COPI	11	14	18	21	ns
ENT to RCO				11	14	18	21	
Maximum Propagation Delay, CLR to any Q		t <sub>PHL</sub>		21	28	35	42	ns
Maximum Propag	gation Delay,	t <sub>PHL</sub>	,	21	28	35	42	ns
Minimum Pulse	CLK High or Low			10	13	17	20	
Width	CLR Low	t <sub>w</sub>		10	13	17	20	ns
	A, B, C, D		,	10	13	17	20	
Minimum Setup	LOAD	1		10	13	17	20	ns
Time before	ENP, ENT	t <sub>su</sub>		10	13	17	20	113
CLK1	CLR inactive	1		10	13	17	20	1
Minimum Hold Time, All Synchronous Inputs after CLK†		th		0	0	. 0	0	ns
Input Capacitano	е	CIN		5		r		рF
Power Dissipation	n Capacitance*	C <sub>PD</sub>		80				pF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} \ V_{CC}^2 \ f \ + \ I_{CC} \ V_{CC}$ .

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.



# KS54HCTLS 160A/161A KS74HCTLS 162A/163A

# Synchronous 4-Bit Decade and Binary Counters

# AC ELECTRICAL CHARACTERISTICS (Input tr, tr 66 ns), HCTLS162A, HCTLS163A

Characteristic		Symbol	Conditions†	-	25°C = 5.0V	KS74HCTLS $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 10^{\circ}\text{M}$	KS54HCTLS $T_a = -55$ °C to +125°C $V_{CC} = 5.0V \pm 10\%$	Unit
				Тур	Typ Guaranteed Limits			1
Maximum Clock	Frequency	f <sub>max</sub>		40	30	25	20	MHz
Maximum Propag	gation Delay,	t <sub>PLH</sub>		26	35	44	53	ns
CLK to RCO		t <sub>PHL</sub>		26	35	44	53	
Maximum Propag	gation Delay,	t <sub>PLH</sub>		20	26	33	39	ns
CLK to any Q		t <sub>PHL</sub>	C <sub>1</sub> = 50pF	20	26	33	39	110
Maximum Propag	gation Delay,	t <sub>PLH</sub>	OL COPI	11	14	18	21	ns
ENT to RCO		t <sub>PHL</sub>		11	14	18	21	110
Maximum Propagation Delay, CLR to any Q		t <sub>PHL</sub>		21	28	35	42	ns
Maximum Propag	gation Delay,	t <sub>PHL</sub>		21	28	35	42	ns
Minimum Pulse	CLK High or Low			10	13	17	20	
Width	CLR Low	t <sub>w</sub>		10	13	17	20	ns
	A, B, C, D			10	13	17	20	
Minimum Setup	LOAD			10	13	17	20	
Time before	ENP, ENT	t <sub>su</sub>		10	13	1.7	20	ns
CLKf	CLR inactive	1		10	13	17	20	
	CLR Low	]		10	13	17	20	
Minimum Hold Time, All Synchronous Inputs after CLK↑		t <sub>h</sub>		-3	0	. 0	0	ns
Input Capacitano	е	C <sub>IN</sub>		5				рF
Power Dissipatio	n Capacitance*	C <sub>PD</sub>		80				pF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} \ V_{CC}^2 \ f \ + \ I_{CC} \ V_{CC}$ .

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

- AND—Gated (enable/disable) serial inputs
- Fully buffered clock and serial inputs
- Direct clear
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs: IOL = 8 mA @ VOL = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

### DESCRIPTION

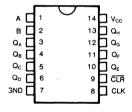
These are high-speed 8-bit registers with AND-gated serial inputs and an asynchronous clear. Data is entered serially through either one of the two inputs, A and B. A high on one input enables the other one, which will then determine the state of the first flip-flop. A low at either or both inputs inhibits data entry and resets the first flip-flop to a low level at the next positive clock transition.

Data at the serial inputs may be changed while the clock is high or low, provided the minimum setup time requirements are met. Clocking occurs on the low-to-high-level transition of their clock input.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

### PIN CONFIGURATION



### **FUNCTION TABLE**

	Inputs	Outputs				
Clear	Clock	A	В	QA	Q <sub>B</sub> .	Q <sub>H</sub>
L	Х	Х	Х	L	·L	L
н	Ŀ	Х	Х	Q <sub>AO</sub>	$Q_{B0}$	Q <sub>H0</sub>
н	1	Н	Н	Н	$Q_{An}$	$Q_{Gn}$
н	1	L	Χ	L	$Q_{An}$	$Q_{Gn}$
Н	1	Х	L	L	$Q_{An}$	$Q_{Gn}$

H = high level (steady state), L = low level (steady state)

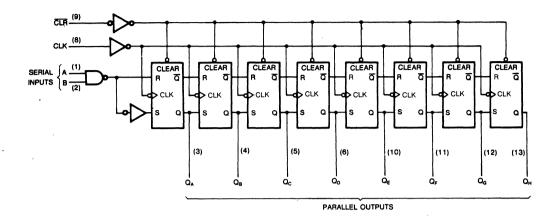
X = irrelevant (any input, including transitions)

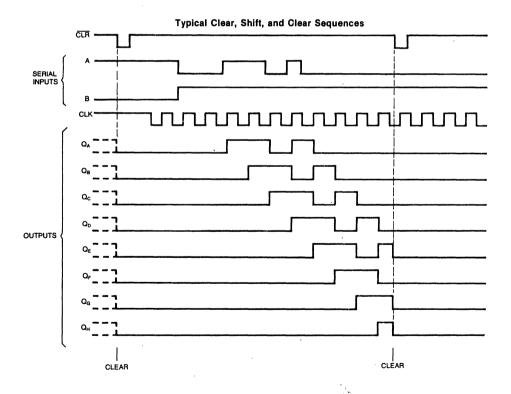
t = transition from low to high level.

 $Q_{A0}$ ,  $Q_{B0}$ ,  $Q_{H0}$ =the level of  $Q_{A}$ ,  $Q_{B}$  or  $Q_{H}$ , respectively, before the indicate steady-state input conditions were established.

 $Q_{An}$ ,  $Q_{Gn}$  = the level of  $Q_A$  or  $Q_G$  before the most-recent † transition of the clock; indicates a one-bit shift.

# **LOGIC DIAGRAM**





# 8-Bit Serial-In/Parallel-Out Shift Registers

# **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_{I} < -0.5V \text{ or } V_{I} > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW
* Absolute Meximum Petings are those values beyond

Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation

of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

		4.5V to 5.5V V <sub>OUT</sub> OV to V <sub>CC</sub>
Operating Tempe	rature	
Range	KS74HCTLS:	-40°C to +85°C

KS54HCTLS: -55°C to +125°C Input Rise & Fall Times, tr, tf ..... Max 500 ns

\* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

# DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T <sub>a</sub> = 25°C		KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-4m A$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> -0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	liN	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin  V <sub>I</sub> =2.4V  other Inputs: at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0µA		2.7	2.9	3.0	mA

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# AC ELECTRICAL CHARACTERISTICS (Input tr, tr 6 ns), HCTLS164

Charact	Characteristic		Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74HCTLS T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%	KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> =5.0V± 10%	Unit	
				Тур		Guaranteed	l Limits		
Maximum Clock Fre	equency	f <sub>max</sub>		40	30	25	20	MHz	
Maximum Propagat CLR to any Q	Maximum Propagation Delay, CLR to any Q		C <sub>L</sub> =50pF	27	36	45	54	ns	
Maximum Propagation Delay, CLK to any Q		tpLH	GL-SUPP	22	30	37	45	ns	
		t <sub>PHL</sub>		22	30	37	45		
Minimum	CLR Low	tw		10	13	17	20	ns	
	CLK High or Low			10	13	17	20	113	
Minimum Setup	Data			8	10	13	15	ns	
Time before CLK1	CLR Inactive	t <sub>su</sub>		8	10	13	15	113	
Minimum Hold Tim Data after CLK1	e	th		0	5	5	5	ns	
Maximum Input Capacitance		CiN		5				рF	
Power Dissipation (	Capacitance*	CPD	(per package)	120				рF	

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

- Complementary outputs
- · Direct overriding load (data) inputs
- · Gated clock inputs
- Parallel-to-Serial data conversion
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
   I<sub>OL</sub> = 8 mA @ V<sub>OL</sub> = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

Package options include plastic ""small outline"
 packages, standard plastic and ceramic 300-mil DIPs

### DESCRIPTION

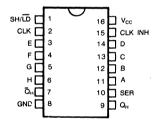
These are high-speed 8-bit parallel-load or serial-in shift registers with complementary serial outputs available from the last stage. Parallel-in access is asynchronous and is enabled by pulling the SH/LD input low. When SH/LD is high, data is entered serially at the SER input and shifted one place to the right with each positive clock transition.

Clocking is accomplished through a 2-input NOR gate which permits one of the clocks to be used as a clock inhibit function. Holding either clock input high inhibits clocking. Either clock input is enabled by holding the other clock input low while the SH/LD input is high.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

### PIN CONFIGURATION

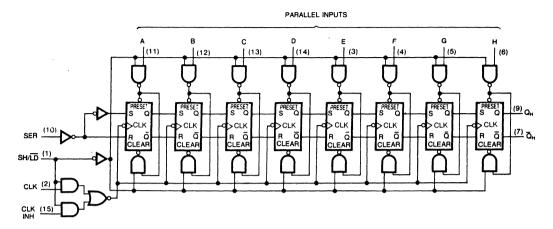


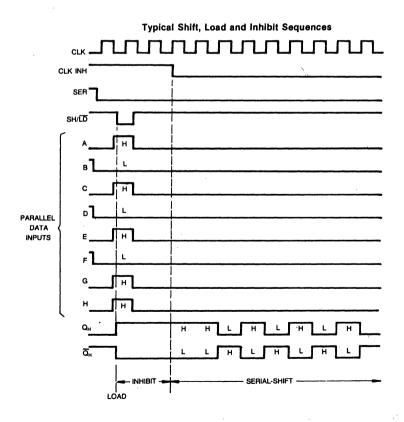
### **FUNCTION TABLE**

,	Inputs			
SH/LD	CLK	CLK INH	Function	
L	Х	Х	PARALLEL LOAD	
Н	Н	X	NO CHANGE	
H	X	Н	NO CHANGE	
Н	L	<b>†</b>	SHIFT*	
Н	1	L	SHIFT*	

<sup>\*</sup>Content of each internal register shifts toward output Q<sub>H</sub>. Data at serial input is shifted into first register.

# **LOGIC DIAGRAM**





# **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±35 mA
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, $T_{stg} \dots -65$ °C to $+150$ °C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Ratings are those values beyond

which permanent damage to the device may occur.

These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

# **Recommended Operating Conditions**

Supply Voltage,	Vcc	4.5V to 5.5\
DC Input & Outp	out Voltages*, V <sub>IN</sub> ,	Vout OV to Vo
Operating Temp	erature	
Range	KS74HCTLS:	-40°C to +85°C

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

# DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	c Symbol Test Condi		T <sub>a</sub> = 25°C		KS74HCTLS T <sub>a</sub> = -40°C to +85°C	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	ViL	,		0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> =0.1 3.84	V <sub>CC</sub> -0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> =20µA I <sub>O</sub> =4mA I <sub>O</sub> =8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	· v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	Δlcc	per input pin  V <sub>I</sub> =2.4V  other Inputs: at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0µA		2.7	2.9	3.0	mA

<sup>†</sup> Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# AC ELECTRICAL CHARACTERISTICS (Input tr, tre6 ns), HCTLS165

C	Characteristic		Characteristic Symbol Conditions		Conditions <sup>†</sup>	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		$V_{CC} = 5.0V \pm 10\%$	$KS54HCTLS$ $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$	Unit	
				Тур	Typ Guaranteed Limits						
Maximum Ck	ock Frequency	f <sub>max</sub>		40	30	25	20	MHz			
Maximum Pr	opagation Delay,	tpLH		26	35	44	53	ns			
SH/LD to Q⊦	ı or Q <sub>H</sub>	tpHL		26	35	44	53				
Maximum Pr	opagation Delay,	t <sub>PHL</sub>	C <sub>L</sub> =50pF	30	40	50	60	ns			
CLK to Q <sub>H</sub> o	or Q <sub>H</sub>	t <sub>PHL</sub>		30	40	50	60	113			
Maximum Pr	opagation Delay,	tpLH		20	27	34	41	ns			
H to Q <sub>H</sub> or $\overline{Q}$		t <sub>PHL</sub>		20	27	34	41				
Minimum	SH/LD Low	tw		7	10	13	15	ns			
Pulse Width	CLK High or Low	ı w	ì.	13	16	20	25	113			
	SH/LD High before CLK1			13	16	20	25				
	SER before CLK1	1		10	13	17	20				
Minimum Setup Time	CLK INH Low before CLK1	t <sub>su</sub>		13	16	20	25	ns			
	CLK INH High before CLK↓			13	16	. 20	25				
	Data before SH/LDt	1	•	5	7	8	10				
Minimum	SER Data after CLK1	th		-3	0	0	0	ns			
Hold Time	PAR Data after SH/LD1			-3	0	0	0	113			
Maximum Inp	out Capacitance	CIN		5				pF			
Power Dissip	oation Capacitance*	C <sub>PD</sub>		100				pF			

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

- Synchronous load
- · Direct overriding clear
- Parallel to serial conversion
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
- IOL = 8 mA @ VOL = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
   KS74HCTLS: -40°C to +85°C
   KS54HCTLS: -55°C to +125°C
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

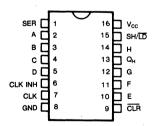
### **DESCRIPTION**

These devices feature parallel-in or serial-in, serial-out registers, gated clock inputs and an overriding clear input. The paralled-in or serial-in modes are established by the shift/load input. When high, the input enables the serial data input and couples the eight fill-flops for serial shifting with each clock pulse. When low, the paralled data inputs are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high edge of the clock pulse through a two-input positive NOR gate permitting one input to be used as a clock-enable or clock-inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. This allows the system clock to be free-running and the register can be stopped on command with the clock input. The clock-inhibit input should be changed to the high level only when the clock input is high. A buffered direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground

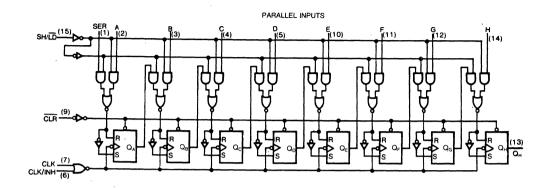
### **PIN CONFIGURATION**



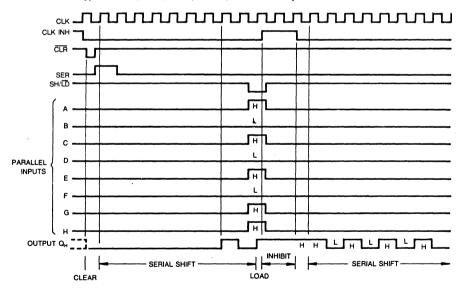
### **FUNCTION TABLE**

		In	puts			Inte	rnal	Output			
CLR	SH/	CLK	CLK	SER	Parallel	Outputs Q <sub>A</sub> Q <sub>B</sub>		Q <sub>H</sub>			
CLR	ĹĎ	INH	CLK	SEK	А Н						
L	Х	Х	Х	Х	Х	L	L	L			
Н	Х	L	L	Х	X	QAO	Q <sub>B0</sub>	Q <sub>H0</sub>			
Н	L	L	↑ ↑	Х	a h	а	b	h			
Н	Н	L	1	Н	X	н	Q <sub>An</sub>	QGn			
Н	Н	L	1	L	X	L	Q <sub>An</sub>	Q <sub>Gn</sub>			
Н	Х	Н	1	Х	X	GAO	Q <sub>B0</sub>	Q <sub>H0</sub>			

# **LOGIC DIAGRAM**



Typical Clear, Shift, Load, Inhibit, and Shift Sequences



# **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V)$ ±20 mA
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.

These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Supply Voltage, V <sub>CC</sub>	4.5V to 5.5V
DC Input & Output Voltages*, VIN, VOUT	OV to Vcc
Operating Temperature	

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . . Max 500 ns
\* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

# DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T <sub>a</sub> = 25°C		KS74HCTLS T <sub>a</sub> = -40°C to +85°C	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit	
			Тур	Guaranteed Limits				
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	٧	
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	0.8	V	
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	V	
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v	
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ	
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μА	
Additional Worst Case Supply Current	Δlcc	per input pin  V <sub>i</sub> =2.4V  other Inputs:  at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0µA		2.7	2.9	3.0	mA	

# AC ELECTRICAL CHARACTERISTICS (Input tr., tre6 ns), HCTLS166

Characteristic		Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		$KS74HCTLS$ $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$	$KS54HCTLS$ $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$	Unit
				Тур		Guaranteed Limits		
Maximum Clock Frequency		f <sub>max</sub>		40	30	25	20	MHz
Maximum Propagation Delay, CLR to Q <sub>H</sub>		t <sub>PHL</sub>	C <sub>1</sub> =50pF	22	30	37	45	ns
Maximum Propagation Delay, CLK to Q <sub>H</sub>		t <sub>PLH</sub>	оц-зорі	26	36	44	53	ns
		t <sub>PHL</sub>		26	35	44	53	
Minimum Pulse Width	CLR Low	t <sub>w</sub>		10	13	17	20	ns
	CLK High or Low	tw.		10	13	17	20	
Minimum Setup Time	SH/LD High before CLK	t <sub>su</sub>		10	13	· 17	20	,
	SER before CLK1			10	13	17	20	1
	CLK INH before CLK1			10	13	17	20	ns
	Data before SH/LD↑			10	13	17	20	
	CLR Inactive before CLK ↑			10	13	17	20	
Minimum Hold Time	SH/LD High after CLK1	t <sub>h</sub>		7	10	12	15	
	SER after CLK1			7	10	12	15	
	CLK INH after CLK1			7	10	12	15	ns
	Ďata after SH/LD↑			7	10	12	15	
	CLR Active after CLK1			7	10	12	15	
Maximum Input Capacitance		CIN		5				pF
Power Dissipation Capacitance*		C <sub>PD</sub>						рF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

# Synchronous 4-Bit Up/Down Decade and Binary Counters

#### **FEATURES**

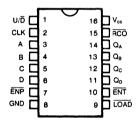
- Fully Synchronous Operation for Counting and Programming
- Internal Look Ahead for Fast Counting
- · Carry Output for N-bit Cascading
- Fully Independent Clock Circuit
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- . Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
   lot = 8 mA @ Vot = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATION



#### DESCRIPTION

These synchronous presettable counters feature an internal carry look-ahead for cascading in high-speed counting applications. The '168 is a decade counter and the '169 is a 4-bit binary counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock waveform.

These counters are fully programmable; that is, the outputs may each be preset to either level. The load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous application without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count enable inputs ( $\overline{\text{ENP}}$  and  $\overline{\text{ENT}}$ ) must be low to count. The direction of the count is determined by the level of the U/ $\overline{\text{D}}$  input. When U/ $\overline{\text{D}}$  is high, the counter counts up; when low, it counts down. Input  $\overline{\text{ENT}}$  is fed forward to enable the carry output. The ripple carry output ( $\overline{\text{RCO}}$ ) thus enabled will produce a low-level pulse while the count is zero (all inputs low) counting down or maximum (9 or 15) counting up. This low-level overflow carry pulse can be used to enable successive cascaded stages. Transition at  $\overline{\text{ENP}}$  or  $\overline{\text{ENT}}$  are allowed regardless of the level of the clock input.

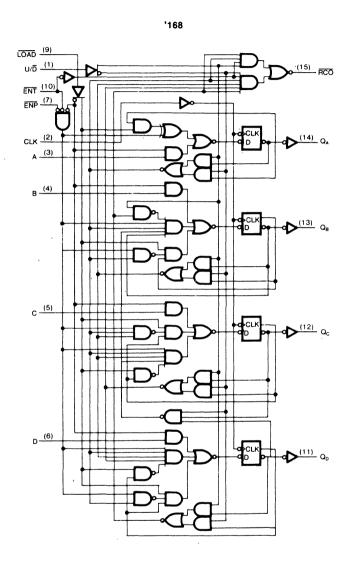
These counters feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, LOAD, U/D) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

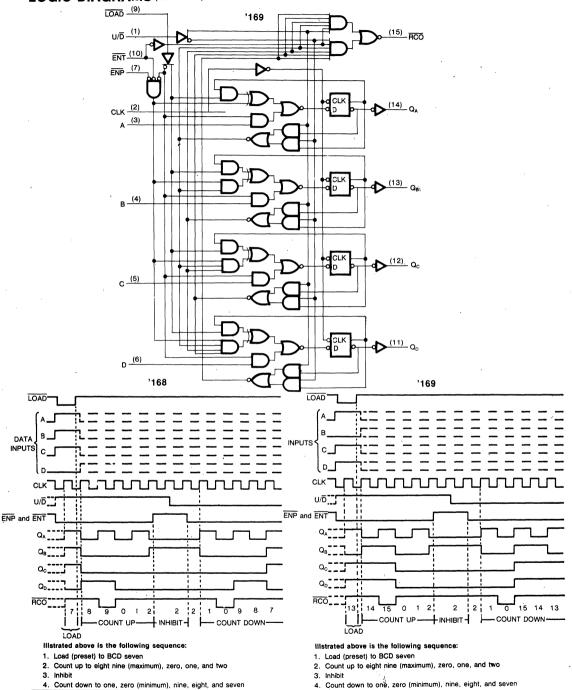
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### 5

# **LOGIC DIAGRAMS**



# LOGIC DIAGRAMS (Continued)





#### **FUNCTION TABLE**

OPERATING MODE			INP	OUTPUTS				
	CLK	U/D	ENP	ENT	LOAD	Dn	Qn	RCO
Parallel Load	1	X	Х	Х	1	i	L	·(1)
	1	Х	X	X	i	h	н	(1)
Count Up	1	h	1	ı	h	Х	Count Up	(1)
Count Down	1	1	1	ì	h	Х	Count Down	(1)
Hold	† †	X X	h X	X h	h h	X	Qn Qn	(1) ` H

H=HIGH voltage level steady state

h=HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition

L=LOW voltage level steady state

I=LOW voltage level one setup time prior to the LOW-to-HIGH clock transition

X=Don't care

q=Lower case letters indicate the state of the referenced output prior to the LOW-to-HIGH clock transition

↑=LOW-to-HIGH clock transition

#### NOTE:

 The RCO is LOW when ENT is LOW and the counter is at Terminal Count Terminal Count Up is (HHHH) and Terminal Count Down is (LLLL) for '169.

The RCO is LOW when ENT is LOW and the counter is at Terminal Count. Terminal Count Up is (HLLH) and Terminal Count Down is (LLLL) for '168.

# **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, $T_{stg} \dots -65$ °C to $+150$ °C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.

Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . . . . . . . 4.5V to 5.5V DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . 0V to  $V_{CC}$  Operating Temperature

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . Max 500 ns

\* Unused inputs must always be tied to an appropriate logic

voltage level (either V<sub>CC</sub> or GND)

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	aracteristic Symbol Test Conditions		T,	a = 25°C	KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit		
			Тур	yp Guaranteed Limits					
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	V		
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	0.8	V		
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	v		
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v		
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND	,	±0.1	±1.0	±1.0	μΑ		
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ		
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>1</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA		

# AC ELECTRICAL CHARACTERISTICS (Input tr, tre6 ns), HCTLS168, HCTLS169

Characteristic		Symbol	1 -		25°C 5.0V	KS74HCTLS T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%	KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> =5.0V ± 10%	Unit						
				Тур	p Guaranteed Limits		Limits							
Maximum Operation	ng Froguency	f <sub>max</sub>		35	30	25	20	MHz						
Maximum Propaga	ation Delay,	t <sub>PLH</sub>		26	35	44	52	ns						
CLK to RCO		t <sub>PHL</sub>	C <sub>L</sub> =50pF	26	35	44	52	115						
Maximum Propaga	ation Delay,	tpLH		17	22	28	33							
CLK to Ary Q	-	t <sub>PHL</sub>		17	22	28	33	ns						
Maximum Propagation Delay,		tPLH		15	20	25	30							
ENT to RCO		tpHL		15	20	25	30	ns						
Maximum Propaga	ation Delay,	tpLH		20	27	34	40							
U/D to RCO		t <sub>PHL</sub>		20	27	34	40	ns						
Minimum Pulse D CLK high or low	uration,	t <sub>w</sub>		12	16	20	24	ns						
	A, B, C or D			12	16	20	24	ns						
Minimum	ENP or ENT	t <sub>su</sub>		12	1.6	20	24							
Setup Time	LOAD	·su								12	16	20	24	ns ns
Before CLK↑	Ų/D̄			12	16	20	24	ns						
Minimum Hold Time, Data after CLK1		th	e.	-3	0	0	0	ns						
Maximum Input C	apacitance	CIN		5				pF						
Power Dissipation	Capacitance*	C <sub>PD</sub>						pF						

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} \ V_{CC}^2 \ f + I_{CC} \ V_{CC}$ .

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.



#### Objective Specifications

#### **FEATURES**

- Gated output control lines for enabling or disabling the outputs
- Fully independent clock for operation in parallel-load or hold modes
- · For application as bus buffer registers
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- . High-Drive-Current outputs:
- I<sub>OL</sub> = 24 mA @ V<sub>OL</sub> = 0.5V for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
   KSTANCTI St. 4000 Apr. 45500

KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### DESCRIPTION

These 4-bit registers contain D-type flip-flops with 3-state outputs, capable of driving highly-capacitive or low-impedance loads. This provides the device with the capability of being connected directly to and driving the bus lines in a busorganized system without need for interface or pull-up components.

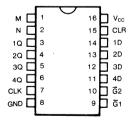
Gated enable inputs are provided for controlling the entry of data into the flip-flops. When both data-enable inputs are low, data at the D inputs are loaded into their respective flip-flops on the next positive transition of the buffered clock input. Gated output control inputs are also provided. When both are low, the normal logic states of the four outputs are available for driving the loads or bus lines. The outputs are disabled independently from the level of the clock by a high logic level at either output control input. The outputs then present a high impedance and neither load nor drive the bus line. Detailed operation is given in the function table.

To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable times are shorter than the average output enable times.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### PIN CONFIGURATION

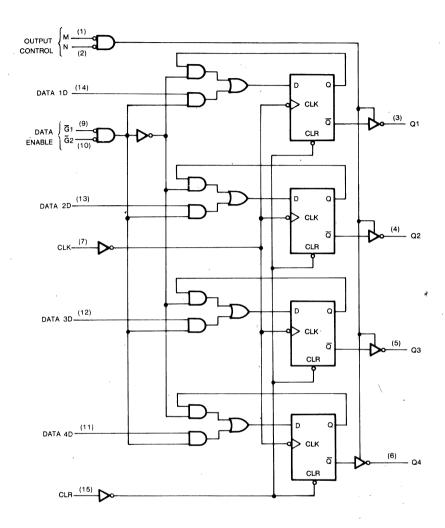


#### **FUNCTION TABLE**

	Input									
Clear	Clock	Data I	Enable	Data	Output					
		Ğ1	G2	D	_					
Н	Х	Х	Х	Х	L					
L	L	X	·X	Х	Qo					
L	<b>↑</b>	Н	X	Х	Q <sub>0</sub>					
L	<b>↑</b>	X	н	Х	Q <sub>0</sub>					
L	1	L	L	Ľ	L					
L	1	L	^ L	Н	Н					

When either  $\overline{M}$  or N (or both) is (are) high the output is disabled to the high-impedance state; however sequential operation of the flip-flops is not affected.

# **LOGIC DIAGRAM**



# **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±70 mA
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.
These are stress ratings only and functional operation
3 ,
of the device at or beyond them is not implied. Long ex-
posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Supply Voltage, V<sub>CC</sub> . . . . . . . . . . . 4.5V to 5.5V DC Input & Output Voltages\*, V<sub>IN</sub>, V<sub>OUT</sub> . . OV to V<sub>CC</sub> Operating Temperature

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . . . Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND).

# DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	pool Test Conditions $T_a = 25^{\circ}\text{C}$ $T_a = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$			KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit	
			Тур		Guaranteed Lim	its	Ì.
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	v
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	, 0.8	v
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-6mA$	V <sub>CC</sub> 4.2	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	l <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA



# AC ELECTRICAL CHARACTERISTICS (Input tr, tr 46 ns), HCTLS173

Characteristic Symbol		Con	Conditions <sup>†</sup>		Conditions <sup>†</sup>		25°C 5.0V	KS74HCTLS T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%	KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> =5.0V ± 10%	Unit
					Тур		Guaranteed	Limits		
Maximum Clo	ck Frequency	f <sub>max</sub>			45	30	25	20	MHz	
Maximum Propagation Delay, CLK to any Q		t <sub>PLH</sub>	C <sub>L</sub> =50pl C <sub>L</sub> =150		20 23	27 30	34 39	41 47		
		t <sub>PHL</sub>	C <sub>L</sub> =50pi		20 23	27 30	34 39	41 47	ns	
Maximum Pro		t <sub>PHL</sub>	C <sub>L</sub> =50pl	/	22 25	30 33	37 42	45 51	ns	
Maximum Output Enable Time, M or N to any Q		t <sub>PZH</sub>	$R_i = 1k\Omega$	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	18 21	25 28	. 31 36	37 43		
		t <sub>PZL</sub>	HL= IKW	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	18 21	25 28	<sup>2</sup> 31 36	37 43	ns	
Maximum Output Disable Time, M or N to any Q $t_{PHZ} = 1k\Omega, C_L = 5$		, C <sub>L</sub> =50pF	15 15	20 20	25 25	30	ns			
Minimum	CLK High or Low	tPLZ			10	13	17	20		
Pulse Width	CLR High	tw			10	13	17	20	ns	
Minimum	G1 and G2				15	20	25 .	30		
before CLKt	Data	tsu			8	11	14	1.7	ns	
	CLR Inactive				5	7	8	10		
Minimum Hold Time	G1 and G2	th			-3	0	0	0	ns	
After CLK1	Data	-				0	0	o		
Maximum Inpo	ut Capacitance	CIN			5				pF	
Maximum Ou Capacitance	tput	Cout	Output D	isabled	10				pF	
Power Dissip Capacitance		C <sub>PD</sub>							pF	

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

# KS54HCTLS 174/175 KS74HCTLS

# Hex/Quad D-type Flip-Flops with Clear

#### **FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
- IoL = 8 mA @ VoL = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### DESCRIPTION

The '174 contains six, and the '175 contains four D-type flip-flops all sharing a common clock and a common clear. The '174 features single rail outputs for every flip-flops whereas the '175 has complementary outputs.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### PIN CONFIGURATIONS

#### 174 CLR [ 1Q [ 15 1 6Q 14 6D 1D 2D С 13 5D 12 5Q 2Q 11 🔲 4D зр Г за Г 10 40 GND [ CLK

#### 175 CLR [ 16 Vcc 1Q 🔲 2 15 4Q 10 🗆 14 🔲 4Q 10 🛮 13 4D 2D 🗌 12 3D 2a 🗆 11 3Q 2Q 🗖 10 7 30 GND [ CLK

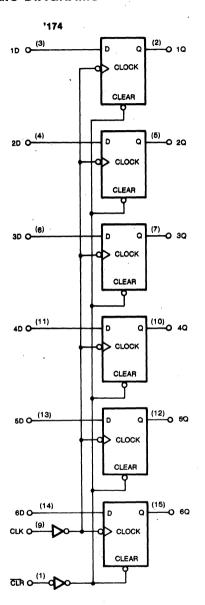
## **FUNCTION TABLE**

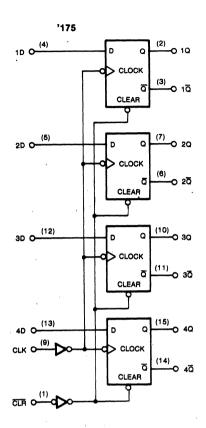
(Each Flip-Flop)

li	nputs	Outputs		
CLR	CLK	D	Q	Q١
L	·Χ	Х	L	Н
Н	1	Н	Н	L
Н	<b>↑</b>	L	L	Н
н	L	Χ	$Q_0$	$\overline{Q}_{0}$

† '175 only

# **LOGIC DIAGRAMS**





# **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V)$ ±20 mA
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
Vcc or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW

<sup>\*</sup> Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Supply Voltage, \	/cc	4.	5V to 5.5V
DC Input & Output	ıt Voltages*, V <sub>IN</sub> ,	Vout	OV to Vcc
Operating Tempe	rature		
Range	KS74HCTLS:	-40°C	to +85°C

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . . Max 500 ns

 Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T <sub>a</sub> = 25°C		KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	
		_	Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	V
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	О	0.1 0.26 0.39	0.1 0.33 0.5	. 0.1 0.4	V
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>i</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

# AC ELECTRICAL CHARACTERISTICS (Input tr., tre6 ns), HCTLS174, HCTLS175

Charac	Characteristic		Conditions <sup>†</sup>	T <sub>A</sub> =2 V <sub>CC</sub> =		KS74HCTLS  T <sub>A</sub> = -40°C to +85°C  V <sub>CC</sub> = 5.0V ± 10%	T <sub>A</sub> = -55°C to +125°C V <sub>CC</sub> =5.0V ± 10%	Unit	
-			,	Тур		Guaranteed	Limits		
Maximum Clock Frequency		f <sub>max</sub>		40	30	25	20	MHz	
Maximum Propaga	tion Delay,	tpLH	C <sub>L</sub> =50pF	22	30	37	45		
CLK to Q or Q		tpHL	OL-SOPP	22	30	37	35		
Maximum Propaga	tion Delay	t <sub>PLH</sub>		26	35	43	52	ns	
CLR to Q or Q	don Bolay,	tpHL		26	35	43	52	1	
Minimum Setup	Data			10	13	17	20		
Time before CLK1	CLR Inactive	t <sub>su</sub>		12	16	20	25	ns	
Minimum Hold Tim Data after CLK†	e,	t <sub>h</sub>		-3	0	<b>O</b> ,	0	ns	
Minimum Pulse	CLK High or Low	tw		10	13	17	20	ns	
Width CLR Low		·w	}	10	13	17	20	113	
Maximum Input Capacitace		CIN		5				рF	
Power Dissipation	Capacitance*	C <sub>PD</sub>	•					pF	

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

# KS54HCTLS **181** KS74HCTLS

# Arithmetic Logic Unit/ Function Generator

# Preliminary Specifications FEATURES

- Arithmetic operating modes:
  - Addition
  - Subtraction
  - Shift operand A one position
  - Magnitude comparison
  - Plus 12 other arithmetic operations
- · Logic function modes:
  - **Exclusive-OR** 
    - Comparator
  - AND, NAND, OR, NOR
  - Plus 10 other logic operations
- Full look-ahead for high-speed operations on long words
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current Outputs:
  - IOL = 8mA @ VOL = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATION

Во 🗗	24 □ V <sub>∞</sub>
ĀO 🏳 2	23 🗖 Ā1
s3 <b>□ 3</b>	22 D B1
S2 🗖 4	21 🗖 🗚
S1 🗗 5	20 🗖 🗟 2
so <b>⊈ 8</b>	19 🗖 🗚
C. 🗖 7	18 🗖 🛱 3
мЦв	17 🗖 Ğ
Fo 🗖 9	16 🗅 C.+4
F1 🗖 10	15DP
F2 🗖 11	14 A=B
GND 🗖 12	13 🗖 F3

#### DESCRIPTION

The '181 is an Arithmetic Logic Unit (ALU)/Function Generator that performs 16 binary arithmetic operations on two 4-bit words as shown in table 1 and 2. These operations are selected by the four functions select lines (SO, S1, S2, S3) and include addition, subtraction, decrement and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low level voltage to the mode control input(M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means of 2 cascadeoutputs (P and G) for the 4-bits in the package. When used in conjunction with HCTLS182, high-speed arithmetic operation can be performed. The typical addition times shown in table below illustrates how little is required for addition of longer words when full carry look-ahead is employed.

If high speed is not important, a ripple-carry input ( $C_n$ ) and a ripple-carry output ( $C_n+4$ ) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small lengths can be performed without external circuitry.

The '181 will accommodate active-high or active-low data, if the pin designations are interpreted as shown below.

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A-B-1, which requires and end-around or forced carry to provide A-B.

The '181 can also be utilized as a comparator. The A=B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of the equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A=B). The ALU should be in the subtract mode with  $C_n=H$  when performing the comparison. The A=B output is open-drain so that it can be wire-AND connected to give a comparison for more than four bits. The carry output ( $C_{n+4}$ ) can also be used to supply relative magnitude information. Again, the ALU should be placed in the subract mode by placing the function select input S3, S2, S1, S0 at L,H,H,L respectively.

These circuits have been d to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two boolean variables without the use of external circuitry. These logical functions are selected by use of the four function select inputs (S0, S1, S2, S3) with the mode control input (M) at a high level to disable the internal carry.

The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, OR and NOR functions.

Pin number	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-Low Data (Table1)	$\widetilde{A}_0$	$\overline{\mathbf{B}}_{0}$	Ā <sub>1</sub>	B <sub>1</sub>	$\overline{A}_2$	B <sub>2</sub>	Ãз	В̃з	Fo	F <sub>1</sub>	F <sub>2</sub>	F <sub>3</sub>	Cn	C <sub>n</sub> +4	P	G
Active-High Data (Table 2)	Ao	Bo	A <sub>1</sub>	B <sub>1</sub>	A <sub>2</sub>	B <sub>2</sub>	А3	Вз	Fo	F <sub>1</sub>	F <sub>2</sub>	F <sub>3</sub>	<b>C</b> <sub>n</sub>	C̄ <sub>n</sub> +4	Х	Υ



#### **ALU SIGNAL DESIGNATION**

The '181 can be used with the signal designations.

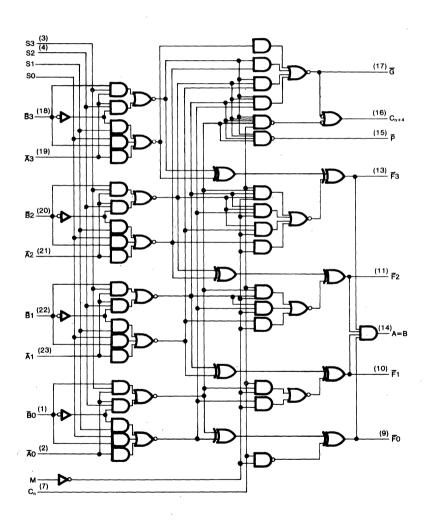
The logic functions and arithmetic operations obtained with signal designations as in Table 1.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels

allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

# LOGIC DIAGRAM





#### O Table 1

	Sala	ction			Active	-Low Data
	0010			M = H	M = L; Arith	metic Operations
<b>S</b> 3	S2	<b>S</b> 1	S1 S0 Logic C <sub>n</sub> =L (no carry)			C <sub>n</sub> =H (with carry)
L	L	L	L	F=Ā	F=A Minus 1	F=A
Ł	L	L	н	F=ĀB	F=AB Minus 1	F=AB
L	L	н	L	F=A + B	F=AB Minus 1	F=AB
L	L	н	н	F=1	F=Minus 1 (2's Comp)	F=Zero
L	н	L	L	F=A+B	F=A Plus (A + B)	F=A Plus (A + B) Plus 1
L	н	L	н	F=B	F=AB Plus (A + B)	F=AB Plus (A + B) Plus 1
L	н	н	L	F=Ā⊕B	F=A Minus B Minus 1	F=A Minus B
L	Н	н	н	F=A + B	F=A + B	F=(A + B) Plus 1
н	L	L	L	F=ĀB	F=A Plus (A + B)	F=A Plus (A + B) Plus 1
н	L	L	н	F=A⊕B	F=A Plus B	F=A Plus B Plus 1
Н	L	н	L	F=B	F≃AB Plus (A + B)	F=AB Plus (A + B) Plus 1
Н	· L	н	н	F=A + B	F=(A + B)	F=(A + B) Plus 1
Н	Н	L	L	F=0	F=A Plus A*	F=A Plus A Plus 1
Н	Н	L	Н	F=AB	F=AB Plus A	F=AB Plus A Plus 1
Н	Н	Н	L	F=AB	F=AB Plus A	F=AB Plus A Plus 1
Н	н	н	н	F=A	F=A	F=A Plus 1

#### O Table 2

-	Sala	ction			Active-High Data					
	3616	CHOII		M = H	M = L; Arithmetic Operations					
<b>S</b> 3	S2	S1	S1 S0 Logic $\overline{C}_n = L$ (no carry)		1 "	C <sub>n</sub> =H (with carry)				
L	L	L	L	F=Ā	F=A	F=A Plus 1				
L	L	L	Н	$F = \overline{A + B}$	F=A + B	F=(A + B) Plus 1				
L	L	н	L	F=ĀB	F=A + B	F=(A + B) Plus 1				
L	L	н	н	F=0	F=Minus 1 (2's Comp)	F=Zero				
L	н	L	L	F=AB	F=A Plus AB	F=A Plus AB Plus 1				
L	н	L	н	F≕B	$F=(A + B) Plus A\overline{B}$	F=(A + B) Plus AB Plus 1				
L	н	Н	L	F=A⊕B	F=A Minus B Minus 1	F=A Minus B				
L	н	н	H	F=AB	F=AB Minus 1	F=AB				
н	L	L	L	F=Ā + B	F=A Plus AB	F=A Plus AB Plus 1				
н	L	L	н	F=A⊕B	F=A Plus B	F=A Plus B Plus 1				
н	L	н	L	F=B	F=(A + B) Plus AB	F=(A + B) Plus AB Plus 1				
н	L	н	н	F=AB	F=AB Minus 1	F=AB				
н	н	L	L	F=1	F=A Plus A*	F=A Plus A Plus 1				
Н	Н	L	Н	F=A + B	F=(A + B) Plus A	A=(A + B) Plus A Plus 1				
Н	Н	н	L	F=A + B	F=(A + B) Plus A	$F=(A + \overline{B})$ Plus A Plus 1				
Н	н	н	н	F=A	F=A Minus 1	F=A				

<sup>\*</sup> Each bit is shifted to the next more significant position

# **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 70 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . . . Max 500 ns

 Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

# DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T	<sub>a</sub> = 25°C	KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V <sub>ОН</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	V.
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	IIN	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μА
Additional Worst Case Supply Current	Δlcc	per input in V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0 、	mA



# INPUT PAIRS HIGH/NOT HIGH TEST TABLE FUNCTION INPUTS: S2 = M = 4.5 V, S0 = S1 = S3 = 0 V

PARAMETER	INPUT UNDER	OTHER SAMI		OTHER DA	TA INPUTS	OUTPUT	OUTPUT WAVEFORM	
	TEST	APPLY 4.5 V APPLY GND		APPLY 4.5 V APPLY GND		TEST		
tpLH	Āi	Bi	None	Remaining	Remaining	P	In-Phase	
tPHL		ы	None	Ā, C <sub>n</sub>	B	-		
tPLH	Bi	Ā:	Ai None Remaining Remaining		Remaining	P	In-Phase	
t <sub>PHL</sub>	Ы	^1	None.	B̄, C <sub>n</sub>	Ā		in-Friase	
t <sub>PHL</sub>	Āi	Bi	Remaining Remaining		0.14	Out-of-Phase		
t <sub>PHL</sub>	<b>A</b> I	ы	None	Ā, C <sub>n</sub>	B	C <sub>n</sub> +4	Out-or-Friase	
t <sub>PLH</sub>	<u> </u>	Ā:	None	Remaining	Remaining	0.14	Out-of-Phase	
t <sub>PHL</sub>	Bi Āi		None	B̄, C <sub>n</sub>	Ā	C <sub>n</sub> +4	Out-of-Pilase	

#### PARAMETER MEASUREMENT INFORMATION

SUM MODE TEST TABLE FUNCTION INPUTS: S0 = S3 = 4.5 V, S1 = S2 = M = 0 V

PARAMETER	INPUT UNDER	OTHER SAME		OTHER DA	TA INPUTS	OUTPUT UNDER	OUTPUT WAVEFORM	
	TEST	APPLY 4.5 V APPLY GND		APPLY 4.5 V	APPLY GND	TEST		
t <sub>PLH</sub>	Āi	Bi	None	Remaining	Cn	· Fi	In-Phase	
t <sub>PHL</sub>	<b>^</b> '	J.	None	A and B	O <sub>n</sub>	''	iii i iiase	
tpLH	Bi	Āi	None	Remaining	Cn	Fi	In-Phase	
t <sub>PHL</sub>	ы	^'	None	A and B	O <sub>n</sub>	''	III-i ilase	
t <sub>PLH</sub>	Āi	Bi	None	None	Remaining	P	In-Phase	
t <sub>PHL</sub>	<b>A</b>	ы	None	None	$\overline{A}$ and $\overline{B}$ , $C_n$	F	III-Filase	
t <sub>PLH</sub>	Bi	Āi	None	None	Remaining	P	In-Phase	
t <sub>PHL</sub>		^'	None	Nume	A and B, C <sub>n</sub>		iii-r iiase	
tpLH	Āi	None	Bi	Remaining	Remaining	Ğ	In-Phone	
t <sub>PHL</sub>	7	None	Di Di	₿	Ā, Cn		in-Frione	
t <sub>PLH</sub>	Bi	None	Āi	Remaining Remaining		G	In-Phase	
t <sub>PHL</sub>	ы	None	^'	B	Ā, Cn	G	III-riidse	
t <sub>PLH</sub>		None	None	All	All	Any F	In-Phase	
t <sub>PHL</sub>	C <sub>n</sub>	None	None	Ā	B	or C <sub>n</sub> +4	iii-Filase	
tpLH	Ãi	None	Bi	Remaining	Remaining	Cn+4	Out-of-Phase	
t <sub>PHL</sub>	<b>^</b>	None	Di	B	Ā, C <sub>n</sub>	On T T	Cut-of-r nase	
tpLH	Bi	None	Āi	Remaining	Remaining	0.14	Out-of-Phase	
tPHL		None	Ai Ai	B	A, C <sub>n</sub>	C <sub>n</sub> +4	Gut-or-r riase	

# AC ELECTRICAL CHARACTERISTICS (Input tr., tr 6 ns), HCTLS181

Characteristic	Symbol	Conditions <sup>†</sup>	T <sub>a</sub> = 2 V <sub>CC</sub> =			KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> =5.0V± 10%	Unit
		C <sub>L</sub> = 50pF	Тур		Guarantee	d Limits	
Propagation Delay,	t <sub>PLH</sub>	M=0V	14	18	23	27	ns
C <sub>n</sub> to C <sub>n</sub> +4	tpHL	Sum or Diff Mode	14	18	23	27	113
Propagation Delay,	tplH	M=S1=S2=0V	20	28	35	42	ns
A or B to C <sub>n</sub> +4	t <sub>PHL</sub>	S0=S3=4.5V	20	28	35	42	
Propagation Delay,	t <sub>PLH</sub>	M=S0=S3=0V	25	34	42	50	ns
$\overline{A}$ or $\overline{B}$ to $C_n+4$	t <sub>PHL</sub>	S1=S2=4.5V	25	34	42	. 50	110
Propagation Delay	t <sub>PLH</sub>	M=S1=S2=0V	22	31	39	47	ns
A or B to G	t <sub>PHL</sub>	S0=S3=4.5V	22	31	39	47	110
Propagation Delay	t <sub>PLH</sub>	M=S0=S3=0V	23	32	40	48	ns
Ā or B to G	t <sub>PHL</sub>	S1=S2=4.5V	23	32	40	48	110
Propagation Delay	tplH	M=S0=S3=0V	25	34	43	51	ns
A or B to P	tpHL	S1=S2=4.5V	25	34	43	51	113
Propagation Delay	t <sub>PLH</sub>	M=S1=S2=0V	25	34	42	50	ns
A or B to P	t <sub>PHL</sub>	S0=S3=4.5V	25	34	42	50	113
Propagation Delay	t <sub>PLH</sub>	M=S1=S2=0V	25	34	42	50	ns
A or B to F	· tphL	S0=S3=4.5V	25	34	42	50	113
Propagation Delay	t <sub>PLH</sub>	M=S0=S3=0V	25	34	42	50	ns
A or B to Fi	tpHL	S1=S2=4.5V	25	34	42	50	113
Propagation Delay	tplH	M=S1=S2=0V	25	34	42	50	ns
A or B to F	tpHL	S1=S2=4.5V	25	34	42	50	113
Propagation Delay	t <sub>PLH</sub>	M=4.5V	20	29	35	42	ns
A or B to A=B	tpHL	101-4.50	20	28	35	42	113
Propagation Delay	tplH	M=S0=S3=0V	25	34	42	50	ns
A or B to A=B	tpHL	S1=S2=4.5V	25	34	42	50	113
Propagation Delay	tplH		20	28	35	42	ns
Cn to any F	tpHL		20	28	35 ,	42	113
Input Capacitance	Cin		5				pF
Power Dissipation Capacitance*	C <sub>PD</sub>						pF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} \ V_{CC}^2 \ f + I_{CC} \ V_{CC}$ .
† For AC switching test circuits and timing waveforms see section 2.



#### PARAMETER MEASUREMENT INFORMATION

# LOGIC MODE TEST TABLE FUNCTION INPUTS: S1 = S2 = M = 4.5 V, S0 = S3 = 0 V

PARAMETER	INPUT UNDER	OTHER SAMI		OTHER DA	TA INPUTS	OUTPUT UNDER	OUTPUT WAVEFORM	
	TEST	ST APPLY 4.5 V APPLY GND		APPLY 4.5 V	APPLY GND	TEST		
t <sub>PLH</sub>	Āi	Bi	None	None	Remaining	Fi	Out-of-Phase	
t <sub>PHL</sub>		ы	None	None	A and B, C <sub>n</sub>	-	Out-or-riase	
t <sub>PLH</sub>	Bi	Āi	None	None	Remaining	Fi	Out-of-Phase	
` t <sub>PHL</sub>	) DI	AI Noile		140116	Ā and B, C <sub>n</sub>	"	Out-or-i nase	

# INPUT BITS EQUAL/NOT EQUAL TEST TABLE FUNCTION INPUTS: S0 = S3 = M = 4.5 V, S1 = S2 = 0 V

PARAMETER	INPUT UNDER	OTHER SAMI		OTHER DA	TA INPUTS	OUTPUT	OUTPUT WAVEFORM	
	TEST	APPLY 4.5 V APPLY GND		APPLY 4.5 V	APPLY GND	TEST		
t <sub>PLH</sub>	Āi	Bi	None	Remaining	None	Ē	Out-of-Phase	
t <sub>PHL</sub>	_ ^'	ы	None	$\overline{A}$ and $\overline{B}$ , $C_n$	None		Out-or-riase	
tpLH	Bi	Āi	None	Remaining	None	P	Out-of-Phase	
tpHL	) Di	^'	MOUE	A and B, C <sub>n</sub>	None		Out-oi-Filase	
tpLH	Āi	None	Bi	Remaining	None	Ē	In-Phase	
t <sub>PHL</sub>	7	None	ы	Ā and B̄, C <sub>n</sub>	None	_	iii-riiase	
tpl.H	Bi	None	Āi	Remaining	None	ē	In-Phase	
t <sub>PHL</sub>	) bi	None	<b>^</b> '	A and B, C <sub>n</sub>	Hone		ii i i i i i i i i i i i i i i i i i i	
t <sub>PLH</sub>	Āi	Bi	None	Remaining	None	Cn+4	In-Phase	
t <sub>PHL</sub>	\ \frac{1}{2}	B1	None	Ā and B̄, C <sub>n</sub>	None	On 1 4	mi nasc	
tplH ,	Bi	Āi	None	Remaining	None	Cn+4	in-Phase	
tpHL	) Bi	^'	None	A and B, C <sub>n</sub>	None	Un T 7	III-I-IIase	
t <sub>PLH</sub>	Āi	None	Bi	Remaining	None	Cn+4	Out-of-Phase	
t <sub>PHL</sub>	<b>^</b>	None	DI	Ā and B, C <sub>n</sub>	None	Un+4	Out-or-rhase	
t <sub>PLH</sub>	Bi	None	Āi	Remaining	None	0.14	Out-of Phase	
tpHL	1 51	None	, AI .	A and B, Cn	NOUE	C <sub>n</sub> +4		

#### DIFF MODE TEST TABLE FUNCTION INPUTS: S1 = S2 = 4.5 V, S0 = S3 = M = 0 V

PARAMETER	INPUT	OTHER SAMI		OTHER DA	TA INPUTS	OUTPUT UNDER	OUTPUT WAVEFORM	
	TEST	APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND	TEST		
tрын	Āi	None	Bi	Remaining	Remaining	Fi	In-Phase	
t <sub>PHL</sub>	Α'	None	J.	· Ā	B, C <sub>n</sub>	''	III I IIdae	
t <sub>PLH</sub>	Bi	Āi	None	Remaining	Remaining	Fi	Out-of-Phase	
t <sub>PHL</sub>	, G	~	None	Ã	B, C <sub>n</sub>	''	Out-of-1 flase	
t <sub>PLH</sub>	Āi	None	Bi	None	Remaining	P	In-Phase	
t <sub>PHL</sub>	7	None	<b>D</b> ,	None	$\overline{A}$ and $\overline{B}$ , $C_n$		III-Filase	
t <sub>PLH</sub>	Bi	Āi	None	None	Remaining	P	Out-of-Phase	
t <sub>PHL</sub>	В	^'	None	None	$\overline{A}$ and $\overline{B}$ , $C_n$			
t <sub>PLH</sub>	Āi	Bi	None	None	Remaining	G	In-Phase	
t <sub>PHL</sub>	7	D,	Hone	None	$\overline{A}$ and $\overline{B}$ , $C_n$	ŭ	III-I IIaoc	
t <sub>PLH</sub>	Di	Bi	None	Āi	None	Remaining	G	Out-of-Phase
t <sub>PHL</sub>	, Di	None	^'	None	A and B, C <sub>n</sub>	ŭ	Out-of-Friase	
t <sub>PLH</sub>	Āi .	None	Bi	Remaining	Remaining	A=B	In-Phase	
t <sub>PHL</sub>		140116	Di Di	Ā	B, C <sub>n</sub>	7-5	III-T Hase	
t <sub>PLH</sub>	Bi	Āi	None	Remaining	Remaining	A=B	Out-of-Phase	
t <sub>PHL</sub>	, Di	<u> </u>	None	Ā	B, C <sub>n</sub>	7-0	Out-of-Friase	
t <sub>PLH</sub>	Cn	None	None	All	None	C <sub>n</sub> +4	In-Phase	
t <sub>PHL</sub>	On	None	·	$\overline{\mathbf{A}}$ and $\overline{\mathbf{B}}$	None	or any F	m-rnase	
t <sub>PLH</sub>	Āi	Bi	None	None	Remaining	Cn+4	Out-of-Phase	
t <sub>PHL</sub>	~	ы	NOHE	NOHE	A, B, C <sub>n</sub>	On T -	Out-Oi-Filase	
t <sub>PLH</sub>	Bi	None	āi	None	Remaining	Cn+4	In-Phase	
t <sub>PHL</sub>	ы	None	di	None	A, B, C <sub>n</sub>	Cn T4	, in-rhase	

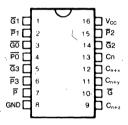
#### **FEATURES**

- Compatible Carry Functions for direct ALU connection
- Cascadable to perform look-ahead across n-bit adders.
- High output current drive: IoL = 8mA @ VoL = 0 5V
- . Low power consumption characteristic of CMOS
- Direct interface capability to TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATION



#### DESCRIPTION

The '182 is a high-speed, look-ahead carry generator, capable of anticipating a carry across four binary adders or group of adders. These devices can be cascaded to perform full look-ahead across n-bit adders. Carry, generate-carry, and propagate-carry functions are provided as shown in the pin designation table.

When used in conjuction with the AHCT181 arithmetic logic unit, these generators provide high-speed carry look-ahead capability for any word length. Each 182 generates the look-ahead (anticipated carry) across a group of four ALUs and, in addition, other carry look-ahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to n-bits. The method of cascading circuits to perform multi-level look-ahead is illustrated under typical application data.

Carry input and output of the ALU's are in their true from, and the carry propagate (P) and carry generate (G) are in negated form; therefore, the carry functions (inputs, outputs, generate, and propagate) of the look-ahead generators are implemented in the compatible forms for direct connection to the ALU. Reinterpretations of carry functions, as explained on the 181 data sheet are also applicable to and compatible with the look-ahead generator. Positive logic equations for the 182 are

#### PIN DESIGNATIONS

Designation	Pin No	Function
<u>G</u> 0,G1,G2,G3	3,1,14,5	Active Low Carry Generate Inputs
P0,P1,P2,P3	4,2,15,6	Active Low Carry Propagate Inputs
Cn	13	Carry Input, Active High
Cn+x, Cn+y, Cn+z	12,11,9	Carry Outputs
G	10	Active Low Carry Generate Output
P	7	Active Low Carry Propagae Output
Vcc	16	Supply Voltage
GND 8		Ground

#### **FUNCTION TABLES**

FOR G OUTPUT

	OUTPUT						
ĞЗ	Ğ2	G1	GO	P3	₽2	P1	Ğ
L	Х	Χ	Х	Х	X.	Х	L
X	L	Χ	Χ	L	Х	Х	Ŀ
Х	X	L	Х	L	L	Х	L
Х	Χ	Χ	L	L	L	L	L
	All other combinations						

FOR P OUTPUT							
INPUTS	OUTPUT						
P3 P2 P1 P0	P						
LLLL	L						
All other combinations	н						

FOR	FOR C <sub>n</sub> + x OUTPUT							
11	<b>IPUT</b>	OUTPUT						
GŌ	ΡŌ	C <sub>n</sub> + x.						
L	Х	Х	Н					
X	L	Н	н					
	ll othe binat	L						

Cn+y OUTPUT

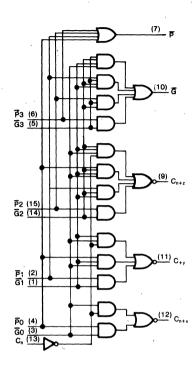
		OUTPUT					
G1	G0	₽1	PO	Cn	C <sub>n+y</sub>		
L	×	Х	×	Х	н		
X	L	L	X	Х	н		
X	Х	L	L	Н	Н		
	All other combinations						

Cn+z OUTPUT

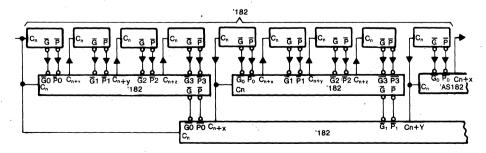
	OUTPUT							
G2	C <sub>n</sub> +z							
L	Х	Х	Х	Х	×	Х	Н	
X	L	Х	L	Х	Χ	Х	н	
X	Х	L	L	L	Χ	χ.	H	
х	Х	X	L	L	L	Н	н	
	All other combinations							

H = high-level, L = low level, X = dont' care Any inputs not shown in a given table are don't care with respect to that output.

# LOGIC DIAGRAM



#### Figure; THE '182 IN A 64-BIT LOOK-AHEAD CARRY CIRCUIT



## **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Supply Voltage, V <sub>CC</sub>	4.5V to 5.5V
DC Input & Output Voltages*, VIN, VOUT	OV to Vcc
Operating Temperature	

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

# DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	rmbol Test Conditions		= 25°C	KS74HCTLS T <sub>a</sub> = -40°C to +85°C	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	VIH			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	l <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μА
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin  V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0µA		2.7	2.9	3.0	mA

# AC ELECTRICAL CHARACTERISTICS (Input $t_r$ , $t_f \leqslant 6$ ns), HCTLS182

Characteristic	Symbol	Conditions†	T <sub>a</sub> =25°C V <sub>CC</sub> =5.0V		KS74HCTLS T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%	KS54HCLTS  T <sub>a</sub> = -55°C to +125°C  V <sub>CC</sub> = 5.0V ± 10%	Unit
			Typ Guaranteed Limits				
Propagation Delay Pi or Gi to	tpLH	C <sub>1</sub> =50pF	19	26	32	39	ns
C <sub>n+x</sub> C <sub>n+y</sub> , C <sub>n+z</sub>	t <sub>PHL</sub>	OL-COP.	19	26	32	39	113
Propagation Delay	tpLH	C <sub>L</sub> =50pF	19	26	32	39	ns
Pior Ĝi to Ĝ	tPHL		19	26	32	39	
Propagation Delay C <sub>n</sub> to	tpLH	C <sub>i</sub> =50pF	25	27	34	41	ns
$C_{n+x}$ , $C_{n+y}$ , $C_{n+z}$	t <sub>PHL</sub>	OL-30bi	25	27	34	41	
Propagation Delay	tpLH	C <sub>I</sub> =50pF	15	20	25	30	ns
Pi to P	tpHL	CL-30bi	15	20	25	30	110
Input Capacitance	Cin		5		,		pF
Power Disipation Capacitance*	CPD						pF

<sup>.\*</sup>C<sub>PD</sub> determines the no-load dynamic power dissipation: PD=C<sub>PD</sub>  $V_{CC}^2$  f+  $I_{CC}$   $V_{CC}$ .

<sup>&</sup>lt;sup>†</sup>For Acc switching test circuits and timing waveforms see section 2.

#### **FEATURES**

- · For use in high-speed wallace-tree summing
- · Fast addition operation
- Low power consumption characteristic of CMOS
- High output current drive: I<sub>OL</sub> = 8mA @ V<sub>OL</sub> = 0.5V
- Direct interface capability with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V

KS54HCTLS: -55°C to +125°C

- Characterized for operation over industrial and military temperature ranges:
   KS74HCTLS: -40°C to +85°C
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

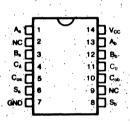
#### DESCRIPTION

The '183 is a dual full adder features an individual carry output from each bit for use in multiple-input, carry-save techniques to produce the true sum and true carry outputs with no more than 2 gate delays.

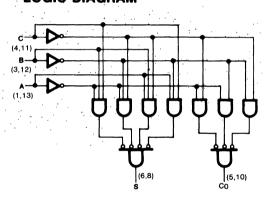
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### PIN CONFIGURATION



# LOGIC DIAGRAM



## **FUNCTION TABLE**

(Each Half)

	Inputs	Output		
Α	В	С	S	C <sub>o</sub>
L	L	L	L	L
н	L	L	н	L
L	н	L	н	L
L	L	н	н	L
н	н	L	L	н
Н	L	н	L	н
L	н	н	L	н
н	н	Н	Н	Н

#### Absolute Maximum Ratings\*

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, $I_{IK}$ ( $V_I < -0.5V$ or $V_I > V_{CC} +0.5V$ ) $\pm 20$ mA
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V)$ ±20 mA
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±35 mA
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, P <sub>d</sub> † 500 mW

Power Dissipation Per Package, Pd<sup>†</sup> . . . . . . 500 mW
 \* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation

of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:

Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . . . . . . . . 4.5V to 5.5V DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . OV to  $V_{CC}$  Operating Temperature

Range KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . Max 500 ns

\* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

# DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	Т	a = 25°C	KS74HCTLS T <sub>a</sub> = -40°C to +85°C	KS54HCTLS $T_a = -55^{\circ}C$ to $+125^{\circ}C$	Unit
			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V <sub>OH</sub>	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> =-20μA I <sub>O</sub> =-4mA	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> -0.1 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	VoL	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> =20µA I <sub>O</sub> =4mA I <sub>O</sub> =8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	<b>V</b>
Maximum Input Current	lin	VIN=VCC or GND		±0.1	±1.0	±1.0	μА
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =OμA		2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	·Δlcc	per input in  V <sub>1</sub> =2.4V  other inputs: at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0µA		2.7	2.9	3.0	mA

#### AC ELECTRICAL CHARACTERISTICS (Input tr., tre 6 ns), HCTLS 183

Characteristic ,	Symbol	Conditions <sup>†</sup>	T <sub>a</sub> = 2 V <sub>CC</sub> =	5°C 5.0V	KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$	$K\$54HCTLS$ $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$	Unit
			Тур		Guarantee	d Limits	
Propagation Delay	tpLH	C <sub>I</sub> = 50pF	15	22	27	33	ns
Propagation Delay	t <sub>PHL</sub>	C[=30pi	17	23	29	35	113
Input Capacitance	C <sub>IN</sub>						pF
Power dissipation Capacitance*	CPD					,	pF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.



# KS54HCTLS 190 KS74HCTLS

# Synchronous 4-Bit Up/Down Decade Counters

#### **FEATURES**

- . Single down/up count control line
- Look-ahead circuitry enhances speed of cascaded counters
- · Fully synchronous in count modes
- Asynchronously presettable with load control
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:

IoL = 8 mA @ VoL = 0.5V

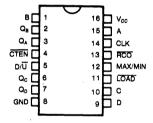
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

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 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATION



#### **FUNCTION TABLE**

OPERATING MODE		OUTPUTS				
OPERATING MODE	LOAD	D/Ū	CTEN	CLK	Input	On
parallel load	L	Х	х	Х	L	L
	L	X	х	Х	н	н
count up	н	′ L	1	†	Х	count up
count down	н	н	1	t	X	count down
hold (do nothing)	Н	X	н	Х	X	no change

RCO AND MAX/MIN FUNCTION TABLE

INPUTS			TER	MINAL C	OUTPUTS			
D/Ū	CTEN	CLK	QA	QB	Qc	Qp	MAX/MIN	RCO
н	н	×	н	х	X	Н	L	н
L	H	X	н	X	X	н	н	н
L	L	T	н	X	X	н	1 TL	Т
L	H	X	L	L	L	L	1 6	н
н	н	х	L	L	L	L	н	н
н	L	Ъ	L	L	L	L	17.	Л

- H = HIGH voltage leve
- L = LOW voltage level
- I = LOW voltage level one setup time prior to the LOW-to-HIGH CLK transition
- X = Don't care
- t = LOW-to-HIGH CLK transition
- ∪ = one LOW level pulse
- L = MAX/MIN goes LOW ON A LOW-to-HIGH CLK transition

#### DESCRIPTION

These are high-speed synchronous reversible 4-bit decade counters. Synchronous counting operation is provided by having all flip-flops clocked simultaneously so that the outputs change with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with a synchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered on a low-to-high-level transition of the clock input if the enable input  $(\overline{CTEN})$  is low. A high at  $\overline{CTEN}$  inhibits counting. The direction of the count is determined by the level of the down/up  $(D/\overline{U})$  input. When  $D/\overline{U}$  is low, the counter counts up and when  $D/\overline{U}$  is high, it counts down.

These counters feature a fully independent clock circuit. Changes at the control inputs  $(\overline{CTEN} \text{ and } D/\overline{U})$  that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter will be dictated solely by the condition meeting the stable setup and hold times.

These counters are fully programmable; that is, the outputs may each be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

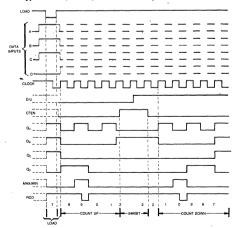
Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock while the count is zero (all outputs low) counting down or maximum (9 or 15) counting up. The ripple clock output produces a low-level output pulse under those same conditions but only while the clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

# 

#### Typical load, count, and inhibit sequences



#### Sequence;

- (1) Load (preset) to BCD seven.
- (2) Count up to eight, mine(maximum) zero, one, and two.
- (3) Inhibit
- (4) Count down to one, zero (minimum), nine, egiht, and seven

NOTE A: Clear overrides load data, and count inputs.

Note B:When count up, count down input must be high;
when counting down, countup intput must be high.

#### **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Supply Voltage, V<sub>CC</sub> . . . . . . . . . . . . 4.5V to 5.5V DC Input & Output Voltages\*, V<sub>IN</sub>, V<sub>OUT</sub> . . OV to V<sub>CC</sub> Operating Temperature

 Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

# DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	a = 25°C	KS74HCTLS $T_a = -40$ °C to +85°C	KS54HCTLS $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	VIH			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	<b>^</b>
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-4m A$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	Vol	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> =20µA I <sub>O</sub> =4mA I <sub>O</sub> =8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	IIN	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0µA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	ΔΙσο	per input in  V <sub>I</sub> =2.4V  other Inputs: at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0µA		2.7	2.9	3.0	mA

# AC ELECTRICAL CHARACTERISTICS (Input tr, tre6 ns), HCTLS 190

Characteristic		Symbol	Conditions†	Ta=2 V <sub>CC</sub> =		KS74HCTLS  T <sub>a</sub> = -40°C to +85°C  V <sub>CC</sub> = 5.0V ± 10%	KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> =5.0V± 10%	Unit
				Тур		Guaranteed	l Limits	
Maximum Clock	Maximum Clock Frequency		· .	30	20	16	14	MHz
Maximum Propa	agation Delay,	tpLH		30	40	50	60	ns
LOAD to any C	)	t <sub>PHL</sub>		30	40	50	60	
Maximum Propa		tpLH		27	36	45	64	ns
A,B,C, D to an	y Q	t <sub>PHL</sub>		27	36	. 45	54	
Maximum Propa	agation Delay,	T <sub>PLH</sub>		17	22	28	33	ns
CLK to RCO		t <sub>PHL</sub>		17	22	28	33	
Maximum Propa	agation Delay,	tpLH		23	30	37	45	ns
CLK to any Q		t <sub>PHL</sub>	C <sub>L</sub> =50pF	23	30	37	45	
Maximum Propa	agation Delay,	tpLH	CL-20br	35	47	59	70	ns
CLK to MAX/MIN		t <sub>PHL</sub>		35	47	59	70	1.0
Maximum Propa	Maximum Propagation Delay,			33	45	56	67	ns
D/U to RCO	•	tpHL		33	45	56	67	115
Maximum Propa	agation Delay,	t <sub>PLH</sub>		25	33	41	50	
D/U to MAX/MI	N	t <sub>PHL</sub>		25	33	41	50	
Maximum Propa	agation Delay,	tpLH		25	33	41	50	ns
CTEN to RCO	•	t <sub>PHL</sub>		25	33	41	. 50	115
Minimum	CLK High or Low	t <sub>w</sub>		13	17	21	25	ns
Pulse Width	LOAD Low	·w		13	17	21	25	113
	Data before LOAD1			10	13	17	20	
Minimum	CTEN before CLK†	tsu		20	26	34	40	ns
Setup Time	D/Ū before CLKf	tsu		10	13	17	20	1115
	LOAD Inactive before CLK1			15	20	25	30	
Minimum Hold	Data after LOAD1			1	3	5	5	
Time	CTEN after CLK1	th		-3	0	0	0	ns
	D/Ū after CLK†			-3	0	0	0	
Maximum Input	Capacitance	CiN		5			,	pF
Power Dissipati	on Capacitance*	CPD		80				pF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

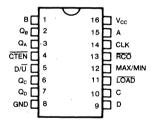
#### **FEATURES**

- . Single down/up count control line
- Look-ahead circuitry enhances speed of cascaded counters
- · Fully synchronous in count modes
- Asynchronously presettable with load control
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
   A Company of the Company of t

 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5 \text{V}$ 

- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
   KS74HCTLS: -40°C to +85°C
- KS54HCTLS: -55°C to +125°C
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATION



#### **FUNCTION TABLE**

OPERATING MODE		OUTPUTS				
OPERATING MODE	LOAD	D/Ū	CTEN	CLK	Input	On
	L	X	х	Х	L	L
parallel load	L	Χ	x	X	Н	н
count up	н	L	ı	1	Х	count up
count down	н	н	1	t	Х	count down
hold (do nothing)	н	X	н	X	×	no change

RCO AND MAX/MIN FUNCTION TABLE

INPUTS			TER	MINAL C	OUTPUTS			
D/Ü	CTEN	CLK	QA	QB	Qc	QD	MAX/MIN	RCO
Н	н	Х	Н	Х	Х	Н	L	Н
L	н.	Х	н	Х	Х	н	н	н
L	L	IJ	н	X	X	н	7_	T
L	н	Х	L	L	L	L	L	н
Н	н	Х	L	L	L	L	н	Н
н	L	T	L	L	L	L	1 7	T

- H = HIGH voltage level
- L = LOW voltage level
- I = LOW voltage level one setup time prior to the LOW-to-HIGH CLK transition
- X = Don't care
- t = LOW-to-HIGH CLK transition
- ∪ = one LOW level pulse
- T = MAX/MIN goes LOW ON A LOW-to-HIGH CLK transition

#### **DESCRIPTION**

These are high-speed synchronous, reversible 4-bit binary counters. Synchronous counting operation is provided by having all flip-flops clocked simultaneously so that the outputs change with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with a synchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered on a low-to-high-level transition of the clock input if the enable input ( $\overline{\text{CTEN}}$ ) is low. A high at  $\overline{\text{CTEN}}$  inhibits counting. The direction of the count is determined by the level of the down/up ( $D/\overline{U}$ ) input. When  $D/\overline{U}$  is low, the counter counts up and when  $D/\overline{U}$  is high, it counts down.

These counters feature a fully independent clock circuit. Changes at the control inputs  $(\overline{CTEN})$  and  $D/\overline{U}$  that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter will be dictated solely by the condition meeting the stable setup and hold times.

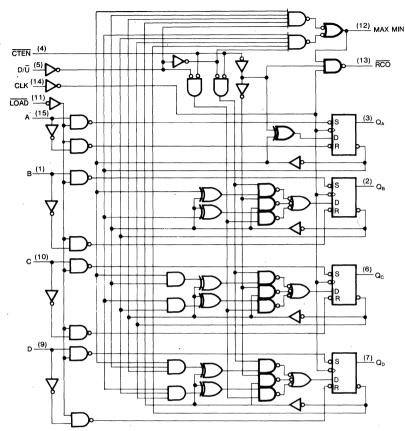
These counters are fully programmable; that is, the outputs may each be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock while the count is zero.(all outputs low) counting down or maximum (9 or 15) counting up. The ripple clock output produces a low-level output pulse under those same conditions but only while the clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

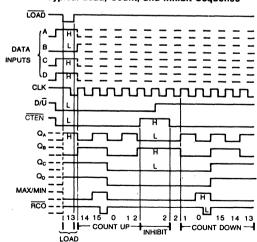
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

## **LOGIC DIAGRAM**



Typical Load, Count, and Inhibit Sequence



#### Seauence:

- (1) Load (preset) to binary thirteen
- (2) Count up to fourteen, fifteen, zero, one, and two
- (3) Inhibit
- (4) Count down to one, zero, fifteen, fourteen, and thirteen



# **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, IIK
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through .
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, P <sub>d</sub> <sup>†</sup> 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Supply Voltage, Vo	с	4.	5V to 5.5	٧
DC Input & Output	$Voltages ^{\star},\ V_{IN},$	Vout .	OV to Vo	c
Operating Tempera	ture			
Range	KS74HCTLS:	-40°C	to +85°	С
	KS54HCTLS:	-55°C	to +125°	C

Input Rise & Fall Times,  $t_{r},\;t_{f}$  . . . . . Max 500 ns

 Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

# DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T <sub>a</sub> = 25°C		KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS $T_a = -55$ °C to +125°C	Unit	
			Тур	Guaranteed Limits				
Minimum High-Level Input Voltage	V <sub>iH</sub>			2.0	2.0	2.0	٧	
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧	
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	V	
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V	
Maximum Input Current	l <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ	
Maximum Quiescent Supply Current	l lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ	
Additional Worst Case Supply Current	Δlcc	per input pin $V_1=2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA	

# Synchronous 4-Bit Up/Down Binary Counters

# AC ELECTRICAL CHARACTERISTICS (Input t<sub>r</sub>, t<sub>f</sub>≤6 ns), HCTLS191

Characteristic		Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74HCTLS T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%	$KS54HCTLS$ $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$	Unit
				Тур		Guaranteed	Limits	
Maximum Clock Frequency		f <sub>max</sub>		30	20	16	14	MHz
Maximum Propagation Delay,		tpLH		30	40	50	60	ns
LOAD to any Q	LOAD to any Q			30	40	50	60	
Maximum Propagation Delay, A,B,C, D to any Q		tpLH		27	36	45	64	ns ns
		t <sub>PHL</sub>	C <sub>L</sub> =50pF	27	36	45	54	
Maximum Propagation Delay, CLK to RCO		TPLH		17	22	28	33	
		t <sub>PHL</sub>		17	22	28	33	
	Maximum Propagation Delay,		tpuH		30	37	45	ns
CLK to any Q		tpHL		23	30	37	45	ns
Maximum Propagation Delay,		tpLH		35	47	59	70	
CLK to MAX/MI	CLK to MAX/MIN			35	47	59	70	
Maximum Propagation Delay, $D/\overline{U}$ to $\overline{RCO}$		tpLH		33	45	56	67	ns
		tpHL		33	45	56	67	
Maximum Propagation Delay,		tplH	PLH		33	41	50	
D/Ū to MAX/MII	D/Ū to MAX/MIN			25	33	41	50	ns
Maximum Propagation Delay, CTEN to RCO		tpLH		25	33	41	50	
		t <sub>PHL</sub>		25	33	41	50	
Minimum	CLK High or Low	t <sub>w</sub>		13	17	21	25	ns
Pulse Width	LOAD Low	- 44		13	17	21	25	
Minimum Setup Time	Data before LOAD1	t <sub>su</sub>		10	13	17	20	ns
	CTEN before CLK1			20	26	34	40	
	D/Ū before CLKt			10	13	17	20	
	LOAD Inactive before CLK1			15	20	25	30	
Minimum Hold Time	Data after LOAD1	t <sub>h</sub>		1	3	5	5	ns
	CTEN after CLK1			-3	0	0 .	0	
	D/U after CLK1			-3	0	0	0	
Maximum Input Capacitance		CiN		5				pF
Power Dissipation Capacitance*		C <sub>PD</sub>	•	80				pF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

# KS54HCTLS 192

# Synchronous 4-Bit Up/Down Decade Counters with Dual Clock

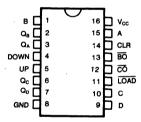
#### **FEATURES**

- Look-ahead circuit enhances cascaded counters
- Fully synchronous in count modes
- Parallel asynchronous load for modulo-N count lengths
- Asynchronous clear
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
  - IOL = 8 mA @ VOL = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
   KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATION



#### DESCRIPTION

These are high-speed synchronous reversible 4-bit decade counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripp le clock) counters.

The outputs of the four flip-flops are triggered by a low-tohigh-level transition of either count (clock) input (Up or Down). The direction of counting is determined by which count input is pulsed while the other count input is high.

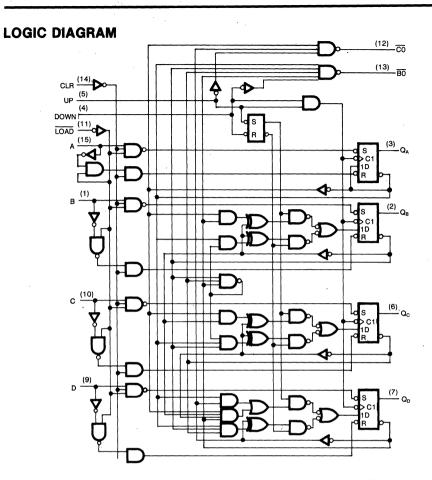
All four counters are fully programmable; that is, each output may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided that forces all outputs to the low level when a high level is applied. The clear function is independent of the count and the load inputs.

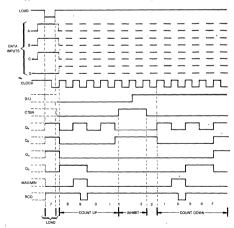
These counters were designed to be cascaded without the need for external circuitry. The borrow output  $(\overline{BO})$  produces a low-level pulse while the count is zero (all outputs low) and the count-down input is low. Similarly, the carry output  $(\overline{CO})$  produces a low-level pulse while the count is maximum (9 or 15) and the count-up input is low. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs, respectively, of the succeeding counter.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.



#### Typical load, count, and inhibit sequences



#### Sequence;

- (1) Load (preset) to BCD seven.
- (2) Count up to eight, mine(maximum) zero, one, and two.
- (3) Inhibit
- (4) Count down to one, zero (minimum), nine, egiht, and seven

NOTE A: Clear overrides load data, and count inputs.

Note B:When count up, count-down input must be high;
when counting down, countup intput must be high.

## **Absolute Maximum Ratings\***

Supply Voltage Range $V_{CC}$ , $-0.5V$ to $+7V$
DC Input Diode Current, I <sub>IK</sub>
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, Tstg65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

	-	_	
Supply Voltage, V <sub>C</sub>	с		4.5V to 5.5V
DC Input & Output	Voltages*, V <sub>IN</sub> ,	$V_{\text{OUT}}$	OV to Vcc
Operating Tempera	ture		

 Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T <sub>a</sub> = 25°C		KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit					
			Тур		Guaranteed Lim	its						
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	<b>v</b>					
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	0.8	<					
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> -0.1 3.7	v					
Maximum Low-Level Output Völtage	V <sub>OL</sub>	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> =20µA I <sub>O</sub> =4mA I <sub>O</sub> =8mA	o	0.1 0.26 0.39	0.1 0.33 0.5	0.1	>					
Maximum Input Current	lin	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ					
Maximum Quiescent Supply Current	l <b>c</b> c	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ					
Additional Worst Case Supply Current		per input in V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA					

# Synchronous 4-Bit Up/Down Decade Counters with Dual Clock

## AC ELECTRICAL CHARACTERISTICS (Input tr, tr≤6 ns), HCTLS192

Ch	Characteristic		Conditions <sup>†</sup>	Ta = :		KS74HCTLS  T <sub>a</sub> = -40°C to +85°C  V <sub>CC</sub> = 5.0V ± 10%	KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> =5.0V ± 10%	Unit
				Тур		Guaranteed	d Limits	
Maximum Clock	Frequency	f <sub>max</sub>		35	25	20	18	MHz
Maximum Propa	gation Delay,	t <sub>PLH</sub>		18	25	31	37	ns
UP to CO		t <sub>PHL</sub>		18	25	31	37	
Maximum <u>Pro</u> pagation Delay, DOWN to BO		t <sub>PLH</sub>		18	24	30	36	ns
		t <sub>PHL</sub>	C <sub>L</sub> =50pF	18	24	30	36	115
Maximum Propagation Delay, UP or DOWN to any Q		T <sub>PLH</sub>		32	42	52	63	ns
		t <sub>PHL</sub>		32	42	52	63	113
Maximum Propa	Maximum Propagation Delay,			30	. 40	50	60	ns
LOAD to any Q		t <sub>PHL</sub>		30	40	50	60	,,,
Maximum Propagation Delay, CLR to any Q		, t <sub>PHL</sub>	,	18	24	30	36	ns
	CLR High			10	13	17	20	
Minimum Pulse	LOAD Low	t <sub>w</sub>		10	13	17	20	ns
Width	UP or DOWN High or Low			10	13	17	20	
	Data before LOAD1			10	13	17	20	
	CLR Inactive before UP1 or DOWN1			10	13	17	20	ns
Minimum Setup Width	LOAD Inactive before UP1 or DOWN1	t <sub>su</sub>		10	13	17	20	ns
	UP high before DOWN1			10	13	. 17	20	
	DOWNhigh before UP1			10	13	17	20	
Minimum Hold	Data after LOAD1			1 .	3	5	5	
Time	UP High after DOWN1	th		-3	0	0	0	ns
	DOWN High after UP1			-3	0	0	0	
Maximum Input	Capacitance	C <sub>IN</sub>		5				pF
Power Dissipation	on Capacitance*	C <sub>PD</sub>		80				рF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} \ V_{CC}^2 \ f \ + \ I_{CC} \ V_{CC}$ .



<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

# KS54HCTLS 193

## Synchronous 4-Bit Up/Down Binary Counters with Dual Clock

#### **FEATURES**

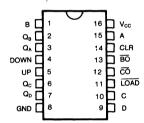
- · Look-ahead circuitry enhances cascaded counters
- · Fully synchronous in count modes
- Parallel asynchronous load for modulo-N count lengths
- . Asynchronous clear
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
- I<sub>OL</sub> = 8 mA @ V<sub>OL</sub> = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATION



#### **FUNCTION TABLE**

#### DESCRIPTION

These are high-speed synchronous reversible 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered by a low-to-high-level transition of either count (clock) input (Up or Down). The direction of counting is determined by which count input is pulsed while the other count input is high.

All four counters are fully programmable; that is, each output may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided that forces all outputs to the low level when a high level is applied. The clear function is independent of the count and the load inputs.

These counters were designed to be cascaded without the need for external circuitry. The borrow output  $(\overline{BO})$  produces a low-level pulse while the count is zero (all outputs low) and the count-down input is low. Similarly, the carry output  $(\overline{CO})$  produces a low-level pulse while the count is maximum (9 or 15) and the count-up input is low. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs, respectively, of the succeeding counter.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

OPERATING MODE		INPUTS									OUTPUTS			
OF ENATING MODE	CLR	LOAD	UP	DOWN	Α	В	С	D	QA	QB	Qc	QD	CO	BO
	Н	Х	Х	L	X	Х	Х	Х	L	L	L	L	Н	L
reset (clear)	Н	X	Х	H.	X	X	Х	Х	L	L	L	L	Н	Н
	L	L	Х	L	L	L	L	L	L	L	L	L	Н	L
	L	L	X	Н	L	L	L	L	L	L	L	L	Н	н
parailel load	L	L	L	X	Н	Н	Н	Н	Н	Н	Н	Н	L	Н
	L	L	Н	X	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
count up	L	Н	1	Н	Х	Х	Х	Х	count up		H*	н		
count down	L	Н	Н	1	Х	Х	Х			count	down		Н	H**

H= HIGH voltage level

↑= LOW-to-HIGH clock transition

L= LOW voltage lovel

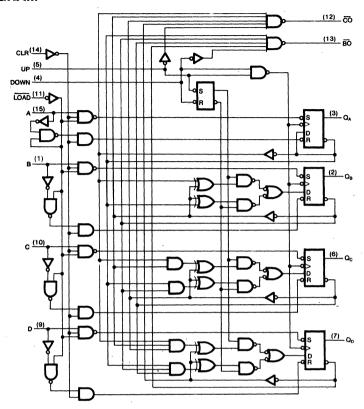
\* CO = UP at terminal count up (HHHH)

X= don't care

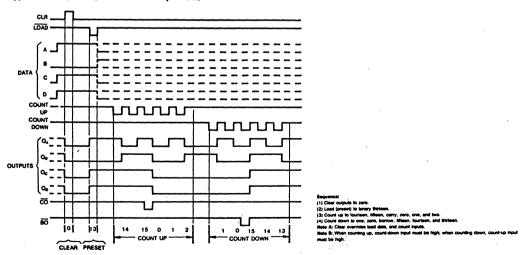
\*\* BO = DOWN at terminal count down (LLLL)



## **LOGIC DIAGRAM**



Typical Clear, Load, and Count Sequences



## **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_{I} < -0.5V \text{ or } V_{I} > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, $T_{stg} \dots -65 ^{\circ} C$ to $+150 ^{\circ} C$
Power Dissipation Per Package, $P_d{}^\dagger$ 500 mW
The state of the s

Storage temperature Hange, 1stg . . . -65°C to +150°C
 Power Dissipation Per Package, Pd† . . . . . 500 mW
 \* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

### **Recommended Operating Conditions**

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . . Max 500 ns

 Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	Т	a = 25°C	KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND	14	±0.1	±1.0	±1.0	μА
Maximum Quiescent Supply Current	Icc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

## AC ELECTRICAL CHARACTERISTICS (Input tr, tr 6 ns), HCTLS193

Ch	aracteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$	KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	Unit
				Тур		Guaranteed	d Limits	
Maximum Clock	Frequency	f <sub>max</sub>		35	25	20	18	MHz
Maximum Propa	gation Delay,	tplH		18	25	31 ^`	37	ns
UP to CO	1	t <sub>PHL</sub>		18	25	31	37	
Maximum Propagation Delay,		tpLH	,	18	24	30	36	ns
DOWN to BO	DOWN to BO		C <sub>L</sub> =50pF	18	24	30	36	
Maximum Propa	Maximum Propagation Delay,			32	42	52	63	ns
UP or DOWN to	any Q	t <sub>PHL</sub>		32	42	52	63	,,,,
Maximum Propa	gation Delay,	t <sub>PLH</sub>		30	40	50	60	ns
LOAD to any Q		t <sub>PHL</sub>		30	40	50	60	,,,,
Maximum Propagation Delay, CLR to any Q		t <sub>PHL</sub>		18	24	30	36	ns
	CLR High	t <sub>w</sub>		10	13	17	20	
Minimum Pulse	LOAD Low			10	13	17	20	ns
Width	UP or DOWN High or Low			10	13	17	20	
	Data before LOAD1			10	13	17	20	
	CLR Inactive before UP1 or DOWN1			10	13	17	20	ns
Minimum Setup Width	LOAD Inactive before UP↑ or DOWN↑	t <sub>su</sub>		10	13	17	20	ns
	UP high before DOWN1		**************************************	10	13	17	20	
	DOWNhigh before UP1			10	13	17	20	
Minimum Hold	Data after LOAD1			1	3	5	5	
Time	UP High after DOWN1	th		-3	0	0	0 ,	ns
	DOWN High after UP1			-3	0	0	0	
Maximum Input	Capacitance	CIN		5				pF
Power Dissipation	on Capacitance*	C <sub>PD</sub>		80				pF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

#### **FEATURES**

- Parallel-to-Serial. Serial-to-Parallel Conversions
- Left or Right Shifts
- Parallel Synchronous Loading
- Direct Overriding Clear
- Temporary Data Latching Capability
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:

IOL = 8 mA @ VOL = 0.5V

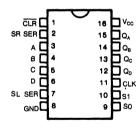
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATION



#### DESCRIPTION

These bidirectional shift registers feature parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation:

- Inhibit clock (temporary data latch/do nothing)
- Shift-right (in the direction QA toward QD)
- Shift-left (in the direction QD toward QA)
- Parallel (broadside) load

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, SO and S1, high. The data is loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited

Shift-right is accomplished synchronously with the rising edge of the clock pulse when SO is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When SO is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial inputs. Clocking of the flip-flop is inhibited when both mode control inputs are low.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### **FUNCTION TABLE**

			INF	PUTS							OUT	PUTS	
CLR	MODE		CLK	SE	RIAL	P/	\RA	\LL	EL	QA	QB	Qc	Qp
OLN	S1 S0	CLK	LEFT	RIGHT	Α	В	С	D	UA.	αв	G.C	GD.	
L	Х	Х	Х	Х	X	Х	Х	Х	Х	L	L	L	L
Н	X	Χ	L	X	Χ	X	Χ	Х	Х	Q <sub>A0</sub>	$Q_{B0}$	$Q_{C0}$	$Q_{D0}$
Н	Н	Н	<b>↑</b>	X	Χ	а	b	С	ď	а	b	С	d
Н	L	Η.	<b>↑</b>	X	Н	X	Х	Х	Х	Н	$Q_{An}$	$Q_{Bn}$	Q <sub>Cn</sub>
H	L	Н	<b>↑</b>	X	L	X	Х	Х	Х	L	$Q_{An}$	$Q_{Bn}$	$Q_{Cn}$
Н	Н	L	<b>↑</b>	Н	Χ	X	Х	Х	Χ	Q <sub>Bn</sub>	Q <sub>Cn</sub>	$Q_{Dn}$	H.
Н	Н	L	<b>↑</b>	L	Χ	X	Х	Х	Х	Q <sub>Bn</sub>			L
Н	L	L	Х	Х	X	Х	Х	Х	Х				$Q_{D\bar{0}}$

H=high level (steady state) L=low level (steady state)

X=irrelevant (any input, including transitions)

1=transition from low to high level a,b,c,d=the level of steady-state input at

inputs, A,B,C, or D, respectively.  $Q_{A0}$ ,  $Q_{B0}$ ,  $Q_{C0}$ ,  $Q_{D0}$ =the level of  $Q_{A}$ ,  $Q_{B}$ ,  $Q_{C}$ , or  $Q_{D}$ , respectively, before

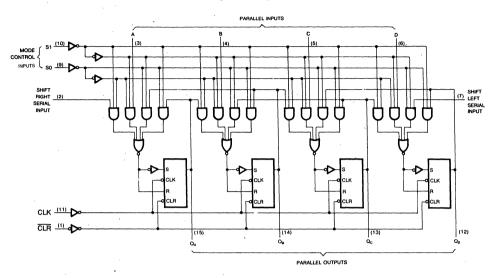
the indicated steady-state input conditions were established. Q<sub>An</sub>, Q<sub>Bn</sub>, Q<sub>Cn</sub>, Q<sub>Dn</sub>=the level of Q<sub>A</sub>, Q<sub>B</sub>, Q<sub>C</sub>, respectively, before the most-

recent 1 transition of the clock.

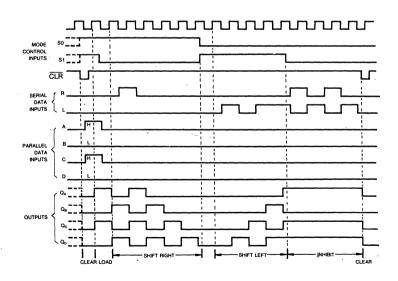


## LOGIC DIAGRAM

#### (positive logic)



typical clear, load, right-shift, inhibit, and clear sequences



## **Absolute Maximum Ratings\***

Supply Voltage Range $V_{CC}$ , $-0.5V$ to $+7V$
DC Input Diode Current, I <sub>IK</sub>
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, $P_d{}^\dagger$ 500 mW
* Absolute Maximum Ratings are those values beyond

which permanent damage to the device may occur.

These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

### **Recommended Operating Conditions**

Supply Voltage, V<sub>CC</sub> . . . . . . . . . . . . . . . . . 4.5V to 5.5V DC Input & Output Voltages\*, V<sub>IN</sub>, V<sub>OUT</sub> . . . OV to V<sub>CC</sub> Operating Temperature

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . . Max 500 ns

#### DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T <sub>a</sub> = 25°C		KS74HCTLS $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$	KS54HCTLS $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	VIH			2.0	. 2.0	2.0	v
Maximum Low-Level input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> -0.1 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	٧
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0′	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

<sup>†</sup> Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

<sup>\*</sup> Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

## AC ELECTRICAL CHARACTERISTICS (Input tr., tr 6 ns), HCTLS194

Cha	Characteristic		Symbol Conditions†		25°C 5.0V	KS74HCTLS $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	KS54HCTLS $T_a = -55$ °C to +125°C $V_{CC} = 5.0V \pm 10\%$	Unit		
				Тур		Guaranteed	Limits			
Maximum Clo	ck Frequency	f <sub>max</sub>		.40	30	25	20	MHz		
Maximum Pro	Maximum Propagation Delay,		1	18	24	30	36	ns		
CLK to Q <sub>H</sub>		t <sub>PHL</sub>	C <sub>L</sub> =50pF	18	24	30	36	113		
Maximum Propagation Delay, CLR to Q <sub>H</sub>		t <sub>PHL</sub>		21	28	35	42	ns		
Minimum	CLR to Low			12	16	20	24			
Pulse Width	CLK High or Low	t <sub>w</sub>		12	16	20	24	ns		
Minimum Sett Any Input bet	•	ts		10	17	20	20	ns		
Minimum Hold Time, Data after CLK1		ts		-3	0	0	0	ns		
Maximum Inp	ut Capacitance	C <sub>IN</sub>		5				pF		
Power Dissipa	ation Capacitance*	C <sub>PD</sub>						pF		

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} \ V_{CC}^2 \ f + I_{CC} \ V_{CC}$ .

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

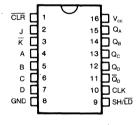
#### **FEATURES**

- Parallel-to-Serial. Serial-to-Parallel Conversions
- Parallel Synchronous Loading
- . J and K Inputs to First Stage
- Right-shift Only with Complementary Outputs on Last Stage
- . Direct Overriding Clear
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
   I<sub>OL</sub> = 8 mA @ V<sub>OL</sub> = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
   (COMMON ASSOCIATION ASSOCIAT

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATION



#### DESCRIPTION

These 4-bit registers feature parallel inputs, parallel outputs,  $J-\overline{K}$  serial inputs, shift/load control input, and a direct overriding clear. The registers have two modes of operation:

Parallel (broadside) load Shift (in the direction A<sub>A</sub> toward Q<sub>D</sub>)

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associate flip-flops and appears at the outputs after the positive transition of the clock input. During loading serial data flow is inhibited.

Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the  $J-\overline{K}$  inputs. These inputs permit the first stage to perform as a  $J-\overline{K}$ , D-, or T-type flip-flop as shown in the function table.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### **FUNCTION TABLE**

	INPUTS									OUTP	OUT	s	
CLR	CLR SHIFT/LOAD		SEF	RIAL	PA	RA	\LL	EL	QA	QB	0-	Qp	$\overline{\mathbf{Q}}_{\mathbf{D}}$
CER	Sim Theoab	CLK	J	K	A	В	С	D	G A	С	СС	uр	αŋ
L	X	Х	X	Х	X	x	х	Х	L	L	L	L	Н
Н	L	1	X	Χ	a	b	С	d	а	b	С	ď	d
H	Н	L	X	Х	X	Х	Х	Χ	QAO	$Q_{B0}$	Qco	Qpo	$\overline{Q}_{DO}$
Н	Н	1	L	Н	X	Χ	Х	Х	QAO	$Q_{A0}$	$Q_{Bn}$	Qcn	$\overline{Q}_{Cn}$
Н	н	1	L	L	X	Χ	Х	Х				Qcn	$\overline{\mathbb{Q}}_{Cn}$
`H	н	1	Н	Н	X	Χ	Х	Х	н	Q <sub>An</sub>	Q <sub>Bn</sub>	Qcn	$\bar{\mathbb{Q}}_{Cn}$
Н	н	<b>†</b>	Н	L	X	Х	Х	Х	$\overline{Q}_{An}$	$Q_{\text{An}}$	$Q_{Bn} \\$	Qcn	$\overline{\mathbb{Q}}_{Cn}$

H=high level (steady state) L=low level (steady state)

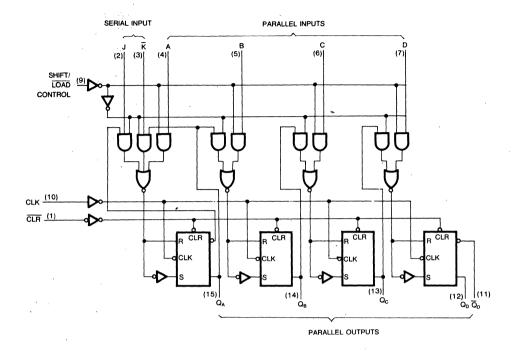
X=irrelevant (any input, including transitions)

↑=transition from low to high level a,b,c,d=the level of steady-state input at A,B,C, or D, respectively.

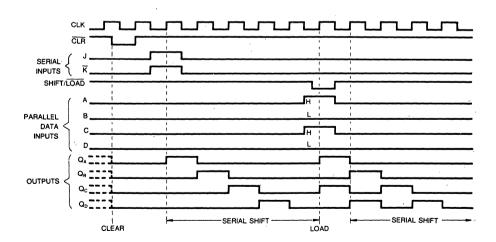
Q<sub>A0</sub>, Q<sub>B0</sub>, Q<sub>C0</sub>, Q<sub>D0</sub>=the level of Q<sub>A</sub>, Q<sub>B</sub>, Q<sub>C</sub>, or Q<sub>D</sub>, respectively, before the indicated steady-state input conditions were established.

Q<sub>An</sub>, Q<sub>Bn</sub>, Q<sub>Cn</sub>=the level of Q<sub>A</sub>, Q<sub>B</sub> or Q<sub>C</sub>, respectively, before the mostrecent transition of the clock.

#### **LOGIC DIAGRAM**



typical clear, shift, and load sequences



## **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V)$ ±20 mA
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Ratings are those values beyond

which permanent damage to the device may occur.

These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Supply Voltage	, V <sub>CC</sub>	4.5V to 5.5V
DC Input & Ou	tput Voltages*, V <sub>IN</sub> ,	Vout OV to Vcc
Operating Temp	perature	
Range	KS74HCTLS:	-40°C to +85°C
	KS54HCTLS:	-55°C to +125°C
Input Rise & Fa	III Times to to	Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

### DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T	<sub>a</sub> = 25°C	KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit	
			Тур		Guaranteed Limits			
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	٧	
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v	
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> -0.1	v	
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v	
Maximum Input Current	l <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ	
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ	
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA	

## AC ELECTRICAL CHARACTERISTICS (Input tr, tre6 ns), HCTLS195

Characteristic		Symbol	Conditions <sup>†</sup>	T <sub>a</sub> = 2 V <sub>CC</sub> =		KS74HCTLS $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	Unit
				Тур		Guaranteed	Limits	
Maximum Cloc	k Frequency	f <sub>max</sub>		50	30	25	20	MHz
Maximum Prop	pagation Delay,	tpLH	0 -50-5	18	24	30	36	ns
CLK to Q <sub>H</sub>		tPHL	C <sub>L</sub> =50pF	18	24	30	36	ns
Maximum Propagation Delay, CLR to Q <sub>H</sub>		t <sub>PHL</sub>		21	28	35	42	ns
Maximum	CLR Low			10	12	15	20	
Pulse Width	CLK High or Low	t <sub>w</sub>		12	16	20	24	ns
Minimum	SH/LD High			15	20	25	25	
Setup Time	Serial or Parallel	t <sub>su</sub>		12	15	20	24	ns
before CLK1	CLR inactive	1		15	20	, 25	25	
Minimum	SH/LD High			-3	0		0	
Hold Time after CLK1	Serial or Parallel Data	th		-3	0		0 .	ns
Maximum Input Capacitance		CIN		5		,		рF
Power Dissipa	tion Capacitance*	CPD						рF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>†</sup> For AC switching test circuits and fiming waveforms see section 2.

#### **FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
  - IOL = 24mA @ VOL = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

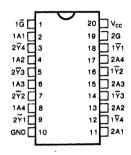
#### **DESCRIPTION**

These high-speed octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

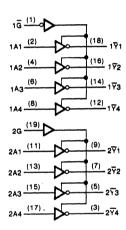
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### PIN CONFIGURATION



## LOGIC DIAGRAM



### **FUNCTION TABLE**

Inj	out	Output
Ğ	Α	Υ
. L	L	Н
L	Н	L
Н	Χ	Z

## Octal Buffers and Line Drivers with 3-State Outputs

## **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V)$ ±20 mA
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_{O.} > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 70 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation

of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

		V <sub>OUT</sub> 0V to V <sub>CC</sub>
Operating Temp		
Range	KS74HCTLS:	-40°C to +85°C
	KS54HCTLS:	-55°C to +125°C
Innut Rise & Fa	II Times to to	Max 500 ns

 <sup>\*</sup> Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	nditions T <sub>a</sub> = 25°C		KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS $T_a = -55$ °C to +125°C	Unit	
			Тур		Guaranteed Lim	its		
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	V	
Maximum Low-Level Input Voltage	V <sub>IL</sub>	,		0.8	0.8	0.8	٠V	
Minimum High-Level Output Voltage	<sup>'</sup> V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-6mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> -0.1 3.84	V <sub>CC</sub> -0.1	v	
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=12mA$ $I_{O}=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v	
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ	
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μА	
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ	

## AC ELECTRICAL CHARACTERISTICS (Input tr. tre6 ns), HCTLS210

Characteristic	Symbol	Conditions†		l i		_	25°C : 5.0V	T. = -40°C to +85°C	KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	Unit
	1			Тур		Guarantee	d Limits			
Maximum Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pl C <sub>L</sub> =150		13 16	18 21	22 27	27 33	ne		
A to $\overline{Y}$	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF		13 16	18 21	22 27	27 33	ns		
Maximum Output Enable	tpzH	$R_i = 1 k\Omega$	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	17 20	23 26	29 34	34 40	ns		
Time, Enable to $\overline{Y}$	t <sub>PZL</sub>	11[-172	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	17 20	23 26	29 34	34 40	115		
Maximum Output Disable	t <sub>PHZ</sub>	$R_L = 1k\Omega$		16	21	26	32	ns		
Time, Enable to $\overline{Y}$	tPLZ	C <sub>L</sub> =50pl	F	16	21	26	32	"3		
Maximum Input Capacitance	CIN							pF		
Maximum Output Capacitance	Cout	Output Disabled		10				pF		
Power Dissipation Capacitance* (per stage)	C <sub>PD</sub>		Output Disabled Output Enabled					рF		

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} \ V_{CC}^2 \ f + I_{CC} \ V_{CC}$ .
† For AC switching test circuits and timing waveforms see section 2.

#### **FEATURES**

- Designed specifically for high-speed memory decoders and data transmission systems
- Incorporates 2 enable inputs to simplify cascading and/or data reception
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
   loL = 8 mA @ Vol = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
   KS74HCTLS: -40°C to +85°C

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### **DESCRIPTION**

These devices are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can be used with high-speed memories utilizing a fast enable circuit. The delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The conditions at the binary select inputs and the three enable inputs select one of eight input lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding.

A 24-line decoder can be implemented without external inverters and a 31-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{\text{CC}}$  and ground.

#### PIN CONFIGURATION

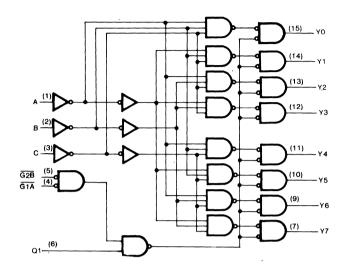
ΑĽ	, )	16 Vcc
в[	2	15 YO
c [	3	14 Y1
G2A	4	13 Y2
G2B	5	12 Y3
G1 [	6	11 Y4
Y7 [	7	10 🔲 Y5
GND [	8	9 🔲 Y6

#### **FUNCTION TABLE**

	Enable Inputs		Select Inputs			Outputs						
G1	G2*	С	В	A	YO	Υ1	Y2	Υ3	Y4	Y5	Y6	Y7
Х	Н	Х	Х	Х	L	L	L	L	L	L	L	L
L	X	Х	Х	Χ	L'	L	L	·L	L	L	L	L
Н	L	L	L	L	Н	L	L	L	L	L	L	L
Н	L	L	L	Н	L	Н	L	L	L	L	Ŀ	L
Н	L	L	Н	L	L	L	Н	L	L	L	L	L
Н	L	Н	L	L	L	L	L	Н	L	L	L	L
Н	L	Н	L	L	L	L	L	L	Н	L	L	L
Н	L	Н	L	Н	L	L	L	L	L	Н	L	L
H	L	Н	Н	L	L	L	L	L	L	L	Н	L
Н	L	Н	Н	Н	L	L	L	L	L	L	L	Н

 $<sup>*\</sup>overline{G2} = \overline{G2A} + \overline{G2B}$ 

#### LOGIC DIAGRAM



## **Absolute Maximum Ratings\***

DC Input Diode Current, IIK

Supply Voltage Range V<sub>CC</sub>, ..... -0.5V to +7V

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Supply Voltage, V<sub>CC</sub> . . . . . . . . . . 4.5V to 5.5V DC Input & Output Voltages\*, V<sub>IN</sub>, V<sub>OUT</sub> . . 0V to V<sub>CC</sub> Operating Temperature

Range KŞ74HCTLS: -40°C to +85°C

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	a = 25°C	KS74HCTLS T <sub>a</sub> = -40°C to +85°C	KS54HCTLS $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$	Unit
	·		Тур	•	Guaranteed Limits		
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	, 0.8	0.8	٧
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	. V <sub>CC</sub> -0.1	V <sub>CC</sub> -0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	lin	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.,1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or'GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin Vz=2.4V Other Inputs: At V <sub>CC</sub> or GND I <sub>O</sub> =0		2.7	2.9	3.0	mA

## AC ELECTRICAL CHARACTERISTICS (Input tr, tre6 ns), HCTLS238

Characteristic	Symbol	Conditions <sup>†</sup>	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74HCTLS $T_a = -40$ °C to +85°C $V_{CC} = 5.0V \pm 10\%$	KS54HCTLS $T_a = -55^{\circ}\text{C to } + 125^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	Unit	
			Typ Guaranteed Limits					
Maximum Propagation Delay,	t <sub>PLH</sub>		22	30	37	45		
A, B, C or any Y	t <sub>PHL</sub>	C <sub>L</sub> =50pF	22	30	37	45	ns ns	
Maximum Propagation Delay,	t <sub>PLH</sub>		24	32	40	48		
G1 to any Y	t <sub>PHL</sub>		24	32	40	48		
Maximum Propagation Delay,	tpLH		18	25	31	37		
G2A or G2B to any Y	t <sub>PHL</sub>		18	25	31	37	ns	
Maximum Input Capacitance	CiN		5				pF	
Power Dissipation Capacitance*	C <sub>PD</sub>		50				pF	

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

#### **FEATURES**

- Designed specifically for high-speed memory decoders and data transmission systems
- Incorporates 2 enable inputs to simplify cascading and/or data reception
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
   I<sub>OL</sub> = 8 mA @ V<sub>OL</sub> = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

### **DESCRIPTION**

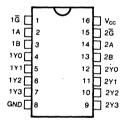
These devices are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can be used to minimize the effects of system decoding. When used with high-speed memories utilizing a fast-enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory.

This means that the effective system delay introduced by the decoder is negligible.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{\text{CC}}$  and ground.

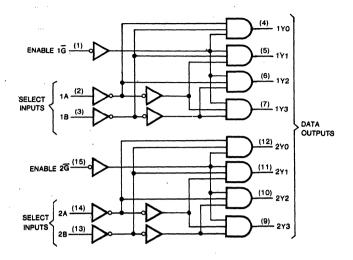
#### PIN CONFIGURATION



#### **FUNCTION TABLE**

In	puts		Outputs						
Enable	able Select		YO	Y1	Y2	Y3			
Ğ			1 10	11	12	13			
Н	Х	Х	L	L	L.	L			
L	L	Ł	н	L	L	L			
L	L	Н	L	Н	L	L			
L	Н	L	L	L	Н	L			
L.	Н	Н	L	L	L	Н			

## LOGIC DIAGRAM



## **Absolute Maximum Ratings\***

Supply Voltage Range Vcc,
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V)$ ±20 mA
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + 1.5V$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Ratings are those values beyond
, which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-
•

posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

KS54HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	= 25°C	KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-4m A$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> -0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	liN	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μА
Additional Worst Case Supply Current	Δlcc	per input pin  V <sub>I</sub> =2.4V  other Inputs: at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0µA		2.7	2.9	3.0	mA

## AC ELECTRICAL CHARACTERISTICS (Input tr, tr 66 ns), HCTLS239

Characteristic	Symbol	Conditions <sup>†</sup>	-	25°C = 5.0V	KS74HCTLS T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%	KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	Unit
			Тур	Typ Guaranteed Limits			
Maximum Propagation Delay,	tpLH	C <sub>L</sub> =50pF	22	30	37	45	ns
A or B any Y	t <sub>PHL</sub>		22	30	37	45	
Maximum Propagation Delay,	t <sub>PLH</sub>		21	8	35	42	ns
G to any Y	t <sub>PHL</sub>		22	8	35	42	1118
Maximum Input Capacitance	CIN		5				pF
Power Dissipation Capacitance*	C <sub>PD</sub>		50				рF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

## KS54HCTLS **240/241/244** Octal Buffers and Line KS74HCTLS **240/241/244** Octal Buffers and Line Drivers with 3-State Outputs

#### **FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current (loL = 24 mA @ VoL = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
   (274)

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### DESCRIPTION

These high-speed octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

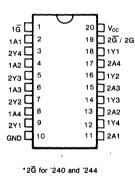
The designer has the choice of combinations of inverting/non-inverting outputs and symmetrical complementary input control (both active-low, or one active-low, the other active-high).

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

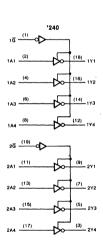
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{\text{CC}}$  and ground.

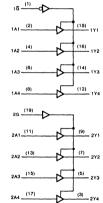
#### PIN CONFIGURATION

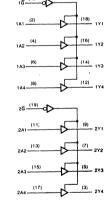
#### LOGIC DIAGRAMS



\*2G for '240 and '244 2G for '241







#### **FUNCTION TABLE**

		:	'241, '244	'240
	Input	,	Output	Output
G	G	A	Y	Y
Н	L	L	L	Н
Ĥ	L	н	н	L
Ĺ	Н	×	Z	Z -



# KS54HCTLS **240/241/244** Octal Buffers and Line KS74HCTLS **240/241/244** Octal Buffers and Line Drivers with 3-State Outputs

## **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, I <sub>OK</sub>
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 70 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.

These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

## **Recommended Operating Conditions**

Supply Voltage, V <sub>CC</sub>	4.5V to 5.5V
DC Input & Output Voltages*, VIN, VOUT	OV to Vcc
Operating Temperature	

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . Max 500 ns

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified).

Characteristic	Symbol	ool Test Conditions	T <sub>a</sub> = 25°C		KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS $T_a = -55$ °C to +125°C	Unit
			Тур		its		
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-6m A$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> = 0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}$ = $V_{IH}$ or $V_{IL}$ $I_{O}$ = $20\mu$ A $I_{O}$ = $12$ mA $I_{O}$ = $24$ mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input - Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μА
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μА



<sup>†</sup> Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

 <sup>\*</sup> Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

# KS54HCTLS **240/241/244** Octal Buffers and Line KS74HCTLS **240/241/244** Octal Buffers and Line Drivers with 3-State Outputs

## AC ELECTRICAL CHARACTERISTICS (Input tr., tre6 ns), HCTLS240 , HCTLS241, HCTLS244

Characteristic	Symbol	Conditions†		T <sub>a</sub> = :	25°C 5.0V	KS74HCTLS T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%	KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	Unit				
,				Тур		Guarantee	d Limits					
Maximum Propagation Delay, A to Y	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF C <sub>L</sub> =50pF C <sub>L</sub> =150pF		13 16	18 21	22 27	27 . 33	ns				
	t <sub>PHL</sub>			13 16	18 21	22 27	27 33					
Maximum Output Enable	tpzh	R <sub>i</sub> = 1kΩ	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	17 20	23 26	29 34	34 40	ns				
Time, Enable to Y	t <sub>PZL</sub>	III — I K.			11[-184	116-174	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	17 20	23 26	29 34	34 40	, ,
Maximum Output Disable	t <sub>PHZ</sub>	$R_L = 1 k\Omega$		16	21	26	32	ns				
Time, Enable to Y	tPLZ	C <sub>L</sub> =50pl	F	16	21	26	32	113				
Maximum Input Capacitance	CiN			5				pF				
Maximum Output Capacitance	Соит	Output Disabled		10				рF				
Power Dissipation Capacitance* (per stage)	C <sub>PD</sub>	Output D Output E		5 30				рF				

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} \ V_{CC}^2 \ f \ + \ I_{CC} \ V_{CC}$ .

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

#### **FEATURES**

- 2-Way Asynchronous Communication Between Data Buses
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current
  - ( $I_{OL} = 24 \text{ mA}$  @  $V_{OL} = 0.5 \text{V}$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges: KS74HCTLS: -40°C to +85°C
  - KS54HCTLS: -55°C to +125°C
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

### PIN CONFIGURATION

ĞAB ☐	1	$\cup$	14	□v
NC 🗌	2		13	GBA
A1	3		12	□NC
A2 🗆	4		11	B1
АЗ□	5		10	□B2
A4 🗌	6		9	□вз
GND	7		8	□в4
ı				I

#### DESCRIPTION

These four-data line transceivers are designed for asynchronous two-way communications between data buses.

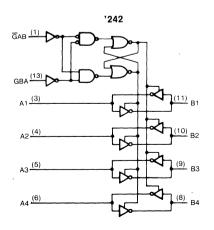
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

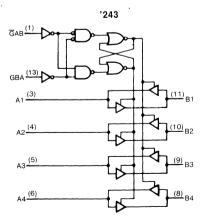
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### **FUNCTION TABLE**

INP	UTS	'242	'243		
ĜAB	GBA	242	243		
L	L	Ā to B	A to B		
Н	Н	B to A	B to A		
Н	L	Isolation	Isolation		
L	Н	Isolation	Isolation		

#### LOGIC DIAGRAMS







### **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + 2.5V$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Supply Voltage, V <sub>CC</sub>	4.5V to 5.5V
DC Input & Output Voltages*, VIN, VOUT	OV to V <sub>CC</sub>
Operating Temperature	

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . . Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	Itions T <sub>a</sub> = 25°C		KS74HCTLS T <sub>a</sub> = -40°C to +85°C	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit
			Тур	i	Guaranteed Limits		
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	≠ V <sub>IL</sub>			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-6mA \ V_{IN}$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	٧
Maximum Input Current	lin	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin  V <sub>I</sub> =2.4V  other Inputs: at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0µA		2.7	2.9	3.0	mA.

## AC ELECTRICAL CHARACTERISTICS (Input tr. tr≤6 ns), HCTLS242, HCTLS243

Characteristic	Symbol	Conditions†		T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74HCTLS $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 10^{\circ}\text{M}$	KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	Unit	
	· _			Тур		Guarantee	d Limits		
Maximum Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF C <sub>L</sub> =50pF C <sub>L</sub> =150pF		14 17	18 21	22 27	27 33	ns	
A to B or B to A	t <sub>PHL</sub>			14 17	18 21	22 27	27 33		
Maximum Output Enable Time	t <sub>PZH</sub>	-R <sub>i</sub> = 1kΩ	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	23 26	30 33	38 43	45 51	ns	
GAB to B, GBA to A	t <sub>PZL</sub>	III— IKW	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	23 26	30 33	38 43	45 51		
Maximum Output Disable	t <sub>PHZ</sub>	$R_L = 1 k\Omega$	•	18	25	31	37	ns	
Time, GAB to B, GBA to A	tPLZ	C <sub>L</sub> =50pF		18	25	31	37	1115	
Maximum Input Capacitance	CIN			5		The same of the sa		pF	
Maximum Output Capacitance	Cout	Output D	Output Disabled					рF	
Power Dissipation Capacitance* (per stage)	C <sub>PD</sub>	Output E		5 30				pF	

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

## Octal Bus Transceivers with 3-State Outputs

#### **FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-state outputs with high drive current ( $I_{OL}=24\text{mA}$  @  $V_{OL}=0.5\text{V}$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

  KETMOTI St. 1000 to 1000

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### **DESCRIPTION**

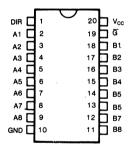
These high-speed octal bus transceivers are designed for synchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction control (DIR) input. The enable input  $(\overline{G})$  can be used to disable the device so that the buses are effectively isolated.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

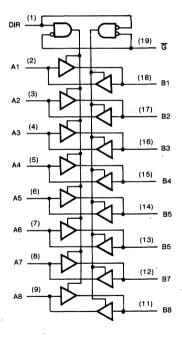
#### **PIN CONFIGURATION**



#### **FUNCTION TABLE**

In	puts	Oneration
G	DIR	Operation
L	L	Bus B Data to Bus A
L	н	Bus A Data to Bus B
Н	X	Isolation

#### LOGIC DIAGRAM



## **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, IIK
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 70 \text{ mA}$
Continuous Current Through
Vcc or GND pins ±250 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Ratings are those values beyond

<sup>\*</sup> Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

## **Recommended Operating Conditions**

	•	•	
Supply Voltage, V <sub>CC</sub>			4.5V to 5.5V
DC input & Output \	/oltages*, V <sub>IN</sub> ,	Vout	OV to Vcc
Operating Temperatu	ıre		

## DC ELECTRICAL CHARACTERISTICS (Vcc=5V±10% Unless Otherwise Specified)

Characteristic	Symbol Test Conditions		T <sub>a</sub> = 25°C		KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	Voh	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-6mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> -0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> =20μA I <sub>O</sub> =12mA I <sub>O</sub> =24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	lin	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

<sup>†</sup> Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

 <sup>\*</sup> Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

## AC ELECTRICAL CHARACTERISTICS (Input tr., tre6 ns), HCTLS245

Characteristic	Symbol	bol Conditions <sup>†</sup>		T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74HCTLS  T <sub>a</sub> = -40°C to +85°C  V <sub>CC</sub> = 5.0V ± 10%	KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	Unit	
				Тур		Guarantee	d Limits		
Maximum Propagation Delay,	tpLH		C <sub>L</sub> =50pF C <sub>L</sub> =150pF		12 15	15 20	18 34	ns	
A to B or B to A	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF		9 12	12 15	15 20	18 34		
Maximum Output Enable		t <sub>PZH</sub> R <sub>I</sub> = 1kΩ	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	30 33	40 43	50 55	60 66	ns	
Time, G to A or B	tpzL		C <sub>L</sub> =50pF C <sub>L</sub> =150pF	30 33	40 43	50 55	60 66	113	
Maximum Output Disable	tpHZ	$R_L = 1k\Omega$		18	25	31	37	ns	
Time, G to A or B	tPLZ	C <sub>L</sub> =50pF		18	25	31	37	1115	
Maximum Input Capacitance	CiN			5				рF	
Maximum Output Capacitance	Соит	Output D	Output Disabled					рF	
Power Dissipation Capacitance* (per stage)	C <sub>PD</sub>	G=V <sub>CC</sub> G=GND	1	5 30				рF	

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} \ V_{CC}^2 \ f \ + \ I_{CC} \ V_{CC}$ .



<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

#### **FEATURES**

- Three-State Version of '151
- Three-State Outputs Interface Directly with System Rus
- Perrorms Parallel-to-Serial Conversion
- Complementary Outputs Provide True and Inverted
   Data
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current (I<sub>OL</sub> = 24 mA @ V<sub>OL</sub> = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### **DESCRIPTION**

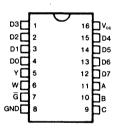
These data selectors/multiplexers contain full binary decoding to select one-of-eight data sources and feature strobe-controlled complementary three-state outputs.

The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state), the low-impedance of the single enabled output will drive the bus line to a high or low logic level. Both outputs are controlled by the strobe  $\{\overline{G}\}$ . The outputs are disabled when  $\overline{G}$  is high.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

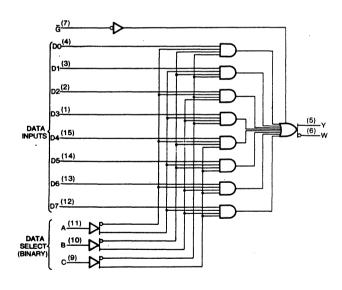
#### PIN CONFIGURATION



#### **FUNCTION TABLE**

		INP	OUT	PUTS		
SELECT			STROBE	٧	w	
С	В	A	Ğ	•	••	
Х	Х	Х	Н	Z	Z	
L	L	٠L	L	DO	DΟ	
L	L	Н	L	D1	D1	
L	Н	L	L	D2	D2	
L	Н	Н	L	DЗ	ĎЗ	
Н	L	L	L	D4	D4	
Н	L	Н	L	D5	D̄5	
Н	Н	L	L	D6	D6	
Н	Н	Н	L '	.D7	D7	

#### LOGIC DIAGRAM



## 1-of-8 Data Selectors/Multiplexers with 3-State Outputs

#### Absolute Maximum Ratings\*

Supply voltage Hange $V_{CC}$ , $-0.5V$ to $+7V$
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V_i < V_O < V_{CC} + 0.5V) + \pm 70 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW

<sup>\*</sup> Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . . . Max 500 ns

 Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T <sub>a</sub> = 25°C		KS74HCTLS T <sub>a</sub> = -40°C to +85°C	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		its		
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-6mA$	V <sub>CC</sub> 4.2	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> -0.1 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	· V
Maximum Input Current	liN	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μА
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μА
Maximum Quiescent Supply Current	Icc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	00	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA



## AC ELECTRICAL CHARACTERISTICS (Input tr, tre6 ns), HCTLS251

Characteristic	Symbol	Conditions†			25°C 5.0V	$KS74HCTLS$ $T_a = -40 ^{\circ}C \text{ to } +85 ^{\circ}C$ $V_{CC} = 5.0V \pm 10 ^{\circ}$	KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	Unit	
				Тур	Typ Guaranteed Limits				
Maximum Propagation Delay.	t <sub>PLH</sub>	$C_L = 50p$ $C_L = 150$		20 23	26 29	33 38 .	40 46	ne	
A, B or C to Y	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF		20 23	26 29	33 38	40 46	ns	
Maximum Propagation Delay,	€PLH	C <sub>L</sub> =50p C <sub>L</sub> =150		25 28	34 37	42 47	50 56	ns	
A, B or C to W	t <sub>PHL</sub>	C <sub>L</sub> =50pl C <sub>L</sub> =150		25 28	34 37	42 47	50 56	TIS I	
Maximum Propagation Delay,	t <sub>PLH</sub> C <sub>L</sub> =50pl C <sub>L</sub> =150			11 14	15 18	19 24	22 28	ns	
Any D to Y	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF		11 14	15 18	19 24	22 28	113	
Maximum Propagation Delay,	t <sub>PLH</sub>	$C_L=50pF$ $C_L=150pF$		17 20	22 25	28 33	33 39	ns	
Any D to W	t <sub>PHL</sub>	C <sub>L</sub> =50pl C <sub>L</sub> =150		17 20	22 25	28 33	33 39		
Maximum Output Enable Time,	t <sub>PZH</sub>	$B_i = 1 k\Omega$	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	24 27	32 35	40 45	48 54	ns	
G to Y or W	tpzL		C <sub>L</sub> =50pF C <sub>L</sub> =150pF	24 27	32 35	40 45	48 54		
Maximum Output Disable Time	t <sub>PHZ</sub>	$R_L = 1 k\Omega$	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	24 27	32 35	40 · 45	48 54	ns	
G to Y or W	t <sub>PLZ</sub>		C <sub>L</sub> =50pF C <sub>L</sub> =150pF	24 27	32 35	40 45	48 54		
Maximum Input Capacitance	C <sub>IN</sub>			5				pF	
Maximum Output Capacitance	Cout	Output Disabled		10				pF	
Power Dissipation Capacitance*	C <sub>PD</sub>			0			•	pF	

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} \ V_{CC}^2 \ f \ + \ I_{CC} \ V_{CC}$ .

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

- Three-State Version of '153
- Permits Multiplexing from N Lines to 1 Line
- Performs Parallel-to-Serial Conversion
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current (I<sub>OL</sub> = 24 mA @ V<sub>OL</sub> = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
   KS74HCTLS: -40°C to +85°C
   KS54HCTLS: -55°C to +125°C
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### **DESCRIPTION**

Each of these data selectors/multiplexers contains inverters and drivers to supply full binary decoding data selection to the AND-OR gates. Separate output control inputs are provided for each of the two four-line sections.

The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the low-impedance of the single enabled output will drive the bus line to a high or low logic level. Each output has its own strobe (G). The output is disabled when its strobe is high.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### PIN CONFIGURATION

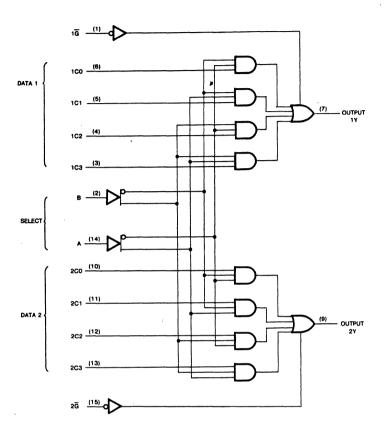
1Ğ	1	16	\v
в	2	15	]2Ğ
1C3	3	14	□ A′
1C2	4	13	<b>]</b> 2C3
101	5	12	]2C2
1C0	6	11	<b>]</b> 20i
17	7	10	<b>]</b> 2C0
GND	8	9	<b>2</b> Y

#### **FUNCTION TABLE**

SEL	SELECT		DATA INPUTS		OUTPUT CONTROL	ОИТРИТ	
В	Α	C0	C1	C2	C3	G	Y
Х	X	· X	X	Х	Х	Н	Z
L	Ĺ	L	Х	Х	X	L	L
L	Ĺ	Н	Х	Х	Х	L	н
L	Н	X	L	Х	Х	L	L
L	Н	X	Н	Х	Х	L	н
Н	L	Х	Χ	L	Χ	L	L
Н	L	Х	Х	Н	Х	L	н
Н	Н	Х	Χ	Х	L	L	L
Н	Н	Х	Χ	Х	Н	L	Н

Address inputs A and B are common to both sections.

### LOGIC DIAGRAM



## **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Supply Voltage, V<sub>CC</sub> . . . . . . . . . . . . 4.5V to 5.5V DC Input & Output Voltages\*, V<sub>IN</sub>, V<sub>OUT</sub> . . 0V to V<sub>CC</sub> Operating Temperature

Range KS74HCTLS: -40°C to +85°C

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

#### DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	= 25°C	KS74HCTLS T <sub>a</sub> = -40°C to +85°C	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-6mA$	V <sub>CC</sub> 4.2	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> -0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}$ = $V_{IH}$ or $V_{IL}$ $I_{O}$ =20 $\mu$ A $I_{O}$ =12 $\mu$ A $I_{O}$ =24 $\mu$ A	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μА
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

## AC ELECTRICAL CHARACTERISTICS (Input tr., tr<6 ns), HCTLS253

Characteristic	Symbol	Conditions†		T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74HCTLS  T <sub>a</sub> = -40°C to +85°C  V <sub>CC</sub> = 5.0V ± 10%	KS54HCTLS  T <sub>a</sub> = -55°C to +125°C  V <sub>CC</sub> = 5.0V ± 10%	Unit
	1			Тур		Guarantee	d Limits	1
Maximum Propagation Delay,	tpLH	C <sub>L</sub> =50pl C <sub>L</sub> =150		24 27	32 35	40 45	48 54	ns
A or B to Any Y	t <sub>PHL</sub>	C <sub>L</sub> =50pl C <sub>L</sub> =150		24 27	32 35	40 45	48 54	113
Maximum Propagation Delay,		C <sub>L</sub> =50pF C <sub>L</sub> =150pF		15 18	20 23	25 30	30 36	ns
Data (any C) to any Y	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF		15 18	20 23	25 30	30 36	110
Maximum Output Enable	tpzH	Ri=1kΩ	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	17 20	22 25	28 33	33 39	ns
Time, $\overline{\mathbf{G}}$ to Y	t <sub>PZL</sub>	III— IKAS	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	17 20	22 25	28 33	33 39	113
Maximum Output Disable	t <sub>PHZ</sub>	$R_L = 1 k\Omega$		17	22	28	. 33	ns
Time, G to Y	ne, G to Y t <sub>PLZ</sub>		C <sub>L</sub> =50pF		22	28	33	113
Maximum Input Capacitance	CIN			5			•	рF
Maximum Output Capacitance	Cout	Output D	isabled	10				pF
Power Dissipation Capacitance*	C <sub>PD</sub>						,	pF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} \ V_{CC}^2 \ f \ + \ I_{CC} \ V_{CC}$ .

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.



# KS54HCTLS **257/258** Quad 2-Line to 1-Line Data Selectors/KS74HCTLS **4 Multiplexers with 3-State Outputs**

#### **FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current (I<sub>OL</sub> = 24 mA @ V<sub>OL</sub> = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
   KS74HCTLS: -40°C to +85°C
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### DESCRIPTION

The '257 and '258 multiplex signals from for-bit data sources to four-output data lines in bus organized systems. The data presented at the outputs is non-inverted for the '257 and inverted for the '258.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### PIN CONFIGURATION

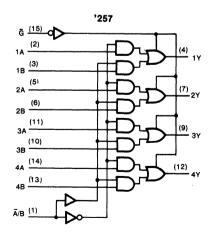
KS54HCTLS: -55°C to +125°C

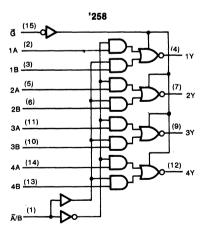
A/B   1A   1B   1Y	1 2 3 4	16 V <sub>cc</sub> 15 G 14 AA 13 4B
2A C	5	12 4Y
2B C	6	11 3A
2Y C	7	10 3B
GND C	8	9 3Y

#### **FUNCTION TABLE**

	Inputs	Output Y			
Output Control	select	Data		'257	'258
Ğ	Ã/Β	A	В		
Н	Х	Х	X	Z	Z
L	L	L	X	L	н
L	L	н	Х	Н	L
L	Н	X	L	L	Н
L	н	X	н	Н	L

#### LOGIC DIAGRAMS





### **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 70 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, P <sub>d</sub> <sup>†</sup> 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

KS54HCTLS: -40 C to +65 C

KS54HCTLS: -55°C to +125°C

Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	ns T <sub>a</sub> = 25°C		KS74HCTLS KS54HCTLS $T_a = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ $T_a = -55^{\circ}\text{C}$ to $+125^{\circ}$		Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-6mA$	V <sub>CC</sub> 4.2	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=12mA$ $I_{O}=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	lin	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μА
Maximum Quiescent Supply Current	l lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA





# KS54HCTLS **257/258** Quad 2-Line to 1-Line Data Selectors/KS74HCTLS **4 Multiplexers with 3-State Outputs**

## AC ELECTRICAL CHARACTERISTICS (Input tr, tr≤6 ns), HCTLS257, HCTLS258

Characteristic	Symbol Conditions†		1		25°C = 5.0V	KS74HCTLS T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%	KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> =5.0V ± 10%	Unit	
				Тур		Guarantee	d Limits	1 1	
Maximum Propagation Delay.	t <sub>PLH</sub>	C <sub>L</sub> =50pl C <sub>L</sub> =150		14 17	18 21	23 28	27 33	ns	
A to B to any Y	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF		14 17	18 21	23 28	27 33	113	
Maximum Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>I</sub> =150pF		16 19	21 24	26 31	31 37	ns	
Ā/B to any Y	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF		16 19	21 24	26 31	31 37		
Maximum Output Enable	t <sub>PZH</sub>	$R_i = 1 k\Omega$	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	22 25	30 33	37 42	45 51	ns	
Time, G to any Y	t <sub>PZL</sub>	t <sub>PZL</sub>	115-147	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	22 25	30 33	37 42	<b>45</b> 51	ns
Maximum Output Disable	t <sub>PHZ</sub>	$R_L = 1 k\Omega$		20	27	34	41	ns	
Time, G to any Y	tPLZ	C <sub>L</sub> =50pl	F	20	27	34	41	113	
Maximum Input Capacitance	CiN			5				pF	
Maximum Output Capacitance	Cout	Output Disabled		10				рF	
Power Dissipation Capacitance*	C <sub>PD</sub>							pF	

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

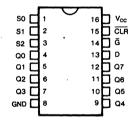
<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

- 8-Bit parallel-out storage register performs serial-toparallel conversion with storage
- Asynchronous parallel clear
- · Active high decoder
- Enable/Disable input simplifies expansion
- Expandable for N-bit applications
- Four distinct functional modes
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
   I<sub>OL</sub> = 8 mA @ V<sub>OL</sub> = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATION



#### **FUNCTION TABLE**

Inpu	ts	Output of Addressed	Each Other	Function
CLR	Ğ	Latch Output		Puliction
Н	L	D	Q <sub>iO</sub>	Addressable Latch
Н	Н	QiO	Qio	Memory
L	L	D	L	8-Line Demultiplexer
L	Н	L	L	Clear

D = the level at the data input.

 $Q_{i0}=$  the level of  $Q_{i0}\,(i=Q,\,1,\,\dots\,7,$  as appropriate) before the indicated steady-state input conditions were established.

#### **DESCRIPTION**

The '259 is a high-speed addressable latch designed for general purpose storage applications in digital systems. It can be used for implementing working registers, serial-holding registers and active-high decoders or demultiplexers.

The '259 has four distinct modes of operation that are selected via the clear ( $\overline{\text{CLR}}$ ) and enable ( $\overline{\text{G}}$ ) inputs: 1) addressable latch; 2) memory; 3) active-high eight-channel demultiplexer; and 4) clear.

In the addressable latch mode, data on the data input (D) is written into the addressed latch. In this mode, data will be written into the addressed latch with all non-addressed latches remaining in their previous states.

In the memory mode, all latches remain in their previous state and are unaffected by the data of address inputs.

In the demultiplexing mode, addressed outputs will follow the state of the D input and all other outputs will remain low.

In the clear mode, all outputs are low and unaffected by the address and data inputs.

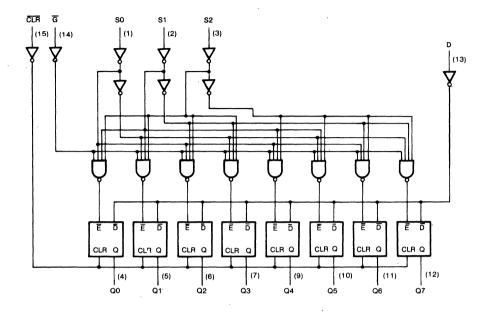
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### LATCH SELECTION TABLE

Sel	ect Inp	Latch	
S2	S1	SO	Addressed
L	L	L	0
L	L	Н	1
L	Н	L	2
L	Н	Н	3
н	L	L	4
н	L	н	5
Н	H.	L	6
Н	н	Н	7

#### LOGIC DIAGRAM



## **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> , −0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) + \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±35 mA
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stq</sub> 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Input Rise & Fall Times,  $t_{r},\;t_{f}$  . . . . . . . . Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	Т	a = 25°C	KS74HCTLS T <sub>a</sub> = -40°C to +85°C	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	V <sub>IH</sub>	,		2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-4mA$	V <sub>CC</sub> 4.2	V <sub>CC</sub> -0.1	V <sub>CC</sub> −Ö.1 3.84	V <sub>CC</sub> −0.1	v
Maximum Low-Level Output Voltage	. V <sub>OL</sub>	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> =20µA I <sub>O</sub> =4mA I <sub>O</sub> =8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μА
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin  V <sub>I</sub> =2.4V  other Inputs: at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0µA		2.7	2.9	3.0	mA

## AC ELECTRICAL CHARACTERISTICS (Input t<sub>r</sub>, t<sub>f</sub>≤6 ns), HCTLS259

Characteristic		Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74HCTLS T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%	KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	Unit
				Тур		Guaranteed Limits		
Maximum Propagation	on Delay	t <sub>PHL</sub>		22	30	37	45	ns
Maximum Propagation	n Delay,	t <sub>PLH</sub>		20	27	34	41	ns
Data to Any Q		t <sub>PHL</sub>		20	27	34	41	110
Maximum Propagation	n Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pF	26	34	43	51	ns
Address to any Q		t <sub>PHL</sub>		26	34	43	51	
Maximum Propagation	n Delay,	tpLH		22	30	37	45	ns
G to any Q	-	t <sub>PHL</sub>		22	30	37	45	
Minimum Pulse	CLR LOW	tw		8	10	13	15	ns
Width	G Low			8	10	13	15	
Minimum Setup Tim Data or Address bef		t <sub>su</sub>		8	10	13	15	ns
Minimum Hold Time, Data or Address before Gt		t <sub>h</sub>		-3	o	0	Ò	ns
Maximum Input Capa	acitance	CIN		5				pF
Power Dissipation C	apacitance*	C <sub>PD</sub>		80				pF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} \ V_{CC}^2 \ f \ + \ I_{CC} \ V_{CC}$ .



<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
  - IOL = 8 mA @ VOL = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
   \*\*TOTALIZED TOTALIZED  - KS74HCTLS: -40°C to +85°C
- KS54HCTLS: -55°C to +125°C
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

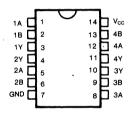
### **DESCRIPTION**

These devices contain four independent exclusive-NOR gates with open-drain outputs. Using a suitable pull-up resistor, these outputs may be connected to other open-drain outputs to implement wired-AND functions.

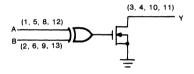
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### PIN CONFIGURATION



#### **LOGIC DIAGRAM**



#### **FUNCTION TABLE**

inp	uts	Output
Α	В	Y
L	L	Н
L	Н	L
Н	L	L
Н	Н	н

## Quad Exclusive-NOR Gates with Open-Drain Outputs

#### **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V	/
DC Input Diode Current, I <sub>IK</sub>	
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$	٩
DC Output Diode Current, IOK	
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$	١
Continuous Output Current Per Pin, Io	
$(-0.5V < V_0 < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$	١
Continuous Current Through	
Vcc or GND pins ±125 mA	١
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C	)
Power Dissipation Per Package, Pd† 500 mW	V

Storage Temperature Hange, Tatg... -65°C to +150°C
 Power Dissipation Per Package, Pd<sup>†</sup>... 500 mW
 Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

#### **Recommended Operating Conditions**

Supply Voltage, V<sub>CC</sub> . . . . . . . . . . . . 4.5V to 5.5V DC Input & Output Voltages\*, V<sub>IN</sub>, V<sub>OUT</sub> . . OV to V<sub>CC</sub> Operating Temperature

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . . . . Max 500 ns

\* Unused inputs must always be tied to an appropriate logic
voltage level (either V<sub>CC</sub> or GND)

#### DC ELECTRICAL CHARACTERISTICS (Vcc=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	Ta = 25°C		KS74HCTLS Ta = -40°C to +85°C	$KS54HCTLS$ $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$	Unit			
			Тур		Guaranteed Lim	its				
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	v			
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧			
Maximum Low-Level Output Voltage	VoL	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> =20µA I <sub>O</sub> =4mA I <sub>O</sub> =8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v			
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ			
Maximum Output Leakage Current	loz	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> =V <sub>CC</sub>		±0.5	±5.0	±10.0	μΑ			
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.0	20.0	40.0	μΑ			
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA			

#### AC ELECTRICAL CHARACTERISTICS (Input tr., tres 6 ns), HCTLS266

Characteristic	Symbol	Conditions†	1 -	- 1. = - 40°C: to +85°C:		$= 25^{\circ}\text{C}$ $T_a = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ $T_a = -55^{\circ}\text{C}$ to $+125^{\circ}$		T <sub>a</sub> = -55°C to +125°C	Unit
			Typ Guaranteed Limits						
Maximum Propagation Delay	t <sub>PLH</sub>	C <sub>L</sub> =50pF	18	25	31	37	ns		
Waximum Topagation Delay	t <sub>PHL</sub>	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	33	113					
Maximum Input Capacitance	CIN		5				рF		
Power Dissipation Capacitance*	C <sub>PD</sub>	(per gate)	15				рF		

<sup>\*</sup> CPD determines the no-load dynamic power dissipation: PD=CPD VCc2 f + ICC VCC.

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.



- Eight positive-edge-triggered D-type flip-flops with single-rail outputs
- Buffered common clock and asynchronous clear
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
  - ( $I_{OL} = 24 \text{mA}$  @  $V_{OL} = 0.5 \text{V}$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range; 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

  KSTANOTIO: 4000 45 40500

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### DESCRIPTION

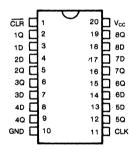
These devices are high-speed octal registers. They consist of eight positive-edge-triggered D-type flip-flops with individual D inputs and Q outputs. All flip flops are loaded and cleared simultaneously by the common buffered clock (CLK) and clear (CLR) inputs.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to Vcc and ground.

#### PIN CONFIGURATION

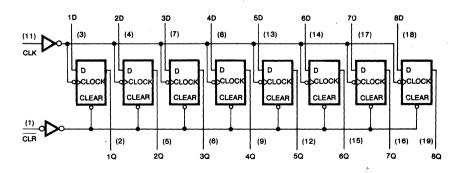


#### **FUNCTION TABLE**

## (Each Flip-Flop)

li	puts	Output	
CLR	CLK	D	Q
L	Х	Х	L
Н	<b>↑</b>	Н	н
Н	<b>↑</b>	L	L
Н	L	Χ	Q <sub>0</sub>

#### LOGIC DIAGRAM



## **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ m/A}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 70 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, $P_d^{\dagger}$ 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.

These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

#### **Recommended Operating Conditions**

Supply Voltage, V <sub>CC</sub>	4.5V to 5.5V
DC Input & Output Voltages*, VIN, VOUT	$$ . OV to $V_{CC}$
Operating Temperature	

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	a = 25°C	KS74HCTLS T <sub>0</sub> = -40°C to +85°C	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit
	,		Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	Voh	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-6m A$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	٧
Maximum Low-Level Output Voltage	ì	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=12mA$ $I_{O}=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

## AC ELECTRICAL CHARACTERISTICS (Input tr, tr<6 ns), HCTLS273

					· · · · · · · · · · · · · · · · · · ·					
Characteristic		Symbol	Conditions <sup>†</sup>	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74HCTLS  T <sub>a</sub> = -40°C to +85°C  V <sub>CC</sub> = 5.0V ± 10%	KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	Unit		
				Тур		Guaranteed	Limits			
Maximum Clock	Frequency	f <sub>max</sub>	C <sub>L</sub> =50pF	40	30	25	20	MHz		
Maximum Propagation Delay, CLK to any		t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	20 23	27 30	33 38	40 46	ns		
		t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	20 23		33 38	40 46	113		
Maximum Propagation Delay, CLR to any Q		t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	20 23		33 38	40 46	ns		
Minimum Pulse	CLR Low	tw		10	13	17	20	ns		
Width	CLK High or Low	·w		10	13	17	20	113		
Minimum Setup	Data	tsu		10	13	17	20	ns		
Time before CLKt	Clear inactive State	lsu		13	17	21	25	115		
Minimum Hold Time, Data after CLKf		th		-3	0	0	0	ns		
Maximum Input	Capacitance	CIN		5				pF		
Power Dissipati	on Capacitance*	C <sub>PD</sub>	(per package)	150				pF		

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

- . Generates Odd or Even Parity for Nine Data Lines
- . Cascadable for N-Bits Parity
- Can be used to Upgrade Existing Systems using MSI Parity Circuits
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
  - ( $I_{OL} = 24 \text{ mA} @ V_{OL} = 0.5 \text{V}$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### **DESCRIPTION**

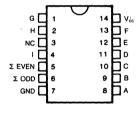
These universal, nine-bit parity generators/checkers feature odd and even outputs to facilitate operation of either odd or even parity application. The word-length capability is easily expanded by cascading.

The devices can be used to upgrade the performance of most systems utilizing the '180 parity generator/checker, Although the '280 is implemented without expander inputs, the corresponding function is provided by the availability of an input at pin 4 and the absence of any internal connection at pin 3. This permits the '280 to be substituted for the '180 in existing designs to produce an identical function even if the devices are mixed with existing '180's.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

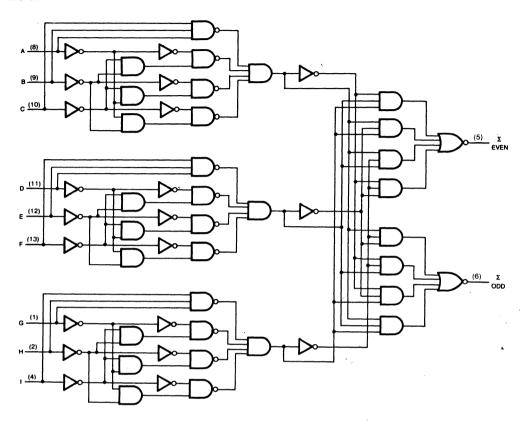
### PIN CONFIGURATION



#### **FUNCTION TABLE**

NUMBER OF INPUTS A	OUTPUTS					
THRU I THAT ARE HIGH	Σ EVEN	Σ ODD				
0,2,4,6,8	н	L				
1,3,4,5,9	L	Н				

#### LOGIC DIAGRAM



## Absolute Maximum Ratings\*

Supply Voltage Range $V_{CC}$ , $-0.5V$ to $+7V$
DC Input Diode Current, I <sub>IK</sub>
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V)$ ±20 mA
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Patings are those values havend

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Supply Voltage,	V <sub>CC</sub> 4.5V to 5.5V
DC Input & Outp	ut Voltages*, V <sub>IN</sub> , V <sub>OUT</sub> OV to V <sub>CC</sub>
Operating Tempe	erature
Range	KS74HCTLS: -40°C to +85°C
	KS54HCTLS: -55°C to +125°C
Input Rise & Fall	Times, $t_r,\;t_f$ Max 500 ns

 Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	= 25°C	KS74HCTLS T <sub>a</sub> = -40°C to +85°C	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit
			Тур	,	its		
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			ა.8	0.8	0.8	٧
Minimum High-Level Output Voltage	Voh	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-6m A$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> =0.1 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	VòL	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> =20µA I <sub>O</sub> =12mA I <sub>O</sub> =24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	IIN	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =O <sub>µ</sub> A		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

## AC ELECTRICAL CHARACTERISTICS (Input t<sub>r</sub>, t<sub>f</sub>≤6 ns), HCTLS280

Characteristic	Symbol	Conditions <sup>†</sup>	T. =: Vcc =	25°C 5.0V	KS74HCTLS T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%	KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> =5.0V± 10%	Unit	
•			Тур		Guaranteed	Limits		
Maximum Propagation Delay, Any input to Σ Even	PLH	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	30 33	40 43	50 55	60 66	ns	
	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	30 33	40 43	50 55	60 66		
Maximum Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	30 33	40 43	50 55 .	60 66	ns	
Any input to ΣOdd	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	30 33	40 43	50 55	60 66		
Minimum Input Capacitance	CIN		5				pF	
Power Dissipation Capacitance*	C <sub>PD</sub>						pF	

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.



<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

- Multiplexed I/O ports provides improved bit density
- Four modes of operation: hold (store), shift, shift left, and load data
- . Operates with outputs enabled or at high impedance
- · Can be cascaded for N-bit word lengths
- Direct overriding clear
- Application:
  - Stacked or push-down registers, buffer storage, and accumulator registers
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with drive current
- ( $I_{OL} = 24 \text{ mA}$  @  $V_{OL} = 0.5 \text{V}$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### DESCRIPTION

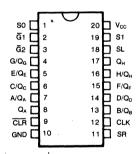
These eight-bit universal registers feature multiplexed I/O ports to achieve full eight-bit data handling. Two function-select inputs and two output-control inputs can be used to choose the modes of operation listed in the function table.

Synchronous parallel loading is accomplished by taking both function-select lines SO and S1 high. This places the three-state outputs in a high-impedance state and permits data that is applied on the I/O ports to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. Clearing occurs asynchronously when  $\overline{\text{CLR}}$  is low. Pulling either of the output controls,  $\overline{\text{G1}}$  or  $\overline{\text{G2}}$ , high disables the outputs but this has no effect on clearing, shifting, or storage of data.

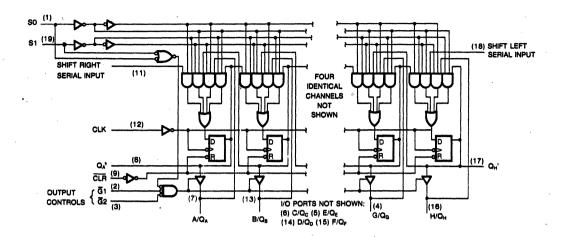
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### PIN CONFIGURATION



#### LOGIC DIAGRAM



#### **FUNCTION TABLE**

	Inputs							i/O Ports					Outputs					
Mode	CLR	S1	SO-	1	put ntrol G2	CLK	SL	SR	A/Q <sub>A</sub>	B/Q <sub>B</sub>	C/Qc	D/Q <sub>D</sub>	E/Q <sub>E</sub>	F/Q <sub>F</sub>	G/Q <sub>G</sub>	H/Q <sub>H</sub>	Q <sub>A</sub> '	Q <sub>H</sub> '
Clear	L L L	X L H	L X H	L L X	L L X	X X X	X X X	X X X	L L X	L L X	L L X	L L X	L X	L L "	L L X	L L X	L L L	L L L
Hold	H	L X	L X	L	L L	X L	X	X	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>C0</sub>	Q <sub>D0</sub>	Q <sub>E0</sub>	Q <sub>F0</sub>	Q <sub>G0</sub> Q <sub>G0</sub>	Q <sub>H0</sub>		Q <sub>H0</sub> Q <sub>H0</sub>
Shift Right	H H	L L	Н	L L	L L	<b>†</b>	X	H	H	Q <sub>An</sub> Q <sub>An</sub>	Q <sub>Bn</sub> Q <sub>Bn</sub>	Q <sub>Cn</sub> Q <sub>Cn</sub>	Q <sub>Dn</sub> Q <sub>Dn</sub>	Q <sub>En</sub> Q <sub>En</sub>	Q <sub>Fn</sub>	Q <sub>Gn</sub> Q <sub>Gn</sub>	H L	Q <sub>Gn</sub> Q <sub>Gn</sub>
Shift Left	H	H	L L	L L	L	<b>†</b>	H	X	Q <sub>Bn</sub> Q <sub>Bn</sub>	Q <sub>Cn</sub> Q <sub>Cn</sub>	Q <sub>Dn</sub> Q <sub>Dn</sub>	Q <sub>En</sub> Q <sub>En</sub>	Q <sub>Fn</sub> Q <sub>Fn</sub>	Q <sub>Gn</sub> Q <sub>Gn</sub>	Q <sub>Hn</sub> Q <sub>Hn</sub>	H	Q <sub>Bn</sub> Q <sub>Bn</sub>	H
Load	Н	. Н	Н	Х	Х	1	, <b>X</b>	Х	а	b	С	d	е	f	g	h	а	h

When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

#### **Absolute Maximum Ratings\***

<sup>\*</sup> Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

## **Recommended Operating Conditions**

Supply Voltage, V<sub>CC</sub> . . . . . . . . . . . 4.5V to 5.5V DC Input & Output Voltages\*, V<sub>IN</sub>, V<sub>OUT</sub> . . OV to V<sub>CC</sub> Operating Temperature

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

Input Rise & Fall Times,  $t_r,\;t_f$   $\ldots$  . . . . . Max 500 ns

#### DC ELECTRICAL CHARACTERISTICS (Vcc=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	= 25°C	KS74HCTLS T <sub>a</sub> = -40°C to +85°C	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit	
			Тур		Guaranteed Limits			
Minimum High-Level Input Voltage	VIH			2.0	2.0	2.0	v	
Maximum Low-Level Input Voltage	VIL	·		0.8	0.8	0.8	V	
Minimum High-		$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $Q'_A$ and $Q'_H$ outputs: $I_O=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1	V <sub>CC</sub> -0.1	V <sub>CC</sub> =0.1	v	
Level Output Voltage	Vон	Q <sub>A</sub> thru Q <sub>H</sub> outputs: I <sub>O</sub> = -6 mA	4.2	3.84	3.7	<b>3.7</b>		
Miximum		V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> =20μΑ Q' <sub>A</sub> and Q' <sub>H</sub> outputs:	0	0.1	0.1	0.1		
Low-Level Output Voltage	Vol	I <sub>O</sub> =4mA I <sub>O</sub> =8mA Q <sub>A</sub> thru Q <sub>H</sub> outputs:		0.26 0.39	0.33 0.5	0.4	٧	
		I <sub>O</sub> =12mA I <sub>O</sub> =24mA		0.26 0.39	0.33 0.5	0.4		
Maximum Input Current	liN	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ	
Maximum 3-State Leakage Current	loz	Output Enable = V <sub>IN</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μА	
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ	
Additional Worst Case Supply Current	ΔΙσο	per input pin  V <sub>1</sub> =2.4V  other Inputs:  at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0µA		2.7	2.9	3.0	mA	

<sup>†</sup> Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

# 8-Bit Universal Shift/Storage Registers with 3-State Outputs

## AC ELECTRICAL CHARACTERISTICS (Input tr., tr<66 ns), HCTLS299

Characteristic		1 1		T <sub>a</sub> = :	,	KS74HCTLS $T_a = -40$ °C to +85°C $V_{CC} = 5.0V \pm 10$ %	KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	Unit		
					Тур		Guarantee	d Limits		
Maximum Clo	ck Frequency	f <sub>max</sub>			35	25	20	18	MHz	
Maximum Pro	pagation Delay,	t <sub>PLH</sub>			26	35	4	53	ns	
CLK to Q'A o		t <sub>PHL</sub>	C <sub>L</sub> =5	OpF	26	35	44	53	113	
Maximum Pro	pagation Delay, r Q' <sub>H</sub>	t <sub>PHL</sub>			30	40	50	60	ns	
Maximum Pro	pagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =5 C <sub>L</sub> =1	0p <b>F</b> 50pF	24 27	32 35	40 45	48 54		
CLK to Q <sub>A</sub> thru Q <sub>H</sub>		t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>l</sub> =150pF		24 27	32 35	40 45	48 54	ns	
Maximum Propagation Delay, CLR to Qa thru QH		tpHL	C <sub>L</sub> =5 C <sub>L</sub> =1	0pF 50pF	30 33	40 43	50 55	.60 66	ns	
- Maximum Ou	Maximum Output Enable Time.		D - 11:0	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	20 23	26 29	33 38	, 39 45	ns	
G1, G2, to C		t <sub>PZL</sub>	R <sub>L</sub> =1kΩ	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	20 23	26 29	33 38	39 45	113	
Maximum Ou	tput Disable Time,	t <sub>PHZ</sub>	$R_L=1k\Omega$		13	17	21	26	ns	
G  1, G  2 to Q	A thru QH	t <sub>PLZ</sub>	C <sub>L</sub> =5	0pF	13	17	21	26		
Minimum	CLK High or Low	tw			10	13	17	20	ns	
Pulse Width	CLR Low	·w			10	13	17	20		
	S0 and S1				13	17	21	-25		
Minimum	High-Level Inputs	tsu			10	13	17	20	ns	
Setup time before CLK1	High-Level Inputs				10	13	17	20		
Delore OLIVI	CLR Inactive		-		10	13	17	20	]	
Minimum Hold Time after CLK1  All Inputs		th			5	7	8	10	ns	
		41				0	0	0		
Maximum Inp	ut Capacitance	CIN				5			pF	
Maximum Ou	tput Capacitance	C <sub>OUT</sub>	Outp	ut Disabled		10			pF	
Power Dissip	ation Capacitance*	CPD							pF	

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.



For AC switching test circuits and timing waveforms see section 2.

- Inverting Version of '153
- Permits Multiplexing from N Lines to 1 Line
- Performs Parallel-to-Serial Conversion
- Strobe (Enable) Line Provided for Cascading (N Lines to n Lines)
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
- (I<sub>OL</sub> = 24 mA @  $V_{OL}$  = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
   KS74AHCT: -40°C to +85°C

KS54AHCT: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

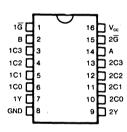
## DESCRIPTION

Each of these data selectors/multiplexers contains inverters and drivers to supply fully complementary binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs (G) are provided for each of the two four-line sections.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### PIN CONFIGURATION

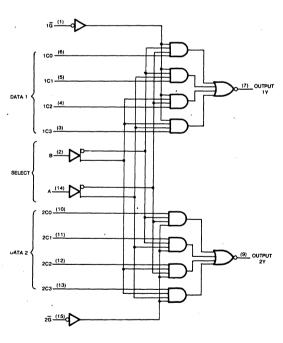


#### **FUNCTION TABLE**

SEL	SELECT		TA	INPU	JTS	STROBE	ОИТРИТ
В.	Α	CO	C1	C2	СЗ	Ğ	Y
Х	Х	Х	Х	Х	Х	Н	H.
L	L	L	Х	Χ	Χ	L	Н
L	Ĺ	Н	Х	Χ	Χ	L	L
L	٠H	Х	L	Χ	Χ	L	Н
L	Н	Х	Н	Χ	Χ	L	L
Н	L	Х	Х	L	Χ	L	Н
Н	L	Х	Х	Н	Χ	L	L
. н	Н	Х	Х	Χ	L	L	Н
Н	Н	Х	Х	Х	Н	L	L

Select inputs A and B are common to both sections.

#### LOGIC DIAGRAM



## **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> , -0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V)$ ±20 mA
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + 2.5V$
Continuous Current Through
Vcc or GND pins ±250 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-
posure to these conditions may affect device reliability

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

		•	
Supply Voltage, V <sub>CC</sub>			4.5V to 5.5V
DC Input & Output '	Voltages*, V <sub>IN</sub> ,	Vout	OV to Vcc
Operating Temperat	ure		
Range	KS74HCTLS:	-40	°C to +85°C
	KS54HCTLS: -		
Input Rise & Fall Tin	nes, t <sub>r</sub> , t <sub>f</sub>		. Max 500 ns

Unused inputs must always be tied to an appropriate logic

voltage level (either V<sub>CC</sub> or GND)

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	Т	<sub>a</sub> = 25°C	KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit
	·	, .	Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH} \text{ or } V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-6\text{mA}$	V <sub>CC</sub>	V <sub>CC</sub> −0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=12mA$ $I_{O}=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin  V <sub>I</sub> =2.4V  other Inputs:  at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0µA		2.7	2.9	3.0	mA

#### 9

## AC ELECTRICAL CHARACTERISTICS (Input tr., tre6 ns), HCTLS352

Characteristic	Symbol	Symbol Conditions <sup>†</sup>		25°C = 5.0V	KS74HCTLS T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%	KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	Unit	
			Тур		Guaranteed	Limits		
Maximum Propagation Delay.	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	23 26	30 33	38 43	45 51	ns	
A or B to Y	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	23 26	30 33	38 43	45 51	ns	
Maximum Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	19 21	26 29	32 37	39 <b>45</b>	-	
Data (Any C) to Y	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	19 21	26 29	32 37	39 <b>4</b> 5	ns	
Maximum Propagation Delay.	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	19 21	26 29	32 37	39 45	ns	
G to Y	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	19 21	26 29	32 37	39. 45	110	
Maximum Input Capacitance	CiN			5			pF	
Power Dissipation Capacitance*	C <sub>PD</sub>						pF	

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

- Inverting Version of '253
- Permits Multiplexing from N lines to 1 line
- Performs Parallel-to-Serial Conversion
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current (I<sub>OL</sub> = 24 mA @ V<sub>OL</sub> = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### DESCRIPTION

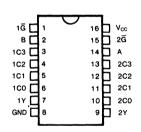
Each of these data selectors/multiplexers contains inverters and drivers to supply full binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs  $(\widetilde{G})$  are provided for each of the two four-line sections.

The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the low-impedance of the single enabled output will drive the bus line to a high or low logic level. Each output has its own strobe (\$\overline{G}\$). The output is disabled when its strobe is high.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{\text{CC}}$  and ground.

#### PIN CONFIGURATION

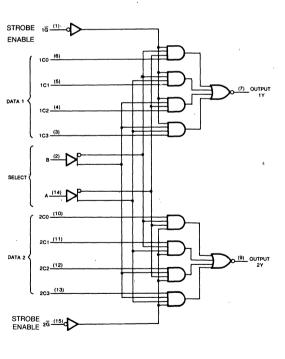


#### **FUNCTION TABLE**

SEL	SELECT		DATA INPUTS		OUTPUT CONTROL	ОИТРИТ	
В	Α	CO	C1	C2	СЗ	Ğ	Y
Х	Х	Х	Х	Х	Х	Н	Z
L	L	L	Х	Х	X	L	Н
L	L	Н	Х	Х	Х	L ·	. L
L	Н	X	L	Х	Х	L	н
L	Н	X	Н	Х	Х	L	L
Н	L	X	Х	L	Х	L	Н
Н	L	Х	Х	Н	Χ	L	L
Н	н	Х	Х	Х	L	L	н
H	Н	Х	Χ.	Х	Н	L	L

Select inputs A and B are common to both sections.

#### LOGIC DIAGRAM



### **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, IIK
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) + \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 70 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-
posure to these conditions may affect device reliability

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

### **Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . . . . . . . 4.5V to 5.5V DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . OV to  $V_{CC}$  Qperating Temperature

Range KS74HCTLS:  $-40^{\circ}$ C to  $+85^{\circ}$ C KS54HCTLS:  $-55^{\circ}$ C to  $+125^{\circ}$ C Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . . Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T	a = 25°C	KS74HCTLS T <sub>a</sub> = -40°C to +85°C	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	v
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $\vdots=-6mA$	V <sub>CC</sub> 4.2	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> =0.1, 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

# Dual 1-of-4 Data Selectors/Multiplexers with 3-State Outputs

## AC ELECTRICAL CHARACTERISTICS (Input tr, tre6 ns), HCTLS353

Characteristic	Symbol Conditions†		Conditions†			KS74HCTLS T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%	KS54HCTLS  T <sub>a</sub> = -55°C to +125°C  V <sub>CC</sub> = 5.0V ± 10%	Unit
,				Тур		Guarantee	a= -55°C to +125°C V <sub>CC</sub> =5.0V ± 10%	
Maximum Propagation Delay, A or B to Any Y	t <sub>PLH</sub>	C <sub>L</sub> =50pl C <sub>L</sub> =150		24 27	32 35	40 45		ns
	t <sub>PHL</sub>	C <sub>L</sub> =50pl C <sub>L</sub> =150		24 27	32 35	40 45		113
Maximum Propagation Delay, Data (any C) to any Y	tpLH	C <sub>L</sub> =50pF C <sub>L</sub> =150pF		15 18	20 23	25 30		ns
	t <sub>PHL</sub>	C <sub>L</sub> =50pl C <sub>L</sub> =150	15 18	20 23	26 31			
Maximum Output Enable	t <sub>PZH</sub>	$R_1 = 1 k\Omega$	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	17 20	23 26	29 34	1	ns
Time, G to Y	tpzL	LIL - I KI	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	17 20	23 26	29 34		113
Maximum Output Disable	t <sub>PHZ</sub>	$R_L = 1 k\Omega$		20	27	34	41	ns
Time, G to Y	tpLZ	CL=50pl	F	20	27	34	41	1113
Maximum Input Capacitance	CIN			5				pF
Maximum Output Capacitance	Cout			10				pF
Power Dissipation	C <sub>PD</sub>							pF

<sup>\*</sup> CPD determines the no-load dynamic power dissipation: PD=CPD Vcc² f + Icc Vcc.

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

## KS54HCTLS 367A/368A KS74HCTLS 367A/368A

## Hex Bus-Drivers with 3-State Outputs

#### **FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current (I<sub>OL</sub> = 24 mA @ V<sub>OL</sub> = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
   (2744071.5: 4090.45 + 8590.5)

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### DESCRIPTION

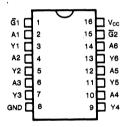
These high-speed Hex bus drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus oriented receivers and transmitters.

The '365 and '366 have two output enables (\$\overline{G}\$1 and \$\overline{G}\$2) NOR'ed together to control all six gates. The '367 and '368 have two output enables which are configured so that one enable (\$\overline{G}\$1) controls four gates and the other (\$\overline{G}\$2) controls the remaining two gates. The '366 and '368 have inverting data paths. The '365 and '367 have noninverting data paths.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V<sub>CC</sub> and ground.

#### PIN CONFIGURATION



#### **FUNCTION TABLES**

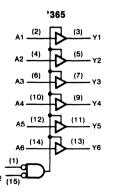
'365 and '366

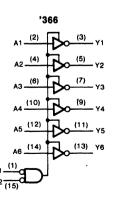
•	lr	puts	,	Y Outputs			
•	Ğ1	Ğ2	A	'365	'366		
	Ĺ	L	L	L	Н		
	L	L	Н	н	L		
	Н	Χ	X	Z	Z		
	Х	Н	X	Z	Z		

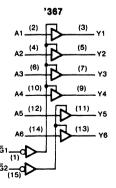
'367 and '368

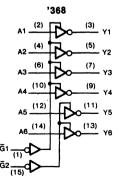
Inputs	Y Outputs			
Ğ1 & Ğ2	A	'367	'368	
. L	L	L	Н	
L	Н	н	L	
н	X	Z	Z	

#### LOGIC DIAGRAMS









## **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_{I} < -0.5V \text{ or } V_{I} > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 70 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, $P_d^{\dagger}$ 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.

These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

## **Recommended Operating Conditions**

		•
Supply Voltage, \	/cc	4.5V to 5.5V
DC Input & Output	ut Voltages*, V <sub>IN</sub> ,	Vout OV to Vcc
Operating Tempe	rature	
Range	KS74HCTLS:	-40°C to +85°C

 $\label{eq:KS54HCTLS:} -55\,^{\circ}\text{C to } +125\,^{\circ}\text{C}$  Input Rise & Fall Times,  $t_r,\,t_f$  . . . . . . . Max 500 ns

#### DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	a = 25°C	KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit		
			Тур		Guaranteed Limits				
Minimum High-Level Input Voltage	VIH	, .		2.0	2.0	2.0	V		
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	0.8	v		
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-6mA$	V <sub>CC</sub> 4.2	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> -0.1 3.7	V		
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 12\text{mA}$ $I_O = 24\text{mA}$	0	0.1 0.26 0.39	. 0.1 0.33 0.5	0.1 0.4	V,		
Maximum Input Current	l <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ		
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μА		
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ		
Additional Worst Case Supply Current	Δlcc	per input pin  V <sub>I</sub> =2.4V  other Inputs: at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0μA*		2.7	2.9	3.0	mA		



<sup>†</sup> Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

 <sup>\*</sup> Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

## KS54HCTLS 367A/368A KS74HCTLS 367A/368A

## Hex Bus-Drivers with 3-State Outputs

## AC ELECTRICAL CHARACTERISTICS (Input tr, tr 66 ns), HCTLS365A, HCTLS367A

Characteristic	Symbol Conditions†		Conditions†					25°C : 5.0V	KS74HCTLS $T_a = -40$ °C to +85°C $V_{CC} = 5.0V \pm 10$ %	KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	Unit
_				Тур	Typ Guaranteed Limits						
Maximum Propagation Delay, A to Y	t <sub>PLH</sub>		C <sub>L</sub> =50pF C <sub>L</sub> =150pF		19 22	24 29	28 34	ns			
	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF		14 17	19 22	<b>24</b> 29	28 34	lis			
Maximum Output Enable	t <sub>PZH</sub>	$R_L = 1 k\Omega$	$C_L = 50pF$ $C_L = 150pF$	26 29	35 38	<b>44</b> 49	52 . 58	ns			
Time, G to Y	t <sub>PZL</sub>	11[-1742	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	26 29	35 38	<b>44</b> 49	52 58				
Maximum Output Disable	t <sub>PHZ</sub>	$R_L = 1 k\Omega$		26	35	44	52	ns			
Time, G to Y	t <sub>PLZ</sub>	C <sub>L</sub> =50pl	F	26	35	44	52	1115			
Maximum Input Capacitance	CIN			5				рF			
Maximum Output Capacitance	Cout	Output disabled		10				рF			
Power Dissipation Capacitance* (per driver)	C <sub>PD</sub>	$\overline{G} = V_{CC}$ $\overline{G} = GND$		5 30				рF			

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC^2} f + I_{CC} V_{CC}$ .

## AC ELECTRICAL CHARACTERISTICS (Input t<sub>r</sub>, t<sub>f</sub>≤6 ns), HCTLS366A, HCTLS368A

Characteristic	Symbol	Conditions†		T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74HCTLS $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 10^{\circ}\text{M}$	KS54HCTLS $T_{a} = -55^{\circ}C \text{ to } +125^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$	Unit
				Тур		Guarantee	d Limits	
Maximum Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF C <sub>L</sub> =50pF C <sub>L</sub> =150pF		13 16	17 20	21 26	25 31	ns
A to Y	t <sub>PHL</sub>			13 16	17 20	21 26	25 31	
Maximum Output Enable	t <sub>PZH</sub>	R <sub>L</sub> =1kΩ	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	26 29	35 38	44 49	<b>52</b> 58	ns
Time, G to Y	t <sub>PZL</sub>	III_IK	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	26 29	35 38	44 49	<b>52</b> 58	
Maximum Output Disable	tpHZ	$R_L = 1 k\Omega$		26	35	44	52	ns
Time, $\overline{G}$ to Y	t <sub>PLZ</sub>	C <sub>L</sub> =50pF		26	35	44	52	113
Maximum Input Capacitance	C <sub>IN</sub>			5				рF
Maximum Output Capacitance	Соит	Output disabled		10				рF
Power Dissipation Capacitance* (per driver)	C <sub>PD</sub>	$\overline{G} = V_{CC}$ $\overline{G} = GND$		5 30				pF

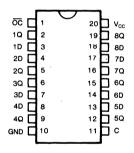
<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

- 8 latches in a single package
- · Full parallel access for loading
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current (loL = 24 mA @ VoL = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
   KS74HCTLS: -40°C to +85°C
   KS54HCTLS: -55°C to +125°C
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATION



#### DESCRIPTION

The '373 consists of 8 high-speed D-type latches coupled to 3-state output buffers with high drive current capability. It can be used in implementing buffer registers, I/O ports, bidirectional bus drivers and working registers.

The latches are transparent: when the enable (C) is high, the Q outputs follow the data (D) inputs. When the enable is low, the outputs latch at the levels that were set up at the D inputs.

The output buffers are controlled by a common signal ( $\overline{OC}$ ) which places the outputs at a high-impedance state when it is taken high. The  $\overline{OC}$  signal does not affect the internal operations of the latches. Old data can be retained or new data can be entered while outputs are off.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

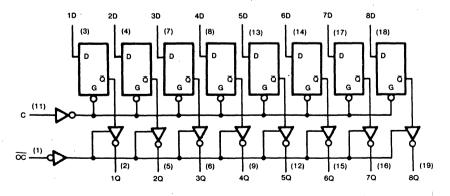
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### **FUNCTION TABLE**

(Each Latch)

	Inputs		Output
<u>oc</u>	Enable C	D	Q
L	Н	Н	Н
L	Н	L	L
·L	L	X	Q <sub>0</sub>
Н	X	Х	Z

#### **LOGIC DIAGRAM**





## . Absolute Maximum Ratings\*

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

, , , , , , , , , , , , , , , , , , ,
Supply Voltage, V <sub>CC</sub> 4.5V to 5.5V
DC Input & Output Voltages*, VIN, VOUT OV to VCC
Operating Temperature
Range KS74HCTLS: -40°C to +85°C
KS54HCTLS: -55°C to +125°C
Input Rise & Fall Times, tr, tf Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Symbol Test Conditions		a = 25°C	KS74HCTLS T <sub>A</sub> = -40°C to +85°C	KS54HCTLS T <sub>A</sub> = -55°C to +125°C	Unit			
			Тур		Guaranteed Limits					
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	, v			
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	V			
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-6mA$	V <sub>CC</sub> 4.2	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	v			
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V.			
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0′	±1.0	μΑ			
Maximum 3-State Leakage Current	l <sub>OZ</sub>	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μА			
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ			
Additional Worst Case Supply Current	ΔΙσο	per input pin V <sub>Z</sub> =2.4V Other Inputs: At V <sub>CC</sub> or GND I <sub>O</sub> =0		2.7	2.9	3.0	mA			

## AC ELECTRICAL CHARACTERISTICS (Input tr, tre6 ns), HCTLS373

Characteristic	Symbol	Cenditions†		T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74HCTLS $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 5.0V \pm 10\%$	$KS54HCTLS$ $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$	Unit
				Тур		Guarantee	d Limits	
Maximum Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> = 50pF C <sub>L</sub> =150pF		14 17	18 21	23 28	27 33	ns
D to Q	t <sub>PHL</sub>	C <sub>L</sub> =50pl C <sub>L</sub> =150		14 17	18 21	23 28	27 33	
Maximum Propagation Delay,	tpLH	C <sub>L</sub> =50pl C <sub>L</sub> =150		22 25	30 33	37 42	45 51	ns
C to any Q	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF		22 25	30 33	37 42	45 51	115
Maximum Output Enable	t <sub>PZH</sub>	Βι=1kΩ	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	24 27	32 35	40 45	48 54	ns
Time, OC to any Q	tpzL		C <sub>L</sub> =50pF C <sub>L</sub> =150pF	24 27·	32 35	40 45	48 54	
Maximum Output Disable Time, OC to any Q	t <sub>PHZ</sub>	R <sub>L</sub> =1kΩ C <sub>L</sub> =50pl	F	19 19	25 25	31 31	37 37	ns
Minimum Pulse Width, C High	t <sub>w</sub>	,		6	10	12	15	ns
Minimum Setup Time, D before C↓	t <sub>su</sub>			2	3	4	5	ns
Minimum Hold Time, D after C↓	th			6	10	12	15	ns
Maximum Input Capacitance	CIN			5				pF
Maximum Output Capacitance	Cout	Output D	isabled	10				рF
Power Dissipation Capacitance* (per latch)	C <sub>PD</sub>	OC=V <sub>CC</sub>		5 30		· . )		pF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

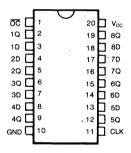
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current
   (I<sub>OL</sub> = 24 mA @ V<sub>OL</sub> = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATION



#### DESCRIPTION

The '374 consists of 8 high-speed D-type edge-triggered flip-flops coupled to 3-state output buffers with high drive current capability. It can be used in implementing buffer registers, I/O ports, bidirectional bus driver and working registers.

The flip-flops are edge-triggered on the positive transition of the clock. The Q outputs are set to the logic levels that were set up at the D inputs.

The output buffers are controlled by a common signal ( $\overline{OC}$ ) which places the outputs at a high-impedance state when it is taken high. The  $\overline{OC}$  signal does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while outputs are off.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

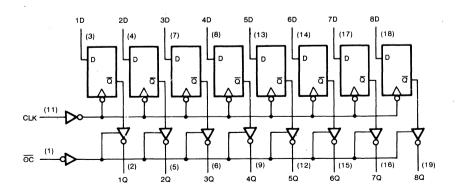
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### **FUNCTION TABLE**

(Each Flip-Flop)

11	nputs	Output	
οc	CLK	D	Q
L	1	Н	Н
L	1	L	L
L	L	Χ	$Q_0$
Н	Χ	Χ	Z

#### LOGIC DIAGRAM



#### **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_0 < V_{CC} + 0.5V) + \pm 70 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW

<sup>\*</sup> Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

#### **Recommended Operating Conditions**

Operating Temperature
Range KS74HCTLS: -40°C to +85°C
KS54HCTLS: -55°C to +125°C
Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . Max 500 ns

\* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

### DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	ons T <sub>a</sub> = 25°C		KS74HCTLS T <sub>a</sub> = -40°C to +85°C	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit	
*		,	Тур		Guaranteed Limits			
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	٧	
Maximum Low-Level Input Voltage	VIL	,		0.8	0.8	0.8	٧	
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-6mA$	V <sub>CC</sub> 4.2	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	v	
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v	
Maximum Input Current	l <sub>IN</sub> .	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ	
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μА	
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ	
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA	

## AC ELECTRICAL CHARACTERISTICS (Input tr., tre6 ns), HCTLS374

Characteristic	Symbol	C <sub>L</sub> =50pF		T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74HCTLS  T <sub>a</sub> = -40°C to +85°C  V <sub>CC</sub> = 5.0V ± 10%	KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	Unit
				Тур		d Limits		
Maximum Operating Frequency	f <sub>max</sub>			45	35	30	25	MHz
Maximum Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pl C <sub>L</sub> =150		21 24	28 31	<b>35</b> 40	<b>42</b> 48	
CLK to any Q	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF		21 24	28 31	<b>35</b> 40	42 48	ns
Maximum Output Disable . Time, OC to any Q	tpzH	R <sub>L</sub> =1kΩ	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	21 24	28 31	35 40	42 48	ns
	tpzL		C <sub>L</sub> =50pF C <sub>L</sub> =150pF	21 24	28 31	35 40	42 48	
Maximum Output Disable	tpHZ	$R_L = 1 k\Omega$		19	25	31	37	ns
Time, OC to any Q	tPLZ	C <sub>L</sub> =50pF		19	25	31	37	113
Minimum Pulse Width, CLK High or Low	tw			7	10	12	15	ns
Minimum Setup Time, D before CLKt	t <sub>su</sub>			10	13	1,7	20	ns
Minimum Hold Time, D after CLK1	t <sub>h</sub>			-3	0	0	0	ns
Maximum Input Capacitance	CiN			5				pF
Maximum Output Capacitance	Cout	Output D	isabled	10				рF
Power Dissipation Capacitance* (per stage)	C <sub>PD</sub>	OC=V <sub>CC</sub> OC=GNI		5 30				pF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

- · Can be used for implementing
  - Buffer/Storage Registers
  - Shift Registers
  - Pattern Generators
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
  - IoL = 8 mA @ VoL = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### DESCRIPTION

The '377 contains eight positive-edge-triggered D-type flip-flops with an enable input. This part is similar to '273 but features a latched clock enable  $(\overline{G})$  instead of a common clear

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse if  $\overline{G}$  is low. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output. The circuits are designed to prevent false clocking by transitioins at the  $\overline{G}$  input.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### PIN CONFIGURATION

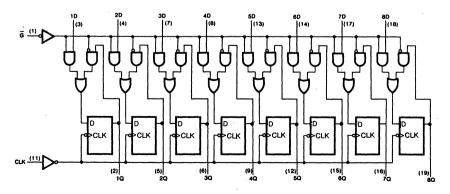
Ğ□	1	$\overline{}$	20	پ∨۔۔
10	2		19	□8Q
1D 🗌	3		18	□8D
2D 🗀	4		17	□7D
2Q 🗀	5		16	□7Q
3Q 🗀	6		15	☐6Q
3D [	7		14	□6D
4D 🗀	8		13	□ 5D
40	9		12	□5Q
GND [	10		11	CLK
				ı

#### **FUNCTION TABLE**

(EACH FLIP-FLOP)

	INPU	OUTPUT			
Ğ	CLK	DATA	Q		
Н	Х	Х	Qo		
L	Ť	н	н		
L	Ť	L	L		
Х	L ·	X	Qo		

#### LOGIC DIAGRAM



# **Absolute Maximum Ratings\***

Supply Voltage Range $V_{CC},\ \dots \ -0.5V$ to $+7V$
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> −65°C to +150°C
Power Dissipation Per Package, $P_d{}^\dagger$ 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Supply Voltage, Vo	c	4.5V to 5.5V
DC Input & Output	Voltages*, V <sub>IN</sub> ,	$V_{OUT}$ OV to $V_{CC}$
Operating Tempera	iture	
Range	KS74HCTLS:	-40°C to +85°C
	KS54HCTLS:	-55°C to +125°C

Characteristic	Symbol	Test Conditions	Т	a = 25°C	KS74HCTLS T <sub>a</sub> = -40°C to +85°C	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	}
Minimum High-Level Input Voltage				2.0	. 2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH} \text{ or } V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-4\text{mA}$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> -0.1 3.84	V <sub>CC</sub> -0.1	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin  V <sub>I</sub> =2.4V  other Inputs:  at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0µA		2.7	2.9	3.0	mA

# AC ELECTRICAL CHARACTERISTICS (Input tr, tre6 ns), HCTLS377

Charact	Characteristic Symbol Condition		Symbol Conditions <sup>†</sup> $T_a = 25^{\circ}C$ $V_{CC} = 5.0V$		KS74HCTLS  T <sub>a</sub> = -40°C to +85°C  V <sub>CC</sub> = 5.0V ± 10%	KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	Unit	
· ·		1		Тур		Guaranteed Limits		
Maximum Clock Fr	equency	f <sub>max</sub>		45	35	30	25	MHz
Maximum Propaga	tion Delay,	tpLH	t <sub>PLH</sub> C <sub>L</sub> =50pF		27	32	38	ns
CLK to Any Q		tPHL	CL=50pr	18	27	32	38	1115
Minimum	G Low	t <sub>w</sub>		12	16	20	25	ns
Pulse Width	CLK high or Low			12	16	20	25	113
Minimum Setup	Data			6	10	15	. 20	ns
Time before CLK1	G high or LOW	t <sub>su</sub>		15	20	25	25	IIS
Minimum Hold Time Data after CLK1	e,	th		-3	0	0	0	ns
Maximum Input Capacitance		CIN		5				pF
Power Dissipation	Capacitance*	C <sub>PD</sub>						pF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

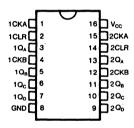
<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

- Individual clock for A and B flip-flops provide dual ÷ 2 and ÷ 5 counters
- · Direct clear for each 4-bit counter
- Significant provement in system density through reduced counter package count.
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
   lot = 8 mA @ Vot = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATION



#### DESCRIPTION

These devices incorporate dual divide-by-two and divide-five counters, which can be used to implement cycle lengths equal to any whole and/or cumulative multiple of 2 and/or 5 up to divide-by-100. When conneoted as a biquinary counter, the separate divide-by-two circuit can be used to provide symmetry (a square ware) at the final outpur stage. The '390 incorporates dual divide-by-two and divide-by-five counters, which can be used to implement cycle lengths equal to any whole and/or cumulative multiples of 2 and/or 5 up to divide-by-100. When connected as a bi-quinary counter, the separate divide-by-tow circuit can be used to provide symmetry (a square wave) at the final outpur stage. The '390 has parallel outputs from each counter stage so that any submultiple of the input count frequency is available for system-timing signals.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### **FUNCTION TABLES**

BCD COUNT SEQUENCE (Each Counter) (See Note A)

COUNT	OUTPUT							
COUNT	QD	Qc	QB	QA				
0	L	L	L	L				
1	L	L	L	Н				
2	L	L	Н	L				
3	L	L	Н	Н				
4	L	Н	L	L				
5	L	Н	L	Н				
6	L	Н	Н	L				
7	L	Н	Н	Н				
8	Н	L	L	L				
9	Н	L	L	Н				

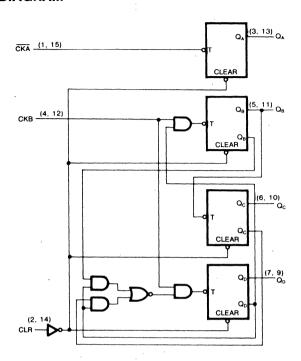
BIQUINARY (5-2) ( Each Counter) (See Note B)

COUNT	OUTPUT						
Joon	QD	Qc	QB	QA			
0	L	L	L	L			
1	L	L	L	Н			
2	L	L	Н	L			
3	L	L	Н	н			
4	L	Н	L	L			
5	Н	L	L	L			
6	Н	L	L	Н			
7	Н	L	Н	L			
8	Н	L	Н	Н			
9	Н	Н	L	L			

NOTES A. Output QA is connected to input CKB for BCD count.

B. Output QD is connected to input CKA for biquinary count.

#### LOGIC DIAGRAM



# **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . . . . . . . . 4.5V to 5.5V DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . OV to  $V_{CC}$  Operating Temperature

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

# DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	a = 25°C	KS74HCTLS T <sub>a</sub> = -40°C to +85°C	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	<b>v</b>
Maximum Low-Level Input Voltage	· VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V <sub>ОН</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> -0.1 3.84	V <sub>CC</sub> -0.1	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

# AC ELECTRICAL CHARACTERISTICS (Input tr, tre6 ns), HCTLS390

	Characteristic		Conditions <sup>†</sup>	, -	25°C : 5.0V	$KS74HCTLS$ $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$	$KS54HCTLS$ $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$	Unit
				Тур		Guarantee	d Limits	
	ock Frequency or CKB to Q <sub>B</sub>	f <sub>max</sub>		35	25	20	20	MHz
Maximum Pr	opagation Delay,	tpLH		15	20	.25	30	ns
CKA to Q <sub>A</sub>		t <sub>PHL</sub>		15	20	25	30	113
Maximum Pr	opagation Delay,	tpLH		36	48	60	72	ns
CKA to Q <sub>C</sub>		tPHL		36	48	60	72	113
Maximum Pr	Maximum Propagation Delay, tplh CKB to QB tphL		$C_L = 50pF$		21	26	31	ns
CKB to Q <sub>B</sub>			OL OOD!	16	21	26	31	
Maximum Pr	aximum Propagation Delay, KB to Q <sub>C</sub>			24	32	40	48	ns
CKB to Q <sub>C</sub>				24	32	40	48	
Maximum Pr	opagation Delay,	t <sub>PLH</sub>	t <sub>PLH</sub>		21	26	31	ns
CKB to Q <sub>D</sub>		t <sub>PHL</sub>		16	21	26	31	
Maximum Pr	opagation Delay, Q	t <sub>PHL</sub>		24	32	40	48	ns
Minimum	CKA or CKB high or low	t <sub>su</sub>		12	16	20	24 .	ns
Pulse Width	CLR high	·Su		12	16	20	24	113
Minimum Setup Time, CLR inactive before CKA or CKB		t <sub>su</sub>		15	20	25	30	ns
Maximum Inp	out Capacitance	CIN		5				pF
Power Dissip	oation Capocitance	C <sub>PD</sub>						pF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} \ V_{CC}^2 \ f + I_{CC} \ V_{CC}$ .
† For AC switching test circuits and timing waveforms see section 2.

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs: IOL = 8 mA @ VOL = 0.5V
- . Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

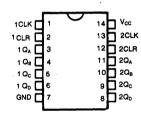
#### DESCRIPTION

The '393 consists of two independent' 4-bit binary counters each with its own clear and clock inputs. N-bit binary counters can be implemented with each package providing the capability of divide-by-256. Parallel outputs from each counter stage provide any submultiple of the input count frequency for system timing signals.

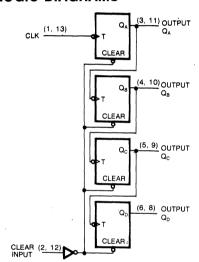
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and vet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V<sub>CC</sub> and

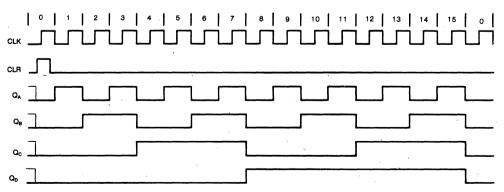
#### PIN CONFIGURATION



#### LOGIC DIAGRAMS



### LOGIC TIMING WAVEFORMS



#### **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
(-0.5V < Vo < Vcc +0.5V) ±35 mA
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Supply Voltage, V<sub>CC</sub> . . . . . . . . . . . . 4.5V to 5.5V DC Input & Output Voltages\*, V<sub>IN</sub>, V<sub>OUT</sub> . . OV to V<sub>CC</sub> Operating Temperature

Operating Temperature

Range KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . Max 500 ns

\* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

Characteristic	Symbol	Test Conditions	T,	= 25°C	KS74HCTLS T <sub>a</sub> = -40°C to +85°C	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit
	*		Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	Vон	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> -0.1 3.84	V <sub>CC</sub> -0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> =20µA I <sub>O</sub> =4mA I <sub>O</sub> =8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1	v
Maximum Input Current	IIN	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin  Vi=2.4V  other Inputs: at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0µA		2.7	2.9	3.0	mA

# AC ELECTRICAL CHARACTERISTICS (Input tr., tre6 ns), HCTLS393

Cha	Characteristic		Characteristic Symbol Condition		Conditions <sup>†</sup>	T <sub>a</sub> =			KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	Unit
				Тур		Guaranteed	i Limits			
Maximum Clock	Frequency	f <sub>max</sub>		40	30	25	20	MHz		
Maximum Propa	gation Delay,	tpLH		15	20	25	30	ns		
A to Q <sub>A</sub>	**	t <sub>PHL</sub>		15	20	25	30	110		
Maximum Propa	gation Delay,	tpLH		26	35	44	53	ns		
A to Q <sub>B</sub>		t <sub>PHL</sub>	C <sub>L</sub> =50pF	26	35	44	53	113		
Maximum Propagation Delay.		t <sub>PLH</sub>			45	56	67	ns		
A to Q <sub>C</sub>	· · · · · · · · · · · · · · · · · · ·	t <sub>PHL</sub>	-	34	45	56	67	110		
Maximum Propa	gation Delay,	tplH		45	60	75	90	ns		
A to Q <sub>D</sub>		t <sub>PHL</sub>		45	60	75	90	113		
Maximum Propa	gation Delay,	t <sub>PHL</sub>		29	39	49	58	ns		
Minimum Pulse	A Input High or Low	t <sub>w</sub>		10	13	17	20	ns		
Width CLR High		] ·w		10	13	17	20	113		
Minimum Hold Time, CLR Inactive before A		t <sub>su</sub>		10	13	17	20	ns		
Maximum Input Capacitance		CiN		5				рF		
Power Dissipati	on Capacitance*	C <sub>PD</sub>	(per counter)	40				pF		

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
  - $I_{OL} = 8 \text{ mA } @ V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
   KS74HCTLS: -40°C to +85°C
   KS54HCTLS: -55°C to +125°C
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### DESCRIPTION

These are high-speed quad 2-port registers. They are the logical equivalent of a quad 2-input multiplexer followed by a quad 4-bit edge-triggered register. A common select input (SEL) selects between two 4-bit input ports. The selected data is transferred to the output register on the low-to-high transition of the clock input.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{\text{CC}}$  and ground.

#### **PIN CONFIGURATION**

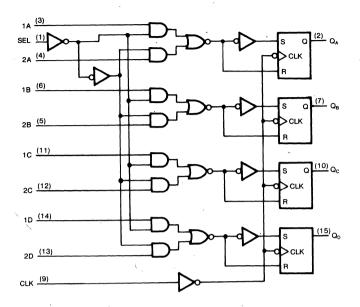
				_	
SEL [	1	$\cup$	16	Ь	Vcc
Q, [	2		15	Ь	$Q_D$
1A 🗀	3		14	Þ	1D
2A 🗀	4		13	þ	2D
2B	5		12		2C
1B 🗀	6		11	Þ	1C
QB [	7		10	Ь	$Q_{C}$
GND 🗀	8		9	Þ	CLK
	<u> </u>			ı	

#### **FUNCTION TABLE**

	Output		
SEL	Port 1	Port 2	Q
ı	ı	Х	L
1	h	Х	Н
h	X	ı	L
h	×	h	Н

- I = Low Voltage Level one setup time prior to the low-to-high clock transition
- h = High Voltage Level one setup time prior to the low-to-high clock transition.

#### LOGIC DIAGRAM



#### Absolute Maximum Ratings\*

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Range KS74HCTLS:  $-40\,^{\circ}\text{C}$  to  $+85\,^{\circ}\text{C}$  KS54HCTLS:  $-55\,^{\circ}\text{C}$  to  $+125\,^{\circ}\text{C}$  Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns

 Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

# DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	= 25°C	KS74HCTLS $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit
	1		Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	VIH			2.0	2.0	2.0	v
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μА
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

# AC ELECTRICAL CHARACTERISTICS (Input tr., tie6 ns), HCTLS399

Characte	Characteristic		Conditions†	T <sub>a</sub> = 2 V <sub>CC</sub> =		KS74HCTLS $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	KS54HCTLS $T_a = -55^{\circ}\text{C to } + 125^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	Unit
				Тур		Guaranteed	Limits	
Propagation Delay	,	t <sub>PLH</sub>	C <sub>L</sub> =50pF	22	30	37	45	ns
CLK to Q or Q		t <sub>PHL</sub>	OL-3001	22	30	37	45	113
Minimum Pulse W	idth,	t <sub>w</sub>		10	13	17	20	ns
Minimum Setup	Data			10	13	17	20	
Time before CLK1	Word Select	t <sub>su</sub>		10	13	17	20	ns
Minimum Hold	Data	th		-3	0	0	0	ns
Time after CLK1	Word Select	<u>س</u>		-3	0	0	0	113
Maximum Input Ca	pacitance	CIN		5				pF
Power Dissipation	Capacitance*	C <sub>PD</sub>	,					рF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

# Dual Retriggerable Monostable Multivibrator with Clear

Preliminary Specifications

#### **FEATURES**

- Simple pulse width formula tw = 0.45RC
- DC triggered from active HIGH or active Low inputs
- Retriggerable for very long output pulses up to 100% duty cycle
- . Overriding clear terminates output pulse
- Schmitt trigger A & B inputs allow infinite rise and fall times on these inputs
- Functions, pin-out, speed and drive compativility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High drive current outputs:
- $I_{OL} = 8mA @ V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range; 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
   KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### DESCRIPTION

The '423 contains dual retriggerable monostable multivibrators with output pulsewidth control by two methods. The basic pulse time is programmed by selection of an external resistor (R<sub>EXT</sub>) and capacitor (C<sub>EXT</sub>). The external resistor and capacitor are normally connected as shown timing component.

Once triggered, the basic output pulse width may be extended by retriggering the gated active Low-going edge input (Ai) or the active High-going edge input (Bi). By repeating this process, the output pulse period (nQ=HIGH,  $n\overline{Q}$ =LOW) can be made as long as desired.

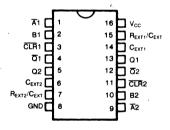
Pulse width stability over a wide range of temperature and supply is achieved using linear CMOS techniques.

The output pulse equation is simply;

 $t_w = 0.45 \times R_{EXT} \times C_{EXT}(typ)$ .

Where  $t_w$  is in seconds. R is in ohm. and C is in fards. All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### PIN CONFIGURATION



#### **FUNCTION TABLE**

· ·	Inputs	Out	puts	
CLR	Ā	В	Q	Q
L	X	Х	L	Н
X	Н	X	L	Н -
X	X	L	L	Н
Н	L	1	J.	T
Н	1	Н	л	T

H= HIGH voltage level

L= LOW voltage level

X= don't care

↑= LOW to HIGH transition

↓= HIGH to LOW transition

.П= one HIGH level output pulse

" one LOW level output pulse

# **Absolute Maximum Ratings\***

Supply Voltage Range $V_{CC}, \dots -0.5V$ to +7V DC Input Diode Current, $I_{IK}$
(V <sub>I</sub> <-0.5V or V <sub>I</sub> >V <sub>CC</sub> +0.5V) ±20 mA
DC Output Diode Current, IOk
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous OUtput Current Per Pin, Io
(-0.5V <v<sub>O<v<sub>CC+0.5V) ±35 mA</v<sub></v<sub>
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> -65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-
posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package(N): -12mW/°C from 65°C to 85°C Ceramic Package(J): -12mW/°Cfrom100°C to 125°C

# **Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ...... 4.5V to 5.5V DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ..... 0V to  $V_{CC}$  Operating Temperature

Range

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

Characteristic	Symbol	Test Conditions	T,	$T_a = 25$ °C KS74HCTLS $T_a = -40$ °C to H		KS54HCTLS C T <sub>a</sub> = -55°C to +125°C	
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	VIL	·		0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-4m A$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> =0.1	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current		per input in V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

#### AC ELECTRICAL CHARACTERISTICS (Input tr. tre6 ns), HCTLS423

Characteristic	Symbol	Conditions <sup>†</sup>	T <sub>s</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74AHCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$	KS54AHCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	Unit
			Тур		Guaranteed	Limits	
Propagation Delay	tpLH		23	33	41	50	ns
Ā, B to Q, Q	tpHL	C <sub>L</sub> =50pF	23	33	41	50	]
Propagation Delay	tpLH	C <sub>ext</sub> =0,	20	27	34	41	ns
CLR to Q, Q	tpHL	R <sub>ext</sub> =5kΩ	20	27	34	41	
Output Pulse Width 1	twq1		116	200	207	209	ns
Output Pulse Width 2	twq2	$C_L$ =50pF $C_{ext}$ =1000pF $R_{ext}$ =10k $\Omega$	4.5	4.0 5.0	3.8(min) 5.2(max)	2.7(min) 7.5(max)	μS
Trigger Pulse Width	t <sub>w</sub>	C <sub>L</sub> =50pF A <sub>I</sub> =LOW	7	20	25	30	ns
Trigger Pulse Width	tw	C <sub>L</sub> =50pF B <sub>i</sub> =High	7	20	25	30	ns
Clear Pulse Width	t <sub>w</sub>	C <sub>L</sub> =50pF CLR <sub>i</sub> =LOW	8	20	25	30	ns
External Timing Resistance	Rext			2 1000	2(min) 1000(max)	2(min) 1000(max)	kΩ
External Timing Capacitance	Cin				no restriction	n	
Input Capacitance	Cin		5				pF
Power Dissipation Capacitance	C <sub>PD</sub>						pF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

# **Application Information**

The basic output pulse width is determined by the value of external capacitance and timing resistance. For output pulse widths greater than  $100\mu s$  or external capacitance greater than 1000pF the following equation should be used.

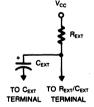
 $t_w = k \cdot R_{ext} \cdot C_{ext}$ 

Where

 $t_W$  is in second K is the multiplying factor and is approximately 0.45 for  $C_{ext} \ge 1000 pF$   $C_{ext}$  is in F

For best results, system ground should be applied to the  $C_{\text{ext}}$  terminal. These devices do not require a switching diode in series with the  $R_{\text{ext}}/C_{\text{ext}}$  terminal (as required by some other monostable multivibrators)

#### **TIMING COMPONENT**



<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current (lo<sub>L</sub> = 24 mA @ V<sub>OL</sub> = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
   KS74HCTLS: -40°C to +85°C
- KS54HCTLS: -55°C to +125°C
   Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### DESCRIPTION

These high-speed octal buffers and drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The designer has the choice of inverting/noninverting outputs and various types of output controls.

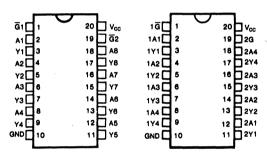
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### PIN CONFIGURATIONS

#### '465 and '466

'467 and '468

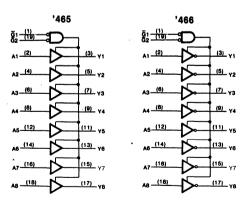


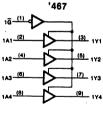
#### **FUNCTION TABLE**

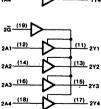
	Input	Out	put	
$\overline{\mathbf{G}_{i}}$	<b>G</b> ₂	A	'465	'466
L	L	L	L	Н
L	L	Н	н	L
н	×	X	Z	Z
X	H	X	Z	Z

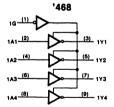
#### Input Output Ğ G A '467 '468 Н L L L н Н L Н н Н X z z

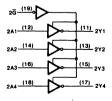
### LOGIC DIAGRAMS











# KS54HCTLS 467/468

# Octal Buffers and Line Drivers with 3-State Outputs

# **Absolute Maximum Ratings\***

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Range KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . Max 500 ns

 Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

Characteristic	Symbol	Test Conditions	T,	= 25°C	KS74HCTLS T <sub>a</sub> = -40°C to +85°C	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-6mA$	V <sub>CC</sub> 4.2	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1° 0.33 0.5	0.1 (0.4	v
Maximum Input Current	lin	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μА
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND	**	±0.5	±5.0	±10.0	μĄ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA



# KS54HCTLS 467/468 KS74HCTLS 467/468

# Octal Buffers and Line Drivers with 3-State Outputs

# AC ELECTRICAL CHARACTERISTICS (Input tr. tr<6 ns), HCTLS465, HCTLS466, HCTLS467, HCTLS468

Characteristic	Symbol	abol Conditions		54/74/ T <sub>a</sub> = 2 V <sub>CC</sub> =	25°C	KS74HCTLS T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5V ± 10%	54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	Unit	
				Тур		Guara	anteed Limits		
Maximum Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF		11 14	15 18		22 28		
A to Y		C <sub>L</sub> =50pF C <sub>L</sub> =150pF		11 14	15 18		22 28	ns	
Maximum Output Enable Time	t <sub>PZH</sub>	R <sub>L</sub> =1kΩ	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	24 27	32 35		.48 54	ns	
Enable to Y			C <sub>L</sub> =50pF C <sub>L</sub> =150pF	24 27	32 35		48 54		
Maximum Output disable Time,	t <sub>PHZ</sub>	$R_L = 1 k\Omega$		24	32	40	48		
Enable to Y	tpLZ	C <sub>L</sub> =50pl	C <sub>L</sub> =50pF		32	40	48	ns	
Maximum Input Capacitance	Cin			4			,	pF	
Maximum Output Capacitance	Cout	Output D	isabled	10		,		рF	
Power Dissipation Capacitance* (per stage)	C <sub>PD</sub>		output Disabled					рF	

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

- · Compares two 8-bit words
- '518, '520 and '522 have 20KΩ Pull-up resistors on Q inputs

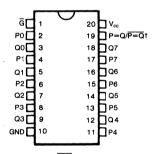
TYPE	INPUT PULL-UP RESISTOR	OUTPUT FUNCTION AND CONFIGURATION
'518	Yes	P=Q open-drain
'519	No	P=Q open-drain
'520	Yes	P=Q totem-pole
'521	No	P=Q totem-pole
'522	Yes	P=Q open-drain

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current (loL = 24 mA @ VoL = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
   KS74HCTLS: \_40°C to \_485°C

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATION



 $\dagger$  P=Q for '518 and '519;  $\overline{P}=Q$  for '520, '521, '522.

#### **DESCRIPTION**

These identity comparators perform comparisons on two eight-bit binary or BCD words. The '518 and '519 provide P=Q outputs, while the '520, '521, and '522 provide  $\overline{P}=\overline{Q}$  outputs. The '518, '519, and '522 have open-drain outputs. The '518, '520, and '522 feature 20-k $\overline{Q}$  inputs for analog or switch data.

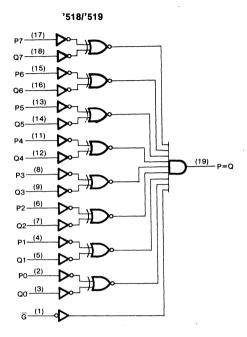
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface, with TTL, NMOS and CMOS devices without any external components.

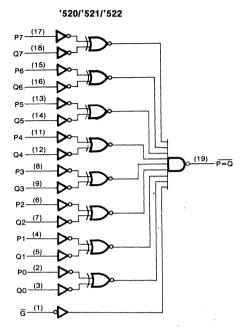
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### **FUNCTION TABLE**

IN	PUTS	OUTPUTS			
DATA P, Q	ENABLE G	P=Q	P=Q		
P=Q	L	н	L		
P>Q	L.	L	Н		
P <q< td=""><td>L</td><td>L</td><td>Н</td></q<>	L	L	Н		
X	н	L	Н		

#### LOGIC DIAGRAMS





# Absolute Maximum Ratings\*

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, IIK
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±70 mA
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, T <sub>stg</sub> −65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Abaduta Marianus Dationa are those values become

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): —12mW/°C from 65°C to 85°C Ceramic Package (J): —12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Supply Voltage, V<sub>CC</sub> . . . . . . . . . . 4.5V to 5.5V DC Input & Output Voltages,\*, V<sub>IN</sub>, V<sub>OUT</sub> . . OV to V<sub>CC</sub> Operating Temperature

Range KS74HCTLS:  $-40\,^{\circ}\text{C}$  to  $+85\,^{\circ}\text{C}$  KS54HCTLS:  $-55\,^{\circ}\text{C}$  to  $+125\,^{\circ}\text{C}$  Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . . Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

Parameter	Symbol Test Conditions		ol Test Conditions T <sub>a</sub> = 25°C		KS74HCTLS T <sub>A</sub> = -40°C to +85°C	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit
		,	Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	VIH		,	2.0	2.0	2.0	v
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage (Totem-pole Outputs)	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-6mA$	V <sub>CC</sub> 4.2	V <sub>CC</sub> -0.1 3.93	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	V
Maximum Low-Level Output Voltage (All Outputs)	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=12mA$ $I_{O}=24mA$	С	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current, ('518, '520 and '522 Q input)		V <sub>CC</sub> =Max V <sub>IN</sub> =2.7V V <sub>IN</sub> =0.4V		-0.2 -0.6	-0.2 -0.6	-0.2 -0.6	mA
Maximum Input Current (All other Inputs)	IIN	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Output Leakage Current (Open-Drain Outputs)	loz	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> =V <sub>CC</sub>		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent	lcc	For '518, '520 and '522: V <sub>IN</sub> =GND (Q0-Q7) V <sub>IN</sub> =V <sub>CC</sub> or GND (all other inputs)		3.5	3.5	3.5	mA
Supply Current	,	For '519 and '521: $V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	ΔΙσο	per input pin  V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0µA		2.7	2.9	3.0	mA



# AC ELECTRICAL CHARACTERISTICS (Input tr., tr≤6 ns), HCTLS518, HCTLS519

Characteristic	Symbol	Conditions	1	ACHT 25°C = 5V	KS74HCTLS  T <sub>a</sub> = -40°C to +85°C  V <sub>CC</sub> = 5V ± 10%	54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> =5.0V ± 10%	Unit	
		′	Typ Guaranteed Limits			enteed Limits	7 '	
Maximum Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	26 29	33 36	40 45	47 53		
from P or Q to P=Q	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	21 24	28 31	35 40	42 48	ns	
Maximum Propagation Delay,	t <sub>PLH</sub>	C=50pF C <sub>L</sub> =150pF	23 26	29 32	35 40	41 47		
from G to P=Q	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	18 21	24 .27	30 35	36 42	ns	
Maximum Input Capacitance	CIN		5				pF	
Maximum Output Capacitance	Cout						рF	
Power Dissipation Capacitance*	C <sub>PD</sub>						рF	

# AC ELECTRICAL CHARACTERÍSTICS (Input tr, tr≤6 ns), HCTLS520, HCTLS521

Characteristic	Symbol	Conditions	54/74ACHT T <sub>a</sub> = 25°C V <sub>CC</sub> = 5V		KS74HCTLS T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5V ± 10%	54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	Unit
			Тур		Guar	anteed Limits	
Maximum Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	12 15	22 25	28 33	33 39	ns
from P or Q to P=Q	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	16 19	22 25	28 33	33 39	
Maximum Propagation Delay,	t <sub>PLH</sub>	C=50pF C <sub>L</sub> =150pF	15 18	20 23	25 30	30 36	ns
from $\overline{G}$ to $\overline{P}=Q$	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	15 18	20 23	25 30	30 36	
Maximum Input Capacitance	CIN		5				рF
Maximum Output Capacitance	Соит						рF
Power Dissipation Capacitance*	C <sub>PD</sub>						pF

#### AC ELECTRICAL CHARACTERISTICS (Input tr, tres ns), HCTLS522

Characteristic	Symbol	Symbol Conditions		ACHT 25°C = 5V	KS74HCTLS  T <sub>a</sub> = -40°C to +85°C  V <sub>CC</sub> = 5V ± 10%	54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	Unit
			Тур	Typ Guara		nteed Limits	
Maximum Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	24 27	31 34	37 42	43 49	
from P or Q to P=Q	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	19 22	26 29	32 37	38 44	ns
Maximum Propagation Delay,	t <sub>PLH</sub>	C=50pF C <sub>L</sub> =150pF	23 27	29 32	35 40	41 47	200
from $\bar{G}$ to $\bar{P}=\bar{Q}$	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	18 21	24 27	30 35	36 42	ns
Maximum Input Capacitance	CIN		5				рF
Power Dissipation Capacitance*	C <sub>PD</sub>						рF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

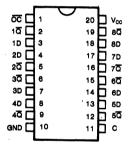


# Octal D-Type Transparent Latches with 3-State Outputs

#### **FEATURES**

- · 8 latches in a single package
- · Full parallel access for loading
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current (loL = 24 mA @ VoL = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges: KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### **PIN CONFIGURATION**



#### **DESCRIPTION**

The '533 consists of 8 high-speed D-type latches coupled to 3-state output buffers with high drive current capability. It can be used in implementing buffer registers, I/O ports, bidirectional bus drivers and working registers.

The latches are transparent: when the enable (C) is high, the  $\overline{\mathbb{Q}}$  outputs follow the complements of the data (D) inputs. When the enable is low, the outputs latch at the levels that were set up at the D inputs.

The output buffers are controlled by a common signal ( $\overline{OC}$ ) which places the outputs at high-impedance state when it is taken high. The  $\overline{OC}$  signal does not affect the internal operations of the latches. Old data can be retained or new data can be entered while outputs are off.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

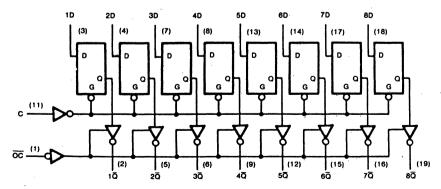
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### **FUNCTION TABLE**

(Each Latch)

	Inputs	Output	
<u>oc</u>	Enable C	. D	ā
L	Н	Н	L
L	Н	L	Н
L	L	Х	Ō₀
Н	X	X	Z

#### LOGIC DIAGRAM



### **Absolute Maximum Ratings\***

Supply Voltage Range $V_{CC}$ , $-0.5V$ to $+7V$
DC Input Diode Current, I <sub>IK</sub>
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mÅ}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 70 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, $T_{stg} \dots -65$ °C to $+150$ °C
Power Dissipation Per Package, $P_d^{\dagger}$ 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-
posure to these conditions may affect device reliability.

<sup>†</sup> Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Supply Voltage, V <sub>CC</sub>	4.5V to 5.5V
DC Input & Output Voltages*, VIN, VOUT	OV to Vcc
Operating Temperature	

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . . Max 500 ns

 Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

Characteristic	Symbol	Symbol Test Conditions		= 25°C	KS74HCTLS T <sub>a</sub> = -40°C to +85°C	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit			
			Тур	Typ Guaranteed Limits						
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	٧			
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧			
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-6mA$	V <sub>CC</sub> 4.2	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> = 0.1 3.84	V <sub>CC</sub> −0.1 3.7	v			
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v			
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ			
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μΑ			
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ			
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA			

# AC ELECTRICAL CHARACTERISTICS (Input tr, tr 46 ns), HCTLS533

Characteristic	Symbol Conditions†		Conditions <sup>†</sup>		Conditions†		25°C : 5.0V	KS74HCTLS  T <sub>a</sub> = -40°C to +85°C  V <sub>CC</sub> = 5.0V ± 10%	KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> =5.0V ± 10%	Unit
				Тур		Guaranteed	Limits			
Maximum Propagation	t <sub>PLH</sub>		CL=50pF CL=150pF		18 21	23 28	27 33			
Delay, D to Q	t <sub>PHL</sub>	C <sub>L</sub> =50p C <sub>L</sub> =150		14 17	18 21	23 28	27 33	ns		
Maximum Propagation	t <sub>PLH</sub>	C=50pF C <sub>L</sub> =150		22 25	30 33	37 43	45 41			
Delay C to Q	t <sub>PHL</sub>	C <sub>L</sub> =50p C <sub>L</sub> =150		22 25	30 33	37 43	48 54	ns		
Time, OC to any Q	t <sub>PZH</sub>	Rı = 1kΩ	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	24 27	. 32 35	40 45	48 54			
	t <sub>PZL</sub>	HL= IKW	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	24 27	32 35	· 40 45	48 54	ns		
Maximum Output Disable	t <sub>PHZ</sub>	$R_L=1k\Omega$		19	25	31	37	ns		
Time, OC to any Q	t <sub>PLZ</sub>	C <sub>L</sub> =50p	F	19	25	31	37	113		
Minimum Pulse Width, C High	tw			6	10	12	15	ns		
Minimum Setup Time, D before C↓	t <sub>su</sub>		,	2	3	4 ·	5	ns		
Minimum Hold Time, D after C↓	t <sub>n</sub>			6	10	12	15	ns		
Maximum Input Capacitance	C <sub>IN</sub>					,		рF		
Maximum Output Capacitance	Соит	Output D	Output Disabled					pF		
Power Dissipation Capacitance* (per stage)	C <sub>PD</sub>	OC=V <sub>CC</sub> OC=GNI		5 30				pF		

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.



<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

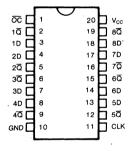
- · Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- . 3-State outputs with high drive current
  - ( $I_{OL} = 24 \text{ mA} @ V_{OL} = 0.5 \text{V}$ ) for direct bus interface
- . Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- · Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATION



#### DESCRIPTION

The '534 consists of 8 high-speed D-type edge-triggered flip-flops coupled to 3-state output buffers with high drive current capability. It can be used in implementing buffer registers, I/O ports, bidirectional bus driver and working registers.

The flip-flops are edge-triggered on the positive transition of the clock: the Q outputs are set to the complement of the logic levels that were set up at the D inputs.

The output buffers are controlled by a common signal (OC) which places the outputs in high-impedance state when it is taken high. The OC signal does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while outputs are off.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

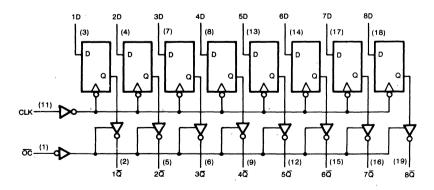
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V<sub>CC</sub> and around.

#### **FUNCTION TABLE**

(Each Latch)

1	nputs		Output
ŌĊ	CLK	D	ā
L	<b>†</b>	H	L
L	<b>↑</b>	L	Н
L	L	Χ	$\overline{\mathtt{Q}}_{\mathtt{0}}$
Н	Χ	X	Z

#### LOGIC DIAGRAM



# Absolute Maximum Ratings\*

Power Dissipation Per Package, Pat. . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

### **Recommended Operating Conditions**

Supply Voltage, V <sub>CC</sub>	4.5V to 5.5V
DC Input & Output Voltages*, VIN, VOUT	OV to Vcc
Operating Temperature	

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . Max 500 ns

Characteristic	Symbol	Test Conditions	T <sub>a</sub> = 25°C		KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$	Unit
1.			Тур		Guaranteed Lim	its	7
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-6mA$	V <sub>CC</sub> 4.2	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> -0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	. 0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	>
Maximùm Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μА
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current		per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

 <sup>\*</sup> Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

# AC ELECTRICAL CHARACTERISTICS (Input tr, tre6 ns), HCTLS534

Characteristic	Symbol			bol Conditions†		T <sub>a</sub> =		KS74HCTLS T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%	KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> =5.0V ± 10%	Unit
				Тур		Guaranteed Limits				
Maximum Operating Frequency	f <sub>max</sub>	C <sub>L</sub> =50pl	C <sub>L</sub> =50pF		35	30	25	MHz		
Maximum Propagation	t <sub>PLH</sub>	C <sub>L</sub> =50pl C <sub>L</sub> =150	CL=50pF 2 CL=150pF 2		28 31	· 35 40	<b>42</b> 48			
Delay, CLK to any Q	t <sub>PHL</sub>	C <sub>L</sub> =50pl C <sub>L</sub> =150		21 24	28 31	35 40	42 48	ns		
Maximum Output Enable Time, OC to any Q	t <sub>PZH</sub>	R <sub>L</sub> =1kΩ	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	21 24	28 31	35 40	42 48			
				21 24	28 31	35 40	42 48	ns		
Maximum Output Disable	t <sub>PHZ</sub>	$R_L = 1k\Omega$		19	25	31	37			
Time, OC to any Q	tpLZ	C <sub>L</sub> =50pl	F	19	25	31	37	ns		
Minimum Pule Width, CLK High or Low	tw			9	13	15	18	ns		
Minimum Setup Time, D before CLK†	tsu			10	13	17	20	ns		
Minimum Hold Time, D after CLKt	t <sub>h</sub>			-3	0	0	0	ns		
Maximum Input Capacitance	C <sub>IN</sub>							pF		
Maximum Output Capacitance	Соит	Output D	isabled	10				pF		
Power Dissipation Capacitance* (per stage)	C <sub>PD</sub>	OC=V <sub>CC</sub>		5 30 .				pF		

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current (I<sub>OL</sub> = 24 mA @ V<sub>OL</sub> = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### **DESCRIPTION**

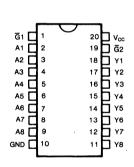
The '540 and '541 are general purpose high-speed octal line drivers/buffers with 3-state outputs. The inputs and outputs are located on opposite sides of the 20-pin package, thus improving circuit board density. The '540 provides inverted data and the '541 provides true data at the outputs.

The three-state control gate is a 2-input NOR such that if either  $\overline{G}1$  or  $\overline{G}2$  is high, all eight outputs are in the high impedance state.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground

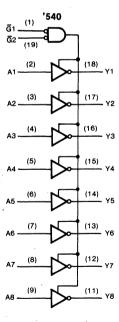
#### PIN CONFIGURATION

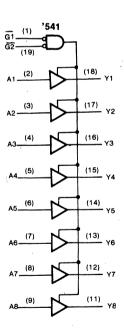


#### **FUNCTION TABLE**

	Input	Out	put	
<b>G</b> ₁	<b>G</b> ₂	A	'540	'541
L	L	L	Н	L
L	L	H .	L	Н
Н	X	×	Z	Z
X	Н	Х	Z	Z

#### LOGIC DIAGRAMS





# KS54HCTLS **540/541** KS74HCTLS

# Octal Buffers and Line Drivers with 3-State Outputs

# **Absolute Maximum Ratings\***

Supply Voltage Range $V_{CC}, \ldots -0.5V$ to $+7V$
DC Input Diode Current, I <sub>IK</sub>
$(V_{I} < -0.5V \text{ or } V_{I} > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 70 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, $T_{stg} \dots -65$ °C to $+150$ °C
Power Dissipation Per Package, $P_d{}^\dagger$ 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.  These are stress ratings only and functional operation.

of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

### **Recommended Operating Conditions**

Supply Voltage, V <sub>CC</sub>	4.5V to 5.5V
DC Input & Output Voltages*, VIN, VOUT	OV to Vcc
Operating Temperature	

\* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

Characteristic	Symbol	Test Conditions	T,	= 25°C	KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-6m A$	V <sub>CC</sub> 4.2	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ

<sup>†</sup> Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# Octal Buffers and Line Drivers with 3-State Outputs

# AC ELECTRICAL CHARACTERISTICS (Input tr, tre6 ns), HCTLS540, HCTLS541

Characteristic	Symbol Conditions†		T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74HCTLS  T <sub>a</sub> = -40°C to +85°C  V <sub>CC</sub> = 5.0V ± 10%	KS54HCTLS  T <sub>a</sub> = -55°C to +125°C  V <sub>CC</sub> = 5.0V ± 10%	Unit		
				Тур		Guaranteed Limits			
Maximum Propagation	' t <sub>PLH</sub>	C <sub>L</sub> = 50pF C <sub>L</sub> =150pF C <sub>L</sub> = 50pF C <sub>L</sub> =150pF		11 14	15 18	19 24	23 29	ns	
Delay, A to Y	t <sub>PHL</sub>			11 14	15 18	19 24	23 29		
Maximum Output Enable Time, $\overline{G}$ to Y	t <sub>PZH</sub>		C <sub>L</sub> = 50pF C <sub>L</sub> =150pF	18 21	25 28	25 30	37 43	-	
	tpzL		C <sub>L</sub> =50pF C <sub>L</sub> =50pF	18 21	25 28	31 36	37 43	ns	
Maximum Output Disable	tpHZ	R <sub>L</sub> =1kΩ		13	18	23	27		
Time, G to Y	tpLZ	C <sub>L</sub> =50pF		13	18	23	27	ns	
Maximum Input Capacitance	CIN	. 1		5				pF	
Maximum Output Capacitance	Cout	Output Disabled		10		,		pF	
Power Dissipation Capacitance* (per stage)	C <sub>PD</sub>	Ğ=V <sub>CC</sub> Ğ=GND		5 30				pF	

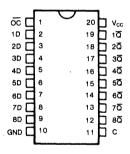
<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} \ V_{CC}^1 \ f + I_{CC} \ V_{CC}$ .
† For AC switching test circuits and timing waveforms see section 2.

- 8 latches in a single package
- · Full parallel access for loading
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current
- $(I_{OL} = 24 \text{mA} @ V_{OL} = 0.5 \text{V})$  for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
   KS74AHCT: -40°C to + 85°C

KS54AHCT: -55°C to + 125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATION



#### **DESCRIPTION**

The '563 consists of 8 high-speed D-type latches coupled to 3-state output buffers with high drive current capability. It can be used in implementing buffer register, I/O ports, bidirectional bus drivers and working registers.

The latches are transparent; when the enable (C) is high, the Q outputs follow complements of the data (D) inputs. When the enable is low, the outputs latch at the levels that were set up at the D inputs.

The output buffers are controlled by a common signal (OC) which places the outputs at a high-impedance stage when it is taken high. The OC signal does not affect the internal operations of the latches. Old data can be retained or new data can be entered while outputs are off.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

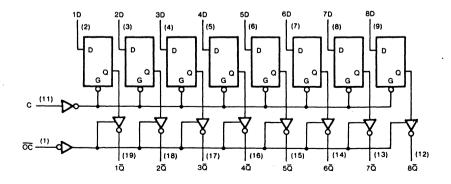
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{\text{CC}}$  and ground.

#### **FUNCTION TABLE**

(Each Latch)

	Inputs		Output
ŌĊ	Enable C	D	ā
L	Н	Н	L
L	н	L	Н
L	L	X	$\bar{\mathbf{Q}}_{0}$
Н	×	X	Z

#### LOGIC DIAGRAM



# Octal D-Type Transparent Latches with 3-State Outputs

# **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 70 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Ratings are those values beyond

<sup>\*</sup> Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

### **Recommended Operating Conditions**

	•	_	
Supply Voltage,	V <sub>CC</sub>	4.5	V to 5.5V
DC Input & Outp	ut Voltages*, V <sub>IN</sub> ,	Vout	OV to Vcc
Operating Tempe	erature		*
Range	KS74HCTLS:	-40°C	to +85°C

Characteristic Symbol Test Conditions		Test Conditions	T <sub>a</sub> = 25°C		KS74HCTLS KS54HCTLS $T_a = -40$ °C to $+85$ °C $T_a = -55$ °C to $+125$ °		Unit
		Тур	yp Guaranteed Limits				
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	٧
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-6mA$	V <sub>CC</sub> 4.2	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	٧
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	l <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	. ±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA



<sup>†</sup> Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

 <sup>\*</sup> Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

# AC ELECTRICAL CHARACTERISTICS (Input tr, tre6 ns), HCTLS563

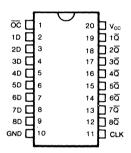
Characteristic	Symbol	Conditions <sup>†</sup>		T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74HCTLS  T <sub>a</sub> = -40°C to +85°C  V <sub>CC</sub> = 5.0V ± 10%	KS54HCTLS  T <sub>a</sub> = -55°C to +125°C  V <sub>CC</sub> =5.0V ± 10%	Unit
			Тур	Typ Guaranteed Limits				
Maximum Propagation	tpLH	C <sub>L</sub> = 50 C <sub>L</sub> =150		14 17	18 21	23 28	27 33	
Delay, D to Q	t <sub>PHL</sub>	C <sub>L</sub> = 50 C <sub>L</sub> =150		14 17	18 21	23 28	27 33	ns
Maximum Propagation	t <sub>PLH</sub>	C= 50p C <sub>L</sub> =150		22 25	30 33	37 42	45 51	
Delay C to Q	t <sub>PHL</sub>	C <sub>L</sub> = 50pF C <sub>1</sub> =150pF		22 25	30 33	37 42	45 51	ns
Maximum Output Enable Time, OC to any Q	t <sub>PZH</sub>	R <sub>i</sub> = 1kΩ	C <sub>L</sub> = 50pF C <sub>L</sub> =150pF		32 35	40 45	48 54	
	t <sub>PZL</sub>	1112	C <sub>L</sub> = 50pF C <sub>L</sub> =150pF	1 .	32 35	40 45	48 54	ns
Maximum Output Disable Time, OC to any Q	t <sub>PHZ</sub>	$R_L = 1 k\Omega$ $C_L = 50 pl$	-	19 19	25 25	31 31	37 37	ns
Minimum Pulse Width, C High	t <sub>w</sub>			9	13	15	18	ns
Minimum Setup Time, D before C↓	t <sub>su</sub>			6	8	10	10	ns
Minimum Hold Time, D after C↓	th			6	10	12	15	ns
Maximum Input Capacitance	CiN			5				рF
Maximum Output Capacitance	Cout	Output D	isabled	10				рF
Power Dissipation Capacitance* (per stage)	C <sub>PD</sub>	ÖC=V <sub>CC</sub> ÖC=GNI		5 30				pF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current
   (I<sub>OL</sub> = 24 mA @ V<sub>OL</sub> = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
   KS74HCTLS: -40°C to +85°C
   KS54HCTLS: -55°C to +125°C
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

### PIN CONFIGURATION



#### DESCRIPTION

The '564 consists of 8 high-speed D-type edge-triggered flip-flops coupled to 3-state output buffers with high drive current capability. It can be used in implementing buffer registers, I/O ports, bidirectional bus driver and working registers.

The flip-flops are edge-triggered: on the positive transition of the clock, the  $\overline{\mathbb{Q}}$  outputs are set to the complement of the logic levels that were set up at the D inputs.

The output buffers are controlled by a common signal ( $\overline{OC}$ ) which places the outputs at high impedance state when It is taken high. The  $\overline{OC}$  signal does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while outputs are off.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

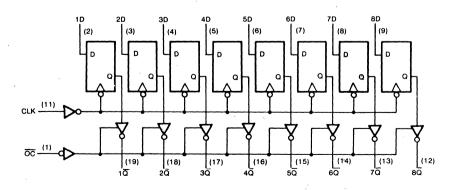
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{\text{CC}}$  and ground.

#### **FUNCTION TABLE**

(Each Flip-Flop)

ı	nputs	Output	
ŌĈ	CLK	D	Q
L	1	Н	L
L	<b>↑</b>	L	н
L	L	Х	$\vec{Q}_{o}$
Н	Х	Χ	Z

#### LOGIC DIAGRAM



### **Absolute Maximum Ratings\***

Supply Voltage Range $V_{CC}$ , $-0.5V$ to $+7V$
DC Input Diode Current, I <sub>IK</sub>
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V)$ $\pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 70 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, $T_{stg} \dots -65^{\circ}\text{C}$ to $+150^{\circ}\text{C}$
Power Dissipation Per Package, Pd† 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

### **Recommended Operating Conditions**

Range KS74HCTLS:  $-40^{\circ}$ C to  $+85^{\circ}$ C KS54HCTLS:  $-55^{\circ}$ C to  $+125^{\circ}$ C Input Rise & Fall Times,  $t_r$ ,  $t_t$  . . . . . . Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

Characteristic	Symbol	Test Conditions		<sub>a</sub> = 25°C	KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS $T_a = -55^{\circ}C \text{ to } +125^{\circ}C$	Unit
			Тур		Guaranteed Lim	its	1
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	Voh	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-6mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	liN	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

# AC ELECTRICAL CHARACTERISTICS (Input tr., tr. 60, ns), HCTLS564

Characteristic	Symbol	ol Conditions†		T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74HCTLS T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%	KS54HCTLS T <sub>e</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	Unit	
				Тур		1 Limits			
Maximum Operating * Frequency	f <sub>max</sub>	C <sub>L</sub> = 50	C <sub>L</sub> = 50pF		35	30	25	MHz	
Maximum Propagation Delay,	t <sub>PLH</sub>		C <sub>L</sub> = 50pF C <sub>L</sub> =150pF		28 31	35 40	42 48		
CLK to any Q	t <sub>PHL</sub>	C <sub>L</sub> = 50 C <sub>L</sub> =150		21 24	28 31	35 40	42 48	ns	
Maximum Output Enable Time, OC to any Q	t <sub>PZH</sub>	$R_L = 1 k\Omega$	C <sub>L</sub> = 50pF C <sub>L</sub> =150pF		28 31	35 40	42 48		
	t <sub>PZL</sub>	UL— IKW	C <sub>L</sub> = 50pF C <sub>L</sub> =150pF		28 31	35 40	42 48	ns	
Maximum Output Disable Time, OC to any Q	t <sub>PHZ</sub>	$R_L = 1 k\Omega$ $C_L = 50 p$		19 19	25 25	31 31	37 37	ns	
Minimum Pulse Width, CLK High or Low	t <sub>w</sub>	,		9	12	15	18	ns	
Minimum Setup Time, D before CLK1	t <sub>su</sub>			10	13	17	20	ns	
Minimum Hold Time, D after CLK†	th			-3	0	0	0	ns	
Maximum Input Capacitance	CIN			5				pF	
Maximum Output Capacitance	Cout	Output D	isabled	10				pF	
Power Dissipation Capacitance* (per stage)	C <sub>PD</sub>	OC=V <sub>CC</sub> OC=GNI		5 30				pF	

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

#### **FEATURES**

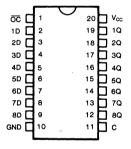
- 8 latches in a single package
- · Full parallel access for loading
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ( $I_{OL} = 24$  mA @  $V_{OL} = 0.5V$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

  KC744107: 4000 https://doi.org/10.000/10.000/10.0000/10.0000/10.0000/10.0000/10.0000/10.0000/10.0000/10.00000/10.00

KS74AHCT: -40°C to + 85°C KS54HACT: -40°C to + 125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATION



#### DESCRIPTION

The '573 consists of 8 high-speed D-type latches coupled to 3-state output buffers with high drive current capability. It can be used in implementing buffer registers, I/O ports, bidirectional bus drivers and working registers.

The latches are transparent: when the enable (C) is high, the Q outputs follow the data (D) inputs. When the enable is low, the outputs latch at the levels that were set up at the D inputs.

The output buffers are controlled by a common signal  $(\overline{OC})$  which places the outputs at a high-impedance state when it is taken high. The  $\overline{OC}$  signal does not affect the internal operations of the latches. Old data can be retained or new data can be entered while outputs are off.

There devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

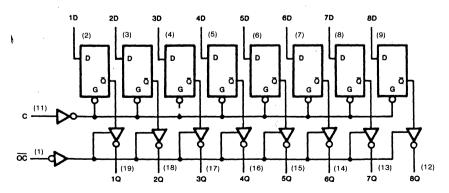
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### **FUNCTION TABLE**

(Each Latch)

	Inputs		Output
OC	Enable C	D	Q
L	Н	Н	Н
L	Н	L	L
L	L	X	$Q_0$
н	X	Х	Z

#### LOGIC DIAGRAM



# Octal D-Type Transparent Latches with 3-State Outputs

# **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 70 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, $P_d{}^{\dagger}$ 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

 Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

# DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T	= 25°C	KS74HCTLS T <sub>a</sub> = -40°C to +85°C	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit
,			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	. VIL			0.8	0.8	0.8	ν
Minimum High-Level Output Voltage	VoH	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_0=-20\mu A$ $I_0=-6mA$	V <sub>CC</sub> 4.2	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> -0.1 3.7	v
Maximum Low-Level Output Voltage	VoL	$V_{IN}$ = $V_{IH}$ or $V_{IL}$ $I_{O}$ =20 $\mu$ A $I_{O}$ =12 $m$ A $I_{O}$ =24 $m$ A	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	lin	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μА
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

# AC ELECTRICAL CHARACTERISTICS (Input tr., tr 46 ns), HCTLS573

Characteristic	Symbol	Con	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74HCTLS T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%	KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	Unit	
				Тур		Guaranteed	i Limits	
Maximum Propagation	tpLH	C <sub>L</sub> = 50 C <sub>L</sub> =150		14 17	18 21	23 28	27 33	
Delay, D to Q	t <sub>PHL</sub>	C <sub>L</sub> = 50 C <sub>L</sub> =150		14 17	18 21	23 28	27 33	ns
Maximum Propagation	tpLH		C=50pF C <sub>L</sub> =150pF		30 33	37 42	45 51	
Delay C to Q	t <sub>PHL</sub>	C <sub>L</sub> = 50pF C <sub>L</sub> =150pF		22 25	30 33	37 42	45 51	ns
Maximum Output Enable	t <sub>PZH</sub>	Rı=1kΩ	C <sub>L</sub> = 50pF C <sub>L</sub> =150pF		32 35		48 54	
Time, OC to any Q	tpzL	11[-1745	C <sub>L</sub> = 50pF C <sub>L</sub> =150pF		32 35	40 45	48 54	ns
Maximum Output Disable Time, OC to any Q	t <sub>PHZ</sub>	R <sub>L</sub> =1kΩ C <sub>L</sub> =50pl	F	19 19	25 25		37 37	ns
Minimum Pulse Width, C High	tw			9	12	15	. 18	ns
Minimum Setup Time, D before C∔	tsu			6	8	10	12	ns
Minimum Hold Time, D after C↓	t <sub>h</sub>			6	10	12	15	ns
Maximum Input Capacitance	CIN			5				pF
Maximum Output Capacitance	Cour	Output D	isabled	10				pF
Power Dissipation Capacitance*	C <sub>PD</sub>	OC=Vcc	(per stage)	5 30				pF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} \ V_{CC}^2 \ f + I_{CC} \ V_{CC}$ .
† For AC switching test circuits and timing waveforms see section 2.

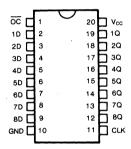
#### **FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current (I<sub>OL</sub> = 24 mA @ V<sub>OL</sub> = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
   KS74HCTLS: -40°C to +85°C

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATION



#### **DESCRIPTION**

The '574 consists of 8 high-speed D-type edge-triggered flip-flops coupled to 3-state output buffers with high drive current capability. It can be used in implementing buffer registers, I/O ports, bidirectional bus drivers and working registers.

The flip-flops are edge-triggered on the positive transition of the clock. The Q outputs are set to the logic levels that were set up at the D inputs.

The output buffers are controlled by a common signal  $(\overline{OC})$  which places the outputs at a high-impedance state when it is taken high. The  $\overline{OC}$  signal does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while outputs are off.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

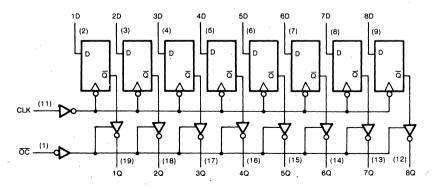
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $\rm V_{CC}$  and ground.

#### **FUNCTION TABLE**

(Each Flip-Flop)

ı	nputs	Output	
OC	CLK	D	Q
L	1	Н	н
L	<b>↑</b>	L	L
L	L	Χ	$\mathbf{Q}_0$
Н	Х	Х	Z

#### LOGIC DIAGRAM



# **Absolute Maximum Ratings\***

Supply Voltage Range V<sub>CC</sub>, ..... -0.5V to +7V

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . . . . . . 4.5V to 5.5V DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . OV to  $V_{CC}$  Operating Temperature

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . . Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

#### DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T <sub>a</sub> = 25°C		KS74HCTLS T <sub>a</sub> = -40°C to +85°C	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-6m A$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=12mA$ $I_{O}=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	l <sub>IN</sub> .	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μА
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin  V <sub>I</sub> =2.4V  other Inputs: at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0µA		2.7	2.9	3.0	mA

# AC ELECTRICAL CHARACTERISTICS (Input tr., tr 46 ns), HCTLS574

Characteristic	Symbol	bol Conditions†		T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74HCTLS  T <sub>a</sub> = -40°C to +85°C  V <sub>CC</sub> = 5.0V ± 10%	KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	Unit	
				Тур		Guaranteed Limits			
Maximum Operating Frequency	f <sub>max</sub>	C <sub>L</sub> = 50	pF	45	35	30	25	MHz	
Maximum Propagation	t <sub>PLH</sub>	C <sub>L</sub> = 50 C <sub>L</sub> =150		21 24	28 31	35 40	42 48		
Delay, CLK to any Q	t <sub>PHL</sub>		C <sub>L</sub> = 50pF C <sub>l</sub> =150pF		28 31		42 48	ns	
Maximum Output Enable Time, OC to any Q	t <sub>PZH</sub>	$R_i = 1 k\Omega$	C <sub>L</sub> = 50pF C <sub>L</sub> =150pF		28 31		42 48		
	t <sub>PZL</sub>	ÜΓ− IKΩ	C <sub>L</sub> = 50pF C <sub>L</sub> =150pF		28 31		42 48	ns	
Maximum Output Disable	t <sub>PHZ</sub>	$R_L = 1 k\Omega$		19	25	31	37		
Time, OC to any Q	tpLZ	C <sub>L</sub> =50p	F	19	25	31	37	ns	
Minimum Pulse Width, CLK High or Low	t <sub>w</sub>			9	12	15	18	ns	
Minimum Setup Time, D before CLKt	t <sub>su</sub>			10	13	17	20	ns	
Minimum Hold Time, D after CLK†	th			-3	0	0	О .	ns	
Maximum Input Capacitance	CIN							pF	
Maximum Output Capacitance	Cour	Output D	isabled	10				pF	
Power Dissipation Capacitance* (per stage)	C <sub>PD</sub>	OC=V <sub>CC</sub> OC=GNI		5 30		,		pF	

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} \ V_{CC}^2 \ f + I_{CC} \ V_{CC}$ .
† For AC switching test circuits and timing waveforms see section 2.

## **FEATURES**

- Choice of 3-State ('590) and Open-Drain ('591) Outputs
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs
- $(I_{OL} = 24 \text{mA} @ V_{OL} = 0.5 \text{V})$  for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

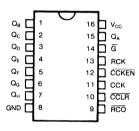
   (274) 271 2 2000 1 2

KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

# PIN CONFIGURATION



#### DESCRIPTION

These devices each consist of an 8-bit counter which feeds an 8-bit register. The counter is incremented on the rising edge of the CCK input, provided that clock enable,  $\overline{\text{CCKEN}}$ , is low. When the counter increments to the all ones condition, ripple carry out,  $\overline{\text{RCO}}$ , will go low. This enables either synchronous cascading of the counters by connecting the  $\overline{\text{RCO}}$  of the first stage to the  $\overline{\text{CCKEN}}$  of the second, or clocking both circuits in parallel. Ripple cascading is accomplished by connecting the  $\overline{\text{RCO}}$  of the first to the CCK of the second stage. A clear input is also provided which will reset the counter to the all zeros state.

The output register is loaded with the contents of the counter on the rising edge of the register clock, RCK. The outputs of this register feed the outputs which are enabled when the enable input, G, is taken low. This enables connection of this part to a system bus. The Q outputs of the '590 are 3-State and those for '591 are Open-drain.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{\text{CC}}$  and ground.

# **FUNCTION TABLE**

INPUTS			FUNCTION					
Ğ	RCK	CCLR	CCKEN	ССК	PONCTION			
н	Х	Х	Х	х	Q Outputs disable			
L	Х	Х	Х	Х	Q Outputs enable			
L		X	Х	х	Counter data is stored into register			
L	7_	X	Х	Х	Register state is not changed			
L	Х	L	Х	Х	Counter clear			
L	Х	Н	L		Advance one count			
L	Х	Н	L	L	No count			
L	Х	Н	Н	Х	No count			

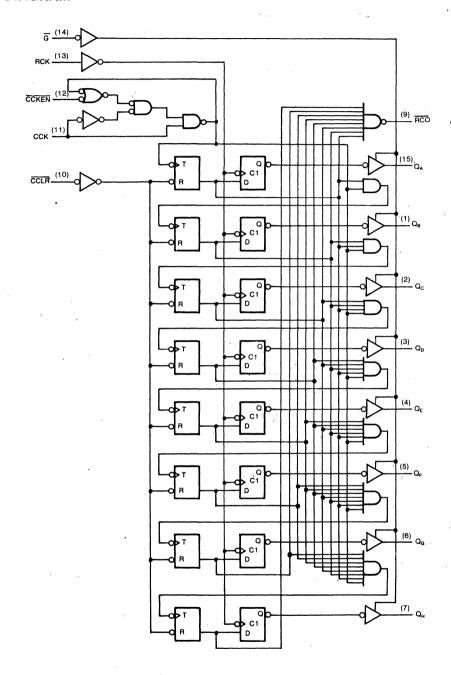
X: Don't care

 $RCO = Q_A' \bullet Q_B' Q_C' \bullet Q_D' Q_E' \bullet Q_F' Q_G' \bullet Q_H'$ 

(QA' ~ QH': Internal outputs of the counter)



# **LOGIC DIAGRAM**



# **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V DC Input Diode Current. lik
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
( $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ ) $\pm 20$ mA
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 70 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, T <sub>stq</sub> 65°C to +150°C
Power Dissipation Per Package, $P_d^{\dagger}$ 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Supply Voltage, V<sub>CC</sub> . . . . . . . . . . . . . . . . . 4.5V to 5.5V DC Input & Output Voltages\*, V<sub>IN</sub>, V<sub>OUT</sub> . . OV to V<sub>CC</sub> Operating Temperature

Range KS74HCTLS:  $-40^{\circ}$ C to  $+85^{\circ}$ C KS54HCTLS:  $-55^{\circ}$ C to  $+125^{\circ}$ C Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns

\* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

## DC ELECTRICAL CHARACTERISTICS (Vcc=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	mbol Test Conditions		a = 25°C	KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	v
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v
Minimum High-Level Output Voltage (All '590 Outputs and '591 RCO Outputs)	V <sub>OH</sub>	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -6\text{mA}$	V <sub>CC</sub> 4.2	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> -0.1 3.84	V <sub>CC</sub> -0.1 3.7	V
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $J_{O}=20\mu A$ $I_{O}=12mA$ $I_{O}=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μА
Maximum Quiescent Supply Current	lcc	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

# AC ELECTRICAL CHARACTERISTICS (Input tr, tre6 ns), HCTLS590

Chara	Characteristic		Conditions†	-	25°C = 5.0V	KS74HCTLS T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%	KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	Unit
•		·		Тур		Guaranteed	Limits	
Maximum Clock	Frequency	f <sub>max</sub>		35	25	20	20	ns
Maximum Propa	agation Delay,	t <sub>PLH</sub>		24	32	40	48	ns
CCK1 to RCO		t <sub>PHL</sub>		24	32	40	48	115
Maximum Propa CCLR↓ to RCO	agation Delay,	tpLH	C <sub>L</sub> =50pF	26	35	44	52	ns
Maximum Propagation Delay, RCK1 to Q		tpLH	,	16	21	26	31	
		t <sub>PHL</sub>	į.	16	21	26	31	ns
Maximum Output Enable Time, G↓ to Q		tpzh	R <sub>L</sub> =1kΩ C <sub>L</sub> =50pF	18	24	30	36	ns
		tpzL		18	24	30	36	
Maximum Output Disable Time.		t <sub>PHZ</sub>		18	24	30	36	
Gf to Q		tpLZ		18	24	30	36	ns
Minimum Pulse Width	CCK or RCK High or Low	t <sub>w</sub>	2	12	16	20	24	ns
	CCLR Low			12	16	20	24	
	CCKEN↓ before CCK↑			12	16	20	24	
Minimum Setup Time	CCLR1 before CCK1	tsu	,	12	16	20	24	ns
	GCK† to RCK†††			24	32	40	48	
Maximum Input	Capacitance	CiN		5				pF
Maximum Outpo	ut Capacitance	Cour	Output Disabled	10				рF
Power Dissipati	on Capacitance*	CPD						pF

<sup>\*</sup> CPD determines the no-load dynamic power dissipation: PD=CPD VCC2 f + ICC VCC.

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

<sup>††</sup> The RCK† to CCK† setup time ensures that the counter will see stable data from the register output.

# AC ELECTRICAL CHARACTERISTICS (Input tr, tr<6 ns), HCTLS591

* Characteristic		Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74HCTLS T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%	KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	Unit
				Тур		Guaranteed	Limits	
Maximum Clock	Frequency	f <sub>max</sub>		35	25	20	20	ns
Maximum Propa	agation Delay,	tpLH		24	32	40.	48	
CCK† to RCO		t <sub>PHL</sub>		24	32	40	48	ns
Maximum Propagation Delay, CCLR↓ to RCO		t <sub>PLH</sub>	C <sub>L</sub> =50pF R <sub>I</sub> =1kΩ	26	35	44	52	ns
Maximum Propagation Delay, RCK† to Q		tpLH	11_10	27	37	46	55	
		t <sub>PHL</sub>	1	16	21	26	31	ns
Maximum Output Enable Time, G↓ to Q		t <sub>PZL</sub>		18	24	30	36	ns
Maximum Output Disable Time, G↑ to Q		t <sub>PLZ</sub>	,	18	24	30	36	ns
Minimum Pulse Duration	CCK or RCK High or Low	t <sub>w</sub>		12	16	20	24	ns
	CCLR Low		-	12	16	20	24	
	CCKEN↓ before CCK1			12	16	20	` 24	
Minimum Setup Time	CCLRt before CCKt	t <sub>su</sub>		12	16	20	24	ns
	CCK† to RCK†††			24	32	40	48	
Maximum Input	Capacitance	CIN		5				рF
Maximum Outpi	ut Capacitance	Cout	Output Disabled					рF
Power Dissipati	on Capacitance*	CPD						pF

<sup>\*</sup> CPD determines the no-load dynamic power dissipation: PD=CPD Vcc² f + Icc Vcc.

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

<sup>††</sup> The clocks may be tied together, in which case the register state will be one clock pulse behind the counter.

Preliminary Specifications

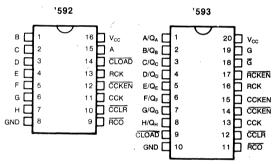
#### **FEATURES**

- Parallel Register Inputs ('592)
- Parallel 3-State I/O: Register Inputs/Counter Outputs ('593)
- Counter Has Direct Overriding Load and Clear
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current
   (IoL = 24 mA @ Vol. = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATIONS



#### DESCRIPTION

The '592 and '593 both contain an 8-bit register which feeds an 8-bit binary counter. The counter is incremented on the rising edge of the CCK input, provided that clock enable,  $\overline{\text{CCKEN}}$ , is low. When the counter increments to the all ones condition, ripple carry out,  $\overline{\text{RCO}}$ , will go low. This enables either synchronous cascading of the counters by connecting the  $\overline{\text{RCO}}$  of the first stage to the  $\overline{\text{CCKEN}}$  of the second, or clocking both circuits in parallel. Ripple cascading is accomplished by connecting the  $\overline{\text{RCO}}$  of the first to the CCK of the second stage. A clear input is also provided which will reset the counter to the all zeros state.

The input register is loaded on the rising edge of the register clock, RCK. The outputs of this register feed the counter. The counter is loaded with the register's contents when the clock load, CLOAD, input is taken low.

The '592 differs from the '593 in that the latter device has bidirectional input/output pins. The 3-state outputs of the counter can be enabled and are active when enable input,  $\overline{G}$ , is taken low and input G is taken high. The outputs of the counter then appear on the register inputs. This enables connection of this part to a system bus. The '593 also has a second clock enable pin,  $\overline{CCKEN}$ , which is active high and it also has an active low register clock enable,  $\overline{RCKEN}$ .

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### **FUNCTION TABLE**

		INPUTS			FUNCTION		
RCK	CLOAD	CCLR	CCKEN	ССК	FUNCTION		
Х	L	н	X	Х	Register data is loaded into counter		
Х	Н	L	X	Х	Counter clear		
	Н	Н	×	х	The data of a thru H inputs is stored into register		
7_	Н.	Н	X	Х	Register state is not changed		
Х	Н	Н	L		Counter advances the count		
Х	Н	Ή	L	ī	No count		
Х	н	Н	Н	. X	No count		

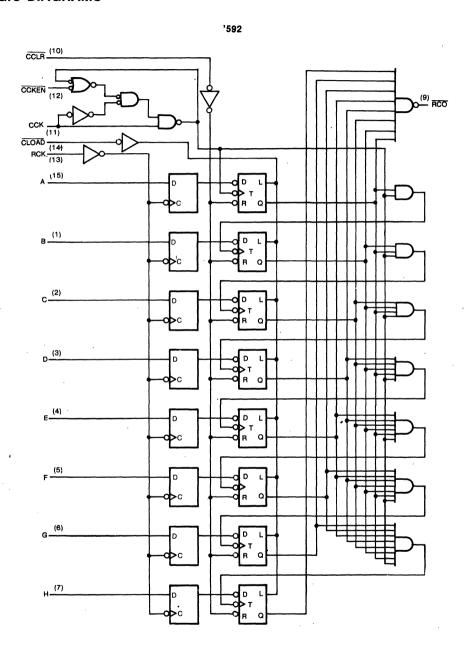
X: Don't care

 $\mathsf{RCO} \ = \ \mathsf{Q}_\mathsf{A}{'} \bullet \ \mathsf{Q}_\mathsf{B}{'} \ \mathsf{Q}_\mathsf{C}{'} \bullet \ \mathsf{Q}_\mathsf{D}{'} \ \mathsf{Q}_\mathsf{E}{'} \bullet \ \mathsf{Q}_\mathsf{F}{'} \ \mathsf{Q}_\mathsf{G}{'} \bullet \ \mathsf{Q}_\mathsf{H}{'}$ 

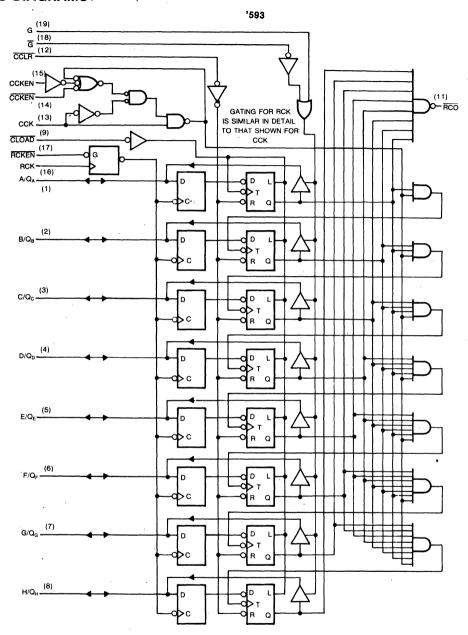
(Q<sub>A</sub>' ∼ Q<sub>H</sub>': Internal outputs of the counter)



# **LOGIC DIAGRAMS**



## LOGIC DIAGRAMS (Continued)



# **Absolute Maximum Ratings\***

Supply Voltage Range $V_{CC}, \ldots, -0.5V$ to $+7V$
DC Input Diode Current, I <sub>IK</sub>
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 70 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, $T_{stg} \dots -65^{\circ}C$ to $+150^{\circ}C$
Power Dissipation Per Package, Pd† 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Supply Voltage, Vo	c		4.5V	to 5	5.5V
DC Input & Output	Voltages*, V <sub>IN</sub> ,	$V_{\text{OUT}}$	0	V to	Vcc
Operating Tempera	ature				
_	LICE ALIOTIC				

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . Max 500 ns

\* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

### DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions		a = 25°C	KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-6mA$	V <sub>CC</sub> 4.2	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	l <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA	,	2.7	2.9	3.0	mA

# AC ELECTRICAL CHARACTERISTICS (Input tr, tre2 ns), HCTLS592

Characteristic		Symbol	Conditions†	_	25°C - 5.0V	KS74HCTLS $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 5.0V \pm 10\%$	KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	Unit
	•,			Тур		Guaranteed	Limits	
Maximum Clock Frequency		f <sub>max</sub>		35	25	20	20	MHz
Maximum Propagation Delay,		tpLH		24	32	40	48	
CCKt to RCO		t <sub>PHL</sub>		24	. 32	40	48	ns
Maximum Prope	agation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pF	24	32	40	48	~
CLOAD↓ to RC	5 ,	t <sub>PHL</sub>		24	32	40	48	ns
Maximum Propagation Delay, CCLR↓ to RCO		t <sub>PHL</sub>		24	32	40	48	ns
Maximum Propagation Delay, RCK1 to RCO		tpLH	C <sub>L</sub> =50pF	26	35	44	52	
		t <sub>PHL</sub>	CLOAD=GND	26	35	44	52	ns
Minimum Pulse CCK or RCK			12	16	20	24		
Width	CCLR Low	t <sub>w</sub>	1	12	16	20	24	ns
·	CLOAD Low			12	16	20	24	
	CCKEN↓ before			12	16	20	24	
Minimum Setup Time	CCLRt before CCKt	t <sub>su</sub>		12	16	20	24	ns
	RCK1 before CCK111		•	24	32	. 40 . ,	48	
	Data A-H1 before			12	16	20	24	
Minimum Hold	lime -	th		-3	0	0	0	ns
Maximum Input	Capacitance	CIN		5				pF
Power Dissipati	on Capacitance*	CPD						рF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

<sup>††</sup> The RCK† to CCK† setup time ensures that the counter will see stable data from the register output.

# AC ELECTRICAL CHARACTERISTICS (Input tr, tr <6 ns), HCTLS593

Cha	Characteristic Symbol		Con	ditions†	_	25°C = 5.0V	KS74HCTLS $T_{a} = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm .10\%$	KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	Unit
					Тур		Guaranteed	Limits	
Maximum Cl	ock Frequency	f <sub>max</sub>			35	25	20	20 .	MHZ
· ·		tplH	C <sub>L</sub> =50p		24	32	40	48	
Maximum Pr	opagation Delay,		C <sub>L</sub> =150		27	35	45	. 54	ns
CCKI IO Q		tpHL	C <sub>L</sub> =50p		24 27	32	40	48	
		-	C <sub>L</sub> =150	pr		35	45	54	<del> </del>
CCK† to RC	opagation Delay,	tPLH	C <sub>L</sub> =50p	F	24	32	40	48	ns
CONTRO TIO		tpHL	0 50-		24	32	40	48	-
Maximum Pr	opagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pl C <sub>L</sub> =150		24 27	32	40 45	48 54	
	CLOADI to Q				24	32	40	48	ns
		t <sub>PHL</sub>		C <sub>L</sub> =50pF C <sub>L</sub> =150pF		35	45	54	
Maximum Pr	opagation Delay,	tpLH			24	32	40	48	†
CLOAD↓ to		t <sub>PHL</sub>	C <sub>L</sub> =50pl	F	24	32	40	48	ns
Maximum Pr	opagation Delay,	tpLH	C <sub>L</sub> =50pl		26	35	44	52	ļ ——
RCKf to RC		tpHL	CLOAD=		26	35	44	52	ns
Maximum Pr	opagation Delay,		C =50p5			1			
CCLR↓ to Q		tPHL	C <sub>L</sub> =50pl		24 27	32	40	48	ns
	opagation Delay,	t <sub>PLH</sub>	$C_L=150pF$ $C_L=50pF$		24	32	45	48	ns
OOLITY TO TH				C <sub>1</sub> = 50pF	21	28	39	42	1
Maximum Enable Time,	tpzL	D 41.0	C <sub>L</sub> =150pF	24	31	44	48	ns	
Gt or Gี↓ to	Q		$R_L=1k\Omega$	C <sub>1</sub> = 50pF	21	28	35	42	t l
		tpzL		C <sub>L</sub> =150pF	24	31	44	48	ns
Maximum Di	sable Time	tpLH	$R_L = 1k\Omega$	24	28	35	42	ns	
G  ↓ or G1 to	Q	tPLZ	C <sub>L</sub> =50pl	F	21	28	35	42	IIS
Minimum	CCK or RCK High or Low				12	16	20	24	ns
Pulse Width	CCLR Low	tw			12	16	20	24	
	CLOAD Low				12	16	20	24	
	CCKEN↓ before CCKt				12	16	20	24	
Minimum	RCKEN↓ to RCK1					12	16	24	
Setup Time	CCLR↓ before CCKt	t <sub>su</sub>			12	16	20	24	ns
	RCK† before CCK†††				24	32	40	48	
	Data A-H before RCK1				12	16	20	24	
Hold Time		t <sub>h</sub>			-3	0	0	0	ns
Maximum Inp	out Capacitance	CIN			5				рF
Maximum Ou	tput Capacitance	Cout	Output Di	isabled	10	10			рF
Power Dissipa	ition Capacitance*	CPD							рF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

<sup>††</sup> The RCK† to CCK† setup time ensures that the counter will see stable data from the register output.



<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

#### **FEATURES**

- 8-Bit Serial-In, Parallel-Out Shift Registers With Storage
- Choice of 3-State ('595) or Open-Drain ('596) Parallel Outputs
- Shift Register Has Direct Clear
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current
   (IoL = 24 mA @ Vol = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### DESCRIPTION

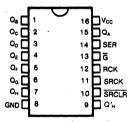
These devices each contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state ('595) or opendrain ('596) outputs. Separate clocks are provided for both the shift register and the storage register. The shift register has a direct-overriding clear, serial input, and serial output pins for cascading.

Both the shift register and storage register clocks are positive-edge triggered. If the user wishes to connect both clocks together, the shift register state will always be one clock pulse ahead of the storage register.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### PIN CONFIGURATION



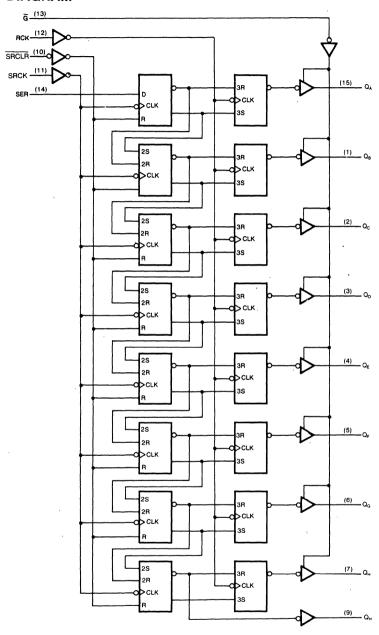
#### **FUNCTION TABLE**

		INPUTS			FUNCTION			
SER	SRCK	SRCLR	RCK	Ğ	FONCTION			
×	Х	Х	Х	Н	Q <sub>A</sub> thru Q <sub>H</sub> outputs disable			
X	X	×	<b>x</b> ,	L	Q <sub>A</sub> thru Q <sub>H</sub> outputs enable			
Х	Х	L	X	X	Shift register is cleared.			
L	1	Н	х	х	First stage of S.R. becomes "L". Other stages store the data of previous stage, respectively.			
Н		Н	х	×	First stage of S.R. becomes "H". Other stages store the data of previous stage, respectively.			
X	7_	Н	Х	Х	State of S.R. is not changed.			
X	Х	Х		Х	S.R. data is stored into storage register.			
X	Х	Χ.	L	Х	Storage register state is not changed.			

X: DON'T CARE



## LOGIC DIAGRAM



# **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V DC Input Diode Current, I <sub>IK</sub>
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 70 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, $P_d^{\dagger}$ 500 mW

<sup>\*</sup> Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

Input Rise & Fall Times,  $t_{r}$ ,  $t_{f}$  . . . . . . . . Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

## DC ELECTRICAL CHARACTERISTICS (VCC=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T <sub>a</sub> = 25°C		KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	V V V ν μΑ
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v
Minimum High-Level Output Voltage (All '595 Outputs and '596 Q' <sub>H</sub> Output)	V <sub>ОН</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-6mA$	V <sub>CC</sub> 4.2	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> = 0.1 3.84	V <sub>CC</sub> -0.1 3.7	V
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=12mA$ $I_{O}=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Output Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μА
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>1</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA



# AC ELECTRICAL CHARACTERISTICS (Input tr., tre6 ns), HCTLS595, HCTLS596

Characteristic		Symbol	Con	ditions†	T <sub>a</sub> = 1	25°C = 5.0V	KS74HCTLS T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%	KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	Unit
					Тур		Guaranteed	Limits	
Maximum Pi		tpLH	C <sub>L</sub> =50pl	F	15	18	25	30	ns
Delay, SHC	Delay, SRCKt to Q'H				15	18	25	30	<u> </u>
Maximum Pi	ronagation	t <sub>PLH</sub>	C <sub>L</sub> =50pl		17 20	22 25	28 33	33 39	
Delay, RCK† to Q <sub>A</sub> thru Q <sub>H</sub>		tpHL	C <sub>L</sub> =50pl	F	17	22	28	33	ns
		4711	C <sub>L</sub> =150		20	25	33	39	Ļ
Maximum Output Enable Time, GI to Q <sub>A</sub> thru Q <sub>H</sub> ('595 only)		tpzH		C <sub>L</sub> =50pF C <sub>L</sub> =150pF	18 21	24	30 35	36 42	
		tezu	R <sub>L</sub> =1kΩ	C <sub>L</sub> =50pF	18	24	30	36	ns
				C <sub>L</sub> =150pF	21	27	35	42	
Maximum Output Disable Time, Gt to Q <sub>A</sub> thru Q <sub>H</sub> ('595 only)		t <sub>PHZ</sub>	$R_L = 1 k\Omega$ $C_L = 50 pF$		18 21	24 27	30 35	36 42	ns
		t <sub>PLZ</sub>			18 21	24 27	30 35	36 42	
Maximum Propagation			C <sub>L</sub> =50pl	F	18	24	30	36	
Delay, Gf to ('596 only)	Q <sub>A</sub> thru Q <sub>H</sub>	t <sub>PLH</sub>	C <sub>L</sub> =150	pF	21	27	35	. 42	ns
Maximum Pi		t <sub>PHL</sub>	C <sub>L</sub> =50pl	F ,	18	24	` 30	36	ns
('596 only)	Q <sub>A</sub> thru Q <sub>H</sub>	TPHL	C <sub>L</sub> =150pF		21	27	35	42	ns
Minimum	SRCK or RCK	t <sub>w</sub>			12	16	20	24	
Pulse Width	SRCLR Low				12	16	20	24	ns
Minimum	SRCLRt to SRCKt				12	16	20	. 24	
Setup Time	SER to SRCK1	t <sub>su</sub>			12	16	20	24	ns
SRCK† to					24	32	40	48	
Minimum H	lold Time	t <sub>h</sub>			-3	0	0	0	ns
Maximum In	put Capacitance	C <sub>IN</sub>			5				pF
Maximum O Capacitai	•	Cout	Output D	isabled	10				pF
Power Diss Capacitai		C <sub>PD</sub>		h and the second					pF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

<sup>††</sup> This setup time ensures the register will see stable data from the register output.

#### **FEATURES**

- 8-Bit Parallel Storage Register Inputs
- shift Register has Direct Overiding Load and Clear
- . Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Prive-Current outputs:
- IOL = 8 mA @ VOL = 0.5V
- · Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

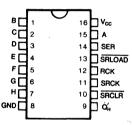
#### DESCRIPTION

The '597 consists of an 8-bit storage latch feeding a parallel-in, serial-out 8-bit shift register. Both the storage register and the shift register have positive-edge triggered clocks. The shift register also has direct load (from storage) and clear inputs.

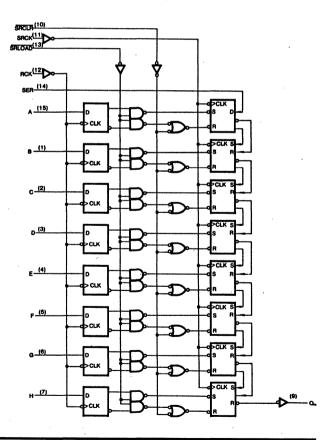
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to VCC and ground.

#### PIN CONFIGURATION



#### LOGIC DIAGRAM



# KS54HCTLS 597

# 8-Bit Shift-Registers with Input Latches

#### **FUNCTION TABLE**

		INPUTS			FUNCTION
SER	SRCK	SRCLR	SRLOAD	RCK .	FONCTION
Х	Х	L	Н	Х	S.R. is cleared to "L"
×	X	Н	J	Х	Input register data is stored into S.R.
L	J.	н	Н	x	First stage of S.R. becomes "L". Other stages store the data of previous stage, respectively.
н	1	н	н	x	First stage of S.R. becomes "H". Other stages stores the data of previous stage, respectively.
Х	х	х	Х		State of S.R. is not changed.
Х	х	х	Х	5	Input data on A∿H line is stored into input register
Х	х	Х	х	7	Storage register state is not changed.

# **Absolute Maximum Ratings\***

•
Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ m/s}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* About 44 to Day

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

### **Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . . . . . . . . . . . . 4.5V to 5.5V DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . OV to  $V_{CC}$  Operating Temperature

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . Max 500 ns

\* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	bol Test Conditions		<sub>a</sub> = 25°C	KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit
			Тур	Guaranteed Limits			
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	lin	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> ≂V <sub>CC</sub> or GND J <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	ΔΙ <sub>CC</sub>	per input pin  V <sub>1</sub> =2.4V  other Inputs:  at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0µA		2.7	2.9	3.0	mA



# AC ELECTRICAL CHARACTERISTICS (Input tr, tr 46 ns), HCTLS597

Ch	aracteristic	Symbol	Conditions†	-	25°C = 5.0V	$KS74HCTLS$ $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$	KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> =5.0V ± 10%	Unit
	•			Тур		Guaranteed	Limits	
Maximum Clo	ock Frequency	f <sub>max</sub>		35	25	20	20	MHz
Maximum Pro	opagation Delay,	tpLH		15	18	25	30	
SRCK† to Q'	н	t <sub>PHL</sub>		15	18	25	30	ns
Maximum, Pro	opagation Delay,	t <sub>PLH</sub>	$C_L = 50pF$	18	24	30	36	
SRLOAD↓ to	Q' <sub>H</sub>	t <sub>PHL</sub>		18	24	30	36	ns
Maximum Propagation Delay, SRCLR√ to Q'H		t <sub>PHL</sub>		17	22	28	33	ns
Maximum Propagation Delay, RCK1 to Q'H		tpLH	C <sub>L</sub> =50pF SLOAD=Low	21	29	35	42	ns
		t <sub>PHL</sub>		21	29	35	42	
Minimum	RCK or SRCK High or Low			12	16	20	24	
Pulse Width	SRCLR or SRLOAD Low	t <sub>w</sub>		12	16	20	24	ns
	SRCLR† before			12	16	20	24	
Minimum Setup Time	RCK1 before	t <sub>su</sub>		24	32	40	48	ns
*	SER before SRCK1		•	12	16	20	24	
	A thru H before RCK1			12	16	20	24	
Minimum Hold Time		th		-3	0	0	0	ns
Maximum Inp	out Capacitance	CIN		5				pF
Power Dissip	ation Capacitance*	CPD						pF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .



<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

<sup>††</sup> The RCK† before SRCK† setup time ensures that shift register will see stable data comming from the register output.

Octal Bus Transceivers

# FEATURES

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ( $I_{OL}=24$  mA @  $V_{OL}=0.5V$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
   KS74HCTLS: -40°C to +85°C

KS74HC1LS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include plastic."small outline" packages, standard plastic and ceramic 300-mil DIPs

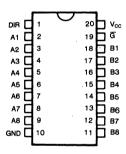
#### DESCRIPTION

These high-speed octal/bus transceivers are designed for asynchronous two-way communication between data buses. A direction control input (DIR) controls the flow direction of data. When DIR is high, data flows from the A inputs to the B outputs. When DIR is low, data flows from B to A. The '643 transfers inverted data from the A bus to the B bus and non-inverted data from the B bus to the A bus. The '640 transfers inverted data in both directions.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

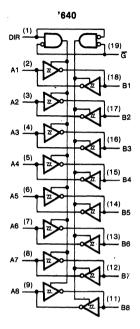
#### PIN CONFIGURATION

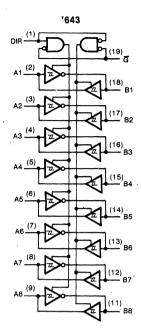


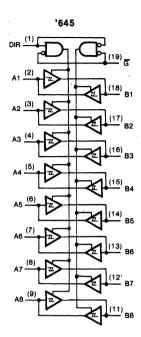
#### **FUNCTION TABLE**

,	ntrol puts	Operation						
G	DIR	'640	'643	'645				
L	L	Inverted data transmitted from Bus B to Bus A	Data transmitted from Bus B to Bus A	Data transmitted from Bus B to Bus A				
Ļ	Н	Inverted data transmitted from Bus A to Bus B	Inverted data transmitted from Bus A to Bus B	Data transmitted from Bus A to Bus B				
н	x	Buses isolated (High-impedance state)	Buses isolated (High-impedance state)	Buses isolated (High-impedance state)				

### LOGIC DIAGRAMS







# **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 70 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Supply Voltage, V<sub>CC</sub> . . . . . . . . . . . . 4.5V to 5.5V DC Input & Output Voltages\*, V<sub>IN</sub>, V<sub>OUT</sub> . . OV to V<sub>CC</sub> Operating Temperature

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C Input Rise & Fall Times,  $t_r, t_f$  ..................... Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

# DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T <sub>a</sub> = 25°C		KS74HCTLS T <sub>a</sub> = -40°C to +85°C	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	Voн	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-6m A$	V <sub>CC</sub> 4.2	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> =0.1 3.84	V <sub>CC</sub> = 0.1 3.7	v
Maximum Low-Level Output Voltage	VoL	$V_{IN}$ = $V_{IH}$ or $V_{IL}$ $I_{O}$ = $20\mu$ A $I_{O}$ = $12m$ A $I_{O}$ = $24m$ A	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	IIN	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μА
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =O <sub>µ</sub> A		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

# AC ELECTRICAL CHARACTERISTICS (Input tr., tres ns), HCTLS640, HCTLS643, HCTLS645

Characteristic	Symbol	Condition	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0°		KS74HCTLS  T <sub>a</sub> = -40°C to +85°C  V <sub>CC</sub> = 5.0V ± 10%	KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	Unit		
				Тур	Typ Guaranteed Limits				
Maximum Propagation	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF C <sub>L</sub> =50pF C <sub>L</sub> =150pF		9 12	12 15	16 21	19 25	ns	
Delay, A to B, or B to A	t <sub>PHL</sub>			9 12	12 15	16 21	19 25	IIS	
Maximum Output Enable	t <sub>PZH</sub>	R <sub>L</sub> =1kΩ	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	30 33	40 43	50 55	60 65	ns	
Time, G or DIR to A or B	tpzL		C <sub>L</sub> =50pF C <sub>L</sub> =150pF	30 33	40 43	50 55	60 65		
Maximum Output Disable	t <sub>PHZ</sub>	$R_L = 1 k\Omega$		.20	27	34	40		
Time, G or DIR to A or B	tPLZ	C <sub>L</sub> =50pF		20	27	34	40	ns	
Maximum Input Capacitance	CIN			5		1		pF	
Maximum Output Capacitance	Cout	Output di	sabled	10				pF	
Power Dissipation Capacitance* (per stage)	C <sub>PD</sub>	Ğ=V <sub>CC</sub> Ğ=GND	,	5 30			•	pF	

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

# Octal 3-State Bus Transceivers with Registers

#### **FEATURES**

- . 8 bi-directional data paths
- · Transmits direct or stored data in either direction
- 24-pin 0.3" slim DIP package
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current
   (I<sub>OL</sub> = 24 mA @ V<sub>OL</sub> = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to + 85°C KS54HACT: -55°C to + 125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATION

CAB	1	24	D V <sub>CC</sub>
SAB	2	23	CBA
DIR	3	22	SBA
A1 🗆	4	21	ΒĒ
A2 🗖	5 .	20	<b>В</b> 1
A3	6	19	B2
A4 🗖	7 .	18	_ вз
A5 🗖	8	17	B4 □
A6 🗖	9	16	B5
A7 🗆	10	15	<b>⊒</b> B6
A8 🗖	11	14	B7
GND 🗖	12	13	<b>□</b> B8
			•

#### DESCRIPTION

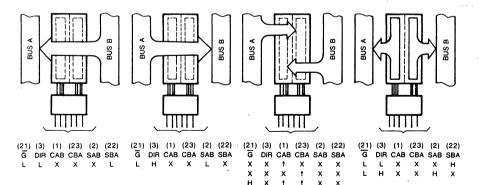
The '646 and '648 are bi-directional bus transceivers with D-type flip-flops and control circuitry to facilitate high speed multiplexed data transmission. The '646 transmits true data and the '648 transmits inverted data.

Data can be transmitted directly from one port to the other in either direction. It also can be stored in the flip-flops from either or both ports for subsequent transmission to the opposite port. Six control inputs govern the data flow:

- G (output enable) when high, all outputs are disabled, isolating the A and B ports. When low, one port is enabled at a time as determined by the DIR pin.
- DIR (direction control) disables A or B outputs permitting the pins to be used as inputs thus determining the direction of a data flow. When DIR=high, data flows from A to B.
- SAB,SBA (data source AB and BA) determines whether data transmitted is from the data inputs or the registers associated with those inputs.
- CAB,CBA (Clock AB and BA) clocks data from the A inputs and the B inputs, respectively, into their associated registers. Since the clocks are not gated with the  $\overline{G}$  and DIR pins, data at the A and B pins can be clocked into the flip-flops at any time.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{\text{CC}}$  and ground.



Real-Time transfer bus B to bus A

Real-Time transfer bus A to bus B

Storage from A AND/OR B

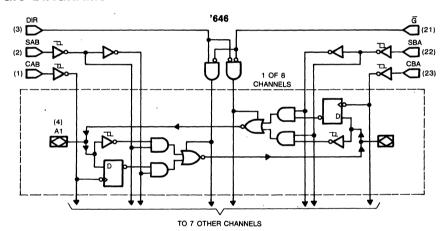
Transfer stored data to A AND/OR B

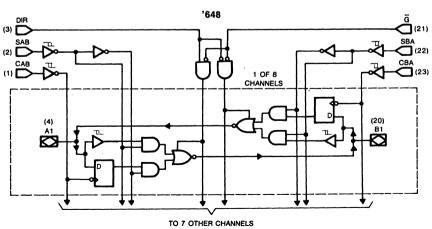
## **FUNCTION TABLE**

Inputs						Data	1/0*	Operation or Function			
Ğ	DIR	CAB	CBA	SAB	SBA	A1 thru A8	B1 thru B8	'646	'648		
Х	Х	<b>↑</b>	. X	Х	Х	input	input	Store A, B unspecified	Store A, B unspecified		
Χ	Χ	X	<b>↑</b>	Х	Χ	Not specified	Not specified	Store B, A unspecified	Store B, A unspecified		
Н	Х	1	<b>↑</b>	Х	Х	Innut	lanut	Store A and B data	Store A and B data		
Н	Χ	H or L	H or L	Х	Χ	Input	Input	Isolation, hold storage	isolation, hold storage		
L	L	Х	Х	·X	L	Output	lam.ut	Real-Time B data to A bus	Real-Time B data to A bus		
L	L	Х	H or L	Χ	Н	Output	Input	Stored B data to A bus	Stored B data to A bus		
L	Н	Х	Х	L	Х	I	0	Real-Time A data to B bus	Real-Time A data to B bus		
L	Н	H or L	X	Н	X	Input	Output	Stored A data to B bus	Stored Ā data to B bus		

<sup>\*</sup>The data output functions may be enabled or disabled by various signals at the  $\overline{G}$  and DIR inputs. Data input functions are always enabled, ie., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

## **LOGIC DIAGRAMS**





# **Absolute Maximum Ratings\***

Supply Voltage Range $V_{CC}$ , $-0.5V$ to $+7V$
DC Input Diode Current, I <sub>IK</sub>
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 70 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Ratings are those values beyond

which permanent damage to the device may occur.

These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

# **Recommended Operating Conditions**

Supply Voltage, V <sub>CC</sub>	4.5V to 5.5V
DC Input & Output Voltages*, VIN, VOUT	OV to Vcc
Operating Temperature	•

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

D :

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T <sub>a</sub> = 25°C		KS74HCTLS $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	V <sub>IH</sub>	3		2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-6mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA	,	2.7	2.9	3.0	mA



<sup>†</sup> Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# AC ELECTRICAL CHARACTERISTICS (Input tr. tie6 ns), HCTLS646. HCTLS648.

Characteristic	Symbol	Condition	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V Typ			KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	Unit	
					Guarantee	d Limits		
Maximum Clock Frequency	f <sub>max</sub>	C <sub>L</sub> =50pF		40	30	25	- 20	MHz
Maximum Propagation	t <sub>PHL</sub>	C <sub>L</sub> =50pl C <sub>L</sub> =150pl	14 17	19 22	24 29	29 35	ns	
Delay, A or B Input to B or A Output	t <sub>PHL</sub>	C <sub>L</sub> =50pl C <sub>L</sub> =150pl		14 17	19 22	24 29	29 35	
Maximum Propagation	tpLH	C <sub>L</sub> =50pF C <sub>L</sub> =150p		22 25	30 33	37 42	45 51	ne
Delay, CBA or CAB Input to A or B Output	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150p		22 25		37 42	45 51	ns
Maximum Propagation Delay,†† SBA or SAB input	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF C <sub>L</sub> =50pF C <sub>L</sub> =150pF		26 29	35 38	44 49	53 59	ns
to A or B Output (with A or B High)	t <sub>PHL</sub>			26 29	35 38	44 49	53 59	
Maximum Propagation Delay, SBA or SAB Input	t <sub>PLH</sub>	$C_L=50pF$ $C_L=150pF$		26 29	35 38	44 49	53 59	ns
to A or B Output (with A orB Low)	t <sub>PHL</sub>	C <sub>L</sub> =50pf C <sub>L</sub> =150p	26 29	35 38	44 49	53 59		
Maximum Output Enable	t <sub>PZL</sub>	R <sub>L</sub> =1kΩ	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	33 36	45 48	56 61	67 73	ns
Time, G or DIR Input to A or B Output			C <sub>L</sub> =50pF C <sub>L</sub> =150pF	33 36	45 48	56 61	67 73	
Maximum Output Disable Time, G or DIR Input to	t <sub>PHZ</sub>	$R_L = 1 k\Omega$	_	26	35	44	53	ns
A or B Output	tplZ	C <sub>L</sub> =50pf		26	35	44	53	
Pulse Duration, Clocks High or Low	t <sub>w</sub>			10	13	17	20	ns
Setup Time, A before CAB1 or B before CBA1	t <sub>su</sub>			10	13	17	20	ns
Hold Time, A after CAB† or B after CBA†	t <sub>h</sub>			-3	0		0	ns
Maximum Input Capacitance	CiN	,	5				pF	
Maximum Output Capacitance	Соит	Output Di	10				рF	
Power Dissipation Capacitance*	C <sub>PD</sub>							рF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

<sup>††</sup> These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

Preliminary Specifications

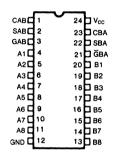
#### **FEATURES**

- Independent Registers and Enables for A and B Buses
- Multiplexed Real-Time and Stored Data
- . Choice of Time and Inverting Data Paths
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current (I<sub>OL</sub> = 24 mA @ V<sub>OL</sub> = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
   KS74HCTLS: -40°C to +85°C

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATION



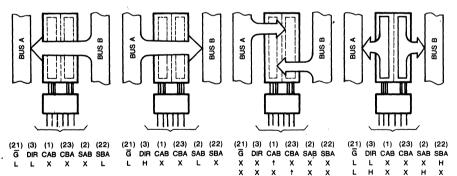
#### DESCRIPTION

These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Enable GAB and GBA are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether real-time or stored data is transferred. A low input level selects real-time data, and a high selects stored data. The following examples demonstrate the four fundamental busmanagement functions that can be performed with the octal bus transceivers and registers.

Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and GBA. In this configuration each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.



Real-Time transfer bus B to bus A

Real-Time transfer bus A to bus B

Storage from A AND/OR B

Transfer stored data to A and/or B

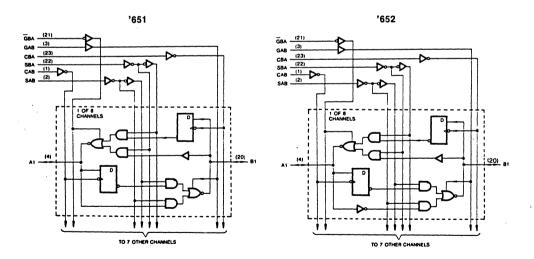
SAMSUNG SEMICONDUCTOR

#### **FUNCTION TABLE**

INPUTS						DATA	1/0*	OPERATION OR FUNCTION		
GAB	ĞΒΑ	CAB	СВА	SAB	SBA	A1 THRU A8	B1 THRU B8	'651	'652	
L L	Н	H or L	H or L	X	X X	Input	Input	Isolation Store A and B Data	Isolation Store A and B Data	
X	H H	† †	H or L	X**	X	Input Input	Not specified Output*	Store A, Hold B Store A in both registers	Store A Hold B Store A in both registers	
L L	X L	H or L ↑	† †	X X	X X**	Not specified Output*	Input Input	Hold A, Store B Store B in both registers	Hold A, Store B Store B in both registers	
L L	L	X X	X H or L	X X	L H	Output	Input	Real-Time $\bar{B}$ Data to A Bus Stored $\bar{B}$ Data to A Bus	Real-Time B Data to a Bus Stored B Data to A Bus	
H	H	X H or L	X	H	X	Input -	Output	Real-Time Ā Data to B Bus Stored Ā Data to Bus	Real-Time A Data to B Bus Stored A Data to B Bus	
н	L	H or L	H or L	н	н	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus	Stored A Data to B Bus and Stored B Data to A Bus	

<sup>•</sup> The data output functions may be enabled or disabled by various signals at the GAB and GBA inputs. Data input functions are always enabled, ie., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

# LOGIC DIAGRAMS



<sup>\*\*</sup> Select control=L: clocks can occur simultaneously
Select control=H: clocks must be staggered in order to load both registers

# Octal 3-State Bus Transceivers with Registers

# **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> , −0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, I <sub>OK</sub>
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + 0.5V$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, $T_{stg} \dots -65$ °C to $+150$ °C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW

<sup>\*</sup> Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Supply Voltage, V <sub>CC</sub>	4.5V to 5.5V
DC Input & Output Voltages*, VIN, VOUT	OV to Vcc
Operating Temperature	

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . Max 500 ns

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T <sub>a</sub> = 25°C		KS74HCTLS $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit	
			Тур		Guaranteed Limits			
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	٧	
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	>	
Minimum High-Level Output Voltage	V <sub>ОН</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-6mA$	V <sub>CC</sub> 4.2	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	٧	
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=12mA$ $I_{O}=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	<b>v</b>	
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ	
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μΑ	
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ	
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA	



 <sup>\*</sup> Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

## AC ELECTRICAL CHARACTERISTICS (Input tr. tre6 ns), HCTLS651, HCTLS652

Characteristic	Symbol			T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74HCTLS T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> =5.0V±10%	KS54HCTLS  T <sub>a</sub> = -55°C to +125°C  V <sub>CC</sub> = 5.0V ± 10%	Unit
				Тур		Guaranteed Limits		
Maximum Clock Frequency	f <sub>max</sub>			40	30	25	20	MHz
Maximum Propagation Delay, A or B Input to	tpLH	C <sub>L</sub> =50pl C <sub>L</sub> =150		14 17	19 22	24 29	29 35	
B or A Ouput	tpHL	C <sub>L</sub> =50pF C <sub>L</sub> =150pF		14 17	19 22	21 26	20 26	ns
Maximum Propagation Delay, CBA or CAB Input to	t <sub>PLH</sub>	C <sub>L</sub> =50pl C <sub>L</sub> =150		22 25	30 33	37 42	45 51	
A or B Output	t <sub>PHL</sub>	C <sub>L</sub> =50pl C <sub>L</sub> =150		22 25	30 33	37 <b>42</b>	45 51	ns
Maximum Propagation Delay, SBA or SAB Input to	t <sub>PLH</sub>	C <sub>L</sub> =50pl C <sub>L</sub> =150		26 29	35 38	44 49	53 59	
A or B Output (with A or B High)	t <sub>PHL</sub>	C <sub>L</sub> =50pl C <sub>L</sub> =150	26 29	35 38	44 49	53 59	ns	
Maximum Propagation Delay, SBA or SAB Input to	t <sub>PLH</sub>	C <sub>L</sub> =50pl C <sub>L</sub> =150		26 29	35 38	44 49	53 59	
A or B Output (with A or B Low)	t <sub>PHL</sub>	C <sub>L</sub> =50pl C <sub>L</sub> =150	26 29	35 38	44 49	53 59	ns	
Maximum Output Enable Time, GBA to A or	t <sub>PZL</sub>	$R_L = 1 k\Omega$	$C_L = 50pF$ $C_L = 150pF$	33 39	45 48	56 61	67 73	ns
GAB to B	t <sub>PZH</sub>		C <sub>L</sub> =50pF C <sub>L</sub> =150pF	33 39	45 48	56 61	67 73	
Maximum Output Disable Time, GBA to A or GAB to	t <sub>PHZ</sub>	$R_L = 1 k\Omega$		26	35	44	53	ns
В	tpLZ	C <sub>L</sub> =50pF		26	35	44	53	
Minimum Pulse Width Clocks High or Low	tw			10 <sup>-</sup>	13	17	20	ns
Minimum Setup Time, A before CAB† or B before CBA†	t <sub>su</sub>			10	13	17	20	ns
Minimum Hold Time, A after CAB† or B after CBA†	th			-3	0	0	0	ns
Maximum Input Capacitance	CIN			5				pF
Maximum Output Capacitance	Cout	Output D	isabled		10			pF
Power Dissipation Capacitance*	C <sub>PD</sub>		•					pF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

Preliminary Specifications

### **FEATURES**

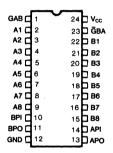
- Bus Transceivers with Inverting Outputs ('658) or True Outputs ('659)
- Generates a Parity Bit for A Bus and B Bus
- Easily Cascadable
- Internal Active Pull-Ups and Pull-Downs
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current
   (IoL = 24 mA @ Vol. = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATION



#### DESCRIPTION

These octal bus transceivers are designed for asynchronous, bidirectional communication between data buses. The devices transmit data from the A Bus to the B Bus, or from the B Bus to the A Bus, depending on the levels at the direction control inputs, GAB and  $\overline{G}BA$ . These devices also generate parity outputs, APO and BPO, which reflect the number of high levels at the A Bus and B Bus, respectively, taking into account the parity inputs API and BPI.

The bidirectional I/O ports feature active circuits on the input stage that, when the output shared by that pin is disabled, will maintain the input in the last state taken by the output. This state will be maintained until changed by activity on the bus. The advantage of this arrangement is that when all outputs on the bus are disabled, the inputs will be prevented from floating, resulting in minimum power dissipation and minimum susceptibility to noise. This eliminates any need for external pull-up or pull-down resistors. The parity inputs API and BPI have similar circuits.

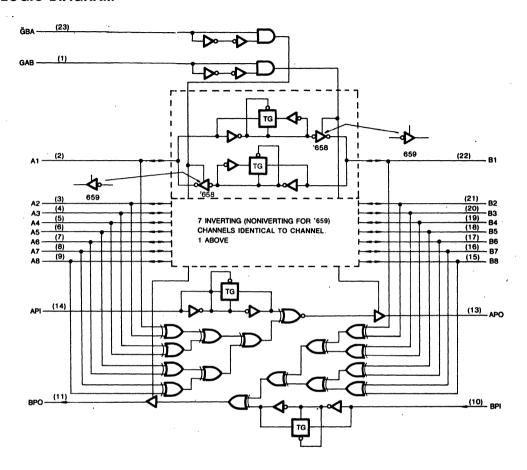
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### **FUNCTION TABLE**

1	TROL UTS	NUMBER OF HIGH INPUTS ON	NUMBER OF HIGH INPUTS ON	OUT	PUTS	OPERATION		
ĞBA	GAB	A BUS AND API	B BUS AND BPI	APO	BPO	HCTLS658	HCTLS659	
	L	X	0, 2, 4, 6, 8	Z	Н	B Data to A Bus	B Data to A Bus	
_		X	1, 3, 5, 7, 9	Z	L	D Data to A Bus	B bata to A bus	
н	н	0, 2, 4, 6, 8	X	Н	Z	A Data to B Bus	A Data to B Bus	
	''	1, 3, 5, 7, 9	X	L	Z	A Data to B bus	A Data to B Bus	
Н	L	X	X	Z	Z	Isolation	Isolation	
		х	0, 2, 4, 6, 8		Н	,		
L	н	Х	1, 3, 5, 7, 9		L	B Data to A Bus,	B Data to A Bus,	
	''	0, 2, 4, 6, 8	X	Н		A Data to B Bus	A Data to B Bus	
		1, 3, 5, 7, 9	X	L			* *	

#### LOGIC DIAGRAM



#### Absolute Maximum Ratings\* Supply Voltage Range Vcc. -0.5V to +7V

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Supply Voltage, V<sub>CC</sub> . . . . . . . . . 4.5V to 5.5V DC Input & Output Voltages\*, VIN, VOUT ... OV to VCC Operating Temperature

Range

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

Input Rise & Fall Times, tr, tf . . . . . . . . Max 500 ns

\* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

Characteristic	Symbol	Symbol Test Conditions		a = 25°C	KS74HCTLS T <sub>a</sub> = -40°C to +85°C	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	
,			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	V <sub>IL</sub>	4		0.8	0.8	0.8	v
Minimum High-Level Output Voltage	Voh	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-6m A$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	٧
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=12mA$ $I_{O}=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	l <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	· ±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	, Icc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	ΔΙσο	per input pin V <sub>i</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA



## AC ELECTRICAL CHARACTERISTICS (Input tr., tr<6 ns), HCTLS658, HCTLS659

Characteristic	Symbol Conditions†		T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74HCTLS Ta = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%	KS54HCTLS  T <sub>a</sub> = -55°C to +125°C  V <sub>CC</sub> = 5.0V ± 10%	Unit	
				Тур		Guaranteed	Limits	
Maximum Propagation	tpLH	C <sub>L</sub> =50pF C <sub>L</sub> =150p		20 23	25 28	30 35	39 45	
Delay, A or B to B or A	t <sub>PHL</sub>	C <sub>L</sub> =50pf C <sub>L</sub> =150p		20 23	25 28	30 35	39 45	ns
Maximum Propagation	t <sub>PLH</sub>	(	C <sub>L</sub> =50pF C <sub>I</sub> =150pF		32 35	40 45	48 54	ns
Delay, A or B to B or A	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF		24 27	32 35	40 45	48 54	
Maximum Propagation	tpLH	C <sub>L</sub> =50pF C <sub>L</sub> =150pF		20 23	. 25 28	30 35	39 45	ns
Delay A or B to APO or BPO	tpHL	C <sub>L</sub> =50pF C <sub>L</sub> =150pF		20 23	25 28	30 35	39 45	
Maximum Enable Time,	tрzн	R <sub>L</sub> =1kΩ	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	20 23	25 28	30 35	39 45	ns
GAB or GBA to APO or BPO	tpzL		C <sub>L</sub> =50pF C <sub>L</sub> =150pF	20 23	25 28	30 35	39 45	
Maximum Disable Time, GAB or GBA to	tpLZ	R <sub>L</sub> =1kΩ		20	25	30	39	ns
APO or BPO	t <sub>PHZ</sub>	C <sub>L</sub> =50pl	=	20	25	30	39	ns
Maximum Input Capacitance	CIN			5				рF
Maximum Output Capacitance	C <sub>OUT</sub>				,		,	pF
Power Dissipation Capacitance*	C <sub>PD</sub>		,					pF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

Preliminary Specifications

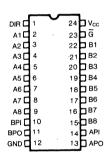
#### **FEATURES**

- Bus Transceivers with Inverting Outputs ('664) or True Outputs ('665)
- Generates a Parity Bit for A Bus and B Bus
- Easily Cascadable
- Internal Active Pull-Ups and Pull-Downs
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current
   (I<sub>OL</sub> = 24 mA @ V<sub>OL</sub> = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
   KS74HCTLS: -40°C to +85°C

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATION



#### DESCRIPTION

These octal bus transceivers are designed for asynchronous, bidirectional communication between data buses. The devices transmit data from the A Bus to the B Bus or from the B Bus to the A Bus, depending on the level at the direction control input, DIR. The enable input,  $\overline{G}$  can be used to disable the device so that the buses are isolated. These devices will also generate parity outputs, APO and BPO, which reflect the number of high levels at the A Bus and B Bus, respectively, taking into account the parity inputs API and BPI.

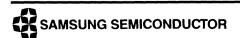
The bidirectional I/O ports feature active circuitry on the input stage that, when the output shared by that pin is disabled, will maintain the input in the last state taken by the output. This state will be maintained until changed by the activity on the bus. The advantage of this arrangement is tht when all outputs on the bus are disabled, the inputs will be prevented from floating, resulting in minimum power dissipation and minimum susceptibility to noise. This eliminates any need for external pull-up or pull-down resistors. The parity inputs API and BPI have similar circuitry.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

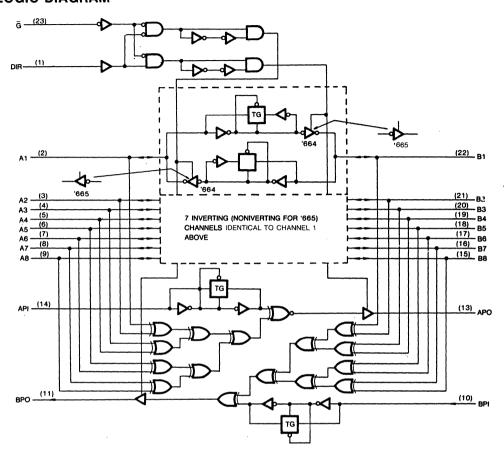
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### **FUNCTION TABLE**

	NTROL PUTS	NUMBER OF HIGH INPUTS ON	NUMBER OF HIGH INPUTS ON	OUT	PUTS	OPERATION		
G	DIR	A BUS AND API	B BUS AND BPI	APO	вро	'664	'665	
		X	0, 2, 4, 6, 8	Z	Н	B Data to A Bus	B Data to A Bus	
-	_	. X	1, 3, 5, 7, 9	Z	L	B Data to A Das		
	Н	0, 2, 4, 6, 8	X	н	Z	Ā Data to B Bus	A Data to B Bus	
	L	1, 3, 5, 7, 9	X	L	Z	A Data to B Dus	A Data to B Bus	
Н	Х	X	X	Z	Z	Isolation	Isolation	



## LOGIC DIAGRAM



## **Absolute Maximum Ratings\***

Supply Voltage Range $V_{CC}$ , $-0.5V$ to $+7V$
DC Input Diode Current, I <sub>IK</sub>
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 70 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, $T_{stg}\ldots -65^{\circ}\text{C}$ to $+150^{\circ}\text{C}$
Power Dissipation Per Package, $P_d{}^{\dagger}$ 500 mW
* Absolute Maximum Ratings are those values beyond

Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . . . . . . . 4.5V to 5.5V DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . OV to  $V_{CC}$  Operating Temperature

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

Input Rise & Fall Times,  $t_r,\,t_f$  . . . . . . . Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

Characteristic	Symbol	Test Conditions	T,	<sub>a</sub> = 25°C	KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Limits		
Minimum High-Level Input Voltage	- V <sub>IH</sub>			2.0	2.0	2.0	v
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	Voh	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-6mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> -0.1	٧
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=12mA$ $I_{O}=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	٧
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-Staté Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =UμA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin  V <sub>I</sub> =2.4V  other Inputs: at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0µA		2.7	2.9	3.0	mA

## AC ELECTRICAL CHARACTERISTICS (Input tr., tr46 ns), HCTLS664/655

Characteristic	Symbol	conditions†			25°C = 5.0V	KS74HCTLS  T <sub>a</sub> = -40°C to +85°C  V <sub>CC</sub> = 5.0V ± 10%	KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	Unit	
				Тур		Guaranteed	Limits		
Maximum Propagation	tpLH	C <sub>L</sub> =50pl C <sub>L</sub> =150pl		20 23	25 28	30 35	39 <b>45</b>	ns	
Delay, A or B to B or A	t <sub>PHL</sub>	C <sub>L</sub> =50pl C <sub>L</sub> =150pl		20 23	25 28	30 35	38 <b>36</b>		
Maximum Propagation	tpLH	C <sub>L</sub> =50pl C <sub>L</sub> =150		24 27	32 35	40 45	48 54	ns	
Delay, A or B to APO or BPO	tpHL	C <sub>L</sub> =50pl C <sub>L</sub> =150		24 27	32 35	40 45	48 54	lis	
Maximum Propagation	tpLH		C <sub>L</sub> =50pF C <sub>L</sub> =150pF		25 28	30 35	39 <b>45</b>		
Delay, API or BPI to APO or BPO	t <sub>PHL</sub>	C <sub>L</sub> =50pl		20 23	25 28	30 35	39 <b>45</b>	ns	
Maximum Output Enable	t <sub>PZL</sub>	R <sub>i</sub> = 1kΩ	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	24 27	32 35	40 45	48 <b>54</b>	ns	
Time, G to A or B		חני– ואמ	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	24 27	32 35	40 45	48 <b>54</b>	113	
Maximum Output Delay	tpHZ	$R_L = 1 k\Omega$		24	32	40	48		
Time, G to A or B	tpLZ	C <sub>L</sub> =50pl	F	24	22	40	50	ns	
Maximum Output Enable	tpzh	R <sub>i</sub> = 1kΩ	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	24 27	32 35	40 45	48 <b>54</b>	ns	
Time DIR to A or B	t <sub>PZH</sub>	11_114	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	24 27	32 35	40 45	48 54	118	
Maximum Output Disable Time, DIR to A or B	t <sub>PHZ</sub>	$R_L = 1 k\Omega$ $C_1 = 50 pl$	F	20 24	32	40 40	48 48	ns	
Maximum Input Capacitance		- C		5	32	40	40	pF	
Maximum Output Capacitance	Cout	Output D	isabled	10				pF	
Power Dissipation Capacitance*	C <sub>PD</sub>					And the second s		pF	

<sup>\*</sup> CPD determines the no-load dynamic power dissipation: PD=CPD VCC2 f + ICC VCC.

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

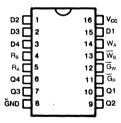
#### **FEATURES**

- Separaté Read/Write
   Addressing Permits Simultaneous Reading and
  Writing
- . Expandable to 512 Words of N-bits
- · For use as:
  - Scratch pad memory
  - Buffer storage between processors
  - Bit storage in fast multiplication designs
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:

I<sub>OL</sub> = 8 mA @ V<sub>OL</sub> = 0.5V

- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
   KS74HCTLS: -40°C to +85°C
   KS54HCTLS: -55°C to +125°C
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATION



#### **FUNCTION TABLES**

#### WRITE MODE SELECT TABLE

OPERATING	INPL	JTS	INTERNAL	
MODE	Ğw	Dn	LATCHES(a)	
Write Data	L. L	L H	L H	
Data Latched	н	х	no change	

#### NOTE:

a. The Write Address (W<sub>A</sub> and W<sub>B</sub>) to the "Internal latches" must be stable while  $\bar{G}_W$  is LOW for conventional operation.

#### DESCRIPTION

The '670 is a 16-bit 3-State Register File organized as 4 words of 4 bits each. Separate Read and Write Address and Enable Inputs are available, permitting simultaneous writing into one word location and reading from another location. The 4-bit word to be stored is presented to four Data inputs. The Write Address inputs ( $W_A$  and  $W_B$ ) determine the location of the stored word. When the write enable ( $\overline{G}_W$ ) input is LOW, the data is entered into the addressed location. The addressed location remains transparent to the data while the  $\overline{G}_W$  is LOW. Data supplied at the inputs will be read out in true (non-inverting) form from the 3-State outputs. Data and Write Address inputs are inhibited when  $\overline{G}_W$  is HIGH.

Direct acquisition of data stored in any of the four registers is made possible by individual Read Address inputs ( $\overline{R}_A$  and  $R_B$ ). The addressed word appears at the four outputs when the read enable ( $\overline{G}_R$ ) is LOW. Data outputs are in the HIGH impedance "off" state when the read enable input is HIGH. This permits outputs to be tied together to increase the word capacity to very large numbers.

Up to 128 devices can be stacked to increase the word size to 512 locations by tying the 3-State outputs together. Since the limiting factor for expansion is the output HIGH current, further stacking is possible by tying pull-up resistors to the outputs to increase the I<sub>OH</sub> current available. Design of the read enable signals for the stacked devices must ensure that there is no overlap in the LOW levels which would cause more than one output to be active at the same time. Parallel expansion to generate n-bit words is accomplished by driving the Enable and Address inputs of each device in parallel.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{\text{CC}}$  and ground.

#### **READ MODE SELECT TABLE**

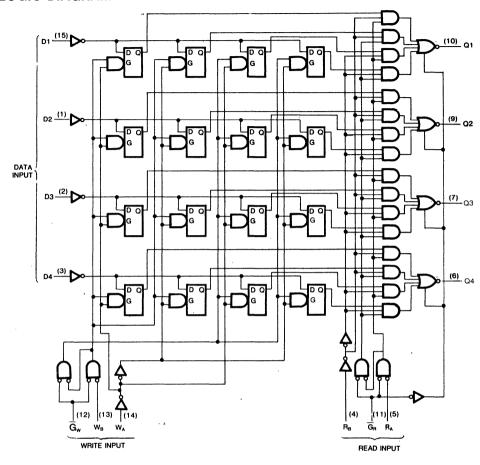
OPERATING	ı	NPUTS	OUTPUT Q <sub>n</sub>	
MODE	ĞR	INTERNAL LATCHES(b)		
Read	L	L H	L H	
Disabled	Н	Н	(Z)	

#### NOTE:

b. The selection of the "internal latches" by Read Address  $(\overline{R}_A$  and  $R_B)$  are not constrained by  $\overline{G}_W$  or  $\overline{G}_R$  operation.



#### **LOGIC DIAGRAM**



# **Absolute Maximum Ratings\***

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V)$ $\pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 70 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability. † Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

KS54HCTLS: -55°C to +125°C

Input Rise & Fall Times,  $t_{r},\; t_{f}\; \ldots \ldots$  Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

Characteristic	Symbol	Test Conditions	T <sub>a</sub> = 25°C		KS74HCTLS • KS54HCTLS T <sub>a</sub> = -40°C to +85°C T <sub>a</sub> = -55°C to +125°				
		•	Тур		Guaranteed Limits				
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	v		
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	0.8	v		
Minimum High-Level Output Voltage	VoH	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-6mA$	V <sub>CC</sub> 4.2	V <sub>CC</sub> −0.1 3.98	V <sub>CC</sub> -0.1 3.84	y <sub>cc</sub> −0.1 3.7	v		
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v		
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ		
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μΑ		
Maximum Quiescent Supply Current	lcc	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μΑ		
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		. 2.7	2.9	3.0	mA		



## AC ELECTRICAL CHARACTERISTICS (Input tr., tr<6 ns), HCTLS670

Characteristic	Symbol	cymbol Conditions†			25°C : 5.0V	KS74HCTLS T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%	KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> =5.0V ± 10%	Unit	
				Тур		Guaranteed Limits			
Maximum Propagation Delay,	telH	C <sub>L</sub> =50pl C <sub>L</sub> =150		20 23	32 35	40 45	48 54	ns	
R <sub>A</sub> or R <sub>B</sub> to Output	t <sub>PHL</sub>	C <sub>L</sub> =50pl C <sub>L</sub> =150		20 23	32 35	40 45	48 54	113	
Maximum Propagation Delay, Gw to Output	tpLH	C <sub>L</sub> =50pl C <sub>L</sub> =150		27 30	36 39	45 50	59 65	ns	
	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF		27 30	36 39	45 50	59 65	,,,5	
Maximum Propagation Delay.	tpLH	C <sub>L</sub> =50pl C <sub>L</sub> =150		27 30	36 39	45 50	59 65	ns	
Data to Output	t <sub>PHL</sub>	C <sub>L</sub> =50pl C <sub>L</sub> =150		27 30	36 39	45 50	<b>54</b> 60		
Maximum Output Enable	tрzн	Rı=1kΩ	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	24 27	32 35	40 45	48 54	ns	
Time, G <sub>R</sub> to Output	tpzL		C <sub>L</sub> =50pF C <sub>L</sub> =150pF	24 27	32 35	40 45	48 54		
Maximum Output Disable	t <sub>PHZ</sub>	R <sub>L</sub> =1kΩ		24	32	40	48	ns	
Time, GR to Output	tpLZ	C <sub>L</sub> =150	pF	24	32	40	48	113	
Maximum Input Capacitance	CiN			5				рF	
Maximum Output Capacitance	Cour	Output d	isabled	10				pF	
Power Dissipation Capacitance*	C <sub>PD</sub>							pF	

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

#### Preliminary Specifications

#### **FEATURES**

- '679: 12-bit to 4-bit comparator with enable
- · '680: 12-bit to 4-bit comparator with latch
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
- (I<sub>OL</sub> = 24 mA @ V<sub>OL</sub> = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges;
   KS74HCTLS: - 40°C to +85°C
- KS54HCTLS: -55°C to +125°C
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### DESCRIPTION

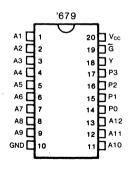
The '679 and '680 address comparators simplify addressing of memory boards and/or other peripheral devices. The four P inputs are normally hard wired with a preprogrammed address. An internal decoder determines what input information applied to the 12 A inputs must be low or high to cause a low state at the output (Y). For example, a positive-logic bit combination of 0111 (decimal 7) at the P input determines that inputs A1 through A7 must be low and that inputs A8 through A12 must be high to cause the output to go low. Equality of the address applied at the A inputs to the preprogrammed address is indicated by the output being low.

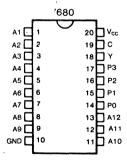
The '679 features an enable input  $(\overline{G})$ . When  $\overline{G}$  is low, the device is enabled. When  $\overline{G}$  is high, the device is disabled and the output is high regardless of the A and P inputs. The '680 features a transparent latch and a latch enable input (C). When C is high, the device is in the transparent mode. When C is low, the previous logical state of Y is latched.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

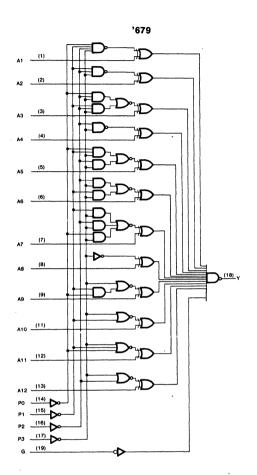
#### PIN CONFIGURATIONS

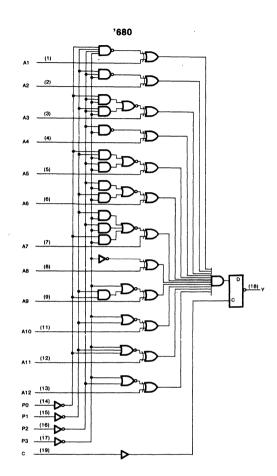






## **LOGIC DIAGRAMS**





### **FUNCTION TABLE**

'679	'680					INI	PUTS	CON	MON	I TO	'679	AND	'680					OUTPUT
Ğ	C	Р3	P2	P1	P0	A1	A2	А3	A4	<b>A</b> 5	A6	A7	A8	A9	A10	A11	A12	Y
L	Н	L	L	' L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L
L	н	L	L	L	Н	L	Н	Н	Н	Н	H.	Н	Н	Н	Н	Н	Н	L
L	Н	. L	L	Н	L	L	L	Н	·H	Н	Н	н	Н	Н	н	н	Н	L
L	Н	L	L	Н	Н	L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	L
L	Н	L	Н	L	L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	L
L	н	L	Н	L	Н	L	L	L	٠L	L	Н	Н	Н	Н	Н	н	Н	L
L	Н	L	Н	Н	L	L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н	L
L	Н	L	Н	Н	Н	L.	L	Ļ	L	L	L	L	Н	Н	Н	Н	Н	L
L	н	Н	L.	L	L	L	L	L	L	L	L	L	L	Н	Н	. н	Н	L
L	. н	Н	L	L	Н	L	L	L	L	L	L	L	L	L	Н	Н	Н	L
L	Н	Н	L	Н	. <b>L</b>	L	L	L	L	L	L	L	L	L	L	Н	Н	L
L	Н	Н	L	Н	Н	L	L	L	L	L	L	L	L	L	L	L	Н	L
L	Н	Н	Н	L	L	L	L	L	L	L	L	L	L	Н	Н	Н	L	L*
L	Н	Н	Н	L	Н	L	L	L	L	L	L	L	L	L	Н	н	L .	L*
L	н	Н	Н	Н	L	L	L	L	L	L	L	L	L	L	L	Н	L	L*
L	Н	Н	Н	Н	Н	L	L	L	. L	L	L	L	L	L	L	L	L	L
L	Н							All o	ther o	comb	natio	ns						Н
Н							,	'679	: Any	com	binati	on		,				н
	L							'680	: Any	com	binati	on						Latched

<sup>\*</sup> These three rows of the function table show combinations that would normally not be used in address comparator applications. The logic symbols above are not valid for all combinations in which P=12, 13 and 14. If symbols valid for all combinations are required, starting with the fourth Exclusive-OR from the bottom, change P≥9 to P=9 ... 11/13 ... 15, P≥10 to P=10/11/14/15, and P≥11 to P=11/15.

## Absolute Maximum Ratings\*

Supply Voltage Range V <sub>CC</sub> ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 70 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW
<ul> <li>Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.</li> <li>These are stress ratings only and functional operation</li> </ul>

of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

t	Power Dissipation temperature derating:
	Plastic Package (N): -12mW/°C from 65°C to 85°C
	Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

	5.5V
DC Input & Output Voltages*, VIN, VOUT OV to	Vcc
Operating Temperature	
Range KS74HCTLS: -40°C to +8	5°C

KS54HCTLS: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . Max 500 ns

 Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T,	= 25°C	KS74HCTLS T <sub>a</sub> = -40°C to +85°C	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit		
			Тур	Guaranteed Limits					
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	٧		
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v		
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-6mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	v		
Maximum Low-Level Output Voltage	l .	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v		
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ		
Maximum Quiescent Supply Current	CC	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ		
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA		

## AC ELECTRICAL CHARACTERISTICS (Input tr, tre6 ns), HCTLS679

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74HCTLS  T <sub>a</sub> = -40°C to +85°C  V <sub>CC</sub> = 5.0V ± 10%	KS54HCTLS $T_a = -55^{\circ}\text{C to } + 125^{\circ}\text{C}$ $V_{CC} = 5.0V \pm 10\%$	Unit
			Тур		Guaranteed	Limits	
Maximum Propagation Delay, Any P to Y	tpLH	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	24 27	32 35	40 <b>4</b> 5	48 54	ns
	tpHL	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	27 30	32 35	40 45	48 54	113
Maximum Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	21 24	28 31	35 <b>40</b>	42 48	ns
Any A to Y	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	21 24	28 31	35 40	42 48	113
Maximum Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	18 21	24 27	30 35	36 42	ns
G to Y	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	18 21	24 27	30 35	36 <b>4</b> 2	113
Maximum Input Capacitance	CIN		·5			V	pF
Power Dissipation Capacitance*	C <sub>PD</sub>						pF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

## AC ELECTRICAL CHARACTERISTICS (Input tr. tre6 ns), HCTLS680

Characteristic	Symbol	Conditions <sup>†</sup>	-	25°C 5.0V	KS74HCTLS $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	Unit
,			Тур		Guaranteed	Limits	
Maximum Propagation Delay, Any P to Y	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	27 30	36 39	45 50	54 60	ns
	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	27 30	32 35	40 45	48 64	113
Maximum Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	24 27	32 35	40 45	48 64	ns
Any A to Y	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	24 27	32 35	40 45	48 64	110
Maximum Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	19 22	26 29	32 37	38 44	ns
C to Y	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	19 22	26 29	32 37	32 38	
Maximum Input Capacitance	CIN		5				pF
Power Dissipation Capacitance*	C <sub>PD</sub>						pF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} \ V_{CC}^2 \ f + I_{CC} \ V_{CC}$ .
† For AC switching test circuits and timing waveforms see section 2.

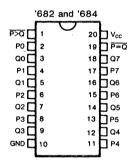
## **FEATURES**

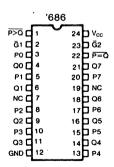
- . Compares Two 8-Bit Words
- '682 has  $20k\Omega$  pull-up Resistors on the Q Inputs
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High drive current outputs:
  - ( $I_{OL} = 24 \text{ mA}$  @  $V_{OL} = 0.5 \text{V}$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

## PIN CONFIGURATIONS





NC-No internal connection

#### DESCRIPTION

These magnitude comparators perform comparisons of two eight-bit binary or BCD words. All types provide  $\overline{P=Q}$  and  $\overline{P>Q}$  outputs. The '682 features 20-k $\Omega$  pull-up termination resistors on the Q inputs for analog or switch data.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### **FUNCTION TABLE**

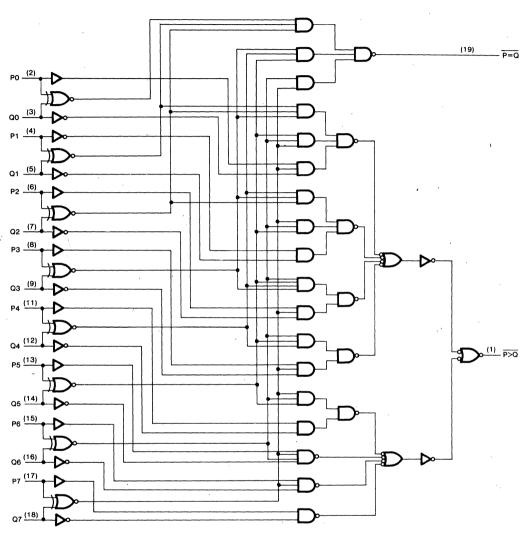
	1	NPUTS	}	OUTE	DITE
	DATA	ENA	BLES	0011	-013
	P, Q	Ğ1	Ğ2	P=Q	P>Q
į	P≔Q	L	X	L	Н
į	P>Q	Х	L	н	L
	P <q< td=""><td>Х</td><td>Х</td><td>Н</td><td>н</td></q<>	Х	Х	Н	н
	P≈Q	H	Х	Н	Н
	P>Q	Х	н	н	Н
	Х	Н	Н	н	Н

NOTES: 1. The last 3 lines of the function table apply only to the device having enable inputs, i.e., '686.

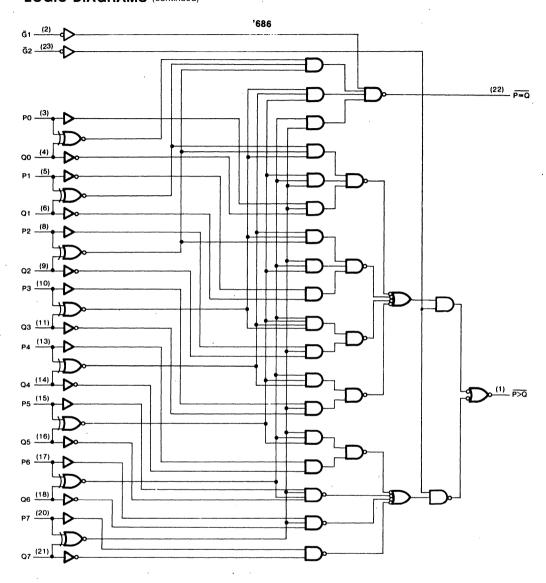
The P≺Q function can be generated by applying the P=Q and P>Q outputs to a 2-input NAND gate.

# LOGIC DIAGRAMS

'682 or '684



## LOGIC DIAGRAMS (continued)



## **Absolute Maximum Ratings\***

Supply Voltage Range $V_{CC}, \ldots -0.5V$ to $+7V$
DC Input Diode Current, I <sub>IK</sub>
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V)$ $\pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±35 mA
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, $T_{stg}\ldots -65^{\circ}\text{C}$ to $+150^{\circ}\text{C}$
Power Dissipation Per Package, $P_d{}^\dagger$ 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation

of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

## **Recommended Operating Conditions**

Supply Voltage, V <sub>CC</sub>	4.5V to 5.5V
DC Input & Output Voltages*, VIN, VOUT	OV to Vcc
Operating Temperature	•

Range KS74HCTLS: −40°C to +85°C KS54HCTLS: −55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . Max 500 ns

Parameter	Symbol	Test Conditions	Т	<sub>A</sub> = 25°C	KS74AHCT T <sub>A</sub> = -40°C to +85°C	54AHCT T <sub>A</sub> = -55°C to +125°C	Unit
		,	Тур		Guaranteed Limit		
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v
Minimum High-Level Output Voltage (Totem-pole Outputs)	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-6mA$	V <sub>CC</sub> 4.2	V <sub>CC</sub> -0.1 3.93	V <sub>CC</sub> -0.1 3.84	V <sub>CC</sub> -0.1	V
Maximum Low-Level Output Voltage (All Outputs)	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current, ('682 Q Inputs)		V <sub>CC</sub> =Max V <sub>IN</sub> =2.7V V <sub>IN</sub> =0.4V		-0.2 -0.4	-0.2 -0.4	-0.2 -0.4	mA
Maximum Input Current (All other Inputs)	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent	Icc	For '682: V <sub>IN</sub> =GND (Q0-Q7) V <sub>IN</sub> =V <sub>CC</sub> or GND (all other inputs)		3.5	3.5	3.5	.mA
Supply Current		For '684 and '688 V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0µA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	ΔΙσο	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

<sup>†</sup> Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

<sup>\*</sup> Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

## AC ELECTRICAL CHARACTERISTICS (Input tr., tre6 ns), HCTLS682, HCTLS684, HCTLS686

Characteristic	Symbol	nbol Conditions†		25°C :5.0V	KS74HCTLS T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%	KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> =5.0V ± 10%	Unit
			Тур		Guaranteed	Limits	
Maximum Propagation Delay, P or Q to P=Q	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	18 21	25 28	31 36	38 44	ns
	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	18 21	25 28	31 36	38 44	113
Maximum Propagation Delay, P or Q to P>Q	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	22 25	32 35	38 43	45 51	ns
	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	22 25	30 33	38 43	45 51	110
Maximum Propagation Delay, G1 to P=Q ('686 Only)	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	15 18	20 23	25 30	30 36	ns
	t <sub>PHL</sub>	C <sub>1</sub> =50pF C <sub>L</sub> =150pF	15 18	20 23	25 30	30 36	
Maximum Propagation Delay, G2 to P <q ('686="" only)<="" td=""><td>tpLH</td><td>C=50pF C<sub>L</sub>=150pF</td><td>18 21</td><td>25 28</td><td>31 36</td><td>38 44</td><td>ns</td></q>	tpLH	C=50pF C <sub>L</sub> =150pF	18 21	25 28	31 36	38 44	ns
	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	18 21	25 28	31 36	38 44	,,,,
Maximum Input Capacitance	CIN		5				рF
Power Dissipation Capacitance*	C <sub>PD</sub>						рF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} \ V_{CC}^2 \ f + I_{CC} \ V_{CC}$ .
† For AC switching test circuits and timing waveforms see section 2.

KS54HCTLS 682/684/686 KS74HCTLS

#### **FEATURES**

- Compares Two 8-Bit Words
- Choice of Totem-pole ('688) and open-drain ('689) outputs ('688 is identical to '521)
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High drive current outputs:
- (I<sub>OL</sub> = 24 mA @ V<sub>OL</sub> = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

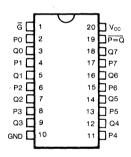
## **DESCRIPTION**

These identity comparators perform comparisons of two 8-bit binary or BCD words. The output of '688 is totempole while '689's are open-drain.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

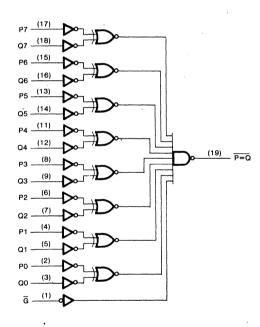
#### PIN CONFIGURATION



#### **FUNCTION TABLE**

INF	UTS	ОПТРИТ
DATA P.Q	ENABLE G	P=Q
P=Q	L	Ĺ
P>Q	L	Н
P <q< td=""><td>L</td><td>Н</td></q<>	L	Н
X	. н	Н

#### LOGIC DIAGRAM (Positive Logic)



## **Absolute Maximum Ratings\***

Supply Voltage Range $V_{CC}$ , $-0.5V$ to $+7V$
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V)$ $\pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±70 mA
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd <sup>†</sup> 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

# **Recommended Operating Conditions**

Supply Voltage, V <sub>CC</sub>	. 4.5V to 5.5V
DC Input & Output Voltages*, VIN, VOUT	OV to V <sub>CC</sub>
Operating Temperature	

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . . . Max 500 ns

 Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

Characteristic	Characteristic Symbol Test Conditions		Т,	<sub>a</sub> = 25°C	KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL		-	0.8	0.8	0.8	v
Minimum High-Level Output Voltage ('688 only)	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-6mA$	V <sub>CC</sub> 4.2	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	lin	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μА
Maximum 3-State Leakage Current ('689 only)	loz	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> =V <sub>CC</sub>		±0.5	±5.0	±10.0	μА
Maximum Quiescent Supply Current	lcc	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μА
Additional Worst Case Supply Current	Δlcc	per input pin $V_{l}{=}2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}{=}0\mu A$		.2.7	2.9	3.0 .	mA

# AC ELECTRICAL CHARACTERISTICS (input tr, tre6 ns), HCTLS688

Characteristic	Symbol	bol Conditions†		25°C = 5.0V	KS74HCTLS T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%	KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> =5.0V± 10%	Unit
			Тур		Guaranteed	Limits	
Maximum Propagation Delay, P to P=Q	tpLH	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	16 19	22 25	28 33	33 <b>39</b>	ns
	tene	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	16 19	22 25	28 33	33 39	113
Maximum Propagation Delay, Q to P=Q	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	16 19	22 25	28 33	33 39	ns
	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	16 19	22 25	28 33	33 39 ·	113
Maximum Propagation Delay, G to P=Q	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	15 18	20 23	25 30	30 36	ns
	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	15 18	20 23	25 30	30 36	,,,,
Maximum Input Capacitance	Cin		5				pF
Power Dissipation Capacitance*	CPD		\				pF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

## AC ELECTRICAL CHARACTERISTICS (Input tr, tr 6 ns), HCTLS689

Characteristic	Symbol	Conditions <sup>†</sup>	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74HCTLS T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%	KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> =5.0V ± 10%	Unit
			Limits				
Maximum Propagation Delay,	tpLH	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	24 27	31 34	37 - 42	43 49	ns
	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	19 22	26 29	32 37	38 44	113
Maximum Propagation Delay, Q to P=Q	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	24 27	31 34	37 42	43 49	ns
	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	19 22	26 29	32 37	38 44	113
Maximum Propagation Delay, G to P=Q	tpLH	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	23 27	29 32	35 40	41 47	ns
	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	18 21	24 27	30 35	36 42	113
Maximum Input Capacitance	CIN		5				pF
Power Dissipation Capacitance*	C <sub>PD</sub>					,	pF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

## **Preliminary Specifications**

#### **FEATURES**

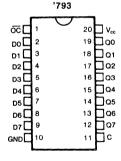
- I/O port configuration enables output data back onto input bus
- . Latch ('793) and and Register ('794) options
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current
   (loL = 24 mA @ VoL = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

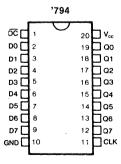
KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

## PIN CONFIGURATIONS





#### DESCRIPTION

These are 8-bit latches/registers that allow temporary storage and retrieval of data on a bus. This operation is important in control algorithms which make decisions based on the previous status of output controls. Rather than storing a redundant copy of the output data in memory, simply reading the register as an I/O port allows the data to be retrieved from where it has been stored in a '793 or '794, for verification and/or updating.

The data is loaded in the registers on the positive-edge of the clock (CLK) for the '794. The data is passed through the '793 when C is high, and it is latched when C goes low The output control ( $\overline{OC}$ ) is used to enable data on the D0-D7 pins. when  $\overline{OC}$  is low the output of the latches/registers is enabled on D0-D7, enabling D as an output bus so that the host can perform a read operation. When  $\overline{OC}$  is high, D0-D7 are inputs to the latches/registers configuring D as an input bus.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{\text{CC}}$  and ground.

#### **FUNCTION TABLES**

793

С	ос	Q	D
L	L	Q <sub>0</sub> ** Q <sub>0</sub> **	Output, Q
L	Н	Qo**	Input
H†	L	D*	Output, Q*
H	Н	D	· Input

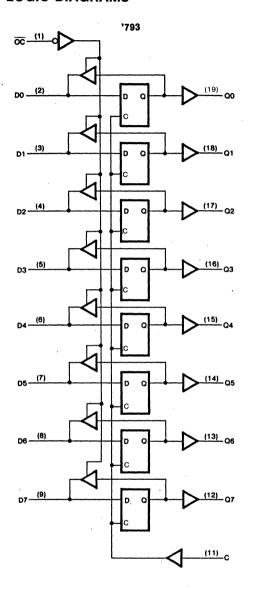
- In this case the output of the latch feeds the input, and a "race" condition results.
- \*\* Qo represents the previous "latched" state.
- † This transition is not a normal mode of operation and may produce hazards.

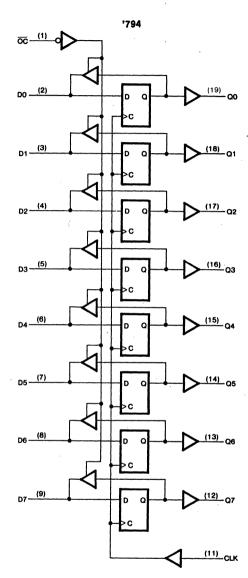
794

CLK	<u>oc</u>	Q	D
L or H or ↓	L	Qo	Output, Q
L or H or ↓	Н	Q <sub>O</sub>	Input
1	L	Qo	Output, Q*
1	Н	D	Input

\* In this case the output of the register is clocked to the inputs and the overall Q output is unchanged at Q<sub>O</sub>.

## **LOGIC DIAGRAMS**





## **Absolute Maximum Ratings\***

Supply Voltage Range $V_{CC}, \ldots -0.5V$ to $+7V$
DC Input Diode Current, I <sub>IK</sub>
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 70 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, $T_{stg} \dots -65^{\circ}C$ to $+150^{\circ}C$
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.

These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Supply Voltage, V <sub>CC</sub>	4.5V to 5.5V
DC Input & Output Voltages*, ViN, Vout	OV to Vcc
Operating Temperature	

Range KS74HCTLS:  $-40^{\circ}$ C to  $+85^{\circ}$ C KS54HCTLS:  $-55^{\circ}$ C to  $+125^{\circ}$ C Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . . . . Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

Characteristic	Symbol	ymbol Test Conditions		<sub>a</sub> = 25°C	KS74HCTLS T <sub>a</sub> = -40°C to +85°C	KS54HCTLS  T <sub>a</sub> = -55°C to +125°C	Unit
			Тур				
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V <sub>JL</sub>			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-6mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=12mA$ $I_{O}=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μА
Maximum Quiescent Supply Current	lcc	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

## AC ELECTRICAL CHARACTERISTICS (Input tr, tr<6 ns), HCTLS793, 794

Characteristic		Symbol	Con	Conditions†		25°C 5.0V	KS74HCTLS  T <sub>a</sub> = -40°C to +85°C  V <sub>CC</sub> = 5.0V ± 10%	KS54HCTLS T <sub>e</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	Unit
					Тур		Guarantee	d Limits	1
Maximum C ('794 only)	Maximum Clock Frequency ('794 only)		C <sub>L</sub> =50pl	C <sub>L</sub> =50pF		40	35	30	MHz
Maximum P	ropagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pl C <sub>L</sub> =150pl		14 17	18 21	23 28	27 33	ns
	('793 only)	t <sub>PHL</sub>	C <sub>L</sub> =50pl C <sub>L</sub> =150pl		14 17	18 21	23 28	27 33	113
Maximum P	ropagation Delay.	t <sub>PLH</sub>	C <sub>1</sub> =50pF		15 18	20 23	25 30	30 36	ns
	CLK/C to Any Q		C <sub>L</sub> =50pl C <sub>L</sub> =150pl		15 18	20 23	25 30	30 36	113
Maximum E	nable Time.	t <sub>PZH</sub>	Bı = 1kΩ	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	15 18	20 23	25 30	30 36	ns
OC to D		t <sub>PZL</sub>	(C=Low	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	15	20 23	25 30	30 36	113
Maximum D	Disable Time,	t <sub>PHZ</sub>		C <sub>L</sub> =50pF for '793)	15 15	20 20	25 25	30 30	ns
Minimum Pi CLK/C High		tw			10	15	. 18	20	ns
Minimum	D before C↓ ('793)	t <sub>su</sub>			8	10	13	15	ns
Setup Time	D before CLKf('794)	·su			10	15	18	20	
Minimum	D after C↓ ('793)	th			8	10	13	15	ns
Hold Time	D after CLK† ('794)	- un			-3	0	0	0	113
Maximum Inp	ut Capacitance	CIN			5				pF
Maximum Ou	tput Capacitance	Cout			10				pF
Power Dissip	ation Capacitance*	C <sub>PD</sub>							ns

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

# KS54HCTLS **821/822** KS74HCTLS

# 10-Bit Bus Interface Flip-Flops with 3-State Outputs

## **Preliminary Specifications**

#### **FEATURES**

- Functionally Equivalent to AMD's Am29821 and Am29822
- Provides Extra Data Width Necessary for Wider Address/Data Paths or Buses with Parity
- Power-Up High-Impedance State
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current
- ( $I_{OL} = 24 \text{ mA } @ V_{OL} = 0.5V$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATIONS

	,	821			
OC (	4	$\sim$	24	Ь	Vcc
1D (	2		23	Ь	1Q
2D [	<b>∃</b> 3		22	þ	2Q
3D [	<b>1</b> 4		21	þ	3Q
4D (	<b>‡</b> 5		20	Þ	4Q
5D [	<b>⋬</b> 6		19	ь	5Q
6D (	<b>1</b> 7		18	Þ	6Q
7D [	<b>∄</b> 8		17	Ь	7Q
8D (	19		16	Ь	8Q
	10		15	ь	9Q
100	<b>‡</b> 11		14	þ	10Q
GND [	12		13	þ	CLK



## **DESCRIPTION**

These 10-bit bus-interface flip-flops feature three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. They are suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

All of the flip-flops are edge-triggered and D-type. On the positive transition of the clock the Q outputs on the '821 will be true, and on the '822 will be complementary to the data input.

A buffered output-control input can be used to place the ten outputs in either a normal logic state (high or low levels) or a high-impedance state. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output control  $(\overline{OC})$  does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### **FUNCTION TABLES**

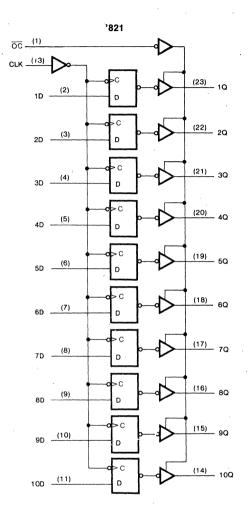
(Each Flip-Flop)

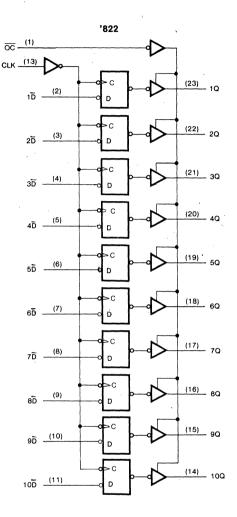
	'821								
	Inputs	Output							
OC	CLK	Q							
L	1	Н	Н						
L	1	L	L						
L	L	X	Q <sub>0</sub> Q <sub>0</sub>						
L	Н	Х	$Q_0$						
Н	X	Χ	Z						

'822

Γ		Inputs	Output	
	оc	CLK	D	Q
Γ	L	1	Н	L
	L	<b>†</b>	L	Н
ĺ	L	L	X	Q <sub>0</sub> Q <sub>0</sub>
	L	Н	X	Q <sub>0</sub>
L	Н	X	X	Z

## LOGIC DIAGRAMS





## **Absolute Maximum Ratings\***

Supply Voltage Range $V_{CC}$ , $-0.5V$ to $+.7V$ DC Input Diode Current, $I_{IK}$
$(V_1 < -0.5V \text{ or } V_1 > V_{CC} + 0.5V)$ ±20 mA
DC Output Diode Current, Iok
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V)$ ±20 mA
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±70 mA
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Supply Voltage, V			
Operating Temper	ature		
Range	KS74HCTLS:	~40°C	to +85°C

KS54HCTLS:  $-55^{\circ}$ C to  $+125^{\circ}$ C Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . . . Max 500 ns

 Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

Characteristic	Symbol	bol Test Conditions		<sub>a</sub> = 25°C	KS74HCTLS $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V <sub>OH</sub> .	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-6mA$	V <sub>CC</sub> 4.2	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> − 0.1 3.84	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	VoL	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	l <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	$V_{IN}=V_{CC}$ or GND $I_{OUT}=O\mu A$		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δlcc	per input pin $V_1=2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

# 10-Bit Bus Interface Flip-Flops with 3-State Outputs

## AC ELECTRICAL CHARACTERISTICS (Input tr, tre6 ns), HCTLS821, HCTLS822

Characteristic	Symbol	Conditions†		$T_a = 25$ °C $V_{CC} = 5.0$ V		$KS74HCTLS$ $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$ $V_{CC} = 5.0V \pm 10^{\circ}$	KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	Unit	
1				Тур		Guarantee	d Limits		
Maximum Operating Frequency	f <sub>max</sub>	C <sub>L</sub> =50pl	=	40	35	30	25	MHz	
Maximum Propagation Delay,	t <sub>PLH</sub>		C <sub>L</sub> =50pF C <sub>L</sub> =150pF		20 23	25 30 .	30 36	ns	
CLK to any Q	t <sub>PHL</sub>	C <sub>L</sub> =50pl C <sub>L</sub> =150pl		15 18	20 23	25 30	30 36	113	
Maximum Output Enable	t <sub>PZL</sub>	$R_L = 1 k\Omega$	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	18 21	24 27	30 35	36 42	ns	
Time, OC to any Q	t <sub>PZL</sub>	11[-172	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	18 21	24 27	30 35	36 42	113	
Maximum Output Disable	t <sub>PHZ</sub>	$R_L = 1 k\Omega$		18	24	30	36	ns	
Time, OC to any Q	' t <sub>PLZ</sub>	C <sub>L</sub> =50pl	= ·	18	24	30	36	113	
Minimum Pulse Width, CLK High or Low	t <sub>w</sub>			12	16	20	24	ns	
Minimum Setup Time, Data before CLK†	t <sub>su</sub>			12	16	20	24	ns	
Minimum Hold Time, Data after CLK†	th			-3	0	0	0	ns	
Maximum Input Capacitance	CIN			5				pF	
Maximum Output Capacitance	Cout	OC=Vcc		10				рF	
Power Dissipation Capacitance* (per stage)	C <sub>PD</sub>	$\overline{OC} = V_{CC}$ $\overline{OC} = GNI$		5 'O				pF	

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} \ V_{CC}^2 \ f + I_{CC} \ V_{CC}$ .



<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

#### **FEATURES**

- Functionally Equivalent to AMD's Am29823 and Am29824
- Provides Extra Data Width Necessary for Wider Address/Data Paths or Buses with Parity
- · Power-Up High-Impedance State
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current
   (I<sub>OL</sub> = 24 mA @ V<sub>OL</sub> = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- . Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATIONS

'823

ᅈᅺ	1	24	$b_{v_{cc}}$
100	2	23	10
200	3	22	<b>1</b> 2Q
зрД	4	21	<b>3</b> 30
4DQ	5	20	<b>1</b> 40
5DQ	6	19	<b>D</b> 5Q
6D □	7	18	<b>⊐</b> 6Q
7DQ	8	17	70
80년	9	16	⊒8Q
9D 🛛	10	15	<b>1</b> 9Q
CLR C	11	14	CLKEN
GND	12	13	CLK
,			•

'824

<del>∞</del> d	1	24	$\mathbf{b}_{v_{cc}}$
100	2	23	1a
25 <b>d</b>	3	22	20
3₫	4	21	<b>⊒</b> 3Q
4DC	5 .	20	<b>1</b> 40
5D[	6	19	<b>⊃</b> 5Q
6D [	7	18	<b>□</b> 6Q
700	8	17	70
854	9	16	<b>□</b> 8Q
9 <u>D</u> Q	10	15	<b>⊒</b> 90
ZER C	11		CLKEN
ND [	12	13	CLK

## DESCRIPTION

These 9-bit bus interface flip-flops feature three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. They are suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers, parity bus interfacing and working registers.

With the clock enable ( $\overline{\text{CLKEN}}$ ) low, the D-type edgetriggered flip-flops enter data on the low-to-high transitions of the clock. Taking  $\overline{\text{CLKEN}}$  high will disable the clock buffer, thus latching the outputs. The '823 has noninverting D inputs and the '824 has inverting D inputs. Taking the  $\overline{\text{CLR}}$  input low causes the nine Q outputs to go low independently of the clock.

A buffered output-control input ( $\overline{OC}$ ) can be used to place the ten outputs in either a normal logic state (high or low levels) or a high-impedance state. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output control does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### **FUNCTION TABLES**

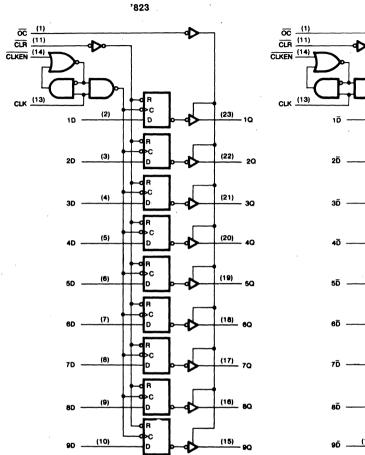
'823

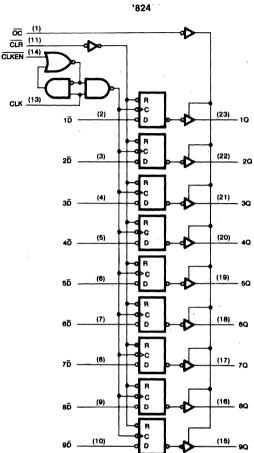
		INPUT			
		OUTPUT			
оc	CLR	CLKEN	CLK	D	Q
L	L	X	X	Х	L
L	Н	L	. ↓	Н	н
L	Н	L	<b>↑</b>	L	L
L	Н	Н	X	X	$Q_0$
Н	X	X	X	Х	Z '
	L L L L	L L L H L H	L L X L H L L H L	L L X X L H L †	L L X X X L H L ↑ ↑ H L

824

		OUTPUT			
ŌĊ	CLR	CLKEN	· CLK	D	Q
L	· L	Х	X	Χ	L
L	Ή	L	<b>↑</b>	H	L
L	Н	L	<b>↑</b>	L	Н
L	Н	Н	X	Х	$Q_0$
Н	X	Х	Х	Х	Z ·

# LOGIC DIAGRAMS





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## **Absolute Maximum Ratings\***

<sup>\*</sup> Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

## **Recommended Operating Conditions**

Supply Voltage, V	cc	4	₽.5V to	5.5V
DC Input & Outpu				
Operating Temper	ature			
Pange	KS74HCTLS	-40°	C to +	85°C

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C Input Rise & Fall Times,  $t_r$ ,  $t_t$  . . . . . . Max 500 ns

Characteristic	Symbol	Test Conditions	T,	a = 25°C	KS74HCTLS $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	VIH			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	v
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=-20\mu A$ $I_{O}=-6mA$	V <sub>CC</sub> 4.2	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> -0.1	V <sub>CC</sub> −0.1 3.7	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δl <sub>CC</sub>	per input pin $V_1$ =2.4V other Inputs: at $V_{CC}$ or GND $I_{OUT}$ =0 $\mu$ A		2.7	2.9	3.0	mA

Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

# 9-Bit Bus Interface Flip-Flops with 3-State Outputs

#### AC ELECTRICAL CHARACTERISTICS (Input tr, tr<6 ns), HCTLS823, HCTLS824

Characteristic		Symbol	Conditions†		Conditions <sup>†</sup>		Conditions <sup>†</sup>		T <sub>A</sub> = :		KS74HCTLS T <sub>A</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%	KS54HCTLS $T_A = -55^{\circ}C \text{ to } +125^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$	Unit
					Тур		Guarantee	Limits					
Maximum Op	perating Frequency	f <sub>max</sub>	C <sub>L</sub> =50pl		40	35	30	25	MHz				
Maximum Pr	opagation Delay,	tpLH	C <sub>L</sub> =50pl C <sub>L</sub> =150		15 18	20 23	25 30	30 <b>3</b> 6	ns				
CLK to any		t <sub>PHL</sub>	CL=50pl CL=150		15 18	20 23	25 30	30 36	113				
Maximum Pr CLR to Any	opagation Delay,	tецн	C <sub>L</sub> =50pl C <sub>L</sub> =150		17 20	22 25	28 33	34 40	ns				
Maximum Output Enable Time, ÖC to any Q		tpzL	Rı = 1 kΩ	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	18 21	24 27	30 35	36 <b>42</b>	ns				
		tpzL	NL- 1Ku	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	18 21	24 27	30 35	36 <b>42</b>	113				
Maximum Ou	utput Disable	t <sub>PHZ</sub>	$R_L = 1 k\Omega$ $C_L = 50 pF$		18	24	30	36	ns				
Time, OC to	any Q	tpLZ			18	24	30	36	113				
Minimum	CLR Low	tw			12	16	20	24	ns				
Pulse Width	CLK high or Low	\w			12	16	20	24					
Minimum	CLR Inactive				12	16	20	24					
Setup Time	Data	tsu			12	16	20	24	ns				
Before CLK1	CLKEN high or Low				12	16	20	24					
Minimum Hold Time, CLKEN or data after CLK†		t <sub>h</sub>			-3	0	0 ,	0	ns				
Maximum Inj	put Capacitance	CIN			5				pF				
Maximum O	utput Capacitance	Cout	Output D	isabled	10				pF				
Power Dissipation Capacitance* (per stage)		C <sub>PD</sub>	OC=V <sub>CC</sub> OC=GNI		5 30				pF				

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

#### KS54HCTLS **825/826** KS74HCTLS

8-Bit Bus Interface Flip-Flops with 3-State Outputs

Preliminary Specifications

#### **FEATURES**

- Functionally Equivalent to AMD's Am29825 and Am29826
- Improved I<sub>OH</sub> Specifications
- Multiple Output Enables Allow Multiuser Control of the Interface
- Power-Up High-Impedance State
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- . 3-State outputs with high drive current
- ( $I_{OL} = 24$  mA @  $V_{OL} = 0.5$ V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
   KS74HCTLS: -40°C to +85°C
   KS54HCTLS: -55°C to +125°C
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATIONS

	'82	5	
OC1 [	<u></u>	24	$V_{cc}$
OC2	2	23	ОCЗ
1D [	3	22	1Q
2D [	4	21	2Q
3D [	5	20	3Q
4D [	16	19	4Q
5D C	7	18	5Q
6D [	8	17	6Q
7D 🕻	9 '	16	7Q
8D [	10	15 🗖	8Q
CLR	111	14	CLKEN
GND [	12	13	CLK

	′826		
0C1 d 0C2 d	1 2		D v
10 d	3	22	10
2D 🗖	4	21	2Q
зō 🗖	5	20	<b>3</b> 0
4D 🗆	6	19	4Q `
5D 🗖		18	<b>5</b> 0
6D 🗖		17	<b>⊐</b> 60
7Ď 🗖		16	<b>1</b> 70
8D 🗖		15	D 8Q
CLR C	11	14	CLKEN
GND [	12	13	CLK

#### DESCRIPTION

These 8-bit bus interface flip-flops leature three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. They are suitable for implementing multiuser buffer registers, I/O ports, bidirectional bus drivers and working registers.

With the clock enable ( $\overline{\text{CLKEN}}$ ) low, all D-type edge-triggered flip-flops enter data on the low-to-high transitions of the clock. Taking  $\overline{\text{CLKEN}}$  high will disable the clock buffer, thus latching the outputs. The '825 has non-inverting D inputs and the '826 has inverting  $\overline{\text{D}}$  inputs. Taking the  $\overline{\text{CLR}}$  inputs low causes the eight Q outputs to go low independently of the clock.

Multiuser buffered output-control inputs ( $\overline{OC1}$ ,  $\overline{OC2}$ , and  $\overline{OC3}$ ) can be used to place the eight outputs in either a normal logic state (high or low level) or a high-impedance state. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output controls do not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground

#### **FUNCTION TABLES**

'825

	Inputs							
<u>oc</u> +	CLR	CLKEN	CLK	D	Q			
L	L	. X	X	Х	L			
L	Н	L	<b>†</b>	Н	Н			
L	Н	L	<b>†</b>	L	L			
L	Н	н	Х	Χ	Qo			
Н	Х	Х	X	Χ	Z			

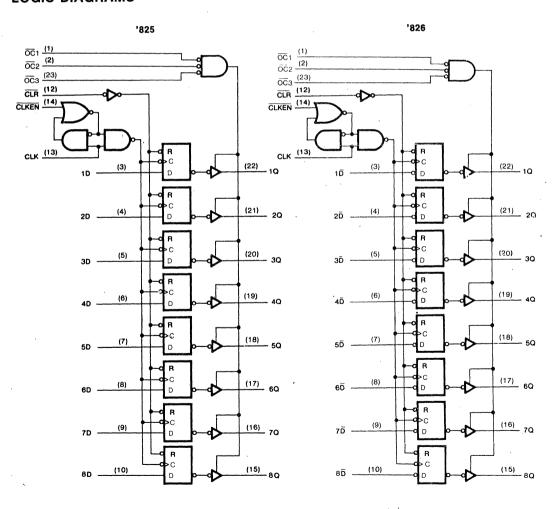
<sup>\*</sup> OC=H if any of OC1, OC2, or OC3 are high. OC=L of OC1, OC2, and OC3 are low.

'826

	Inputs						
ŌĈ*	CLR	CLKEN	CLK	D	a		
L	L	X	Х	X	L		
L	H	L	Ť	Н	L		
L	Н	L	Ť	L	н		
Ľ	Н	н	Х	Х	Q <sub>0</sub>		
н	Х	Х	Х	Х	·Z		

\* OC = H if any of OC1, OC2, or OC3 are high. OC = L of OC1, OC2, and OC3 are low.

#### LOGIC DIAGRAMS



#### KS54HCTLS **825/826** KS74HCTLS

# 8-Bit Bus Interface Flip-Flops with 3-State Outputs

#### **Absolute Maximum Ratings\***

Supply Voltage Range $V_{CC}, \ldots -0.5V$ to $+7V$
DC Input Diode Current, I <sub>IK</sub>
$(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V)$ $\pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V)$ ±20 mA
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 70 \text{ mA}$
Continuous Current Through
$V_{CC}$ or GND pins
Storage Temperature Range, $T_{stg} \dots -65 ^{\circ}\text{C}$ to $+150 ^{\circ}\text{C}$
Power Dissipation Per Package, $P_d{}^\dagger$ 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

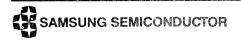
#### **Recommended Operating Conditions**

Range KS74HCTLS:  $-40^{\circ}$ C to  $+85^{\circ}$ C KS54HCTLS:  $-55^{\circ}$ C to  $+125^{\circ}$ C Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . . Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

#### DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions		<sub>a</sub> = 25°C	KS74HCTLS $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its .	
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	. 0.8	v
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN} = V_{IH}$ or $V_{IL}$ $I_O = -20\mu A$ $I_O = -6mA$	V <sub>CC</sub> 4.2	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> -0.1 3.84	V <sub>CC</sub> -0.1 3.7	v
Maximum Low-Level Output Voltage	Vol	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=12mA$ $I_{O}=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I <sub>IN</sub>	· V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μΑ
Additional Worst Case Supply Current	Δl <sub>CC</sub>	per input pin $V_1$ =2.4V other inputs: at $V_{CC}$ or GND $I_{OUT}$ =0 $\mu$ A		2.7	2.9	3.0	mA



# 8-Bit Bus Interface Flip-Flops with 3-State Outputs

#### AC ELECTRICAL CHARACTERISTICS (Input tr, tr≤6 ns), HCTLS825, HCTLS826

Characteristic		Symbol	Conditions <sup>†</sup>		I Conditions <sup>↑</sup>		T <sub>a</sub> = 2 V <sub>CC</sub> =		KS74HCTLS  T <sub>a</sub> = -40°C to +85°C  V <sub>CC</sub> = 5.0V ± 10%	KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	Unit
					Тур		Guarantee	d Limits	1		
Maximum Op	erating Frequency	f <sub>max</sub>	C <sub>L</sub> =50pl	L=50pF		35	30	25	MHz		
Maximum Pr	opagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pl C <sub>L</sub> =150		15 18	i	25 30	30 <b>36</b>	- ns		
CLK to any Q		t <sub>PHL</sub>	C <sub>L</sub> =50pl C <sub>L</sub> =150		15 18	20 23	25 30	30 <b>36</b>	113		
Maximum Pr CLR to Any	opagation Delay, Q	t <sub>PLH</sub>	C <sub>L</sub> =50pl C <sub>L</sub> =150		17 20	22 25	28 33	34 40	ns		
Maximum Output Enable		t <sub>PZL</sub>	B <sub>1</sub> = 1k0	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	18 21	24 27	30 35	. 36 <b>42</b>	ns		
	Time, OC to any Q		11[-114	$C_L = 50pF$ $C_L = 150pF$	18	24 27	30 35	36 <b>42</b>	113		
Maximum Output Disable		t <sub>PHZ</sub>	$R_L = 1 k\Omega$		18	24	30	36	ns		
Time, OC to	any Q	t <sub>PLZ</sub>	C <sub>L</sub> =50pF		18	24	. 30	36	110		
Minimum Pulse Width	CLR Low CLK high or Low	t <sub>w</sub>			12	16 16	20 20	24	- ns		
Minimum	CLR Inactive				12	16	20	24			
Setup Time	Data	t <sub>su</sub>			12	16	20	24	ns		
Before CLK1	CLKEN high or Low				12	16	20	24			
Minimum Hold Time, CLKEN or data after CLK†		t <sub>h</sub>			-3	0	0	0	ns		
Maximum Inj	Maximum Input Capacitance				5	1			pF		
Maximum O	utput Capacitance	Cout			10				pF		
Power Dissipation Capacitance* (per stage)		C <sub>PD</sub>			5 30				pF		

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} \ V_{CC}^2 \ f \ + \ I_{CC} \ V_{CC}$ .

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

#### KS54HCTLS **841/842** KS74HCTLS

# 10-Bit Bus Interface D-Type Latches with 3-State Outputs

## Preliminary Specifications FEATURES

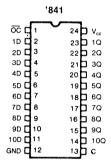
- Bus-Structured Pinout
- · Provides Extra Bus Driving Latches
- Necessary for Wider Address/Data Paths or Buses with Parity
- Power-Up High-Impedance State
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- . Low power consumption characteristic of CMOS
- . 3-State outputs with high drive current
- ( $I_{OL} = 24 \text{ mA}$  @  $V_{OL} = 0.5 \text{V}$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

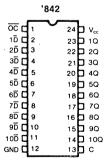
KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATIONS





#### DESCRIPTION

These 10-bit bus interface latches feature three state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are suitable for implementing wider buffer registers. I/O ports, bidirectional bus drivers, and working registers.

The ten latches are transparent D-type. The '841 has noninverting data (D) inputs and the '842 has inverting ( $\overline{D}$ ) inputs.

A buffered output control ( $\overline{OC}$ ) input can be used to place the ten outputs in either a normal logic state (high or low levels) or a high-impedance state. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are off.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V<sub>CC</sub> and ground.

#### **FUNCTION TABLES**

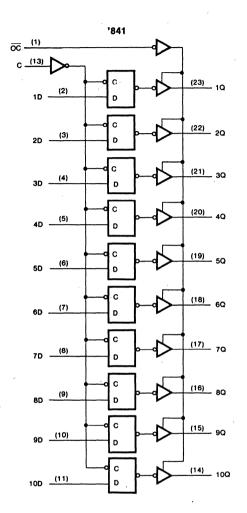
'841

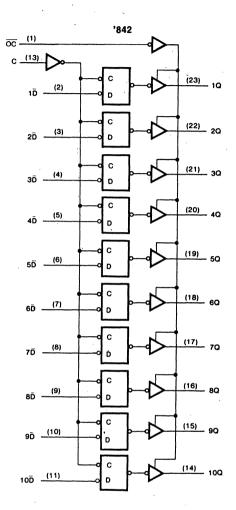
		-	li e	
IN	PUT	OUTPUT.		
ōc	С	D	Q	
L	Н	Н	H	
, L	Н	L	L	
L	L	Χ	$Q_0$	
Н	Χ	Х	Z	

'842

IN	PUT	ОИТРИТ		
ŌĊ	С	Ď		Q
L	Н	Н		L
L	Н	L		н
L	L	Χ		$Q_0$
Н	Χ	Χ	-	. Z

#### **LOGIC DIAGRAMS**





#### **Absolute Maximum Ratings\***

posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

#### **Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . . . . . . 4.5V to 5.5V DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . 0V to  $V_{CC}$  Operating Temperature

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

#### DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Symbol Test Conditions		<sub>a</sub> = 25°C	KS74HCTLS $T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	its	
Minimum High-Level Input Voltage	ViH			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8,	0.8	0.8	٧
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-6mA$	V <sub>CC</sub> 4.2	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> −0.1 3.7	V
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=12mA$ $I_{O}=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μΑ
Maximum Quiescent Supply Current	lcc	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μА
Additional Worst Case Supply Current	Δlcc	per input pin $V_1=2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=O\mu A$		2.7	2.9	3.0	mA

#### AC ELECTRICAL CHARACTERISTICS (Input tr, tre6 ns), HCTLS841, HCTLS842

Characteristic	Symbol	conditions <sup>†</sup>		_	25°C : 5.0V	KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$	KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> =5.0V ± 10%	Unit	
				Тур		Guarantee	d Limits		
Maximum Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> = 50 C <sub>L</sub> =150		15 18	20 23	25 30	30 3 <b>6</b>	ns	
Data to Q	t <sub>PHL</sub>	C <sub>L</sub> =50pl C <sub>L</sub> =150		15 18	20 23	25 30	30 36		
Maximum Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50pl C <sub>L</sub> =150		21 24	28 31	35 / 40	42 48	ns	
C to any Q	t <sub>PHL</sub>	C <sub>L</sub> =50pl C <sub>L</sub> =150		21 24	28 31	35 40	42 48	IIS	
Maximum Output Enable	t <sub>PZH</sub>	$R_i = 1 k\Omega$	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	18 21	24 27	30 35	36 42	ns	
Time, OC to any Q	t <sub>PZL</sub>	110	$C_L=50pF$ $C_L=150pF$	18 21	24 27	30 35	36 42		
Maximum Output Disable Time, OC to any Q	t <sub>PHZ</sub>	$R_L=1k\Omega$ $C_L=50pl$	=	18 18	24 24	30 30	36 36	ns	
Minimum Pulse Width, C High	t <sub>w</sub>			15	20	25	30	ns	
Minimum Setup Time, Data before C↓	t <sub>su</sub>			12	16	. 20	24	ns	
Minimum Hold Time, Data after C↓	th			6	8	10	12	ns	
Maximum Input Capacitance	CIN			5		,		pF	
Maximum Output Capacitance	Соит			10				рF	
Power Dissipation Capacitance* (per stage)	C <sub>PD</sub>	OC=V <sub>CC</sub> OC=GNI		5 30		٠		pF	

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub>² f + I<sub>CC</sub> V<sub>CC</sub>.
† For AC switching test circuits and timing waveforms see section 2.

#### KS54HCTLS **843/844** KS74HCTLS

# 9-Bit Bus Interface D-Type Latches with 3-State Outputs

#### Preliminary Specifications

#### **FEATURES**

- Bus-Structured Pinout
- Provide Extra Bus Driving Latches
   Necessary for Wider Address/Data Paths or Buses with Parity
- Power-Up High Impedance
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current
- ( $I_{OL} = 24 \text{ mA } @ V_{OL} = 0.5 \text{V}$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
   KS74HCTLS: -40°C to +85°C
- KS54HCTLS: -55°C to +125°C
   Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATIONS

	′843			
ᅙ	1	24	Ь	V <sub>cc</sub>
1D 🗖	2	23	þ	1Q
2D 🗖	3	22	þ	2Q
3D 🗖	4	21	þ	3Q
4D 🗆	5	20	Þ	4Q
5D 🗖	6	19	Þ	5Q
6D 🗖	7	18	b	6Q
7D 🗖	8	17	Þ	7Q
8D 🗖	9	16	Ь	8Q
9D 🗖		15	Ь	9Q
CLR	11	14	Ь	PRE
GND 🗆	12	13	Þ	С

		844			
	1	$\overline{}$		•	
ОC	_	1	24	p	$V_{cc}$
1D			23	Þ	1Q
2D	d	3	22	Þ	2Q
3D	-	4	21	þ	3Q
4D	_		20	þ	4Q
5D		6	19	þ	5Q
6D		7	18	þ	6Q
7D		8	17	Þ	7Q
8D		9	16	Þ	8Q
9D	-	10	15	Ь	9Q
CLR	d	11	14	Ь	PRE
GND	d	12	13	þ	С

#### DESCRIPTION

These 9-bit bus interface latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers, parity bus interfacing and working registers.

The nine latches are transparent D-type. The '843 has noninverting data (D) inputs and the '844 has inverting  $\overline{D}$  inputs

A buffered output control  $(\overline{OC})$  input can be used to place the nine outputs in either a normal logic state (high or low levels) or a high-impedance state. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control ( $\overline{OC}$ ) does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are off.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and  $\tilde{\ }$  ground.

#### **FUNCTION TABLES**

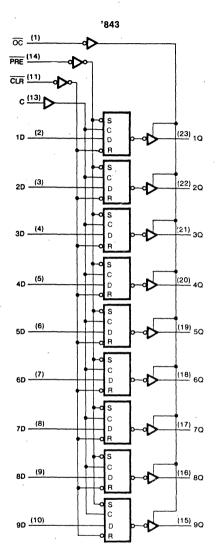
'843

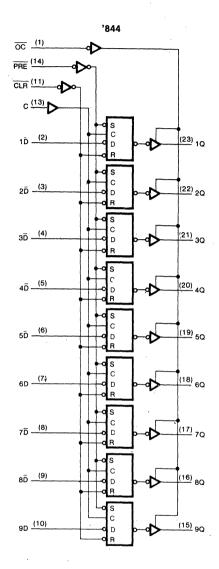
	IN	OUTPUT			
PRE	CLR	оc	С	D	Q
L	Х	L	Χ	Х	Н
Н	L	L	Χ	Χ	L
Н	Н	L	Н	L	L
Н	Н	L	Н	Н	Н
Н	Н	L	L	Χ	Qo
X	X	Н	X	Х	Z

'844

	INF	OUTPUT			
PRE	CLR	ōc	С	D	Q
L	X	L	Х	Χ	Н
Н	L	L	Χ	Χ	L
H.	Н	L	Н	L	Н
Н	Н	L	Н	Н	L
Н	н	L	L	Χ	$Q_0$
Х	Х	Н	X	Χ	Z

#### **LOGIC DIAGRAMS**





#### KS54HCTLS **843/844** KS74HCTLS

## 9-Bit Bus Interface D-Type Latches with 3-State Outputs

#### **Absolute Maximum Ratings\***

Supply Voltage Range $V_{CC}$ ,0.5V to +7V
DC Input Diode Current, I <sub>IK</sub>
$(V_I < -0.5 V \text{ or } V_I > V_{CC} + 0.5 V) \ \dots \ \pm 20 \text{ mA}$
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V)$ $\pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) + \pm 70 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±250 mA
Storage Temperature Range, $T_{stg} \dots -65$ °C to $+150$ °C
Power Dissipation Per Package, $P_d{}^\dagger$ 500 mW
* Absolute Maximum Ratings are those values beyond
which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-
posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

#### **Recommended Operating Conditions**

Range KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . . . Max 500 ns

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

#### DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	ns T <sub>a</sub> = 25		KS74HCTLS T <sub>a</sub> = -40°C to +85°C	KS54HCTLS C T <sub>a</sub> = -55°C to +125°C			
			Тур	Guaranteed Limits					
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	٧		
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	0.8	v		
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN} = V_{IH}$ or $V_{IL}$ $I_O = -20\mu A$ $I_O = -6mA$	V <sub>CC</sub> 4.2	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> -0.1 3.84	V <sub>CC</sub> −0.1 3.7	v		
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=12mA$ $I_{O}=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v		
Maximum Input Current	l <sub>IN</sub> •	V <sub>IN</sub> =V <sub>CC</sub> or GND	•	±0.1	±1.0	±1.0	μΑ		
Maximum 3-State Leakage Current	loz	Output Enable =V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μА		
Maximum Quiescent Supply Current	lcc	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μΑ		
Additional Worst Case Supply Current	Δlcc	per input pin V <sub>1</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA		



# 9-Bit Bus Interface D-Type Latches with 3-State Outputs

#### AC ELECTRICAL CHARACTERISTICS (Input t<sub>r</sub>, t<sub>i</sub>≤6 ns), HCTLS843, HCTLS844

Characteristic	Symbol	Symbol Conditions <sup>†</sup>		T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74HCTLS  T <sub>a</sub> = -40°C to +85°C  V <sub>CC</sub> = 5.0V ± 10%	KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	Unit
				Тур		Guaranteed Limits		
Maximum Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> = 50 C <sub>L</sub> =150		18 21	24 27	30 35	36 42	ns
to	t <sub>PHL</sub>	C <sub>L</sub> =50p C <sub>L</sub> =150		18 21	24 27	30 35	36 42	113
Maximum Propagation Delay,	t <sub>PLH</sub>	C <sub>L</sub> =50p C <sub>L</sub> =150		21 24	28 31	35 40	42 <b>48</b>	ns
C to any Q	t <sub>PHL</sub>	C <sub>L</sub> =50pl C <sub>L</sub> =150		21 24	28 31	35 40	42 48	113
Maximum Propagation Delay, PRE to Q	t <sub>PLH</sub>	C <sub>L</sub> =50p C <sub>L</sub> =150		23 26	30 33	38 43	46 52	ns
Maximum Propagation Delay, CLR to Q	t <sub>PHL</sub>	C <sub>L</sub> =50p C <sub>L</sub> =150		23 26	30 33	- 38 43	46 52	ns
Maximum Output Enable	t <sub>PZH</sub>	Rı = 1kΩ	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	18 21	24 27	30 35	36 42	ns
Time, OC to any Q	t <sub>PZL</sub>	11[-1722	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	18 21	24 27	30 35	36 42	113
Maximum Output Disable	t <sub>PHZ</sub>	$R_L = 1 k\Omega$		18	24	30	36	ns
Time, OC to any Q	tPLZ	C <sub>L</sub> =50pl	F	18	24	30	36	113
Minimum Pulse Width, C High	tw			15	20	25	30	ns
Minimum Setup Time, Data after C↓	t <sub>su</sub>			12	16	20	24	ns
Minimum Hold Time, Data before C↓	th			6	8	10	12	ns
Maximum Input Capacitance	CiN			5				pF
Maximum Output Capacitance	Cout			10				рF
Power Dissipation Capacitance (per stage)	C <sub>PD</sub>	OC=V <sub>CC</sub> OC=GNI		5 30				pF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.



<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

#### KS54HCTLS **845/846** KS74HCTLS

#### 8-Bit Bus Interface D-Type Latches with 3-State Outputs

#### Preliminary Specifications

#### **FEATURE**

- . 3-state buffer-type outputs drive bus-lines directly
- · Bus-structured pinout
- Provides extra bus driving latches necessary for wider address/data paths or buses with parity
- Low power consumption characteristic of CMOS devices
- 3-state outputs with high drive current (I<sub>OL</sub> = 24mA @ V<sub>OL</sub> = 0.5V) for direct bus interface
- Direct interface capability with TTL, NMOS and CMOS devices
- Wide operating volage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to 125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATIONS

	'845		
0C1 C	<u></u> _	24	Ь v
OC2	2	23	<b>□</b> <del>0</del> <del>0</del> <del>0</del> <del>0</del> 3
1D 🗀	3	22	<b>1</b> 0
2D 🗀	4	21	2Q
3D 🗀	5	20	] 3Q
4D 🗆	6	19	<b>□</b> 4Q
5D 🗖	7	18	] 5Q
6D 🗀	8	17	<b>]</b> 6Q
7D 🗀	9	16	7Q
8D C	10	15	BQ [
CLR C	11	14	PRE
GND [	12	13	DС

	•	940			
∞1 d	1	<u> </u>	24	Ь	Vcc
<u></u> <del>C</del>	2		23		<del>oc</del> 3
1 D C	3		22	þ	1Q
20 🗖	4		21	þ	2Q
3Ď 🗖			20	Þ	3Q
40 □	6		19	Ь	4Q
5D C	7		18	þ	5Q
6 <u>D</u> ☐	8		17	Þ	6Q
7页 ₫	9		16	Ь	7Q
8D C	10		15	Ь	8Q
CLR C	11		14	þ	PRE
GND [	12		13	þ	С
		_	_	,	

#### DESCRIPTION

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches are transparent D-type. The '845 has noninverting data(D) inputs. The '846 has inverting D inputs. Since CLR and PRE are independent of the clock, taking the CLR input low will cause the eight Q outputs to go low. Taking the PRE input low will cause the eight Q outputs to go high. When both PRE and CLR are taken low, the outputs will follow the preset condition.

The buffered output control inputs ( $\overline{OC}1$ ,  $\overline{OC}2$ , and  $\overline{OC}3$ ) can be used to place the eight outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impendance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output controls do not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

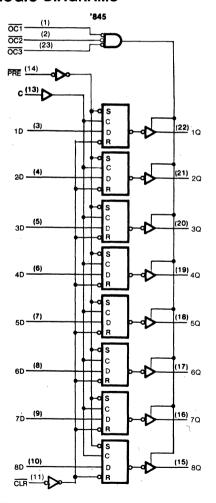
## FUNCTION TABLE '845

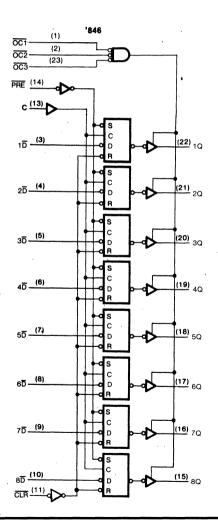
	INPUTS									
PRE	CLR	OC1	OC2	OC3	С	D	a			
L	Н	L	L	L	Х	Х	Н			
Н	L	L	L	L	Х	Х	L			
L	L	L	L	L	Х	Х	Н			
Н	Н	L	L	L	Н	L	L			
Н	Н	L	L	L'	Н	н	н			
Н	Н	L	L	L	L	Х	$Q_0$			
х	Х	X	Х	Н	Х	Х	Q <sub>0</sub> Ż			
X	X	X	Н	Х	Х	Х	Z			
X	Х	Н	Х	Х	Х	Х	Z			

'846

	INPUTS										
PRE	CLR	OC1	OC2	OC3	С	D	Q				
L	Н	L	L	L	Χ	Х	Η				
Н	L	L	L	L	Χ	X	L				
L	L	L	L	L	Х	Х	н				
Н	н	L	L	L	Н	L	Н				
Н	Н	L	L	L	Н	Н	L				
Н	Н	L	L	L	L	X	$Q_0$				
Х	Х	Х	Χ	Н	Χ	X	Z				
Х	Х	Х	Н	Х	Χ	Х	Z				
Х	Χ	Н	. X	Χ	Χ	Χ	Z				

#### **LOGIC DIAGRAMS**





#### KS54HCTLS **845/846** KS74HCTLS

# 8-Bit Bus Interface D-Type Latches with 3-State Outputs

#### **Absolute Maximum Ratings\***

Supply Voltage Range $V_{CC}, \ldots -0.5V$ to $+7V$
DC Input Diode Current, I <sub>IK</sub>
$(V_I < -0.5 \cVec{V}$ or $V_I > V_{CC} + 0.5 \cVec{V}$ $\pm 20$ mA
DC Output Diode Current, IOK
$(V_0 < -0.5V \text{ or } V_0 > V_{CC} + 0.5V)$ ±20 mA
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V) \dots \pm 35 \text{ mA}$
Continuous Current Through
V <sub>CC</sub> or GND pins ±125 mA
Storage Temperature Range, $T_{stg}$ $-65^{\circ}C$ to $+150^{\circ}C$
Power Dissipation Per Package, Pd† 500 mW

Power Dissipation Per Package, P<sub>d</sub>† . . . . . 500 mW
 Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

#### **Recommended Operating Conditions**

Range KS74HCLTS: -40°C to +85°C KS54HCLTS: -55°C to +125°C Input Rise & Fall Times, t<sub>r</sub>, t<sub>t</sub> . . . . . . . . . . Max 500 ns

 Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

#### DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T <sub>a</sub> = 25°C		KS74HCTLS T <sub>a</sub> = -40°C to +85°C	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit	
					Guaranteed Limits		1	
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	٧	
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	>	
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> −0.1 3.84	V <sub>CC</sub> -0.1 3.7	٧	
Maximum Low-Level Output Voltage	, V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	v	
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μΑ	
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μΑ	
Additional Worst Case Supply Current	ΔΙ <sub>CC</sub>	per input pin V <sub>1</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA	



#### AC ELECTRICAL CHARACTERISTICS (Input tr, tr 66 ns), HCTLS845

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		$KS74HCTLS$ $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$ $V_{CC} = 5.0V \pm 10\%$	KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> =5.0V ± 10%	Unit
			Тур			Limits	
Propagation Delay	t <sub>PLH</sub>		23	30	38	46	ns
Clk to Q	t <sub>PHL</sub>		23	30	38	46	113
Propagation Delay	t <sub>PLH</sub>		18	24	30	36	ns
D to Q	t <sub>PHL</sub>	,	18	24	30	36	115
Propagation Delay	telH		27	36	45	54	ns
CLR to Q	t <sub>PHL</sub>		27	36	45	54	
Propagation Delay	tplH		27	36	45	54	ns
PRE to Q	t <sub>PHL</sub>		27	36	45	54	
Propagation Delay	t <sub>PZH</sub>		23	30	38	46	ns
OC to Q	t <sub>PZL</sub>		23	30	38	46	115
Propagation Delay	t <sub>PHZ</sub>		16	21	26	31	ns
OC to Q	t <sub>PLZ</sub>		16	21	26	31	113
Input Capacitance	Cin		5				рF
Power dissipation Capacitance*	C <sub>PD</sub>						рF

<sup>\*</sup> CPD determines the no-load dynamic power dissipation: PD=CPD VCC2 f + ICC VCC.

#### AC ELECTRICAL CHARACTERISTICS (Input tr, tre6 ns), HCTLS846

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74HCTLS T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%	KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> =5.0V ± 10%	Unit
N c			Тур	·	Guaranteed	Limits	
Propagation Delay	t <sub>PLH</sub>		25	34	42	65	ns
Clk to Q	t <sub>PHL</sub>	,	25	34	42	65	"
Propagation Delay	t <sub>PLH</sub>		20	27	34	40	ns
D to Q	t <sub>PHL</sub>		20	27	34	40	113
Propagation Delay	tpĹH		26	35	44	53	ns
CLR to Q	t <sub>PHL</sub>		26	35	44	53	
Propagation Delay	t <sub>PLH</sub>		26	35	44	52	ns
PRE to Q	t <sub>PHL</sub>		26	35	44	52	
Propagation Delay	t <sub>PZH</sub>		19	26	32	38	ns
OC to Q	t <sub>PZL</sub>		19	26	32	38	
Propagation Delay	t <sub>PHZ</sub>		14	19	24	30	ns
OC to Q	tPLZ		14	19	24	30	IIS
Input Capacitance	CiN		5				pF
Power dissipation Capacitance*	C <sub>PD</sub>						pF

<sup>\*</sup> C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

 $<sup>^{\</sup>dagger}$  For AC switching test circuits and timing waveforms see section 2.



<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

#### **FEATURES**

- Modified input structure allows voltages up to 15V
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High drive current outputs: I<sub>OL</sub>=8mA @ V<sub>OL</sub>=0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
   KS74HCTLS: -40°C to +85°C

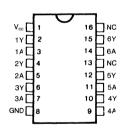
KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C

 Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### DESCRIPTION

The '4049 and '4050 have a modified input protection structure that enable them to be used as logic level translators which will convert high level logic to a low level logic while operating from the low logic supply. For example, 0-15V logic can be corverted to 0-5V logic when using a 5V supply. The modified input protection has no diode connected to  $V_{\rm cc}$ , thus allowing the input voltage to exceed the supply. The lower zener diode protects the input from both positive and negative static voltages. In addition the '4049 and '4050 can be used as simple buffers or inverters without level translation.

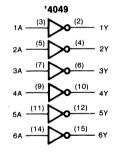
#### PIN CONFIGURATION

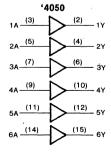


#### **FUNCTION TABLE**

INPUT	OUTPUT Y						
A	'4049	'4050					
Н	L	Н					
L	H	L					

#### LOGIC DIAGRAMS





#### Absolute Maximum Ratings\*

Supply Voltage Hange $V_{CC}$ , $-0.5V$ to $+7V$
DC Input Diode Current, I <sub>IK</sub>
$(V_1 < -0.5V \text{ or } V_1 > +15.5V)$ ±20 mA
DC Output Diode Current, IOK
$(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V) \dots \pm 20 \text{ mA}$
Continuous Output Current Per Pin, Io
$(-0.5V < V_O < V_{CC} + 0.5V)$ ±35 mA
Continuous Current Through
. Vcc or GND pins ±125 mA
Storage Temperature Range, T <sub>stg</sub> 65°C to +150°C
Power Dissipation Per Package, Pd† 500 mW
* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.
These are stress ratings only and functional operation
of the device at or beyond them is not implied. Long ex-
posure to these conditions may affect device reliability.

† Power Dissipation temperature derating: Plastic Package (N): -12mW/°C from 65°C to 85°C Ceramic Package (J): -12mW/°C from 100°C to 125°C

#### **Recommended Operating Conditions**

		. 5
Supply Voltage, V	′cc	4.5V to 5.5V
DC Input & Output	it Voltages*, V <sub>IN</sub> ,	Vout OV to Vcc
Operating Temper	ature	
Range	KS74HCTLS:	-40°C to +85°C
	MOT ALIOTI O	EE00

 \* Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

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#### DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

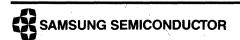
Characteristic	Symbol	Test Conditions	T <sub>a</sub> = 25°C		KS74HCTLS $T_a = -40^{\circ}C \text{ to } +85^{\circ}C$	KS54HCTLS T <sub>a</sub> = -55°C to +125°C	Unit
			Тур		Guaranteed Lim	iits	
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	٧
Maximum Low-Level Input Voltage	VIL			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V <sub>OH</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$ .	V <sub>CC</sub>	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> -0.1 3.84	V <sub>CC</sub> -0.1	v
Maximum Low-Level Output Voltage	V <sub>OL</sub>	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_{O}=20\mu A$ $I_{O}=4mA$ $I_{O}=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	٧
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND V <sub>IN</sub> =15V		±0.1	±1.0 ±10.0	±1.0 ±10.0	μΑ
Maximum Quiescent Supply Current	lcc	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.0	20.0	40.0	μΑ
Additional Worst Case Supply Current	ΔΙσο	per input pin  V <sub>I</sub> =2.4V  other Inputs: at V <sub>CC</sub> or GND  I <sub>OUT</sub> =0µA		2.7	2.9	3.0	mA

#### AC ELECTRICAL CHARACTERISTICS (Input tr, tr 66 ns), HCTLS4049, HCTLS4050

Characteristic Symbo		Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74AHCTLS $T_a = -40 ^{\circ}C \text{ to } +85 ^{\circ}C$ $V_{CC} = 5.0V \pm 10 \%$	KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	Unit
			Тур		Guaranteed	Limits	
Maximum Propagation Delay	t <sub>PLH</sub>	C <sub>L</sub> =50pF	13	17	21	26	ns
Waximum Fropagation Belay	t <sub>PHL</sub>	оц-зорі	13	17	21	26	113
Maximum Input Capacitance	CIN		5				pF
Power Dissipation Capacitance*	CPD	(per gate)					pF

<sup>\*</sup>  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

<sup>&</sup>lt;sup>†</sup> For AC switching test circuits and timing waveforms see section 2.



# ENHANCEMENT PROGRAMS 6

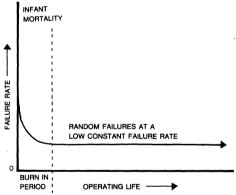


#### SAMSUNG's A + Program

The SST A+ Program has been designed to offer the customer an alternative to standard off-the-shelf plastic encapsulated CMOS circuits. The A+ Program will significantly reduce incoming inspection requirements as well as early device failures (infant mortality). These results are achieved by a tightened AQL inspection plan and a burn-in of each unit for 160 + 8, -0 hours at 125°C or equivalent conditions established from a time/temperature regression curve.

The AQL Plan. Acceptable Quality Levels (AQL) are a measure of the quality of outgoing CMOS circuits. These levels are established by the manufacturer to show the process percent defective being produced and to ensure that the customer is receiving material that meets his requirements. The SST A+ Program has tightened these AQL levels to a point at which incoming inspection by the customer is no longer a necessity. A+ product quality is monitored significantly more closely than standard product; those lots which fail the AQL level are 100% reworked before resubmission to the AQL gate.

The Reliability Plan. Reliability is the statistical probability that a product will give satisfactory performance for a specified period of time when used under specified conditions. A typical rate curve is shown below:



Reliability theory assumes that devices fail according to the above curve. When a group of devices is manufactured a small portion of the units will be inherently weaker than

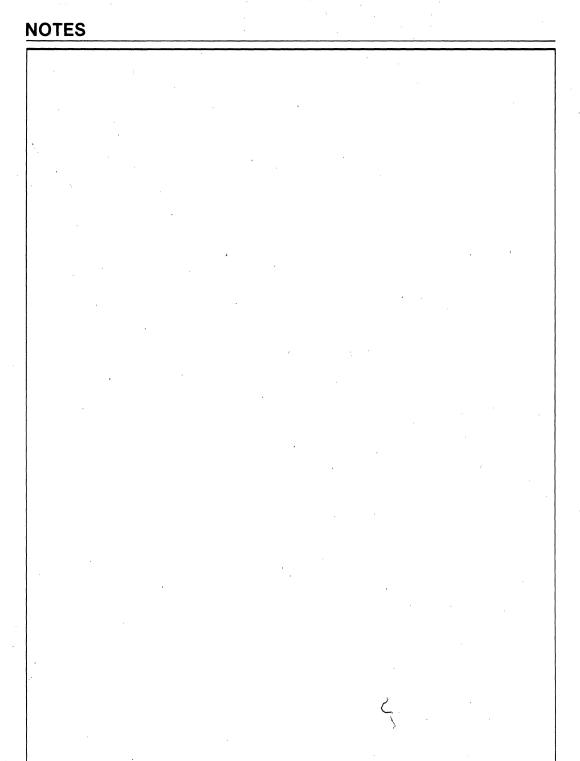
the average. These weak units will *probably* fail during the first few hours of operation—hence the term "infant mortality." If the units are burned-in however, thereby allowing the weak units to fail, there is a much lower probability that those finally put into system use will fail.

The SST A+ Flow. In order to achieve an extremely high quality unit and reduce infant mortality failures the following flow has been established:

#### **Process Flow**

DESCRIPTION
WAFER FABRICATION CMOS PROCESS CV PLOTS OXIDE AND NITRIDE THICKNESS MEASUREMENTS OPTICAL INSPECTIONS SEM ANALYSIS
ENCAPSULATION NITTO HC10 TYPE 2 EPOXY MOLDING COMPOUND ULTRA PURE FOR CMOS APPLICATIONS
POST MOLD BAKE 6 HOURS AT 175 DEG. C. CURES PLASTIC STRESSES ALL WIRE BONDS AND DIE
O/S FUNCTIONAL ELECTRICAL 100% TESTING OPENS/SHORTS AND INTERMITTENTS REMOVE
HIGH TEMPERATURE BURN-IN 160 HOURS AT 125 DEG. C. OR EQUIVALENT CONDITIONS ESTABLISHED FROM A TIME/ TEMPERATURE REGRESSION CURVE. 0.96 eV
FULL FUNCTIONAL AND PARAMETRIC ELECTRICAL TESTING 100% ELECTRICAL TESTING AC, DC 88 DEG, C.
THERMAL SHOCK MONITOR  -65 DEG. C. TO + 125 DEG. C. LIQUID TO LIQUID 5 CYCLES: SAMPLES SELECTED AT RANDOM
TIGHT AQL SAMPLING PLAN ELECTRICAL -0.05% AQL AT 88 DEG. C. MECHANICAL -0.01% AQL CRITICAL & MAJOR
SHIP UNITS



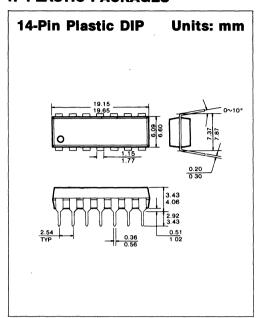


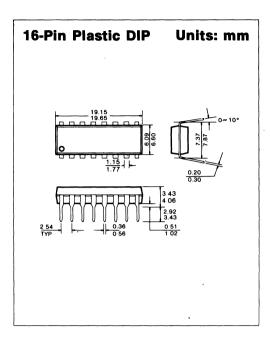
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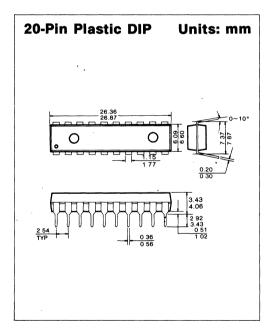


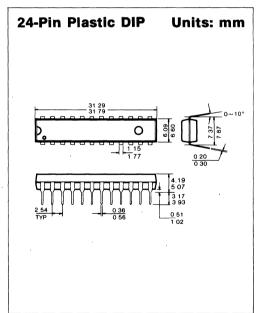
#### Z

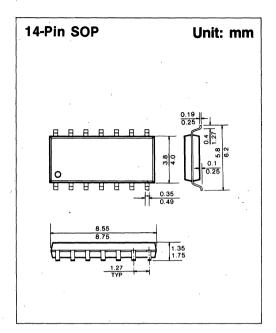
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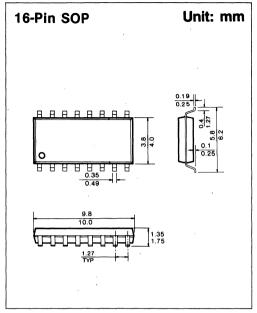


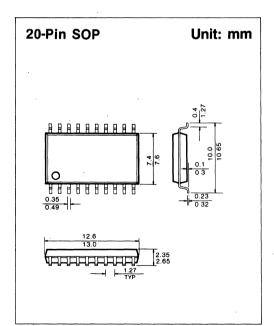


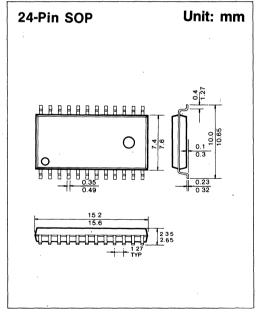




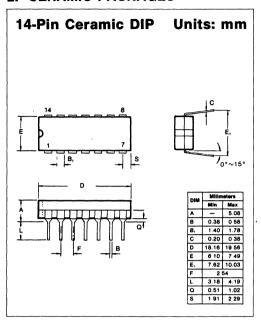


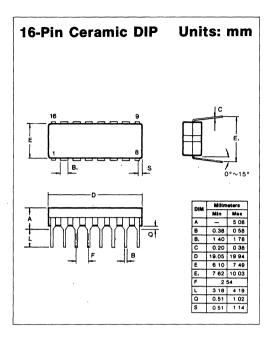


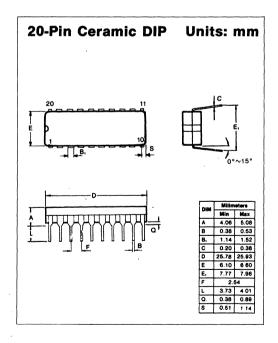


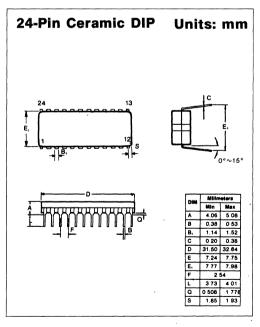


#### 2. CERAMIC PACKAGES



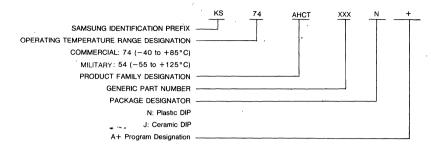




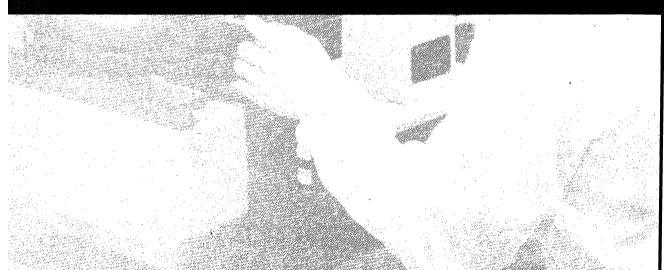


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PRINTED IN KOREA JUNE, 1988