Scenic/MX1

PCI MPEG-1 Audio/Video Decoder

Preliminary

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NOTATIONAL CONVENTIONS

The following notational conventions are used in this data book:

Signal names are shown in all uppercase letters. For example, XD.

A bar over a signal name indicates an active low signal. For example, $\overline{OE}$.

n-m indicates a bit field from bit n to bit m. For example, 7-0 specifies bits 7 through 0, inclusive.

n:m indicates a signal (pin) range from n to m. For example D[7:0] specifies data lines 7 through 0, inclusive

Use of a trailing letter H indicates a hexadecimal number. For example, 7AH is a hexadecimal number.

Use of a trailing letter b indicates a binary number. For example, 010b is a binary number.

When K or M are used, they refer to binary rather than decimal form. Thus, for example, 1 KByte would be equivalent to 1024, not 1,000 bytes.

When k is used, it refers to the decimal form. For example, 1 kbit means 1000 bits.

NOTICES

Additional information may be obtained from:

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Section 1: Introduction

The S3® Scenic/MX1™ PCI MPEG-1 audio/video decoder (hereinafter referred to as Scenic/MX1) is optimized for the PC platform. It can be used in conjunction with any S3 graphics accelerator that provides color space conversion (such as the Vision868™, Vision968™ or Trio64V+™). The other video features supported by these graphics accelerators, including video scaling, can be used to enhance the display of the MPEG-1 video decompressed by Scenic/MX1.

1.1 GENERAL CAPABILITIES

Scenic/MX1 integrates into a single device the following functions:

- MPEG-1 30 frames/second video decoding
- MPEG-1 CD-quality audio decoding
- A timer to facilitate synchronization of decoded audio and video
- A serial output port for direct connection of a low cost stereo audio D/A converter
- A PCI bus master interface to enable the Scenic/MX1 to transmit decompressed video across the PCI bus to a separate graphics subsystem for display in synchronization with the decompressed audio

Scenic/MX1 works in tandem with the host CPU and graphics accelerator to decode and display MPEG-1 video and audio:

- The host CPU is responsible for demultiplexing the MPEG-1 system stream into separate compressed video and audio data streams and for preprocessing the compressed audio data.
- Scenic/MX1 is responsible for decompressing the MPEG-1 video stream into a sequence of YUV video images and for decompressing the preprocessed audio stream into 16-bit stereo audio samples for playback. Scenic/MX1's on-chip timer enables the software driver to control the synchronization of audio and video during playback.
- The graphics accelerator is responsible for receiving the sequence of decompressed video images over the PCI bus, converting the YUV images into RGB format for display on a computer monitor, and for any additional video processing (video scaling, dithering, video effects, etc.).

1.2 PRODUCT FEATURES

Scenic/MX1's main features are listed below by functional area:

1.2.1 General Features

- MPEG-1 video and audio decompression (30 frames per second)
- Simultaneous video decompression and audio decompression
- Complete audio and video synchronization support

1.2.2 Video Features

- Decompression of "Constrained Parameter" MPEG-1 bit streams
- MPEG-1 video slow playback, fast search, fast forward, freeze frame, audio mute, single step, and random access
- MPEG-1 video error detection and resynchronization
- 4:2:2 video data format output

1.2.3 Audio Features

- Decompression of any MPEG-1 level 1 or 2 compressed audio bit stream
  - 32, 44.1 and 48 KHz sampling rates
  - 32 to 448 kbit/sec compressed bit rates
  - Single-channel, dual-channel, stereo, and joint-stereo stream decompression
- Decompressed audio is transmitted to an external stereo audio D/A converter through a serial audio port
- Audio mute and de-emphasis supported

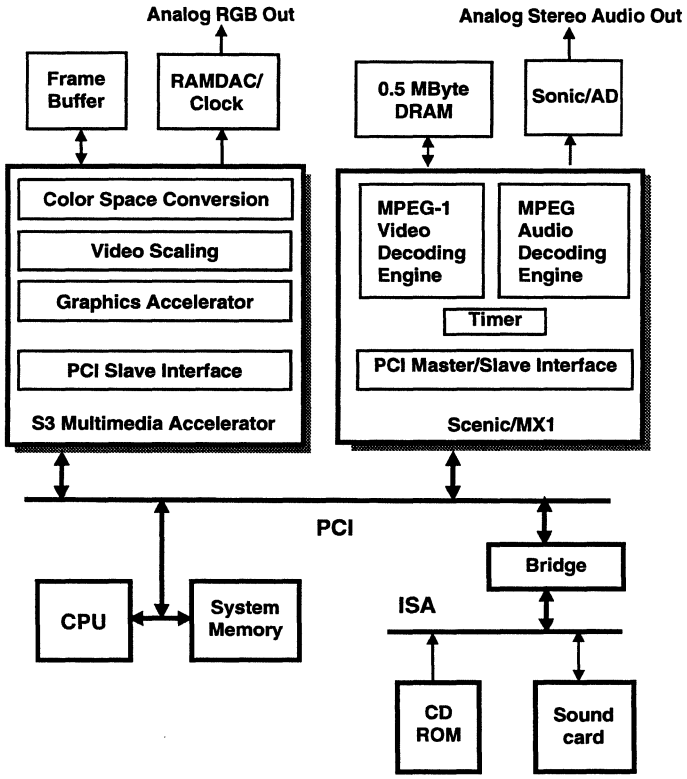

Figure 1-1. System Architecture

1.2.4 System Interface

Scenic/MX1 has three main functional interfaces:

- 16-bit page mode DRAM interface
- PCI master/slave bus interface
- Serial audio interface

1.2.5 Miscellaneous

Scenic/MX1 is available in a 128-pin plastic quad flat pack (PQFP) package.

1.3 SOFTWARE SUPPORT

S3 will provide software drivers which allow Scenic/MX1, in conjunction with the appropriate graphics accelerator, to decode MPEG-1 compressed video and/or games conforming to the following standards and APIs:

- CD- I movies ("Green Book")
- Video CD movies ("White Book")
- Microsoft Windows® 3.1 and Windows® 95 MCI MPEG API
- Open MPEG (OM/1) DOS API

Section 2: Mechanical Data

2.1 THERMAL SPECIFICATIONS

Parameter	Typ	Unit
Thermal Resistance Θ_{JC}	TBD	°C/W
Thermal Resistance Θ_{JA} (Still Air)	24.0	°C/W
Power Dissipation	2.25	W

2.2 MECHANICAL DIMENSIONS

Scenic/MX1 comes in a 128-pin PQFP package. The mechanical dimensions are given in Figure 2-1.

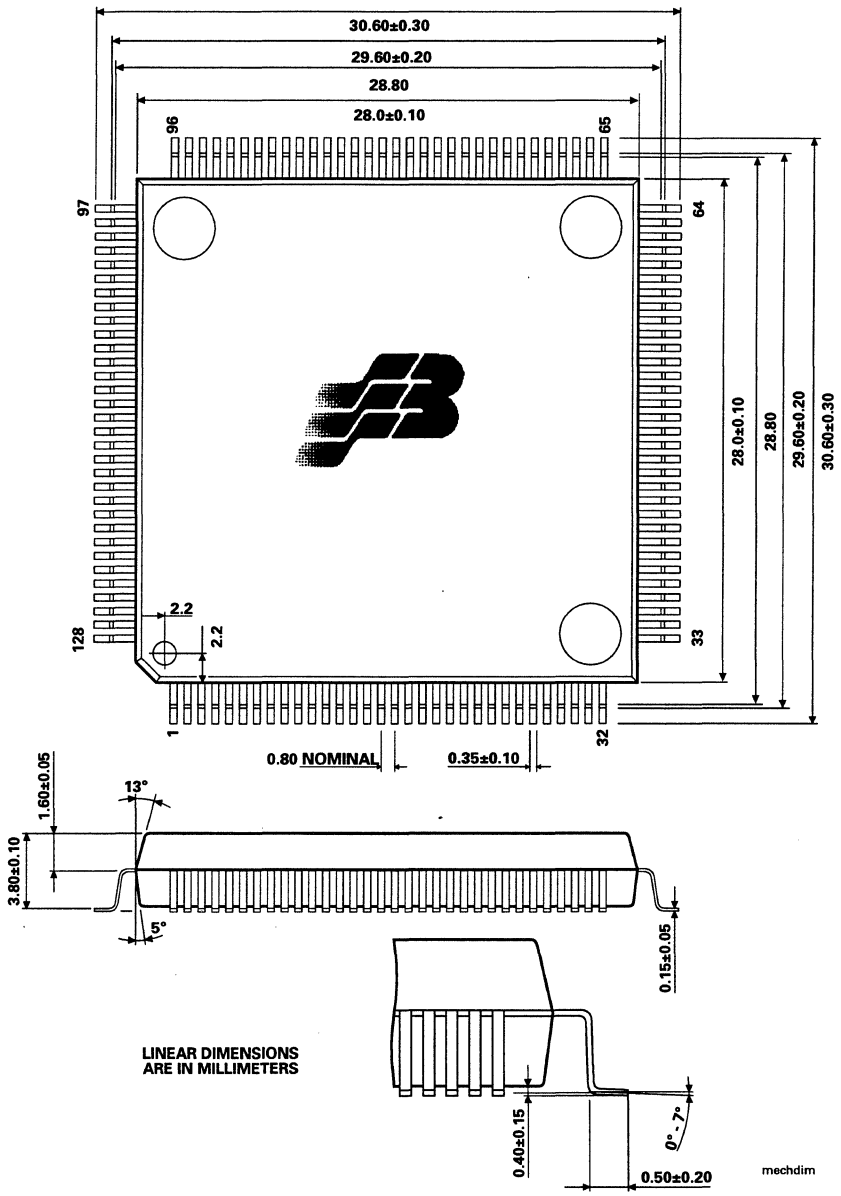

Figure 2-1. 128-pin PQFP Mechanical Dimensions

Section 3: Pin Descriptions

3.1 PINOUT DIAGRAMS

Scenic/MX1 comes in a 128-pin PQFP package. The pinout is shown in Figure 3-1. An active low pin is indicated by an overbar.

Pin layout conforms to the signal placement pinout recommendations of the PCI specification draft revision 2.1, section 4.2.6. This minimizes PCI bus-related layout issues.

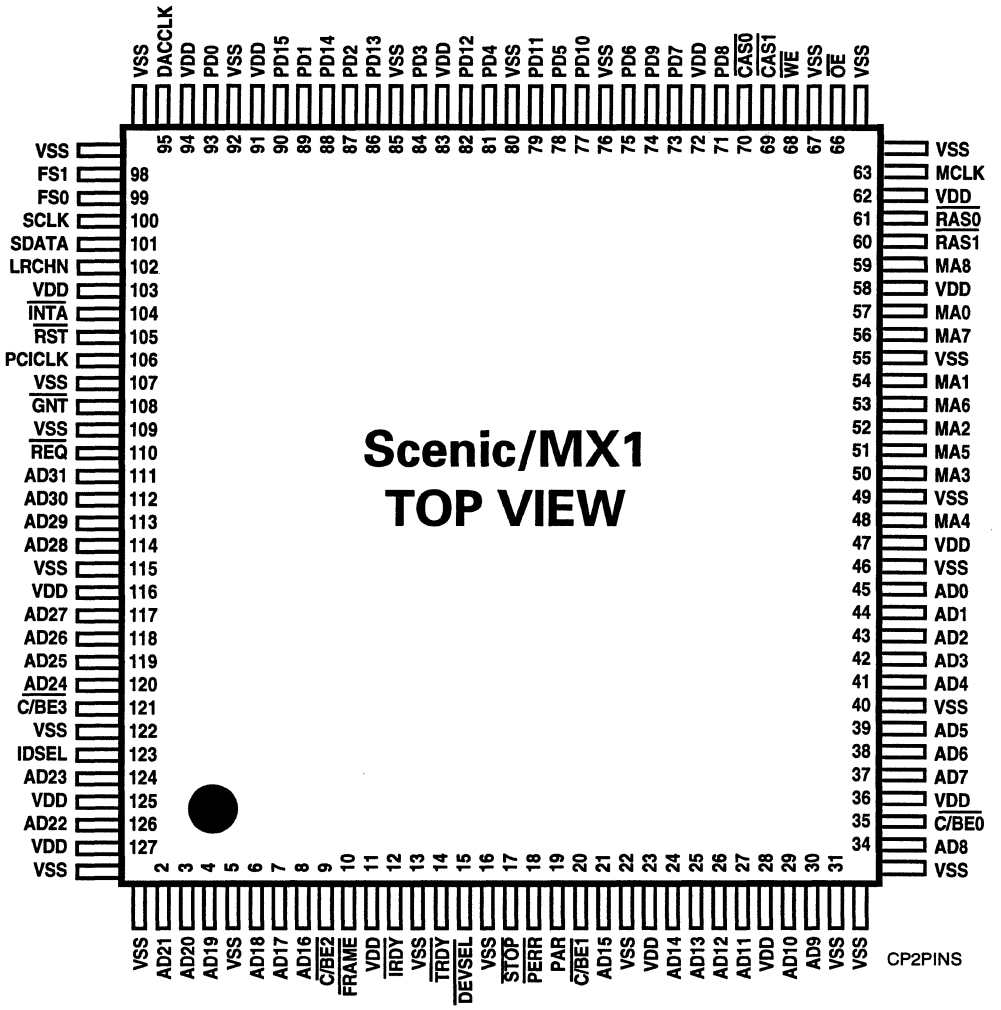

Figure 3-1. Pinout

3.2 PIN DESCRIPTIONS

The following table provides a brief description of each pin. The following definitions are used in these descriptions:

I - Input signal
O - Output signal
B - Bidirectional signal

Table 3-1. Pin Descriptions

Symbol	Type	Pin Number(s)	Description
PCI BUS INTERFACE			
Address and Data			
AD[31:0]	B	111-114,117-120, 124, 126, 2-4, 6-8, 21, 24-27, 29-30, 34, 37-39, 41-45	Multiplexed Address/Data Bus. A bus transaction (cycle) consists of an address phase followed by one or more data phases.
$\overline{C/BE[3:0]}$	B	121, 9, 20, 35	Bus Command/Data Byte Enables. These signals carry the bus command during the address phase and the byte enables during the data phase.
Bus Control			
PCICLK	I	106	PCI Bus Clock.
$\overline{INTA}$	O	104	Interrupt Request.
$\overline{IRDY}$	B	12	Initiator Ready. A bus data phase is completed when both $\overline{IRDY}$ and $\overline{TRDY}$ are asserted on the same cycle.
$\overline{TRDY}$	B	14	Target Ready. A bus data phase is completed when both $\overline{IRDY}$ and $\overline{TRDY}$ are asserted on the same cycle.
$\overline{DEVSEL}$	B	15	Device Select. The slave drives this signal active when it decodes its address as the target of the current access.
IDSEL	I	123	Initialization Device Select. This input is the chip select for Scenic/MX1 PCI configuration register reads/writes.
$\overline{RST}$	I	105	System Reset. Asserting this signal forces the Scenic/MX1 registers and state machines to a known state.
$\overline{FRAME}$	B	10	Cycle Frame. This signal is asserted by the bus master to indicate the beginning of a bus transaction.
PAR	B	19	Parity. The slave asserts this signal to verify even parity during reads.
$\overline{PERR}$	B	18	Parity Error. This signal is asserted whenever a data parity error is detected.
$\overline{STOP}$	B	17	Stop. The slave asserts this signal to indicate a target disconnect.

Table 3-1. Pin Descriptions (Continued)

Symbol	Type	Pin Number(s)	Description
$\overline{REQ}$	O	110	Request. Scenic/MX1 asserts this signal to request control of the PCI bus.
$\overline{GNT}$	I	108	Grant. Assertion of this input indicates that Scenic/MX1 has been granted control of the PCI bus.
PRIVATE MEMORY INTERFACE			
Address and Data			
PD[15:0]	B	90, 88, 86, 82, 79, 77, 74, 71, 73, 75, 78, 81, 84, 87, 89, 93	Private Memory Data Bus.
MA[8:0]	O	59, 56, 53, 51, 48, 50, 52, 54, 57	Memory Address Bus.
Memory Control			
MCLK	I	63	Memory Clock. External clock; controls data transfer rate between Scenic/MX1 and private memory.
$\overline{RAS[1:0]}$	O	60-61	Row Address Strobes.
$\overline{CAS[1:0]}$	O	69-70	Column Address Strobes.
$\overline{WE}$	O	68	Write Enable
$\overline{OE}$	O	66	Output Enable
SERIAL INTERFACE			
SCLK	O	100	Serial Clock. Sample clock for audio data.
SDATA	O	101	Serial Data. Audio data.
LRCHN	O	102	Left/Right Channel Select.
FS[1:0]	O	98-99	Frequency Select. These outputs are externally decoded to allow generation of the clock generator input that results in the desired DACCLK frequency.
DACCLK	I	95	DAC Clock. This input is generated by an external clock source and is used by Scenic/MX1 to generate the audio DAC control signals.
POWER AND GROUND			
VDD	I	11, 23, 28, 36, 47, 58, 62, 72, 83, 91, 94, 103, 116, 125, 127	Power supply
VSS	I	1, 5, 13, 16, 22, 31, 32, 33, 40, 46, 49, 55, 64, 65, 67, 76, 80, 85, 92, 96, 97, 107, 109, 115, 122, 128	Ground

3.3 PIN LISTS

Table 3-2 lists all pins alphabetically. Table 3-3 lists all pins in numerical order.

Table 3-2. Alphabetical Pin Listing

Name	Pins
AD[31:0]	111-114, 117-120, 124, 126, 2-4, 6-8, 21, 24-27, 29-30, 34, 37-39, 41-45
$\overline{\text{CAS}}$[1:0]	69-70
$\overline{\text{C/BE}}$[3:0]	121, 9, 20, 35
DACCLK	95
$\overline{\text{DEVSEL}}$	15
$\overline{\text{FRAME}}$	10
FS[1:0]	98-99
$\overline{\text{GNT}}$	108
IDSEL	123
$\overline{\text{INTA}}$	104
$\overline{\text{IRDY}}$	12
LRCHN	102
MA[8:0]	59, 56, 53, 51, 48, 50, 52, 54, 57
MCLK	63
$\overline{\text{OE}}$	66
PAR	19
PCICLK	106
PD[15:0]	90, 88, 86, 82, 79, 77, 74, 71, 73, 75, 78, 81, 84, 87, 89, 93
$\overline{\text{PERR}}$	18
$\overline{\text{RAS}}$[1:0]	60-61
$\overline{\text{REQ}}$	110
$\overline{\text{RST}}$	105
SCLK	100
SDATA	101
$\overline{\text{STOP}}$	17
$\overline{\text{TRDY}}$	14
VDD	11, 23, 28, 36, 47, 58, 62, 72, 83, 91, 94, 103, 116, 125, 127
VSS	1, 5, 13, 16, 22, 31, 32, 33, 40, 46, 49, 55, 64, 65, 67, 76, 80, 85, 92, 96, 97
	107, 109, 115, 122, 128
$\overline{\text{WE}}$	68

Table 3-3. Numerical Pin Listing

Pin #	Name
1	**VSS**
2	AD21
3	AD20
4	AD19
5	**VSS**
6	AD18
7	AD17
8	AD16
9	C/BE2
10	FRAME
11	**VDD**
12	IRDY
13	**VSS**
14	TRDY
15	DEVSEL
16	**VSS**
17	STOP
18	PERR
19	PAR
20	C/BE1
21	AD15
22	**VSS**
23	**VDD**
24	AD14
25	AD13
26	AD12
27	AD11
28	**VDD**
29	AD10
30	AD9
31	**VSS**
32	**VSS**
33	**VSS**
34	AD8
35	C/BE0
36	**VDD**
37	AD7
38	AD6
39	AD5
40	**VSS**

Pin #	Name
41	AD4
42	AD3
43	AD2
44	AD1
45	AD0
46	**VSS**
47	**VDD**
48	MA4
49	**VSS**
50	MA3
51	MA5
52	MA2
53	MA6
54	MA1
55	**VSS**
56	MA7
57	MA0
58	**VDD**
59	MA8
60	RAS1
61	RAS0
62	**VDD**
63	MCLK
64	**VSS**
65	**VSS**
66	OE
67	**VSS**
68	WE
69	CAS1
70	CAS0
71	PD8
72	**VDD**
73	PD7
74	PD9
75	PD6
76	**VSS**
77	PD10
78	PD5
79	PD11
80	**VSS**

Table 3-3. Numerical Pin Listing (Continued)

Pin #	Name
81	PD4
82	PD12
83	**VDD**
84	PD3
85	**VSS**
86	PD13
87	PD2
88	PD14
89	PD1
90	PD15
91	**VDD**
92	**VSS**
93	PD0
94	**VDD**
95	DACCLK
96	**VSS**
97	**VSS**
98	FS1
99	FS0
100	SCLK
101	SDATA
102	LRCHN
103	**VDD**
104	$\overline{\text{INTA}}$
105	$\overline{\text{RST}}$
106	PCICLK
107	**VSS**
108	$\overline{\text{GNT}}$
109	**VSS**
110	$\overline{\text{REQ}}$
111	AD31
112	AD30
113	AD29
114	AD28
115	**VSS**
116	**VDD**
117	AD27
118	AD26
119	AD25

Pin #	Name
120	AD24
121	$\overline{\text{C/BE3}}$
122	**VSS**
123	IDSEL
124	AD23
125	**VDD**
126	AD22
127	**VDD**
128	**VSS**

Section 4: Electrical Data

4.1 MAXIMUM RATINGS

Table 4-1. Absolute Maximum Ratings

Ambient temperature	0° C to 70° C
Storage temperature	-40° C to 125° C
DC Supply Voltage	-0.5V to 7.0V
I/O Pin Voltage with respect to V_{SS}	-0.5V to V_{DD}+0.5V

4.2 DC SPECIFICATIONS

Table 4-2. DC Specifications (VDD = 5V ± 5%)

Symbol	Parameter	Min	Max	Unit
V_{IL}	Input Low Voltage		0.8	V
V_{IH}	Input High Voltage	2.0		V
V_{OL}	Output Low Voltage		V_{SS} + 0.4	V
V_{OH}	Output High Voltage	2.4		V
I_{OZ}	Output Tri-state Current		1	µA
C_{IN}	Input Capacitance		TBD	pF
C_{OUT}	Output Capacitance		TBD	pF
I_{CC}	Power Supply Current		TBD	mA

4.3 AC SPECIFICATIONS

TBD

Section 5: Reset and Initialization

The $\overline{RST}$ signal resets Scenic/MX1's internal state machines and places all registers in their power-on default states. It also initiates several configuration actions, as described in this section.

5.1 CONFIGURATION STRAPPING

Certain Scenic/MX1 configuration information, as detailed in this section, is set by hardware strapping. The PD[15:0] pins can be individually pulled either high or low through 47 KΩ resistors. These pull-ups and pull-downs do not affect normal operation of the pins as part of the private memory data bus, but force the pins to a defined state during reset. Scenic/MX1 samples this state at the rising edge of the reset signal and loads the data into register bits as noted in Table 5-1 and Section 10.

Table 5-1. Definition of PD[15:0} at the Rising Edge of the Reset Signal

Register Number	Bit(s)	PD Pins	Value	Function
		15		Reserved for future use
	SCLK Inverted			
R0300	22	14	0	Data latched on rising edge of SCLK
			1	Data latched on falling edge of SCLK
	Audio DAC Absent			
R0300	21	13	0	Audio DAC present
			1	Audio DAC absent
	Audio Data Bit Order			
R0300	20	12	0	Audio data bit 0 first
			1	Audio data bit 15 first
	Lag Time			
R0300	19	11	0	First 16 bits latched on an LRCHN phase
			1	Last 16 bits latched on an LRCHN phase

Table 5-1. Definition of PD[15:0} at the Rising Edge of the Reset Signal (Continued)

Register Number	Bit(s)	PD Pins	Value	Function
	SCLK and LRCHN Definition			
R0300	14 - 12	[10:8]	000	256 DAC clocks per LRCHN, 2 DAC clocks per SCLK
			001	256 DAC clocks per LRCHN, 4 DAC clocks per SCLK
			010	384 DAC clocks per LRCHN, 2 DAC clocks per SCLK
			011	384 DAC clocks per LRCHN, 4 DAC clocks per SCLK
			100	384 DAC clocks per LRCHN, 6 DAC clocks per SCLK
			101	384 DAC clocks per LRCHN, 8 DAC clocks per SCLK
			110	512 DAC clocks per LRCHN, 4 DAC clocks per SCLK
			111	512 DAC clocks per LRCHN, 8 DAC clocks per SCLK
	LRCHN Channel Interpretation			
R0300	11	7	0	LRCHN active high left channel
			1	LRCHN active high right channel
	$\overline{\text{RAS}}$ Length Select			
R0230	6	6	See Tables 5-2 and 5-3	This bit together with bits 5-4 sets $\overline{\text{RAS}}$ Precharge value - see Table 5-2 for details. Also, this bit together with bits 3-2 sets $\overline{\text{RAS}}$ Pulse width - see Table 5-3.
	$\overline{\text{RAS}}$ Precharge			
R0230	5 - 4	[5:4]	See Table 5-2	These bits together with bit 6 set the $\overline{\text{RAS}}$ Precharge Length
	$\overline{\text{RAS}}$ Pulse Width			
R0230	3 - 2	[3:2]	See Table 5-3	These bits together with bit 6 set the $\overline{\text{RAS}}$ Pulse Width
	$\overline{\text{CAS}}$/$\overline{\text{OE}}$/$\overline{\text{WE}}$ Stretch			
R0230	1 - 0	[1:0]	00	6.5 ns (nominal)
			01	5.0 ns (nominal)
			10	3.5 ns (nominal)
			11	0 ns - no stretch

Table 5-2. Setting RAS Precharge Length

R0230 bits 5-4 (default is the value strapped on PD[5:4])	R0230 bit 6 value: $\overline{RAS}$ Length Select	Resulting $\overline{RAS}$ Precharge length used
00	0	4 MCLKs
00	1	4.5 MCLKs
01	0	3 MCLKs
01	1	3.5 MCLKs
10	0	2 MCLKs
10	1	2.5 MCLKs
11	0	reserved
11	1	reserved

Table 5-3. Setting RAS Pulse Width

R0230 bits 3-2 value (default is the value strapped on PD[3:2])	R0230 bit 6 value: $\overline{RAS}$ Length Select	Resulting $\overline{RAS}$ Pulse Width used
00	0	7 MCLKs
00	1	6.5 MCLKs
01	0	6 MCLKs
01	1	5.5 MCLKs
10	0	5 MCLKs
10	1	4.5 MCLKs
11	0	4 MCLKs
11	1	3.5 MCLKs

5.2 RESET BEHAVIOR

5.2.1 Hardware Reset

Hardware reset occurs when the PCI reset signal is asserted. Upon a hardware reset, these actions occur:

- All Scenic/MX1 internal operations are halted and the chip modules enter an idle state
- All internal control and configuration registers assume their default values as specified in Sections 9 and 10
- The memory control pins $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, and $\overline{OE}$ go high and the strappings on the PD pins are read
- The SP module stops driving the audio DAC

5.2.2 Soft Reset

Soft reset occurs when software sets a control bit in the MIU register. Upon a soft reset, these actions occur:

- All actions as noted for Hardware Reset, except that PCI configuration registers are not altered.

Section 6: Hardware Interfaces

Scenic/MX1 has three main interfaces: to the PCI bus, to local memory, and to an audio DAC. This section describes the interfaces, their functional characteristics, and related information.

6.1 PCI BUS INTERFACE

Scenic/MX1 provides a complete PCI interface and does not require 'glue' logic. The pinout and other specifications are in conformance with Revision 2.1 of the PCI specification.

6.1.1 PCI Configuration

The Vendor ID register (Index 00H) in the PCI Configuration space is hardwired to 5333H to specify S3 Incorporated as the vendor. The Device ID register is hardwired to 8820H to specify the Scenic/MX1. Additional values are hardwired as defined in the register descriptions in Section 9 of this manual.

6.1.2 PCI Bus Cycles

Figures 6-1 and 6-2 show the basic PCI read and write cycles respectively. Bit 1 of the PCI Command register (Index 04H) must be set to 1 to allow memory and register access.

Figures 6-3 and 6-4 show two examples of PCI bus disconnection. These examples show cases where data is transferred after $\overline{\text{STOP}}$ is asserted. In example A, data is transferred after $\overline{\text{FRAME}}$ is deasserted because the master was not ready ($\overline{\text{IRDY}}$ deasserted on clock 2). In example B, data is transferred before $\overline{\text{FRAME}}$ is deasserted. See the *PCI Local Bus Specification* for a complete explanation of disconnects.

The PCI configuration register space occupies 256 bytes. When a configuration read or write command is issued, the AD[7:0] lines contain the address of the register in this space to be accessed. Figures 6-5 and 6-6 show the configuration read and write cycles respectively.

Scenic/MX1 drives even parity information onto the PAR line during read transactions. This operation is depicted in Figure 6-7.

Scenic/MX1 also provides PCI bus mastering capabilities according to specifications given in the *PCI Local Bus Specification*. Behavior of arbitration pins $\overline{\text{REQ}}$ and $\overline{\text{GNT}}$ is in accordance with sections 2.2.4 and also 3.4 of that document. Behavior of the $\overline{\text{STOP}}$ pin is in accordance with section 3.3.3.2, *Target Initiated Termination*. Behavior of the $\overline{\text{PERR}}$ signal is in accordance with the PCI specification.

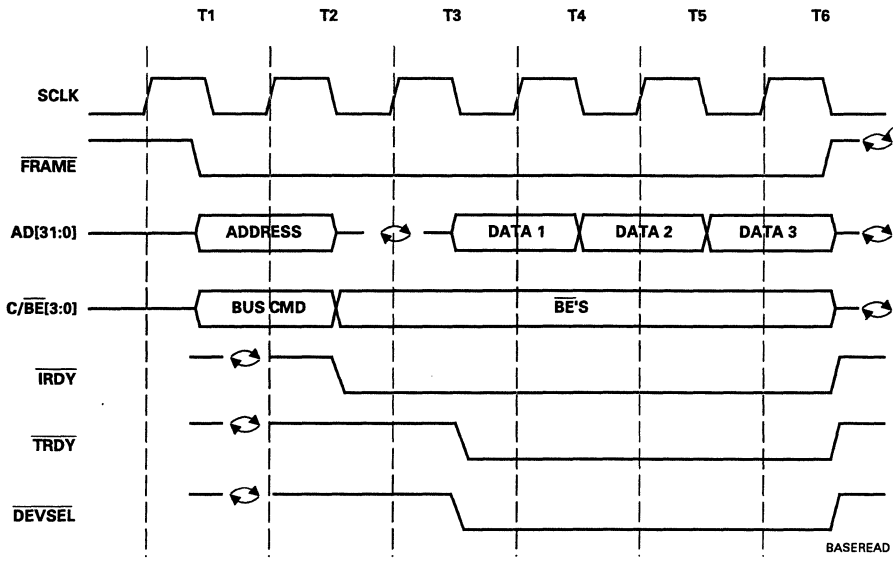

Figure 6-1. Basic PCI Read Cycle

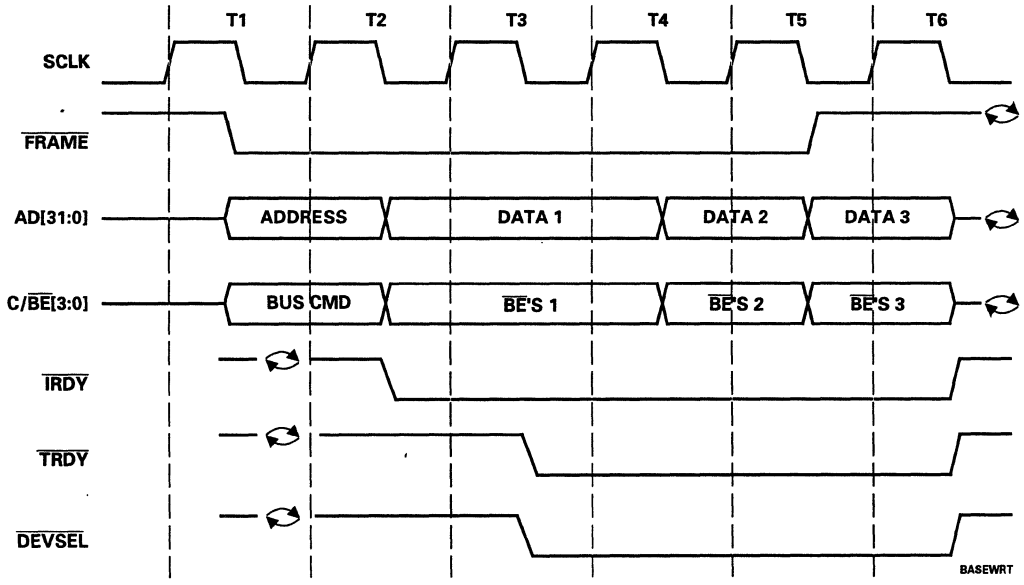

Figure 6-2. Basic PCI Write Cycle

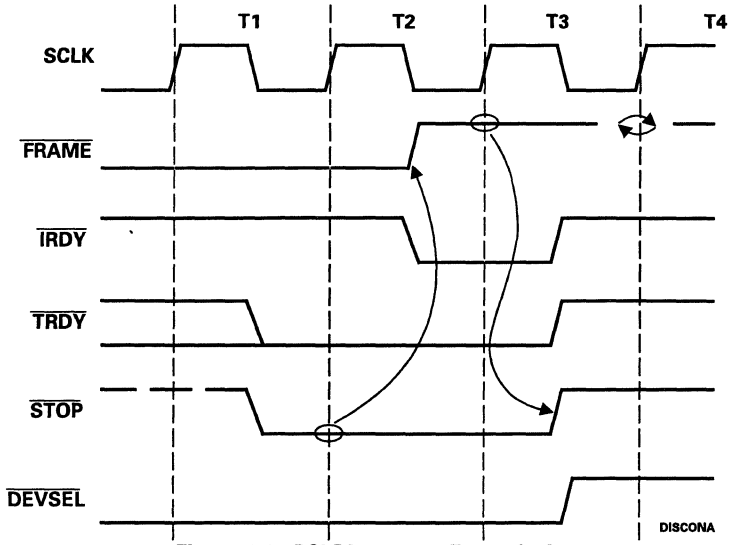

Figure 6-3. PCI Disconnect Example A

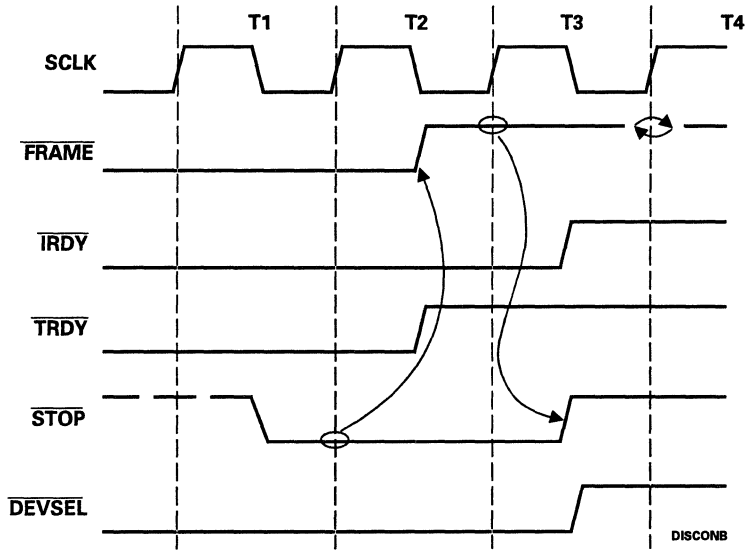

Figure 6-4. PCI Disconnect Example B

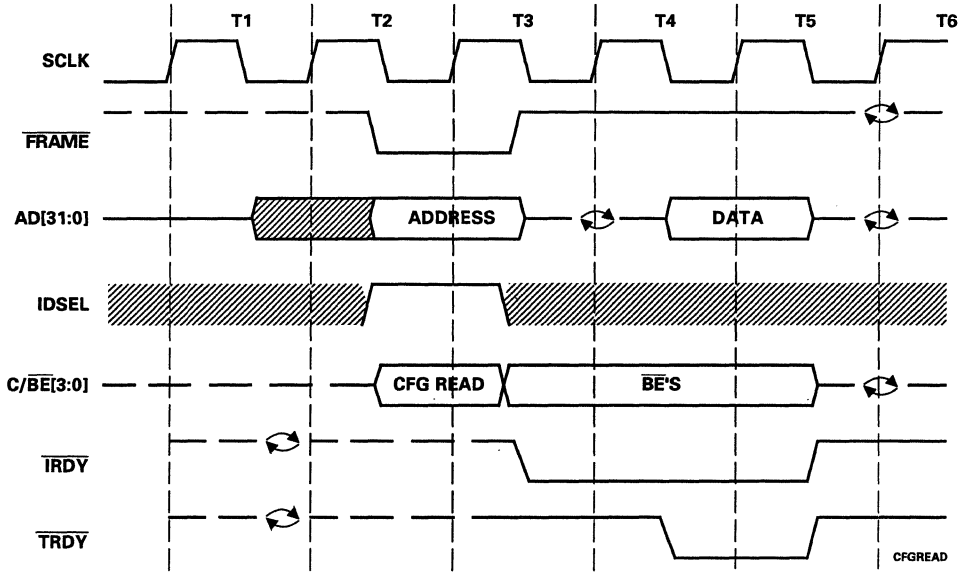

Figure 6-5. PCI Configuration Read Cycle

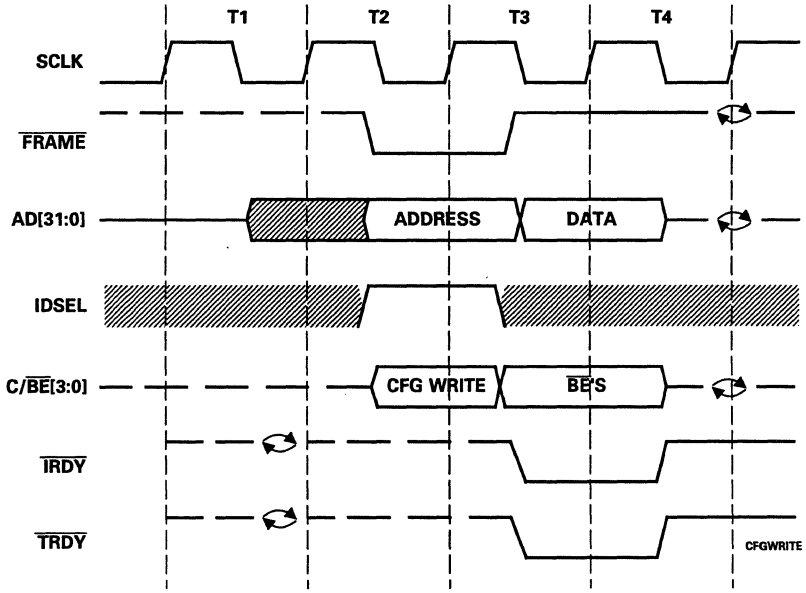

Figure 6-6. PCI Configuration Write Cycle

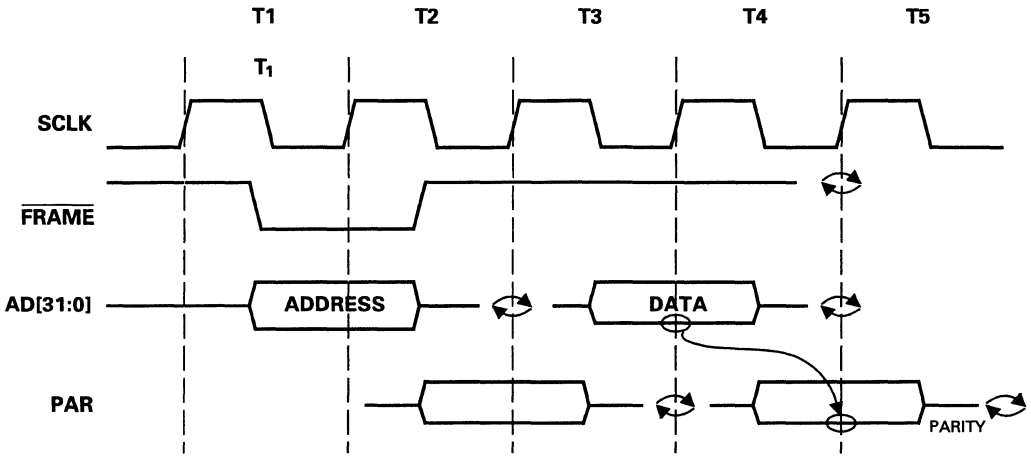

Figure 6-7. Read Parity Operation

6.2 LOCAL MEMORY INTERFACE

Scenic/MX1 can use either 512 KBytes or 1 MByte of fast page mode 256Kx16 DRAMs. The memory interface operates at the system clock frequency of 40 MHz, allowing use of inexpensive DRAMs. Scenic/MX1 contains all necessary interface and refresh circuitry for these DRAMs.

6.2.1 Memory Configurations

Figure 6-8 shows a 0.5 MByte configuration using a 256Kx16 DRAM. $\overline{RAS0}$ selects the first 512K; when an additional 0.5 MByte is used, $\overline{RAS1}$ selects the second 512K.

In general, 512 KBytes is sufficient for decoding most MPEG-1 data streams. 1 MBytes is required for decoding streams such as Green Book encoded PAL video, and larger memory may also improve performance in some systems by reducing interrupt service requests to the host CPU.

6.2.2 Memory Functional Timing

Figure 6-9 shows the functional timing for a fast page mode read cycle, and Figure 6-10 shows fast page mode write cycle timing. These diagrams also show how certain parameters for various control signals can be adjusted to meet the access time requirements of a variety of DRAMs.

6.3 SERIAL AUDIO INTERFACE

Scenic/MX1's programmable serial audio interface is designed to interface to a variety of audio DACs with few or no additional parts. When the S3 Sonic/AD™ audio DAC is used, as shown in Figure 6-11, no glue logic is required. A design using the Sonic/AD requires only a clock crystal plus a small number of analog discretes to implement the low-pass filters required on the analog outputs.

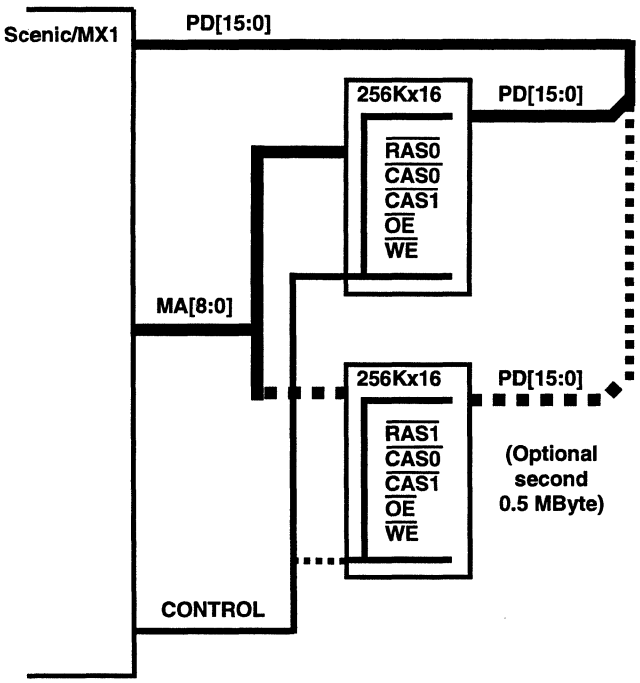

Figure 6-8. 256Kx16 DRAM Configuration

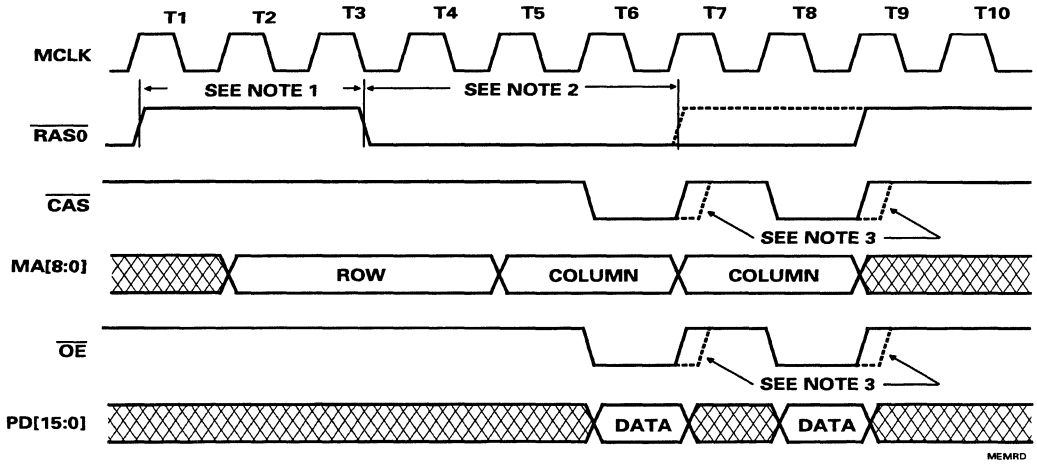

Figure 6-9. Fast Page Mode Read Cycle

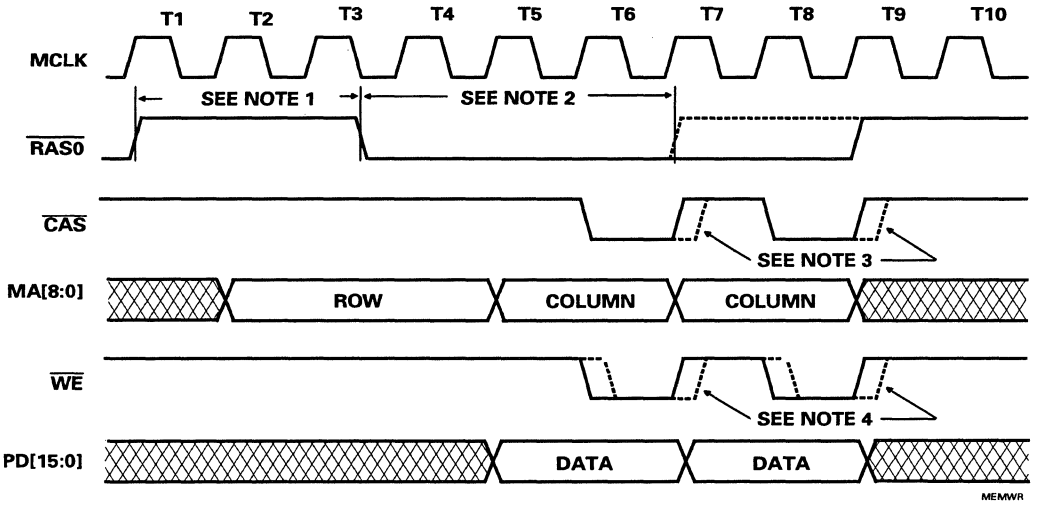

Figure 6-10. Fast Page Mode Write Cycle

Notes

1. The minimum $\overline{RAS}$ Precharge time can be adjusted using register R0230 bits 5-4.
2. The minimum $\overline{RAS}$ Pulse Width can be set using register R0230 bits 3-2.
3. The $\overline{CAS}$ and $\overline{WE}$ low times can be adjusted using register R0230 bits 1-0.

Functional timing for the audio DAC interface is shown in Figures 6-12 and 6-13.

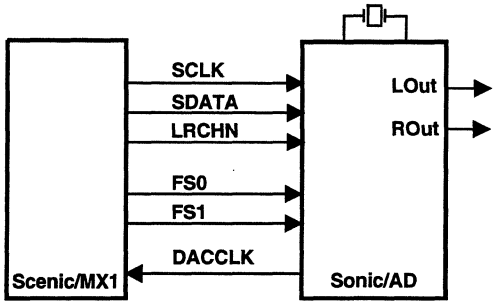

Figure 6-11. Sonic/AD Interface

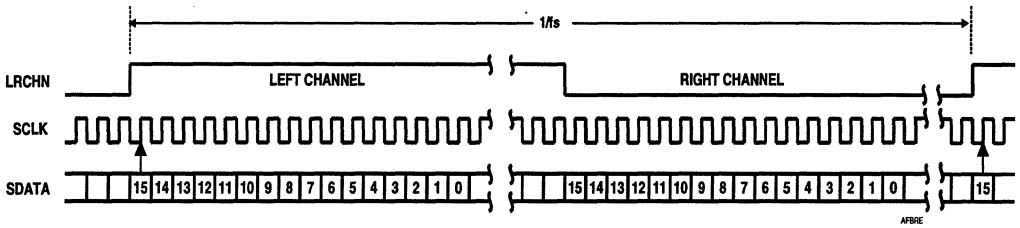

Figure 6-12. First Audio Bits Latched on Rising Edge

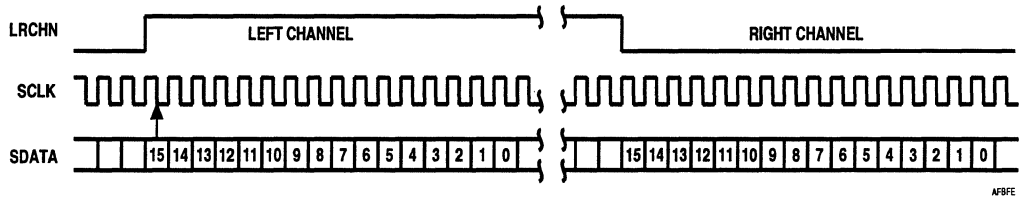

Figure 6-13. First Audio Bits Latched on Rising Edge

Section 7: Functional Description

7.1 OVERVIEW

This section provides a high level description of Scenic/MX1 operation and system data flow.

MPEG is described by the ISO/IEC document IS11172. An MPEG-encoded system stream contains a video stream and one or more audio streams, and optionally may also have private data streams. In a Scenic/MX1 application, the host acts as a front end preprocessor, separating the video and audio streams, which it then routes to Scenic/MX1. The host processor provides high level data flow control and sets control parameters for Scenic/MX1.

Scenic/MX1 provides dedicated stream-decoding and its decompression engines return decoded video data and decoded audio data. The hardware engines provide video and audio decompression, transfer data using PCI bus mastering, manage private data buffers kept in local memory, and output decoded digital audio to an external audio DAC.

The primary functions of Scenic/MX1 are:

- Decoding MPEG1 video and audio streams sent to it on the PCI bus by a host processor
- Returning a stream of decompressed video data
- Providing decompressed audio data output

These processes are shown in the context of system data flow in Figures 7-1 and 7-2.

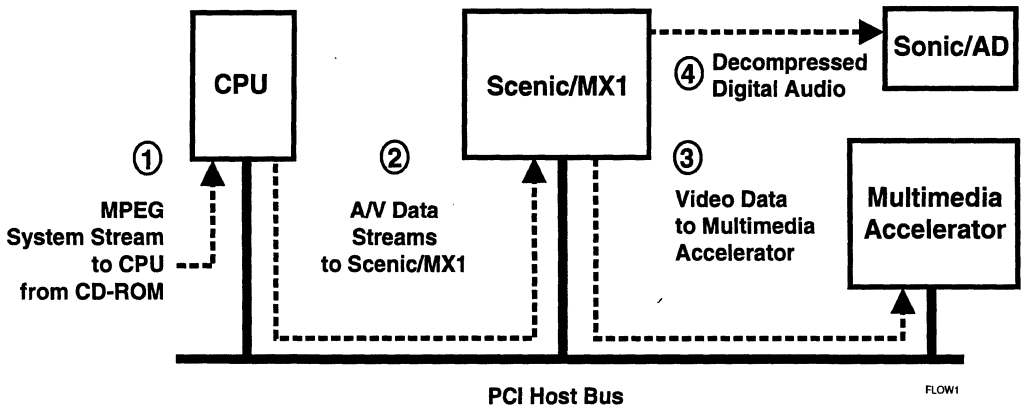

Figure 7-1. Data Flow with Multimedia Accelerator

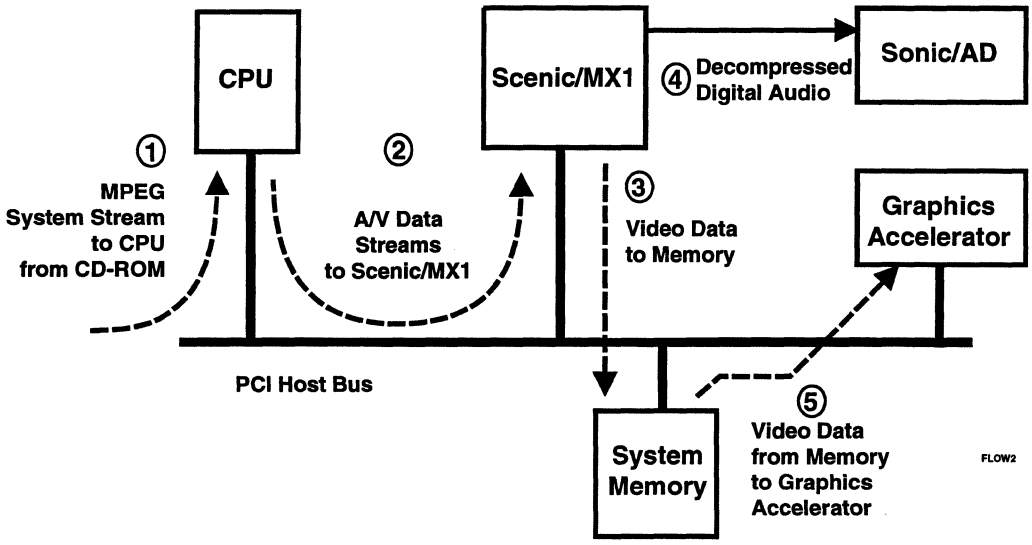

Figure 7-2. Data Flow with Graphics Accelerator

The overall hierarchy of system-level control is shown in Figure 7-3. The application accesses Scenic/MX1 through the application interface level, using Windows- or DOS-compatible calls. These are interpreted by Scenic/MX1 driver software, which commands and controls Scenic/MX1.

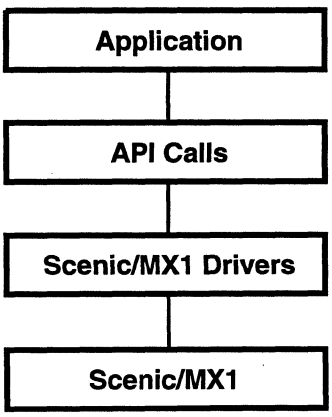

Figure 7-3. Control Hierarchy

7.2 Scenic/MX1 FUNCTIONAL PARTITIONING

Figure 7-3 shows the main functional modules within Scenic/MX1 together with the related external components. The functions of these modules are described in the following sections.

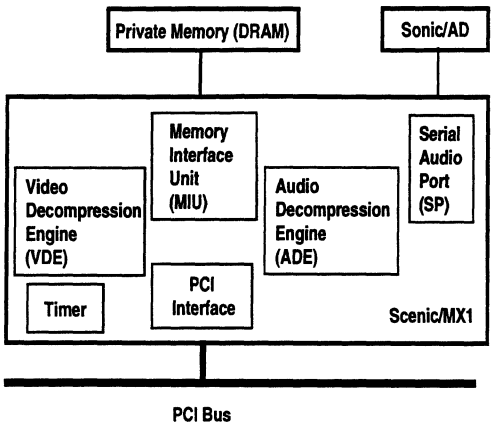

Figure 7-4. Scenic/MX1 Block Diagram

7.3 VIDEO DECOMPRESSION ENGINE (VDE)

The Video Decompression Engine:

- Accepts input streams of MPEG compressed video data
- Outputs decompressed video data

7.4 AUDIO DECOMPRESSION ENGINE (ADE)

The Audio Decoding Engine:

- Accepts input streams of MPEG compressed audio data
- Outputs decompressed audio data

7.5 MEMORY INTERFACE UNIT (MIU)

The Memory Interface Unit:

- Controls buffers in private memory (local DRAM)
- Manages DMA access to/from private memory
- Provides DRAM refresh control
- Performs arbitration of memory access by all Scenic/MX1 functional modules

Scenic/MX1 uses external dedicated DRAM for data buffers. It needs only 0.5 MByte DRAM for data storage when decoding most MPEG-1 bit streams, but has provision for using 1.0 MByte (2 DRAMs). The memory size supported is 256Kx16.

7.6 PCI INTERFACE (PCI)

- Manages all transactions across the PCI Local Bus
- Provides PCI Bus Mastering for data transfers

Scenic/MX1 contains a PCI bus interface. It handles data transfers in and out of Scenic/MX1 across the bus, and is a PCI bus master.

7.7 SERIAL AUDIO PORT (SP)

- Provides digital stereo audio interface to an external audio DAC
- Accepts DACCLK timing from the audio DAC
- Compatible with I^2S standard

7.8 TIMER

The on-chip timer enables the software driver to control the synchronization of audio and video during playback.

Section 8: Software Driver

This section provides a description of the functions supported by the driver software for the Scenic/MX1.

The Scenic/MX1 drivers will support two standard MPEG software interfaces: the Microsoft Windows 3.1 and Windows 95 MCI MPEG interface, and the Open MPEG (OM/1) DOS API.

8.1 FUNCTIONS SUPPORTED BY DRIVER SOFTWARE

Table 8-1 identifies low-level Scenic/MX1 functions supported by Scenic/MX1 software drivers.

Close	Closes Scenic/MX1 as a device; mutes the audio output
Get	Returns driver settings
Open	Opens and initializes Scenic/MX1 as a device
Pause	Pauses playing
Seek	Puts output in pause mode, seeks required place in data source
Set	Puts system information into system memory and sets Scenic/MX1 configuration
Step	Multiple types of stepping supported
Freeze	Freezes last displayed frame and continues outputting audio
Unfreeze	Resumes playing after a freeze
Play	Play MPEG video and audio

8.2 DRIVER MEMORY ACCESS

The Scenic/MX1 driver does not use the first 2 KBytes of private memory. This area is reserved and should not be accessed by other software.

Section 9: PCI Configuration Register Descriptions

The PCI specification defines a Configuration Register space containing a standard set of registers that allow device relocation, device independent system address map construction and automatic configurations. Scenic/MX1 provides a subset of these registers.

Scenic/MX1 also contains additional registers for flow-control specific to Scenic/MX1 MPEG data operations across the PCI bus. For information on these registers which lie in Scenic/MX1 PCI module space, see Section 10.

The PCI configuration register space occupies 256 bytes. When a configuration read or write command is issued, the AD[7:0] lines contain the address of the register to be accessed in this space. Scenic/MX1 supports the registers within this space listed in Table 9-1 or returns a value of zero upon a read if no register is present.

In the register descriptions, 'R' stands for reserved (a reserved bit's read value is undefined unless noted, and you may write only zero to a reserved bit).

Table 9-1. PCI Configuration Space Registers

DeviceID = 8820H		VendorID = 5333H		00H
PCI Status		PCI Command		04H
ClassCode = 040000H			01H	08H
00H		Latency Timer	00H	0CH
BaseAddr1 (sets base for access to Scenic/MX1 Control and Status registers)				10H
BaseAddr2 (sets base for access to Scenic/MX1 private memory)				14H
(Not implemented - returns 0000 0000H)				18H
(Not implemented - returns 0000 0000H)				1CH
(Not implemented - returns 0000 0000H)				20H
(Not implemented - returns 0000 0000H)				24H
(Not implemented - returns 0000 0000H)				28H
(Not implemented - returns 0000 0000H)				2CH
(Not implemented - returns 0000 0000H)				30H
(Not implemented - returns 0000 0000H)				34H
(Not implemented - returns 0000 0000H)				38H
MaxLat = 10H	MinGnt - 05H	IntrPin = 01H	IntrLine	3CH
Master Timeout	Target Timeout	Memory Timeout	Reserved	40H

Vendor ID

Read Only Address: 00H
Power-On Default: 5333H

This read-only register identifies the device manufacturer.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Vendor ID															

Bits 15–0 Vendor ID
This is hardwired to 5333H to identify S3 Incorporated.

Device ID

Read Only Address: 02H
Power-On Default: 8820H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Device ID															

Bits 15–0 Device ID
This is hardwired to 8820H to identify Scenic/MX1.

Command

Read/write Address: 04H
Power-On Default: 0000H

This register controls which types of PCI cycles Scenic/MX1 can generate and respond to. Bits with functions defined by the PCI specification but not supported by Scenic/MX1 are shown as reserved.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R =0	R =0	R =0	R =0	R =0	R =0	R =0	R =0	R =0	PER	R =0	MWI EN	R =0	BM EN	MS EN	R =0

Bit 0 Reserved

Bit 1 MS EN - Memory Space Accesses
This bit controls Scenic/MX1's response to memory space accesses.
0 = Disable Scenic/MX1 response to memory space accesses
1 = Enable response to memory space accesses

Bit 2 BM EN- Bus Master Enable
This bit controls Scenic/MX1's ability to act as a master on the PCI bus.
0 = Disables Scenic/MX1 as a bus master
1 = Enables Scenic/MX1 as a bus master

Bit 3 Reserved

Bit 4 MWI EN - Memory Write and Invalidate Enable
0 = Disable use of Memory Write and Invalidate command
1 = Enables use of Memory Write and Invalidate command

Bit 5 Reserved

Bit 6 PER - Parity Error Response
0 = Scenic/MX1 does not respond to parity errors
1 = Scenic/MX1 responds to parity errors

Bits 15-7 Reserved.

Status

See bit descriptions Address: 06H
Power-On Default: 0200H

Bits with functions defined by the PCI specification but not supported by Scenic/MX1 are shown as reserved.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	R				DEVSEL			R	R	R	R	R	R	R	R
APE	=0	RMA	RTA	STA	=01		PE	=0	=0	=0	=0	=0	=0	=0	=0

Bits 7–0 Reserved

Bit 8 PE - Parity Error
0 = PERR not asserted
1 = PERR asserted

Bits 10–9 DEVSEL - Device Select Timing
These bits are hardwired to value of 01 - Medium DEVSEL timing.

Bit 11 STA = Signaled Target Abort
0 = Scenic/MX1 has not terminated a transaction as a target
1 = Scenic/MX1 has terminated a transaction as a target

Bit 12 RTA - Received Target Abort
0 = Transaction not terminated by target abort
1 = Transaction terminated by target abort

Bit 13 RMA - Received Master Abort
0 = Transaction not terminated by master abort
1 = Transaction terminated by master abort

Bit 14 Reserved

Bit 15 APE - Address Parity Error
0 = Parity error not detected in AD or C/BE lines
1 = Parity error detected in AD or C/BE lines

Class Code

Read Only Address: 08H
Power-On Default: 0480 0000H

This register is hardwired to 0480 0000H to specify that Scenic/MX1 is an "other multimedia device".

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROGRAMMING INTERFACE								REVISION ID							
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASE CLASS CODE								SUB-CLASS							

Latency Timer

Read/Write Address: 0DH
Power-On Default: 0000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BM LATENCY TIMER					0	0	0	R	R	R	R	R	R	R	R

Bits 7–0 Reserved

Bits 10–8 Reserved = 0

These are the 3 lsb's of the latency timer value, providing 8 clocks granularity.

Bits 15–11 BM LATENCY TIMER - Bus Master Latency Timer

Value = number of PCI clocks Scenic/MX1 can keep its bus master grant without having it removed

These are the 5 msb's of this value. The three lsb's are 000b. This value is normally programmed by the system BIOS based in part on the requested value in bits 15-8 of 3EH.

Base Address 1

Read/Write Address: 12H (high) 10H (low)
Power-On Default: 0000 0000H

This is a 32-bit register in PCI configuration space that provides for address relocation. This is the base address for Scenic/MX1 control registers.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BASE ADDRESS 1					R	R	R	R	R	R	R	PREF = 0	TYPE =00		MSI = 0
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASE ADDRESS 1															

Bit 0 MSI - Memory Space Indicator
0 = Base registers map into memory space (hardwired)

Bits 2–1 TYPE - Type of Address Relocation
00 = Locate anywhere in 32-bit address space (hardwired)

Bit 3 PREF - Prefetchable
0 = Does not meet the prefetchable requirements (hardwired)

Bits 10–4 Reserved

Bits 31–11 BASE ADDRESS 1
These are the upper bits of the base address used to access Scenic/MX1 control registers. The low order bits of Scenic/MX1 register address must contain the offset value comprised of the register module number together with the register index within the module, as shown in Section 10. The control register space occupies 2 KBytes of space.

Base Address 2

Read/Write Address: 16H (high) 14H (low)
Power-On Default: 0000 0000H

This is a 32-bit register in PCI configuration space that provides for address relocation. This is the base address for Scenic/MX1 local memory.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R	R	R	R	R	PREF = 0	TYPE =00		MSI = 0
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASE ADDRESS 2												R	R	R	R

Bit 0 MSI - Memory Space Indicator
0 = Base registers map into memory space (hardwired)

Bits 2–1 TYPE - Type of Address Relocation
00 = Locate anywhere in 32-bit address space (hardwired)

Bit 3 PREF - Prefetchable
0 = Does not meet the prefetchable requirements (hardwired)

Bits 10–4 Reserved

Bits 31–11 BASE ADDRESS 2

These are the upper bits of the address used to access Scenic/MX1 local (private) memory. The low order bits of the address are the private memory address based on a starting address of 0. Local memory will occupy either 512 KBytes or 1 MByte of space.

Interrupt Line

Read/Write Address: 3CH
Power-On Default: 00H

This register contains interrupt line routing information written by the POST program during power-on initialization.

7	6	5	4	3	2	1	0
INTERRUPT LINE							

Bits 7–0 INTERRUPT LINE

Interrupt Pin

Read Only Address: 3DH
Power-On Default: 01H

This register is hardwired to a value of 1 to specify that $\overline{\text{INTA}}$ is the interrupt pin used.

7	6	5	4	3	2	1	0
INTERRUPT PIN							

Bits 7–0 INTERRUPT PIN

Latency/Grant

Read Only Address: 3EH
Power-On Default: 1005H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAXIMUM LATENCY								MINIMUM GRANT							

Bits 7–0 MINIMUM GRANT

Value = Length of burst period required in units of 250 ns (33 MHz clock). This value is hardwired to 05H.

Bits 15–8 MAXIMUM LATENCY

Value = Maximum latency of PCI access in units of 250 ns (33 MHz clock). This value is hardwired to 10H.

Timeout

Read/Write Address: 40H
Power-On Default: See bit definitions

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MTE	R	R	R	MEMORY TIMEOUT				R	R	R	R	R	R	R	R
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
		MASTER TIMEOUT				R	R	R	R	TARGET TIMEOUT				R	PTE

Bits 7-0 Reserved - reads all 0s

Bits 11-8 MEMORY TIMEOUT

value = timeout in PCI clocks for obtaining control of the private memory bus

The timer starts when the Scenic/MX1 receives a private memory access request from a master. If control of the private memory bus cannot be obtained before the timer expires, the Scenic/MX1 disconnects with retry. This function is enabled by setting bit 15 of this register to 1. The default value is 1111b.

Bits 14-12 Reserved - reads 000

Bit 15 MTE - Memory Timeout Enable
0 = Memory timeout function disabled
1 = Memory timeout function enabled (default)

Bit 16 PTE - PCI Timeout Enable
0 = Master and target timeout functions disabled
1 = Master and target timeout functions enabled (default)

Bit 17 Reserved - reads 0

Bits 21-18 TARGET TIMEOUT

value = timeout value in PCI clocks for receiving $\overline{\text{IRDY}}$ asserted by the master

The timer starts when the Scenic/MX1 as a target asserts $\overline{\text{TRDY}}$ and the master has deasserted $\overline{\text{IRDY}}$ at this time. If the master does not assert $\overline{\text{IRDY}}$ before the timer expires, the Scenic/MX1 will disconnect. This function is enabled by setting bit 16 of this register to 1.

Bits 25-22 Reserved - reads 0000

Bits 29-26 MASTER TIMEOUT

value = timeout value in PCI clocks for receiving DEVSEL after initiating a master cycle to a target

If the Scenic/MX1 acting as master does not receive DEVSEL before the timer expires, it will disconnect. This function is enabled by setting bit 16 of this register to 1.

Bits 31-30 Reserved - reads 00

Section 10: Control Register Descriptions

This section describes the Control Registers for Scenic/MX1.

In all register bit descriptions, "U" stands for undefined or unused; the letter "R" identifies reserved bits (a reserved bit's read value is undefined unless noted, and you may write only zero to a reserved bit). In Power-On Default values, "S" in a bit position means that upon a reset the bit assumes the value of the related strap.

10.1 REGISTER MAPPING AND ADDRESSING

Scenic/MX1 interfaces to 0.5 or 1.0 MByte of private memory, all of which is mapped into the PC system linear memory address space. As shown in Figure 10-1 below, the location of the private memory in the system linear address space is determined by the programmable PCI Base Address 2 register.

In addition, Scenic/MX1 has internal control and status registers which are also memory mapped. The location of these registers in the system linear address space is determined by the programmable PCI Base Address 1 register.

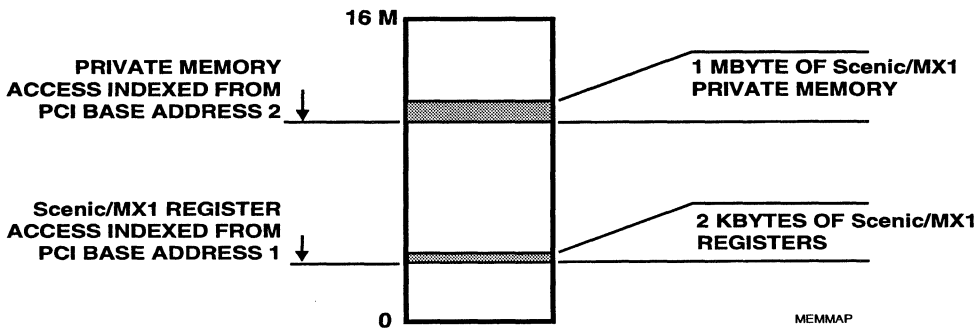

Figure 10-1. Addressing in MS Windows Environment

The 2 KByte address space for Scenic/MX1 control registers is subdivided into 8 equally sized address blocks. Each address block is associated with the registers for a programmable/observable hardware module. Each address block contains 256 bytes of control/status information.

Table 10-1. Module Register Base Addresses

Module Name	Module Address (hex)
MIU	2
SP	3
PCI	5

In this section's register descriptions, register addresses are given as a three digit hexadecimal value labeled 'Offset'. The first hex digit of the offset is the base address of the module containing the register. The next two digits are the two-byte index position of the register within the module. For example, the MIU's DRAM Configuration register is in module 2 at index 30H and has an offset value of 230H.

The complete register address is formed from the PCI Base Address 1 for the 2K register space, plus the offset, and has this structure:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Base Address 1					Module Address			Register Address (index within module)							
					- Offset -										
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Base Address 1															

10.2 MIU REGISTERS

MIU Module Address = 2H

This section lists the Control Registers for the MIU.

DRAM Configuration (R0230)

Read/Write Offset: 0230H
Power-On Default: 0000 00SSH

DRAM configuration parameters listed here require hardware strapping. For details on hardware pin strapping, see Section 5.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R	R	RAS LS	RAS PC		RAS PW		CAS/OE/ WE	
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bits 1-0 CAS/OE/WE Stretch - Default: PD [1:0] straps
00 = 6.5 ns (nominal)
01 = 5.0 ns (nominal)
10 = 3.5 ns (nominal)
11 = 0 ns (no stretch)

These bits set the additional duration by which CAS/OE/WE are extended.

Bits 3-2 RAS PW - RAS Pulse Width-Default: PD[3:2] straps
00 = 7 or 6.5 MCLKs
01 = 6 or 5.5 MCLKs
10 = 5 or 4.5 MCLKs
11 = 4 or 3.5 MCLKs

These bits are used in combination with bit 6 to select a pulse width. For example, setting bits 3-2 to 01 and bit 6 to 1 will select 5.5 MCLKs as the RAS pulse width. See Tables 5-2 and 5-3.

Bits 5-4 RAS PC - RAS Precharge-Default: PD [5:4] straps
00 = 4 or 4.5 MCLKs
01 = 3 or 3.5 MCLKs
10 = 2 or 2.5 MCLKs
11 = Reserved

These bits are used in combination with bit 6 to select a precharge duration.

Bit 6 RAS LS - RAS Length Select-Default: PD6 strap
0 = $\overline{RAS}$ Precharge = 2, 3, or 4 MCLKs;
$\overline{RAS}$ Pulse Width= 4, 5, 6, or 7 MCLKs
1 = $\overline{RAS}$ Precharge = 2.5, 3.5, or 4.5 MCLKs
$\overline{RAS}$ Pulse Width= 3.5, 4.5, 5.5, or 6.5 MCLKs

This bit is used together with bits 3-2 and bits 5-4 to select timing values. See details in Section 5.

Bits 31-7 Reserved. (Returns zero upon read)

Refresh Count (R0238)

Read/Write Offset: 0238H
Power-On Default: 0000 1200H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	REF EN	RCT											
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bits 11-0 RCT - Refresh Count in MCLKs
The default value is 512.

Bit 12 REF EN- Refresh Enable
0 = Disable DRAM Refresh
1 = Enable DRAM Refresh (default)

Bits 31-13 Reserved. (Returns zero upon read)

10.3 SP REGISTERS

SP Module Address = 3H

This section lists the Control Registers for the Serial Port functions.

Data Output (R0300)

See bit descriptions Offset: 0300H
Power-On Default: 0000 0000 0SSS S000 0SSS S001 0000 0101 b

Certain bits of this register require hardware strapping to set the values upon power up. These bits are identified in the accompanying text below and the corresponding signal line to strap is identified. For details of hardware pin strapping, see Section 5.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	SLD			LRC	R	AM		AF	Reserved			SF		R	SA EN
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	SCI	ADA	ABO	LT	R	R	R

Bit 0 SA EN - Software Audio Enable (read/write)
0 = Audio Enable
1 = Audio Disable (default)

Bit 1 Reserved

Bits 3-2 SF - Sampling Frequency (read/write)
00 = 32 KHz
01 = 44.1 KHz (default)
10 = 48 KHz
11 = PLL Select (S3 Sonic/AD)

Bits 6-4 Reserved

Bit 7 AF - Audio Freeze (read/write)
When this is asserted, the data in the output FIFO is untouched. Scenic/MX1 can resume without losing samples when this is deasserted.
0 = Audio Freeze off (default)
1 = Audio Freeze on

Bit 9-8 AM - Audio Mute (read/write)
Sets audio mask to zero and also sends mute control bit to audio DAC.
00 = No mute
01 = Hard mute
10 = Soft mute (10 ms)
11 = Soft mute (20 ms)

Bit 10 Reserved (Returns zero upon read)

Bit 11 LRC - LRCHN Channel Interpretation (read)-Default: PD7 strap.
0 = LRCHN active high left channel
1 = LRCHN active high right channel

Bits 14-12 SLD-SCLK and LRCHN Definition (read)-Default: PD[10:8] strap
000 = 256 DAC clocks per LRCHN, 2 DAC clocks per SCLK
001 = 256 DAC clocks per LRCHN, 4 DAC clocks per SCLK
010 = 384 DAC clocks per LRCHN, 2 DAC clocks per SCLK
011 = 384 DAC clocks per LRCHN, 4 DAC clocks per SCLK
100 = 384 DAC clocks per LRCHN, 6 DAC clocks per SCLK
101 = 384 DAC clocks per LRCHN, 8 DAC clocks per SCLK
110 = 512 DAC clocks per LRCHN, 4 DAC clocks per SCLK
111 = 512 DAC clocks per LRCHN, 8 DAC clocks per SCLK

Bit 18-15 Reserved (Returns zero upon read)

Bit 19 LT - Lag Time (read)-Default: PD11 strap
0 = First 16 bits latched on an LRCHN phase
1 = Last 16 bits latched on an LRCHN phase

Bit 20 ABO - Audio Bit Order-Default: PD12 strap
0 = Bit 0 first
1 = Bit 15 first

Bit 21 ADA - Audio DAC Absent (read)-Default: PD13 strap
0 = Audio DAC present
1 = Audio DAC absent

Bit 22 SC I- SCLK Inverted (read)-Default: PD14
0 = Data latched on rising edge of SCLK
1 = Data latched on falling edge of SCLK

Bits 31-23 Reserved (Returns zero upon read)

S3 DAC Control Data (R0308)

Read/Write Offset: 0308H
Power-On Default: 0000 0000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PLL RC								PLL LC							
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	R	R	R	R	APR LC	ISF SEL

Bits 7-0 PLL LC - PLL Data on Left Channel

M[7:0] data for the S3 Sonic/AD

Bits 15-8 PLL RC - PLL Data on Right Channel

N[7:0] data for the S3 Sonic/AD

Bit 16 ISF SEL - ISF Select
0 = Choose the sampling frequency from external FS pins
1 = Choose the sampling frequency from the audio data

Bit 17 APR LC - S3 Sonic/AD PLL Registers Load Control
0 = Do not load PLL registers
1= Load Sonic/AD PLL registers from SDATA

Bits 31-18 Reserved. (Returns zero upon read)

10.4 PCI CONTROL REGISTERS

PCI Module Address = 5H

This section lists the Scenic/MX1 PCI Control Registers. These registers provide functions that supplement those of the PCI configuration registers described in Section 9.

PCI Address R0 (R0500)

Write Offset: 0500H
Power-On Default: 0000 0002H

This is register 0 of a double-buffer pair.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA ADR0														TM0	
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DMA ADR0															

Bits 1-0 TM0 - TransferMode0
00 = Burst Transfer
01 = Not Supported.
10 = Single Cycle transfer (default)
11 = Single Cycle transfer (same as 10)

These bits determine the master transfer mode; complies with PCI specification definitions of low address bits.

Bits 31-2 DMA ADR0 - DMA DWORD Address 0

This value sets the start address for the DMA. The default value is zero.

PCI Address R1 (R0504)

Write Offset: 0504H
Power-On Default: 0000 0000 0000 0002H

This is register 1 of a double-buffer pair.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA ADR1														TM1	
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DMA ADR1															

Bits 1-0 TM1 - TransferMode1
00 = Burst Transfer
01 = Not Supported.
10 = Single Cycle transfer (default)
11 = Single Cycle transfer (same as 10)

These bits determine the master transfer mode; complies with PCI specification definitions of low address bits.

Bits 31-2 DMA ADR1 - DMA DWORD Address 1

This value sets the start address for the DMA. The default value is zero.

DMA Transfer Count R0 (R0508)

Write Offset: 0508H
Power-On Default: 0000 0000H

This is register 0 of a double-buffer pair.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS0															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	R	R	R	R	R	R	R	R	R	R	R	R	TS0		

Bits18-0 TS0 - Transfer Size R0

Sets number of PCI transfers. Each transfer moves 4 bytes.

Bits 31-19 Reserved

DMA Transfer Count R1 (R050C)

Write Offset: 050CH
Power-On Default: 0000 0000H

This is register 1 of a double-buffer pair.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS1															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	R	R	R	TS1		

Bits 18-0 TS1 - Transfer Size R1
Sets number of PCI transfers. Note: each transfer moves 4 bytes.

Bits 31-19 Reserved (Returns zero upon read)

DMA Control/Status (R0510)

See bit descriptions Offset: 0510H
Power-On Default: 0000 0000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	HEN	DAB	DMS ST	HDIR	DMS EN	HB EN			
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit 3-0 HB EN - Host Byte Enable (read/write)
Host DMA Byte Enables; the Host DMA generates PCI byte enables according to the settings of these bits. Writing a low to a bit enables transfer of the corresponding byte. When all bits are '0', all four bytes are enabled and a Dword is transferred. Default is '0000' causing Dword transfer.

Bit 0:
0 = enables transfer of Byte 0
1 = disables transfer of Byte 0

Bit 1:
0 = enables transfer of Byte 1
1 = disables transfer of Byte 1

Bit 2:
0 = enables transfer of Byte 2
1 = disables transfer of Byte 2

Bit 3:
0 = enables transfer of Byte 3
1 = disables transfer of Byte 3

Bit 4 DMS EN - DMA Manual Start Enable (write)
Master DMA Enable. Active high.
0 = Disable PCI Master DMA (default)
1 = Enables Host and PCI Master DMA. When this bit is set, assertion of the DMA Manual Start bit (bit 6 of this register) starts the Master DMA transfer in the direction set by bit 5 of this register.

Bit 5 HDIR - Transfer Direction (write)
Master DMA transfer direction. Only applies to DMA Manual Starts.
0 = Data is transferred from Scenic/MX1 to PCI. (Default)
1 = Data is transferred from the PCI system to Scenic/MX1.

Bit 6 DMS ST- DMA Manual Start (write)
0 = No effect (default)
1 = Starts a PCI Master DMA operation. If transfer direction is from PCI to Scenic/MX1, the Host DMA reads from PCI and writes to Scenic/MX1. If transfer direction is to PCI, the Host DMA waits for Scenic/MX1 to have data (to be 'un-empty') and then starts accessing the PCI bus. The bit is automatically reset to '0' after the DMA operation has started.

Bit 7 DAB - DMA Abort (write)
0 = No effect (default)
1 = Stops Host and PCI Master DMAs. FIFO pointers are cleared and the DMA control register state machine is reset into the IDLE state. This bit is automatically deasserted by hardware.

Bit 8 HEND - HDMA End (read/write)

Master DMA End. This bit is set to '1' when Master DMA Transfer Counter expires (reaches '0'). The software clears this bit to 0 by writing '1' to this location.

Bits 31-9 Reserved. (Returns zero upon read)

PM DMA Control and Status Register (R052C)

Read/Write Offset: 052CH
Power-On Default: 0000 0000 0000 0010H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NFD			LFD	R	R	R	R	R	R	R	PF	R	R	R	R
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	NFD						

Bits 3- 0 Reserved

Bit 4 PF - Pixel Format
0 = PCI mode: Y1, V0,Y0, U0
1 = S3 mode: V0, Y1, U0, Y0 (Default)

Bits 11-5 Reserved

Bit 12 LFD - Last Frame Dropped
0 = Frame not dropped
1 = Last frame was not completely sent out across the PCI bus

Bits 22-13 NFD - Number of Frames Dropped

This is the value of a counter that accumulates the number of frames that have been dropped.

Bits 31-23 Reserved

S3 Incorporated

Scenic/MX1 PCI MPEG-1 Audio/Video Decoder

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