Evaluation Kit Manual for the RCA CDP1802 COSMAC Microprocessor

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EVALUATION KIT MANUAL FOR THE RCA CDP1802 COSMAC MICROPROCESSOR MPM-203

FOREWORD

The RCA CDP18S020 Evaluation Kit provides the key hardware and firmware elements for a computer system based on the RCA CDP1802 COSMAC Microprocessor. The kit is a useful, convenient evaluation tool intended to encourage and facilitate the application of the RCA 1800 series of microprocessors and associated components. With the hardware and firmware provided with this Kit, and augmented with an input/output terminal and power supply, the user can readily prototype dedicated systems and evaluate software programs, components, and systems operation.

This Evaluation Kit Manual provides detailed information on the Kit, its components, its over-all configuration, and how it operates. The Manual tells how the Kit is assembled, how it can be used with various terminals, how to troubleshoot hardware, how the various systems are designed, how they operate, how to check out software, and how to make use of the resident firmware. In addition, a number of application notes are provided describing the I/O and control features, the memory systems available and their utilization, and the use of resident firmware for Read and Type routines.

As additional application notes are developed, they will be made available. Along with a careful study of this Manual, the user should refer to the following publications:

MPM-201 User Manual for the RCA CDP1802 COSMAC Microprocessor

MPM-206 Binary Arithmetic Subroutines for RCA COSMAC Microprocessors

DESCRIPTION

The CDP18S020 COSMAC Evaluation Kit is a complete microcomputer built around the CDP1802 microprocessor. All components including PC card are supplied for building a fully operational microprocessor system. A functional diagram of the Evaluation Kit is shown in Fig. 1-1 and Fig. 1-2 shows the topological layout of the PC card.

At the heart of the system is the CDP1802 COSMAC microprocessor. It is a single chip, 8-bit, static microprocessor fabricated in a self-aligned, silicon gate, CMOS technology. The CDP1802 offers all the advantages of CMOS technology including low power dissipation, single wide-range power supply, full operating temperature range, high noise immunity, and single-phase clock. It combines a repertoire of 91 powerful instructions with the unique COSMAC architecture. This design maximizes performance with minimal memory usage. A comprehensive CDP1802 User Manual (MPM-201) and Data Sheet are provided with the Evaluation Kit to assist the user in understanding and applying the CDP1802 to his specific applications.

In addition to the CDP1802, the Evaluation Kit includes several other sections:

Clock and Control
Display
Memory
I/O

The Clock and Control section contains a crystal-controlled clock generator utilizing the CDP1802 on-chip oscillator, and control logic to interface the CPU with switches for Reset, Run Program, Run Utility, and Single-Step operations.

The Display section consists of interface circuits and LED's configured to display the 16-bit memory address bus (MA), 8-bit data bus (DB), and CPU status. A separate LED power supply connection is provided to permit low-power operation by disabling the LED displays.

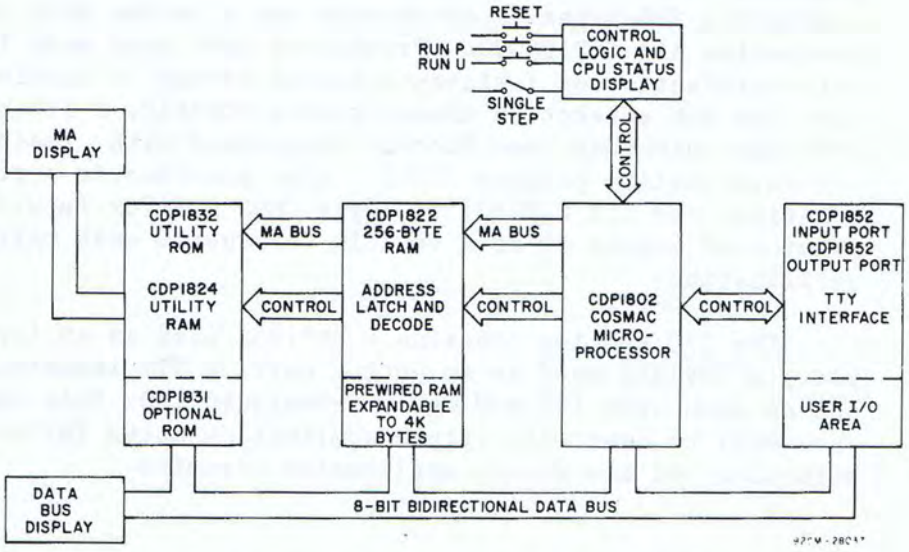


Fig. 1-1 - Functional diagram of CDP18S020 Evaluation Kit.

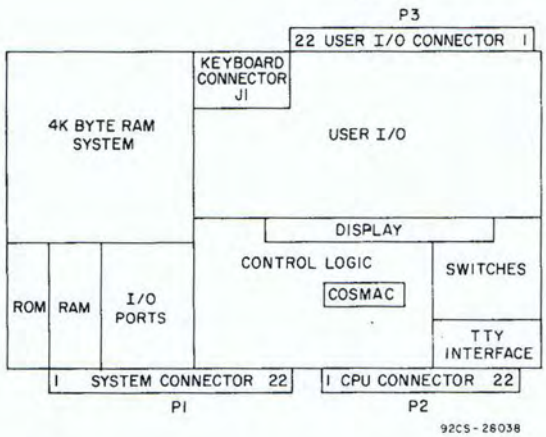


Fig. 1-2 - Topological layout of CDP18S020 Evaluation Kit from the component side.

The Memory section is divided into RAM and ROM subsections. The RAM subsection contains a fully decoded, prewired, CDP1822-based 4K byte RAM system. Devices for populating 256 bytes of the system are provided with the Evaluation Kit CDP18S020. Provisions have been made for write-protection of 1-kilobyte blocks of RAM to simulate ROM. The ROM subsection consists of a CDPR512, a 512-byte CMOS ROM which has been factory programmed with resident software utility program (UT4). Also provided is a prewired location for the CDP1831 512-byte CMOS ROM for future expansion of memory or as a vehicle for custom mask pattern verification.

The I/O section contains a CDP1852 used as an input port, a CDP1852 used as an output port, a TTY interface, and an open area for adding user-designed I/O. This open area will be used with future application notes for construction of new device application circuits.

CDP18S020 EVALUATION KIT CONTENTS

The following items are supplied with the CDP18S020 Evaluation Kit:

a) PC card - prewired for CPU, RAM, ROM, Control, and Display.
b) CDP1802 Microprocessor.
c) 2 - CDP1822 256x4 CMOS RAM's.
d) CDP1824 32-byte CMOS RAM.
e) CDP1832 512-byte CMOS ROM factory programmed with Utility Program UT4.
f) 3 - CDP1852 8-bit Input/Output Ports (1 used as address latch).
g) Switches and standard CD4000 Series COS/MOS components for control.
h) Discrete LED memory address bus, data bus, and CPU status display.
i) Components for 20-mA TTY or RS232C interface.
j) 2-MHz crystal.
k) Miscellaneous hardware for mechanical assembly.
l) MPM-203, Evaluation Kit Manual for the RCA CDP1802 COSMAC Microprocessor.
m) MPM-201, User Manual for the CDP1802 COSMAC Microprocessor.
n) User registration card.

CDP18S020 EVALUATION KIT SPECIFICATIONS

Specifications for the completed CDP18S020 Evaluation Kit are as follows:

a) PC card size : 14 x 9.7 x .062"
b) Mating connectors : 44 pin, .156" spacing
c) Power requirements (minimum configuration):
V_{DD} = 5 V, 10 mA; 10 V, 20 mA
V_{CC} = 5 V, 20 mA; 10 V, 40 mA
V_{LED} = 5 V, 600 mA
V_{TTY} = 5 V, 100 mA
d) Operating speed: 2 MHz at V_{DD} = 4-12 volts
e) CPU: CDP1802 COSMAC microprocessor
f) ROM: CDP1832, 512 bytes, factory programmed with UT4
g) RAM: 2 - CDP1822's, 256 bytes, expandable to 4K bytes
CDP1824, 32 bytes (used by UT4)
h) I/O: CDP1852 8-bit Input Port
CDP1852 8-bit Output Port
i) Data terminal interface: 20-mA current loop (TTY) or EIA RS232C (selectable)
j) Display: 29 discrete LED's with separate supply
k) Controls: RESET - initializes CPU and control logic.
RUN U - initiates Utility Program (UT4) execution.
RUN P - initiates program execution
CONTINUOUS/STEP - mode control.

ASSEMBLY INSTRUCTIONS

Your CDP18S020 COSMAC Evaluation Kit has been designed for minimum assembly time. The procedure consists of mounting and soldering the kit components and a minimal amount of discretionary wiring to configure the kit to your specific requirements. To assist you in the assembly operation, a step by step procedure is given below. Following this procedure and the use of good workmanship practices will assure successful completion of the assembly operation.

1. Unpack the shipping carton, identify and sort all components, and check the contents against the parts list given in Table 1-I on the following page.

Note: Prior to mounting on the PC card, all IC's should be kept in the conductive foam shipping carrier. The carrier keeps the IC leads shorted together and also protects the leads from physical damage.

2. Orient the PC card as shown in Fig. 1-3. You are now looking at the component side of the card. All components will be mounted on this side and all soldering will be done on the reverse side. The component side of the PC card has silk-screened part numbers and location guides. It is recommended that you study the PC card and components and become familiar with the parts placement and nomenclature before beginning assembly.

3. General discrete component assembly instructions.

   a) When mounting components, bend the leads on the solder side of the PC card in the direction of the metal run - away from adjacent components or metal runs.

   b) When soldering components, preheat the connection and apply just enough solder to "wet" the connection. Avoid using excessive amounts of solder. Use only rosin-core solder.

Table 1-I - CDP18S020 parts list.

TYPE NUMBER	CDP18S020 I.D.#	QTY.	DESCRIPTION
CDP1802	U9	1	COSMAC Microprocessor
CDP1822	U24,U25	2	256x4 Static RAM
CDP1824	U3	1	32x8 Static RAM
CDP1832	U2	1	512x8 Static ROM
CDP1852	U4,U5,U8	3	8-Bit Input/Output Port
CD4001	U15	1	Quad 2 Input NOR Gate
CD4011	U13	1	Quad 2 Input NAND Gate
CD4013	U14	1	Dual D Master-Slave Flip-Flop
CD4023	U6	1	Triple 3-Input NAND Gate
CD4028	U7	1	BCD-to-Decimal Decoder
CD4049	U10,U11,U16 thru U21,U23	9	Hex Inverter Buffer
CD4096	U12	1	Gated JK Master-Slave Flip-Flop
CD4555	U22	1	Dual Binary 1 of 4 Decoder
76B04	S1	1	Quad SPST DIP Switch
8125	S2,S3	2	SPDT Pushbutton Switch
8225	S4	1	DPDT Pushbutton Switch
7101	S5	1	SPDT Toggle Switch
2N3053	Q1	1	NPN Transistor
2N4037	Q2,Q3	2	PNP Transistor
D1201F	CR1,CR2	~~2~~	Diode (1N4001 or equiv.)
5082-4494	LED's	29	Red LED
T 310(C)	C1 thru C5,C9, C10	7	15-Microfarad, 20-Volt Capacitor
CK05BX104	C8	1	0.1-Microfarad, 30-Volt Capacitor
898-1	RN1,RN2	2	22KΩ, DIP Resistor Network
---	R1,R5,R6,R7, R13,R19	6	22KΩ, 1/4 Watt Resistor
---	R3	1	390Ω, 1/4 Watt Resistor
---	R4,R15	2	3.9KΩ, 1/4 Watt Resistor
---	R8,R9,R10,R11,	4	33 KΩ, 1/4 Watt Resistor
	R12	5	100KΩ, 1/4 Watt Resistor
---	R14	1	10MΩ, 1/4 Watt Resistor
---	R16,R17,R18,R20, R21,R25	6	1KΩ, 1/4 Watt Resistor
---	R22	1	10KΩ, 1/4 Watt Resistor
---	R23	1	2.7KΩ, 1/4 Watt Resistor
---	R24	1	220/47Ω, 1/4 Watt Resistor

Table 1-I - CDP18S020 parts list (cont'd)

TYPE NUMBER	CDP18S020 I.D.#	QTY.	DESCRIPTION
---	XTAL-2	1	2MHz, AT-Cut Quartz Crystal, C_L=15pF
C934002	DS-40	1	40-Pin DIP Socket
C932402	DS-24	1	24-Pin DIP Socket
C932202	DS-22	2	22-Pin DIP Socket
---	N1	5	8-32 Nut for Mounting Foot
MAC 51	F1	5	Rubber Foot
R644	P1	1	44-Pin Connector-Solder Terminals
---	2468306	1	Printed Circuit Card
MPM-201	MPM-201	1	User Manual for the CDP1802 COSMAC Microprocessor
MPM-203	MPM-203	1	Evaluation Kit Manual for the RCA CDP1802 COSMAC Microprocessor

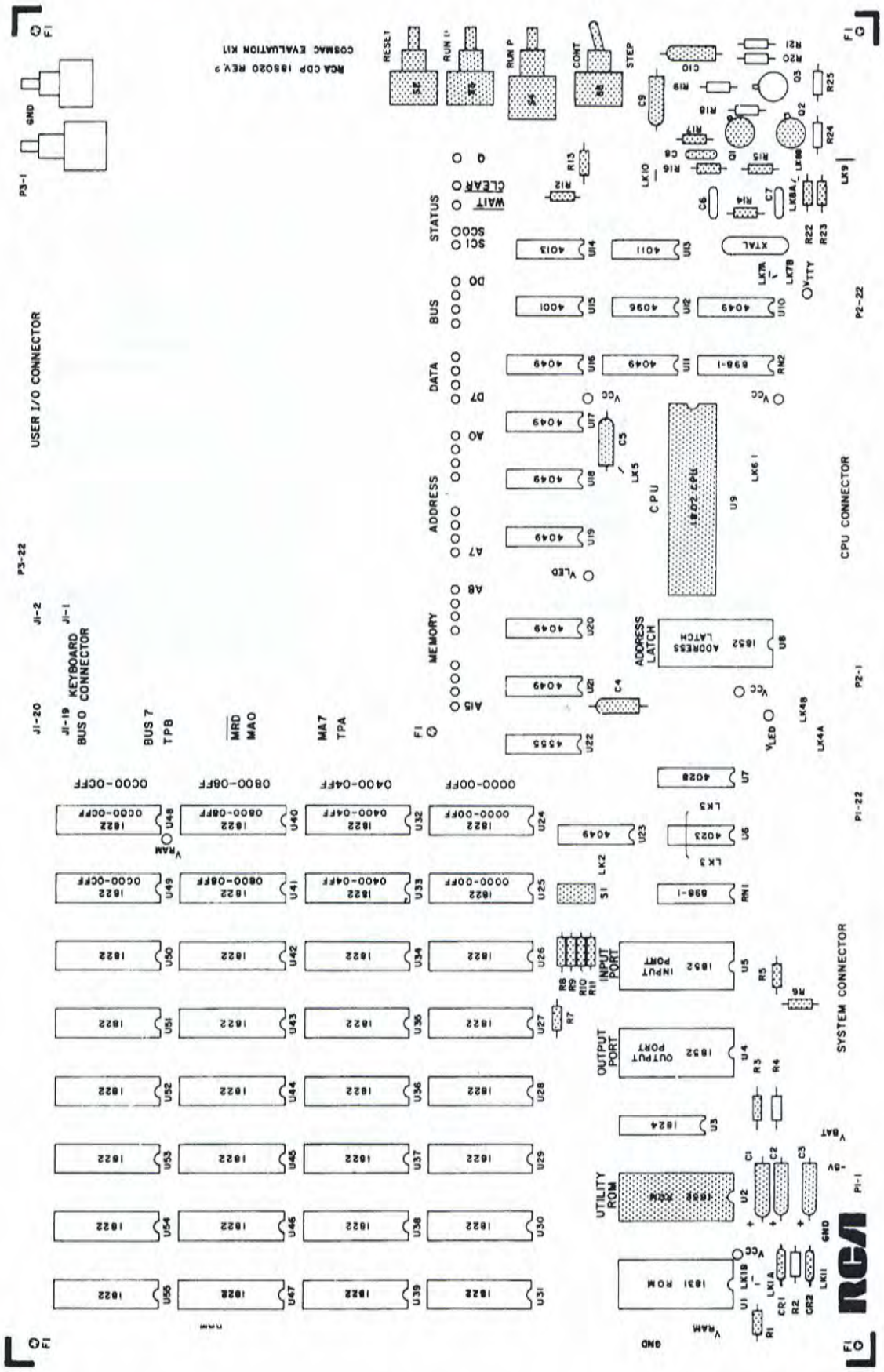


Fig. 1-3 - PC card orientation and discrete component placement.

c) After soldering, carefully inspect the connection for integrity and possible shorts on both component and solder sides on the PC card. Clean away excess flux with an electronic-grade flux remover.

d) Always double check component placement. Because of the compact nature of the PC card, it is possible to insert components in the wrong position.

4. Specific discrete component assembly instructions.

Refer to Fig. 1-3 for component placement and Table 1-I for part description.

a) Mount the five feet (F1) at the positions indicated and secure with 8-32 nuts.

b) Mount and solder the 22, 24, and 40 pin DIP sockets at locations U24 & U25, U2, and U9 respectively.

c) Mount and solder the guard DIP switch (S1) as indicated. Switch 1 (S1-1) should be closest to the SYSTEM CONNECTOR and switch 4 (S1-4) should be closest to the USER I/O CONNECTOR.

d) Mount and solder the three pushbutton switches (S2,S3,S4) and the toggle switch (S5) at the positions indicated.

e) Mount and solder capacitors C1 through C5, C9, and C10. The rounded ends (positive terminal) must be pointed in the direction indicated.

f) Mount and solder capacitor C8 (0.1 microfarad) as indicated.

g) Add jumper LK11 across connections labelled CR2. CR1 and R2 are left vacant.

h) Mount and solder transistors Q1 (2N3053) and Q2 (2N4037) as indicated. The tabs or index

marks on the metal cans must be oriented as shown in Fig. 1-3. Avoid excessive heat when soldering. Avoid shorting the metal can to the transistor leads or to the adjacent metal runs on the board.

i) Mount and solder resistors R1, R5, R6, R7, R13, R19 (22KΩ, red-red-orange); R3 (390Ω, orange-white-brown); R15 (3.9KΩ, orange-white-red); R8, R9, R10, R11, R12, (100KΩ, brown-black-yellow); R14 (10MΩ, brown-black-blue); R16, R17 (1KΩ, brown-black-red); R22 (10KΩ, brown-black-orange); and R23 (2.7KΩ, red-violet-red) at the positions indicated in Fig. 1-3.

j) Mount and solder the 29 LED's at the position indicated. In order to provide for neat LED configuration, only one terminal on each LED should be soldered at first, using a straight edge to help align them. The longer LED lead must be inserted in the hole that is closest to the edge of the user area. Avoid using excessive heat when soldering.

5. General IC assembly instructions.

a) Refer to ICE-402 and ICAN-6525 in the Miscellaneous Section of this Manual for general handling precautions.

b) Soldering iron tips, fixtures, tools, and card handling facilities should be grounded.

c) When mounting IC components, bend only the two leads at opposite corners to hold the device for soldering. This will facilitate removal, if necessary at a later time.

d) When soldering IC's on the PC card always solder the V_{DD} pin first. This pin is the directly across from pin 1 on all IC's provided with your kit. Next solder V_{SS}. This pin is the bottom-most pin on the same side as pin 1. The order after V_{DD} and V_{SS} have been soldered is not important.

In soldering the IC leads, care should be taken to avoid overheating. A short pre-heat followed by flowing just enough solder to "wet" the connection should be sufficient. All leads are either solder dipped or gold plated and will solder very easily.

e) After soldering, carefully inspect the connections for integrity and possible shorts on both component and solder sides of the PC card. Clean away excess flux with an electronic grade solvent.

6. Specific IC assembly instructions. Refer to Fig. 1 -4 for component placement and Table 1-I for part description.

a) Mount and solder IC's U3 through U5 as indicated.

b) Mount and solder RN1 (22-KΩ DIP resistor network) to the right of U5.

c) Mount and solder IC's U6 through U8* as indicated.

d) Mount and solder RN2 (22-KΩ DIP resistor network) to the lower right of U9.

e) Mount and solder IC's U10 through U23 as indicated.

f) U24 and U25 are CDP1822 256 x 4 RAM's. 32 positions have been prewired for up to 4K bytes of RAM in the Evaluation Kit. Positions U24 and U25 are at the lower right of the first row of the prewired RAM and correspond to the first 256 bytes of memory. Insert the two CDP1822 RAM's into the previously mounted 22-pin DIP sockets at locations U24 and U25 with pin 1 oriented as shown.

g) Mount and solder the 2 MHz crystal (XTAL-2) as indicated. Avoid shorting the metal case to adjacent metal runs.

h) 24- and 40-pin DIP sockets have been previously mounted at U2 and U9, respectively. Insert the CDP1832 and the CDP1802 in their sockets with pin 1 oriented as shown.

* NOTE: Before installing U8, refer to Appendix I for special instructions for Load Mode Adaptation.

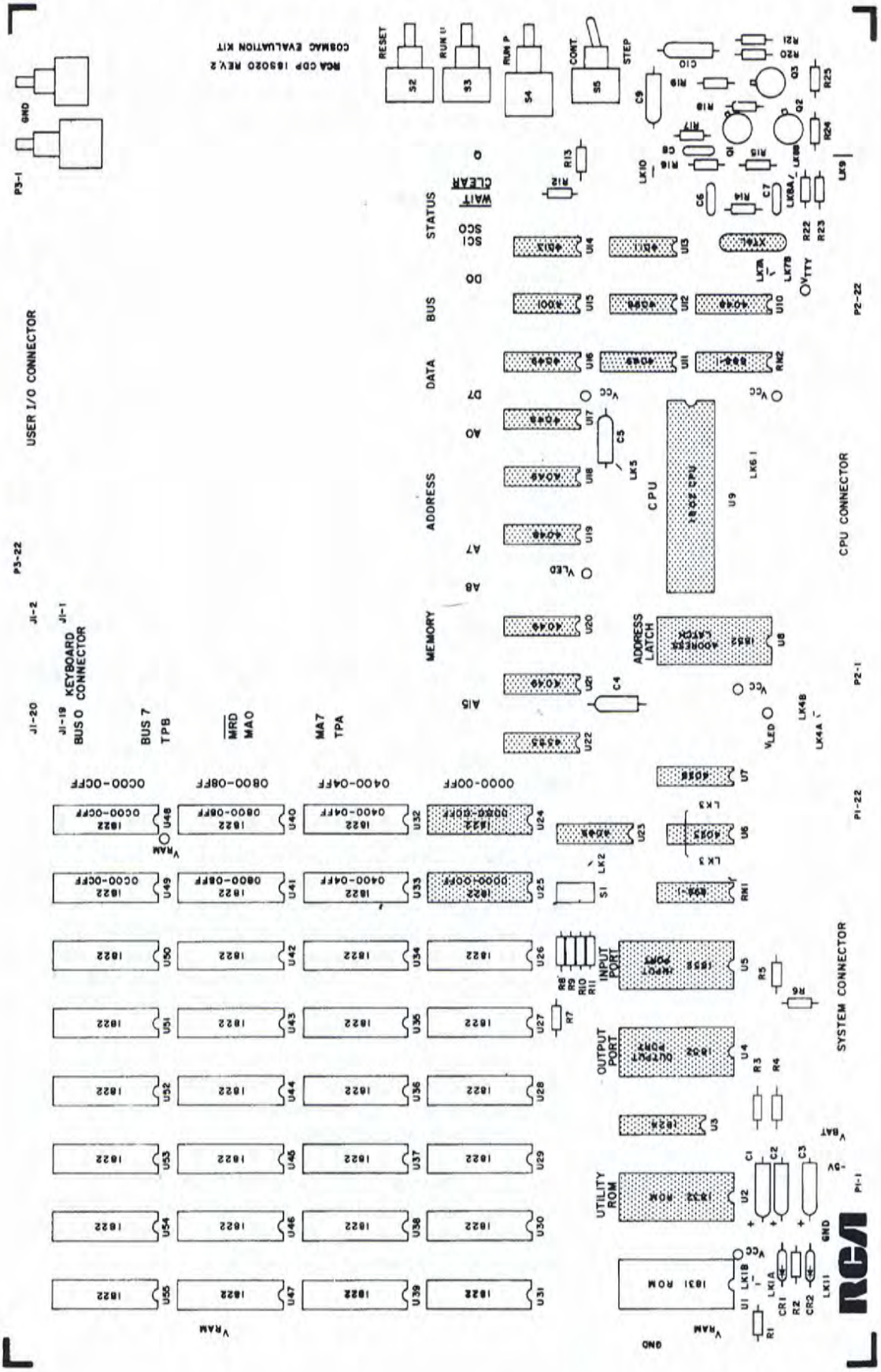


Fig. 1-4 - IC Component Placement

7. Discretionary wiring.

The discretionary wiring assembly steps will configure the Evaluation Kit to your specific requirements.

a) 20-mA current loop (TTY) or EIA RS232C optional configuration.

Refer to Fig. 1-5 in the following procedure.

Note: To complete this step it is necessary to determine the TTY configuration required. An explanation of the 20-mA current loop and EIA RS232-C interfaces can be found in the application note entitled, "Data Terminal Interface Considerations for RCA Microprocessor Evaluation Kit CDP18S020" in the I/O and Control Application Note section of this Manual

1) 20-mA current loop (TTY)

A. Insert link LK8B using a small length of hook-up wire.

B. Mount and solder resistor R24 (220Ω, red-red-brown) at the position indicated in Fig. 1-5. (Note: The value of R24 may need to be changed if a data terminal other than a TTY is configured for the 20-mA current loop interface. A 47-ohm, yellow-violet-black resistor is included to be used as a possible alternate R24 in this case. For further details, refer to the application note entitled "Data Terminal Interface Considerations for RCA Microprocessor Evaluation Kit CDP18S020" in the I/O and Control Application Note section of this Manual.

2) RS232C.

A. Insert link LK8A using a small piece of hook-up wire.

B. Insert link LK9 using small piece of hook-up wire.

C. Mount and solder resistor R24 (220Ω, red-red-brown) at the position indicated in Fig. 1-5.

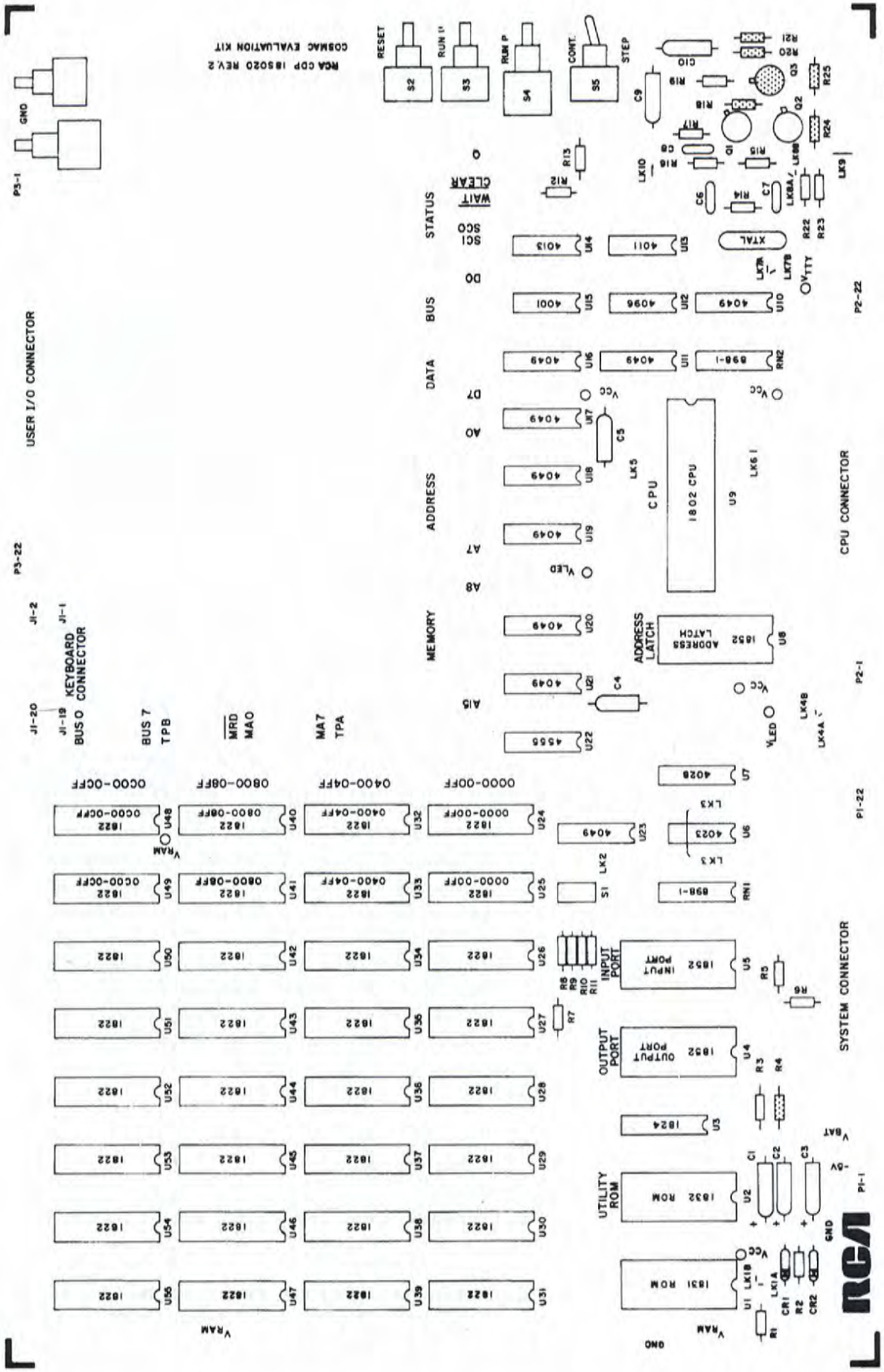


Fig. 1-5 - Discretionary Wiring

D. Mount and solder transistor Q3 (2N4037) as indicated. The tab or index mark must be oriented as shown. Avoid excessive heat when soldering.

E. Mount and solder resistors R4 (3.9K , orange-white-red); and R18, R20, R21, R25 (1KΩ, brown-black-red) at the positions indicated in Fig. 1-5.

b) Mounting of optional components. (Not provided.)

Refer to Fig. 1-6 in the following procedure.

1) C6 and C7 are oscillator stabilizing capacitors with recommended values of 20pF. Mount and solder at the positions indicated in Fig. 1-6.

2) R2 is a triekle-charge-limiting resistor for a rechargeable battery. Refer to the battery manufacturer's specifications for appropriate value. Mount and solder as indicated.

3) Location U1 has been prewired to accept a CDP1831 mask-programmable 512-byte ROM. It is intended to be used to verify custom mask patterns. Mount and solder the CDP1831 at location U1 as indicated in Fig. 1-6. Follow the handling and mounting procedure described in section 5.

4) Thirty additional prewired CDP1822 locations have been provided for RAM system expansion. Refer to Table 2-I to correlate a specific RAM address to a given RAM location.

c) Alternate location of specific supplied components.

It is possible to mount 18 LED's, switch S2 (RESET SPDT pushbutton switch), and switch S4 (RUN P DPDT pushbutton switch) in alternate locations. These locations are at the top of the PC card.

To use, mount the appropriate component at the desired position and connect hook-up wire between the primary location terminals and the holes provided at the alternate location. (Note: The

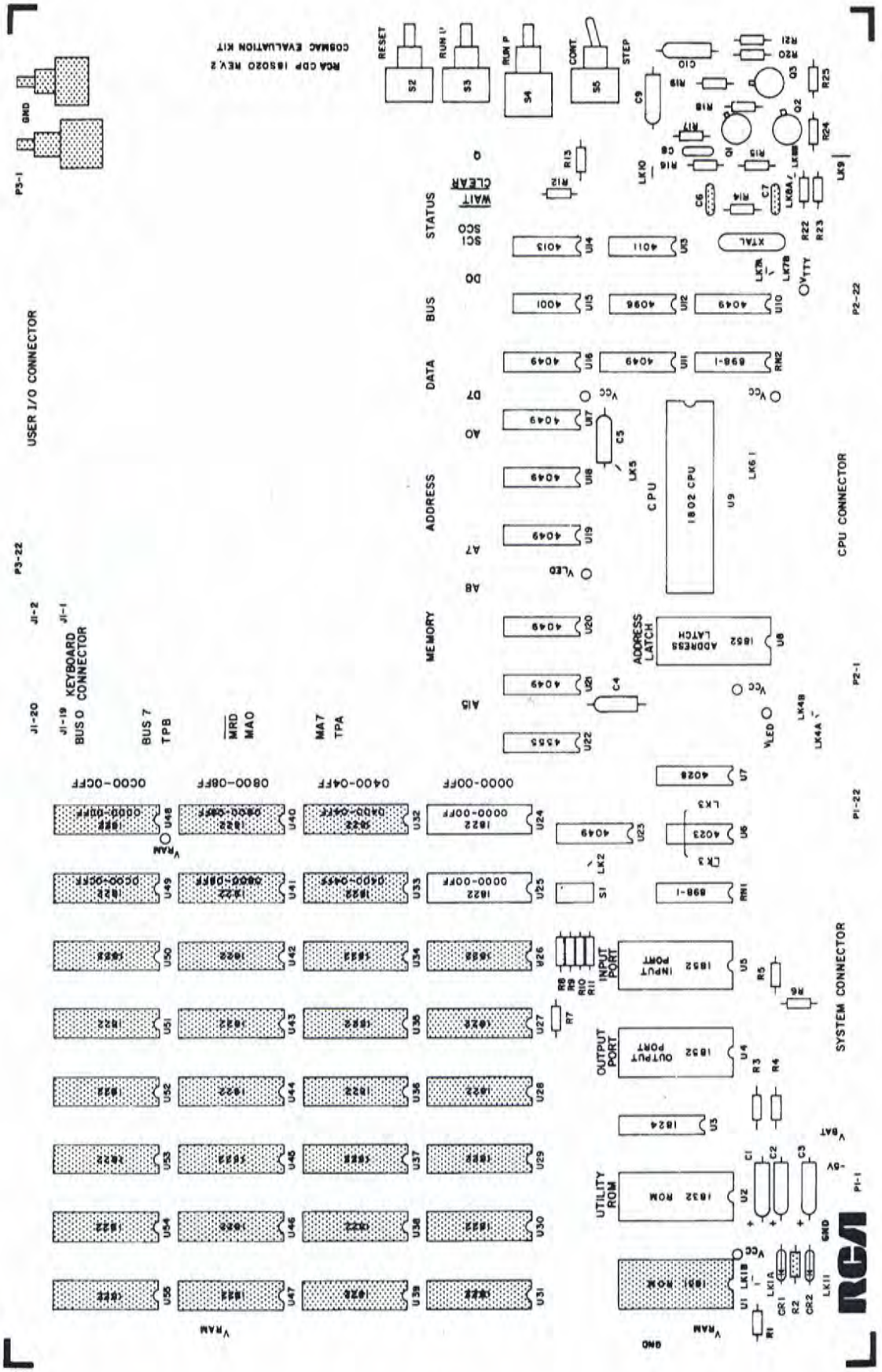


Fig. 1-6 - Mounting of Optional Components

subject locations are also intended for general use and system expansion.)

d) Input port service request (SR) termination.

The input port (U5-CDP1852) service request ($\overline{SR}$-pin 23) can be optionally connected to either INTERRUPT or EF3 of the CDP1802 microprocessor. This is the purpose of link LK4A and LK4B, respectively. It is recommended that LK4B be shorted with a small piece of wire to connect the $\overline{SR}$ output to $\overline{EF3}$. Operation will be explained later.

e) V_{LED}/V_{TTY} power supply separation (link 10).

It is possible to use the Evaluation Kit with separate LED and data terminal interface power supplies. By inserting LK10 the user connects the V_{LED} and V_{TTY} power busses together. The advantage of separating these two supplies is that the user may then shut off the V_{LED} supply and still run a program that interacts with his data terminal (like the utility program, UT4). This would be done in the interest of saving power once the user has written and debugged a program and no longer requires the debugging facility of the LED's. The disadvantage of separating these two supplies is that the user simply needs another power supply in order to perform the check-out procedure in the next section and get his Kit running.

It is recommended that the user insert LK10 to connect V_{LED} and V_{TTY} as one power supply, while following the directions in the next section. The check-out procedure in the following section explains the power supply functions and connections. The specifications for all the power supplies required can be found in the introductory description.

f) Optional links.

Optional prewired links have been provided on the PC card for convenience and application flexibility. To use these links, the printed conductor must be carefully removed from the designated area. A tabulation of the links and their function is given in Appendix G.

8. You have now completed assembly of your Evaluation Kit. You should go back and verify component placement, making sure all leads have been soldered. (Note: No soldering is required on the component side of the card.) Excess flux should be cleaned from the card and the solder side inspected for shorts. You are now ready to begin the check-out procedure.

CHECK-OUT PROCEDURE

The following procedure is provided to verify proper operation of your assembled kit.

1. Orient the PC card as shown in Fig. 1-3. The component side of the PC card should be facing up. The connector on the lower left side, labeled SYSTEM CONNECTOR, (P1), contains all connections required to operate the kit. For check-out and initial operation, a 44-pin mating connector has been provided. Appendices A and B show connector pin placement and pin assignments. Wire the mating connector at this time as follows:

   a) Attach 24-inch lengths of hook-up wire to pins A (V_{SS} ground), B (V_{CC}), D (V_{LED}), H (V_{TTY}), and L (V_{DD}). These wires will be connected to appropriate power supplies later.

   b) Refer to Appendix F for data terminal connections.

2. Attach the wired connector to the SYSTEM CONNECTOR (P1) location on the PC card. Be sure that pin 1 on the PC card is mated with pin 1 on the mating connector. To assure proper electrical connection, the printed fingers on the PC card must be free of flux and solder bumps. Also, if the fingers appear corroded, they can be cleaned by lightly rubbing with an eraser.

3. Connect the negative lead of an ohmmeter to the free end of the wire on pin A (V_{SS}).* With the other lead, test the resistance to the following connector pins as follows:

   a) V_{CC} (pin B) - greater than 1 KΩ.
   b) V_{LED} (pin D) - greater than 5 KΩ.
   c) V_{DD} (pin L) - greater than 10 KΩ.

---

* Note: The black or common lead of an ohmmeter is not always negative.

If the readings are less than the values given, it indicates a short-circuit or high-leakage condition between two power supply connections. If so, reverify component placement and check for possible short-circuit conditions such as solder bridges between adjacent printed metal runs. Also, a very low reading may indicate that an IC is inserted backwards.

4. Having successfully completed item 3 above, you are ready to start operating your microcomputer.

   The power supply functions and appropriate connections are explained below:

   a) V_{DD} is the CDP1802 Microprocessor main supply. It is positive polarity voltage and should be set between +3 and +12 volts. (If you plan to be using the C version, CDP1802CD, your power supply should be set between +4 and +6 volts. However, the kit has been provided with a full voltage range part, CDP1802D. (For more information see the CDP1802 data sheet in the DATA SHEET section of this manual.)

   b) V_{CC} is the memory, I/O, and control circuit supply. It is a positive polarity and must be less than or equal to V_{DD}. During the Check-Out Procedure, V_{CC}, V_{DD}, V_{TTY}, and V_{LED} will be connected together.

   c) V_{LED} is the supply voltage for the LED displays. It must be set to +5 volts, ±10%. A separate connection is provided so that the Evaluation Kit can be optionally operated with or without V_{LED} to conserve power.

   d) V_{TTY} is the terminal interface positive supply voltage. It should be set to +5 volts, ±10%. For additional information, refer to the "Data Terminal Interface Considerations for RCA Microprocessor Evaluation Kit CDP18S020" application note in the I/O and Control Application Note section of this Manual.

e) V_{SS} is the system common or ground. All other supplies are referenced to V_{SS}.

f) An optional -5 volt supply connection is available at SYSTEM CONNECTOR (P1) pin 1 for the RS232C interface.

g) Also, an optional +12 volt supply connection is available at system connector (P1) pin C. The +12 volt and the -5 volt connections are provided for the optional use of a 2704 PROM in location U2.

5. Refer to Fig. 1-3.

Adjust all power supply voltages before plugging the system connector onto the Evaluation Board.

Connect V_{DD}, V_{CC}, and V_{LED} together to a 5-volt (800-mA) power supply. Connect V_{TTY} to 5 volts either by inserting LK10 or by an external connection to P1-H. Connect V_{SS} to ground. Put the CONTINUOUS/STEP switch (S4) in the STEP (down) position and the four DIP switches (S1-1, -2, -3, -4) in the closed position. Apply power. Verify +5 volts at the V_{DD}, V_{CC}, and V_{LED} terminals on the connector. The current drawn is a function of the number of LED's that are on but should not exceed 800 mA. Push RESET followed by RUN U twice. The LED's should display the following condition:

0000 0000 0000 0000	XXXX XXXX	00		____01_____		0
MEMORY ADDRESS	DATA BUS	SC1	SCO	WAIT	CLEAR	Q

Push RUN U once more. The LED's should read:

0000 0000 0000 0001	XXXX XXXX	01		____01_____		0
MEMORY ADDRESS	DATA BUS	SC1	SCO	WAIT	CLEAR	Q

NOTE: X = Indeterminate state since the system RAM has just been powered up.

Turn-off power.

If your Evaluation Kit fails this test it will be necessary to isolate the failure. Refer to the Trouble Shooting section immediately following this section for assistance.

6. Connect the TTY. For assistance, refer to the "Data Terminal Interface Considerations for RCA Microprocessor Evaluation Kit CDP18S020" application note in the Control and I/O Application Note section of this Manual.

   Apply power. (When using the RS232C interface, turn on the -5 volt supply coincident with or after the +5 volt supply.) Push RESET. Switch the TTY to the LINE mode and switch CONTINUOUS/STEP to CONTINUOUS (up). Push RESET followed by RUN U. RUN U means start execution of the Utility Program called UT4. This program is permanently stored in the CDP1832 ROM (U2). It enables the microprocessor to communicate to the TTY via the CPU flag input EF4 and the serial output Q. The Utility Program interprets the serial ASCII code from the TTY and generates the proper serial ASCII code to the TTY. The TTY interface provides the proper signal conditioning to enable the CDP1802 and TTY to communicate with each other. For more information, see the UTILITY PROGRAM section of this Manual and the "Data Terminal Interface Considerations for the RCA Microprocessor Evaluation Kit CDP18S020" in the I/O and Control Application Note section of this Manual.

   After hitting RUN U, type either CR (carriage return)or LF (line feed):

   a) For Full Duplex, hit CR.

   b) For Half Duplex, hit LF.

   This routine sets up bit-serial timing and specifies echo or no echo, respectively.

   The Utility Program (UT4) responds with *. This is called a prompt character and is typed out by UT4 whenever it is ready to accept input from the TTY.

7. Via the TTY, type the following:

   !MO 7B7A3000 CR (carriage return)

   The TTY will respond with *.

   Next type:

   ?MO 4CR

   The TTY should print

   0000 7B7A 3000

   *

8. Now switch the TTY to LOCAL mode and then switch S5 to STEP (down). Push RESET followed by RUN P twice. (In the following example the 16-bit MA display will be written as 4 hexadecimal characters, and the 8-bit DB will be written as 2 hexadecimal characters. (For readers unfamiliar with hexadecimal notation, please refer to Appendix D for hexadecimal-to-binary-and-decimal conversion.)

   The display should read

MA	DB	SC1	SC0	WAIT	CLEAR	Q	
0000	7B	00		01		0	(FETCH)

   Push RUN P. The display should read

0001	00	01	01	1	(EXECUTE)

   Push RUN P,

0001	7A	00	01	1	(FETCH)

   Push RUN P,

0002	00	01	01	0	(EXECUTE)

   Push RUN P,

0002	30	00	01	0	(FETCH)

   Push RUN P,

0003	00	01	01	0	(EXECUTE)

   Push RUN P - The display will recycle through the six states just defined.

   A detailed description of this small 4-byte program and how to interpret the display can be found in the Operation Section of this Manual.

9. Now switch the TTY to LINE MODE and then switch S5 to CONTINUOUS (up) and push RESET followed by RUN U. Type CR or LF on the TTY. The TTY should respond with *. Type

   !MO 7B F8 FF B4 24 94 3A 04 7A F8

   FF B4 24 94 3A 0C 30 00 CR

   (Note: Spaces are shown between bytes for clarity but are not necessary.)

After the TTY responds with * type

```
?M0 12CR
```

The TTY should respond

```
0000 7BF8 FFB4 2494 3A04 7AF8 FFB4 2494 3AOC;

0010 3000

*
```

Type $P0CR

If the program is executing properly the Q LED will blink off and on with about two seconds between each state change.

A detailed description of this program is given in the Design and Operation section of this Manual.

If your kit passes these tests, congratulations! You have successfully completed assembly and check-out of a complete microcomputer.

If you are having trouble refer to the Trouble-Shooting Guide for assistance.

The Evaluation Kit is ready to load and execute programs. It is recommended that you proceed to the Design and Operation section for further information on the Evaluation Kit design and operation.

TROUBLESHOOTING GUIDE

The following guide is intended to assist you in locating and correcting problems which were identified in Steps 3, 5, 6, 7, 8, or 9 of the Check-Out Procedure. If you successfully completed all nine steps of the Check-Out Procedure you should proceed to the Design and Operation section of this manual.

1. Locating and correcting short-circuit or low-impedance conditions between two power supply connections. (Step 3)

   a) General.

      1) Verify proper orientation and alignment of the SYSTEM CONNECTOR (P1) mating connector.

      2) Verify that the ohmmeter <u>negative</u> lead is connected to V_{SS}. Reversing the ohmmeter connections will cause failure of the resistance test.

      3) Make sure all IC's are inserted properly.

      4) Look for solder bridges, especially around IC pins.

   b) Impedance between V_{CC} and V_{SS} less than 1KΩ.

      This condition indicates problems with the memory, control, or I/O power distribution. If the cause cannot be located by inspection, the components must be removed one at a time to isolate the problem.

   c) Impedance between V_{DD} and V_{SS} less than 10KΩ.

      This condition indicates problems around the CDP1802 socket (U9) pin 40. Inspect for short-circuit conditions and verify that the IC has been properly inserted in the socket.

   d) Impedance between V_{LED} and V_{SS} less than 5KΩ.

This condition indicates either an LED inserted backwards; Q1, Q2, or Q3 improperly mounted; or a short circuit. If the cause cannot be located by inspection, the LED's LED drivers, and transistors must be removed to isolate the problem.

2. Incorrect LED display from Step 5.

   a) Verify operation of the CPU as follows:

      1) Apply power.

      2) Put the CONTINUOUS/STEP switch (S4) in the continuous (up) position.

      3) Connect a scope probe to pin 33 of U9 - TPB of the CDP1802.

      4) You should observe a 500-nanosecond pulse at a frequency of 250 KHz.

   b) If the TPB pulse is not observed, the CDP1802 (U9) is not operating. To locate the cause check the following:

      1) Verify power (5 volts) at U9 pins 16 and 40. This should be done with the CPU removed.

      2) Look for short circuits or missed solder connections at the CDP1802 socket.

      3) Verify oscillator operation by observing a 2-MHz waveform on U9 pin 39, or P2-19.

   c) Error on memory address display.

      1) Check the address latch (U8) and verify TPA on pin 11 (same characteristics as TPB in 2.a)4) of this Troubleshooting Guide).

      2) Trace the address lines from the CDP1802 to the address latch and from the address latch to the LED drivers and verify proper operation.

      3) Check for inoperative LED or driver.

d) Error on data bus display.

1) Turn on power and advance to state where display error occurs.

2) Trace the data bus lines from the CPU through the LED drivers and verify proper operation.

3) Check for inoperative LED or driver.

e) Error on CDP1802 status display.

1) Verify that controls are in the proper condition.

2) Trace the CPU status lines (SC1, SC0, CLEAR, WAIT, and Q) from the socket to the LED drivers and verify proper operation.

3) Check for inoperative LED or driver.

3. No prompt character (*) in Step 6.

a) Verify CDP1802 operation by following b)1) and b)2) in the preceding step.

b) Make sure the mode switch (S5) is in the CONTINUOUS (up) position.

c) Trace through the TTY interface - refer to the application note entitled, "Data Terminal Interface Considerations for the RCA Microprocessor Evaluation Kit CDP18S020" in the I/O and Control Application Note section of this Manual.

d) Switch the mode control (S5) to STEP, push RESET, and RUN U. Check that the MA15 LED display is on while the RUN U button is depressed. After 8 steps (on RUN U) the MA15 LED should remain permanently on. If operation is not as described, the Utility Program is not being properly addressed. Trace through the memory address section of the PC card and verify proper addressing and enabling of the memory.

e) If the Q LED flashes but the TTY does not print * after the sequence RESET, RUNU, CARRIAGE RETURN, the TTY connections are incorrect or Q2 or Q3 is not operating correctly. Trace through the TTY interface and verify proper operation.

4. Incorrect response to ?M in Step 7 of the Check-Out Precedure.

   a) CDP1822 RAM's in incorrect location.

   b) General RAM system problem. Trace the RAM section of the PC card for proper selection and operation.

   c) Write protect switch (S5-1) in open position Close switch and repeat test.

5. Incorrect operation of program in Step 8 and 9.

   a) Program improperly loaded.

   b) Control logic problem. Verify proper operation.

Once the problem has been isolated and corrected it is recommended that all steps of the Check-Out Procedure be repeated. If successful, proceed to the Design and Operation section of the manual. If trouble persists and to help in tracing various parts of the system, refer to the Design and Operation section for detailed design information.

CDP18S020 EVALUATION KIT DESIGN

The CDP18S020 COSMAC Evaluation Kit is a complete microprocessor-based computer system. It is intended for use as an evaluation tool for the RCA 1800 series microprocessor family, as a hardware prototype for custom applications, and as a software generation and debugging aid. The Evaluation Kit is organized into seven general sections:

1. CPU
2. Clock
3. Control
4. Display
5. Memory System
6. Input/Output
7. User I/O

Fig. 1-1 in the previous section shows the overall system organization and interconnection of the component sections. The general location of these sections on the PC card is shown in Fig. 1-2. Logic diagrams of the Evaluation Kit are given in Appendix H.

1. CPU

At the heart of the microcomputer system is the CDP1802 COSMAC microprocessor. The CDP1802 is an LSI COS/MOS register-oriented central processing unit designed for use as a general-purpose computing or control element in a wide range of stored program systems.

The CDP18S020 has been designed to assist the user in understanding the basic CDP1802 architecture as well as how to apply the I/O control and data signals provided by the microprocessor. One feature of the Evaluation Kit is the accessibility provided to the CPU. The CPU CONNECTOR (P2) provides direct access to all CPU terminals and can be used to monitor CPU operation or provide an input for a CDP1802 remote emulation function. Refer to Appendix B for the pin assignment of the CPU CONNECTOR.

A detailed description of the CPU architecture and instruction set is provided in the MPM-201 User Manual for the RCA CDP1802 COSMAC Microprocessor supplied with the Evaluation Kit. Electrical specifications can be found in the CDP1802 data sheet in the Data Sheet section of this Manual. It is recommended that the reader study the CPU data flow, state diagram, instruction set, and pin functions before proceeding with the CDP18S020 system design description.

2. CLOCK

The CPU clock is generated by an on-chip crystal-controlled oscillator. There are eight clocks per machine cycle and two or three machine cycles per instruction.* Therefore, the instruction time is 16 or 24 clock periods. A 2-MHz crystal has been provided with the Kit to permit operation of the system over the full recommended voltage range. With a 2-MHz clock, the instruction time is (500 ns) (16) = 8 microseconds or (500 ns) (24) = 12 microseconds. The 8-microsecond instruction time applies to all instructions except the long branch and long skip instructions which take 12 microseconds.

Much faster instruction times are possible. For example, a 6.4-MHz clock frequency at 10 volts results in 2.5 and 3.75 microsecond instruction times. Other frequencies can be used - see the CDP1802 data sheet for maximum clock frequency versus supply voltage. There is no minimum frequency required since the CDP1802 is a static device.

The CDP18S020 clock generator circuit is shown in Fig. 2-1. The on-chip CDP1802 oscillator amplifier is used with a 2-MHz crystal to generate the required single-phase clock. R14 is used to bias the oscillator amplifier in the high-gain region. Optional load capacitor connections are provided to enable the user to add trim and stabilizing capacitors to the clock generator.

* A machine cycle is an instruction fetch or instruction execute operation. All instructions require 1 fetch and 1 execute cycle (2 machine cycles) except long branch and long skip which take two execute cycles for a total of 3 machine cycles.

Clock frequency changes with the crystal oscillator can be made by replacing the provided crystal with one of the desired frequency. Alternatively, an external clock can be brought in via CPU CONNECTOR pin W. When using the external clock option it is necessary to remove LK7A and insert LK7B. If the user wants to switch frequently between internal and external clock, a switch can be inserted in the User I/O area to control the clock source. Details of the clock generator design as well as design alternatives are given in the Clock Generator Design Application Note in the I/O and Control Application Note section of this Manual.

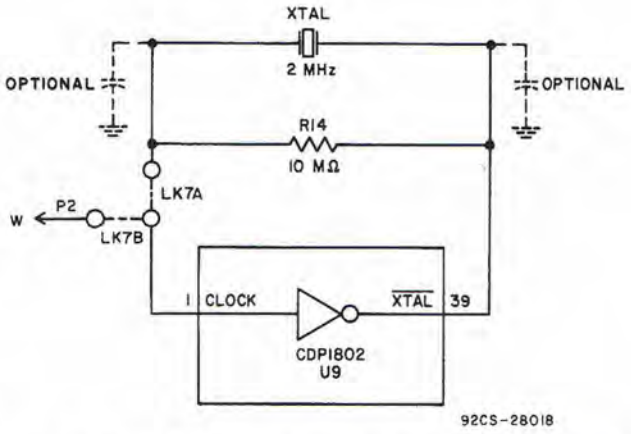


Fig. 2-1 - CDP1802 Microprocessor clock generator circuit.

3. CONTROL

The function of the Control section is to initiate program execution and to facilitate hardware and software debugging. Four controls with associated logic are provided. The first three are momentary contact pushbuttons,

1. RESET SPDT (S2)
2. RUN U SPDT (S3)
3. RUN P DPDT (S4)

and the remaining one is a SPST toggle switch,

4. CONTINUOUS/STEP (S5)

The four controls generate signals which are connected to the $\overline{\text{CLEAR}}$ and $\overline{\text{WAIT}}$ pins of the CDP1802. These pins control the microprocessor modes of operation as follows:

$\overline{\text{CLEAR}}$	$\overline{\text{WAIT}}$	MODE
0	0	LOAD
0	1	RESET
1	0	PAUSE
1	1	RUN

Fig. 2-2 shows the detailed control logic used to interface the four controls with the microprocessor. Refer to Fig. 2-2 in the following discussion.

The RUN U and RUN P pushbuttons are debounced by cross-coupled inverters, and the RESET pushbutton is debounced by an R-S latch. The RESET latch stores the requested clear condition and holds the microprocessor in the RESET mode. When either RUN U or RUN P is activated, the RESET latch is cleared. Program execution begins at location 0000 for RUN P or 8000 for RUN U. (See the description of memory operation for details on generating the 8000 starting address for RUN U.)

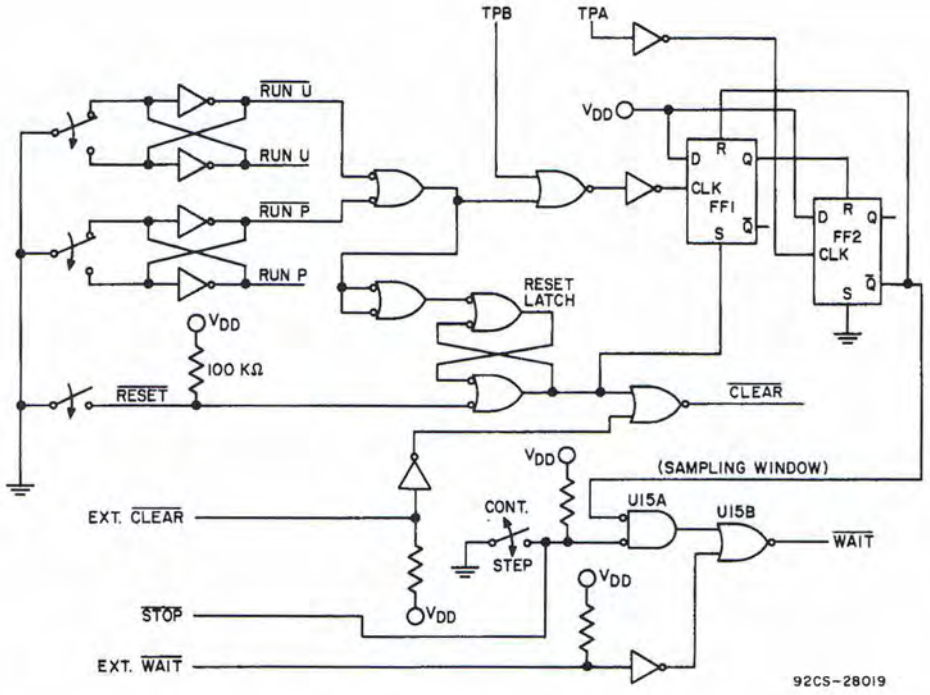


Fig. 2-2 - CDP18S020 control logic.

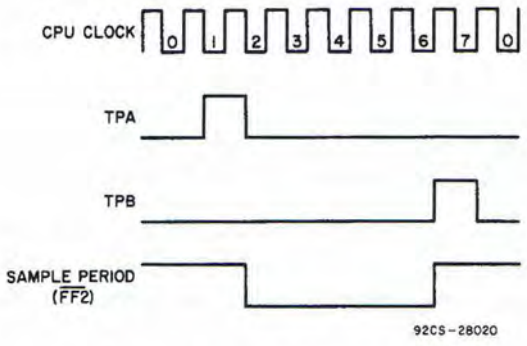


Fig. 2-3 - Control logic timing.

The Evaluation Kit control logic has been designed to permit operation of the system in two general modes; CONTINUOUS - normal run and STEP - single cycle. The CONTINUOUS/STEP toggle switch controls the Evaluation Kit mode.

Mode control is provided by sampling a stop request signal during a specific time period or window. A stop request may be generated by the toggle switch in the STEP position or an external input (a memory address comparison for example) at CPU CONNECTOR (P2) pin Y. The period during which a stop request is acknowledged is shown in Fig. 2-3. This window is the $\overline{Q}$ output of flip flop 2 and is gated with stop request in U15A and U15B to generate the CPU WAIT signal.

To better understand the single step operation it is helpful to first understand how the stop request sample period is generated. Flip flop 2 is set (clocked to 1) on the negative going edge of TPA. The $\overline{Q}$ output of flip flop 2 will be the period used to sample stop requests. Q of flip flop 2 will remain low until the positive edge of TPB. At this time flip flop 1 is clocked to 1 and resets flip flop 2 ($\overline{Q}$ = 1). The timing is shown in Fig. 2-3.

When the logic receives a stop request, the microprocessor is stopped (between TPA and TPB) by being forced into the PAUSE mode. During this time TPA and TPB are suppressed and as a result TPB cannot set flip flop 1 to terminate the window as described above. As long as the stop request is low, the CPU will remain in the PAUSE mode. This condition is provided by the CONTINUOUS/STEP switch in the STEP position. The user can terminate the current cycle by pressing RUN P or RUN U. The choice will depend on whether the user wishes to step through his program in RAM (RUN P) or the Utility Program in ROM (RUN U). The effect of pushing RUN P or RUN U is to clock flip flop 1 high and terminate the sampling period. However, as long as the stop request is valid, the machine will stop in the next cycle at the negative edge of TPA. By switching to the STEP mode and continuously pushing RUN P (or RUN U) the user can sequence through his program one machine cycle at a time and watch the instruction execution on the LED display. Remember that there are two or three machine cycle per instruction; one fetch and one or two execute cycles.

The CDP1802D state code uniquely defines the microprocessor machine cycles, as listed in the data sheet and repeated here:

STATE TYPE	STATE CODE LINES	
	SC1	SC0
S0 (FETCH)	L	L
S1 (EXECUTE)	L	H
S2 (DMA)	H	L
S3 (INTERRUPT)	H	H

In order to return to the CONTINUOUS mode the user switches the CONTINUOUS/STEP switch to CONTINUOUS. This terminates the stop request and the CPU immediately resumes program execution beginning at the current step in the program.

While using the Evaluation Kit in the single step mode, the user should note that the stopping point is early in each machine cycle (just past the negative-going edge of TPA). Therefore, when the state code indicates an instruction execution cycle (S1), the microprocessor has actually been paused "in the process" of executing an instruction. This should not be misconstrued to mean that complete instruction execution has taken place. For example; if the user attempts to step through the fetch and execution of an instruction which loads the output port (65), he will observe that the output port does not latch the data until the machine has been stepped past the execution cycle to the fetch of the next instruction.

4. DISPLAY

Discrete LED displays have been provided with the Kit to display memory address, data bus, and CPU status. Fig. 2-4 shows the driver circuit and driver and LED characteristics.

Referring to Fig. 2-4a, the CD4049 driver interfaces directly with the LED. When IN_1=1, the CD4049 output goes low and sinks current from V_{LED} through the LED diode, turning it on. As a result the LED displays the positive logic state of the signal applied to the input of the CD4049.

The operating characteristics of the driver and display are shown in Figs. 2-4b and 2-4c. At current levels above 1 mA the LED presents a constant voltage drop of 1.6 volts. (This value is a first approximation but is valid for this design because of the low LED dynamic impedance of 1Ω.) When presented as a load to the CD4049 as in Fig. 2-4a, the voltage at the CD4049 is V_{LED}-1.6 volts when the LED is on. This condition is plotted on the CD4049 N-channel output characteristic in Fig. 2-4b and identified as the operating point for V_{LED}=5 volts. As can be seen, the N-channel device is in saturation and will sink 10 mA through the LED. The LED will provide 0.5 millicandles at this current level. The LED driver will dissipate (3.4x10)=34 milliwatts, well within the 100-milliwatt maximum rating of the device. Since there are 6 drivers per CD4049 package, total package dissipation will be (6x34)=204 milliwatts, again well below the 500-milliwatt rating of the package at room temperature.

The design presented above used a V_{LED} supply voltage of 5 volts. The range of V_{LED} should always be restricted as follows:

$$0 \leq V_{LED} \leq V_{CC} + 1.5 \text{ volts}$$

When using V_{LED} voltage levels in excess of five volts, care must be taken not to over dissipate the CD4049 package. This precaution is accomplished by inserting a resistor in series with the CD4049 output.

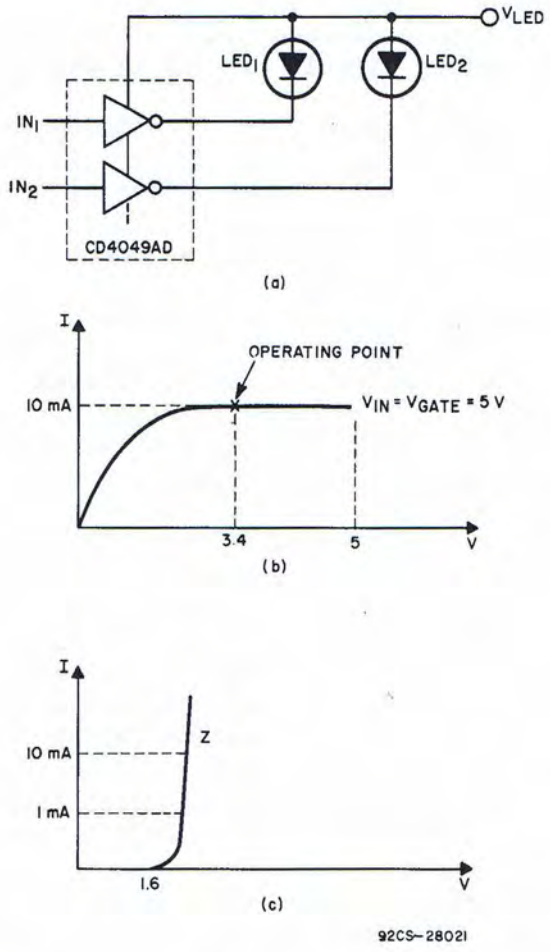


Fig. 2-4 - LED driver circuit.

5. MEMORY SYSTEM

The CDP18S020 Evaluation Kit is provided with an extensive, expandable memory system as follows:

1) 256-byte RAM prewired for expansion to 4096 bytes.

2) 512-byte Utility Program ROM.

3) 32-byte Utility Program RAM

4) Optional 512-byte prewired ROM location.

The memory system interfaces with the CDP1802 microprocessor via address latch, decode, and read/write control logic. The memory system is shown functionally in Fig. 2-5 and the system memory map is shown in Fig. 2-6.

a) General Description

The CDP1802 microprocessor directly addresses 64K of memory. The memory can be any combination of RAM or ROM without restriction. The 16-bit address is multiplexed 8 bits at a time on the 8 memory address lines (MA0-MA7) from the CDP1802. The CPU generates a timing pulse, TPA, during which time the most significant memory address bits, MA15-MA8 (also referred to as the most significant address byte), are present on the 8 address lines. TPA is used to latch the address bits required to form the full memory address. One-half clock period after the termination of TPA, the 8 least significant address bits (MA7-MA0) are multiplexed onto the address bus and will remain stable and valid for the remainder of the machine cycle.

The Evaluation Kit uses a CDP1852 (U8) to latch the most significant byte with TPA. The circuitry for generating a full 16-bit address is shown in Fig. 2-7. Timing for the general address multiplexing cycle is shown in Fig. 2-8. The remainder of the memory system control logic is used to decode the 16-bit address for memory chip selection.

b) Ram System

The Evaluation Kit is provided with a 256-byte CMOS RAM consisting of two CDP1822 256x4 RAM's. The RAM system has been prewired for expansion to 4096 bytes by simply inserting additional CDP1822's in the designated locations. The RAM

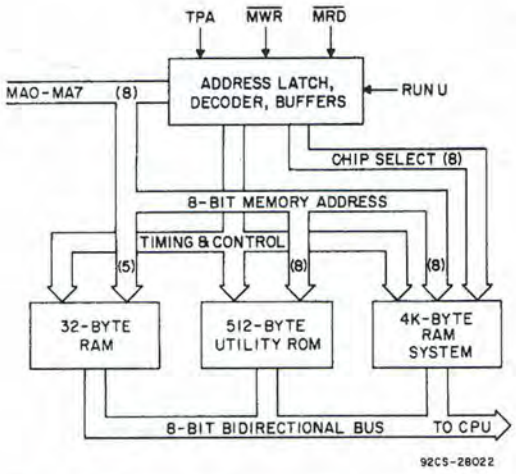
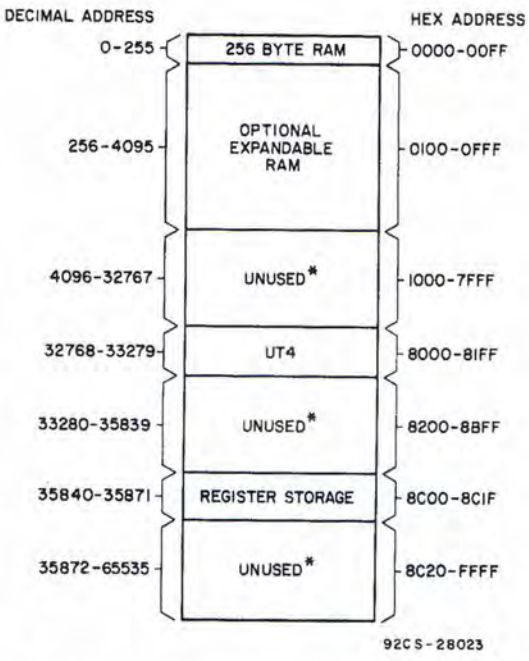


Fig. 2-5 - Evaluation Kit memory system.



* THESE AREAS REQUIRE ADDITIONAL ADDRESS DECODING BEFORE USE.

Fig. 2-6 - Evaluation Kit memory map.

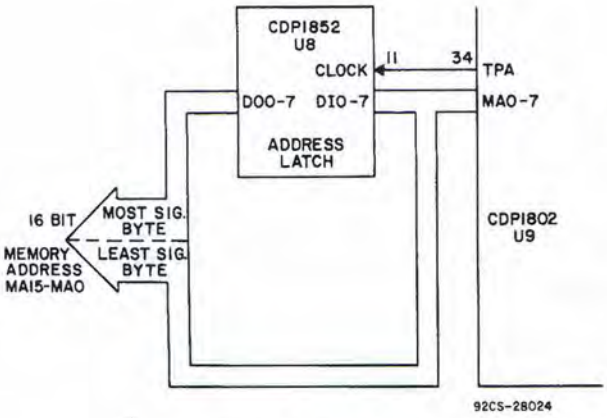


Fig. 2-7 - CDP18S020 address latch.

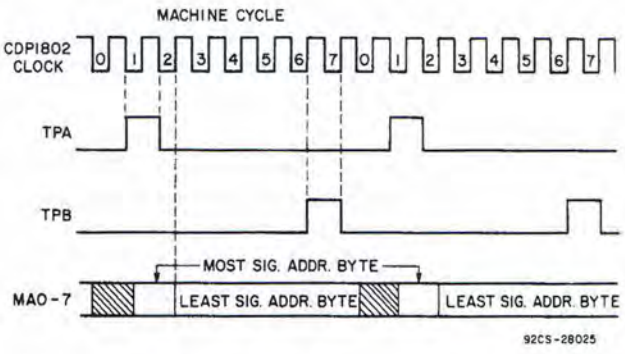


Fig. 2-8 - Address timing.

system is assigned the first 4K locations of the 64K system as indicated in the memory map, Fig. 2-6. Table 2-I gives the memory address in decimal and hexadecimal notation for each RAM location on the Evaluation Kit PC card.

Fig. 2-9 shows the RAM system address decode and select logic. A CD4555 (U22) dual 1 of 4 decoder decodes address lines MA8, MA9 and MA10, MA11 respectively. The 8 decoded outputs drive a CDP1822 4x4 matrix where the column drivers are connected to the CS inputs and the row drivers are connected to the $\overline{CS}$ inputs of the CDP1822's. Coincidence of CS=1, $\overline{CS}$=0 selects a given 256-byte pair of RAM's corresponding to one of 16 256-byte RAM sectors designated by the four memory address lines MA8-MA11. The 8 least significant address lines (MA0-MA7) are connected to all CDP1822 RAM's and specify one of 256 memory locations in the selected RAM pairs.

It should be obvious that the 4K RAM system decode and select logic does not yet uniquely locate the RAM in the first 4K bytes of memory. As presently described, it will occupy each of 16 4K memory sectors throughout the 64K memory space. This is true because only 12 of the 16 memory address bits have been used to address the memory system. In many applications this number is sufficient because 4K or fewer memory bytes are actually used. However, the Evaluation Kit contains provisions for further uniquely defining the RAM system. First, gate U6-pin 9 is connected to the decoder enable input, U22-pin 15, and will disable the RAM system in the upper half (8000-FFFF) of memory. Second, link 2 (LK2) can be broken and used to gate additional disable conditions to the RAM system. For example, a 1 of 16 decoder could be used to decode MA12-MA15 and the low order output connected (gated) via LK2 to the RAM system enable ($\overline{E}$) U22-pin 15. (Note that U22-pin 1 has the same effect.) The result of this gating would be to restrict the RAM system uniquely to the first 4K bytes of the 64K byte memory space.

The CDP1822 RAM's interface directly to the CDP1802 data bus (BUS0-7). The CDP1802 $\overline{MRD}$ signal connected to the CDP1822 $\overline{MRD}$ input enables data on the data bus at the proper time.

The CDP1802 $\overline{MWR}$ signal is also directly compatible with the CDP1822 R/$\overline{W}$ input for controlling the write operation. However, a provision has been included in the Evaluation Kit for "write protecting" RAM in 1K byte segments. The memory write control ($\overline{MWR}$) is connected to the RAM system through DIP switch S1-1, 2, 3, and 4. When closed, the RAM

TABLE 2-I

CDP18S020 RAM address versus PC card location

PC CARD LOCATION NO.*	HEXADECIMAL ADDRESS	DECIMAL ADDRESS
U24,U25	0000-00FF	0-255
U26,U27	0100-01FF	256-511
U28,U29	0200-02FF	512-767
U30,U31	0300-03FF	768-1023
U32,U33	0400-04FF	1024-1279
U34,U35	0500-05FF	1280-1535
U36,U37	0600-06FF	1536-1791
U38,U39	0700-07FF	1792-2047
U40,U41	0800-08FF	2048-2303
U42,U43	0900-09FF	2304-2559
U44,U45	0A00-0AFF	2560-2815
U46,U47	0B00-0BFF	2816-3071
U48,U49	0C00-0CFF	3072-3327
U50,U51	0D00-0DFF	3328-3583
U52,U53	0E00-0EFF	3584-3839
U54,U55	0F00-0FFF	3840-4095

* The first location interfaces with BUS4-7, the second with BUS0-3.

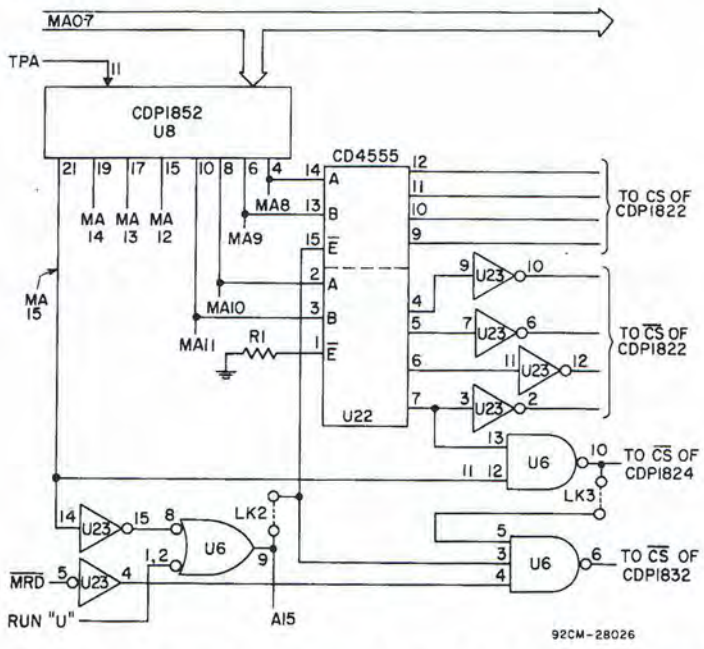


Fig. 2-9 - General address latch and decode logic.

system operates normally for both read and write operations. When open, $\overline{MWR}$ is inhibited from controlling the specified 1K byte RAM segment and forces the RAM to a "read-only" mode. Fig. 2-10 summarizes this operation. In excessively noisy electrical environments when DMA's, branches, and the like go to widely varying locations, it may be advisable to remove the DIP switch and jumper R/$\overline{W}$ to V_{CC} (for protect) or to $\overline{MWR}$ (for write enable) in each 1K byte segment.

For more information on the CDP1822 RAM system design and operation refer to the application note entitled, "Use of CMOS-SOS RAM CDP1822S with RCA Microprocessor Evaluation Kit CDP18S020" in the Memory Application Note section of this Manual.

c) ROM System

The CDP18S020 and CDP18S024 ROM system consists of a CDPR512D, a 512-byte CDP1832 ROM factory programmed with the Utility Program UT4. Because this ROM is a static CMOS device, operation is straight-forward. It is addressed by nine address lines and will put data on the bidirectional data bus within one access time (t_{AA}) of the last address change when selected. A single chip select ($\overline{CS}$) is provided for selecting or enabling the device. The Kit design locates the Utility Program in the upper half of memory. As a result, the chip select logic selects the ROM when A15 (8000) is true. The RUN U pushbutton (S3) forces A15 valid and the result is to select the ROM and begin execution of the Utility Program. A detailed description of the ROM system design is presented in the application note entitled, "Use of CMOS ROM's CDP1831 and CDP1832 with the RCA Microprocessor Evaluation Kit CDP18S020" in the Memory Application Note section of this Manual. The application note also explains how to use the CDP1831 location (U1) for evaluating the CDP1831 512-byte ROM.

Another application note, "Use of Erasable and Electronically Reprogrammable ROM 2704 with RCA Microprocessor Evaluation Kit CDP18S020" explains how the CDP1832 CMOS ROM location (U2) can be used with the 2704.

d) Utility RAM

A CDP1824 32x8 CMOS RAM is supplied in location U3 and used for a register save feature by the Utility Program. It is assigned locations 8C00 to 8C1F. The CDP1824 is compatible with the CDP1802 memory system interface. It is selected by "anding" MA15 (8000) with a decoded 0C00 address state. A detailed description of the CDP1824 RAM interface in the Evaluation Kit is given in the application note entitled, "Use of CMOS RAM CDP1824 with RCA Microprocessor Evaluation Kit CDP18S020" in the Memory Application Note section of this Manual.

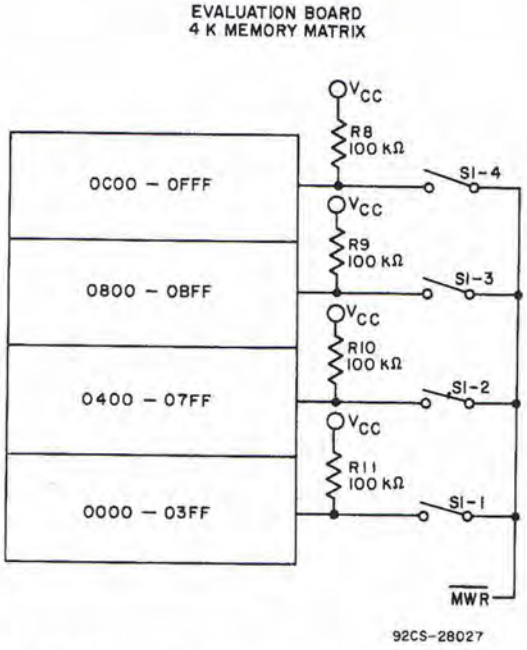


Fig. 2-10 - Memory write protection control.

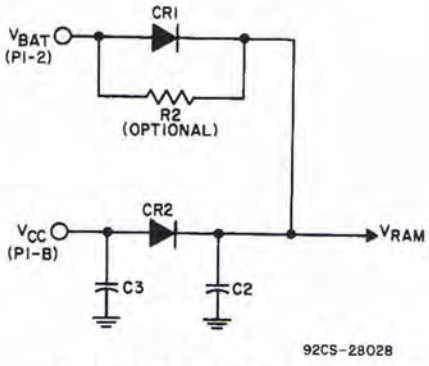


Fig. 2-11 - RAM power connection.

6. INPUT/OUTPUT

The Input/Output section of the Evaluation Kit consists of an 8-bit parallel output port (U4), an 8-bit parallel input port (U5), a 1 of 8 (N bit) decoder for selecting I/O devices, such as a paper tape reader and a keyboard. The I/O section has been designed for flexibility, accessibility, and experimentation.

a) Output Port

The output port is designed to respond to CDP1802 programmed output data transfers. The microprocessor I/O instructions are all of the 6N format where N is a variable input or output device select code. For output instructions, N is 1-7. The binary N code is available on CPU pins 17 through 19 for device selection. For example, a 65 is an output instruction since N=5 and will cause the following code to appear on the N lines;

N Line	CDP1802 Pin No.	Logic Level for 65 Instruction	
N2	17	1	MSB
N1	18	0	
N0	19	1	LSB

The circuit configuration for the output port is shown in Fig. 2-12. The CDP1852 8-bit Input/Output Port is programmed as an output port (mode=1) and used to latch output data transfers. The three CDP1802 N lines are connected to the 1 of 8 N-bit decoder (U7). Output "5" (pin 6) from U7 is connected to the CDP1852 chip select input CS2 and used to select the port. The CDP1802 $\overline{MRD}$ output is connected to $\overline{CS1}$ of the output port and used as the second select input. Output data transfers occur between the CDP1802 memory and the output device. Execution of the 65 instruction selects the output port, $\overline{MRD}$=0 during the execute cycle specifies that the transfer is an output transfer, and TPB clocks valid data off the data bus into the output port at the proper time. Fig. 2-13 summarizes the data transfer timing. Data from the output port is available at the SYSTEM CONNECTOR (P1) as indicated in Fig. 2-12.

It should be noted that the N-bit decoder is not necessary for three or less I/O devices. For these cases an N-line can be connected directly to the I/O port chip select input. A detailed description with examples of the

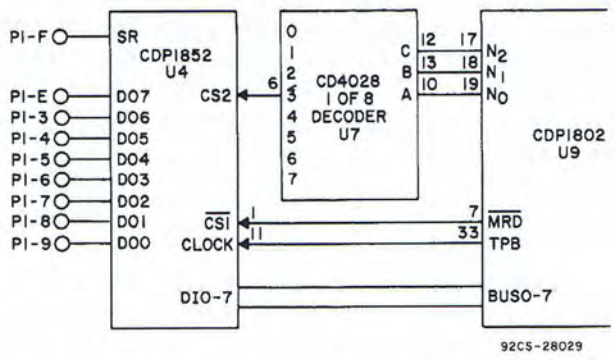


Fig. 2-12 - Output port circuit.

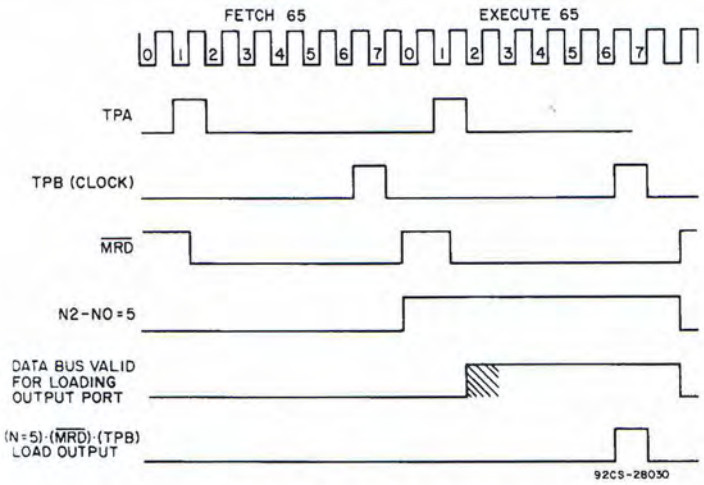


Fig. 2-13 - Output port timing.

CDP1852 I/O port operation can be found in the I/O and Control Application Note section of this Manual in the application note entitled "Use of the CDP1852 8-Bit I/O Port with RCA Microprocessor Evaluation Kit CDP18S020".

b) Input Port

Operation of the input port is similar to that of the output port. The input port is designed to respond to CDP1802 programmed input data transfers. Input instructions are of the format 6N where N is 9-F. In analyzing the seven N codes it can be seen that the three least significant N bits range from 1-7. The N line coding is summarized below.

I/O instruction format 6N

Output instruction 61-67

Input instruction 69-6F

4-bit N field

Output Instruction				Input Instruction			
Binary		Hex 4 Bit	Hex 3 Bit	Binary		Hex 4 Bit	Hex 3 Bit
MSB	LSB			MSB	LSB		
0	001	1	1	1	001	9	1
0	010	2	2	1	010	A	2
0	011	3	3	1	011	B	3
0	100	4	4	1	100	C	4
0	101	5	5	1	101	D	5
0	110	6	6	1	110	E	6
0	111	7	7	1	111	F	7

As can be seen from the above table, the only difference between output and input instructions is the MSB of the four-bit N field. Therefore, the three N-lines (N_2, N_1, and N_0) will respond identically to the 65 and 6D instructions. The most significant N bit indicates the direction of the transfer. It turns out that this N line is identical to $\overline{MRD}$ during execution of I/O instructions; $\overline{MRD}$=0 for output instructions and $\overline{MRD}$=1 for input instructions. Therefore, by gating MRD with the N lines, device selection and direction can be uniquely defined.

The circuit configuration for the input port is shown in Fig. 2-14. The CDP1852 is programmed as an input port (mode=0) and used to hold data for input transfer to the CDP1802 memory and D register. Output "6" (pin 7) from the N-bit decoder is connected to the CDP1852 chip select input CS2 and used to select the port. MRD is connected to the CS1 input and used as a second (direction) select input.

Operation is as follows. Data is loaded into the port by an external device clock. The data inputs and clock signal are available on SYSTEM CONNECTOR pins as indicated. The negative CLOCK transition sets the service request flip flop (SR) to 0. The SR signal can be connected to either EF3 or INTERRUPT of the CDP1802. The user has this option when assembling the Evaluation Kit by inserting a wire jumper across LK4A for INTERRUPT or LK4B for EF3. This allows either an interrupt service routine or software loop (36 for example will cause a branch when EF3=1 which is equivalent to EF3=0) to respond to the service request which is an input data transfer. (Note: The common point of LK4A and LK4B, which is the SR signal of the input port, can in actuality be connected to any flag input of CDP1802 microprocessor. The choice is up to the user. LK4A connecting SR to INTERRUPT and LK4B connecting SR to EF3 have been arbitrarily chosen for the wiring options on LINK 4; however, the user may tie the common point of LINK 4 (input port SR) to any other EF input available at the CPU connector if he so desires.) The CPU, by executing a 6E instruction (during which MRD=1), will enable the input port on the data bus and load M(R(X)) and D with the latched data. At the completion of the 6E instruction execution, the SR signal will be reset to 1. Fig. 2-15 summarizes the input port data transfer timing. Additional details with examples of using the CDP1852 as an input port can be found in the I/O and Control Application Note section of this Manual in the application note entitled "Use of the CDP1852 8-Bit I/O Port with RCA Microprocessor Evaluation Kit CDP18S020".

An interesting example demonstrating the input port operation can be set up on the Evaluation Kit. Enter a 6E instruction at location 0. Switch to STEP operation and push RUN P. This first cycle is an initializing cycle. Push RUN P again to fetch the 6E instruction. Now push RUN P a third time and the LED display should read,

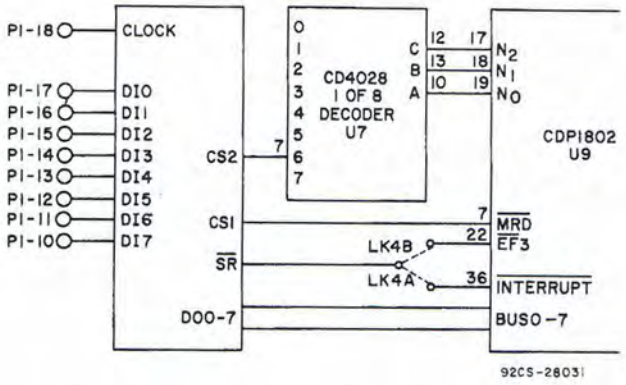


Fig. 2-14 - Input port circuit.

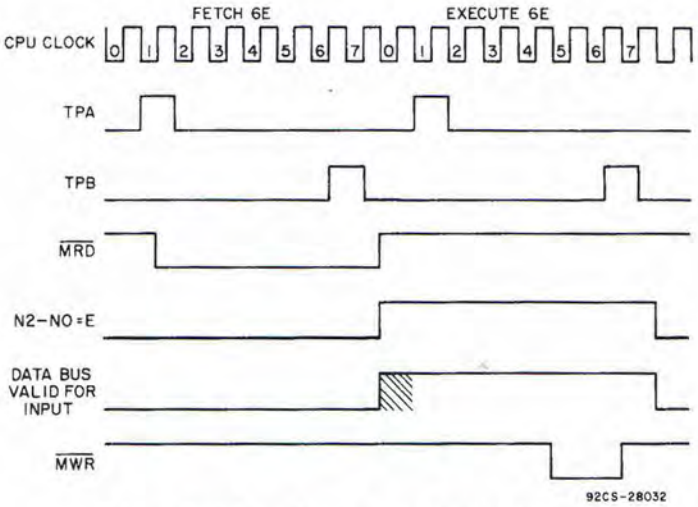


Fig. 2-15 - Input port timing.

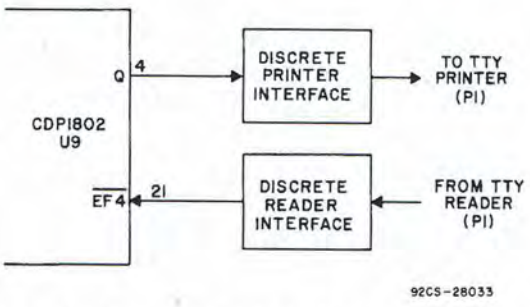


Fig. 2-16 - TTY interface functional diagram.

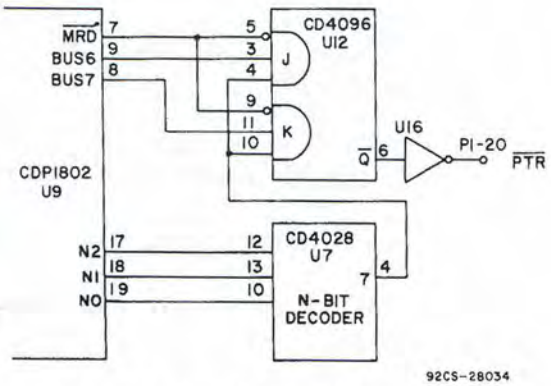


Fig. 2-17 - Paper tape reader interface.

0001	00	1	0	0	1	0
MA	DB	SC1	SC0	$\overline{\text{WAIT}}$	$\overline{\text{CLEAR}}$	0

Next, on the SYSTEM CONNECTOR (P1), connect pin 18 (input port CLOCK - U5, pin 11) to pin B (V_{CC}). This connection puts the input port in the data following mode. All inputs to the port are held low by 22K ohm pull down resistors in RN1. By connecting an input pin to V_{CC}, the corresponding data bus LED should light. For example, on SYSTEM CONNECTOR (P1), connect pin 17 to pin B - the BUS 0 LED should light. Verify the N-bit decoder inputs and outputs to see that the port is indeed selected. This example illustrates the basis of executing any programmed input data transfer.

c) TTY Reader and Printer Interface

The TTY reader and printer interface is shown functionally in Fig. 2-16. The Utility Program UT4 uses the CDP1802 serial output Q (pin 4) as a serial data link to the TTY printer. The discrete printer interface electronics can be optionally configured for either 20-mA current loop or EIA RS232C compatibility. All TTY connections are available at the SYSTEM CONNECTOR pins (P1). For details of the printer interface design and connections, refer to the application note entitled "Data Terminal Interface Considerations for RCA Microprocessor Evaluation Kit CDPS020" in the I/O and Control Application Note section of this Manual.

The Utility Program UT4 uses the CDP1802 external flag $\overline{\text{EF4}}$ (pin 21) to sense serial data input from the TTY reader. The discrete interface electronics between $\overline{\text{EF4}}$ and the TTY can also be optionally configured for 20-mA current loop or EIA RS232C compatibility. Additional design details can be found in the TTY application note. A discussion on how UT4 uses the Q and $\overline{\text{EF4}}$ for serial communication with the CDP1802 can be found in the Utility Program section of this Manual.

d) Paper Tape Reader Interface

The paper tape reader interface circuit is shown in Fig. 2-17. The output $\overline{\text{PTR}}$ is used to turn the reader mechanism ON and OFF. In operation, when a character is to be read, a 67 instruction is executed by UT4 with BUS6=0 and BUS7=1. The result will be to set $\overline{\text{Q}}$ of U12 to one and force $\overline{\text{PTR}}$=0. This starts the read mechanism in the terminal and when UT4 detects a start bit from the reader, a 67 instruction will be executed with BUS6=1 and BUS7=0 to reset $\overline{\text{Q}}$ to zero, force $\overline{\text{PTR}}$=1 and stop the reader at the current character.

7. USER I/O

A unique feature of the CDP18S020 Evaluation Kit is the User I/O area. This area is intended for construction of user-defined memory and I/O systems. It will accomodate any combination of 8, 14, 16, 18, 22, 24, 28 or 40 pin dual-in-line packages. For example, the area can be used to assemble a system consisting of 18 sixteen-pin packages or 12 24-pin packages. To assist in assembling custom memory and I/O systems, convenient access to the CPU data bus (BUS0-7), memory address bus (MA0-7), TPA, TPB, and $\overline{\text{MRD}}$ signals is provided on the left side of the User I/O area. Also provided is an uncommitted USER I/O CONNECTOR for interfacing with external systems, 18 LED locations, and two switch locations. Access to all CPU signals is available from the plated-through holes at the CPU CONNECTOR. This technique can be used generally to access Evaluation Kit signals around the PC card.

The User I/O area will play an important part in personalizing the Evaluation Kit to a specific application. Used together with the prewired memory and control functions, it enables the user to quickly construct and debug prototype microprocessor systems. In addition, future CDP18S020 application notes will describe how to construct specific systems using the User I/O area.

CDP18S020 EVALUATION KIT OPERATION

The CDP18S020 COSMAC Evaluation Kit has been designed for ease of operation. Once assembled, the user has only to connect a terminal and voltage supply to begin operation. This section will summarize the voltage required, primary controls, operating procedure, and general operation of the system.

1. SUPPLY VOLTAGE REQUIREMENTS

The supply voltage requirements for the basic CDP18S020 are as follows:

a) V_{DD}: 3-12 volts; 1-10mA, SYSTEM CONNECTOR PIN L. V_{DD} is the separate CDP1802 supply voltage and is chosen for maximum performance or minimum power.

b) V_{CC}: 3 volts $\leq V_{CC} \leq V_{DD}$, 1-200mA, SYSTEM CONNECTOR PIN B. V_{CC} is the memory and I/O supply voltage and is the same as or less than V_{DD}.

2. OPTIONAL SUPPLY VOLTAGES

The following voltage requirements are optional for the basic CDP18S020:

a) V_{LED}: 5 volts, 400mA, SYSTEM CONNECTOR PIN D. V_{LED} is the LED positive supply voltage. It should be regulated to ±10% and always be less than or equal to V_{CC}, but not greater than +5 volts.

b) V_{BAT}: V_{BAT} is the RAM system hold-up supply voltage and is in the range,

$$3 \leq V_{BAT} \leq V_{CC}$$

It should be left open circuited when not used.

c) -5 volts, 100mA, SYSTEM CONNECTOR Pin 1. This is the negative EIA RS232C interface supply voltage and the substrate bias voltage for the optional 2704 EPROM. Regulate to ±10% without the 2704 and ±5% with the 2704.

d) +12 volts, 100mA, SYSTEM CONNECTOR PIN C. This is the optional 2704 V_{DD} supply and should be regulated to ±5%.

e) V_{TTY}: V_{TTY} is the data terminal interface supply voltage (can be supplied by the V_{LED} supply if LK10 is inserted) and is specified as 100mA, $V_{TTY} \leq V_{CC}$, SYSTEM CONNECTOR PIN H.

3. TTY CONNECTIONS

See Appendix F.

4. PRIMARY CONTROLS

There are four basic controls provided with the Evaluation Kit:

a) RESET (S2) - initializes the CDP1802 and control logic. After RESET, the CPU program counter is R0 and points to memory location 0000.

b) RUN U (S3) - initiates execution of the Utility Program UT4 from memory location 8000 by forcing MA15 to one.

c) RUN P (S4) - initiates program execution from the memory location specified by the current value of the program counter (0000 after RESET).

d) CONTINUOUS/STEP (S5) - a mode control which specifies either CONTINUOUS (normal run) or STEP - single cycle.

5. OPERATING PROCEDURE

The following general procedure should be followed when operating the system.

a) Apply power either coincidentally or in the following order

1) V_{DD}
2) V_{CC}
3) V_{LED}
4) V_{TTY}
5) −5 volts
6) +12 volts

6. OPERATING EXAMPLES

a) The simple four-byte routine presented in section 7 and 8 of the Check-Out Procedure illustrates the basic operation of the Evaluation Kit. The routine sets the CDP1802 output flip flop Q (7B), resets Q (7A), and branches back to repeat the 7B and 7A instructions (30 00).

A flow diagram of the routine is given in Fig. 2-18.

To load the routine (S5 in CONTINUOUS mode).

1) Push RESET
2) Push RUN U
3) Type CR or LF
4) The TTY responds with *
5) Type !M0 7B7A3000 CR

To verify proper loading,

1) Type ?M0 4CR
2) The TTY responds,

```
0000 7B7A3000
*
```

Switch S5 to STEP and push RESET followed by RUN P twice. The system is now reset and by pushing RUN P and observing the LED display you can monitor the system operation as it executes the routine.

Explanation of the routine execution is given in Fig. 2-19.

b) A more complex program is used in section 9 of the Check-Out Procedure to verify proper operation of the Evaluation Kit. This program sets and resets Q and the "on" and "off" duty cycles are programmable. Register 4 (R4) is used as a 16-bit interval timer. For simplicity only the most significant byte (8 bits) is loaded with a delay constant, but a 16-bit decrement is performed on the register until it reaches 0000. At this point, Q is set or reset and a new delay constant is loaded into the most significant byte of R4. The cycle is then repeated. A flow diagram of the program is given in Fig. 2-20.

To load the program (S5 in CONTINUOUS mode),

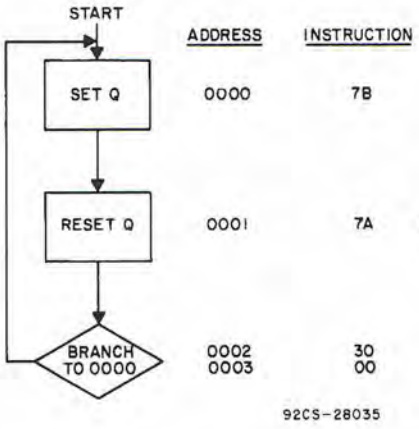


Fig. 2-18 - Flow diagram of simple four-byte routine.

ACTION	DISPLAY STATE					COMMENTS
	MA	DB	SC1 SC0	WAIT CLEAR	Q	
State after Initialization	0000	7B	00	01	0	Fetch 7B (Set Q) from address 0000
Push RUNP	0001	00	01	01	1	Execute 7B and increment R(0) Note: P = 0 after RESET making R(0) the Program Counter
Push RUNP	0001	7A	00	01	1	Fetch 7A (Reset Q) from address 0001
Push RUNP	0002	00	01	01	0	Execute 7A and increment R(0)
Push RUNP	0002	30	00	01	0	Fetch 30 (short branch to location specified in next byte) from address 0002
Push RUNP	0003	00	01	01	0	Execute 30 and increment R(0) Note: The CPU is frozen in the middle of the 30 execute cycle. At the end of this cycle the 00 on the Data Bus will replace the least significant byte (03) in R(0)
Push RUNP	0000	7B	00	01	0	Fetch 7B from address 0000 - branch has been executed.

Fig. 2-19 - Four-byte routine execution description in STEP mode.

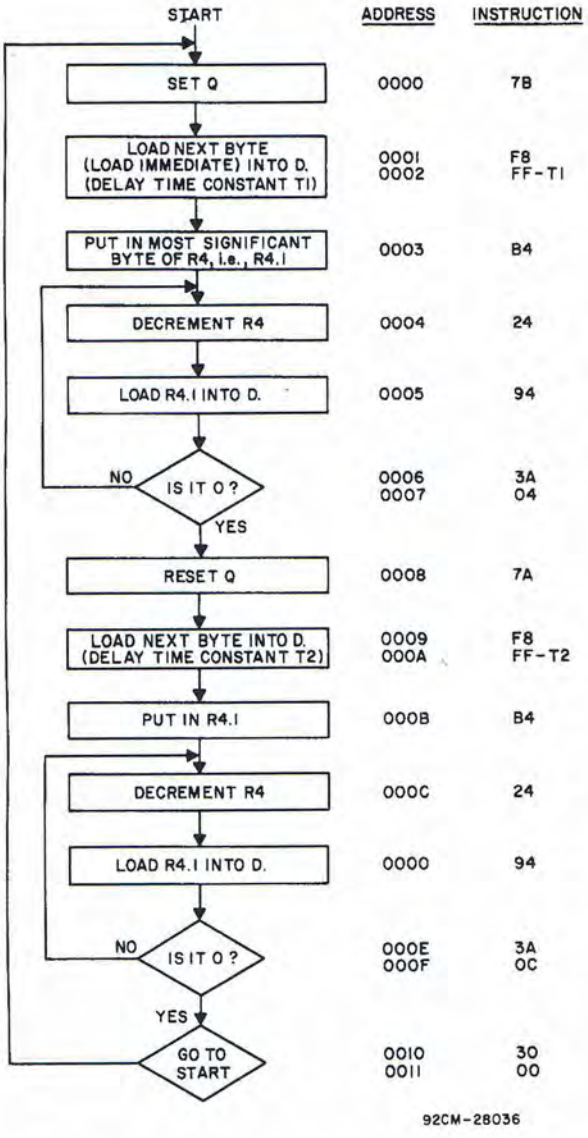


Fig. 2-20 - Flow diagram of Evaluation Kit operation check.

1) Push RESET
2) Push RUN U
3) Type CR or LF
4) The TTY responds with *
5) Type
   !M0 7BF8FFB424943A047AF8FFB424943A0C3000 CR

To verify proper loading,

1) Type ?M0 12CR
2) The TTY responds,

   0000 7BF8 FFB4 2494 3A04 7AF8 FFB4 2494 3A0C;
   0010 3000
   *

To execute the program, push RESET followed by RUN P. The program turns the Q LED off and on with about two seconds between each state change. During execution you will notice the Memory Address display cycling through a counting sequence. This is actually the value of R4 which is displayed during the execute cycle of the 24 and 94 instructions in the time delay loop.

To change the duty cycle of Q,

1) Push RESET
2) Push RUN U
3) Type CR or LF
4) The TTY responds with *
5) Type !M2 yy CR, where yy is the Q "on" time constant T1.

   or

   Type !MA zz CR, where zz is the Q "off" time constant T2.

After making the change, push RESET followed by RUN P to start execution of the program and observe the change in the duty cycle of Q.

7. WHAT NEXT ?

At this point it is possible to start evaluating your particular application on the kit. However, before starting, it is recommended that you review the Check-Out Procedure, Design and Operation, Utility Program, and Application Note sections of this Manual to become more familiar with the system operation and capabilities. Examples and applications are described throughout this Manual to assist you with memory, I/O, and software designs. Some specific experiments or projects you might want to try include:

A) Verify the memory write protect feature of the RAM.

B) Add LED's and LED drivers to the output port to display data transfers.

C) Check the UT4 register save feature.

D) Vary the supply voltage over the recommended 3 to 12 volt range (+10 volts maximum when using CDP1822S memories).

UTILITY PROGRAM UT4*

The CDP18S020 COSMAC Evaluation Kit is supplied with a fixed ROM program, UT4, which gives immediate access to all memory locations and allows the user to begin program execution at any desired point in memory. Capability is provided to load a program from an external source such as the Teletype keyboard, a paper tape, or a timeshare system. Tapes may be punched and used subsequently to reload memory. The various operations are executed through the Evaluation Kit terminal by use of three commands: "?M" to read from memory and/or to punch a reloadable paper tape, "!M" to modify memory contents or to load a program into it, and "$P" to "proceed" with program execution.

In general, after the system has been RESET, the user has two choices: Pressing RUN PROGRAM begins execution of his program at location 0000, while pressing RUN UTILITY begins execution of UT4 (at 8000). After pressing RUN UTILITY, the user next types either a LF (line feed) or a CR (carriage return), depending upon his installation. The latter initiates FULL DUPLEX operation, the former HALF DUPLEX. Besides

---

* NOTE The following discussion, written in terms of a Teletype and its paper tape, may be applied equally to the Silent 700 and its magnetic tape cassettes, if the following text substitutions are made: -

Teletype Terminal	Silent 700 Terminal
Punch.	Write.
Mount paper tape in reader.	Mount cassette. Rewind it and press LOAD/FF to advance to first record.
Turn on tape punch.	Turn Record Control switch ON.
Punch NULL's	Not required.
Press START on tape reader.	Press CONT/START on terminal console.

establishing the need to echo, UT4 uses this input to calculate the timing parameters necessary to run the terminal. Thus, a single program can operate with wide variations in clock speed or terminal speed.

When UT4 is ready to accept a command, it types out a prompt character *.

?M COMMAND

To interrogate memory, the user types a command such as

```
?MF5 3
```

and terminates it with CR carriage return. UT4 responds by printing out the contents of memory beginning at location 00F5: three bytes are printed out as two hex digits each. Each line of output begins with the address, and data is grouped in 2-byte (4-digit) blocks. When necessary, new lines are begun every 16 bytes, with the previous lines ending in semicolons. The user may enter any number of digits to specify the beginning location (leading zeroes are implied, if necessary). If more than four digits are entered, only the last four are used. The number of bytes to be typed out should be in hex. Again, if more than four digits are entered, only the last four are used. This feature allows the user to correct a mistake. He simply keeps typing, putting in the correct 4-digit values (230024 is effectively 0024).

When the user wants to punch a reloadable paper tape, he requests a memory type-out. But, before returning the carriage, he turns on his tape punch and punches several null characters as a header for the tape (using the REPEAT key and CONTROL-SHIFT-P). UT4 ignores the nulls. The resulting tape can be used with the !M command to load memory.

!M COMMAND

In general, data is entered into memory by means of a command such as

```
!M2F 434F534D4143
```

This command enters six bytes (two hex digits each) into memory beginning at location 2F. It is normally

terminated by a CR. Once again, the starting location is determined by the last four digits entered. Data is entered into memory after each two hex digits are typed. If the user types an odd number of digits, the last digit is ignored, and the error message ('?') is typed out.

The !M command provides two options that facilitate memory loading. First, a string of data can be extended from line to line by typing in a comma just before the normal CR. (In this case the user must type CR-LF [carriage return-line feed] before he can begin a new line.) For example:

```
!M23 56789ABC,(CR)(LF)

DEF0123456,(CR)(LF)

3047(CR)
```

enters 11 successive bytes beginning at location 0023. Between successive hex pairs while data is being entered, any non-hex character except the comma (and semicolon, as will be discussed) is ignored. This arrangement permits arbitrary LF's, spaces (for readability), nulls (generated by the utility program or by a time-share system to give the carriage time to return), etc.

As a second optional form of data entry, a string of input data can be terminated by a semicolon (and a CR). The utility program then expects more data to follow on the next line, but preceded by a new beginning address. The line must have the format of an !M command, but with the initial !M omitted. This option provides the mechanism for reading in a paper tape previously punched out as a result of the ?M command. (Recall the format of multiline ?M outputs discussed above.) The user types in !M, positions the paper tape in its header section, and presses START on the tape reader. (The utility program ignores all non-hex characters following !M, which allows the CR, LF, and nulls to be input from the Teletype without disturbing the !M command.) Note also that the semicolon feature on input allows non-contiguous memory areas to be loaded.

$P COMMAND

A third utility command is $P. For example

```
$P6C
```

starts execution at location 6C with R0 as the program counter* (after the user presses CR and the utility program provides a LF). The last-four-digits-in rule applies to the address typed in.

SUMMARY OF COMMAND USAGE

In summary, after receiving the prompt character, '*' the user may type

?M [address] Δ [count] CR

!M [non-hex] [address] Δ[data] [optional , or ;] CR

(where the data may have non-hex digits between each hex pair)

or

$P [address] CR

UT4 ignores initial characters until it detects ?, !, or $. Then, inputs which are not compatible with the above formats cause an error message.

SUMMARY OF UT4 OPERATING INSTRUCTIONS

A further detailed summary of these basic operating instruction is given below, repeating the information just given in a more concise form.

1. After pressing "RUN UTILITY", the user should press either CR or LF: LF for half duplex, CR for full duplex. This instruction sets up the bit-serial timing and specifies echo or not.

2. UT4 will return * as a prompt.

3. Following*, UT4 ignores all characters until one of ?, $, or ! is typed in.

4. Following ?M or !M, UT4 waits for a hex character. It then assembles an address. If more than four hex digits are typed, only the last four are used. Next, a space is required. Note: Δ denotes a space.

* $P always begins with R0 as program counter and X=0. This arrangement is consistent with the fact that P=0 and X=0 after the CPU is RESET. Refer to the CDP1802 data sheet for other actions of RESET.

a. For ?M addr Δ a hex count must follow (again, only the last four digits are kept), and the command is terminated by CR.

b. For !M addrΔ data must follow. An even number of hex digits is required. Before each hex pair arbitrary filler, except for a CR, comma, or semicolon, is allowed. CR terminates the command, unless it is immediately preceded by a comma or, as is generally the case, by a semicolon.

   i. In case of comma CR the user must insert an LF for UT4 to continue to accept data. This procedure is a form of line continuation.

   ii. In case of a semicolon all following characters are ignored until the CR is typed. Then, the user must again provide an LF, and UT4 continues as if it had received optional filler, then a starting address, then a space, and then data.

   iii. The !M command can be followed by as many continuation lines as needed, mixed between the two types if desired, and is finally terminated with a CR not preceded by a comma or semicolon.

5. Command $P must be followed by starting address (last four digits used if more than four are typed in). If no address is entered, 0 is assumed. Program execution begins at this location with R0 as program counter with X set to 0.

6. When a !M or ?M command is accepted and completed, UT4 types another prompt character.

7. When UT4 detects bad syntax, it types out a ? and returns the carriage. If a mistake is made when data is entered (by typing in an odd number of digits), all data will have been entered except the last hex digit. Note that the "only-last-four digits" rule in the address field allows the user to correct an error without retyping the whole command. For example, a mistaken 234 can be corrected by continuing 2340235=0235. A bad command can be aborted by typing in any illegal character except after !M or ?M or between input hex data pairs. In these cases, the user should type any digit and then, for example, a period.

8. To punch reloadable paper tape, the user should type ?M addr Δ count, then a header of nulls (control-shift-P, ignored completely by UT4), then CR. After the tape is punched, some more nulls should be added at its end.

9. To load a paper tape, the user should type !M, position the tape reader in the header, and turn on the tape reader.

UT4 READ AND TYPE ROUTINES

The UT4 read and type routines allow a calling program to read or type a character from or to a terminal which is connected to the Evaluation Kit through the terminal interface. Their main function is to convert parallel 8-bit ASCII-coded bytes to and from 11-bit serial Teletype codes.

Auxiliary functions allow the user to type a CPU byte as two hex characters or to assemble ASCII input as hex characters in a CPU register.

The routines are designed to allow adaption to various clock speeds and terminal speeds, and to determine whether or not characters read in should be "echoed" (i.e., typed back immediately). For these purposes, a "sub-subroutine" DELAY is included, which provides the necessary bit timing delays to READ and TYPE. A pointer to this routine must be set up before reading and typing. A control constant is assumed to be available in one specific register†, AUX. This constant occupies the upper half of AUX (AUX.1) and has two parts. The least significant bit specifies echo or not (0 denotes echo, 1 denotes no echo). For Teletypes connected in full duplex, the bit should be 0. For Execuports, the bit should be 0 if full duplex operation is employed, and 1 for half duplex.

The remainder of AUX.1 constitutes a timing parameter (TP). TP is calculated as follows:

$$TP = 2x \frac{\text{interval between two serial bits}}{320x(\text{CPU clock period})} \quad **$$

** The factor of 2 comes from the fact that the input serial waveform is sampled over two successive bit times. The factor of 320 comes from the fact that the time between samples is 20 instruction times, with each instruction taking 16 clock periods.

† See Table 3-I and 3-II for the assignment of register numbers and memory addresses to the names mentions here.

where the fraction is rounded to the nearest integer. For example, because a Teletype operates at 10 characters per second and 11 bits per character, for the Evaluation Kit running from the supplied 2.0 MHz crystal,

$$TP = 2 \times \left(\frac{\frac{1\ s}{10\ char} \times \frac{1\ char}{11\ bits}}{320 \times \frac{1\ s}{2.0 \times 10^6}} \right)$$

$$= 2 \times [56.8 \text{ (rounded to 57)}]$$

$$= 114_{10} = 72_{16}$$

For proper operation TP must be equal to or less than 255. Faster terminals or slower clocks can be supported to the extent that round-off errors do not cause bad timing. For example, at 2.0 MHZ and 30 10-bit characters per seconds,

$$TP = 2 \times \left(\frac{\frac{1}{30} \times \frac{1}{10}}{320/2.0 \times 10^6} \right) = 2(20.8) = 42_{10} = 2A_{16}$$

and the round-off error is small (21.0 instead of 20.8). On the other hand, for 2.0 MHz and 1200 characters per second, TP=2(0.521) and the round-off error would be huge

The utility program UT4 uses a subroutine "TIMALC" to generate the operating time constant, using the first character typed in by a user. This routine times the intervals between incoming bits to calculate TP, and reads one bit to determine whether or not to echo. Specifically, if a CR is entered while TIMALC is running, then echoes will be provided; a LF suppresses echoes. In either case, AUX.1 is loaded with the appropriate constant. TIMALC also loads the subroutine pointer for the DELAY routine. The user of TYPE and READ has the option of calling TIMALC or setting up AUX.1 and the pointer to the DELAY routine himself.

All read and type routines and TIMALC use SUB=R3 as their program counter, and return to the caller with SEP5. They can be called directly from a program using R5 as the program counter, or they may be called through the standard subroutine linkage procedure described in the User Manual for The RCA CDP1802 COSMAC Microprocessor, MPM-201 in the Section Programming Techniques under "Subroutine Techniques" (p.54). DELAY uses RC as its program counter.

AUX.1 = RE.1 is reserved for the operating constant (control constant 0 or 1 added to the timing parameter TP) discussed above.

CHAR.1 = RF.1 is used in certain cases to pass the byte being read or typed between the calling routine and these subroutines. When READ is exited, it leaves the input byte in CHAR.1. When TYPE is entered at location TYPE (See Table 3-II)the byte to be typed is taken from CHAR.1.

All routines alter AUX.0 and CHAR.0. They also alter D, DF, and X. The READ routine leaves the input byte in D as well as in CHAR.1, but this byte will be destroyed if the standard subroutine linkage is used.

When TIMALC exits, R3.1 is left holding A.1 (READ) = A.1 (TYPE), but R3.0 is meaningless. When READ exits, R3 is ready for entry at READAH (see Table 3-II). When TYPE exits, R3 is ready for entry at TYPE5 (see same table). When DELAY exits, RC is ready for another call to DELAY.

The READ routine has three entry points -- READ, READAH, and TTYRED. READ acts as described above and has no other side-effects. READAH operates just as READ does, but with the following side-effect. If the character read in is a hex character (0-9,A-F), then the contents of ASL=RD are shifted four bits to the left, and the 4-bit hex equivalent of the input character is entered at the right. DF is then set to 1 on exiting. If the input character is not a hex character, ASL is not affected, but DF is set to 0 on exiting. The TTYRED entry point performs the same functions as the READ entry point but with an additional feature: it controls the paper tape reader. Upon entering at TTYRED, the paper tape reader is turned on by a 67 instruction with an 80 on the data bus. One half-bit time after the start bit is sensed, the reader is turned off by a 67 instruction with a 40 on the data bus. As a result, the reader transmits one character and then stops.

CAUTION: A READ may immediately be followed by another READ, but not by a TYPE. The caller should wait 1.5 bit times first, which he can do by entering TYPE at TYPE5D or by calling DELAY.

The TYPE routine has five different entry points. Three of them simply specify different places to fetch the character from: TYPE types from CHAR.1, TYPE5 types from M(R5) and increments R5, and TYPE6 types from M(R6) and increments R6. TYPE5D is an entry which provides a 1.5 bit delay before going to TYPE5. The purpose of this delay is to let an immediately preceding echoed READ process to completion before typing. TYPE2 is an entry which results in CHAR.1 being typed out in hex form as two hex digits. Each 4-bit half is converted to a ASCII hex digit (0-9,A-F) and separately typed out.

Notice that the READ routines are designed to facilitate repeated calls on READAH, while the TYPE routines are designed for repeated calls to TYPE5. In order to output a string of variable data characters following a READ, given the timing restriction mentioned earlier, it is most logical to call TYPE5D first, using an immediate "punctuation" byte (i.e., non-data such as space, null, etc.) to get the required initial delay and to follow either with repeated calls on TYPE (with the output variable data characters deposited into CHAR.1) or repeated calls on TYPE5 using immediate data characters. This procedure permits a maximum output character rate.

The DELAY subroutine assumes that the calling program counter is R3. It uses the value, n, of the immediate byte at M(R3) to generate a delay equal to

$$[20+m(2n+6)] \text{ instruction times,}$$

where m is the 7-bit time constant in AUX.1 (see previous discussion). It then increments R3 past the calling parameter and returns via a SEP R3.

Table 3-I and 3-II summarize the register utilization and entry points for UT4.

UT4 REGISTER STORAGE FEATURE

UT4 provides for storing in RAM 13 1/2 of the 16 CDP1802 scratch-pad registers. The CDP1824 32-byte RAM in location U3 has been provided with the Evaluation Kit for this function. The RAM occupies addresses 8C00 - 8C1F. By pressing RESET followed by RUN U, registers R0 - RF are automatically stored in the CDP1824, in numerical order, most significant byte first. R0, R1, and R4.1 are altered in the process.

By using the command

```
?M8C00 20
```

the register contents which existed in the microprocessor at the instant that RESET was pressed preceding the depression of RUN U can be examined. It should be remembered that UT4 uses registers R0, R1, R3, R4.1, R5, and RC - RF. These registers, therefore, will be modified. Should the user wish to continue program execution, he must initialize these registers, by program if necessary. A sample listing is given in Fig. 3-1. It should be recalled that R0, R1, and R4.1 are not correct.

THE BIT SERIAL TERMINAL INTERFACE

The serial terminal interface is an example of minimizing hardware complexity by the use of software. Further, it illustrates the increased flexibility that can be more readily achieved by software. The CPU receives serial data by sampling $\overline{EF4}$. It transmits serial data via its Q output. Details on the electrical I/O interface are given in the Application Note entitled "Data Terminal Interface Considerations for RCA Microprocessor Evaluation Kit CDP18S020."

The sample character waveform in Fig. 3-2 helps to show what the interface software must do. Each character is framed by a START bit and one or two STOP bits. On input, this signal is tied to $\overline{EF4}$ which is sensed by UT4 at the

```
            R0     R1     R4.1
?M8C00 20  /     /      /
8C00 D0D0 8202 2222 3333 9444 5555 6666 7777;
8C10 8888 9999 AAAA BBBB CCCC DDDD EEEE FFFF
*
```

Fig. 3-1 - Sample listing illustrating register storage.

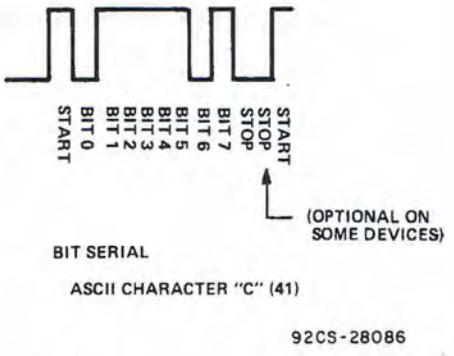


Fig. 3-2 - Sample character waveform.

midpoints of each of the bits. Software assembles the resultant ASCII character. On output, the character is transmitted one bit at a time through the Q output of the CDP1802.

The flexibility obtainable with software is demonstrated by the ability of the program UT4 to sample a character string and adjust its timing so as to cope with terminals of different, even non-standard, character rates. However, it should be noted that while a program is timing either input or output in this manner (i.e., by counting instruction executions), it is completely dedicated to that task and cannot be interrupted except for an occasional DMA service.

Examples of the use of UT4 are given in Appendix E of this Manual.

Table 3-I - UT4 register utilization

REGISTER NAME	REGISTER NUMBER	FUNCTION and COMMENTS
PTER	R0	Altered by UT4 while storing registers.
CL	R1	
SUB	R3	Program counter for all READ, all TYPE, and TIMALC routines.
PC	R5	Program counter for UT4, which calls the routines above.
DELAY	RC	Program counter for the DELAY routine. Points to DELAY1 in memory.
ASL	RD	Assembled into by READAH (input hex digits).
AUX	RE	AUX.1 holds time constant and echo bit. AUX.0 is used by all READ and TYPE routines and by TIMALC.
CHAR	RF	CHAR.1 holds input/output ASCII character. CHAR.0 is used by all READ and TYPE routines and by TIMALC.

Table 3-II - UT4 entry points.

ENTRY NAME	ABSOLUTE ADDRESS	FUNCTION and COMMENTS
READ	813E	Input ASCII → CHAR.1, D (if non-standard linkage).
READAH	813B	Same as READ. If hex character, DIGIT → ASL (see text).
TTYRED	8140	Same as READ. Controls paper tape reader (see text).
TYPE5D	819C	1.5-bit delay. Then TYPE5 function.
TYPE5	81A0	Output ASCII character at M(R5). Then increment R5.
TYPE6	81A2	Output ASCII character at M(R6). Then increment R6.
TYPE	81A4	Output ASCII character at CHAR.1
TYPE2	81AE	Output hex digit pair in CHAR.1
TIMALC	80FE	Read input character and set up control byte in AUX.1. Initialize RC to point to DELAY1.
DELAY1	80EF	Delay, as function of M(R3) (see text). Then, R3+1 → R3.

NOTES:

1. All routines except DELAY use R3 as program counter, exit with SEP5, and alter registers X, D, DF, AUX, and CHAR.
2. DELAY routine uses RC as program counter, exits with SEP3 after incrementing R3, and alters register X, D, DF, and AUX.
3. READ and READAH exit with R3 pointing back at READAH.
4. All five TYPE routines exit with R3 pointing at TYPE5.
5. As indicated in Table 3-I, ASL = RD, AUX = RE, and CHAR = RF.

UTILITY PROGRAM UT4 LISTING

```
!M
0000 ;                  0001            ORG #8000
8000 ;                  0002        .. UT4 IS A UTILITY PROGRAM TO ALTER
8000 ;                  0003        .. MEMORY, DUMP MEMORY, AND BEGIN PROGRAM
8000 ;                  0004        .. EXECUTION AT A GIVEN LOCATION. THE COMMANDS
8000 ;                  0005        .. ACCEPTED ARE $HHHHH (BEGIN EXECUTION AT THE
8000 ;                  0006        .. SPECIFIED LOCATION WITH R0 AS PROGRAM
8000 ;                  0007        .. COUNTER), !MHHHHH DATA (PUT DATA AT SPECIFIED
.
8000 ;                  0008        .. LOCATION), AND ?MHHHHH HHHH (OUTPUT DATA
8000 ;                  0009        .. FROM SPECIFIED LOCATION FOR SPECIFIC COUNT)
8000 ;                  0010        .. AT THE BEGINNING OF A COMMAND ALL CHARACTERS
.
8000 ;                  0011        .. ARE IGNORED UNTIL A ?,!,OR $ IS
8000 ;                  0012        .. ENCOUNTERED. IN THE ?M AND !M COMMANDS NON
8000 ;                  0013        .. HEX CHARACTERS ARE IGNORED AFTER M UNTIL A
8000 ;                  0014        .. HEX IS READ, THEN THE FIRST NON HEX
8000 ;                  0015        .. CHARACTER MUST BE A SPACE . NON HEX
8000 ;                  0016        .. CHARACTERS BETWEEN HEX PAIRS OF THE DATA IN
8000 ;                  0017        .. THE !M COMMAND ARE IGNORED EXCEPT FOR CR,
8000 ;                  0018        .. SEMICOLON, AND COMMA.
8000 ;                  0019        .. THE BAUD RATE OF UT4 IS DEPENDENT UPON THE
8000 ;                  0020        .. TERMINAL BEING USED. A CR OR LF IS ENTERED
8000 ;                  0021        .. AT THE BEGINNING TO SPECIFY THE APPROPRIATE
8000 ;                  0022        .. DELAY BETWEEN BITS. UT4 WILL ECHO
8000 ;                  0023        .. CHARACTERS IF A CR IS CHOOSEN AS THE
8000 ;                  0024        .. TIMING CHARACTER. ECHOING WILL NOT TAKE
8000 ;                  0025        .. PLACE IF A LF IS INPUT AS THE TIMING
8000 ;                  0026        .. CHARACTER.
8000 ;                  0027        .. UT4, AT INITIATION, STORES, ALL REGISTERS
8000 ;                  0028        .. BETWEEN 8C00 AND 8C1F IF IT FINDS RAM THERE
8000 ;                  0029        .. (BUT R0, R1, AND R4.1 ARE CLOBBERED).
8000 ;                  0030          PTER=#00    ..AUXILIARY FOR MAIN ROUTINE
8000 ;                  0031            CL=#01    ..CLOBBERED
8000 ;                  0032            ST=#02    ..STACK POINTER-ONLY
8000 ;                  0033                      ..REFERENCE TO RAM
8000 ;                  0034          SUB=#03      ..SUBROUTINE PC
8000 ;                  0035            PC=#05    ..MAIN PROGRAM COUNTER
8000 ;                  0036        SWITCH=CL     ..DISTINGUSHES BETWEEN ?M AND !M
8000 ;                  0037         DELAY=#0C    ..DELAY ROUTINE PROGRAM COUNTER
8000 ;                  0038           ASL=#0D    ..HEX ASSYMBLY REG ON INPUT,
8000 ;                  0039                      ..AUX FOR HEX OUTPUT
8000 ;                  0040        CENTER=ASL    ..USED TO COUNT OUTPUT BYTES
8000 ;                  0041           AUX=#0F    ..AUX.1 HOLDS BIT-TIME CONSTANT
8000 ;                  0042          CHAR=#0F    ..CHAR.1 HOLDS I/O BYTE
8000 ;                  0043        ..
8000 ;                  0044        .. ENTER IN R0
8000 C4;                0045          NOP
8001 F880B0;            0046          LDI A.1(UT4) ;PHI R0 ..SET PC WHILE
8004 ;                  0047                               ..FINGER IS ON
8004 ;                  0048        ..
8004 ;                  0049        .. THE FOLLOWING WRITES REGISTER CONTENTS INTO
8004 ;                  0050        .. 8C00-8C1F IF IT EXISTS. 8BFF IS ASSUMED NOT
.
                                        (ELSE ROUTINE OVERRUNS).
                                    PHI CL    ..CL IS CLOBBERED
                                              ..BY THIS ROUTINE
                                    PLO CL    ..SET UP WHERE RF.0
                                              ..IS TO GO, MINUS 1
                                    PHI R4    ..R4.1 STORES A MODIFIED
```

```
800D ;              0057                          ..INSTRUCTION
800D F1;            0058          SEX CL
800F F8D051;        0059  LOOP2: LDI #D0 ;STR CL   ..SET UP SEP INSTRUCTION
.
8011 ;              0060                          ..FOR RETURN
8011 F3;            0061          XOR             ..CHECK THAT IT WROTE
8012 3A29;          0062          BNZ UT4         ..
8014 21;            0063          DEC CL          ..PREPARE FOR MODIFIED
8015 ;              0064                          ..INSTRUCTION
8015 94FC70;        0065          GHI R4  ;ADI#70 ..SEE IF IT IS IN THE 90'S
.
8018 331C;          0066          BDF *+#04
801A FC21;          0067          ADI#21          ..IF NO,8N BECOMES 9N
801C FC7F;          0068          ADI#7F          ..IF YES, 9N BECOMES 8(N-1)
.
801F B451;          0069          PHI R4   ;STR CL   ..SET MODIFIED INSTR
8020 ;              0070                          ..INTO RAM
8020 F3;            0071          XOR           ..CK THAT IT WROTE
8021 3A29;          0072          BNZ UT4
8023 D1;            0073          SEP CL          ..GO TO EXECUTE INSTR
8024 ;              0074                          ..(80-9F)
8024 51;            0075          STR CL          ..STORE RESULT IN RAM
8025 2121;          0076          DEC CL  ;DEC CL ..BACK UP FOR NEXT BYTE
8027 300F;          0077          BR LOOP2
8029 ;              0078       ..
8029 90B5B3;        0079  UT4:GHI R0     ;PHI PC   ;PHI SUB  ..#80->PC.1
802C ;              0080                              ..AND SUB.1
802C F830A5;        0081          LDI A.0(UT4A)     ;PLO PC   ..
802F D5;            0082          SEP PC
8030 F5;            0083  UT4A:SEX PC
8031 7155;          0084          DIS,#55         ..NOTE PC=5 ASSUMED
8033 ;              0085                          ..HERE!
8033 6101;          0086          OUT 1,#01     ..SELECT RCA GROUP
8035 F8FEA3;        0087          LDI A.0(TIMALC)   ;PLO SUB     ..READ ONE
8038 ;              0088                              ..TO SET TIMER
8038 D3;            0089          SEP SUB
8039 ;              0090       .. ,
8039 ;              0091       ... INITIATION NOW DONE
8039 ;              0092       ..
8039 F89CA3;        0093  START:LDI A.0(TYPE5D) ;PLO SUB
803C D30D;          0094          SEP SUB; ,#0D       ..CR=CARRIAGE RETURN
803E D30A;          0095  ST2:SEP SUB; ,#0A  ..LF=LINE FEED
8040 D32A;          0096          SEP SUB; ,#2A     ..* AS PROMPT CHARACTER
8042 F800ADAD;      0097  IGNORE:LDI #00;PLO ASL;PHI ASL     ..PREPARE TO
8046 ;              0098                                    ..INPUT HEX
8046 ;              0099                          ..DIGITS,CLEAR ASL
8046 F83BA3;        0100          LDI A.0(READAH) ;PLO SUB
8049 D3;            0101          SEP SUB       ..INPUT COMMAND
804A FB24;          0102          XRI #24               ..IS IT $ ?
804C 32D6;          0103          BZ DOLLAR
804E FB05;          0104          XRI #05       ..IS IT ! ? (TEST WITH $.XOR.!)
.
8050 A1;            0105          PLO SWITCH    ..AND SAVE RESULT
8051 CE;            0106          LSZ           ..EQIV. TO BR RDARGS
8052 FB1E;          0107          XRI #1E       ..IS IT ?
8054 ;              0108                          ..?(TEST WITH $.XOR.!.XOR.?)
.
8054 3A42;          0109          BNZ IGNORE ..IGNORE ALL UNTIL A COMMAND IS
8056 ;              0110                     ..READ
8056 ;              0111       ..
```

```
8056 ;              0112      ..THE FOLLOWING IS COMMON FOR ?M AND !M
8056 ;              0113      ..(SWITCH.0 =0 FOR THE LATTER)
8056 ;              0114      ..
8056 D3;            0115  RDARGS:SEP SUB          ..NOTE SUB AT READAH. NOW
8057 ;              0116                          ..READ HEX ARGS
8057 FB4D;          0117          XRI #4D         ..SHOULD BE M
8059 3ACA;          0118          BNZ SYNERR
805B D3;            0119  RD1:SEP SUB
805C 3B5B;          0120          BNF * -#01      ..IGNORE NON HEX CHARS.
805E ;              0121                          ..AFTER M.
805E D3;            0122          SEP SUB
805F 335F;          0123          BDF *-#01       ..READ IN FIRST ARG
8061 ;              0124                         ..(LOCATION IN MEMORY)
8061 FB20;          0125          XRI #20         ..NEXT CHAR SHOULD BE A SPACE
.
8063 3ACA;          0126          BNZ SYNERR
8065 9DB0;          0127          GHI ASL ;PHI PTER
8067 BDA0;          0128          GLO ASL ;PLO PTER  ..PTER NOW POINTS INTO
8069 ;              0129                             ..USER MEMORY
8069 81;            0130          GLO SWITCH         ..LOOK AT SWITCH
806A 32B4;          0131          BZ EX1             ..IF 0 IT WAS !
806C ;              0132                             ..OTHERWISE IT WAS ?
806C ;              0133      ..THE FOLLOWING DOES (?M LOC COUNT) COMMAND
806C ;              0134 ..
806C F800ADBD;      0135          LDI #00 ;PLO ASL ;PHI ASL  ..CLEAR ASL
8070 D3;            0136  RD2:SEP SUB
8071 3370;          0137          BDF RD2            ..READ IN SECOND ARG
8073 ;              0138                             ..(NUMBER OF BYTES)
8073 FB0D;          0139          XRI #0D            ..NEXT CK FOR CR
8075 3ACA;          0140          BNZ SYNERR
8077 F89CA3;        0141          LDI A.0(TYPE5D) ;PLO SUB    ..TYPE
807A BDA1;          0142          GLO ASL            ;PLO SWITCH
807C 9DB1;          0143          GHI ASL            ;PHI SWITCH
807E D30A;          0144  LINE:SEP SUB; ;#0A                  ..LF
8080 90BF;          0145  LINE1:GHI PTER            ;PHI CHAR  ..PREPARE LINE
8082 ;              0146                                       ..HEADING
8082 F8AFA3;        0147          LDI A.0(TYPE2)  ;PLO SUB
8085 D3;            0148          SEP SUB                      ..TYPE 2 HEX DIGIT
.S
8086 B0BF;          0149          GLO PTER    ;PHI CHAR
8088 F8AFA3;        0150          LDI A.0(TYPE2)  ;PLO SUB
808B D3;            0151          SEP SUB                      ..TYPE
808C D320;          0152          SEP SUB; ;#20                ..SPACE
808E ;              0153      ..
808F 40BF;          0154  TLOOP:LDA PTER            ;PHI CHAR  ..FETCH 1 BYTE FOR
.
8090 ;              0155                                       ..TYPING
8090 F8AFA3;        0156          LDI A.0(TYPE2)  ;PLO SUB
8093 D3;            0157          SEP SUB          ..TYPE 2 HEX
8094 21;            0158          DEC SWITCH
8095 81;            0159          GLO SWITCH
8096 3A9B;          0160          BNZ TL3          ..BRANCH IF NOT DONE YET
8098 91;            0161          GHI SWITCH
8099 3239;          0162          BZ START         ..BRANCH IF DONE
809B B0FA0F;        0163  TL3:GLO PTER ;ANI#0F ..IS PTER DIV BY 16
809E 3AA6;          0164          BNZ TL2
80A0 D33B;          0165          SEP SUB; ;#3B ..IF YES TYPE ; THEN
80A2 D30D;          0166          SEP SUB; ;#0D ..CR AND
80A4 307F;          0167          BR LINE
80A6 F6;            0168  TL2:SHR                ..DIV BY 2?
```

```
80A7 33BF;          0169          BDF TLOOP      ..IF NO LOOP BACK, ELSE
80A9 30AC;          0170          BR TLOOP -#02 ..AND THEN LOOP BACK
80AB ;              0171       ..
80AB ;              0172       ..THE FOLLOWING DOES(!M LOC DATA) COMMAND
80AB ;              0173       ..ENTER AT EX1
80AB ;              0174       ..
80AB ;              0175       ..EFFECT OF THE FOLLOWING IS TO READ IN HEX
80AB ;              0176       ..TERMINATING WITH A CR,IGNORING NON-HEX CHARS.
.
80AB ;              0177       ..PAIRS; EXCEPTIONS: A COMMA BEFORE A CR ALLOWS
.
80AB ;              0178       ..THE INPUT TO CONTINUE ON THE NEXT LINE AND A
80AB ;              0179       ..SEMICOLON ALLOWS AN !M COMMAND TO
80AB ;              0180       ..BE ASSUMED.
80AB ;              0181       ..
80AB D3;            0182  EX3:SEP SUB              ..INPUT UNTIL A HEX IS READ
.
80AC 3BAB;          0183          BNF EX3
80AE ;              0184       ..
80AE D3;            0185  EX2:SEP SUB              ..LOOKING FOR SECOND HEX
80AF ;              0186                           ..DIGIT
80AF 3BCA;          0187          BNF SYNERR       ..BR IF NOT HEX
80B1 8D50;          0188          GLO ASL   ;STR PTER       ..**SFT BYTE**
80B3 10;            0189          INC PTER
80B4 D3;            0190  EX1:SEP SUB                       ..NOTE SUB AT
80B5 ;              0191                                    ..READAH
80B5 33AE;          0192          BDF EX2                   ..BR IF HEX
80B7 FB0D;          0193          XRI #0D                   ..CHECK IF CR
80B9 3239;          0194          BZ START
80BB FB21;          0195  EX4;XRI #21                       ..ELSE CK IF COMMA
.
80BD ;              0196                           ..(TEST WITH CR.XOR.,)
80BD 32AB;          0197          BZ EX3      ..IF ELSE BRANCH
80BF FB17;          0198          XRI #17          ..CK FOR SEMICOLON(TEST WITH
.
80C1 ;              0199                           ..CR.XOR.,.XOR.;)
80C1 3AB4;          0200          BNZ EX1          ..IGNORE ALL ELSE
80C3 D3;            0201          SEP SUB          ..ON SEMI IGNORE AL UNTIL CR
.
80C4 ;              0202                           ..THEN LOOP BACK
80C4 FB0D;          0203          XRI #0D
80C6 3AC3;          0204          BNZ *-#03
80C8 305B;          0205          BR RD1           ..THEN BRANCH BACK
80CA ;              0206                           ..FOR !M COMMAND
80CA ;              0207       ..
80CA F89CA3;        0208  SYNERR:LDI A.0(TYPE5D) ;PLO SUB    ..GENERAL
80CD ;              0209                                 ..RESULT OF
80CD ;              0210                                 ..SYNTACTIC ERROR
80CD D30D;          0211          SEP SUB; ,#0D                    ..CR
80CF C0B1FB;        0212          LBR FSYNER                  ..FINISH ERROR MSG
.
80D2 ;              0213       ..
80D2 ;              0214       ..THE FOLLOWING DOES $P HHHH
80D2 ;              0215       ORG #80D6
80D6 D3;            0216  DOLLAR:SEP SUB              ..NOTE SUB.0=READAH
80D7 FB50;          0217          XRI #50             ..SHOULD BE P
80D9 3ACA;          0218          BNZ SYNERR
80DB D3;            0219  D1:SEP SUB
80DC 33DB;          0220          BDF D1              ..ASSEMBLE HEX
80DF ;              0221                              ..STING INTO ASL
```

```
80DF FB0D;          0222          XRI #0D                ..FIRST NONHEX
80E0 ;              0223                                 ..MUST BE CR
80E0 3ACA;          0224          BNZ SYNERR
80E2 9DB0;          0225          GHI ASL    ;PHI R0
80E4 BDA0;          0226          GLO ASL    ;PLO R0     ..SET UP NEXT PC
80E6 F89CA3;        0227          LDI A.0(TYPE5D)    ;PLO SUB
80E9 D30A;          0228          SEP SUB; ;#0A          ..LF
80EB E5;            0229          SEX PC
80EC 7000;          0230          RET;#00             ..AND USER PROGRAM
80EE ;              0231                              ..BEGINS (IN R0)
80EF ;              0232                                 ..EXIT TO UT4
80EF ;              0233       ..
80EF ;              0234       ..
80EF ;              0235       ..
80EF ;              0236       ..
80EF ;              0237       ..SUBROUTINES
80EF ;              0238       ..
80EF ;              0239       ..DELAY ROUTINE
80EF ;              0240       ..DELAY IS 2(1+AUX.1(3+@SUB))
80EF ;              0241       ..USED BY TYPE, READ, AND TIMALC.
80EF ;              0242       ..AUX.1 IS ASSUMED TO HOLD A DELAY CONSTANT
80EF ;              0243       ..=((BIT TIME OF TERMINAL)/
80EF ;              0244       ..(20*INSTR TIME OF COSMAC))-1.
80EF ;              0245       ..THIS CONSTANT CAN BE GENERATED
80EF ;              0246       ..AUTOMATICALLY BY THE TIMALC ROUTINE.
80EF ;              0247       ..
80EF D3;            0248  DEXIT:SEP SUB
80F0 9EF6AE;        0249  DELAY1:GHI AUX ;SHR  ;PLO AUX     ..SHIFT OUT
80F2 ;              0250                                    ..ECHO FLAG
80F2 2E;            0251  DELAY2:DEC AUX             ..AUX.0 HOLDS BASIC
80F3 ;              0252                             ..BIT DELAY
80F3 43FF01;        0253          LDA SUB     ;SMI #01    ..PICK UP A CONSTANT
80F6 3AF4;          0254          BNZ *-#02               ..LOOP AS SPECIFIED
80F8 ;              0255                                  ..BY CALL
80F8 8E;            0256          GLO AUX                      ..DONE YET ?
80F9 32EF;          0257          BZ DEXIT
80FB 23;            0258          DEC SUB                      ..POINTS SUB
80FC ;              0259                                ..AT DELAY POINTER
80FC 30F2;          0260          BR DELAY2
80FE ;              0261       ..
80FE ;              0262       ..ROUTINE TO CALCULATE BYTE TIME AND ECHO
80FE ;              0263       ..FLAG. WAITS FOR LF (NO ECHO) OR CR(ECHO)
80FE ;              0264       ..BE TYPED IN. ALSO SETS UP POINTER TO
80FE ;              0265       ..DELAY ROUTINE.
80FE ;              0266       ..AUX.1 ENDS UP HOLDING, IN THE MOST
80FE ;              0267       ..SIGNIFICANT 7 BITS,THE DELAY CONSTANT.
80FE ;              0268       ..LEAST SIGNIFICANT BIT IS 0 FOR ECHO, 1 FOR
80FE ;              0269       ..NO ECHO
80FE ;              0270       ..
80FE 93BC;          0271  TIMALC:GHI SUB     ;PHI DELAY
8100 F800AEAF;      0272          LDI #00     ;PLO AUX         ;PLO CHAR
8104 F8FFAC;        0273          LDI A.0(DELAY1)              ;PLO DELAY
8107 ;              0274                                ..DELAY ROUTINE READY
8107 3707;          0275          B4 *                   ..WAIT FOR START BIT
8109 3F09;          0276          BN4 *                  ..WAIT FOR FIRST
810B ;              0277                             ..NON ZERO DATA BIT
810B F803;          0278          LDI #03                   ..SET UP FOR
810D ;              0279                               ..10 EXECUTIONS
810D ;              0280                               ..SO ROUND-OFF IS MINIMAL
810D FF01;          0281  TC2:SMI #01
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810F 3A0D;          0282          BNZ *-#02
8111 8F;            0283          GLO CHAR                    ..LOOK TO SEE
8112 ;              0284                                      ..IF DATA
8112 ;              0285                                      ..CHANGED PREVIOUSLY
.
8112 3A17;          0286          BNZ ZRONE                   ..BR IF IT HAD
8114 3719;          0287          B4 INCR                     ..ELSE LOO FOR
8116 ;              0288                                    ..CHANGE TO 0 NOW
8116 ;              0289                                    ..BRANCH IF NO
8116 1F;            0290          INC CHAR                    .. IF YES SET SWITCH
.
8117 371F;          0291  ZRONE:B4 DAUX                       ..LOOK FOR CHANGE
8119 ;              0292                                      ..TO 1, BR IF YES
8119 1F;            0293  INCR:INC AUX
811A F807;          0294          LDI #07                     ..SET UP FOR
811C ;              0295                                       ..20 INSTR. LOOP
811C 300D;          0296          BR TC2
811E ;              0297       ..AUX.0 NOW HOLDS #LOOPS IN 2 BIT TIMES
811E 2F2E;          0298  DAUX:DEC AUX   ;DEC AUX             ..REDUCE COUNT
8120 ;              0299                                      ..TO BALANCE
8120 ;              0300                                    ..FIXED OVERLOAD
8120 ;              0301                                    ..IN CALLING DELAY
8120 BFF901BF;      0302          GLO AUX ;ORI #01 ;PHI AUX          ..LSB AUX.1=
.1
8124 DC0C;          0303          SEP RC; ;#0C                      ..1.5 BIT
8126 ;              0304                                    ..TIME DEAY
8126 3F2C;          0305          BN4 WAIT  ..BR IF LF=>NO ECHO, LSB AUX.1=1
8128 ;              0306
8128 9FFAFF;        0307          GHI AUX   ;ANI#FE
812B BF;            0308          PHI AUX     ..CR=>ECHO, LBB AUX.1=0
812C DC26;          0309  WAIT:SEP RC; ;#26
812F D5;            0310          SEP R5
812F ;              0311  ..
812F ;              0312  ..
812F ;              0313  ..
812F ;              0314  ..READ ROUTINE--READS 1 BYTE INTO CHAR.1.
812F ;              0315  ..WHEN ENTERED VIA READAH,THEN
812F ;              0316  ..IF INPUT IS A HEX DIGIT ITS HEX VALUE
812F ;              0317  ..IS SHIFTED INTO ASL FROM THE RIGHT
812F ;              0318  ..AND DF=1,ELSE DF=0; CLOBBERS CHAR, AUX.0,(ASL
812F ;              0319  ..ON READAH). LEAVES BYTE IN D (BUT CLOBBERED IF
812F ;              0320  ..SUBR LINKAGE IS USED). LEAVES PC AT READAH
812F ;              0321  ..ENTRY POINT; EXITS TO R5.
812F ;              0322  ..
812F ;              0323  ..WARNING:READ PROCESS HAS NOT FINISHED. DO
812F ;              0324  ..NOT TYPE IMMEDIATELY, OR ELSE ENTER TYPE VIA
812F ;              0325  ..TYPE5D
812F ;              0326  ..
812F ;              0327          ORG #812F
812F FC07;          0328  CKDEC:ADI #07      ..CK FOR ASCII DECIMAL INPUT
8131 3337;          0329          BDF NFND
8133 FC0A;          0330          ADI #0A
8135 3387;          0331          BDF FND       ..SUB NET 30
8137 FC00;          0332  NFND:ADI #00        ..SETS DF=0
8139 9F;            0333  REXIT:GHI CHAR      ..CHARACTER INTO D
813A D5;            0334          SEP R5
813B F800;          0335  READAH:LDI #00
813D 38;            0336          SKP       ..SKIP OVER TO READ1
813F 83;            0337  READ:GLO SUB      ..CONSTANT WITH A VALUE >0
813F C8;            0338          LSKP
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8140 F801;          0339  TTYRED:LDI #01
8142 AF;            0340  READ1:PLO CHAR      ..SET ENTRY FLAG
8143 F880BF;        0341  READ2:LDI #80    ;PHI CHAR      ..INITIALIZE
8146 ;              0342                                 ..INPUT BYTE
8146 ;              0343                                    ..WHEN SHIFTED 80
8146 ;              0344                                    ..IS 1, WILL BE DONE
.
8146 E3;            0345          SEX SUB
8147 9FF6;          0346          GLO CHAR    ;SHR      ..DF=1 =>ENTRY VIA TTYRED
.
8149 3B4D;          0347          BNF TTY1-#02
814B 6780;          0348          OUT 7 ,#80      ..READER ON
814D 3F4D;          0349          BN4 *       ..WAIT FOR END OF LAST DATA BIT
814F 374F;          0350  TTY1:B4 *       ..WAIT FOR PRESENT START BIT
8151 DC02;          0351          SEP RC; ,#02      ..DELAY HALF BIT TIME
8153 374F;          0352          B4 TTY1       ..BR IF NO START BIT
8155 9FF6;          0353          GLO CHAR    ;SHR      ..ENTRY VIA TTYRED?
8157 3B5B;          0354          BNF NOBIT       ..BR IF NO
8159 6740;          0355          OUT 7 ,#40
815B ;              0356  ..
815B F2C4;          0357  NOBIT:SEX R2    ;NOP      ..RESET X, AND DELAY
815D 9FF6;          0358  BIT:GHI AUX    ;SHR      ..ECHO ?
815F 3368;          0359          BDF NOECHO      ..BR IF NO
8161 3766;          0360          B4 OUTBIT       ..IS THE BIT A 1 ?
8163 7B;            0361          SEQ         ..SET Q
8164 3068;          0362          BR NOECHO
8166 7A;            0363  OUTBIT:REQ      ..RESET Q
8167 C4;            0364          NOP         ..DELAY
8168 DC07;          0365  NOECHO:SEP RC; ,#07       ..WAIT ONE BIT TIME
816A C4C4;          0366          NOP    ;NOP       ..MORE DELAY
816C 9FF6BF;        0367          GHI CHAR    ;SHR    ;PHI CHAR      ..SHIFT
816F ;              0368                                    ..THE INPUT CHAR
816F 3378;          0369          BDF NEXT      ..BR IF INPUT FINISHED
8171 ;              0370                        ..D=CHAR.1
8171 F980;          0371          ORI#80
8173 3F5B;          0372          BN4 NOBIT       ..BR IF INPUT WAS A ZERO
8175 BF;            0373          PHI CHAR
8176 305D;          0374          BR BIT      ..CONTINUE LOOP
8178 ;              0375  ..
8178 ;              0376  ..
8178 7A;            0377  NEXT:REQ      ..OUTPUT THE STOP BIT
8179 3243;          0378          BZ READ2      ..BR IF D=0, =>CHAR.1
817B ;              0379                        ..IS A NULL
817B 8F;            0380          GLO CHAR      ..CK ENTRY FLAG
817C 3A39;          0381          BNZ REXIT       ..BR IF ENTRY WAS VIA READ
817E 9F;            0382          GHI CHAR
817F FF41;          0383          SMI#41      ..CK FOR ASCII HEX
8181 3B2F;          0384          BNF CKDEC       ..(AT TOP OF ROUTINE)
8183 FF06;          0385          SMI#06      ..CK FOR A THRU F
8185 3337;          0386          BDF NFND
8187 ;              0387  ..
8187 ;              0388  ..
8187 FEFEFEFE;      0389  END:SHL    ;SHL    ;SHL    ;SHL
818B FC08FE;        0390          ADI#08    ;SHL
818E AF;            0391  END1:PLO AUX      ..READY TO SHIFT INTO RD
818F 8D7FAD;        0392          GLO ASL   ;SHLC   ;PLO ASL      ..SHIFT
8192 ;              0393                                    ..LOW HALF
8192 9D7FBD;        0394          GHI ASL   ;SHLC   ;PHI ASL      ..SHIFT
8195 ;              0395                                    ..HIGH HALF
8195 8EFF;          0396          GLO AUX   ;SHL
```

```
8197 3A8E;          0397        BNZ FND1     ..BR IF NOT FINISHED
8199 3039;          0398        BR REXIT
819B ;              0399  ..TYPE ROUTINE--TYPES 1 BYTE FROM @R5!,@R6!,
819B ;              0400  ..OR CHAR.1,OR TYPES A BYTE AS TWO HEX DIGITS
819B ;              0401  ..FROM CHAR.1 FOLLOWS A LINE FEED BY SIX NULLS.
819B ;              0402  ..USES 2 AUXILIARY REGS-AUX AND CHAR-PLUS
819B ;              0403  ..RAM LOCATION @ST.EXITS READY TO TYPE 1 BYTE
819B ;              0404  ..FROM @R5!. EXITS TO R5
819B ;              0405  ..WHEN ENTERED AT TYPE5D,PAUSES TO ALLOW AN
819B ;              0406  ..EARLIER READ TO COMPLETE.
819B ;              0407  ..
819B ;              0408  ..AUX.0 HOLDS OUTPUT CHAR (AT FIRST), THEN
819B ;              0409  ..THE DELAY CONSTANT BETWEEN BITS. CHAR.0 HOLDS
819B ;              0410  ..THE NUMBER OF BITS (11) IN ITS LOWER DIGIT,
819B ;              0411  ..AND IN ITS UPPER DIGIT HOLDS A CODE--
819B ;              0412  ..      0 FOR BYTE OUTPUT
819B ;              0413  ..      1 FOR FIRST HEX OUTPUT
819B ;              0414  ..      2 FOR LST NULL OUTPUT
819B ;              0415  ..      8 FOR LF OUTPUT
819B ;              0416  ..
819B ;              0417        ORG #819C
819C DC17;          0418  TYPE5D:SEP RC; ;#17     ..3 BIT TIME DELAY
819E 38;            0419        SKP      ..SKP TO TYPE5D
819F D5;            0420  TEXIT:SEP R5
81A0 4538;          0421  TYPE5:LDA R5   ;SKP      ..ENTRY FOR UT4
81A2 ;              0422                           ..SKIP TO TYPE
81A2 4638;          0423  TYPE6:LDA R6   ;SKP     ..ENTRY FOR G.P.
81A4 ;              0424                           ..IMMED TH
81A4 9F;            0425  TYPE:GHI CHAR
81A5 AF;            0426  TY1:PLO AUX      ..SAVE BYTE FOR LATER
81A6 FB0A;          0427        XRI#0A      ..IS IT LINE FEED ?
81A8 3ABF;          0428        BNZ TY2
81AA F88B;          0429        LDI#8B      ..(# OF BITS)+(#OF NULLS
81AC ;              0430                    ..TO FOLLOW LF+1)
81AC 30C1;          0431        BR TY3
81AE 9F;            0432  TYPE2:GHI CHAR      ..UT4 ENTRY
81AF F6F6F6F6;      0433  TY4:SHR    ;SHR    ;SHR    ;SHR       ..SHIFT FIRST
81B3 ;              0434                                       ..HEX TO RIGHT
81B3 FCF6;          0435        ADI#F6      ..CONVERT TO HEX
81B5 3BB9;          0436        BNF *+#04      ..IF A OR MORE
81B7 FC07;          0437        ADI#07      ..ADD NET 37
81B9 FFC6AF;        0438        SMI#C6   ;PLO AUX      ..ELSE ADD NET 30
81BC F81B;          0439        LDI#1B      ..10+(# OF BITS)
81BE C8;            0440        LSKP      ..EQUIV. TO BR TY3
81BF ;              0441  ..
81BF F80B;          0442  TY2:LDI#0B      ..(# OF BITS TO OUTPUT)
81C1 AF;            0443  TY3:PLO CHAR      ..SAVE MAIN TALLY VALUE
81C2 ;              0444  ..
81C2 ;              0445  ..
81C2 7B;            0446  BEGIN:SEQ      ..START BIT
81C3 8F;            0447        GLO AUX      ..GET CHAR TO BE TYPED
81C4 AD;            0448        PLO RD      ..SAVE THE CHAR.
81C5 ;              0449                      ..(AUX.0 CLOBBERED)
81C5 DC07;          0450  PREBIT:SEP RC; ;#07    ..WAIT ONE BIT TIME
81C7 ;              0451             ..RETURN FROM DELAY WITH D=0
81C7 2F;            0452                DEC CHAR      ..DEC THE BIT COUNTER
81C8 F5;            0453        SD      ..SET DF=1
81C9 8D76AD;        0454        GLO RD   ;SHRC   ;PLO RD      ..SHIFT
81CC ;              0455                                  ..OUTPUT CHAR
81CC 33D1;          0456        BDF OUT1B      .. BR IF THE BIT IS A 1
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81CE 7B;          0457        SEQ     ..ELSE SET Q TO ZERO
81CF 30D3;        0458        BR OUT1B+#02
81D1 7A;          0459  OUT1B:REQ     ..SET Q TO 1
81D2 C4;          0460        NOP     ..DELAY
81D3 8FFA0F;      0461        GLO CHAR   ;ANI#0F     ..FINISHED TYPING ?
81D6 C4C4;        0462        NOP   ;NOP      ..DELAY(14 INSTR.LOOP)
81D8 3AC5;        0463        BNZ PREBIT      ..BR IF NOT FINISHED
81DA 8FFCFB;      0464  NXCHAR:GLO CHAR   ;ADI#FB
81DD AF;          0465        PLO CHAR      ..SET UP FOR NEXT CHAR
81DF 3B9F;        0466        BNF TEXIT       ..BUT EXIT IF NO MORE
81E0 FF1B;        0467        SMI#1B      ..TEST FOR ALTERNATIVES
81E2 329F;        0468        BZ TEXIT      ..IF JUST TYPED LST NULL
81E4 3BFA;        0469        BNF HEX2      ..IF JUST TYPED FIRST HEX
81E6 ;            0470                     ..JUST TYPED LF OR NULL--
81E6 F800;        0471        LDI#00      ..PREPARE TO TYPE NULL
81E8 30E5;        0472        BR HX22
81EA ;            0473  ..
81EA 8FFA0F;      0474  HEX2:GHI CHAR   ;ANI#0F     ..GET 2ND HEX DIGIT
81ED FCF6;        0475        ADI#F6      ..CONVERT TO HEX
81EF 3BF3;        0476        BNF *+#04       ..IF A MORE
81F1 FC07;        0477        ADI#07      ..ADD NET 37
81F3 FFC6;        0478        SMI#C6      ..ELSE ALL NET 30
81F5 AF;          0479  HX22:PLO AUX      ..STORE CHAR AWAY
81F6 30C2;        0480        BR BEGIN
81F8 ;            0481  ..
81F8 D30A;        0482  FSYNFR:SEP SUB; ,#0A      ..LF
81FA D33F;        0483        SEP SUB; ,#3F       ..?
81FC C0A039;      0484        LBR START
81FF ;            0485        END
0000
UT
```
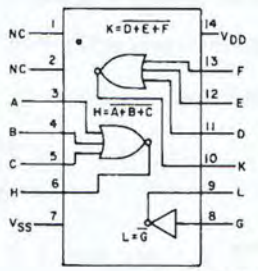

Digital Integrated Circuits

Monolithic Silicon

CD4000UB, CD4001UB CD4002UB, CD4025UB Types



92CS-24757

CD4000UB FUNCTIONAL DIAGRAM

COS/MOS NOR Gates

High-Voltage Types (20-Volt Rating)
Dual 3 Input plus Inverter—CD4000UB
Quad 2 Input-CD4001UB
Dual 4 Input—CD4002UB
Triple 3 Input—CD4025UB

Features:

- **Propagation delay time = 30 ns (typ.) at C_L = 50 pF, V_{DD} = 10 V**
- **Standardized symmetrical output characteristics**
- **100% tested for maximum quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C**
- **5-V, 10-V, and 15-V parametric ratings**

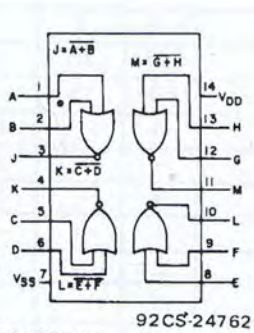
RCA-CD4000UB, CD4001UB, CD4002UB, and CD4025UB NOR gates provide the system designer with direct implementation of the NOR function and supplement the existing family of COS/MOS gates.

The CD4000UB, CD4001UB, CD4002UB, and CD4025UB types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

RECOMMENDED OPERATING CONDITIONS

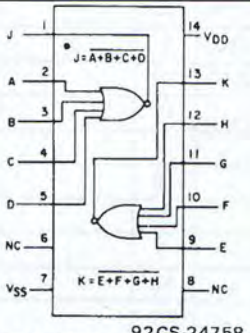
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V



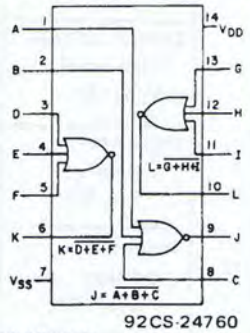
92CS-24762

CD4001UB FUNCTIONAL DIAGRAM



92CS-24758

CD4002UB FUNCTIONAL DIAGRAM



92CS-24760

CD4025UB FUNCTIONAL DIAGRAM

Printed in USA/9-76

Supersedes issue dated 3-76

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,K,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	−	0,5	5	0.25	0.25	7.5	7.5	−	0.01	0.25	μA
	−	0,10	10	0.5	0.5	15	15	−	0.01	0.5	
	−	0,15	15	1	1	30	30	−	0.01	1	
	−	0,20	20	5	5	150	150	−	0.02	5	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	−	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	−	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	−	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	−	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	−	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	−	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	−	
Output Voltage: Low-Level, V_{OL} Max.	−	0,5	5	0.05				−	0	0.05	V
	−	0,10	10	0.05				−	0	0.05	
	−	0,15	15	0.05				−	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	−	0,5	5	4.95				4.95	5	−	
	−	0,10	10	9.95				9.95	10	−	
	−	0,15	15	14.95				14.95	15	−	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	−	5	1				−	−	1	V
	1, 9	−	10	2				−	−	2	
	2, 13	−	15	3				−	−	3	
Input High Voltage, V_{IH} Min.	0.5	−	5	4				4	−	−	
	1	−	10	8				8	−	−	
	2	−	15	12				12	−	−	
Input Current I_{IN} Max.	−	0,18	18	±0.1	±0.1	±1	±1	−	$\pm 10^{-5}$	±0.1	μA

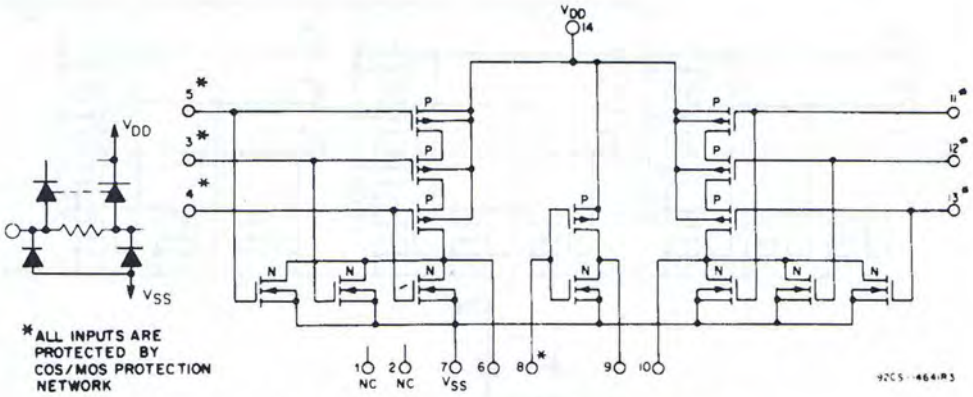


Fig. 1 – Schematic diagram for type CD4000UB.

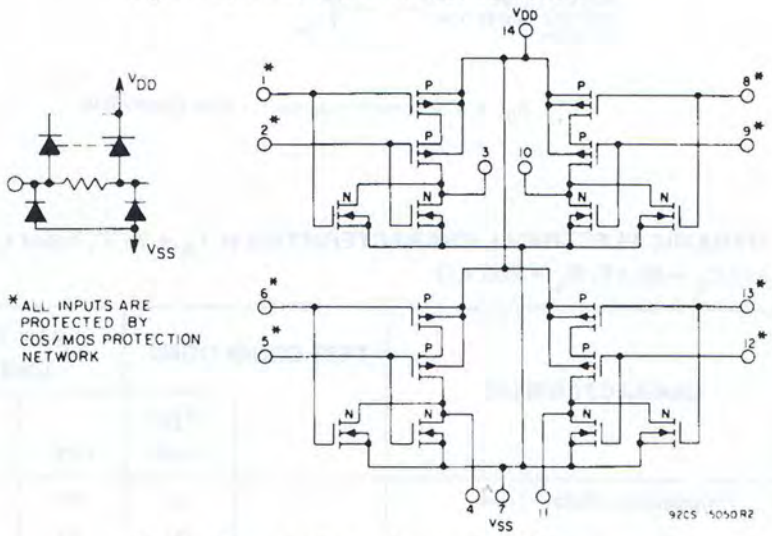


Fig. 2 – Schematic diagram for type CD4001UB.

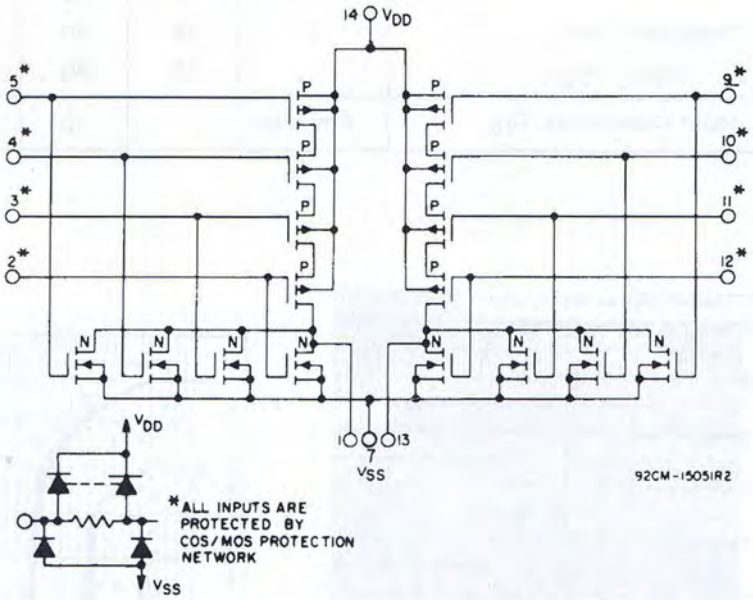


Fig. 3 – Schematic diagram for type CD4002UB.

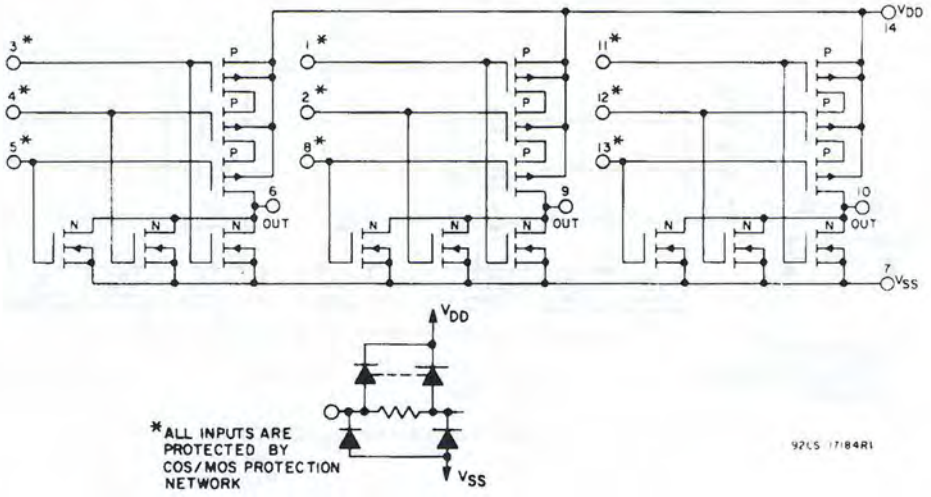


Fig. 4 – Schematic diagram for type CD4025UB.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, and C_L = 50 pF, R_L = 200 KΩ

CHARACTERISTIC	TEST CONDITIONS		ALL TYPES LIMITS		UNITS
		V_{DD} Volts	TYP.	MAX.	
Propagation Delay Time, t_{PHL}, t_{PLH}		5	60	120	ns
		10	30	60	
		15	25	50	
Transition Time, t_{THL}, t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance, C_{IN}	Any Input		10	15	pF

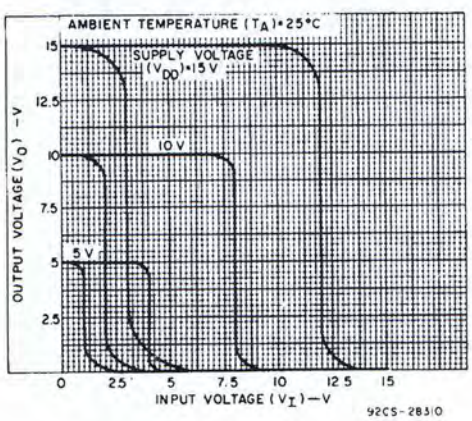


Fig. 5 – Minimum and maximum voltage transfer characteristics.

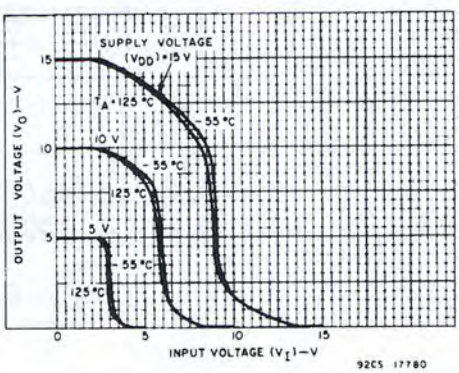


Fig. 6 – Typical voltage transfer characteristics as a function of temperature.

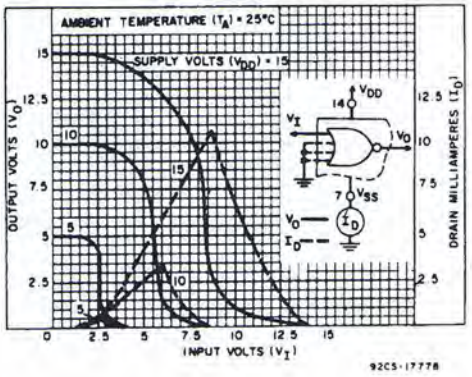


Fig. 7 – Typical current & voltage transfer characteristics.

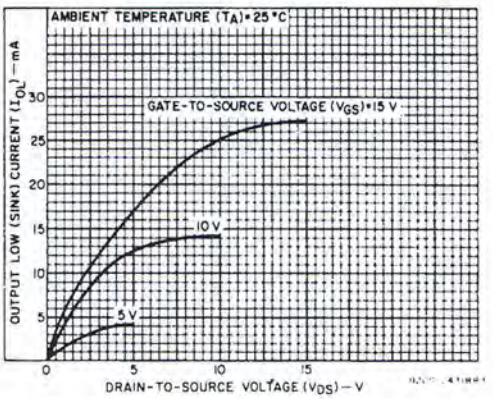


Fig. 8 – Typical output low (sink) current characteristics.

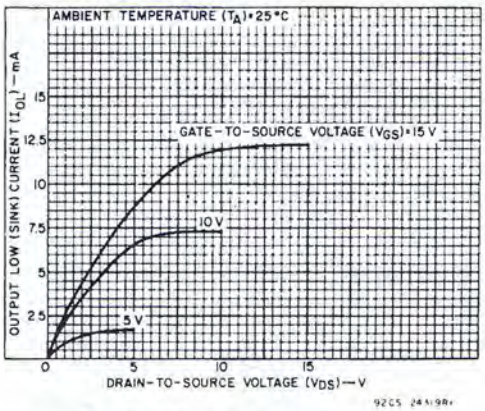


Fig. 9 – Minimum output low (sink) current characteristics.

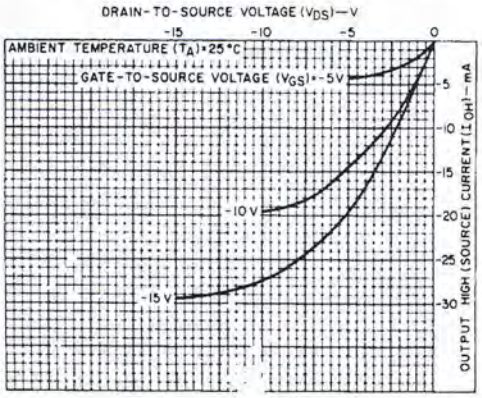


Fig. 10 – Typical output high (source) current characteristics.

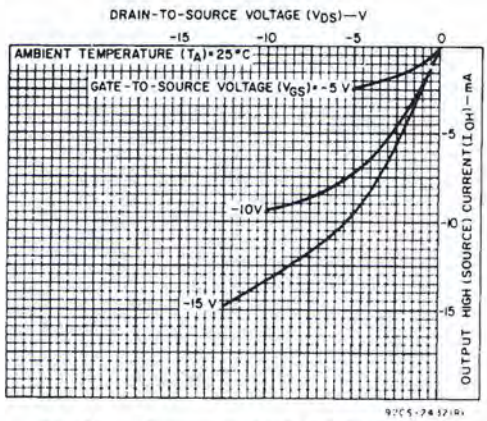


Fig. 11 – Minimum output high (source) current characteristics.

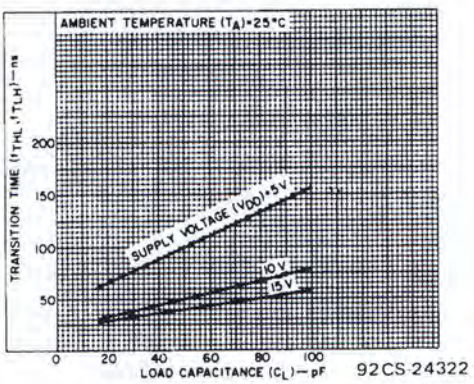


Fig. 12 – Typical transition time vs. load capacitance.

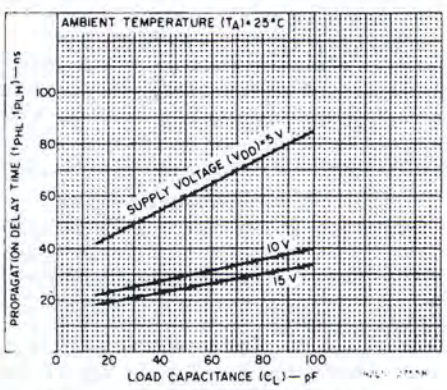


Fig. 13 – Typical propagation delay time vs. load capacitance.

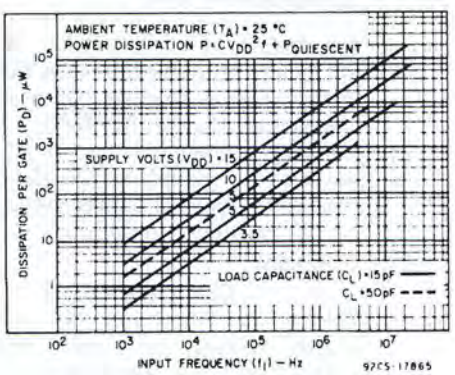


Fig. 14 – Typical power dissipation vs. frequency.

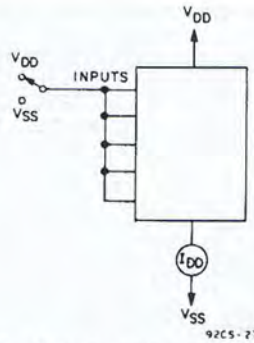


Fig. 15 – Quiescent-device-current test circuit.

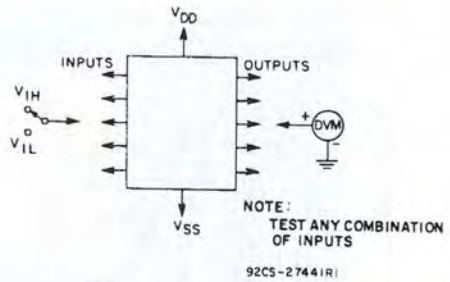


Fig. 16 – Input-voltage test circuit.

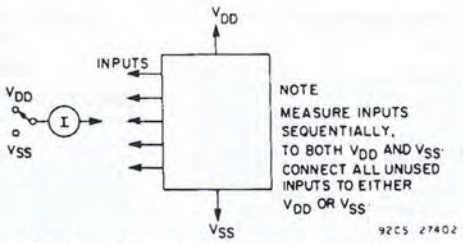
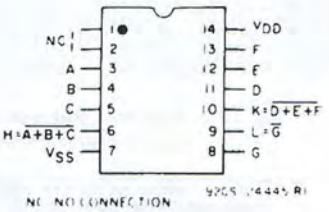
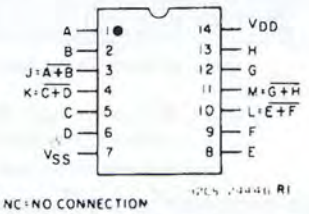


Fig. 17 – Input leakage current test circuit.

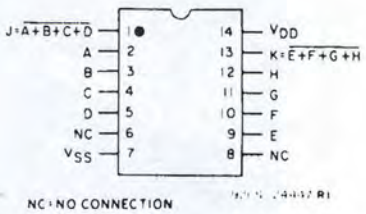
TERMINAL ASSIGNMENTS



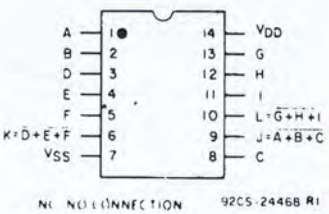
CD4000UB



CD4001UB



CD4002UB



CD4025UB

OPERATING AND HANDLING CONSIDERATIONS

1. **Handling**
   All inputs and outputs of RCA COS/MOS devices have a network for electrostatic protection during handling. Recommended handling practices for COS/MOS devices are described in ICAN-6525, "Guide to Better Handling and Operation of CMOS Integrated Circuits."
2. **Operating**

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause $V_{DD}-V_{SS}$ to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} nor less than V_{SS}. Input currents must not exceed 10 mA even when the power supply is off.

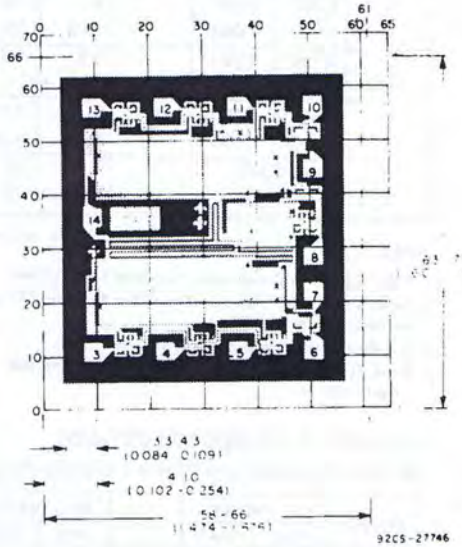
Unused Inputs

A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{DD} or V_{SS}, whichever is appropriate.

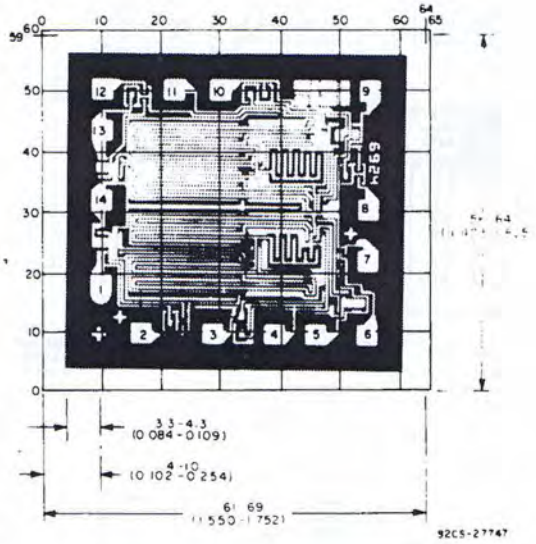
Output Short Circuits

Shorting of outputs to V_{DD} or V_{SS} may damage COS/MOS devices by exceeding the maximum device dissipation.

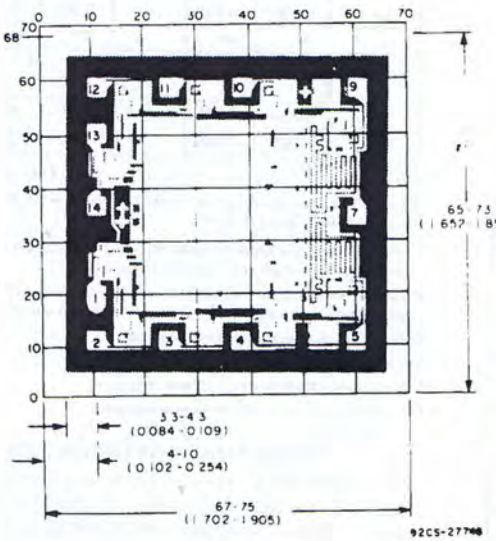
CHIP PHOTOGRAPHS
Dimensions and Pad Layouts



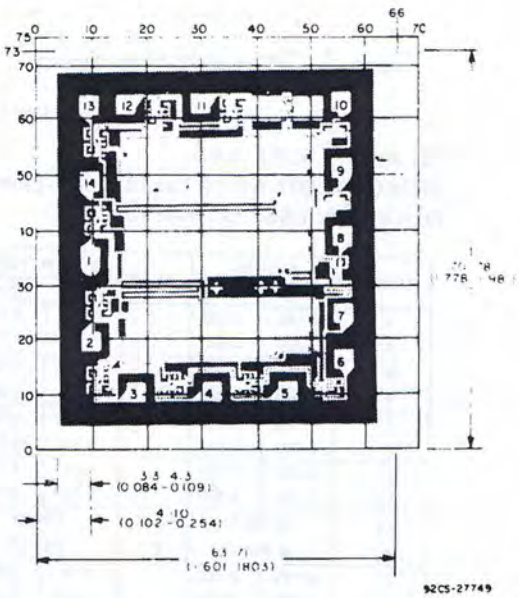
CD4000UB



CD4001UB



CD4002UB

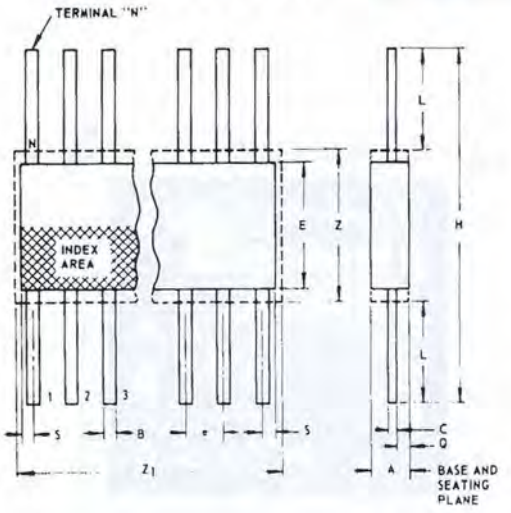


CD4025UB

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

DIMENSIONAL OUTLINES

(K) SUFFIX (JEDEC MO-004-AF)
14-Lead Ceramic Flat Pack



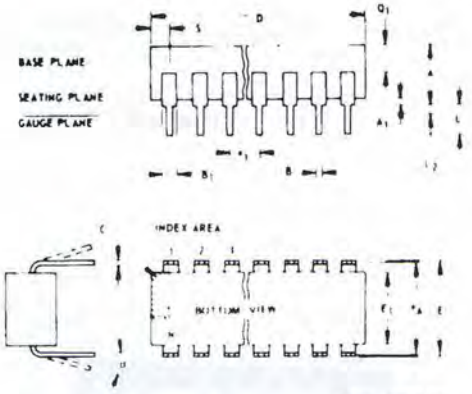
SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.008	0.100		0.21	2.54
B	0.015	0.019	1	0.381	0.482
C	0.003	0.006	1	0.077	0.152
e	0.050 TP		2	1.27 TP	
E	0.200	0.300		5.1	7.6
H	0.600	1.000		15.3	25.4
L	0.150	0.350		3.9	8.8
N	14		3	14	
Q	0.005	0.050		0.13	1.27
S	0.000	0.050		0.00	1.27
Z	0.300		4	7.62	
Z_1	0.400		4	10.16	

92SS-4300R2

NOTES:

1. Refer to Rules for Dimensioning Peripheral Lead Outlines.
2. Leads within .005" (.12 mm) radius of True Position (TP) at maximum material condition.
3. N is the maximum quantity of lead positions.
4. Z and Z_1 determine a zone within which all body and lead irregularities lie.

(D) SUFFIX (JEDEC MO-001-AD)
14-Lead Dual-in-Line White Ceramic Package



92SS-4296R2

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.120	0.160		3.05	4.06
A_1	0.020	0.065		0.51	1.65
B	0.014	0.020		0.356	0.508
B_1	0.050	0.065		1.27	1.65
C	0.008	0.012	1	0.204	0.304
D	0.745	0.770		18.93	19.55
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.76
α	0°	15°	4	0°	15°
N	14		5	14	
N_1	0		6	0	
Q_1	0.050	0.085		1.27	2.15
S	0.065	0.090		1.66	2.28

NOTES 92SS-4411R1

Refer to Rules for Dimensioning (JEDEC Publication No. 13) for Axial Lead Product Outlines

1. When this device is supplied solder dipped, the maximum lead thickness (narrow portion) will not exceed 0.013".
2. Leads within 0.005" (0.12 mm) radius of True Position (TP) at guage plane with maximum material condition and unit installed.
3. e_A applies in zone L_2 when unit installed.
4. α applies to spread leads prior to installation.
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads.

(E) and (F) SUFFIXES
JEDEC MO-001-AB 14-Lead Dual-In-Line Plastic or Frit-Seal Ceramic Package

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.155	0.200		3.94	5.08
A_1	0.020	0.050		0.51	1.27
B	0.014	0.020		0.356	0.508
B_1	0.050	0.065		1.27	1.65
C	0.008	0.012	1	0.204	0.304
D	0.745	0.770		18.93	19.55
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.76
α	0°	15°	4	0°	15°
N	14		5	14	
N_1	0		6	0	
Q_1	0.040	0.075		1.02	1.90
S	0.065	0.090		1.66	2.28

When incorporating RCA Solid State Devices in equipment, it is recommended that the designer refer to "Operating Considerations for RCA Solid State Devices", Form No. 1CE-402, available on request from RCA Solid State Division, Box 3200, Somerville, N. J. 08876.

ORDERING INFORMATION

RCA COS/MOS device packages are identified by letters indicated in the following chart. When ordering a COS/MOS device, it is important that the appropriate suffix letter be affixed to the type number of the device.

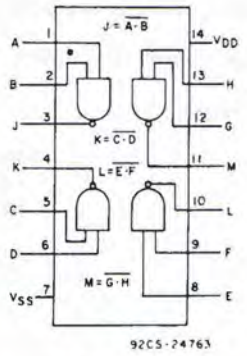
Package	Suffix Letter
Dual-In-Line White Ceramic	D
Dual-In-Line Frit-Seal Ceramic	F
Dual-In-Line Plastic	E
Ceramic Flat Package	K
Chip	H

For example, a CD4000UB type in a dual-in-line plastic package will be identified as CD4000UBE.

Digital Integrated Circuits

Monolithic Silicon

CD4011UB, CD4012UB, CD4023UB Types



CD4011UB
FUNCTIONAL DIAGRAM

COS/MOS NAND Gates

High-Voltage Types (20-Volt Rating)

Quad 2 Input – CD4011UB
Dual 4 Input – CD4012UB
Triple 3 Input – CD4023UB

Features:

- **Propagation delay time = 30 ns (typ). at C_L = 50 pF, V_{DD} = 10 V**
- **Standardized symmetrical output characteristics**
- **100% tested for quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C**
- **5-V, 10-V, and 15-V parametric ratings**

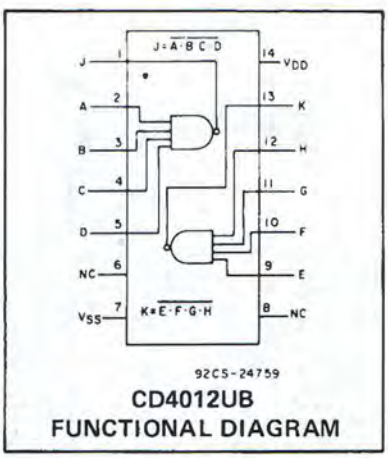
The RCA-CD4011UB, CD4012UB, and CD4023UB NAND gates provide the system designer with direct implementation of the NAND function and supplement the existing family of COS/MOS gates.

The CD4011UB, CD4012UB, and CD4023UB types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

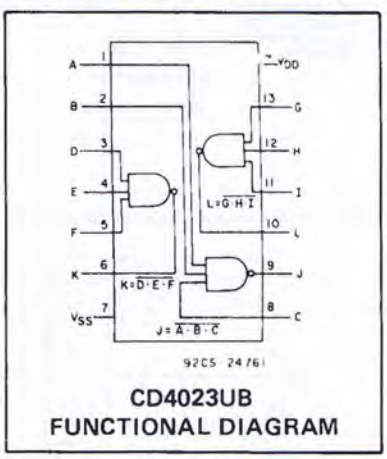
RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	MIN.	MAX.	UNITS
Supply Voltage Range (For T_A = Full Package Temperature Range)	3	18	V



CD4012UB
FUNCTIONAL DIAGRAM



CD4023UB
FUNCTIONAL DIAGRAM

Printed in USA/9-76

Supersedes issue dated 3-76

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

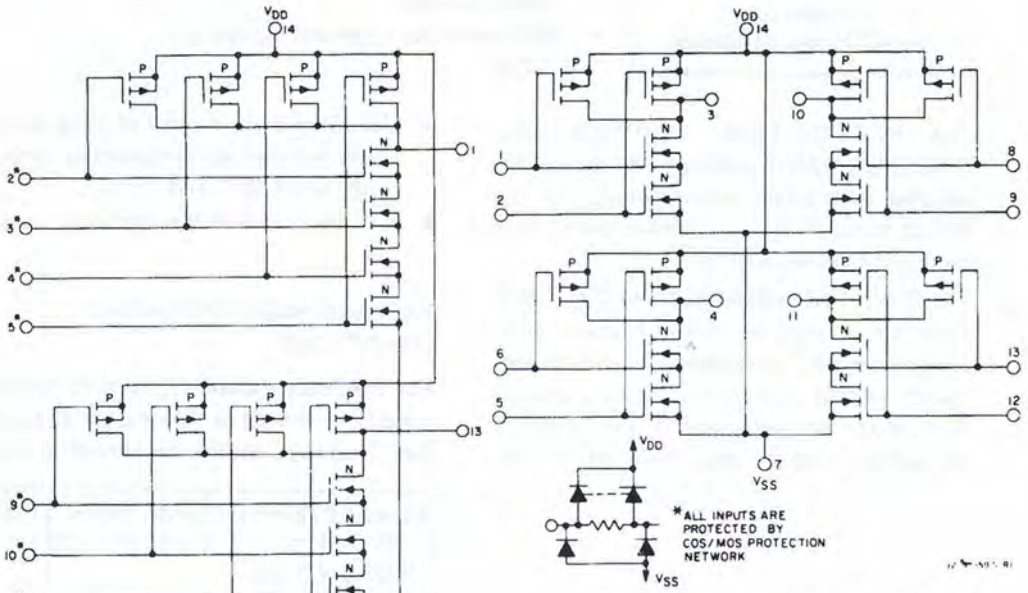


Fig.2 – Schematic diagram for type CD4011UB.

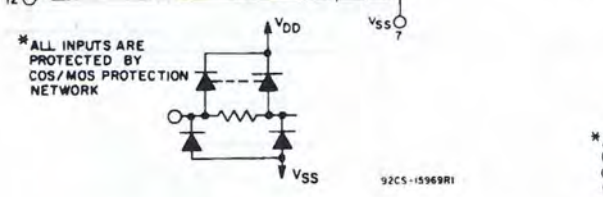
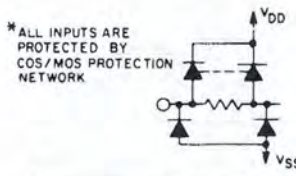


Fig.1 – Schematic diagram for type CD4012UB.



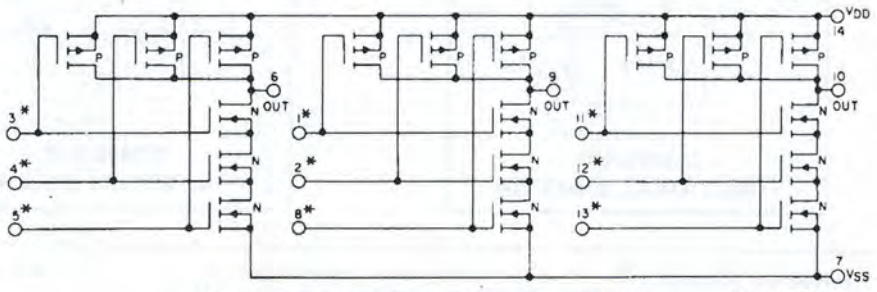


Fig.3 – Schematic diagram for type CD4023UB.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,K,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	0.25	0.25	7.5	7.5	–	0.01	0.25	μA
	–	0,10	10	0.5	0.5	15	15	–	0.01	0.5	
	–	0,15	15	1	1	30	30	–	0.01	1	
	–	0,20	20	5	5	130	130	–	0.02	5	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	--	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3 4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	4.5	–	5	1				—	—	1	V
	9	–	10	2				—	—	2	
	13	–	15	3				–	—	3	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	4				4	—	—	
	1,9	–	10	8				8	—	—	
	2,13	–	15	12				12	—	—	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

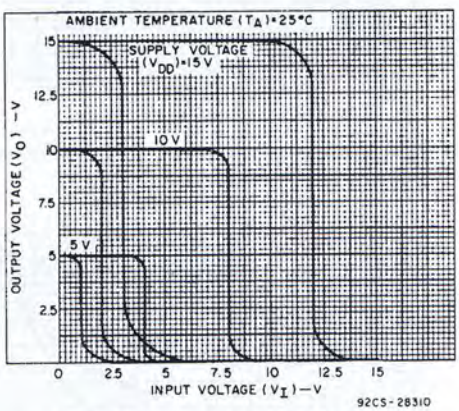


Fig.4 – Minimum and maximum voltage transfer characteristics.

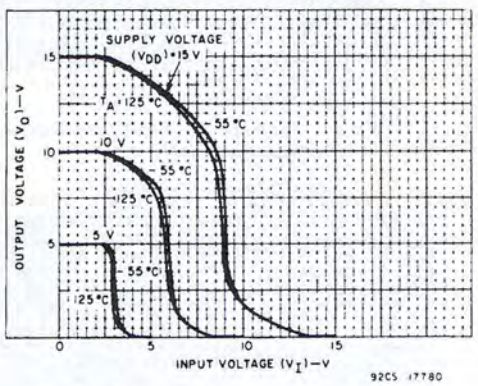


Fig.5 – Typical voltage transfer characteristics as a function of temperature.

DYNAMIC ELECTRICAL CHARACTERISTICS

At T_A = 25°C, Input t_r, t_f = 20 ns, and C_L = 50 pF, R_L = 200kΩ

CHARACTERISTIC	TEST CONDITIONS		ALL TYPES LIMITS		UNITS
		V_{DD} VOLTS	TYP.	MAX	
Propagation Delay Time, t_{PHL}, t_{PLH}		5	60	120	ns
		10	30	60	
		15	25	50	
Transition Time, t_{THL}, t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance, C_{IN}	Any Input		10	15	pF

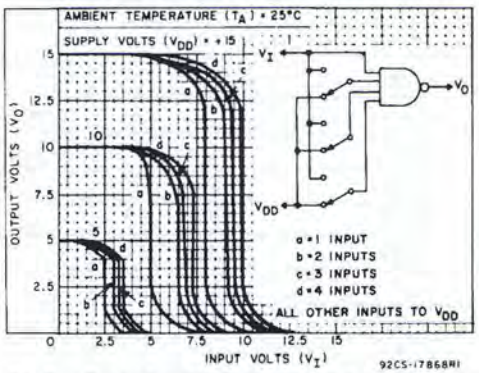


Fig.6 – Typical multiple input switching transfer characteristics for CD4012UB.

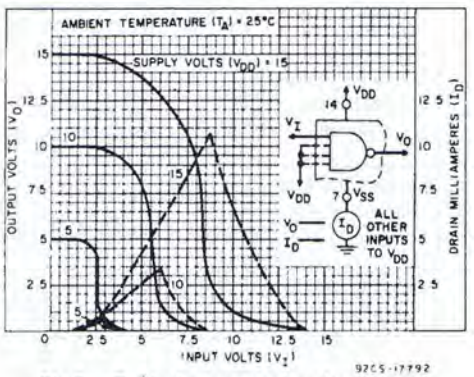


Fig.7 – Typical current and voltage transfer characteristics.

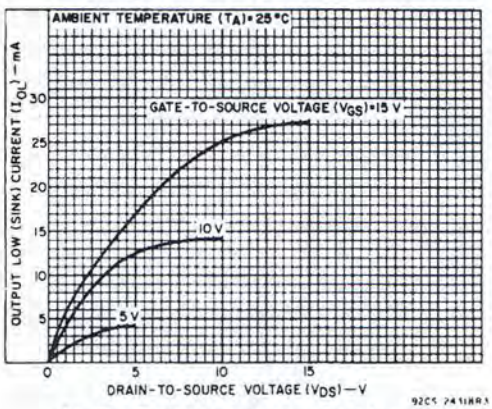


Fig.8 – Typical output low (sink) current characteristics.

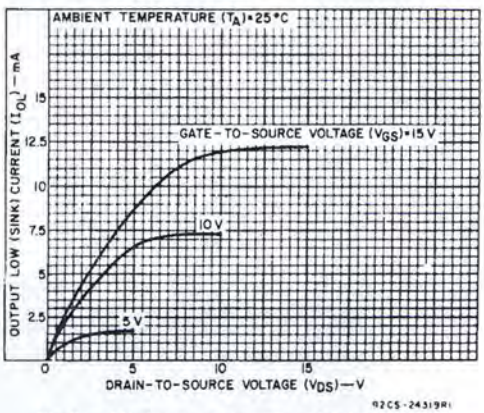


Fig.9 – Minimum output low (sink) current characteristics.

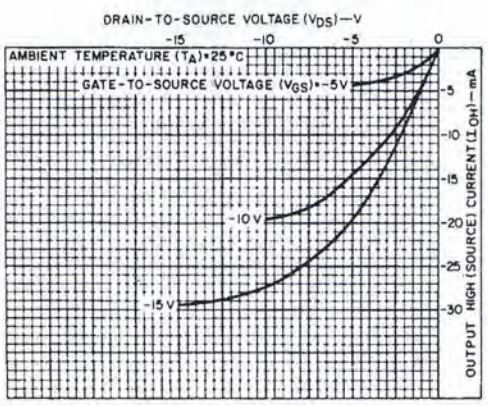


Fig.10 – Typical output high (source) current characteristics.

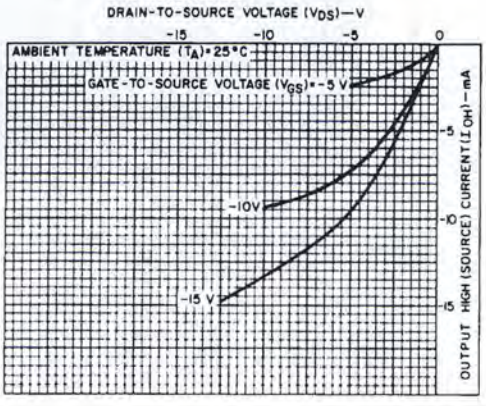


Fig.11 – Minimum output high (source) current characteristics.

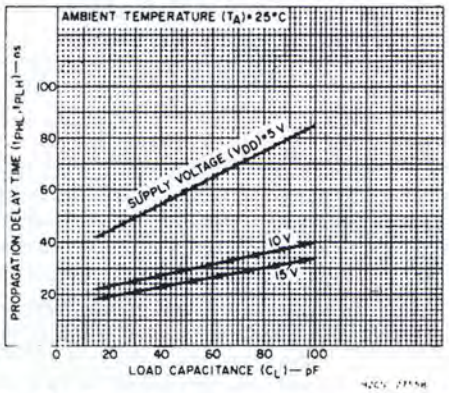


Fig.12 – Typical propagation delay time vs. load capacitance.

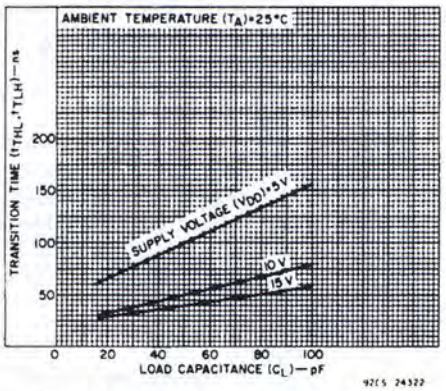


Fig.13 – Typical transition time vs. load capacitance.

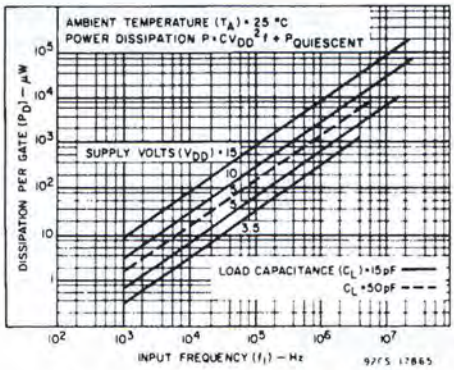


Fig.14 – Typical power dissipation vs. frequency characteristics.

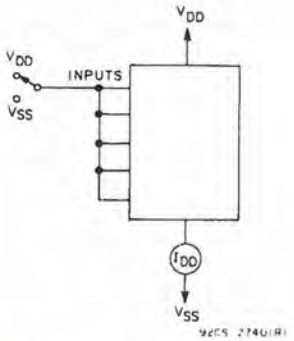


Fig.15 – Quiescent device current test circuit.

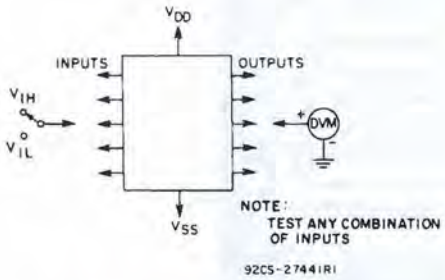


Fig.16 – Input voltage test circuit.

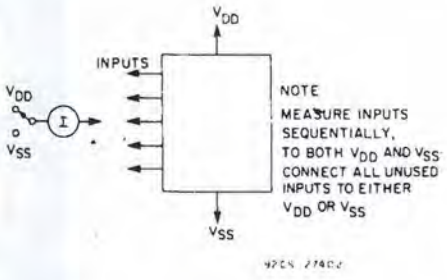
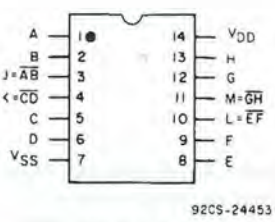
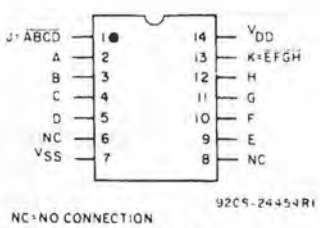


Fig.17 – Input current test circuit.



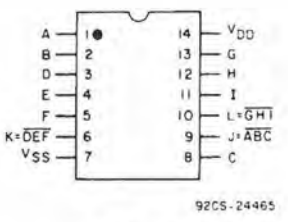
TOP VIEW

CD4011UB



TOP VIEW

CD4012UB



TOP VIEW

CD4023UB

TERMINAL ASSIGNMENTS

OPERATING AND HANDLING CONSIDERATIONS

1. Handling

All inputs and outputs of this device have a network for electronic protection during handling. Recommended handling practices for COS/MOS devices are described in ICAN-6525 "Guide to Better Handling and Operation of CMOS Integrated Circuits".

2. Operating

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause $V_{DD}-V_{SS}$ to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} nor less than V_{SS}. Input currents must not exceed 10 mA even when the power supply is off.

Unused Inputs

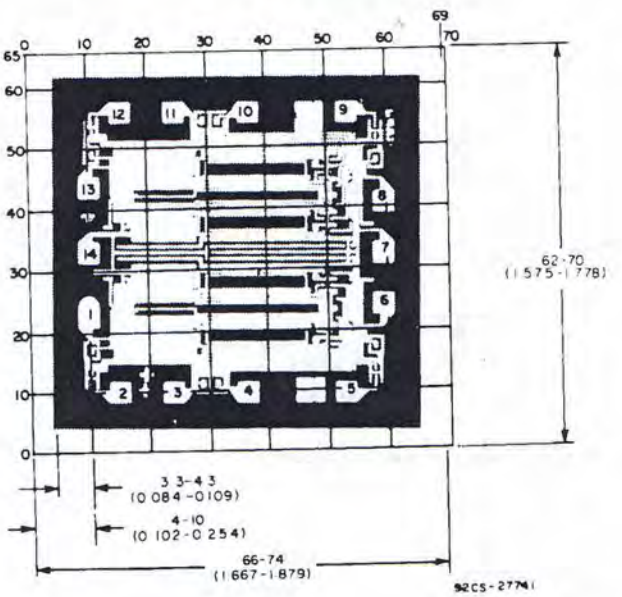
A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{DD} or V_{SS}, whichever is appropriate.

Output Short Circuits

Shorting of outputs to V_{DD} or V_{SS} may damage COS/MOS devices by exceeding the maximum device dissipation.

CHIP PHOTOGRAPHS

Dimensions and Pad Layouts

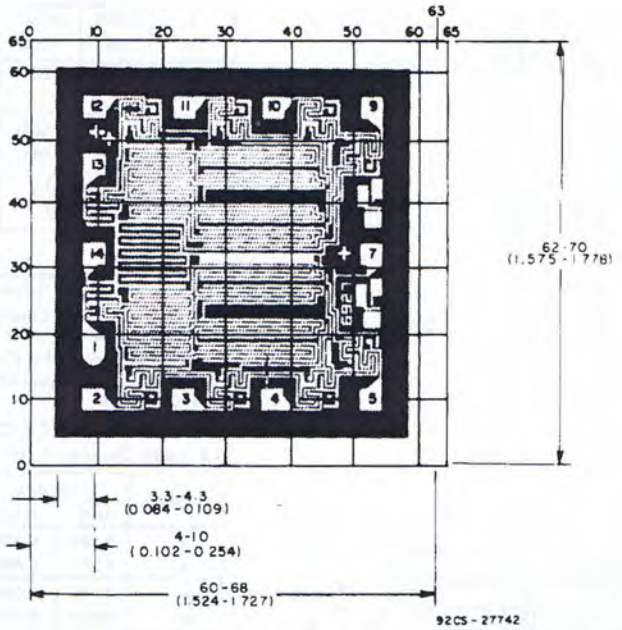


CD4011UBH

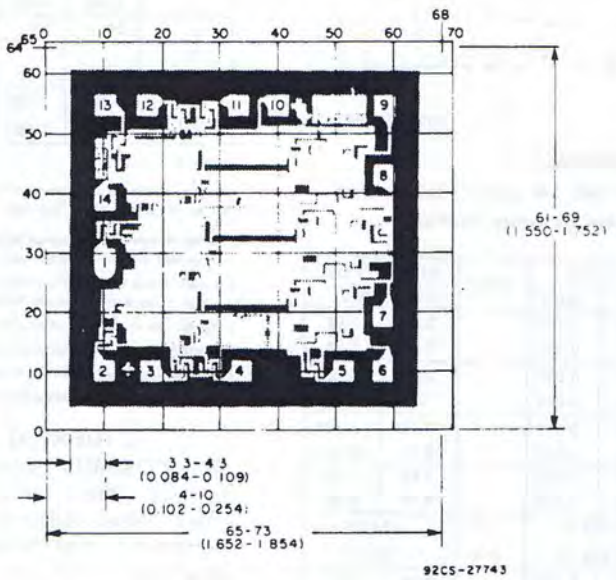
Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

CHIP PHOTOGRAPHS
Dimensions and Pad Layout



CD4012UBH



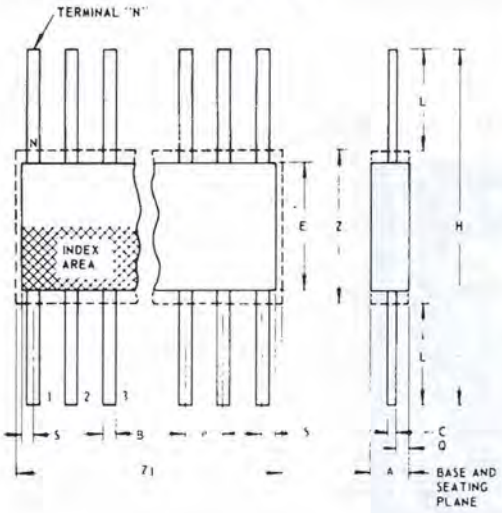
CD4023UBH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

DIMENSIONAL OUTLINES

(K) SUFFIX (JEDEC MO-004-AF)
14-Lead Ceramic Flat Pack

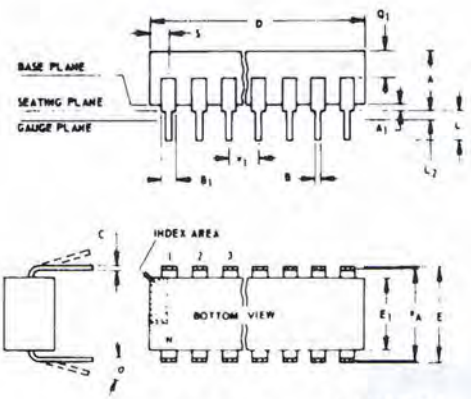


SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.008	0.100		0.21	2.54
B	0.015	0.019	1	0.381	0.482
C	0.003	0.006	1	0.077	0.152
e	0.050 TP		2	1.27 TP	
E	0.200	0.300		5.1	7.6
H	0.600	1.000		15.3	25.4
L	0.150	0.350		3.9	8.8
N	14		3	14	
Q	0.005	0.050		0.13	1.27
S	0.000	0.050		0.00	1.27
Z	0.300		4	7.62	
Z_1	0.400		4	10.16	

NOTES: 92SS-4300R2

1. Refer to Rules for Dimensioning (JEDEC Publication No. 13) for Axial Lead Product Outlines.
2. Leads within .005" (.12 mm) radius of True Position (TP) at maximum material condition.
3. N is the maximum quantity of lead positions.
4. Z and Z_1 determine a zone within which all body and lead irregularities lie.

(D) SUFFIX (JEDEC MO-001-AD)
14-Lead Dual-in-Line White Ceramic Package



SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.120	0.160		3.05	4.06
A_1	0.020	0.065		0.51	1.65
B	0.014	0.020		0.356	0.508
B_1	0.050	0.065		1.27	1.65
C	0.008	0.012	1	0.204	0.30
D	0.745	0.770		18.93	19.55
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.76
α	0°	15°	4	0°	15°
N	14		5	14	
N_1	0		6	0	
Q_1	0.050	0.085		1.27	2.15
S	0.065	0.090		1.66	2.28

NOTES 92SS-44URI

Refer to Rules for Dimensioning (JEDEC Publication No. 13) for Axial Lead Product Outlines.

1. When this device is supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013".
2. Leads within 0.005" (0.12 mm) radius of True Position (TP) at guage plane with maximum material condition and unit installed.
3. e_A applies in zone L_2 when unit installed.
4. α applies to spread leads prior to installation.
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads.

(E) and (F) SUFFIXES
JEDEC MO-001-AB 14-Lead Dual-In-Line Plastic or Frit-Seal Ceramic Package

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.155	0.200		3.94	5.08
A_1	0.020	0.050		0.51	1.27
B	0.014	0.020		0.356	0.508
B_1	0.050	0.065		1.27	1.65
C	0.008	0.012	1	0.204	0.304
D	0.745	0.770		18.93	19.55
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.76
α	0°	15°	4	0°	15°
N	14		5	14	
N_1	0		6	0	
Q_1	0.040	0.075		1.02	1.90
S	0.065	0.090		1.66	2.28

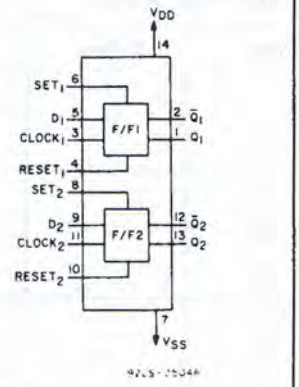
When incorporating RCA Solid State Devices in equipment, it is recommended that the designer refer to "Operating Considerations for RCA Solid State Devices", Form No. 1CE-402, available on request from RCA Solid State Division, Box 3200, Somerville, N. J. 08876.

ORDERING INFORMATION

RCA COS/MOS device packages are identified by letters indicated in the following chart. When ordering a COS/MOS device, it is important that the appropriate suffix letter be affixed to the type number of the device.

Package	Suffix Letter
Dual-In-Line White Ceramic	D
Dual-In-Line Frit-Seal Ceramic:	F
Dual-In-Line Plastic	E
Ceramic Flat Package	K
Chip	H

For example, a CD4011UB type in a dual-in-line plastic package will be identified as the CD4011UBE.



CD4013B
FUNCTIONAL DIAGRAM

Dual 'D'-Type Flip-Flop

High-Voltage Types (20-Volt Rating)

Features:

- **Set-Reset capability**
- **Static flip-flop operation – retains state indefinitely with clock level either "high" or "low"**
- **Medium-speed operation – 16 MHz (typ.) clock toggle rate at 10V**
- **Standardized symmetrical output characteristics**
- **100% tested for quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C**
- **Noise margin (over full package temperature range): 1 V at V_{DD}=5 V, 2 V at V_{DD}=10 V, 2.5 V at V_{DD}=15 V**
- **5-V, 10-V, and 15-V parametric ratings**

Applications:

- **Registers, counters, control circuits**

The RCA-CD4013B consists of two identical, independent data-type flip-flops. Each flip-flop has independent data, set, reset, and clock inputs and Q and $\overline{Q}$ outputs. These devices can be used for shift register applications, and, by connecting $\overline{Q}$ output to the data input, for counter and toggle applications. The logic level present at the D input is transferred to the Q output during the positive-going transition of the clock pulse. Setting or resetting is independent of the clock and is accomplished by a high level on the set or reset line, respectively.

The CD4013B types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	−0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = −40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, K, H	−55 to +125°C
PACKAGE TYPE E	−40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING): At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

Printed in USA/9-76

Supersedes issue of 3-76

RECOMMENDED OPERATING CONDITIONS

At T_A = 25°C, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS		UNITS
		ALL PACKAGES		
		MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	–	3	18	V
Data Setup Time t_S	5	40	–	ns
	10	30	–	
	15	25	–	
Clock Pulse Width t_W	5	140	–	ns
	10	60	–	
	15	40	–	
Clock Input Frequency f_{CL}	5	dc	3.5	MHz
	10		8	
	15		12	
Clock Rise or Fall Time t_rCL,* t_fCL	5	–	15	μs
	10	–	5	
	15	–	5	
Set or Reset Pulse Width t_W	5	200	–	ns
	10	100	–	
	15	50	–	

*If more than one unit is cascaded in a parallel clocked operation, t_rCL should be made less than or equal to the sum of the fixed propagation delay time at 15 pF and the transition time of the output driving stage for the estimated capacitive load.

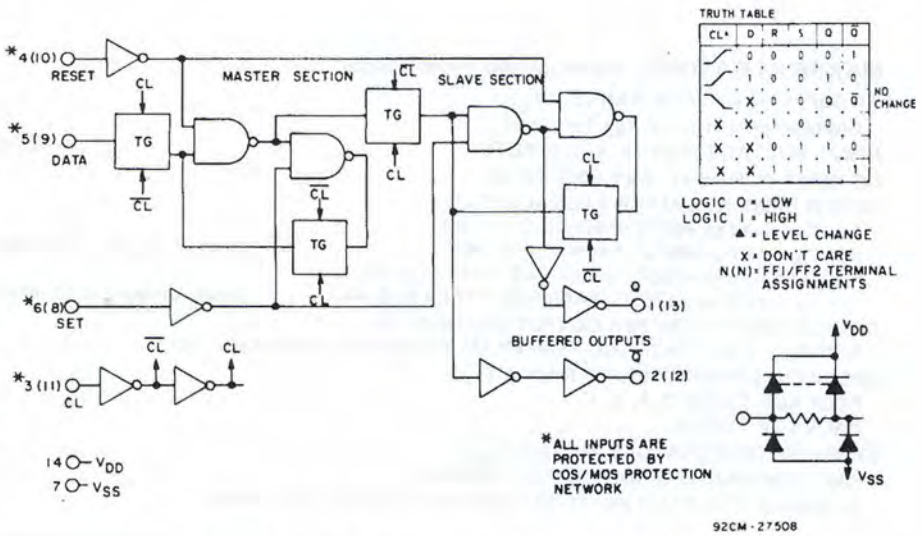


Fig. 1 – Logic diagram and truth table for CD4013B (one of two identical flip-flops).

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55,+25,+125 Apply to D,K,F,H Pkgs. Values at −40,+25,+85 Apply to E Pkgs.							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current I_{DD} Max.	–	0,5	5	1	1	30	30	–	0.02	1	μA
	–	0,10	10	2	2	60	60	–	0.02	2	
	–	0,15	15	4	4	120	120	–	0.02	4	
	–	0,20	20	20	20	600	600	–	0.04	20	
Output Low (Sink) Current, I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current, I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

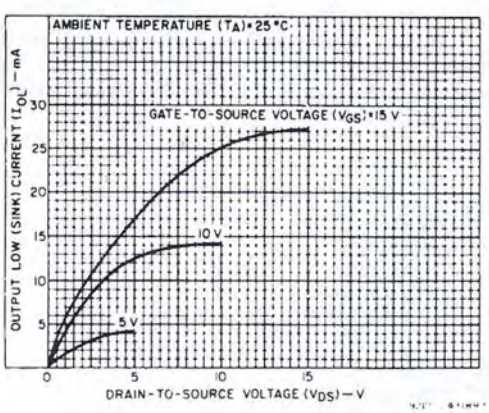


Fig. 2 – Typical output low (sink) current characteristics

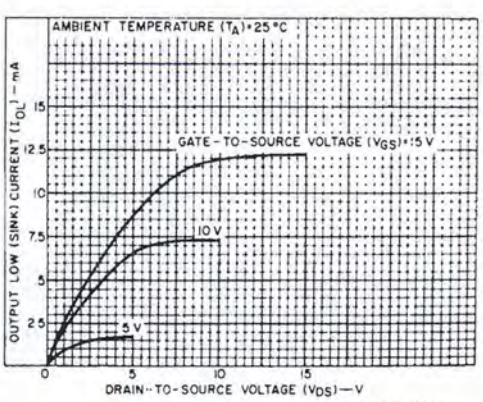


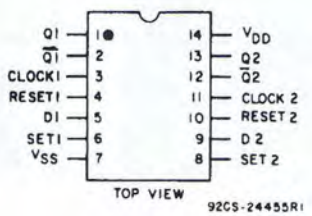
Fig. 3 – Minimum output low (sink) current characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS

At $T_A = 25°C$; Input t_r, $t_f = 20$ ns, $C_L = 50$ pF, $R_L = 200$ kΩ

CHARACTERISTIC	TEST CONDITIONS	LIMITS				UNITS
			ALL PACKAGES			
		V_{DD} (V)	MIN.	TYP.	MAX.	
Propagation Delay Time: Clock to Q or $\overline{Q}$ Outputs t_{PHL}, t_{PLH}		5	–	150	300	ns
		10	–	65	130	
		15	–	45	90	
Set to Q or Reset to $\overline{Q}$ t_{PLH}		5	–	150	300	ns
		10	–	65	130	
		15	–	45	90	
Set to $\overline{Q}$ or Reset to Q t_{PHL}		5	–	200	400	ns
		10	–	85	170	
		15	–	60	120	
Transition Time t_{THL}, t_{TLH}		5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
Maximum Clock Input Frequency Frequency # f_{CL}		5	3.5	7	–	MHz
		10	8	16	–	
		15	12	24	–	
Minimum Clock Pulse Width t_W		5	–	70	140	ns
		10	–	30	60	
		15	–	20	40	
Minimum Set or Reset Pulse Width t_W		5	–	90	180	ns
		10	–	40	80	
		15	–	25	50	
Minimum Data Setup Time t_S		5	–	20	40	ns
		10	–	15	30	
		15	–	12	25	
Clock Input Rise or Fall Time t_{rCL}, t_{fCL}		5	–	–	15	μs
		10	–	–	5	
		15	–	–	5	
Input Capacitance C_{IN}	Any Input		–	5	7.5	pF

#Input t_r, t_f = 5 ns.



TERMINAL ASSIGNMENT

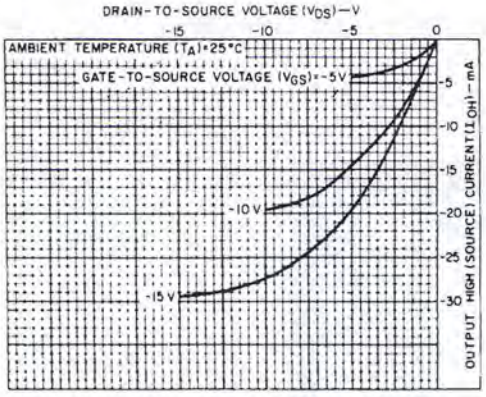


Fig. 4 – Typical output high (source) current characteristics.

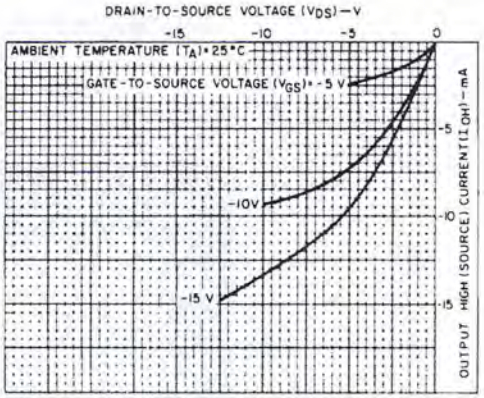


Fig. 5 – Minimum output high (source) current characteristics.

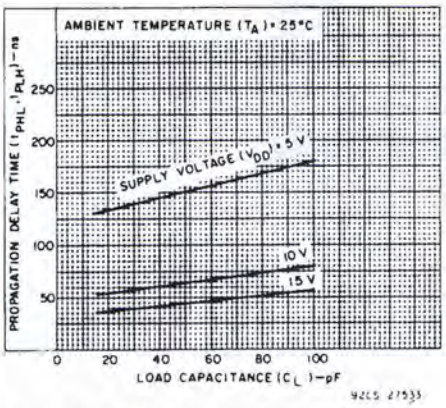


Fig. 6 – Typical propagation delay time vs. load capacitance (CLOCK or SET to Q, CLOCK or RESET to $\overline{Q}$).

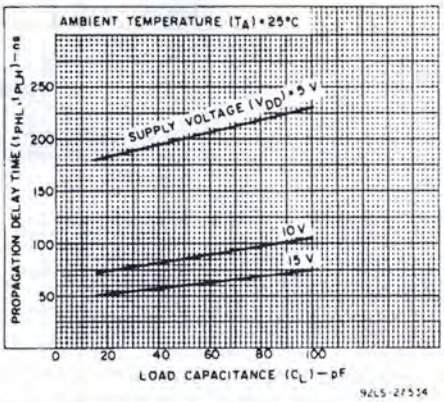


Fig. 7 – Typical propagation delay time vs. load capacitance (SET to $\overline{Q}$ or RESET to Q.

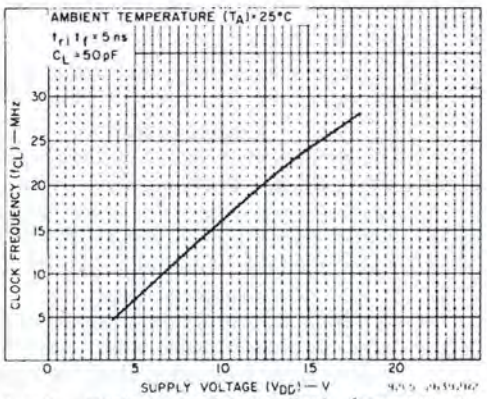


Fig. 8 – Typical maximum clock frequency vs. supply voltage.

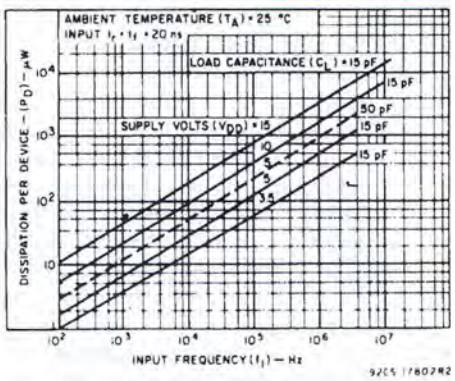


Fig. 9 – Typical power dissipation vs. frequency.

TEST CIRCUITS

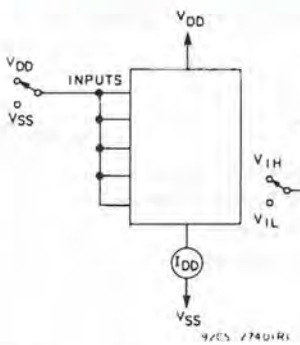


Fig. 10 – Quiescent device current.

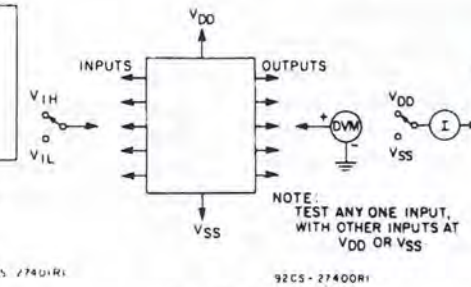


Fig. 11 – Input voltage.

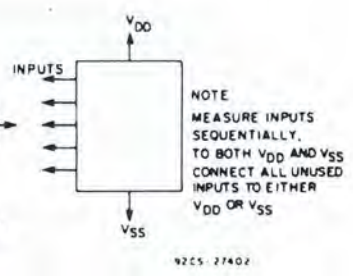
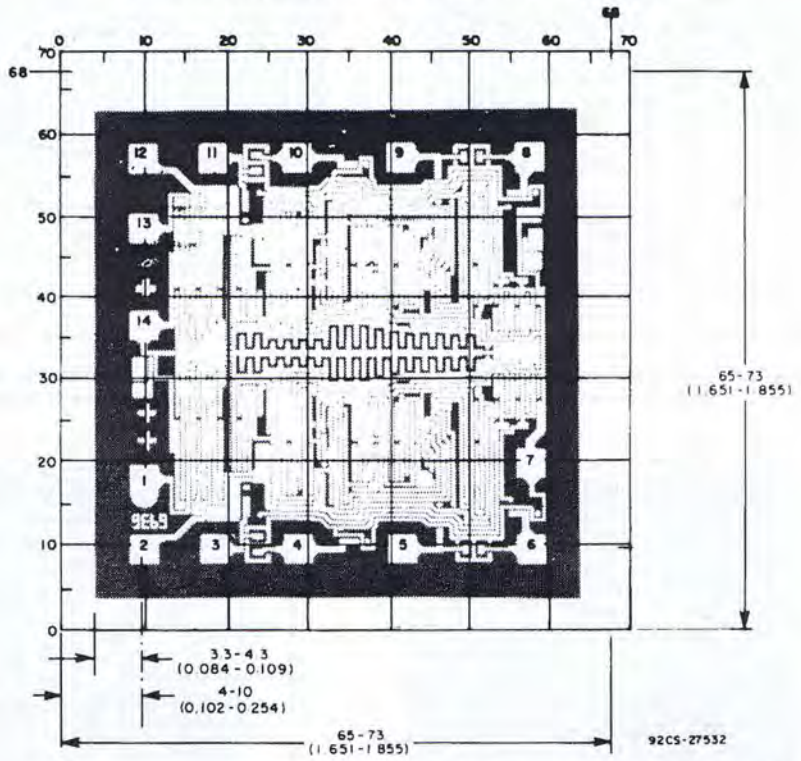


Fig. 12 – Input current.

DIMENSIONS AND PAD LAYOUT FOR CD4013BH



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

OPERATING AND HANDLING CONSIDERATIONS

1. **Handling**
   All inputs and outputs of RCA COS/MOS devices have a network for electrostatic protection during handling. Recommended handling practices for COS/MOS devices are described in ICAN-6525, "Guide to Better Handling and Operation of CMOS Integrated Circuits."
2. **Operating**

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause $V_{DD}-V_{SS}$ to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} nor less than V_{SS}. Input currents must not exceed 10 mA even when the power supply is off.

Unused Inputs

A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{DD} or V_{SS}, whichever is appropriate.

Output Short Circuits

Shorting of outputs to V_{DD} or V_{SS} may damage COS/MOS devices by exceeding the maximum device dissipation.

ORDERING INFORMATION

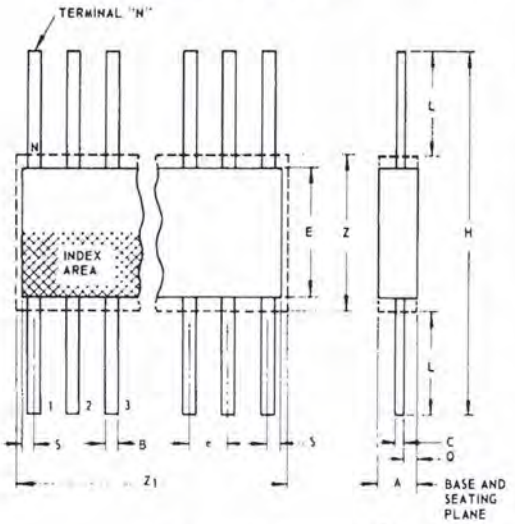
RCA COS/MOS device packages are identified by letters indicated in the following chart. When ordering a COS/MOS device, it is important that the appropriate suffix letter be affixed to the type number of the device.

For example, a CD4013 "B"-Series type in a dual-in-line plastic package will be identified as the CD4013BE.

Package	Suffix Letter
Dual-In-Line White Ceramic	D
Dual-In-Line Frit-Seal Ceramic:	F
Dual-In-Line Plastic	E
Ceramic Flat Package	K
Chip	H

DIMENSIONAL OUTLINES

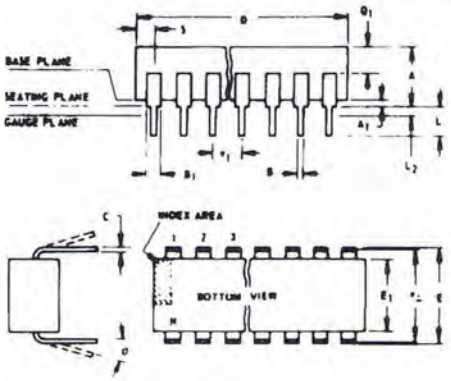
(K) SUFFIX (JEDEC MO-004-AF)
14-Lead Ceramic Flat Pack



SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.008	0.100		0.21	2.54
B	0.015	0.019	1	0.381	0.482
C	0.003	0.006	1	0.077	0.152
e	0.050 TP		2	1.27 TP	
E	0.200	0.300		5.1	7.6
H	0.600	1.000		15.3	25.4
L	0.150	0.350		3.9	8.8
N	14		3	14	
Q	0.005	0.050		0.13	1.27
S	0.000	0.050		0.00	1.27
Z	0.300		4	7.62	
Z_1	0.400		4	10.16	

92SS-4300R2

NOTES:
1. Refer to Rules for Dimensioning Peripheral Lead Outlines.
2. Leads within .005" (.12 mm) radius of True Position (TP) at maximum material condition.
3. N is the maximum quantity of lead positions.
4. Z and Z_1 determine a zone within which all body and lead irregularities lie.



(D) SUFFIX (JEDEC MO-001-AD)
14-Lead Dual-in-Line White Ceramic Package

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.120	0.160		3.05	4.06
A_1	0.020	0.065		0.51	1.65
B	0.014	0.020		0.356	0.508
B_1	0.050	0.065		1.27	1.65
C	0.008	0.012	1	0.204	0.304
D	0.745	0.770		18.93	19.55
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.76
α	0°	15°	4	0°	15°
N	14		5	14	
N_1	0		6	0	
Q_1	0.050	0.085		1.27	2.15
S	0.065	0.090		1.66	2.28

92SS-4411R1

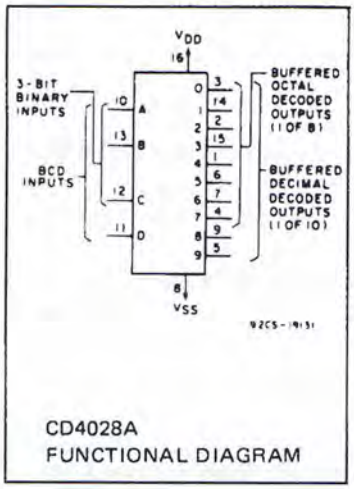
(E), (F), and (Y) SUFFIX
JEDEC MO-001-AB 14-Lead Dual-In-Line Plastic or Frit-Seal Ceramic Package

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.155	0.200		3.94	5.08
A_1	0.020	0.050		0.51	1.27
B	0.014	0.020		0.356	0.508
B_1	0.050	0.065		1.27	1.65
C	0.008	0.012	1	0.204	0.304
D	0.745	0.770		18.93	19.55
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.76
α	0°	15°	4	0°	15°
N	14		5	14	
N_1	0		6	0	
Q_1	0.040	0.075		1.02	1.90
S	0.065	0.090		1.66	2.28

92SS-4296R2

NOTES:
Refer to Rules for Dimensioning (JEDEC Publication No. 13) for Axial Lead Product Outlines.
1. When this device is supplied solder dipped, the maximum lead thickness (narrow portion) will not exceed 0.013 (0.33 mm).
2. Leads within 0.005 (0.12 mm) radius of True Position (TP) at gauge plane with maximum material condition and unit installed.
3. e_A applies in zone L_2 when unit installed.
4. α applies to spread leads prior to installation.
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads.

When incorporating RCA Solid State Devices in equipment, it is recommended that the designer refer to "Operating Considerations for RCA Solid State Devices", Form No. 1CE-402, available on request from RCA Solid State Division, Box 3200, Somerville, N. J. 08876.



CD4028A
FUNCTIONAL DIAGRAM

COS/MOS BCD-to-Decimal Decoder

Features:

- **BCD-to-decimal decoding or binary-to-octal decoding**
- **High decoded output drive capability. . .**
  . . . 8 mA (typ.) sink or source
- **"Positive logic" inputs and outputs. . .**
  . . . decoded outputs go high on selection
- **Medium-speed operation . . .**
  . . . t_{THL}, t_{TLH} = 30 ns (typ.) @ V_{DD} = 10 V
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

Applications:

- **Code conversion**
- **Address decoding—memory selection control**
- **Indicator-tube decoder**

The RCA-CD4028A types are BCD-to-decimal or binary-to-octal decoders consisting of pulse-shaping circuits on all 4 inputs, decoding-logic gates, and 10 output buffers. A BCD code applied to the four inputs, A to D, results in a high level at the selected one of 10 decimal decoded outputs. Similarly, a 3-bit binary code applied to inputs A through C is decoded in octal code at output 0 to 7. A high-level signal at the D input inhibits octal decoding and causes outputs 0 through 7 to go low. If unused, the D input must be connected to V_{SS}. High drive capability is provided at all outputs to enhance dc and dynamic performance in high fan-out applications.

The CD4028A-Series types are supplied in 16-lead hermetic dual-in-line ceramic packages (D, F, and Y suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix). For ordering information, see dimensional outlines, pages 7 and 8.

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D, F, K, H PACKAGES		E, Y PACKAGES		
		MIN.	MAX.	MIN.	MAX.	
Supply-Voltage Range (For T_A=Full Package-Temperature Range)		3	12	3	12	V

Printed in USA/2-76

Supersedes File 503 dated 10-73

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . –65 to +150°C

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, F, K, H . . . . . –55 to +125°C

PACKAGE TYPES E, Y . . . . . –40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages references to V_{SS} Terminal) . . . . . –0.5 to +15 V

POWER DISSIPATION PER PACKAGE (P_D):

FOR T_A = –40 to +60°C (PACKAGE TYPES E, Y) . . . . . 500 mW

FOR T_A = +60 to +85°C (PACKAGE TYPES E, Y) . . . . . Derate Linearly at 12 mW/°C to 200 mW

FOR T_A = –55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW

FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS . . . . . –0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)								UNITS
				D, K, F, H PACKAGES				E, Y PACKAGES				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	–55	+25 TYP.	+25 LIMIT	+125	–40	+25 TYP.	+25 LIMIT	+85	
Quiescent Device Current, I_L Max.	–	–	5	5	0.5	5	300	50	5	50	700	μA
	–	–	10	10	1	10	600	100	10	100	1400	
	–	–	15	50	1	50	2000	500	10	500	5000	
Output Voltage: Low-Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max.								V
	–	10	10	0 Typ.; 0.05 Max.								
High Level V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current N-Channel (Sink), I_{DN} Min.	0.5	–	5	0.75	1.2	0.6	0.45	0.35	1.2	0.3	0.25	mA
	0.5	–	10	1.5	2.4	1.2	0.9	0.7	2.4	0.6	0.5	
P-Channel (Source), I_{DP} Min.	4.5	–	5	–0.7	–0.9	–0.45	–0.32	–0.32	–0.9	–0.22	–0.18	
	9	–	10	–1.4	–1.9	–0.95	–0.65	–0.65	–1.9	–0.48	–0.4	
Input Leakage Current, I_{IL}, I_{IH}	Any Input											μA
	–	–	15	$\pm 10^{-5}$ Typ., ±1 Max.								

DYNAMIC ELECTRICAL CHARACTERISTICS

at $T_A = 25^oC$, Input t_r, $t_f = 20$ ns, $C_L = 15$ pF, $R_L = 200$ kΩ

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNITS
		D, F, K, H PACKAGES			E, Y PACKAGES			
	V_{DD} (V)	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Propagation Delay Time; t_{PLH}, t_{PHL}	5	–	250	480	–	250	700	ns
	10	–	100	180	–	100	290	
Transition Time; t_{THL}, t_{TLH}	5	–	60	150	–	60	300	ns
	10	–	30	75	–	30	150	
Average Input Capacitance, C_I	Any Input	–	5	–	–	5	–	pF

TABLE I – TRUTH TABLE

D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	0	0	0	0	0	0	0
0	0	1	1	0	0	0	1	0	0	0	0	0	0
0	1	0	0	0	0	0	0	1	0	0	0	0	0
0	1	0	1	0	0	0	0	0	1	0	0	0	0
0	1	1	0	0	0	0	0	0	0	1	0	0	0
0	1	1	1	0	0	0	0	0	0	0	1	0	0
1	0	0	0	0	0	0	0	0	0	0	0	1	0
1	0	0	1	0	0	0	0	0	0	0	0	0	1
1	0	1	0	0	0	0	0	0	0	0	0	1	0
1	0	1	1	0	0	0	0	0	0	0	0	0	1
1	1	0	0	0	0	0	0	0	0	0	0	1	0
1	1	0	1	0	0	0	0	0	0	0	0	0	1
1	1	1	0	0	0	0	0	0	0	0	0	1	0
1	1	1	1	0	0	0	0	0	0	0	0	0	1

WHERE 1 = HIGH LEVEL
0 = LOW LEVEL

EXTRAORDINARY STATES

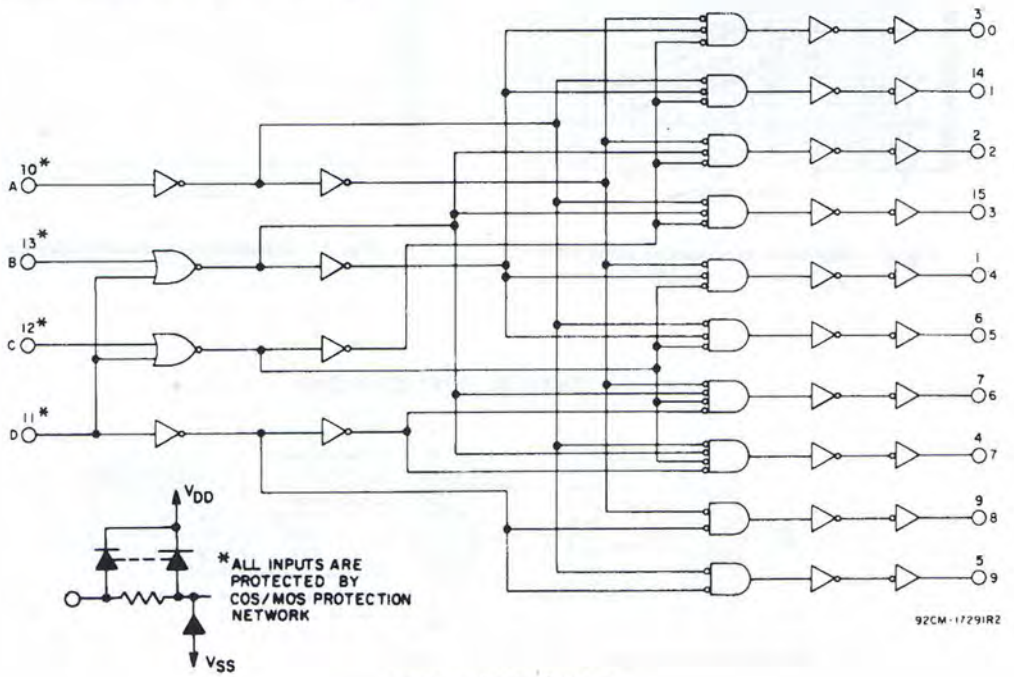
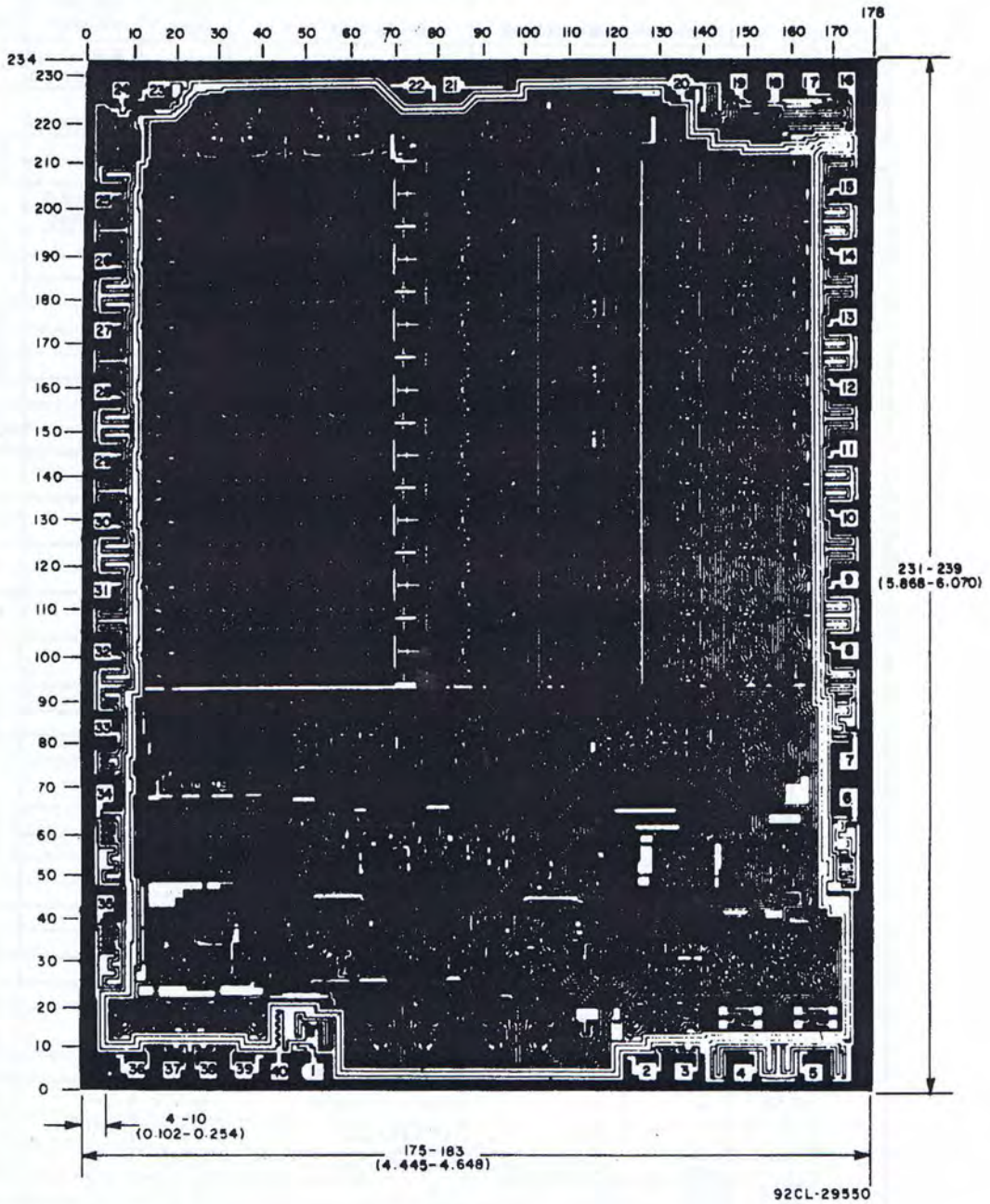


Fig. 1 – Logic diagram.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions and pad layout for CDP1802

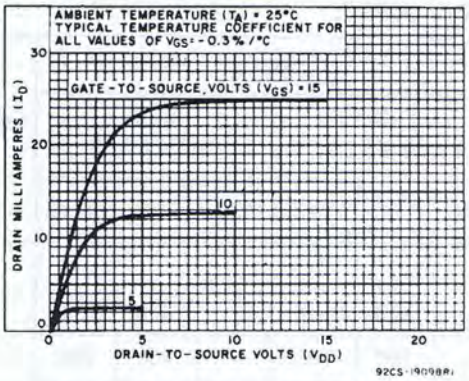


Fig. 2 – Typical output n-channel drain characteristics.

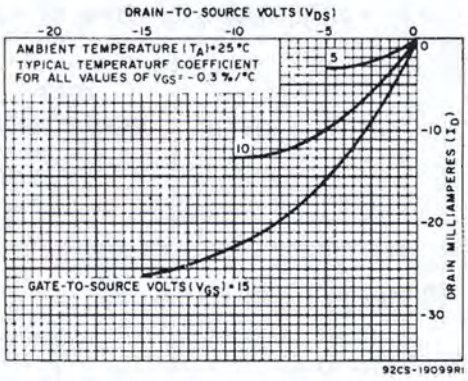


Fig. 3 – Typical output p-channel drain characteristics.

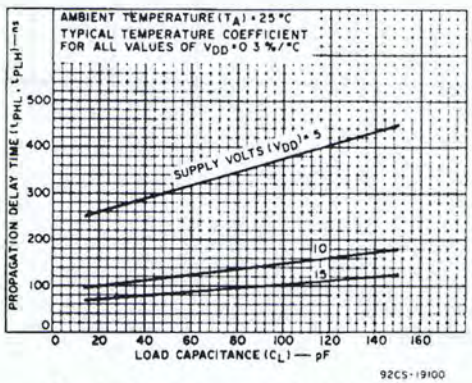


Fig. 4 – Typical propagation delay time vs. C_L.

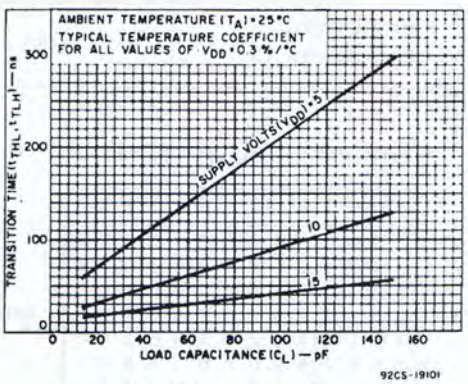


Fig. 5 – Typical transition time vs. C_L.

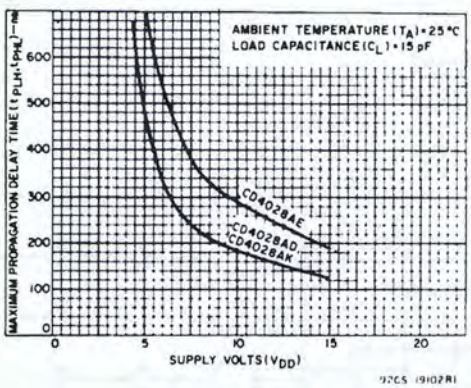


Fig. 6 – Maximum propagation delay time vs. V_{DD}.

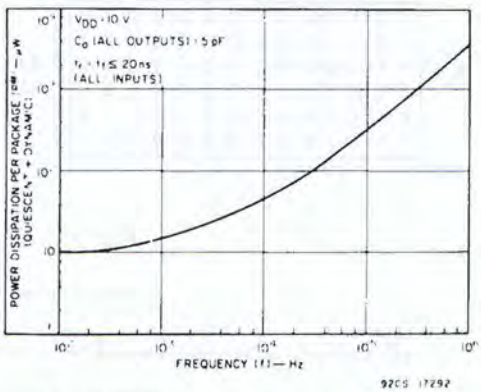
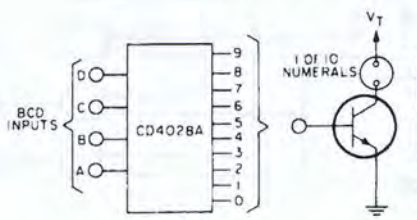


Fig. 7 – Dissipation vs. input frequency.

TYPICAL APPLICATIONS



TUBE REQUIREMENTS

Type		V_T (Vdc)	mA/numeral
Burroughs	B4081	170	1.4
	B4336/718	170	2
	B4032	170	1.4
	B4021	120	1.4

TRANSISTOR CHARACTERISTICS

Leakage with transistor cutoff ≤ 0.05mA

$V_{(BR)CEO}$ ≥ 70V

▲ (Trademark) Burroughs Corp.

Fig. 8 – Neon readout (Nixie Tube▲) display application.

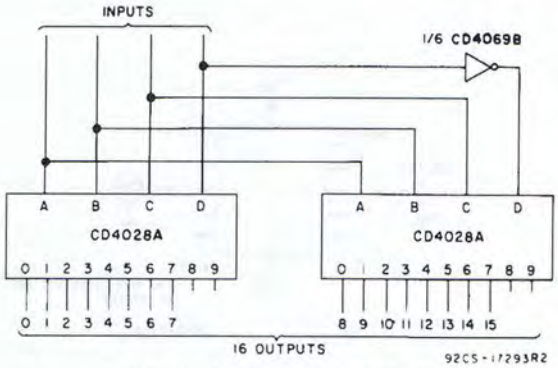


Fig. 9 – Code conversion circuit.

The circuit shown in Fig. 9 converts any 4-bit code to a decimal or hexadecimal code. Table 2 shows a number of codes and the decimal or hexadecimal number in these codes which must be applied to the input terminals of the CD4028A to select a particular output. For example: in order to get a high on output No. 8 the input must be either an 8 expressed in 4-Bit Binary code, a 15 expressed in 4-Bit Gray code, or a 5 expressed in Excess-3 code.

TABLE II – CODE CONVERSION CHART

INPUTS				INPUT CODES						OUTPUT NUMBER																
				Hexa-Decimal		Decimal																				
D	C	B	A	4-BIT BINARY	4-BIT GRAY	EXCESS-3	EXCESS-3 GRAY	AIKEN	4-2-2-1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	0	0			0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	1	1			1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	2	3		0	2	2	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	3	2	0	3	3		0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	4	7	1	4	4		0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
0	1	0	1	5	6	2			3	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
0	1	1	0	6	4	3	1		4	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	1	1	1	7	5	4	2			0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
1	0	0	0	8	15	5				0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1	0	0	1	9	14	6			5	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
1	0	1	0	10	12	7	9		6	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
1	0	1	1	11	13	8		5		0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
1	1	0	0	12	8	9	5	6		0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
1	1	0	1	13	9		6	7	7	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
1	1	1	0	14	11		8	8	8	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
1	1	1	1	15	10		7	9	9	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

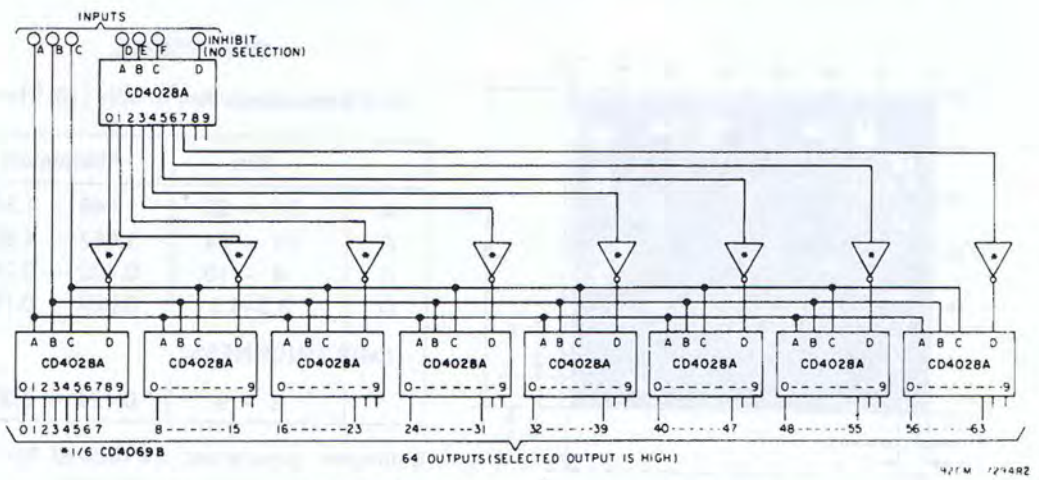


Fig. 10 – 6-bit binary to 1-of-64 address decoder.

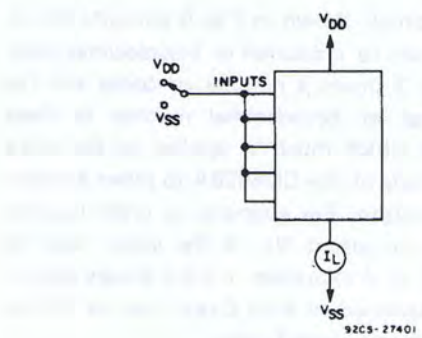


Fig. 11 – Quiescent-device-current test circuit.

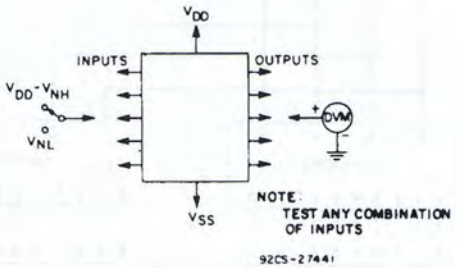


Fig. 12 – Noise-immunity test circuit.

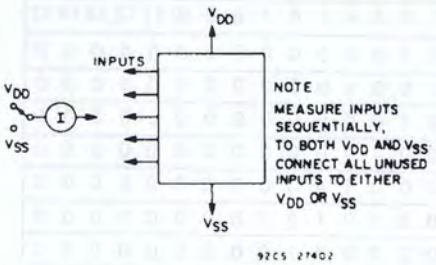
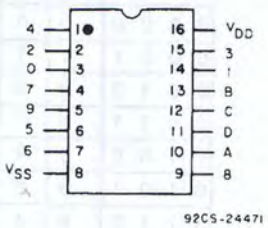
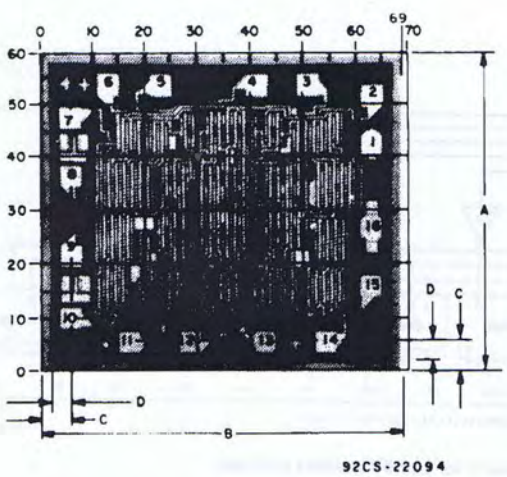


Fig. 13 – Input-leakage-current test circuit.

TERMINAL DIAGRAM
Top View



DIMENSIONS AND PAD LAYOUT FOR CD4028A CHIP



DIMENSIONS

Grid Graduations Are In Mils (10^{-3} Inch)

	Mils	Millimeters
A	57 – 65	1.448 – 1.651
B	66 – 74	1.667 – 1.879
C	4 – 10	0.102 – 0.254
D	3.3–4.3	0.084 – 0.109
CHIP THICKNESS:		
	5 – 9	0.127 – 0.228

Millimeter dimensions are derived from the basic inch dimensions as indicated.

OPERATING & HANDLING CONSIDERATIONS

1. **Handling**

All inputs and outputs of this device have a network for electrostatic protection during handling. Recommended handling practices for COS/MOS devices are described in ICAN-6000 "Handling and Operating Considerations for MOS Integrated Circuits".

2. **Operating**

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause V_{DD}-V_{SS} to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} nor less than V_{SS}. Input currents must not exceed 10 mA even when the power supply is off.

Unused Inputs

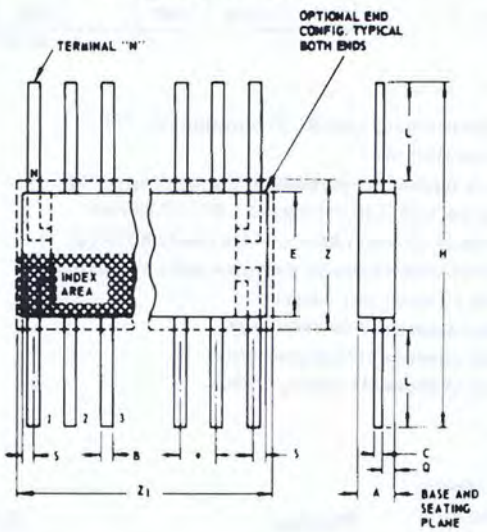
A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{DD} or V_{SS}, whichever is appropriate.

Output Short Circuits

Shorting of outputs to V_{DD} or V_{SS} may damage COS/MOS devices by exceeding the maximum device dissipation.

DIMENSIONAL OUTLINES

(K) SUFFIX
JEDEC MO-004-AG
16-Lead Ceramic Flat Pack

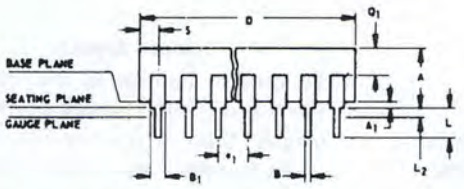


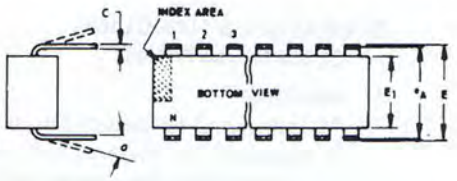
SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.008	0.100		0.21	2.54
B	0.015	0.019	1	0.381	0.482
C	0.003	0.006	1	0.077	0.152
e	0.050 TP		2	1.27 TP	
E	0.200	0.300		5.1	7.6
H	0.600	1.000		15.3	25.4
L	0.150	0.350		3.9	8.8
N	16		3	16	
Q	0.005	0.050		0.13	1.27
S	0.000	0.025		0.00	0.63
Z	0.300		4	7.62	
Z_1	0.400		4	10.16	

92CS-17271R1

NOTES:

1. Refer to Rules for Dimensioning (JEDEC) Publications No. 13) for Axial Lead Product Outlines
2. Leads within 005"(0.12 mm) radius of True Position (TP) at maximum material condition.
3. N is the maximum quantity of lead positions.
4. Z and Z_1 determine a zone within which all body and lead irregularities lie.





(D) SUFFIX
JEDEC MO-001-AE
16-Lead Dual-in-Line White-Ceramic Package

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.120	0.160		3.05	4.06
A_1	0.020	0.065		0.51	1.65
B	0.014	0.020		0.356	0.508
B_1	0.035	0.065		0.89	1.65
C	0.008	0.012	1	0.204	0.304
D	0.745	0.785		18.93	19.93
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.76
α	0°	15°	4	0°	15°
N	16		5	16	
N_1	0		6	0	
Q_1	0.050	0.085		1.27	2.15
S	0.015	0.060		0.39	1.52

92SS-4286R4

(E),(F), and (Y) SUFFIX
JEDEC MO-001-AC 16-Lead Dual-In-Line Plastic or Frit-Seal Ceramic Package

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.155	0.200		3.94	5.08
A_1	0.020	0.050		0.51	1.27
B	0.014	0.020		0.356	0.508
B_1	0.035	0.065		0.89	1.65
C	0.008	0.012	1	0.204	0.304
D	0.745	0.785		18.93	19.93
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.76
α	0°	15°	4	0°	15°
N	16		5	16	
N_1	0		6	0	
Q_1	0.040	0.075		1.02	1.90
S	0.015	0.060		0.39	1.52

92CM-15967R3

NOTES:
Refer to Rules for Dimensioning (JEDEC Publication No. 13) for Axial Lead Product Outlines.

1. When this device is supplied solder dipped, the maximum lead thickness (narrow portion) will not exceed 0.013 (0.33 mm).
2. Leads within 0.005 (0.12 mm) radius of True Position (TP) at gauge plane with maximum material condition and unit installed.
3. e_A applies in zone L_2 when unit installed.
4. α applies to spread leads prior to installation.
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads.

ORDERING INFORMATION

RCA COS/MOS device packages are identified by letters indicated in the following chart. When ordering a COS/MOS device, it is important that the appropriate suffix letter be affixed to the type number of the device.

For example, a CD4028"A"-Series type in a dual-in-line plastic package will be identified as the CD4028AE.

Package	Suffix Letter
Dual-In-Line White Ceramic	D
Dual-In-Line Frit-Seal Ceramic:	
Commercial Type	Y
Premium Type	F
Dual-In-Line Plastic	E
Ceramic Flat Package	K
Chip	H

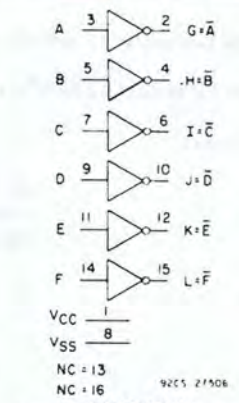
When Incorporating RCA Solid State Devices in equipment, it is recommended that the designer refer to "Operating Considerations for RCA Solid State Devices", Form No. 1CE-402, available on request from RCA Solid State Division, Box 3200, Somerville, N.J. 08876.

RCA
Solid State Division

Digital Integrated Circuits

Monolithic Silicon

CD4049UB, CD4050B Types



CD4049UB
FUNCTIONAL DIAGRAM

COS/MOS Hex Buffer/Converters

High-Voltage Types (20-Volt Rating)

CD4049UB—Inverting Type
CD4050B—Non-Inverting Type

Features:

- **High sink current for driving 2 TTL loads**
- **High-to-low level logic conversion**
- **100% tested for quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C**
- **5-, 10-, and 15-volt parametric ratings**

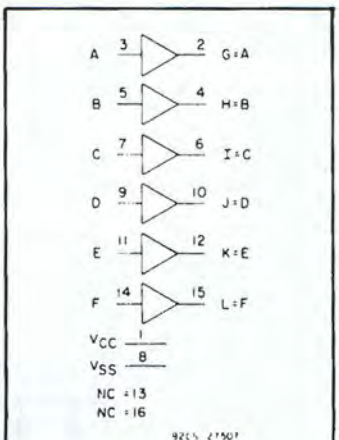
The RCA-CD4049UB and CD4050B are inverting and non-inverting hex buffers, respectively, and feature logic-level conversion using only one supply voltage (V_{CC}). The input-signal high level (V_{IH}) can exceed the V_{CC} supply voltage when these devices are used for logic-level conversions. These devices are intended for use as COS/MOS to DTL/TTL converters and can drive directly two DTL/TTL loads. (V_{CC}=5 V, $V_{OL} \leqslant$ 0.4 V, and $I_{OL} \geqslant$ 3.2 mA.)

The CD4049UB and CD4050B are designated as replacements for CD4009UB and CD4010B, respectively. Because the CD4049UB and CD4050B require only one power supply, they are preferred over the CD4009UB and CD4010B and should be used in place of the CD4009UB and CD4010B in all inverter, current driver, or logic-level conversion applications. In these applications the CD4049UB and CD4050B are pin compatible with the CD4009UB and CD4010B respectively, and can be substituted for these devices in existing as well as in new designs. Terminal No. 16 is not connected internallyon the CD4049UB or CD4050B, therefore, connection to this terminal is of no consequence to circuit operation. For applications not requiring high sink-current or voltage conversion, the CD4069UB Hex Inverter is recommended.

The CD4049UB and CD4050B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).

Applications:

- **COS/MOS to DTL/TTL hex converter**
- **COS/MOS current "sink" or "source" driver**
- **COS/MOS high-to-low logic-level converter**



CD4050B
FUNCTIONAL DIAGRAM

Printed in USA/9-76

Supersedes issue dated 2-76

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{CC})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to +20.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

RECOMMENDED OPERATING CONDITIONS at T_A=25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (V_{CC}) (For T_A=Full Package-Temperature Range)	3	18	V
Input Voltage Range (V_{IN})	V_{CC}*	18	V

*The CD4049 and CD4050 have high-to-low-level voltage conversion capability but not low-to-high-level; therefore it is recommended that $V_{IN} \geq V_{CC}$.

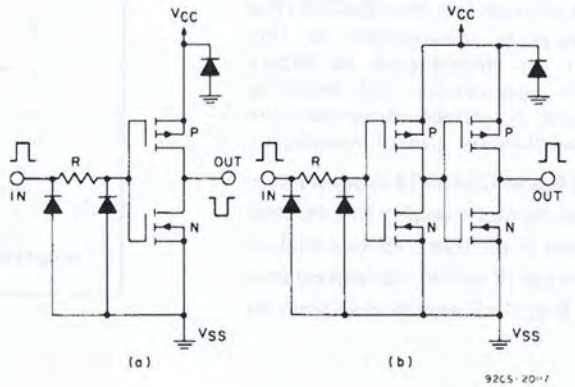


Fig. 1—a) Schematic diagram of CD4049UB, 1 of 6 identical units; b) Schematic diagram of CD4050B, 1 of 6 identical units.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			Limits At Indicated Temperatures (°C) *Values at −55,+25,+125 Apply to D,K,F,H Pkgs. Values at −40,+25,+85 Apply to E Package*							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	1	1	30	30	–	0.02	1	μA
	–	0,10	10	2	2	60	60	–	0.02	2	
	–	0,15	15	4	4	120	120	–	0.02	4	
	–	0,20	20	20	20	600	600	–	0.04	20	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	4.5	3.3	3.1	2.1	1.8	2.6	5.2	–	mA
	0.4	0,5	5	4	3.8	2.9	2.4	3.2	6.4	–	
	0.5	0,10	10	10	9.6	6.6	5.6	8	16	–	
	1.5	0,15	15	26	25	20	18	24	48	–	
Output High (Source) Current I_{OH} Min.	4.6	0,5	5	−1	−0.9	−0.72	−0.6	−0.8	−1.6	–	
	2.5	0,5	5	−4	−3.6	−2.6	−2.3	−3.2	−6.4	–	
	9.5	0,10	10	−2.2	−2	−1.5	−1.3	−1.8	−3.6	–	
	13.5	0,15	15	−6.6	−6.4	−5	−4.4	−6	−12	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05					0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage: V_{IL} Max. CD4049UB	4.5	–	5	1				–	–	1	V
	9	–	10	2				–	–	2	
	13.5	–	15	2.5				–	–	2.5	
Input Low Voltage: V_{IL} Max. CD4050B	0.5	–	5	1.5				–	–	1.5	
	1	–	10	3				–	–	3	
	1.5	–	15	4				–	–	4	
Input High Voltage: V_{IH} Min. CD4049UB	0.5	–	5	4				4	–	–	
	1	–	10	8				8	–	–	
	1.5	–	15	12.5				12.5	–	–	
Input High Voltage: V_{IH} Min. CD4050B	1.5	–	5	3.5				3.5	–	–	
	9	–	10	7				7	–	–	
	13.5	–	15	11				11	–	–	
Input Current, I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=25°C; Input t_r,t_f=20 ns, C_L=50 pF, R_L=200 kΩ

CHARACTERISTIC	CONDITIONS		LIMITS ALL PKGS.		UNITS
	V_{IN}	V_{CC}	Typ.	Max.	
Propagation Delay Time:					
Low-to-High, t_{PLH}					
CD4049UB	5	5	60	120	ns
	10	10	32	65	
	10	5	45	90	
	15	15	25	50	
	15	5	45	90	
CD4050B	5	5	70	140	
	10	10	40	80	
	10	5	45	90	
	15	15	30	60	
	15	5	40	80	
High-to-Low, t_{PHL}					
CD4049UB	5	5	32	65	ns
	10	10	20	40	
	10	5	15	30	
	15	15	15	30	
	15	5	10	20	
CD4050B	5	5	55	110	
	10	10	22	55	
	10	5	50	100	
	15	15	15	30	
	15	5	50	100	
Transition Time:					
Low-to-High, t_{TLH}	5	5	80	160	ns
	10	10	40	80	
	15	15	30	60	
High-to-Low, t_{THL}	5	5	30	60	
	10	10	20	40	
	15	15	15	30	
Input Capacitance, C_{IN}					
CD4049UB			15	22.5	pF
CD4050B	—	—	5	7.5	

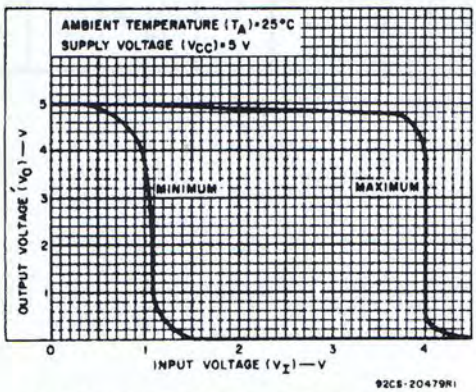


Fig. 2—Minimum and maximum voltage transfer characteristics for CD4049UB.

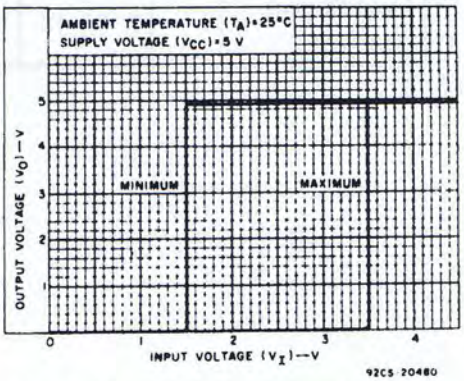


Fig. 3—Minimum and maximum voltage transfer characteristics for CD4050B.

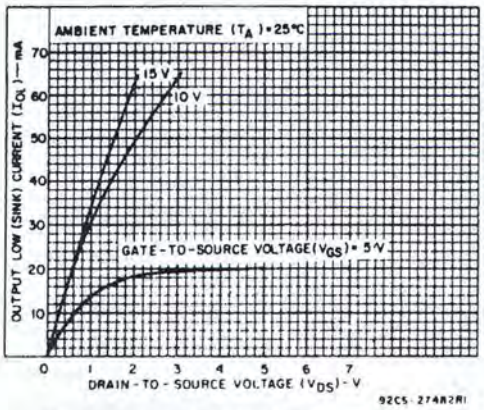


Fig. 4 – Typical output low (sink) current characteristics.

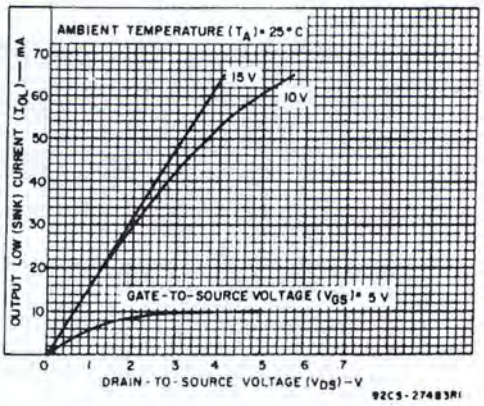


Fig. 5 – Minimum output low (sink) current drain characteristics.

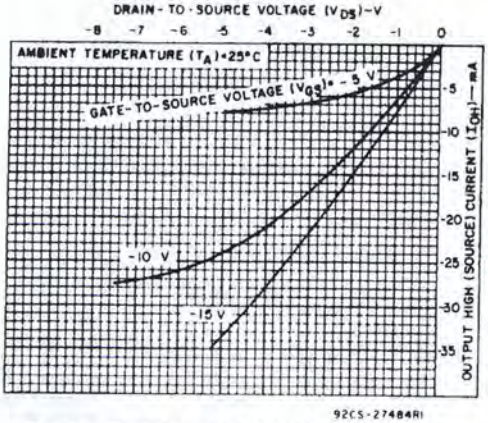


Fig. 6 – Typical output high (source) current characteristics.

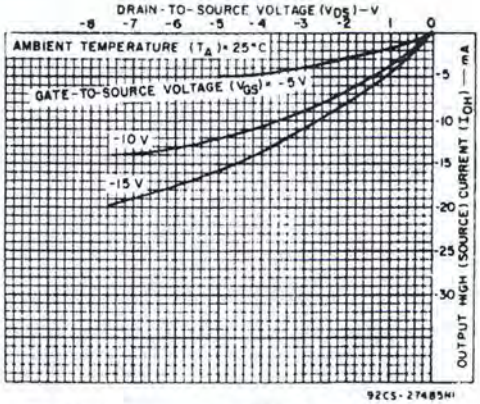


Fig. 7 – Minimum output high (source) current characteristics.

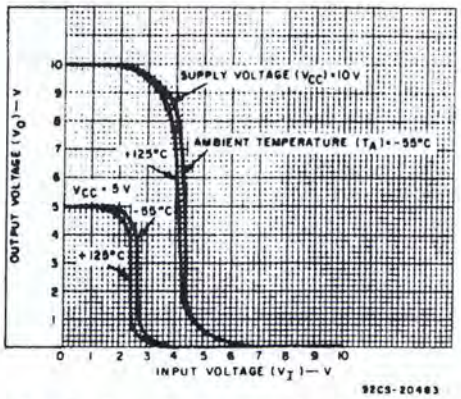


Fig. 8 – Typical voltage transfer characteristics as a function of temperature for CD4049UB.

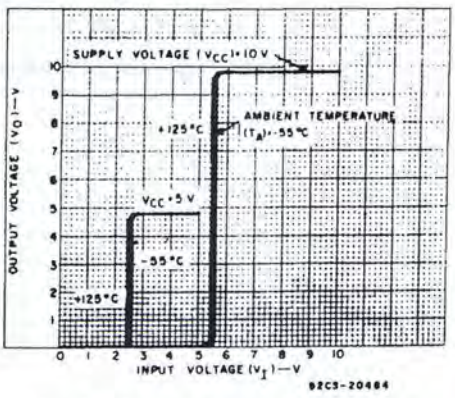


Fig. 9 – Typical voltage transfer characteristics as a function of temperature for CD4050B.

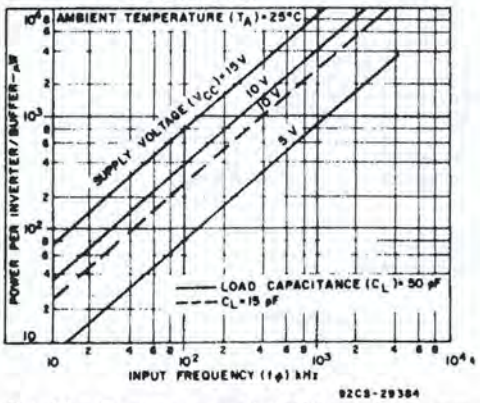


Fig. 10 – Typical power dissipation vs. frequency characteristics.

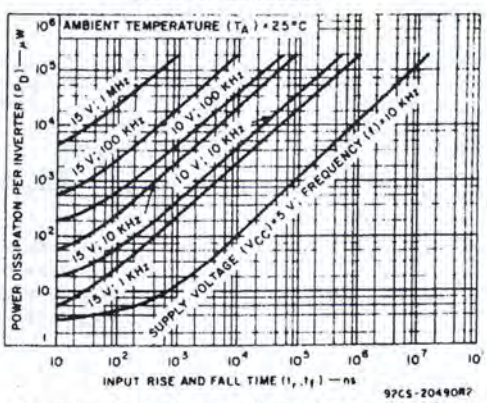


Fig. 11 – Typical power dissipation vs. transition time per inverter for CD4049UB.

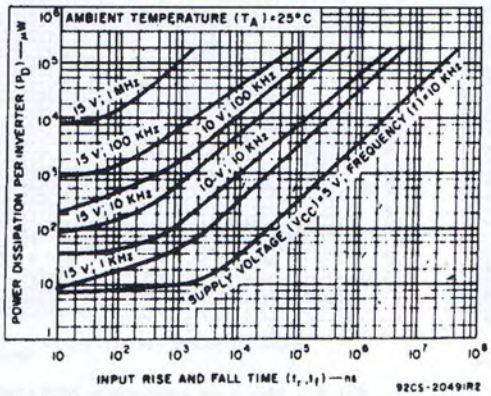


Fig. 12 – Typical power dissipation vs. transition timer per inverter for CD4050B.

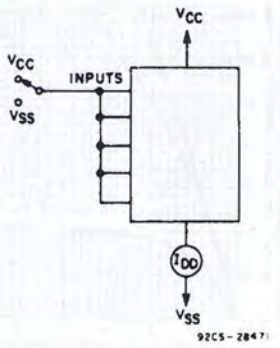


Fig. 13 – Quiescent device current test circuit.

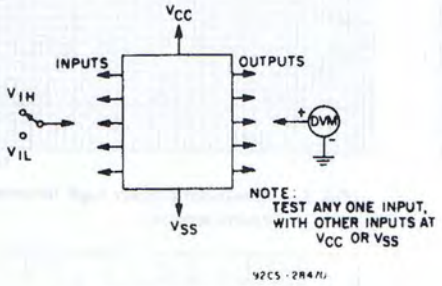


Fig. 14 – Input voltage test circuit.

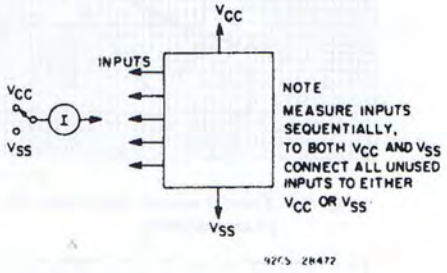


Fig. 15 – Input current test circuit.

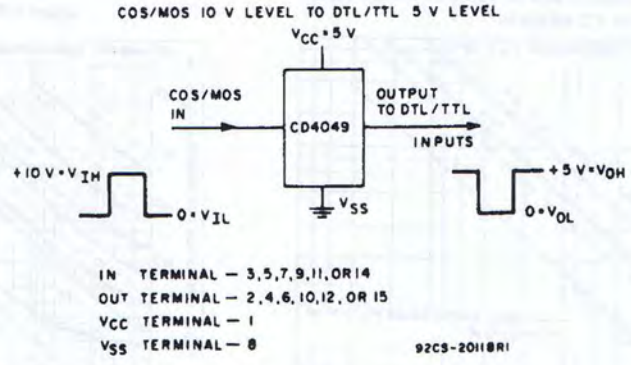


Fig. 16 – Logic-level conversion application.

OPERATING AND HANDLING CONSIDERATIONS

1. **Handling**
   All inputs and outputs of RCA COS/MOS devices have a network for electrostatic protection during handling. Recommended handling practices for COS/MOS devices are described in ICAN-6525, "Guide to Better Handling and Operation of CMOS Integrated Circuits."
2. **Operating**

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause V_{CC} - V_{SS} to exceed the absolute maximum rating.

Input Signals

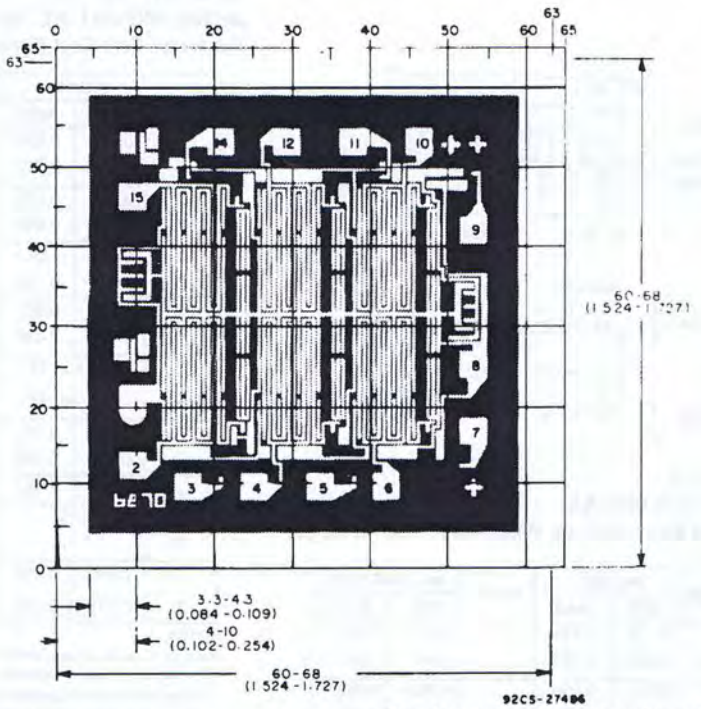
To prevent damage to the input protection circuit, input signals should never be less than V_{SS}. Input currents must not exceed 10 mA even when the power supply is off.

Unused Inputs

A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{CC} or V_{SS}, whichever is appropriate.

Output Short Circuits

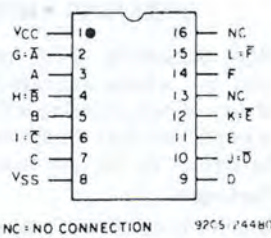
Shorting of outputs to V_{CC} or V_{SS} may damage COS/MOS devices by exceeding the maximum device dissipation.



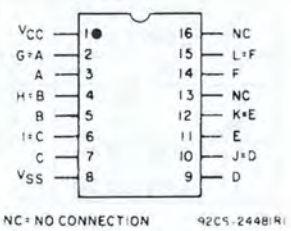
Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

Photograph of chip for CD4049UB. Dimensions and pad layout for CD4050B are identical.

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.



CD4049

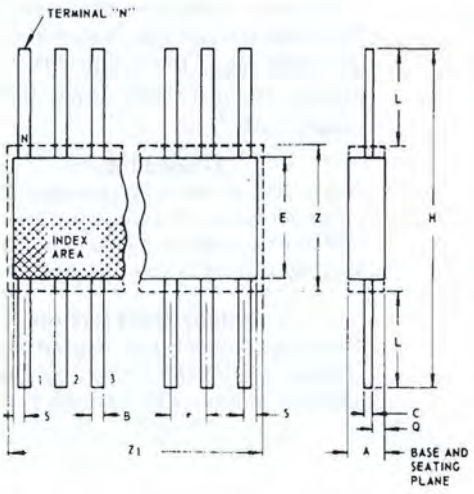


CD4050

TERMINAL ASSIGNMENTS

DIMENSIONAL OUTLINES

(K) Suffix
JEDEC MO-004-AG
16-Lead Ceramic Flat Pack

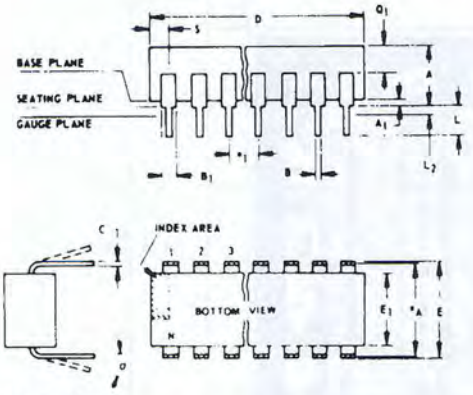


SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.008	0.100		0.21	2.54
B	0.015	0.019	1	0.381	0.482
C	0.003	0.006	1	0.077	0.152
e	0.050 TP		2	1.27 TP	
E	0.200	0.300		5.1	7.6
H	0.600	1.000		15.3	25.4
L	0.150	0.350		3.9	8.8
N	16		3	16	
Q	0.005	0.050		0.13	1.27
S	0.000	0.025		0.00	0.63
Z	0.300		4	7.62	
Z_1	0.400		4	10.16	

92CS-17271R2

NOTES:
1. Refer to Rules for Dimensioning (JEDEC Publication No. 13) for Axial Lead Product Outlines.
2. Leads within .005" (.12 mm) radius of True Position (TP) at maximum material condition.
3. N is the maximum quantity of lead positions.
4. Z and Z_1 determine a zone within which all body and lead irregularities lie.

(E) and (F) Suffixes
JEDEC MO-001-AC 16-Lead Dual-In-Line
Plastic or Frit-Seal Ceramic Package



SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.155	0.200		3.94	5.08
A_1	0.020	0.050		0.51	1.27
B	0.014	0.020		0.356	0.508
B_1	0.035	0.065		0.89	1.65
C	0.008	0.012	1	0.204	0.304
D	0.745	0.785		18.93	19.93
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.76
α	0°	15°	4	0°	15°
N	16		5	16	
N_1	0		6	0	
Q_1	0.040	0.075		1.02	1.90
S	0.015	0.060		0.39	1.52

92CM-15967R3

NOTES:
Refer to Rules for Dimensioning (JEDEC Publication No. 13) for Axial Lead Product Outlines.
1. When this device is supplied solder dipped, the maximum lead thickness (narrow portion) will not exceed 0.013" (0.33 mm).
2. Leads within 0.005" (0.12 mm) radius of True Position (TP) at gauge plane with maximum material condition and unit installed.
3. e_A applies in zone L_2 when unit installed.
4. α applies to spread leads prior to installation.
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads.

(D) Suffix
JEDEC MO-001-AE
16-Lead Dual-In-Line White-Ceramic Package

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.120	0.160		3.05	4.06
A_1	0.020	0.065		0.51	1.65
B	0.014	0.020		0.356	0.508
B_1	0.035	0.065		0.89	1.65
C	0.008	0.012	1	0.204	0.304
D	0.745	0.785		18.93	19.93
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.76
α	0°	15°	4	0°	15°
N	16		5	16	
N_1	0		6	0	
Q_1	0.050	0.085		1.27	2.15
S	0.015	0.060		0.39	1.52

92SS-4286R4

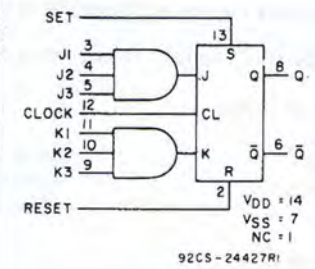
When incorporating RCA Solid State Devices in equipment, it is recommended that the designer refer to "Operating Considerations for RCA Solid State Devices", Form No. 1CE-402, available on request from RCA Solid State Division, Box 3200, Somerville, N. J. 08876.

ORDERING INFORMATION

RCA COS/MOS device packages are identified by letters indicated in the following chart. When ordering a COS/MOS device, it is important that the appropriate suffix letter be affixed to the type number of the device.

Package	Suffix Letter
Dual-In-Line White Ceramic	D
Dual-In-Line Frit-Seal Ceramic	F
Dual-In-Line Plastic	E
Ceramic Flat Package	K
Chip	H

For example, a CD4050B in a dual-in-line plastic package will be identified as the



CD4095B
Functional Diagram

COS/MOS Gated J-K Master-Slave Flip-Flops

With Set-Reset Capability
High-Voltage Types (20-Volt Rating)

CD4095B Non-Inverting J and K Inputs
CD4096B Inverting and Non-Inverting J and K Inputs

Features:

- **16 MHz toggle rate (typ.) at $V_{DD} - V_{SS} = 10$ V**
- **Gated inputs**
- **100% tested for quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C**
- **Noise margin over full package-temperature range: 1 V at V_{DD} = 5 V, 2 V at V_{DD} = 10 V, 2.5 V at V_{DD} = 15 V**
- **5-V, 10-V, and 15-V parametric ratings**
- **Standardized, symmetrical output characteristics**

Applications:

- **Registers** ■ **Counters** ■ **Control circuits**

The RCA-CD4095B and CD4096B are J-K Master-Slave Flip-Flops featuring separate AND gating of multiple J and K inputs. The gated J-K inputs control transfer of information into the master section during clocked operation. Information on the J-K inputs is transferred to the Q and $\overline{Q}$ outputs on the positive edge of the clock pulse. SET and RESET inputs (active high) are provided for asynchronous operation.

The CD4095B and CD4096B types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic package (E suffix), 14-lead ceramic flat package (K suffix), and in chip form (H suffix).

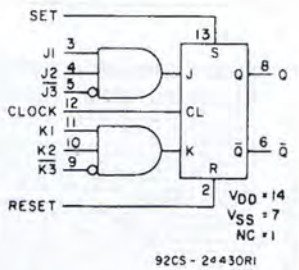


Fig. 1 – CD4096B Functional Diagram.

TRUTH TABLES

SYNCHRONOUS OPERATION (S=0 R=0)

Inputs Before Positive Clock Transition		Outputs After Positive Clock Transition	
J*	K*	Q	$\overline{Q}$
0	0	No Change	
0	1	0	1
1	0	1	0
1	1	Toggles	

* For CD4095B: J = J1 · J2 · J3; K = K1 · K2 · K3
For CD4096B: J = J1 · J2 · $\overline{J3}$; K = K1 · K2 · $\overline{K3}$

ASYNCHRONOUS OPERATION (J and K - DON'T CARE)

S	R	Q	$\overline{Q}$
0	0	No Change	
0	1	0	1
1	0	1	0
1	1	0	0

0 = V_{SS}, 1 = V_{DD}

Printed in USA/9-76

Supersedes issue dated 3-76

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25° C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS		UNITS
		MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	18	V
Data Setup Time, t_S	5	400	–	ns
	10	160	–	
	15	100	–	
Clock Pulse Width, t_W	5	140	–	ns
	10	60	–	
	15	40	–	
Clock Input Frequency, f_{CL}	5	dc	3.5	MHz
	10		8	
	15		12	
Clock Rise and Fall Time, t_rCL, t_fCL:	5	–	15	μs
	10	–	5	
	15	–	5	
Set or Reset Pulse Width, t_W	5	200	–	ns
	10	100	–	
	15	50	–	

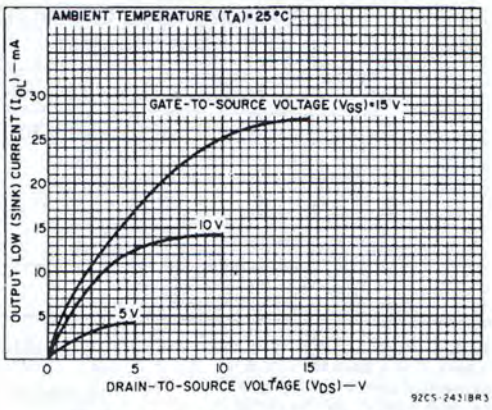


Fig.2 – Typical output low (sink) current characteristics.

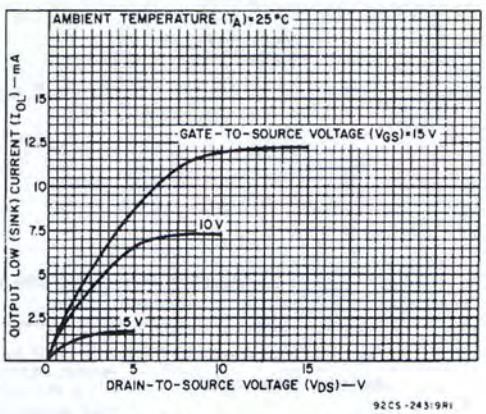


Fig.3 – Minimum output low (sink) current characteristics.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,K,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
									+25		
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	1	1	30	30	–	0.02	1	μA
	–	0,10	10	2	2	60	60	–	0.02	2	
	–	0,15	15	4	4	120	120	–	0.02	4	
	–	0,20	20	20	20	600	600	–	0.04	20	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3 4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				—	—	1.5	V
	1, 9	–	10	3				—	—	3	
	15, 13.5	–	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	—	—	
	1, 9	–	10	7				7	—	—	
	1.5, 13.5	–	15	11				11	—	—	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

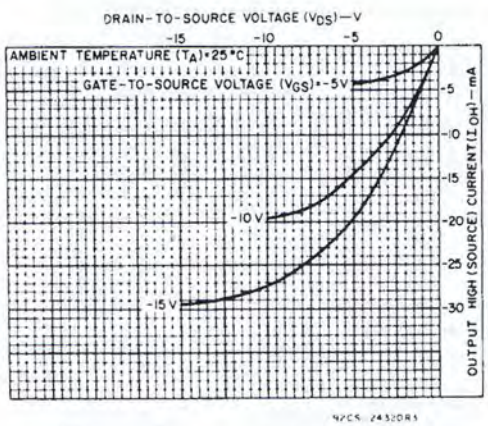


Fig.4 – Typical output high (source) current characteristics.

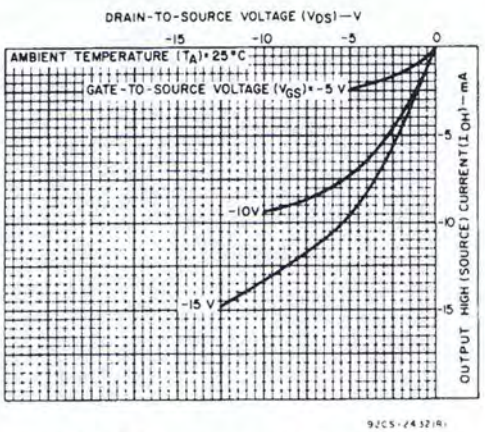


Fig.5 – Minimum output high (source) current characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ

CHARACTERISTIC	TEST CONDITIONS		LIMITS			UNITS
		V_{DD} (V)	MIN.	TYP.	MAX.	
Propagation Delay Time: t_{PHL}, t_{PLH}		5	–	250	500	ns
		10	–	100	200	
		15	–	75	150	
Set or Reset		5	–	150	300	
		10	–	75	150	
		15	–	50	100	
Transition Time, t_{THL}, t_{TLH}		5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
Maximum Clock Input Frequency, (f_{CL})		5	3.5	7	–	MHz
		10	8	16	–	
		15	12	24	–	
Minimum Clock Pulse Width, t_W		5	–	70	140	ns
		10	–	30	60	
		15	–	20	40	
Clock Input Rise or Fall Time, t_{rcl}, t_{rcf}		5	–	–	15	μs
		10	–	–	5	
		15	–	–	5	
Minimum Set or Reset Pulse Width, t_W		5	–	100	200	ns
		10	–	50	100	
		15	–	25	50	
Minimum Data Setup Time, t_S		5	–	200	400	ns
		10	–	80	160	
		15	–	50	100	
Input Capacitance, C_{IN}	Any Input	–	–	5	7.5	pF

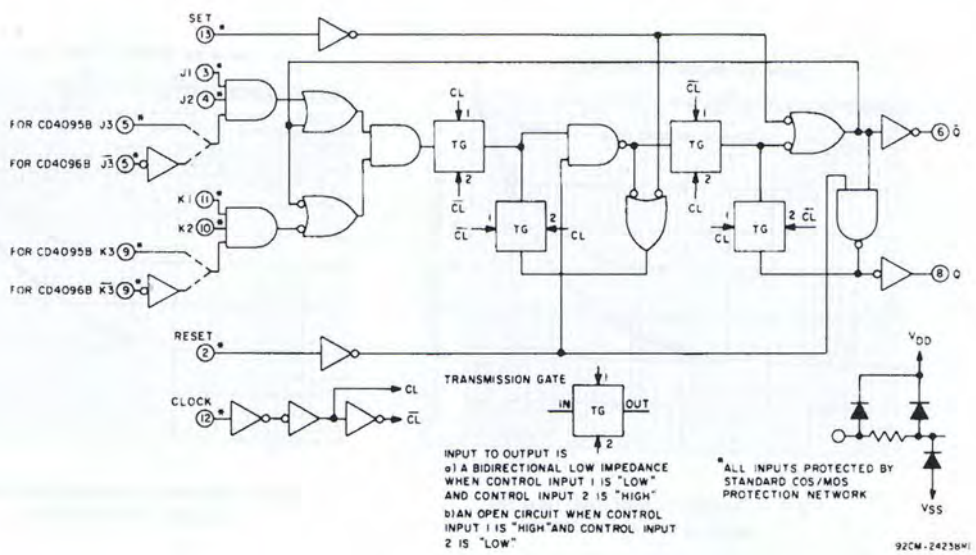


Fig.6 – CD4095B and CD4096B logic diagram.

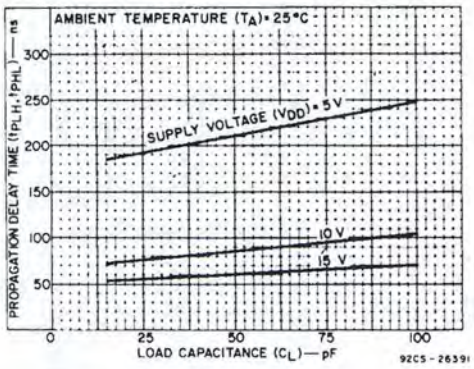


Fig.7 – Typical propagation delay time vs. load capacitance.

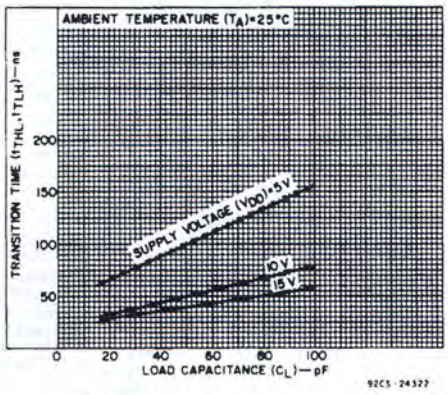


Fig.8 – Typical transition time vs. load capacitance.

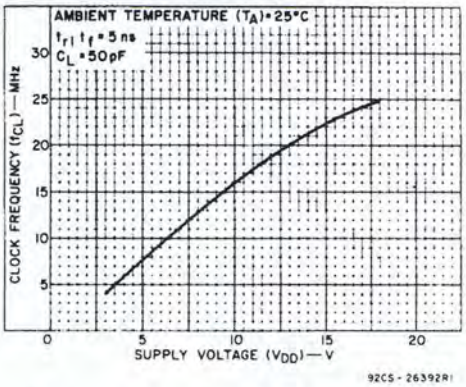


Fig. 9 – Typical clock frequency vs. supply voltage (toggle mode–see Fig. 16).

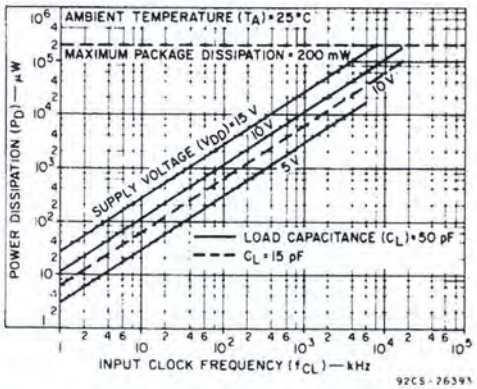


Fig.10 – Typical power dissipation vs. input clock frequency.

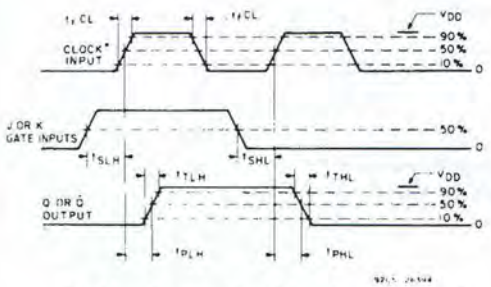


Fig.11 – Propagation delay, transition, and setup-time waveforms.

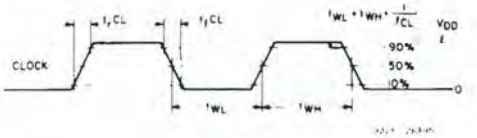


Fig.12 – Clock pulse rise and fall time waveforms.

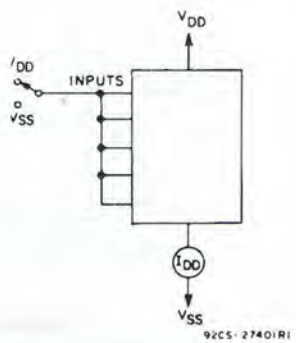


Fig.13 – Quiescent device current test circuit.

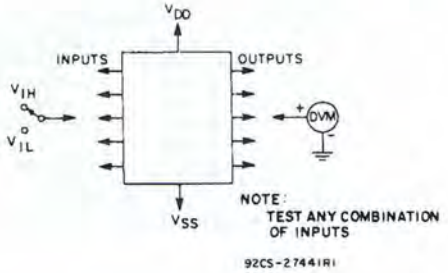


Fig.14 – Input voltage test circuit.

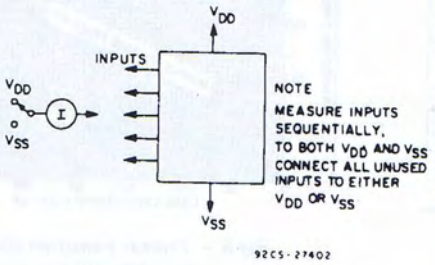


Fig. 15 – Input leakage current test circuit.

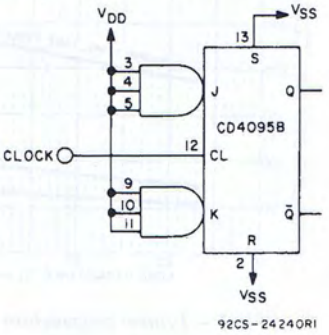


Fig. 16 – CD4095B connected in toggle mode.

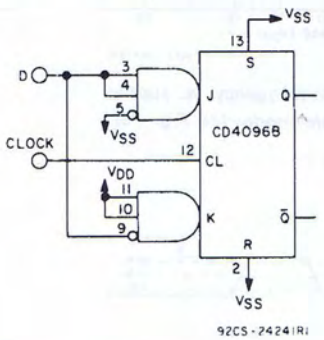
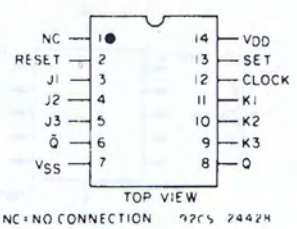
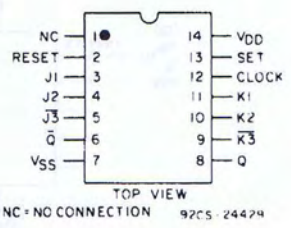


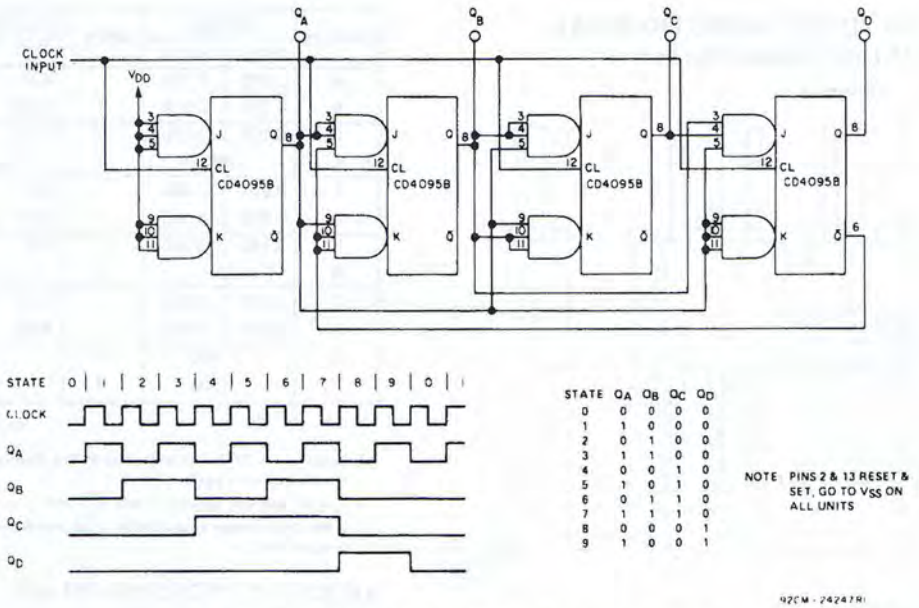
Fig. 17 – CD4096B connected as a "D" type flip-flop.



CD4095B
TERMINAL ASSIGNMENTS



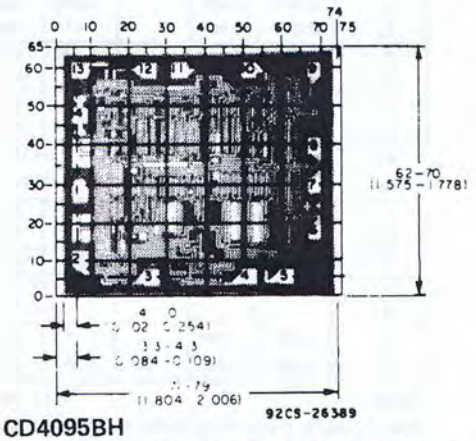
CD4096B
TERMINAL ASSIGNMENTS



STATE	Q_A	Q_B	Q_C	Q_D
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1

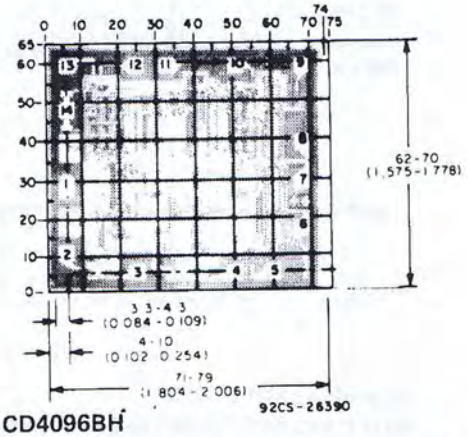
Fig. 18 – Synchronous binary divide-by-ten counter.

DIMENSIONS AND PAD LAYOUT FOR CD4095B AND CD4096B



CD4095BH

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.



CD4096BH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

OPERATING AND HANDLING CONSIDERATIONS

1. **Handling**
   All inputs and outputs of RCA COS/MOS devices have a network for electrostatic protection during handling. Recommended handling practices for COS/MOS devices are described in ICAN-6525, "Guide to Better Handling and Operation of CMOS Integrated Circuits."
2. **Operating**

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause $V_{DD}-V_{SS}$ to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} nor less than V_{SS}. Input currents must not exceed 10 mA even when the power supply is off.

Unused Inputs

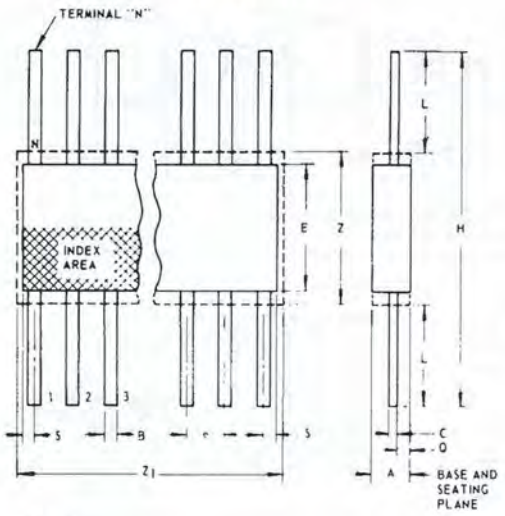
A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{DD} or V_{SS}, whichever is appropriate.

Output Short Circuits

Shorting of outputs to V_{DD} or V_{SS} may damage COS/MOS devices by exceeding the maximum device dissipation.

DIMENSIONAL OUTLINES

(K) SUFFIX (JEDEC MO-004-AF)
14-Lead Ceramic Flat Pack



NOTES:

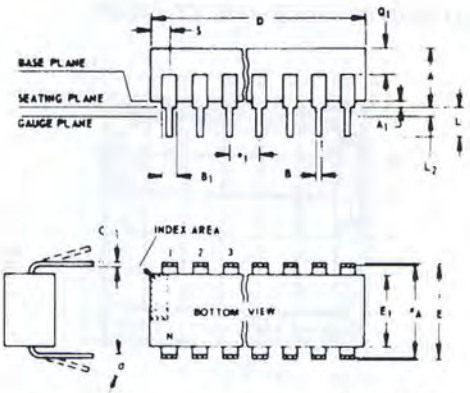
1. Refer to Rules for Dimensioning (JEDEC Publication No. 13) for Axial Lead Product Outlines.

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.008	0.100		0.21	2.54
B	0.015	0.019	1	0.381	0.482
C	0.003	0.006	1	0.077	0.152
e	0.050 TP		2	1.27 TP	
E	0.200	0.300		5.1	7.6
H	0.600	1.000		15.3	25.4
L	0.150	0.350		3.9	8.8
N	14		3	14	
Q	0.005	0.050		0.13	1.27
S	0.000	0.050		0.00	1.27
Z	0.300		4	7.62	
Z_1	0.400		4	10.16	

92SS-4300R2

2. Leads within .005" (.12 mm) radius of True Position (TP) at maximum material condition.
3. N is the maximum quantity of lead positions.
4. Z and Z_1 determine a zone within which all body and lead irregularities lie.

(D) SUFFIX (JEDEC MO-001-AD)
14-Lead Dual-in-Line White Ceramic Package



SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.120	0.160		3.05	4.06
A_1	0.020	0.065		0.51	1.65
B	0.014	0.020		0.356	0.508
B_1	0.050	0.065		1.27	1.65
C	0.008	0.012	1	0.204	0.304
D	0.745	0.770		18.93	19.55
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.76
α	0°	15°	4	0°	15°
N	14		5	14	
N_1	0		6	0	
Q_1	0.050	0.085		1.27	2.15
S	0.065	0.090		1.66	2.28

NOTES 92SS-4411R1

Refer to Rules for Dimensioning (JEDEC Publication No. 13) for Axial Lead Product Outlines.

1. When this device is supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013".
2. Leads within 0.005" (0.12 mm) radius of True Position (TP) at guage plane with maximum material condition and unit installed.
3. e_A applies in zone L_2 when unit installed.
4. α applies to spread leads prior to installation.
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads.

(E) and (F) SUFFIXES
JEDEC MO-001-AB 14-Lead Dual-In-Line Plastic or Frit-Seal Ceramic Package

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.155	0.200		3.94	5.08
A_1	0.020	0.050		0.51	1.27
B	0.014	0.020		0.356	0.508
B_1	0.050	0.065		1.27	1.65
C	0.008	0.012	1	0.204	0.304
D	0.745	0.770		18.93	19.55
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.76
α	0°	15°	4	0°	15°
N	14		5	14	
N_1	0		6	0	
Q_1	0.040	0.075		1.02	1.90
S	0.065	0.090		1.66	2.28

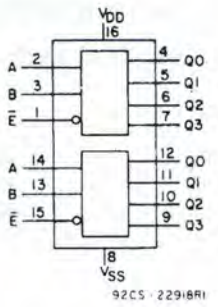
When incorporating RCA Solid State Devices in equipment, it is recommended that the designer refer to "Operating Considerations for RCA Solid State Devices", Form No. 1CE-402, available on request from RCA Solid State Division, Box 3200, Somerville, N. J. 08876.

ORDERING INFORMATION

RCA COS/MOS device packages are identified by letters indicated in the following chart. When ordering a COS/MOS device, it is important that the appropriate suffix letter be affixed to the type number of the device.

Package	Suffix Letter
Dual-In-Line White Ceramic	D
Dual-In-Line Frit-Seal Ceramic	F
Dual-In-Line Plastic	E
Ceramic Flat Package	K
Chip	H

For example, a CD4095B in a dual-in-line plastic package will be identified as the CD4095BE.



CD4555B
Functional Diagram

COS/MOS Dual Binary to 1 of 4 Decoder/Demultiplexers

High-Voltage Types (20-Volt Rating)

CD4555B: Outputs High on Select
CD4556B: Outputs Low on Select

Features:

- Expandable with multiple packages
- Standard, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range): 1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- 5-V, 10-V, and 15-V parametric ratings

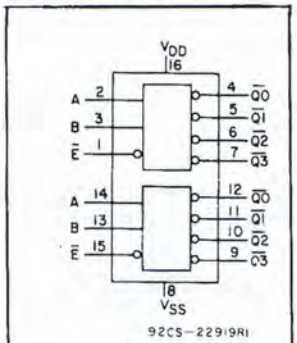
Applications:

- Decoding
- Code conversion
- Demultiplexing (using Enable input as a data input)
- Memory chip-enable selection
- Function selection

The RCA-CD4555B and CD4556B are dual one-of-four decoders/demultiplexers. Each decoder has two select inputs (A and B), an Enable input ($\bar{E}$), and four mutually exclusive outputs. On the CD4555B the outputs are high on select; on the CD4556B the outputs are low on select.

When the Enable input is high, the outputs of the CD4555B remain low and the outputs of the CD4556B remain high regardless of the state of the select inputs A and B. The CD4555B and CD4556B are similar to types MC14555 and MC14556, respectively.

The CD4555B and CD4556B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead-dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).



CD4556B
Functional Diagram

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	V_{DD}	MIN.	MAX.	UNITS
Supply Voltage Range (For T_A = Full Package Temp. Range)	–	3	18	V

Printed in USA/9-76

Supersedes issue dated 3-76

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

TRUTH TABLE

INPUTS			OUTPUTS CD4555B				OUTPUTS CD4556B			
ENABLE	SELECT									
$\overline{E}$	B	A	Q3	Q2	Q1	Q0	$\overline{Q3}$	$\overline{Q2}$	$\overline{Q1}$	$\overline{Q0}$
0	0	0	0	0	0	1	1	1	1	0
0	0	1	0	0	1	0	1	1	0	1
0	1	0	0	1	0	0	1	0	1	1
0	1	1	1	0	0	0	0	1	1	1
1	X	X	0	0	0	0	1	1	1	1

X = DON'T CARE

LOGIC 1 ≡ HIGH
LOGIC 0 ≡ LOW

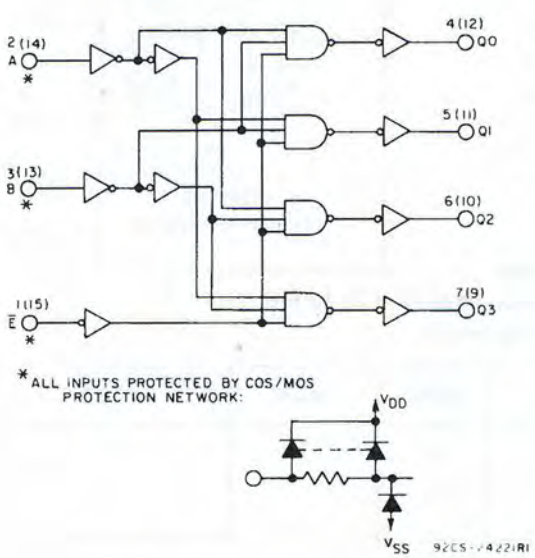


Fig. 1 – CD4555B logic diagram (1 of 2 identical circuits).

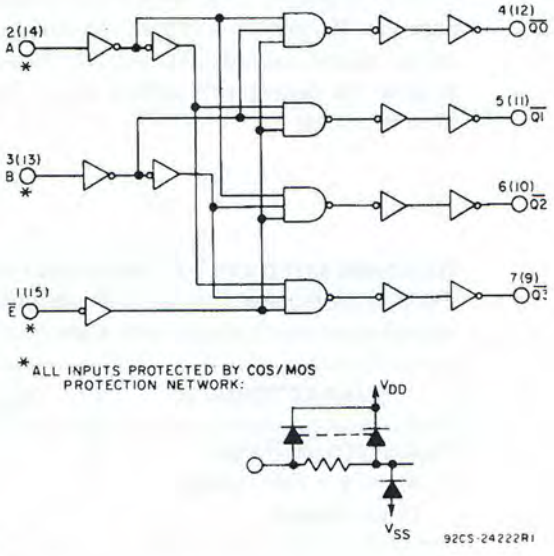
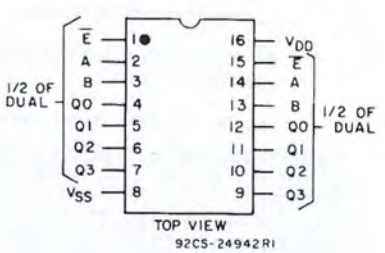


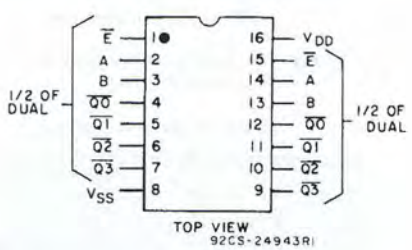
Fig. 2 – CD4556B logic diagram (1 of 2 identical circuits).

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,K,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1		mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6		
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8		
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1		
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2		
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6		
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8		
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5,4.5	–	5	1.5				—	—	1.5	
	1,9	–	10	3				—	—	3	
	1.5,13.5	–	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	—	—	
	1,9	–	10	7				7	—	—	
	1.5,13.5	–	15	11				11	—	—	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA



CD4555B



CD4556B

TERMINAL ASSIGNMENTS

DYNAMIC ELECTRICAL CHARACTERISTICS *at T_A = 25° C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ*

CHARACTERISTIC	TEST CONDITIONS	ALL TYPES LIMITS		UNITS
		V_{DD} Volts	TYP.	MAX.	
Propagation Delay Time, t_{PHL}, A or B Input to t_{PLH} Any Output		5	220	440	ns
		10	95	190	
		15	70	140	
$\overline{E}$ Input to Any Output		5	200	400	ns
		10	85	170	
		15	65	130	
Transition Time t_{THL}, t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance C_{IN}	Any Input		5	7.5	pF

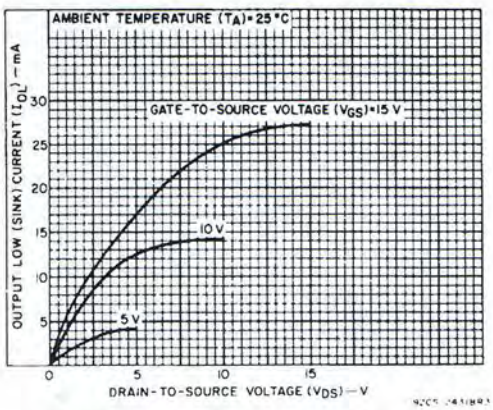


Fig. 3 – Typical output low (sink) current characteristics.

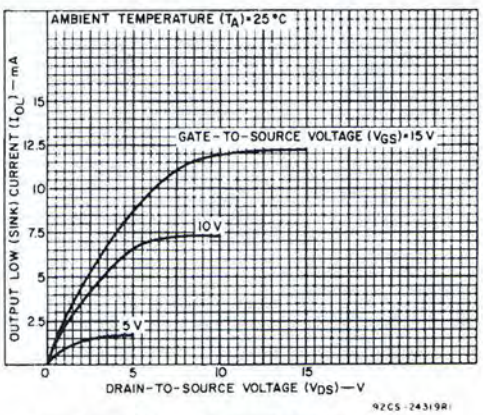


Fig. 4 – Minimum output low (sink) current characteristics.

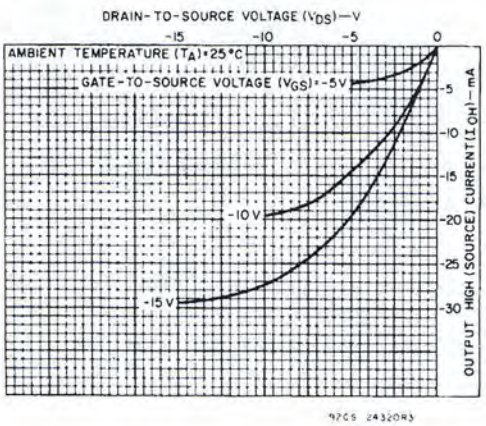


Fig. 5 – Typical output high (source) current characteristics.

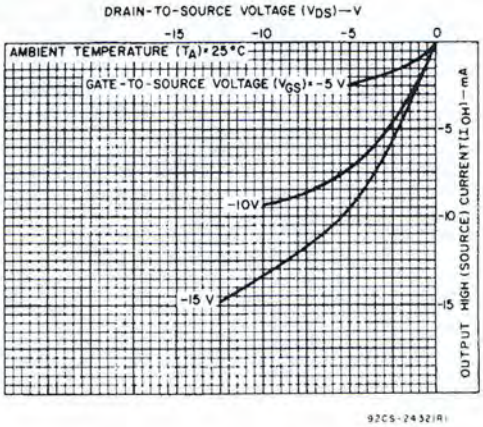


Fig. 6 – Minimum output high (source) current characteristics.

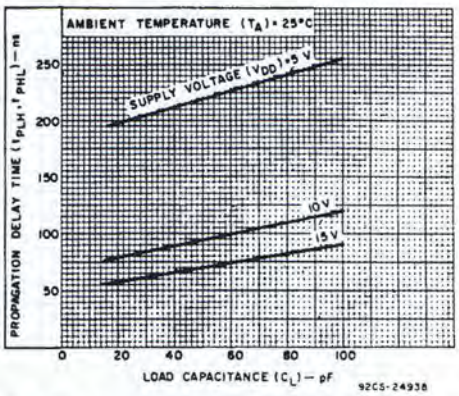


Fig. 7 – Typical propagation delay time vs. load capacitance (A or B input to any output).

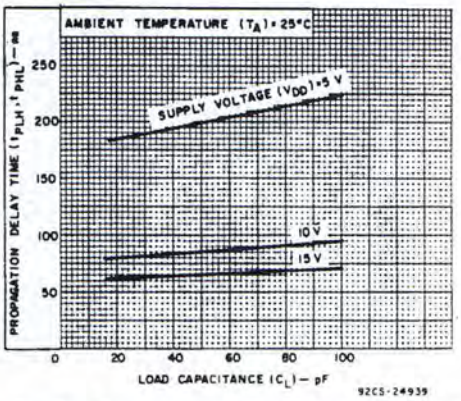


Fig. 8 – Typical propagation delay time vs. load capacitance ($\overline{E}$ input to any output).

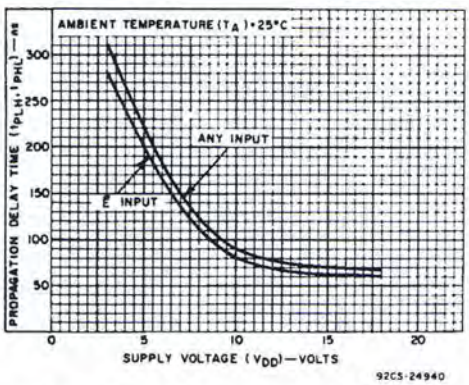


Fig. 9 – Typical propagation delay time vs. supply voltage.

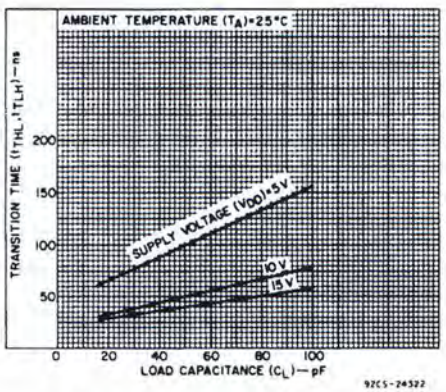


Fig. 10 – Typical transition time vs. load capacitance.

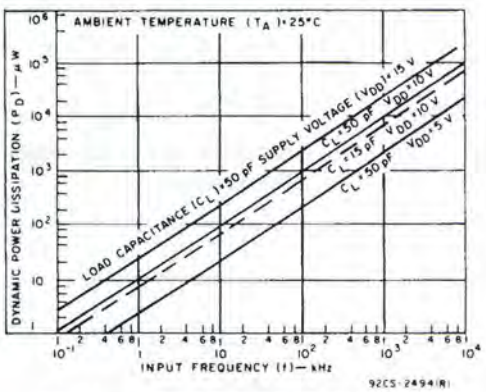
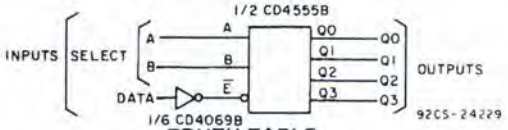


Fig. 11 – Typical dynamic power dissipation vs. frequency.

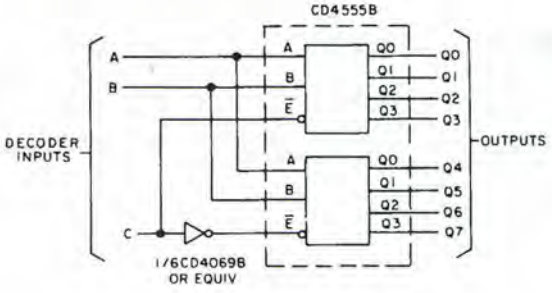
APPLICATIONS



TRUTH TABLE

SELECT INPUTS		OUTPUTS			
B	A	Q0	Q1	Q2	Q3
0	0	DATA	0	0	0
0	1	0	DATA	0	0
1	0	0	0	DATA	0
1	1	0	0	0	DATA

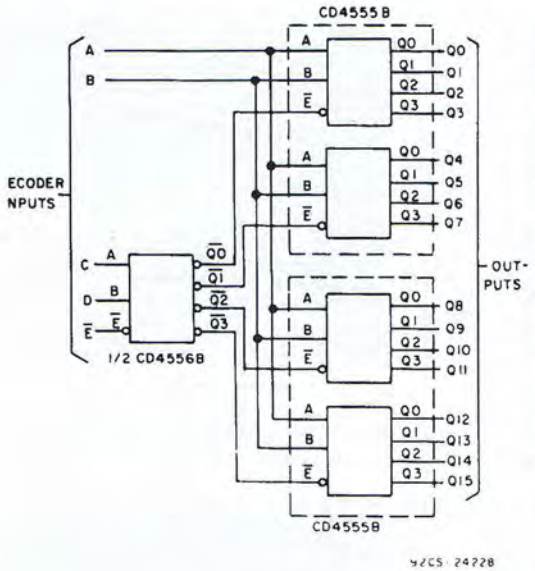
Fig. 12 – 1-of-4 line data demultiplexer using CD4555B.



TRUTH TABLE

INPUTS			Q OUTPUTS							
C	B	A	0	1	2	3	4	5	6	7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

Fig. 13 – 1-of-8 decoder using CD4555B.



TRUTH TABLE

INPUTS					Q OUTPUTS														
E	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	0	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
0	1	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
1	X	X	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

X = don't care

Fig. 14 – 1-of-16 decoder using CD4555B and CD4556B.

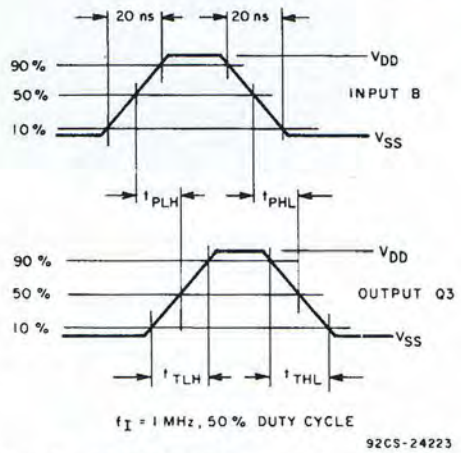


Fig. 15 – CD4555B B input to Q3 output dynamic signal waveforms.

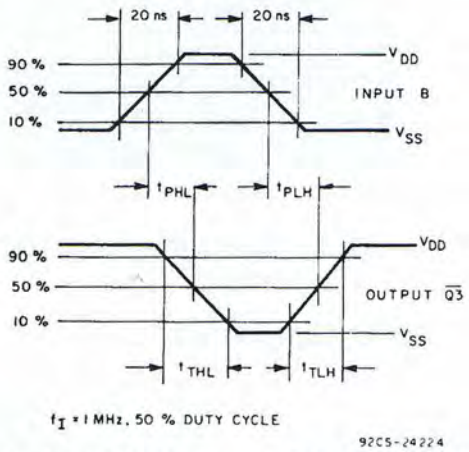


Fig. 16 – CD4556B B input to $\overline{Q3}$ output dynamic signal waveforms.

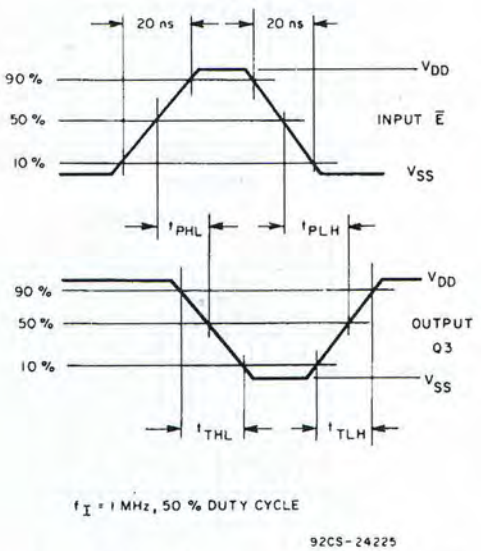


Fig. 17 – CD4555B $\overline{E}$ input to Q3 output dynamic signal waveforms.

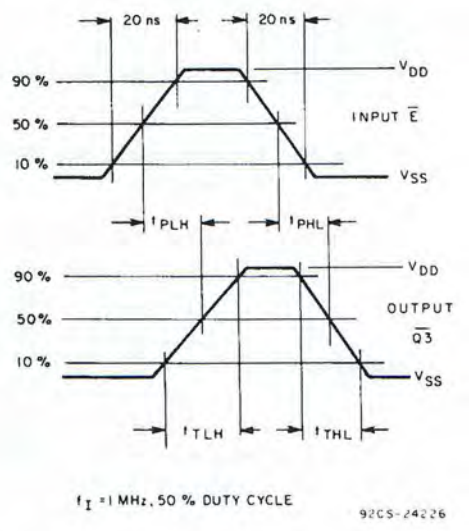


Fig. 18 – CD4556B $\overline{E}$ input to $\overline{Q}_3$ output dynamic signal waveforms.

TEST CIRCUITS

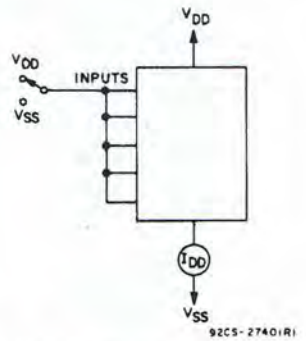


Fig. 19 – Quiescent device current test circuit.

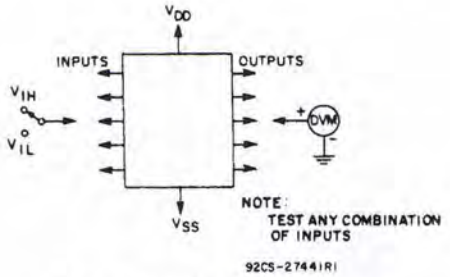


Fig. 20 – Input voltage test circuit.

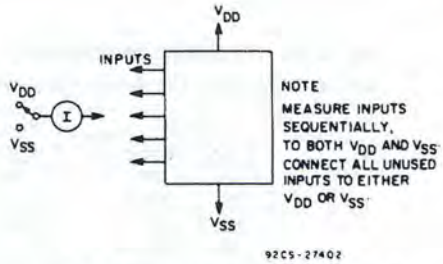
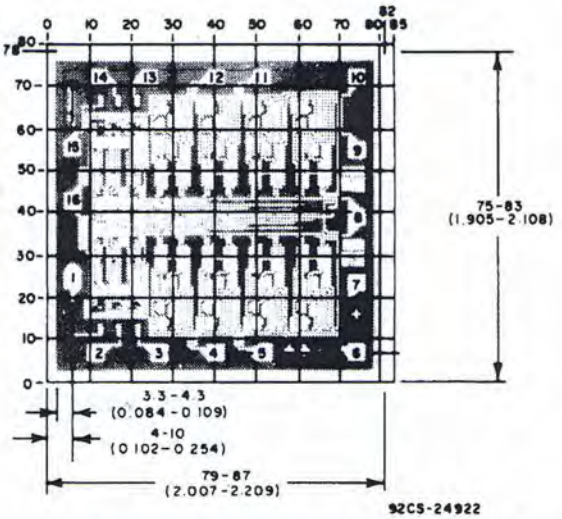


Fig. 21 – Input current test circuit.



DIMENSIONS AND PAD LAYOUT FOR CD4555BH. *(Dimensions and pad layout for CD4556BH are identical).*

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

OPERATING AND HANDLING CONSIDERATIONS

1. **Handling**

All inputs and outputs of RCA COS/MOS devices have a network for electrostatic protection during handling. Recommended handling practices for COS/MOS devices are described in ICAN-6525, "Guide to Better Handling and Operation of CMOS Integrated Circuits."

2. **Operating**

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause $V_{DD}-V_{SS}$ to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} nor less than V_{SS}. Input currents must not exceed 10 mA even when the power supply is off.

Unused Inputs

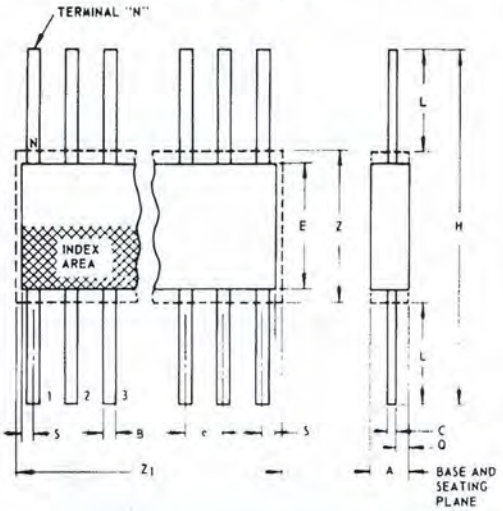
A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{DD} or V_{SS}, whichever is appropriate.

Output Short Circuits

Shorting of outputs to V_{DD} or V_{SS} may damage COS/MOS devices by exceeding the maximum device dissipation.

DIMENSIONAL OUTLINES

(K) SUFFIX (JEDEC MO-004-AF)
14-Lead Ceramic Flat Pack



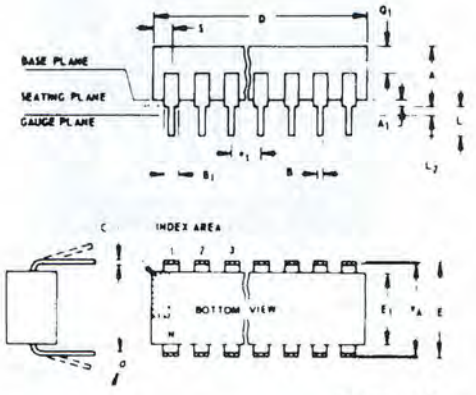
SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.008	0.100		0.21	2.54
B	0.015	0.019	1	0.381	0.482
C	0.003	0.006	1	0.077	0.152
e	0.050 TP		2	1.27 TP	
E	0.200	0.300		5.1	7.6
H	0.600	1.000		15.3	25.4
L	0.150	0.350		3.9	8.8
N	14		3	14	
Q	0.005	0.050		0.13	1.27
S	0.000	0.050		0.00	1.27
Z	0.300		4	7.62	
Z_1	0.400		4	10.16	

92SS-4300R2

NOTES:

1. Refer to Rules for Dimensioning Peripheral Lead Outlines.
2. Leads within .005" (.12 mm) radius of True Position (TP) at maximum material condition.
3. N is the maximum quantity of lead positions.
4. Z and Z_1 determine a zone within which all body and lead irregularities lie.

(D) SUFFIX (JEDEC MO-001-AD)
14-Lead Dual-in-Line White Ceramic Package



92SS-4296R2

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.120	0.160		3.05	4.06
A_1	0.020	0.065		0.51	1.65
B	0.014	0.020		0.356	0.508
B_1	0.050	0.065		1.27	1.65
C	0.008	0.012	1	0.204	0.304
D	0.745	0.770		18.93	19.55
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.76
α	0°	15°	4	0°	15°
N	14		5	14	
N_1	0		6	0	
Q_1	0.050	0.085		1.27	2.15
S	0.065	0.090		1.66	2.28

NOTES 92SS-4411R1

Refer to Rules for Dimensioning (JEDEC Publication No. 13) for Axial Lead Product Outlines

1. When this device is supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013".
2. Leads within 0.005" (0.12 mm) radius of True Position (TP) at guage plane with maximum material condition and unit installed.
3. e_A applies in zone L_2 when unit installed.
4. α applies to spread leads prior to installation.
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads.

(E) and F SUFFIXES
JEDEC MO-001-AB 14-Lead Dual-In-Line Plastic or Frit-Seal Ceramic Package

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.155	0.200		3.94	5.08
A_1	0.020	0.050		0.51	1.27
B	0.014	0.020		0.356	0.508
B_1	0.050	0.065		1.27	1.65
C	0.008	0.012	1	0.204	0.304
D	0.745	0.770		18.93	19.55
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.76
α	0°	15°	4	0°	15°
N	14		5	14	
N_1	0		6	0	
Q_1	0.040	0.075		1.02	1.90
S	0.065	0.090		1.66	2.28

When incorporating RCA Solid State Devices in equipment, it is recommended that the designer refer to "Operating Considerations for RCA Solid State Devices", Form No. 1CE-402, available on request from RCA Solid State Division, Box 3200, Somerville, N. J. 08876.

ORDERING INFORMATION

RCA COS/MOS device packages are identified by letters indicated in the following chart. When ordering a COS/MOS device, it is important that the appropriate suffix letter be affixed to the type number of the device.

Package	Suffix Letter
Dual-In-Line White Ceramic	D
Dual-In-Line Frit-Seal Ceramic	F
Dual-In-Line Plastic	E
Ceramic Flat Package	K
Chip	H

For example, a CD4555B in a dual-in-line plastic package will be identified as the CD4555BE.

40-Lead Dual-In-Line Ceramic Package (D)

CDP1802D
CDP1802CD H-1847

COSMAC Microprocessor

Features:

- Instruction fetch-execute time of 2.5 or 3.75 μs at V_{DD} = 10 V; 5.0 or 7.5 μs at V_{DD} = 5 V
- Static silicon-gate CMOS circuitry — no minimum clock frequency
- Full military temperature range (−55 to +125°C)
- High noise immunity, wide operating-voltage range
- Single voltage supply
- Low power
- Single-phase clock; optional on-chip crystal-controlled oscillator
- TTL compatible
- On-chip DMA
- Simple control of reset, run, and pause
- 8-bit parallel organization with bidirectional data bus
- Any combination of standard RAM and ROM
- Memory addressing up to 65,536 bytes
- Flexible programmed I/O mode
- Program interrupt mode
- Four I/O flag inputs directly tested by branch instructions
- Programmable output port
- 91 easy-to-use instructions
- 16 x 16 matrix of registers for use as multiple program counters, data pointers, or data registers

The RCA-CDP1802 is an LSI COS/MOS 8-bit register-oriented central-processing unit (CPU) designed for use as a general-purpose computing or control element in a wide range of stored-program systems or products.

The CDP1802 includes all of the circuits required for fetching, interpreting, and executing instructions which have been stored in standard types of memories. Extensive input/output (I/O) control features are also provided to facilitate system design.

The COSMAC architecture is designed with emphasis on the total microcomputer system as an integral entity so that systems having maximum flexibility and minimum cost can be realized. The COSMAC CPU also provides a synchronous interface to, memories and external controllers for I/O devices, and minimizes the cost of interface controllers. Further, the I/O interface is capable of supporting devices operating in polled, interrupt-driven, or direct memory-access modes.

The CDP1802D and CDP1802CD are functionally identical. They differ in that the CDP1802D has a recommended operating voltage range of 4-12 volts, and the CDP 1802CD, a recommended operating voltage range of 4-6 volts. These types are supplied in 40-lead dual-in-line ceramic packages (D suffix).

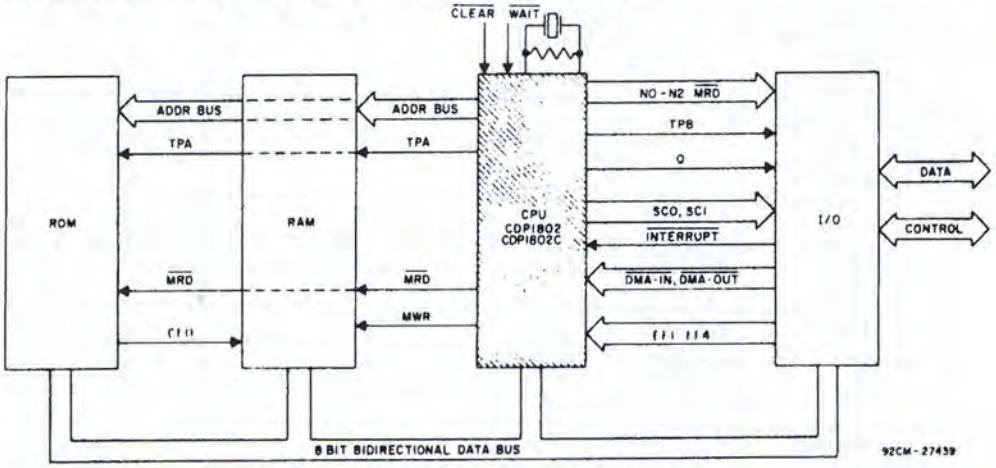


Fig. 1 — Typical CDP1802 microprocessor system.

Printed in USA/8-77

Supersedes preliminary data issued 2/76

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{CC}, V_{DD})
(All voltage values referenced to V_{SS} terminal)
$V_{CC} \leq V_{DD}$:
CDP1802D . . . . . −0.5 to +15 V
CDP1802CD . . . . . −0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −55 to +100°C . . . . . 500 mW
For T_A = +100 to +125°C . . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A) . . . . . −55 to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
				VALUES				+25			
	V_O (V)	V_{IN} (V)	V_{CC}, V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_L Max.	–	–	5	–	–	–	–	–	1	100	μA
	–	–	10	–	–	–	–	–	10	500	
CDP1802D	–	–	15	–	–	–	–	–	–	1000	
CDP1802CD	–	–	5	–	–	–	–	–	–	500	
Output Low Drive (Sink) Current, I_{OL} Min.	0.4	0,5	5	1.98	1.89	1.14	0.90	1.5	2.2	–	mA
(Except $\overline{XTAL}$)	0.5	0,10	10	3.70	3.53	2.13	1.68	2.8	5.2	–	
$\overline{XTAL}$ Output I_{OL} Min.	0.4	5	5	132	126	76	60	100	–	–	μA
Output High Drive (Source Current) I_{OH} Min.	4.6	0,5	5	−0.46	−0.44	−0.27	−0.21	−0.35	−0.51	–	mA
(Except $\overline{XTAL}$)	9.5	0,10	10	−1.12	−1.07	−0.65	−0.51	−0.85	−1.3	–	
$\overline{XTAL}$ Output I_{OH} Min.	4.6	0	5	-66	-63	-38	-30	−50	–	–	μA
Output Voltage Low-Level V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
Output Voltage High Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
Input Low Voltage V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	0.5,4.5	–	5,10	1				–	–	1	
	1,9	–	10	3				–	–	3	
Input High Voltage V_{IL} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	0.5,4.5	–	5,10	4				4	–	–	
	1,9	–	10	7				7	–	–	
Input Leakage Current I_{IN} Max.	Any Input	0,15	15	±1				–	–	±1	μA
3-State Output Leakage Current I_{OUT} Max.	0,15	0,15	15	±1	±1	±12	±12	–	$\pm 10^{-4}$	±1	μA

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C Unless Otherwise Specified

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	CONDITIONS		LIMITS AT 25°C		UNITS
	V_{CC}[1] (V)	V_{DD} (V)	CDP1802D	CDP1802CD	
Supply-Voltage Range	–	–	4 to 12	4 to 6	V
Input Voltage Range	–	–	V_{SS} to V_{CC}	V_{SS} to V_{CC}	V
Maximum Clock Input Rise or Fall Time, t_r or t_f	4–12	4–12	1	1	μs
Instruction Time[2] (See Fig. 8)	5	5	5	5	μs
	5	10	4	–	
	10	10	2.5	–	
Maximum DMA Transfer Rate	5	5	400	400	KBytes/sec
	5	10	500	–	
	10	10	800	–	
Maximum Clock Input Frequency, f_{CL}[3]	5	5	DC – 3.2	DC – 3.2	MHz
	5	10	DC – 4	–	
	10	10	DC – 6.4	–	

NOTES:
1: $V_{CC} \leq V_{DD}$; for CDP1802CD, $V_{DD} = V_{CC} = 5$ volts.
2. Equals 2 machine cycles – one Fetch and one Execute operation for all instructions except Long Branch and Long Skip, which require 3 machine cycles – one Fetch and two Execute operations.
3. Load Capacitance (C_L) = 50 pF.

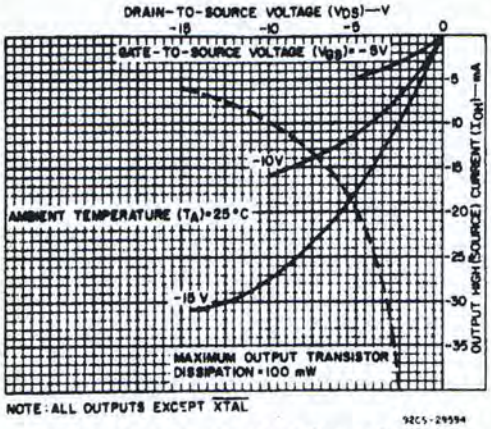


Fig. 2 – Typical output high (source) current characteristics.

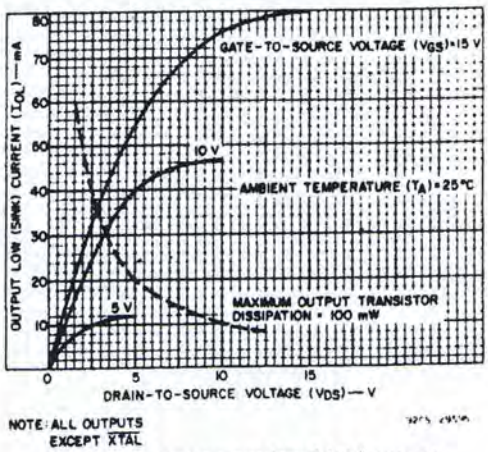


Fig. 3 – Typical output low (sink) current characteristics.

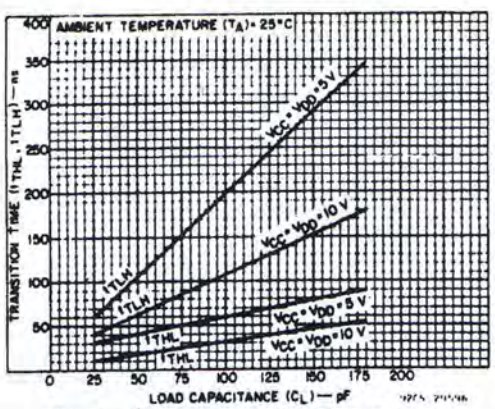


Fig. 4 – Typical transition time vs. load capacitance.

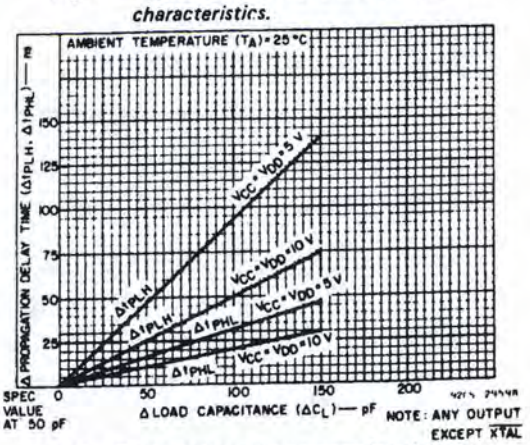


Fig. 5 – Typical change in propagation delay as a function of a change in load capacitance.

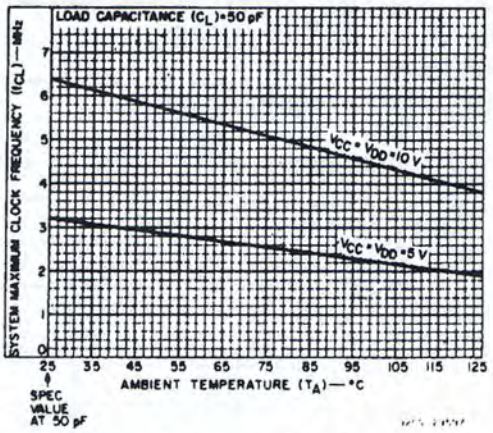


Fig. 6 – Typical maximum clock frequency as a function of temperature.

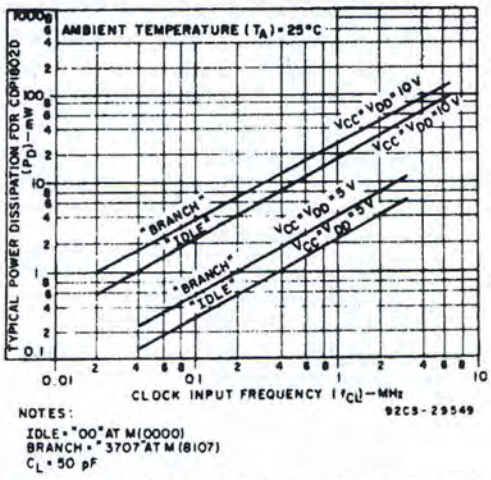


Fig. 7 – Typical power dissipation as a function of clock frequency for BRANCH instruction and IDLE instruction for CDP1802D.

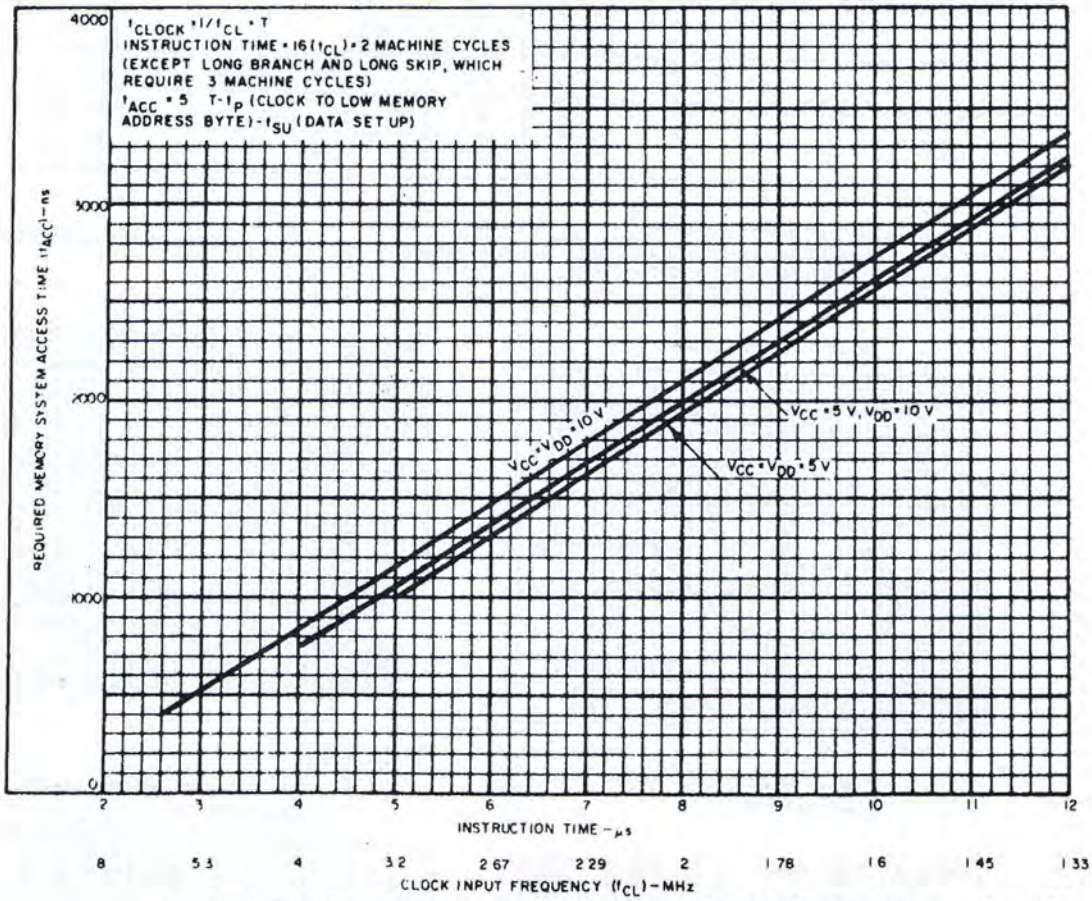


Fig. 8 – Required memory system address time as a function of instruction time. 92CL-29643

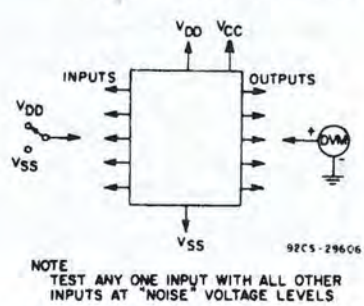


Fig. 9 – Noise immunity test circuit.

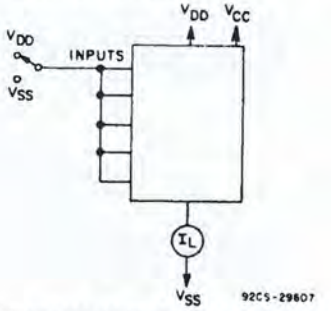


Fig. 10 – Quiescent-device leakage current test circuit.

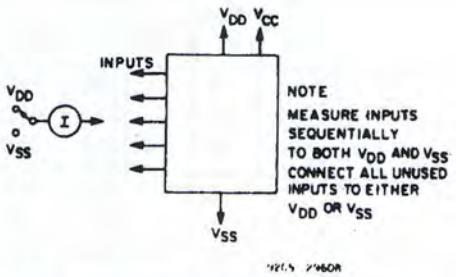


Fig. 11 – Input leakage current test circuit.

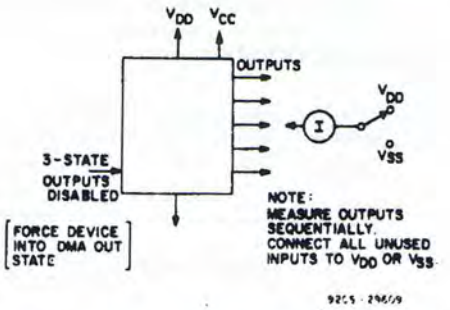
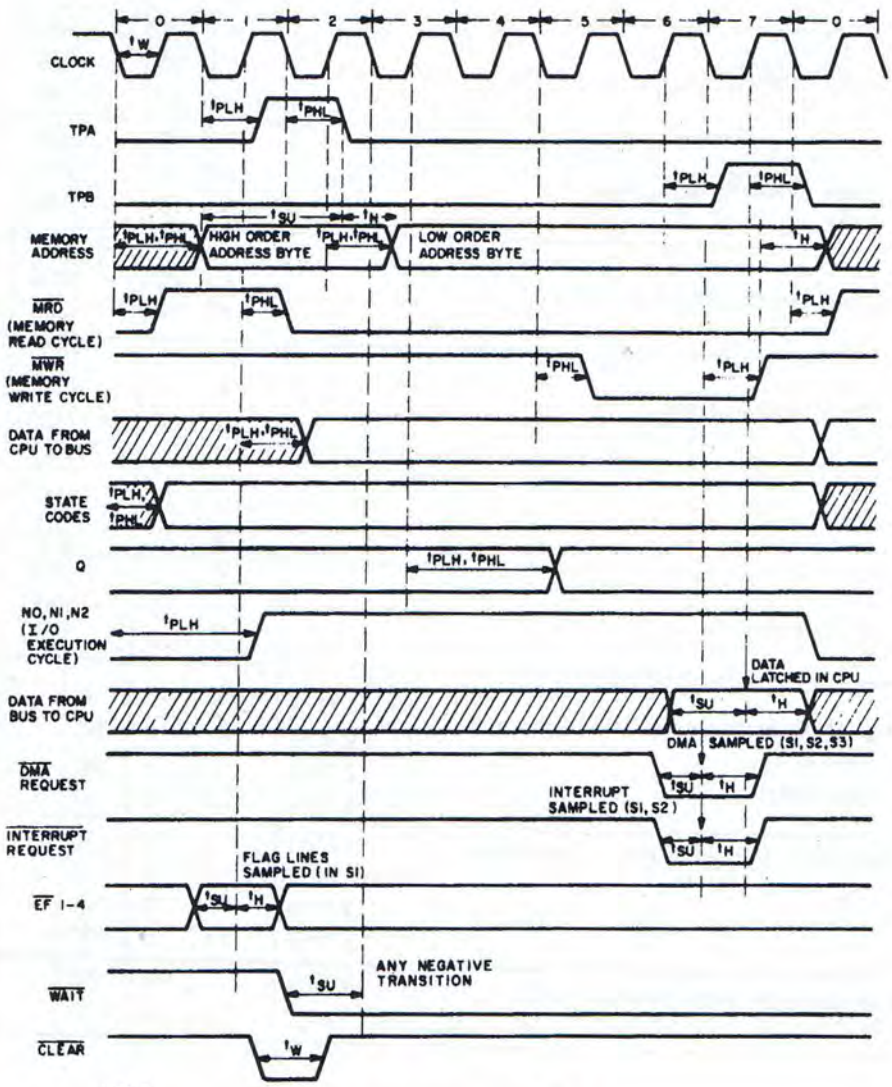


Fig. 12 – Three-state output leakage (data bus) test circuit.



NOTES:
1. THIS TIMING DIAGRAM IS USED TO SHOW SIGNAL RELATIONSHIPS ONLY AND DOES NOT REPRESENT ANY SPECIFIC MACHINE CYCLE
2. ALL MEASUREMENTS ARE REFERENCED TO 50% POINT OF THE WAVEFORMS
3. SHADED AREAS INDICATE "DON'T CARE" OR UNDEFINED STATE; MULTIPLE TRANSITIONS MAY OCCUR DURING THIS PERIOD

92CL-29599

Fig. 13 – Timing waveforms.

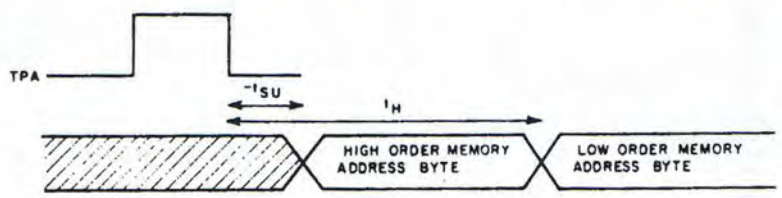
DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, C_L = 50 pF

CHARACTERISTIC	V_{CC} (V)	V_{DD} (V)	LIMITS Min.	Typ.	Max.	UNITS
Propagation Delay Time, t_{PLH}, t_{PHL}: Clock to TPA, TPB	5	5	–	300	450	ns
	5	10	–	250	400	
	10	10	–	150	250	
Clock-to-Memory High-Address Byte	5	5	–	800	1200	ns
	5	10	–	600	900	
	10	10	–	400	600	
Clock-to-Memory Low-Address Byte	5	5	–	300	550	ns
	5	10	–	250	500	
	10	10	–	150	350	
Clock to $\overline{MRD}$, t_{PLH}	5	5	–	300	450	ns
	5	10	–	250	400	
	10	10	–	150	300	
Clock to $\overline{MRD}$, t_{PHL}	5	5	–	300	450	ns
	5	10	–	250	400	
	10	10	–	150	300	
Clock to $\overline{MWR}$, t_{PLH}, t_{PHL}	5	5	–	300	450	ns
	5	10	–	200	300	
	10	10	–	150	250	
Clock to CPU DATA to BUS	5	5	–	350	600	ns
	5	10	–	300	500	
	10	10	–	200	400	
Clock to State Code	5	5	–	400	600	ns
	5	10	–	200	400	
	10	10	–	150	300	
Clock to Q	5	5	–	300	700	ns
	5	10		150	400	
	10	10	–	100	300	
Clock to N(0-2), t_{PLH}	5	5	–	450	800	ns
	5	10	–	300	600	
	10	10	–	200	400	
High-Order Memory-Address Byte Set Up, t_{SU} (See Note) f = 4 MHz	5	10	0	–	–	ns
f = 6.4 MHz	10	10	–50	–	–	
f = 2 MHz	5	5	50	–	–	
f = 5 MHz	10	10	30	–	–	
High-Order Memory-Address Byte Hold t_H f = 4 MHz	5	10	120	–	–	ns
f = 6.4 MHz	10	10	75	–	–	
f = 2 MHz	5	5	200	–	–	
f = 5 MHz	10	10	100	–	–	
Low-Order Memory-Address Hold f = 4 MHz	5	10	100	–	–	ns
f = 6.4 MHz	10	10	50	–	–	

DYNAMIC ELECTRICAL CHARACTERISTICS (cont'd)

CHARACTERISTIC	V_{CC} (V)	V_{DD} (V)	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
Set-Up and Hold Times, t_{SU}, t_H Data Set Up	5	5	0	−50	–	ns
	5	10	25	0	–	
	10	10	50	0	–	
Data Hold	5	5	300	150	–	
	5	10	200	100	–	
	10	10	150	75	–	
$\overline{DMA}$ Set Up	5	5	100	0	–	ns
	5	10	125	25	–	
	10	10	150	50	–	
$\overline{DMA}$ Hold	5	5	250	150	–	
	5	10	200	100	–	
	10	10	150	75	–	
Interrupt Set Up	5	5	100	0	–	ns
	5	10	125	25	–	
	10	10	150	50	–	
Interrupt Hold	5	5	250	150	–	
	5	10	200	100	–	
	10	10	150	75	–	
$\overline{WAIT}$ Set Up	5	5	100	0	–	ns
	5	10	125	25		
	10	10	150	50		
$\overline{EF1\text{-}4}$ Set Up	5	5	100	0	–	ns
	5	10	125	25	–	
	10	10	150	50	–	
$\overline{EF1\text{-}4}$ Hold	5	5	250	150	–	
	5	10	200	100	–	
	10	10	150	75	–	
Pulse Width, t_{WL} $\overline{CLEAR}$ Pulse Width	5	5	600	300	–	ns
	5	10	400	200	–	
	10	10	300	150	–	
$\overline{CLOCK}$ Pulse Width, t_{WL}	5	5	160	–	–	ns
	5	10	125	–	–	
	10	10	80	–	–	
Typical Total Power Dissipation f = 2 MHz Idle "00" at M(0000), C_L = 50 pF f = 4 MHz	5	5		4	–	mW
	10	10		60	–	
Effective Input Capacitance, C_{IN} Any Input			–	5	–	pF
Effective 3-State Terminal Capacitance DATA BUS			–	7.5	–	pF

NOTE: Negative set-up indicates the addresses can change after the falling edge of TPA, as shown below:



92CS-29644

ARCHITECTURE

The COSMAC block diagram is shown in Fig. 14. The principal feature of this system is a register array (R) consisting of sixteen 16-bit scratchpad registers. Individual registers in the array (R) are designated (selected) by a 4-bit binary code from one of the 4-bit registers labeled N, P, and X. The contents of any register can be directed to any one of the following three paths:

1. the external memory (multiplexed, higher-order byte first, on to 8 memory address lines);
2. the D register (either of the two bytes can be gated to D);
3. the increment/decrement circuit where it is increased or decreased by one and stored back in the selected 16-bit register.

The three paths, depending on the nature of the instruction, may operate independently or in various combinations in the same machine cycle.

With two exceptions, COSMAC instructions consist of two 8-clock-pulse machine cycles. The first cycle is the fetch cycle, and the second—and third, if necessary—are execute cycles. During the fetch cycle the four bits in the P designator select one of the 16 registers R(P) as the current program counter. The selected register R(P) contains the address of the memory location from which the instruction is to be fetched. When the instruction is read out from the memory, the higher-order 4 bits of the instruction byte are loaded into the I register and the lower-order 4 bits into the N register. The content of the program counter is automatically incremented by one so that R(P) is now "pointing" to the next byte in the memory.

The X designator selects one of the 16 registers R(X) to "point" to the memory for an operand (or data) in certain ALU or I/O operations.

The N designator can perform the following five functions depending on the type of instruction fetched:

1. designate one of the 16 registers in R to be acted upon during register operations;
2. indicate to the I/O devices a command code or device-selection code for peripherals;
3. indicate the specific operation to be executed during the ALU instructions, types of tests to be performed during the Branch instructions, or the specific operation required in a class of miscellaneous instructions (70-73 and 78-7B);
4. indicate the value to be loaded into P to designate a new register to be used as the program counter R(P);

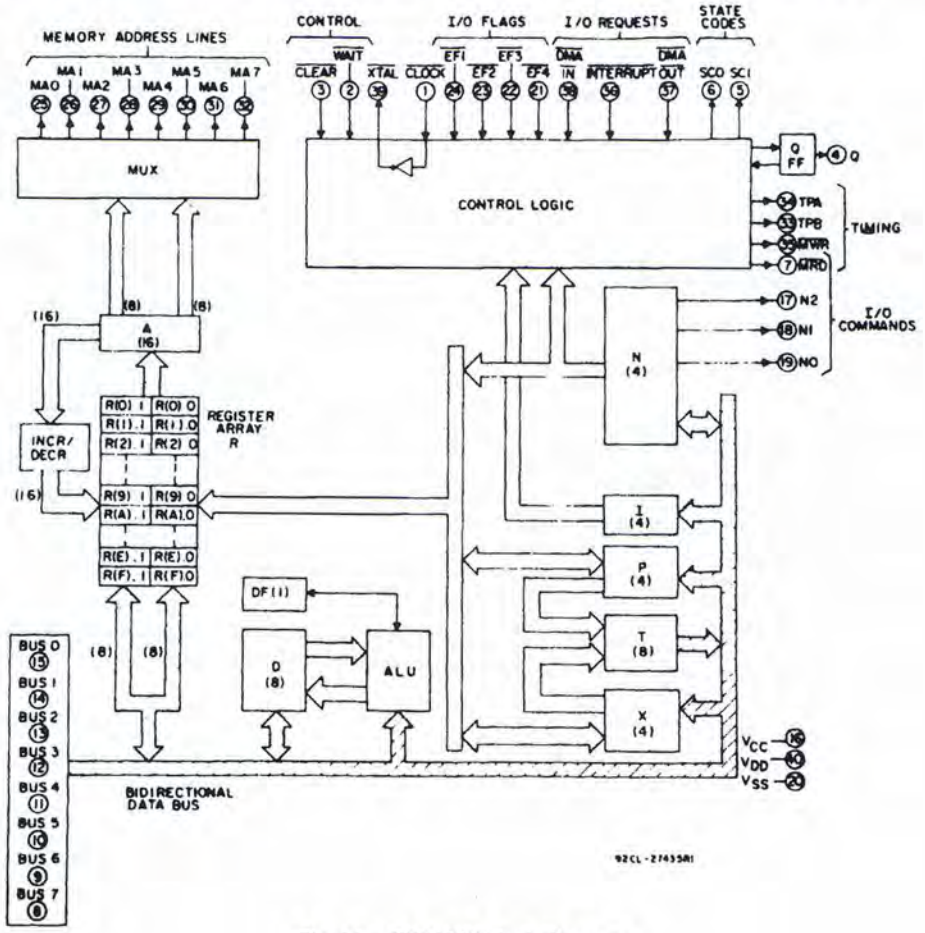


Fig. 14 – CDP1802 block diagram.

5. indicate the value to be loaded into X to designate a new register to be used as data pointer R(X).

The registers in R can be assigned by a programmer in three different ways: as program counters, as data pointers, or as scratchpad locations (data registers) to hold two bytes of data.

Program Counters

Any register can be the main program counter; the address of the selected register is held in the P designator. Other registers in R can be used as subroutine program counters. By a single instruction the contents of the P register can be changed to effect a "call" to a subroutine. When interrupts are being serviced, register R(1) is used as the program counter for the user's interrupt servicing routine. After reset, and during a DMA operation, R (0) is used as the program counter. At all other times the register designated as program counter is at the discretion of the user.

Data Pointers

The registers in R may be used as data pointers to indicate a location in memory. The register designated by X (i.e., R(X)) points to memory for the following instructions (see Table I):

1. ALU operations F1-F5, F7, 74, 75, 77;
2. output instructions 61 through 67;
3. input instructions 69 through 6F;
4. certain miscellaneous instructions—70-73, 78.60, FO.

The register designated by N (i.e., R(N)) points to memory for the "load D from memory" instructions 0N and 4N and the "Store D" instruction 5N. The register designated by P (i.e., the program counter) is used as the data pointer for ALU instructions F8-FD, FF, 7C, 7D, 7F. During these instruction executions, the operation is referred to as "data immediate".

Another important use of R as a data pointer supports the built-in Direct-Memory-Access (DMA) function. When a DMA-In or DMA-Out request is received, one machine cycle is "stolen". This operation occurs at the end of the execute machine cycle in the current instruction. Register R(0) is always used as the data pointer during the DMA operation. The data is read from (DMA-Out) or written into (DMA-In) the memory location pointed to by the R(0) register. At the end of the transfer, R(0) is incremented by one so that the processor is ready to act upon the next DMA byte transfer request. This feature in the COSMAC architecture saves a substantial amount of logic when fast exchanges of blocks of data are required, such as with magnetic discs or during CRT-display-refresh cycles.

A program load facility, using the DMA-In channel, is provided to enable users to load programs into the memory. This facility provides a simple, one-step means for initially entering programs into the microprocessor system and eliminates the requirement for specialized "bootstrap" ROM's.

Data Registers

When registers in R are used to store bytes of data, four instructions are provided which allow D to receive from or write into either the higher-order- or lower-order-byte portions of the register designated by N. By this mechanism (together with loading by data immediate) program pointer and data pointer designations are initialized. Also, this technique allows scratchpad registers in R to be used to hold general data. By employing increment or decrement instructions, such registers may be used as loop counters.

The Q Flip Flop

An internal flip flop, Q, can be set or reset by instruction and can be sensed by conditional branch instructions. The output of Q is also available as a microprocessor output.

Interrupt Servicing

Register R(1) is always used as the program counter whenever interrupt servicing is initiated. When an interrupt request comes in and the interrupt is allowed by the program (again, nothing takes place until the completion of the current instruction) the contents of the X and P registers are stored in the temporary register T, and X and P are set to new values; hex digit 2 in X and hex digit 1 in P. Interrupt enable is automatically deactivated to inhibit further interruptions. The user's interrupt routine is now in control; the contents of T may be saved by means of a single instruction (78) in the memory location pointed to by R (X). At the conclusion of the interrupt, the user's routine may restore the pre-interrupted value of X and P with a single instruction (70 or 71). The interrupt-enable flip-flop can be activated to permit further interrupts or can be disabled to prevent them.

COSMAC Register Summary

D	8 Bits	Data Register (Accumulator)	N	4 Bits	Holds Low-Order Instr. Digit
DF	1 Bit	Data Flag (ALU Carry)	I	4 Bits	Holds High-Order Instr. Digit
R	16 Bits	1 of 16 Scratchpad Registers	T	8 Bits	Holds old X, P after Interrupt (X is high byte)
P	4 Bits	Designates which register is Program Counter	IE	1 Bit	Interrupt Enable
X	4 Bits	Designates which register is Data Pointer	Q	1 Bit	Output Flip Flop

INSTRUCTION SET

The COSMAC instruction summary is given in Table I. Hexadecimal notation is used to refer to the 4-bit binary codes.

In all registers bits are numbered from the least significant bit (LSB) to the most significant bit (MSB) starting with 0.

R(W): Register designated by W, where W=N or X, or P

R(W).0: Lower-order byte of R(W)
R(W).1: Higher-order byte of R(W)
N0 = Least significant Bit of N Register

Operation Notation
M(R(N)) → D; R(N) + 1

This notation means: The memory byte pointed to by R(N) is loaded into D, and R(N) is incremented by 1.

TABLE I – INSTRUCTION SUMMARY

(For Notes, see page 13)

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
MEMORY REFERENCE			
LOAD VIA N	LDN	0N	M(R(N))→D; FOR N NOT 0
LOAD ADVANCE	LDA	4N	M(R(N))→D; R(N) +1
LOAD VIA X	LDX	F0	M(R(X))→D
LOAD VIA X AND ADVANCE	LDXA	72	M(R(X))→D; R(X) +1
LOAD IMMEDIATE	LDI	F8	M(R(P))→D; R(P) +1
STORE VIA N	STR	5N	D→M(R(N))
STORE VIA X AND DECREMENT	STXD	73	D→M(R(X)); R(X) –1
REGISTER OPERATIONS			
INCREMENT REG N	INC	1N	R(N) +1
DECREMENT REG N	DEC	2N	R(N) –1
INCREMENT REG X	IRX	60	R(X) +1
GET LOW REG N	GLO	8N	R(N).0→D
PUT LOW REG N	PLO	AN	D→R(N).0
GET HIGH REG N	GHI	9N	R(N).1→D
PUT HIGH REG N	PHI	BN	D→R(N).1
LOGIC OPERATIONS◆◆			
OR	OR	F1	M(R(X)) OR D→D
OR IMMEDIATE	ORI	F9	M(R(P)) OR D→D; R(P) +1
EXCLUSIVE OR	XOR	F3	M(R(X)) XOR D→D
EXCLUSIVE OR IMMEDIATE	XRI	FB	M(R(P)) XOR D→D; R(P) +1
AND	AND	F2	M(R(X)) AND D→D
AND IMMEDIATE	ANI	FA	M(R(P)) AND D→D; R(P) +1
SHIFT RIGHT	SHR	F6	SHIFT D RIGHT, LSB(D)→DF, 0→MSB(D)
SHIFT RIGHT WITH CARRY	SHRC	76◆	SHIFT D RIGHT, LSB(D)→DF, DF→MSB(D)
RING SHIFT RIGHT	RSHR		
SHIFT LEFT	SHL	FE	SHIFT D LEFT, MSB(D)→DF, 0→LSB(D)
SHIFT LEFT WITH CARRY	SHLC	7E◆	SHIFT D LEFT, MSB(D)→DF, DF→LSB(D)
RING SHIFT LEFT	RSHL		

◆NOTE THIS INSTRUCTION IS ASSOCIATED WITH MORE THAN ONE MNEMONIC. EACH MNEMONIC IS INDIVIDUALLY LISTED.

◆◆NOTE THE ARITHMETIC OPERATIONS AND THE SHIFT INSTRUCTIONS ARE THE ONLY INSTRUCTIONS THAT CAN ALTER THE DF.
AFTER AN ADD INSTRUCTION:
DF = 1 DENOTES A CARRY HAS OCCURRED
DF = 0 DENOTES A CARRY HAS NOT OCCURRED
AFTER A SUBTRACT INSTRUCTION:
DF = 1 DENOTES NO BORROW. D IS A TRUE POSITIVE NUMBER
DF = 0 DENOTES A BORROW. D IS TWO'S COMPLEMENT
THE SYNTAX " (NOT DF)" DENOTES THE SUBTRACTION OF THE BORROW

TABLE I – INSTRUCTION SUMMARY (CONT'D)

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
ARITHMETIC OPERATIONS◆◆			
ADD	ADD	F4	M(R(X)) +D→DF, D
ADD IMMEDIATE	ADI	FC	M(R(P)) +D→DF, D; R(P) +1
ADD WITH CARRY	ADC	74	M(R(X)) +D +DF→DF, D
ADD WITH CARRY, IMMEDIATE	ADCI	7C	M(R(P)) +D +DF→DF, D R(P) +1
SUBTRACT D	SD	F5	M(R(X))–D→DF, D
SUBTRACT D IMMEDIATE	SDI	FD	M(R(P))–D→DF, D; R(P) +1
SUBTRACT D WITH BORROW	SDB	75	M(R(X))–D–(NOT DF)→DF, D
SUBTRACT D WITH BORROW, IMMEDIATE	SDBI	7D	M(R(P))–D–(NOT DF)→DF, D, R(P) +1
SUBTRACT MEMORY	SM	F7	D–M(R(X))→DF, D
SUBTRACT MEMORY IMMEDIATE	SMI	FF	D–M(R(P))→DF, D; R(P) +1
SUBTRACT MEMORY WITH BORROW	SMB	77	D–M(R(X))–(NOT DF)→DF, D
SUBTRACT MEMORY WITH BORROW, IMMEDIATE	SMBI	7F	D–M(R(P))–(NOT DF)→DF, D R(P) +1
BRANCH INSTRUCTIONS–SHORT BRANCH			
SHORT BRANCH	BR	30	M(R(P))→R(P).0
NO SHORT BRANCH (SEE SKP)	NBR	38◆	R(P) +1
SHORT BRANCH IF D=0	BZ	32	IF D=0, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF D NOT 0	BNZ	3A	IF D NOT 0, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF DF=1	BDF	33◆	IF DF=1, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF POS OR ZERO	BPZ		
SHORT BRANCH IF EQUAL OR GREATER	BGE		
SHORT BRANCH IF DF=0	BNF	3B◆	IF DF=0, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF MINUS	BM		
SHORT BRANCH IF LESS	BL		
SHORT BRANCH IF Q=1	BQ	31	IF Q=1, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF Q=0	BNQ	39	IF Q=0, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF EF1=1 (1 = V_{SS})	B1	34	IF EF1=1, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF EF1=0 (0 = V_{CC})	BN1	3C	IF EF1=0, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF EF2=1 (1 = V_{SS})	B2	35	IF EF2=1, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF EF2=0 (0 = V_{CC})	BN2	3D	IF EF2=0, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF EF3=1 (1 = V_{SS})	B3	36	IF EF3=1, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF EF3=0 (0 = V_{CC})	BN3	3E	IF EF3=0, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF EF4=1 (1 = V_{SS})	B4	37	IF EF4=1, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF EF4=0 (0 = V_{CC})	BN4	3F	IF EF4=0, M(R(P))→R(P).0 ELSE R(P) +1

◆NOTE: THIS INSTRUCTION IS ASSOCIATED WITH MORE THAN ONE MNEMONIC. EACH MNEMONIC IS INDIVIDUALLY LISTED.

◆◆NOTE: THE ARITHMETIC OPERATIONS AND THE SHIFT INSTRUCTIONS ARE THE ONLY INSTRUCTIONS THAT CAN ALTER THE DF.
AFTER AN ADD INSTRUCTION:
DF = 1 DENOTES A CARRY HAS OCCURRED
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DF = 1 DENOTES NO BORROW. D IS A TRUE POSITIVE NUMBER
DF = 0 DENOTES A BORROW. D IS TWO'S COMPLEMENT
THE SYNTAX "–(NOT DF)" DENOTES THE SUBTRACTION OF THE BORROW

TABLE I – INSTRUCTION SUMMARY (CONT'D)

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
BRANCH INSTRUCTIONS–LONG BRANCH			
LONG BRANCH	LBR	C0	M(R(P))→R(P).1 M(R(P) +1)→R(P).0
NO LONG BRANCH (SEE LSKP)	NLBR	C8♦	R(P) +2
LONG BRANCH IF D=0	LBZ	C2	IF D=0, M(R(P))→R(P).1 M(R(P) +1)→R(P).0 ELSE R(P) +2
LONG BRANCH IF D NOT 0	LBNZ	CA	IF D NOT 0, M(R(P))→R(P).1 M(R(P) +1)→R(P).0 ELSE R(P) +2
LONG BRANCH IF DF=1	LBDF	C3	IF DF=1, M(R(P))→R(P).1 M(R(P) +1)→R(P).0 ELSE R(P) +2
LONG BRANCH IF DF=0	LBNF	C8	IF DF=0, M(R(P))→R(P).1 M(R(P) +1)→R(P).0 ELSE R(P) +2
LONG BRANCH IF Q=1	LBQ	C1	IF Q=1, M(R(P))→R(P).1 M(R(P) +1)→R(P).0 ELSE R(P) +2
LONG BRANCH IF Q=0	LBNQ	C9	IF Q=0, M(R(P))→R(P).1 M(R(P) +1)→R(P).0 ELSE R(P) +2
SKIP INSTRUCTIONS			
SHORT SKIP (SEE NBR)	SKP	38♦	R(P) +1
LONG SKIP (SEE NLBR)	LSKP	C8♦	R(P) +2
LONG SKIP IF D=0	LSZ	CE	IF D=0, R(P) +2 ELSE CONTINUE
LONG SKIP IF D NOT 0	LSNZ	C6	IF D NOT 0, R(P) +2 ELSE CONTINUE
LONG SKIP IF DF=1	LSDF	CF	IF DF=1, R(P) +2 ELSE CONTINUE
LONG SKIP IF DF=0	LSNF	C7	IF DF=0, R(P) +2 ELSE CONTINUE
LONG SKIP IF Q=1	LSQ	CD	IF Q=1, R(P) +2 ELSE CONTINUE
LONG SKIP IF Q=0	LSNQ	C5	IF Q=0, R(P) +2 ELSE CONTINUE
LONG SKIP IF IE=1	LSIE	CC	IF IE=1, R(P) +2 ELSE CONTINUE
CONTROL INSTRUCTIONS			
IDLE	IDL	00#	WAIT FOR DMA OR INTERRUPT; M(R(0))→BUS
NO OPERATION	NOP	C4	CONTINUE
SET P	SEP	DN	N→P
SET X	SEX	EN	N→X
SET Q	SEQ	7B	1→Q
RESET Q	REQ	7A	0→Q
SAVE	SAV	78	T→M(R(X))
PUSH X,P TO STACK	MARK	79	(X,P)→T; (X,P)→M(R(2)) THEN P→X; R(2)–1
RETURN	RET	70	M(R(X))→(X,P); R(X) +1 1→IE
DISABLE	DIS	71	M(R(X))→(X,P); R(X) +1 0→IE

#An idle instruction initiates a repeating S1 cycle. The processor will continue to idle until an I/O request ($\overline{\text{INTERRUPT}}$, $\overline{\text{DMA-IN}}$, or $\overline{\text{DMA-OUT}}$) is activated. When the request is acknowledged, the IDLE cycle is terminated and the I/O request is serviced, and then normal operation is resumed.

♦NOTE: THIS INSTRUCTION IS ASSOCIATED WITH MORE THAN ONE MNEMONIC. EACH MNEMONIC IS INDIVIDUALLY LISTED.

TABLE I – INSTRUCTION SUMMARY (CONT'D)

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
INPUT–OUTPUT BYTE TRANSFER			
OUTPUT 1	OUT 1	61	M(R(X))→BUS; R(X) +1; N LINES = 1
OUTPUT 2	OUT 2	62	M(R(X))→BUS; R(X) +1; N LINES = 2
OUTPUT 3	OUT 3	63	M(R(X))→BUS; R(X) +1; N LINES = 3
OUTPUT 4	OUT 4	64	M(R(X))→BUS; R(X) +1; N LINES = 4
OUTPUT 5	OUT 5	65	M(R(X))→BUS; R(X) +1; N LINES = 5
OUTPUT 6	OUT 6	66	M(R(X))→BUS; R(X) +1; N LINES = 6
OUTPUT 7	OUT 7	67	M(R(X))→BUS; R(X) +1; N LINES = 7
INPUT 1	INP 1	69	BUS→M(R(X)); BUS→D; N LINES = 1
INPUT 2	INP 2	6A	BUS→M(R(X)); BUS→D; N LINES = 2
INPUT 3	INP 3	6B	BUS→M(R(X)); BUS→D; N LINES = 3
INPUT 4	INP 4	6C	BUS→M(R(X)); BUS→D; N LINES = 4
INPUT 5	INP 5	6D	BUS→M(R(X)); BUS→D; N LINES = 5
INPUT 6	INP 6	6E	BUS→M(R(X)); BUS→D; N LINES = 6
INPUT 7	INP 7	6F	BUS→M(R(X)); BUS→D; N LINES = 7

1. Long-Branch, Long-Skip and No Op instructions are the only instructions that require three cycles to complete (1 fetch + 2 execute).

   Long-Branch instructions are three bytes long. The first byte specifies the condition to be tested; and the second and third byte, the branching address.

   The long-branch instructions can:
   a) Branch unconditionally
   b) Test for D=0 or D≠0
   c) Test for DF=0 or DF=1
   d) Test for Q=0 or Q=1
   e) effect an unconditional no branch

   If the tested condition is met, then branching takes place; the branching address bytes are loaded in the high-and-low-order bytes of the current program counter, respectively. This operation effects a branch to any memory location.

   If the tested condition is not met, the branching address bytes are skipped over, and the next instruction in sequence is fetched and executed. This operation is taken for the case of unconditional no branch (NLBR).

2. The short-branch instructions are two bytes long. The first byte specifies the condition to be tested, and the second specifies the branching address.

   The short-branch instructions can:
   a) Branch unconditionally
   b) Test for D=0 or D≠0
   c) Test for DF=0 or DF=1
   d) Test for Q=0 or Q=1
   e) Test the status (1 or 0) of the four EF flags
   f) Effect an unconditional no branch

   If the tested condition is met, then branching takes place; the branching address byte is loaded into the low-order byte position of the current program counter. This effects a branch with the current 256-byte page of the memory, i.e., the page which holds the branching address. If the tested condition is not met, the branching address byte is skipped over, and the next instruction in sequence is fetched and executed. This same action is taken in the case of unconditional no branch (NBR)

3. The skip instructions are one byte long. There is one Unconditional Short-Skip (SKP) and eight Long-Skip instructions.

   The Unconditional Short-Skip instruction takes 2 cycles to complete (1 fetch + 1 execute). Its action is to skip over the byte following it. Then the next instruction in sequence is fetched and executed. This SKP instruction is identical to the unconditional no-branch instruction (NBR) except that the skipped-over byte is not considered part of the program.

   The Long-Skip instructions take three cycles to complete (1 fetch + 2 execute).

   They can:
   a) Skip unconditionally
   b) Test for D=0 or D≠0
   c) Test for DF=0 or DF=1
   d) Test for Q=0 or Q=1
   e) Test for IE=1

   If the tested condition is met, then Long Skip takes place; the current program counter is incremented twice. Thus two bytes are skipped over and the next instruction in sequence is fetched and executed. If the tested condition is not met, then no action is taken. Execution is continued by fetching the next instruction in sequence.

SIGNAL DESCRIPTIONS

BUS 0 to BUS 7 (Data Bus)

8-bit directional DATA BUS lines. These lines are used for transferring data between the memory, the microprocessor, and I/O devices.

N0 to N2 (I/O Lines)

Activated by an I/O instruction to signal the I/O control logic of a data transfer between memory and I/O interface. These lines can be used to issue command codes or device selection codes to the I/O devices (independently or combined with the memory byte on the data bus when an I/O instruction is being executed). The N bits are low at all times except when an I/O instruction is being executed. During this time their state is the same as the corresponding bits in the N register.

The direction of data flow is defined in the I/O instruction by bit N3 (internally) and is indicated by the level of the $\overline{MRD}$ signal.

$\overline{MRD} = V_{CC}$: Data from I/O to CPU and Memory

$\overline{MRD} = V_{SS}$: Data from Memory to I/O

$\overline{EF1}$ to $\overline{EF4}$ (4 Flags)

These inputs enable the I/O controllers to transfer status information to the processor. The levels can be tested by the conditional branch instructions. They can be used in conjunction with the INTERRUPT request line to establish interrupt priorities. These flags can also be used by I/O devices to "call the attention" of the processor, in which case the program must routinely test the status of these flag(s). The flag(s) are sampled at the beginning of every S1 cycle.

$\overline{INTERRUPT}$, $\overline{DMA\text{-}IN}$, $\overline{DMA\text{-}OUT}$ (3 I/O Requests)

These inputs are sampled by the CDP1802 during the interval between the leading edge of TPB and the leading edge of TPA.

Interrupt Action: X and P are stored in T after executing current instruction; designator X is set to 2; designator P is set to 1; interrupt enable is reset to 0 (inhibit); and instruction execution is resumed. The interrupt action requires one machine cycle (S3).

DMA Action: Finish executing current instruction; R(0) points to memory area for data transfer; data is loaded into or read out of memory; and increment R(0).

Note: In the event of concurrent DMA and INTERRUPT requests, DMA-IN has priority followed by DMA-OUT and then INTERRUPT.

SC0, SC1, (2 State Code Lines)

These outputs indicate that the CPU is: 1 fetching an instruction, or 2) executing an instruction, or 3) processing a DMA request, or 4) acknowledging an interrupt request. The levels of state code are tabulated below. All states are valid at TPA. $H = V_{CC}$, $L = V_{SS}$.

State Type	State Code Lines	
	SC1	SC0
S0 (Fetch)	L	L
S1 (Execute)	L	H
S2 (DMA)	H	L
S3 (Interrupt)	H	H

TPA, TPB (2 Timing Pulses)

Positive pulses that occur once in each machine cycle (TPB follows TPA). They are used by I/O controllers to interpret codes and to time interaction with the data bus. The trailing edge of TPA is used by the memory system to latch the higher-order byte of the 16-bit memory address. TPA is suppressed in IDLE when the CPU is in the load mode.

MA0 to MA7 (8 Memory Address Lines)

The higher-order byte of a 16-bit COSMAC memory address appears on the memory address lines MA0-7 first. Those bits required by the memory system can be strobed into external address latches by timing pulse TPA. The low-order byte of the 16-bit address appears on the address lines after the termination of TPA. Latching of all 8 higher-order address bits would permit a memory system of 64K bytes.

$\overline{MWR}$ (Write Pulse)

A negative pulse appearing in a memory-write cycle, after the address lines have stabilized.

$\overline{MRD}$ (Read Level)

A low level on $\overline{MRD}$ indicates a memory read cycle. It can be used to control three-state outputs from the addressed memory which may have a common data input and output bus. If a memory does not have a three-state high-impedance output, $\overline{MRD}$ is useful for driving memory/bus separator gates. It is also used to indicate the direction of data transfer during an I/O instruction. For additional information see Table I.

Q

Single bit output from the CPU which can be set or reset under program control. During SEQ or REQ instruction execution, Q is set or reset between the trailing edge of TPA and the leading edge of TPB.

CLOCK

Input for externally generated single-phase clock. A typical clock frequency is 6.4 MHz at $V_{CC} = V_{DD} = 10$ volts. The clock is counted down internally to 8 clock pulses per machine cycle.

$\overline{XTAL}$

Connection to be used with clock input terminal, for an external crystal, if the on-chip oscillator is utilized. The crystal is connected between terminals 1 and 39 (CLOCK and $\overline{XTAL}$) in parallel with a resistance (10 megohms typ.). Frequency trimming capacitors may be required at terminals 1 and 39. For additional information see ICAN-6565.

$\overline{WAIT}$, $\overline{CLEAR}$ (2 Control Lines)

Provide four control modes as listed in the following truth table:

$\overline{CLEAR}$	$\overline{WAIT}$	MODE
L	L	Load
L	H	Reset
H	L	Pause
H	H	Run

The function of the modes are defined as follows:

Load

Holds the CPU in the IDLE execution state and allows an I/O device to load the memory without the need for a "bootstrap" loader. It modifies the IDLE condition so that DMA-IN operation does not force execution of the next instruction.

Reset

Registers I, N, Q are reset, IE is set and 0's (V_{SS}) are placed on the data bus. TPA and TPB are suppressed while reset is held and the CPU is placed in S1. The first machine cycle after termination of reset is an initialization cycle which requires 9 clock pulses. During this cycle the CPU remains in S1 and registers X, P, and R(0) are reset. Interrupt and DMA servicing are suppressed during the initialization cycle. The next cycle is an S0, S1, or an S2 but never an S3. With the use of a 71 instruction followed by 00 at memory locations 0000 and 0001, this feature may be used to reset IE, so as to preclude interrupts until ready for them. Power-up reset can be realized by connecting a buffered RC network to $\overline{CLEAR}$. For additional information see ICAN-6581.

Pause

Stops the internal CPU timing generator on the first negative high-to-low transition of the input clock. The oscillator continues to operate, but subsequent clock transitions are ignored.

Run

May be initiated from the Pause or Reset mode functions. If initiated from Pause, the CPU resumes operation on the first negative high-to-low transition of the input clock. When initiated from the Reset operation, the first machine cycle following Reset is always the initialization cycle. The initialization cycle is then followed by a DMA (S2) cycle or fetch (S0) from location 0000 in memory.

V_{DD}, V_{SS}, V_{CC} (Power Levels)

The internal voltage supply V_{DD} is isolated from the Input/Output voltage supply V_{CC} so that the processor may operate at maximum speed while interfacing with various external circuit technologies, including T^2L at 5 volts. V_{CC} must be less than or equal to V_{DD}. All outputs swing from V_{SS} to V_{CC}. The recommended input voltage swing is V_{SS} to V_{CC}.

RUN-MODE STATE TRANSITIONS

The CDP1802 and CDP1802C CPU state transitions when in the RUN mode are shown in Fig. 15. Each machine cycle requires the same period of time 8 clock pulses except the initialization cycle, which requires 9 clock pulses. The execution of an instruction requires either two or three machine cycles, S0 followed by a single S1 cycle or two S1 cycles. S2 is the response to a DMA request and S3 is the interrupt response. Table II shows the conditions on Data Bus and Memory-Address lines during all machine states.

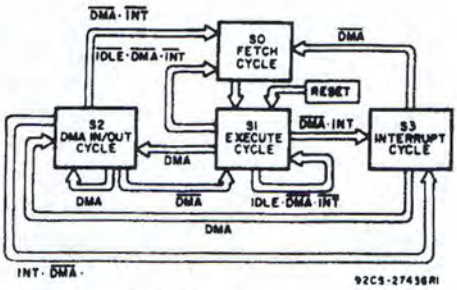
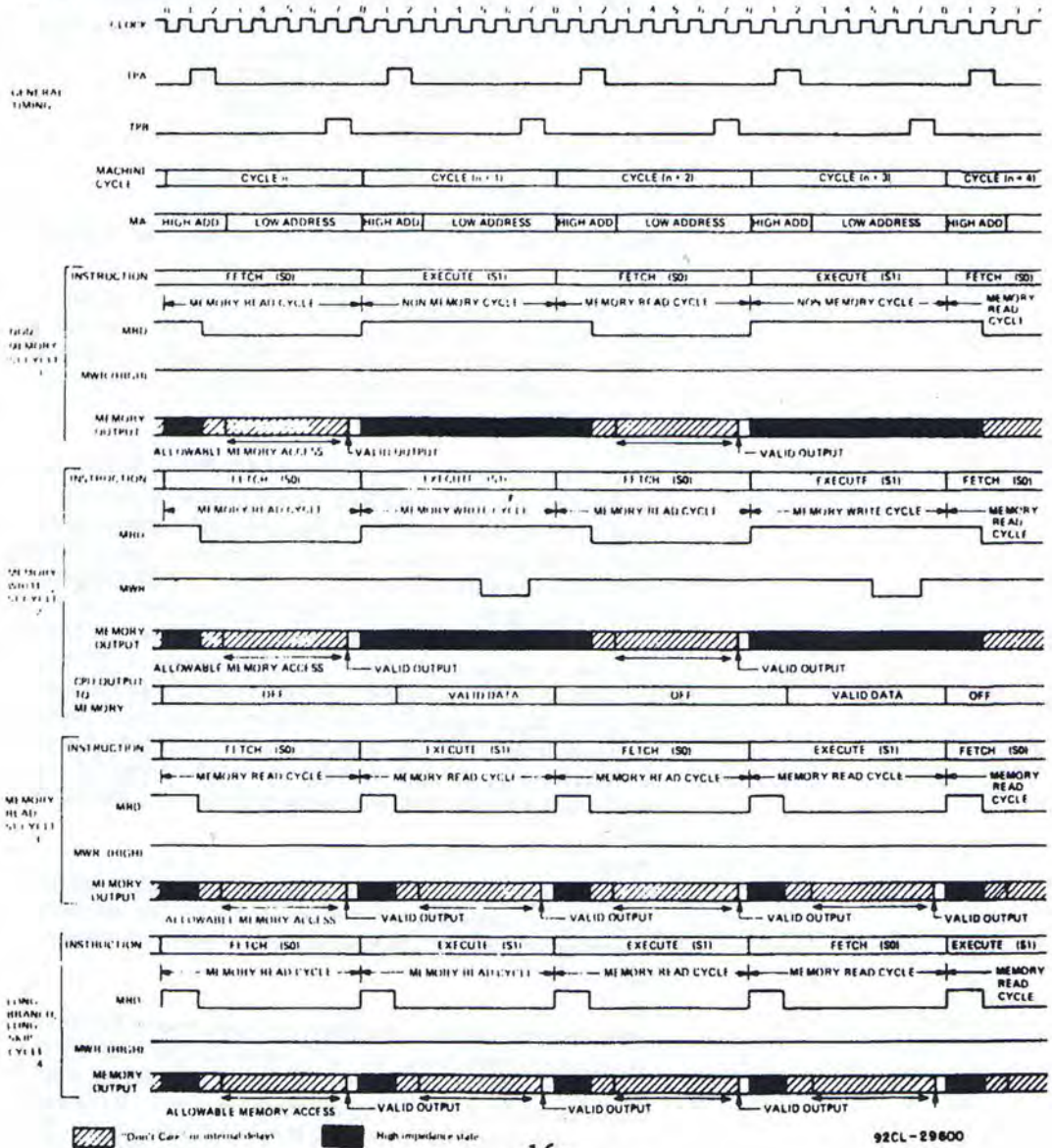


Fig. 15 – CDP1802 microprocessor state transitions (Run Mode).



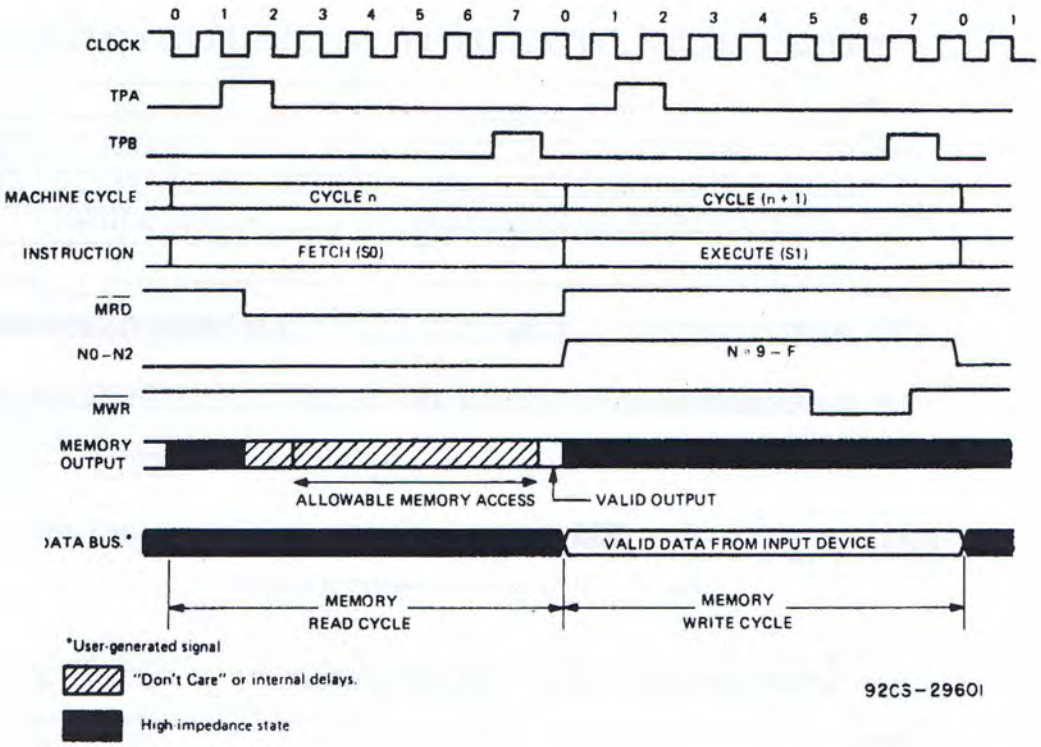


Fig. 17 – Timing diagram for machine cycle type No. 5.

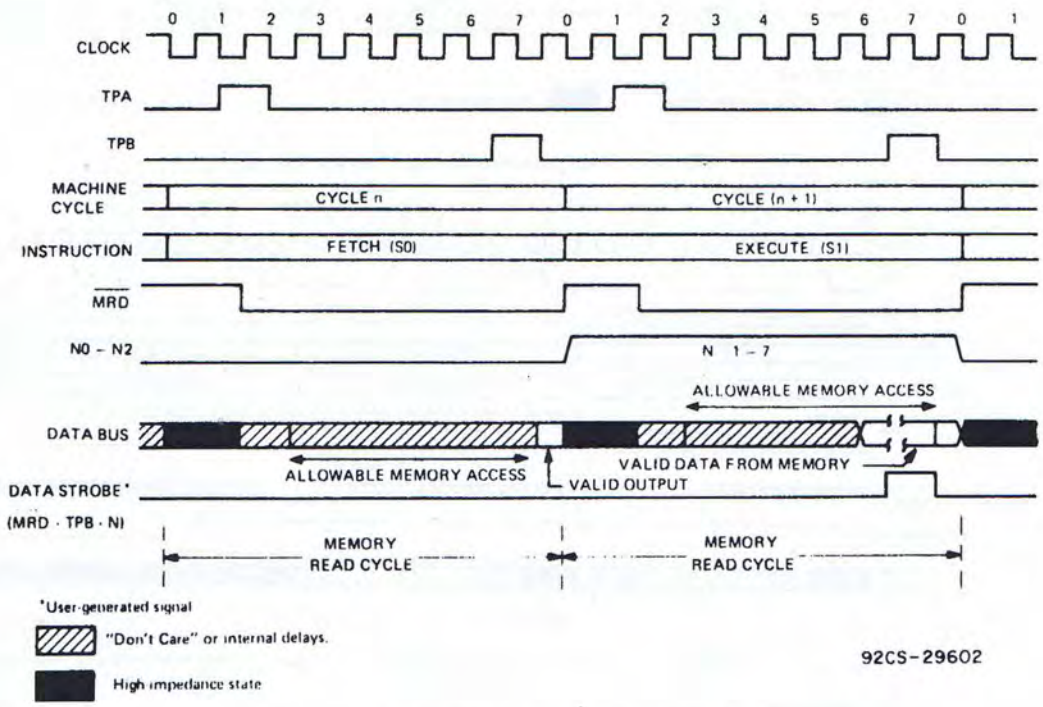


Fig. 18 – Timing diagram for machine cycle type No. 6.

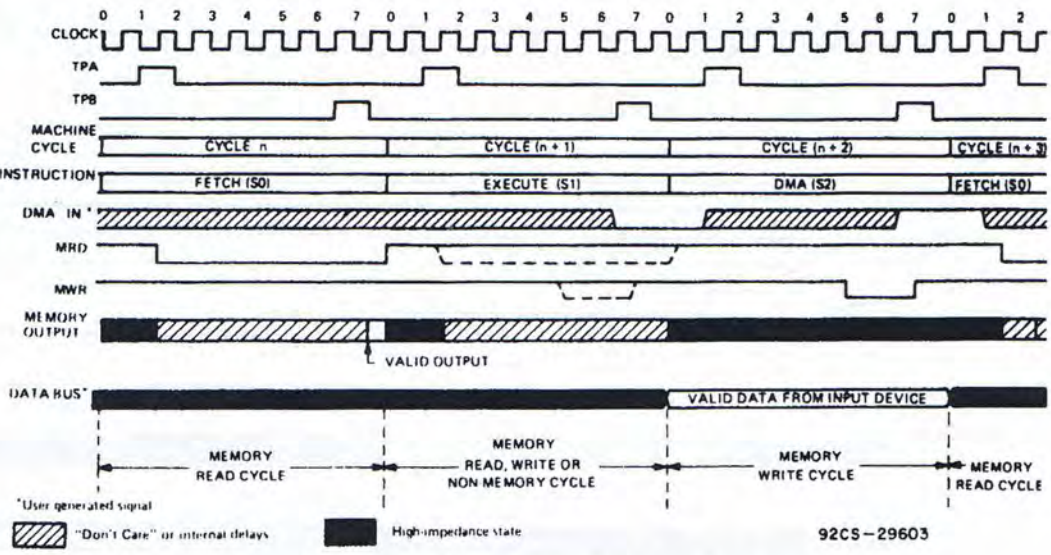


Fig. 19 – Timing diagram for machine cyle type No. 7.

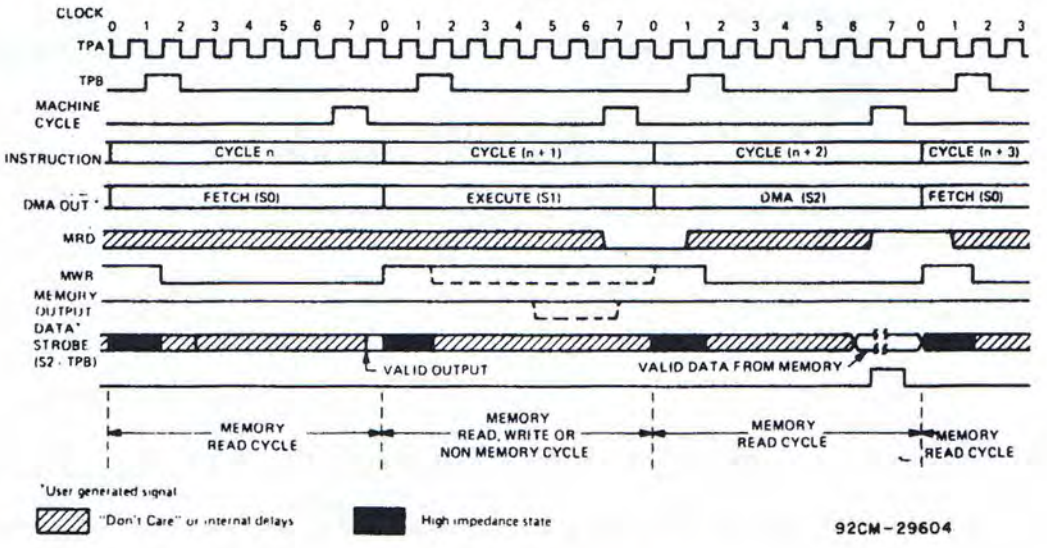


Fig. 20 – Timing diagram for machine cyle type No. 8.

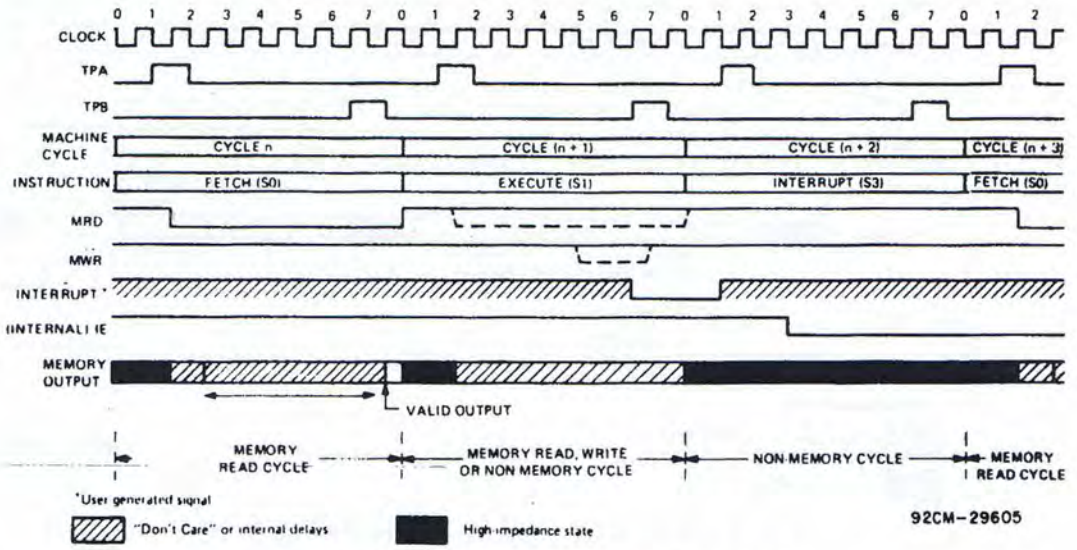


Fig. 21 – Timing diagram for machine cycle type No. 9.

TABLE II. CONDITIONS ON DATA BUS AND MEMORY ADDRESS LINES DURING ALL MACHINE STATES

STATE	I	N	MNEMONIC	INSTRUCTION	OPERATION	DATA BUS	MEMORY ADDRESS	$\overline{MRD}$	NOTES[G]
S1	RESET				JAM: I,N,Q,X,P=0 IE=1	0	R (0) UNDEFINED	1	A
	FIRST CYCLE AFTER RESET NOT PROGRAMMER ACCESSIBLE				INITIALIZE	0	R (0) UNDEFINED	1	B
S0	FETCH				M(R(P))→I,N R(P)+1	M(R(P))	R(P)	0	C
S1 (Execute)	0	0	IDL	IDLE	[Load = 0 (Program Idle)]	M (R(0))	R (0)	0	D,3
					[Load = 1 (Load Mode)]	M(R(0))	PREVIOUS ADDRESS	0	E,3
		N≠0	LDN	LOAD D VIA N	M(R(N))→D	M(R(N))	R(N)	0	3
	1	N	INC	INCREMENT	R(N)+1	FLOAT	R(N)	1	1
	2	N	DEC	DECREMENT	R(N)−1	FLOAT	R(N)	1	1
	3	N	—	SHORT BRANCH	[BRANCH NOT TAKEN]	M(R(P))	R(P)	0	3
					[BRANCH TAKEN]	M(R(P))	R(P)	0	
	4	N	LDA	LOAD ADVANCE	M(R(N))→D R(N)+1	M(R(N))	R(N)	0	3
	5	N	STR	STORE VIA N	D→M(R(N))	D	R(N)	1	3
	6	0	IRX	INC REG X	R(X)+1	M(R(X))	R(X)	0	3
		N=1−7	OUT N	OUTPUT	M(R(X))→BUS R(X)+1	M(R(X))	R(X)	0	6
		N=9−F	INP N	INPUT	BUS→M(R(X)), D	I/O DEVICE	R(X)	1	5
	7	0	RET	RETURN	M(R(X))→(X,P) R(X)+1; 1→IE	M(R(X))	R(X)	0	3
		1	DIS	DISABLE	M(R(X))→(X,P) R(X)+1; 0→IE	M(R(X))	R(X)	0	3
		2	LDXA	LOAD VIA X AND ADVANCE	M(R(X))→D P(X)−1	M(R(X))	R(X)	0	3
		3	STXD	STORE VIA X AND DECREMENT	D→M(R(X)) R(X)−1	D	R(X)	1	2
		4,5,7	—		ALU OPERATION	M(R(X))	R(X)	0	3
		6	—		ALU OPERATION	FLOAT	R(X)	1	1
		8	SAV	SAVE	T→M(R(X))	T	R(X)	1	2
		9	MARK	MARK	(X,P)→T, M(R(2)) P→X; R(2)−1	T	R(2)	1	2
		A	REQ	RESET Q	Q 0	FLOAT	R(P)	1	1
		B	SEQ	SET Q	Q 1	FLOAT	R(P)	1	1
		C,D,F			ALU OPERATION IMMEDIATE	M(R(P))	R(P)	0	3
		E			ALU OPERATION	FLOAT	R(X)	1	1
	8	N	GLO	GET LOW	R(N).0→D	R(N).0	R(N)	1	1
	9	N	GHI	GET HIGH	R(N).1→D	R(N).1	R(N)	1	1
	A	N	PLO	PUT LOW	D→R(N).0	D	R(N)	1	1
	B	N	PHI	PUT HIGH	D→R(N).1	D	R(N)	1	1
	C	0,1,2 3,8,9 A,B		LONG BRANCH	[BRANCH NOT TAKEN]	M(R(P))	R(P)	0	4
					[BRANCH TAKEN]	M(R(P))	R(P)	0	4
		5,6,7 C,D,E F		LONG SKIP	[SKIP NOT TAKEN]	M(R(P))	R(P)	0	4
					[SKIP TAKEN]	M(R(P))	R(P)	0	4
		4	NOP	NO OPERATION	NO OPERATION	M(R(P))	R(P)	0	4
	D	N	SEP	SET P	N→P	N N	R(N)	1	1
	E	N	SEX	SET X	N→X	N N	R(N)	1	1
	F	0	LDX	LOAD VIA X	M(R(X))→D	M(R(X))	R(X)	0	3
		1,2,3 4,5,7			ALU OPERATION	M(R(X))	R(X)	0	3
		6	SHR	SHIFT RIGHT	SHIFT D RIGHT LSB(D)→DF 0→MSB(D)	FLOAT	R(X)	1	1
		8	LDI	LOAD IMMEDIATE	M(R(P))→D R(P)+1	M(R(P))	R(P)	0	3
		9,A,B C,D,F			ALU OPERATION IMMEDIATE	M(R(P))	R(P)	0	3
		E	SHL	SHIFT LEFT	ALU OPERATION	FLOAT	R(P)	1	1
S2	IN REQUEST			DMA IN	BUS→M(R(0))	I/O DEVICE	R (0)	1	F,7
	OUT REQUEST			DMA OUT	M(R(0))→BUS	M(R(0))	R (0)	0	F,8
S3	INTERRUPT				X,P→T, 0→IE 2→X, 1→P	FLOAT	R(N)	1	9

NOTES:

A. IE = 1; TPA, TPB suppressed, state = S1
B. BUS = 0 for entire cycle
C. Next state always S1
D. Wait for DMA or INTERRUPT
E. Suppress TPA, wait for DMA
F. IN REQUEST has priority over OUT REQUEST
G. Numbers refer to machine cycles types — refer to timing diagrams, Figs. 16 through 20.

OPERATING AND HANDLING CONSIDERATIONS

1. **Handling**
   All inputs and outputs of RCA COS/MOS devices have a network for electrostatic protection during handling. Recommended handling practices for COS/MOS devices are described in ICAN-6525, "Guide to Better Handling and Operation of CMOS Integrated Circuits."
2. **Operating**

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause $V_{DD}-V_{SS}$ to exceed the absolute maximum rating.

Input Signals

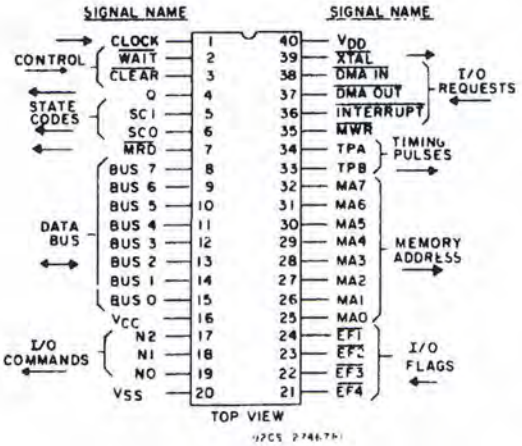
To prevent damage to the input protection circuit, input signals should never be greater than V_{CC} nor less than V_{SS}. Input currents must not exceed 10 mA even when the power supply is off.

Unused Inputs

A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{CC} or V_{SS}, whichever is appropriate.

Output Short Circuits

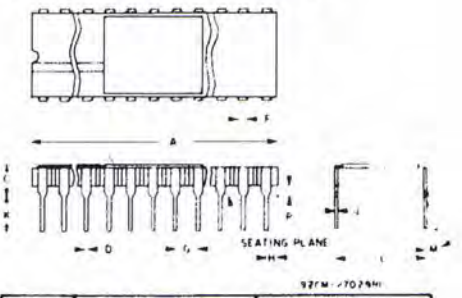
Shorting of outputs to V_{DD}, V_{CC}, or V_{SS} may damage COS/MOS devices by exceeding the maximum device dissipation.



When incorporating RCA Solid State Devices in equipment, it is recommended that the designer refer to "Operating Considerations for RCA Solid State Devices", Form No. 1CE-402, available on request from RCA Solid State Division, Box 3200, Somerville, N. J. 08876.

DIMENSIONAL OUTLINE

CDP1802D, CDP1802CD
40-Lead Dual-In-Line Ceramic



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	50.30	51.30	1.980	2.020
C	2.42	3.93	0.095	0.155
D	0.43	0.56	0.017	0.023
F	1.27 REF		0.050 REF.	
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.30	0.008	0.012
K	3.18	4.45	0.125	0.175
L	14.74	15.74	0.580	0.620
M	—	7°	—	7°
P	0.64	1.27	0.025	0.050
N	40		40	

NOTES
1. Leads within 0.13 mm (0.005) radius of true position at maximum material condition.
2. Dimension "L" to center of leads when formed parallel.
3. When this device is supplied solder dipped, the maximum lead thickness (narrow portion) will not exceed 0.013 in. (0.33 mm).

MWS5101D, CDP1822D
TERMINAL ASSIGNMENTS

256-Word by 4-Bit LSI Static Random-Access Memory

RCA Type No.	Max. Access Time, 0-70°C - ns		Max. Quiescent Current, 0-70°C - μA	
	V_{DD}=5 V	V_{DD}=10 V	V_{DD}=5 V	V_{DD}=10 V
MWS5101DL1	450	–	10	–
MWS5101DL3	450	–	100	–
MWS5101DL8	450	–	500	–
CDP1822DL1	450	250	10	50
CDP1822DL3	450	250	100	200
CDP1822DL8	450	250	500	500

The RCA-MWS5101D and CDP1822D are 256-word by 4-bit static random-access memories designed for use in memory systems where high speed, low power, and simplicity in use are desirable. These types have separate data inputs and data outputs and utilize a single power supply of 4.5 to 5.5 V for the MWS5101D and 4.5 to 10.5 V for the CDP1822D. Two Chip-Select inputs are provided to simplify system expansion. An Output Disable control provides Wire-OR capability and is also useful in common Input/Output systems. The Read/Write input or Output Disable input allows these RAMs to be used in common data Input/Output systems by forcing the output into a high-impedance state during a write operation independent of the Chip-Select input conditions. After valid data appears at the output, the address inputs may be changed immediately. This output data will be valid until either the Output Disable input or the Chip-Select input is high or the new data of the next memory cycle is applied.

The high noise immunity of the CMOS technology is preserved in this design. For TTL interfacing at 5-V operation, excellent system noise margin is preserved by use of a pull-up resistor at each input.

The MWS5101D and CDP1822D types are supplied in 22-lead hermetic dual-in-line side-brazed ceramic packages.

Features:

- **Industry standard pinout**
- **Two Chip-Select inputs – simple memory expansion**
- **Memory retention for standby battery voltage of 2 V min.**
- **Single-power-supply operation – 4.5 to 5.5 V for MWS5101D and 4.5 to 10.5 V for CDP1822D**
- **High noise immunity – 20% of V_{DD}**
- **TTL compatible (MWS5101D)**
  - **Drives one TTL load**
  - **Accepts TTL level inputs using pull-up resistor**
- **Output-Disable for common I/O systems**
- **3-State data output for bus-oriented systems**
- **Separate data inputs and outputs**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE (V_{DD})
(ALL VOLTAGES REFERENCED TO V_{SS} TERMINAL)
MWS5101D . . . . . –0.5 TO +6 V
CDP1822D . . . . . –0.5 TO +11 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . $V_{SS} \leqslant V_I \leqslant V_{DD}$
OPERATING-TEMPERATURE RANGE (T_A) . . . . . –20 TO +85°C
STORAGE-TEMPERATURE RANGE (T_{STG}) . . . . . –65 TO +150°C
LEAD TEMPERATURE (DURING SOLDERING):
AT DISTANCE 1/16 ± 1/32 INCH (1.59 ± 0.79 MM)
FROM CASE FOR 10 S MAX. . . . . +265°C

RECOMMENDED OPERATING CONDITIONS at T_A=25°C Unless Otherwise Specified

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	MWS5101D		CDP1822D		
	Min.	Max.	Min.	Max.	
DC Operating Voltage Range (At T_A = Full Package Temperature Range)	4.5	5.5	4.5	10.5	V
Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V
Operating Temperature Range	0	70	0	70	°C

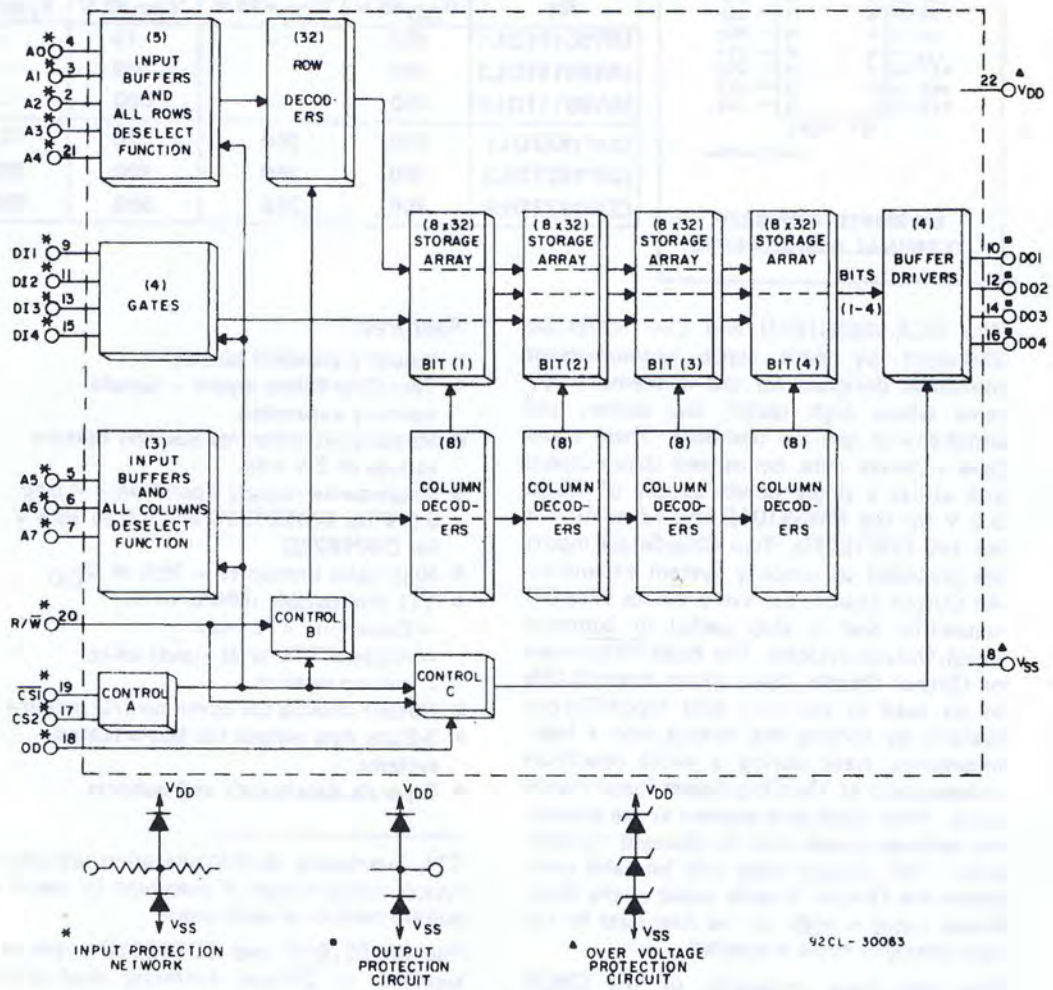


Fig. 1 – Functional block diagram for MWS5101D and CDP1822D.

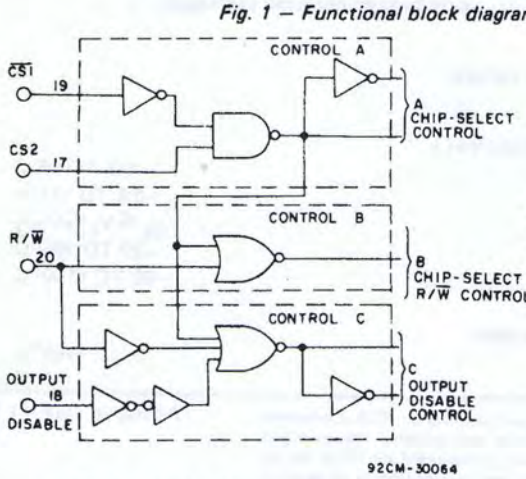


Fig. 2 – Logic diagram of controls for MWS5101D and CDP1822D.

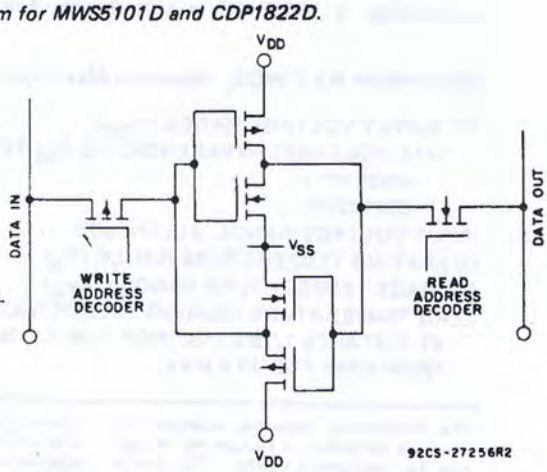


Fig. 3 – Memory cell configuration.

OPERATIONAL MODES

MODE	INPUTS				OUTPUT
	$\overline{\text{Chip Select 1}}$ $\overline{CS_1}$	Chip Select 2 CS_2	Output Disable OD	Read/$\overline{\text{Write}}$ R/$\overline{W}$	
READ	0	1	0	1	Read
WRITE	0	1	X	0	High Impedance
STANDBY	1	X	X	X	High Impedance
STANDBY	X	0	X	X	High Impedance
OUTPUT DISABLE	X	X	1	X	High Impedance

Logic 1 = High Logic 0 = Low X = Don't Care

STATIC ELECTRICAL CHARACTERISTICS at T_A = 0 to 70°C, V_{DD} ± 5%.

CHARACTERISTIC		TEST CONDITIONS			LIMITS						UNITS
					MWS5101D			CDP1822D			
		V_O (V)	V_{IN} (V)	V_{DD} (V)	Min.	Typ.	Max.	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD}	MWS5101DL1	–	0,5	5	–	–	10	–	–	–	μA
	MWS5101DL3	–	0,5	5	–	–	100	–	–	–	
	MWS5101DL8	–	0,5	5	–	–	500	–	–	–	
	CDP1822DL1	–	0,5	5	–	–	–	–	–	10	
		–	0,10	10	–	–	–	–	–	50	
	CDP1822DL3	–	0,5	5	–	–	–	–	–	100	
		–	0,10	10	–					200	
	CDP1822DL8		0,5	5						500	
		–	0,10	10	–		–		–	500	
Output Voltage:* Low-Level, V_{OL}		–	0,5	5	–	0	0.1		0	0.1	V
		–	0,10	10	–	–	–		0	0.1	
High-Level, V_{OH}		–	0,5	5	4.9	5	–	4.9	5	–	
		–	0,10	10	–	–	–	9.9	10	–	
Input Low Voltage, V_{IL}		0.5,4.5	–	5	–	–	1	–	–	1	V
		0.5,9.5	–	10	–	–	–	–	–	2	
Input High Voltage, V_{IH}		0.5,4.5	–	5	4	–	–	4	–	–	
		0.5,9.5	–	10	–	–	–	8	–	–	
Output Low (Sink) Current, I_{OL}		0.4	0,5	5	2	4	–	2	4	–	mA
		0.5	0,10	10	–	–	–	4.5	9	–	
Output High (Source) Current, I_{OH}		4.6	0,5	5	−1	−2	–	−1	−2	–	
		9.5	0,10	10	–	–	–	−2.2	−4.4	–	
Input Current, I_{IN}			0,5	5	–	–	±1			±1	μA
		–	0,10	10		–			–	±1	
3-State Output Leakage Current, I_{OUT}		0,5	0,5	5			±1		–	±1	
		0,10	0,10	10						±1	
Operating Current, I_{DD1} #			0,5	5		4	8		4	8	mA
		–	0,10	10	–	–	–	–	8	16	
Input Capacitance, C_{IN}		–	–	–	–	5	7.5	–	5	7.5	pF
Output Capacitance, C_{OUT}		–	–	–	–	5	7.5	–	5	7.5	

*I_O 1 μA.

#Outputs open circuited; cycle time 1 μs.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=0 to 70°C; V_{DD} ±5%; t_r,t_f=20 ns; V_{IH}=0.8 V_{DD}; V_{IL}=0.2 V_{DD}; C_L=100 pF and 1 TTL Load; See Fig. 4.

CHARACTERISTIC		V_{DD} (V)	LIMITS				UNITS
			MWS5101D		CDP1822D		
			Min.	Max.	Min.	Max.	
Read Cycle Times							
Read Cycle,	t_{RC}	5	450	–	450	–	ns
		10	–	–	250	–	
Access from Address,	t_{ADA}	5	–	450	–	450	ns
		10	–	–	–	250	
Output from $\overline{\text{Chip-Select 1}}$,	t_{DOA1}	5	–	400	–	400	ns
		10	–	–	–	250	
Output from Chip-Select 2,	t_{DOA2}	5	–	500	–	500	ns
		10	–	–	–	250	
Output from Output-Disable,	t_{DOA3}	5	–	250	–	250	ns
		10	–	–	–	60	
Output Hold from $\overline{\text{Chip-Select 1}}$	t_{DOH1}	5	0	–	0	–	ns
		10	–	–	0	–	
Output Hold from Chip-Select 2,	t_{DOH2}	5	0	–	0	–	ns
		10	–	–	0	–	
Output Hold from Output-Disable,	t_{DOH3}	5	0	130	0	130	ns
		10	–	–	0	100	

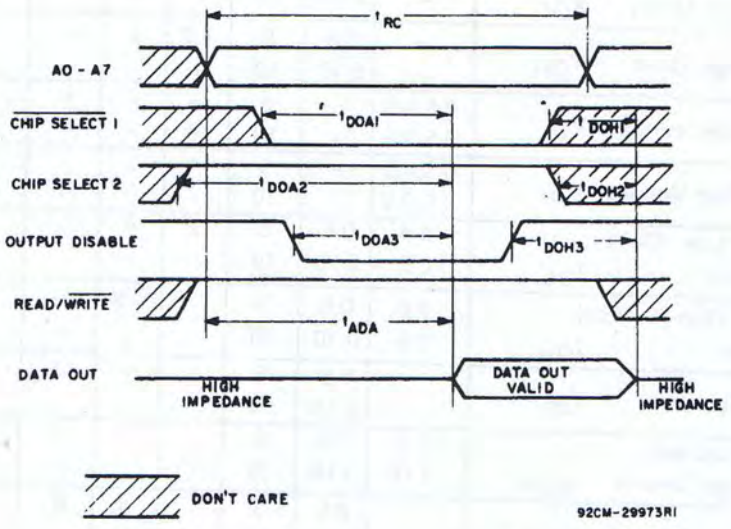


Fig. 4 – Read cycle waveforms.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=0 to 70°C; V_{DD} ±5%; t_r,t_f=20 ns; V_{IH}=0.8 V_{DD}; V_{IL}=0.2 V_{DD}; C_L=100 pF and 1 TTL Load.

CHARACTERISTIC		V_{DD} (V)	LIMITS				UNITS
			MWS5101D		CDP1822D		
			Min.	Max.	Min.	Max.	
Write Cycle Times							
Write Cycle,	t_{WC}	5	450	–	450	–	ns
		10	–	–	250	–	
$\overline{\text{Chip-Select 1}}$ Setup,	t_{CSS1}	5	350	–	350	–	ns
		10	–	–	200	–	
Chip-Select 2 Setup,	t_{CSS2}	5	350	–	350	–	ns
		10	–	–	200	–	
Read Hold,	t_{RDH}	5	150	–	150	–	ns
		10	–	–	100	–	
Write Recovery,	t_{WR}	5	50	–	50	–	ns
		10	–	–	35	–	
Write Width,	t_{WRW}	5	250	–	250	–	ns
		10	–	–	150	–	
Data In Width Effective,	t_{DIW}	5	250	–	250	–	ns
		10	–	–	150	–	
Data In Hold,	t_{DIH}	5	50	–	50	–	ns
		10	–	–	30	–	

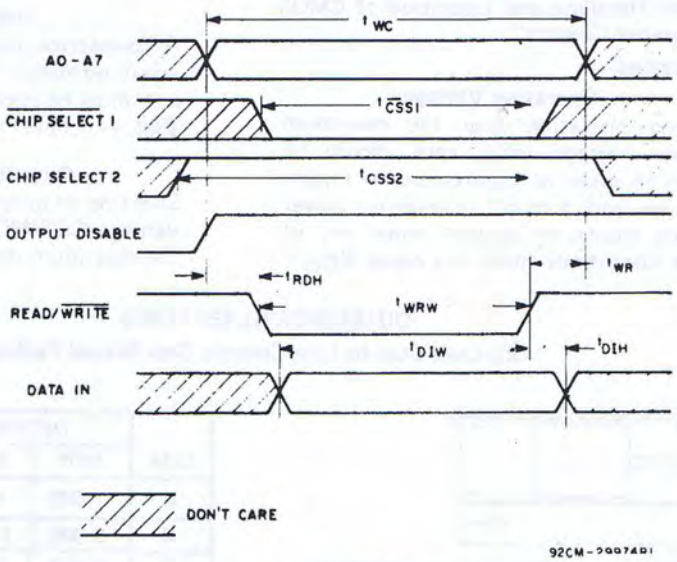


Fig. 5 – Write cycle waveforms.

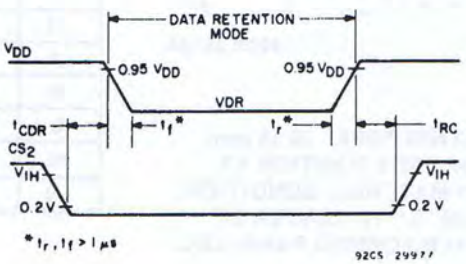


Fig. 6 – Low V_{DD} data retention waveforms and timing.

DATA RETENTION CHARACTERISTICS at T_A = 0 to 70°C; see Fig. 6.

CHARACTERISTIC	TEST CONDITIONS	V_{DD} (V)	MWS5101D Min.	MWS5101D Max.	CDP1822D Min.	CDP1822D Max.	UNITS
Data Retention Voltage, V_{DR}		5	2	–	2	–	V
		10	2	–	2	–	
Data Retention Quiescent Current, I_{DD} MWS5101DL1	V_{DR}=2 V	–	–	10	–	–	μA
MWS5101DL3		–	–	100	–	–	
MWS5101DL8		–	–	500	–	–	
CDP1822DL1		–	–	–	–	10	
CDP1822DL3		–	–	–	–	100	
CDP1822DL8		–	–	–	–	500	
Chip Deselect to Data Retention Time, t_{CDR}	V_{DR}=2 V	5	600	–	600	–	ns
		10	–	–	300	–	
Recovery to Normal Operation Time, t_{RC}		5	600	–	600	–	
		10	–	–	300	–	

OPERATING AND HANDLING CONSIDERATIONS

1. **Handling**

All inputs and outputs of this device have a network for electronic protection during handling. Recommended handling practices for COS/MOS devices are described in ICAN-6525 "Guide to Better Handling and Operation of CMOS Integrated Circuits".

2. **Operating**

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause V_{DD}–V_{SS} to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} nor less than V_{SS}. Input currents must not exceed 10 mA even when the power supply is off.

Unused Inputs

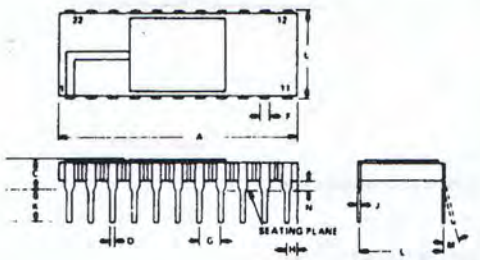
A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{DD} or V_{SS}, whichever is appropriate.

Output Short Circuits

Shorting of outputs to V_{DD} or V_{SS} may damage COS/MOS devices by exceeding the maximum device dissipation.

DIMENSIONAL OUTLINE

22-Lead Dual-In-Line Ceramic Side-Brazed Package



92CS-25186

DIM.	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.
A	1.065	1.100	27.05	27.94
C	0.085	0.145	2.16	3.68
D	0.017	0.023	0.43	0.56
F	0.040 REF.		1.02 REF.	
G	0.100 BSC		2.54 BSC	
H	0.030	0.070	0.76	1.78
J	0.008	0.012	0.20	0.30
K	0.125	0.175	3.18	4.45
L	0.380	0.420	9.65	10.67
M	–	7°	–	7°
N	0.025	0.050	0.64	1.27

NOTES

1. LEADS WITHIN 0.005" (0.13 mm) RADIUS OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. WHEN THIS DEVICE IS SUPPLIED SOLDER-DIPPED, THE MAXIMUM LEAD THICKNESS (NARROW PORTION) WILL NOT EXCEED 0.013" (0.33 mm).

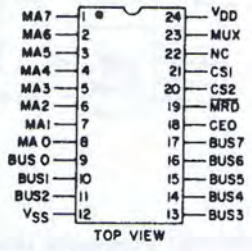
When incorporating RCA Solid State Devices in equipment, it is recommended that the designer refer to "Operating Considerations for RCA Solid State Devices", Form No. 1CE-402, available on request from RCA Solid State Division, Box 3200, Somerville, N. J. 08876.

RCA
Solid State Division

Microprocessor Products

Preliminary Data▲

CDP1831D
CDP1831CD



Terminal Assignment

512-Word x 8-Bit Static Read-Only Memory

Features:

- **Static Silicon-Gate CMOS circuitry—CD4000-series compatible**
- **Compatible with CDP1800-series microprocessors at maximum speed**
- **Interfaces with CDP1801, CDP1802 microprocessors without additional components**
- **Fast access time: 400 ns typ. at V_{DD} = 10 V**
- **Single voltage supply**
- **On-chip address latch**
- **Full military temperature range (−55°C to +125°C)**
- **Optional programmable location within 64K memory space**
- **Low quiescent and operating power**

The RCA-CDP1831D and CDP1831CD are static 4096-bit mask-programmable COS/MOS read-only memories organized as 512 words x 8 bits and designed for use in CDP1800-series microprocessor systems. They will directly interface with either the CDP1801 or CDP1802 microprocessors without additional components.

The CDP1831 responds to 16-bit address multiplexed on 8 address lines. Address latches are provided on-chip to store the 8 most significant bits of the 16-bit address. By mask option, this ROM can be programmed to operate in any 512-word byte of 64K memory space. Three Chip-Select signals—CS1, CS2, $\overline{MRD}$—are also provided.

The polarity of the clock (TPA), and CS1 and CS2 are user mask-programmable. The Chip-Enable output signal (CEO) goes "high" when the device is selected. This signal is intended for use as an output disable control for small memory systems.

The CDP1831D is functionally identical to the CDP1831CD. The CDP1831D has a recommended operating voltage range of 3 to 12 volts, and the CDP1831CD has a recommended operating voltage range of 4 to 6 volts.

The CDP1831D and CDP1831CD are supplied in 24-lead, hermetic, dual-in-line ceramic packages.

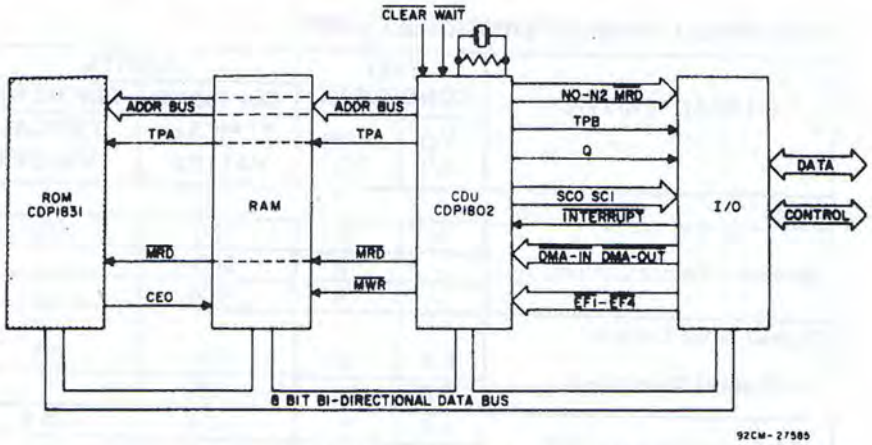


Fig. 1—Typical CDP1802 microprocessor system.

▲The Preliminary Data are intended for guidance purposes in evaluating the device for equipment design. The device is now being designed for inclusion in our standard line of commercially available products. For current information on the status of this program, please contact your RCA Sales Office.

Printed in USA/6-77

Supersedes data issued 2-76

MAXIMUM RATINGS,
Absolute-Maximum Values

Storage-Temperature Range (T_{stg}) ..... −65 to +150°C

Operating-Temperature Range (T_A) ..... −55 to +125°C

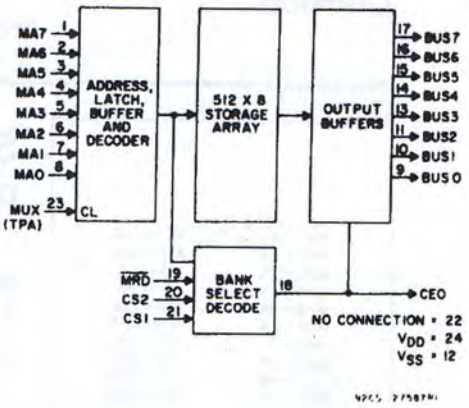
DC Supply-Voltage Range (V_{DD})
(All voltage values referenced to V_{SS} terminal)
- CDP1831D ..... −0.5 to +15 V
- CDP1831CD ..... −0.5 to +7 V

Power Dissipation Per Package (P_D):
- For T_A= −55 to +100°C ..... 500 mW
- For T_A=+100 to +125°C ..... Derate Linearly to 200 mW

Device Dissipation Per Output Transistor:
- For T_A= −55°C to +125°C ..... 100 mW

Input Voltage Range, All Inputs ..... −0.5 to V_{DD} +0.5 V

Lead Temperature (During Soldering):
- At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C



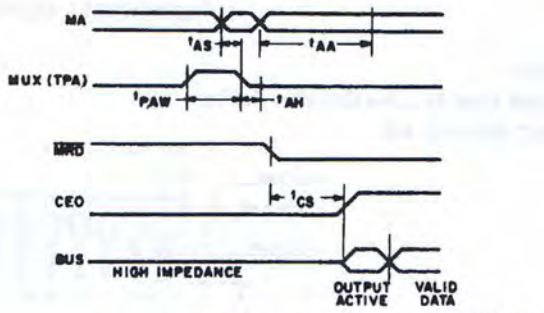
CDP1831 Functional Diagram

OPERATING CONDITIONS at T_A=25°C Unless Otherwise Specified
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	CONDITIONS V_{DD} (V)	LIMITS CDP1831D Min.	LIMITS CDP1831D Max.	LIMITS CDP1831CD Min.	LIMITS CDP1831CD Max.	UNITS
Supply-Voltage Range (At T_A=Full Package-Temperature Range)	–	3	12	4	6	V
Recommended Input Voltage Range	–	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V
MUX Pulse Width (TPA), t_{PAW}		Typical		Typical		ns
	5	200		100		
	10	100		–		
Address Setup Time, t_{AS}	5	100		100		ns
	10	50		–		
Address Hold Time, t_{AH}	5	150		150		ns
	10	75		–		

ELECTRICAL CHARACTERISTICS at T_A=25°C

CHARACTERISTIC	TEST CONDITIONS V_O (V)	TEST CONDITIONS V_{DD} (V)	LIMITS CDP1831D TYPICAL VALUES	LIMITS CDP1831CD TYPICAL VALUES	UNITS
Static					
Quiescent Device Current, I_L	–	5	100	100	μA
	–	10	500	–	
	–	15	1000	–	
Output Drive Current: N-Channel (Sink), I_DN	0.4	5	0.8	0.8	mA
	0.5	10	1.8	–	
P-Channel (Source), I_DP	4.6	5	−0.8	−0.8	
	9.5	10	−1.8	–	
Dynamic: t_r,t_f =10 ns, C_L=50 pF					
Access Time From Address Change, t_{AA}	–	5	850	850	ns
	–	10	400	–	
Chip Enable Output Delay Time From CS, t_{CS}	–	5	400	400	ns
	–	10	200	–	



Timing Diagram

Note:
The dynamic characteristics and timing diagrams indicate maximum performance capability of the CDP1831. When used directly with the CDP1802 microprocessor, timing will be determined by the clock frequency and internal delays of the microprocessor.

The following general timing relationships will hold when the CDP1831 is used with the CDP1802 microprocessor:

$t_{AH} = 0.5\ t_c$

$t_{PAW} = 1.0\ t_c$

$\overline{MRD}$ occurs one clock period (t_c) earlier than the address bits MA0-MA7.

where $t_c = \dfrac{1}{\text{CDP1802 clock frequency}}$

The CDP1831 is capable of operating at the maximum clock frequency of the CDP1802 microprocessor.

OPERATING & HANDLING CONSIDERATIONS

1. **Handling**
   All inputs and outputs of this device have a network for electrostatic protection during handling. Recommended handling practices for COS/MOS devices are described in ICAN-6000 "Handling and Operating Considerations for MOS Integrated Circuits".

2. **Operating**

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause V_{DD}-V_{SS} to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} nor less than V_{SS}. Input currents must not exceed 10 mA even when the power supply is off.

Unused Inputs

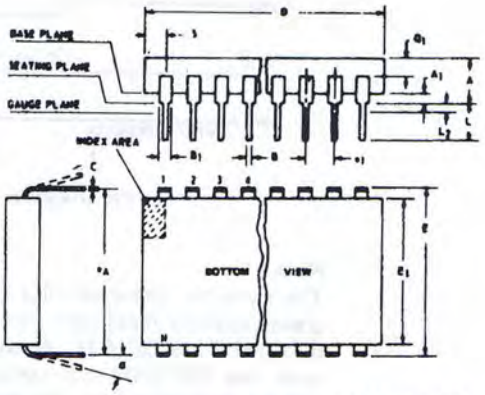
A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{DD} or V_{SS}, whichever is appropriate.

Output Short Circuits

Shorting of outputs to V_{DD} or V_{SS} may damage COS/MOS devices by exceeding the maximum device dissipation.

DIMENSIONAL OUTLINE

D Suffix
24-Lead Dual-In-Line Ceramic Package
JEDEC MO-015-AG



92CS-19948

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.090	0.150		2.29	3.81
A_1	0.020	0.065	2	0.51	1.65
B	0.015	0.020		0.381	0.508
B_1	0.045	0.055		1.143	1.397
C	0.008	0.012	1	0.204	0.304
D	1.15	1.22		29.21	30.98
E	0.600	0.625		15.24	15.87
E_1	0.480	0.520		12.20	13.20
e_1	0.100 TP		3	2.54 TP	
e_A	0.600 TP		3	15.24 TP	
L	0.100	0.180		2.54	4.57
L_2	0.000	0.030	3	0.00	0.76
α	0°	15°	4	0°	15°
N	24		5	24	
N_1	0		6	0	
Q_1	0.020	0.080		0.51	2.03
S	0.020	0.060		0.51	1.52

NOTES:

Refer to JEDEC Publication No. 13 for Rules for Dimensioning Axial Lead Product Outlines.

1. When this device is supplied solder dipped, the maximum lead thickness (narrow portion) will not exceed 0.013" (0.33 mm).
2. When base of body is to be attached to heat sink, terminal lead standoffs are not required and $A_1 = 0$. When $A_1 = 0$, the leads emerge from the body with the B_1 dimension and reduce to the B dimension above the seating plane.
3. e_1 and e_A apply in zone L_2 when unit is installed. Leads within 0.005 " (0.127 mm) radius of True Position (TP) at gauge plane with maximum material condition.
4. Applies to spread leads prior to installation.
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads.

When Incorporating RCA Solid State Devices in equipment, it is recommended that the designer refer to "Operating Considerations for RCA Solid State Devices", Form No. 1CE-402, available on request from RCA Solid State Division, Box 3200, Somerville, N.J. 08876.

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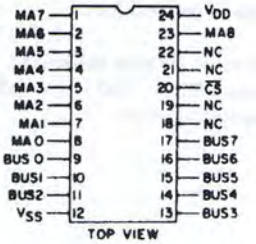
Microprocessor Products

Preliminary Data▲

CDP1832D
CDP1832CD



Terminal Assignment

512-Word x 8-Bit Static Read-Only Memory

Features:

- Static Silicon-Gate CMOS circuitry—CD4000-series compatible
- Compatible with CDP1800-series microprocessors at maximum speed
- Fast access time: 400 ns typ. at V_{DD} = 10 V
- Single voltage supply
- Full military temperature range (−55°C to +125°C)
- Functional replacement for industry type 8704 512 x 8 PROM
- Three-state outputs
- Low quiescent and operating power

The RCA-CDP1832D and CDP1832CD are static 4096-bit mask-programmable COS/MOS read-only memories organized as 512 words x 8 bits and designed for use in CDP1800-series microprocessor systems. The CDP1832 ROM's are completely static—no clocks are required.

A Chip-Select input ($\overline{CS}$) is provided for memory expansion. Outputs are enabled when $\overline{CS}$=0.

The CDP1832 is a pin-for-pin compatible replacement for the industry types 2704/8704 Reprogrammable Read-Only Memories.

The CDP1832D is functionally identical to the CDP1832CD. The CDP1832D has a recommended operating voltage range of 3 to 12 volts, and the CDP1832CD has a recommended operating voltage range of 4 to 6 volts.

The CDP1832D and CDP1832CD are supplied in 24-lead, hermetic, dual-in-line ceramic packages.

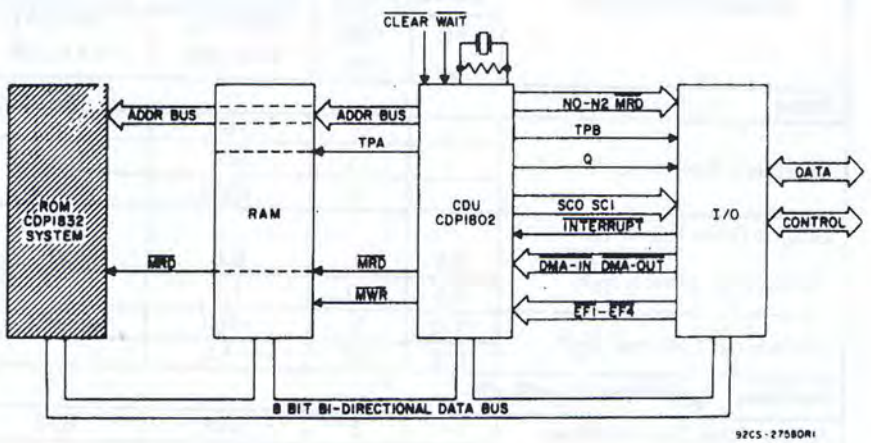


Fig. 1—Typical CDP1802 microprocessor system.

▲The Preliminary Data are intended for guidance purposes in evaluating the device for equipment design. The device is now being designed for inclusion in our standard line of commercially available products. For current information on the status of this program, please contact your RCA Sales Office.

Printed in USA/6-77
Supersedes data issued 2-76

MAXIMUM RATINGS, *Absolute-Maximum Values*

Storage Temperature Range (T_{stg}) ..... −65 to +150°C

Operating Temperature Range (T_A) ..... −55 to +125°C

DC Supply Voltage Range (V_{DD})
(All voltage values referenced to V_{SS} terminal)
- CDP1832D ..... −0.5 to +15 V
- CDP1832CD ..... −0.5 to +7 V

Power Dissipation Per Package (P_D):
- For T_A = −55 to +100°C ..... 500 mW
- For T_A = +100 to +125°C ..... Derate Linearly to 200 mW

Device Dissipation Per Output Transistor:
- For T_A = −55°C to +125°C ..... 100 mW

Input Voltage Range, All Inputs ..... −0.5 to V_{DD} +0.5 V

Lead Temperature (During Soldering):
- At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

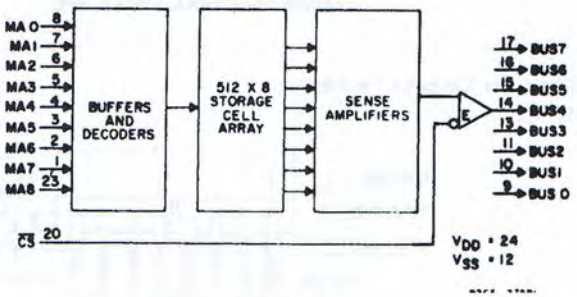
OPERATING CONDITIONS at T_A=25°C Unless Otherwise Specified

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

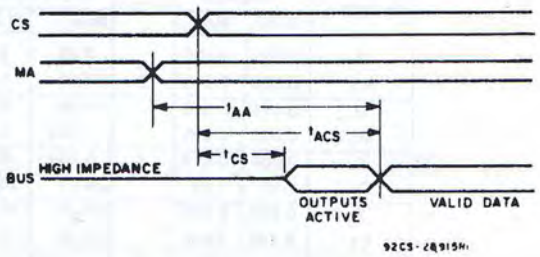
CHARACTERISTIC	CONDITIONS	LIMITS				UNITS
	V_{DD} (V)	CDP1832D		CDP1832CD		
		Min.	Max.	Min.	Max.	
Static						
Supply Voltage Range (At T_A = Full Package Temperature Range)	–	3	12	4	6	V
Recommended Input Voltage Range	–	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V

ELECTRICAL CHARACTERISTICS at T_A=25°C

CHARACTERISTIC	TEST CONDITIONS		LIMITS		UNITS
			CDP1832D	CDP1832CD	
	V_O (V)	V_{DD} (V)	TYPICAL VALUES	TYPICAL VALUES	
Static					
Quiescent Device Current, I_L	–	5	100	500	μA
	–	10	500	–	
	–	15	1000	–	
Output Drive Current: N-Channel (Sink), I_DN	0.4	5	0.8	0.8	mA
	0.5	10	1.8	–	
P-Channel (Source), I_DP	4.6	5	−0.8	−0.8	
	9.5	10	−1.8	–	
Dynamic: t_r, t_f=10 ns, C_L=50 pF					
Access Time From Address Change, t_{AA}	–	5	850	850	ns
	–	10	400	–	
Access Time From Chip Select, t_{ACS}	–	5	400	400	ns
	–	10	200	–	
Chip Select Delay, t_{CS}	–	5	400	400	ns
	–	10	200	–	



CDP1832
Functional Diagram



CDP1832
Timing Diagram

OPERATING & HANDLING CONSIDERATIONS

1. **Handling**
   All inputs and outputs of this device have a network for electrostatic protection during handling. Recommended handling practices for COS/MOS devices are described in ICAN 6000 "Handling and Operating Considerations for MOS Integrated Circuits"

2. **Operating**

   Operating Voltage

   During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause V_{DD}-V_{SS} to exceed the absolute maximum rating.

   Input Signals

   To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} nor less than V_{SS}. Input currents must not exceed 10 mA even when the power supply is off.

   Unused Inputs

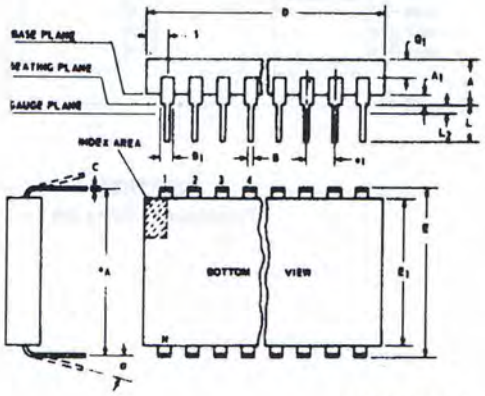
   A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{DD} or V_{SS}, whichever is appropriate.

   Output Short Circuits

   Shorting of outputs to V_{DD} or V_{SS} may damage COS/MOS devices by exceeding the maximum device dissipation.

DIMENSIONAL OUTLINE

D Suffix
24-Lead Dual-In-Line Ceramic Package
JEDEC MO-015-AG



92CS-19948

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.090	0.150		2.29	3.81
A_1	0.020	0.065	2	0.51	1.65
B	0.015	0.020		0.381	0.508
B_1	0.045	0.055		1.143	1.397
C	0.008	0.012	1	0.204	0.304
D	1.15	1.22		29.21	30.98
E	0.600	0.625		15.24	15.87
E_1	0.480	0.520		12.20	13.20
e_1	0.100 TP		3	2.54 TP	
e_A	0.600 TP		3	15.24 TP	
L	0.100	0.180		2.54	4.57
L_2	0.000	0.030	3	0.00	0.76
α	0°	15°	4	0°	15°
N	24		5	24	
N_1	0		6	0	
Q_1	0.020	0.080		0.51	2.03
S	0.020	0.060		0.51	1.52

NOTES:

Refer to JEDEC Publication No. 13 for Rules for Dimensioning Axial Lead Product Outlines.

1. When this device is supplied solder dipped, the maximum lead thickness (narrow portion) will not exceed 0.013" (0.33 mm).
2. When base of body is to be attached to heat sink, terminal lead standoffs are not required and $A_1 = 0$. When $A_1 = 0$, the leads emerge from the body with the B_1 dimension and reduce to the B dimension above the seating plane.
3. e_1 and e_A apply in zone L_2 when unit is installed. Leads within 0.005 " (0.127 mm) radius of True Position (TP) at gauge plane with maximum material condition.
4. Applies to spread leads prior to installation.
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads.

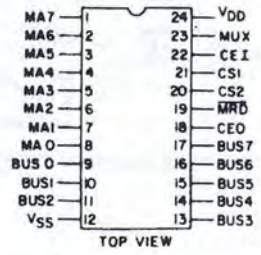
When Incorporating RCA Solid State Devices in equipment, it is recommended that the designer refer to "Operating Considerations for RCA Solid State Devices", Form No. 1CE-402, available on request from RCA Solid State Division, Box 3200, Somerville, N.J. 08876.

RCA
Solid State Division

Microprocessor Products

Preliminary Data▲

CDP1833D
CDP1833CD



Terminal Assignment

1024-Word x 8-Bit Static Read-Only Memory

Features:

- Compatible with CDP1800-series microprocessors at maximum speed
- Static silicon-gate CMOS circuitry—CD4000-series compatible
- Interfaces with CDP1801, CDP1802 microprocessors without additional components
- Fast access time: 350 ns typ. at V_{DD} = 10 V
- Single voltage supply
- On-chip address latch
- Full military temperature range (−55°C to +125°C)
- Optional programmable location within 64K memory space
- Low quiescent and operating power

The RCA-CDP1833D and CDP1833CD are static 8192-bit mask-programmable COS/MOS read-only memories organized as 1024-words x 8 bits and designed for use in CDP1800-series microprocessor systems. They will directly interface with either the CDP1801 or CDP1802 microprocessors without additional components.

The CDP1833 responds to 16-bit address multiplexed on 8 address lines. Address latches are provided on-chip to store the 8 most significant bits of the 16-bit address. By mask option, this ROM can be programmed to operate in any 1024-word byte of 64K memory space. Two Chip-Select signals are also provided.

The polarity of MUX(TPA), CEI, MRD, CS1 and CS2 are user mask-programmable. The Chip-Enable output signal (CEO) is "high" when either CEI is high or the chip is selected. CEO and CEI can be connected in a daisy chain to control selection of RAM chips in a microprocessor system without additional components.

The CDP1833D is functionally identical to the CDP1833CD. The CDP1833D has a recommended operating voltage range of 3 to 12 volts, and the CDP1833CD has a recommended operating voltage range of 4 to 6 volts.

The CDP1833D and CDP1833CD are supplied in 24-lead hermetic dual-in-line ceramic packages.

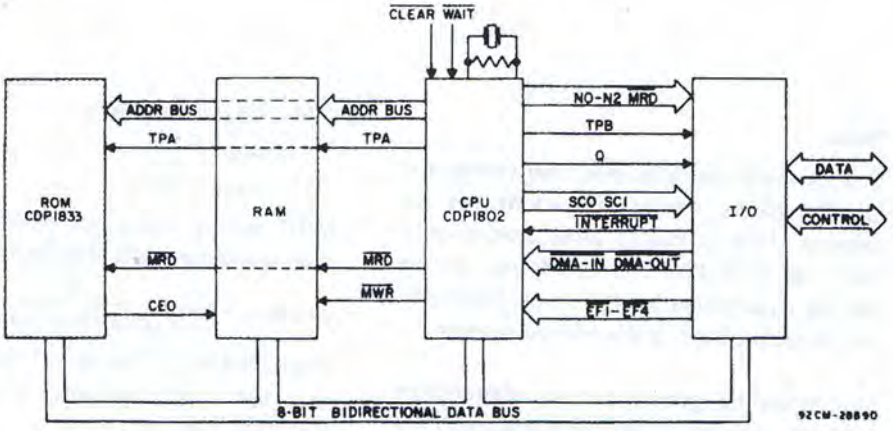


Fig. 1 – Typical CDP1802 microprocessor system.

▲ The Preliminary Data are intended for guidance purposes in evaluating the device for equipment design. The device is now being designed for inclusion in our standard line of commercially available products. For current information on the status of this program, please contact your RCA Sales Office.

Printed in USA/6-77
Supersedes data issued 3-77

MAXIMUM RATINGS,
Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE (V_{DD})
(All voltage values referenced to V_{SS} terminal)
CDP1833D . . . . . −0.5 to +15 V
CDP1833CD . . . . . −0.5 to +7 V
INPUT VOLTAGE RANGE,
ALL INPUTS . . . . −0.5 to V_{DD} +0.5 V
POWER DISSIPATION PER
PACKAGE (P_D):
For T_A = −55 to +100°C . . . . 500 mW
For T_A = +100 to
+125°C . . . Derate Linearly to 200 mW
DEVICE DISSIPATION PER
OUTPUT TRANSISTOR:
For T_A = −55°C to +125°C . . . 100 mW
OPERATING-TEMPERATURE
RANGE (T_A) . . . . . −55 to +125°C
STORAGE-TEMPERATURE
RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE
(During Soldering):
At distance 1/16 ± 1/32 inch (1.59
± 0.79 mm) from case for
10 s max. . . . . +265°C

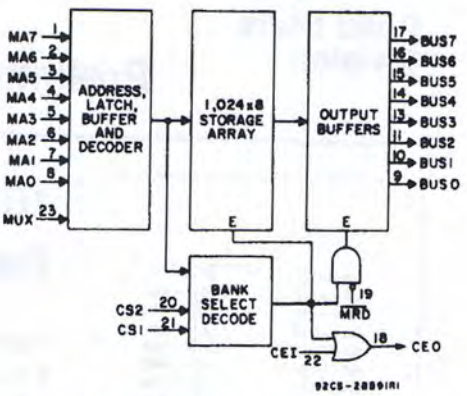


Fig. 2 – CDP1833 functional diagram.

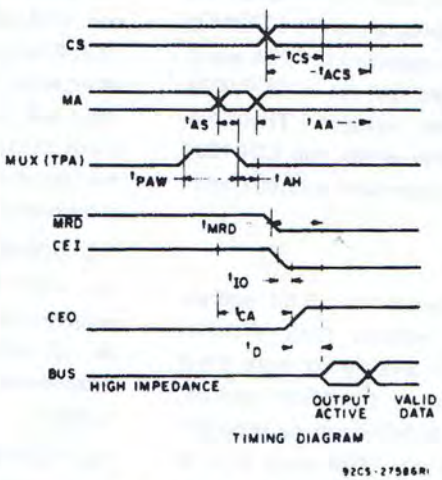


Fig. 3 – Timing diagram.

Note:

The dynamic characteristics and timing diagrams indicate maximum performance capability of the CDP1833. When used directly with the CDP1802 microprocessor, timing will be determined by the clock frequency and internal delays of the microprocessor.

The following general timing relationships will hold when the CDP1833 is used with the CDP1802 microprocessor:

$$t_{AH} = 0.5\ t_c$$

$$t_{PAW} = 1.0\ t_c$$

$\overline{MRD}$ occurs one clock period (t_c) earlier than the address bits MA0-MA7.

where $t_c = \frac{1}{\text{CDP1802 clock frequency}}$

The CDP1833 is capable of operating at the maximum clock frequency of the CDP1802 microprocessor.

OPERATING CONDITIONS at T_A=25°C Unless Otherwise Specified

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	CONDITIONS V_{DD} (V)	LIMITS CDP1833D Min.	LIMITS CDP1833D Max.	LIMITS CDP1833CD Min.	LIMITS CDP1833CD Max.	UNITS
Supply Voltage Range (At T_A Full Package Temperature Range)		3	12	4	6	V
Recommended Input Voltage Range		V_{SS}	V_{DD}	V_{SS}	V_{DD}	V
MUX Pulse Width (TPA), t_{PAW}	5	Typical 200		Typical 200		ns
	10	100		–		
Address Setup Time, t_{AS}	5	50		50		ns
	10	25		–		
Address Hold Time, t_{AH}	5	150		150		ns
	10	75		–		

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	TEST CONDITIONS V_O (V)	TEST CONDITIONS V_{DD} (V)	LIMITS CDP1833D TYPICAL VALUES	LIMITS CDP1833CD TYPICAL VALUES	UNITS
Static					
Quiescent Device Current, I_L Max.	–	5	100	1000	μA
	–	10	500	–	
	–	15	1000	–	
Output Drive Current: N-Channel (Sink), I_DN Min.	0.4	5	3.2	3.2	mA
	0.5	10	7.2	–	
P-Channel (Source), I_DP Min.	4.6	5	–2	–2	
	9.5	10	–5	–	
Dynamic: t_r, t_f = 10 ns, C_L = 50 pF					
Dynamic Power Dissipation● Chip Active CL - 3.2 MHz	–	5	30	30	mW
	–	10	120	–	
Chip Inactive CL = 3.2 MHz	–	5	5	5	
	–	10	20	–	
Access Time From Address Change, t_{AA}	–	5	850	850	ns
	–	10	350	–	
CEO From Address Change, t_{CA}	–	5	500	500	ns
	–	10	250	–	
Bus Contention Delay, t_D	–	5	300	300	ns
	–	10	150	–	
Daisy Chain Delay, t_{IO}	–	5	200	200	ns
	–	10	100	–	
Read Delay $t_{\overline{MRD}}$	–	5	500	500	ns
	–	10	250	–	
Chip Select Delay t_{CS}	–	5	600	600	ns
	–	10	300	–	
Access Time From Chip Select, t_{ACS}	–	5	700	700	ns
	–	10	300	–	

●Measured with random bit pattern at a system clock rate of 3.2 MHz, which results in a memory-cycle time of 2.5 μs. Power dissipation at other voltages and frequencies follows the relation $P = KfV^2$. Chip is inactive when deselected by either the Bank Select code or the Chip Select inputs.

OPERATING AND HANDLING CONSIDERATIONS

1. **Handling**
   All inputs and outputs of RCA COS/MOS devices have a network for electrostatic protection during handling. Recommended handling practices for COS/MOS devices are described in ICAN-6525, "Guide to Better Handling and Operation of CMOS Integrated Circuits."
2. **Operating**

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause $V_{DD}-V_{SS}$ to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} nor less than V_{SS}. Input currents must not exceed 10 mA even when the power supply is off.

Unused Inputs

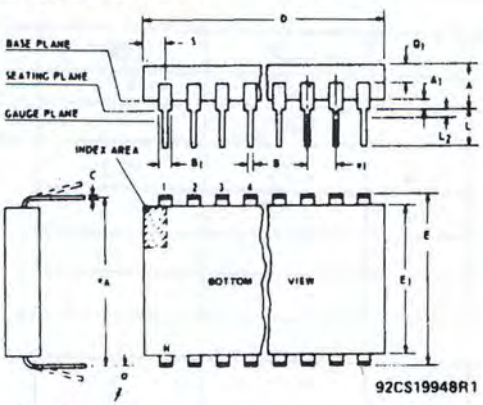
A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{DD} or V_{SS}, whichever is appropriate.

Output Short Circuits

Shorting of outputs to V_{DD} or V_{SS} may damage COS/MOS devices by exceeding the maximum device dissipation.

DIMENSIONAL OUTLINE

D SUFFIX
24-Lead Dual-In-Line Ceramic Package
JEDEC MO-015-AG



SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.090	0.150		2.29	3.81
A_1	0.020	0.065	2	0.51	1.65
B	0.015	0.020		0.381	0.508
B_1	0.045	0.055		1.143	1.397
C	0.008	0.012	1	0.204	0.304
D	1.15	1.22		29.21	30.98
E	0.600	0.625		15.24	15.87
E_1	0.480	0.520		12.20	13.20
e_1	0.100 TP		3	2.54 TP	
e_A	0.600 TP		3	15.24 TP	
L	0.100	0.180		2.54	4.57
L_2	0.008	0.030	3	0.00	0.76
α	0°	15°	4	0°	15°
N	24		5	24	
N_1	0		6	0	
Q_1	0.020	0.080		0.51	2.03
S	0.020	0.060		0.51	1.52

NOTES:

Refer to JEDEC Publication No. 95 for Rules for Dimensioning Axial Lead Product Outlines.

1. When this device is supplied solder dipped, the maximum lead thickness (narrow portion) will not exceed 0.013" (0.33 mm).
2. When base of body is to be attached to heat sink, terminal lead standoffs are not required and $A_1 = 0$. When $A_1 = 0$, the leads emerge from the body with the B_1 dimension and reduce to the B dimension above the seating plane.
3. e_1 and e_A apply in zone L_2 when unit is installed. Leads within 0.005 " (0.127 mm) radius of True Position (TP) at gauge plane with maximum material condition.
4. Applies to spread leads prior to installation.
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads.

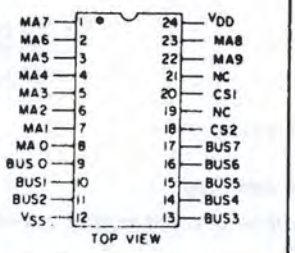
When incorporating RCA Solid State Devices in equipment, it is recommended that the designer refer to "Operating Considerations for RCA Solid State Devices", Form No. 1CE-402, available on request from RCA Solid State Division, Box 3200, Somerville, N. J. 08876.

RCA
Solid State Division

Microprocessor Products

Preliminary Data▲

CDP1834D
CDP1834CD



Terminal Assignment

1024-Word x 8-Bit Static Read-Only Memory

Features:

- Static Silicon-Gate CMOS circuitry-CD4000-series compatible
- Compatible with CDP1800-series microprocessors at maximum speed
- Fast access time: 350 ns typ. at V_{DD} = 10 V
- Single voltage supply
- Full military temperature range (−55°C to +125°C)
- Functional replacement for industry type 2708 1024 x 8 PROM
- Three-state outputs
- Low quiescent and operating power

The RCA-CDP1834D and CDP1834CD are static 8192-bit mask-programmable COS/MOS read-only memories organized as 1024 words x 8 bits and designed for use in CDP1800-series microprocessor systems. The CDP1834 ROM's are completely static—no clocks are required.

Two CHIP-SELECT inputs (CS1, CS2) are provided for memory expansion. The polarity of each CHIP-SELECT input is user mask-programmable.

The CDP1834 is pin-compatible with industry type 2308 ROMs and 2708 PROMs.

The two memories are functionally identical. They differ in that the CDP1834D has a recommended operating voltage range of 3 to 12 volts, and the CDP1834CD has a recommended operating voltage range of 4 to 6 volts.

The CDP1834D and CDP1834CD are supplied in 24-lead, hermetic, dual-in-line ceramic packages.

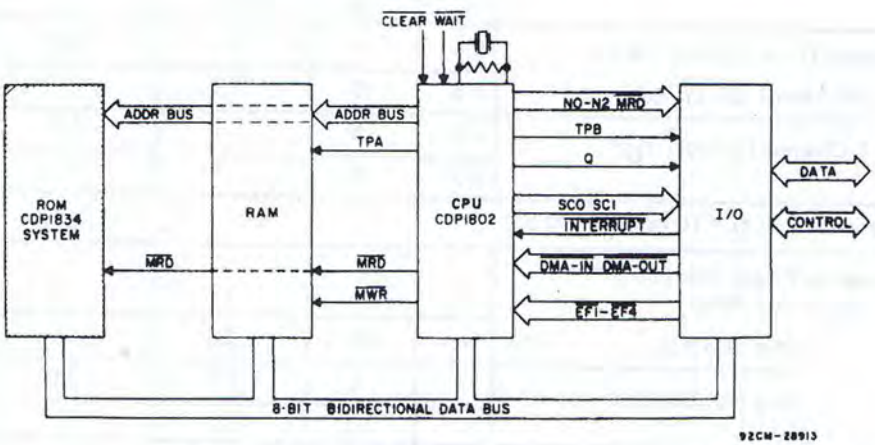


Fig. 1 – Typical CDP1802 microprocessor system.

▲ The Preliminary Data are intended for guidance purposes in evaluating the device for equipment design. The device is now being designed for inclusion in our standard line of commercially available products. For current information on the status of this program, please contact your RCA Sales Office.

Printed in USA/6-77

Supersedes data issued 3-77

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE (V_{DD})
(All voltage values referenced to V_{SS} terminal):
- CDP1834D . . . . . −0.5 to +15 V
- CDP1834CD . . . . . −0.5 to +7 V

POWER DISSIPATION PER PACKAGE (P_D):
- FOR T_A = −55 to +100°C . . . . . 500 mW
- FOR T_A = +100 to +125°C . . . . . Derate Linearly to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
- FOR T_A = −55°C to +125°C . . . . . 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A) . . . . . −55 to +125°C
LEAD TEMPERATURE (DURING SOLDERING):
- At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

OPERATING CONDITIONS at T_A = 25°C Unless Otherwise Specified

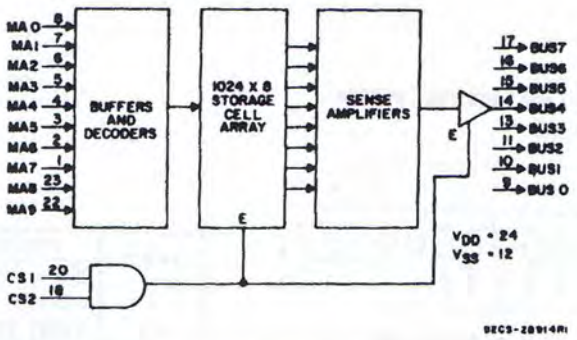
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	CONDITIONS	LIMITS				UNITS
	V_{DD} (V)	CDP1834D		CDP1834CD		
		Min.	Max.	Min.	Max.	
Static						
Supply-Voltage Range (At T_A = Full Package-Temperature Range)	–	3	12	4	6	V
Recommended Input Voltage Range	–	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V

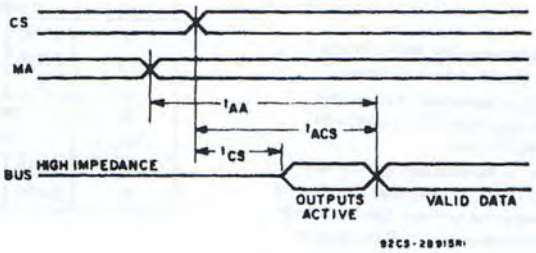
ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	TEST CONDITIONS		TYPICAL VALUES		UNITS
	V_O (V)	V_{DD} (V)	CDP1834D	CDP1834CD	
Static					
Quiescent Device Current, I_L (Max.)	–	5	100	1000	μA
	–	10	500	–	
	–	15	1000	–	
Output Drive Current: (Min.)	0.4	5	3.2	3.2	mA
N-Channel (Sink), I_DN	0.5	10	7.2	–	
P-Channel (Source), I_DP	4.6	5	−2	−3.2	
	9.5	10	−5	–	
Dynamic: t_r, t_f = 10 ns, C_L = 50 pF					
Dynamic Power Dissipation* (f_{CL} = 3.2 MHz)	–	5	15	15	mW
Chip Selected	–	10	60	–	
Chip Not Selected	–	5	2.5	2.5	mW
	–	10	10	–	
Access Time From Address	–	5	850	850	ns
Change, t_{AA}	–	10	350	–	
Access Time From Chip	–	5	700	700	ns
Select, t_{ACS}	–	10	300	–	
Chip Select Delay, t_{CS}	–	5	600	600	ns
	–	10	300	–	

* Measured with random bit pattern at a microprocessor system clock rate of 3.2 MHz which results in a memory cycle time of 2.5 μs. Power dissipation at other voltages and frequencies follows the relation



CDP1834
Functional Diagram



CDP1834
Timing Diagram

OPERATING AND HANDLING CONSIDERATIONS

1. **Handling**
   All inputs and outputs of RCA COS/MOS devices have a network for electrostatic protection during handling. Recommended handling practices for COS/MOS devices are described in ICAN-6525, "Guide to Better Handling and Operation of CMOS Integrated Circuits."
2. **Operating**

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause $V_{DD}-V_{SS}$ to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} nor less than V_{SS}. Input currents must not exceed 10 mA even when the power supply is off.

Unused Inputs

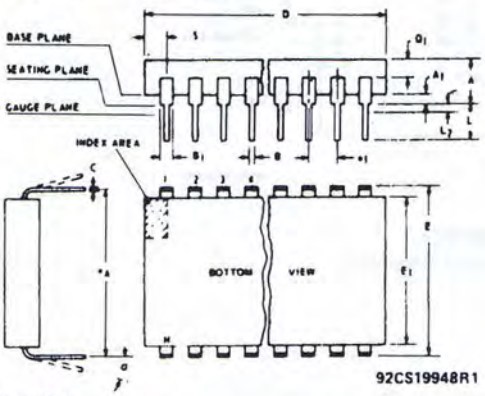
A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{DD} or V_{SS}, whichever is appropriate.

Output Short Circuits

Shorting of outputs to V_{DD} or V_{SS} may damage COS/MOS devices by exceeding the maximum device dissipation.

DIMENSIONAL OUTLINE

D SUFFIX
24-Lead Dual-In-Line Ceramic Package
JEDEC MO-015-AG



SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.090	0.150		2.29	3.81
A_1	0.020	0.065	2	0.51	1.65
B	0.015	0.020		0.381	0.508
B_1	0.045	0.055		1.143	1.397
C	0.008	0.012	1	0.204	0.304
D	1.15	1.22		29.21	30.98
E	0.600	0.625		15.24	15.87
E_1	0.480	0.520		12.20	13.20
e_1	0.100 TP		3	2.54 TP	
e_A	0.600 TP		3	15.24 TP	
L	0.100	0.180		2.54	4.57
L_2	0.000	0.030	3	0.00	0.76
α	0°	15°	4	0°	15°
N	24		5	24	
N_1	0		6	0	
Q_1	0.020	0.080		0.51	2.03
S	0.020	0.060		0.51	1.52

NOTES:

Refer to JEDEC Publication No. 95 for Rules for Dimensioning Axial Lead Product Outlines.

1. When this device is supplied solder dipped, the maximum lead thickness (narrow portion) will not exceed 0.013" (0.33 mm).
2. When base of body is to be attached to heat sink, terminal lead standoffs are not required and $A_1 = 0$. When $A_1 = 0$, the leads emerge from the body with the B_1 dimension and reduce to the B dimension above the seating plane.
3. e_1 and e_A apply in zone L_2 when unit is installed. Leads within 0.005 " (0.127 mm) radius of True Position (TP) at gauge plane with maximum material condition.
4. Applies to spread leads prior to installation.
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads.

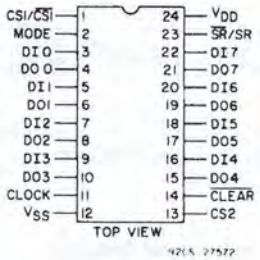
When incorporating RCA Solid State Devices in equipment, it is recommended that the designer refer to "Operating Considerations for RCA Solid State Devices", Form No. 1CE-402, available on request from RCA Solid State Division, Box 3200, Somerville, N. J. 08876.

RCA
Solid State Division

Microprocessor Products

Preliminary Data▲

CDP1852D
CDP1852CD



Terminal Assignment

8-Bit Input/Output Port

Features:

- **Static Silicon-Gate CMOS circuitry—CD4000-series compatible**
- **Compatible with CDP1800-series microprocessors at maximum speed**
- **Interfaces with CDP1802 microprocessor without additional components**
- **Single voltage supply**
- **Full military temperature range (−55°C to +125°C)**
- **Parallel 8-bit data register and buffer**
- **Flip-flop for service request**
- **Asynchronous register clear**
- **Low quiescent and operating power**

The RCA-CDP1852D and CDP1852CD are parallel, 8-bit, mode-programmable COS/MOS input/output ports designed for use in CDP-1800 series microprocessor systems. These input/output ports are compatible and will interface directly with the CDP1802 without additional components.

The mode control is used to program the device as an input port (mode=0) or output port (mode=1). If the CDP1852 is used as an input port (mode=0), data is strobed into the port's 8-bit register by a high (1) level on the clock line. The negative, high-to-low transition of the clock sets the Service Request Flip-Flop ($\overline{SR}$=0) and latches the data in the register. The $\overline{SR}$ output can be used to signal the microprocessor. When CS1·CS2=1 the three-state output drivers are enabled, the negative high-to-low transition of CS1·$\overline{CS2}$ resets the Service Request Flip-Flop, $\overline{SR}$=1.

If the CDP1852 is used as an output port (mode=1), data is strobed into the port's 8-bit register when $\overline{CS1}$·CS2·CLOCK=1. The three-state output drivers are enabled at all times when the CDP1852 is configured as an output port. The service request signal is generated at the termination of $\overline{CS1}$·CS2=1 and will be present, 1 level, until the following negative, high-to-low transition of the clock.

A $\overline{CLEAR}$ control is provided for resetting the port's register and service request flip-flop.

The CDP1852D is functionally identical to the CDP1852CD. The CDP1852D has a recommended operating voltage range of 3 to 12 volts, and the CDP1852CD has a recommended operating voltage range of 4 to 6 volts.

The CDP1852D and CDP1852CD are supplied in 24-lead, hermetic, dual-in-line ceramic packages.

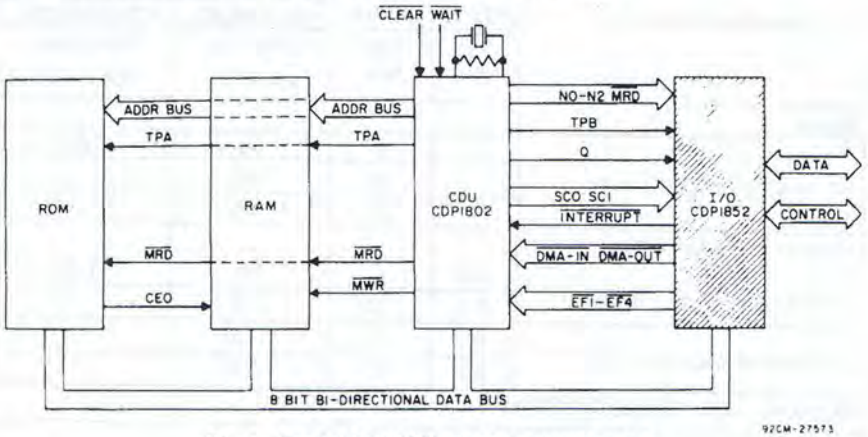


Fig. 1—Typical CDP1802 microprocessor system.

▲The Preliminary Data are intended for guidance purposes in evaluating the device for equipment design. The device is now being designed for inclusion in our standard line of commercially available products. For current information on the status of this program, please contact your RCA Sales Office.

Printed in USA/2-76

MAXIMUM RATINGS,
Absolute-Maximum Values

Storage-Temperature Range (T_{stg}) ..... −65 to +150°C

Operating-Temperature Range (T_A) ..... −55 to +125°C

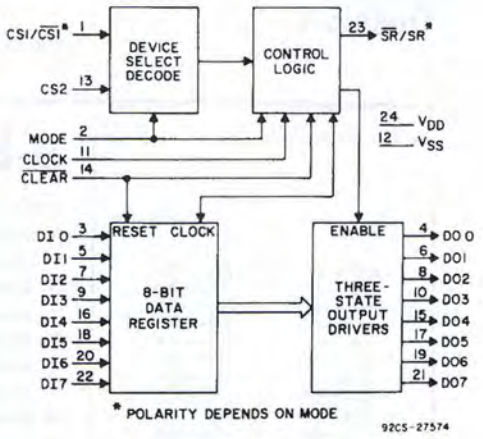
DC Supply-Voltage Range (V_{DD})
(All voltage values referenced to V_{SS} terminal)
- CDP1852D ..... −0.5 to +15 V
- CDP1852CD ..... −0.5 to +7 V

Power Dissipation Per Package (P_D):
- For T_A=−55 to +100°C ..... 500 mW
- For T_A=+100 to +125°C ..... Derate Linearly to 200 mW

Device Dissipation Per Output Transistor:
- For T_A=−55°C to +125°C ..... 100 mW

Input Voltage Range, All Inputs ..... −0.5 to V_{DD} +0.5 V

Lead Temperature (During Soldering):
- At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C



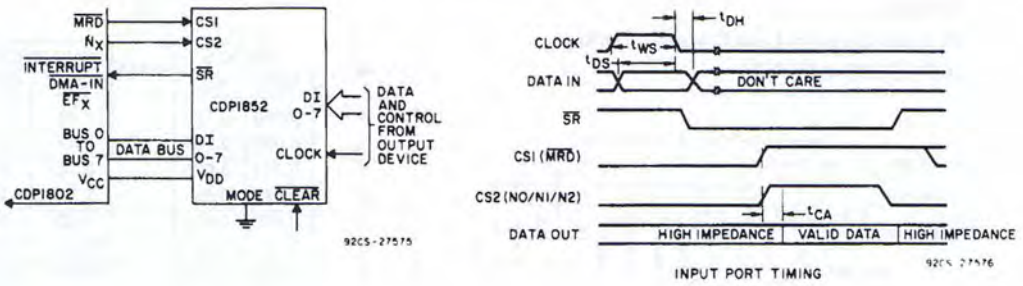
Functional Diagram

OPERATING CONDITIONS at T_A=25°C Unless Otherwise Specified
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	CONDITIONS V_{DD} (V)	LIMITS CDP1852D Min.	LIMITS CDP1852D Max.	LIMITS CDP1852CD Min.	LIMITS CDP1852CD Max.	UNITS
Supply-Voltage Range (At T_A=Full Package-Temperature Range)	–	3	12	4	6	V
Recommended Input Voltage Range	–	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V
		Typical		Typical		
Strobe Pulse Width, t_{WS}	5	200		200		ns
	10	100		–		
Data Setup Time, t_{DS}	5	0		0		ns
	10	0		–		
Data Hold Time, t_{DH}	5	100		100		ns
	10	50		–		

ELECTRICAL CHARACTERISTICS at T_A=25°C

CHARACTERISTIC	TEST CONDITIONS V_O (V)	TEST CONDITIONS V_{DD} (V)	LIMITS CDP1852D TYPICAL VALUES	LIMITS CDP1852CD TYPICAL VALUES	UNITS
Static					
Quiescent Device Current, I_L	–	5	50	100	μA
	–	10	100	–	
	–	15	500	–	
Output Drive Current:					mA
N-Channel (Sink), I_DN	0.4	5	1.6	1.6	
	0.5	10	3.6	–	
P-Channel (Source), I_DP	4.6	5	−1.6	−1.6	
	9.5	10	−3.6	–	
Dynamic: t_r, t_f=10 ns, C_L=50 pF					
Propagation Delay Times:					ns
Output from CS, t_{CA}	–	5	200	200	
	–	10	100	–	
Data to Output, t_{OD}	–	5	200	200	
	–	10	100	–	

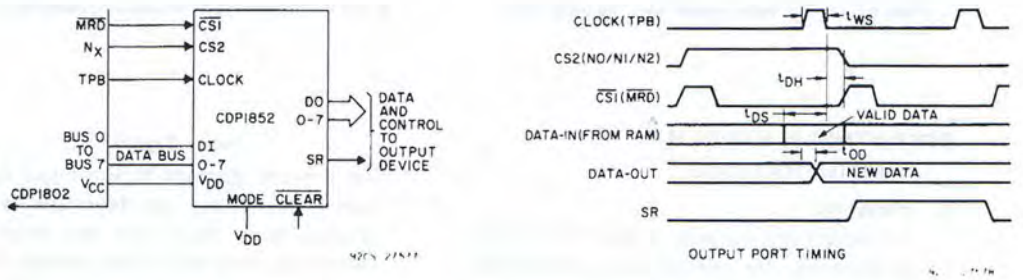


MODE = 0

CLOCK	CS1·CS2	$\overline{CLEAR}$	Data Out Equals
X	0	X	High-Impedance
0	1	0	0
0	1	1	Data Latch
1	1	X	Data In

$\overline{SR}$ = 0	$\overline{SR}$ = 1▲
CLOCK ↘	CS1·CS2 ↘ Or $\overline{CLEAR}$ ↘

Fig. 2—CDP1852 input port operation.



MODE = 1

CLOCK	$\overline{CS1}$·CS2	$\overline{CLEAR}$	Data Out Equals
0	X	0	0
0	X	1	Data Latch
X	0	1	Data Latch
1	1	X	Data In

SR = 1▲	SR = 0
$\overline{CS1}$·CS2 ↘	CLOCK ↘ Or $\overline{CLEAR}$ ↘

Fig. 3—CDP1852 output port operation.

Note:
The dynamic characteristics and timing diagrams indicate maximum performance capability of the CDP1852. When used directly with the CDP1802 microprocessor, timing will be determined by the clock frequency and internal delays of the microprocessor.

The following general timing relationships will hold when the CDP1852 is used as an output port with the CDP1802 microprocessor:

$$t_{WS}(TPB) = 1.0\ t_c$$

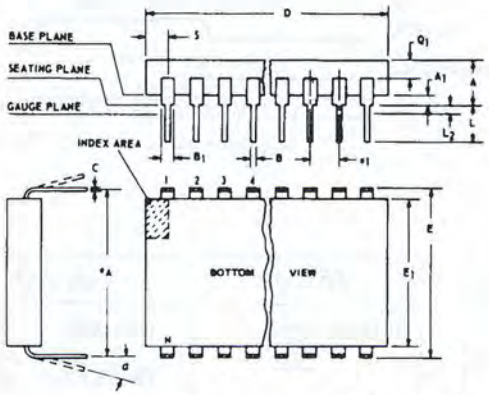
$$t_{DH} = 0.5\ t_c$$

$$t_c = \frac{1}{\text{CDP1802 clock frequency}}$$

▲ The service request flip-flop is placed in the "1" state by the termination of the I/O port selection, CS1·CS2 or $\overline{CS1}$·CS2. System implementations should be avoided which cause a transient selection of the port. The termination of the signal may improperly place the service request flip-flop in the "1" state. The transition used to set and reset $\overline{SR}$/SR may be positive or negative. The polarity will not affect circuit operation shown in Figs.2 and 3.

DIMENSIONAL OUTLINE

D Suffix
24-Lead Dual-In-Line Ceramic Package
JEDEC MO-015-AG



92CS-19948

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.090	0.150		2.29	3.81
A_1	0.020	0.065	2	0.51	1.65
B	0.015	0.020		0.381	0.508
B_1	0.045	0.055		1.143	1.397
C	0.008	0.012	1	0.204	0.304
D	1.15	1.22		29.21	30.98
E	0.600	0.625		15.24	15.87
E_1	0.480	0.520		12.20	13.20
e_1	0.100 TP		3	2.54 TP	
e_A	0.600 TP		3	15.24 TP	
L	0.100	0.180		2.54	4.57
L_2	0.000	0.030	3	0.00	0.76
α	0°	15°	4	0°	15°
N	24		5	24	
N_1	0		6	0	
Q_1	0.020	0.080		0.51	2.03
S	0.020	0.060		0.51	1.52

NOTES:

Refer to JEDEC Publication No. 13 for Rules for Dimensioning Axial Lead Product Outlines.

1. When this device is supplied solder dipped, the maximum lead thickness (narrow portion) will not exceed 0.013" (0.33 mm).
2. When base of body is to be attached to heat sink, terminal lead standoffs are not required and $A_1 = 0$. When $A_1 = 0$, the leads emerge from the body with the B_1 dimension and reduce to the B dimension above the seating plane.
3. e_1 and e_A apply in zone L_2 when unit is installed. Leads within 0.005 " (0.127 mm) radius of True Position (TP) at gauge plane with maximum material condition.
4. Applies to spread leads prior to installation.
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads.

OPERATING & HANDLING CONSIDERATIONS

1. Handling

All inputs and outputs of this device have a network for electrostatic protection during handling. Recommended handling practices for COS/MOS devices are described in ICAN-6000 "Handling and Operating Considerations for MOS Integrated Circuits".

2. Operating

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause V_{DD}-V_{SS} to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} nor less than V_{SS}. Input currents must not exceed 10 mA even when the power supply is off.

Unused Inputs

A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{DD} or V_{SS}, whichever is appropriate.

Output Short Circuits

Shorting of outputs to V_{DD} or V_{SS} may damage COS/MOS devices by exceeding the maximum device dissipation.

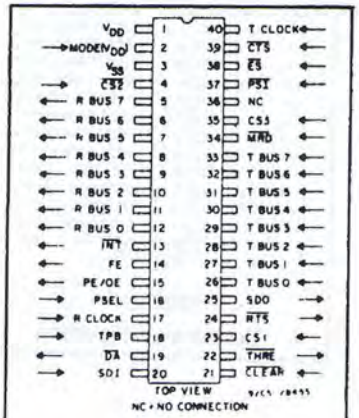
When Incorporating RCA Solid State Devices in equipment, it is recommended that the designer refer to "Operating Considerations for RCA Solid State Devices", Form No. 1CE-402, available on request from RCA Solid State Division, Box 3200, Somerville, N.J. 08876.

RCA
Solid State Division

Microprocessor Products

CDP1854D
CDP1854CD

Preliminary Data ▲



MODE 1
Terminal Assignment

CMOS Universal Asynchronous Receiver/Transmitter (UART)

Features:

- Static silicon-gate CMOS circuitry— CD4000 Series compatible
- Two operating modes:
  - Mode 0—functionally compatible with industry standard types such as the TR1602A
  - Mode 1—interfaces directly with the CDP1802 Microprocessor without additional components
- Full- or half-duplex operation
- Baud rate— DC to 200K baud @ V_{DD}=5 V
  DC to 400K baud @ V_{DD}=10 V
- Fully programmable with externally selectable word length (5-8 bits), parity inhibit, even/odd parity, and 1, 1½, or 2 stop bits
- False start bit detection
- Parity, framing, and overrun error detection
- Low quiescent and operating power
- Single-voltage supply
- Wide operating-voltage range
- Full military temperature range: −55 to +125°C

The CDP1854D and CDP1854CD are silicon-gate COS/MOS Universal Asynchronous Receiver/Transmitter (UART) circuits. They are designed to provide the necessary formatting and control for interfacing between serial and parallel data. For example, it can be used to interface between a peripheral or terminal with serial I/O ports and the 8-bit CDP1802 parallel data bus system. The CDP1854 is capable of full duplex operation, i.e., simultaneous conversion of serial input data to parallel output data and parallel input data to serial output data.

The CDP1854 UART can be programmed to operate in one of two modes by using the mode control input. When the mode input is high (MODE=1), the CDP1854 is directly compatible with the CDP1802 microprocessor system without additional interface circuitry.

When the mode input is low (MODE=0), the device is functionally compatible with industry standard UART's such as the TR1602A. It is also pin compatible with these types, except that pin 2 is used for the mode control input instead of a V_{GG}=−12 V supply connection.

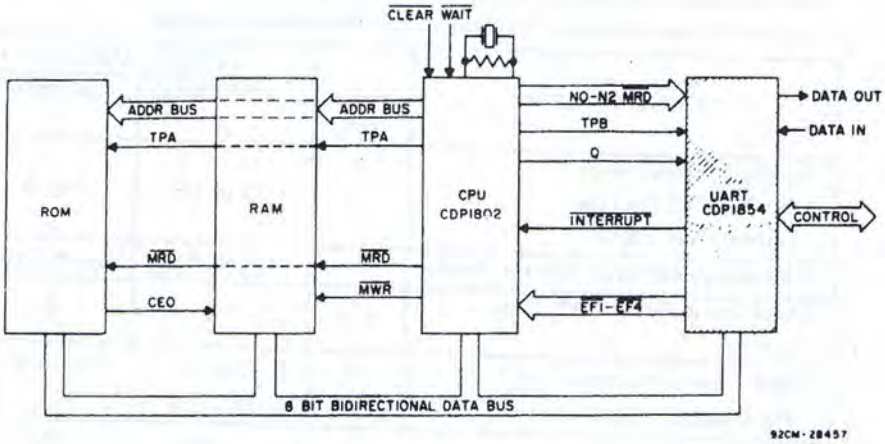


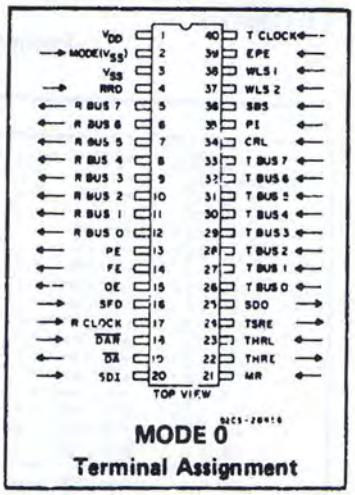
Fig. 1 — Typical CDP1802 microprocessor system.

▲ The Preliminary Data are intended for guidance purposes in evaluating the device for equipment design. The device is now being designed for inclusion in our standard line of commercially available products. For current information on the status of this program, please contact your RCA Sales Office.

Printed in USA/12-76

The CDP1854D and the CDP1854CD are functionally identical. The CDP1854D has a recommended operating-voltage range of 3-12 volts, and the CDP:854CD has a recommended operating-voltage range of 4-6 volts.

The CDP1854D, and CDP1854CD are supplied in hermetic 40-lead dual-in-line ceramic packages.



MODE 0
Terminal Assignment

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) ..... −65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A) ..... −55 to +125°C
DC SUPPLY-VOLTAGE RANGE (V_{DD})
(All voltage values referenced to V_{SS} terminal)
CDP1854D ..... −0.5 to +15 V
CDP1854CD ..... −0.5 to +7 V
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −55 to +100°C ..... 500 mW
For T_A = +100 to +125°C ..... Derate Linearly to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
For T_A = −55°C to +125°C ..... 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS ..... −0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm)
from case for 10 s max. ..... +265°C

RECOMMENDED OPERATING CONDITIONS at T_A=25°C Unless Otherwise Specified
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	V_{DD} (V)	TYPICAL VALUES		UNITS
		CDP1854D	CDP1854CD	
Supply-Voltage Range (At T_A=Full Package-Temperature Range)	–	3 to 12	4 to 6	V
Recommended Input Voltage Range	–	V_{SS} to V_{DD}	V_{SS} to V_{DD}	V
Clock Input Rise or Fall Time, t_r or t_f	3-15	5	5	μs
Clock Input Frequency, f_{CL} (16 times bit rate)	5 10	DC–3.2 DC–6.4	DC–3.2 –	MHz
Minimum Clock Pulse Width, t_{WL}, t_{WH}	5 10	150 75	150 –	ns
Minimum Master Reset, $\overline{CLEAR}$ Pulse Width	5 10	500 250	500 –	ns

ELECTRICAL CHARACTERISTICS at T_A=25°C

CHARACTERISTIC	CONDITIONS		TYPICAL VALUES		UNITS
	V_O (V)	V_{DD} (V)	CDP1854D	CDP1854CD	
Quiescent Device Current, I_L	–	5	100	500	μA
	–	10	500	–	
	–	15	1000	–	
Output Voltage: Low-Level, V_{OL}	–	5	0.01	0.01	V
	–	10	0.01	–	
High-Level, V_{OH}	–	5	5	5	
	–	10	10	–	
Noise Immunity: Inputs Low, V_{NL}	0.5	5	2.25	2.25	V
	1	10	3.45	–	
Inputs High, V_{NH}	4.5	5	2.25	2.25	
	9	10	3.45	–	
Output Drive Current: N-Channel (Sink), I_DN	0.4	5	0.4	0.4	mA
	0.5	10	0.9	–	
P-Channel (Source), I_DP	2.5	5	−1.6	−1.6	
	4.6	5	−0.4	−0.4	
	9.5	10	−0.9	–	
Input Leakage Current (Any Input), I_{IL}, I_{IH}	–	5	±1	±1	μA
	–	15	±1	–	
Total Power Dissipation (f_{CL}=3.2 MHz)	–	5	5	7	mW
	–	10	15	–	

STANDARD MODE 0 (See Fig. 2)

RECOMMENDED OPERATING CONDITIONS at T_A=25°C Unless Otherwise Specified

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	CONDITIONS	TYPICAL VALUES		UNITS
	V_{DD} (V)	CDP1854D	CDP1854CD	
Control Register Load (CRL) Pulse Width, t_{CLW}	5	200	200	ns
	10	150	–	
Transmitter Holding Register Load (THRL) Pulse Width, t_{TLW}	5	200	200	ns
	10	150	–	
Data Available Reset ($\overline{DAR}$) Pulse Width	5	200	200	ns
	10	150	–	
Input Data Setup Time, t_{DS}	5	150	150	ns
	10	75	–	
Input Data Hold Time, t_{DH}	5	150	150	ns
	10	75	–	
Control Input Overlap, t_{CLO} With CRL	5	200	200	ns
	10	100	–	
Control Input Hold Time, t_{CH}	5	100	100	ns
	10	50	–	

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=25°C, C_L=50 pF

CHARACTERISTIC	CONDITIONS	TYPICAL VALUES		UNITS
	V_{DD} (V)	CDP1854D	CDP1854CD	
Status Flag Disconnect, (SFD) to STATUS OUT Delay, t_{SS}	5	200	200	ns
	10	100	–	
Receiver Register Disconnect, (RRD) to DATA OUT Delay, t_{RDB}	5	200	200	ns
	10	100	–	

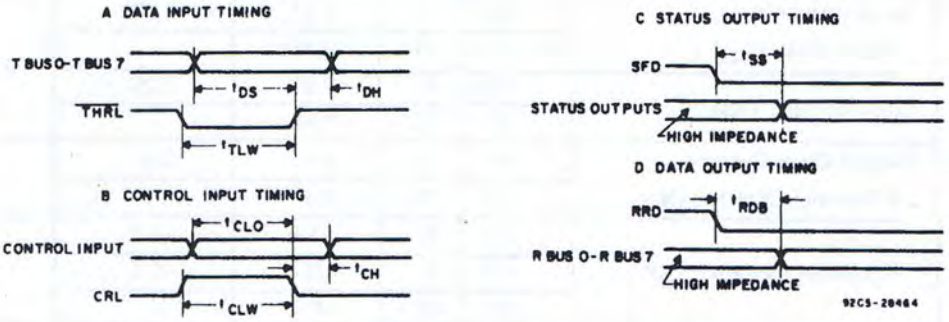


Fig. 2 – Standard Mode 0 timing diagrams.

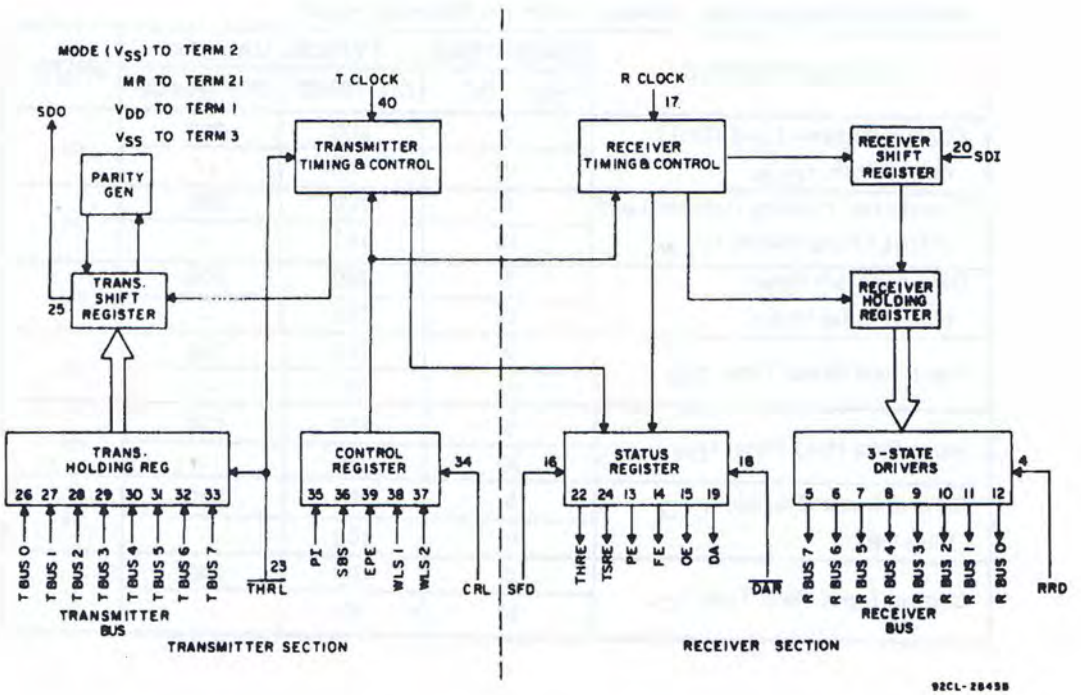


Fig. 3 – Standard Mode 0 block diagram.

Standard MODE 0 Operation (MODE Input = V_{SS})

1. Initialization and Controls

The MASTER RESET (MR) input is pulsed, resetting the Control, Status, and Receiver Holding Registers and setting the SERIAL DATA OUTPUT (SDO) signal high. Timing is generated from the clock inputs, Transmitter Clock (TCLOCK) and Receiver Clock (RCLOCK), at a frequency equal to 16 times the serial data bit rate. When the receiver data input rate and the transmitter data output rate are the same, the TCLOCK and RCLOCK inputs may be connected together. The CONTROL REGISTER LOAD (CRL) input is pulsed to store the control inputs PARITY INHIBIT (PI), EVEN PARITY ENABLE (EPE), STOP BIT SELECT (SBS), and WORD LENGTH SELECTs (WLS1 and WLS2). These inputs may be hardwired to the proper voltage levels (V_{SS} or V_{DD}) instead of being dynamically set and CRL may be hardwired to V_{DD}. The CDP1854 is then ready for transmitter and/or receiver operation.

2. Transmitter Operation

For the transmitter timing diagram refer to Fig. 4. At the beginning of a typical transmitting sequence the Transmitter Holding Register is empty (THRE is HIGH). A character is transferred from the transmitter bus to the Transmitter Holding Register by applying a low pulse to the TRANSMITTER HOLDING REGISTER LOAD ($\overline{THRL}$) input causing THRE to go low. If the Transmitter Shift Register is empty (TSRE is HIGH) and the clock is low, on the next high-to-low transition of the clock the character is loaded into the Transmitter Shift Register preceded by a start bit. Serial data transmission begins ½ clock period later with a start bit and 5-8 data bits followed by the parity bit (if programmed) and stop bit(s). The THRE output signal goes high ½ clock period later on the high-to-low transition of the clock. When THRE goes high, another character can be loaded into the Transmitter Holding Register for transmission beginning with a start bit immediately following the last stop bit of the previous character. This process is repeated until all characters have been transmitted. When transmission is complete, THRE and Transmitter Shift Register Empty (TSRE) will both be high. The format of serial data is shown in Fig. 5. Duration of each serial output data bit is determined by the transmitter clock frequency (f_{CLOCK}) and will be 16/f_{CLOCK}.

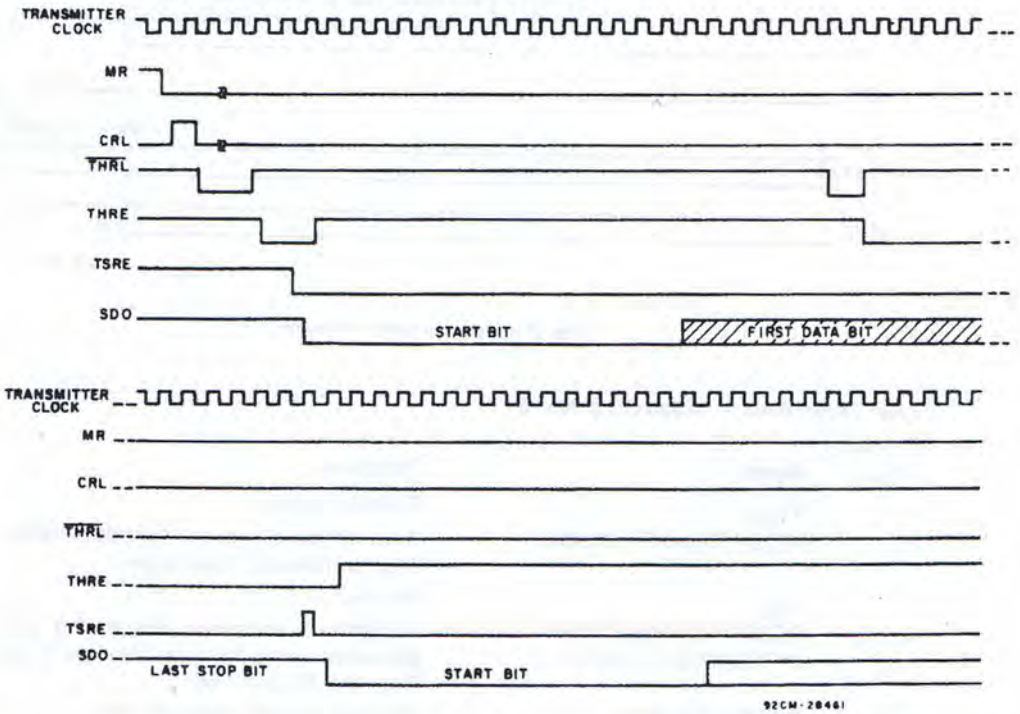


Fig. 4 – Transmitter timing diagram.

3. Receiver Operation

The receive operation begins when a start bit is detected at the SERIAL DATA IN (SDI) input. After the detection of a high-to-low transition on the SDI line, a divide-by-16 counter is enabled and a valid start bit is verified by checking for a low-level input 6½ receiver clock periods later. When a valid start bit has been verified, the following data bits, parity bit (if programmed), and stop bit(s) are shifted into the Receiver Shift Register at clock pulse 6½ in each bit time. If programmed, the parity bit is checked, and receipt of a valid stop bit is verified. On

count 6½ of the first stop bit, the received data is loaded into the Receiver Holding Register. If the word length is less than 8 bits, zeros (low output voltage level) are loaded into the unused left-most bits. If DATA AVAILABLE (DA) has not been reset by the time the Receiver Holding Register is loaded, the OVERRUN ERROR (OE) signal is raised. One-half clock period later, the PARITY ERROR (PE) and FRAMING ERROR (FE) signals become valid for the character in the Receiver Holding Register. The DA signal is also raised at this time. The 3-state output drivers for DA, OE, PE and FE are enabled when STATUS FLAG DISCONNECT (SFD) is low. When RECEIVER REGISTER DISCONNECT (RRD) goes low, the receiver bus 3-state output drivers are enabled and data is available at the RECEIVER BUS (R BUS 0-R BUS 7) outputs. Applying a negative pulse to the DATA AVAILABLE RESET ($\overline{DAR}$) resets DA. The preceding sequence of operation is repeated for each serial character received. A receiver timing diagram is shown in Fig. 6.

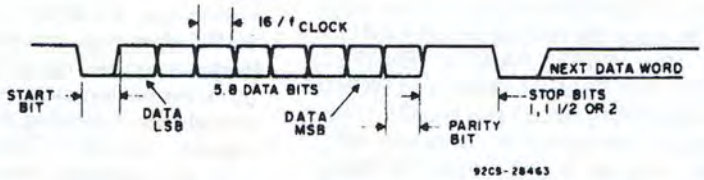


Fig. 5 – Serial data word format.

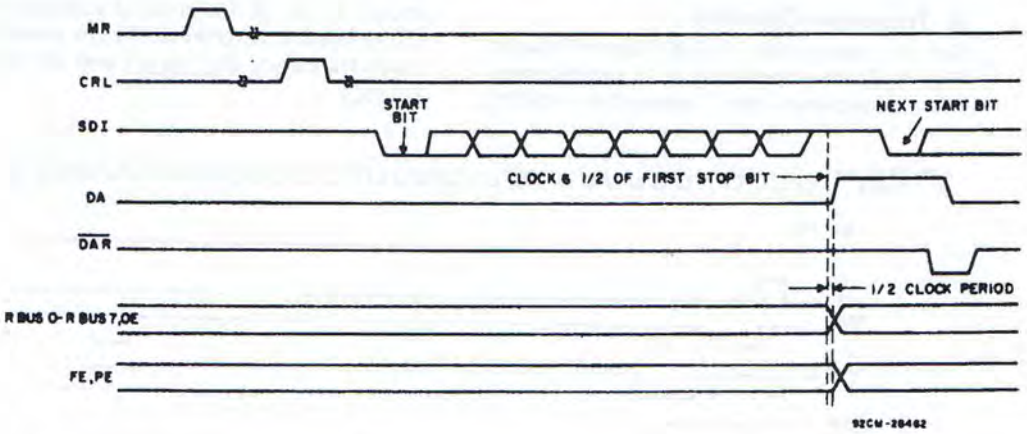


Fig. 6 – Receiver timing diagram

Signal Definitions – Standard Mode 0

Terminal No.	Signal	Function
1	V_{DD}	Positive supply
2	MODE SELECT (MODE)	A low-level voltage at this input selects Standard Mode 0 Operation.
3	V_{SS}	Ground
4	RECEIVER REGISTER DISCONNECT (RRD)	A high-level voltage applied to this input disconnects the Receiver Holding Register from the Receiver Bus.
5-12	RECEIVER BUS (R BUS 7 - R BUS 0)	Receiver parallel data outputs
13	PARITY ERROR (PE)	A high-level voltage at this output indicates that the received parity does not compare to that programmed by the EVEN PARITY ENABLE (EPE) control. This output is updated each time a character is transferred to the Receiver Holding Register. PE lines from a number of arrays can be bused together since an output disconnect capability is provided by the STATUS FLAG DISCONNECT (SFD) line.

14	FRAMING ERROR (FE)	A high-level voltage at this output indicates that the received character has no valid stop bit, i.e., the bit following the parity bit (if programmed) is not a high-level voltage. This output is updated each time a character is transferred to the Receiver Holding Register. FE lines from a number of arrays can be bused together since an output disconnect capability is provided by the STATUS FLAG DISCONNECT (SFD) line.
15	OVERRUN ERROR (OE)	A high-level voltage at this output indicates that the DATA AVAILABLE (DA) flag was not reset before the next character was transferred to the Receiver Holding Register. OE lines from a number of arrays can be bused together since an output disconnect capability is provided by the STATUS FLAG DISCONNECT (SFD) line.
16	STATUS FLAG DISCONNECT (SFD)	A high-level voltage applied to this input disables the 3-state output drivers for PE, FE, OE, DA, and THRE, allowing these status outputs to be bus connected.
17	RECEIVER CLOCK (RCLOCK)	Clock input with a frequency 16 times the desired receiver shift rate.
18	DATA AVAILABLE RESET ($\overline{\text{DAR}}$)	A low-level voltage applied to this input resets the DA flip-flop.
19	DATA AVAILABLE (DA)	A high-level voltage at this output indicates that an entire character has been received and transferred to the Receiver Holding Register.
20	SERIAL DATA IN (SDI)	Serial data received at this input enters the receiver shift register at a point determined by the character length. A high-level voltage must be present when data is not being received.
21	MASTER RESET (MR)	A high-level voltage at this input resets the Receiver Holding Register, Control Register, and Status Register, and sets the serial data output high.
22	TRANSMITTER HOLDING REGISTER EMPTY (THRE)	A high-level voltage at this output indicates that the Transmitter Holding Register has transferred its contents to the Transmitter Shift Register and may be reloaded with a new character.
23	TRANSMITTER HOLDING REGISTER LOAD ($\overline{\text{THRL}}$)	A low-level voltage applied to this input enters the character on the bus into the Transmitter Holding Register. Data is latched on the trailing edge of this signal.
24	TRANSMITTER SHIFT REGISTER EMPTY (TSRE)	A high-level voltage at this output indicates that the Transmitter Shift Register has completed serial transmission of a full character including stop bit(s). It remains at this level until the start of transmission of the next character.
25	SERIAL DATA OUTPUT (SDO)	The contents of the Transmitter Shift Register (start bit, data bits, parity bit, and stop bit(s)) are serially shifted out on this output. When no character is being transmitted, a high-level is maintained. Start of transmission is defined as the transition of the start bit from a high-level to a low-level output voltage.
26-33	TRANSMITTER BUS (T BUS 0 - T BUS 7)	Transmitter parallel data inputs
34	CONTROL REGISTER LOAD (CRL)	A high-level voltage at this input loads the Control Register with the control bits (PI, EPE, SBS, WLS1, WLS2). This line may be strobed or hardwired to a high-level input voltage.

35	PARITY INHIBIT (PI)	A high-level voltage at this input inhibits the parity generation and verification circuits and will clamp the PE output low. If parity is inhibited the stop bit(s) will immediately follow the last data bit on transmission.
36	STOP BIT SELECT (SBS)	This input selects the number of stop bits to be transmitted after the parity bit. A high-level selects two stop bits, a low-level selects one stop bit. Selection of two stop bits with five data bits programmed selects 1.5 stop bits.
37	WORD LENGTH SELECT 2 (WLS2)	These two inputs select the character length (exclusive of parity) as follows:
38	WORD LENGTH SELECT 1 (WLS1)	
39	EVEN PARITY ENABLE (EPE)	A high-level voltage at this input selects even parity to be generated by the transmitter and checked by the receiver. A low-level input selects odd parity.
40	TRANSMITTER CLOCK (TCLOCK)	Clock input with a frequency 16 times the desired transmitter shift rate.

WLS2	WLS1	Word Length
Low	Low	5 Bits
Low	High	6 Bits
High	Low	7 Bits
High	High	8 Bits

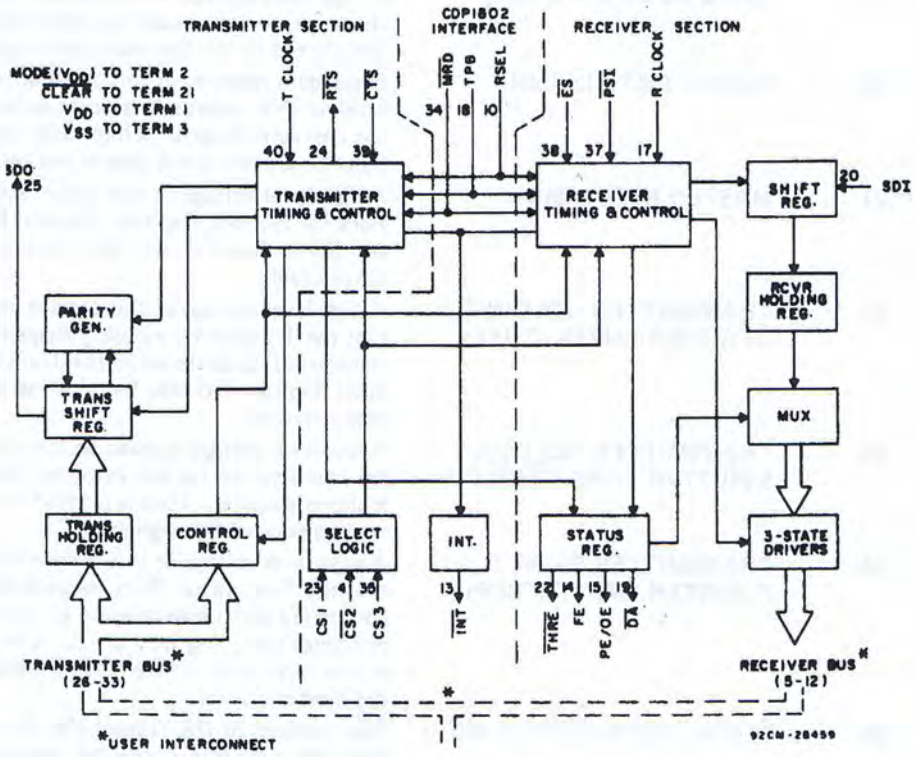


Fig. 7 – MODE 1 block diagram (CDP1802 compatible).

CDP1802 Compatible MODE 1 Operation (MODE Input = V_{DD})

1. Initialization and Controls

In the CDP1802 compatible mode, the CDP-1854 is configured to receive commands and send status via the microprocessor data bus. The register connected to the transmitter bus or the receiver bus is determined by the MRD and RSEL inputs as follows:

RSEL	$\overline{MRD}$	Function
Low	Low	Load Transmitter Holding Register from Transmitter Bus
Low	High	Read Receiver Holding Register from Receiver Bus
High	Low	Load Control Register from Transmitter Bus
High	High	Read Status Register from Receiver Bus

In this mode the CDP1854 is compatible with a bidirectional bus system. The receiver and transmitter buses are connected to the bus. CDP1802 I/O control output signals can be connected directly to the CDP1854 inputs as shown in Fig. 8. The CLEAR input is pulsed, resetting the Control, Status, and Receiver Holding Registers and setting SERIAL DATA OUT (SDO) high. The Control Register is loaded from the Transmitter Bus in order to determine the operating configuration for the UART. Data is transferred from the Transmitter Bus inputs to the Control Register during TPB when the UART is selected (CS1 · $\overline{CS2}$ · CS3) and the Control Register is designated (RSEL = H, $\overline{MRD}$ = L). The CDP1854 also has a Status Register which can be read onto the Receiver Bus (R BUS 0-R BUS 7) in order to determine the status of the UART. Some of these status bits are also available at separate terminals as indicated in Fig. 10.

2. Transmitter Operation

Before beginning to transmit, the TRANSMIT REQUEST (TR) bit in the Control Register (see bit assignment, page 10) must be set. This setting is done by executing the same operation used to load the Control Register except that the TR bit must be set (TR=1) in the byte transmitted via the bus. When TR has been set, a TRANSMITTER HOLDING REGISTER EMPTY (THRE) interrupt will occur, signalling the microprocessor that the Transmitter Holding Register is empty and may be loaded. Setting TR also causes assertion of a low-level on the REQUEST TO SEND ($\overline{RTS}$) output to the peripheral. The Transmitter Holding Register is loaded from the bus by TPB during execution of an output instruction. The CDP1854 is selected by CS1 · $\overline{CS2}$ · CS3 = 1, and the Holding Register is selected by RSEL = low and $\overline{MRD}$ = low. When the $\overline{CLEAR\ TO\ SEND}$ ($\overline{CTS}$) input, which can be connected to a peripheral device output, goes low, the Transmitter Shift Register will be loaded from the Transmitter Holding Register and data transmission will begin. If $\overline{CTS}$ is always low, the Transmitter Shift Register will be loaded on the first high-to-low edge of the clock which occurs at least ½ clock period after the trailing edge of TPB and transmission of a start bit will occur ½ clock period later (see Fig. 4). Parity (if programmed) and stop bit(s) will be transmitted following the last data bit.

One transmitter clock period after the Transmitter Shift Register is loaded from the Transmitter Holding Register, the $\overline{THRE}$ signal will go low and an interrupt will occur ($\overline{INT}$ goes low). The next character to be transmitted can then be loaded into the Transmitter Holding Register for transmission with its start bit immediately following the last stop bit of the previous character. This cycle can be repeated until the last character is transmitted, at which time a final THRE · TSRE interrupt will occur. This interrupt signals the microprocessor that TR can be turned off. This is done by reloading the original control byte in the Control Register with the TR bit = 0, thus terminating the $\overline{REQUEST\ TO\ SEND}$ ($\overline{RTS}$) signal.

SERIAL DATA OUT (SDO) can be held low by setting the BREAK bit in the Control Register (see Fig. 9). SDO is held low until the BREAK bit is reset.

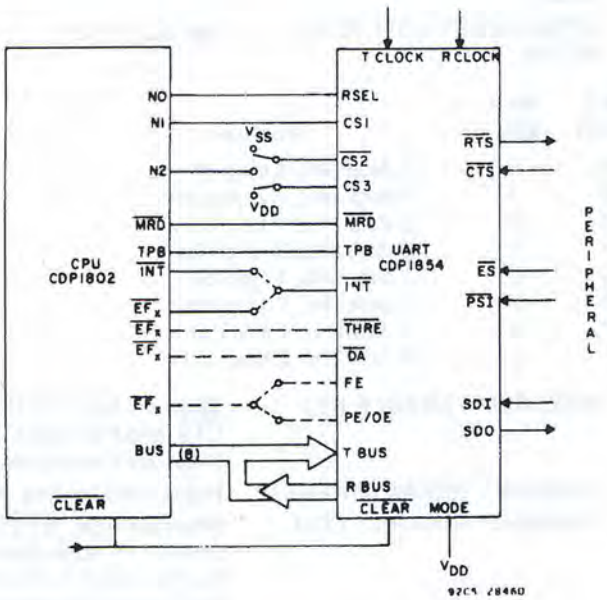


Fig. 8 – CDP1802/CDP1854 connection diagram.

3. Receiver Operation

The receive operation begins when a start bit is detected at the SERIAL DATA IN (SDI) input. After detection of the first high-to-low transition on the SDI line, a valid start bit is verified by checking for a low-level input 6½ receiver clock periods later. When a valid start bit has been verified, the following data bits, parity bit (if programmed) and stop bit(s) are shifted into the Receiver Shift Register by clock pulse 6½ in each bit time. The parity bit (if programmed) is checked and receipt of a valid stop bit is verified. On count 6½ of the first stop bit, the received data is loaded into the Receiver Holding Register. If the word length is less than 8 bits, zeros (low output level) are loaded into the unused left-most bits. If DATA AVAILABLE (DA) has not been reset by the time the Receiver Holding Register is loaded, the OVERRUN ERROR (OE) status bit is set. One half clock period later, the PARITY ERROR (PE) and FRAMING ERROR (FE) status bits become valid for the character in the Receiver Holding Register. At this time, the Data Available status bit is also set and the DATA AVAILABLE (DA) and INTERRUPT (INT) outputs go low, signalling the microprocessor that a received character is ready. The microprocessor responds by executing an input instruction. The UART's 3-state bus drivers are enabled when the UART is selected (CS1 · $\overline{CS2}$ · CS3 = 1) and $\overline{MRD}$ = high. Status can be read when RSEL = high. Data is read when RSEL = low. When reading data, TPB latches data in the microprocessor and resets DATA AVAILABLE (DA) in the UART. The preceding sequence is repeated for each serial character which is received from the peripheral.

Bit	7	6	5	4	3	2	1	0
Signal	TR	BREAK	IE	WLS2	WLS1	SBS	EPE	PI

Control Register Bit Assignment

Bit	Signal	Function
0	PARITY INHIBIT (PI)	When set high parity generation and verification are inhibited and the PE Status bit is held low. If parity is inhibited the stop bit(s) will immediately follow the last data bit on transmission, and EPE is ignored.
1	EVEN PARITY ENABLE (EPE)	When set high, even parity is generated by the transmitter and checked by the receiver. When low, odd parity is selected.
2	STOP BIT SELECT (SBS)	See table below.
3	WORD LENGTH SELECT 1 (WLS1)	See table below.
4	WORD LENGTH SELECT 2 (WLS2)	See table below.

Bit 4 WLS2	Bit 3 WLS1	Bit 2 SBS	Function
0	0	0	5 data bits, 1 stop bit
0	0	1	5 data bits, 1.5 stop bits
0	1	0	6 data bits, 1 stop bit
0	1	1	6 data bits, 2 stop bits
1	0	0	7 data bits, 1 stop bit
1	0	1	7 data bits, 2 stop bits
1	1	0	8 data bits, 1 stop bit
1	1	1	8 data bits, 2 stop bits

5	INTERRUPT ENABLE (IE)	When set high THRE, DA, THRE · TSRE, $\overline{CTS}$, and PSI interrupts are enabled (see Interrupt Conditions table, Fig. 11).
6	TRANSMIT BREAK (BREAK)	Holds SDO spacing (low) when set.
7	TRANSMIT REQUEST (TR)	When set high, $\overline{RTS}$ is set low and data transfer through the transmitter is initiated by the initial THRE interrupt. (When loading the Control Register from the bus, this (TR) bit inhibits changing of other control flip-flops.)

Fig. 9 – Control Register bit assignment.

Peripheral Interface

In addition to serial data in and out, four signals are provided for communication with a peripheral. The REQUEST TO SEND ($\overline{RTS}$) output signal alerts the peripheral to get ready to receive data. The CLEAR TO SEND ($\overline{CTS}$) input signal is the response, signalling that the peripheral is ready. The EXTERNAL STATUS ($\overline{ES}$) input latches a peripheral status level, and the PERIPHERAL STATUS INTERRUPT ($\overline{PSI}$) input senses a status edge (high-to-low) and also generates an interrupt. For example, the modem DATA CARRIER DETECT line could be connected to the $\overline{PSI}$ input on the UART in order to signal the microprocessor that transmission failed because of loss of the carrier on the communications line. The PSI and ES bits are stored in the Status Register (see Fig. 10).

Bit	7	6	5	4	3	2	1	0
Signal	THRE	TSRE	PSI	ES	FE	PE	OE	DA
Also Available at Terminal	22*	–	–	–	14	15	15	19*

* Polarity reversed at output terminal.

Status Register Bit Assignment Table

Bit	Signal	Function
0	DATA AVAILABLE (DA)	When set high, this bit indicates that an entire character has been received and transferred to the Receiver Holding Register. This signal is also available at Term.19 but with its polarity reversed.
1	OVERRUN ERROR (OE)	When set high, this bit indicates that the Data Available bit was not reset before the next character was transferred to the Receiver Holding Register. This signal OR'ed with PE is output at Term.15.
2	PARITY ERROR (PE)	When set high, this bit indicates that the received parity bit does not compare to that programmed by the EVEN PARITY ENABLE (EPE) control. This bit is updated each time a character is transferred to the Receiver Holding Register. This signal OR'ed with OE is output at Term.15.
3	FRAMING ERROR (FE)	When set high, this bit indicates that the received character has no valid stop bit, i.e., the bit following the parity bit (if programmed) is not a high-level voltage. This bit is updated each time a character is transferred to the Receiver Holding Register. This signal is also available at Term.14.
4	EXTERNAL STATUS (ES)	This bit is set high by a low-level input at Term.38 ($\overline{ES}$).
5	PERIPHERAL STATUS INTERRUPT (PSI)	This bit is set high by a high-to-low voltage transition at Term.37 ($\overline{PSI}$). The INTERRUPT output (Term.13) is also asserted ($\overline{INT}$ = low) when this bit is set.
6	TRANSMITTER SHIFT REGISTER EMPTY (TSRE)	When set high, this bit indicates that the Transmitter Shift Register has completed serial transmission of a full character including stop bit(s). It remains set until the start of transmission of the next character.
7	TRANSMITTER HOLDING REGISTER EMPTY (THRE)	When set high, this bit indicates that the Transmitter Holding Register has transferred its contents to the Transmitter Shift Register and may be reloaded with a new character. Setting this bit also resets the $\overline{THRE}$ output (Term.22) low and causes an INTERRUPT ($\overline{INT}$ = low).

Fig. 10 – Status Register bit assignment.

SET* ($\overline{INT}$ = LOW)	RESET ($\overline{INT}$ = HIGH)	
CAUSE	CONDITION	TIME
DA (Receipt of data)	Read of data	TPB leading edge
THRE▲ (Ability to reload)	Read of status or write of character	TPB leading edge
THRE · TSRE (Transmitter done)	Read of status or write of character	TPB leading edge
$\overline{PSI}$ (Negative edge)	Read of status	TPB trailing edge
$\overline{CTS}$ (Positive edge when $\overline{THRE \cdot TSRE}$)	Read of status	TPB leading edge

* Interrupts will occur only after the IE bit in the Control Register (see Fig. 9) has been set.

▲ THRE will cause an interrupt only after the TR bit in the Control Register (see Fig. 9) has been set.

Fig. 11 – Interrupt conditions.

Signal Definitions – CDP1802 Compatible Mode 1

Terminal No.	Signal	Function
1	V_{DD}	Positive supply
2	MODE SELECT (MODE)	A high-level voltage at this input selects CDP1802 Mode operation.
3	V_{SS}	Ground
4	$\overline{CHIP\ SELECT\ 2}$ ($\overline{CS2}$)	A low-level voltage at this input together with CS1 and CS3 selects the CDP1854 UART.
5-12	RECEIVER BUS (R BUS 7 - R BUS 0)	Receiver parallel data outputs (may be externally connected to corresponding transmitter bus terminals).
13	$\overline{INTERRUPT}$ ($\overline{INT}$)	A low-level voltage at this output indicates the presence of one or more of the interrupt conditions listed in Fig. 11.
14	FRAMING ERROR (FE)	A high-level voltage at this output indicates that the received character has no valid stop bit, i.e., the bit following the parity bit (if programmed) is not a high-level voltage. This output is updated each time a character is transferred to the Receiver Holding Register.
15	PARITY ERROR or OVERRUN ERROR (PE/OE)	A high-level voltage at this output indicates that either the PE or OE bit in the Status Register has been set (see Status Register Bit Assignment, Fig. 10).
16	REGISTER SELECT (RSEL)	This input is used to choose either the Control/Status Registers (high input) or the transmitter/receiver data registers (low input) according to the truth table on page 8.
17	RECEIVER CLOCK (RCLOCK)	Clock input with a frequency 16 times the desired receiver shift rate.
18	TPB	A positive input pulse used as a data load or reset strobe.
19	$\overline{DATA\ AVAILABLE}$ ($\overline{DA}$)	A low-level voltage at this output indicates that an entire character has been received and transferred to the Receiver Holding Register.
20	SERIAL DATA IN (SDI)	Serial data received on this input line enters the Receiver Shift Register at a point determined by the character length. A high-level input voltage must be present when data is not being received.

21	$\overline{\text{CLEAR}}$ ($\overline{\text{CLEAR}}$)	A low-level voltage at this input resets the Receiver Holding Register, Control Register, and Status Register, and sets SERIAL DATA OUT (SDO) high.
22	$\overline{\text{TRANSMITTER HOLDING REGISTER EMPTY}}$ ($\overline{\text{THRE}}$)	A low-level voltage at this output indicates that the Transmitter Holding Register has transferred its contents to the Transmitter Shift Register and may be reloaded with a new character.
23	CHIP SELECT 1 (CS1)	A high-level voltage at this input together with $\overline{\text{CS2}}$ and CS3 selects the UART.
24	$\overline{\text{REQUEST TO SEND}}$ ($\overline{\text{RTS}}$)	This output signal tells the peripheral to get ready to receive data. $\overline{\text{CLEAR TO SEND}}$ ($\overline{\text{CTS}}$) is the response from the peripheral. $\overline{\text{RTS}}$ is set to a low-level voltage when data is latched in the Transmitter Holding Register and reset high when both the Transmitter Holding Register and Transmitter Shift Register are empty and TR is low.
25	SERIAL DATA OUTPUT (SDO)	The contents of the Transmitter Shift Register (start bit, data bits, parity bit, and stop bit(s) are serially shifted out on this output. When no character is being transmitted, a high level is maintained. Start of transmission is defined as the transition of the start bit from a high-level to a low-level output voltage.
26-33	TRANSMITTER BUS (T BUS 0 - T BUS 7)	Transmitter parallel data inputs. These may be externally connected to corresponding Receiver bus terminals.
34	$\overline{\text{MRD}}$	A low-level voltage at this input gates data from the bus to the Transmitter Holding Register or the Control Register as chosen by register select. A high-level voltage gates data from the Receiver Holding Register or the Status Register, as chosen by register select, to the bus.
35	CHIP SELECT 3 (CS3)	With high-level voltage at this input together with CS1 and $\overline{\text{CS2}}$ selects the UART.
36	No Connection	
37	$\overline{\text{PERIPHERAL STATUS INTERRUPT}}$ (PSI)	A high-to-low transition on this input line sets a bit in the Status Register and causes an $\overline{\text{INTERRUPT}}$ ($\overline{\text{INT}}$ = low).
38	$\overline{\text{EXTERNAL STATUS}}$ ($\overline{\text{ES}}$)	A low-level voltage at this input sets a bit in the Status Register.
39	$\overline{\text{CLEAR TO SEND}}$ ($\overline{\text{CTS}}$)	When this input from peripheral is high, transfer of a character to the Transmitter Shift Register and shifting of serial data out is inhibited.
40	TRANSMITTER CLOCK (TCLOCK)	Clock input with a frequency 16 times the desired transmitter shift rate.

OPERATING AND HANDLING CONSIDERATIONS FOR CDP1854D AND CDP1854CD

OPERATING AND HANDLING CONSIDERATIONS

1. Handling

All inputs and outputs of these devices have a network for electrostatic protection during handling. Recommended handling practices for COS/MOS devices are described in ICAN-6525 "Guide to Better Handling and Operation of CMOS Integrated Circuits".

2. Operating

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause $V_{DD}-V_{SS}$ to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} nor less than V_{SS}. Input currents must not exceed 10 mA even when the power supply is off.

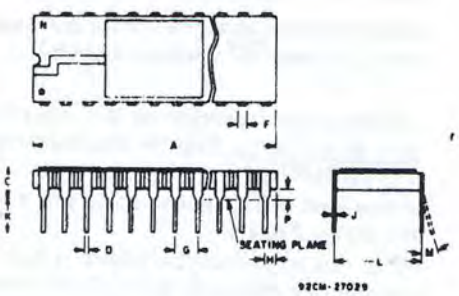
Unused Inputs

A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{DD} or V_{SS}, whichever is appropriate.

Output Short Circuits

Shorting of outputs to V_{DD} or V_{SS} may damage COS/MOS devices by exceeding the maximum device dissipation.

CDP1854D, CDP1854CD
40-Lead Side-Brazed Dual-In-Line Ceramic



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	50.30	51.30	1.980	2.020
C	2.42	3.93	0.095	0.155
D	0.43	0.56	0.017	0.023
F	1.27 REF.		0.050 REF.	
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.30	0.008	0.012
K	3.18	4.45	0.125	0.175
L	14.74	15.74	0.580	0.620
M	–	7°	–	7°
P	0.64	1.27	0.025	0.050
N	40		40	

NOTES:
1. Leads within 0.13 mm (0.005) radius of true position at maximum material condition.
2. Dimension "L" to center of leads when formed parallel.
3. When this device is supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013 in. (0.33 mm).

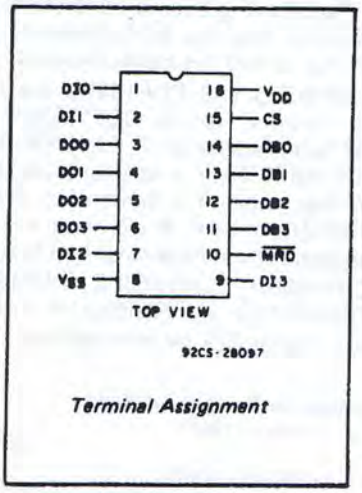
When incorporating RCA Solid State Devices in equipment, it is recommended that the designer refer to "Operating Considerations for RCA Solid State Devices", Form No. 1CE-402, available on request from RCA Solid State Division, Box 3200, Somerville, N. J. 08876.

RCA
Solid State Division

Microprocessor Products

CDP1856D CDP1857D
CDP1856CD CDP1857CD

Preliminary Data▲



Terminal Assignment

4-Bit Bus Buffers/Separators

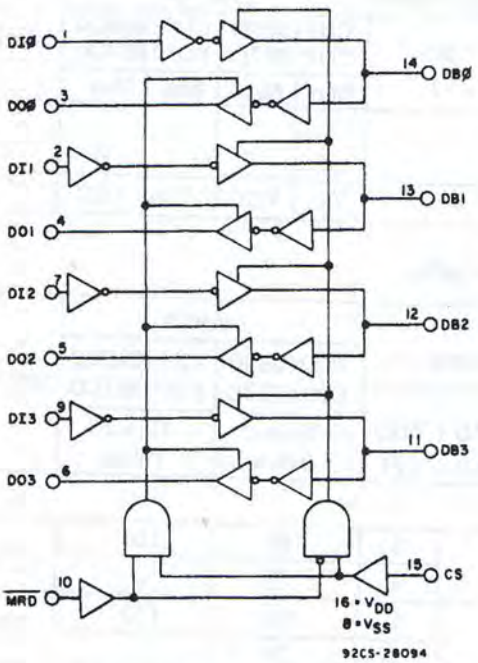
Features:

- **Static Silicon-Gate CMOS circuitry — CD4000-series compatible**
- **Compatible with CDP1800-series microprocessors at maximum speed**
- **Provides easy connection of memory and I/O devices to CDP1802 microprocessor data bus.**
- **Single voltage supply**
- **Full military-temperature range (−55°C to +125°C)**
- **Low quiescent and operating power**
- **Non-inverting fully buffered data transfer**

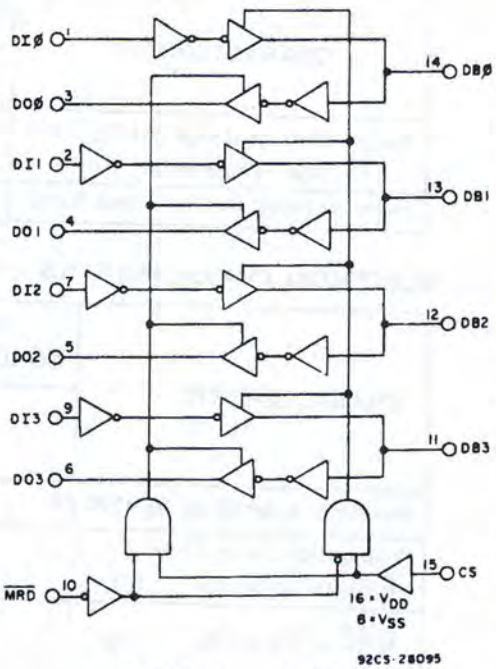
The RCA-CDP1856D, CDP1856CD, CDP-1857D, and CDP1857CD are 4-bit COS/MOS non-inverting bus separators designed for use in CDP1800-series microprocessor systems. They can be controlled directly by the CDP1802 microprocessor without the use of additional components.

The CDP1856 is designed for use as a bus buffer or separator between the CDP1802 data bus and memories. The CDP1857 is designed for use as a bus buffer or separator between the CDP1802 data bus and I/O devices. Both types provide a chip-select (CS) input signal which, when high (1), enables the bus-separator three-state output drivers. The direction of data flow, when enabled, is controlled by the MRD input signal.

In the CDP1856, when the $\overline{MRD}$ signal = 0 (low), it enables the three-state bus drivers (DB0 – DB3) and outputs data from the DATA-IN terminals to the data bus. When $\overline{MRD}$ = 1 (high), it disables the three-state



CDP1856 – Functional Diagram



CDP1857 – Functional Diagram

CDP1856, CDP1857 4-Bit Bus Buffers/Separators

▲The Preliminary Data are intended for guidance purposes in evaluating the device for equipment design. The device is now being designed for inclusion in our standard line of commercially available products. For current information on the status of this program, please contact your RCA Sales Office.

Printed in USA/10-76

bus drivers and enables the three-state data output drivers (DO0-DO3), thus transferring data from the data bus to the DATA-OUT terminals.

In the CDP1857, when $\overline{MRD}$ = 1, it enables the three-state bus drivers (DB0-DB3) and transfers data from the DATA-IN lines onto the data bus. When $\overline{MRD}$ = 0, it disables the three-state bus drivers (DB0-DB3) and enables the three-state data output drivers (DO0-DO3), thus transferring data from the data bus to the DATA-OUT terminals.

The CDP1856 or CDP1857 can be used as a bi-directional bus buffer by connecting the corresponding DI and DO terminals (Fig.2).

The $\overline{MRD}$ output signal from the CDP1802 microprocessor has the correct polarity to control the CDP1856 when this device is used as a memory data bus buffer/separator, or the CDP1857 when it is used as an I/O bus buffer/separator. Therefore, the CDP1802 $\overline{MRD}$ signal can be connected directly to the $\overline{MRD}$ input of either device. See Function Tables 1 and 2 in Fig.3 for use of the CDP1856 as a memory data bus buffer/separator and CDP1857 as an I/O bus buffer/separator.

The CDP1856D and CDP1857D are functionally identical to the CDP1856CD and CDP1857CD, respectively. The CDP1856D and CDP1857D have a recommended operating-voltage range of 3 to 12 volts, and the CDP1856CD and CDP1857CD have a recommended operating-voltage range of 4 to 6 volts.

The CDP1856D, CDP1856CD, CDP1857D and CDP1857CD are supplied in 16-lead hermetic, dual-in-line ceramic packages.

MAXIMUM RATINGS,
Absolute-Maximum Values

Storage-Temperature Range (T_{stg}) . . . . . −65 to +150°C

Operating-Temperature Range (T_A) . . . . . −55 to +125°C

DC Supply-Voltage Range (V_{DD})
(All voltage values referenced to V_{SS} terminal)
CDP1856D, CDP1857D . . . −0.5 to +15 V
CDP1856CD, CDP1857CD . . −0.5 to +7 V

Power Dissipation Per Package (P_D):
For T_A = −55 to +100°C . . . . . 500 mW
For T_A = +100 to +125°C . . . . . Derate linearly to 200 mW

Device Dissipation Per Output Transistor:
For T_A = −55°C to +125°C 100 mW

Input Voltage Range, All Inputs . . . . . −0.5 to V_{DD} +0.5 V

Lead Temperature (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

OPERATING CONDITIONS at T_A = 25°C Unless Otherwise Specified

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	CONDITIONS	LIMITS				UNITS
	V_{DD} (V)	CDP1856D CDP1857D		CDP1856CD CDP1857CD		
		Min.	Max.	Min.	Max.	
Supply Voltage Range (At T_A = Full Package-Temperature Range)	–	3	12	4	6	V
Recommended Input Voltage Range	–	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	TEST CONDITIONS		LIMITS		UNITS
			CDP1856D CDP1857D	CDP1856CD CDP1857CD	
	V_O (V)	V_{DD} (V)	Typical Values	Typical Values	
Dynamic: t_r,t_f=10 ns, C_L=100 pF					
Propagation Delay Time: $\overline{MRD}$ or CS to DO, t_{ED}		5	150	150	ns
		10	75	–	
$\overline{MRD}$ or CS to DB, t_{EB}		5	150	150	ns
		10	75	–	
DI to DB, t_{IB}		5	100	100	ns
		10	50	–	
DB to DO, t_{BD}		5	100	100	ns
		10	50	–	

ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$

CHARACTERISTIC	TEST CONDITIONS			LIMITS		UNITS
				CDP1856D CDP1857D	CDP1856CD CDP1857CD	
		V_O (V)	V_{DD} (V)	Typical Values	Typical Values	
Static						
Quiescent Device Current, I_L		–	5	50	100	μA
		–	10	100	–	
		–	15	500	–	
Output Voltage: Low-Level, V_{OL}		–	5-10	0.01	0.01	V
High-Level, V_{OH}		–	5	4.99	4.99	
		–	10	9.99	–	
Noise Margin: V_{NML}	Any Input	0.5	5	1	1	V
		1	10	1.5	–	
V_{NMH}	Any Input	4.5	5	1	1	
		9	10	1.5	–	
Output Drive Current: N-Channel (Sink), I_{DN}	Any Output	0.4	5	1.8	1.8	mA
		0.5	10	3.6	–	
P-Channel (Source), I_{DP}	Any Output	4.6	5	−1.6	−1.6	
		9.5	10	−3.6	–	
Data Output Off-Resistance, R_O(Off)	CS Low	–	5-10	5	5	MΩ
Input Leakage, I_{IL}, I_{IH}	Any Input	–	5-10	1	1	μA

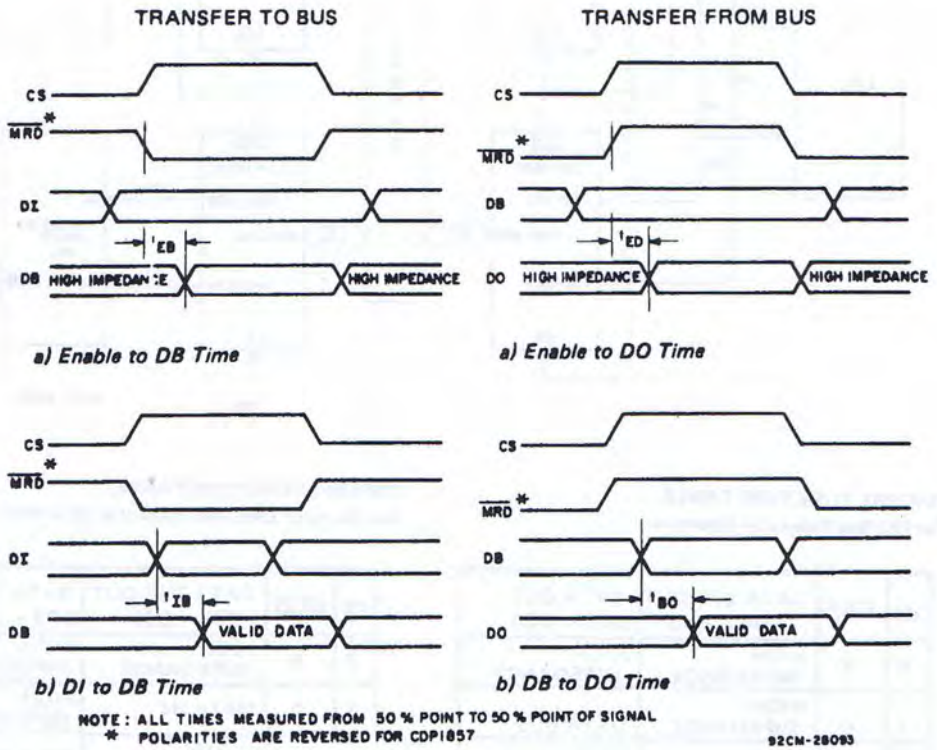


Fig. 1 – Timing Diagrams for CDP1856.

TYPICAL APPLICATIONS

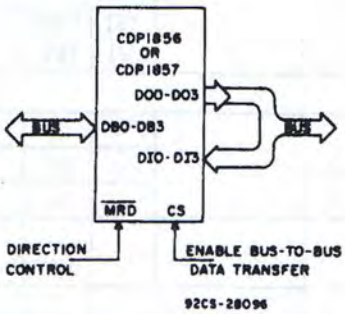
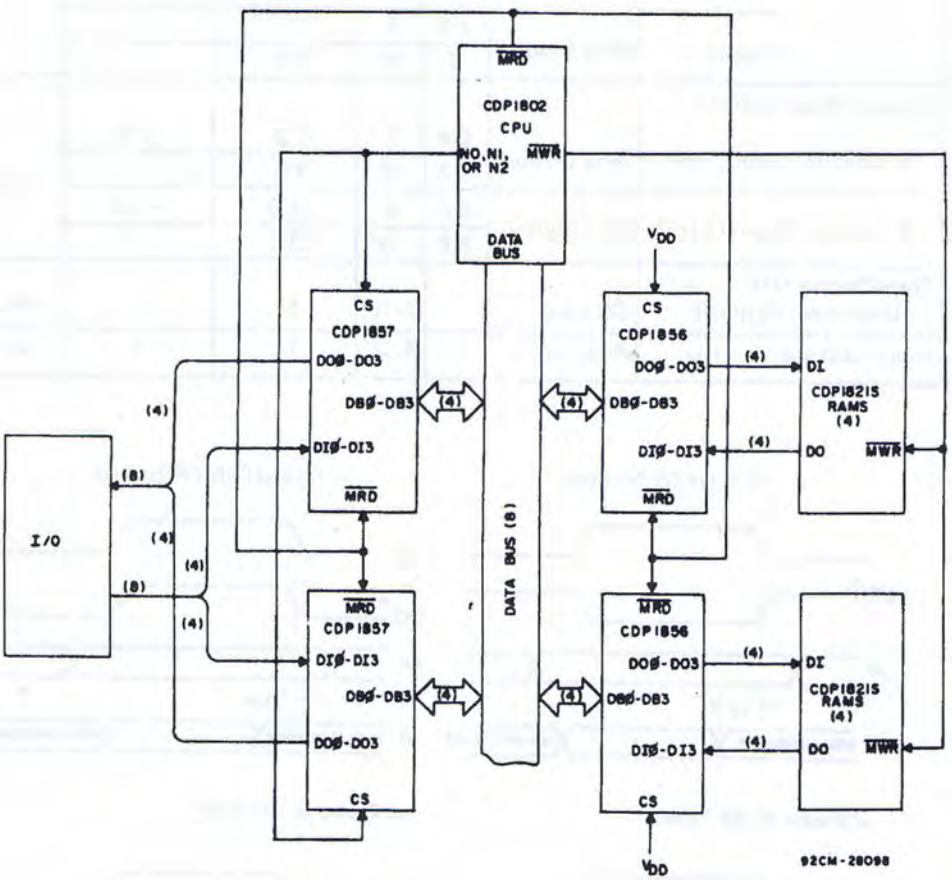


Fig. 2 – CDP1856, CDP1857 Bidirectional Bus Buffer Operation.



CDP1857 FUNCTION TABLE
For I/O Bus Separator Operation

CS	$\overline{MRD}$	DATA BUS OUT DB0 – DB3	DATA OUT DO0 – DO3
0	X	HIGH IMPEDANCE	HIGH IMPEDANCE
1	0	HIGH IMPEDANCE	DATA BUS
1	1	DATA IN	HIGH IMPEDANCE

CDP1856 FUNCTION TABLE
For Memory Data Bus Separator Operation

CS	$\overline{MRD}$	DATA BUS OUT DB0 – DB3	DATA OUT DO0 – DO3
0	X	HIGH IMPEDANCE	HIGH IMPEDANCE
1	0	DATA IN	HIGH IMPEDANCE
1	1	HIGH IMPEDANCE	DATA BUS

Fig. 3 – CDP1856 and CDP1857 Bus Separator Operation.

OPERATING AND HANDLING CONSIDERATIONS

1. **Handling**
   All inputs and outputs of RCA COS/MOS devices have a network for electrostatic protection during handling. Recommended handling practices for COS/MOS devices are described in ICAN-6525, "Guide to Better Handling and Operation of CMOS Integrated Circuits."
2. **Operating**

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause $V_{DD}-V_{SS}$ to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} nor less than V_{SS}. Input currents must not exceed 10 mA even when the power supply is off.

Unused Inputs

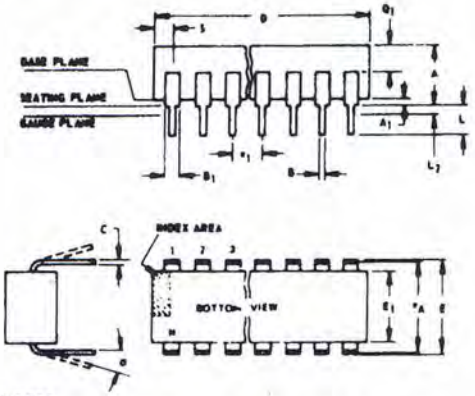
A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{DD} or V_{SS}, whichever is appropriate.

Output Short Circuits

Shorting of outputs to V_{DD} or V_{SS} may damage COS/MOS devices by exceeding the maximum device dissipation.

DIMENSIONAL OUTLINE

D Suffix
16-Lead Dual-In-Line
Ceramic Package



SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.120	0.160		3.05	4.06
A_1	0.020	0.065		0.51	1.65
B	0.014	0.020		0.356	0.508
B_1	0.035	0.065		0.89	1.65
C	0.008	0.012	1	0.204	0.304
D	0.745	0.785		18.93	19.93
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.76
α	0°	15°	4	0°	15°
N	16		5	16	
N_1	0		6	0	
Q_1	0.050	0.085		1.27	2.15
S	0.015	0.060		0.39	1.52

92SS-4286R4

NOTES:
Refer to Rules for Dimensioning (JEDEC Publication No. 13) for Axial Lead Product Outlines.

1. When this device is supplied solder dipped, the maximum lead thickness (narrow portion) will not exceed 0.013" (0.33 mm).
2. Leads within 0.005" (0.12 mm) radius of True Position (TP) at gauge plane with maximum material condition and unit installed.
3. e_A applies in zone L_2 when unit installed.
4. α applies to spread leads prior to installation.
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads.

When incorporating RCA Solid State Devices in equipment, it is recommended that the designer refer to "Operating Considerations for RCA Solid State Devices", Form No. 1CE-402, available on request from RCA Solid State Division, Box 3200, Somerville, N. J. 08876.

Microprocessor Products

Application Note

ICAN-6657

USE OF THE CDP1856 AND CDP1857 BUFFER/SEPARATOR IN CDP1802 MICROPROCESSOR SYSTEMS

by J. Oberman

The RCA CDP1856 and CDP1857 are four-bit bus buffers or separators intended for those applications that require interface with the CDP1802 bidirectional three-state data bus. They can be used to buffer the bidirectional data bus, for increased driving capability, or to separate the data bus into two unidirectional data buses. This Note describes the uses of the CDP1856 and CDP1857 and, more specifically, how they may be utilized in the RCA Evaluation Kit CDP18S020 and the EK/Assembler-Editor Design Kit CDP18S024.

DESCRIPTION

The functional logic diagram for both the CDP1856 and CDP1857 is shown in Fig. 1. Both parts require a positive chip-select input signal to enable their outputs. They differ only in the polarity of the MRD input signal required to transfer data to the bidirectional data bus. The CDP1856 requires a negative polarity MRD signal and can be used to buffer or separate data transfers between memory and microprocessor. The CDP1857 requires a positive MRD input signal and can be used for data transfers between the bus and various I/O devices.

As shown in Fig. 1, a typical buffer consists of two three-state drivers. On the bus side, the input of one driver is connected to the output of the other driver; they share a common terminal. However, their respective output and input are connected to separate terminals. When the chip is selected, only one output will be enabled, depending upon the polarity of the MRD input signal and the particular part.

APPLICATION INFORMATION

The CDP1856 may be used as a bus separator or bus buffer on the memory side of the bidirectional data bus. Similarly, the CDP1857 can be used for the same functions on the I/O side of the data bus. If an I/O command (N-bits) is present, the data transfer is from I/O to memory and microprocessor. Otherwise the transfer is between microprocessor and memory. The MRD command, pin 7 of the CDP1802, determines the direction of the transfer.

If an I/O command is present, and MRD is high, the data transfer is from I/O device to memory and microprocessor, I/O→M(R(X)),D. The MWR command will be asserted by the microprocessor. If MRD is low, the transfer is directly from the memory to the I/O device, M(R(X))→I/O. The microprocessor will ignore the data placed on the bus.

For a non-I/O instruction, I/O command lines low, a low level on the CDP1802 MRD output terminal indicates a data transfer from memory to microprocessor. If MRD is high, a data transfer from microprocessor to memory may occur; the output of data from the microprocessor to the bus and the presence of an MWR command later in the cycle will be the only indication of this occurrence.

The CDP1856 or CDP1857 may be used in conjunction with the RCA COSMAC Kits CDP18S020 and CDP18S024 when large amounts of logic will be added to the microprocessor's data bus. The components may be mounted in the user area provided on the card with connections made directly to the user I/O connector if the additional logic is to be breadboarded externally. The points for connections to the data bus and MRD command are available along the left-hand side of the user area. Decoded I/O commands, I/O − 1 to I/O − 7, are available at the system to connnector, P-1.

Fig. 2 illustrates two techniques for using the CDP1856 either as a bus buffer or a bus separator to reduce the loading effects of large memory systems on the data bus. If the memory employs common I/O pins, the buffer configuration should be used. The bus separator configuration is useful if the memory does not have an output disable input or if it is desirable to maintain separate inputs and output connections to the memory devices.

The use of the CDP1857 is illustrated in Fig. 3. It is used on the I/O side of the data bus; its chip enable input may be connected to an I/O command output. Therefore, the CDP1857 can be used to gate information to a particular I/O device under control of the microprocessor. As discussed above, the use of the buffer or bus separator configuration will depend upon the needs of the particular application.

The CDP1856 and CDP1857 provide an efficient low-cost solution to the problem of interfacing with the CDP1802 bidirectional data bus.

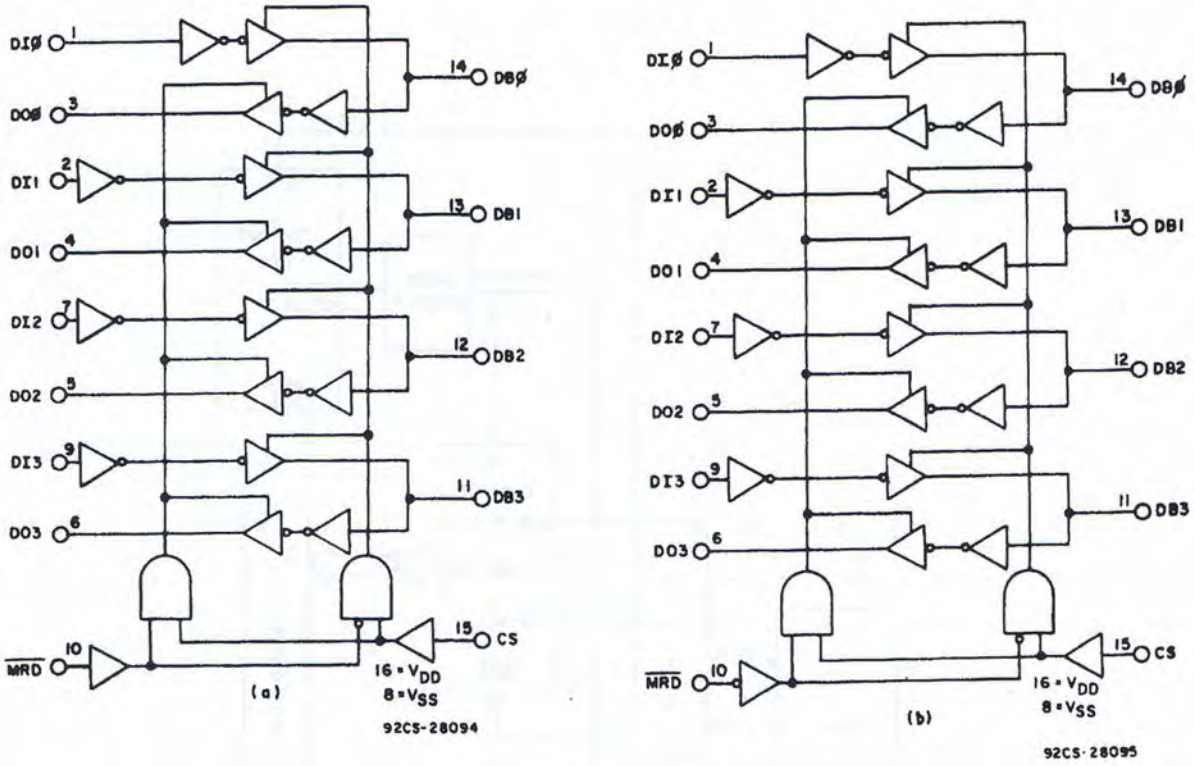


Fig. 1 - Functional diagrams (a) CDP1856, (b) CDP1857.

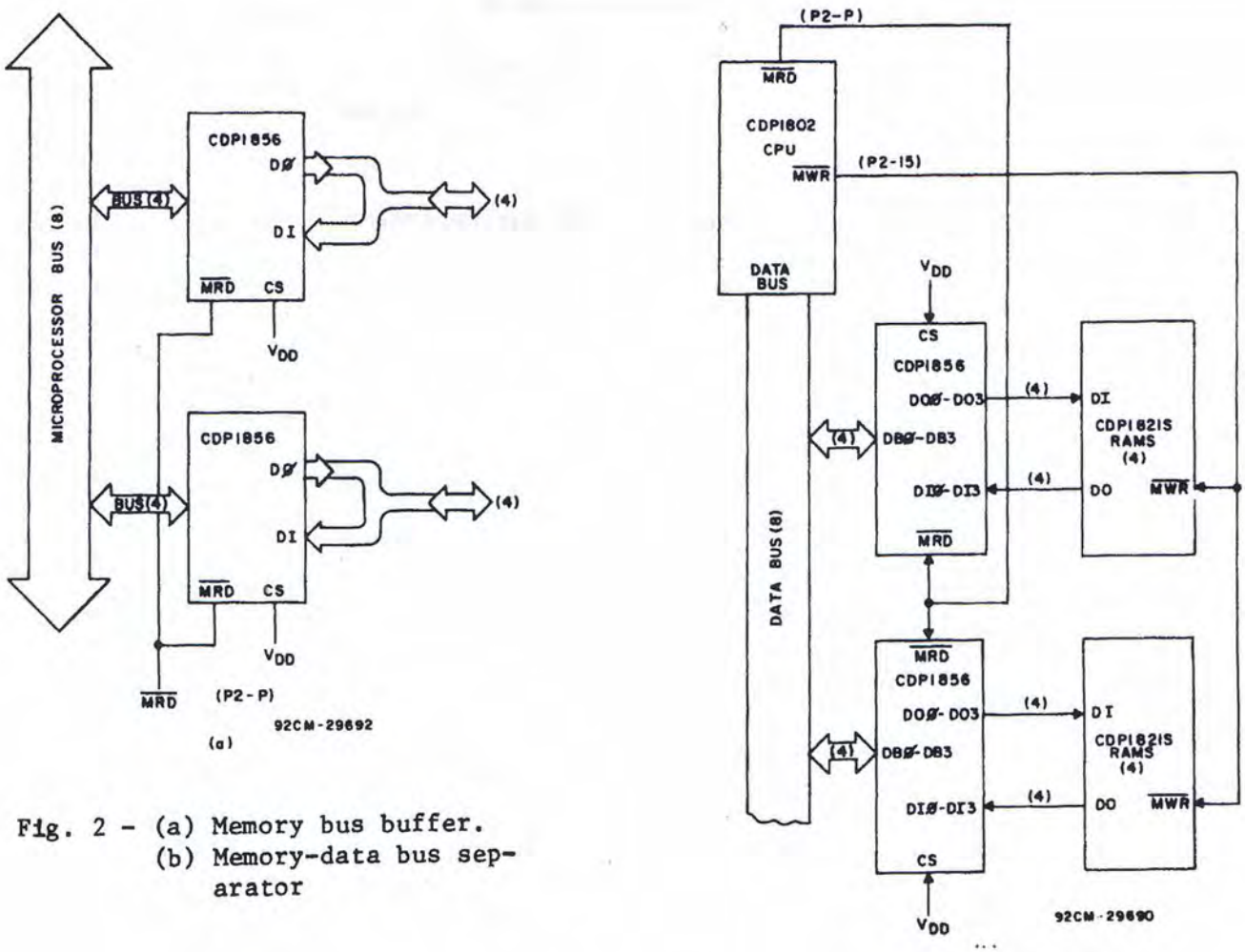


Fig. 2 - (a) Memory bus buffer.
(b) Memory-data bus separator

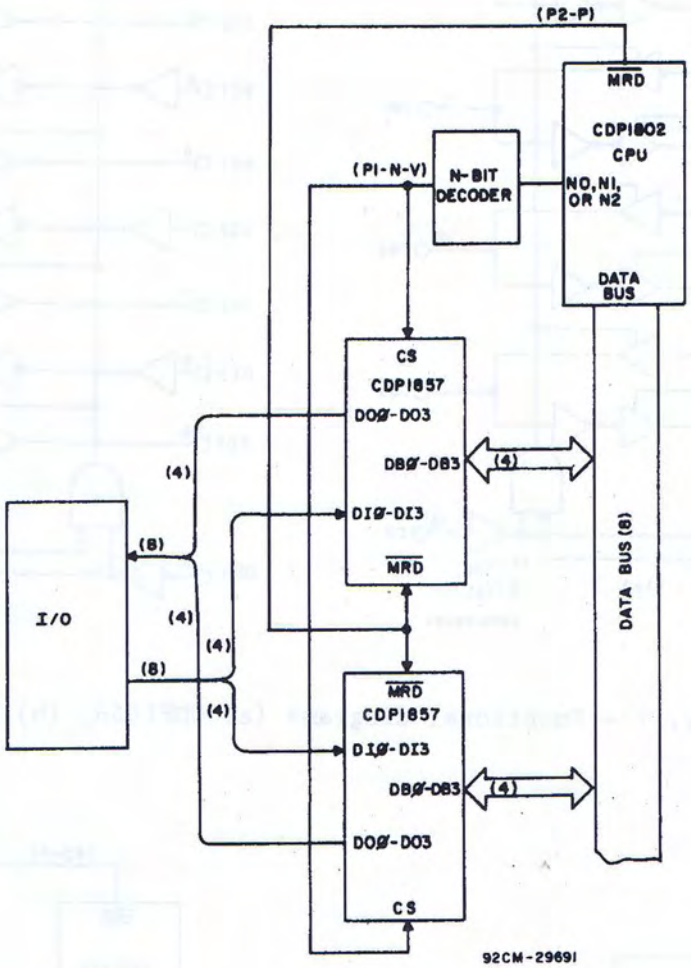


Fig. 3 - I/O bus separator.

Microprocessor Products

Application Note

ICAN-6538

USE OF THE CDP1852 8-BIT I/O PORT WITH RCA MICROPROCESSOR EVALUATION KIT CDP18S020

by R. G. Ott

The CDP1852 I/O Port is a versatile circuit permitting fully parallel data transfer between the 8-bit bus of the CDP1802 microprocessor and an external device. The on-chip 8-bit data latch and the service request output signal of the CDP1852 make it an excellent interface circuit for synchronous or asynchronous data transfers. The CDP1852 is mode programable to function as either an input or an output port and can serve additional functions depending on the use of its control signals. This note describes several applications of the CDP1852 I/O Port and specifically explains its use in the CDP18S020 Evaluation Kit.

DESCRIPTION OF THE CDP1852 FEATURES

The CDP1852, when programmed as an input port (mode=0) or an output port (mode=1), will interface directly with the CDP1802 microprocessor without additional components. When the CDP1852 is used as an input port, data are strobed into the 8-bit register by a high (1) level on the clock line. The high-to-low transition of the clock latches the data in the register and sets the $\overline{SR}$ service request output to 0. The three-state output drivers are enabled by $\overline{CS1}\cdot CS2=1$, and the high-to-low transition of $CS1\cdot CS2$ resets $\overline{SR}=1$.

When the CDP1852 is used as an output port, data are strobed into the 8-bit register when $\overline{CS1}\cdot CS2\cdot CLOCK=1$. The data are available at the outputs at all times because the three-state output drivers are always enabled when the mode input = 1. The Service Request (SR) pulse is generated at the termination of $\overline{CS1}\cdot CS2=1$ and is present (high level) until the next high-to-low transition of the clock.

A CLEAR control is provided for resetting the port's register and $\overline{SR}$ (input mode) or SR (output mode) signal. It is important to note that the polarities of service request ($SR/\overline{SR}$) and chip select 1 ($CS1/\overline{CS1}$) change when the polarity of the mode input signal is changed.

A functional block diagram of the I/O Port is shown in Fig. 1. For the electrical characteristics of the I/O Port, including loading and timing specifications, refer to the CDP1852 data sheet.

APPLICATION OF CDP1852 AS AN INPUT PORT, OUTPUT PORT, AND ADDRESS LATCH

The CDP18S020 Evaluation Kit uses the CDP1852 I/O Port in three different applications: as an input port, as an output port, and as an address latch. In each of these applications, the CDP1852 is controlled by microprocessor signals.

As an input port, the CDP1852 (location U5 in the Evaluation Kit) is used to latch 8 bits of data from an external device. The Evaluation Kit connections for this application and the associated timing diagram are given in Fig. 2. The mode input is tied low (mode=0). When data are latched on the high-to-low transition of the external clock, the SR service request signal is set low ($\overline{SR}$=0). This signal can be connected either to the microprocessor EF3 or INT inputs depending on the control program being used. An optional connection is made via a jumper on the Evaluation Kit Board. When the microprocessor responds to a service request, the input port is enabled by $\overline{MRD}$ (connected to the CS1 input) which is normally high and will remain high. The decoded "6" output of the N bit decoder (connected to the CS2 input) selects the I/O port. In a minimal system (up to three ports) it is possible to bypass the N bit decoder and connect an N line directly to CS2. After the data has been written into memory, the service request is reset ($\overline{SR}$=1) on the trailing edge of the N line. The input port is then ready to accept the next data byte from the external device.

An example of a simple system using the input port follows. Switches can be connected to the data inputs. These lines come from the following connector pins: DI7 to P1-10, DI6 to P1-11, DI5 to P1-12, DI4 to P1-13, DI3 to P1-14, DI2 to P1-15, DI1 to P1-16, DI0 to P1-17. The switches can be used to connect either a logic 1 (V_{DD} voltage) or a logic 0 (ground) to the input port data inputs. A positive pulse for the clock can be generated by connecting a switch to connector P1-18. Once the data switches are set, the clock can be pulsed. Data are transferred to the input port, and the service request signal goes to ground (logic 0).

Table I gives a machine-language routine for acknowledging a service request when the SR line is connected to the EF3 input of the microprocessor. Verification that the correct byte was input into memory can be obtained by using utility program UT4 to read the memory location where the input byte was stored (in this case, location 0F). To read the memory location, press the Reset and then the RUN U button on the Evaluation Kit. Typing a carriage return on the terminal (for some terminals, a line feed is required)

```
!M
0000 ;          0001          ORG 00    ..PROGRAM STARTS AT M(0000)
0000 F80F;      0002          LDI #0F   ..SET R5 TO POINT TO
0002 A5;        0003          PLO R5    ..M(000F)
0003 F800;      0004          LDI 00
0005 B5;        0005          PHI R5
0006 E5;        0006          SEX R5    ..SET X TO R5
0007 3E07;      0007 WAIT:    BN3 *     ..WAIT FOR EF3=1
0009 6E;        0008          INP 6     ..INPUT FROM INPUT PORT
000A 3007;      0009          BR WAIT   ..LOOP BACK TO WAIT
000C ;          0010          ORG *+3
000F ;          0011 STACK:   ORG *     ..LOCATION FOR STORING INPUT DATA
000F ;          0012          END
0000
```

Table I - Machine-language routine for acknowledging a service request.

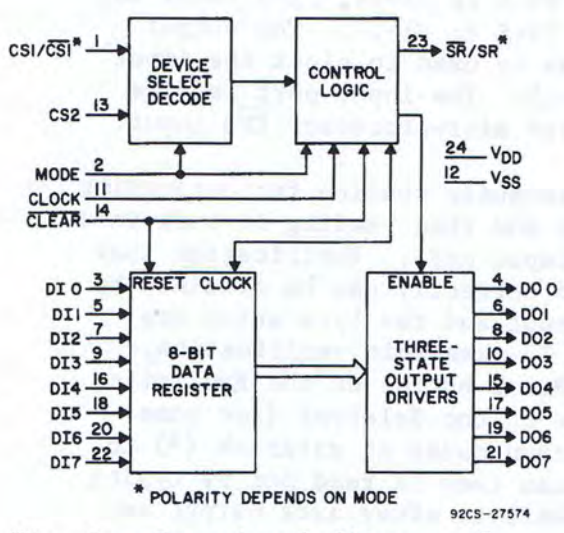


Fig. 1 - Functional diagram of CDP1852 8-bit Input/Output Port.

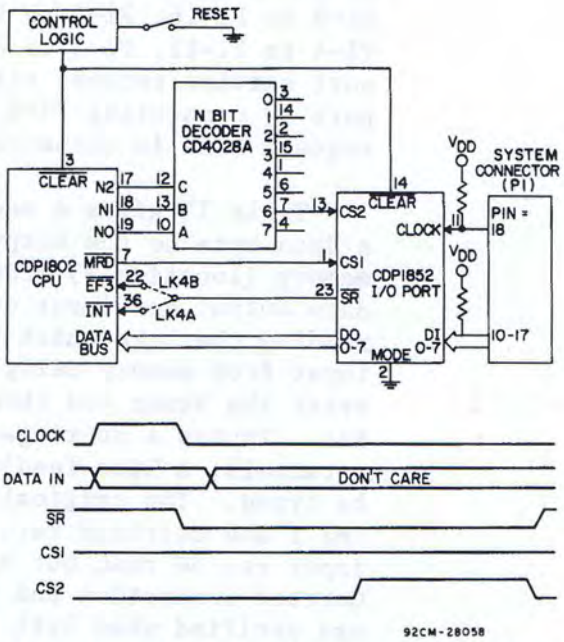


Fig. 2 - Circuit diagram of CDP1852 used as an input port with RCA Microprocessor Evaluation Kit CDP18S020 and associated timing diagram.

will then cause an asterisk (*) to be typed. The byte can be read out by typing ?MF 1 and carriage return. Two hexadecimal digits will be typed and can be checked against the input byte set with switches.

As an output port, the CDP1852 (location U4 in the Evaluation Kit) is used to latch 8 bits of data from the CDP1802 data bus for asynchronous transfer to an external device. The Evaluation Kit connections for this application and the associated timing diagram are given in Fig. 3. The mode input is tied high (mode=1). To begin the sequence, the microprocessor executes an output instruction. The output of the N bit decoder (connected to the CS2 input) selects the output port. When $\overline{MRD}$ (connected to the $\overline{CS1}$ input) goes low, the output port is enabled and data is latched on the trailing edge of TPB (connected to the clock input). On the trailing (high-to-low) edge of $\overline{CS1} \cdot CS2$, SR is asserted (SR=1) and held valid until the trailing edge of the next TPB, which signals the external device that new data is available. If it is necessary to extend the duration of this service request, an external latch must be provided.

The previous example for use of an input port can be extended to use both the input and output ports. Instead of connecting switches to the input port data inputs, the corresponding output port data outputs should be connected to the input port data inputs as follows: P1-9 to P1-17, P1-8 to P1-16, P1-7 to P1-15, P1-6 to P1-14, P1-5 to P1-13, P1-4 to P1-12, P1-3 to P1-11, P1-E to P1-10. The output port service request signal can be used to clock the input port by connecting P1-F to P1-18. The input port service request line is connected to the microprocessor $\overline{EF3}$ input.

Table II gives a machine-language routine for outputting a data byte to the output port and then reading it back into memory (location F) from the input port. Verification that data output and input occurred correctly can be obtained by reading the byte which was output and the byte which was input from memory using UT4. To make this verification, press the Reset and then the Run U button on the Evaluation Kit. Typing a carriage return on the Teletype (for some terminals, a line feed) will then cause an asterisk (*) to be typed. The original byte can then be read out by typing ?M2 1 and carriage return. The byte after data output and input can be read out by typing ?MF 1 and carriage return. Correct connection and functioning of the CDP1852 I/O Ports are verified when both bytes are the same. For example, if location 02 contained 2B, then location 0F will contain 2B when the transfer is complete.

```
!M
0000 ;          0001          ORG 00    ..PROGRAM STARTS AT M(0000)
0000 E0;        0002          SEX R0    ..SET X TO R0
0001 65;        0003          OUT 5     ..OUTPUT IMMEDIATE
0002 FF;        0004          ,#FF
0003 F80F;      0005          LDI #F    ..SET R5 TO POINT TO
0005 A5;        0006          PLO R5    ..M(000F)
0006 F800;      0007          LDI 00
0008 B5;        0008          PHI R5
0009 E5;        0009          SEX R5    ..SET X TO R5
000A 3E0A;      0010 WAIT:    BN3 *     ..WAIT FOR EF3=1
000C 6E;        0011          INP 6     ..INPUT DATA FROM INPUT PORT
000D 300A;      0012          BR WAIT   ..LOOP BACK TO WAIT
000F ;          0013 STACK:   ORG *     ..LOCATION FOR STORING DATA
000F ;          0014          END
0000
```

Table II - Machine language routine for outputting a data byte to the output port and then reading it back into memory from the input port.

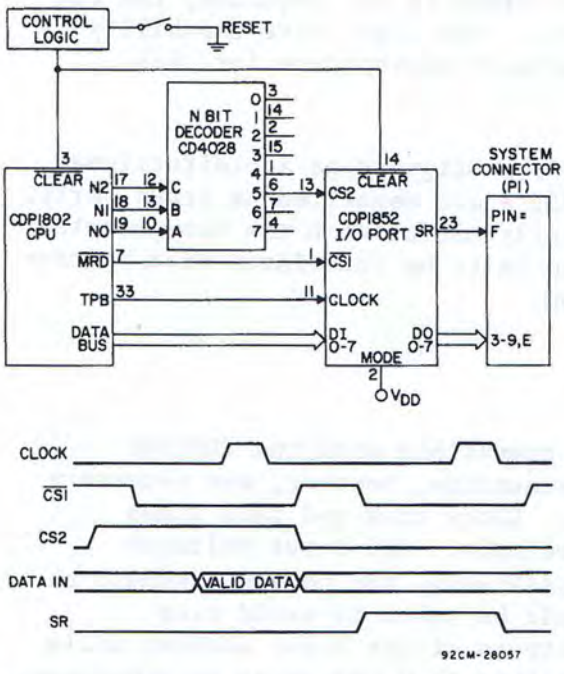


Fig. 3 - Circuit diagram of CDP1852 used as an output port with RCA Microprocessor Evaluation Kit CDP18S020 and associated timing diagram.

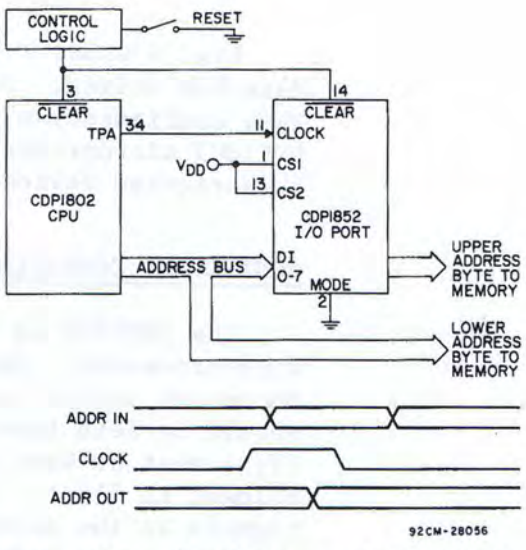


Fig. 4 - Circuit diagram of CDP1852 used as an address latch with RCA Microprocessor Evaluation Kit CDP18S020 and associated timing diagram.

Note that the decode (decode "6")of the N bits used to select the input port is different from the decode (decode "5") used to select the output port. If the same decode is used, the input port SR signal will be reset ($\overline{SR}$=1) at the beginning of every cycle in which the output port is selected. The use of different N decodes prevents loss of data resulting from resetting SR before it is acknowledged.

As an address latch, the CDP1852 (location U8 in the Evaluation Kit) is used to latch the upper byte of the microprocessor memory address in each machine cycle. The port is, therefore, always selected. TPA is used as the clock to latch the address byte, and the mode input is tied low (mode=0). Fig. 4 shows the I/O Port connected for this application, together with its associated timing diagram.

OTHER APPLICATIONS OF THE CDP1852

Additional applications of the CDP1852 I/O Port include its use as a tri-state buffer and as a bidirectional bus driver.

Fig. 5 shows the CDP1852 connected as a noninverting, tri-state, 8-bit buffer. With MODE=0, CLOCK=1, and CS1=1, CS2 can be used as a tri-state control. When CS2=0, the output is a high impedance, but when CS2=1, data out equals data in. If a high-impedance state is not required, the CS2 input can be tied high (CS2=1). The high drive capability of the CDP1852 makes it especially appropriate for this application.

Fig. 6 shows two CDP1852's configured as a bidirectional data-bus driver. Both CDP1852's are connected as input ports. This configuration is especially useful when the bus-oriented CDP1802 microprocessor system is to be interfaced with another bus-oriented device or system.

ADDITIONAL CONSIDERATIONS

The CDP1852 is directly compatible with the CDP1802 microprocessor. Certain precautions, however, are necessary to assure correct operation. Clock rise and fall times should be less than 5 microseconds. All input voltages (V_{in}) must be kept within $V_{SS} \leq V_{in} \leq V_{DD}$ and no input should be allowed to float. Care should be taken to avoid true signals at the unselected outputs of the N-bit decoder while the N-bits are switching, because they may cause an erroneous service request or erroneous resetting of a service request.

Erroneous resetting of an input port service request ($\overline{SR}$) can also occur if the same N line or decode of the N lines is used to select both an input port and an output port. If $\overline{MRD}$ is connected to chip select 1, the input port will be selected and enabled briefly at the beginning of each cycle in which the output port is selected. The reason this condition occurs is that $\overline{MRD}$ goes low to enable the output port 1-1/2 CPU clock periods after the N lines are valid. If the input port is requesting service ($\overline{SR}$=0), $\overline{SR}$ will be reset ($\overline{SR}$=1) without servicing the request. This error is avoided by using different N lines or decodes of the N lines to select the input and output ports. Another solution to this problem would be to clock both chip-select input signals with the trailing edge of the CDP1802 microprocessor TPA signal.

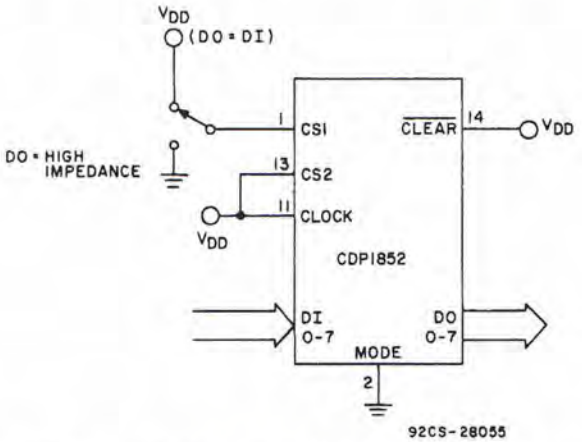


Fig. 5 - Diagram showing use of CDP1852 as tri-state buffer.

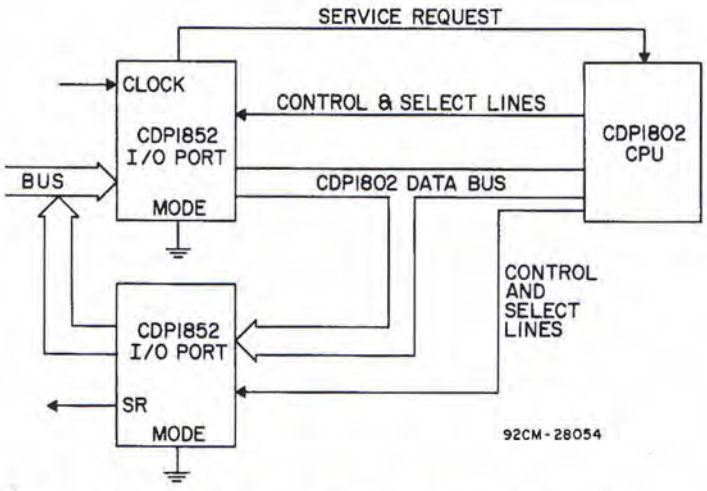


Fig. 6 - Diagram showing use of two CDP1852's as a bidirectional data-bus driver.

Microprocessor Products
Application Note
ICAN-6543

DESIGN OF CLOCK GENERATORS FOR USE WITH RCA COSMAC MICROPROCESSOR CDP1802

by D. Hillman

Clock signal generation for the CDP1802 COSMAC microprocessor is simple and straightforward. The CDP1802 features of static operation, single-phase clock input, and the on-chip oscillator amplifier make practical the use of a low-cost, highly stable, crystal-controlled oscillator as its clock generator. The design of external oscillators for this purpose, crystal or RC controlled, is equally straightforward and they require only minimal circuitry. In addition to the oscillator amplifier, the CDP1802 incorporates all necessary start/stop logic on-chip. This application note describes the clock generator used with the CDP18S020 Evaluation Kit as well as alternate clock generator designs suitable for other applications.

CRYSTAL OSCILLATOR DESIGN

The basic oscillator circuit for the CDP1802 consists of the on-chip amplifier and an external feedback network as illustrated in Fig. 1. For oscillation to occur, the gain of the amplifier (α) times the attenuation (β) of the feedback network must be greater than or equal to one. In addition, the total phase shift through the amplifier and feedback network must be equal to N times 360 degrees, where N in an integer. Oscillations occur in any system in which the amplified signal is returned in phase to the amplifier after being attenuated less than it was originally amplified.

The frequency stability of an oscillator is primarily dependent upon the phase-changing properties of the feedback network. Because of their high Q and inherent frequency stability, quartz crystals are commonly used in the feedback network.

A parallel resonant oscillator circuit is shown in Fig. 2. The phase angle for the type of feedback network shown in this figure is extremely sensitive to a change in frequency, a condition necessary for stable oscillation. If the equivalent resistance of the crystal is in fact zero (infinite Q),

a change in phase angle of the feedback circuit would not cause any change in oscillator frequency. Therefore, for an oscillator of highest stability, the Q of the crystal should be as high as possible. In general, Q increases with increasing frequency.

The crystal load capacitance, C_L, is defined as the series sum of C_6 and C_7. Higher values of crystal load capacitance generally improve frequency stability but also increase power consumption. The choice of equivalent load capacitance (usually specified to the crystal suppliers) only fixes the series sum of the two capacitors C_6 and C_7. The value of the amplifier output capacitance C_7 should not be fixed. A trimmer should be connected in parallel with, or used in place of, a fixed output capacitor to permit compensation for variation in stray capacitance and circuit component values.

The required capacitance range for the oscillator trimmer capacitor is determined by the variation in oscillation frequency with load capacitance. The total trimming range is mainly a function of the crystal characteristics. For a more detailed analysis see Reference 4.

PRACTICAL OSCILLATOR CIRCUITS

The amplifier, feedback network, and crystal considerations discussed in the preceding paragraphs can be combined for the design of a crystal-controlled oscillator for the CDP1802. The majority of microprocessor applications do not require the frequency of oscillation to be so exact as to require oscillator trimming. An "untrimmed" crystal oscillator will be within 1% of its specified crystal frequency. For most microprocessor applications the following simple guideline can be used.

1. The crystal should be connected between terminals 1 and 39 of the CDP1802.

2. For crystal frequencies between 100 kHz and 6.4 MHz, a 10- to 22-megohm feedback resistor should be used in parallel with the crystal.

3. Capacitors C_6 and C_7 are not required but a value of between 20 and 30 pF for each is recommended to improve stability.

It should be noted that the on-chip oscillator and timing generator are capable of operating at frequencies higher than the microprocessor maximum operating frequency. For reliable operation, the crystal frequency must always be less than or equal to the maximum operating frequency specified in the CDP1802 data sheet.

A practical example, the CDP18S020 Evaluation Kit oscillator, consists of a 10-megohm feedback resistor and a 2-MHz AT-cut crystal, both connected in parallel across terminals 1 and 39 of the CDP1802. Provisions for oscillator capacitors are made in the Evaluation Kit, but their use is not required. The increase in oscillator stability that can be obtained by adding the capacitors in shown in Fig. 3.

The amplifier stability also depends upon the value of the resistor in the feedback network. Fig. 4 shows the relationship between the feedback resistor value and oscillator stability. The curve indicates that 10 megohms is an adequate value for the feedback resistor.

EXTERNAL CLOCK GENERATORS

For low-frequency applications (less than 500 kHz) a cost-effective approach may be to use external RC-controlled oscillators. Fig. 5 shows how to change from an on-chip crystal oscillator to a single-phase external clock. Three simple RC-controlled oscillators that may be used to clock the CDP1802 are shown in Fig. 6. When an external clock is used in high-noise environments, a 20- to 30-pF capacitor between terminal 39 (XTAL) of the CDP1802 and ground may be used to increase the microprocessor noise immunity.

The selection of the R and C should be compatible with system requirements. The capacitor should be non-polarized and have low leakage. There is no upper limit for either R or C values to maintain oscillation. However, C should be larger than the inherent stray capacitance. R must be larger than the output impedance of the COS/MOS device, which is typically hundreds of ohms. In addition, with very large values of R, some short-term instability with respect to time may be noted. Based on these considerations recommended values for these components are:

C - greater than 100 pF, up to any practical value

R - greater than 10 kilohm, but less than one megohm

With large values of R and C, the circuit in Fig. 6c can be used. This circuit, because of its hysteresis, eliminates multiple output pulses caused by noise on the input RC waveform. For a more detailed analysis see References 5 and 6.

CLOCK GENERATOR CONTROL LOGIC

In addition to the clock signal, operation of the CDP1802 microprocessor requires two control lines $\overline{\text{CLEAR}}$ and $\overline{\text{WAIT}}$ to provide all the necessary start/stop logic. The logic circuits that these lines control are built in to the CDP1802. The two

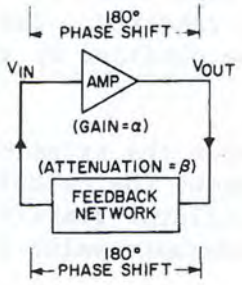


Fig. 1 - Basic oscillator circuit.

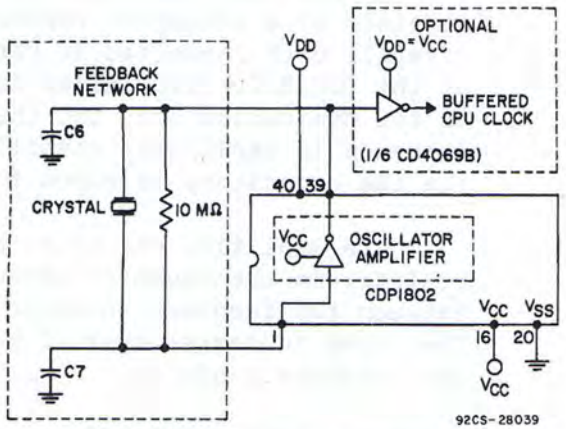


Fig. 2 - Parallel resonant oscillator circuit.

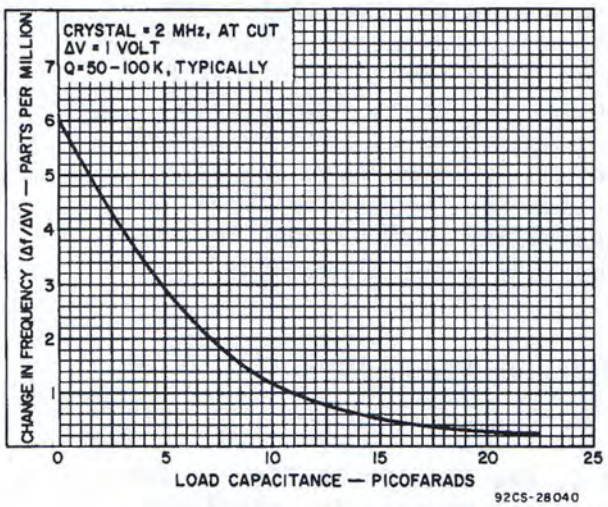


Fig. 3 - Stability of CDP1802 crystal oscillator as a function of load capacitance value.

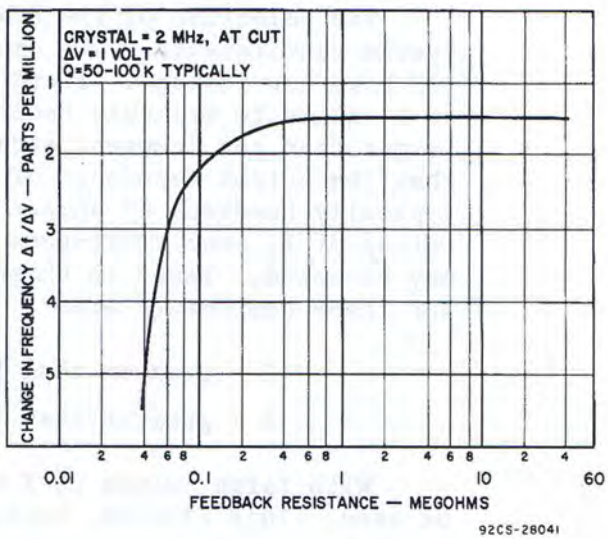


Fig. 4 - Stability of CDP1802 crystal oscillator as a function of feedback resistance value.

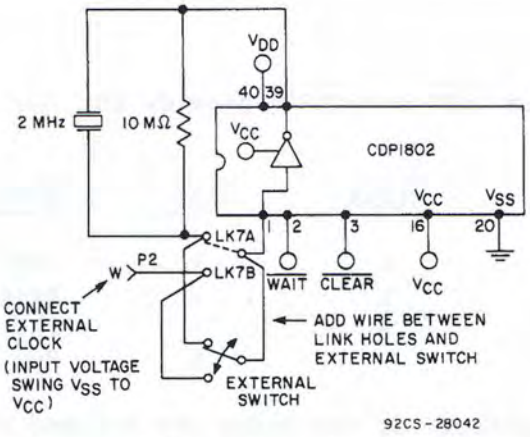


Fig. 5 - Modifications for connection of external clock to CDP18S020 Evaluation Kit.

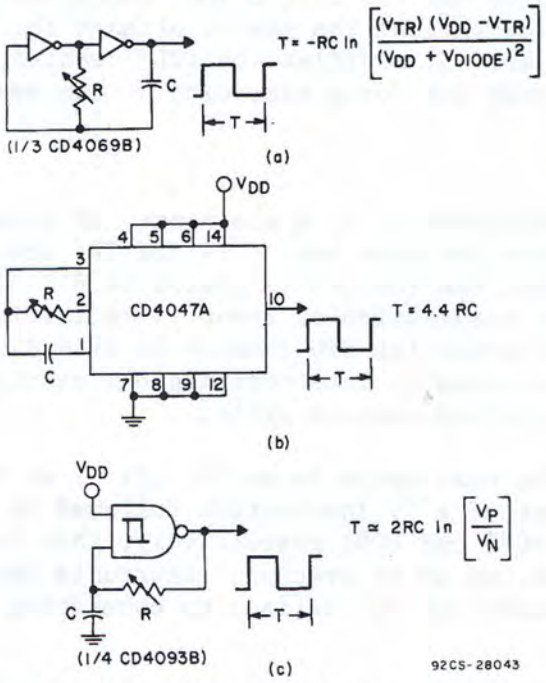


Fig. 6 - Three simple RC-controlled oscillator circuits suitable for use as external clock for CDP1802 microprocessor (Output connected to pin 1 through Evaluation Kit P2-W).

(a) Inverter type oscillator (see references 5 and 6).

(b) RC oscillator using digital IC CD4047A (see references 5 and 6).

(c) Schmitt-trigger-type RC oscillator (see CD4093B data sheet).

control lines $\overline{\text{WAIT}}$ and $\overline{\text{CLEAR}}$ provide the four control modes listed below:

$\overline{\text{CLEAR}}$	$\overline{\text{WAIT}}$	$\overline{\text{MODE}}$
L	L	Load
L	H	Reset
H	L	Pause
H	H	Run

The functions of the modes are defined as follows:

Load

Holds the CPU in the IDLE execution state and allows an I/O device to load the memory without the need for a "bootstrap" loader. It modifies the IDLE condition so that DMA-IN operation does not force exectuion of the next instruction.

Reset

Registers I, N, Q are reset, IE is set, and 0's (V_{SS}) are placed on the data bus. TPA and TPB are suppressed while reset is held and the CPU is placed in S1. The first machine cycle after termination of reset is an initialization cycle. During this cycle the CPU remains in S1 and registers S, P, and R(0) are reset. Interrupt and DMA servicing are suppressed during the initialization cycle.

The next cycle is an S0, S1, or an S2 but never an S3. With the use of a 71 instruction followed by 00 at memory locations 0000 and 0001 respectively, this feature may be used to reset IE, so as to preclude interrupts until ready for them. Power-up reset can be realized by connecting an external RC to $\overline{\text{CLEAR}}$.

Pause

Stops the internal CPU timing generator on the first negative high-to-low transition of the input clock. The oscillator continues to operate, but subsequent clock transitions are ignored.

Run

May be initiated from the Pause or Reset mode functions. If initiated from Pause, the CPU resumes operation on the first negative high-to-low transition of the input clock. When initiated from the Reset operation, the first machine cycle following Reset is always the initialization cycle. The initialization cycle is then followed by a DMA (S2) cycle or fetch (S0) from location 0000 in memory.

References:

1. CDP1802 data sheet.

2. CD4047A data sheet, File #623.

3. CD4093B data sheet, File #836.

4. "Timekeeping Advances Through COS/MOS Technology," ICAN-6086.

5. "Using the CD4047A in COS/MOS Timing Applications," ICAN-6230.

6. "Astable and Monostable Oscillators Using RCA COS/MOS Digital Integrated Circuits," ICAN-6267.

7. User Manual for the RCA CDP1802 COSMAC Microprocessor, MPM-201.

Microprocessor Products

Application Note

ICAN-6551

DATA TERMINAL INTERFACE CONSIDERATIONS FOR RCA MICROPROCESSOR EVALUATION KIT CDP18S020

by R. J. Sedlak

One of the most common methods of communicating with a microprocessor-based system such as the CDP18S020 Evaluation Kit is through a data terminal. Although almost any data terminal is capable of being used to take advantage of the full operating capabilities of the Evaluation Kit, one of the more common ones is the Teletype† Model 33ASR (TTY). Because of the flexibility designed into the Evaluation Kit and the resources of its Utility Program UT4, the user does not need to give special concern to whether the terminal is in the half-duplex or full-duplex mode or what the data transmission rate is. He merely needs to determine whether the terminal uses a 20-mA current loop or the EIA RS232C interface configuration and then follow the appropriate instructions given in this application note.

In addition to providing interface information for both 20-mA current loop and EIA RS232C data terminals, this Note contains instructions for converting a Teletype terminal from 60-mA to 20-mA current loop operation and for converting one from half- to full-duplex operation.

SOME GENERAL I/O INTERFACE CONSIDERATIONS

Because information can be transmitted as digital data in a variety of ways, standards or conventions have been developed which have been adopted by the telecommunications industry to eliminate confusion and improve the reliability of digital communication systems. Systems can be and have been devised which use almost any number of data-carrying signals. When a single signal is used, the data transmission is known as "serial;" when multiple signals are used, the data transmission is "parallel." The CDP18S020 Evaluation Kit contains two data ports, one input port U5 and output port U4, to provide for the parallel transfer of data in groups of eight signals at a time. However, because most data terminals operate in a serial manner, the terminal interfaces provided with the Evaluation Kit are designed to accomodate serial operation.

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† Registered trademark, Teletype Corporation.

Regardless of whether the interface accomodates serial or parallel signals, digital information is always handled in the form of binary bits, which is the smallest unit of information. A bit exhibits either one of two conditions, a "1" or a "0." One state is called a "mark" or active condition; the other a "space" or passive condition. These states can be realized electrically in a number of ways such as current flow or no current flow, voltage within a specified range and voltage within a different specified range with respect to the same ground reference, and others. The only problem has been that of defining which state is which. One definition promulgated by the International Telegraph and Telephone Consultative Committee (CCITT) of the International Telecommunications Union (ITU), and given in Table I, is used by Teletype equipment. Another, promulgated by the Electronic Industries Association (EIA RS232C), is used by the TI Silent 700 Terminal and other American-made terminals of recent design. The EIA RS232C convention establishes the mark as a negative voltage and binary "1", and the space as a positive voltage and binary "0".

Another important consideration in data transmission is coding. Information is usually coded in some manner in order to reduce error transmission through any medium. Coding is performed in a number of ways which work by adding redundancy to the information and thereby reducing the uncertainties inherent in any transmission process. Standards have been adopted in this area of telecommunications also. One of the standards most widely used in the transmission of data, including serial data to and from data terminals, is the ASCII code (American Standard Code for Information Interchange), shown in Table II. This table shows the assignment of characters or information to the various code combinations in the seven-bit code. An extra bit, called a parity bit, is sometimes transmitted with each ASCII character for the purpose of revealing transmission errors.

SERIAL DATA INTERFACE FOR 20-mA CURRENT LOOP EQUIPMENT

Because the Teletype Model 33ASR (TTY) is one of the data terminals most widely available, the information in this section illustrates an interface to this device. However, any terminal that can be operated via a 20-mA current loop can be connected to the Evaluation Kit through the interface described in this section. If the user has a data terminal other than the TTY 33ASR, he should consult the instruction manual for that equipment to effect any necessary modifications and to locate the 20-mA current loop connection points.

ACTIVE CONDITION	PASSIVE CONDITION
MARK	SPACE
CURRENT ON	CURRENT OFF
POSITIVE VOLTAGE	NEGATIVE VOLTAGE
BINARY "1"	BINARY "0"
HOLE (IN PAPER TAPE)	NO HOLE (IN PAPER TAPE)
TONE ON (AMPLITUDE MODULATION)	TONE OFF

Table I - Mark-space convention and equivalent binary designations [established by International Telegraph and Telephone Consultative Committee (CCITT) of the International Telecommunications Union (ITU)]. Used in Teletype Terminal 33ASR.

MOST SIGNIFICANT HEX DIGIT

LEAST SIGNIFICANT HEX DIGIT	0	1	2	3	4	5	6	7
0	NUL	DLE	SP	0	@	P	`	p
1	SOH	DC1	!	1	A	Q	a	q
2	STX	DC2	"	2	B	R	b	r
3	ETX	DC3	#	3	C	S	c	s
4	EOT	DC4	$	4	D	T	d	t
5	ENQ	NAK	%	5	E	U	e	u
6	ACK	SYN	&	6	F	V	f	v
7	BEL	ETB	'	7	G	W	g	w
8	BS	CAN	(	8	H	X	h	x
9	HT	EM	)	9	I	Y	i	y
A	LF	SUB	*	:	J	Z	j	z
B	VT	ESC	+	;	K	[	k	{
C	FF	FS	,	<	L	\	l	|
D	CR	GS	-	=	M	]	m	}
E	SO	RS	.	>	N	↑	n	~
F	SI	US	/	?	O	←	o	DEL

NOTES:

(1) PARITY BIT IN MOST SIGNIFICANT HEX DIGIT NOT INCLUDED.
(2) CHARACTERS IN COLUMNS 0 AND 1 (AS WELL AS SP AND DEL) ARE NON-PRINTING.
(3) MODEL 33 TELETYPE PRINTS CODES IN COLUMNS 6 AND 7 AS IF THEY WERE COLUMN 4 AND 5 CODES.

Table II - ASCII-hex table.

Getting Data into the Evaluation Kit

When a user strikes a key on the TTY keyboard (an "M" for example) the information denoting that character is converted to its ASCII code ($4D_{16}$) and appears on the output terminals as a serial data bit stream. The serial data originating at the TTY appears as shown in Fig. 1. The character is framed by a start bit B and two stop bits FF. By convention, two stop bits are used for data transmitted at 10 characters per second, and one stop bit for higher data transmission rates. A parity bit P is also shown. The parity bit is a "1" only if the seven data bits contain an odd number of "1's." Hence, the total number of 1's in the eight intelligence bits, i.e., seven data bits plus one parity bit, is always an even number. This convention is called the even parity option for ASCII-coded data transmission.

To configure the Evaluation Kit for the 20-mA current loop interface, the assembly instructions and the check-out procedure given in the Evaluation Kit Manual for the RCA CDP1802 COSMAC Microprocessor, MPM-203, should be carefully followed. Care should be taken to assure that links LK8A and LK9 are left open (not inserted) and that link LK8B is inserted.

The bit serial 20-mA current loop interface can be connected to the TTY at either the terminal strip TS or the jack J2. Fig. 2 shows the connection details. Table III lists the critical interface connections. For the Evaluation Kit pin connections, see Fig. 3. The TTY data depicted in Fig. 1 appear as contact openings or closures at terminals 3 and 4 of the terminal strip TS and at terminals 5 and 6 of jack J2. A logic 1 results in a closed contact with a current flow; a logic 0 results in an open contact with no current flow. It is the task of the interface to convert the current pulses that result from the contact closures into a form compatible with the Evaluation Kit logic signals. In the circuit of Fig. 2, the logic 1 or closed contact between the TTY output terminals supplies current to the base of Q1 driving Q1 into saturation. Its collector, consequently, is driven to a low voltage level (ground). The collector voltage state is detected through link LK8B by the CDP1802 microprocessor on $\overline{EF4}$ (U9/pin 21). The logic 0 or open condition between the TTY terminals stops the flow of Q1 base current and allows Q1 to return to cutoff. Its collector, consequently, is returned to a high voltage level (V_{CC}) which is again detected by the microprocessor on $\overline{EF4}$ through LK8B.

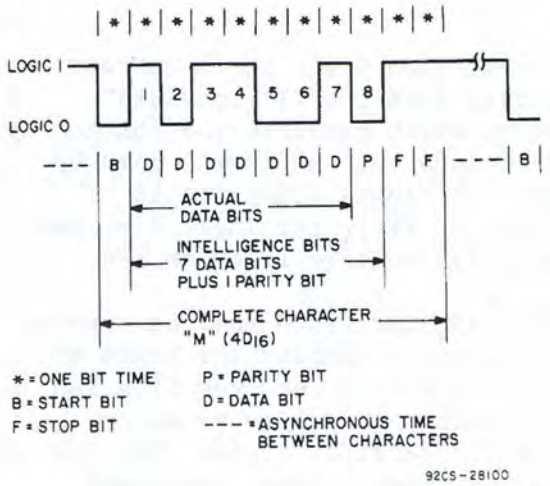


Fig. 1 - Data terminal bit serial output for the character "M".

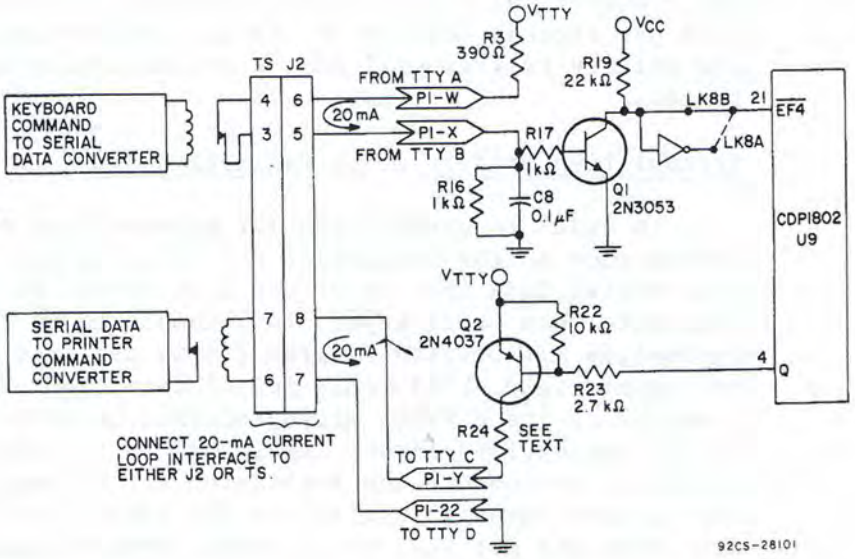


Fig. 2a - The bit serial 20-mA current loop interface for connecting teletypewriter terminal 33ASR in the full-duplex mode to Evaluation Kit CDP18S020.

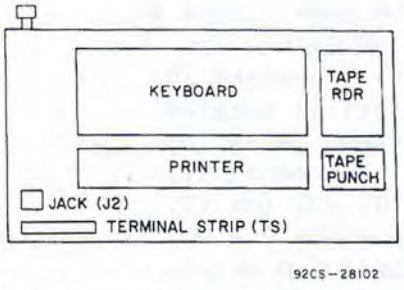


Fig. 2b - Top view of teletypewriter terminal showing relative position of key components.

TELETYPE 33ASR		EVALUATION KIT SYSTEM CONNECTOR
TS	OR J2 (Fig.2)	P1 (Fig.3)
4	6	P1-W
3	5	P1-X
7	8	P1-Y
6	7	P1-22

Table III - 20-mA current loop interface connections for Teletype terminal 33ASR and Evaluation Kit CDP18S020.

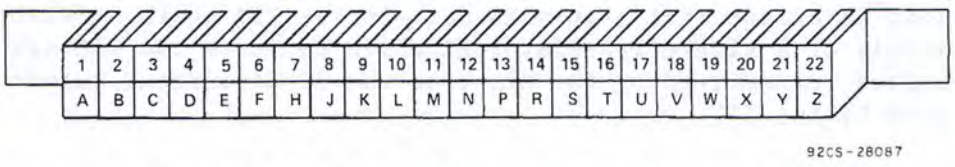


Fig. 3 - Evaluation Kit CDP18S020 connector pin placement.

Hence, the part of the Evaluation Kit's 20-mA current loop interface that receives data from the TTY consists merely of a single transistor Q1 which converts the contact closures originating in the TTY into voltage levels used by the Evaluation Kit. The logic 1 = closed (current) is converted to a low voltage level on $\overline{EF4}$;; the logic 0 = open (no current) is converted to a high voltage level on $\overline{EF4}$.

To detect the data at $\overline{EF4}$, the CDP18S020 must be running the Utility Program UT4. This program samples the state of $\overline{EF4}$ and gathers the data bits as they are received from the TTY. No special interfacing considerations are necessary to deal with half- or full-duplex operation of the TTY; the Utility Program will run in either mode. Also, terminals which operate at a different speed (10, 15, 30, etc. characters per second) require no special interfacing considerations. The Utility Program will adjust automatically to any of these speeds.

Transmitting Data from the Evaluation Kit

In order to operate the TTY printer from an external source such as the Evaluation Kit, the TTY must be supplied with serial data that is of the same format as the data it transmits when it is keyed. An example is in Fig. 1. The Evaluation Kit Utility Program UT4 is designed to provide the appropriate ASCII-coded serial data by "toggling" the Q output of the CDP1802 microprocessor between V_{CC} and V_{SS} at the appropriate times. Again, it is the task of the interface to convert the Evaluation Kit voltage levels into a form compatible with the TTY input circuit. The data from the Kit must be converted from voltage pulses to 20-mA pulses of current flowing in the direction indicated in Fig. 2. The connection can be made either at terminals 8 and 7 of terminal strip TS or at terminals 7 and 6 of jack J2 of the TTY. The logic 1 = current is supplied to the TTY when the CDP1802 Q output is toggled to a low voltage level (ground). The Q output going low drives the transistor Q2 into saturation. Consequently, current flows in the collector circuit of Q2 and the TTY printer is driven as shown in Fig. 2. The logic 0 = no current is supplied to the TTY when the CDP1802 Q output is toggled to a high voltage level (V_{CC}). The Q output going high puts the transistor Q2 into cutoff, and no current flows through the TTY printer input circuit.

Hence, the part of the Evaluation Kit's 20-mA current loop interface that transmits data to the TTY again consists merely of a single transistor Q2 which converts the voltage pulses transmitted by the Kit into the 20-mA current pulses used by the TTY.

Because the Evaluation Kit 20-mA current loop interface has been designed with the objective of providing a flexible, simple interface having a minimum number of components, it is by no means an ideal current source. The current derived from P1-Y and P1-22 will depend upon the dynamic impedance shunting these two terminals. Because the TTY printer input circuit has an impedance between 10 and 50 ohms, this impedance added to the 220-ohm resistor supplied for R24 will deliver about 20 mA through the collector circuit of Q2 (for $V_{TTY} \simeq +5$ volts). Therefore, if data terminals are used which exhibit a significantly different (higher) impedance between their 20-mA printer input terminals, the value of R24 must be adjusted so that R24 plus the data terminal input impedance is within the 220- to 330-ohm range. For this eventuality, a 47-ohm resistor is included with the Evaluation Kit to be used as a possible alternate R24.

SUMMARY OF INSTRUCTIONS FOR IMPLEMENTING THE 20-mA CURRENT LOOP INTERFACE

1. Make sure the TTY is configured for 20-mA current loop operation.

2. Verify that the assembly procedure for this interface configuration has been followed by checking whether the following items have been correctly inserted and soldered on the Evaluation Kit PC card.

   Links: LK8B (Make sure LK8A and LK9 are open)
   Resistors: R3, R16, R17, R19, R22, R23, R24
   Capacitors: C8, C9
   Transistors: Q1, Q2

3. Locate the four 20-mA current loop interface terminals on either the jack J2 or the terminal strip TS of the TTY, and make the connections to the Evaluation Kit, as shown in Fig. 2.

4. Choose an appropriate value for R24 to provide for 20-mA of current when Q2 saturates. (For a TTY 33ASR, R24 should be about 220 ohms. For other data terminals, refer to the preceding instructions on determining a suitable value for R24.)

SERIAL DATA INTERFACE FOR THE EIA RS232C

Because of the variety of possible interface circuits capable of handling the transmission of serial data between two communicating devices, the Electronic Industries Association has recommended the use of a standard interface, the EIA RS232C. As a result, many manufacturers of data terminals have adopted this standard for their products. The CDP18S020 Evaluation Kit has been designed to accomodate such data terminals and is equipped with this EIA RS232C standard interface.

The user need only determine where these interface signals may be accessed on his data terminal and complete the appropriate connections as described in the assembly instructions and check-out procedure given in the Evaluation Kit Manual for the RCA CDP1802 Microprocessor, MPM-203 and in this application note. In this section on the EIA RS232C interface, the TI "Silent 700" data terminal is used as an example.

The EIA RS232C interface standard specifies a number of interfacing signals and their functions. Table IV shows the set of EIA RS232C signals most commonly used in data terminals. This table also shows the location of these signals on Jack J1 of the TI Silent 700 data terminal, the corresponding location of these signals on connector P1 of the Evaluation Kit, and the direction of the signal information, i.e., its source and its destination.

The general operating characteristics of the EIA ES232C serial data interface standard are:

1. The interface uses positive and negative voltage levels. Logic 0 is represented by a positive voltage level between + 3 and + 25 volts. Logic 1 is represented by a negative voltage level between - 3 and - 25 volt. Most data terminals operate with voltages between + 5 and + 10 volts and between - 5 and - 10 volts.

2. The EIA RS232C signals given in Table IV can be grouped as follows:

1 and 7	are ground references
2 and 3	are data-carrying signals
4 and 20	are signals generated by the data terminal for coordinating data transfer to the external communicating unit, the Evaluation Kit.
5, 6, and 8	are acknowledgement signals that must be supplied to the data terminal to coordinate the data transfer.

Getting Data into the Evaluation Kit

As with a TTY, when a user strikes a key on the data terminal, the ASCII code of that character is produced on the serial output of the data terminal (EIA RS232C data set 2). An example character, "M" = $4D_{16}$, is shown in Fig. 1. But, instead of current pulses as in the 20-mA current loop interface, the EIA RS232C standard uses positive and negative voltage pulses to represent the ASCII coded character, with logic 0 = positive voltage and logic 1 = negative voltage. It is

the task of the interface to convert the EIA voltage levels to voltage levels usable by the Evaluation Kit.

To configure the Evaluation Kit for the EIA RS232C interface, after the assembly instructions and check-out procedure given in the Evaluation Kit Manual for the CDP1802 Microprocessor, MPM-203, are followed, the user should make sure that links LK8A and LK9 are inserted and LK8B is left open. The bit serial EIA RS232C interface can be connected to the data terminal as shown in Fig. 4 and Table IV. Because of the simplicity of the Evaluation Kit interface, only a subset of the EIA signals listed in Table IV need be used. The signals EIA 1 and EIA 7 can both be tied to ground (P1-22 as shown in Fig. 4). The signals EIA 4 and EIA 20 supplied by the data terminal are ignored by the Evaluation Kit because Utility Program UT4 coordinates the data transfer. No connections to the Evaluation Kit, therefore, are necessary for these two signals. The signals EIA 5, EIA 6, and EIA 8 must all be permanently tied to a high voltage level (V_{TTY}), P1-19 as shown in Fig. 4. These acknowledgement signals must be supplied to the data terminal if the data terminal possesses them as part of its EIA RS232C interface. However, no special manipulation of these signals is required because Utility Program UT4 will coordinate the transfer of all data. The remaining signals are the data-carrying signals of the interface. They merely need to be connected as follows: EIA 2 connects to P1-21 and EIA 3 connects to P1-Z, as shown in Fig. 4.

When the interface is connected, it transfers data to the Evaluation Kit in the following manner. The logic 1 or negative EIA voltage puts Q1 in a cutoff state. Its collector, consequently, is raised to V_{CC}. This voltage level is fed through an inverter and link LK8A to the CDP1802 microprocessor, which detects a low voltage level (ground) on $\overline{EF4}$ (U9/pin 21).

The logic 0 or positive voltage drives Q1 into saturation. Its collector, consequently, has a low voltage level (ground) which is again fed through the inverter and LK8A to $\overline{EF4}$ (U9/pin 21), and CDP1802 detects a high voltage level (V_{CC}) on $\overline{EF4}$. The Utility Program UT4 must be running in order to detect the voltage level changes on $\overline{EF4}$ as the ASCII data arrives serially. UT4 samples $\overline{EF4}$, gathers the serial data, interprets its meaning, and makes appropriate responses to commands. Half- or full-duplex operating modes and different terminal operating speeds need not concern the user because UT4 is capable of operating in either mode and at any terminal speed equal to or less than 1200 baud.

EIA RS232C DATA SET PIN NUMBER	SIGNAL FUNCTION	TI SILENT 700 JACK J1	SIGNAL DIRECTION	CDP18S020 EVALUATION KIT PIN NUMBER
1	PROTECTIVE GROUND	A	⟷	P1-22
2	TRANSMITTED DATA	H	→	P1-21
3	RECEIVED DATA	10	←	P1-Z
4	REQUEST TO SEND	F	→	*
5	CLEAR TO SEND	8	←	P1-19
6	DATA SET READY	9	←	P1-19
7	SIGNAL GROUND (COMMON RETURN)	7	⟷	P1-22
8	DATA CARRIER DETECT	K	←	P1-19
20	DATA TERMINAL READY	6	→	*

* No connection necessary

Table IV - Set of EIA RS232C signals most commonly used in data terminals.

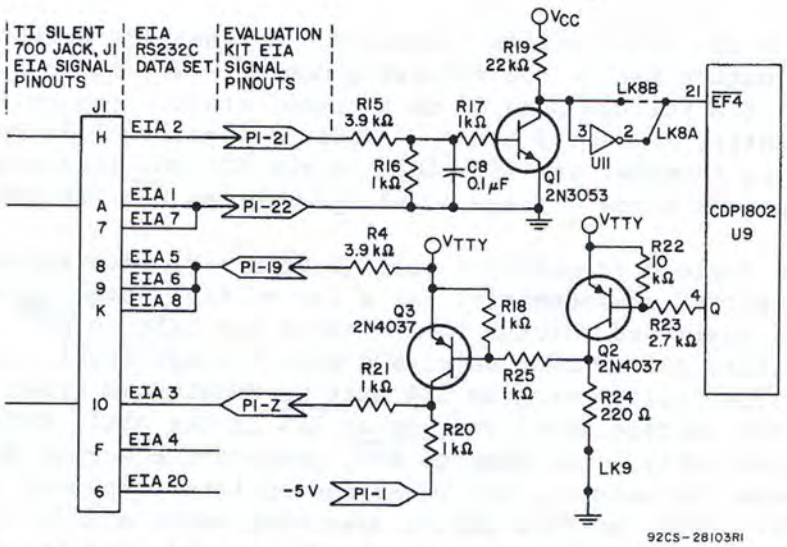


Fig. 4 - The EIA RS232C serial data interface for connecting TI Silent 700 data terminal to Evaluation Kit CDP18S020.

Transmitting Data to the Data Terminal

The Evaluation Kit Utility Program UT4 is designed to provide the appropriate ASCII-coded serial data to the data terminal by toggling the Q output of the CDP1802 microprocessor between V_{CC} and V_{SS} at the appropriate times. Again, the interface must convert the Evaluation Kit voltage levels to the EIA RS232C voltage levels used by the data terminal. This conversion is performed as follows. The logic 1 or negative EIA voltage is supplied to the data terminal when the CDP1802 output is toggled to a low voltage level (V_{SS}). The Q output going low drives the transistor Q2 into saturation. This action drives the base of Q3 to a high voltage level (V_{TTY}) putting Q3 into a cutoff state. As a result, no current flows through the collector of Q3, and EIA 3 is supplied with a negative voltage level (- 5 volts) as shown in Fig. 4.

The logic 0 or positive EIA voltage is supplied to the data terminal when the Q output of the CDP1802 is toggled to a high voltage level (V_{CC}). The Q output going high puts the transistor Q2 into cutoff. This action drives the base of Q3 to a low voltage level (V_{SS}) and puts Q3 into saturation. As a result, a positive voltage level (V_{TTY}) is supplied to EIA 3. In this manner, the interface transfers the data as bipolar serial voltage pulses in accordance with the EIA RS232C interface specifications.

SUMMARY OF INSTRUCTIONS FOR IMPLEMENTING THE EIA RS232C INTERFACE

1. Consult the instruction manual provided by the manufacturer of the data terminal for information on where to access the EIA RS232C interface signals.

2. Verify that the assembly procedure for this interface configuration has been followed by checking whether the following items have been correctly inserted and soldered on the Evaluation Kit PC card.

   Links: LK8A, LK9 (Make sure LK8B is open)
   Resistors: R3, R4, R15, R16, R17, R18, R19, R20, R21, R22, R23, R24, R25
   Capacitors: C8, C9
   Transistors: Q1, Q2, Q3

3. Connect the EIA RS232C interface signals from the data terminal to the Evaluation Kit as shown in Fig. 4. Verify these connections with the list in Table IV. Refer to Fig. 3 for Evaluation Kit connector pin placement.

4. Connect a -5-volt power supply to P1-1 of the Evaluation Kit.

FURTHER CONSIDERATIONS

The Evaluation Kit data terminal interface has been designed to provide a simple, flexible serial-data interface having a minimum of components. Most of the interface components are used in both the 20-mA current loop and the EIA RS232C interface configurations. For example, to input data to the Evaluation Kit, Q1 is used to detect the serial data in both configurations. To output data from the Evaluation Kit, Q2 is used in both configurations but Q3 only in the EIA RS232C interface.

The CDP1802 data-handling input $\overline{EF4}$ and the Q output are negative logic signals; that is, a low voltage level (V_{SS}) represents a binary 1 and a high voltage level (V_{CC}) represents a binary 0. For proper operation, therefore, the interface must provide the appropriate voltage levels to the microprocessor. The purpose of links LK8A and LK8B, which when inserted either merely invert or directly couple, respectively, the output of Q1 to the CDP1802, is to allow Q1 to operate correctly in each of the two interface configurations. Table V shows that the inversion of the signal at the collector of Q1 is necessary in the EIA RS232C interface configuration to provide to $\overline{EF4}$ the low voltage level (V_{SS}) representing a binary 1 and a high voltage level (V_{CC}) representing a binary 0.

A similar situation is present in the output interface circuit in that an inversion of the signal at the collector of transistor Q2 is necessary in order to provide the correct voltage levels to the data terminal. The transistor Q3 provides this inversion for the EIA interface, and the correct polarity output signal EIA data set 3 is derived from the collector of transistor Q3 on P1-Z of the Evaluation Kit. Table VI shows the output circuit conditions equivalent to the binary designations of the EIA convention.

One possible source of confusion is that Table I shows the mark-space convention or the equivalent binary designations listed under columns labelled "active" and "passive." When the TTY is in an apparently inactive or passive state (just after reset is depressed, for example, causing the CDP1802 Q output to go low), the Evaluation Kit interface for the 20-mA current loop is supplying current to the TTY printer input circuit. According to the mark-space convention, it is, therefore, also in an active state. This seeming contradiction can be explained by referring to Fig. 1, the example bit serial ASCII character. If this figure is compared with the states of the Evaluation Kit interface depicted in Tables V and VI, it can be seen that within the framing of the start and stop bits, the mark-space convention holds true. That is, for the binary 1 bits the Evaluation Kit 20-mA interface has current flowing and for the binary 0 bits no current flows. The apparent departure from the mark-space convention occurs only during

BINARY STATE	TTY 20-mA CURRENT LOOP	STATE OF Q1 COLLECTOR	EIA RS232C	STATE OF Q1 COLLECTOR
1	CLOSED OR CURRENT (SATURATE Q1)	V_{SS}	NEGATIVE VOLTAGE (CUTOFF Q1)	V_{CC}
0	OPEN OR NO CURRENT (CUTOFF Q1)	V_{CC}	POSITIVE VOLTAGE (SATURATES Q1)	V_{SS}

Table V - Signal state at collector of transistor Q1 for data terminal output of binary 1 and binary 0.

BINARY STATE	CDP1802 Q OUTPUT	TTY 20-mA CURRENT LOOP	STATE OF Q2	EIA RS232C	STATE OF Q2	STATE OF Q3 COLLECTOR
1	V_{SS}	CURRENT	SATURATED	NEGATIVE VOLTAGE	SATURATED; COLLECTOR= V_{TTY}	- 5 V
0	V_{CC}	NO CURRENT	CUTOFF	POSITIVE VOLTAGE	CUTOFF; COLLECTOR= V_{SS}	V_{TTY}

Table VI - Signal state at collector of transistors Q2 and Q3 for CDP1802 Q output of binary 1 and binary 0.

the relatively long asynchronous time period between the transmission of each ASCII character. During this period, no data is transmitted or received and the state of the interface signal is arbitrary. Consequently, because it is very simple to detect the interruption of a flow of current on a data transmission line (and, hence, a broken data link if one occurs), the telecommunications industry has adopted a convention of having the interface in the active (current flowing) or logical 1 state during this period between characters. As a result, when the TTY appears functionally inactive, its interface must be supplied with an active or current-flowing signal.

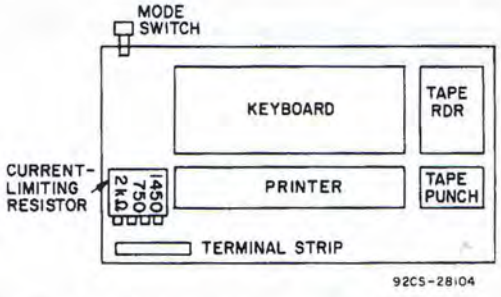


Fig. 5a - Location of terminal strip for model 33 Teletype data terminal.

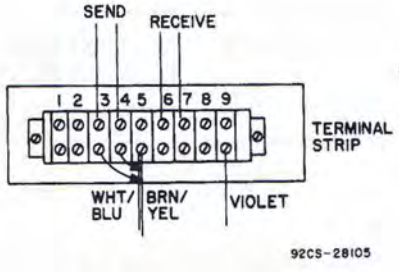


Fig. 5b - Terminal strip connections for 20-mA loop full-duplex operation.

CONVERTING A TELETYPE TERMINAL FROM HALF- TO FULL-DUPLEX OPERATION

To convert a Teletype terminal connected for half- duplex operation to full-duplex operation, the following modifications should be made.

1. Locate the black terminal strip in the back of the data terminal. See Fig. 5.

2. Move the brown/yellow and white/blue wires from pins 3 and 4 to pin 5.

CONVERTING A TELETYPE TERMINAL FROM 60-mA to 20-mA OPERATION

To convert a Teletype terminal connected for 60-mA operation to 20-mA operation, the following modifications should be made.

1. Locate the black terminal strip in the back of the data terminal. See Fig. 5.

2. Move the violet wire from pin 8 to pin 9.

3. Move the blue wire connected to the current source resistor (a flat green resistor having four tabs located to the right of the keyboard) from the 750-ohm tab to the 1450-ohm tab.

REFERENCES

1. INTERFACE BETWEEN DATA TERMINAL EQUIPMENT AND DATA COMMUNICATION EQUIPMENT EMPLOYING SERIAL BINARY DATA INTERCHANGE, EIA Standard RS232C, Electronic Industries Association, Washington, D.C.

2. CATALOG FOR 33 DATA TERMINALS, Teletype Corporation, Skokie, Ill.

3. COSMAC MICROKIT OPERATOR'S MANUAL, MPM-103, RCA Solid State Division, Somerville, N.J.

4. SILENT 700 ELECTRONIC DATA TERMINALS MODEL 733 ASR/KSR OPERATING INSTRUCTIONS, Texas Instruments Corp., Houston, Tex.

5. TELECOMMUNICATION TRANSMISSION HANDBOOK, Roger L. Freeman, 1975, John Wiley & Sons, New York, N.Y.

Microprocessor Products
Application Note
ICAN-6632

USE OF THE CDP1854 UART WITH RCA MICROPROCESSOR EVALUATION KIT CDP18S020 OR EK/ASSEMBLER-EDITOR DESIGN KIT CDP18S024

by R. G. Ott

The CDP1854 is a CMOS Universal Asynchronous Receiver/Transmitter (UART) circuit. It is designed to provide the necessary formatting and control for interfacing between serial and parallel data. For example, it can be used to interface between a peripheral or terminal with serial I/O ports and the 8-bit CDP1802 parallel data bus.

The CDP1854 can be used in the CDP18S020 Evaluation Kit or the CDP18S024 EK Design Kit to relieve the user's program of the task of formatting and controlling serial I/O data. It can also be used when high-speed serial data transfer at speeds up to 200K baud at a V_{DD} of 5 volts is needed. Space for a CDP1854 is provided in the user I/O area of the Kit. This application note describes several methods of interfacing the CDP1854 with the CDP1802 microprocessor and specifically explains the use of the CDP1854 in the CDP18S020 and CDP18S024 Kits.

DESCRIPTION OF THE CDP1854 FEATURES

The CDP1854 is capable of half duplex or full duplex operation, i.e., simultaneous conversion of serial input data to parallel output data and parallel input data to serial output data. It is fully programmable with externally selectable word length (5-8 bits), parity inhibit, even/odd parity, and 1, 1 1/2, or 2 stop bits. The transmitter converts parallel data to a serial word containing a start bit, the data bits, a parity bit (optional) and stop bit(s). The receiver converts a serial input word with start, data, parity, and stop bits into parallel data. It verifies proper code by checking parity and the receipt of a valid stop bit. Both the receiver and transmitter are double buffered.

The CDP1854 can be programmed to operate in one of two modes by using the mode control input (pin 2). When the mode input is low (MODE = 0) the device is functionally compatible with industry standard UART's such as the TR1602A and 6402. It is also pin compatible with these types, except that pin 2 is used for the mode control input instead of a V_{GG} = -12V supply connection. A block diagram for mode 0 operation is shown in Fig. 1. When the mode input is high (MODE = 1), the CDP1854 is directly compatible with the CDP1802 microprocessor system without

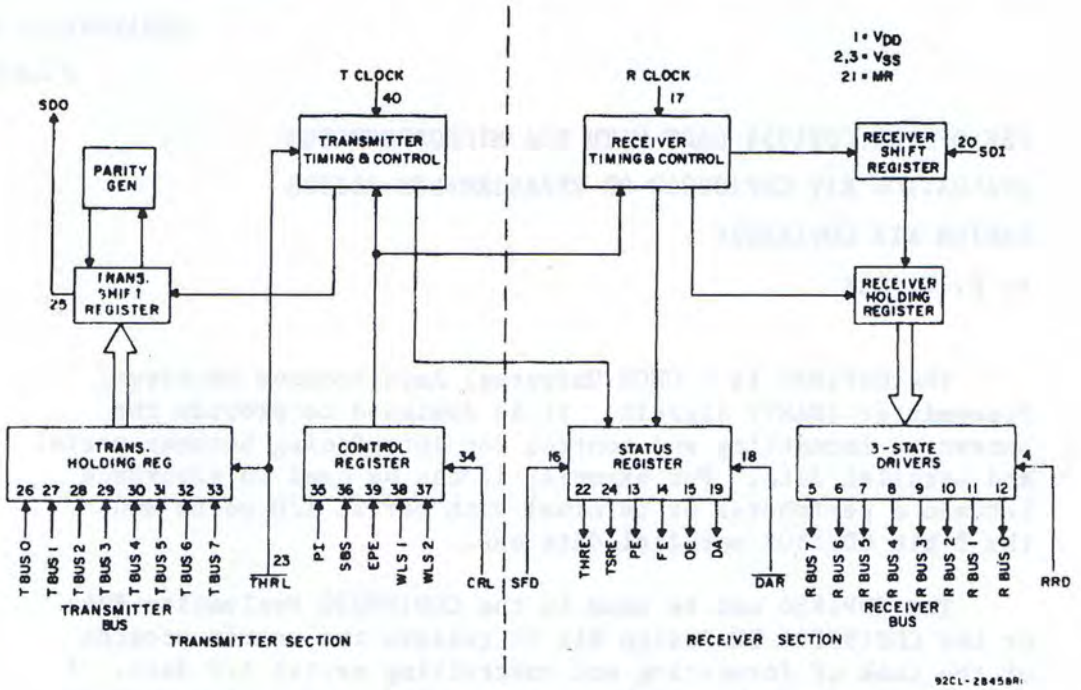


Fig. 1 - Standard Mode 0 block diagram.

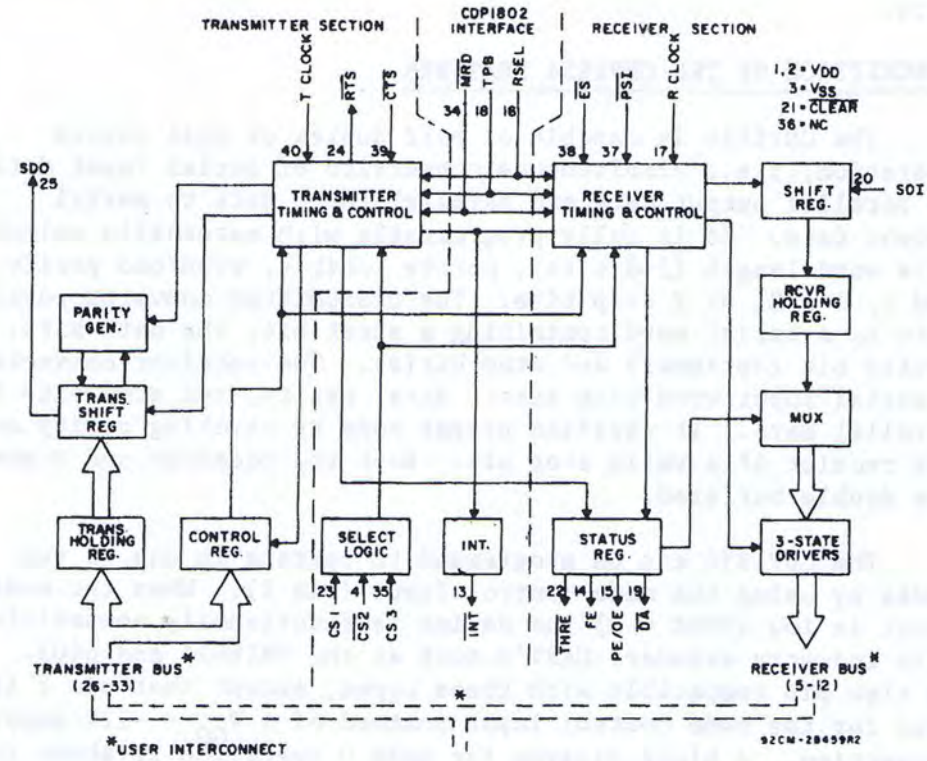


Fig. 2 - Mode 1 block diagram (CDP1802 compatible).

additional interface circuitry. All control and status bits, as well as the data bits, are set up or interrogated through the bus. A block diagram for mode 1 operation is shown in Fig. 2. For additional information refer to the CDP1854 data sheet.

USING THE CDP1854 TO INTERFACE THE CDP1802 MICROPROCESSOR IN THE CDP18S020 OR CDP18S024 KIT

When the mode input (pin 2) is high (Mode = V_{DD}), the CDP1854 interfaces directly with the CDP1802 microprocessor. This interfacing can be done either in the user I/O area or on a PC board which plugs onto the P2 connector of the Kit. A general CPU-UART connection diagram is shown in Fig. 3. Several options are shown in this figure.

The first option involves the choice of N-bit code which is used to select the CDP1854. One choice is to connect N0 to the RSEL input, N1 to the CS1 input, and N2 to the $\overline{CS2}$ input. The CS3 input is connected to V_{DD}. This alternative uses N decodes 2 and 3 (decoded by the CDP1854 chip). If the CDP18S021 Microterminal is used, N decode 3 will address the Microterminal. As long as the user's program does not output to the Microterminal, no conflict or display flickering will occur. If the CDP1852 output port is not used, an alternate connection is the following:

N0 to the CS1 input, N1 to the $\overline{CS2}$ input,
N3 to the RSEL input, and V_{DD} to the CS3 input.

The first alternative will be discussed in the remainder of this section.

The second option shown in Fig. 3 involves the connection to the microprocessor interrupt and flag lines. For interrupt driven I/O, the $\overline{INT}$ output from the CDP1854 is connected directly to the $\overline{INT}$ input of the CDP1802. Determination of whether an input request or an output request caused the interrupt can be made either by connecting $\overline{THRE}$ and $\overline{DA}$ to flag lines ($\overline{EF1}$ through $\overline{EF4}$) or by reading the UART's status register. A second approach is to test for input or output requests by polling flag lines. A third approach would be to connect the $\overline{DA}$ output to the microprocessor $\overline{INT}$ input and $\overline{THRE}$ to a flag line. For the remainder of this section transfer of data by polling flag lines will be discussed. A system in which $\overline{DA}$ is connected to the microprocessor $\overline{EF1}$ input and $\overline{THRE}$ is connected to the microprocessor $\overline{EF2}$ input will be used as an example.

In addition to the CDP1802 and CDP1854, only peripheral drive and sense circuitry and a clock or baud-rate generator circuit is necessary to complete the interface between the CDP1802 and a terminal.

A schematic diagram of the parallel to serial I/O interface is shown in Fig. 4. Table I lists a machine language routine for setting the UART's Control Register and continuously outputting the data byte in memory location 27 to a terminal until an input character is received and stored in memory location 28. The program then branches to the beginning of the Kit Utility Program (memory location 8000). A flow chart for this program is shown in Fig. 5. Correct program operation can be verified by observing that the terminal continuously prints the character (in this example "J") whose ASCII bit equivalent is listed in the program at address 14 until a key on the terminal is depressed. The program will then transfer control to the Kit Utility Program and the ASCII bit equivalent of the input character can be read from memory location 28. Proper operation will verify both correct hardware and software.

I/O SYSTEMS USING THE CDP1854 ON THE CDP18S020 ON THE CDP18S024

One or more CDP1854 UART's can easily be interfaced with the CDP18S020 or CDP18S024 Kit. The system described in the previous section of this note is an example of a single-level I/O system with one CDP1854, a CDP1852 used as an input port, and a CDP1852 used as an output port. The following CDP1802 I/O instructions with the corresponding N-line decodes are used in this system:

I/O Instruction	N - Decode	Device (Register) Addressed
62	2	CDP1854 (THR) - Transmitter data
63	3	CDP1854 (Control)
65	5	CDP1852 - Output Port
6A	2	CDP1854 (RHR) - Receiver Data
6B	3	CDP1854 (Status)
6E	6	CDP1852 - Input Port

A maximum of three CDP1854's can be used in a single level I/O system. Such a system would leave only one I/O instruction for data transfer to or from a CDP1852 I/O Port. A larger number of I/O devices can be connected to a CDP18S020 or CDP18S024 Kit by using a two level I/O Structure. A system with 2 I/O Ports (included on the CDP18S020 and CDP18S024 Kits) and eight UART's is shown in Fig. 5. A CDP1852 I/O Port is used as a chip select latch, and the CD4028A included in the Kit (U7) is used as an N-bit decoder. This system uses the following CDP1802 I/O instructions with the corresponding N-line decodes:

I/O Instruction	N - Decode	Device (Register) Addressed
62	2	Selected CDP1854 (THR) - Transmitter data
63	3	Selected CDP1854 (Control)
65	5	CDP1852 - Output Port
67	7	2 - level I/O device select
6A	2	Selected CDP1854 (RHR) - Receiver data
6B	3	Selected CDP1854 (Status)
6E	6	CDP1852 - Input Port

If output port (U4) is not used, it can be used to replace the two level I/O chip select latch. I/O Instruction 65 will then be the two-level I/O select instruction.

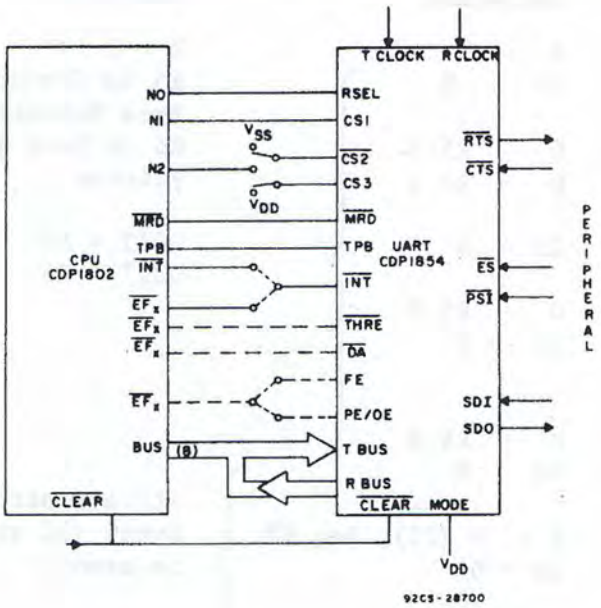


Fig. 3 - CDP1802/CDP1854 connection diagram.

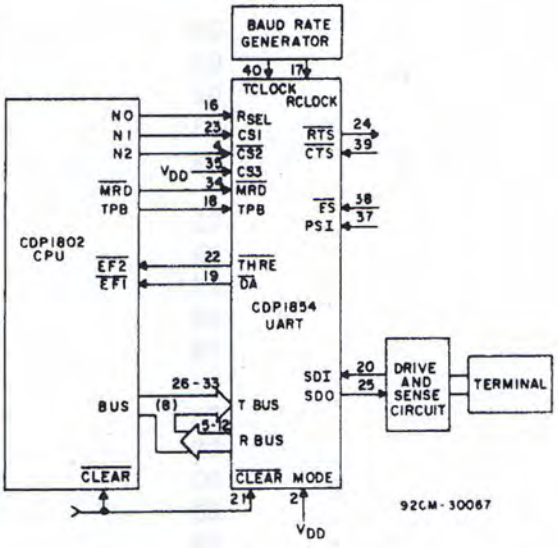


Fig. 4 - Interface of CPU CDP1802 to data terminal using UART CDP1854.

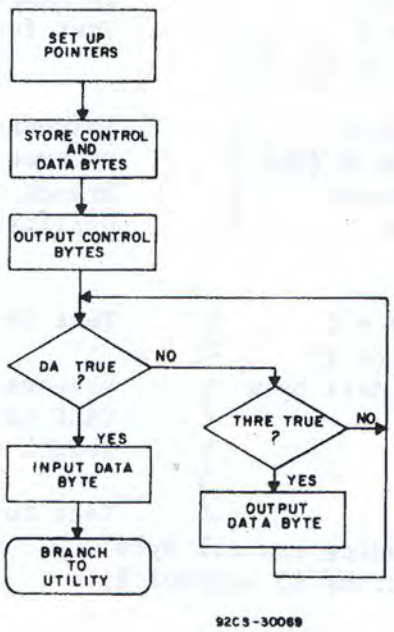


Fig. 5 - Program flow chart.

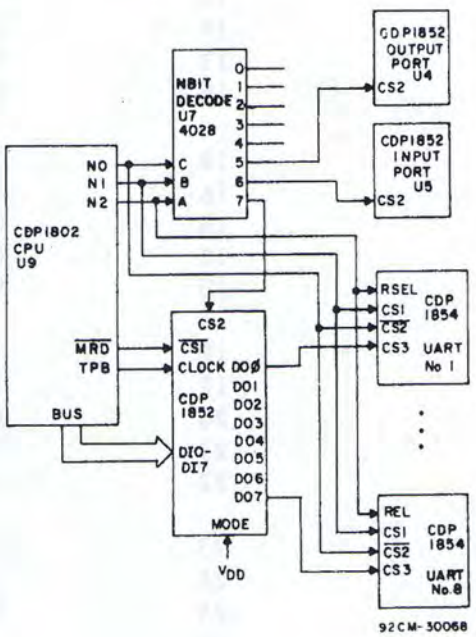


Fig. 6 - Diagram of two-level I/O system.

TABLE I - CDP1854 INTERFACE TEST PROGRAM

Memory Address	Byte	Operation	Comments
00	E5	5 → X	X = 5
01	F8	00 → D	R5 is Control
02	00		Byte Pointer
03	B5	D → R5.1	R6 is Data Byte
04	B6	D → R6.1	Pointer
05	F8	25 → D	0025 → R5
06	25		0027 → R6
07	A5	D → R5.0	
08	F8	27 → D	
09	27		
0A	A6	D → R6.0	
0B	F8	80 → D	
0C	80		Store Control
0D	73	D → M (25), Dec R5	Bytes (3D and 80)
0E	F8	3D → D	in memory
0F	3D	Control Byte	
10	55	D → M (24)	
11	63	Output 3D	Output Control
12	63	Output 80	bytes to CDP1854
13	E6	6 → X	X = 6
14	F8	4A → D	Store data byte
15	4A	Data byte	(4A = J (ASCII)
16	56	D → M (27)	in memory location 30
17	3C	If DA = 0	Test for DA
18	1E	Branch to 1E	
19	16	41 → R6.0	Response if
1A	6A	Input to M (28)	DA true
1B	C0	Long Branch	Branch to
1C	80	to 8000	Utility
1D	00		
1E	3D	If THRE = 0	Test for THRE
1F	17	Branch to 17	
20	62	Output data byte	Response if
21	26	Dec R6	THRE true
22	30	Branch	Branch to
23	17	to 17	Test for DA
24	Location for storing control Byte		
25	Location for storing 80 Control Byte		
26			
27	Location for storing Output Data Byte		
28	Location for storing Input Data Byte		

Microprocessor Products
Application Note
ICAN-6536

USE OF CMOS ROM'S CDP1831 AND CDP1832 WITH THE RCA MICROPROCESSOR EVALUATION KIT CDP18S020

by A. W. Young

The CDP1800 family of microprocessor products includes two 4096-bit static CMOS mask-programmable read-only memories, the CDP1831 and CDP1832. Each is organized as 512 8-bit words but they differ in addressing structure. The CDP18S020 Evaluation Kit is designed to accept the two ROM's in prewired locations and will also accomodate expanded ROM systems in the User I/O area. The Evaluation Kit is provided with a factory-programmed CDP1832 which contains the Utility Program UT4.

This application note describes the operation and design of CDP1831-and CDP1832-based read-only memory systems in the CDP18S020 Evaluation Kit.

DESCRIPTION OF CDP1831 FEATURES

The CDP1831 interfaces directly with the CDP1802 without additional components. The CDP1831 responds to a 16-bit address multiplexed on 8 address lines (MA0-MA7) 8 bits at a time. Fig. 1 shows how the address lines are multiplexed and latched to form the 16-bit address. The most significant address byte is latched internally by either a positive or negative (user mask programmable) level of TPA. For compatibility with the CDP1802, this level should be programmed negative, as also indicated in Fig. 1.

Fig. 2 shows the internal allocation of the 16 address lines. The seven most significant address lines select one of 128 512-byte sectors of the 64K microprocessor memory space. The sector address is equivalent to a ROM select and is user-programmable for a specific CDP1831. The seven-bit ROM select code is "ANDed" with the three chip selects (CS1, CS2, and $\overline{\text{MRD}}$) to enable a given ROM. This signal is provided on an output pin ($\overline{\text{CEO}}$) of the CDP1831 to indicate when the ROM is enabled. The nine least significant address lines are decoded to select one of 512 bytes in the ROM (sector).

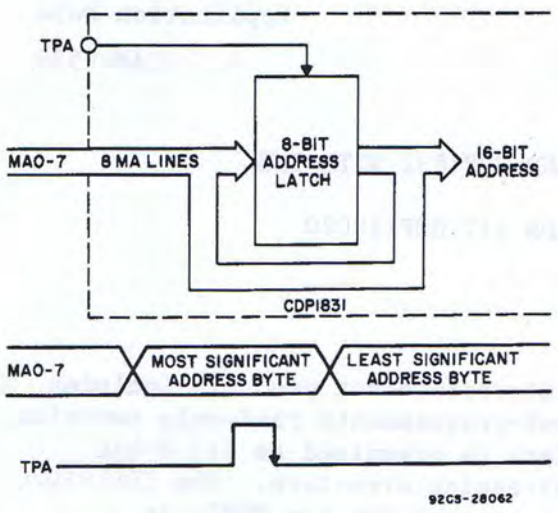


Fig. 1 - CDP1831 ROM address line multiplexing.

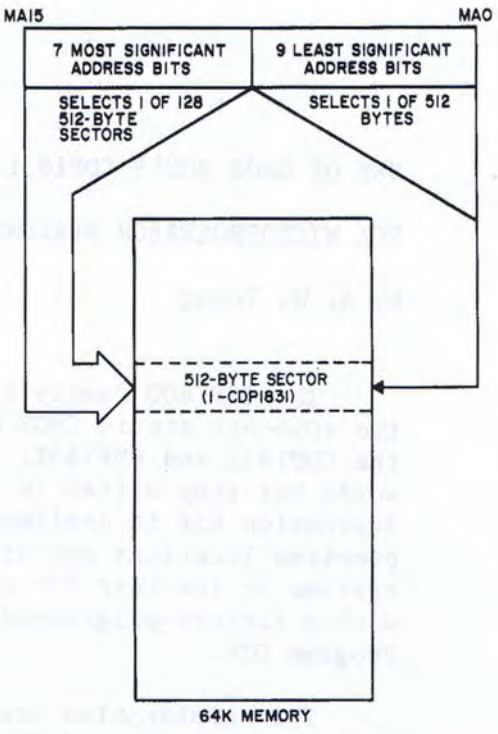


Fig. 2 - Internal allocations of 16 address lines.

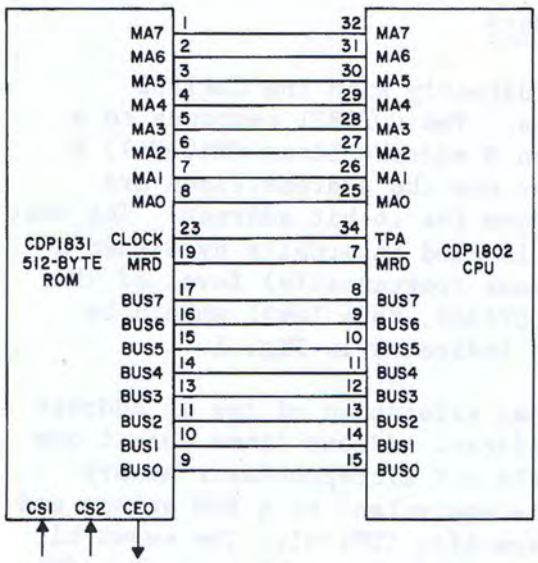


Fig. 3 - Interconnections of ROM CDP1831 to microprocessor CDP1802.

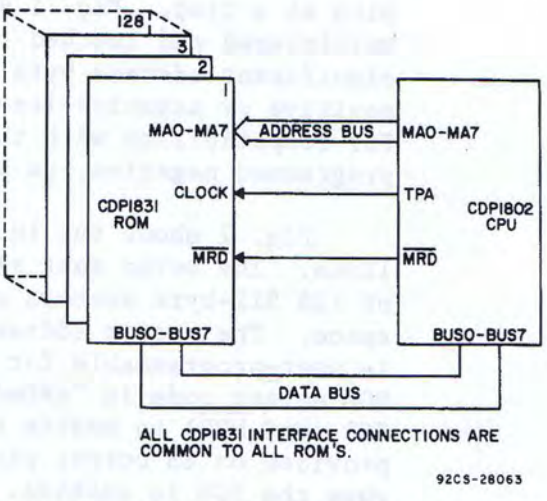


Fig. 4 - Multiple CDP1831 ROM system.

In summary, the CDP1831 responds to a 16-bit address; this address specifies one of 128 memory sectors, which is fixed for a given ROM, and one of 512 contiguous bytes within the specified ROM.

There are three important features of the CDP1831 which result from this addressing structure. First, it is directly compatible with the CDP1802 multiplexed address bus. The specific connections are shown in Fig. 3. Second, a ROM system of from 512 to 64K bytes can be configured which is directly compatible with the CDP1802 and requires no address decoding. This system is shown in Fig. 4. Third, when the ROM is selected, the CEO output goes high and can be used directly to disable a RAM system. A minimal system consisting of the CDP1802 CPU, CDP1824 32-byte RAM, and CDP1831 512-byte ROM is shown in Fig. 5.

Reading data out of the CDP1831 follows a standard procedure. The device is selected by clocking the proper sector address into the address latch. The tri-state output buffers are enabled by the proper combination of the three chip selects, CS1, CS2, and $\overline{MRD}$. The chip-select enable polarities are user mask programmable. Valid data will appear at the output within one access time (t_{AA}) from the last address change.

Operating conditions and static and dynamic characteristics for the CDP1831 are given in the device data sheet. The CDP1831 is available in two versions. The CDP1831D has a recommended operating voltage range of 3 to 12 volts; the CDP1831CD has a recommended operating voltage range of 4 to 6 volts. Both versions are functionally identical and are supplied in 24-lead dual-in-line packages.

APPLICATION OF CDP1831 IN EVALUATION KIT ROM SYSTEMS

The CDP18S020 Evaluation Kit has been prewired to accept the CDP1831 ROM in position U1. Fig. 6 shows the U1 pin connections. The eight CDP1802 memory address lines (MA0-MA7) and TPA are wired to the appropriate ROM pins. The CDP1831 data outputs are connected directly to the data bus. The CS1 and CS2 inputs are connected permanently high, and the $\overline{MRD}$ input is connected to the CDP1802 $\overline{MRD}$ output. As a result, the ROM puts data on the bus when $\overline{MRD}$ = 0. The chip enable output CEO is connected to the $\overline{E}$ (pin 1 of U22) control input of the RAM system decoder. When the ROM is addressed (enabled), the CEO output goes high and disables the RAM system. The CEO output can be used to disable the CDP1832 Utility Program ROM (U2) as shown in Fig. 7. Link 3 must be broken and the indicated gating inserted. The effect of the extra gating is to "OR" the CEO output with

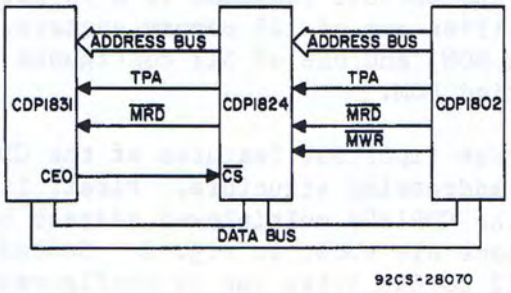


Fig. 5 - Minimal microprocessor memory system consisting of ROM CDP1831 and RAM CDP1824.

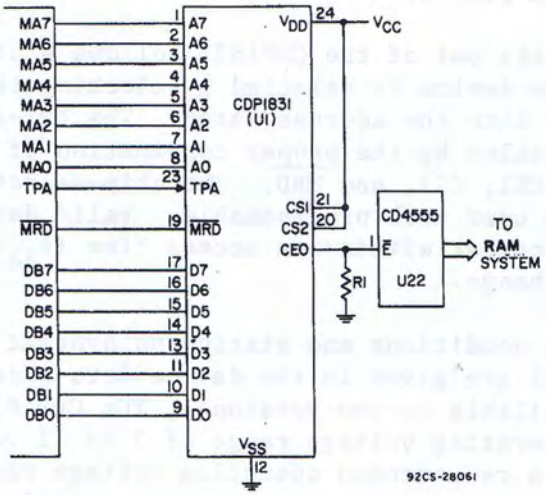


Fig. 6 - Pin connections for CDP1831 ROM in U1 location of Evaluation Kit.

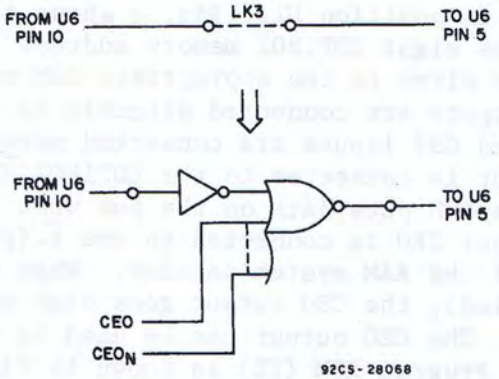


Fig. 7 - Use of CDP1831 CEO output to disable the CDP1832 ROM (U2) Utility Program.

the existing CDP1832 $\overline{CS}$ signal. These controls assure the ability to place the CDP1831 sector address in any of the possible 128 locations regardless of the RAM or ROM memory space allocation. Note that a pull-down resistor (R1 = 22 K Ω) is on the CEO line to assure proper operation of the RAM system when the CDP1831 ROM is removed. When the system operates with a ROM in the U1 location, this resistor may be removed.

The CDP1831 V_{DD} (pin 24) is connected to the Evaluation Kit V_{CC}. This connection permits maximum memory-system flexibility with or without the CDP1831.

To use the U1 position for the CDP1831, the device is simply inserted in the location as indicated on the PC card. (Optionally, R1 = 22K Ω can be removed). Proper operation can be verified by use of the ?M[Starting Address]Δ[FF] command of UT4 to list the memory contents. This check assumes that the CDP1831 does not occupy locations 8000_{16} to $81FF_{16}$.

Expanding the ROM System on the Evaluation Kit is especially easy. In the User I/O section of the PC card, the CDP1802 memory address bus, data bus, $\overline{MRD}$, and TPA signals are provided on the left side. Multiple CDP1831's (up to 12) can be inserted in the pre-drilled locations and interfaced to the address and data busses. Multiple CEO outputs can be combined with a standard AND gate to generate a ROM system CEO. Example devices for this function are the CD4081, CD4082, and CD4085.

It should be noted that memory pattern generation and verification is possible in the CDP18S020 RAM system by using the write-protect and battery hold-up features. Once a pattern has been verified, it can be permanently stored by the custom masking of one or more CDP1831 ROM's.

DESCRIPTION OF CDP1832 FEATURES

The CDP1832, like the CDP1831, is a static 4096-bit mask-programmable COS/MOS read-only memory organized as 512 8-bit words. It is conventionally organized, requiring nine address lines and a chip select $\overline{CS}$ to read one of 512 8-bit words onto a bidirectional data bus. Data is available within one access time (t_{AA}) from the last address change. The chip-select control $\overline{CS}$ functions as an output disable. The CDP1832 is pin-compatible with the 2704 512-word x 8-bit erasable and electrically reprogrammable ROM. It can be directly inserted into a 2704 socket without any PC board changes. Additional details on the CDP1832/2704 compatibility and design considerations can be found in the RCA Application Note entitled "Use of Erasable and Electrically Reprogrammable ROM 2704 With RCA Microprocessor Evaluation Kit CDP18S020", ICAN-6540.

A functional diagram of the CDP1832 is shown in Fig. 8. Operating conditions and static and dynamic characteristics are given in the device data sheet. The CDP1832 is available in two versions. The CDP1832D has a recommended operating voltage range of 3 to 12 volts; the CDP1832CD, has a recommended operating voltage range of 4 to 6 volts. Both versions are functionally identical and are supplied in 24-lead dual-in-line packages.

APPLICATION OF CDP1832 IN EVALUATION KIT ROM SYSTEMS

The CDP18S020 Evaluation Kit has been prewired to accept the CDP1832 ROM in position U2. Fig. 9 shows the U2 pin connections. The basic Evaluation Kit is supplied with a CDP1832 factory-programmed with the Utility Program UT4. Because of the desire to have UT4 in the upper half of memory, the circuitry which interfaces with the CDP1832 in position U2 selects the ROM when either A15 8000_{16} or RUN U are true. The effect is as follows: when RUN U is activated, the ROM (UT4) is selected and the first 4 locations of the Utility Program initialize the most significant byte of the CDP1802 program counter to 80_{16}. By the time the RUN U pushbutton is released, A15=1 and the ROM continues to be selected. As shown in Fig. 9, gates U6A and U6B control the CDP1832 chip select $\overline{CS}$. U6A performs the logic for starting the Utility Program in 8000_{16}. U6B AND's the enable request with MRD which assures that the ROM puts data on the data bus at the proper time. In addition, a UT4 RAM-select-input disables the ROM when UT4 writes data in the CDP1824 Utility RAM.

Because the CDP1832 is compatible with the 2704 EPROM, location U2 has been prewired for the necessary V_{BB} and V_{DD} voltages required by the 2704. These pin connections are available at the SYSTEM CONNECTOR (P1). The CDP1832 does not require any connections to these pins; however, if they have been connected for 2704 operation they need not be disconnected for proper operation of the CDP1832. The CDP1832 V_{DD} supply (pin 24) has been connected to the Evaluation Kit V_{CC}.

Expanded CDP1832 ROM-based memory systems are easily constructed in the User I/O section of the PC card. In addition to wiring ROM locations, address latch and decode functions must be provided. A sample 2K ROM system which can be constructed in the User I/O section of the PC card is shown in Fig. 10.

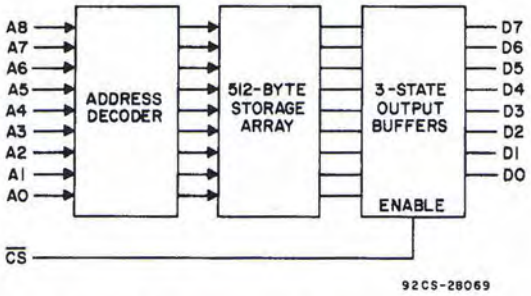


Fig. 8 - Functional diagram of CDP1832 512-word x 8-bit static read-only memory.

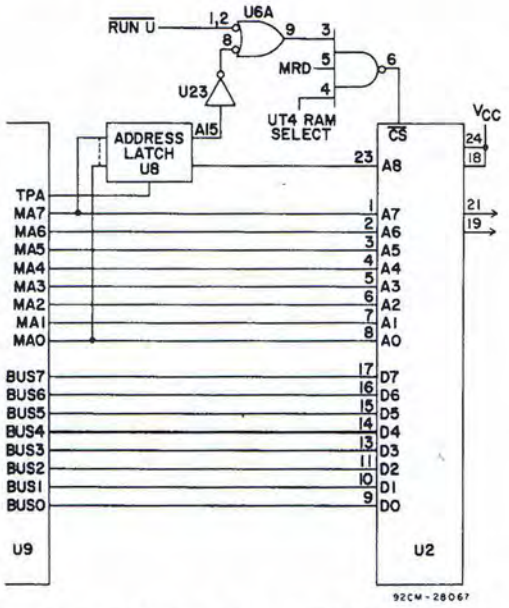


Fig. 9 - Pin connections for CDP1832 ROM in U2 location of Evaluation Kit.

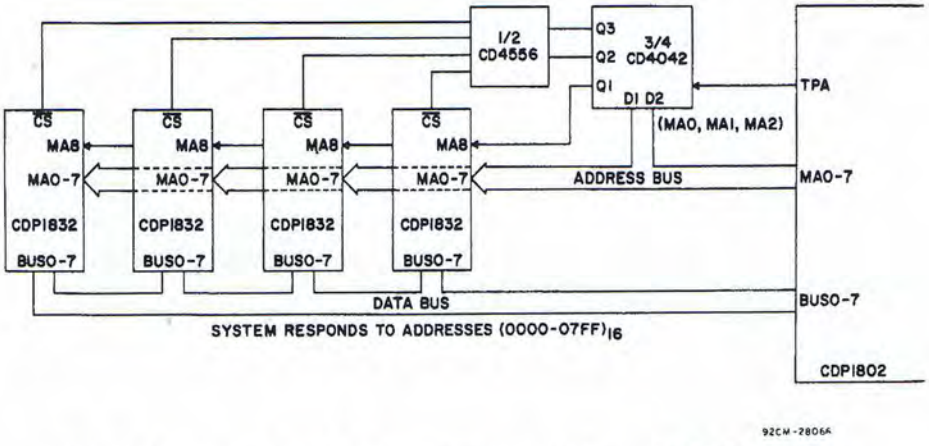


Fig. 10 - Sample 2K ROM system using CDP1832 ROM's.

Microprocessor Products

Application Note

ICAN-6537

USE OF CMOS RAM CDP1824 WITH

RCA MICROPROCESSOR EVALUATION KIT CDP18S020

by J. R. Oberman

The CDP1824, a 32-byte, static, silicon-gate CMOS, random-access memory, is intended for use in microprocessor systems requiring a minimal amount of writable storage. It is directly compatible with the CDP1802 microprocessor, requiring no additional interface components, and operates at maximum microprocessor speeds. In many systems the availability of memory in 32-byte increments will prove to be a cost-effective means of implementing working space or stack storage requirements.

This note describes the CDP1824, its application in the CDP18S020 Evaluation Kit, and presents examples of how the CDP1824 can be combined with the CDP1831 ROM to form efficient ROM-RAM systems.

DESCRIPTION OF CDP1824 FEATURES

The CDP1824 is an 18-pin device consisting of five address inputs, an output disable control ($\overline{MRD}$), a memory write control ($\overline{MWR}$), a chip-select control ($\overline{CS}$), eight common data input-output terminals, and two voltage connections. The CDP1824 requires no precharge or clocked signals for proper operation. The CDP1824 electrical characteristics are given in its data sheet.

The five address inputs MA0-MA4 are buffered and decoded to uniquely select one of 32 bytes. The eight input-output data lines can interface directly with the microprocessor bidirectional data bus. Operation is determined by the state of the $\overline{MWR}$ and $\overline{MRD}$ terminals. These inputs can also be driven directly from the CDP1802 microprocessor. When $\overline{MRD}$ = 0, the output drivers are enabled, and the output data corresponds to the addressed byte. If $\overline{MRD}$ = 1 and $\overline{MWR}$ = 0, the contents of the data bus are stored at the addressed location. A chip-select input signal $\overline{CS}$ is required to enable the memory. Table I indicates the operational modes of the RAM and Fig. 1 shows the functional block diagram.

The RAM is available in two functionally identical versions. The CDP1824D has a recommended operating voltage range of 3 to 12 volts; the CDP1824CD a recommended operating voltage range of 4 to 6 volts. Both devices operate over the full military temperature range of $-55^{o}C$ to $+125^{o}C$, and both have the same dynamic characteristics.

APPLICATION OF CDP1824 IN EVALUATION KIT

The CDP1824 is used in the CDP18S020 Evaluation Kit by the Utility Program to provide CDP1802 register storage. This application of the RAM is useful in program debugging and illustrates a cost-effective means of implementing minimum storage requirements.

The memory is automatically loaded by the Utility Program upon the initiation of the RUN U control. Memory contents can be examined by use of the Utility Program "?M" command. Refer to the Utility Program section of the Evaluation Kit Manual for the RCA CDP1802 COSMAC Microprocessor, MPM-203 for a detailed description of the Utility Program commands and the register-save feature. The CDP1824 is located at the memory addresses $8C00_{16}$ to $8C1F_{16}$.

In the Evaluation Kit the CDP1824 address, $\overline{MRD}$, and $\overline{MWR}$ terminals are connected directly to the corresponding terminals of the CDP1802. The RAM input-output terminals are connected directly to the bidirectional data bus. The $\overline{CS}$ input is used to control the selection of the memory.

Fig. 2 shows how the CDP1824 chip-select decoding is implemented. The eight higher-order address bits are latched in the CDP1852 (Location U8 in the Evaluation Kit) by TPA. The CD4555, a dual binary to 1 of 4 decoder, is used to decode address bit MA8 and MA9 in one section and MA10 and MA11 in the other section. These decodes are used by the CDP1822S RAM system. However, the decode of MA11 and MA10 is also used as part of the CDP1824 chip-select decode together with the MA15 output from the address latch. These two signals are combined in a NAND gate whose output is connected to the $\overline{CS}$ terminal of the CDP1824. As a result, the CDP1824 will be selected whenever MA15·MA11·MA10 is true.

The CDP1824 is spaced 2560 memory locations above the end of the Utility Program. Therefore, if desired, additional memory can be located at 8200_{16} to $8BFF_{16}$ without the need to inhibit the CDP1824.

If it is desired to locate additional memory above location $8C1F_{16}$, the CDP1824 must be inhibited. Selection of the CDP1824 can be inhibited by disabling the CD4555

Function	$\overline{CS}$	$\overline{MRD}$	$\overline{MWR}$	Data Pins Status
READ	0	0	X	Output: High/ Low Dependent on Data
WRITE	0	1	0	Input, Output Disabled
Not Selected	1	X	X	Output Disabled High-Impedance State
Standby	0	1	1	

Logic 1 = High Logic 0 = Low X = Don't Care

Table I - CDP1824 RAM operational modes.

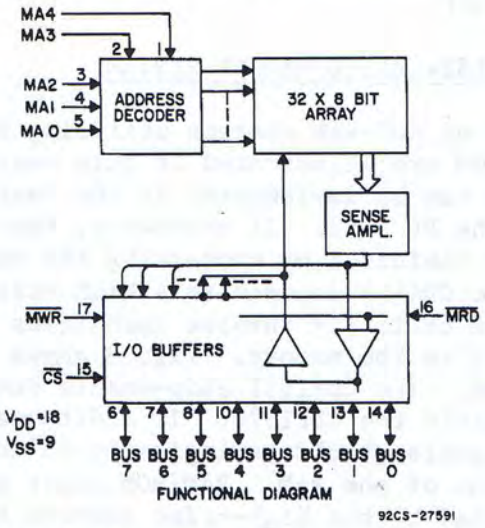


Fig. 1 - Functional diagram of CDP1824 32-word x 8-bit static COS/MOS random-access memory.

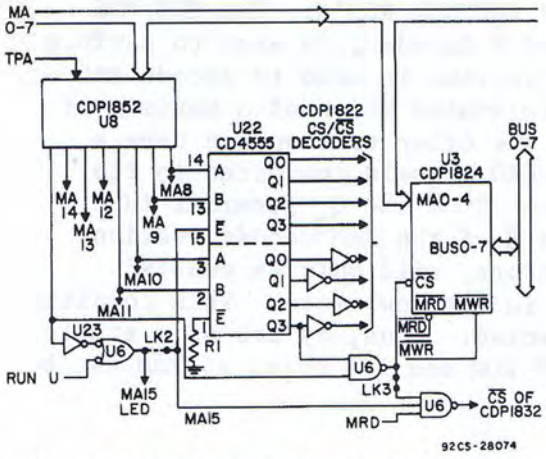


Fig. 2 - Implementation of chip-select decoding for the CDP1824 RAM.

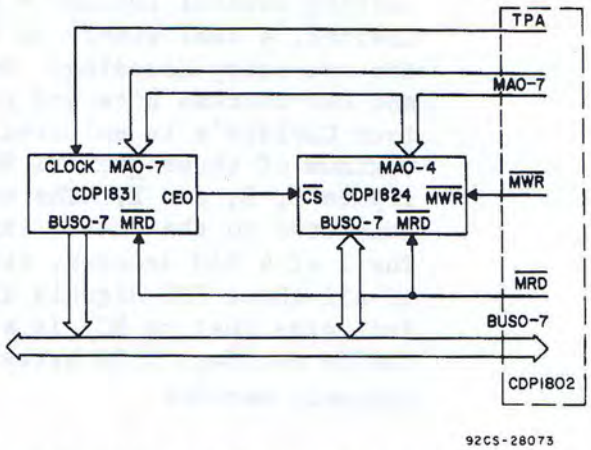


Fig. 3 - Minimum memory system utilizing RAM CDP1824 and ROM CDP1831.

decoder by applying a high voltage level to the enable terminal, pin 1 of the CD4555, whenever the add-on memory at location $8C20_{16}$ or above is selected.

For memory expansion above $81FF_{16}$, the CDP1832 Utility Program ROM (location U2) must be inhibited. Provisions have been made in the Evaluation Kit to facilitate the necessary logic changes; LINK "LK3" should be removed to disconnect MA15 from the NAND gate which forms the $\overline{CS}$ input for the Utility Program ROM. Modified $\overline{CS}$ logic can be externally generated and applied to this point to accomodate additional memory.

DESIGN OF CDP1824-BASED MEMORY SYSTEM

Examples of ROM-RAM systems utilizing the CDP1824RAM and CDP1831 ROM are illustrated in this section. If desired, these systems can be implemented in the User I/O area provided on the PC card. If necessary, the existing RAM's can easily be inhibited by connecting the enable terminal, pin 15, of the CD4555 decoder to a high voltage level. These examples basically involve techniques for generating the $\overline{CS}$ command to the memory. Fig. 3 shows a minimum RAM-ROM system. The CDP1831 chip-enable output CEO signal is used to enable the CDP1824. If additional ROM's are used, CEO output signals should be logically OR'ed and connected to the $\overline{CS}$ input of the RAM. RAM/ROM space may also be uniquely defined by the high-order address bit, as illustrated in Fig. 4. This technique is the one used in the Evaluation Kit.

Fig. 5 illustrates a simple technique for interconnecting several CDP1824's and CDP1831 ROM's. The COS/MOS CD4556B, a dual binary to 1 of 4 decoder, is used to perform the necessary decoding. One section is used to decode MA5 and MA6 address bits and to determine which of a maximum of four CDP1824's is selected. The other section can have a maximum of three CDP1831 ROM CEO signals connected to its inputs A, B, and $\overline{E}$. The output from the $\overline{Q}_0$ terminal is connected to the enable input $\overline{E}$ of the RAM decode section. The 1 of 4 RAM decoder, therefore, will only be enabled if all three CEO signals are in the low state. This condition indicates that no ROM is selected. Thus, by use of a single CD4556 decoder, 1536 bytes of ROM and 128 bytes of RAM can be uniquely decoded.

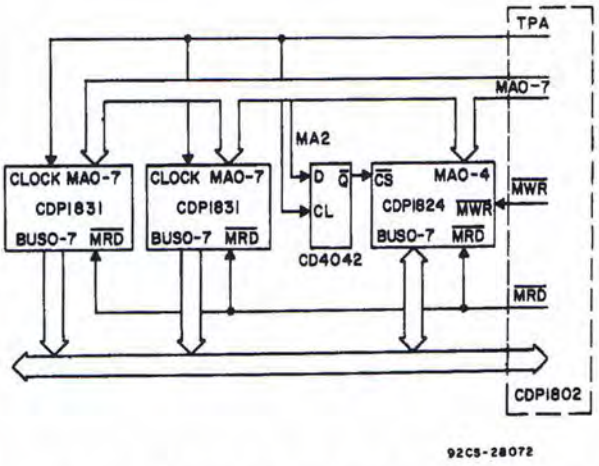


Fig. 4 - Multiple ROM/RAM memory system.

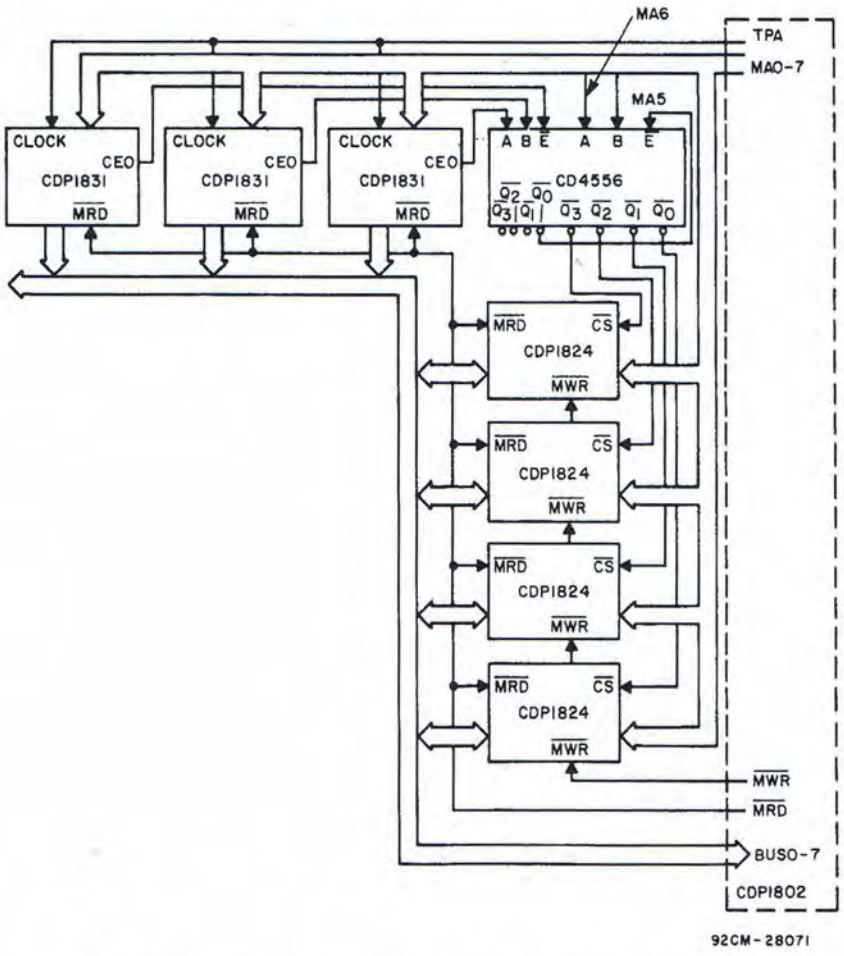
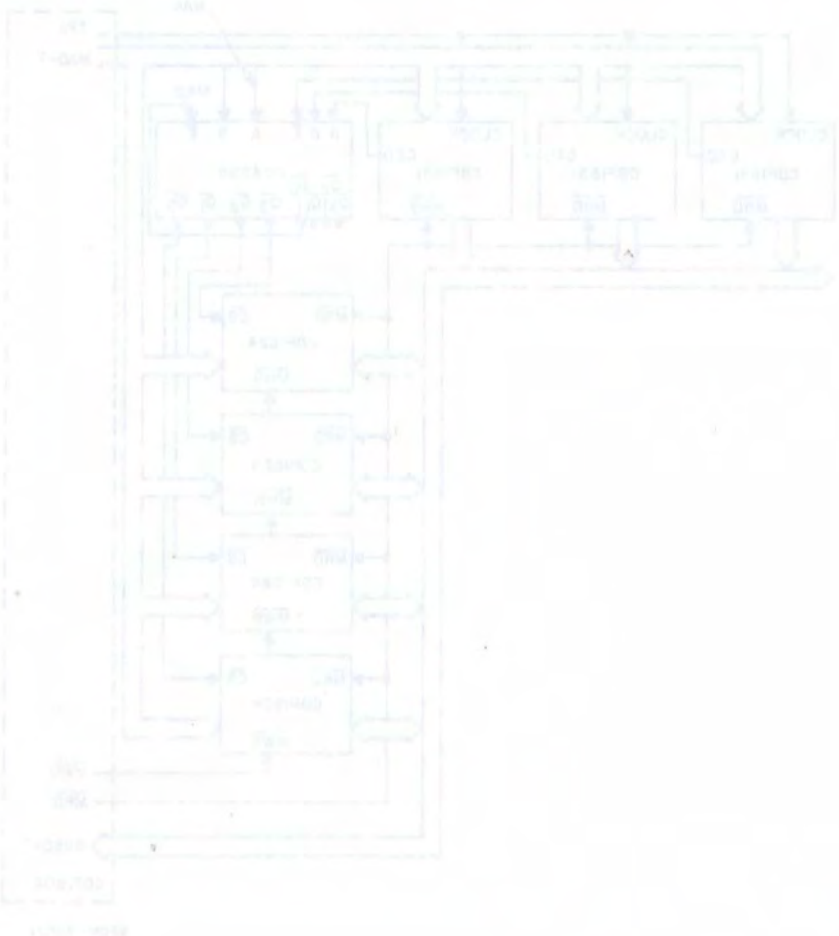


Fig. 5 - Technique for interconnecting several CDP1824 RAM's and CDP1831 ROM's.



Microprocessor Products

Application Note

ICAN-6539

USE OF CMOS-SOS RAM CDP1822S WITH

RCA MICROPROCESSOR EVALUATION KIT CDP18S020

by J. R. Oberman

The CDP1822S is a 256 x 4, CMOS-SOS, static, random-access memory. It can be used directly in CDP1802 microprocessor systems such as the CDP18S020 Evaluation Kit and requires no additional interface components. The CMOS-SOS technology has all the advantages of CMOS plus the high-speed, low-dynamic-power performance of SOS.

The CDP18S020 Evaluation Kit is designed to accept 32 CDP1822 RAM's in prewired locations forming 4K bytes of RAM storage. The Evaluation Kit is provided with two CDP1822S's, 256 bytes of RAM storage, and the necessary decoders to facilitate expansion, if desired, to 4K.

This Application Note describes the CDP1822S, its operation, and its application in the CDP18S020 Evaluation Kit.

DESCRIPTION OF CDP1822S FEATURES

The CDP1822S is contained in a 22-lead dual-in-line package consisting of eight address inputs, an output disable control $\overline{MRD}$, a memory write control $\overline{MWR}$, two chip-select controls $\overline{CS1}$, CS2, four data-input and four data-output terminals, and two voltage connections.

The eight address inputs, MA0-MA7, are buffered and decoded to uniquely select 1 of 256 four-bit words. The four data-output terminals are driven from three-state drivers enabled by the $\overline{MRD}$ signal when the device is selected. Valid data appears at the output ($\overline{MRD}$ = 0) of the CDP1822S in one access time following the latest address change to a selected chip. The output data is valid until either the $\overline{MRD}$ signal goes high or the device is deselected ($\overline{CS1}$ = 1 or CS2 = 0). Operation is determined by the state of the $\overline{MRD}$ and $\overline{MWR}$ lines. These inputs are driven directly from the CDP1802 microprocessor. The operational modes are listed in Table I and a functional diagram of the memory is shown in Fig. 1. The CDP1822S requires no precharge or clocked signals for proper operation.

Function	$\overline{MWR}$	$\overline{CS1}$	CS2	$\overline{MRD}$	Data Out DO
READ	1	0	1	0	Storage State of Addressed Cell
WRITE (Output Disabled)	0	0	1	1	High-Impedance
WRITE	0	0	1	0	New Data In State
Standby	X	1	X	X	High-Impedance
	X	X	0	X	High-Impedance
	1	0	1	1	High-Impedance

Logic 1 = High Logic 0 = Low X = Don't Care

Table I - CDP1822S operational modes.

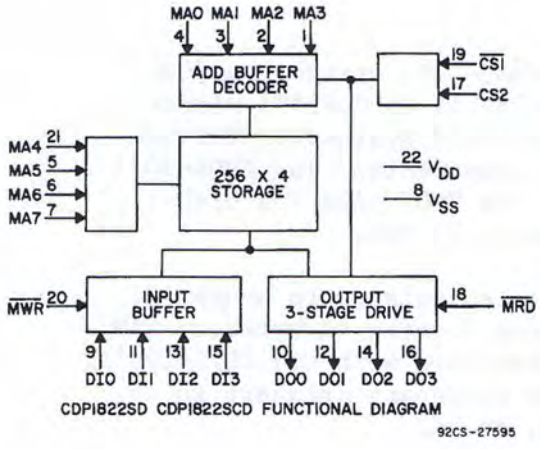


Fig. 1 - Functional diagram of CDP1822S 256-word x 4-bit static COS/MOS silicon-on-sapphire random-access memory.

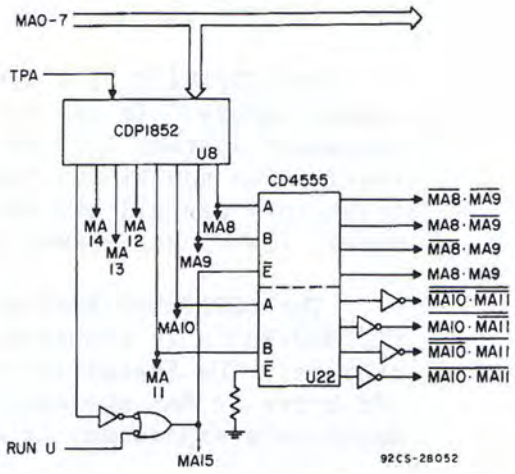


Fig. 2 - Interconnections of CDP1822S RAM with CDP1802 microprocessor in Evaluation Kit CDP18S020 system.

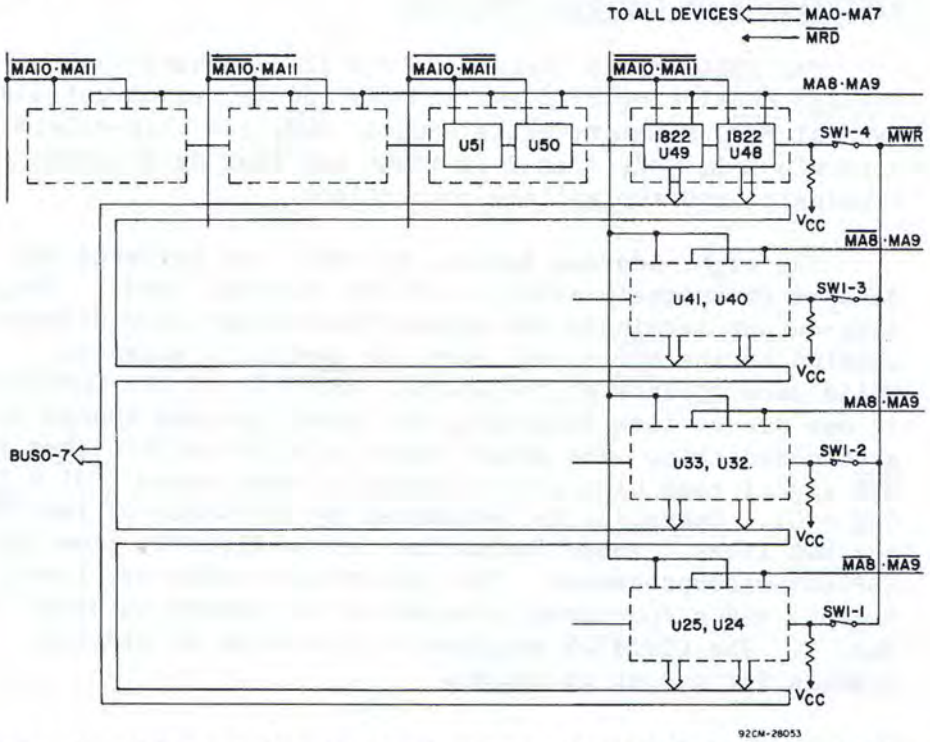


Fig. 3 - Address decode logic for full CDP1822S RAM system.

The CSP1822S is available in two versions. One, the CDP1822SD, has a recommended operating voltage range of 4 to 10 volts. The other, the CDP1822SCD, has a recommended operating voltage range of 4 to 6 volts. Both units are functionally identical and have the same dynamic characteristics.

The electrical characteristics of the CDP1822S are given in its data sheet. It should be noted that because the CDP1822SD has a maximum recommended operating voltage of 10 volts, the Evaluation Kit V_{CC} should be limited to 10 volts when it uses CDP1822S RAM's.

APPLICATION OF CDP1822S IN EVALUATION KIT MEMORY SYSTEM

The CDP18S020 Evaluation Kit is prewired for 4K bytes of CDP1822S, 256 x 4 RAM storage at locations $(0000)_{16}$ - $(0FFF)_{16}$. The basic kit is supplied with two CDP1822S's forming a 256-byte RAM. At maximum expansion it will contain 32 CDP1822S's. The necessary decoding logic for the 4K expansion is also included in the basic kit. Expansion is accomplished by adding additional CDP1822S's at the prewired locations in 256-byte multiples (two CDP1822S's at a time). To assure contiguous memory when additional devices are added, the CDP1822S's should be placed in their designated locations in the Evaluation Kit (U24-U55) in numerical order on the printed circuit card. Fig. 2 shows the memory interconnections. The $\overline{MRD}$, $\overline{MWR}$, and eight address lines (MA0-MA7) are connected to all 32 RAM locations and directly to the CDP1802 microprocessor. In the CDP18S020, the four data-in and four data-out terminals of the CDP1822S are connected together and to the CDP1802 bidirectional data bus.

Chip selection is determined by enabling the two chip-select inputs, $\overline{CS1}$ and CS2, for each pair of CDP1822S's. The chip selects are arranged in a 4 x 4 matrix. This arrangement provides unique selection of 1 of 16 pairs of RAM's and requires only an eight-wire interconnect, as indicated in Fig. 2. Fig. 3 shows the address decode logic for the full RAM system. The I/O port, CDP1852 (U8) is used as an address latch for the higher-order address bits, MA8-MA15. The MA8-MA11 outputs from the latch are decoded by a CD4555B (U22) dual binary to 1 of 4 decoder. MA8-MA9 are decoded in one section and MA10-MA11 in the other section of the decoder. The four outputs from the MA10-$\overline{MA11}$ decoder section are inverted and connected to the $\overline{CS1}$ terminals of the RAM's; the other four outputs are connected to the CS2 terminals. Together, they form a 4 x 4 selection matrix. Each section of the decoder has a separate enable ($\overline{E}$) input and both must be enabled in order to select the RAM system.

The enable input of the MA8-MA9 decoder is prewired to ground (continuously enabled) and intended for use for additional memory expansion. The other enable input is connected to MA15. As a result, the RAM is inhibited for all address locations of $(8000)_{16}$ or above. This simple technique is used for separating the Utility ROM and its support RAM from the RAM system. If a finer level of decoding is desired for an expanded RAM system, the second enable input can be used. The CDP1824 RAM application note ICAN-6537 discusses one application for this input.

CDP1822 WRITE PROTECTION AND BATTERY HOLD-UP

Memory write protection and provisions for standby power have been included in the design of the Evaluation Kit RAM system to permit ROM simulation. A write-inhibit switch (SW-1, -2, -3, and -4) is placed in the write ($\overline{MWR}$) line for each 1K of RAM. The user manually sets the switches, in any combination, to inhibit a write signal from occurring in the protected sections of memory and destroying the information stored there.

Because of the low current drain, battery power may be substituted for V_{DD} and V_{CC} where non-volatile memory is desired.

Microprocessor Products

Application Note

ICAN-6540

USE OF ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM 2704 WITH RCA MICROPROCESSOR EVALUATION KIT CDP18S020

by A. W. Young

The CDP18S020 COSMAC Evaluation Kit has been designed to accept a 2704 electronically programmable ROM for system evaluation and prototyping. This application note describes design and interface considerations for the 2704 when used with the COSMAC Evaluation Kit CDP18S020.

DESCRIPTION OF 2704 FEATURES

The 2704 is a 4096-bit erasable and electrically reprogrammable read-only memory organized as 512 8-bit words. The memory is enabled when $\overline{CS}$ (terminal 20) goes low. Valid data appears on the eight three-state output buffers within t_{ACC} = 450 ns of the last address change. The three-state output buffers are disabled when $\overline{CS}$=1 and appear as high impedances to the data bus. All input and output signals are referenced to V_{CC} = 5 volts for a high level and V_{SS} = 0 volts for a low level. The memory is completely static and requires no clocks or precharge signals for the read operation. Terminal assignments for the 2704 are shown in Fig. 1.

APPLICATION OF THE 2704 IN EVALUATION KIT MEMORY SYSTEM

The 2704 can be located in either the Utility Program ROM location (U2) or the User I/O section of the Evaluation Kit PC card. When location U2 is used all required supply voltages are available prewired to the SYSTEM CONNECTOR as shown in Fig. 2. If the 2704 is located in the User I/O area, the required supply voltages can be wired to the device from the SYSTEM CONNECTOR or the USER I/O CONNECTOR.

For proper application of the 2704 in the Evaluation Kit, voltage, interface levels, and timing requirements must be considered.

a) Voltage requirements.
   The 2704 requires four supply voltage connections. Table I summarizes these voltage requirements and also gives 2704 and SYSTEM CONNECTOR pin locations. When location U2 is used, connection of the voltage supplies shown in Table I to the SYSTEM CONNECTOR pin indicated will provide the supply connections required by 2704 on the proper U2 pin.

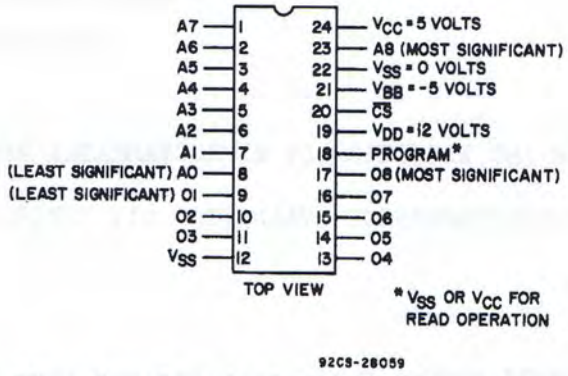


Fig. 1 - Terminal assignment diagram for the 2704 electronically reprogrammable ROM.

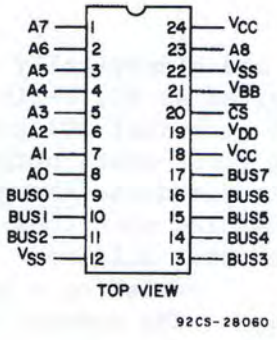


Fig. 2 - Wiring connections for 2704 ROM available at U2 location of Evaluation Kit system connector.

Name	Value (Volts, ±5%)	Max. Current/device (mA)	2704 and U2 Pin Connection	SYSTEM CONNECTOR Pin Location
V_{CC}	+5	10	24	P1-B
V_{DD}	+12	65	19	P1-C
V_{BB}	-5	45	21	P1-1
V_{SS}	0 (ground)	-	12,22	P1-A, 22

Table I - Voltage requirements for 2704 ROM and pin connections and locations.

b) Interface level requirements.
All 2704 input/output voltage levels are in the range $V_{SS} \leq V_{IN/OUT} \leq V_{CC}$. To be compatible with the Evaluation Kit, the memory and I/O circuits must have the same input/output voltage levels. This provision has been made and will automatically be implemented when the V_{CC} and V_{SS} pins on the Evaluation Kit SYSTEM CONNECTOR and are tied to +5 and 0 volts, respectively.

It should be noted that the CDP1802 has been designed for this type of interface requirement. Separate V_{DD} and V_{CC} supply connections are available on the chip. V_{DD} is used to internally power the CDP1802 logic and can be selected for maximum performance or minimum power. V_{CC} is used to reference all input and output signals of the microprocessor and is less than or equal to V_{DD}. For this application, V_{CC} is 5 volts and V_{DD} could be between 5 and 12 volts. A separate V_{DD} connection for the CDP1802 is provided on the Evaluation Kit SYSTEM CONNECTOR for this purpose.

c) Timing Requirements.
Because of the static design of the 2704 and the CDP1802, the only timing requirement of concern is system read-access time. This time is the sum of the 2704 read-access time (t_{ACC}) and the CDP18S020 memory system delay. The latter delay is 150 nanoseconds for a V_{CC} of 5 volts. The 2704 read-access time (t_{ACC}) is a maximum of 450 nanoseconds for the voltage supply values previously defined and a value for C_L of 100 picofarads. The system read-access time, therefore, is 600 nanoseconds. (This system read-access time applies to the basic Evaluation Kit with a 2704 PROM and up to 1K bytes of RAM.)

To choose the proper CDP1802 maximum operating frequency when the 2704 EPROM is used with the Evaluation Kit, the reader should refer to the figure in the CDP1802 data sheet which shows clock input frequency versus memory system access time. The intersection of the 600-nanosecond memory system access time with the curve labeled V_{CC} = 5 volts, V_{DD} = 10 volts indicates a clock frequency of up to 4.3 MHz. This value is within the operation range of DC to 5.0 MHz given in the table of Operating Conditions in the CDP1802 data sheet.

For $V_{DD} = V_{CC}$ = 5 volts, the curve indicates a clock frequency of up to 4.2 MHz. This value is above the operation range of DC to 3.2 MHz shown in the table of Operating Conditions. It will be necessary, therefore, to limit the clock frequency to 3.2 MHz.

ADDRESSING

When the 2704 is used in the U2 location on the CDP18S020 PC card, it will respond to addresses 8000_{16} to $81FF_{16}$. Pushing the RESET then the RUN U pushbuttons on the PC card will start program execution at location 8000_{16}. A detailed description of the address latch and decode circuitry in the Evaluation Kit can be found in the Design and Operation section of the Evaluation Kit Manual for the RCA CDP1802 COSMAC Microprocessor, MPM-203 and also in the Application Note "Use of CMOS-SOS RAM CDP1822S with RCA Microprocessor Evaluation Kit CDP18S020", ICAN-6539.

Location of the 2704 in the User I/O section of the PC card requires addition of address circuitry to control operation of the memory. The 16-line address bus is available in the User I/O section for this purpose.

CDP1832/2704 COMPATIBILITY

The CDP1832 static, CMOS, mask-programmable ROM is pin and functionally compatible with the 2704. One result of this compatibility is that the CDP1832 Utility Program ROM location U2 can be used for the 2704. The CDP1832, however, only requires a V_{CC} supply of 3 to 12 volts for proper operation. The extra voltage supplies required by the 2704 have been prewired to the U2 location but are not used (not internally connected in the CDP1832) by the CDP1832. When the CDP1832 is used at location U2, the V_{BB} (-5 volts) and V_{DD} voltage supply connections on the SYSTEM CONNECTOR can be left unterminated. Once the contents and operation of the program stored in the 2704 have been verified, a compatible CDP1832 CMOS ROM can be ordered and substituted for the 2704.

Microprocessor Products

Application Note

ICAN-6635

USE OF CMOS ROM'S CDP1833 AND CDP1834 WITH THE RCA MICROPROCESSOR EVALUATION KIT CDP18S020 AND THE EK/ASSEMBLER-EDITOR DESIGN KIT CDP18S024

by A. W. Young

The RCA1800 family of microprocessor products includes two 8192-bit static CMOS mask-programmable read-only memories, the CDP1833 and CDP1834. Each is organized as 1024 8-bit words but they differ in addressing structure. The CDP18S020 Evaluation Kit and the CDP18S024 EK/Assembler-Editor Design Kit are designed to accept the CDP1833 and CDP1834 as described in this application note.

APPLICATION OF CDP1833 IN EVALUATION KIT AND EK DESIGN KIT ROM SYSTEMS

The CDP1833 read-only memory is functionally identical to the CDP1831 read-only memory except for the storage array size (8192 bits versus 4096 bits) and addition of a mask selectable chip enable input (CEI). Refer to ICAN-6536 "Use of CMOS ROM's CDP1831 and CDP1832 with the RCA Microprocessor Evaluation Kit CDP18S020" in Section VI "Application Notes: Memory" of this Manual for a description of CDP1831 features. All features of the CDP1831 apply to the CDP1833. For the CDP1833 the 10 least significant bits of the 16-bit address select one of 1024 bytes in the ROM and the six most significant bits of the 16-bit address select one of 64 1024-byte sectors. Refer to Figs. 1 and 2 in ICAN-6536 for a comparison with the CDP1831.

An additional feature of the CDP1833 is the mask-selectable chip enable input (CEI). This input, as shown in Fig. 1, is logically "OR'd" with the internal ROM select signal to generate the chip enabled output (CEO). As a result, multiple CDP1833's can be cascaded by appropriate connections of CEO and CEI to generate a combined CEO signal.

The CEI signal appears on pin 22 of the CDP1833. To maintain socket compatibility with the CDP1831, which has no connection on pin 22, the user can either program out the CEI input (when ordering custom patterns) or provide a 22-kilohm pull-down or pull-up resistor on pin 22 when CEI is selected positive or negative, respectively.

The CDP18S020 and CDP18S024 Kits have been prewired to accept the CDP1833 in position U1. Fig. 2 shows the U1 pin connections. The eight CDP1802 memory address lines (MA0-MA7) and TPA are wired to the appropriate ROM pins. The CDP1833 ROM outputs are connected directly to the data bus. The CS1 and CS2 inputs are connected permanently high, and the $\overline{\text{MRD}}$ input is connected to the CDP1802 $\overline{\text{MRD}}$ output. As a result, the

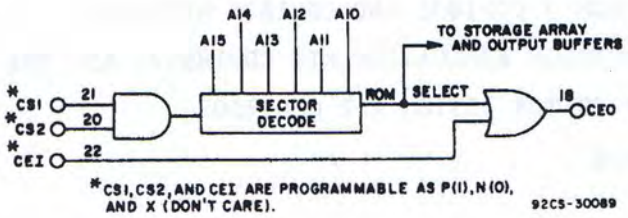


Fig. 1 - Function of CEI for CDP1833.

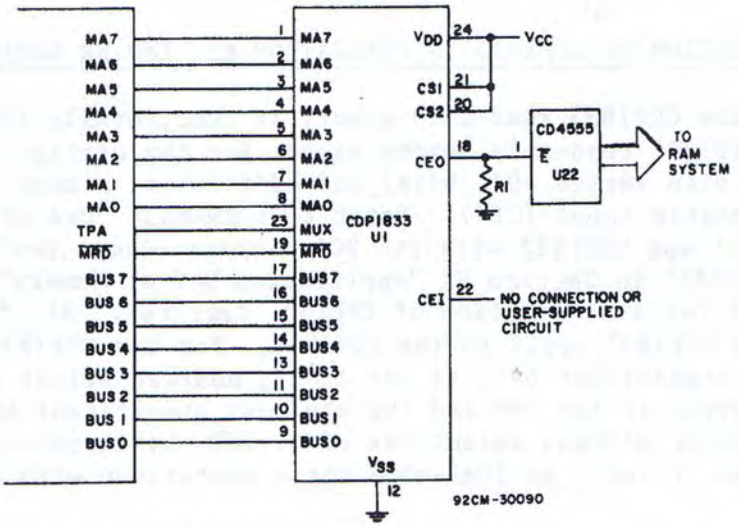


Fig. 2 - Pin connections for CDP1833 ROM in U1 location of CDP18S020 or CDP18S024 Kit.

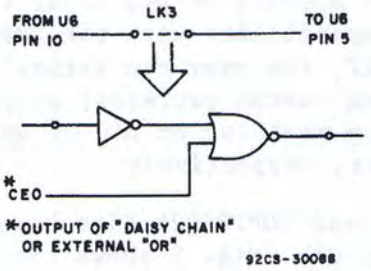


Fig. 3 - Use of CDP1833 CEO output to disable the CDP1832 ROM (U2) Utility Program.

ROM puts data on the bus when $\overline{MRD}$ = 0. The chip enabled output CEO is connected to the $\overline{E}$ (pin 1 of U22) control input of the RAM system decoder. When the ROM is addressed (enabled), the CEO output goes high and disables the RAM system. The CEO output can be used to disable the CDP1832 Utility Program ROM (U2) as shown in Fig. 3. Link 3 must be broken and the indicated gating inserted. The effect of the extra gating is to "OR" the CEO output with the existing CDP1832 $\overline{CS}$ signal. When using multiple 1833's, the "daisy chained" CEO output is used as shown. These controls assure the ability to place the CDP1833 sector address in any of the possible 64 locations regardless of the RAM or ROM memory space allocation. Note that a pull-down resistor (R1 = 22 KΩ) is on the CEO line to assure proper operation of the RAM system when the CDP1833 ROM is removed. When the system operates with a ROM in the U1 location, this resistor may be removed.

The CDP1833 V_{DD} (pin 24) is connected to the Kit V_{CC}. This connection permits maximum memory-system flexibility with or without the CDP1833.

To use the U1 position for the CDP1833, the device is simply inserted in the location as indicated on the PC card. (Optionally, R1 = 22 kilohms can be removed). Proper operation can be verified by use of the ?M[Starting Address]Δ [400] command of UT4 to list the memory contents. This check assumes that the CDP1833 does not occupy locations 8000_{16} to $83FF_{16}$.

Expanding the ROM System on the Evaluation or EK Design Kit is especially easy. In the User I/O section of the PC card, the CDP1802 memory address bus, data bus, $\overline{MRD}$, and TPA signals are provided on the left side. Multiple CDP1833's (up to 12) can be inserted in the pre-drilled locations and interfaced to the address and data busses. A combined CEO output can be generated by appropriate CEI/CEO connections.

It should be noted that memory pattern generation and verification are possible in the Kit RAM system by using the write-protect and battery hold-up features. Once a pattern has been verified, it can be permanently stored by the custom masking of one or more CDP1833 ROM's.

APPLICATION OF CDP1834 IN EVALUATION KIT AND EK DESIGN KIT ROM SYSTEMS

The CDP1834 read-only memory is functionally identical to the CDP1832 read-only memory except for the addition of a tenth address input on pin 22 to select one of 1024 8-bit words and mask selectable chip selects on pins 18 and 20. ICAN-6536 describes the operation of the CDP1832 in detail and applies equally to the CDP1834 except as noted above.

The CDP1834 is pin-compatible with the 2708 1024 x 8 bit erasable and electrically reprogrammable ROM and will operate in the same socket when pin 20 is programmed as $\overline{CS}$(N) and pin 18 as CS(P) or don't care (X).

Both the CDP18S020 Evaluation Kit and the CDP18S024 EK Design Kit have been prewired to accept the CDP1832/2704 and CDP1834/2708 combinations at location U2. However, only the Evaluation Kit CDP18S020, when operated at suitable voltages, can accomodate the 2704 and 2708 because these two types are limited to a V_{CC} of 5 volts. Links 1A and 1B personalize U2 for either combination. The Evaluation Kit PC board is factory programmed for the CDP1832/2704 combination. To change to the CDP1834/2708 combination, remove link 1A (scratch off with a sharp object) and insert link 1B. This change removes ground from U2 pin 22. The ROM which is inserted in location U2 will be selected when either A15 (address 8000_{16}) or RUN U are true. Refer to ICAN-6536 page 6 for operating details when RUN U is activated. Fig. 4 shows pin connections for the CDP1834 ROM in location U2 after the proper link adjustments have been made.

Expanded CDP1834 ROM-based memory systems are easily constructed in the User I/O section of the Evaluation Kit and EK Design Kit PC card. In addition to wiring ROM locations, address latch and decode functions must be provided. A sample 4-kilobyte system which can be constructed in the User I/O section of the PC card is shown in Fig. 5.

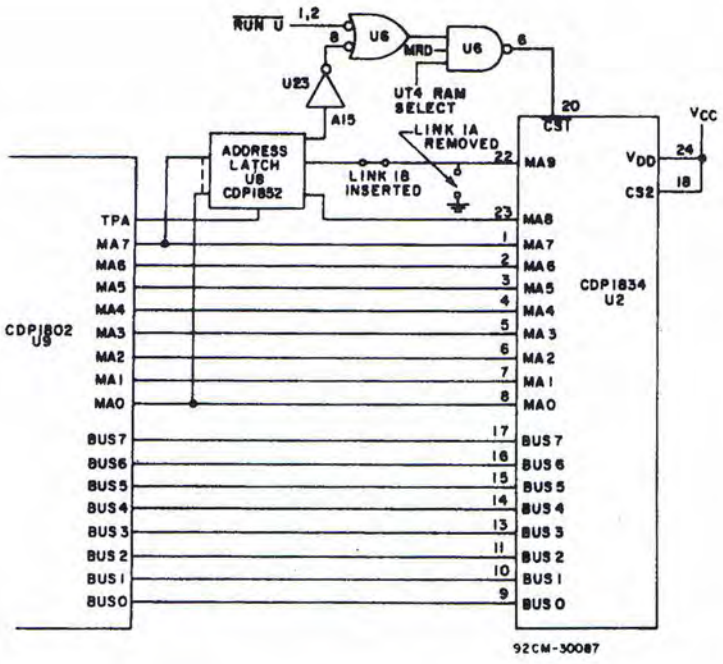


Fig. 4 - Pin connections for CDP1834 ROM in U2 location of CDP18S020 or CDP18S024 Kit.

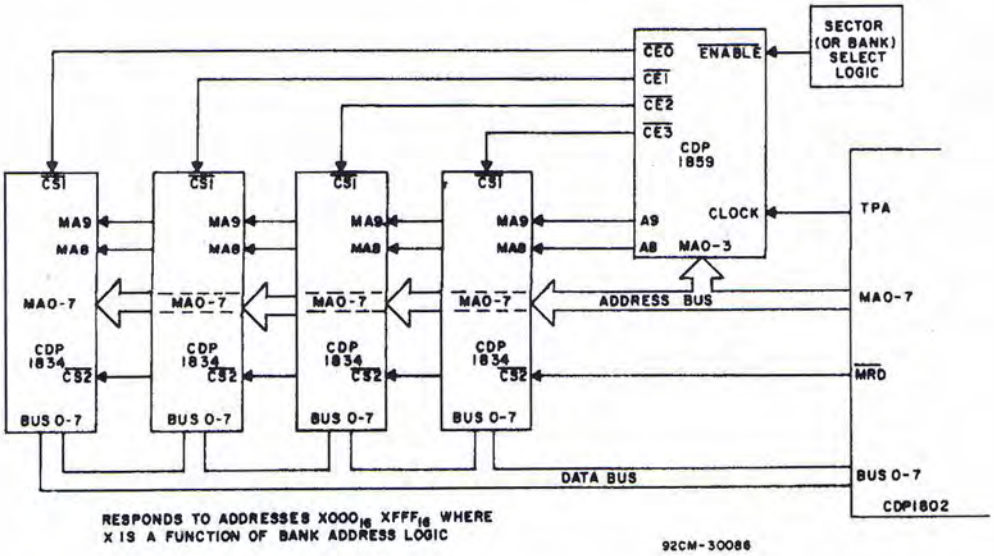


Fig. 5 - Sample 4-kilobyte ROM system using CDP1834 ROM's.

Microprocessor Products

Application Note

ICAN-6547

USE OF UTILITY PROGRAM UT4 READ AND TYPE ROUTINES WITH RCA MICROPROCESSOR EVALUATION KIT CDP18S020

By D. Block

The most elementary level of program generation for the RCA COSMAC Microprocessor Evaluation Kit CDP18S020 is done directly in machine code. With machine code programs, each instruction, all data constants, and all branch addresses are written in hexadecimal notation and directly entered into the Evaluation Kit RAM. A description of how to organize and generate a machine language program is given in the User Manual for the RCA CDP1802 COSMAC Microprocessor MPM-201 provided with the Evaluation Kit. This note describes the mechanism of entering, running, and modifying machine language programs on the Evaluation Kit. It is assumed that a TTY terminal is used and that the user has read the Utility Program UT4 section of the Evaluation Kit Manual for the RCA CDP1802 COSMAC Microprocessor MPM-203.

REVIEW OF UTILITY PROGRAM UT4 BASIC READ AND TYPE ROUTINES

To read a character from the I/O TTY terminal, the user's program can transfer control to the READ routine in the Utility Program UT4. This transfer is accomplished by loading address 813E into R3 and executing a D3 instruction. The calling program should use R5 as its program counter because the READ routine exits by setting P = 5. The ASCII code for the input character (with a 0 parity bit) will be in RF.1 and also in D. Registers R3.0, RE, RF, X, and DF will have been altered. All other register contents will not be changed by the READ routine. Because the READ routine uses the values in RC and RE which it has previously initialized to hold timing and echo constants, it is essential that these registers not be used. Table I gives UT4 register utilization information.

To type a character, the user's program can transfer control to TYPE5D by loading R3 with 819C and executing a D3 instruction. Again, the calling program should use R5 as its program counter because TYPE5D returns by executing a D5 instruction. The ASCII code for the output character should be an immediate byte, i.e., the byte after the D3 instruction.

After the character is typed, the program will automatically advance R5 past this byte and return control to the main program. For the reason mentioned earlier, registers RC and RE should not be used.

These read and type routines are not necessarily the best to use under all circumstances. UT4 offers several alternatives which can, for instance, offer higher throughput rates (see Table II). However, with the ability to use these two basic typewriter I/O functions, the user will be able to code elementary machine language programs to run on the Evaluation Kit that communicate via the teletype terminal.

PROGRAM EXAMPLES

A Simple Read and Type Program

As a first step, consider a program that will input a hex digit, add 1 to it, and print out the result. A flow chart for this operation is given in Fig. 1. Example program 1 in Fig. 2 does this function and illustrates some general principles of using the Read and Type routines. The next programming step is to consider register assignments. It is necessary to use register R5 as the main program counter because the Read and Type routines exit by setting P = 5. Because a program always starts out with R0 as the PC, at some point in the program before calling Read, the program counter will have to be changed to R5 (previously initialized to the correct value). Register R3 will be used by the Read and Type routines as their program counter. Register R4 was chosen arbitrarily to point at the memory location where the byte to be typed will be stored. Because the particular typing routine used, TYPE5D, picks up the next (immediate) byte for typing, this memory storage location will be within the area of the main program. Register assignments are summarized in Fig. 3.

Register initialization for R2, R4, and R5 occupy up to M(0009) in the program. The next instruction changes the program counter to R5. The subsequent six instructions set R3 = 813E, the address of UT4's READ routine. Changing the program counter to R3 (at M(0011)) causes this program to run, inputting the digit to D and RF.1.[Ø] The next instruction adds 1 to the contents of D. The result is stored at M(0019) where it is picked up by the TYPE5D routine. Before calling the Type routine, R3 is set to the appropriate address (819C). Finally, the last instruction causes the program to loop back on itself and await the next input.

[Ø] Note that the stored number is in ASCII notation. The least significant digit of the two hex digits stored there is the number of interest.

REGISTER NUMBER	
R0 R1	Clobbered by UT while storing registers
R3	Program counter for all READ, all TYPE and TIMALC routines.
R5	Program counter for UT4 (which calls the routines above).
RC	Program counter for the DELAY routine. Points to DELAY1 in memory.
RD	Assembled into by READAH (input hex digits).
RE	RE.1 holds time constant and echo bit. RE.0 used by all READ, TYPE routines and by TIMALC.
RF	RF.1 holds input/output ASCII character. RF.0 used by all READ, TYPE routines and by TIMALC.

TABLE I - UT4 register utilization.

ENTRY NAME	ABSOLUTE ADDRESS	FUNCTION/COMMENTS
READ	813E	Input ASCII→RF.1, D (if non-standard subroutine linkage)
READAH	813B	Same as READ. If hex char, DIGIT→RD
TYPE5D	819C	1.5 bit delay. Then TYPE5 function
TYPE5	81A0	Output ASCII char at M(R5). Then increment R5.
TYPE6	81A2	Output ASCII char at M(R6). Then increment R6.
TYPE	81A4	Output ASCII char at RF.1
TYPE2	81AE	Output hex digit pair in RF.1
TIMALC	80FE	Read input char and set up control byte in RE.1 Initialize RC to point to DELAY1.
DELAY1	80EF	Delay, as function of M(R3). Then R3+1.

NOTES ON ABOVE:

1. All routines, except DELAY, use R3 as program counter, exit with SEPR5, and alter registers X, D, DF, RE, and RF.

2. DELAY routine uses RC as program counter, exists with SEPR3 after incrementing R3, and alters registers X, D, DF, and RE.

3. READ and READAH exit with R3 pointing back at READAH.

4. All five TYPE routines exit with R3 pointing at TYPE5.

TABLE II - UT4 read and type addresses.

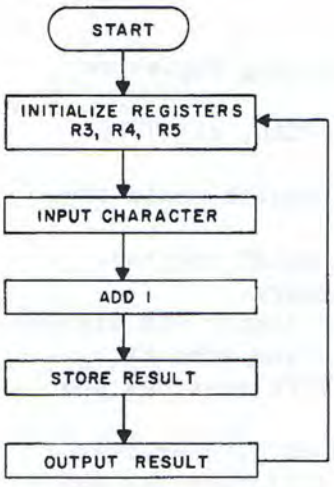


Fig. 1 - Flow chart for example program one.

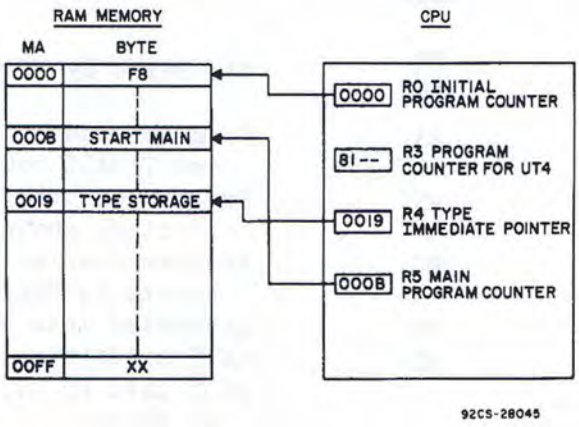


Fig. 3 - Register and memory utilization for example program one.

	Memory Address	Machine Code	Operation	Comment
	0000	F8		
	1	00	00→D	
	2	B4	D →R4.1	Initialize upper half
	3	B5	D →R5.1	of R4, R5
	4	F8		
*	5	19	19→D	Point R4 to the TYPE
	6	A4	D →R4.0	immediate location
	7	F8		
*	8	0B	0B→D	Initialize R5 to start
	9	A5	D →R5.0	of main program
	A	D5	P = 5	Change program counter
	B	F8		
	C	81	81→D	Initialize R3 to READ
	D	B3	D →R3.1	address 813E
	E	F8		
	F	3E	3E→D	
	0010	A3	D →R3.0	
	11	D3	P = 3	Call READ
	12	FC	ADD IMM	
	13	01		
	14	54	D →M(R(4))	Store input byte
	15	F8		
	16	9C	9C→D	Set R3 to TYPE
	17	A3	D →R3.0	address 819C
	18	D3	P = 3	Call TYPE
	19	00		TYPE imm. storage location
	1A	30		Return to start
*	1E	07		

Fig. 2 - Example program one.

The program can be entered and run by the following steps. Underlined text represents UT4 typeout; text not underlined represents user input; bracketed text is commentary. A <CR> denotes the 'Return' key and a <LF> the 'Line Feed' key.

Entering the program is begun by turning power ON and hitting RESET followed by RUN U; then

```
<CR>     (Carriage Return is then entered to establish TTY
          timing and echo character)

*        (UT4 prompt character)

!M0 F8 00 B4 B5 F8 19 A4 F8, <CR> <LF >
    0B A5 D5 F8 81 B3 F8 3E, <CR> <LF >
    A3 D3 FC 01 54 F8 9C A3, <CR> <LF >
    D3 00 30 07 <CR>
```

The program is now loaded. It can be read back with a ?M0 1C <CR> to determine whether it has been properly entered.

```
* (UT4 ready)

  $P0 <CR>(Start the Program)

  1256AB9:
```

A 'bug' has been discovered in this program. Instead of getting an 'A' typeout after the digit 9 is entered, a semicolon appears. Reference to the ASCII - HEX Conversion Table (Table III) shows why. This problem provides an opportunity to use programming skills to correct it. Correction should take another seven steps of code. It is important to update absolute addresses in the program while changes are made. These areas are marked with a * in the program.

The above program is meant only to show the general principles of using UT4 for Reading and Typing and to provide a short program to enter and verify that the Evaluation Kit is operating properly. When the user actually works with a program that inputs and outputs hex digits, the READAH and TYPE2 routines at M(813B) and M(81AE) respectively would be used, because they are specifically designed to facilitate the handling of hex digits.

Modifying a Given Program

The second example is a program, discussed on page 91 and 92 of the User Manual for the RCA CDP1802 COSMAC Microprocessor MPM-201, for inputting two bytes, comparing them, and outputting the larger or setting the Q flag if the bytes are identical. Flow charts are given in Figs. 4 and 5. The discussion of this program in the MPM-201 should be referred to before proceeding with this section.

LEAST SIGNIFICANT HEX DIGIT	MOST SIGNIFICANT HEX DIGIT 0	1	2	3	4	5	6	7
0	NUL	DLE	SP	0	@	P	`	p
1	SOH	DC1	!	1	A	Q	a	q
2	STX	DC2	"	2	B	R	b	r
3	ETX	DC3	#	3	C	S	c	s
4	EOT	DC4	$	4	D	T	d	t
5	ENQ	NAK	%	5	E	U	e	u
6	ACK	SYN	&	6	F	V	f	v
7	BEL	ETB	'	7	G	W	g	w
8	BS	CAN	(	8	H	X	h	x
9	HT	EM	)	9	I	Y	i	y
A	LF	SUB	*	:	J	Z	j	z
B	VT	ESC	+	;	K	[	k	{
C	FF	FS	,	<	L	\	l	¦
D	CR	GS	-	=	M	]	m	}
E	SO	RS	.	>	N	↑	n	~
F	SI	US	/	?	O	←	o	DEL

NOTES:

(1) PARITY BIT IN MOST SIGNIFICANT HEX DIGIT NOT INCLUDED.
(2) CHARACTERS IN COLUMNS 0 AND 1 (AS WELL AS SP AND DEL) ARE NON-PRINTING.
(3) MODEL 33 TELETYPE PRINTS CODES IN COLUMNS 6 AND 7 AS IF THEY WERE COLUMN 4 AND 5 CODES.

Table III - ASCII - Hex table.

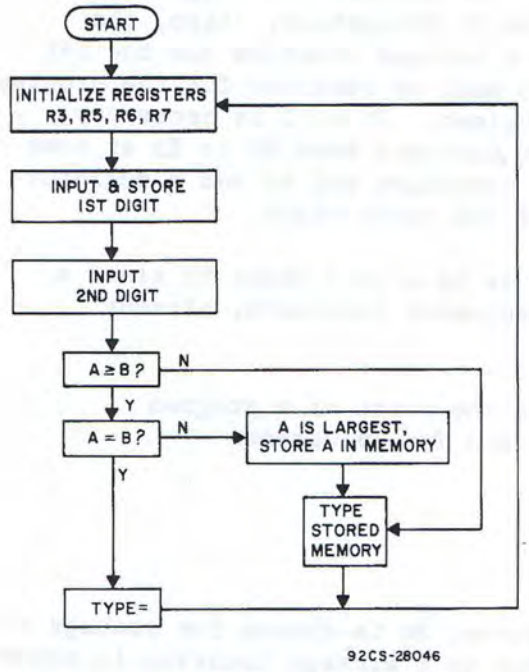


Fig. 4 - Elementary flow chart for example program two.

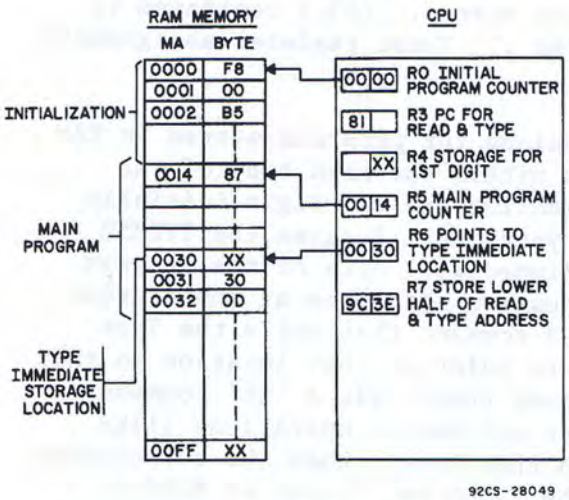


Fig. 6 - Register and memory utilization for example program two.

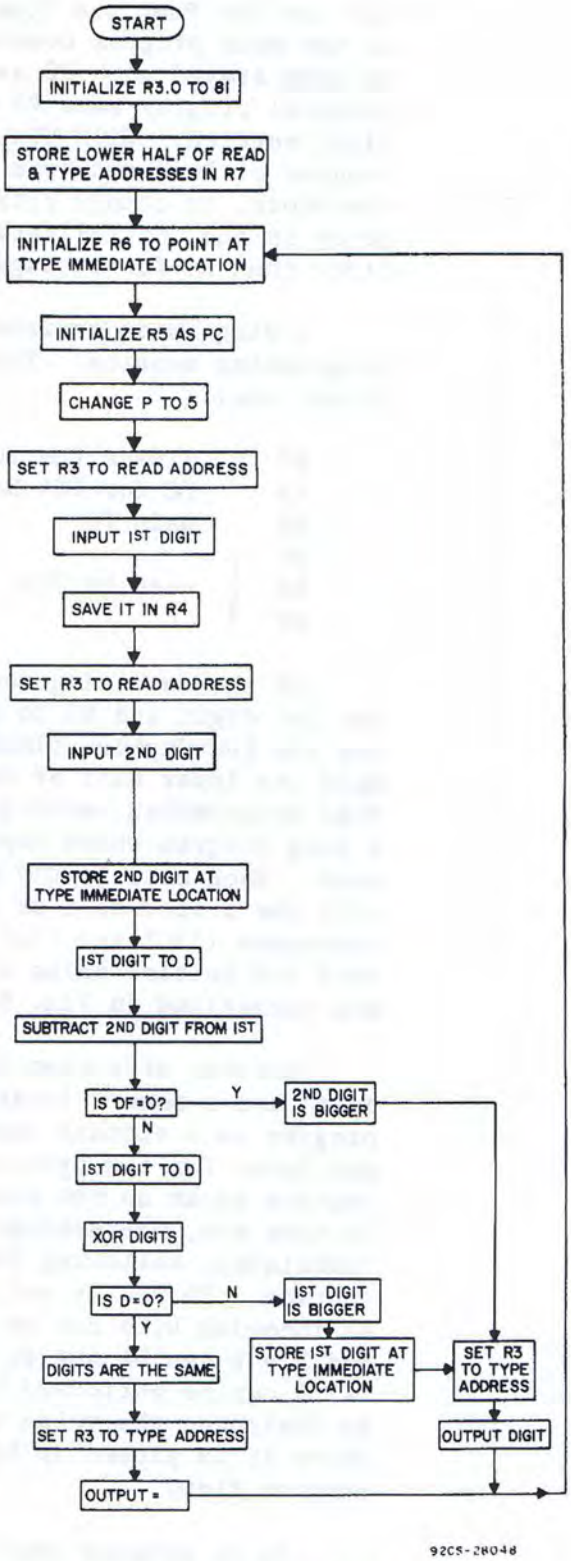


Fig. 5 - Detailed flow chart for example program two.

This program requires some modifications in order to use the UT4 Read and Type routines. First, R5 must be used as the main program counter (PC) whereas the original program stayed with R0 as the PC throughout. Also, the original program uses R3 as a storage location for the 1st digit entered. With UT4, R3 must be reserved for the program counter of Read and Type routines. It will be necessary, therefore, to change program counters from R0 to R5 at some point in the initialization procedure and to use a register other than R3 for storage of the input digit.

A diagram of register use is a good place to start a programming session. The dedicated registers, already known, are:

R0	always the PC at the start of a program
R3	PC for UT4 Read and Type programs
R5	main PC
RC, RE, RF	used by UT4

Of the remaining registers, R4 is chosen for storage of the 1st digit and R6 to point to a storage location in memory for the 2nd digit. Finally, R7.1 and R7.0 are chosen to hold the lower half of the READ and TYPE addresses respectively. This programming technique saves memory bytes, especially in a long program where repeated calls to READ and TYPE5D are used. Each call to UT4 will be made after R3.0 is initialized with the proper half of R7 in which the two lower-half addresses ('9C' and '3E') are stored. (R3.1 continues to hold its initial value of '81'.) These register assignments are summarized in Fig. 6.

Another effective technique for programs stored in RAM is to use a memory location within the main body of the program as a storage location for the 2nd digit initially and later for the byte to typed out. Because the TYPE5D routine picks up the next (immediate) byte of the program to type out, the storage location should be at the address immediately following the D3 command that calls the Type routine. R6 can be set up to point at that location so that an incoming byte can be stored there (via a '56' command) and X = 6 can be set so that arithmetic operations (like 'F7') can be performed with that byte. When the computation is finished, the value to be typed out is put at M(R(6)) where it is picked up by the Type routine in the normal program flow.

It is obvious that the initialization portion of the program is going to be considerably longer than that of the original program (see Fig. 7). However, the main programs are similar. The initialization section is above the dashed lines, the main program starts at M(0014).

	Memory Address	Machine Code	Operation	Comment
	0000	F8		
	1	00	00 → D	
	2	B5	D → R5.1	Initialize upper half
	3	B6	D → R6.1	of R5, R6
	4	F8		
	5	81	81 → D	
	6	B3	D → R3.1	Initialize upper half of R3
	7	F8		
	8	3E	3E → D	Lower half of READ
	9	A7	D → R7.0	address saved in R7.0
	A	F8		
	B	9C	9C → D	Lower half of TYPE
	C	B7	D → R7.1	saved in R7.1
	D	F8		
*	E	30	30 → D	Point R6 to the
	F	A6	D → R6.0	TYPE immediate location
	0010	F8		
*	11	14	14 → D	Initialize R5 to start
	12	A5	D → R5.0	of main program
	13	D5	P = 5	Change program counter
	14	87	R7.0 → D	
	15	A3	D → R3.0	R3 now points to READ
	16	D3	P = 3	Call READ. Input 1st digit to D
	17	A4	D → R4.0	Save it in R4
	18	87	R7.0 → D	Reinitialize R3
	19	A3	D → R3.0	
	1A	D3	P = 3	READ 2nd digit
	001B	56	D → M(R(6))	Store at TYPE imm. loc.
	1C	84	R4.0 → D	1st digit to D
	1D	E6	X = 6	Point to TYPE imm. loc.
	1E	F7	SUB	Subtract 2nd digit from 1st
	1F	3B		Br if DF=0; Type 2nd digit
*	0020	2D		
	21	84	R4.0 → D	1st digit to D
	22	F3	XOR	Check if 1st digit = 2nd
	23	3A		Br on D≠0; Type 1st digit
*	24	2B		
	25	97	R7.1 → D	Initialize R3 to TYPE
	26	A3	D → R3.0	
	27	D3	P = 3	Call TYPE
	28	3D		This byte (= sign) will be typed
	29	30		Return to start
*	2A	0D		
	2B	84	R4.0 → D	Get 1st digit
	2C	56	D → M(R(6))	Store at TYPE imm. loc.
	2D	97	R7.1 → D	Initialize R3 for TYPE
	2E	A3	D → R3.0	
	2F	D3	P = 3	Call TYPE
	0030	00		TYPE immediate storage location
	31	30		
*	32	0D		Return to start

Fig. 7 - Example program two.

R5 is the program counter once the main program is entered. First, R3 is initialized to the READ address and the first digit is entered and saved in R4.0. Next R3 is reinitialized (since it is not left pointing at 813E by UT4) and the second digit entered and saved at the Type immediate location (M(0030)). Note that X is set to 6 at M(001D) immediately before it is needed for the F7 statement at M(001E). Because X is altered by the UT4 program, it cannot be set during the initialization portion of the program. If the program determines that the digits are identical, R3 is set to the TYPE5D address, and an = sign is typed. Otherwise, another program path is taken (refer to the detailed flow diagram, Fig. 5) in which the larger digit is typed after R3 is appropriately set.

Note that the steps for setting or resetting the Q output are omitted from this program. The Q output is used for the TTY interface on the Evaluation Kit and should not be set or reset by the program being run.

SOME GENERAL PRINCIPLES

A side-by-side comparison of the two programs just discussed reveals some general principles that can be used when a machine language program is converted to use the UT4 READ and TYPE5D routines. Examples of machine language programs are given in the COSMAC Microtutor Manual, MPM-109.

1. The program calling UT4 should use R5 as the program counter (PC).
2. Another register (R6 in these examples) should point to a storage area for I/O digits.
3. Input codes (69-6F) can be replaced by setting R3 to 813E (READ) and doing a D3 command.
4. Output codes (61-67) can be replaced by setting R3 to 819C (TYPE5D) where the next byte will be the one typed. It must be an ASCII encoded character.

ENTERING AND RUNNING THE PROGRAM

The program given in Example 2 can be entered and run by the following steps. Underlined text represents UT4 typeout; text not underlined represents user input; bracketed text is commentary.

Entering the program is begun by turning power ON and hitting RESET followed by RUN U; then

[CR]	(Carriage Return is then entered to establish TTY terminal timing and echo character)
*	(UT4 prompt character)

```
!M0 F8 00 B5 B6 F8 81 B3 F8, <CR> <LF>
    3E A7 F8 9C B7 F8 30 A6, <CR> <LF>
    F8 14 A5 D5 87 A3 D3 A4, <CR> <LF>
    87 A3 D3 56 84 E6 F7 3B, <CR> <LF>
    2D 84 F3 3A 2B 97 A3 D3, <CR> <LF>
    3D 30 0D 84 56 97 A3 D3, <CR> <LF>
    00 30 0D <CR>
```

The program is now loaded. It can be read back with a ?M0 33 [CR] command to determine whether it has been properly entered.

* (UT4 ready for next command.)

$P0 [CR] (Start the program)

12221255=ABBMM=

Each character triplet represents one pass through the main program loop consisting of two user input characters and one system response character.

ON-LINE PROGRAM MODIFICATION

The program can be modified on-line by using !M command to change memory contents. For example, it may be desirable to generate a more readable typeout by inserting spaces, other characters (such as >or<), and Carriage Returns. When such modifications are made, it is necessary to update branch addresses and to register initialization numbers as required. These addresses are marked with an asterisk (*) in the program for easy reference.

Operating Considerations for RCA Solid State Devices

Solid state devices are being designed into an increasing variety of electronic equipment because of their high standards of reliability and performance. However, it is essential that equipment designers be mindful of good engineering practices in the use of these devices to achieve the desired performance.

This Note summarizes important operating recommendations and precautions which should be followed in the interest of maintaining the high standards of performance of solid state devices.

The ratings included in RCA Solid State Devices data bulletins are based on the Absolute Maximum Rating System, which is defined by the following Industry Standard (JEDEC) statement:

Absolute-Maximum Ratings are limiting values of operating and environmental conditions applicable to any electron device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

The device manufacturer chooses these values to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in device characteristics.

The equipment manufacturer should design so that initially and throughout life no absolute-maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply-voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in device characteristics.

It is recommended that equipment manufacturers consult RCA whenever device applications involve unusual electrical, mechanical or environmental operating conditions.

GENERAL CONSIDERATIONS

The design flexibility provided by these devices makes possible their use in a broad range of applications and under many different operating conditions. When incorporating these devices in equipment, therefore, designers should anticipate the rare possibility of device failure and make certain that no safety hazard would result from such an occurrence.

The small size of most solid state products provides obvious advantages to the designers of electronic equipment. However, it should be recognized that these compact devices usually provide only relatively small insulation area between adjacent leads and the metal envelope. When these devices are used in moist or contaminated atmospheres, therefore, supplemental protection must be provided to prevent the development of electrical conductive paths across the relatively small insulating surfaces. For specific information on voltage creepage, the user should consult references such as the JEDEC Standard No. 7 "Suggested Standard on Thyristors," and JEDEC Standard RS282 "Standards for Silicon Rectifier Diodes and Stacks".

The metal shells of some solid state devices operate at the collector voltage and for some rectifiers and thyristors at the anode voltage. Therefore, consideration should be given to the possibilify of shock hazard if the shells are to operate at voltages appreciably above or below ground potential. In general, in any application in which devices are operated at voltages which may be dangerous to personnel, suitable precautionary measures should be taken to prevent direct contact with these devices.

Devices should not be connected into or disconnected from circuits with the power on because high transient voltages may cause permanent damage to the devices.

TESTING PRECAUTIONS

In common with many electronic components, solid-state devices should be operated and tested in circuits which have reasonable values of current limiting resistance, or other forms of effective current overload protection. Failure to observe these precautions can cause excessive internal heating of the device resulting in destruction and/or possible shattering of the enclosure.

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TRANSISTORS AND THYRISTORS WITH FLEXIBLE LEADS

Flexible leads are usually soldered to the circuit elements. It is desirable in all soldering operatings to provide some slack or an expansion elbow in each lead to prevent excessive tension on the leads. It is important during the soldering operation to avoid excessive heat in order to prevent possible damage to the devices. Some of the heat can be absorbed if the flexible lead of the device is grasped between the case and the soldering point with a pair of pliers.

TRANSISTORS AND THYRISTORS WITH MOUNTING FLANGES

The mounting flanges of JEDEC-type packages such as the TO-3 or TO-66 often serve as the collector or anode terminal. In such cases, it is essential that the mounting flange be securely fastened to the heat sink, which may be the equipment chassis. Under no circumstances, however, should the mounting flange of a transistor be soldered directly to the heat sink or chassis because the heat of the soldering operation could permanently damage the device. Soldering is the preferred method for mounting thyristors; see "Rectifiers and Thyristors," below. Devices which cannot be soldered can be installed in commercially available sockets. Electrical connections may also be made by soldering directly to the terminal pins. Such connections may be soldered to the pins close to the pin seals provided care is taken to conduct excessive heat away from the seals; otherwise the heat of the soldering operation could crack the pin seals and damage the device.

During operation, the mounting-flange temperature is higher than the ambient temperature by an amount which depends on the heat sink used. The heat sink must have sufficient thermal capacity to assure that the heat dissipated in the heat sink itself does not raise the device mounting-flange temperature above the rated value. The heat sink or chassis may be connected to either the positive or negative supply.

In many applications the chassis is connected to the voltage-supply terminal. If the recommended mounting hardware shown in the data bulletin for the specific solid-state device is not available, it is necessary to use either an anodized aluminum insulator having high thermal conductivity or a mica insulator between the mounting-flange and the chassis. If an insulating aluminum washer is required, it should be drilled or punched to provide the two mounting holes for the terminal pins. The burrs should then be removed from the washer and the washer anodized. To insure that the anodized insulating layer is not destroyed during mounting, it is necessary to remove the burrs from the holes in the chassis.

It is also important that an insulating bushing, such as glass-filled nylon, be used between each mounting bolt and the chassis to prevent a short circuit. However, the insulating bushing should not exhibit shrinkage or softening under the operating temperatures encountered. Otherwise the thermal resistance at the interface between device and heat sink may increase as a result of decreasing pressure.

PLASTIC POWER TRANSISTORS AND THYRISTORS

RCA power transistors and thyristors (SCR's and triacs) in molded-silicone-plastic packages are available in a wide range of power-dissipation ratings and a variety of package configurations. The following paragraphs provide guidelines for handling and mounting of these plastic-package devices, recommend forming of leads to meet specific mounting requirements, and describe various mounting arrangements, thermal considerations, and cleaning methods. This information is intended to augment the data on electrical characteristics, safe operating area, and performance capabilities in the technical bulletin for each type of plastic-package transistor or thyristor.

Lead-Forming Techniques

The leads of the RCA VERSAWATT in-line plastic packages can be formed to a custom shape, provided they are not indiscriminately twisted or bent. Although these leads can be formed, they are not flexible in the general sense, nor are they sufficiently rigid for unrestrained wire wrapping

Before an attempt is made to form the leads of an in-line package to meet the requirements of a specific application, the desired lead configuration should be determined, and a lead-bending fixture should be designed and constructed. The use of a properly designed fixture for this operation eliminates the need for repeated lead bending. When the use of a special bending fixture is not practical, a pair of long-nosed pliers may be used. The pliers should hold the lead firmly between the bending point and the case, but should not touch the case.

When the leads of an in-line plastic package are to be formed, whether by use of long-nosed pliers or a special bending fixture, the following precautions must be observed to avoid internal damage to the device:

1. Restrain the lead between the bending point and the plastic case to prevent relative movement between the lead and the case.
2. When the bend is made in the plane of the lead (spreading), bend only the narrow part of the lead.
3. When the bend is made in the plane perpendicular to that of the leads, make the bend at least 1/8 inch from the plastic case.
4. Do not use a lead-bend radius of less than 1/16 inch.
5. Avoid repeated bending of leads.

The leads of the TO-220AB VERSAWATT in-line package are not designed to withstand excessive axial pull. Force in this direction greater than 4 pounds may result in permanent damage to the device. If the mounting arrangement tends to impose axial stress on the leads, some method of strain relief should be devised.

Wire wrapping of the leads is permissible, provided that the lead is restrained between the plastic case and the point of the wrapping. Soldering to the leads is also allowed. The maximum soldering temperature, however, must not exceed 275°C and must be applied for not more than 5 seconds at a distance not less than 1/8 inch from the plastic case. When

wires are used for connections, care should be exercised to assure that movement of the wire does not cause movement of the lead at the lead-to-plastic junctions.

The leads of RCA molded-plastic high-power packages are not designed to be reshaped. However, simple bending of the leads is permitted to change them from a standard vertical to a standard horizontal configuration, or conversely. Bending of the leads in this manner is restricted to three 90-degree bends: repeated bendings should be avoided.

Mounting

Recommended mounting arrangements and suggested hardward for the VERSAWATT package are given in the data bulletins for specific devices and in RCA Application Note AN-4142. When the package is fastened to a heat sink, a rectangular washer (RCA Part No. NR231A) is recommended to minimize distortion of the mounting flange. Excessive distortion of the flange could cause damage to the package. The washer is particularly important when the size of the mounting hole exceeds 0.140 inch (6-32 clearance). Larger holes are needed to accommodate insulating bushings; however, the holes should not be larger than necessary to provide hardware clearance and, in any case, should not exceed a diameter of 0.250 inch.

Flange distortion is also possible if excessive torque is used during mounting. A maximum torque of 8 inch-pounds is specified. Care should be exercised to assure that the tool used to drive the mounting screw never comes in contact with the plastic body during the driving operation. Such contact can result in damage to the plastic body and internal device connections. An excellent method of avoiding this problem is to use a spacer or combination spacer-isolating bushing which raises the screw head or nut above the top surface of the plastic body. The material used for such a spacer or spacer-isolating bushing should, of course, be carefully selected to avoid "cold flow" and consequent reduction in mounting force. Suggested materials for these bushings are diallphtalate, fiberglass-filled nylon, or fiberglass-filled polycarbonate. Unfilled nylon should be avoided.

Modification of the flange can also result in flange distortion and should not be attempted. The package should not be soldered to the heat sink by use of lead-tin solder because the heat required with this type of solder will cause the junction temperature of the device to become excessively high.

The TO-220AA plastic package can be mounted in commercially available TO-66 sockets, such as UID Electronics Corp. Socket No. PTS-4 or equivalent. For testing purposes, the TO-220AB in-line package can be mounted in a Jetron Socket No. DC74-104 or equivalent. Regardless of the mounting method, the following precautions should be taken:

1. Use appropriate hardware.
2. Always fasten the package to the heat sink before the leads are soldered to fixed terminals.
3. Never allow the mounting tool to come in contact with the plastic case.
4. Never exceed a torque of 8 inch-pounds.
5. Avoid oversize mounting holes.
6. Provide strain relief if there is any probability that axial stress will be applied to the leads.
7. Use insulating bushings to prevent hot-creep problems. Such bushings should be made of diallphthalate, fiberglass-filled nylon, or fiberglass-filled polycarbonate.

The maximum allowable power dissipation in a solid state device is limited by the junction temperature. An important factor in assuring that the junction temperature remains below the specified maximum value is the ability of the associated thermal circuit to conduct heat away from the device.

When a solid state device is operated in free air, without a heat sink, the steady-state thermal circuit is defined by the junction-to-free-air thermal resistance given in the published data for the device. Thermal considerations require that a free flow of air around the device is always present and that the power dissipation be maintained below the level which would cause the junction temperature to rise above the maximum rating. However, when the device is mounted on a heat sink, care must be taken to assure that all portions of the thermal circuit are considered.

To assure efficient heat transfer from case to heat sink when mounting RCA molded-plastic solid state power devices, the following special precautions should be observed:

1. Mounting torque should be between 4 and 8 inch-pounds.
2. The mounting holes should be kept as small as possible.
3. Holes should be drilled or punched clean with no burrs or ridges, and chamfered to a maximum radius of 0.010 inch.
4. The mounting surface should be flat within 0.002 inch/inch.
5. Thermal grease (Dow Corning 340 or equivalent) should always be used on both sides of the insulating washer if one is employed.
6. Thin insulating washers should be used. (Thickness of factory-supplied mica washers range from 2 to 4 mils).
7. A lock washer or torque washer, made of material having sufficient creep strength, should be used to prevent degradation of heat sink efficiency during life.

A wide variety of solvents is available for degreasing and flux removal. The usual practice is to submerge components in a solvent bath for a specified time. However, from a reliability stand point it is extremely important that the solvent, together with other chemicals in the solder-cleaning system (such as flux and solder covers), do not adversely affect the life of the component. This consideration applies to all non-hermetic and molded-plastic components.

It is, of course, impractical to evaluate the effect on long-term device life of all cleaning solvents, which are marketed with numerous additives under a variety of brand names. These solvents can, however, be classified with

respect to their component parts as either acceptable or unacceptable. Chlorinated solvents tend to dissolve the outer package and, therefore, make operation in a humid atmosphere unreliable. Gasoline and other hydrocarbons cause the inner encapsulant to swell and damage the transistor. Alcohol is an acceptable solvent. Examples of specific, acceptable alchols are isopropanol, methanol, and special denatured alcohols, such as SDA1, SDA30, SDA34, and SDA44.

Care must also be used in the selection of fluxes for lead soldering. Rosin or activated rosin fluxes are recommended, while organic or acid fluxes are not. Examples of acceptable fluxes are:

1. Alpha Reliaros No. 320-33
2. Alpha Reliaros No. 346
3. Alpha Reliaros No. 711
4. Alpha Reliafoam No. 807
5. Alpha Reliafoam No. 809
6. Alpha Reliafoam No. 811-13
7. Alpha Reliafoam No. 815-35
8. Kester No. 44

If the completed assembly is to be encapsulated, the effect on the molded-plastic transistor must be studied from both a chemical and a physical standpoint.

RECTIFIERS AND THYRISTORS

A surge-limiting impedance should always be used in series with silicon rectifiers and thyristors. The impedance value must be sufficient to limit the surge current to the value specified under the maximum ratings. This impedance may be provided by the power transformer winding, or by an external resistor or choke.

A very efficient method for mounting thyristors utilizing the "modified TO-5" package is to provide intimate contact between the heat sink and at least one half of the base of the device opposite the leads. This package can be mounted to the heat sink mechanically with glue or an expoxy adhesive, or by soldering, the most efficient method.

The use of a "self-jigging" arrangement and a solder preform is recommended. If each unit is soldered individually, the heat source should be held on the heat sink and the solder on the unit. Heat should be applied only long enough to permit solder to flow freely. For more detailed thyristor mounting considerations, refer to Application Note AN3822, "Thermal Considerations in Mounting of RCA Thyristors".

MOS FIELD-EFFECT TRANSISTORS

Insulated-Gate Metal Oxide-Semiconductor Field-Effect Transistors (MOS FETs), like bipolar high-frequency transistors, are susceptible to gate insulation damage by the electrostatic discharge of energy through the devices. Electrostatic discharges can occur in an MOS FET if a type with an unprotected gate is picked up and the static charge, built in the handler's body capacitance, is discharged through the device. With proper handling and applications procedures, however, MOS transistors are currently being extensively used in production by numerous equipment manufacturers in military, industrial, and consumer applications, with virtually no problems of damage due to electrostatic discharge.

In some MOS FETs, diodes are electrically connected between each insulated gate and the transistor's source. These diodes offer protection against static discharge and in-circuit transients without the need for external shorting mechanisms. MOS FETs which do not include gate-protection diodes can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs attached to the device by the vendor, or by the insertion into conductive material such as "ECCOSORB* LD26" or equivalent.
   (NOTE: Polystyrene *insulating* "SNOW" is not sufficiently conductive and should not be used.)
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means, for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.

RF POWER TRANSISTORS

Mounting and Handling

Stripline rf devices should be mounted so that the leads are not bent or pulled away from the stud (heat sink) side of the device. When leads are formed, they should be supported to avoid transmitting the bending or cutting stress to the ceramic portion of the device. Excessive stresses may destroy the hermeticity of the package without displaying visible damage.

Devices employing silver leads are susceptible to tarnishing; these parts should not be removed from the original tarnish-preventive containers and wrappings until ready for use. Lead solderability is retarded by the presence of silver tarnish; the tarnish can be removed with a silver cleaning solution, such as thiourea.

The ceramic bodies of many rf devices contain beryllium oxide as a major ingredient. These portions of the transistors should not be crushed, ground, or abraded in any way because the dust created could be hazardous if inhaled.

Operating

Forward-Biased Operation. For Class A or AB operation, the allowable quiescent bias point is determined by reference to the infrared safe-area curve in the appropriate data bulletin. This curve depicts the safe current/voltage combinations for extended continuous operation.

Load VSWR. Excessive collector load or tuning mismatch can cause device destruction by over-dissipation or secondary breakdown. Mismatch capability is generally included on the data bulletins for the more recent rf transistors.

See RCA RF Power Transitor Manual, Technical Series RMF-430, pp 39-41, for additional information concerning the handling and mounting of rf power transistors.

*Trade Mark: Emerson and Cumming, Inc.

INTEGRATED CIRCUITS

Handing

All COS/MOS gate inputs have a resistor/diode gate protection network. All transmission gate inputs and all outputs have diode protection provided by inherent p-n junction diodes. These diode networks at input and output interfaces protect COS/MOS devices from gate-oxide failure in handling environments where static discharge is not excessive. In low-temperature, low-humidity environments, improper handling may result in device damage. See ICAN-6000, "Handling and Operating Considerations for MOS Integrated Circuits", for proper handling procedures.

Mounting

Integrated circuits are normally supplied with lead-tin plated leads to facilitate soldering into circuit boards. In those relatively few applications requiring welding of the device leads, rather than soldering, the devices may be obtained with gold or nickel plated Kovar leads.* It should be recognized that this type of plating will not provide complete protection against lead corrosion in the presence of high humidity and mechanical stress. The aluminum-foil-lined cardboard "sandwich pack" employed for static protection of the flat-pack also provides some additional protection against lead corrosion, and it is recommended that the devices be stored in this package until used.

When integrated circuits are welded onto printed circuit boards or equipment, the presence of moisture between the closely spaced terminals can result in conductive paths that may impair device performance in high-impedance applications. It is therefore recommended that conformal coatings or potting be provided as an added measure of protection against moisture penetration.

In any method of mounting integrated circuits which involves bending or forming of the device leads, it is extremely important that the lead be supported and clamped between the bend and the package seal, and that bending be done with care to avoid damage to lead plating. In no case should the radius of the bend be less than the diameter of the lead, or in the case of rectangular leads, such as those used in RCA 14-lead and 16-lead flat-packages, less than the lead thickness. It is also extremely important that the ends of the bent leads be straight to assure proper insertion through the holes in the printed-circuit board.

Operating

Unused Inputs

All unused input leads must be connected to either V_{SS} or V_{DD}, whichever is appropriate for the logic circuit involved. A floating input on a high-current type, such as the CD4049 or CD4050, not only can result in faulty logic operation, but can cause the maximum power dissipation of 200 milliwatts to be exceeded and may result in damage to the device. Inputs to these types, which are mounted on printed-circuit boards that may temporarily become unterminated, should have a pull-up resistor to V_{SS} or V_{DD}. A useful range of values for such resistors is from 10 kilohms to 1 megohm.

Input Signals

Signals shall not be applied to the inputs while the device power supply is off unless the input current is limited to a steady state value of less than 10 milliamperes. Input currents of less than 10 milliamperes prevent device damage; however, proper operation may be impaired as a result of current flow through structural diode junctions.

Output Short Circuits

Shorting of outputs to V_{SS} or V_{DD} can damage many of the higher-output-current COS/MOS types, such as the CD4007, CD4041, CD4049, and CD4050. In general, these types can all be safely shorted for supplies up to 5 volts, but will be damaged (depending on type) at higher power-supply voltages. For cases in which a short-circuit load, such as the base of a p-n-p or an n-p-n bipolar transistor, is directly driven, the device output characteristics given in the published data should be consulted to determine the requirements for a safe operation below 200 milliwatts.

For detailed COS/MOS IC operating and handling considerations, refer to Application Note ICAN-6000 "Handling and Operating Considerations for MOS Integrated Circuits".

SOLID STATE CHIPS

Solid state chips, unlike packaged devices, are non-hermetic devices, normally fragile and small in physical size, and therefore, require special handling considerations as follows:

1. Chips must be stored under proper conditions to insure that they are not subjected to a moist and/or contaminated atmosphere that could alter their electrical, physical, or mechanical characteristics. After the shipping container is opened, the chip must be stored under the following conditions:
   A. Storage temperature, 40°C max.
   B. Relative humidity, 50% max.
   C. Clean, dust-free environment.
2. The user must exercise proper care when handling chips to prevent even the slightest physical damage to the chip.
3. During mounting and lead bonding of chips the user must use proper assembly techniques to obtain proper electrical, thermal, and mechanical performance.
4. After the chip has been mounted and bonded, any necessary procedure must be followed by the user to insure that these non-hermetic chips are not subjected to moist or contaminated atmosphere which might cause the development of electrical conductive paths across the relatively small insulating surfaces. In addition, proper consideration must be given to the protection of these devices from other harmful environments which could conceivably adversely affect their proper performance.

*Mil-M-38510A, paragraph 3.5.6.1 (a), lead material.

RCA
Solid State
Division

Digital Integrated Circuits Application Note ICAN-6525

Guide to Better Handling and Operation of CMOS Integrated Circuits

by J. Flood and H. L. Pujol

This Note recommends specific handling and operating practices that minimize the probability of damage to CMOS integrated circuits in the manufacturing operation and the field environment.

A description of various gate-oxide networks that protect against electrostatic discharge in both A-series and B-series RCA COS/MOS product is provided. A practical explanation of the SCR latch-up mechanism and its associated failure mode is given. In addition, operating procedures that help prevent device malfunction are described.

HANDLING CONSIDERATIONS

All CMOS devices are susceptible to damage by the discharge of electrostatic energy between any two pins. The gate input is equivalent to a small, low-leakage capacitor (5 picofarads typical) in parallel with a very high resistance (10^{12} ohms typical). This extremely high input impedance lends itself readily to the buildup of electrostatic charges. Therefore, because the gate-oxide breakdown of a CMOS device is typically 80 volts, damage by high levels of electrostatic discharge can occur.

To protect the gate oxide against high levels of electrostatic discharge, protective networks are implemented on all RCA CMOS (COS/MOS) devices, as described below.

Standard Protection Networks

Fig. 1 shows the standard protection network incorporated on all A-series devices and some B-series devices. Input-diode D_2 is a distributed resistor-diode network that appears as two diodes to V_{DD}.

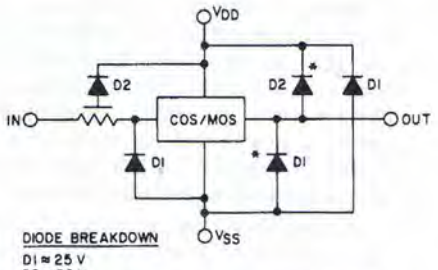

Fig.1 – Standard protection network.

Improved Protection Network

Fig. 2 shows the improved protection network incorporated on all new B-series devices as well as on all A-series, B-converted types.

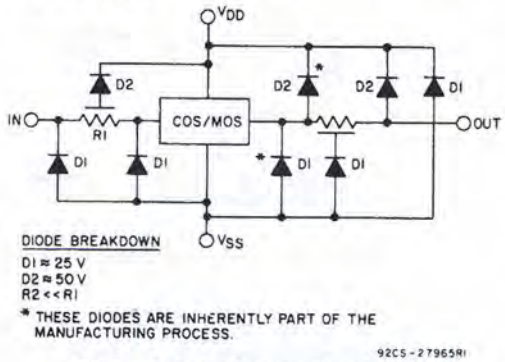

Fig.2 – Improved protection network.

Other Protective Networks

Fig. 3 shows the modified protective network for a CD4049/4050 buffer. The input diode to V_{DD} is not incorporated so that the level-shifting function can occur.

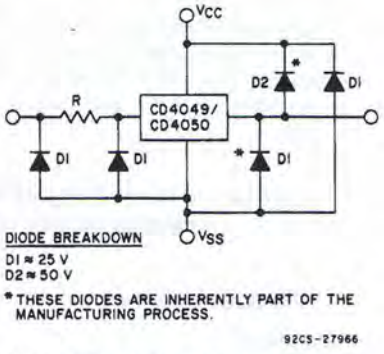

Fig.3 – Modified protection network.

Fig. 4 shows a transmission gate with the intrinsic diodes that protect against electrostatic discharge.

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Supersedes ICAN-6000

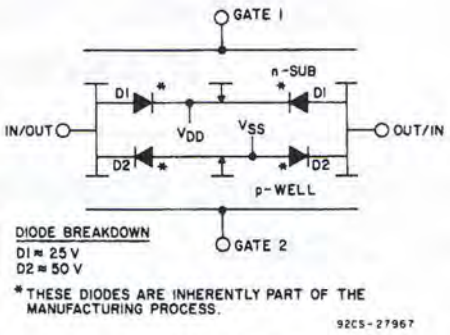


Fig.4 — Transmission gate with intrinsic diodes that protect against electrostatic discharge.

The protection networks described in this Note were characterized by using the equivalent body discharge network of Fig. 5. There are 12 possible combinations by which a device can be damaged. A discussion of the combinations is beyond the scope of

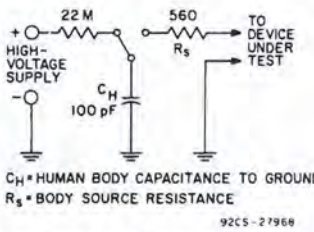


Fig.5 — Equivalent-body discharge network.

this Note; however, Table I shows worst-case protection levels for the above networks. Additional protection can be obtained by adding external series resistors at device inputs. The value of this resistance should be 10 kilohms for gate inputs and 1 kilohm for transmission gate inputs, where applicable. In addition, zener diodes at the output pins can clamp the voltage at a safe level. The zener value should not exceed the absolute maximum rating of the part.

On-chip protection networks are not used on transmission gates to maintain low on resistance. The 800-volt worst case capability is provided by the intrinsic diodes shown in Fig. 4.

TABLE I — Worst-Case Capability of Protective Networks

Protective Network	Worst-Case Capability
Standard (inc. CD4049, CD4050)	1 kV to 2 kV
Improved	4 kV
Transmission Gate	< 800 V

General Handling Rules

Table I indicates the typical, worst-case voltage levels that the above networks can withstand. Because every manufacturing environment is different, levels above those shown in Table I should be anticipated and protected against by following the handling recommendations of Table II.

Basic protection starts with personnel and materials all at the same or ground potential.

Dry weather (relative humidity less than 30 percent) tends to multiply the accumulation of static charges on any surface. Conversely, higher humidity levels (40 to 50 percent) tend to reduce the magnitude of the static voltage generated. In a low-humidity environment, the handling precautions listed above take on added importance and should be adhered to without exception.

HANDLING OF UNMOUNTED CHIPS

In handling unmounted chips, differences in voltage potential should be avoided. A conductive carrier or a carrier having a conductive overlay should be used. Another important consideration is the sequence in which bonds are made; the V_{DD} (device supply) connection should always be made before the V_{SS} (ground) bond.

HANDLING OF SUBASSEMBLY BOARDS

After COS/MOS units have been mounted on circuit boards, proper handling precautions should still be observed. Until these subassemblies are inserted into a complete system in which the proper voltages are applied, the board is no more than an extension of the leads of the device mounted on the board.

It is good practice to put conductive clips or conductive tape on the circuit-board terminals. This precaution prevents static charges from being transmitted through the board wiring to the devices mounted on it.

AUTOMATIC HANDLING EQUIPMENT

When automatic handling equipment is used, it may not always be possible to eliminate static electricity through grounding techniques alone. Automatic feed mechanisms must be insulated from the devices under test at the point where the devices are connected to the test set. The anvil transport portion of the automatic handling mechanism can generate very high levels of static electricity as a result of the continuous flow of devices over and then separating from the anvil. Total control of these static voltages is critical because of the high throughputs associated with automatic handling.

Fortunately, the resolution of this problem is simple, practical, and inexpensive. Ionized-air blowers, which supply large volumes of ionized air to objects that are to be charge neutralized, are commercially available from many supply sources. Field experience with ionized-air techniques reveals this method to be extremely effective in eliminating static electricity when grounding techniques cannot be used.

TABLE II – General Handling Recommendations

	Should be conductive	Should be grounded to common point
Handling equipment	X	
Metal Parts of Fixtures and Tools		X
Handling Trays	X	
Soldering Irons		X
Table Tops	X	X
Transport Carts	X	
Manufacturing Operating Personnel		Utilize grounded, metal or conductive plastic wrist straps with 1-megohm series resistor
General Handling of Devices		Utilize grounded, metal or conductive plastic wrist straps with 1-megohm series resistor

Failure Mechanisms

Electrical damage resulting from handling is usually caused by either of the two following failure mechanisms:

1. Low-level static electricity (voltage of 1 kV to 4 kV). Input diode protection may be overstressed and input leakage currents as high as 1 milliampere across diodes may cause a malfunction.
2. High-level static electricity (voltages greater than 4 kV). Gate oxides may become short-circuited. Inputs to V_{DD} or V_{SS} terminals will be low-impedance inputs.

The presence of these types of device malfunction can be detected by curve-tracer checks of the input protection diodes described above. Diode degradation resulting from static electricity is observable in the low-reverse-breakdown characteristics shown on the curve tracer. On the other hand, damage resulting from high levels of static electricity are observed as a resistive short to V_{DD} or V_{SS}.

Typical Manufacturing Area Procedure

The example below illustrates all of the above recommendations for handling CMOS devices in a typical manufacturing environment. Although existing protective networks offer a high level of protection against electrostatic discharge, this example emphasizes specific precautions that can help eliminate damage.

Receiving Area

Devices should not be removed from their conductive or antistatic carriers. If devices are not received in conductive or antistatic packing material, they should be returned to the supplier.

Incoming Inspection

Physical – Parts should be counted without removing them from their containers.

Storage – Devices should remain in carriers. Even a partial removal of IC's from a carrier should only be done by a grounded operator. Devices removed should be placed in a conductive tray.

Electrical – All testing should be performed by a grounded operator. Devices should be reinserted in conductive carriers after completion of a test.

PC Board Assembly

It is desirable that PC boards have shorting bars installed prior to assembly (soldering). Where possible, CMOS IC's should be the last component installed on the PC board.

Boards should be transported to the wave-solder area in conductive carriers. Flux removal should be done with an acceptable solvent. Examples of specific, acceptable alcohols are isopropanol, methanol and special denatured alcohols such as SDA1, SDA30, SDA34 and SDA44. The removal of flux from non-hermetic and molded-plastic devices by means of soap and water in a dishwasher is NOT recommended as this procedure will adversely affect the long-term life of the device.

OPERATING CONSIDERATIONS

Proper operating procedures are as important as proper handling techniques. A review of RCA COS/MOS A-series and B-series operating characteristics and ratings is given in Table III.

Operating Voltage

When devices are operated near the maximum supply-voltage range, power-supply turn-on or turn-off transients, power-supply ripple or regulation, and ground noise should be suppressed; any of the above conditions must not cause ($V_{DD} - V_{SS}$) to exceed the absolute maximum rating. A good practice is to use a zener protection diode in parallel with the power bus. The zener value should be above the expected maximum regulation

TABLE III – Maximum Ratings of RCA COS/MOS Devices (Voltages referenced to V_{SS})

DC Supply Voltage Range	3 to 15 V (A Series); 3 to 20 V (B Series)
Recommended Operating Voltage	3 to 12 V (A Series); 3 to 18 V (B Series)
DC Input Voltage Range	-0.5 to $V_{DD} + 0.5$ V
Dissipation per Package	500 mW
Device Dissipation per Output Transistor	100 mW
Storage Temperature Range	-65 to $+150^{o}$C
Operating Temperature Range	
Ceramic Package Types	-55 to $+125^{o}$C
Plastic Package Types	-40 to $+85^{o}$C
Lead Temperature (during soldering) at a distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	$+265^{o}$C

excursion, but should not exceed the maximum supply voltage. Fig. 6 illustrates a practical zener shunt circuit. A current-limiting resistor is included if the supply-current compliance is higher than the zener power-dissipation rating for a given zener voltage. The shunt capacitor value is chosen to supply required peak-current switching transients.

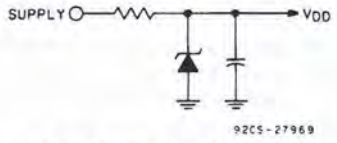


Fig.6 – Zener-diode short circuit.

Unused Inputs

All unused input leads must be connected to either V_{SS} or V_{DD}, whichever is appropriate for the logic circuit involved. A floating input on a high-current type (such as the CD4009A, CD4010A, CD4041A, CD4049A, CD4050A) can result not only in faulty logic operation, but can cause the maximum power dissipation of 500 milliwatts to be exceeded; the result may be damage to the device. Another consideration with high-current devices is the need for a pull-up resistor between the inputs and V_{SS} or V_{DD} should there be any possibility that the device terminals may become temporarily open or unconnected (e.g., if the printed circuit board driving the high-current types is removed from the chassis). A useful range of values for such resistors is from 0.2 to 1 megohm.

Input Signals

Signals should not be applied to the inputs while the device power supply is off unless the input current is limited to a steady-state value of typically less than 10 milliamperes. Input-signal interfaces that are the allowable 0.5 volt above V_{DD} or below V_{SS} should be current-limited to typically 10 milliamperes or less.

Whenever the possibility of exceeding 10 milliamperes of input current exists, a resistor in series with the input is recommended. The value of this resistor can be as high as 10 kilohms without affecting static electrical characteristics. However, speed will be reduced because of the added RC delay. Particular attention should be given to long input-signal lines where high inductance can increase the likelihood of large-signal pickup in noisy environments. In these cases, series resistance with shunt capacitance at the IC input terminals is recommended. The shunt capacitance should be made as large as possible consistent with the system speed requirements.

Fan-Out – COS/MOS to COS/MOS

All RCA COS/MOS devices have a dc fan-out capability of greater than 50. The reduction in COS/MOS switching speed caused by added capacitive loading should, however, be consistent with high-speed system design. The input capacitance is typically 5 picofarads for most types; the CD4009 and CD4049 buffers have a typical input capacitance of 15 picofarads.

Maximum Clock Rise and Fall Time

All COS/MOS clocked devices show maximum clock rise- and fall-time ratings (normally 5 to 15 microseconds). With longer rise or fall times, a device may not function properly.

Parallel Clocking

When two or more different CMOS devices use a common clock, the clock rise time must be kept at a value less than the sum of the propagation delay time, the output transition time, and the setup time. Most flip-flop and shift-register types are included in this rule and are so noted in the individual data sheets.

Output Short Circuits

Shorting of outputs to V_{SS} or V_{DD} can cause the device power dissipation to exceed the safe value of 500 milliwatts. In general, outputs of these types can all be safely shorted when the device is operated with $(V_{DD} - V_{SS}) \geqslant 5$ volts, but the 500 milliwatt dissipation ratings may be exceeded at higher power-supply voltages. For cases in which a short-circuited load, such as the base of a p-n-p or n-p-n bipolar transistor, is directly driven, the device output characteristics given in the published data should be consulted to determine the requirements for safe operation below 500 milliwatts. Note that a single output transistor short must be limited to 100 milliwatts.

SCR Latch-Up

Operation above maximum ratings can force CMOS devices into a p-n-p-n SCR "latch-up" mechanism, which can be destructive. Any transients should be avoided and any large loads occurring during operation near the maximum rating should be avoided.

"Latch-up" is considered to be the creation of a low-resistance path between the power supply and ground on a circuit during an electrical pulse; the path remains a low-resistance path after the pulse. In CMOS circuits, several parasitic bipolar transistors exist, as shown in Fig. 7. The p-n-p transistor

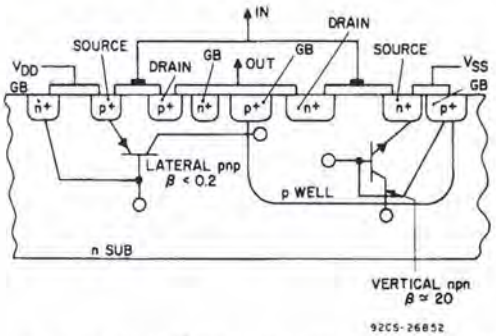


Fig.7 – Parasitic bipolar transistors in CMOS circuits.

is a wide-base lateral structure whose β, normally less than 0.2, is a function of device geometry. The conditions for SCR turn-on are as follows:

1. β n-p-n x β p-n-p $\geqslant$ 1
   (vert.) (lat.)
2. The lateral p-n-p and vertical n-p-n base emitter junctions are forward biased
3. The bias circuit that applies power to V_{DD} and to the input must be capable of supplying current equal to the holding current of potential SCR's.

Fig. 8 shows the equivalent circuit for the SCR structure present in CMOS circuits.

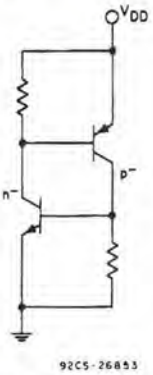


Fig.8 – Equivalent circuit for the SCR structure present in CMOS circuits.

Fig. 9 shows a curve of I_{DD} as a function of V_{DD}, which illustrates the effect of secondary breakdown and SCR latch-up.

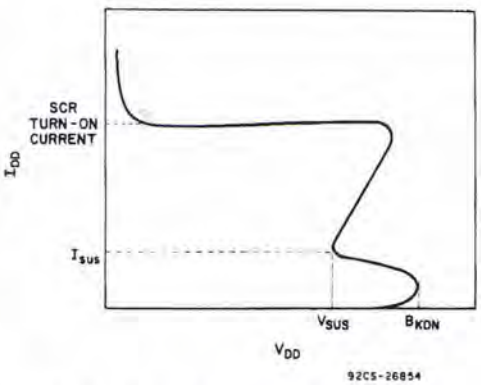


Fig.9 – Curve illustrating effect of secondary breakdown and SCR latch-up.

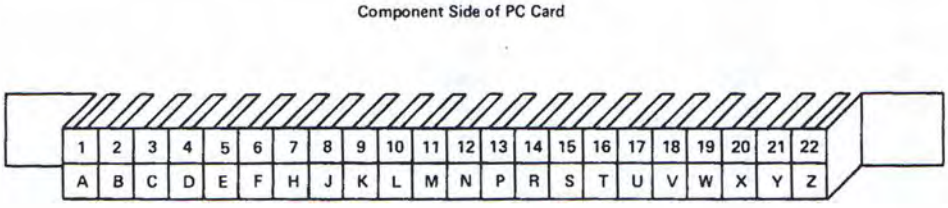
Table IV shows typical values of breakdown voltage and sustaining voltage and current for RCA COS/MOS A-series and and B-series devices. The table shows that B-series devices are much harder to latch than A-series types because of the higher breakdown voltage.

TABLE IV – Breakdown Voltage and Sustaining Voltage and Current Values

Characteristic	A-Series	B-Series
$V_{BKDN_{min}}$	17 V	25 V
V_{sus}	15 V	22 V
I_{sus}	Type-Dependent 2–40 mA	50–100 mA

APPENDIX A

CONNECTOR PIN PLACEMENT



APPENDIX B

CONNECTOR PIN ASSIGNMENT

PIN NUMBER	P1 SYSTEM CONNECTOR	P2 CPU CONNECTOR	P3 USER I/O CONNECTOR*
1	-5 V	$\overline{EF4}$	
2	V_{BAT}	$\overline{EF3}$	
3	DO6	$\overline{EF2}$	
4	DO5	EF1	
5	DO4	MA0	
6	DO3	MA1	
7	DO2	MA2	
8	DO1	MA3	
9	DO0	MA4	
10	DI7	MA5	
11	DI6	MA6	
12	DI5	MA7	
13	DI4	TPB	
14	DI3	$\overline{TPA}$	
15	DI2	$\overline{MWR}$	
16	DI1	$\overline{INTERRUPT}$	
17	DI0	$\overline{DMA\ OUT}$	
18	DATA STROBE	$\overline{DMA\ IN}$	
19	EIA 5, 6, 8	$\overline{XTAL}$	
20	PTR	$\overline{EXT\ CLEAR}$	
21	EIA 2	$\overline{EXT\ WAIT}$	
22	GND†	GND	
A	GND	N0	
B	V_{CC}	N1	
C	+12 V	N2	
D	V_{LED}	V_{CC}	
E	DO7	BUS0	
F	DATA READY	BUS1	
H	V_{TTY}	BUS2	
J	---	BUS3	

* Not assigned - user option.
† Ground connection for EIA 1, 7, and to TTY D.

APPENDIX B

CONNECTOR PIN ASSIGNMENT

(Continued)

PIN NUMBER	P1 SYSTEM CONNECTOR	P2 CPU CONNECTOR	P3 USER I/O CONNECTOR*
K	DECDS	BUS4	
L	V_{DD}	BUS5	
M	I/O EXECUTION	BUS6	
N	I/O 1	BUS7	
P	I/O 2	MRD	
R	I/O 3	SC0	
S	I/O 4	SC1	
T	I/O 5	Q	
U	I/O 6	---	
V	I/O 7	---	
W	FROM TTY A	CLOCK	
X	FROM TTY B	V_{DD}	
Y	TO TTY C	$\overline{STOP}$	
Z	EIA 3	GND	

* Not assigned - user option.

J1 KEYBOARD CONNECTOR

BUS7	BUS6	BUS5	BUS4	BUS3	BUS2	BUS1	BUS0	$\overline{STOP}$	$\overline{RESET}$
20	18	16	14	12	10	8	6	4	2
19	17	15	13	11	9	7	5	3	1
GND	TPB	$\overline{MRD}$	I/O3	I/O4	$\overline{EF3}$	V_{CC}	V_{LED}	RUNP	RUNU

APPENDIX C

ASCII - HEX TABLE

LEAST SIGNIFICANT HEX DIGIT	MOST SIGNIFICANT HEX DIGIT 0	1	2	3	4	5	6	7
0	NUL	DLE	SP	0	@	P	`	p
1	SOH	DC1	!	1	A	Q	a	q
2	STX	DC2	"	2	B	R	b	r
3	ETX	DC3	#	3	C	S	c	s
4	EOT	DC4	$	4	D	T	d	t
5	ENQ	NAK	%	5	E	U	e	u
6	ACK	SYN	&	6	F	V	f	v
7	BEL	ETB	'	7	G	W	g	w
8	BS	CAN	(	8	H	X	h	x
9	HT	EM	)	9	I	Y	i	y
A	LF	SUB	*	:	J	Z	j	z
B	VT	ESC	+	;	K	[	k	{
C	FF	FS	,	<	L	\	l	¦
D	CR	GS	-	=	M	]	m	}
E	SO	RS	.	>	N	↑	n	~
F	SI	US	/	?	O	←	o	DEL

NOTES:

(1) PARITY BIT IN MOST SIGNIFICANT HEX DIGIT NOT INCLUDED.
(2) CHARACTERS IN COLUMNS 0 AND 1 (AS WELL AS SP AND DEL) ARE NON-PRINTING.
(3) MODEL 33 TELETYPE PRINTS CODES IN COLUMNS 6 AND 7 AS IF THEY WERE COLUMN 4 AND 5 CODES.

APPENDIX D

HEXADECIMAL-BINARY AND HEXADECIMAL-DECIMAL CONVERSION TABLES

HEX = BINARY	
0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001
A	1010
B	1011
C	1100
D	1101
E	1110
F	1111

HEX = DEC	
0	0
1	4,096
2	8,192
3	12,288
4	16,384
5	20,480
6	24,576
7	28,672
8	32,768
9	36,864
A	40,960
B	45,056
C	49,152
D	53,248
E	57,344
F	61,440

HEX = DEC	
0	0
1	256
2	512
3	768
4	1,024
5	1,280
6	1,536
7	1,792
8	2,048
9	2,304
A	2,560
B	2,816
C	3,072
D	3,328
E	3,584
F	3,840

HEX = DEC	
0	0
1	16
2	32
3	48
4	64
5	80
6	96
7	112
8	128
9	144
A	160
B	176
C	192
D	208
E	224
F	240

HEX = DEC	
0	0
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8	8
9	9
A	10
B	11
C	12
D	13
E	14
F	15

APPENDIX E

UT4 INSTRUCTION SUMMARY

1. Memory Load

   a) General

      !M [starting address]Δ[data][optional , or ;] CR

      1) data can have non-hex digits between hex pairs
      2) continue a line by ending previous line with ,
      3) ending line with ; requires specification of a new starting address

   b) Examples

      1) !M00 F8FFA4B424943A04 CR

         or

         !M00 F8 FF A4 B4 24 94 3A 04 CR

         or

         !M00 F8FFA4B4,CRLF
         24943A04 CR

         or

         !M00 F8FFA4B4;CRLF
         0004 24943A04 CR

         Each of the above examples enters the 8 bytes indicated starting at address 0000 and ending at address 0007.

      2) !M00 F8FF (NXT BYT) A4B424943A04 CR
         will have the same result as 1). Note however that hex characters (0-9, A-F) are not allowed in embedded text.

      3) Incorrect load instructions

         !M F8FFA43424943A04 CR
         - no starting address

         !M00F8 ------
         - missing space between starting address and data

         !M00 F8FFA CR
         - odd number of hex characters
         (UT4 responds with a ? and the last hex digit is not entered into memory.)

APPENDIX E

UT4 INSTRUCTION SUMMARY

(Continued)

2. Memory Read

a) General

?M[starting address]Δ[hex number of bytes to be typed]CR

b) Examples

1) ?M00 8CR

will print the 8 bytes starting at address 0 in the following format:

0000 F8FF A4B4 2494 3A04

2) ?MF0 10CR

will print the 16 bytes (equivalent to 10 in hexidecimal notation) starting at address F0 as follows:

00F0 HHHH HHHH HHHH HHHH HHHH HHHH HHHH HHH

Note: H = Any hex digit which happens to be in memory.

3. Program Start

a) General

$P[starting address]CR

Starts program at the starting address specified with X set to 0 and with R0 as Program Counter.

b) Examples

$P00CR

Starts program at location 0 with X set to 0 and R0 as Program Counter.

APPENDIX F

DATA TERMINAL CONNECTIONS

Check List for 20-mA Current Loop Interface.

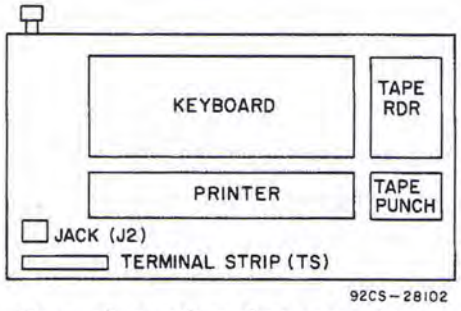
1. Make sure the TTY is configured for 20-mA current loop operation.

2. Verify that the assembly procedure for this interface configuration has been followed by checking whether the following items have been correctly inserted and soldered on the Evaluation Kit PC card.

Links: LK8B (Make sure LK8A and LK9 are open)
Resistors: R3, R16, R17, R19, R22, R23, R24
Capacitors: C8, C9
Transistors: Q1, Q2

3. Locate the four 20-mA current loop interface terminals on either the jack J2 or the terminal strip TS of the TTY, and make the connections to the Evaluation Kit as shown in the figure below.

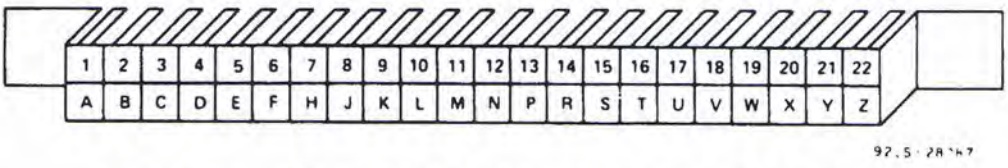
4. Choose an appropriate value for R24 to provide for 20 mA of current when Q2 saturates. For TTY 33ASR, R24 should be about 220 ohms. For other data terminals, refer to application note "TTY Terminal Interface Considerations for RCA Microprocessor Evaluation Kit CDP18S020," ICAN-6551 for instructions on determining a suitable value for R24.



Top view of teletypewriter terminal showing relative position of key components.

TELETYPE 33ASR		EVALUATION KIT SYSTEM CONNECTOR
TS	OR J2	P1
4	6	P1-W
3	5	P1-X
7	8	P1-Y
6	7	P1-22

20-mA current loop interface connections for Teletype terminal 33ASR and Evaluation Kit CDP18S020.



Evaluation Kit CDP18S020 connector pin placement.

APPENDIX F

DATA TERMINAL CONNECTIONS

(CONTINUED)

Check List for EIA RS232C Interface.

1. Consult the instruction manual provided by the manufacturer of the data terminal for information on where to access the EIA RS232C interface signals.

2. Verify that the assembly procedure for this interface configuration has been followed by checking whether the following items have been correctly inserted and soldered on the Evaluation Kit PC card.

Links: LK8A, LK9 (Make sure the LK8B is open)
Resistors: R3, R4, R15, R16, R17, R18, R19, R20, R21, R22, R23, R24, R25
Capacitors: C8, C9
Transistors: Q1, Q2, Q3

3. Connect the EIA RS232C interface signals from the data terminal to the Evaluation Kit as shown in the Table below.

4. Connect a - 5-volt power supply to P1-1 of the Evaluation Kit.

EIA RS232C DATA SET PIN NUMBER	SIGNAL FUNCTION	TI SILENT 700 JACK J1	CDP18S020 EVALUATION KIT PIN NUMBER
1	PROTECTIVE GROUND	A	P1-22
2	TRANSMITTED DATA	H	P1-21
3	RECEIVED DATA	10	P1-Z
4	REQUEST TO SEND	F	*
5	CLEAR TO SEND	8	P1-19
6	DATA SET READY	9	P1-19
7	SIGNAL GROUND (COMMON RETURN)	7	P1-22
8	DATA CARRIER DETECT	K	P1-19
20	DATA TERMINAL READY	6	*

* No connection necessary

Set of EIA RS232C signals most commonly used in data terminals.

APPENDIX G

LINK LIST

LINK	INITIAL STATUS	FROM	TO	FUNCTION
LK1A	IN	U2/22	GND	2704 GND
LK1B	OUT	U2/22	U8/6	2708 A9
LK2	IN	U6/9	U22/15,U6/3	U2 Memory Definition*
LK3	IN	U6/10	U6/5	U2, U3 Memory Definition*
LK4A	OUT	U5/23	U9/36	U5 SERVICE REQUEST on INTERRUPT
LK4B	OUT	U5/23	U9/22	U5 SERVICE REQUEST on EF3
LK5	IN	U9/7	MRD MEMORY	Memory Control for Possible Keyboard Functions
LK6	IN	U9/35	MWR MEMORY	Memory Control for Possible Keyboard Functions
LK7A	IN	U9/1	Crystal	Onboard Crystal Clock Oscillator Hookup
LK7B	OUT	U9/1	P2-W	External Clock Generator Input
LK8A	OUT	U9/21	U11/2	EIA RS232C Data In Polarity
LK8B	OUT	U9/21	U11/3	TTY 20 mA Current Loop Data In Polarity
LK9	OUT	GND	P1-Y,R24	EIA RS232C Data Out Hookup
LK10	OUT	V_{TTY}	V_{LED}	LED and Terminal Interface Supply Separation
LK11	OUT	V_{CC}	V_{RAM}	V_{CC} for RAM's

* More restrictive memory location definition signals may be supplied at U22/15, U6/3 and U6/5 after removal of LK2 and LK3 respectively. Also note that a more restrictive memory location definition signal can be supplied at U1/18 when U1 is not in the system in order to more uniquely define the location of the 4K of RAM within the lower 32K of memory.

NOTE: The notation U2/22 denotes package U2/Pin 22.

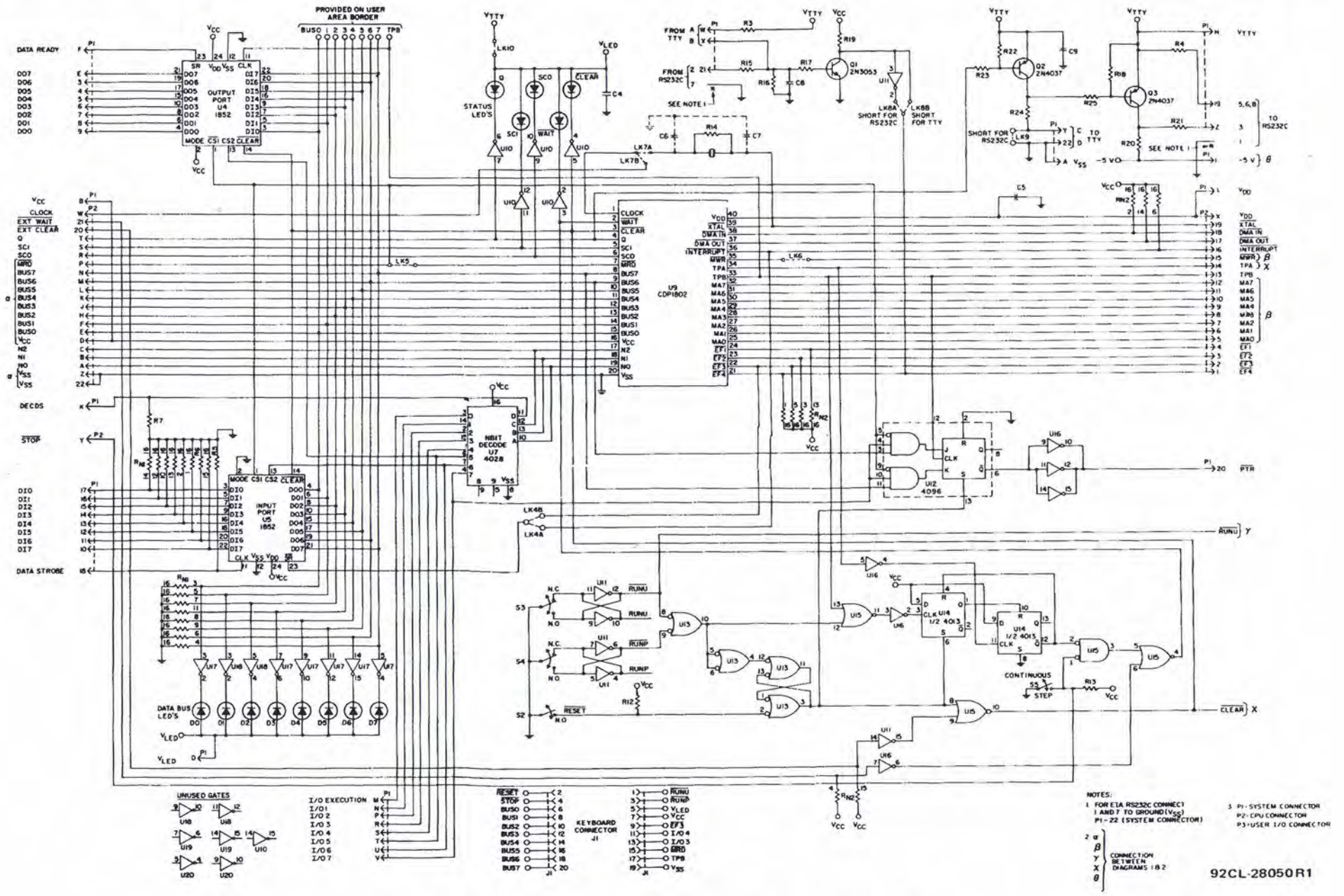


Fig. H-1 - Diagram of CPU, control, and I/O logic.

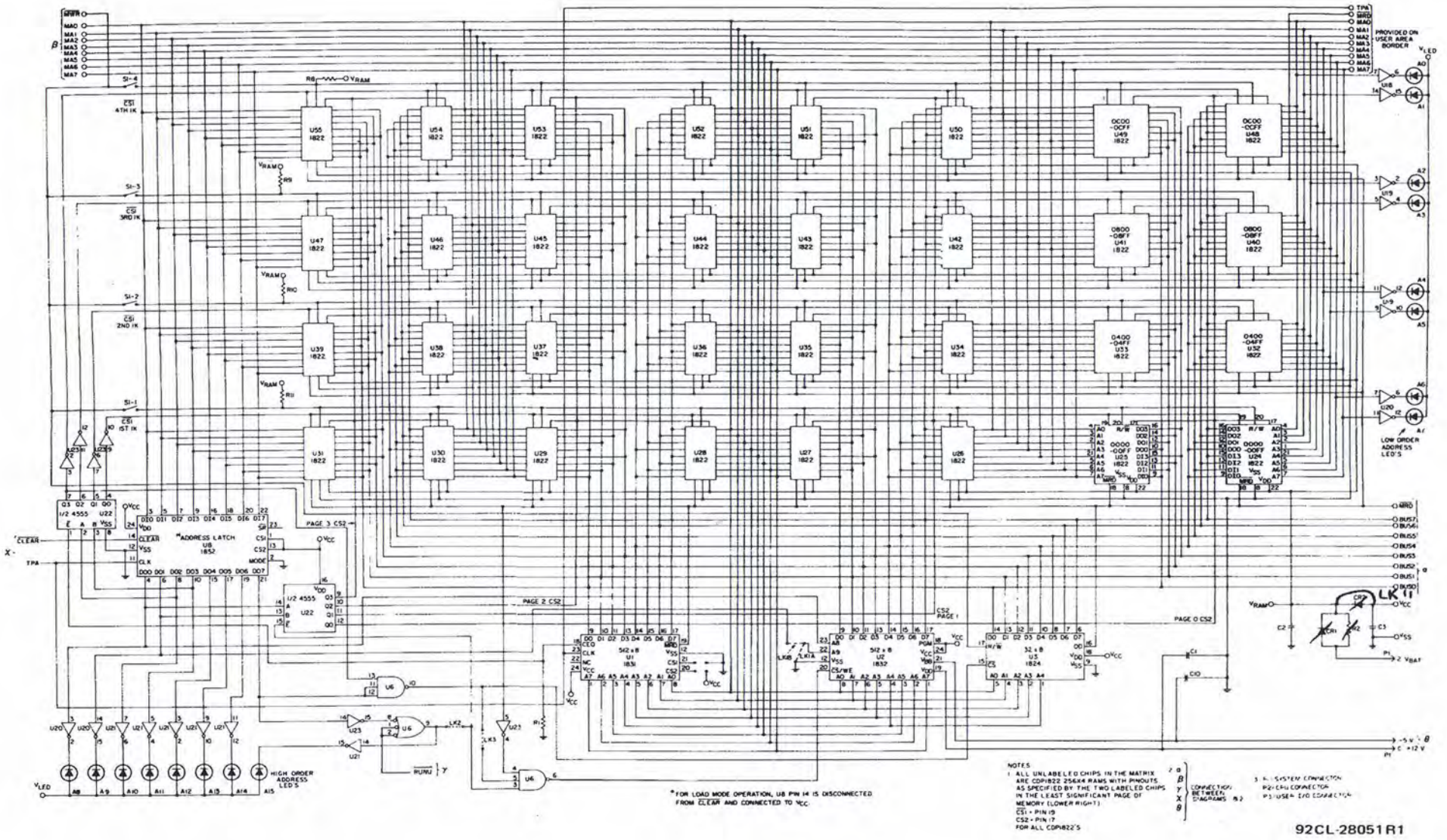


Fig. H-2 - Logic diagram of memory organization.

APPENDIX I

LOAD MODE ADAPTATION

When the Evaluation Kit is used in the Load Mode, both $\overline{WAIT}$ and $\overline{CLEAR}$ control signals must be asserted (driven to the low voltage level V_{SS}). On the Evaluation Kit PC card, $\overline{CLEAR}$ is also connected to the clear function on the Address Latch (U8 Pin 14). This connection prevents the generation of the higher 8 bits of the Memory Address while in the Load Mode. In order to allow for the loading of more than one 256-byte page of memory (more than an 8-bit address), the following change must be implemented:

1. On the component side of the PC card, locate the printed conductor running vertically from U8 Pin 14 to a "via" hole just above the "A" in the silk-screened "ADDRESS LATCH" label (above IC location U8). See Fig. 1.

2. Cut this conductor just below the "A" in the word "ADDRESS" with an Exacto knife or similar tool.

3. With a piece of insulated jumper wire, connect U8 Pin 14 to V_{CC} at the location labelled "V_{CC}" directly to the left of U8 Pin 21. See Fig. 1.

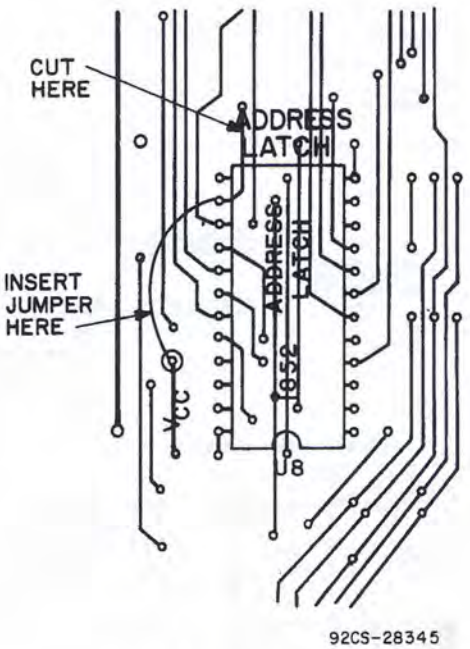


Fig. 1.

APPENDIX J
TELETYPE TERMINAL REMOTE READER CONTROL

A simple wiring change inside the conventional Model 33 Teletype terminal permits the paper-tape reader to be operated under control of an external COSMAC (program-derived) signal. The modifications are indicated in Fig. J1. Two additional components must be appropriately mounted: an electronic relay and a switch. Wiring to be added is indicated by the bold line in the diagram. Note that the wiring connects the added switch and relay to points on the front mode switch and in the array of white plastic Molex connectors located in the back of the unit under the cover. Note also that one brown wire must be broken and reconnected as shown.

System connector P1 contains the logic necessary to permit a COSMAC program to control the paper-tape reader. With the added reader control switch in the remote or open position, a program may turn the reader on and off. In the manual or closed position, the reader can be controlled only manually, by means of the original reader control switch on the tape reader. Note particularly that this latter switch must also be activated (in the start position) in order for the remote program control to operate properly.

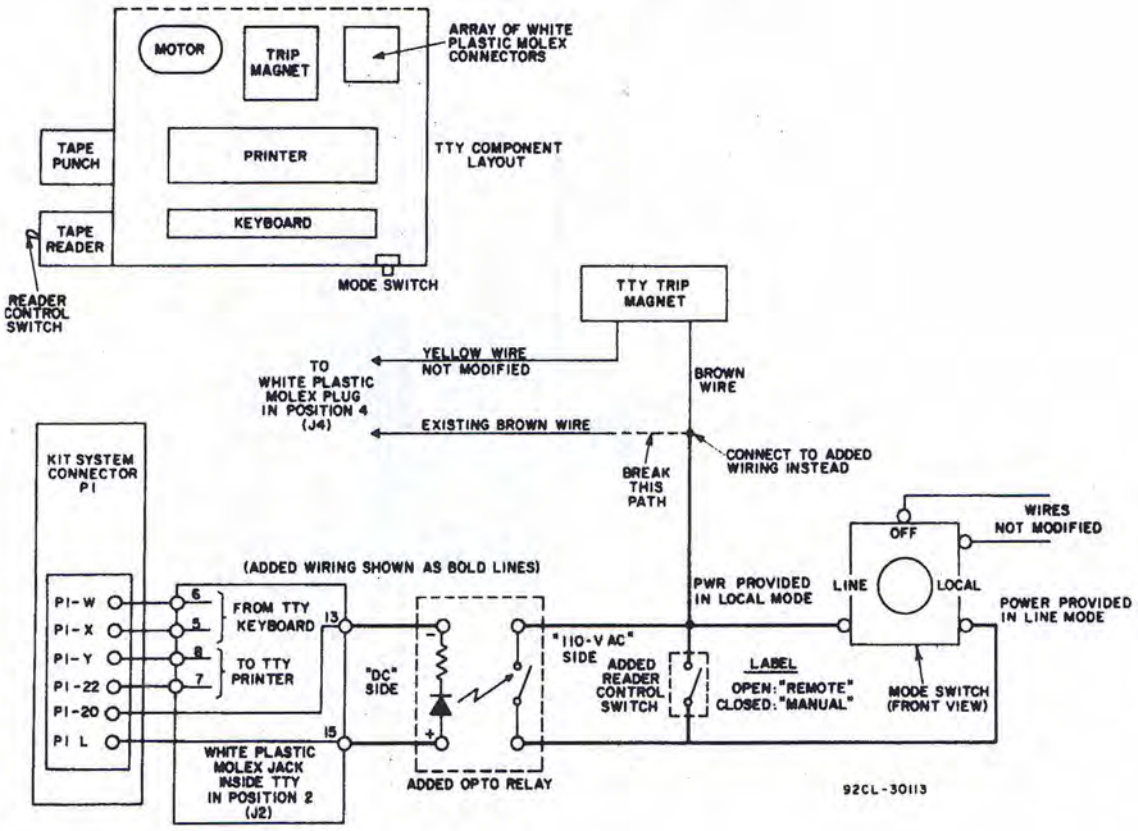


Fig. J-1.

APPENDIX K
CONNECTING THE TI DATA TERMINAL TO THE KIT EIA RS232C INTERFACE

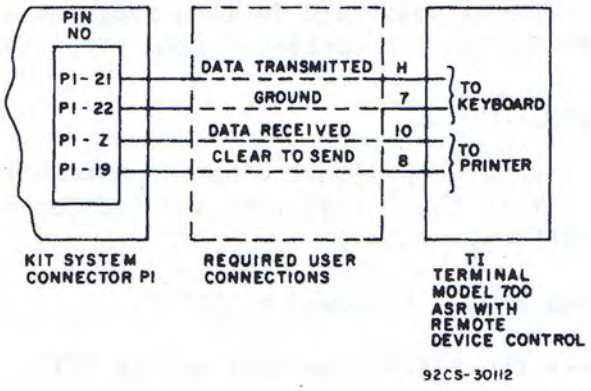


Fig. K-1 - Connections required.

APPENDIX L
LOADING PROGRAMS

Programs may be entered manually by use of the !M command. Ordinarily, programs are loaded from paper tape via a TTY, or from magnetic tape cassettes via the TI terminal.

Following are the methods used to load programs into the Evaluation Kit CDP18S020 or the EK Design Kit CDP18S024 from paper tape and magnetic cassette:

Paper Tape Systems

To load a paper tape (including the Assembler or Editor): Put the TTY in the "Line" mode and the installed switch in the "MANUAL" position.

1) Press RESET, followed by RUN U.

2) Press the Return Key (CR) on the TTY.

3) UT4 will return the symbol * indicating it is ready to accept commands.

4) Position the tape in the NULL header and turn on the tape reader.

5) When loading is complete, UT4 will issue another *. Turn off the reader and remove the tape.

6) To start the program at location zero, type $PØ(CR).

If preferred, typing can be suppressed during paper-tape loading by pressing the LINE FEED Key instead of CR at Step 2. In this case, the user should re-initialize the system after loading by pressing RESET, RUN U, and CR before attempting to start the loaded program at Step 6.

UT4 monitors the program being loaded and will issue a ? if a format error is detected. If an error is detected, stop and reload the tape from the beginning starting with Step 1.

To Punch Reloadable Tape

1) With the TTY in the "LOCAL" mode, position tape in the punch, turn the punch ON, and make a header of nulls (control-shift-p and the repeat key).

2) Type

!Maaaa

where aaaa is the hex address of where the data is to be reloaded (normally, location ØØØØ).

3) Turn the punch OFF and put the TTY in the LINE mode.

4) Initialize the EVALUATION KIT with a RESET, RUN U, followed by a RETURN (CR).

5) Next, type

?Maaaa Δ count

where the address is the starting address of data to be read from memory, and count is the number of bytes, in hex, to be punched.

6) Turn the punch ON and press CR. After the tape is punched, some more nulls should be added to its end as in Step 1.

The Assembler and Editor programs automatically punch reloadable tape as described in the next section.

Magnetic Tape Systems

To load a magnetic tape (including the Assembler and Editor):

1) Press RESET, RUN U, then CR.

2) UT4 will return the prompt *.

3) Mount the cassette. Rewind it and press LOAD/FF to advance to the first record. Make sure the drive is in the LINE and PLAYBACK mode.

4) Press CONT/START on the playback control; Tape starts to load.

5) When loading is completed, UT4 will issue another *. Start the program by typing $PØ(CR). If a ? is typed during loading, an error has been detected and the tape should be reloaded.

To Record Reloadable Tape

1) Put the drive in the LOCAL and RECORD mode.

2) Mount a blank cartridge, and press Load/FF to advance to first record.

3) Turn "Record Control" switch on.

4) Type

!Maaaa Δ

where aaaa is the hex address of where data is to be reloaded (normally, location ØØØØ).

5) Switch the drive to the LINE mode and initialize the KIT with a RESET, RUN U and CR.

6) Type

?Maaaa count,

where aaaa is the starting address of the data to be read from memory, and count is the number of hex bytes to be recorded.

7) Turn the Record Control switch ON and press CR. The data should now record on tape. After the data has been recorded, UT4 will issue another *.

8) Turn the Record Control switch off.

Preface

TINY BASIC provides the most fundamental of those functions normally attributed to the high-level programming language called BASIC. It is specifically designed for a microcomputer with minimal memory. The TINY BASIC interpreter program requires only 2K bytes of storage. Thus, an Evaluation Kit with 4K of RAM can accomodate modest (about 100 statements in length) TINY BASIC programs.

TINY BASIC is perhaps the best language for the beginning microcomputer programmer. It is easily learned, and elementary application programs may be developed quickly. For the more experienced programmer, TINY forms the kernel of a system whose facilities may be extended indefinitely by the addition of machine-language subroutines (limited only by the amount of memory which is available).

TINY packs a significant amount of processing capability within 2K bytes. For example, it includes its own line editor, and it provides a rich assortment of error messages to the user. However, clearly one cannot expect certain features which are normally available only in 8K systems. For example, TINY does not do floating-point arithmetic. (Its numeric capability is limited to integers in the range -32768 to +32767.) It cannot directly handle arrays or alphanumeric strings. (On the other hand, each of these (and other) advanced facilities may be added via a machine-language extension). In addition, one must recognize that economies in memory space used were achieved at the expense of processing speed.

Generally, then, TINY BASIC may be considered as a good "budget" high-level language for a user with a comparable microcomputer setup. Although TINY is quite slow and is of limited capability, it can act as the nucleus of a system whose sophistication may be indefinitely extended.

COSMAC TINY BASIC

INTRODUCTION

We assume that you are already familiar with section III of the Evaluation Kit Manual which explains the functions available from the resident utility program UT4. UT4 permanently resides in memory locations 8000-81FF. After it is given control (via the RESET, RUN U, CR or LF sequence), it types its prompt character, an asterisk, indicating that it is awaiting your input. Each of your input lines (terminated with a CR) is interpreted and executed by UT4. After disposing of your input command, UT4 indicates that it is ready for new input by typing another * prompt.

One important function of UT4 is to permit you to load an arbitrary sequence of hexadecimal digits (a machine language program) into an arbitrary area in memory and then to invoke this program (transfer control to it; run it) via the appropriate $P command. When your program completes its computation, it may relinquish control back to UT4 by executing a C08039 instruction (a long branch to the location labeled START on p.3-16), provided all registers used by UT4 have the values they had when UT4 exited.† Under these conditions, a user program halt (or exit) would be signified by a new * UT4 prompt.

COSMAC 2K TINY BASIC is a program which must be loaded into the lowest 2K bytes of memory (locations 0000-07FF). A hexadecimal listing of the program and loading instructions for it appear in Appendix A. After TINY BASIC is made resident, control is transferred to it using the proper $P UT4 command (see Appendix A). Once it receives control, TINY BASIC delivers its prompt character, a colon, and awaits your input. Each time after it has properly disposed of an input line (terminated with a carriage return - CR), TINY BASIC again types its : prompt.

---

† In particular, P should be 5.

If an input line does not begin with a number, TINY BASIC immediately interprets it and executes it. (The line is called a statement.) If the line begins with a number (normally followed by a statement), then TINY BASIC merely stores it, in the proper position, in an area of memory where the user program (a sequence of statements ordered by statement number) is assembled. If the statement number is the same as one already existing in this area, then the new statement replaces the old one. Thus, you load a TINY BASIC program by entering a sequence of statements (one per line), each preceded by a unique statement number. The program must have at least one END statement in it.

After your program has been loaded, you can run it by typing a RUN command (equivalent to the $P command to UT4). TINY BASIC will then interpret and execute your program's statements, in order, following the rules discussed in subsequent sections. When an END statement is encountered during execution, control will be passed back to TINY BASIC's "enter" mode, and another : prompt will be issued.

Note that TINY BASIC assembles statements which begin with numbers into the program area in memory without any further analysis. Errors are detected only when execution is attempted. If an entered line consists only of a line number, it is considered a deletion. The previously inserted statement with the same line number is erased. Note also that 0 is not a valid line number. Blanks within a line have no significance to TINY. All spaces, until the first non-numeric character, are totally ignored. After that, however, blanks are preserved in the memory copy of the statement (i.e., each blank character occupies one byte).

NUMBERS

A number is any sequence of decimal digits optionally preceded by a sign. If no sign is present, the number is assumed positive. Since TINY BASIC stores all numbers internally as 16-bit signed integers, positive values may run from 0 to 32767 (2^{15}-1) and negative values may run from -1 to -32768 (-2^{15}).

VARIABLES

A variable is any single capital letter (A-Z). Each possible variable is assigned a unique two-byte location in memory. The value of the variable is the contents of that location -- i.e., a number in the range -32768 to +32767.

EXPRESSIONS

An expression is a combination of one or more numbers or variables, joined by operators and possibly grouped by parenthesis pairs. The permissible operators are:

- `+` addition
- `-` subtraction
- `*` multiplication
- `/` division

Whenever TINY BASIC encounters an expression within a statement (during its execution) it evaluates the expression -- combining the numbers and the values of the variables, using the indicated operations. The exact disposition of the final computed value depends on the type of statement. This is discussed further later.

Internal sub-expressions within parentheses are evaluated first. Usually parentheses make clear the order in which operations are to be performed. However, if there is ambiguity because parentheses are absent, TINY gives precedence to multiplication and division over addition and subtraction. Thus, in evaluating

```
B-14*C
```

the multiplication is performed first. In cases involving two operators of equal precedence, evaluation would proceed from left to right. An expression may be optionally preceded by a sign.

Note that during the evaluation of an expression, all intermediate values, and the final value, are truncated -- using the lowest 16 bits of the results. That is, expressions are evaluated modulo 2^{16}. TINY BASIC makes no attempt to discover arithmetic overflow conditions, except that an attempt to divide by zero results in an error stop.

The following are some examples of valid expressions:
(Note that a single variable or number is also an expression.)

```
A
123
1+2-3
B-14*C
(A+B)/(C+D)
-128/(-32768+(I*I))
((((Q))))
```

The following are some examples of

```
-4096
15*4096
32768/8
30720+30720
```

because any number in the range 32768 to 65535 (2^{15} to 2^{16}-1) has a sign bit of 1(making it negative), so that it is actually treated by TINY BASIC as if 65536 (2^{16}) were subtracted from it.

THE RND FUNCTION

TINY BASIC includes the ability to generate a positive pseudo-random number in a specified range. Whenever it encounters the form

RND (expression 1, expression 2)

during execution of a statement, TINY generates a random number in the range from the value of expression 1 to the value of expression 2, inclusive. The resulting number may be used as would any other number. In particular, the above form may itself be used within another expression. If the arguments are invalid, an error stop may result.

THE RND FUNCTION (cont'd)

```
RND (1,100)
RND (A,B)
```

are valid RND functions (assuming 0<A<B).

STATEMENT TYPES

A statement normally begins with a keyword, such as PRINT or GOTO, indicating the type of statement. The interpretation of the remainder of the statement depends on this keyword. In some cases, a short form of the key word is also acceptable -- for example, PR instead of PRINT.

REM STATEMENT

Following the keyword REM (for remark or comment) any sequence of characters may appear. This statement is ignored by TINY BASIC. It is used to permit you to intersperse arbitrary comments or remarks within your program.

END STATEMENT

END must be the last statement executed in a program. It is used to halt execution and return to TINY BASIC's "enter" mode. There may be as many END statements in a program as needed.

LET STATEMENT

This statement has the form

```
LET variable = expression
```

Alternatively, the keyword LET may be omitted entirely. Execution of this statement assigns the value of the expression to the variable. The following are valid LET statements:

```
LET A = B+C
I = I+1
J = 0
LET Q = RND (5,33)
```

IF STATEMENT

This statement has the form

IF expression1 relation expression2 THEN statement

The keyword THEN may be omitted entirely. Execution of this statement evaluates the two expressions and compares them according to the relation specified. If the condition specified is TRUE, then the associated statement is executed. Otherwise, the associated statement is skipped. The permissible relational operators are as follows:

=	equal
<	less than
>	greater than
<=	less than or equal (not greater)
>=	greater than or equal (not less)
<> or ><	not equal (greater than or less than)

The associated statement may be any other valid TINY BASIC statement including, in particular, another IF statement. The following are some valid IF statements:

```
IF I>25  THEN END
IF A>B  IF B>C  I=I+1
```

(The last statement increments I only if B is between C and A.)

TRANSFERS OF CONTROL

TINY BASIC normally executes statements in a program in statement number order. The following statements may be used to alter this flow:

(a) GOTO expression

The subsequent statement executed is the one whose line number equals the value of the expression. Note that this permits you to compute the line number of the next statement on the basis of program parameters during execution. The following are some valid GOTO statements:

```
GOTO 100
GO TO 200 + I*10
```

(b) GOSUB expression

This statement executes exactly as does the GOTO statement, except that in addition TINY records (remembers) the statement number of the following statement (the one which would have been executed next, had the branch not taken place).

(c) RETURN

This statement (which also has the short form RET) executes by transferring control back to the statement whose number was last recorded as the result of the execution of a GOSUB. This last-recorded statement number is also forgotten.

SUBROUTINE NESTING

A subroutine is a sub-program which is normally evoked in two or more places within a main program. Rather than duplicate the statements of the sub-program in several places, it appears only once. It is written so that it exits with a RETURN statement. It is evoked at any point in a program by a GOSUB statement which transfers control to it.

Whenever one subroutine calls another subroutine (termed subroutine "nesting"), an additional "return-statement-number" is recorded. These are stored in order, so that every RETURN jumps back to the statement following the GOSUB which called it. Subroutines may be nested to any depth, limited only by the amount of user program memory remaining.

PRINT STATEMENT

This statement has the form

PRINT printlist

where printlist is a succession of one or more items to be printed separated by either commas or semicolons. The acceptable short form for PRINT is PR. Each print item may be either an expression or a character string enclosed in quotes. In the first case the value of the expression is typed. In the second case the character string is printed verbatim. No spaces are generated

between the printouts of items separated by semicolons in the PRINT statement. On the other hand, the printout of an item, preceded by a comma in the PRINT statement, begins at the next "tab setting". Tabs are automatically set every eight character spaces. Thus,

```
PRINT 1,2,3  prints as
1       2       3
```

while PRINT 1;2;3 prints as

```
123
```

Commas and semicolons, character strings and expressions may be mixed in one PRINT statement in any manner.

Normally, the execution of a PRINT statement terminates with the generation of a carriage return and line feed to begin a new line. However, if the PRINT statement ends with a comma or semicolon, then the CR-LF sequence is suppressed, permitting subsequent PRINT statements to output on the same line or permitting an input message (see INPUT, next) to appear on the same line as previous output.

The following are valid PRINT statement examples:

```
PRINT "A=";A,"B+C=";B+C
PR                          (generates a blank line)
PRI                         (prints the value of variable I)
PRINT 1,",",Q*P;",",R/42;
```

INPUT STATEMENT

This statement has the form

```
INPUT inputlist
```

where inputlist is a succession of one or more variables separated by commas. The acceptable short form for INPUT is IN. Normally, execution of this statement begins with the typing of a question mark prompt indicating that TINY is expecting the user to type in data. The user should respond by typing in a line of one or more expressions separated by commas and terminated with a carriage return. Each input expression is evaluated and assigned to its associated variable in the INPUT statement.

If the number of requested variables in the inputlist is not satisfied by the number of expressions in the user's input line, a new ? prompt will be issued asking for more input information. If the number of expressions in the user's input line is greater than the number of requested variables, then those input expressions not requested are saved internally and used to satisfy subsequent INPUT requests. Thus, before a ? prompt is issued during execution of an INPUT instruction, TINY first checks to see if any saved expressions exist. If so, then these are used first - to satisfy some or all of the variables requesting values. Only when no saved data exists is the ? prompt issued. The user is cautioned to use the latter property of the INPUT statement with care.

Example: Suppose statement INPUT X,Y,Z is executed, and the user responds by typing A,C,B. The results are the same as if X=A, Y=C and Z=B had been executed. Note that commas are required in the user's input line only to avoid ambiguity. If he had entered ACB, the same results would have occurred. On the other hand, an input line of +1 -3 +6 0 in response to INPUT A,B,C,D will result in A being given the value 58 and a new ? prompt issued for values for B,C and D.

SYSTEM CONTROL STATEMENTS

The statements listed below are normally not included as part of a program. That is, they are normally entered without line numbers:

(a) NEW

Execution of this statement clears the program area in memory. It is used before entering a new program.

(b) RUN

Begin program execution at the first (lowest) line number. Note: If RUN is followed by a comma followed by a sequence of one or more expressions (separated with commas), then the expression list is treated as an initial input line -- which will be scanned first whenever INPUT statements are executed. (See discussion of INPUT statement.)

(c) LIST

LIST expression

LIST expression, expression

SYSTEM CONTROL STATEMENTS (cont'd)

(c) (cont'd)

The LIST statement causes part or all of a stored user program to be printed. If no parameters are given, the whole program is listed. A single expression parameter is evaluated to a line number. If the line exists, it is printed. If both parameters are given, all lines with numbers in the range specified are printed.

SUMMARY OF COSMAC TINY BASIC REPERTOIRE

The following should serve as your short form guide to the facilities offered by TINY BASIC. Characters enclosed in brackets [ ] are optional and may be omitted.

FORM OF STATEMENT	BRIEF EXPLANATION OF EXECUTION
REM any comment	Ignored.
END	Halt execution and return to "enter" mode.
[LET] variable = expression	Assign the value of the expression to the variable
IF expr rel expr [THEN] statement	If the relation between the values of the expressions is TRUE, execute the statement. Otherwise, skip it.
GOTO expression	Jump to the statement whose number is the expression's value.
GOSUB expression	Save the statement number of the next statement in sequence. Then execute a GOTO.
RET[URN]	Jump to the last saved statement number (see GOSUB) and "unsave" this number.
PR[INT] printlist	Type the items in the printlist. Type values of expressions. Type quoted strings verbatim. Horizontal TAB on comma.
IN[PUT] inputlist	Read and evaluate expressions from the keyboard and assign them in order to the variables specified in the inputlist.
NEW	Clear the program area.
RUN[,expression sequence]	Start execution at first statement. (Save the expression sequence to satisfy subsequent INPUT's.)
LIST[expression][,expression]	Print entire program, or one selected line, or a range of lines.

where:

number = -32768 to +32767; variable = single capital letter.

expression = one or more numbers or variables (possibly grouped by parentheses) joined by operators +,-,*, or /.

relations are =,>,<,<=,>=,<>, or >< .

printlist = one or more expressions or quoted strings separated by commas or semicolons.

inputlist = one or more variables separated by commas.

expression sequence = one or more expressions separated by commas.

NOTE: The RND(expr1,expr2) function generates a positive random number in the range between the values of the expressions. This function may be used anywhere in place of a number.

IMMEDIATE EXECUTION VS. PROGRAM MODE

One important use of the immediate execution mode (entering a statement without a line number) is to permit line-at-a-time testing. LET, IF and PRINT can be demonstrated this way. Due to the way TINY BASIC buffers its input lines, the INPUT statement cannot be directly executed for more than one variable at a time, and if the following statement is typed in without a line number,

```
INPUT A,B,C
```

the value of B will be copied to A, and only one value (for C) will be requested from the console/terminal. Similarly, the statement,

```
INPUT X,1,Y,2,Z,3
```

will execute directly (loading X,Y, and Z with the values 1,2,3), requesting no input, but with a line number, in a program, this statement will produce an error stop after requesting one value.

Clearly there is no point to executing REM or END in the immediate mode. Furthermore, GOSUB and RETURN are normally meant for the program mode. On the other hand, an immediate GOTO has the same effect as if RUN were typed, but execution may begin at other than the program's first statement.

Similarly, the stored program should not contain a NEW statement (self destruct!), and a stored RUN statement will be equivalent to a GOTO to the first statement. On the other hand, a LIST statement may be included as part of a program and used for printing large text strings, such as instructions to the operator.

PROGRAMMING EXAMPLES

The following two simple programs are designed to give you examples of TINY BASIC in action. The first uses most of the statements in TINY's repertoire. The second demonstrates particularly the use of subroutines. REMarks are omitted from the listings to keep them short. Instead, each program is accompanied by a detailed explanation of its functioning. (It should be emphasized that omission of comments is generally bad documentation practice, but it suits our present objectives.) Each program can be entered in a few minutes. It is recommended that you run both of them to gain experience with the system.

I. Arithmetic Drill Program

This program generates a random sequence of arithmetic problems. After the program prints the problem, you respond with your solution. The program tells you whether your answer was correct or not (providing the right answer in the latter case) and then proceeds to generate a new problem, and so on.

Stepping through the program listed below: first,three random numbers are generated. The value of F (1 to 4) will be used to decide whether this will be an add, subtract, multiply or divide problem. The range of possible values for the arguments A and B was chosen to prevent the possiblity of overflow under two conditions: First, 181*181 is still less than 32767. Second, division by zero is prevented. Because TINY BASIC discards division remainders, the fourth statement is included to keep the division problems interesting. It says: If this is a division problem where the quotient would ordinarily come out as zero (true for many of the A,B combinations that might be generated), arbitrarily increase the size of the dividend (to a maximum of 18100 in this case) to make the problem non-trivial. Statement 50 begins the presentation of the problem to the user by printing an encouraging message followed by the value of the first argument. Notice that the final semicolon keeps the printer on the same line without advancing the carriage further.

Statement 60 does a four-way branch based on the value of F (the arithmetic function selected). Thus, control passes next to one of the following statement numbers: 70, 100, 130 or 160. Each of these statements begins a short sequence which prints the sign for the arithmetic operation and then computes the proper

I. Arithmetic Drill Program (cont'd)

function, placing the result in C. (Notice the final semicolons again, in the PRINT statements.) No matter which path is taken, control passes next to statement 180, which prints the second argument value followed by an = sign. The presentation of the problem to the user is now complete, and the INPUT statement at 190 delivers a ? prompt on the same print line and reads the user's answer into D. Statement 200 congratulates the user on a correct answer, while 210 points out that his answer was incorrect and provides him with the proper result. The commas at the end of both PRINT statements here again inhibit a new line from starting, but they space over to the next tab setting, where a new problem is posed as a result of the loop (at 220) back to the top.

```
10 A=RND(1,181)
20 B=RND(1,181)
30 F=RND(1,4)
40 IF F=4 IF A/B<1 A=A*100
50 PRINT "TRY THIS ONE: ";A;
60 GO TO 40+F*30
70 PRINT "+";
80 C=A+B
90 GO TO 180
100 PRINT "-";
110 C=A-B
120 GO TO 180
130 PRINT "*";
140 C=A*B
150 GO TO 180
160 PRINT"/";
170 C=A/B
180 PRINT B;"=";
190 INPUT D
200 IF D=C PRINT "RIGHT!".
210 IF D<>C PRINT "WRONG. CORRECT ANSWER IS ";C,
220 GO TO 10
```

Notice that an END statement is not present here -- contrary to earlier advice. The nature of this program is such that TINY will never go past the last statement. The program as written loops endlessly, and only under these conditions is the omission of an END permissible.

Running this program should give you some practice in learning how TINY divides.

II. Geometric Print Pattern Program

This program is designed to print three identical, trapezoidal patterns across the page, each filled with repeated imprints of the same numeric digit. The user can specify which digit is to fill each trapezoid and, for all three, the number of characters across its top, the slope of its sides (positive or negative) and its height. He can also specify the spacing between the patterns on the page.

Since the printer prints line-by-line, the program prints the pattern in a scanning mode. Every line consists of a sequence of three identical segments, and each segment contains D spaces followed by E identical digits followed by D spaces again. The values of D and E vary from line to line. For each new line, D is decremented by a value I (positive or negative) and E is incremented by 2*I (to keep the pattern symmetrical).

To analyze the program listed below, let us begin by identifying its subroutines. Reading from the bottom up, the subroutine from 250 to 280 prints the digit N, M times across (notice the semicolon). Similarly, the subroutine from 210 to 240 prints a sequence of M spaces. Finally, the subroutine from 140 to 200 prints D spaces followed by E digits (all N) followed again by D spaces. Notice that this subroutine calls the other two.

The main part of the program runs from 10 to 130. First, the program initializes a counter J for the number of lines which have been printed. Then it reads (from the user) initial values for A to E, I and L (the total number of lines to be printed). A,B and C should be single digits. D,E and L must be > 0. Each of the three sequences 30-40, 50-60, and 70-80 prints one segment of a line using the digit specified by the user. 85 starts a new line. 90 and 100 advance D and E as explained earlier, and 110-120 decide whether or not a sufficient number of lines have yet been printed. If not, a new line is started.

GEOMETRIC PRINT PATTERN PROGRAM

```
10 J=0
20 INPUT A,B,C,D,E,I,L
30 N=A
40 GOSUB 140
50 N=B
60 GOSUB 140
70 N=C
80 GOSUB 140
85 PRINT
90 D=D-I
100 E=E+2*I
110 J=J+1
120 IF J<>L GO TO 30
130 END
140 M=D
150 GOSUB 210
160 M=E
170 GOSUB 250
180 M=D
190 GOSUB 210
200 RETURN
210 PRINT " ";
220 M=M-1
230 IF M>0 GOTO 210
240 RETURN
250 PRINT N;
260 M=M-1
270 IF M>0 GOTO 250
280 RETURN
```

For this program to run properly the values of D and E should not become too small. Nor should they be so large as to requ ire excessive line length. The inital values should obey the following relations: $3(E+2D) <$ maximum line width; If $I<0$, $E>2|I|(L-1)$; If $I>0$, $D>I(L-1)$.

THE USR FUNCTION

TINY BASIC includes an important feature to permit you to extend its facilities via machine language subroutines. To use this feature, you must be familiar with many of the intricate details associated with machine language programming. Not only must you know the instruction set for the CPU (See MPM-201, User Manual for the CDP1802 Microprocessor), but you must also be aware of which CPU and memory registers are reserved for TINY, which are freely available for your use and which can act as an interface between your machine-language program and your TINY BASIC program. We assume here that you are familiar with the manual cited above and that you have some introductory machine language programming experience.

The form of the USR construct within a TINY BASIC statement is as follows:

```
USR (expression [,expression][, expression ])
```

where the brackets indicate that either or both of the latter two expressions may be omitted. On encountering this form, TINY evaluates the first expression and transfers control to that address. (Remember that a desired hex address must be converted into its equivalent decimal expression value, and that addresses in the upper half of memory have negative equivalent decimal values.) If a second expression is included, it is evaluated and the resulting value is passed to the called program as the contents of CPU register 8. If a third expression is included, its value is passed in register A (with D also holding RA.0). The subroutine receives control with P=3 and X=2.

Your called program must return with a SEP 5 (D5) instruction. When it returns, its 16-bit function value is the final contents of RA.1 and D (lower 8 bits in D) just before the SEP 5 was executed. This is why USR is called a function. Whenever it is called, it returns a result - a number. Thus, the USR form can appear anywhere in a TINY BASIC statement where a number can normally appear. (Recall our previous discussion of the RND function. Exactly the same idea applies here.)

Thus, in addition to performing some machine-language function (for example, moving a block of data), your USR program will always return a value or result in RA.1 and D. In many cases, this is desirable -- for example, when your subroutine is given two arguments X and Y (in R8 and RA) and returns a number which is, say, the larger of the two. In other cases, however, your USR program will not need to return a value. In that case the value returned must be ignored in the TINY BASIC program which called it. There are several ways to do this. For example, if

```
+0*USR(.......)
```

were included in an expression, then the USR function would be executed but the returned value would be ignored.

For your convenience, TINY itself includes four built-in subroutines which you may want to make use of via the USR mechanism. They are as follows:

(1) USR(20,N)

Returns the decimal value of the byte at memory location N (decimal), where N is the value of the second expression. (Note that this machine language routine begins at location 14 hex.)

(2) USR(24,N,M)

Stores the value of the third expression, M (mod 256) into the byte at location N (decimal), the value of the second expression. Also returns the value M as the function's "value".

Examples: PRINT USR(20,3072) prints the decimal contents of memory location 0C00
A=USR(24,3072,254) loads memory location 0C00 with FE and also loads the"returned value", 254, into A.

(3) USR(6)

Reads one ASCII character from the keyboard and returns its decimal equivalent (including parity bit if any).

(4) USR(9,0,C)

Prints the ASCII character whose code is the right half of the (hex) value of expression C. (Note: The second expression, in this case 0, is ignored. The character to be typed must start out in a D register. Hence, the above format. The third expression is passed in RA with its lower half also in D.) This routine happens to return a "value" 251 in all cases -- which would normally be ignored, as explained earlier.

Examples: PRINT USR(6) will read a character and print its decimal equivalent. On the printer you would see, for example, A65 for a zero parity bit (where A was typed by you).

A=A+0*USR(9,0,66) will print the character B and ignore the returned result (251).

Register Usage and An Example USR Routine:

When you write your own USR routine, you must be careful not to modify the contents of those registers which are used by TINY BASIC. These include CPU registers and memory registers. Appendix B lists how the CPU registers are used by TINY. Machine language subroutines have the free use of

R0,R1,R8,RA,RD and RF.

In addition, R2 is pointing at a free byte on the control stack.

Clearly, the memory areas used by TINY should also not be modified, except with care. TINY uses most of the first page of the available RAM (beginning at 0800) for its own storage. A table of the allocation of this space is given in Appendix C. You probably will not want to bother with any part of this area except for that which includes the A to Z variable cells. These are located at 0882 to 08B5. Note also that, by reducing the address value stored in 0822, you can make space for your added program and data areas in upper memory.

Appendix D lists some key locations at the beginning of the TINY BASIC program itself. (Notice locations 6, 9, 14 and 18 which correspond to the entry points for the built-in subroutines discussed earlier.) TINY BASIC was written as a pure procedure (capable of execution out of ROM) -- not modified in any way as it runs. This area should not be altered except, conceivably, for modifications to the special character codes beginning at location F. This is discussed further later in this manual.

Consider now an example of a USR added routine. Assume we wish to add a logica AND operation to TINY's repertoire. The machine language routine given below will do the job, given that the two arguments are passed in R8 and RA, and that the computed result must be passed back in RA.1 and D.

```
98   GHI   R8
52   STR   R2
9A   GHI   RA
F2   AND
BA   PHI   RA
88   GLO   R8
52   STR   R2
8A   GLO   RA
F2   AND
D5   SEP   R5
```

Given two 16-bit arguments, this routine computes the 16-bit AND of these and returns that result. Note the use of the spare byte pointed to by R2 and the assumption that X=2 on entry Notice also the SEP5 exit. This routine can be stored in any available memory area.

Assuming the above program is stored at location 0C00, then if L=3072, the statement T=USR(L,R,S) will assign to T the 16-bit AND of the values of variables R and S.

ERROR MESSAGES AND PROGRAM DEBUGGING

Error Messages:

Whenever TINY BASIC detects an error in a statement, it generates an error message consisting of an exclamation point followed by a decimal error number. A listing of error numbers and their corresponding meanings is given in Appendix E. If the error is detected during program execution, the error code is followed by the word AT followed by the offending statement's number.

Almost all of the errors detected by TINY are syntax errors. TINY was in the process of interpreting a statement and found it unacceptable for some reason. Only two of the errors in the error list are detected during execution of a statement (i.e., after its syntax has been accepted). These are errors 141 and 243.

Any other error number not listed in the table signifies a memory "full" condition -- probably due to too many nested GOSUB's or an excessively complex expression.

Program Debugging:

Most program execution errors are due to either incorrect flow or improper modification of variable values. To find an error of the first kind, you must determine whether your program is sequencing properly -- whether certain sections of code are indeed executed when expected. Often, the insertion of dummy PRINT statements within suspected code sections will reveal whether the flow within the program is proper.

The second type of error is most easily detected by inserting dummy program stops at key point. This procedure is also useful for diagnosing incorrect flow. A dummy stop is an inserted END, or some other inserted statement which is intentionally erroneous to cause an error stop. Once the stop occurs, you may examine the values of key variables (using the immediate execution mode - e.g., PRINT A,B,C) to see if they indeed have the expected behavior. In some cases, variable values may be corrected, in the immediate mode, while the program is still stopped. In this case, and in the case where the program behavior is proper so far, you will want to resume the program at the point where it last stopped. An immediate or direct GOTO, using the statement number after the stop, will permit the program to proceed as if it had not been interrupted.

APPENDIX A

LOADING AND STARTING TINY BASIC

The hexadecimal listing given below is the TINY BASIC object program (listed in UT4 semicolon format). Initially, you will have to load this file into memory by hand from the keyboard and then verify that it is a faithful copy. While this process is time consuming, it needs to be done only once. After memory is loaded, the contents of the first 2K bytes should be properly recorded on your peripheral file storage medium. Section III of your Evaluation Kit Manual contains instructions for recording a file from memory (using UT4's ?M command) onto a Teletype's paper tape or a TI terminal's magnetic tape cassette. If your terminal is different from either of these, you must develop equivalent procedures to those described in the manual. Once you have correctly recorded a copy of TINY BASIC on paper tape or tape cassette, it should be easily reloadable by preceding the tape read with a !M from the keyboard. This is discussed in the Evaluation Kit Manual.

Once TINY BASIC has been loaded, it may be started at one of two locations:

$P1 is the normal "cold" start. TINY BASIC initializes itself (sizes memory; copies a control block from 000F-001B to 0813-081F; and marks the user program space empty) and then delivers the,: prompt.

$P3 is the "warm" start, which skips the initialization procedure and preserves the state of RAM. It is used as a restart, when there is already a useful program resident in RAM or when certain control parameters have been modified so that they are different from those which were first initialized. If, after a "warm" start, you wish to enter a new program, type the NEW command.

```
0000 0130 B0C0 00ED C006 6FC0 0676 C006 665F;
0010 1882 8020 3022 3020 58D5 0681 08C8 0008;
0020 4838 97BA 48D5 C006 51D3 BFE2 8673 9673;
0030 83A6 93B6 46B3 46A3 9F30 29D3 BFE2 96B3;
0040 86A3 1242 B602 A69F 303B D343 ADF8 08BD;
0050 4DED 304A 0198 01A0 021F 01DD 01F0 01D4;
0060 0481 0249 00ED 044E 0104 05A2 01D3 01D3;
0070 04AA 01D3 01D3 02C5 02D5 0303 0279 0318;
0080 053C 01D3 0429 036C 03CB 03A7 0398 039B;
0090 040E 0460 046D 0581 01B6 0267 0348 034B;
00A0 01D3 01D3 01C9 01C5 024E 0244 0241 01D3;
00B0 F8B3 A3F8 00B3 D3BA F81C AA4A B24A A24A;
00C0 BDF8 00AD 0DBF E212 F0AF FBFF 52F3 EDC6;
00D0 9FF3 FCFF 8F52 3BC6 220A BDF8 23AD 8273;
00E0 9273 2A2A 0A73 8DFB 123A E3F6 C8FF 00F8;
00F0 F2A3 F800 B3D3 B4B5 B7F8 2AA4 F83C A5F8;
0100 4BA7 331A D720 BB4D AB97 5B1B 5BD7 168B;
0110 F4BF D724 9F73 9B7C 0073 D722 B24D A2D7;
0120 2682 7392 73D4 02CC D71E B94D A9E2 49FF;
0130 3033 4BFD D733 85FE FCB0 A6F8 2D22 2273;
0140 9373 97B6 4652 46A6 F0B6 D5FF 103B 6AA6;
0150 FA1F 325C 5289 F473 997C 0038 7373 86F6;
0160 F6F6 F6FA FEFC 54A6 3042 FC08 FA07 B649;
0170 A633 7A89 7399 73D4 0237 D71E 86F4 A996;
0180 2D74 B930 2DFD 0752 D71A ADE2 F4A6 9DB6;
0190 0D52 065D 0256 302D 86FF 20A6 967F 0038;
01A0 96C2 027F B986 A930 2D1B 0BFF 2032 A9FF;
01B0 10C7 FD09 0BD5 D401 C54D AD9A 5D1D 8A5D;
01C0 30C9 D401 C5D4 01C9 BAD7 1A2D FC01 5DAD;
01D0 2D4D AAD5 D401 AAFB 0D32 2D30 A0D4 01AA;
01E0 FF41 3BA0 FF1A 33A0 1B9F FED4 0259 302D;
01F0 D401 AA3B A097 BAAA D402 544B FA0F AA97;
0200 BAF8 0AAF ED1D 8AF4 AA9A 2D74 BA2F 8F3A;
0210 059A 5D1D 8A73 D401 AAC3 01FB C001 2D9B;
0220 BA8B AAD4 01AA 1B52 49F3 3223 FB80 321C;
0230 9ABB 8AAB C001 A0D7 2482 F52D 9275 337F;
0240 D549 3059 49BA 4930 55D4 0525 3055 D401;
0250 C5D4 0254 8AD4 0259 9A52 D719 F733 7FF8;
0260 01F5 5DAD 025D D5D4 01C9 AD4D BA4D 3055;
0270 FB2F 3266 FB22 D402 F44B FB0D 3A70 29D7;
0280 18B8 D402 CCF8 21D4 02F4 D71E 89F7 AA99;
0290 2D77 BAD4 0315 9832 A9F8 BDA9 93B9 D402;
02A0 C5D7 28BA 4DAA D403 15F8 07D4 0009 D402;
02B0 D5D7 1A97 5DD7 26B2 4DA2 C001 2820 4154;
02C0 20A3 D402 F249 FC80 3BC2 30F2 D719 F880;
02D0 7397 7373 C8D7 1BFE 3366 D715 AAF8 0DD4;
02E0 0009 D71A 8AFE 32EF 2A97 C7F8 FF30 DF73;
02F0 F88A FF80 BFD7 1B2D FC81 FC80 3B66 5D9F;
0300 C000 09D7 1BFA 07FD 08AA 8A32 97F8 20D4;
0310 02F4 2A30 0AD4 0254 D71A ADD4 0413 3B25;
0320 F82D D402 F497 73BA F80A D402 551D D403;
0330 E38A F6F9 3073 1D4D EDF1 2D2D 3A2E 1202;
0340 C201 C2D4 02F4 303E D72E 389B FB08 3A5E;
0350 8B52 F0FF 8033 5ED7 2E8B 739B 5DD5 D72E;
0360 B80D A88B 739B 5D98 BB88 ABD5 D401 C59A;
0370 FB80 738A 73D4 01C9 AFD4 01C5 128A F7AA;
0380 129A FB80 7752 3B92 8AF1 328F 8FF6 388F;
0390 F638 8FF6 C7C4 19D5 D404 0ED4 01C5 ED1D;
03A0 8AF4 739A 745D D5D4 01C5 F810 AF4D B80D;
03B0 A80D FE5D 2D0D 7E5D D404 223B C5ED 1D88;
03C0 F473 9874 5D2F 8F1D 3AB1 D5D4 01C5 9A52;
03D0 8AF1 C202 7F0D F373 D404 132D 2DD4 0413;
03E0 1D97 C897 73AA BAF8 11AF ED8A F752 2D9A;
03F0 773B F6BA 02AA 1D1D 1DF0 7E73 F07E 738A;
```

2 K

TINY

BASIC

Cold start $P1

Warm start $P3

```
0400 7ED4 0424 2F8F CA03 EA12 02FE 3B21 D71A;
0410 AD30 18ED F0FE 3B21 1D97 F773 9777 5DFF;
0420 00D5 8AFE AA9A 7EBA D5D7 18C2 02B1 4BFB;
0430 0D3A 2ED4 0598 324B D400 0C33 46D7 1CB9;
0440 4DA9 D717 5DD5 D71E B94D A9C0 027F D720;
0450 BB4D ABD4 0598 324B D71C 8973 995D 3042;
0460 D404 FE32 38D7 288A 739A 5D30 4BD4 048B;
0470 42BA 02AA D726 8273 9273 D405 013A 6530;
0480 88D4 048B 42B9 02A9 C001 2DD7 2212 1282;
0490 FC02 F32D 3A9C 927C 00F3 324B 12D5 D716;
04A0 3897 FED7 1A97 765D 30B2 F830 ABD4 0254;
04B0 9DBB D400 06FA 7F32 B252 FB7F 32B2 FB75;
04C0 329E FB19 32A1 D713 02F3 32D7 2D02 F33A;
04D0 DD2B 8BFF 3033 B2F8 30AB F80D 3802 5BD7;
04E0 198B F73B ECF8 07D4 02F4 0B38 4BFB 0D3A;
04F0 B2D4 02D5 D718 8B5D F830 ABC0 01C5 D401;
0500 C58A 529A F1C2 027F D720 BB4D ABD4 0598;
0510 C68D D5ED 8AF5 529A 2D75 E2F1 3312 4BFB;
0520 0D3A 1E30 0DD4 0528 D401 C54D B84D A84D;
0530 B64D A68D 52D7 1902 5DAD 8AD5 D72C 8B73;
0540 9B5D D404 FED7 2A8B 739B 73D4 04FE 2B2B;
0550 D72A 8BF7 2D9B 7733 7B4B BA4B AA3A 629A;
0560 327B D403 15F8 2DFB 0DD4 02F4 D400 0C33;
0570 7B4B FB0D 3A67 D402 D530 50D7 2CBB 4DAB;
0580 D5D7 2682 7392 5DD7 182D CED7 28AA 4D12;
0590 12E2 738A 73C0 012D D727 4B5D 1D4B 73F1;
05A0 1DD5 D403 5ED4 04FE FCFF 97AF 33BA 9BBD;
05B0 8BAD 2F2F 2F4D FB0D 3AB4 2B2B D403 5ED7;
05C0 280B FB0D 735D 32D9 9A5D 1D8A 5D9B BA8B;
05D0 AA1F 1F1F 4AFB 0D3A D3D7 2EBA 4DAA D724;
05E0 8AF7 AA2D 9A77 BA1D 8FF4 BF8F FA80 CEF8;
05F0 FF2D 74E2 73B8 9F73 5282 F598 5292 75C3;
0600 027E 8F32 3052 FE3B 1ED7 2EBF 4DAF E2F7;
0610 A89F 7C00 B848 5F1F 1A9A 3A15 3030 9FAF;
0620 98BF D724 B84D A82A EF08 2873 1A9A 3A29;
0630 D724 1242 7302 5DD7 2EBA 4DAA D728 AFF1;
0640 324E 8F5A 1A4D 5A1A 4B5A FB0D 3A47 C002;
0650 B573 5297 BA2D 43D5 5D2D 88FA 0FF9 605D;
0660 FA08 CEC4 12DD FC00 376E FF00 3F6C D5D7;
0670 118D 73C0 8140 D712 327E DC17 2D5D C081;
0680 A424 3A91 2710 E159 C32A 562C 8A47 4F54;
0690 CF30 D010 11EB 6C8C 474F 5355 C230 D010;
06A0 11E0 1416 8B4C 45D4 A080 BD30 D0E0 131D;
06B0 8C50 D283 494E D4E1 6285 BA38 5338 5583;
06C0 A221 6330 D020 83AC 2262 84BB E167 4A83;
06D0 DE24 93E0 231D 9149 C630 D031 1F30 D084;
06E0 5448 45CE 1C1D 380B 9B49 CE83 5055 D4A0;
06F0 10E7 243F 2091 27E1 5981 AC30 D013 1182;
0700 AC4D E01D 8A52 45D4 8355 52CE E015 1D85;
0710 454E C4E0 2D87 5255 CE10 1138 0A84 4E45;
0720 D72B 9F4C 4953 D4E7 0A00 010A 7FFF 6530;
0730 D030 CBE0 2400 0000 0000 000A 801F 2493;
0740 231D 8452 45CD 1DA0 80BD 382A 82AC 620B;
0750 2F85 AD30 E617 6481 AB30 E685 AB30 E618;
0760 5A93 AD30 E619 5430 F585 AA30 F51A 5A85;
0770 AF30 F51B 542F 8852 4E44 A831 1539 448E;
0780 5553 52A8 30D0 30CB 30CB 311C 2E2F A212;
0790 2FC1 2F80 A865 30D0 0B80 AC30 D080 A92F;
07A0 84BD 0902 2F83 3CBE 7485 3CBD 0903 2F84;
07B0 BC09 012F 853E BD09 062F 853E BC09 052F;
07C0 80BE 0904 2F19 170A 0001 1809 8009 8012;
07D0 0A09 291A 0A1A 8518 0813 0980 1203 0102;
07E0 316A 3175 1B1A 1931 7518 2F0B 0105 0104;
07F0 0B01 0701 062F 0B09 060A 0000 1C17 2F00
```

◆

APPENDIX B

REGISTER ALLOCATIONS

Registers R0 and R1 are not used by TINY BASIC in any way. In addition, the program makes no reference to Q or EF1,2,3 or 4. All character I/O is funnelled through a vector near the beginning of the program. The user may request the performance of INP or OUT instructions as part of the BASIC program, but these are up to the user's discretion.

The other registers used by TINY are as follows:

2	Control stack pointer.
3	Inner interpreter Program Counter.
4	Call linkage PC.
5	Return linkage PC.
6	Top of control stack; =address of caller. Also holds branch address.
7	Byte Fetch PC.
8	Temporary work register. Receives second argument in USR call
9	Outer interpreter Program Counter. =address of next IL opcode.
A	16-bit accumulator and work register. Contains third argument of USR calls, and part of response from USR calls.
B	BASIC Pointer. Points to next token.
C	Timing subroutine in Terminal I/O.
D	Workspace memory pointer. =Expression Stack Pointer in USR calls.
E	Subroutine linkage temporary and Terminal timing constant.
F	Temporary work register.

Machine language subroutines called via the USR function have the free use of R0,R1,R8,RA,RD,RF.

APPENDIX C

USE OF FIRST PAGE OF USER RAM BY TINY BASIC

0812	UT3/UT4 output delay flag
0813	Copy of BACKSPACE code
0814	Copy of CANCEL code
0815	Copy of Pad code
0816	Copy of Tape Mode Enable
0817	Copy of Spare stack Space
0818	Execution mode flag
0819	End of input line
081A	Expression Stack pointer
081B	Output Control
081C-081D	Saved address for NX
081E-081F	Copy of IL base address
0820-0821	Lowest address of user program space
0822-0823	Highest address of user program space
0824-0825	End of user program + stack reserve
0826-0827	Top of GOSUB stack
0828-0829	Current Line number in BASIC
082A-082D	Temporary
082E-082F	Input line pointer
0830-087F	Input line, buffer and expression computation stack
0880-0881	Random Number Generator seed
0882-08B5	BASIC variables A-Z

Note: Each variable occupies two bytes beginning page which is twice its ASCII code.

Displacement	Variable
0082	A
0084	B
:	
00B4	Z

APPENDIX D

ALLOCATIONS IN LOW RAM

0001	Cold Start
0003	Warm Start
0006-0008	LBR to character input
0009-000B	LBR to character output
000C-000E	LBR to Break test
000F	Backspace code
0010	Line Cancel code
0011	Pad character
0012	Tape Mode enable flag (hex 80=enabled)
0013	Space stack size
0014	Byte fetch subroutine
0016	Double byte fetch entry vector
0018	Byte store Subroutine
001A-001B	Address of IL
001C-001D	User space start for scan
001E	Page for memory wrap test
001F	Page for workspace
0120	Entry vector for Hex input
0123	Entry vector for Hex print
0126	Entry vector for I/O
0129	Entry vector for AND
0800	Beginning of user RAM space

APPENDIX E

ERROR MESSAGE SUMMARY

0	Break during execution
8	Memory overflow; line not inserted
9	Line number 0 not allowed
11	RUN with no program in memory
33	Improper syntax in GOTO
35	No line to GO TO
40	LET is missing a variable name
42	LET is missing an =
45	Improper syntax in LET
47	LET is not followed by END
65	Missing close quote in PRINT string
83	Circumflex in PRINT is not at end of statement
85	PRINT not followed by END
101	IF not followed by END
111	INPUT syntax bad - expects variable name
130	INPUT syntax bad - expects comma
131	INPUT not followed by END
140	RETURN syntax bad
141	RETURN has no matching GOSUB
142	GOSUB not followed by END
147	END syntax bad
179	LIST syntax error - expects comma
189	Can't LIST line number 0
193	LIST not followed by END
198	REM not followed by END
199	Missing statement type keyword
201	Misspelled statement type keyword
243	Divide by zero
276	Syntax error in Expression - expects value
281	RND expects two arguments
286	Missing right parenthesis
321	IF expects relation operator
356	Invalid arguments in RND

All other error numbers signify memory overflow (too many nested GOSUBS) or an excessively complex expression.

APPENDIX F

SPECIAL KEYBOARD CONTROL CHARACTERS

You may erase (backspace over) an incorrectly-entered character by hitting the "erase previous character" key. Its hex code is stored in location 000F, and it is presently an ASCII Left-arrow or Underline (Shift 0; hex 5F). Each occurrence of __ erases the last stored input character. Thus,

POINT _ _ _ _ RINT

corrects the erroneous second character. Similarly, you may erase the entire input line and start over by hitting the "cancel line" character. Its hex code is stored in location 0010, and it is presently an ASCII CANCEL (Control X; hex 18). You may change either of these edit control characters by changing its stored code to any value except DC3, LF, NULL or DELETE (hex codes 13, 0A, 00 and FF, respectively). These special characters are trapped by TINY before its line edit code is entered.

The BREAK key may be used for two purposes: to interrupt a long LISTing or to interrupt the execution of a program (for example, one caught in an endless loop). While executing the LIST command, TINY checks BREAK at the beginning of every typed line. While executing a stored program, TINY checks BREAK between statements.

Each of your input lines from the keyboard is terminated with a carriage return (CR). Whenever TINY generates a new line (for example, when it echoes your CR), it generates CR PAD PAD LF PAD, where the pad character depends on the 2^7 bit of location 0011 (hex). If 0, it is the NULL character (hex 00). If 1, it is the RUBOUT/DELETE character (hex FF). The rest of the byte in location 0011 defines the count of the number of pads to be sent between each CR and LF. It is presently set to 2.

SUMMARY OF KEY CHARACTERS

CR	Terminates every entry line.
__	Backspace.
CAN	Cancel line.
BREAK	Interrupt long printout or execution.

Appendix G

Tape Control Characters

Whenever TINY generates the ? prompt character (during execution of an INPUT statement), it follows this by generating the XON (ASCII DC1) control character. If the input comes from tape, the user may elect to use this special control character to activate the tape reader.

Similarly, TINY generates the XOFF (ASCII DC3; hex 13; Control S) control character whenever an error stop or NEW or END occurs - under the assumption that the user may want to deactivate the reader with this character.

These control characters may be ignored if the user has found an alternative method for tape I/O.

RCA
Solid State
Division

Memory/Microprocessor Products
Application Note
ICAN-6991

A Slave CDP1802 Serial Printer Buffer System

by K. Nagy

This Note describes a CDP1802-based stand-alone line-printer buffer that links a master processor system to a serial printer through an RS-232C interface. The main buffer board consists of a CDP1802 Microprocessor (configured as a peripheral controller), a CDP1854A UART with baud-rate generation devices (configured in industry mode 0 and able to handle separate receive and transmit baud rates), and a CDP18U42 EPROM (to store a minimal user program). With the addition of RCA Microboards for system RAM (CDP18S620, CDP18S621, CDP18S622, CDP18S623, CDP18S624, or CDP18S625 in various configurations from 4K to 16K), a buffer system with a printer character storage capacity of up to 32K bytes can be implemented.

The line buffer is especially useful with interactive computer systems; it frees high-speed terminals for other tasks while a slower printer (connected in parallel to the terminal through a serial port, such as is used with RCA Development Systems) prints from buffer memory. The buffer circuitry also illustrates how a CDP1800 processor can be configured as a slave controller that communicates with a master system through a serial port. In this configuration, some of the special I/O features of CDP1800 architecture are highlighted; these features include DMA control for high-speed data transfer, I/O instructions for communication with peripheral chips such as the CDP1854A UART, and the availability of several input flag lines for event polling.

The low power consumption of the system makes it ideal for operation from a storage battery, which provides portability of user data, and also protects data integrity should a line power failure occur.

System Modes

The line buffer operates in the following modes:

1. Receive data—The print buffer is loaded at some (usually high) baud rate (through a serial interface under CDP1802 DMA control).
2. Transmit data—Data is transmitted, usually at a low baud rate (through a serial interface under CDP1802 programmed I/O control), to the printer when the printer is selected and ready.
3. Instant replay—Data is retransmitted to the printer upon request.

These modes permit the system to accommodate a wide range of input and output conditions, and to communicate with many different peripheral devices.

System Set Up

The line-buffer system input and output is connected to suitable sending and receiving units equipped with RS-232C interfaces by means of cables and connectors. The system output contains a feedback (handshake) line that permits the printer to operate at its optimum speed; the feedback feature can be eliminated if necessary through software changes.

The printer-buffer prototype was evaluated using a CDP18S007 CDS Development System, an ADM-3A CRT Terminal, and an EPSON MX-80 Printer. However, the universal nature of the buffer design permits it to be used with a wide variety of master system and printer combinations.

Hardware

A block diagram of the system is shown in Fig. 1; detailed system interconnection diagrams are shown in Appendix A. The "U" designators used in the following text refer to the figures in Appendix A, and are identified in Table I and in the Appendix. Table II summarizes register assignments.

Table I — List of IC's Used in System

IC	Identity
U1	CDP1802 CPU
U2	CDP18U42 EPROM
U3	CDP1854A UART
U4	CD4013 D FF
U5, U6	CD4069 Hex Inverter
U7	CD4093 Quad 2-Input NAND
U8	CD4013 D FF
U9, U10, U11	CD40161 Sync Binary Counter
U12	MC1489 Quad Line Receiver
U13	MC1488 Quad Line Driver

Table II — Line-Buffer Register Use

R0	Initial Program Counter/DMA-IN Pointer
R3	Program Counter
R4	Printer Pointer
R5	End of Memory Pointer
R6	XOR Temporary Location Pointer
R7	Temporary DMA-IN Pointer
R8	Cold Start Flag

The system program resides in the CDP18U42, 256-byte UV Erasable PROM, U2, located in the lower 32K address space on the system map. The chip-select signal for the EPROM is generated by latching the high-order address byte of the MA7 signal by means of a CD4013 flip-flop (U4). The EPROM is selected when MA.1 is low ($\overline{CS1}$), $\overline{MRD}$ is low ($\overline{CS3}$), and $\overline{CLR}$ is high (CS2).

Printed in USA/8-81

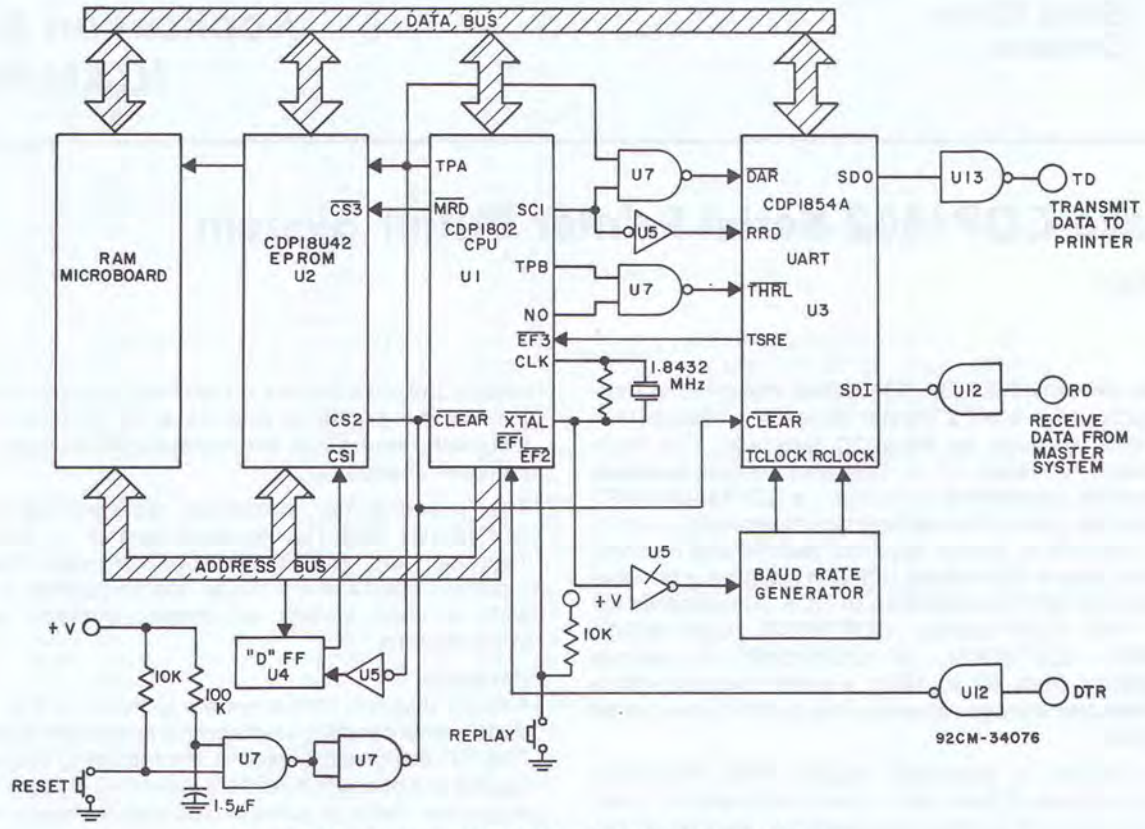


Fig. 1 – Block diagram of the serial printer buffer system.

The internal oscillator of the CDP1802 microprocessor is driven by a 1.8432-MHz external crystal, which acts as the system master clock. The crystal is connected between the CLOCK and $\overline{XTAL}$ terminals of the microprocessor. One inverter of the CD4069 (U5) provides a buffered signal called CLK OUT to the baud-rate generator divider chain for the UART.

Part of a CD4093 (U7) forms a power-on reset circuit that outputs a $\overline{CLEAR}$ signal to the microprocessor and the UART. An external reset signal can force the processor to restart program execution. An SPST switch connected to the $\overline{EF2}$ flag-input terminal of the microprocessor provides the instant-replay request signal for the program. If this switch is in the replay mode, activation of the reset button will start the printing of the previously deposited contents of the RAM buffer. This feature relieves the host computer of the time-consuming task of producing copies on the printer.

A CDP4013, Dual D Flip-Flop (U8), forms a synchronous divide-by-three circuit; its output is connected to two CD40161B cascaded synchronous binary counters (U9 and U10). The Q outputs of U9 and U10 provide baud rates from 150 to 19,200 baud. The accuracy of these baud rates is comparable to that of the crystal oscillator. Another CD40161B synchronous binary counter (U11) is used in a divide by 11 configuration to generate the 110 baud used by some teletypes and other slow mechanical printers. Because it is possible to input to, or output from, this system at varying baud rates, the system is very useful in interactive applications or where baud-rate exchange is required.

The CDP1854A UART (U3) has two modes of operation. Mode 1 is directly compatible with the CDP1800 family of microprocessors without additional interface circuitry; software techniques are used for programming in this mode.[1] In Mode 0, the mode used in the serial printer buffer system, the CDP1854A is compatible with a great many other UART's, such as the TR1602A by Western Digital, and provides the user with hardware-option selection in the form of five independent switches. The functions of the switches are as follows:

SW5 - When open, the generation of parity is inhibited.

SW6 - When open, two stop bits are selected, when closed, one is selected. Selection of two stop bits with five data bits programmed selects 1.5 stop bits.

SW7, SW8 - These two switches select the character length (exclusive of parity) of five to eight data bits.

SW9 - This switch is closed for odd parity, opened for even parity.

Fig. 2 shows serial-word format-programming data. The UART has two independent byte-wide buses. Both receive and transmit buses are connected to the system data bus.

The system receive operation is initiated when a serial bit stream is sent via the RS-232 receiver interface to the UART. When the UART receiver assembles a full received character, the data available (DA) output goes high and initiates a DMA-IN cycle. During DMA, the CPU is forced into a DMA cycle (S2), which causes SC1 to go high; the result is a transfer of data from the UART receiver holding register to the data bus. The address and control signals needed to direct the flow of data into the RAM pointed to by DMA pointer R0 are generated during DMA. Additionally, hardware interconnections are made that cause the data available reset (DAR) flag to be reset. Reset is accomplished through a signal to the data available reset (DAR) input; the signal terminates the DMA-IN request before it is again sampled by the CPU. Finally, R0 is incremented at the end of the S2 cycle, and the system is ready for transfer of another byte of data when it is received.

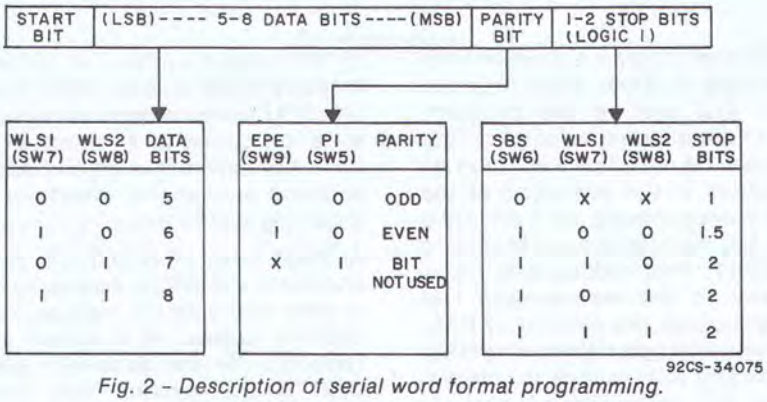


Fig. 2 - Description of serial word format programming.

The system transmit operation begins when the UART transmitter shift register is empty (TSRE high, polled via $\overline{EF3}$) and the printer is selected (polled via $\overline{EF1}$). The CPU issues an I/O command that signals the transmitter holding register load ($\overline{THRL}$) input to transfer data from the data bus to the transmitter holding register. The data is serialized by the transmitter shift register and output, in the format selected by the user, through the serial data out (SDO) line and the RS-232 line driver to the printer. During the time that data is actively being transmitted by the UART, the TSRE signal will be low, preventing transmission of additional data. When the TSRE signal becomes high, and the printer is ready, a character can be transferred from the system data bus to the transmitter holding register. The microprocessor then outputs a low pulse to the UART transmitter holding register load ($\overline{THRL}$) input, causing TSRE to go low. When the TSRE output signal goes high again, and $\overline{EF1}$ is low (indicating that the printer is ready), another character can be loaded into the transmitter holding register for transmission. This process is repeated until all of the line-buffer memory contents are transmitted.

Baud-Rate Generation

The CDP1854A UART requires a clock signal that is 16 times the desired bit rate for proper operation. This 16X clock rate is applied to the UART receive clock (RCLOCK) and transmitter clock (TCLOCK) inputs. In the subject system, the RCLOCK and TCLOCK inputs are connected to separate frequencies (through SW 3 and SW 4). Both of these bit rates are derived from the same crystal oscillator and divider circuitry.

The bit rate and the number of bits per character determine the number of characters that can be transmitted in one second. If the UART receiver is required to operate at a data rate of 19,200 bits/s, then the receive clock (RCLOCK) frequency must be 16 x 19,200 = 307,200 Hz. Consequently, if the data transmission rate must be 300 bits/s, then the TCLOCK input of the UART must be connected to a clock frequency of 16 x 300 = 4800 Hz. Table III shows baud rates and frequencies supported by the system.

Software

The program flowchart is shown in Fig. 3. Upon power-on,

Table III — Baud Rates and Frequencies Supported by System

Baud Rate	16X Freq. (kHz)	Time (μs)
110	1.760	568.18
150	2.400	416.67
300	4.800	208.33
600	9.600	104.17
1200	19.200	52.08
2400	38.400	26.04
4800	76.800	13.02
9600	153.600	6.51
19200	307.200	3.26

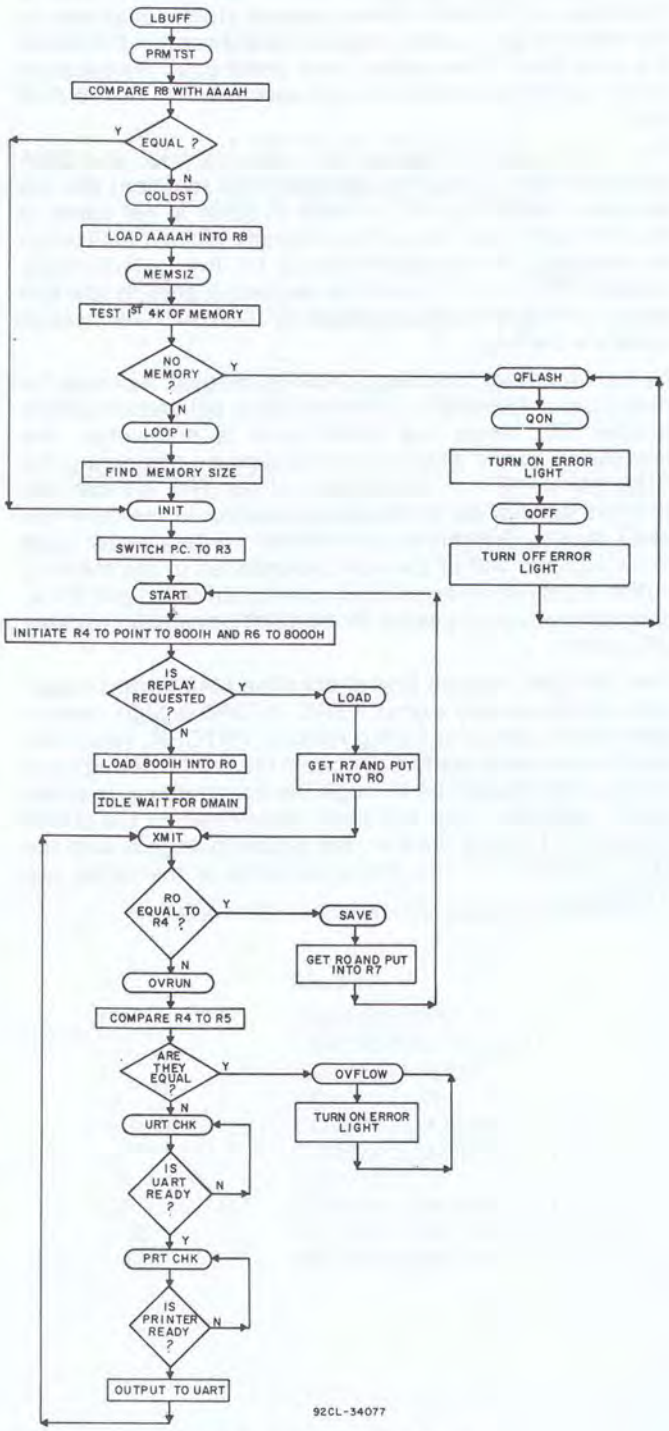


Fig. 3 - Program flowchart.

the power-on reset circuit initiates program execution from the first ROM location (located at 0000). After program execution has begun, the first part of the program, PRMTST, tests register R8 to determine if a "cold" or first start is being initiated. If the start is not a first start, then R8 contains AAAAH, which results in the execution of the routine INIT. If a cold start is encountered, R8.1 and R8.0 will contain random values, and the program will branch to the cold-start routine COLDST. This routine sets R8 to AAAAH, and passes control to the memory-size test routine, MEMSIZ, which determines the amount of RAM available in the system for line-buffer use. If there is no RAM connected to the system, the QFLASH routine is entered, and the error LED flashes on and off until the condition is corrected and the reset button pressed. Upon completion of the memory-size routine, register R5 will contain the size of the user RAM. The system then undergoes initialization under software control through execution of the routine INIT.

The INIT routine initializes the printer pointer and DMA pointer to 8001H (the first available RAM location) and the program counter to R3. A byte of RAM is set aside at location 8000H for use by the program. When initialization is complete, the program checks for the instant-replay request ($\overline{EF2}$ low); if it finds no request, it goes to idle and waits for the first byte received by the UART receiver to initiate a DMA-IN.

As the processor receives a DMA-IN request, it places the byte, now on the data bus, in the location pointed to by DMA pointer R0. When the DMA cycle is completed, the processing of the XMIT routine begins by comparing the DMA pointer (R0) to the printer pointer (R4). If these two pointers are not set to the same location in memory, the XMIT routine determines whether the printer pointer is set to an address within the valid boundaries of the memory buffer. If it is not, an error is indicated by an error light; if it is, program control is passed to the UART checking routine, URTCHK.

The URTCHK routine first checks the UART transmitter-shift-register-empty signal, TSRE. If TSRE is high, control goes to the printer checking routine, PRTCHK. When this routine receives a ready signal from the printer, it outputs a character to the printer through the transmitter side of the UART. After the byte has been transferred to the UART transmitter holding register, the system proceeds with the XMIT routine until the entire contents of the buffer are printed out.

In the subject system, all incoming data is deposited in memory in real time by DMA-IN within an execution time of one CPU machine cycle per byte. This method is similar but superior to that of an interrupt driven system because it does not have the overhead associated with the interrupt software routine and, therefore, can easily cope with high incoming baud rates.

At baud rates of 19,200 bits per second and 10 bits per character, the system has approximately 520 microseconds of time available for processing between two successive DMA-IN pulses. At a system clock rate of 1.8432 MHz (selected for the baud-rate generation circuits for the UART), the system has enough time to execute approximately 120 machine cycles before the next DMA-IN cycle comes in.

The software assembly listing in ASM 4 is shown in Appendix B.

Summary

In summary, this system is especially useful in applications requiring interaction with a variety of types of equipment as it is capable of taking input or providing output at varying baud rates. The instant-replay feature relieves a host computer of the time consuming task of producing copies on a printer. The system UART, when used in mode 0, constitutes a peripheral device that makes interfacing of the line-buffer system with other systems a simple matter. The low power consumption of the line-buffer system makes it an ideal one for operation from a storage battery, which provides portability of user data and protection of this data in the event of a line-power failure.

References and Bibliography

1. "Use of the CDP1854 UART with RCA Microprocessor Evaluation Kit CDP18S020 or EK/Assembler-Editor Design Kit CDP18S034," R.G. Ott, RCA Solid State Application Note ICAN-6632.
2. "COS/MOS Memories, Microprocessors, and Support Systems," RCA Solid State Databook SSD-260.
3. "COS/MOS Integrated Circuits," RCA Solid State Databook SSD-250.
4. "COS/MOS Integrated Circuits Manual," RCA Solid State publication CMS-272.
5. "User Manual for the CDP1802 COSMAC Microprocessor," RCA Solid State publication MPM-201.

Appendix A

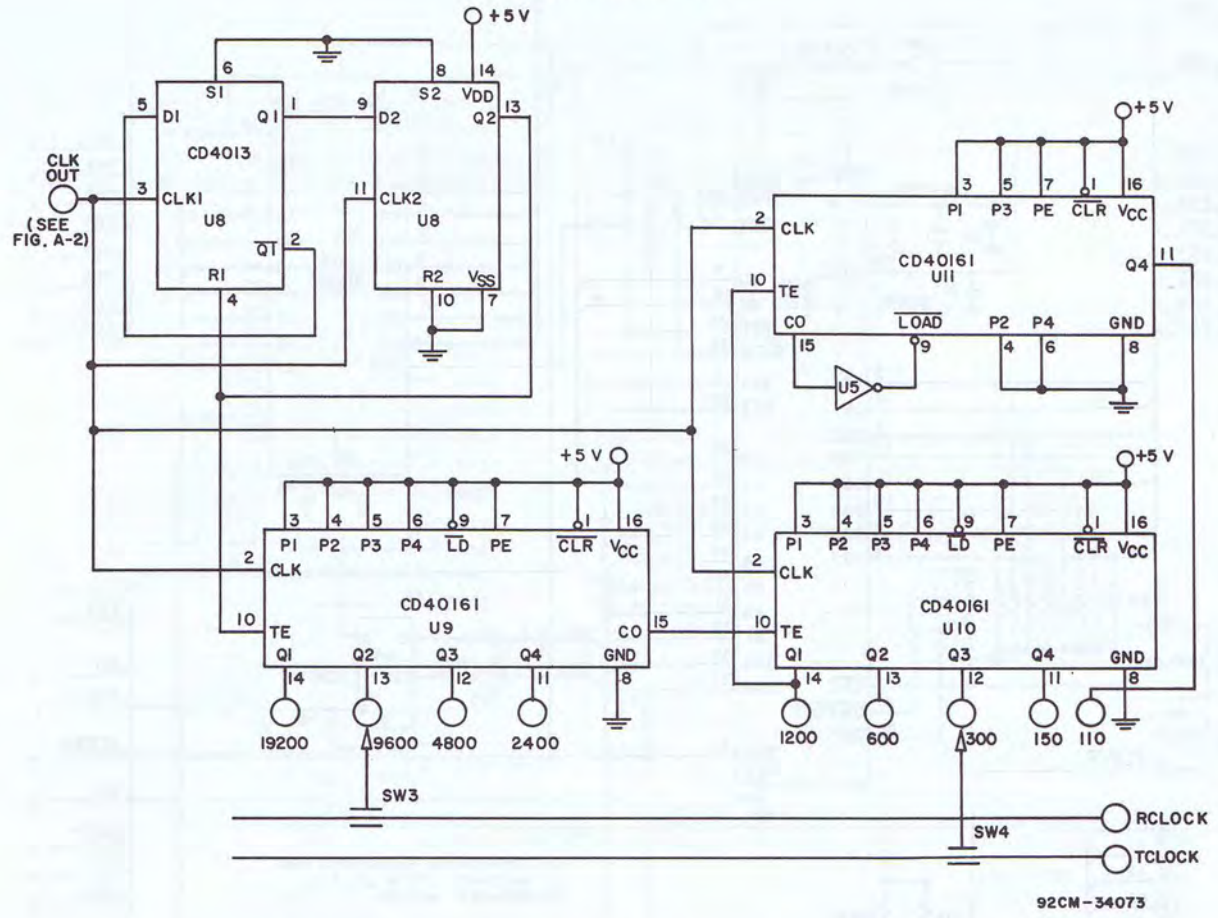


Fig. A-1 – Interconnection diagram for line-buffer baud-rate generator.

Table A-I — Microboard Computer Bus Interface (Fig. A-2)

Pin	Signal	Pin	Signal
A	TPA-P	1	DMA1-N
B	TPB-P	2	DMA0-N
C	DB0-P	3	RNU-P
D	DB1-P	4	INT-N
E	DB2-P	5	MRD-N
F	DB3-P	6	Q-P
H	DB4-P	7	SC0-P
J	DB5-P	8	SC1-P
K	DB6-P	9	CLEAR-N
L	DB7-P	10	WAIT-N
M	A0-P	11	−5 V/−15 V
N	A1-P	12	SPARE
P	A2-P	13	CLOCK OUT
R	A3-P	14	N0-P
S	A4-P	15	N1-P
T	A5-P	16	N2-P
U	A6-P	17	EF1-N
V	A7-P	18	EF2-N
W	MRW-N	19	EF3-N
X	EF4-N	20	+12 V/+15 V
Y	+5 V	21	+5 V
Z	GND	22	GND

Table A-II — List of IC's Used in System

IC	Identity
U1	CDP1802 CPU
U2	CDP18U42 EPROM
U3	CDP1854A UART
U4	CD4013 D FF
U5, U6	CD4069 Hex Inverter
U7	CD4093 Quad 2-Input NAND
U8	CD4013 D FF
U9, U10, U11	CD40161 Sync Binary Counter
U12	MC1489 Quad Line Receiver
U13	MC1488 Quad Line Driver

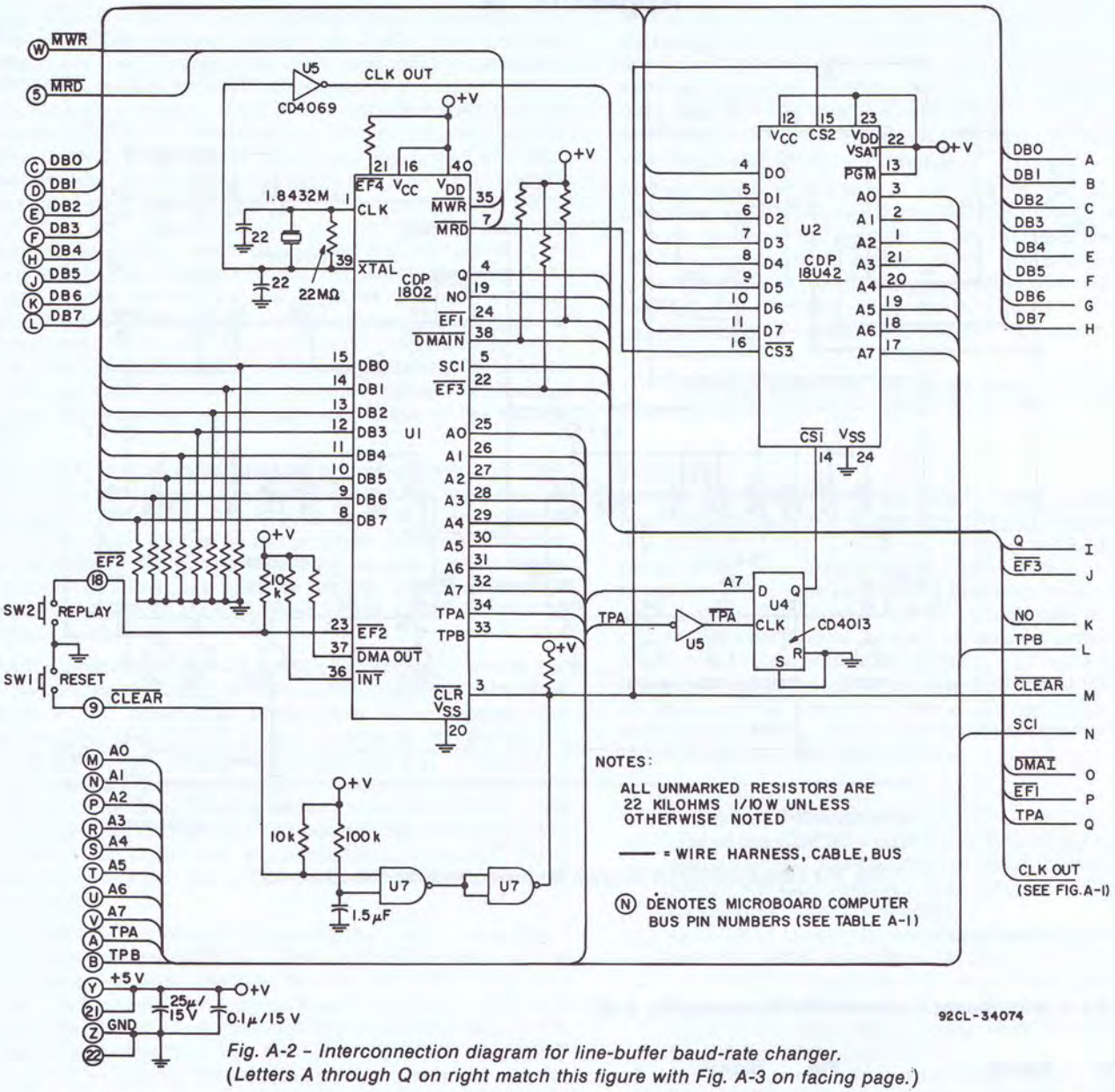


Fig. A-2 – Interconnection diagram for line-buffer baud-rate changer.
(Letters A through Q on right match this figure with Fig. A-3 on facing page.)

Appendix B — Program Listing

```
0000 ;          0001 ..*****************************************
0000 ;          0002 ..*                                       *
0000 ;          0003 ..* * *  LBUFF  3-15-81   K. NAGY   * * *
0000 ;          0004 ..*                                       *
0000 ;          0005 ..*****************************************
0000 ;          0006 ..
0000 ;          0007 ..
0000 ;          0008          ORG #0000
0000 F880;      0009 PRMTST:  LDI #80       ..CHECK FOR COLD START
0002 B5;        0010          PHI R5
0003 F800;      0011          LDI #00
0005 A5;        0012          PLO R5
0006 E5;        0013          SEX R5
0007 98;        0014          GHI R8
0008 55;        0015          STR R5
0009 F8AA;      0016          LDI #AA
000B F5;        0017          SD
000C 3A89;      0018          BNZ COLDST
000E 88;        0019          GLO R8
000F 55;        0020          STR R5
0010 F8AA;      0021          LDI #AA
0012 F5;        0022          SD
0013 3A89;      0023          BNZ COLDST
0015 3044;      0024          BR  INIT
0017 F88F;      0025 MEMSIZ:  LDI #8F       ..CHECK FOR MEMORY SIZE
```

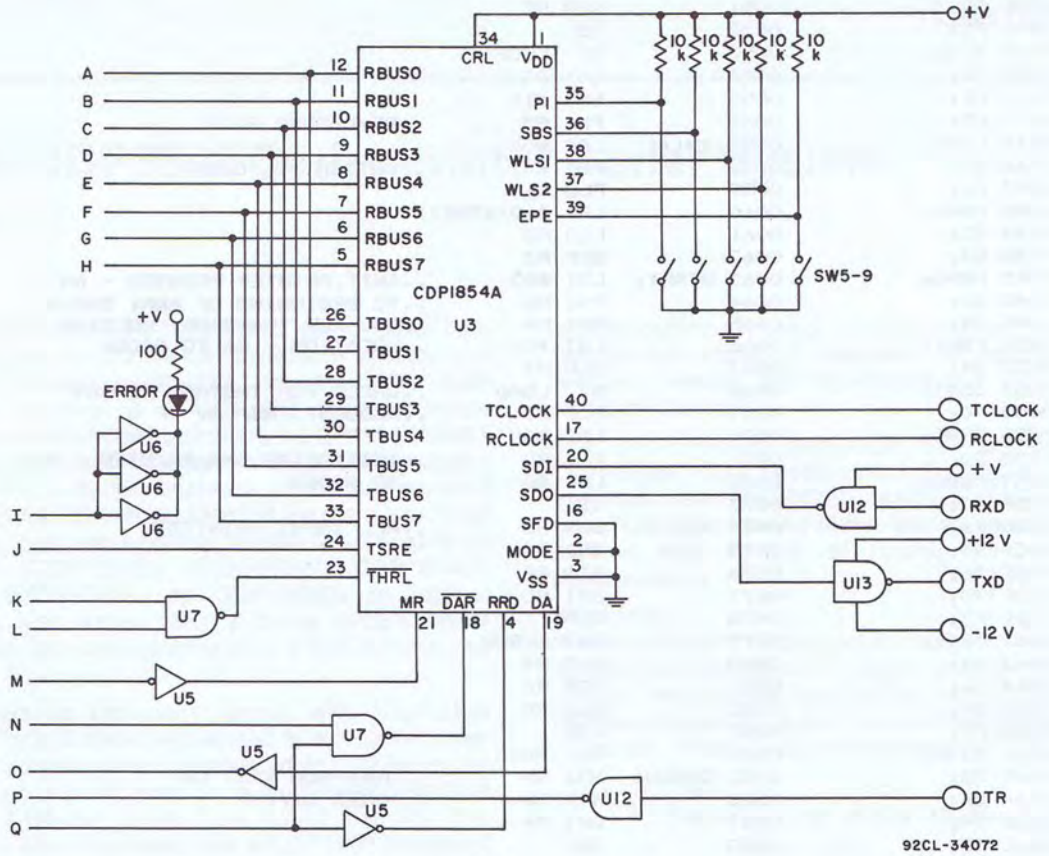


Fig. A-3 – Interconnection diagram for line-buffer receiver/transmitter.
(Letters A through Q on left match this figure with Fig. A-2 on facing page.)

Appendix B (Cont'd)

```
0019 B5;        0026          PHI R5      ..IN THE SYSTEM MIN. 4K.
001A F8FF;      0027          LDI #FF     ..MAX. 32K.
001C A5;        0028          PLO R5
001D E5;        0029          SEX R5
001E F8AA;      0030          LDI #AA
0020 55;        0031          STR R5
0021 F5;        0032          SD
0022 3236;      0033          BZ  LOOP1
0024 7B;        0034 QFLASH:  SEQ         ..IF SYSTEM MEMORY IS
0025 F820;      0035          LDI #20     ..LESS THAN 4K FLASH
0027 B5;        0036          PHI R5      ..ERROR LITE
0028 25;        0037 QON:     DEC R5
0029 95;        0038          GHI R5
002A 3A28;      0039          BNZ QON
002C 7A;        0040          REQ
002D F820;      0041          LDI #20
002F B5;        0042          PHI R5
0030 25;        0043 QOFF:    DEC R5
0031 95;        0044          GHI R5
0032 3A30;      0045          BNZ QOFF
0034 3024;      0046          BR  QFLASH
0036 95;        0047 LOOP1:   GHI R5
0037 FC10;      0048          ADI #10
0039 B5;        0049          PHI R5
003A F8AA;      0050          LDI #AA
```

Appendix B (Cont'd)

```
003C 55;          0051          STR R5
003D F5;          0052          SD
003E 3236;        0053          BZ  LOOP1
0040 95;          0054          GHI R5
0041 FF10;        0055          SMI #10
0043 B5;          0056          PHI R5        ..R5=MEMORY SIZE
0044 F800;        0057 INIT:    LDI #00
0046 B3;          0058          PHI R3        ..SWITCH PC TO R3
0047 A6;          0059          PLO R6
0048 F84C;        0060          LDI A.0(START)
004A A3;          0061          PLO R3
004B D3;          0062          SEP R3
004C F880;        0063 START:   LDI #80       ..INIT.PRINTER POINTER - R4
004E B6;          0064          PHI R6        ..TO BEGINNING OF RAM: 8001H
004F B4;          0065          PHI R4        ..AND XOR TEMPORARY HOLDING
0050 F801;        0066          LDI #01       ..LOCATION - R6 TO 8000H
0052 A4;          0067          PLO R4
0053 3583;        0068          B2  LOAD      ..CHECK FOR INSTANT REPLAY
0055 A0;          0069          PLO R0        ..REQUEST. REPLAY IF 0
0056 F880;        0070          LDI #80
0058 B0;          0071          PHI R0        ..INITIALIZE DMA POINTER - R0
0059 F800;        0072          LDI #00       ..TO 8001H
005B 00;          0073          IDL
005C E6;          0074 XMIT:    SEX R6        ..ALL INPUT PRINTED?
005D 94;          0075          GHI R4
005E 56;          0076          STR R6
005F 90;          0077          GHI R0
0060 F3;          0078          XOR
0061 3A69;        0079          BNZ OVRUN
0063 84;          0080          GLO R4
0064 56;          0081          STR R6
0065 80;          0082          GLO R0
0066 F3;          0083          XOR
0067 327D;        0084          BZ  SAVE
0069 95;          0085 OVRUN:   GHI R5        ..OVER-RUN TEST ON
006A 56;          0086          STR R6        ..PRINT BUFFER
006B 94;          0087          GHI R4
006C F3;          0088          XOR
006D 3A75;        0089          BNZ URTCHK
006F 85;          0090          GLO R5
0070 56;          0091          STR R6
0071 84;          0092          GLO R4
0072 F3;          0093          XOR
0073 328F;        0094          BZ  OVFLOW
0075 3675;        0095 URTCHK:  B3  URTCHK    ..WAIT FOR UART READY
0077 3C77;        0096 PRTCHK:  BN1 PRTCHK    ..PRINTER READY TEST
0079 E4;          0097          SEX R4        ..READY IF HI
007A 61;          0098          OUT 1
007B 305C;        0099          BR  XMIT
007D 90;          0100 SAVE:    GHI R0
007E B7;          0101          PHI R7
007F 80;          0102          GLO R0
0080 A7;          0103          PLO R7
0081 304C;        0104          BR  START
0083 97;          0105 LOAD:    GHI R7
0084 B0;          0106          PHI R0
0085 87;          0107          GLO R7
0086 A0;          0108          PLO R0
0087 305C;        0109          BR  XMIT
0089 F8AA;        0110 COLDST:  LDI #AA
008B B8;          0111          PHI R8
008C A8;          0112          PLO R8
008D 3017;        0113          BR  MEMSIZ
008F 7B;          0114 OVFLOW:  SEQ           ..PRINT LENGTH EXCEEDED AMOUNT
0090 308F;        0115          BR  OVFLOW    ..OF AVAILABLE RAM IN SYSTEM.
0092 ;            0116          END           ..ERROR LITE IS ON STEADY.
0000
```

RCA
Solid State
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Memory/Microprocessor Products
Application Note
ICAN-6991

A Slave CDP1802 Serial Printer Buffer System

by K. Nagy

This Note describes a CDP1802-based stand-alone line-printer buffer that links a master processor system to a serial printer through an RS-232C interface. The main buffer board consists of a CDP1802 Microprocessor (configured as a peripheral controller), a CDP1854A UART with baud-rate generation devices (configured in industry mode 0 and able to handle separate receive and transmit baud rates), and a CDP18U42 EPROM (to store a minimal user program). With the addition of RCA Microboards for system RAM (CDP18S620, CDP18S621, CDP18S622, CDP18S623, CDP18S624, or CDP18S625 in various configurations from 4K to 16K), a buffer system with a printer character storage capacity of up to 32K bytes can be implemented.

The line buffer is especially useful with interactive computer systems; it frees high-speed terminals for other tasks while a slower printer (connected in parallel to the terminal through a serial port, such as is used with RCA Development Systems) prints from buffer memory. The buffer circuitry also illustrates how a CDP1800 processor can be configured as a slave controller that communicates with a master system through a serial port. In this configuration, some of the special I/O features of CDP1800 architecture are highlighted; these features include DMA control for high-speed data transfer, I/O instructions for communication with peripheral chips such as the CDP1854A UART, and the availability of several input flag lines for event polling.

The low power consumption of the system makes it ideal for operation from a storage battery, which provides portability of user data, and also protects data integrity should a line power failure occur.

System Modes

The line buffer operates in the following modes:

1. Receive data—The print buffer is loaded at some (usually high) baud rate (through a serial interface under CDP1802 DMA control).
2. Transmit data—Data is transmitted, usually at a low baud rate (through a serial interface under CDP1802 programmed I/O control), to the printer when the printer is selected and ready.
3. Instant replay—Data is retransmitted to the printer upon request.

These modes permit the system to accommodate a wide range of input and output conditions, and to communicate with many different peripheral devices.

System Set Up

The line-buffer system input and output is connected to suitable sending and receiving units equipped with RS-232C interfaces by means of cables and connectors. The system output contains a feedback (handshake) line that permits the printer to operate at its optimum speed; the feedback feature can be eliminated if necessary through software changes.

The printer-buffer prototype was evaluated using a CDP18S007 CDS Development System, an ADM-3A CRT Terminal, and an EPSON MX-80 Printer. However, the universal nature of the buffer design permits it to be used with a wide variety of master system and printer combinations.

Hardware

A block diagram of the system is shown in Fig. 1; detailed system interconnection diagrams are shown in Appendix A. The "U" designators used in the following text refer to the figures in Appendix A,and are identified in Table I and in the Appendix. Table II summarizes register assignments.

Table I — List of IC's Used in System

IC	Identity
U1	CDP1802 CPU
U2	CDP18U42 EPROM
U3	CDP1854A UART
U4	CD4013 D FF
U5, U6	CD4069 Hex Inverter
U7	CD4093 Quad 2-Input NAND
U8	CD4013 D FF
U9, U10, U11	CD40161 Sync Binary Counter
U12	MC1489 Quad Line Receiver
U13	MC1488 Quad Line Driver

Table II — Line-Buffer Register Use

R0	Initial Program Counter/DMA-IN Pointer
R3	Program Counter
R4	Printer Pointer
R5	End of Memory Pointer
R6	XOR Temporary Location Pointer
R7	Temporary DMA-IN Pointer
R8	Cold Start Flag

The system program resides in the CDP18U42, 256-byte UV Erasable PROM, U2, located in the lower 32K address space on the system map. The chip-select signal for the EPROM is generated by latching the high-order address byte of the MA7 signal by means of a CD4013 flip-flop (U4). The EPROM is selected when MA.1 is low ($\overline{CS1}$), $\overline{MRD}$ is low ($\overline{CS3}$), and $\overline{CLR}$ is high (CS2).

Printed in USA/8-81

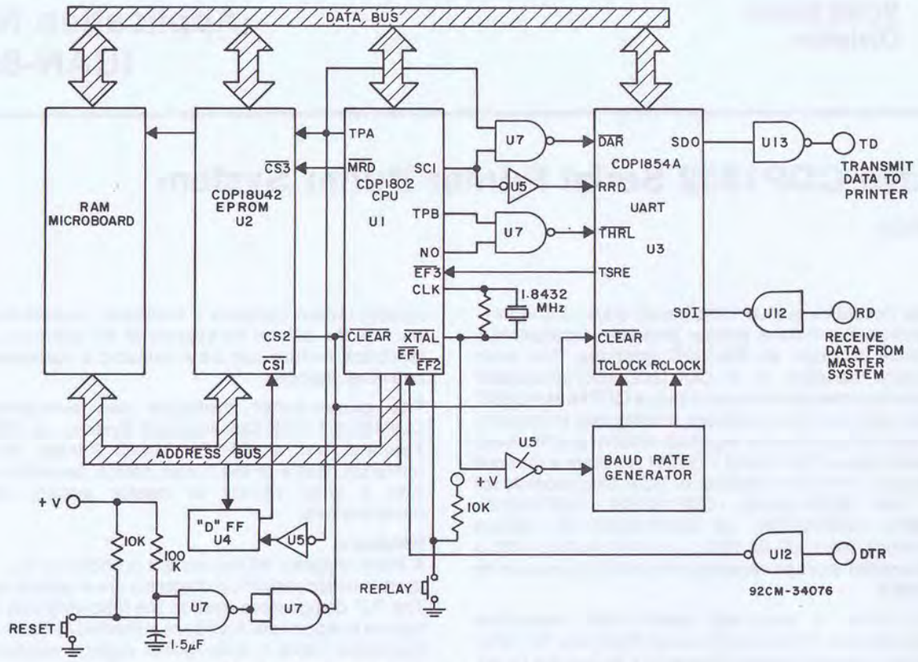

Fig. 1 - Block diagram of the serial printer buffer system.

The internal oscillator of the CDP1802 microprocessor is driven by a 1.8432-MHz external crystal, which acts as the system master clock. The crystal is connected between the CLOCK and XTAL terminals of the microprocessor. One inverter of the CD4069 (U5) provides a buffered signal called CLK OUT to the baud-rate generator divider chain for the UART.

Part of a CD4093 (U7) forms a power-on reset circuit that outputs a CLEAR signal to the microprocessor and the UART. An external reset signal can force the processor to restart program execution. An SPST switch connected to the EF2 flag-input terminal of the microprocessor provides the instant-replay request signal for the program. If this switch is in the replay mode, activation of the reset button will start the printing of the previously deposited contents of the RAM buffer. This feature relieves the host computer of the time-consuming task of producing copies on the printer.

A CDP4013, Dual D Flip-Flop (U8), forms a synchronous divide-by-three circuit; its output is connected to two CD40161B cascaded synchronous binary counters (U9 and U10). The Q outputs of U9 and U10 provide baud rates from 150 to 19,200 baud. The accuracy of these baud rates is comparable to that of the crystal oscillator. Another CD40161B synchronous binary counter (U11) is used in a divide by 11 configuration to generate the 110 baud used by some teletypes and other slow mechanical printers. Because it is possible to input to, or output from, this system at varying baud rates, the system is very useful in interactive applications or where baud-rate exchange is required.

The CDP1854A UART (U3) has two modes of operation. Mode 1 is directly compatible with the CDP1800 family of microprocessors without additional interface circuitry; software techniques are used for programming in this mode.[1] In Mode 0, the mode used in the serial printer buffer system, the CDP1854A is compatible with a great many other UART's, such as the TR1602A by Western Digital, and provides the user with hardware-option selection in the form of five independent switches. The functions of the switches are as follows:

SW5 - When open, the generation of parity is inhibited.

SW6 - When open, two stop bits are selected, when closed, one is selected. Selection of two stop bits with five data bits programmed selects 1.5 stop bits.

SW7, SW8 - These two switches select the character length (exclusive of parity) of five to eight data bits.

SW9 - This switch is closed for odd parity, opened for even parity.

Fig. 2 shows serial-word format-programming data. The UART has two independent byte-wide buses. Both receive and transmit buses are connected to the system data bus.

The system receive operation is initiated when a serial bit stream is sent via the RS-232 receiver interface to the UART. When the UART receiver assembles a full received character, the data available (DA) output goes high and initiates a DMA-IN cycle. During DMA, the CPU is forced into a DMA cycle (S2), which causes SC1 to go high; the result is a transfer of data from the UART receiver holding register to the data bus. The address and control signals needed to direct the flow of data into the RAM pointed to by DMA pointer R0 are generated during DMA. Additionally, hardware interconnections are made that cause the data available reset (DAR) flag to be reset. Reset is accomplished through a signal to the data available reset (DAR) input; the signal terminates the DMA-IN request before it is again sampled by the CPU. Finally, R0 is incremented at the end of the S2 cycle, and the system is ready for transfer of another byte of data when it is received.

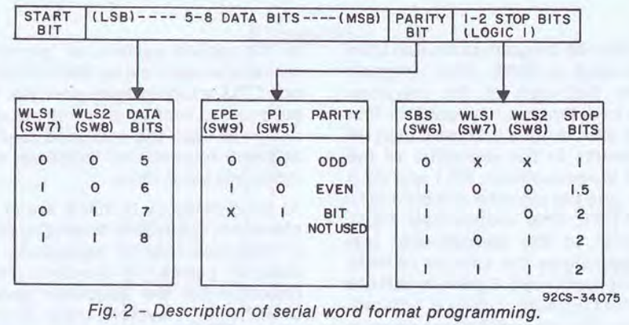

Fig. 2 - Description of serial word format programming.

The system transmit operation begins when the UART transmitter shift register is empty (TSRE high, polled via EF3) and the printer is selected (polled via EF1). The CPU issues an I/O command that signals the transmitter holding register load (THRL) input to transfer data from the data bus to the transmitter holding register. The data is serialized by the transmitter shift register and output, in the format selected by the user, through the serial data out (SDO) line and the RS-232 line driver to the printer. During the time that data is actively being transmitted by the UART, the TSRE signal will be low, preventing transmission of additional data. When the TSRE signal becomes high, and the printer is ready, a character can be transferred from the system data bus to the transmitter holding register. The microprocessor then outputs a low pulse to the UART transmitter holding register load (THRL) input, causing TSRE to go low. When the TSRE output signal goes high again, and EF1 is low (indicating that the printer is ready), another character can be loaded into the transmitter holding register for transmission. This process is repeated until all of the line-buffer memory contents are transmitted.

Baud-Rate Generation

The CDP1854A UART requires a clock signal that is 16 times the desired bit rate for proper operation. This 16X clock rate is applied to the UART receive clock (RCLOCK) and transmitter clock (TCLOCK) inputs. In the subject system, the RCLOCK and TCLOCK inputs are connected to separate frequencies (through SW 3 and SW 4). Both of these bit rates are derived from the same crystal oscillator and divider circuitry.

The bit rate and the number of bits per character determine the number of characters that can be transmitted in one second. If the UART receiver is required to operate at a data rate of 19,200 bits/s, then the receive clock (RCLOCK) frequency must be 16 x 19,200 = 307,200 Hz. Consequently, if the data transmission rate must be 300 bits/s, then the TCLOCK input of the UART must be connected to a clock frequency of 16 x 300 = 4800 Hz. Table III shows baud rates and frequencies supported by the system.

Software

The program flowchart is shown in Fig. 3. Upon power-on,

Table III — Baud Rates and Frequencies Supported by System

Baud Rate	16X Freq. (kHz)	Time (μs)
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1200	19.200	52.08
2400	38.400	26.04
4800	76.800	13.02
9600	153.600	6.51
19200	307.200	3.26

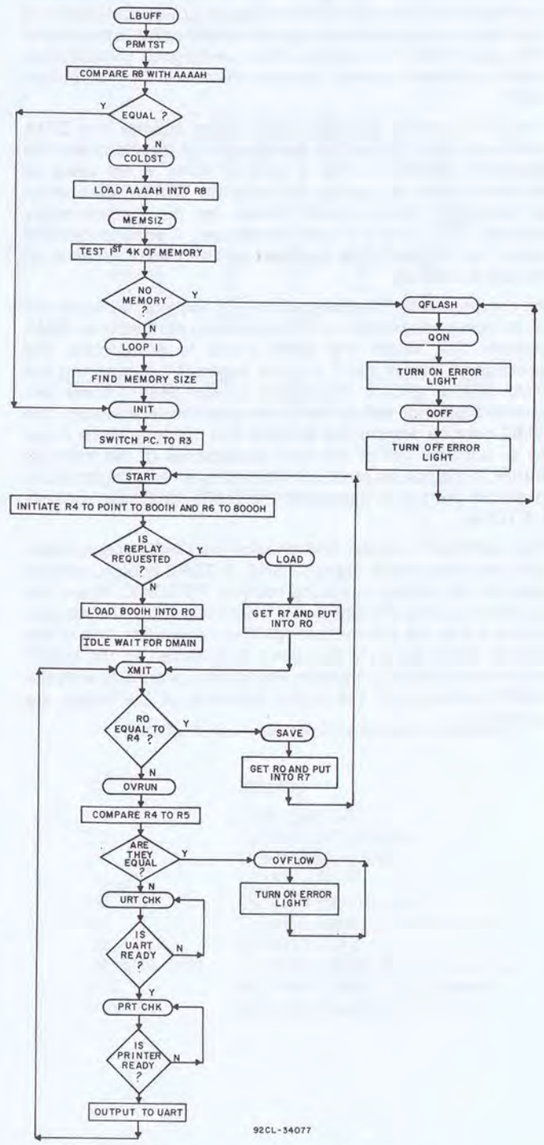

Fig. 3 - Program flowchart.

the power-on reset circuit initiates program execution from the first ROM location (located at 0000). After program execution has begun, the first part of the program, PRMTST, tests register R8 to determine if a "cold" or first start is being initiated. If the start is not a first start, then R8 contains AAAAH, which results in the execution of the routine INIT. If a cold start is encountered, R8.1 and R8.0 will contain random values, and the program will branch to the cold-start routine COLDST. This routine sets R8 to AAAAH, and passes control to the memory-size test routine, MEMSIZ, which determines the amount of RAM available in the system for line-buffer use. If there is no RAM connected to the system, the QFLASH routine is entered, and the error LED flashes on and off until the condition is corrected and the reset button pressed. Upon completion of the memory-size routine, register R5 will contain the size of the user RAM. The system then undergoes initialization under software control through execution of the routine INIT.

The INIT routine initializes the printer pointer and DMA pointer to 8001H (the first available RAM location) and the program counter to R3. A byte of RAM is set aside at location 8000H for use by the program. When initialization is complete, the program checks for the instant-replay request ($\overline{EF2}$ low); if it finds no request, it goes to idle and waits for the first byte received by the UART receiver to initiate a DMA-IN.

As the processor receives a DMA-IN request, it places the byte, now on the data bus, in the location pointed to by DMA pointer R0. When the DMA cycle is completed, the processing of the XMIT routine begins by comparing the DMA pointer (R0) to the printer pointer (R4). If these two pointers are not set to the same location in memory, the XMIT routine determines whether the printer pointer is set to an address within the valid boundaries of the memory buffer. If it is not, an error is indicated by an error light; if it is, program control is passed to the UART checking routine, URTCHK.

The URTCHK routine first checks the UART transmitter-shift-register-empty signal, TSRE. If TSRE is high, control goes to the printer checking routine, PRTCHK. When this routine receives a ready signal from the printer, it outputs a character to the printer through the transmitter side of the UART. After the byte has been transferred to the UART transmitter holding register, the system proceeds with the XMIT routine until the entire contents of the buffer are printed out.

In the subject system, all incoming data is deposited in memory in real time by DMA-IN within an execution time of one CPU machine cycle per byte. This method is similar but superior to that of an interrupt driven system because it does not have the overhead associated with the interrupt software routine and, therefore, can easily cope with high incoming baud rates.

At baud rates of 19,200 bits per second and 10 bits per character, the system has approximately 520 microseconds of time available for processing between two successive DMA-IN pulses. At a system clock rate of 1.8432 MHz (selected for the baud-rate generation circuits for the UART), the system has enough time to execute approximately 120 machine cycles before the next DMA-IN cycle comes in.

The software assembly listing in ASM 4 is shown in Appendix B.

Summary

In summary, this system is especially useful in applications requiring interaction with a variety of types of equipment as it is capable of taking input or providing output at varying baud rates. The instant-replay feature relieves a host computer of the time consuming task of producing copies on a printer. The system UART, when used in mode 0, constitutes a peripheral device that makes interfacing of the line-buffer system with other systems a simple matter. The low power consumption of the line-buffer system makes it an ideal one for operation from a storage battery, which provides portability of user data and protection of this data in the event of a line-power failure.

References and Bibliography

1. "Use of the CDP1854 UART with RCA Microprocessor Evaluation Kit CDP18S020 or EK/Assembler-Editor Design Kit CDP18S034," R.G. Ott, RCA Solid State Application Note ICAN-6632.
2. "COS/MOS Memories, Microprocessors, and Support Systems," RCA Solid State Databook SSD-260.
3. "COS/MOS Integrated Circuits," RCA Solid State Databook SSD-250.
4. "COS/MOS Integrated Circuits Manual," RCA Solid State publication CMS-272.
5. "User Manual for the CDP1802 COSMAC Microprocessor," RCA Solid State publication MPM-201.

Appendix A

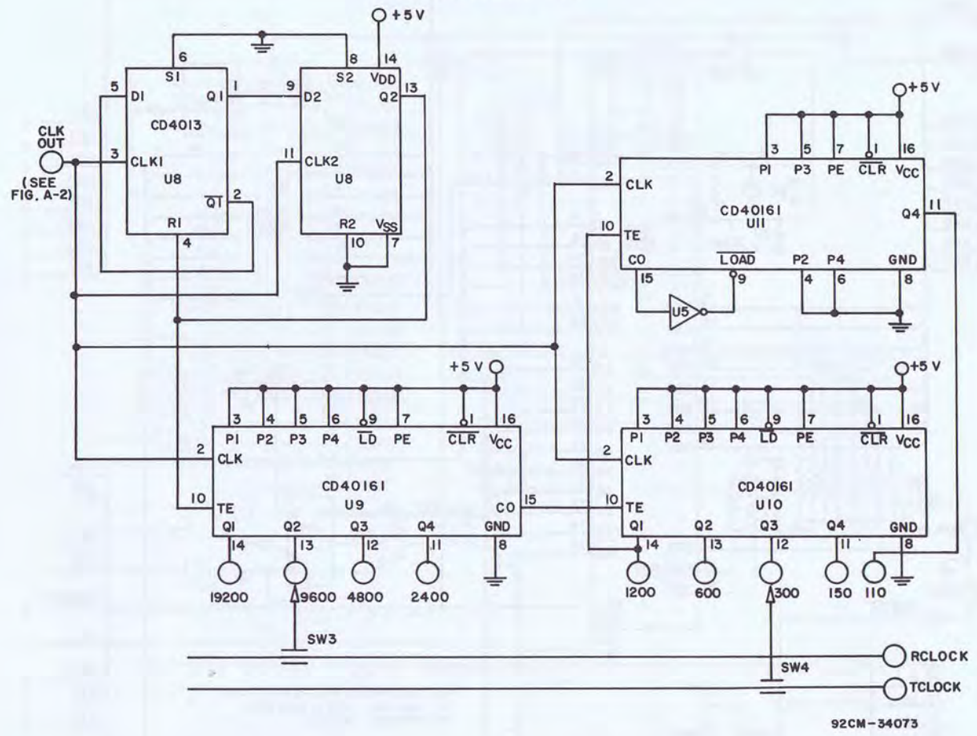

Fig. A-1 - Interconnection diagram for line-buffer baud-rate generator.

Table A-I — Microboard Computer Bus Interface (Fig. A-2)

Pin	Signal	Pin	Signal
A	TPA-P	1	DMA1-N
B	TPB-P	2	DMA0-N
C	DB0-P	3	RNU-P
D	DB1-P	4	INT-N
E	DB2-P	5	MRD-N
F	DB3-P	6	Q-P
H	DB4-P	7	SC0-P
J	DB5-P	8	SC1-P
K	DB6-P	9	CLEAR-N
L	DB7-P	10	WAIT-N
M	A0-P	11	−5 V/−15 V
N	A1-P	12	SPARE
P	A2-P	13	CLOCK OUT
R	A3-P	14	N0-P
S	A4-P	15	N1-P
T	A5-P	16	N2-P
U	A6-P	17	EF1-N
V	A7-P	18	EF2-N
W	MRW-N	19	EF3-N
X	EF4-N	20	+12 V/+15 V
Y	+5 V	21	+5 V
Z	GND	22	GND

Table A-II — List of IC's Used in System

IC	Identity
U1	CDP1802 CPU
U2	CDP18U42 EPROM
U3	CDP1854A UART
U4	CD4013 D FF
U5, U6	CD4069 Hex Inverter
U7	CD4093 Quad 2-Input NAND
U8	CD4013 D FF
U9, U10, U11	CD40161 Sync Binary Counter
U12	MC1489 Quad Line Receiver
U13	MC1488 Quad Line Driver

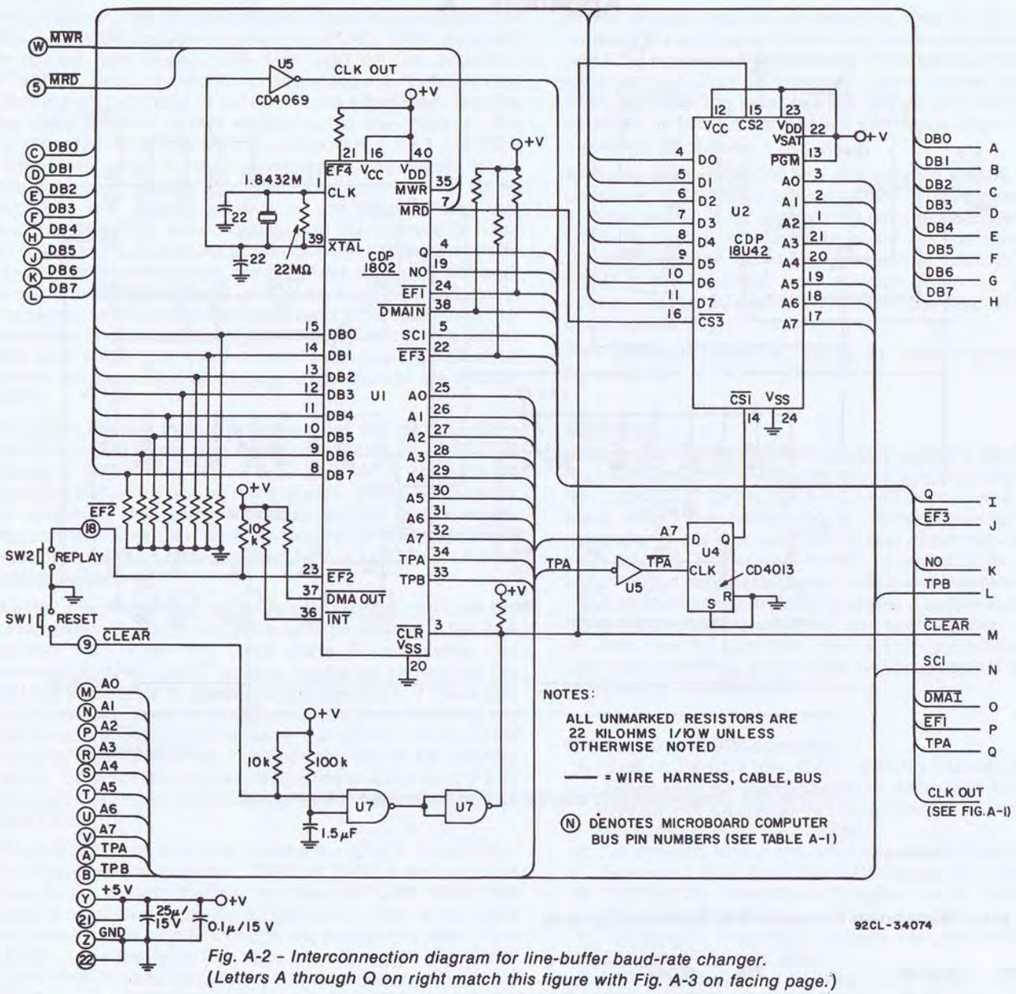

Fig. A-2 – Interconnection diagram for line-buffer baud-rate changer.
(Letters A through Q on right match this figure with Fig. A-3 on facing page.)

Appendix B — Program Listing

```
0000 ;          0001 ..*****************************************
0000 ;          0002 ..*                                       *
0000 ;          0003 ..* * *  LBUFF  3-15-81   K. NAGY   * * *
0000 ;          0004 ..*                                       *
0000 ;          0005 ..*****************************************
0000 ;          0006 ..
0000 ;          0007 ..
0000 ;          0008          ORG #0000
0000 F880;      0009 PRMTST: LDI #80       ..CHECK FOR COLD START
0002 B5;        0010          PHI R5
0003 F800;      0011          LDI #00
0005 A5;        0012          PLO R5
0006 E5;        0013          SEX R5
0007 98;        0014          GHI R8
0008 55;        0015          STR R5
0009 F8AA;      0016          LDI #AA
000B F5;        0017          SD
000C 3A89;      0018          BNZ COLDST
000E 88;        0019          GLO R8
000F 55;        0020          STR R5
0010 F8AA;      0021          LDI #AA
0012 F5;        0022          SD
0013 3A89;      0023          BNZ COLDST
0015 3044;      0024          BR  INIT
0017 F88F;      0025 MEMSIZ: LDI #8F       ..CHECK FOR MEMORY SIZE
```


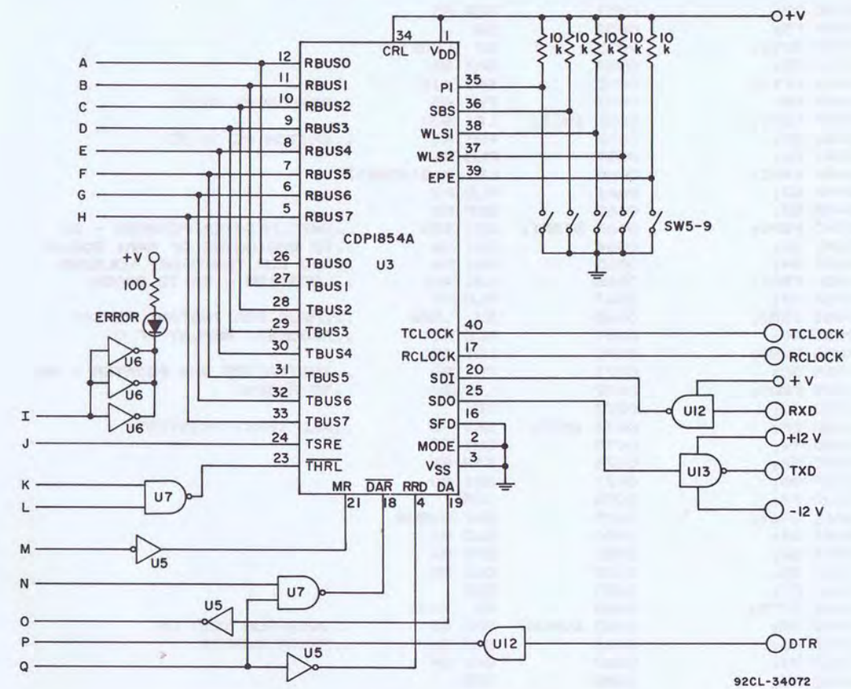

Fig. A-3 – Interconnection diagram for line-buffer receiver/transmitter.
(Letters A through Q on left match this figure with Fig. A-2 on facing page.)

Appendix B (Cont'd)

```
0019 B5;        0026          PHI R5       ..IN THE SYSTEM MIN. 4K.
001A F8FF;      0027          LDI #FF      ..MAX. 32K.
001C A5;        0028          PLO R5
001D E5;        0029          SEX R5
001E F8AA;      0030          LDI #AA
0020 55;        0031          STR R5
0021 F5;        0032          SD
0022 3236;      0033          BZ  LOOP1
0024 7B;        0034 QFLASH: SEQ          ..IF SYSTEM MEMORY IS
0025 F820;      0035          LDI #20      ..LESS THAN 4K FLASH
0027 B5;        0036          PHI R5       ..ERROR LITE
0028 25;        0037 QON:    DEC R5
0029 95;        0038          GHI R5
002A 3A28;      0039          BNZ QON
002C 7A;        0040          REQ
002D F820;      0041          LDI #20
002F B5;        0042          PHI R5
0030 25;        0043 QOFF:   DEC R5
0031 95;        0044          GHI R5
0032 3A30;      0045          BNZ QOFF
0034 3024;      0046          BR  QFLASH
0036 95;        0047 LOOP1:  GHI R5
0037 FC10;      0048          ADI #10
0039 B5;        0049          PHI R5
003A F8AA;      0050          LDI #AA
```

Appendix B (Cont'd)

```
003C 55;          0051          STR R5
003D F5;          0052          SD
003E 3236;        0053          BZ  LOOP1
0040 95;          0054          GHI R5
0041 FF10;        0055          SMI #10
0043 B5;          0056          PHI R5        ..R5=MEMORY SIZE
0044 F800;        0057 INIT:    LDI #00
0046 B3;          0058          PHI R3        ..SWITCH PC TO R3
0047 A6;          0059          PLO R6
0048 F84C;        0060          LDI A.0(START)
004A A3;          0061          PLO R3
004B D3;          0062          SEP R3
004C F880;        0063 START:   LDI #80       ..INIT.PRINTER POINTER - R4
004E B6;          0064          PHI R6        ..TO BEGINNING OF RAM: 8001H
004F B4;          0065          PHI R4        ..AND XOR TEMPORARY HOLDING
0050 F801;        0066          LDI #01       ..LOCATION - R6 TO 8000H
0052 A4;          0067          PLO R4
0053 3583;        0068          B2  LOAD      ..CHECK FOR INSTANT REPLAY
0055 A0;          0069          PLO R0        ..REQUEST. REPLAY IF 0
0056 F880;        0070          LDI #80
0058 B0;          0071          PHI R0        ..INITIALIZE DMA POINTER - R0
0059 F800;        0072          LDI #00       ..TO 8001H
005B 00;          0073          IDL
005C E6;          0074 XMIT:    SEX R6        ..ALL INPUT PRINTED?
005D 94;          0075          GHI R4
005E 56;          0076          STR R6
005F 90;          0077          GHI R0
0060 F3;          0078          XOR
0061 3A69;        0079          BNZ OVRUN
0063 84;          0080          GLO R4
0064 56;          0081          STR R6
0065 80;          0082          GLO R0
0066 F3;          0083          XOR
0067 327D;        0084          BZ  SAVE
0069 95;          0085 OVRUN:   GHI R5        ..OVER-RUN TEST ON
006A 56;          0086          STR R6        ..PRINT BUFFER
006B 94;          0087          GHI R4
006C F3;          0088          XOR
006D 3A75;        0089          BNZ URTCHK
006F 85;          0090          GLO R5
0070 56;          0091          STR R6
0071 84;          0092          GLO R4
0072 F3;          0093          XOR
0073 328F;        0094          BZ  OVFLOW
0075 3675;        0095 URTCHK:  B3  URTCHK    ..WAIT FOR UART READY
0077 3C77;        0096 PRTCHK:  BN1 PRTCHK    ..PRINTER READY TEST
0079 E4;          0097          SEX R4        ..READY IF HI
007A 61;          0098          OUT 1
007B 305C;        0099          BR  XMIT
007D 90;          0100 SAVE:    GHI R0
007E B7;          0101          PHI R7
007F 80;          0102          GLO R0
0080 A7;          0103          PLO R7
0081 304C;        0104          BR  START
0083 97;          0105 LOAD:    GHI R7
0084 B0;          0106          PHI R0
0085 87;          0107          GLO R7
0086 A0;          0108          PLO R0
0087 305C;        0109          BR  XMIT
0089 F8AA;        0110 COLDST:  LDI #AA
008B B8;          0111          PHI R8
008C A8;          0112          PLO R8
008D 3017;        0113          BR  MEMSIZ
008F 7B;          0114 OVFLOW:  SEQ           ..PRINT LENGTH EXCEEDED AMOUNT
0090 308F;        0115          BR  OVFLOW    ..OF AVAILABLE RAM IN SYSTEM.
0092 ;            0116          END           ..ERROR LITE IS ON STEADY.
0000
```


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