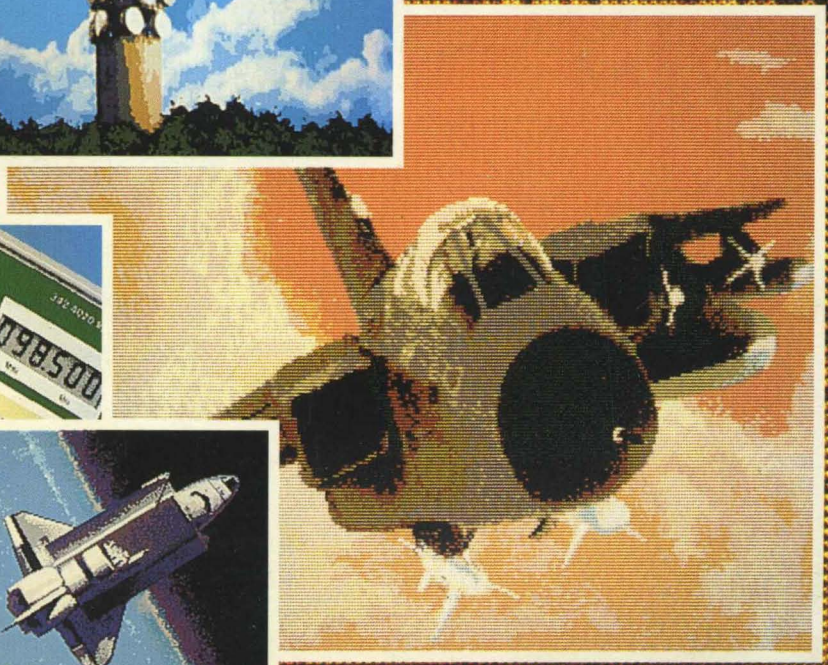
FREQUENCY DIVIDERS and SYNTHESISERS

IC Handbook



Plessey Semiconductors

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PLESSEY
Semiconductors

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Foreword

Plessey Semiconductors has long been recognised as a leading source of high speed dividers ICs. The SP8000 series of dividers has led the world over the past 15 years in speed and technical performance. One of the most comprehensive ranges of fixed and programmable dual-modulus frequency dividers currently available, the SP8000 series has found design slots in a wide variety of applications. In the Military market, our devices are used in Frequency Synthesis systems in Radio Communications, Guidance systems in Missiles, Electronic Warfare etc. In the Professional market, they are used in Instrumentation equipment, and in Cellular/Cordless telephones and Private Mobile Radio equipment.

To satisfy the differing requirements of these markets, all products in the SP8000 series can be supplied with a variety of packaging and screening options.

Plessey Semiconductors also offers a wide variety of parts to cater to the various requirements of Frequency Synthesiser systems. From UHF Two-Modulus Synthesiser systems to a single chip self-contained PLL Synthesiser IC, our products have truly established themselves, with more innovative designs in the pipeline to further our reputation as a suplier of synthesiser circuits.

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SP8000 series high speed dividers Product Index

Plessey Semiconductors' SP8000 series leads the world in technical performance. One of the most comprehensive ranges of dividers available, the SP8000 series has been developed and extended to cater for the exacting requirements of the instrumentation and communications markets. The range includes prescalers from divide-by-2 up to divide-by-129, operating from 1Hz to 3.5GHz.

Suffix A Military	-55°C to +125°C
Suffix B Commercial	-40°C to +85°C
	0°C to +70°C
	-30°C to 70°C
	(please check with data sheet of device type)

Fixed modulus dividers

Division ratio	Type	Temperature Range (°C)				f_{max} (MHz)	Supply Voltage (V)			I_{max} (mA)	Output		Package		
		-55 +125	-40 +85	-30 +70	0 +70		5.0	5.2	6.8		TTL	ECL	CM	DG	DP
2	SP8604A	●				300		●		18		●	●		
	SP8604B			●		300		●		18		●	●		
	SP8602A	●				500		●		18		●	●		
	SP8602B			●		500		●		18		●	●		
	SP8607A	●				600		●		18		●	●		
	SP8607B			●		600		●		18		●	●		
	SP8605A	●				1000		●		100		●		●	
	SP8605B				●	1000		●		100		●		●	
	SP8606A	●				1300		●		100		●		●	
	SP8606B				●	1300		●		100		●		●	
	SP8822A	●				1800	●			53		●		●	
	SP8822B			●		1800	●			53		●			●
	SP8812A	●				2400	●			65		●		●	
	SP8812B			●		2400	●			65		●			●
	SP8802A	●				3300	●			100		●		●	
	SP8832B				●	3500	●			100		●			●
4	SP8790A	●				60	●			11	●		●		
	SP8790B			●		60	●			11	●		●		
	SP8601A	●				150		●		25	●	●	●		
	SP8601B			●		150		●		25	●	●	●		
	SP8600A	●				250		●		25	●	●	●		
	SP8600B			●		250		●		25	●	●	●		
	SP8610A	●				1000		●		100		●		●	
	SP8610B				●	1000		●		100		●		●	
	SP8611A	●				1300		●		100		●		●	
	SP8611B				●	1500		●		100		●		●	
	SP8712B				●	2400			●	110		●		●	
	SP8824A	●				1800	●			48		●		●	
	SP8824B			●		1800				48	●	●			●
	SP8814A	●				2400	●			52				●	
	SP8814B			●		2400	●			52				●	
	SP8804A	●				3300	●			90				●	
	SP8835B				●	3500	●			90		●			●
5	SP8620A	●				400		●		55		●		●	
	SP8620B			●		400		●		55		●		●	

Fixed modulus dividers (continued)

Division ratio	Type	Temperature Range (°C)				f_{max} (MHz)	Supply Voltage (V)			I_{max} (mA)	Output		Package		
		-55 +125	-40 +85	-30 +70	0 +70		5.0	5.2	6.8		TTL	ECL	CM	DG	DP
8	SP8794A	●				120	●			11	●		●		
	SP8794B			●		120	●			11	●		●		
	SP8670A	●				600		●		45		●		●	
	SP8670B			●		600		●		45		●		●	
	SP8735B				●	600		●		90	BN	●		●	
	SP8675B				●	1000			●	95		●		●	
	SP8678B				●	1500			●	95		●		●	
	SP8828A	●				1800	●			45		●		●	
	SP8828B			●		1800	●			45		●			●
	SP8818A	●				2400	●			48		●		●	
	SP8818B			●		2400	●			48		●			●
	SP8808A	●				3300	●			85		●		●	
	SP8838B			●		3500	●			85					●
10	SP8660A	●				150	●			13	●		●		
	SP8660B			●		150	●			13	●		●		
	SP8660			●		150	●			13	●				●
	SP8637B				●	400		●		90	BN	●		●	
	SP8630A	●				600		●		70		●		●	
	SP8630B			●		600		●		70		●		●	
	SP8635B				●	600		●		90	BN	●		●	
	SP8634B				●	700		●		90	BN	●		●	
	SP8665B				●	1000			●	105		●		●	
	SP8668B				●	1500			●	105		●		●	
	SP8830A	●				1500	●			50		●		●	
	SP8830B			●		1500	●			50		●			●
16	SP8659A	●				200	●			13	●		●		
	SP8659B			●		200	●			13	●		●		
	SP8650A	●				600		●		45		●		●	
	SP8650B			●		600		●		45		●		●	
20	SP8657A	●				200	●			13	●		●		
	SP8657B			●		200	●			13	●		●		
32	SP8655A	●				200	●			13	●		●		
	SP8655B			●		200	●			13	●		●		
64	SP8755A	●				1200	●			75	●			●	
	SP8755B			●		1200	●			75	●			●	
100	SP8629		●			150	●	●		45	●			●	●

BN = Binary outputs
Package codes: CM = Metal Can, DG = Ceramic DIL, DP = Plastic DIL, MP = Miniature Plastic DIL

Two-modulus programmable dividers

Division ratio	Type	Temperature Range (°C)				f_{max} (MHz)	Supply Voltage (V)			I_{max} (mA)	Control Input		Output		Package			
		-55 +125	-40 +85	-30 +70	0 +70		5.0	5.2	9.5		TTL	ECL	TTL	ECL	CM	DG	DP	MP
3/4	SP8720A	●				300		●		65		●		●		●		
	SP8720B			●		300		●		65		●		●		●		
5/6	SP8740A	●				300		●		60		●		●		●		
	SP8740B			●		300		●		60		●		●		●		
6/7	SP8741A	●				300		●		60		●		●		●		
	SP8741B			●		300		●		60		●		●		●		
8/9	SP8691A	●				200	●	●		21		●	●	●		●		
	SP8691B			●		200	●	●		21		●	●	●		●		
	SP8743A	●				500		●		60		●		●		●		
	SP8743B			●		500		●		60		●		●		●		
10/11	SP8695A	●				200	●	●		21		●	●	●		●		
	SP8695B			●		200	●	●		21		●	●	●		●		
	SP8690A	●				200	●	●		21		●	●	●		●		
	SP8690B			●		200	●	●		21		●	●	●		●		
	SP8799A	●				200		●		7	●		●			●		
	SP8799		●			225		●		7	●		●				●	●
	SP8647A	●				250	●	●		65		●	●	●		●		
	SP8647B			●		250	●	●		65		●	●	●		●		
	SP8643A	●				350		●		65		●		●		●		
	SP8685A	●				500		●		70		●		●		●		
	SP8685B			●		500		●		70		●		●		●		
	SP8680A	●				550	●	●		111		●	●	●		●		
	SP8680B		●			575	●	●		111		●	●	●		●	●	
16/17	SP8782A	●				1000	●			40						●		
	SP8782B			●		1000	●			40							●	
20/21	SP8789A	●				200		●		7	●		●			●		
	SP8789		●			225		●		7	●		●				●	●
20/22	SP8785A	●				1000		●		115		●		●		●		
	SP8785B			●		1000		●		115		●		●		●		
	SP8786A	●				1300		●		115		●		●		●		
	SP8786B			●		1300		●		115		●		●		●		
32/33	SP8795A	●				200		●		7	●		●			●		
	SP8795		●			225		●		7	●		●				●	●
40/41	SP8793A	●				200		●		7	●		●			●		
	SP8793		●			225	●	●	●	7	●		●			●	●	●
	SP8716		●			520		●		11.9	●			C			●	●
	SP8716A	●				520		●		11.9	●			C		●		
64/65	SP8704[1]		●			950	●			13	●						●	●
	SP8718		●			520		●		11.9	●			C			●	●
	SP8718A	●				520		●		11.9	●			C		●		

1. The SP8704 is programmable to divide by either 64/65 or 128/129.
C = CMOS output and control input.

Two-modulus programmable dividers (continued)

Division Ratio	Type	Temperature Range (°C)				f_{max} (MHz)	Supply Voltage (V)			I_{max} (mA)	Control Input		Output		Package			
		-55 +125	-40 +85	-30 +70	0 +70		5.0	5.2	9.5		TTL	ECL	TTL	ECL	CM	DG	DP	MP
80/81	SP8792A	●				200		●		7	●		●			●		
	SP8792		●			225	●	●	●	7	●		●				●	●
	SP8719		●			520		●		11.9	●			C			●	●
	SP8719A	●				520		●		11.9	●			C		●		
100/101	SP8710A	●				225	●			8	●			C		●		
	SP8710			●		250	●			6	●			C			●	
128/129	SP8703			●		1000	●			40	●			C		●		●
	SP8704[1]		●			950	●			13	●						●	●

1. The SP8704 is programmable to divide by either 64/65 or 128/129.
C = CMOS output and control input.

Frequency synthesisers

Type	Function	Temperature Range (0 °C)	Page
NJ8820	Frequency synthesiser, PROM interface	-30 to +70	229
NJ8820B	Frequency synthesiser, PROM interface	-40 to +85	229
NJ8821	Frequency synthesiser, microprocessor interface, resettable counters	-30 to +70	236
NJ8821B	Frequency synthesiser, microprocessor interface, resettable counters	-40 to +85	236
NJ8821A	Frequency synthesiser, microprocessor interface, resettable counters	-55 to +125	241
NJ8822	Frequency synthesiser, microprocessor serial interface, resettable counters	-30 to +70	246
NJ8822B	Frequency synthesiser, microprocessor serial interface, resettable counters	-40 to +85	246
NJ8822A	Frequency synthesiser, microprocessor serial interface, resettable counters	-55 to +125	251
NJ8823	Frequency synthesiser, microprocessor interface, non-resettable counters	-30 to +70	256
NJ8823B	Frequency synthesiser, microprocessor interface, non-resettable counters	-40 to +85	256
NJ8824	Frequency synthesiser, microprocessor serial interface, non-resettable counters	-30 to +70	261
NJ8824B	Frequency synthesiser, microprocessor serial interface, non-resettable counters	-40 to +85	261
NJ882C25	Frequency synthesiser, microprocessor serial interface, for 3V to 5V operation	-30 to +70	266
NJ88C30	VHF frequency synthesiser	-30 to +70	272
NJ88C31	MF/VHF frequency synthesiser	-40 to +85	277
SP2001	Direct digital synthesiser with 100MHz output	-10 to +85	282
SP8850	1.5GHz professional synthesiser	-55 to +125	284

Product List

High speed dividers

Frequency synthesisers

Semi-Custom design

For more than a decade Plessey Semiconductors has led and consistently advanced the state of the art in semi-custom technology.

This leadership has been based on the use of comprehensive design software, Plessey Design System (PDS). PDS is independent of both technology and function in that Gate Arrays and cell based designs using CMOS or Bipolar can be developed.

PDS is supported on a DEC VAX/VMS based system. However, Plessey supports Daisy, Valid and Mentor workstations, which are all interfaced into PDS, thereby offering an easy design route to meet your needs and costs.

These support routes offer the user the maximum flexibility in their design. However, Plessey also offers a 'turnkey' design function where we will complete the design from start to finish.

We offer a complete range of CMOS and Bipolar processes to meet all requirements of speed, power, packing density and cost and a very comprehensive range of through-hole, surface mount and pin grid array packages.

Gate Array Families

Plessey offers a complete range of Gate Array families, in both CMOS and ECL, for cost-effective, fast turn-round projects - see tables below.

CLA 3000 SERIES (CMOS)

- Double layer metal
- 4 micron channel length
- 2.8ns typ. gate delay
- 20MHz system clock
- Fully auto-routed
- 3V to 6V power supply
- Static protected I/O
- Military screening
- >90 % utilization of gates

PRODUCT FAMILY:

	Gates	I/O	Power
CLA31XX	840	40	4
CLA33XX	1440	52	4
CLA35XX	2400	64	4

CLA 5000 SERIES (CMOS)

- Double layer metal
- 2 micron channel length
- 1.2ns typ. gate delay
- 40MHz system clock rate
- Fully auto-routed
- 3V to 6V power supply
- Static protected I/O
- Military screening
- >90% utilization of gates

PRODUCT FAMILY:

	Gates	I/O	Power
CLA51XX	640	36	4
CLA52XX	1232	48	8
CLA53XX	2016	64	8
CLA54XX	3060	80	8
CLA55XX	4408	96	16
CLA56XX	5984	112	16
CLA57XX	7104	128	16
CLA58XX	8064	144	16
CLA59XX	10044	160	16

ELA 60000 (ECL)

- High performance: 1GHz
- 180ps typ. gate speed
- ECL 10K, ECL 100K, TTL and
- CMOS compatible
- Programmable speed/power
- Full military operation

PRODUCT FAMILY:

	Gates	Pads
ELA61000	660	48
ELA62000	1400	68
ELA63000	2900	96
ELA65000	4500	120

Plessey MEGACELL

PLESSEY MEGACELL offers the ASIC designer the opportunity to move to VHSIC gate complexities without losing the simplicity of gate array design methods. MEGACELL also offers design freedom and product innovation through creative design.

Cell Library

Four types of library elements are available giving functional, dynamic, and physical design flexibility:

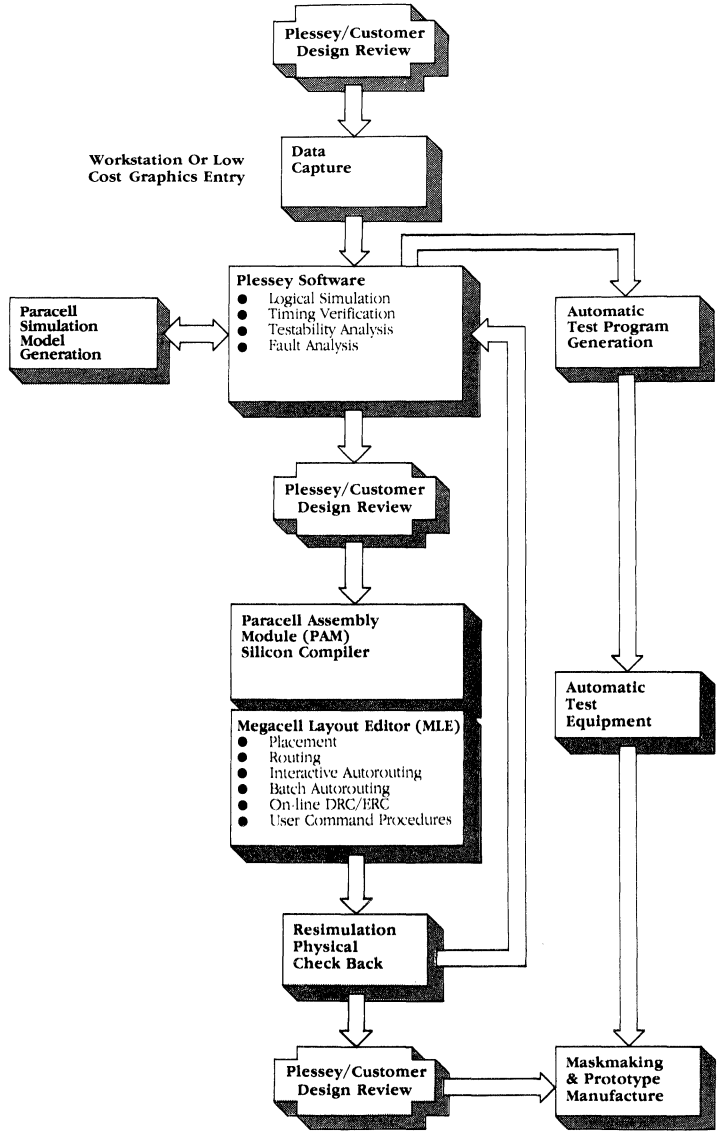
Microcells are modular size cells of simple logic functions (gates and flip-flops) similar to those in current standard logic families.

Macrocells comprise a user-library of building-blocks (e.g. 74 Series TTL) compiled from Microcells to speed up design entry.

Paracells are cells which can be parameterised through their regular composition (e.g. ROM, RAM, PLA). The simple netlist cell code is auto-compiled into a physical entity requiring very little design effort for these types of cells.

Supracells are large fixed-function cells pre-designed to replicate or improve existing VLSI standard functions. Many standard products can be incorporated into the Supracell concept.

Design Route



The Quality Concept

Quality cannot be inspected into a product; it is only by careful design and evaluation of materials, parts and processes (followed by strict control and ongoing assessment) that quality products will be produced.

All designs conform to standard layout rules, all processes are thoroughly evaluated and all new piece part designs and suppliers are investigated before authorisation for production use.

The same basic procedures are used on all products up to and including device packing. It is only then that extra operations are performed for certain customers in terms of lot qualification or release procedure.

By working to common procedures all users benefit; the high reliability user gains the advantage of scale hence improving the confidence factor in the quality achieved, whilst the volume user gains the benefits of basic high reliability design concepts.

Plessey Semiconductors have the following factory approvals:

BS9300 and **BS9400** (BSI Approval No. 1053/M).

CECC50000 and **CECC90000** (Reg. No. M/0020/CECC/UK-1053/M).

DEF-STAN 05-21 (DCL Reg. No. 1SB PO1).

Plessey Semiconductors conforms to **MIL-M-38510F** and is qualified to supply to **MIL-STD-883C.**

Screening

Different screening procedures are carried out by Plessey Semiconductors Limited, a brief description of the differences involved are explained in the next few pages.

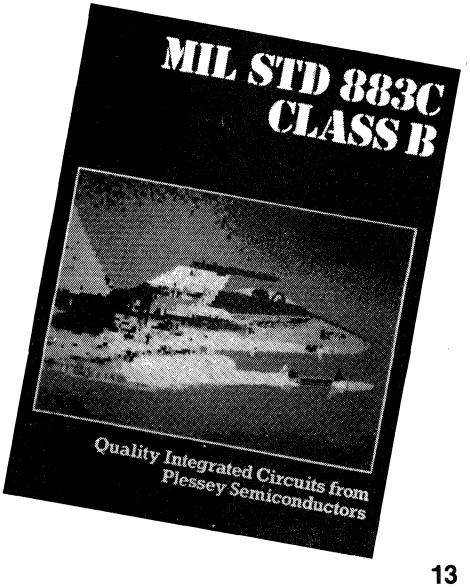
Stage/Operation	PLESSEY HI-REL CLASS B (References are to MIL-STD-883C)	MIL-STD-883C CLASS B Method 5004
Internal Visual	Method 2010 Test Condition B 100%	Method 2010 Test Condition B 100%
Stabilisation Bake	Method 1008 24 Hrs at Condition C 100%	Method 1008 24 Hrs at Condition C 100%
Temperature Cycling	Method 1010 Test Condition C 100%	Method 1010 Test Condition C 100%
Constant Acceleration	Method 2001 Test condition E Y1 only. 100%	Method 2001 Test Condition E Y1 only. 100%
Visual Inspection	-	100 %
Initial Electrical	Those parameters requiring Delta calculations. 100%	Those parameters requiring Delta calculations. 100%
Burn-In	Method 1015 160 Hrs at 125 °C min. 100%	Method 1015 160 Hrs at 125 °C min. 100%
Post Burn-In Electrical Test	Full Electrical Test to guarantee Data Sheet. 100%	Those parameters requiring Delta Calculations. 100%
PDA Calculation	5 % max. All lots.	5 % max. All lots.
Final Electrical Test	Done as Post Burn-in Test 100%	Full Group A tests as Method 5005 100%
Seal (a) Fine Seal (b) Gross	Method 1014 100%	Method 1014 100%
Qualification/Quality Conformance Test	-	Method 5005 Class B Samples as necessary
External Visual	Plessey Spec. sample	Method 2009 100%

Stage/ Operation	Standard Product	Plessey Hi-Rel B	MIL-STD-883C Class B	MIL-STD-883C Class S	BS9400 Level S2
Coding (example)	SPxxxxA	SPxxxxAB	SPxxxxAC	SPxxxxAS	SPxxxxABSS2
Wafer-fab				Wafer-lot accept Method 5007	
Probe test	100 %	100 %	100 %	100 %	100 %
Visual inspect chips	Usually 2010 Cond B	2010 Cond B	2010 Cond B	2010 Cond A	BS9400 1.2.10 Cond B
Assemble				Includes 100 % bond pull	
Screen	None	As list attached	Method 5004 Class B	Method 5004 Class S	BS9400 1.2.9 Level B
Test	100 %	100 %	100 %	100 %	100 %
Conformance testing	None	None	Method 5005 Class B Group A Group B Group C Group D	Method 5005 Class S Group A Group B Group D	BS9400 Group A Group B Group C Group D
Ship					

NOTES
1. Visual inspection BS9400 1.2.10 Cond B is equivalent to MIL-STD-883 Method 2010 Cond B.
2. Screening BS9400 1.2.9 Level B is equivalent to MIL-STD-883 Method 5004 Class B EXCEPT it does not include 100% hot and cold test.
3. Conformance testing BS9400 is similar to MIL-STD-883 Class B EXCEPT:
   Group A does not necessarily include hot and cold testing.
   Group B does include 160 hour operating life test.
   Group C does include 2000 hour operating life test and hot and cold testing.
   Group D only usually includes 8000 hour life test and dimension checks.

MIL-STD-883C Class B Integrated Circuits

Many of the ICs contained in this Handbook are also available from Plessey Semiconductors screened to MIL-STD-883C Class B. For technical information on these plus other MIL grade linear and digital circuits, ask for our MIL-STD-883C Class B Integrated Circuit Handbook, Publication No. P.S.2162.



Technical Data

1. SP8000 Series High speed dividers

SP8600A & B

250MHz ÷ 4

The SP8600 is an asynchronous ECL counter with open collector outputs. It requires external input bias and an AC coupled input signal of 600mV p-p.

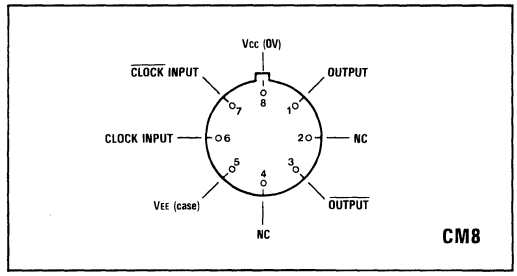


Fig.1 Pin connections - bottom view

FEATURES

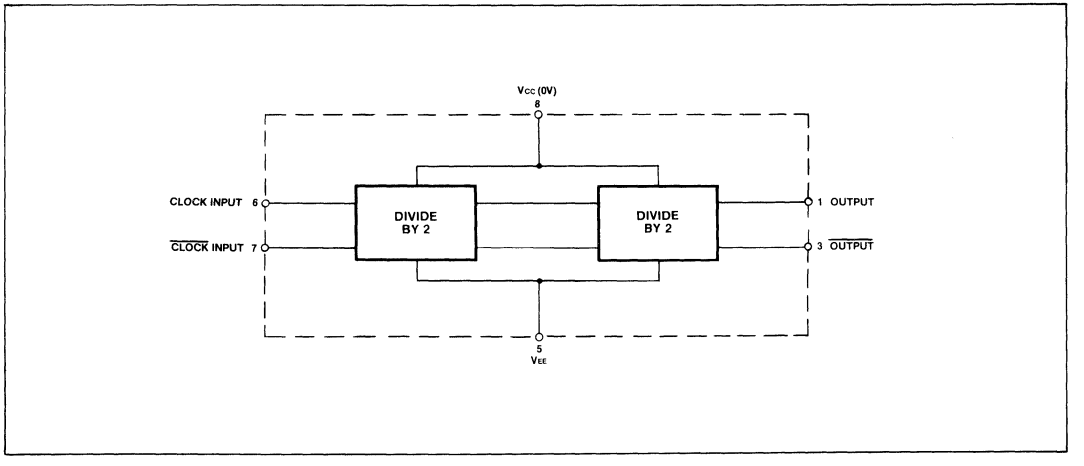
- Open Collector Output
- AC Coupled Input

QUICK REFERENCE DATA

- Supply Voltage: -5.2V
- Power Consumption: 85mW
- Max. Input Frequency: 250MHz
- Temperature Range:
  - -55°C to +125°C (A Grade)
  - -30°C to +70°C (B Grade)

ABSOLUTE MAXIMUM RATINGS

Supply voltage	-10V
Output voltage (Pins 1 and 3)	VEE +14V
Storage temperature range	-55°C to +175°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p

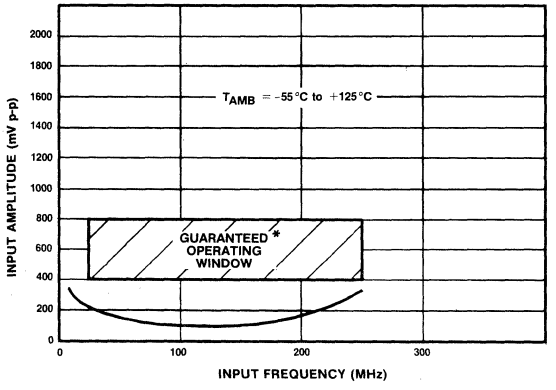


ELECTRICAL CHARACTERISTICS

Supply voltage: V_{EE} = -5.2V ± 0.25V V_{CC} = 0V
Temperature: A Grade T_{amb} = -55°C to +125°C
B Grade T_{amb} = -30°C to +70°C

Characteristic	Symbol	Value		Units	Conditions
		Min.	Max.		
Maximum frequency (sinewave input)	f_{max}	250		MHz	Input = 400-800mV
Minimum frequency (sinewave input)	f_{min}		25	MHz	Input = 400-800mV
Power supply current	I_{EE}		25	mA	V_{EE} = -5.2V
Output current	I_{OUT}	1.65		mA	

NOTES
1. Unless otherwise stated the electrical characteristics are guaranteed over specified supply, frequency and temperature range.
2. The dynamic test circuit is shown in Fig. 5.



*Tested as specified in table of Electrical Characteristics

Fig.3 Typical input characteristics of SP8600A

OPERATING NOTES

1. The input is normally AC coupled to one of the inputs or, if complementary signals are available, to both inputs. The inputs require an external bias as shown in Fig.5.
2. If no signal is present the device will self-oscillate. If this is undesirable this can be prevented by offsetting the two inputs by approximately 40mV as shown in Fig. 6.
3. The outputs are in the form of complementary free collectors with about 2mA available from them over full temperature range. The outputs can be interfaced to ECL or Schottky TTL as shown in Fig. 7.
4. For maximum frequency operation the output load resistor values must be such that the output transistors will not saturate. If the output load resistors are connected to 0V then saturation occurs with resistor values greater than 600 ohms. If only one output is used the other output can be connected to 0V.
5. The input can be operated down to DC but input slew rate must be better than 20V/µs.
6. The input impedance varies as a function of frequency. See Fig. 4.

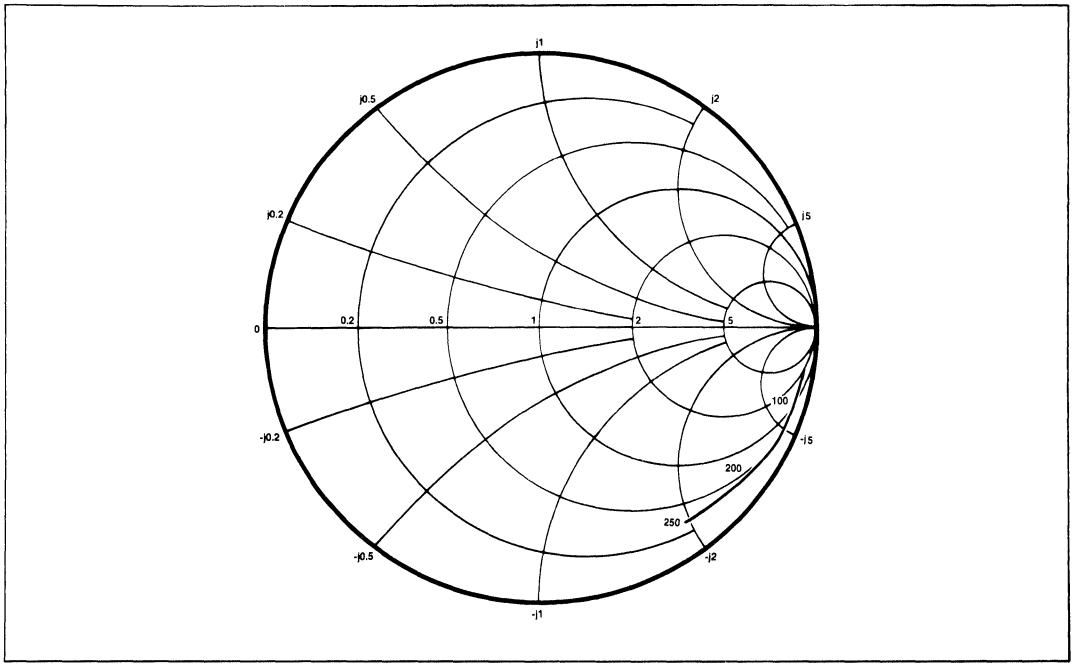


Fig.4 Typical input impedance: supply voltage -5.2V, temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

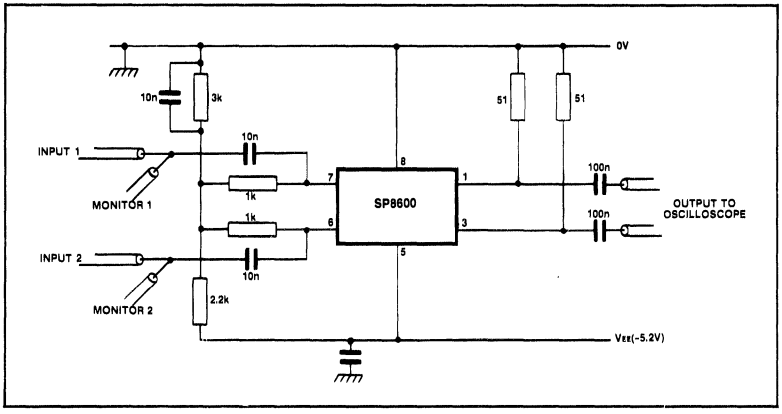


Fig.5 Test circuit

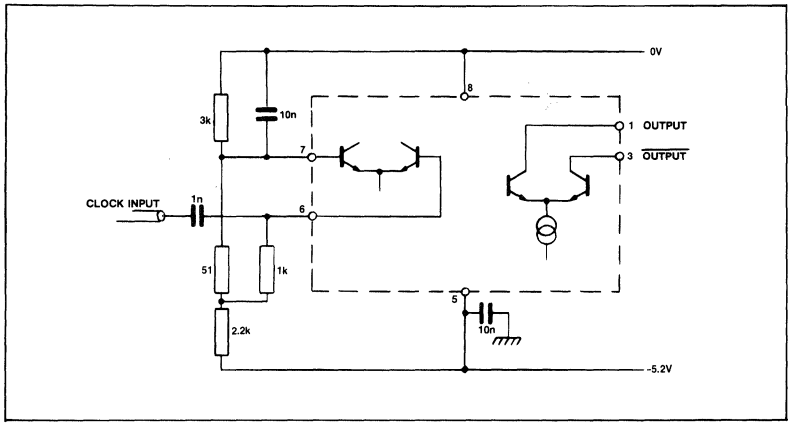


Fig.6 Biasing to prevent oscillation under no signal conditions

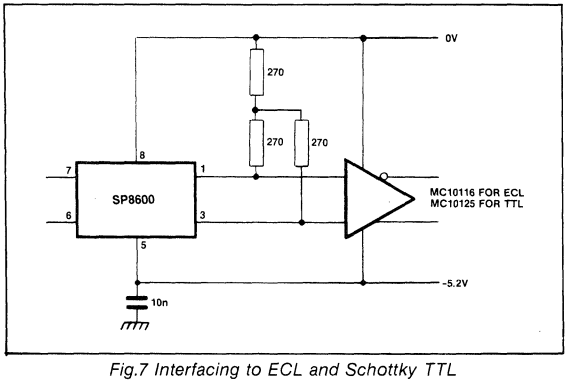


Fig.7 Interfacing to ECL and Schottky TTL

SP8601A & B

150MHz ÷ 4

The SP8601 is an asynchronous ECL counter with a current steered output which can be used to drive TTL or CMOS. Biased externally, it may be directly driven from an ECL II source.

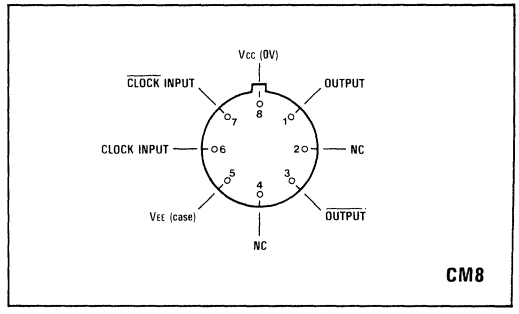


Fig.1 Pin connections - bottom view

FEATURES

- Current steered output can drive TTL or CMOS
- AC or DC Coupled Input
- Inputs ECL II Compatible

QUICK REFERENCE DATA

- Supply Voltage: -5.2V
- Power Consumption: 85mW
- Temperature Range:
  -55°C to +125°C (A Grade)
  -30°C to +70°C (B Grade)

ABSOLUTE MAXIMUM RATINGS

Supply voltage	-10V
Output voltage (Pins 1 and 3)	VEE +14V
Storage temperature range	-55°C to +150°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p

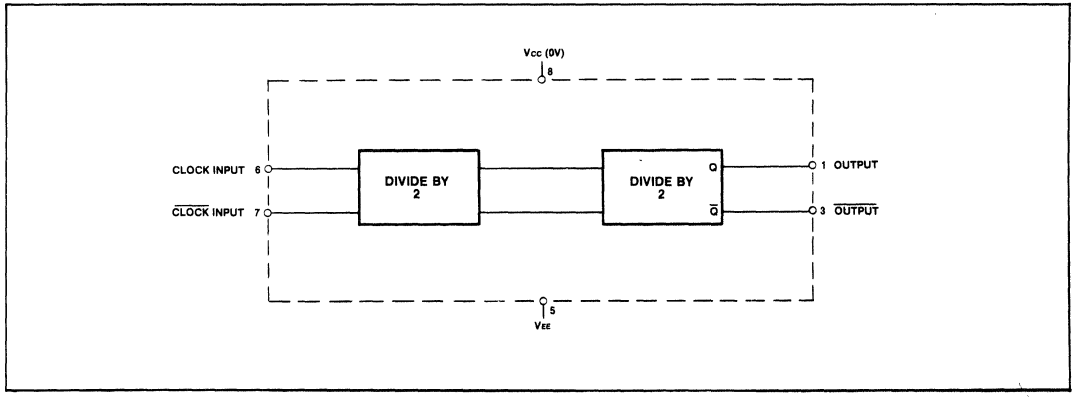


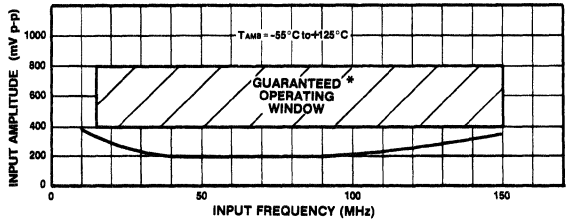
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply voltage: V_{CC} = 0V, V_{EE} = -5.2V ± 0.25V
Temperature: A Grade T_{amb} = -55°C to +125°C
B Grade T_{amb} = -30°C to +70°C

Characteristics	Symbol	Value		Units	Conditions
		Min.	Max.		
Maximum frequency (sinewave input)	f_{max}	150		MHz	Input = 400-800mV p-p
Minimum frequency (sinewave input)	f_{min}		15	MHz	Input = 400-800mV p-p
Power supply current	I_{EE}		25	mA	V_{EE} = -5.2V
Output current	I_{OUT}	1.6		mA	

NOTES
1. Unless otherwise stated the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The test configuration for dynamic testing is shown in Fig. 5.



*Tested as specified in table of Electrical Characteristics

Fig.3 Typical characteristic of SP8601A

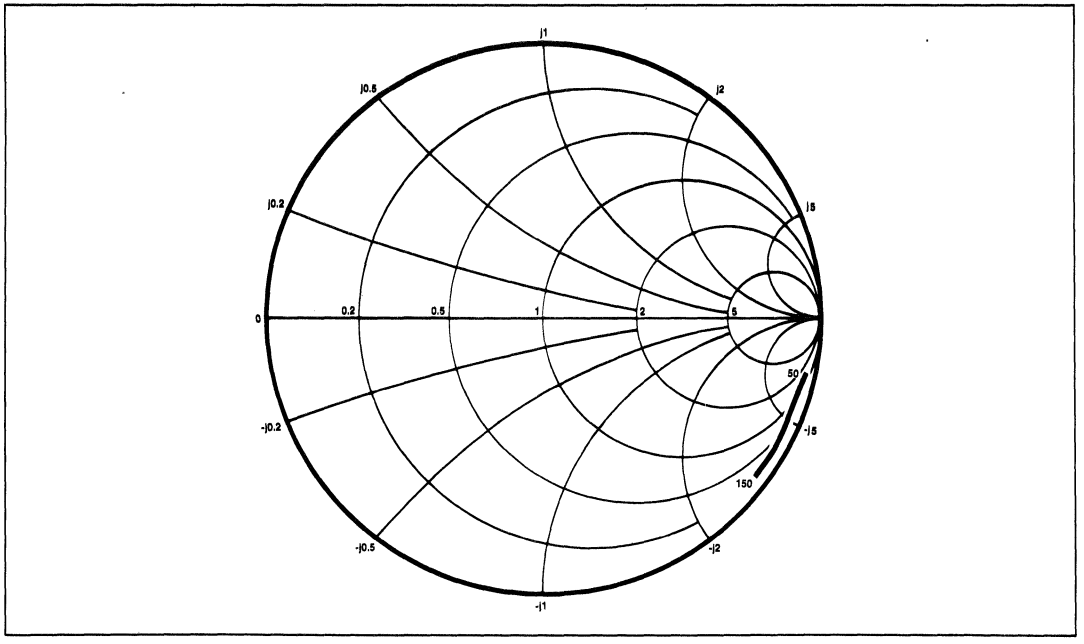


Fig.4 Typical input impedance. Test conditions: supply voltage -5.2V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

OPERATING NOTES

1. The signal source can be capacitively coupled to the clock input if input bias is provided (See Fig.6) but is normally directly coupled with ECL II levels. The inputs can be operated either singly or with double complementary input drive.
2. The outputs are in the form of complementary free collectors with 1.6mA available from them over full military temperature range (A grade). The outputs can be interfaced to ECL or Schottky TTL as shown in Figs. 6 and 7. Interfacing to TTL at frequencies above 20MHz requires low capacitance interconnections and the use of Schottky TTL.
3. For maximum frequency operation the output load resistor values must be such that the output transistors will not saturate. If the output load resistors are connected to 0V then saturation will occur with resistor values greater than 600Ω. If only one output is used the other output can be connected to 0V. See Table 1 for typical variation of maximum input frequency with output load resistor.

Minimum Output Voltage (mV)	Load Resistor (ohms)	Input Frequency (MHz)
1100	1000	120
320	200	150
80	50	180

Table 1

4. Input impedance is a function of frequency. See Fig.4.
5. The input can be operated down to DC but input slew rate must be better than 20V/μs.
6. All components should be suitable for the frequency in use.

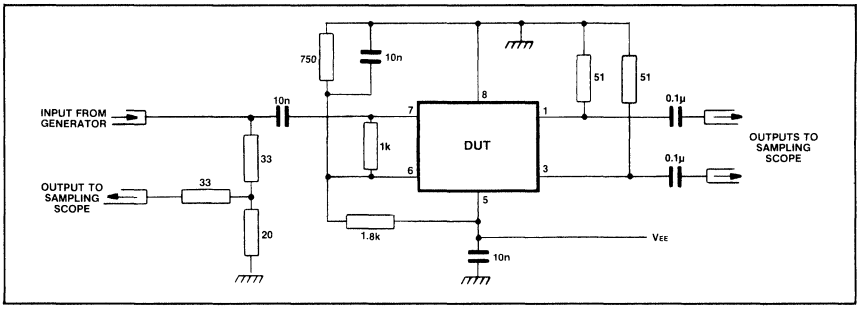


Fig.5 Test circuit

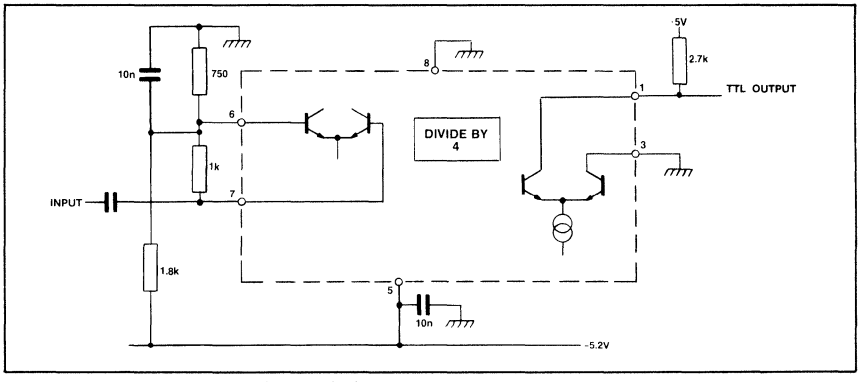


Fig.6 Typical application showing interfacing

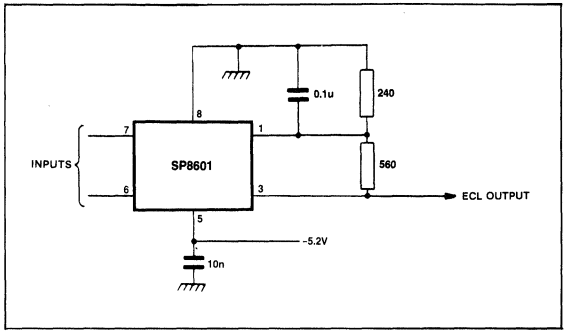


Fig.7 Interfacing to ECL

SP8602A & B 500MHz ÷ 2
SP8604A & B 300MHz ÷ 2

The SP8602 and SP8604 are emitter coupled logic dividers which feature ECL 10K compatible outputs when used with external pulldown resistors. The inputs are AC coupled.

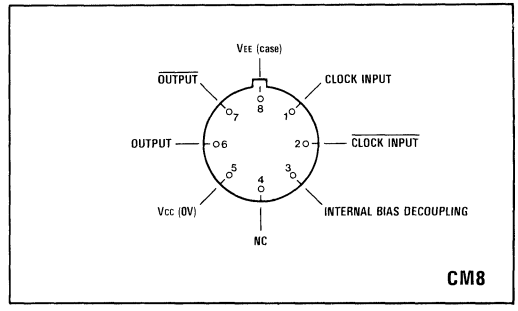


Fig.1 Pin connections - bottom view

FEATURES

- ECL Compatible Outputs
- AC Coupled Inputs (Internal Bias)

QUICK REFERENCE DATA

- Supply Voltage: -5.2V
- Power Consumption: 85mW
- Temperature Range:
  - -55°C to +125°C (A Grade)
  - -30°C to +70°C (B Grade)

ABSOLUTE MAXIMUM RATINGS

Supply voltage	-8V
Output current	10mA
Storage temperature range	-55°C to +175°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p

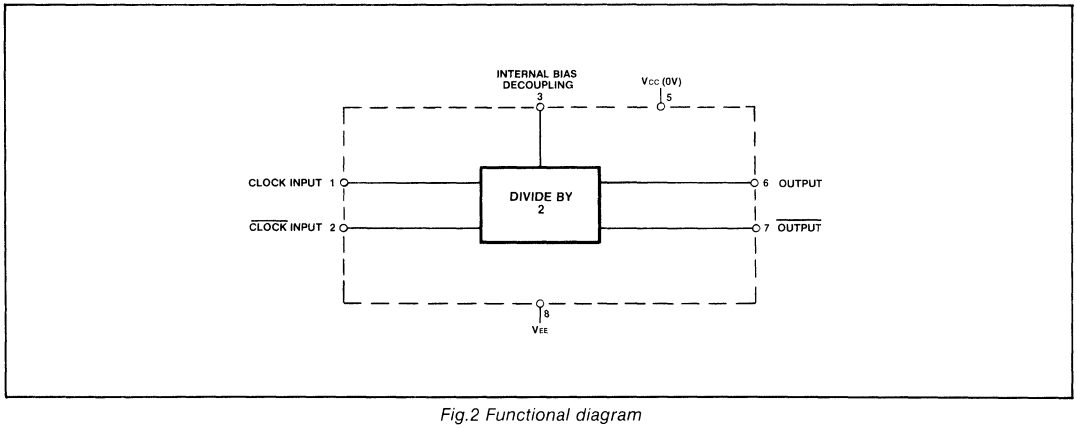


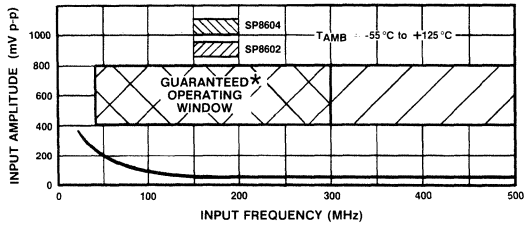
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply voltage: V_{CC} = 0V, V_{EE} = -5.2V ± 0.25V
Temperature: T_{amb} A Grade = -55°C to +125°C
B Grade = -30°C to +70°C

Characteristics	Symbol	Value Min.	Value Max.	Units	Grade	Conditions	Notes
Maximum frequency (sinewave input)	f_{max}	500		MHz	SP8602	Input = 400-800mV p-p	
		300		MHz	SP8604		
Minimum frequency (sinewave input)	f_{min}		40	MHz	All	Input = 400-800mV p-p	
Power supply current	I_{EE}		18	mA	All	V_{EE} = 5.2V Outputs unloaded	
Output low voltage	V_{OL}	-1.8	-1.4	V	All	V_{EE} = -5.2V	Note 4
Output high voltage	V_{OH}	-0.85	-0.7	V	All	V_{EE} = -5.2V	Note 4
Minimum output swing	V_{OUT}	400		mV	All	V_{EE} = -5.2V	

NOTES
1. Unless otherwise stated the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The temperature coefficients of V_{OH} = +1.63mV/°C and V_{OL} = +0.34mV/°C but these are not tested.
3. The test configuration for dynamic testing is shown in Fig.5.
4. Tested at 25°C only.



*Tested as specified in table of Electrical Characteristics

Fig.3 Typical characteristic of SP8602 and SP8604

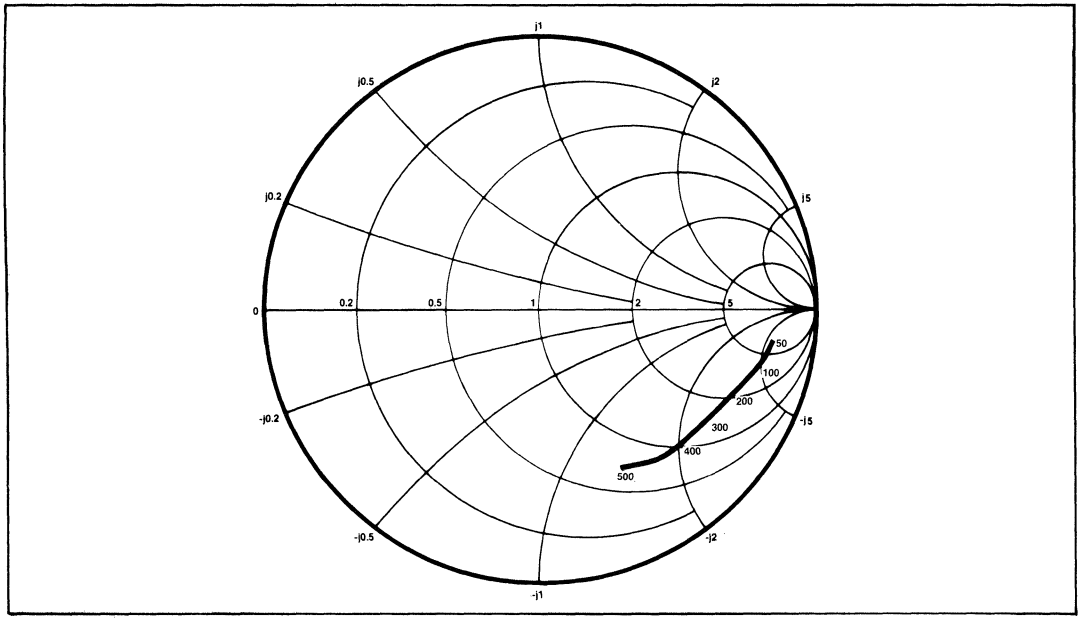


Fig.4 Typical input impedance. Test conditions: supply voltage -5.2V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

OPERATING NOTES

1. The clock inputs (pins 1 and 2) can be driven single-ended or differentially and should be capacitively coupled to the signal source. The input signal path is completed by connecting a capacitor from the internal bias decoupling, pin 3, to ground.
2. In the absence of a signal the device will self-oscillate. If this is undesirable it may be prevented by connecting a 15k resistor from the unused input to V_{EE} (ie pin 1 or 2 to pin 8). This causes a drop in sensitivity of about 100mV.
3. The circuit will operate down to DC but slew rate must be better than 100V/µs.
4. The outputs are compatible with ECL II. There is an internal load of 4k on each output. The outputs can be interfaced to ECL 10K by addition of a pulldown resistor of 1.5k from the outputs to V_{EE} to increase output voltage swing.
5. Input impedance is a function of frequency. See Fig. 4.
6. All components should be suitable for the frequency in use.

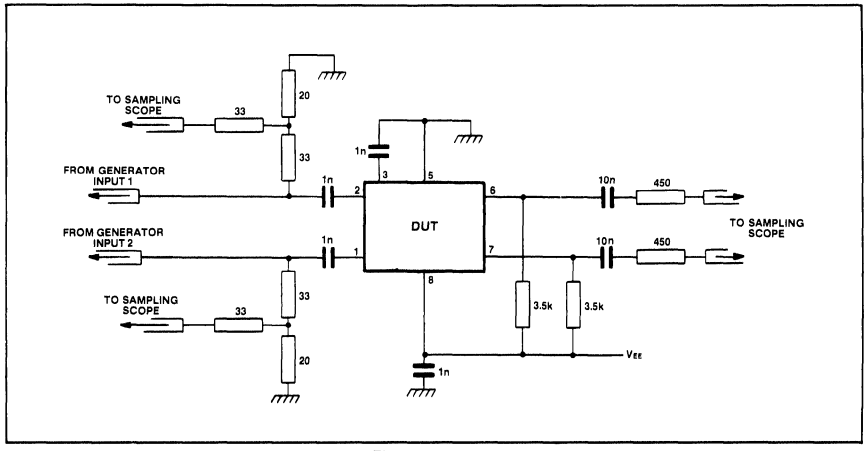


Fig.5 Test circuit

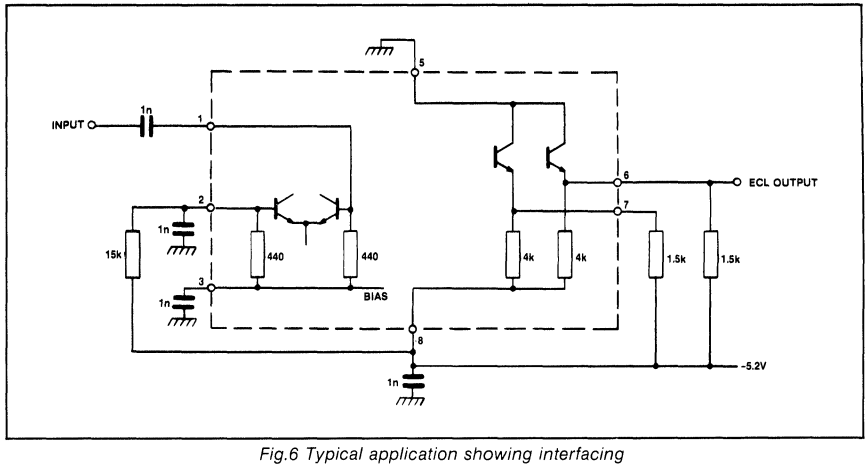


Fig.6 Typical application showing interfacing

SP8605A & B 1000MHz ÷ 2
SP8606A & B 1300MHz ÷ 2

The SP8605 and SP8606 are emitter coupled logic dividers with ECL III compatible outputs. Specified from -55°C to +125°C (A Grade), these devices feature AC coupled inputs and 600mV p-p clock input sensitivity.

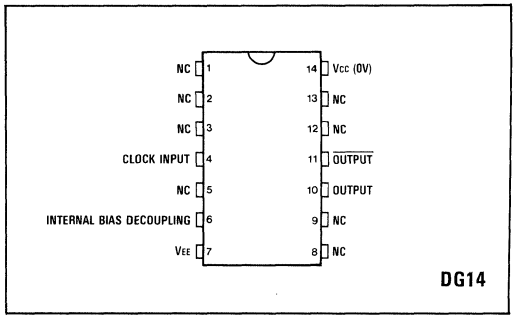


Fig.1 Pin connections - top view

FEATURES

- ECL Compatible Outputs
- AC Coupled Inputs (Internal Bias)

QUICK REFERENCE DATA

- Supply Voltage: -5.2V
- Power Consumption: 320mW
- Max. Input Frequency: 1300MHz (SP8606)
- Temperature Range:
  A Grade: -55°C to +110°C
  (125°C with suitable heat sink)
  B Grade: 0°C to +70°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage	-8V
Output current	15mA
Storage temperature range	-55°C to +150°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p

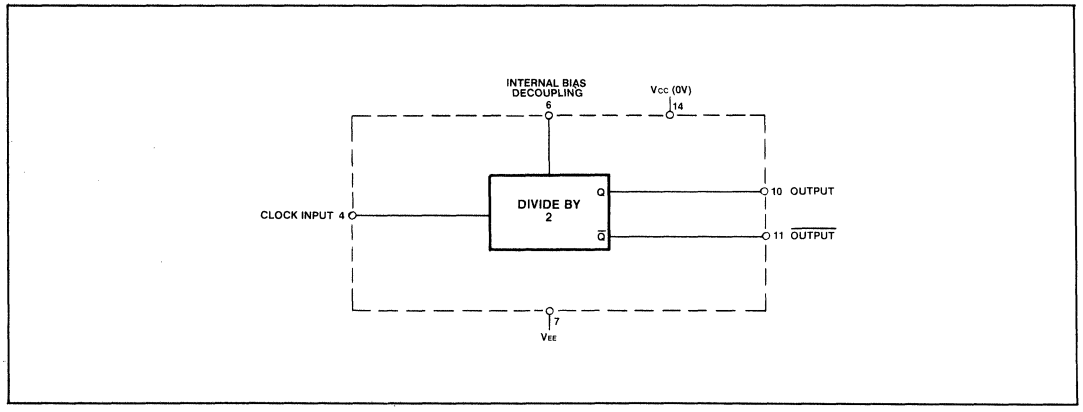


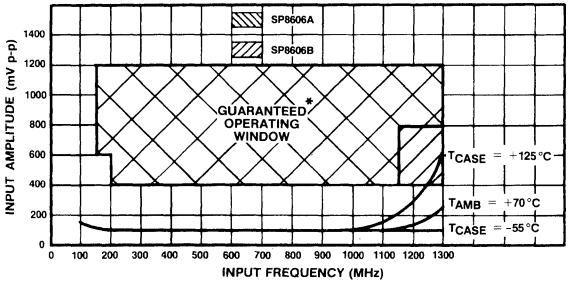
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply voltage: V_{CC} = 0V, V_{EE} = -5.2V ± 0.25V
Temperature: A Grade T_{case} = -55°C to +125°C (Note 2)
B Grade T_{amb} = 0°C to +70°C

Characteristics	Symbol	Value		Units	Grade	Conditions	Notes
		Min.	Max.				
Maximum frequency	f_{max}	1.0		GHz	SP8605A,B	Input = 400-1200mV p-p	Note 7
(sinewave input)		1.3		GHz	SP8606A	Input = 800-1200mV p-p	Note 7
		1.3		GHz	SP8606B	Input = 400-1200mV p-p	Note 7
Minimum frequency	f_{min}		150	MHz	All	Input = 600-1200mV p-p	Note 5
(sinewave input)							
Current consumption	I_{EE}		100	mA	All	V_{EE} = -5.45V Outputs unloaded	Note 6
Output low voltage	V_{OL}	-1.92	-1.62	V	All	V_{EE} = -5.2V Outputs loaded with 430Ω(25° C)	
Output high voltage	V_{OH}	-0.93	-0.75	V	All	V_{EE} = -5.2V Outputs loaded with 430Ω(25° C)	
Minimum output swing	V_{OUT}	500		mV	All	V_{EE} = -5.2V Outputs loaded with 430 ohms	Note 6

NOTES
1. Unless otherwise stated the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The A grade devices must be used with a heat sink to maintain chip temperature below +175°C when operating in an ambient of +125°C.
3. The temperature coefficients of V_{OH} = +1.2mV/°C and V_{OL} = +0.24mV/°C but these are not tested.
4. The test configuration for dynamic testing is shown in Fig.5.
5. Tested at 25°C and +125°C only (+70°C for B grade).
6. Tested at 25°C only.
7. Tested at +125°C only (+70°C for B grade).



*Tested as specified in table of Electrical Characteristics

Fig.3 Typical characteristic of SP8606

THERMAL CHARACTERISTICS

θ_{JC} approximately 30°C/W
θ_{JA} approximately 110°C/W

OPERATING NOTES

1. The clock inputs (pin 4) should be capacitively coupled to the signal source. The input signal path is completed by connecting a capacitor from the internal bias decoupling, pin 6, to ground.
2. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 10k resistor from the unused input to V_{EE} (ie pin 4 to pin 7). This reduces sensitivity by approximately 100mV.
3. The input can be operated at very low frequencies but slew rate must be better than 200V/µs.
4. The input impedance of the SP8605/6 is a function of frequency. See Fig. 4.
5. The emitter follower outputs require external load resistors. These should not be less than 330 ohms, and a value of 430 ohms is recommended. Interfacing to ECL III/10K is shown in Fig. 7.
6. These devices may be used with split supply lines and earth referenced input using the circuit shown in Fig. 6.
7. All components should be suitable for the frequency in use.

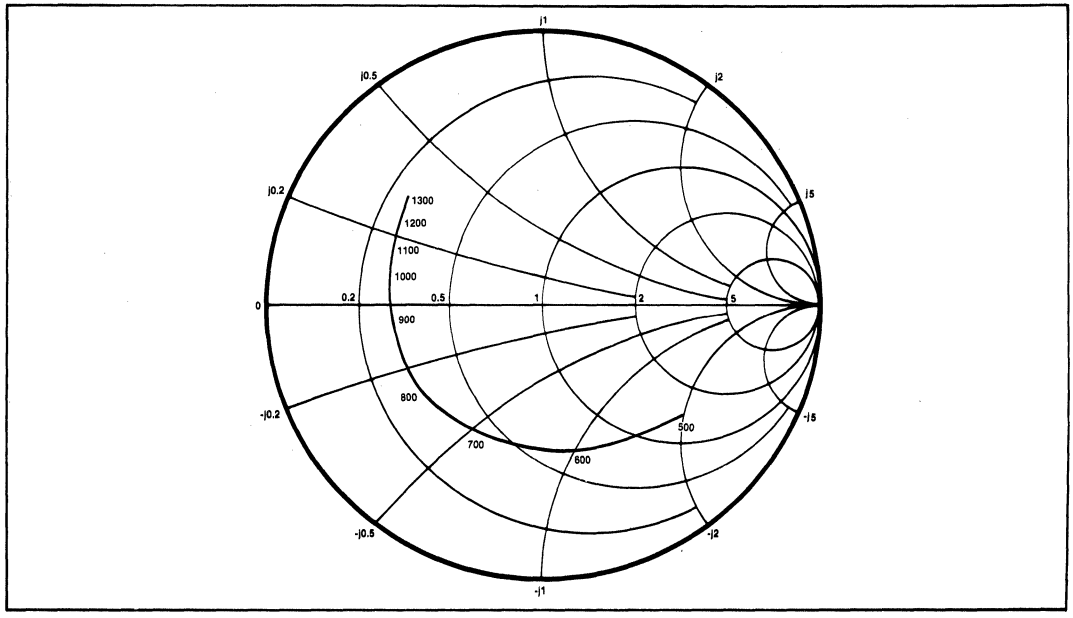


Fig.4 Typical input impedance. Test conditions: supply voltage -5.2V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

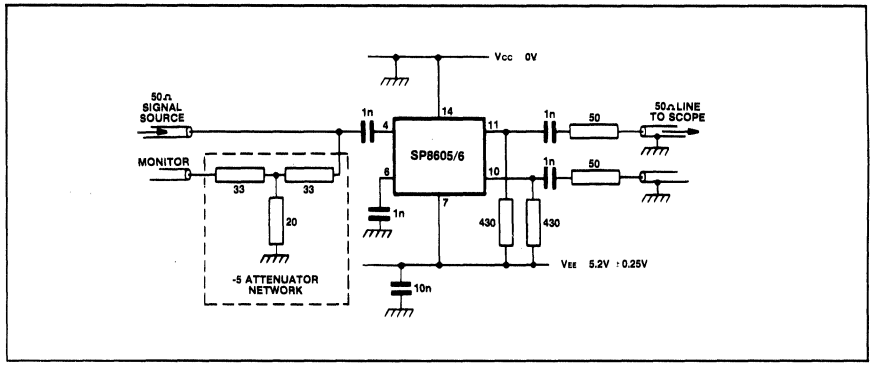


Fig.5 Toggle frequency test circuit

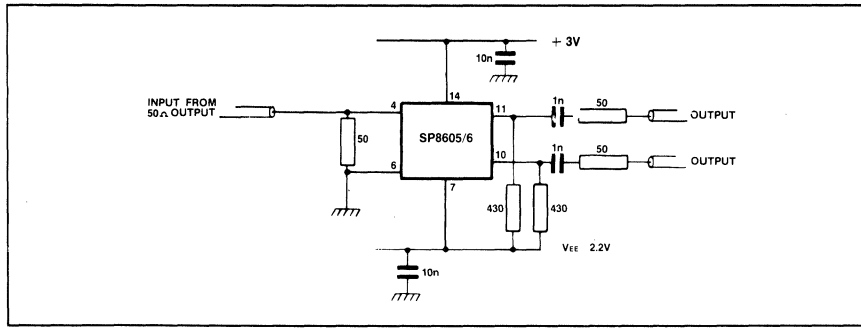


Fig.6 Circuit for using the input signal about ground potential

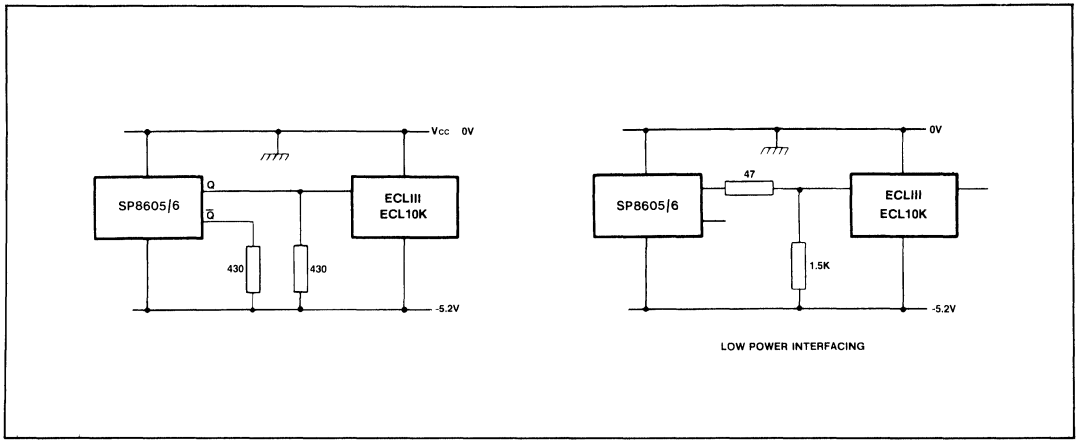


Fig.7 Interfacing SP8605/6 to ECL 10K and ECL III

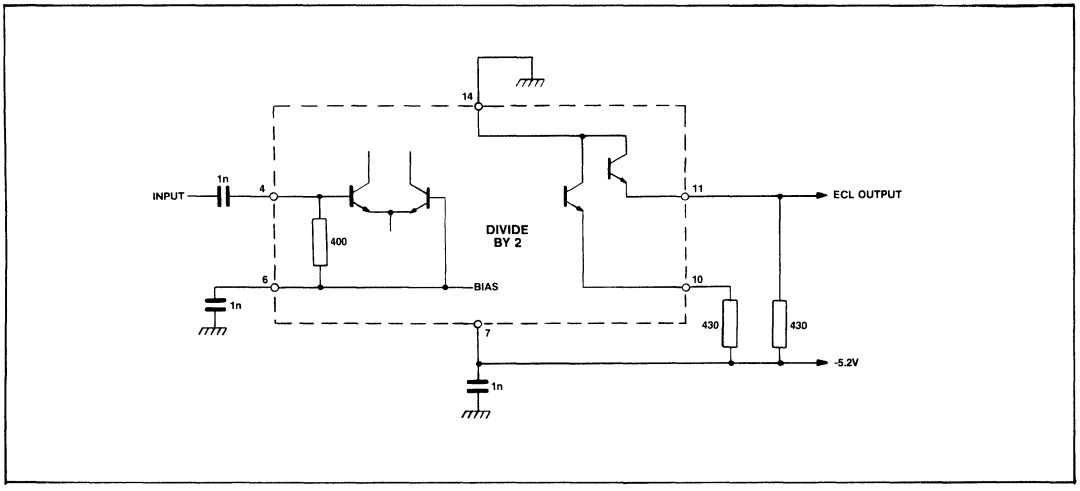


Fig.8 Typical application showing interfacing

SP8607A & B

600MHz ÷ 2

The SP8607 is an emitter coupled logic divider which features ECL 10K compatible outputs when used with external pulldown resistors. The inputs are AC coupled.

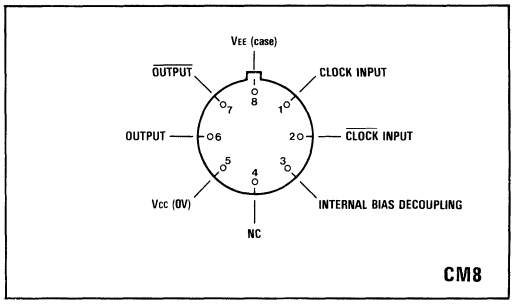


Fig.1 Pin connections - bottom view

FEATURES

- ECL Compatible Outputs
- AC Coupled Inputs (Internal Bias)

QUICK REFERENCE DATA

- Supply Voltage: -5.2V
- Power Consumption: 80mW
- Temperature Range:
  - -55°C to +125°C (A Grade)
  - -30°C to +70°C (B Grade)

ABSOLUTE MAXIMUM RATINGS

Supply voltage	-8V
Output current	10mA
Storage temperature range	-55°C to +150°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p

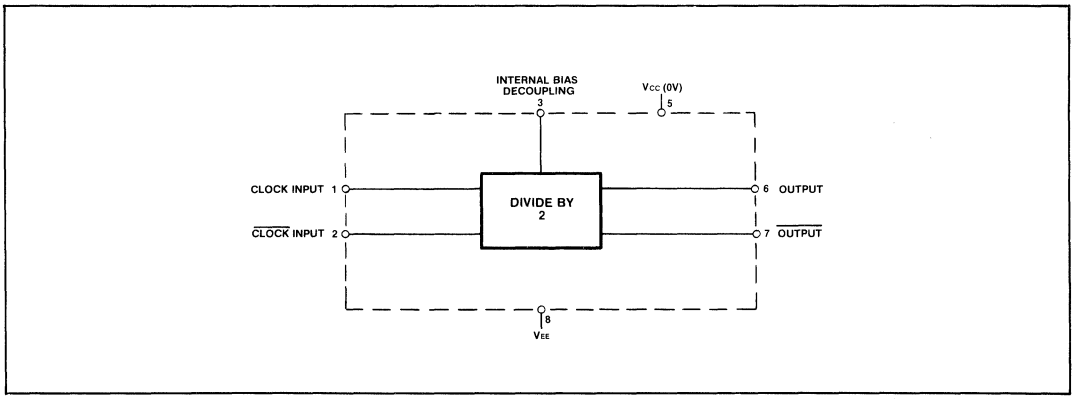


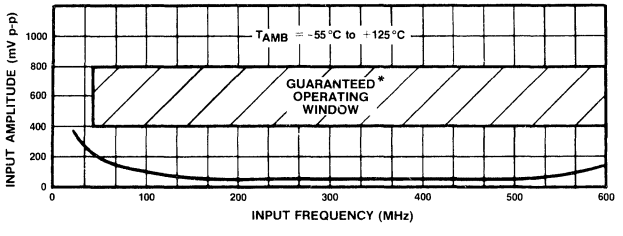
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply voltage: V_{CC} = 0V, V_{EE} = -5.2V ± 0.25V
Temperature: T_{amb} A Grade = -55°C to +125°C
B Grade = -30°C to +70°C

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{max}	600		MHz	Input = 400-800mV p-p	
Minimum frequency (sinewave input)	f_{min}		40	MHz	Input = 400-800mV p-p	
Power supply current	I_{EE}		18	mA	V_{EE} = -5.2V Outputs unloaded	
Output low voltage	V_{OL}	-1.8	-1.4	V	V_{EE} = -5.2V	Note 4
Output high voltage	V_{OH}	-0.85	-0.7	V	V_{EE} = -5.2V	Note 4
Minimum output swing	V_{OUT}	400		mV	V_{EE} = -5.2V	

NOTES
1. Unless otherwise stated the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The temperature coefficients of V_{OH} = +1.63mV/°C and V_{OL} = +0.34mV/°C but these are not tested.
3. The test configuration for dynamic testing is shown in Fig.5.
4. Tested at 25°C only.



*Tested as specified in table of Electrical Characteristics

Fig.3 Typical characteristic of SP8607A

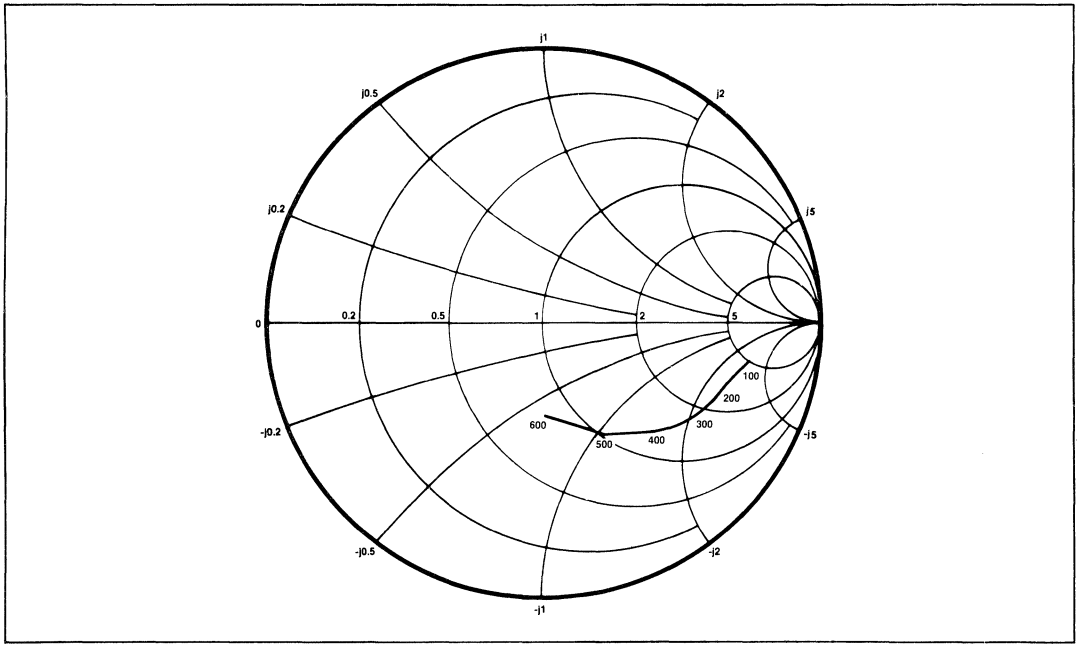


Fig.4 Typical input impedance. Test conditions: supply voltage -5.2V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

OPERATING NOTES

1. The clock inputs (pins 1 and 2) can be driven single-ended or differentially and should be capacitively coupled to the signal source. The input signal path is completed by connecting a capacitor from the internal bias decoupling, pin 3, to ground.
2. In the absence of a signal the device will self-oscillate. If this is undesirable it may be prevented by connecting a 15k resistor from the unused input to V_{EE} (ie pin 1 or 2 to pin 8). This causes a drop in sensitivity of about 100mV.
3. The circuit will operate down to DC but slew rate must be better than 100V/µs.
4. The outputs are compatible with ECL II. There is an internal load of 4k on each output. The outputs can be interfaced to ECL 10K by addition of a pulldown resistor of 1.5k to the outputs to increase the output voltage swing.
5. Input impedance is a function of frequency. See Fig. 4.
6. All components should be suitable for the frequency in use.

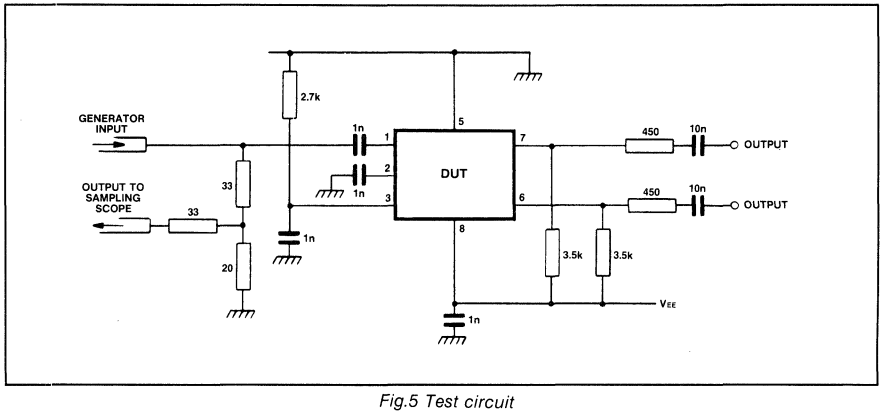


Fig.5 Test circuit

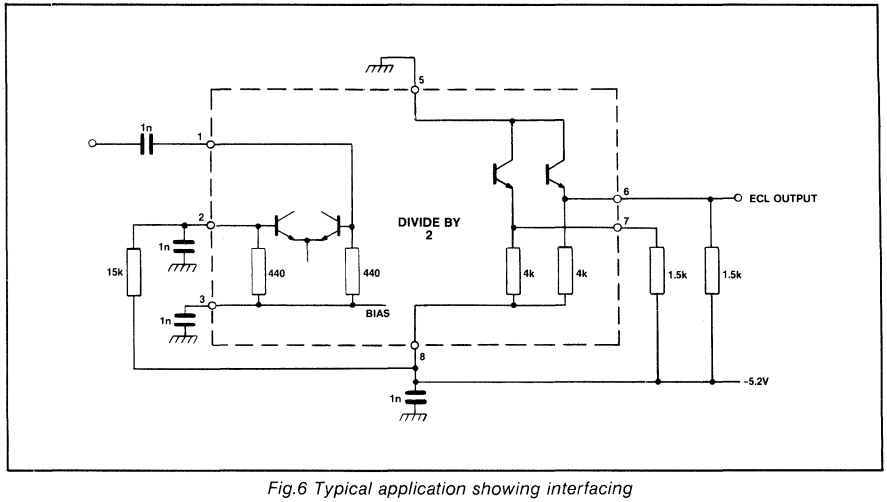


Fig.6 Typical application showing interfacing

SP8610A & B 1000MHz ÷ 4
SP8611A & B 1300/1500MHz ÷ 4

The SP8610/11 are asynchronous ECL divide by four circuits, with ECL compatible outputs which can also be used to drive 100 ohm lines. They feature input sensitivities of 600mV p-p (800mV p-p above 1300MHz).

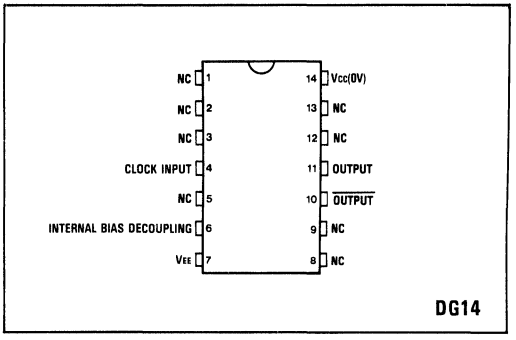


Fig.1 Pin connections - top view

FEATURES

- ECL Compatible Outputs
- AC Coupled Input (internal bias)

QUICK REFERENCE DATA

- Supply Voltage: -5.2V
- Power Consumption: 380mW
- Max. Input Frequency: 1500MHz (SP8611B)
- Temperature Range:
  A Grade: -55°C to +110°C
  (125°C with suitable heat sink)
  B Grade: 0°C to +125°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage	-8V
Output current	15mA
Storage temperature range	-55°C to +150°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p

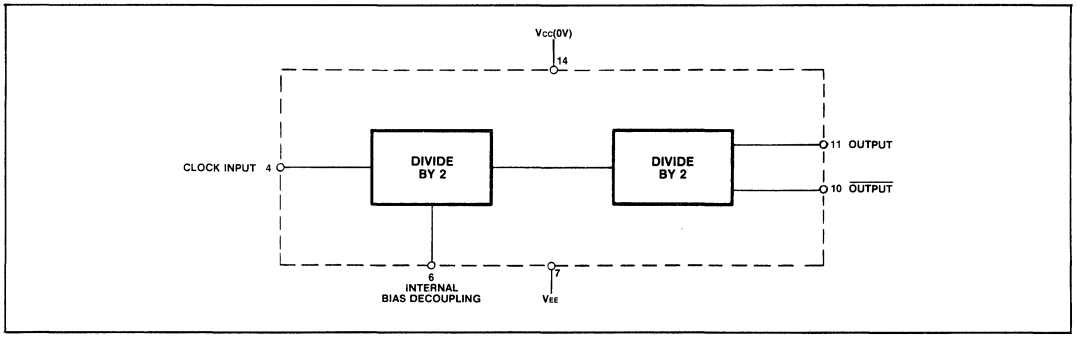


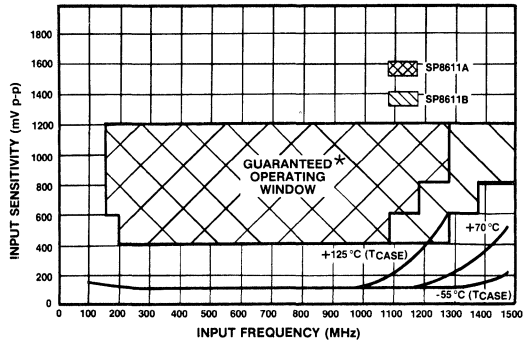
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply voltage: V_{CC} = 0V V_{EE} = -5.2V ± 0.25V
Temperature: T_{CASE} (A grade) = -55°C to +125°C (Note 2)
T_{amb} (B grade) = 0°C to +70°C

Characteristic	Symbol	Value		Units	Grade	Conditions	Note
		Min.	Max.				
Maximum frequency	f_{max}	1.0		GHz	SP8610A,B	Input = 400-1200mV	Note 5
		1.3		GHz	SP8611A	Input = 800-1200mV	Note 7
		1.5		GHz	SP8611B	Input = 800-1200mV	Note 7
Minimum frequency	f_{min}		150	MHz	All	Input = 600-1200mV	Note 5
Current consumption	I_{EE}		100	mA	All	V_{EE} = -5.45V Outputs unloaded	Note 6
Output low voltage	V_{OL}	-1.92	-1.62	V	All	V_{EE} = -5.2V outputs loaded with 430Ω(25°C)	
Output high voltage	V_{OH}	-0.93	-0.75	V	All	V_{EE} = -5.2V outputs loaded with 430Ω(25°C)	
Minimum output swing	V_{OUT}	500		mV	All	V_{EE} = -5.2V outputs loaded with 430Ω	Note 6

NOTES
1. Unless otherwise stated the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The A grade devices must be used with a heat sink to maintain chip temperature below +175°C when operating in an ambient of +125°C.
3. The temperature coefficients of V_{OH} = +1.2mV/°C and V_{OL} = +0.24mV/°C but these are not tested.
4. The test configuration for dynamic testing is shown in Fig.5.
5. Tested at 25°C and +125°C only (+70°C for B grade).
6. Tested at 25°C only.
7. Tested at +125°C only (+70°C for B grade).



*Tested as specified in table of Electrical Characteristics

Fig.3 Typical input characteristics

THERMAL CHARACTERISTICS

θ_{JC} approximately 30°C/W
θ_{JA} approximately 110°C/W

OPERATING NOTES

1. The clock input (pin 4) should be capacitively coupled to the signal source. The input signal path is completed by connecting a capacitor from the internal bias decoupling, pin 6 to ground.
2. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 10k resistor from the input to V_{EE} (i.e. Pin 4 to Pin 7). This reduces sensitivity by approximately 100mV.
3. The input can be operated at very low frequencies but slew rate must be better than 200V/µs.
4. The input impedance of the SP8610/11 is a function of frequency. See Fig. 4.
5. The emitter follower outputs require external load resistors. These should not be less than 330 ohms, and a value of 430 ohms is recommended. Interfacing to ECL III/10K is shown in Fig. 7.
6. These devices may be used with split supply lines and ground referenced input by means of the circuit of Fig. 6.

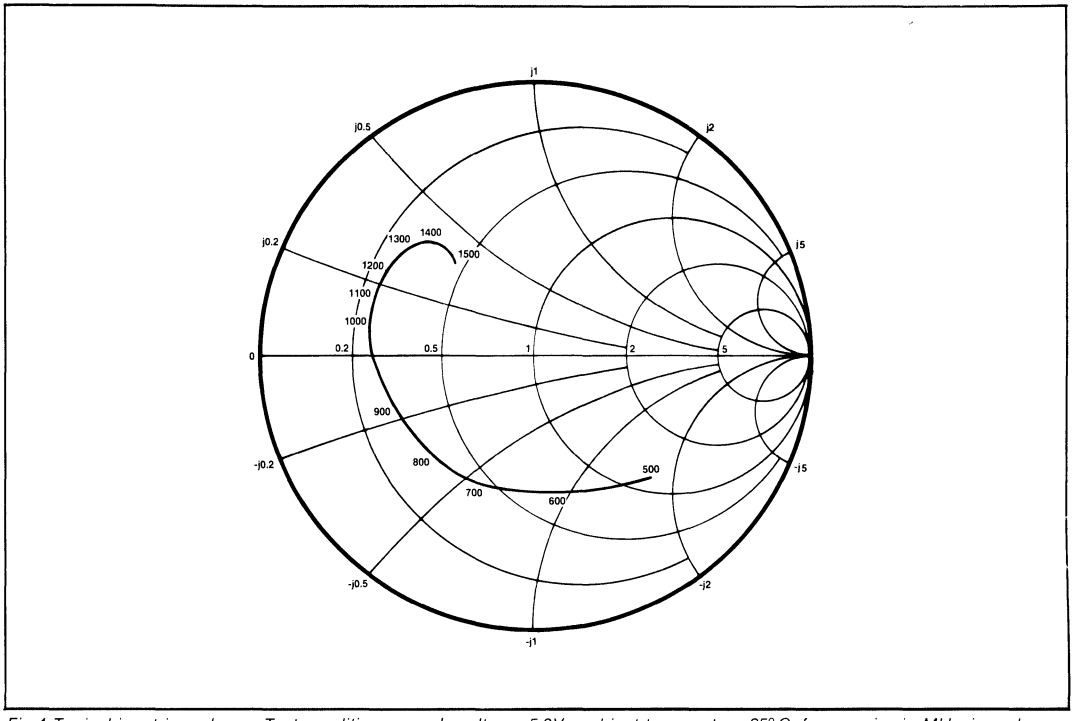


Fig.4 Typical input impedance. Test conditions: supply voltage -5.2V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

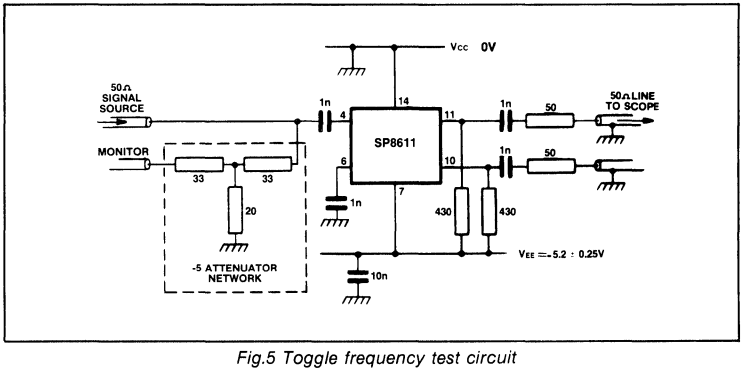


Fig.5 Toggle frequency test circuit

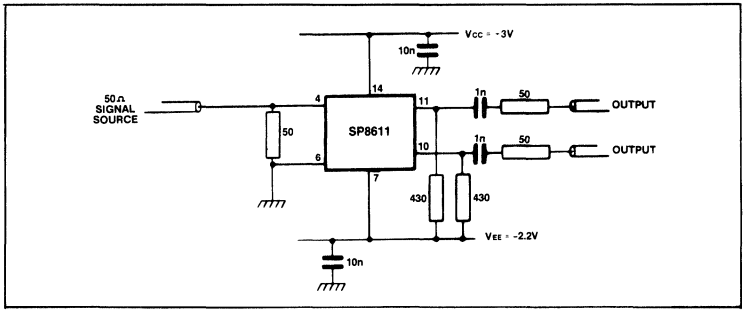


Fig.6 Circuit for using the input signal about earth potential

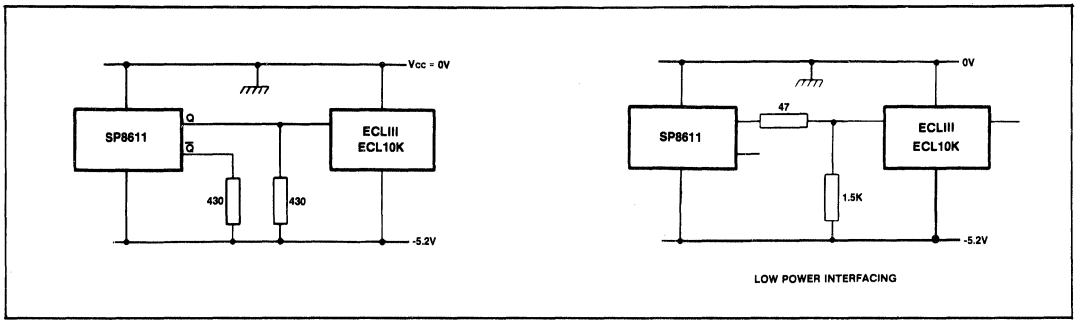


Fig.7 Interfacing SP8611 series to ECL 10K and ECL III

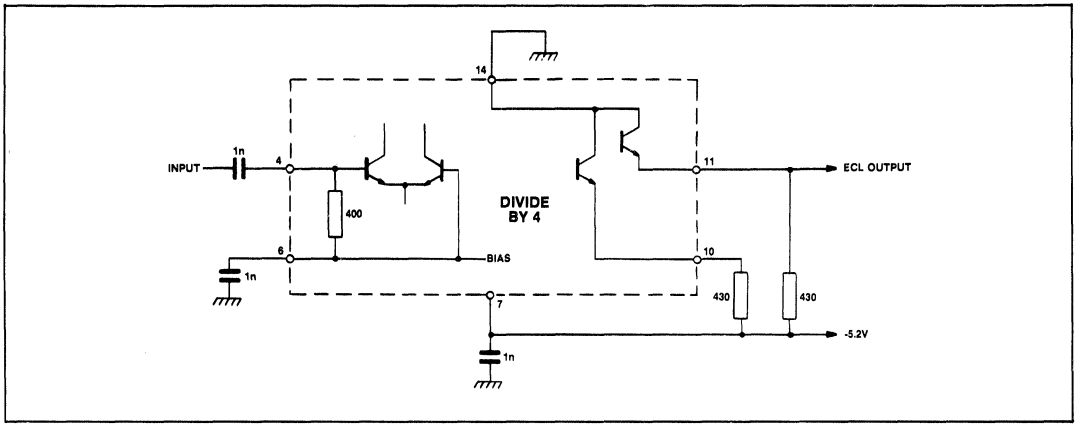


Fig.8 Typical application showing interfacing

SP8620A & B

400MHz ÷ 5

The SP8620 is an asynchronous emitter coupled logic counter which provides an ECL compatible output when an external pulldown resistor is added. It requires an AC coupled input of 600mV p-p.

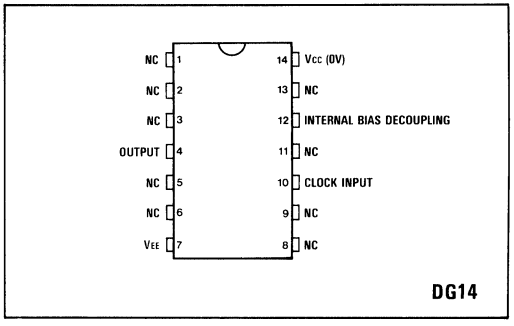


Fig.1 Pin connections - top view

FEATURES

- ECL Compatible Output
- AC Coupled Inputs (Internal Bias)

QUICK REFERENCE DATA

- Supply Voltage: -5.2V
- Power Consumption: 285mW
- Temperature Range:
  - -55°C to +125°C (A Grade)
  - -30°C to +70°C (B Grade)

ABSOLUTE MAXIMUM RATINGS

Supply voltage	-8V
Output current	15mA
Storage temperature range	-55°C to +150°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p

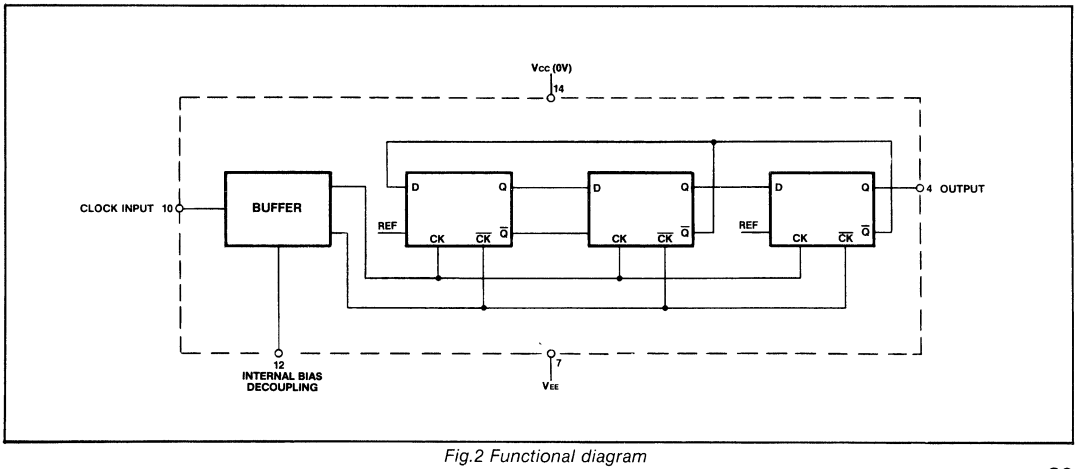


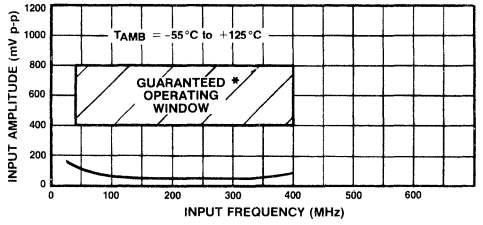
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply voltage: V_{CC} = 0V, V_{EE} = -5.2V ± 0.25V
Temperature: A Grade T_{amb} = -55°C to +125°C
B Grade T_{amb} = -30°C to +70°C

Characteristics	Symbol	Value Min.	Value Max.	Units	Conditions	Note
Maximum frequency (sinewave input)	f_{max}	400		MHz	Input = 400-800mV p-p	
Minimum frequency (sinewave input)	f_{min}		40	MHz	Input = 400-800mV p-p	Note 4
Power supply current	I_{EE}		55	mA	V_{EE} = -5.2V	Note 4
Output low voltage	V_{OL}	-1.8	-1.5	V	V_{EE} = -5.2V (25°C)	
Output high voltage	V_{OH}	-0.85	-0.7	V	V_{EE} = -5.2V (25°C)	
Minimum output swing	V_{OUT}	400		mV	V_{EE} = -5.2V	

NOTES
1. Unless otherwise stated the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The temperature coefficients of V_{OH} = +1.63mV/°C and V_{OL} = +0.94mV/°C but these are not tested.
3. The test configuration for dynamic testing is shown in Fig.5.
4. Tested at 25°C only.



*Tested as specified in table of Electrical Characteristics

Fig.3 Typical input characteristic of SP8620A

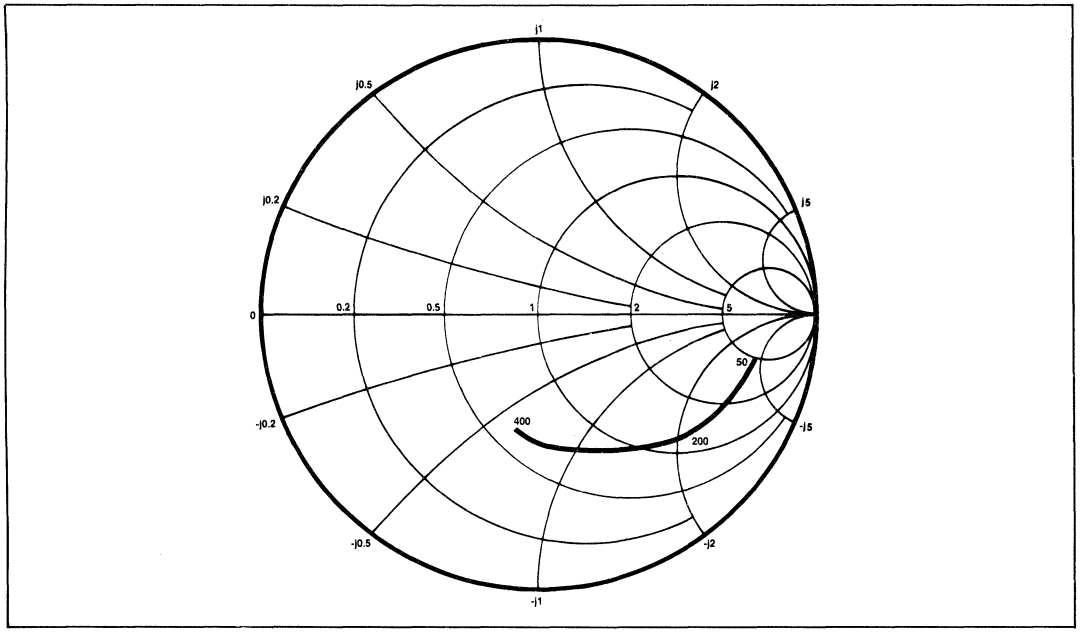


Fig.4 Typical input impedance. Test conditions: supply voltage -5.2V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

OPERATING NOTES

1. The clock input (pin 10) should be capacitively coupled to the signal source. The input signal path is completed by connecting a capacitor from the internal bias decoupling, pin 12, to ground.
2. The circuit will operate down to DC but slew rate must be better than 100V/μs.
3. The outputs are compatible with ECL II. There is an internal load of 3k at the output. The output can be interfaced to ECL/10K by the addition of 1.5k to the output to increase the output voltage swing.
4. Input impedance is a function of frequency. See Fig.4.
5. All components should be suitable for the frequency in use.

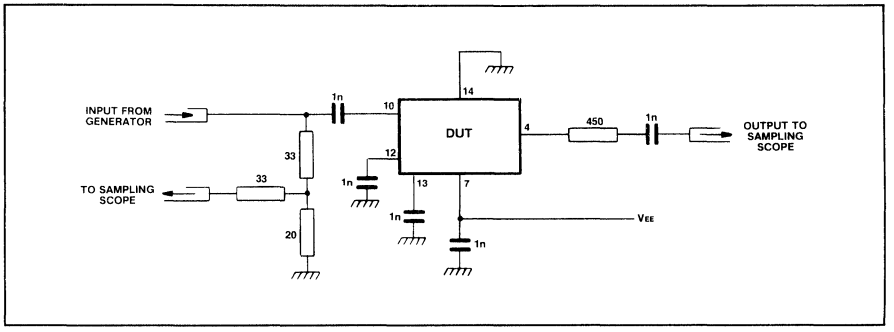


Fig.5 Test circuit

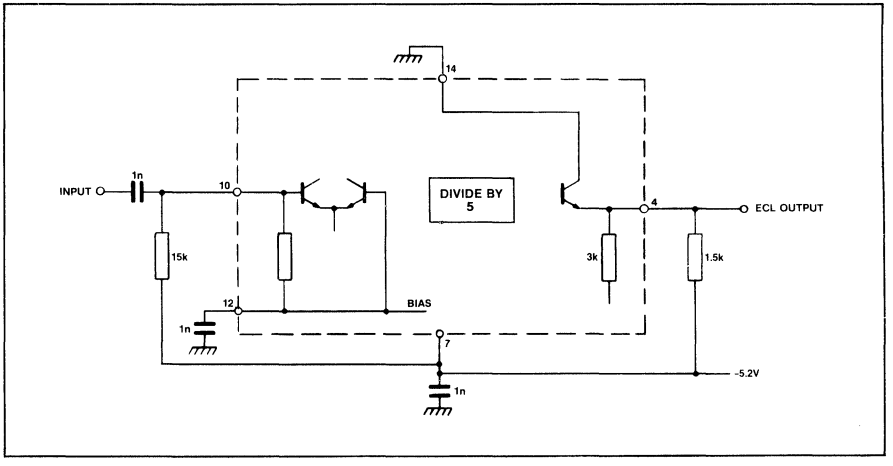


Fig.6 Typical application showing interfacing

SP8629

150MHz ÷ 100

The SP8629 is an ECL counter which provides a TTL compatible output, high input sensitivity and low power consumption. Pin compatible with DM8629, it features a much lower power consumption.

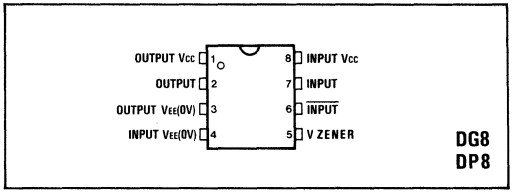


Fig.1 Pin connections - top view

FEATURES

- TTL/CMOS Compatible Output
- High Input Sensitivity
- Ideal Frequency Counter Prescaler
- On Chip Zener Diode

QUICK REFERENCE DATA

- Supply Voltage: 5V
- Power Consumption: 170mW
- Temperature Range: -40°C to +85°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage (Pins 1 and 8)	8V
Output current	40mA
Storage temperature range	-55°C to +125°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p

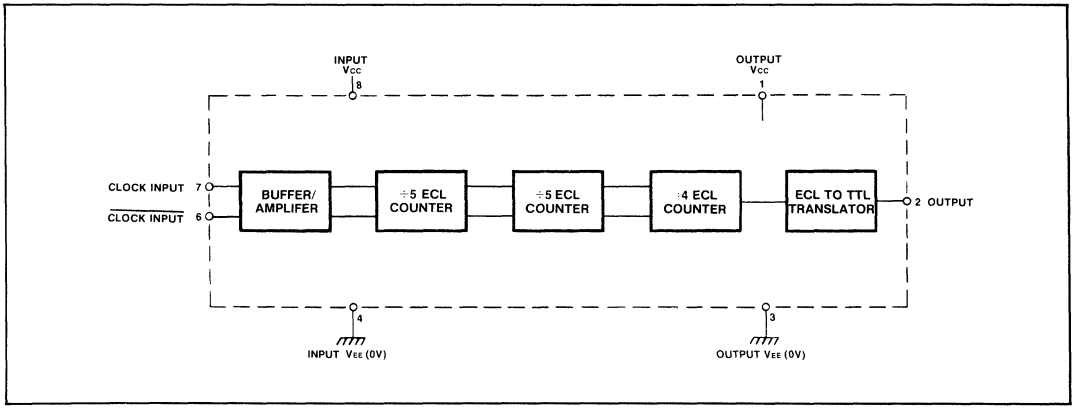


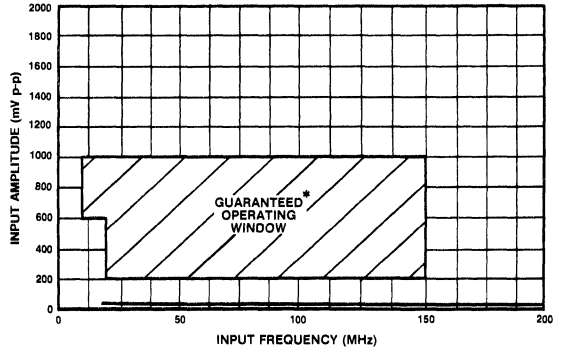
Fig.2 SP8629 logic diagram

ELECTRICAL CHARACTERISTICS

Supply Voltage: V_{CC} = 5.2V ± 0.52V V_{EE} = 0V
Temperature: T_{amb} -40°C to +85°C

Characteristics	Symbol	Value		Units	Conditions
		Min.	Max.		
Maximum toggle frequency sinewave input	f_{max}	150		MHz	Input = 200-1000mV p-p
Minimum toggle frequency sinewave input	f_{min}		10	MHz	Input = 600-1000mV p-p
Power supply current	I_{EE}		45	mA	
Output high voltage	V_{OH}	2.4		V	V_{CC} = 4.68V I_{OH} = -400µA
Output high voltage	V_{OH}	2.0		V	V_{CC} = 4.68V I_{OH} = -1.6mA
Output low voltage	V_{OL}		0.5	V	V_{CC} = 5.72V I_{OL} = 8mA
Output short circuit current	I_{OS}	-10	-40	mA	V_{CC} = 5.72V
Internal zener voltage	V_Z	5.85	6.65	V	

NOTES
1. Unless otherwise stated the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The dynamic test circuit is shown in Fig.5.
3. All characteristics above are tested at 25°C only.



*Tested as specified in table of Electrical Characteristics

Fig.3 Typical input characteristics SP8629

OPERATING NOTES

1. Two V_{EE} and two V_{CC} connections are provided, separating the ECL stages from the TTL section, isolating the noise transients inherent in the TTL structure. In most cases, shorting the two V_{EE} pins to a good ground plane and the V_{CC} pins to a wide V_{CC} bus will provide sufficient isolation. All components used in the circuit layout should be suitable for the frequencies involved and leads should be kept short to minimise stray inductance.
2. The signal source is usually capacitively coupled to the input as shown in Fig. 6. In the single-ended mode a capacitor of 0.01µF (C2) should be connected between the unused input and the ground plane to provide a good high frequency bypass. The capacitor should be increased at lower frequencies. If the input is likely to be interrupted, it may be desirable to connect a 100k resistor between an input and ground.
3. In the single ended mode it is preferable to connect the resistor to the unused input. The addition of the 100k resistor causes a loss of input sensitivity, but prevents circuit oscillations under no signal (open circuit) conditions.
4. The input waveform will normally be sinusoidal but below 10MHz correct operation depends on the slew rate of the input signal. A slew rate of 50V/µs will enable the device to operate down to DC. The device will operate with a TTL input signal as shown in Fig. 7 and is DC coupled to the input.

   The device can be used in phase locked loop applications such as FM radio or other communications bands to prescale the input frequency down to a more useable level. A digital frequency display system can also be derived separately or in conjunction with a phase locked loop, and it can extend the useful range of many inexpensive frequency counters to, typically, 200MHz.
5. The on-chip Zener diode allows a simple stabilised power supply to be constructed with the addition of a few extra external components, as shown in Fig. 8, to the SP8629.
6. The INPUT is positive edge triggered while the $\overline{\text{INPUT}}$ triggers on the negative edge.

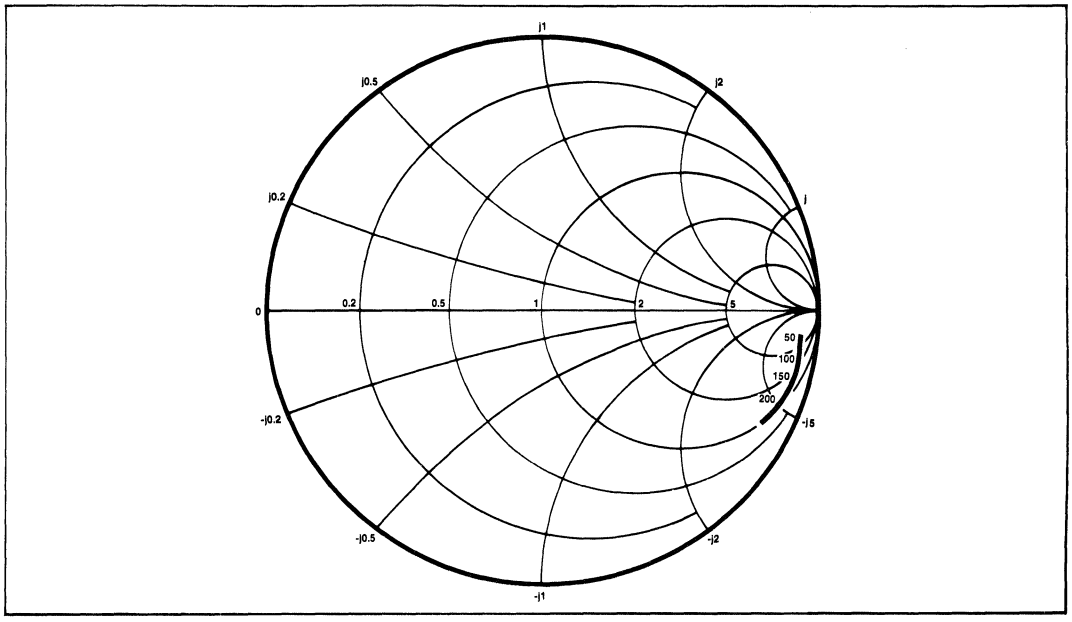


Fig.4 Typical input impedance. Test conditions: supply voltage 5.2V, ambient temperature 25° C. Frequencies in MHz, impedances normalised to 50 ohms.

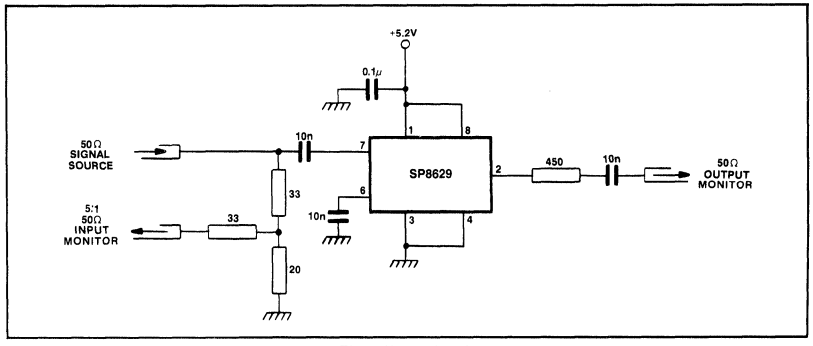


Fig.5 Test circuit

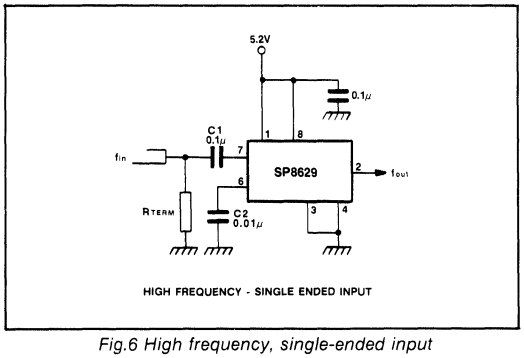


Fig.6 High frequency, single-ended input

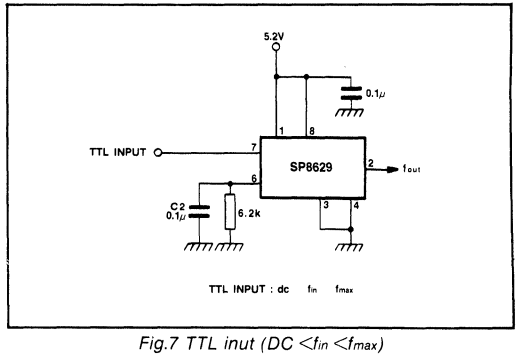


Fig.7 TTL inut (DC <f_{in} <f_{max})

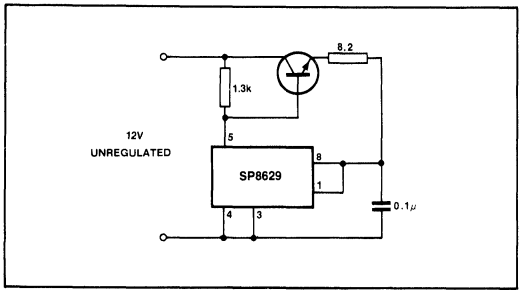


Fig.8 Use of on-chip zener diode for operation from unregulated supply

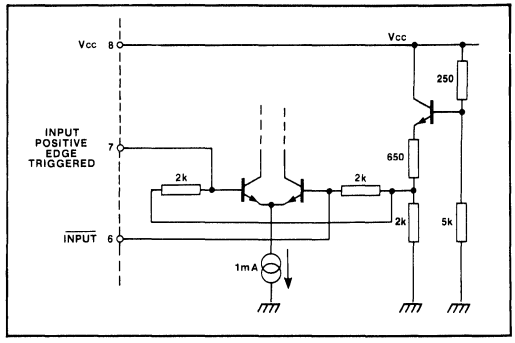


Fig.9 Input circuit diagram

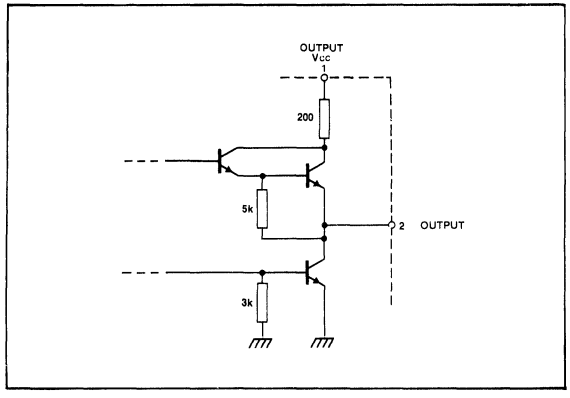


Fig.10 Output circuit diagram

SP8630A & B

600MHz ÷ 10

The SP8630 is an asynchronous emitter coupled logic counter which provides an ECL compatible output when used with an external pulldown resistor. It requires an AC coupled input of 600mV p-p.

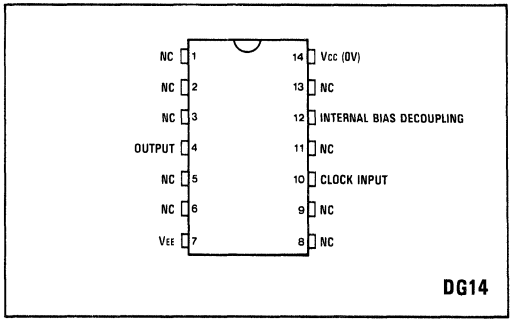


Fig.1 Pin connections - top view

FEATURES

- ECL Compatible Outputs
- AC Coupled Inputs (Internal Bias)

QUICK REFERENCE DATA

- Supply Voltage: -5.2V
- Power Consumption: 350mW
- Temperature Range:
  - -55°C to +125°C (A Grade)
  - -30°C to +70°C (B Grade)

ABSOLUTE MAXIMUM RATINGS

Supply voltage	-8V
Output current	15mA
Storage temperature range	-55°C to +150°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p

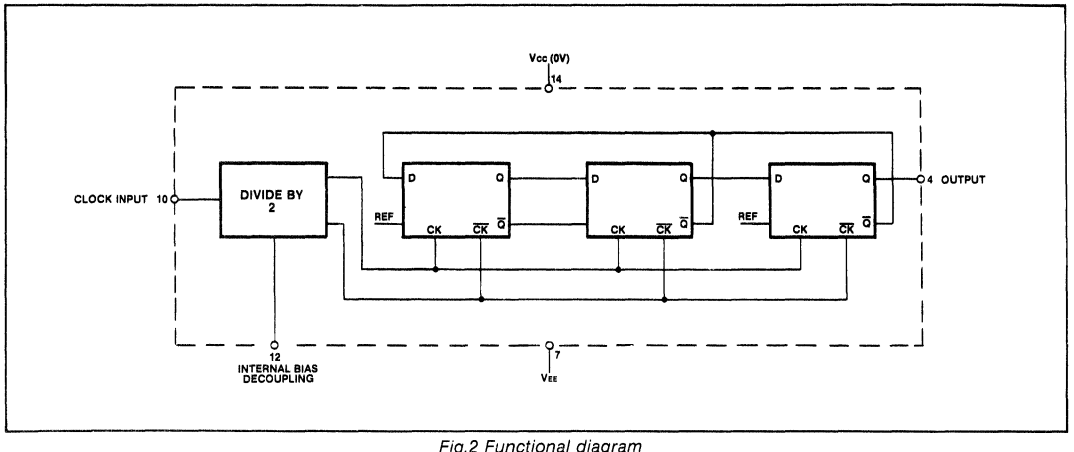


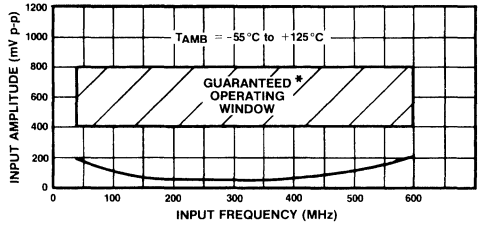
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply voltage: V_{CC} = 0V, V_{EE} = -5.2V ± 0.25V
Temperature: A Grade T_{amb} = -55°C to +125°C
B Grade T_{amb} = -30°C to +70°C

Characteristics	Symbol	Value		Units	Conditions	Note
		Min.	Max.			
Maximum frequency (sinewave input)	f_{max}	600		MHz	Input = 400-800mV p-p	
Minimum frequency (sinewave input)	f_{min}		40	MHz	Input = 400-800mV p-p	Note 4
Power supply current	I_{EE}		70	mA	V_{EE} = -5.2V	Note 4
Output low voltage	V_{OL}	-1.8	-1.5	V	V_{EE} = -5.2V (25°C)	
Output high voltage	V_{OH}	-0.85	-0.7	V	V_{EE} = -5.2V (25°C)	
Minimum output swing	V_{OUT}	400		mV	V_{EE} = -5.2V	

NOTES
1. Unless otherwise stated the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The temperature coefficients of V_{OH} = +1.63mV/°C and V_{OL} = +0.94mV/°C but these are not tested.
3. The test configuration for dynamic testing is shown in Fig.5.
4. Tested at 25°C only.



*Tested as specified in table of Electrical Characteristics

Fig.3 Typical input characteristic of SP8630A

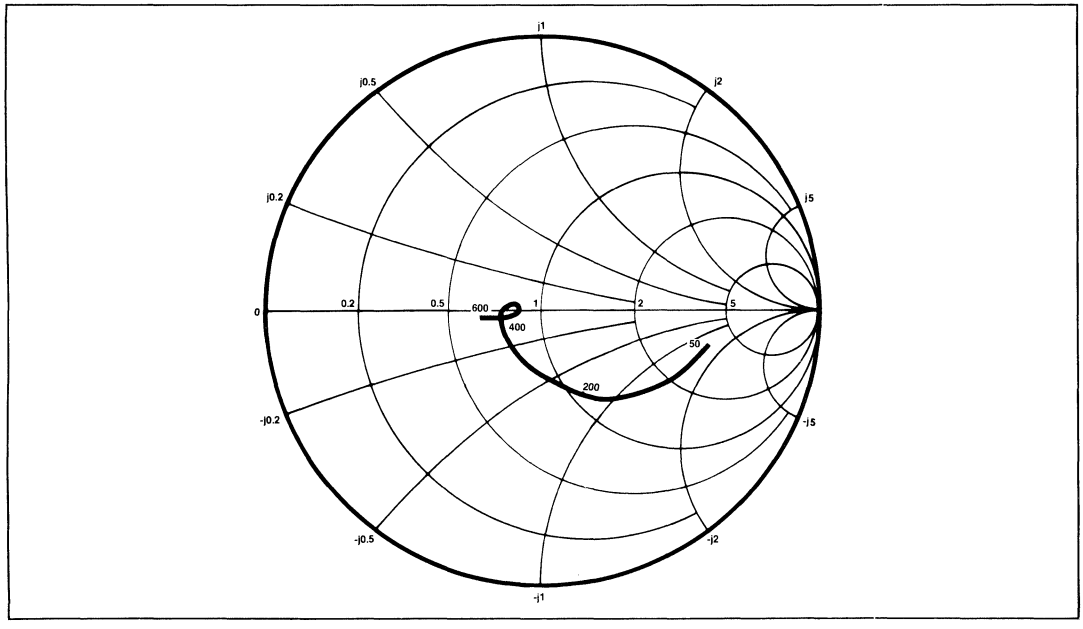


Fig.4 Typical input impedance. Test conditions: supply voltage -5.2V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

OPERATING NOTES

1. The clock input (pin 10) should be capacitively coupled to the signal source. The input signal path is completed by connecting a capacitor from the internal bias decoupling, pin 12, to ground.
2. The circuit will operate down to DC but slew rate must be better than 100V/μs.
3. The outputs are compatible with ECL II. There is an internal load of 3k at output. The output can be interfaced to ECL/10K by the addition of 1.5k to the output to increase the output voltage swing.
4. Input impedance is a function of frequency. See Fig.4.
5. All components should be suitable for the frequency in use.

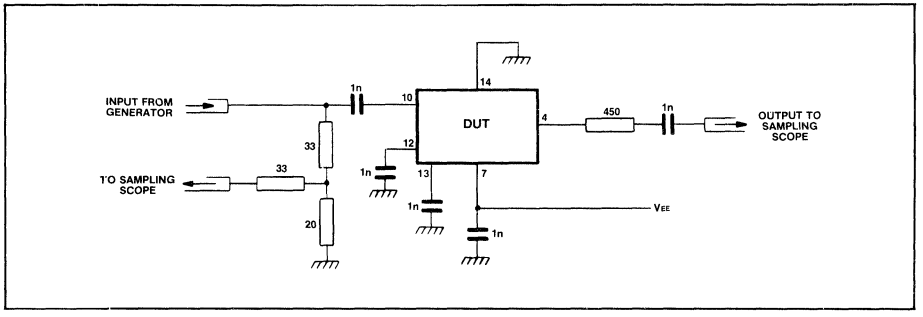


Fig.5 Test circuit

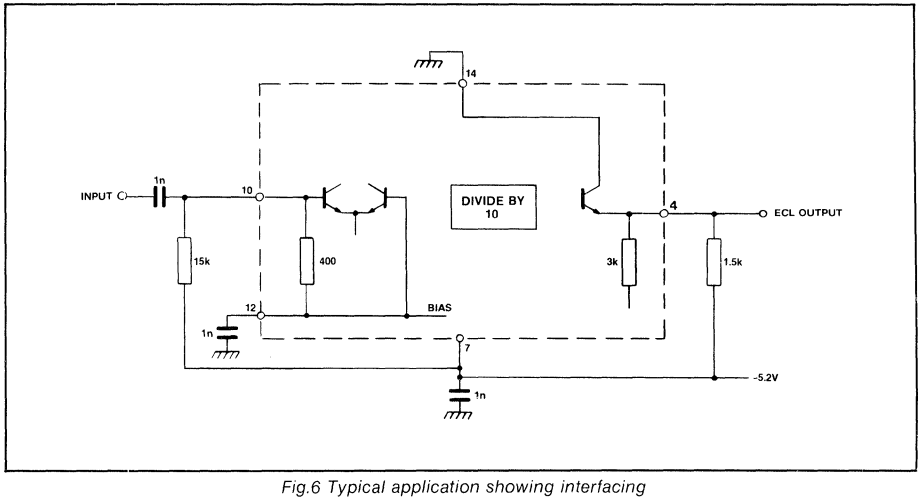


Fig.6 Typical application showing interfacing

SP8634B SP8635B SP8637B

700/600/400MHz ÷ 10 (BCD OUTPUTS)

The SP8634/5 and 7 are ECL decade counters with TTL compatible BCD outputs. They require an AC coupled input of 600mV p-p and have an ECL 10K compatible inhibit input which inhibits the device when in the high state. Both ECL and TTL 'carry' outputs are provided and there is a TTL reset.

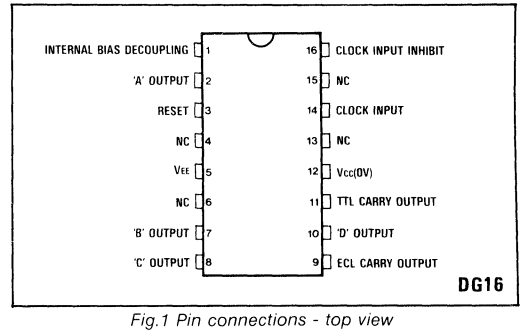


Fig.1 Pin connections - top view

FEATURES

- BCD Outputs TTL Compatible
- Reset Input TTL Compatible
- AC Coupled Input (Internal Bias)
- TTL and ECL Compatible Carry Outputs
- Clock Inhibit Input ECL Compatible

QUICK REFERENCE DATA

- Supply Voltage: 5.2V
- Power Consumption: 400mW
- Temperature Range: 0°C to +70°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage	-8V
BCD outputs voltage	VEE +11V
Storage temperature range	-55°C to +150°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p

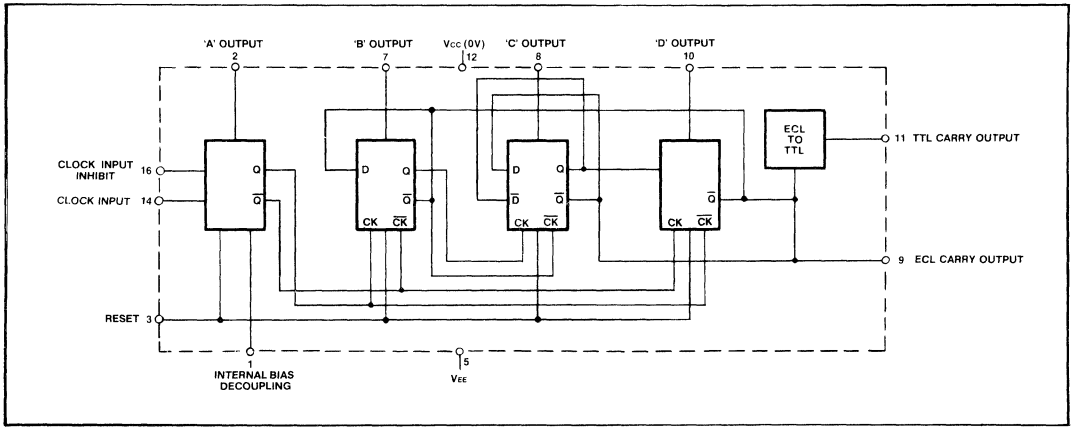


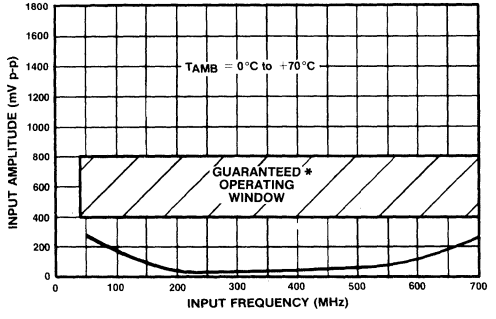
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply Voltage: V_{CC} = 0V V_{EE} = -5.2V ± 0.25V
Temperature: T_{amb} = 0°C to +70°C

Characteristics	Symbol	Value Min.	Value Max.	Units	Grade	Conditions	Notes
Maximum frequency sinewave input	f_{max}	700		MHz	SP8634B	Input = 400-800mV p-p	Note 5
		600		MHz	SP8635B		
		400		MHz	SP8637B		
Minimum frequency sinewave input	f_{min}		40	MHz	All	Input = 400-800mV p-p	Note 7
Power supply current	I_{EE}		90	mA	All	V_{EE} = -5.2V	Note 6
Clock inhibit high voltage	V_{INH}	-0.96		V	All	V_{EE} = -5.2V (25°C)	
Clock inhibit low voltage	V_{INL}		-1.65	V	All	V_{EE} = -5.2V (25°C)	
TTL output high voltage (pin 2,7,8,10)	V_{OH}	2.4		V	All	10kΩ from TTL output too +5V	Note 6
TTL output low voltage (pin 2,7,8,10)	V_{OL}		0.4	V	All	10kΩ from TTL output to +5V	Note 6
TTL output voltage (pin 11)	V_{OH}	2.4		V	All	5kΩ from TTL output to +5V	Note 6
TTL output low voltage (pin 11)	V_{OL}		0.4	V	All	5kΩ from TTL output to +5V	Note 6
ECL output high voltage (pin 9)	V_{OH}	-0.9	-0.7	V	All	V_{EE} = -5.2V (25°C)	
ECL output low voltage (pin 9)	V_{OL}	-1.8	-1.5	V	All	V_{EE} = -5.2V (25°C)	
Edge speed for correct operation at maximum frequency	t_E		2.5	ns	All	10% to 90%	Note 7
Reset on time for correct operation	t_{ON}	100		ns	All		Note 7
Reset input high voltage	V_{INH}	2.4		V	All		Note 6
Reset input low voltage	V_{INL}		0.5	V	All		Note 6

NOTES
1. Unless otherwise stated the electrical characteristics are guaranteed over full specified supply, frequency and temperature range.
2. The temperature coefficient of V_{OH} (ECL) = +1.3mV/°C and V_{OL} = +0.5mV/°C but these are not tested.
3. The temperature coefficient of inhibit threshold voltage = +0.24mV/°C but this is not tested.
4. The test configuration for dynamic testing is shown in Fig.5.
5. Tested at 0°C and +70°C only.
6. Tested at +25°C only.
7. Guaranteed but not tested.



*Tested as specified in table of Electrical Characteristics

Fig.3 Typical input characteristics SP8634

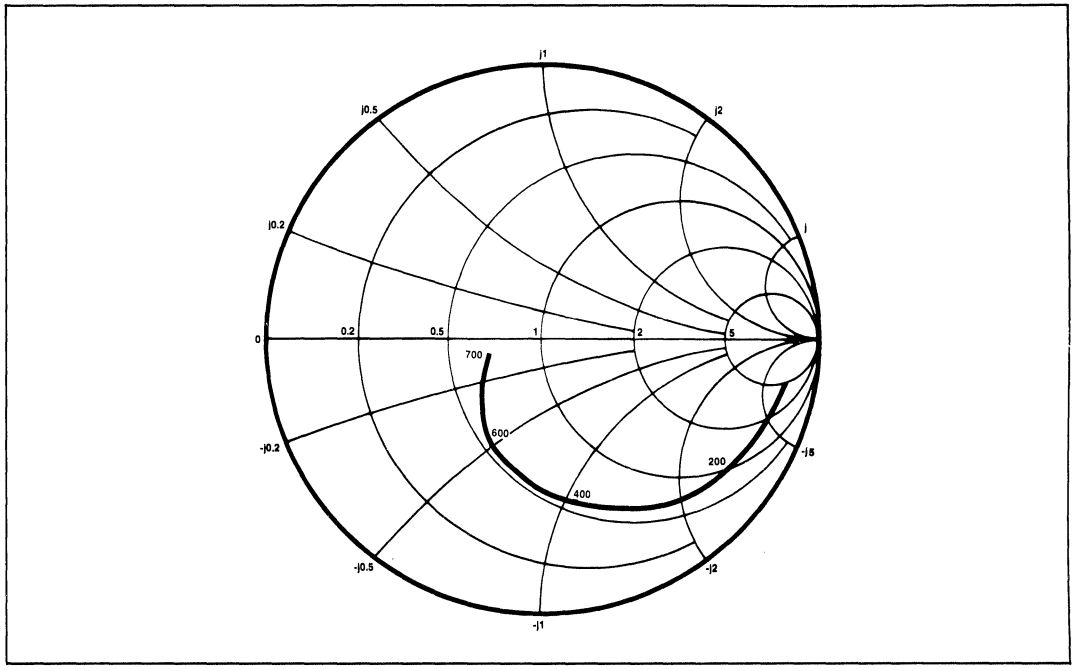


Fig.4 Typical input impedance. Test conditions: supply voltage 5.2V, ambient temperature 25° C. Frequencies in MHz, impedances normalised to 50 ohms.

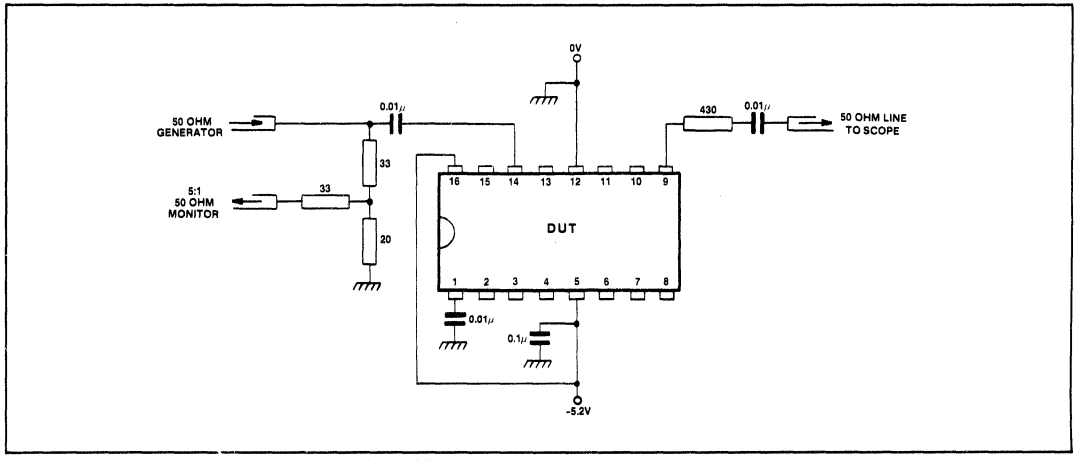


Fig.5 SP8634/5/7 high frequency test circuit

OPERATING NOTES

1. The clock input (pin 14) should be capacitively coupled to the signal source. The input signal path is completed by connecting a capacitor from the internal bias decoupling, pin 1, to ground.
2. In the absence of a signal the devices will self-oscillate. This can be prevented by connecting a 68k resistor between the clock input, pin 14, and the negative supply (pin 5).
3. The device will operate down to DC but the input slew rate must be better than 100V/μs.
4. The Carry O/P is ECL II compatible but can be interfaced ECL III/10K by the inclusion of two resistors. See Fig. 7.
5. The clock inhibit is compatible with ECL III/10K throughout the temperature range.
6. The output (pins 2, 7, 8, 10 and 11) are current sources and can be made TTL compatible by addition of 10k and 5k (pin 11) to +5V. See Fig.6. This gives a fan-out of 1. This can be increased by buffering the output with a PNP emitter follower. See Fig.8.
7. The device is clocked on the positive transition of the clock input on pin 14, provided that the clock inhibit input (pin 16) is in the low state. It is important to note that the positive transition of clock inhibit must occur while the clock is in the high state to avoid spurious counting.

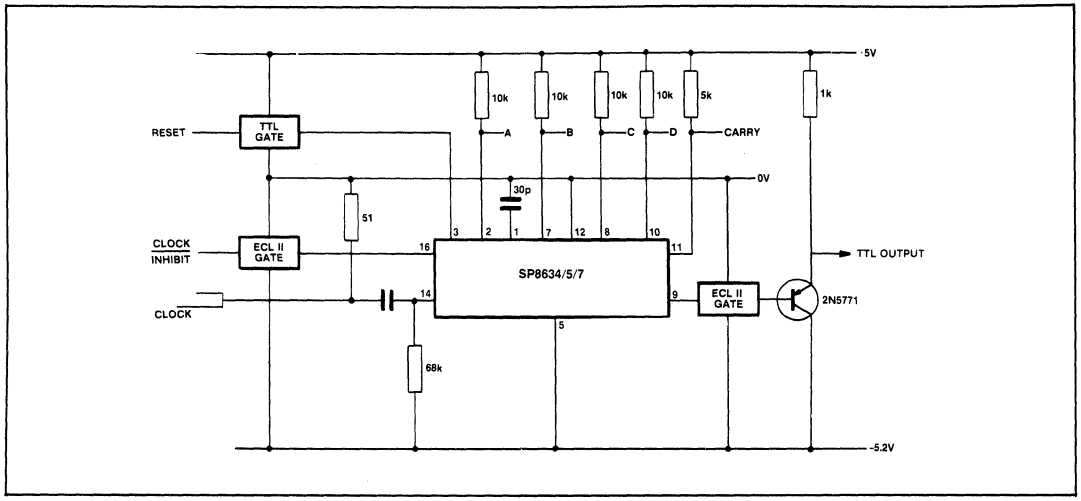


Fig.6 Typical application configuration

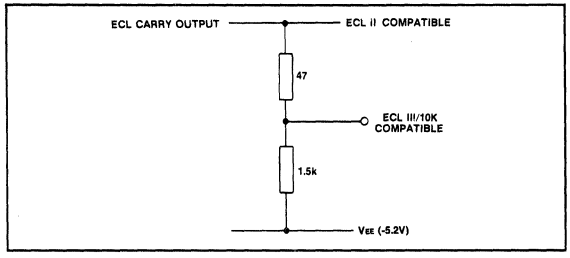


Fig.7 ECL III/10K interfacing

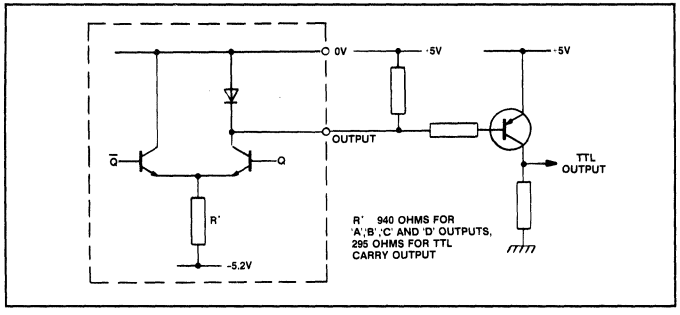


Fig.8 TTL output buffering for increased fan-out

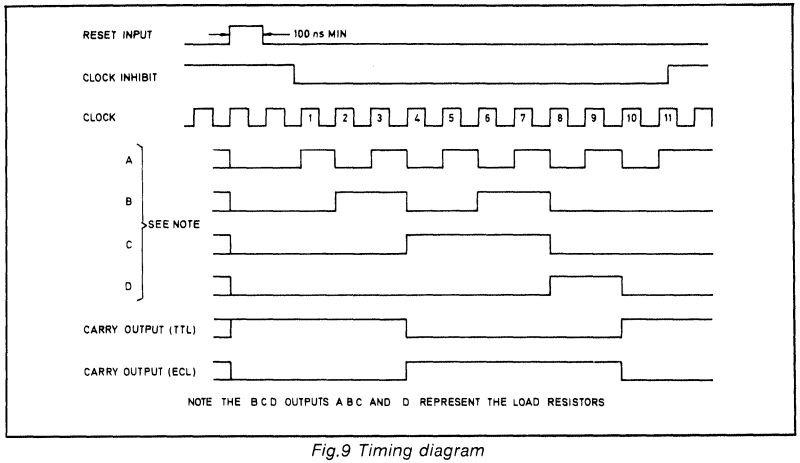


Fig.9 Timing diagram

SP8643A

350MHz ÷ 10/11

The SP8643 is an ECL variable modulus divider, with ECL 10K compatible outputs. It divides by 10 when either of the ECL control inputs, $\overline{PE1}$ or $\overline{PE2}$, is in the high state and by 11 when both are low (or open circuit).

The two clock inputs are interchangeable and either will act as a clock inhibit when connected to an ECL high level. Normally, one input is left open circuit and the other is AC coupled, with externally-applied bias.

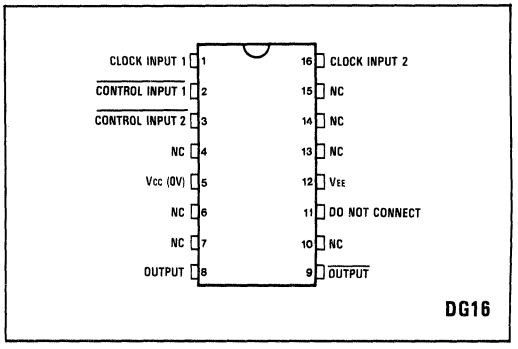


Fig.1 Pin connections - top view

FEATURES

- ECL Compatible Inputs/Outputs
- AC Coupled Input (External Bias)

QUICK REFERENCE DATA

- Supply Voltage: -5.2V
- Power Consumption: 260mW
- Temperature Range: -55°C to +125°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage	-8V
Output current	20mA
Storage temperature range	-55°C to +150°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p

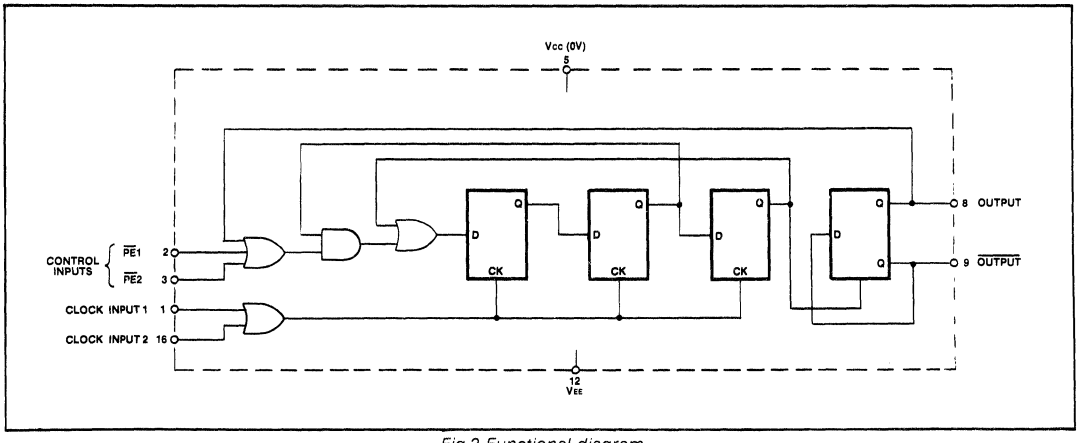


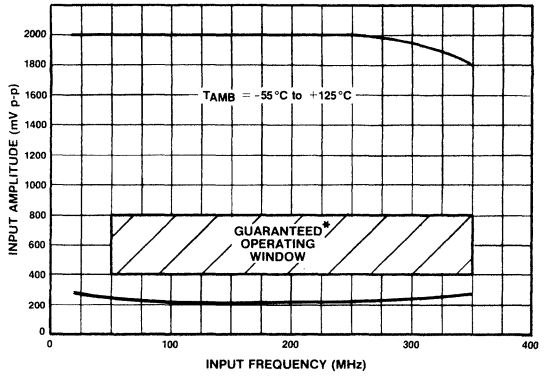
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply Voltage: V_{CC} = 0V V_{EE} = -5.2V ± 0.25V
Temperature: T_{amb} = -55°C to +125°C

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{max}	350		MHz	Input = 400-800mV p-p	
Minimum frequency (sinewave input)	f_{min}		50	MHz	Input = 400-800mV p-p	
Power supply current	I_{EE}		65	mA	V_{EE} = -5.2V	
ECL output high voltage	V_{OH}	-0.85	-0.7	V	V_{EE} = -5.2V (25°C)	
ECL output low voltage	V_{OL}	-1.8	-1.5	V	V_{EE} = -5.2V (25°C)	
$\overline{PE}$ input high voltage	V_{INH}	-0.93		V	V_{EE} = -5.2V (25°C)	
$\overline{PE}$ input low voltage	V_{INL}		-1.62	V	V_{EE} = -5.2V (25°C)	
Clock to ECL output delay	t_p		6	ns		Note 6
Set-up time	t_s	2.5		ns		Note 6
Release time	t_r	3		ns		Note 6

NOTES
1. Unless otherwise stated, the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The temperature coefficient of V_{OH} = +1.63mV/°C, V_{OL} = +0.94mV/°C and of V_{IN} = +1.22mV/°C but these are not tested.
3. The test configuration for dynamic testing is shown in Fig.6.
4. The set up time t_s is defined as minimum time that can elapse between L ⟶ H transition of control input and the next L ⟶ H clock pulse transition to ensure that ÷10 is obtained.
5. The release time t_r is defined as the minimum time that can elapse between H ⟶ L transition of the control input and the next L ⟶ H clock pulse transition to ensure that the ÷11 mode is obtained.
6. Guaranteed but not tested.



*Tested as specified in table of Electrical Characteristics

Fig.3 Typical input characteristic of SP8643A

TRUTH TABLE FOR CONTROL INPUTS

$\overline{PE1}$	$\overline{PE2}$	Division Ratio
L	L	11
H	L	10
L	H	10
H	H	10

OPERATING NOTES

1. The clock and control inputs are ECL III compatible. There is an internal pulldown resistor to V_{EE} of 4.3k on each input and therefore any unused input can be left open circuit when not in use but should be bypassed for RF signals with a 1nF capacitor to ensure maximum noise immunity. If it is desirable to capacitively couple the signal source to the clock input then an external bias is required as shown in Fig. 6. The external bias voltage should be -1.3V at 25°C.
2. The outputs are compatible with ECL II but can be interfaced to ECL 10K as shown in Fig. 7.
3. The circuit will operate down to DC but slew rate must be better than 100V/µs.
4. Input impedance is a function of frequency. See Fig. 5.
5. All components should be suitable for the frequency in use.

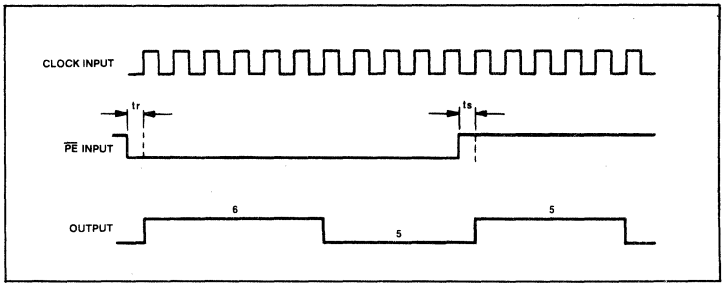


Fig.4 Timing diagram

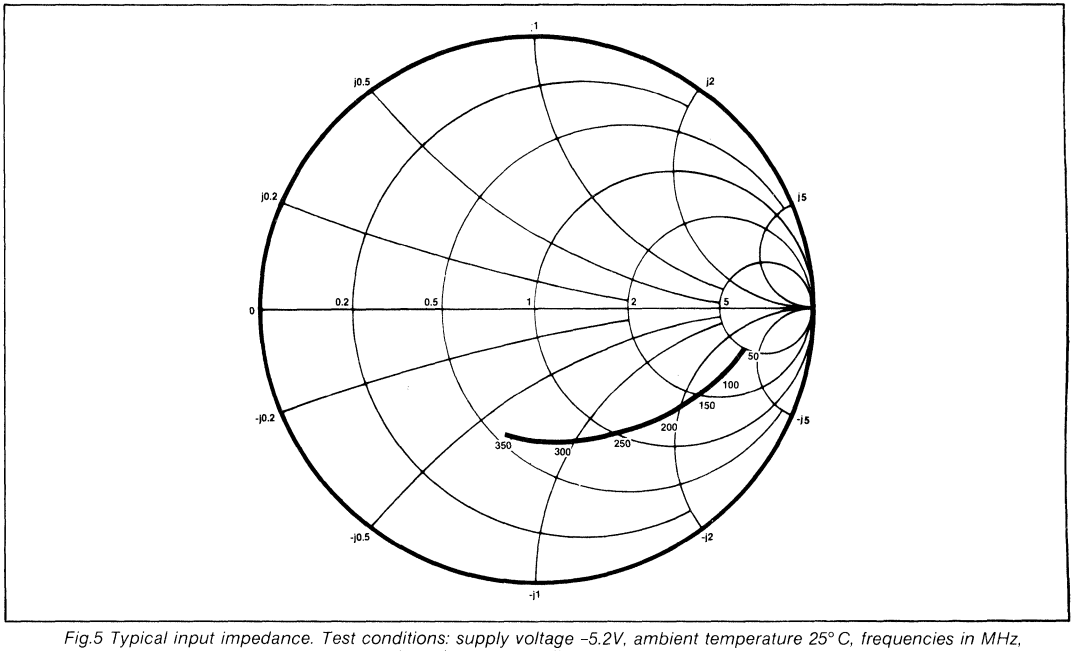


Fig.5 Typical input impedance. Test conditions: supply voltage -5.2V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

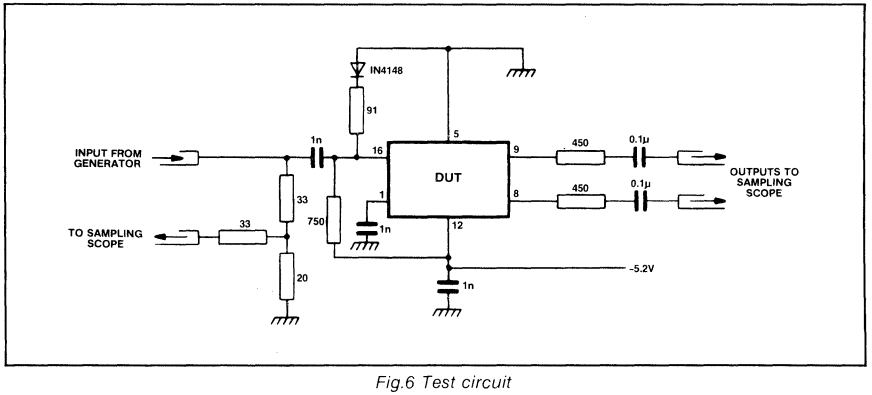


Fig.6 Test circuit

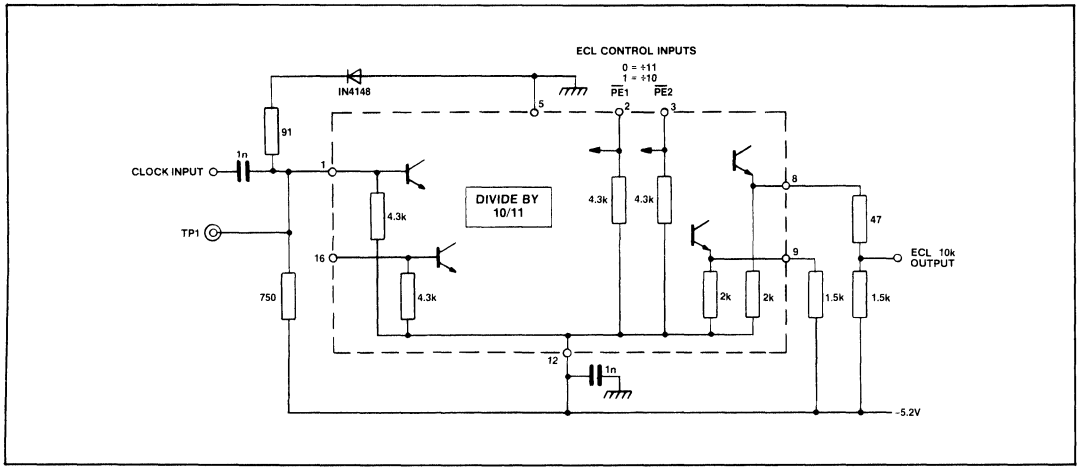


Fig.7 Typical application using ECL outputs. NB Voltage at TP1 should be -1.3V at 25° C

SP8647A & B

250MHz ÷ 10/11

The SP8647 is an ECL variable modulus divider, with ECL 10K and TTL/CMOS compatible outputs. It divides by 10 when either of the ECL control inputs, $\overline{PE1}$ or $\overline{PE2}$, is in the high state and by 11 when both are low (or open circuit).

The two clock inputs are interchangeable and either will act as a clock inhibit when connected to an ECL high level. Normally, one input is left open circuit and the other is AC coupled, with externally-applied bias.

FEATURES

- ECL Compatible Inputs/Outputs
- Open Collector TTL/CMOS Output
- AC Coupled Input (External Bias)

QUICK REFERENCE DATA

- Supply Voltage V_{CC}-V_{EE} : 5.2V ± 0.25V
- Power Consumption: 260mW
- Temperature Range:
  - -55°C to +125°C (A Grade)
  - -30°C to +70°C (B Grade)

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC} - V_{EE}	8V
Output current	20mA
Storage temperature range	-55°C to +150°C
Max. junction temperature	+175°C
Open collector voltage (Pin 11)	+12V
Max. clock I/P voltage	2.5V p-p
Max. open collector current	15mA

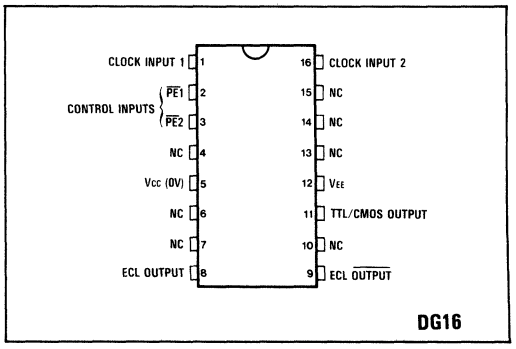


Fig.1 Pin connections - top view

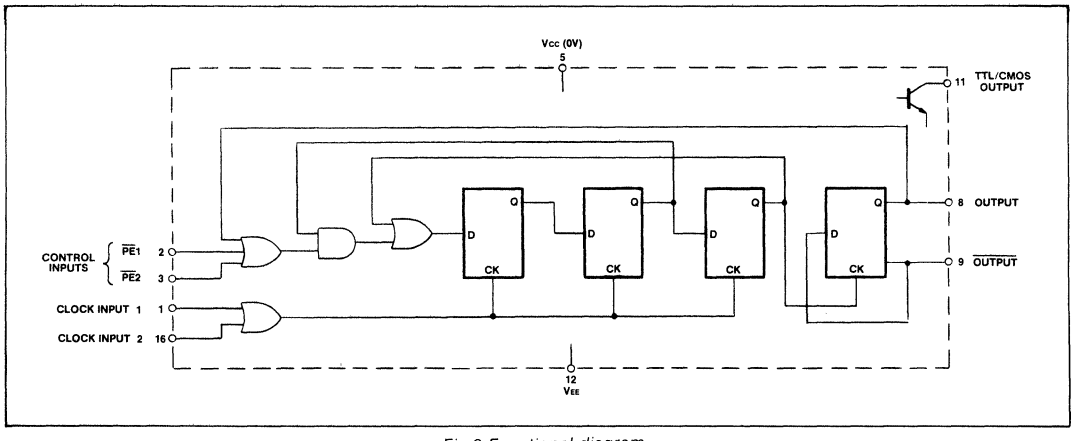


Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS (ECL OPERATION)

Supply Voltage: V_{CC} = 0V V_{EE} = -5.2V ± 0.25V
Temperature: A Grade T_{amb} = -55°C to +125°C B Grade T_{amb} = -30°C to +70°C

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{max}	250		MHz	Input = 400-800mV p-p	Note 6
Minimum frequency (sinewave input)	f_{min}		50	MHz	Input = 400-800mV p-p	Note 6
Power supply current	I_{EE}		65	mA	V_{EE} = -5.2V	Note 6
ECL output high voltage	V_{OH}	-0.85	-0.7	V	V_{EE} = -5.2V (25°C)	
ECL output low voltage	V_{OL}	-1.8	-1.5	V	V_{EE} = -5.2V (25°C)	
Clock and $\overline{PE}$ input high voltage	V_{INH}	-0.93		V	V_{EE} = -5.2V (25°C)	
Clock and $\overline{PE}$ input low voltage	V_{INL}		-1.62	V	V_{EE} = -5.2V (25°C)	
Clock to ECL output delay	t_p		6	ns		Note 7
Set-up time	t_s	2.5		ns		Note 7
Release time	t_r	3		ns		Note 7

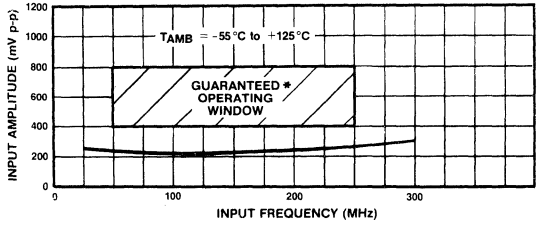
NOTES
1. Unless otherwise stated, the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The temperature coefficient of V_{OH} = +1.63mV/°C, V_{OL} = +0.94mV/°C and of V_{IN} = +1.22mV/°C.
3. The test configuration for dynamic testing is shown in Fig.6.
4. The set up time t_s is defined as minimum time that can elapse between L → H transition of control input and the next L → H clock pulse transition to ensure that ÷10 is obtained.
5. The release time t_r is defined as the minimum time that can elapse between H → L transition of the control input and the next L → H clock pulse transition to ensure that the ÷11 mode is obtained.
6. SP8647B tested at 25°C only.
7. Guaranteed but not tested.

ELECTRICAL CHARACTERISTICS (TTL OPERATION)

Supply Voltage: V_{CC} = 5V ± 0.25V V_{EE} = 0V
Temperature: A Grade T_{amb} = -55°C to +125°C B Grade T_{amb} = -30°C to +70°C

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{max}	250		MHz	Input = 400-800mV p-p	Note 3
Minimum frequency (sinewave input)	f_{min}		50	MHz	Input = 400-800mV p-p	Note 3
Power supply current	I_{EE}		65	mA		Note 3
TTL output low voltage	V_{OL}		0.5	V	V_{CC} = +5.25V Sink current = 8mA	Note 3, 5
TTL output high voltage	V_{OH}	3.5		V	V_{CC} = +5.0V	Note 3, 5
Clock to TTL output high delay (positive going)	t_{PLH}		15	ns		Note 4
Clock to TTL output low delay (negative going)	t_{PHL}		15	ns		Note 4
Set-up time	t_s	2.5		ns		Note 4
Release time	t_r	3		ns		Note 4

NOTES
1. Unless otherwise stated the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The test configuration for dynamic testing is shown in Fig.6.
3. SP8647B tested at 25°C only.
4. Guaranteed but not tested.
5. TTL output for use up to 15MHz output frequency. $C_{load} \leq 5pF$.



*Tested as specified in table of Electrical Characteristics

Fig.3 Typical input characteristic of SP8647A

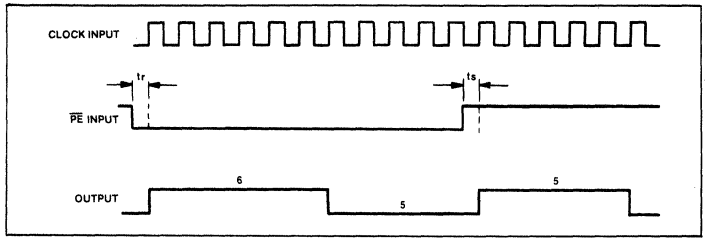


Fig.4 Timing diagram

TRUTH TABLE FOR CONTROL INPUTS

$\overline{PE1}$	$\overline{PE2}$	Division Ratio
L	L	11
H	L	10
L	H	10
H	H	10

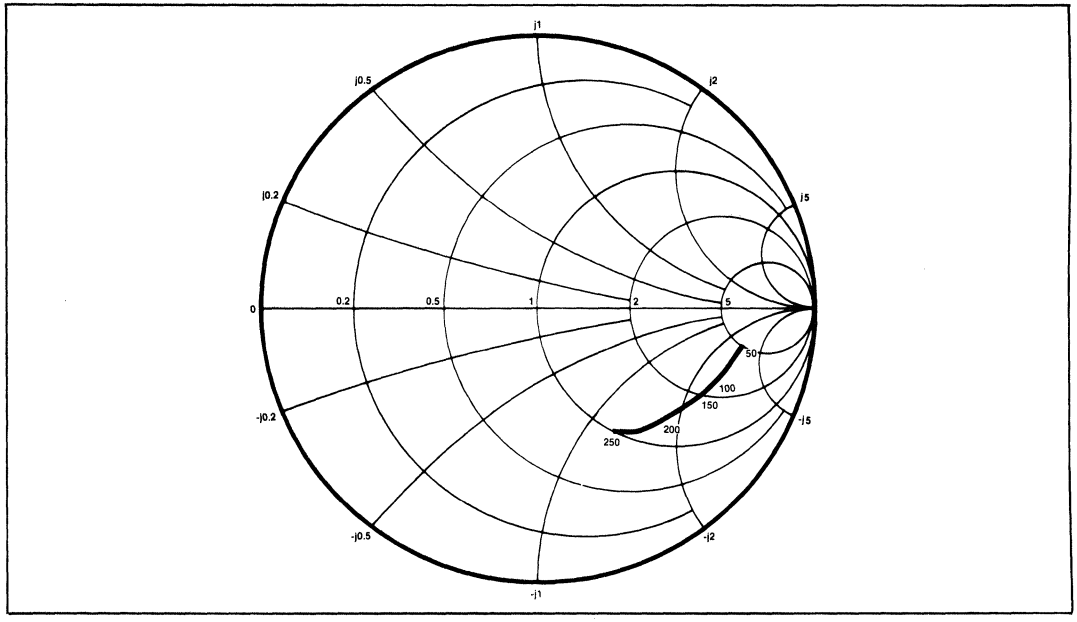


Fig.5 Typical input impedance. Test conditions: supply voltage 5V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

OPERATING NOTES

1. The clock and control inputs are ECL III compatible. There is an internal pulldown resistor to V_{EE} of 4.3k on each input and therefore any unused input can be left open circuit. If it is desirable to capacitively couple the signal source to the clock then an external bias is required as shown in Fig. 6. The external bias voltage should be -1.3V at 25°C.
2. The outputs are compatible with ECL II but can be interfaced to ECL 10K as shown in Fig. 8.
3. The circuit will operate down to DC but slew rate must be better than 100V/µs.
4. Input impedance is a function of frequency. See Fig. 5.
5. The TTL/CMOS O/P is a free collector, with an output rise/fall time which is a function of load resistance and load capacitance. The load capacitance should therefore be kept to a minimum and the load resistance should not be too small otherwise V_{OL} will be too great. eg TTL output current = 8mA V_{OL} = 0.5V. For CMOS outputs, the value of load resistor should be the maximum consistent with satisfactory rise times.
6. All components should be suitable for the frequency in use.

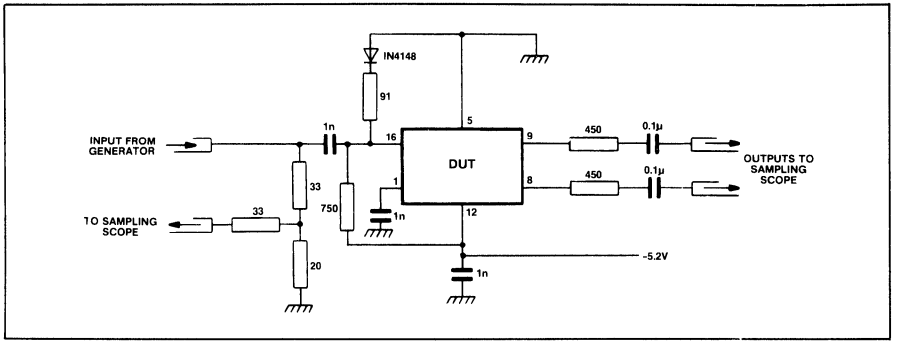


Fig.6 Test circuit

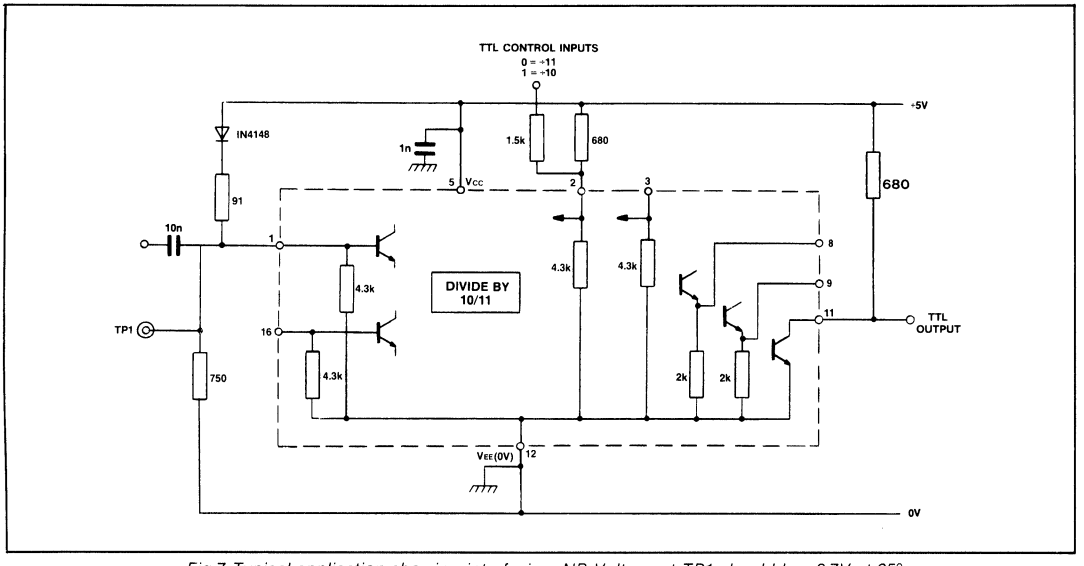


Fig.7 Typical application showing interfacing. NB Voltage at TP1 should be 3.7V at 25°

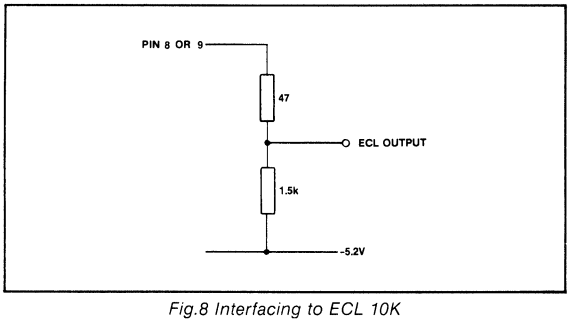


Fig.8 Interfacing to ECL 10K

SP8650A & B

600MHz ÷ 16

The SP8650 is an asynchronous emitter coupled logic counter which provides ECL 10K compatible outputs when external pulldown resistors are added. It requires an AC coupled input of 600mV p-p.

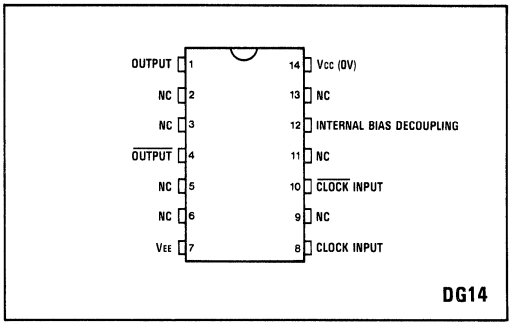


Fig.1 Pin connections - top view

FEATURES

- ECL Compatible Outputs
- AC Coupled Inputs (Internal Bias)

QUICK REFERENCE DATA

- Supply Voltage: -5.2V
- Power Consumption: 300mW
- Temperature Range:
  -55°C to +125°C (A Grade)
  -30°C to +70°C (B Grade)

ABSOLUTE MAXIMUM RATINGS

Supply voltage	-8V
Output current	10mA
Storage temperature range	-55°C to +150°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p

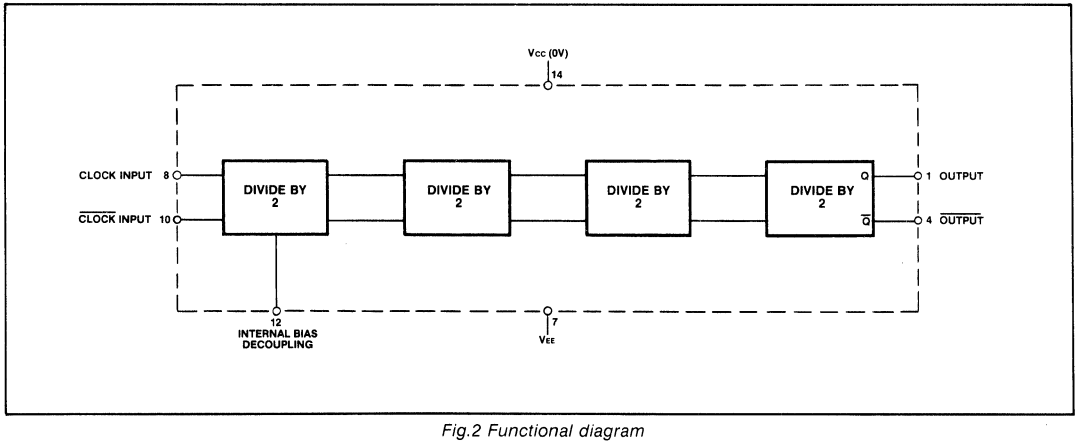


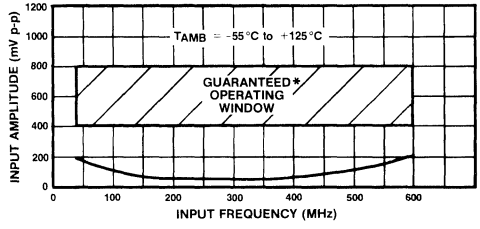
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply voltage: V_{CC} = 0V, V_{EE} = -5.2V ± 0.25V
Temperature: A Grade T_{amb} = -55°C to +125°C
B Grade T_{amb} = -30°C to +70°C

Characteristics	Symbol	Value Min.	Value Max.	Units	Conditions	Notes
Maximum frequency (sinewave input)	f_{max}	600		MHz	Input = 400-800mV p-p	
Minimum frequency (sinewave input)	f_{min}		40	MHz	Input = 400-800mV p-p	Note 4
Power supply current	I_{EE}		60	mA		Note 4
Output low voltage	V_{OL}	-1.8	-1.5	V	V_{EE} = -5.2V (25°C)	
Output high voltage	V_{OH}	-0.85	-0.7	V	V_{EE} = -5.2V (25°C)	

NOTES
1. Unless otherwise stated the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The temperature coefficients of V_{OH} = +1.63mV/°C and V_{OL} = +0.94mV/°C but these are not tested.
3. The test configuration for dynamic testing is shown in Fig.5.
4. Tested at 25° only.



*Tested as specified in table of Electrical Characteristics

Fig.3 Typical input characteristic of SP8650A

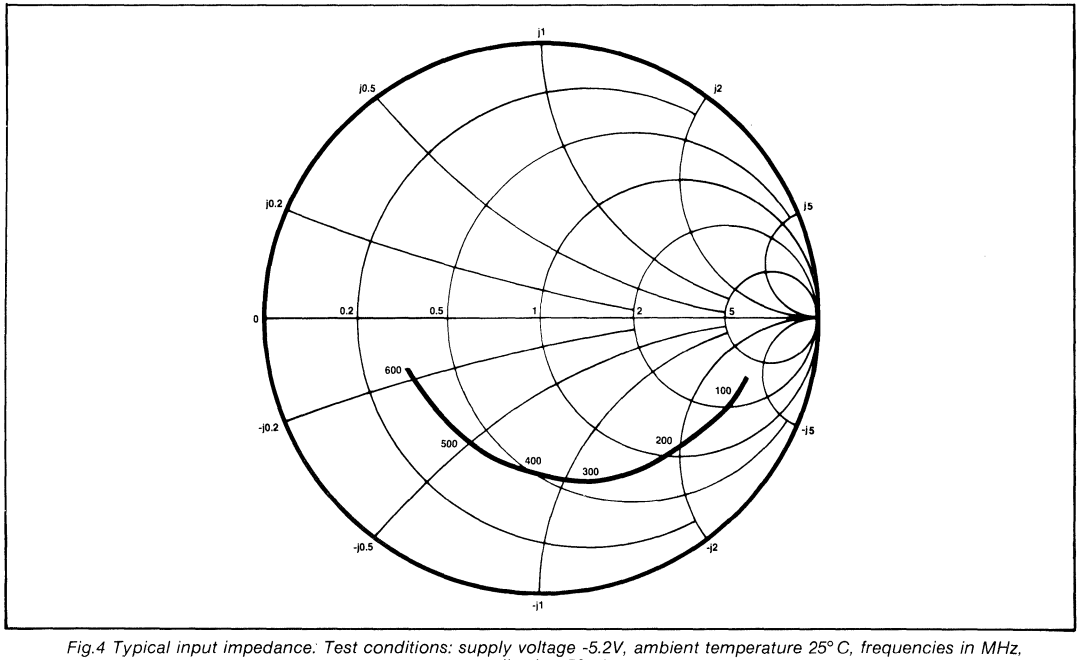


Fig.4 Typical input impedance. Test conditions: supply voltage -5.2V, ambient temperature 25° C, frequencies in MHz, normalised to 50 ohms.

OPERATING NOTES

1. The clock inputs (pins 8 and 10) can be driven single-ended or differentially and should be capacitively coupled to the signal source. The input signal path is completed by connecting a capacitor from the internal bias decoupling, pin 12, to ground.
2. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 10k resistor from one of the inputs to V_{EE}. This will reduce the input sensitivity by approximately 100mV.
3. The circuit will operate down to DC but slew rate must be better than 100V/µs.
4. The outputs are compatible with ECL II. There is an internal load of 4k at each output. The output can be interfaced to ECL 10K by addition of two resistors.
5. Input impedance is a function of frequency. See Fig. 4.
6. All components should be suitable for the frequency in use.

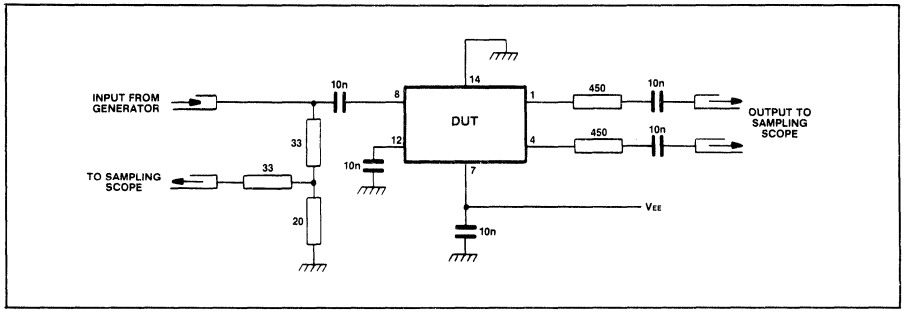


Fig.5 Test circuit

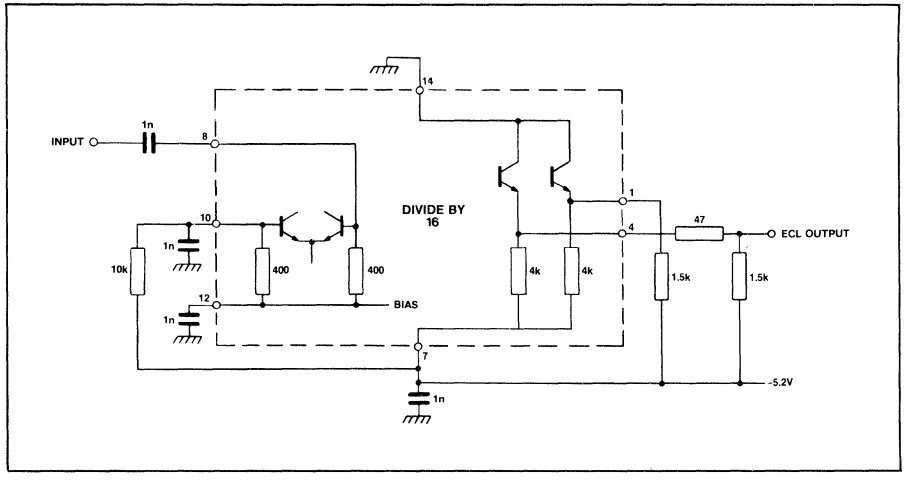


Fig.6 Typical application showing interfacing

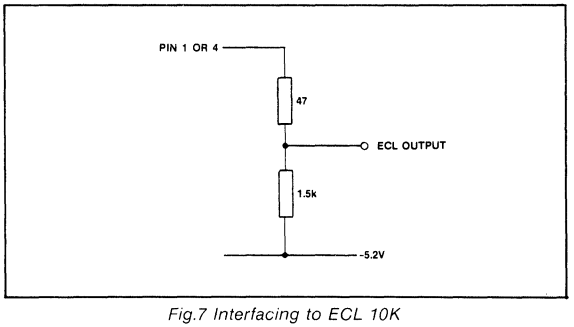


Fig.7 Interfacing to ECL 10K

SP8655A & B 200MHz ÷ 32
SP8657A & B 200MHz ÷ 20
SP8659A & B 200MHz ÷ 16

The SP8655, 57 and 59 are low power emitter coupled logic counters with open collector outputs capable of driving TTL or CMOS. They are available in two temperature ranges: -55°C to +125°C (A grade) and -30°C to +70°C (B grade). It has internally biased inputs.

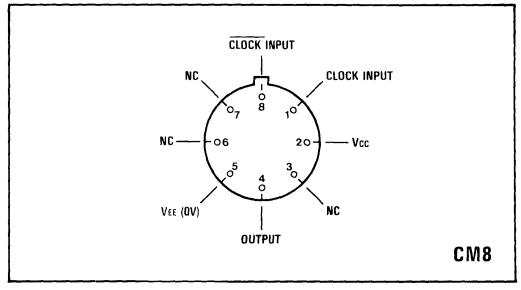


Fig.1 Pin connections - bottom view

FEATURES

- AC Coupled Inputs
- Low Power Consumption
- Open Collector Output CMOS and TTL Compatible

QUICK REFERENCE DATA

- Supply Voltage: 5.0V
- Power Consumption: 50mW
- Temperature Range:
  - -55°C to +125°C (A Grade)
  - -30°C to +70°C (B Grade)

ABSOLUTE MAXIMUM RATINGS

Supply voltage	8V
Open collector output voltage	12V
Storage temperature range	-55°C to +150°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p
Output sink current	10mA

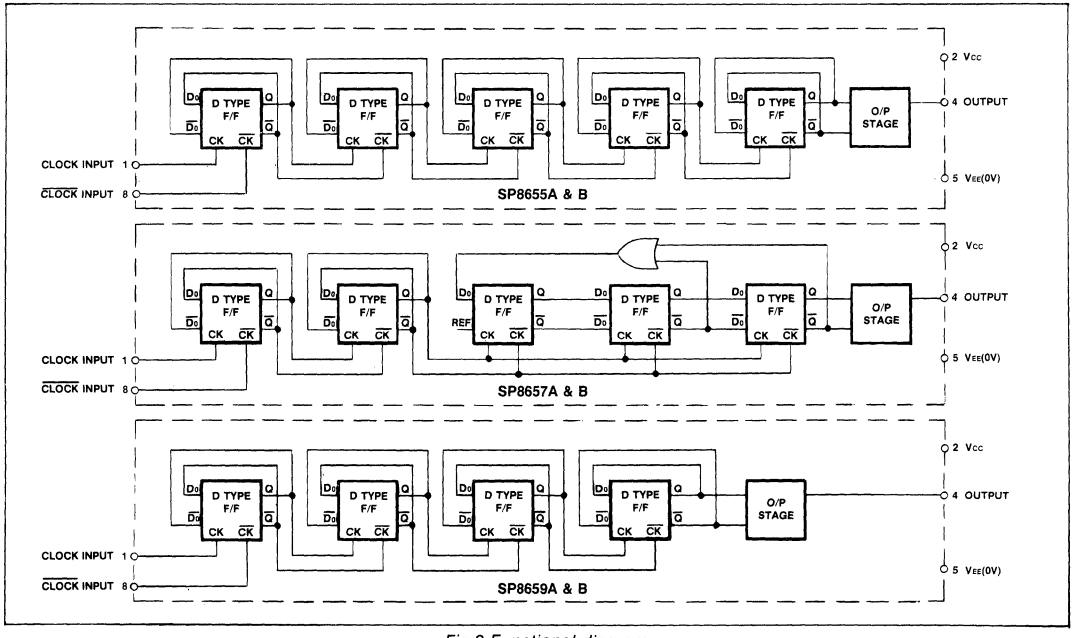


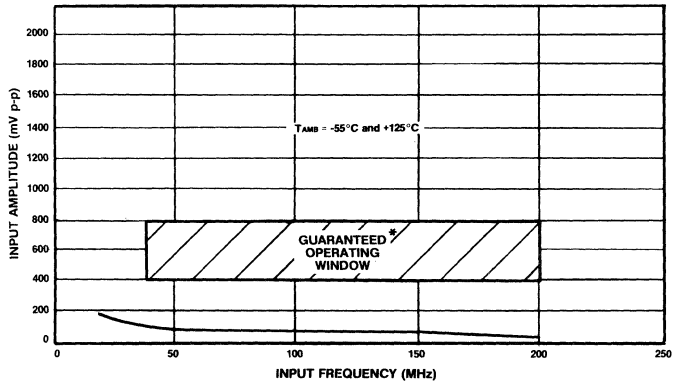
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply voltage: V_{CC} = 5.0V ± 0.25V V_{EE} = 0V
Temperature: A grade T_{amb} = -55°C to +125°C
B grade T_{amb} = -30°C to +70°C

Characteristic	Symbol	Value		Units	Conditions
		Min.	Max.		
Maximum frequency (sinewave input)	f_{max}	200		MHz	Input =400 - 800mV
Minimum frequency (sinewave input)	f_{min}		40	MHz	Input =400 - 800mV
Power supply current	I_{EE}		13	mA	V_{CC}= 5.25V
Output high voltage	V_{OH}	7.5		V	V_{CC}= 5V Note 4
					Pin 4 = 1.5kΩ to 10V
Output low voltage	V_{OL}		400	mV	V_{CC} = 5V
					Pin 4 = 1.5kΩ to 10V

NOTES
1. Unless otherwise stated the electrical characteristics are guaranteed over specified supply, frequency and temperature range.
2. The dynamic test circuit is shown in Fig.5.
3. Above characteristics are not tested at 25°C (tested at low and high temperature only).
4. Open collector output not to be used above 15MHz. $C_{load} \leq 5pF$.



*Tested as specified in table of Electrical Characteristics

Fig.3 Typical input characteristics

OPERATING NOTES

1. The clock inputs (pin 1 and 8) should be capacitively coupled to the signal source. When driven single-ended, the input signal path is completed by connecting a capacitor from the unused input to ground.
2. In the absence of a signal the devices will self-oscillate. This can be prevented by connecting a 39k resistor from either input to ground. If the device is driven single ended, it is recommended that the pulldown resistor be connected to the decoupled unused input. There will be a loss in sensitivity of approximately 200mV.
3. The device will operate down to DC but the input slew rate must be better than 100V/µs.
4. The open collector output will drive 3 TTL loads, and thus requires a suitable resistor to V_{CC} to maintain noise immunity. In order to ensure noise immunity on transitions, this resistor should not exceed 4.7k. For interfacing to CMOS, the open collector may be restored to a +10V line via a 3.3k resistor. The output sink current must not exceed 10mA, and the use of too low a value of resistor may lead to a loss of noise immunity, especially at low temperatures.
5. Input impedance is a function of frequency. See Fig. 4.
6. The rise time of the open collector output waveform is directly proportional to the load capacitance and load resistor value. Therefore the load capacitance should be minimised and the load resistor kept to a minimum compatible with system power requirements. In the test configuration of Fig. 5, the output rise time is approximately 20ns and fall time is typically 10ns.

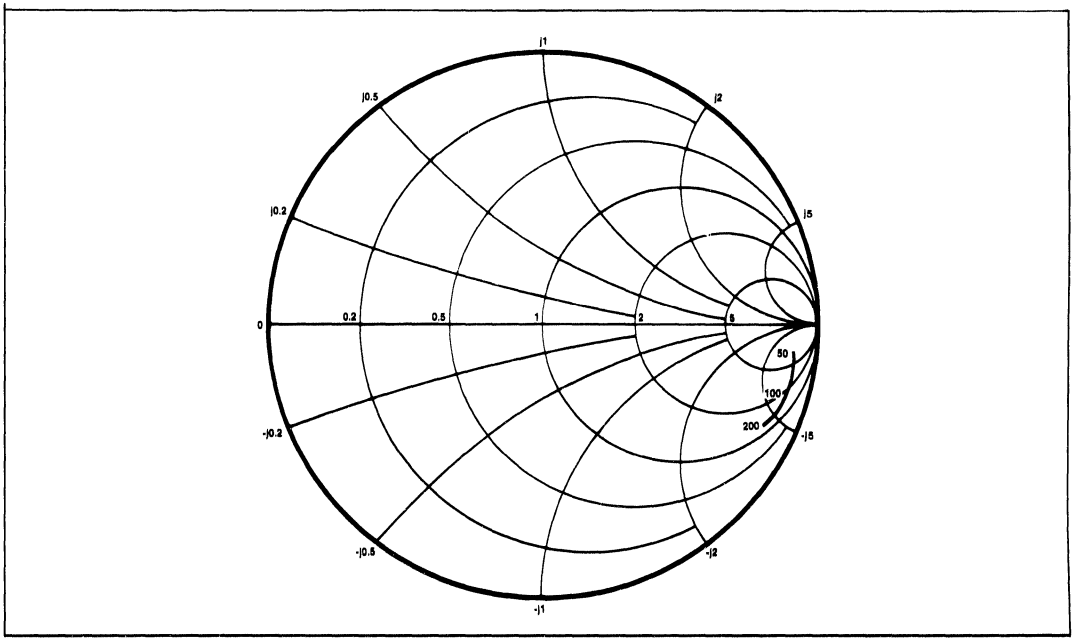


Fig.4 Typical input impedance. Test conditions: supply voltage 5.0V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

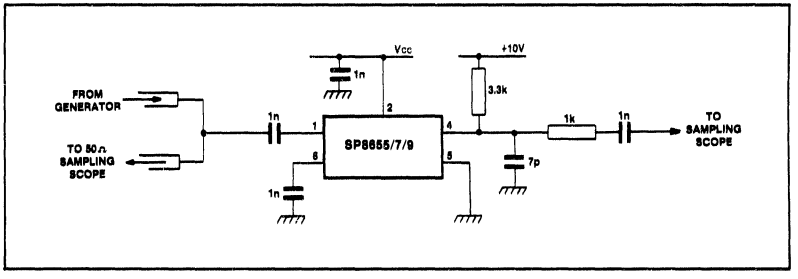


Fig.5 Test circuit

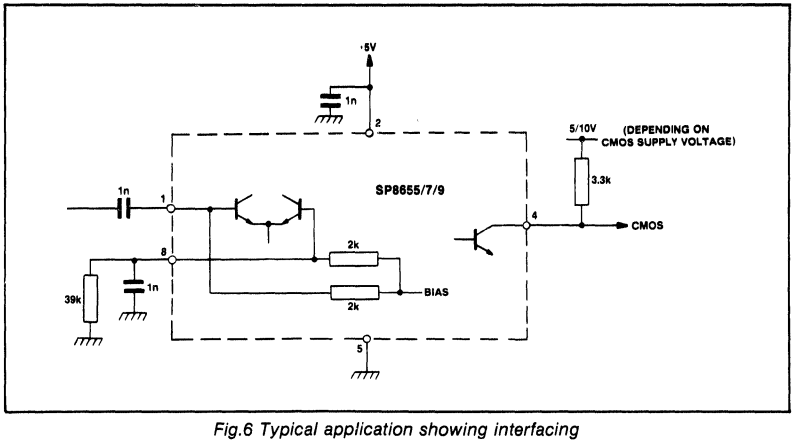


Fig.6 Typical application showing interfacing

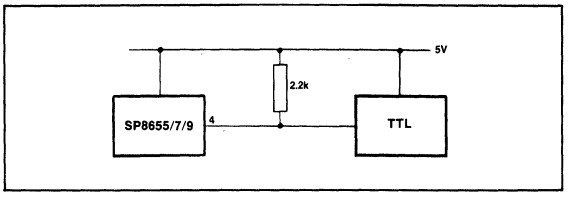


Fig.7 Interfacing to TTL. Load not to exceed 3 TTL unit loads.

SP8660

150MHz ÷ 10

The SP8660 is a low power emitter coupled logic counter with an open collector output capable of driving TTL or CMOS. It has internally biased inputs and an open collector.

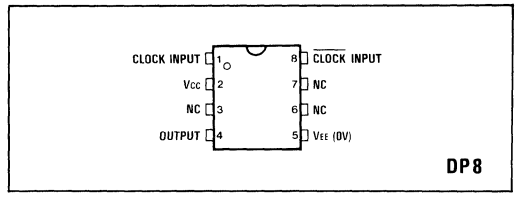


Fig.1 Pin connections - top view

FEATURES

- AC Coupled Inputs
- Low Power Consumption
- Open Collector Output CMOS and TTL Compatible

QUICK REFERENCE DATA

- Supply Voltage: 5.0V
- Power Consumption: 50mW
- Temperature Range: -30°C to +70°C
- 8 Lead Plastic Package

ABSOLUTE MAXIMUM RATINGS

Supply voltage	8V
Open collector output voltage	12V
Storage temperature range	-55°C to +125°C
Max. junction temperature	+175°C
Output sink current	10mA
Max. clock I/P voltage	2.5V p-p

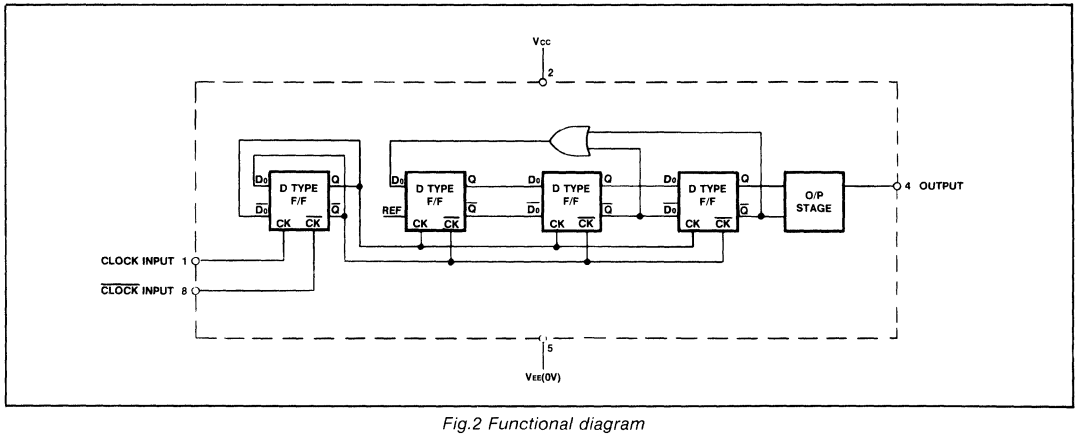


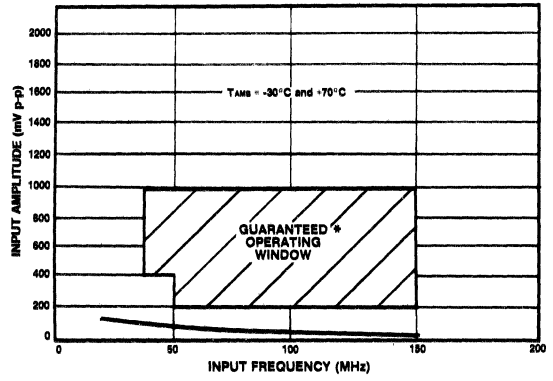
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply voltage: V_{CC} = 5.0V ± 0.25V V_{EE} = 0V
Temperature: T_{amb} = -30°C to +70°C

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{max}	150		MHz	Input = 200-1000mV	
Minimum frequency (sinewave input)	f_{min}		40	MHz	Input = 400-1000mV	
Power supply current	I_{EE}		13	mA	V_{CC} = 5.25V	
Output high voltage	V_{OH}	9		V	V_{CC} = 5V	
					Pin 4 = 1.5kΩ to 10V	Note 4
Output low voltage	V_{OL}		400	mV	V_{CC} = 5V	
					Pin 4 = 1.5kΩ to 10V	Note 4

NOTES
1. Unless otherwise stated the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The dynamic test circuit is shown in Fig.5.
3. All characteristics above are tested at 25°C only.
4. $C_{load} \leq 5pF$.



*Tested as specified in table of Electrical Characteristics

Fig.3 Typical input characteristics

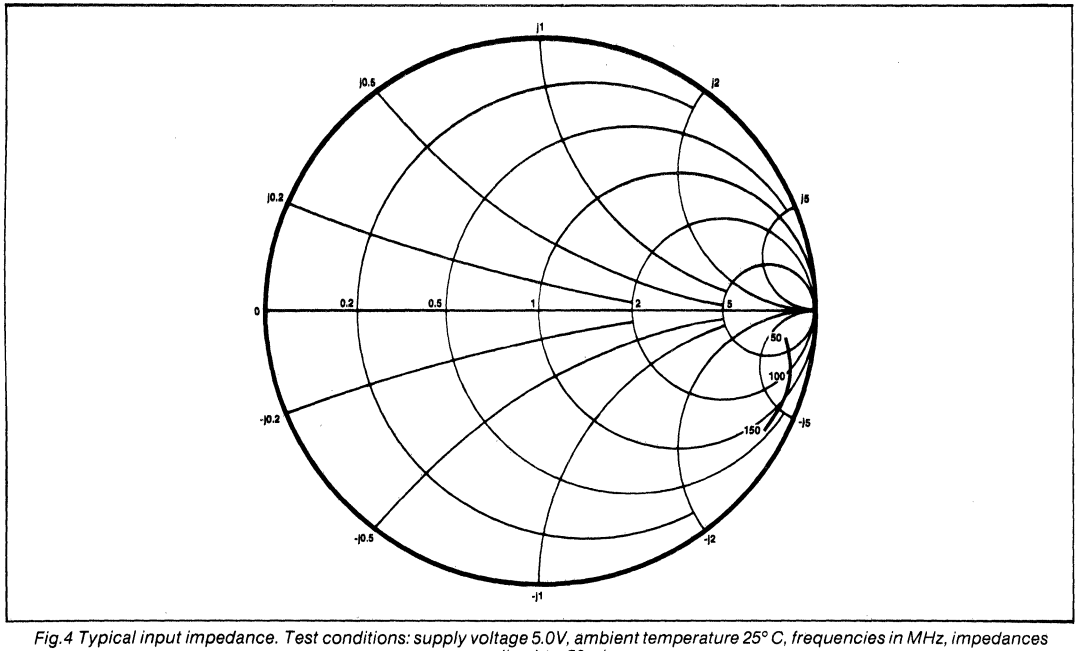


Fig.4 Typical input impedance. Test conditions: supply voltage 5.0V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms

OPERATING NOTES

1. The clock inputs (pin 1 and 8) should be capacitively coupled to the signal source. When driven single-ended, the input signal path is completed by connecting a capacitor from the unused input to ground.
2. In the absence of a signal the devices will self-oscillate. This can be prevented by connecting a 39k resistor from either input to ground. If the device is driven single ended, it is recommended that the pulldown resistor be connected to the decoupled unused input. There will be a loss in sensitivity of approximately 200mV.
3. The device will operate down to DC but the input slew rate must be better than 100V/µs.
4. The open collector output will drive 3 TTL loads, and thus requires a suitable resistor to Vcc to maintain noise immunity. In order to ensure noise immunity on transitions, this resistor should not exceed 4.7k. For interfacing to CMOS, the open collector may be returned to a +10V line via a 3.3k resistor. The output sink current must not exceed 10mA, and the use of too low a value of resistor may lead to a loss of noise immunity, especially at low temperatures.
5. Input impedance is a function of frequency. See Fig.4.
6. The rise time of the open collector output waveform is directly proportional to the load capacitance and load resistor value. Therefore the load capacitance should be minimised and the load resistor kept to a minimum compatible with system power requirements. In the test configuration of Fig. 5, the output rise time is approximately 20ns and fall time is 10ns typically.

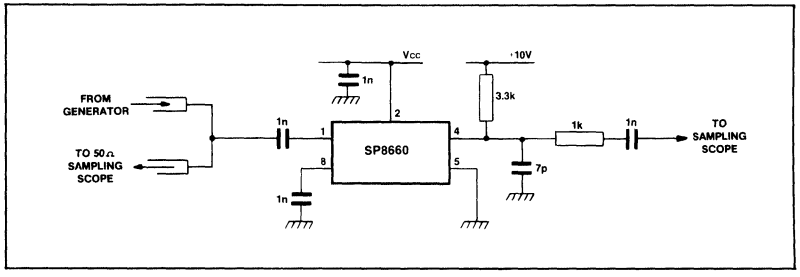


Fig.5 Test circuit

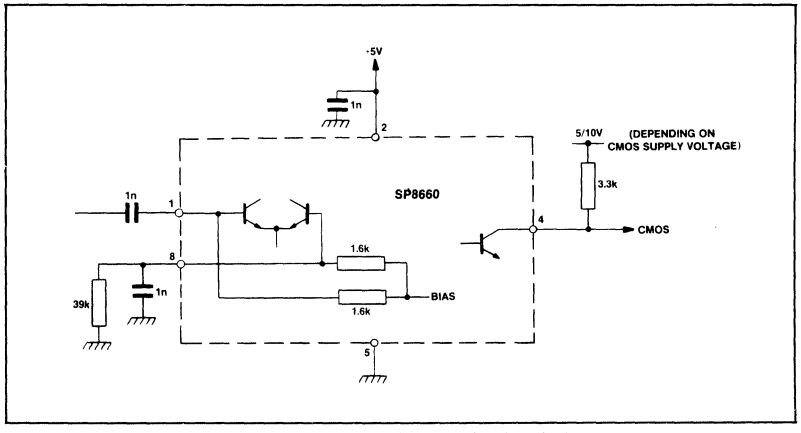


Fig.6 Typical application showing interfacing

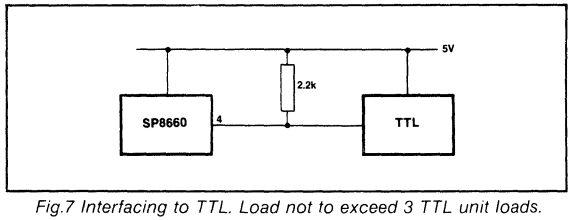


Fig.7 Interfacing to TTL. Load not to exceed 3 TTL unit loads.

SP8660A & B

150MHz ÷ 10

The SP8660A/B is a low power emitter coupled logic counter with an open collector output capable of driving TTL or CMOS. The device is available in two temperature ranges: -55°C to +125°C (A grade) or -30°C to +70°C (B grade). It has internally biased inputs.

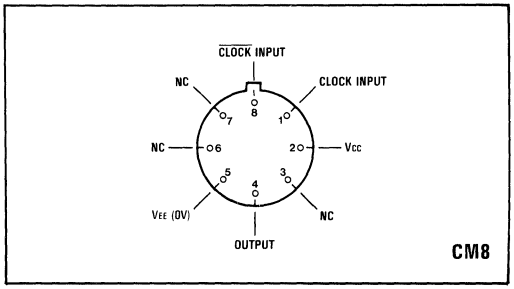


Fig.1 Pin connections - bottom view

FEATURES

- AC Coupled Inputs
- Low Power Consumption
- Open Collector Output CMOS and TTL Compatible

QUICK REFERENCE DATA

- Supply Voltage: 5.0V
- Power Consumption: 50mW
- Temperature Range:
  -55°C to +125°C (SP8660A)
  -30°C to +70°C (SP8660B)

ABSOLUTE MAXIMUM RATINGS

Supply voltage	8V
Open collector output voltage	12V
Storage temperature range	-55°C to +150°C
Max. junction temperature	+175°C
Output sink current	10mA
Max. clock I/P voltage	2.5V p-p

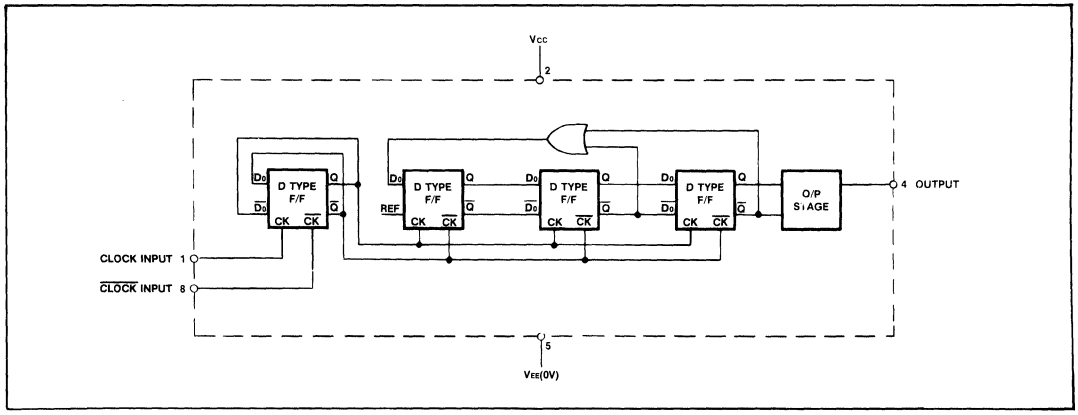


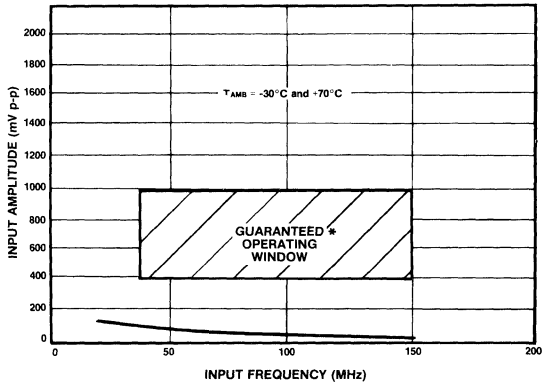
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply voltage: V_{CC} = 5.0V ± 0.25V V_{EE} = 0V
Temperature: A grade T_{amb} = -55°C to +125°C
B grade T_{amb} = -30°C to +70°C

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{max}	150		MHz	Input =400 - 800mV	
Minimum frequency (sinewave input)	f_{min}		40	MHz	Input =400 - 800mV	
Power supply current	I_{EE}		13	mA	V_{CC}= 5.25V	
Output high voltage	V_{OH}	7.5		V	V_{CC}= 5V	
					Pin 4 = 1.5kΩ to 10V	Note 4
Output low voltage	V_{OL}		400	mV	V_{CC} = 5V	
					Pin 4 = 1.5kΩ to 10V	

NOTES
1. Unless otherwise stated the electrical characteristics are guaranteed over specified supply, frequency and temperature range.
2. The dynamic test circuit is shown in Fig.5.
3. Above characteristics are not tested at 25°C (tested at low and high temperature only).
4. $C_{load} \leq 5pF$.



*Tested as specified in table of Electrical Characteristics

Fig.3 Typical input characteristic of SP8660A

OPERATING NOTES

1. The clock inputs (pin 1 and 8) should be capacitively coupled to the signal source. When driven single-ended, the input signal path is completed by connecting a capacitor from the unused input to ground.
2. In the absence of a signal the devices will self-oscillate. This can be prevented by connecting a 39k resistor from either input to ground. If the device is driven single ended, it is recommended that the pulldown resistor be connected to the decoupled unused input. There will be a loss in sensitivity of approximately 200mV.
3. The device will operate down to DC but the input slew rate must be better than 100V/µs.
4. The open collector output will drive 3 TTL loads, and thus requires a suitable resistor to V_{CC} to maintain noise immunity. In order to ensure noise immunity on transitions, this resistor should not exceed 4.7k. For interfacing to CMOS, the open collector may be restored to a +10V line via a 3.3k resistor. The output sink current must not exceed 10mA, and the use of too low a value of resistor may lead to a loss of noise immunity, especially at low temperatures.
5. Input impedance is a function of frequency. See Fig. 4.
6. The rise time of the open collector output waveform is directly proportional to the load capacitance and load resistor value. Therefore the load capacitance should be minimised and the load resistor kept to a minimum compatible with system power requirements. In the test configuration of Fig. 5, the output rise time is approximately 20ns and fall time is 10ns typically.

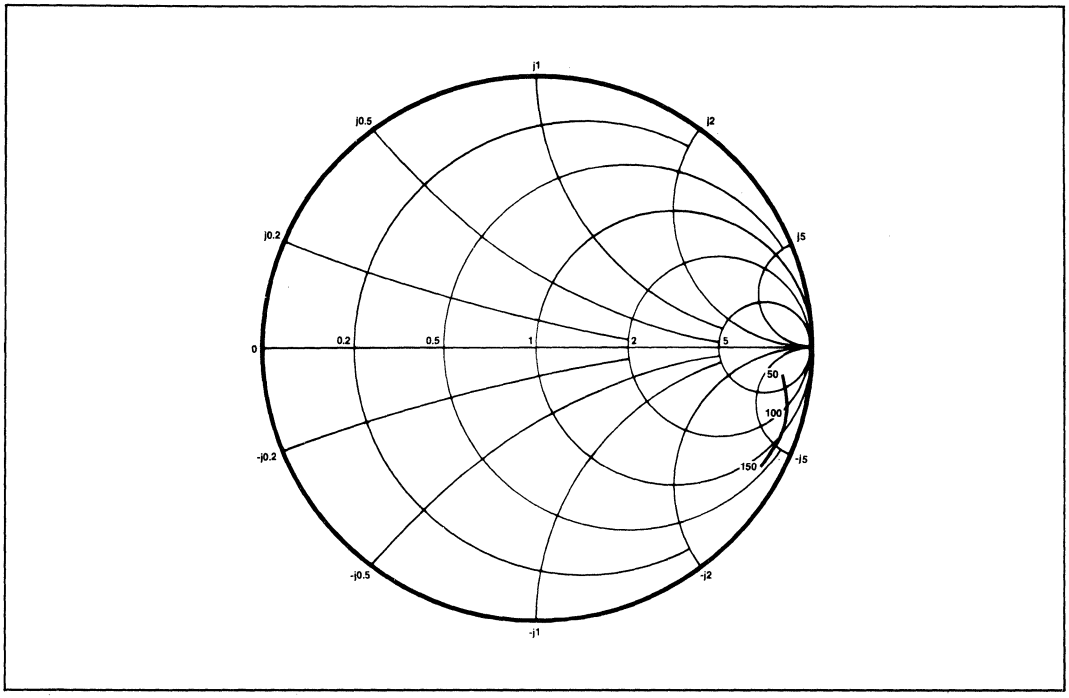


Fig.4 Typical input impedance. Test conditions: supply voltage 5.0V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

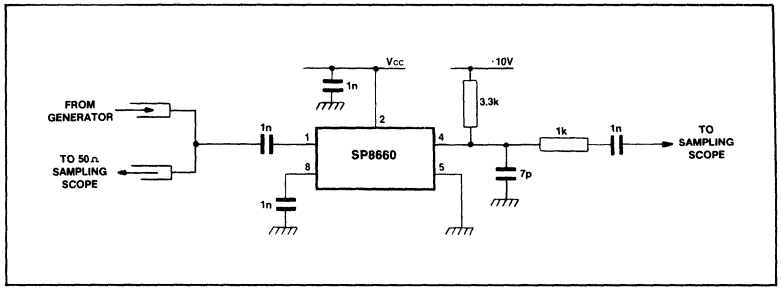


Fig.5 Test circuit

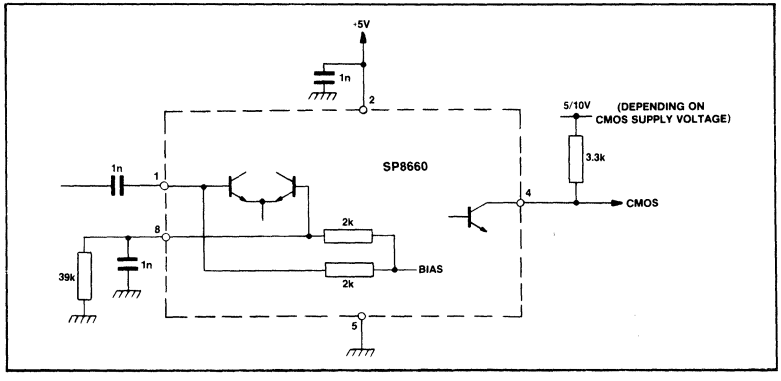


Fig.6 Typical application showing interfacing

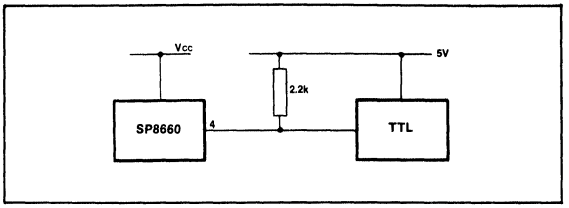


Fig.7 Interfacing to TTL. Load not to exceed 3 TTL unit loads.

SP8665B 1000MHz ÷ 10
SP8668B 1500MHz ÷ 10

The SP8665/8 are asynchronous ECL counters which provide ECL compatible outputs. They feature an ECL compatible input inhibit which simplifies the design of frequency counters and other instrumentation.

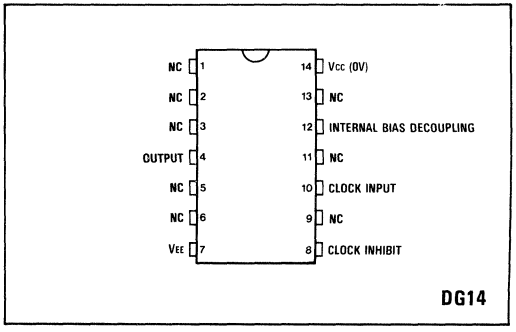


Fig.1 Pin connections - top view

FEATURES

- ECL Compatible Output
- AC Coupled Input
- Clock Inhibit Input

QUICK REFERENCE DATA

- Supply Voltage: -6.8V
- Power Consumption: 500mW
- Temperature Range: 0°C to +70°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage	-8V
Output current	20mA
Storage temperature range	-55°C to +150°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p

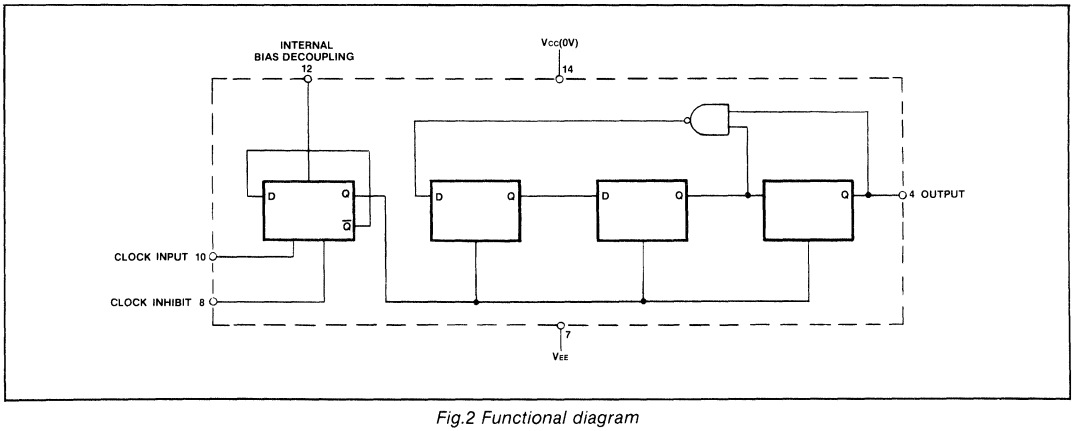


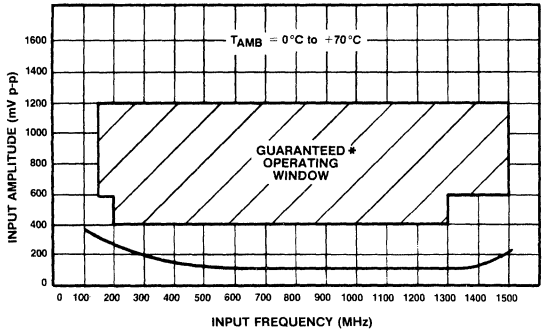
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply voltage: V_{CC} = 0V V_{EE} = -6.8V ± 0.3V
T_{amb} (B grade) = 0°C to +70°C

Characteristic	Symbol	Value Min.	Value Max.	Units	Grade	Conditions	Notes
Maximum frequency(sine wave I/P)	f_{max}	1.0		GHz	SP8665B	Input = 400-1200mV p-p	Note 5
		1.5		GHz	SP8668B	Input = 600-1200mV p-p	Note 5
Minimum frequency(sine wave I/P)	f_{min}		150	MHz	All	Input = 600-1200mV p-p	Note 6
Current consumption	I_{EE}		105	mA	All	V_{EE} = -6.8V	Note 6
Output low voltage	V_{OL}	-1.87	-1.5	V	All	V_{EE} = -6.8V (25° C)	
Output high voltage	V_{OH}	-0.87	-0.7	V	All	V_{EE} = -6.8V (25° C)	
Minimum output swing	V_{OUT}	500		mV	All		Note 5
Clock inhibit high threshold voltage	V_{INBH}	-0.96		V	All	V_{EE} = -6.8V (25° C)	
Clock inhibit low threshold voltage	V_{INBL}		-1.62	V	All	V_{EE} = -6.8V (25° C)	

NOTES
1. Unless otherwise stated the electrical characteristics are guaranteed over specified supply, frequency and temperature range.
2. The test configuration for dynamic testing is shown in Fig.6.
3. The temperature coefficient of V_{OH} = +1.3mV/°C and V_{OL} = +0.5mV/°C but these are not tested.
4. The temperature coefficient of V_{INB} = +0.8mV/°C but this is not tested.
5. Tested at 25°C and 70°C only.
6. Tested at 25°C only.



*Tested as specified in table of Electrical Characteristics

Fig.3 Typical input characteristic SP8668. The SP8665 operating window is similar except for the maximum operating frequency

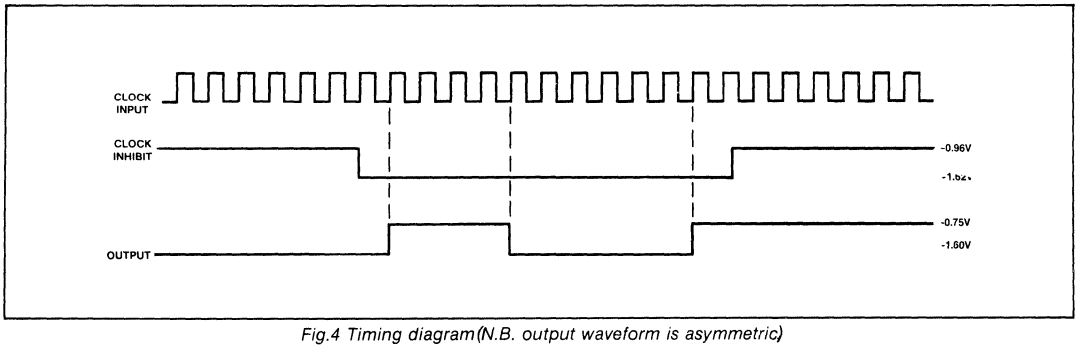


Fig.4 Timing diagram (N.B. output waveform is asymmetric)

OPERATING NOTES

1. The clock input (pin 10) should be capacitively coupled to the signal source. The input signal path is completed by connecting a capacitor from the internal bias decoupling, pin 12, to ground.
2. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 15k resistor from the input to V_{EE} (i.e. Pin 10 to Pin 7). This will reduce the input sensitivity by approximately 100mV.
3. The clock inhibit input is compatible with standard ECL III/10K using a common 0V. A 6k pulldown resistor is included on the chip. The input should be left open to DC when not in use, but should be bypassed for RF signals with a 1nF capacitor to ensure maximum noise immunity.
4. Input impedance is a function of frequency. See Fig. 5.
5. The emitter follower output includes an internal 3k pulldown resistor and is compatible with ECL II, but can be interfaced with ECL III/10K by the inclusion of two resistors. See Fig. 7.
6. Note that all components should be suitable for the frequency in use.
7. The circuit will operate to DC but the input slew rate must be 200V/µs or greater.

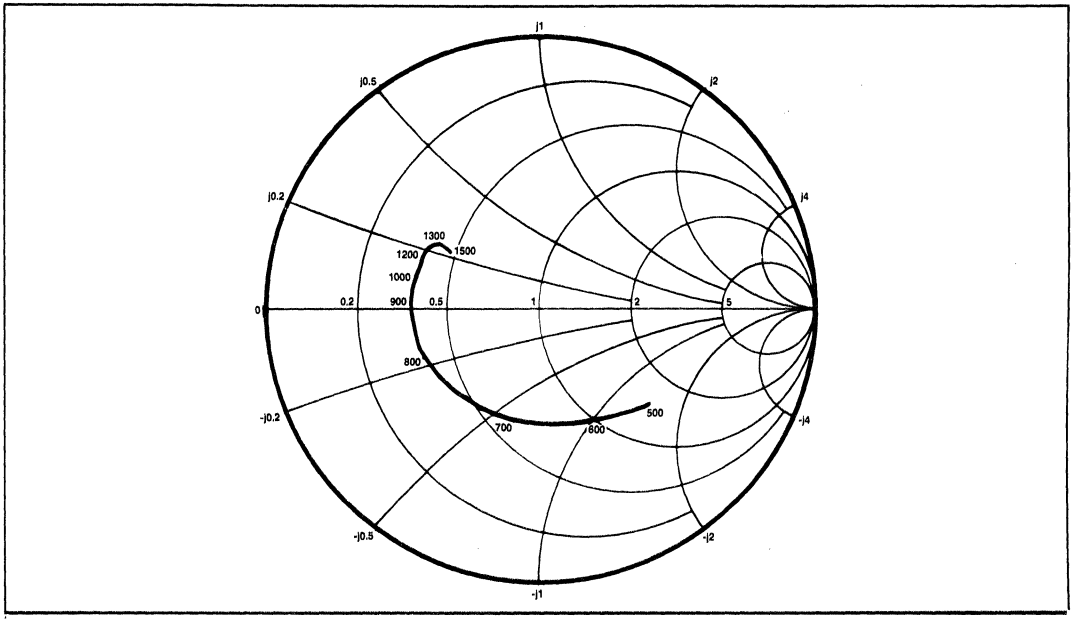


Fig.5 Typical input impedance. Test conditions: supply voltage -6.8V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

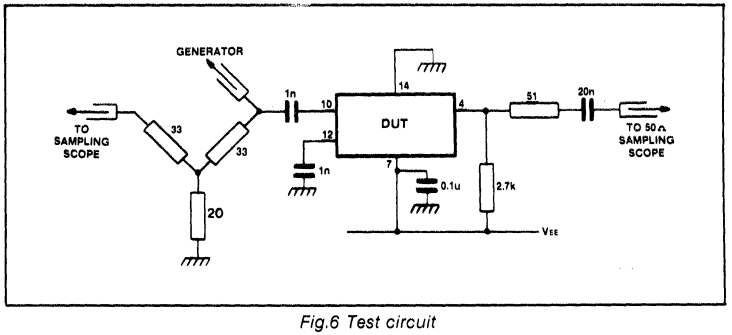


Fig.6 Test circuit

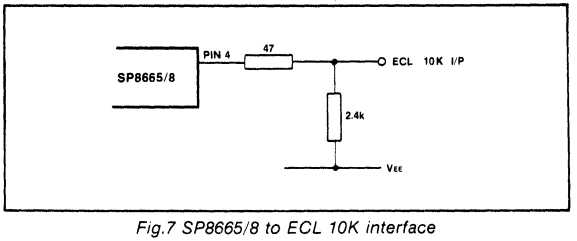


Fig.7 SP8665/8 to ECL 10K interface

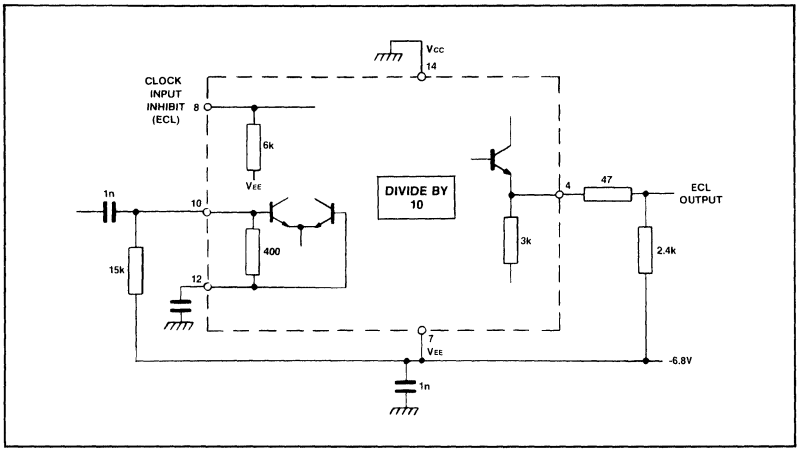


Fig.8 Typical application showing interfacing

SP8670A & B

600MHz ÷ 8

The SP8670 is an asynchronous emitter coupled logic counter which provides ECL 10K compatible outputs when external pulldown resistors are added. It requires an AC coupled input of 600mV p-p.

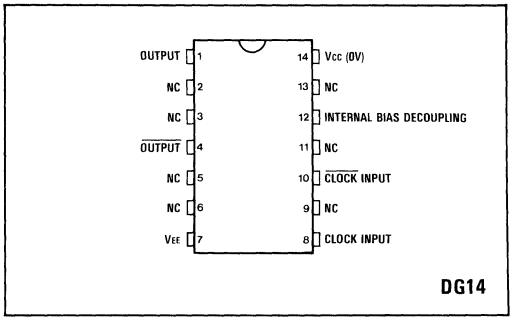


Fig.1 Pin connections - top view

FEATURES

- ECL Compatible Outputs
- AC Coupled Inputs (Internal Bias)

QUICK REFERENCE DATA

- Supply Voltage: -5.2V
- Power Consumption: 300mW
- Temperature Range:
  -55°C to +125°C (A Grade)
  -30°C to +70°C (B Grade)

ABSOLUTE MAXIMUM RATINGS

Supply voltage	-8V
Output current	10mA
Storage temperature range	-55°C to +150°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p

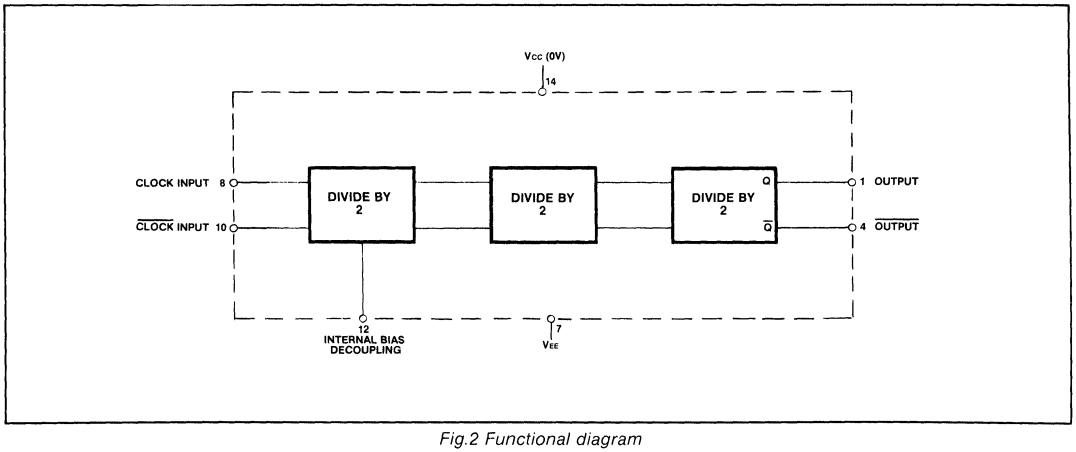


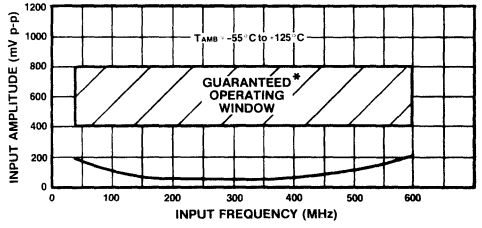
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply voltage: V_{CC} = 0V, V_{EE} = -5.2V ± 0.25V
Temperature: A Grade T_{amb} = -55°C to +125°C
B Grade T_{amb} = -30°C to +70°C

Characteristics	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{max}	600		MHz	Input = 400-800mV p-p	
Minimum frequency (sinewave input)	f_{min}		40	MHz	Input = 400-800mV p-p	Note 4
Power supply current	I_{EE}		60	mA	V_{EE} = -5.2V	Note 4
Output low voltage	V_{OL}	-1.8	-1.5	V	V_{EE} = -5.2V (25° C)	
Output high voltage	V_{OH}	-0.85	-0.7	V	V_{EE} = -5.2V (25° C)	
Minimum output swing	V_{OUT}	500		mV	V_{EE} = -5.2V	

NOTES
1. Unless otherwise stated the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The temperature coefficients of V_{OH} = +1.63mV/°C and V_{OL} = +0.94mV/°C but these are not tested.
3. The test configuration for dynamic testing is shown in Fig.5.
4. Tested at 25°C only.



*Tested as specified in table of Electrical Characteristics

Fig.3 Typical input characteristic of SP8670A

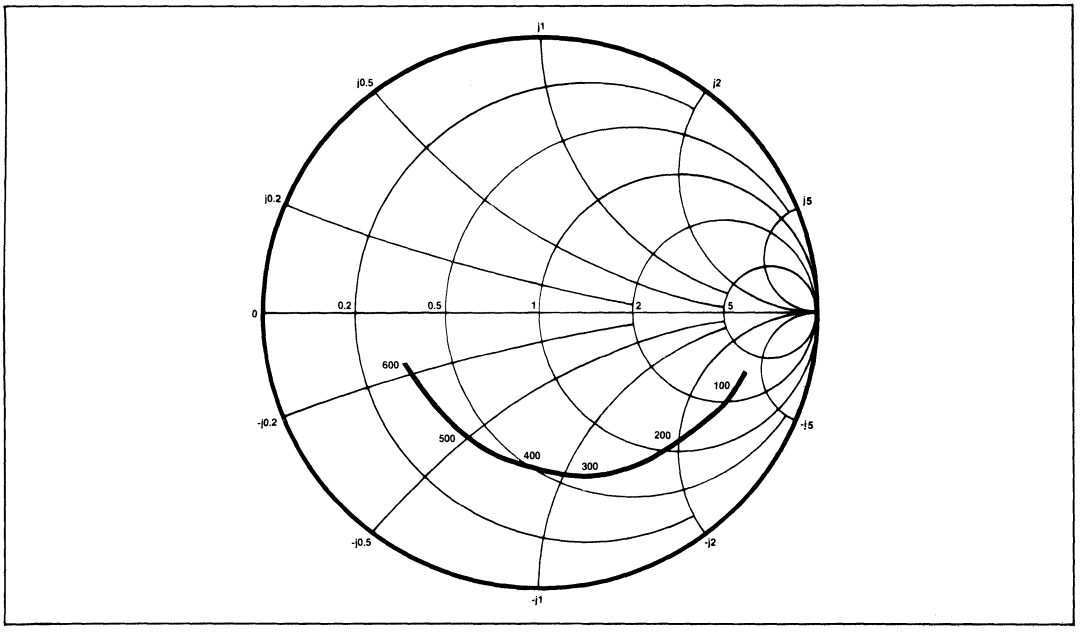


Fig.4 Typical input impedance. Test conditions: supply voltage -5.2V, ambient temperature 25° C, frequencies in MHz, normalised to 50 ohms.

OPERATING NOTES

1. The clock inputs (pins 8 and 10) can be driven single-ended or differentially and should be capacitively coupled to the signal source. The input signal path is completed by connecting a capacitor from the internal bias decoupling, pin 12, to ground.
2. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 10k resistor from one of the inputs to V_{EE}. This will reduce the input sensitivity by approximately 100mV.
3. The circuit will operate down to DC but slew rate must be better than 100V/µs.
4. The outputs are compatible with ECL II. There is an internal load of 4k at each output. The output can be interfaced to ECL 10K by addition of two resistors.
5. Input impedance is shown in Fig. 4.
6. All components should be suitable for the frequency in use.

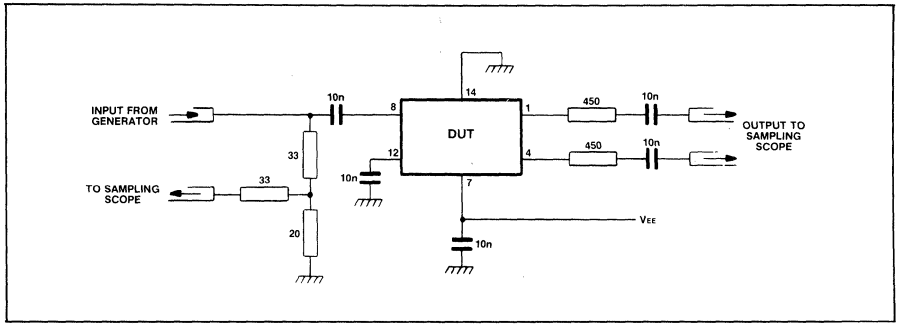


Fig.5 Test circuit

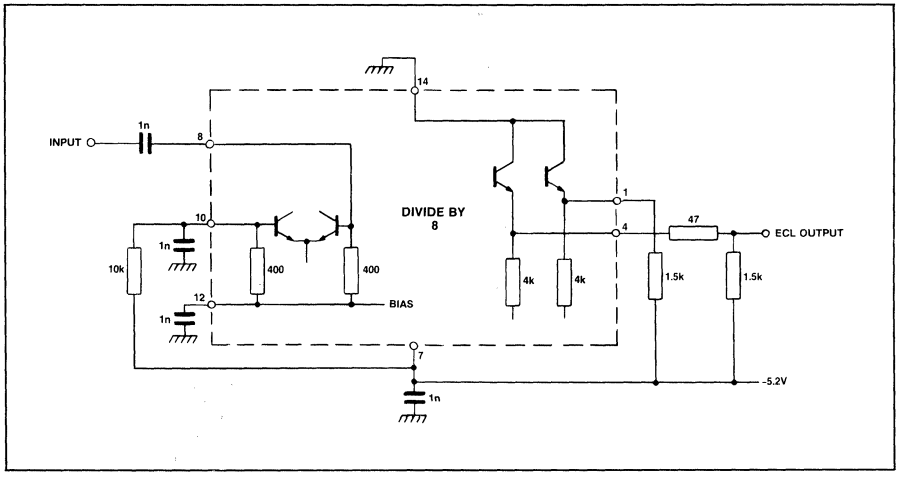


Fig.6 Typical application showing interfacing

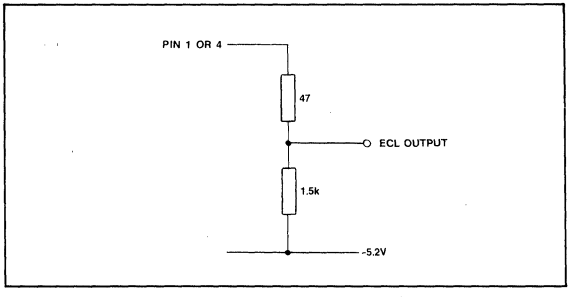


Fig.7 Interfacing to ECL 10K

SP8678B

1500MHz ÷ 8

The SP8678B is an asynchronous ECL counter which provides ECL compatible outputs. It features an ECL compatible input inhibit which simplifies the design of frequency counters and other instrumentation.

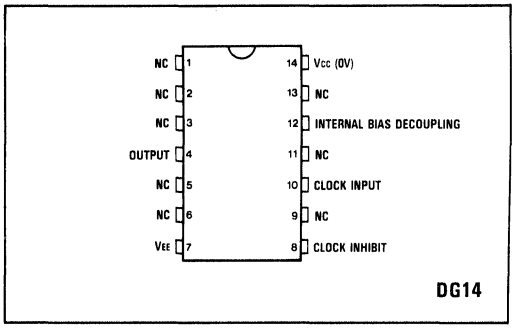


Fig.1 Pin connections - top view

FEATURES

- ECL Compatible Output
- AC Coupled Input
- Clock Inhibit Input

QUICK REFERENCE DATA

- Supply Voltage: -6.8V
- Power Consumption: 475mW
- Temperature Range: 0°C to +70°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage	-8V
Output current	20mA
Storage temperature range	-55°C to +150°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p

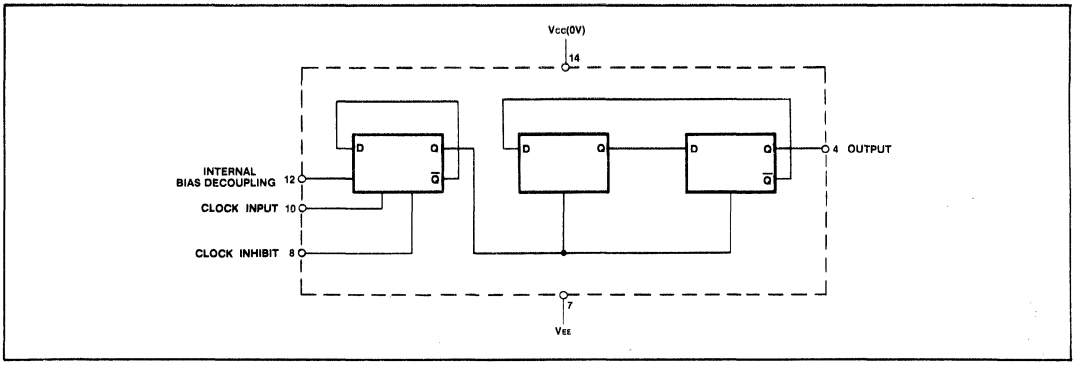


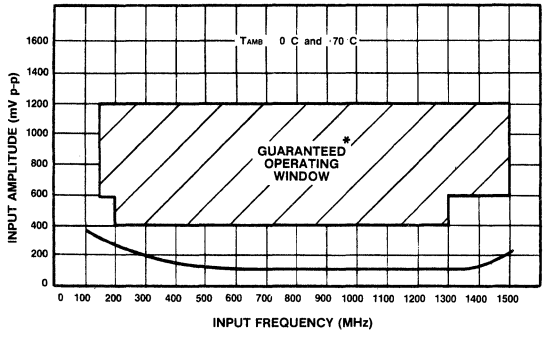
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply voltage: V_{CC} = 0V V_{EE} = -6.8V ± 0.3V
T_{amb} (B grade) = 0°C to +70°C

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{max}	1.5		GHz	Input =600 - 1200mV p-p	Note 5
Minimum frequency (sinewave input)	f_{min}		150	MHz	Input =600 - 1200mV p-p	Note 6
Current consumption	I_{EE}		95	mA	V_{EE} = -6.8V	Note 6
Output low voltage	V_{OL}	-1.87	-1.5	V	V_{EE} = -6.8V(25° C)	
Output high voltage	V_{OH}	-0.87	-0.7	V	V_{EE} = -6.8V(25° C)	
Minimum output swing	V_{OUT}	500		mV		Note 5
Clock inhibit high threshold voltage	V_{INBH}	-0.96		V	V_{EE} = -6.8V(25° C)	
Clock inhibit low threshold voltage	V_{INBL}		-1.62	V	V_{EE} = -6.8V(25° C)	

NOTES
1. Unless otherwise stated, the electrical characteristics are guaranteed over specified supply, frequency and temperature range.
2. The test configuration for dynamic testing is shown in Fig. 6.
3. The temperature coefficient of V_{OH} = +1.3mV/°C and V_{OL} = +0.5mV/°C but these are not tested.
4. The temperature coefficient of V_{INB} = +0.8mV/°C but this is not tested.
5. Tested at 25°C and 70°C only.
6. Tested at 25°C only.



*Tested as specified in table of Electrical Characteristics

Fig.3 Typical input characteristics

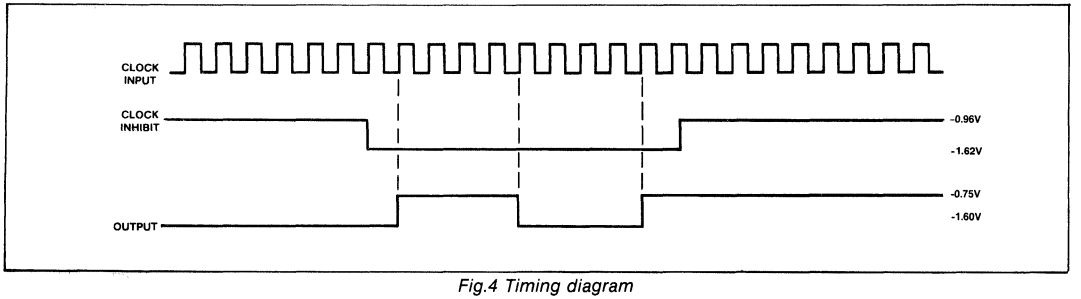


Fig.4 Timing diagram

OPERATING NOTES

1. The clock input (pin 10) should be capacitively coupled to the signal source. The input signal path is completed by connecting a capacitor from the internal bias decoupling, pin 12, to ground.
2. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 15k resistor from the input to V_{EE} (i.e. Pin 10 to Pin 7). This will reduce the input sensitivity by approximately 100mV.
3. The clock inhibit input is compatible with standard ECL III/10K using a common 0V. A 6k pulldown resistor is included on the chip. The input should be left open to DC when not in use, but should be bypassed for RF signals with a 1nF capacitor to ensure maximum noise immunity.
4. Input impedance is a function of frequency. See Fig. 5.
5. The emitter follower output includes an internal 3k pulldown resistor and is compatible with ECL II, but can be interfaced with ECL III/10K by the inclusion of two resistors. See Fig. 7.
6. Note that all components should be suitable for the frequency in use.
7. The circuit will operate to DC but the input slew rate must be 200V/µs or greater.

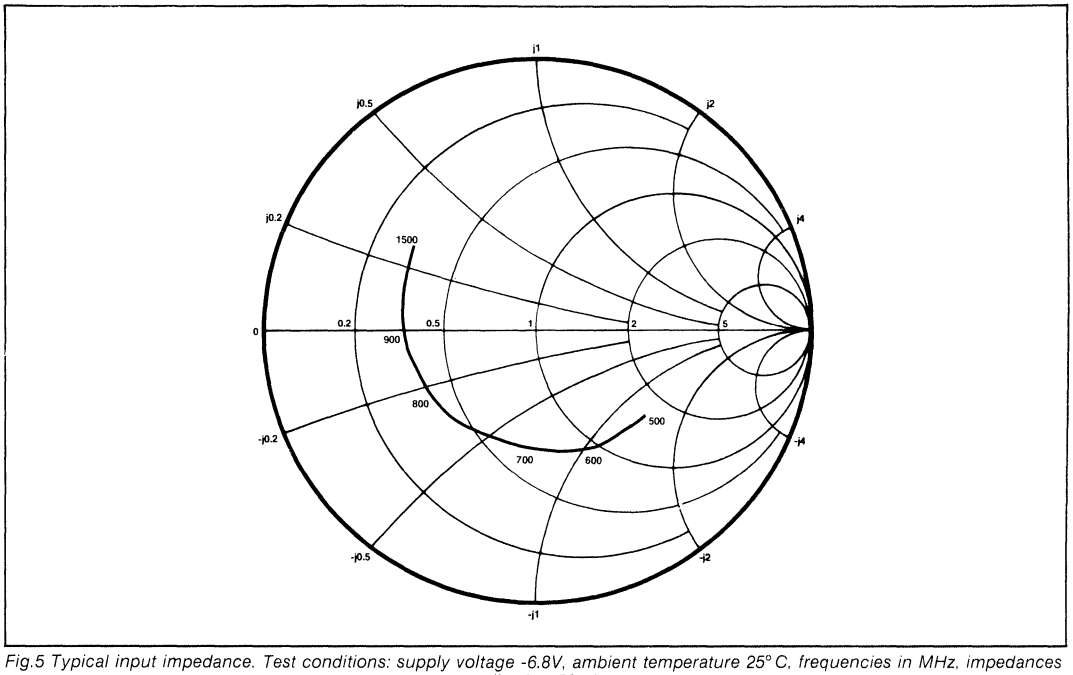


Fig.5 Typical input impedance. Test conditions: supply voltage -6.8V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

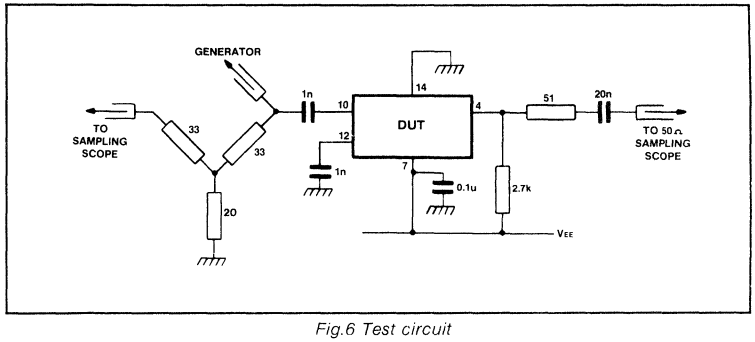


Fig.6 Test circuit

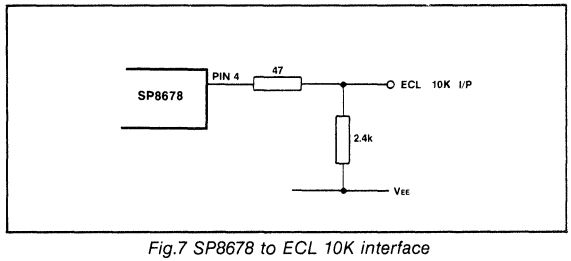


Fig.7 SP8678 to ECL 10K interface

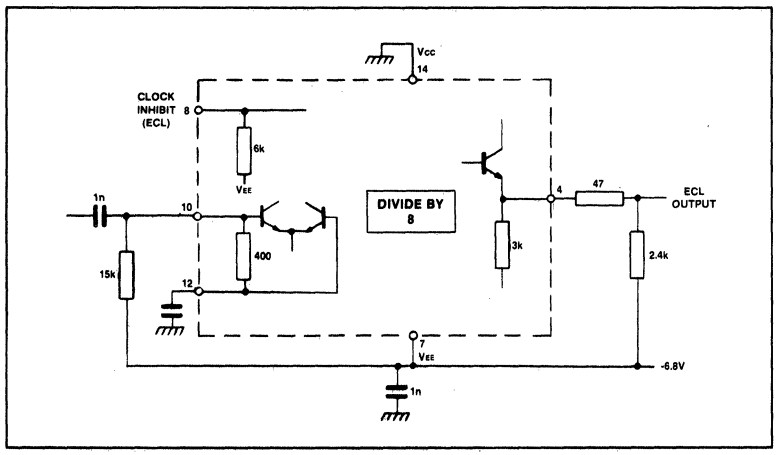


Fig.8 Typical application showing interfacing

SP8680A

600MHz ÷10/11

The SP8680 is an ECL counter with both ECL 10K and TTL compatible outputs. The circuit can operate from either ECL or TTL supplies. The division ratio is controlled by two control inputs (PE1 and PE2) which are ECL compatible. The counter will divide by 10 when either control input is in the high state and by 11 when both inputs are low. The counter can also be set to the eleventh state by applying a high level to the master set input.

FEATURES

- Very High Speed - 650MHz Typ.
- ECL and TTL Compatible Outputs
- DC or AC Clocking
- Clock Enable
- Divide By 10 or 11
- Asynchronous master set
- Equivalent to Fairchild 11C90

QUICK REFERENCE DATA

- Supply Voltage: 5V +0.5V -0.25V
  or -5V -0.5V +0.25V
- Power Consumption: 420mW
- Temperature: -55°C to +125°C

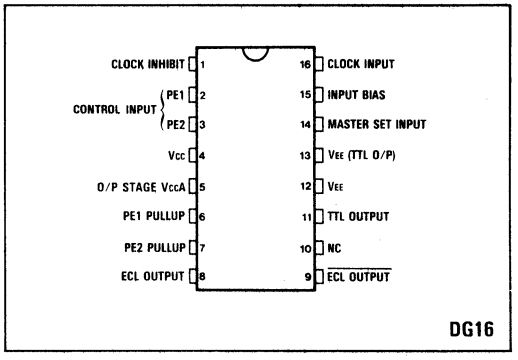


Fig.1 Pin connections - top view

ABSOLUTE MAXIMUM RATINGS

Supply voltage	8V
ECL output source current	50mA
Storage temperature range	-55° C to +150° C
Max. junction temperature	+175° C
TTL output sink current	30mA
Max. clock I/P voltage	2.5V p-p

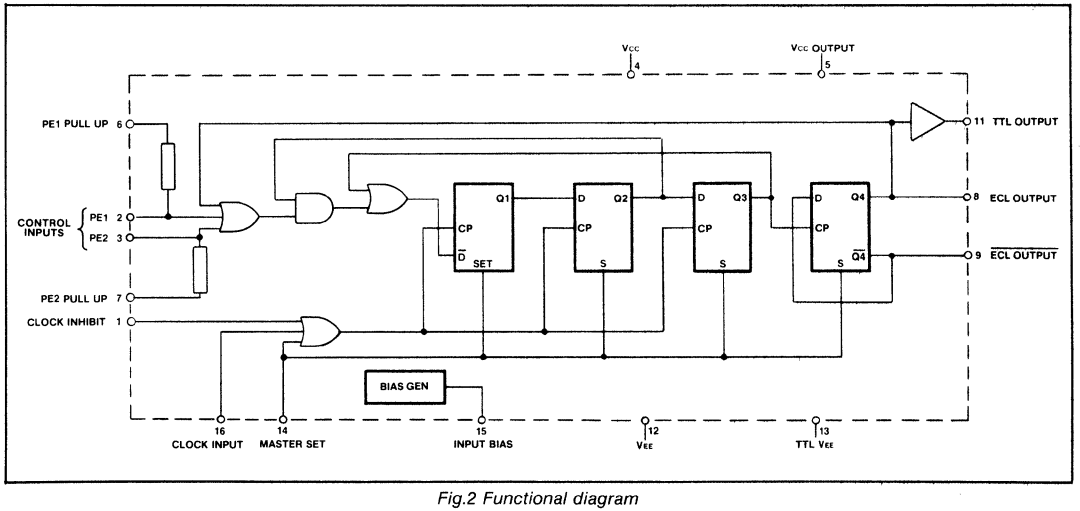


Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS
TTL OPERATION

Supply voltage: $V_{CC} = V_{CCA} = 4.75$ to $5.5V$ $V_{EE} = 0V$
Temperature: $T_{amb} = -55°C$ to $+125°C$

Characteristics	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency sinewave input	f_{max}		550	MHz	Clock input AC coupled = 350mV p-p	Note 4
Minimum frequency sinewave input	f_{min}	10		MHz	Clock input AC coupled = 600mV p-p	Note 5
Power supply current	I_{EE}		105	mA	$V_{CC} = V_{CC}$ max. Pins 6,7,13 open circuit	Note 4
Power supply current including TTL stage	I_{EE}		111	mA	$V_{CC} = V_{CC}$ max. Pins 6,7 open circuit	Note 4
TTL output high voltage	V_{OH}	2.3		V	$V_{CC} = V_{CC}$ min. $I_{OH} = -640\mu A$	Note 4
TTL output low voltage	V_{OL}		0.5	V	$V_{CC} = V_{CC}$ max. $I_{OL} = -20mA$	Note 4
Input high voltage PE1 and PE2 inputs	V_{INH}	3.9		V	$V_{CC} = 5.0V$ (25°C)	
Input low voltage PE1 and PE2 inputs	V_{INL}		3.5	V	$V_{CC} = 5.0V$ (25°C)	
Input low current PE1 and PE2 inputs	I_{IL}	-4		mA	$V_{CC} = V_{CC}$ max. (25°C) Pins 6,7 = V_{CC} $V_{IN} = 0.4V$	
Propagation delay CP to Q TTL	t_{pHL} t_{pLH}	6	14	ns	$V_{CC} = 5.0V$ (25°C)	Note 5
Propagation delay MS to Q TTL	t_p		17	ns	$V_{CC} = 5.0V$ (25°C)	Note 5
Mode control set-up time	t_s	4		ns	$V_{CC} = 5.0V$ (25°C)	Note 5
Mode control release time	t_r	4		ns	$V_{CC} = 5.0V$ (25°C)	Note 5
TTL output rise time (20 % - 80 %)	t_{TLH}		5	ns	$V_{CC} = 5.0V$ (25°C)	Note 5
TTL output fall time (80 % - 20 %)	t_{THL}		5	ns	$V_{CC} = 5.0V$ (25°C)	Note 5

ELECTRICAL CHARACTERISTICS
ECL OPERATION

Supply Voltage: $V_{EE} = -4.75V$ to $-5.5V$ $V_{CC} = 0V$
Temperature: $T_{amb} = -55°C$ to $+125°C$

Characteristics	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency sinewave input	f_{max}		550	MHz	Clock input AC coupled = 350mV p-p	Note 4
Minimum frequency sinewave input	f_{min}	10		MHz	Clock input AC coupled = 600mV p-p	Note 5
Power supply current	I_{EE}		105	mA	$V_{CC} = V_{CC}$ max. Pins 6,7,13 open circuit	Note 4
ECL output high voltage	V_{OH}	-0.93	-0.78	V	$V_{EE} = -5.2V$ (25°C) Load = 100Ω to -2V	
ECL output low voltage	V_{OL}	-1.85	-1.62	V	$V_{EE} = -5.2V$ (25°C) Load = 100Ω to -2V	
Input high voltage	V_{INH}	-1.095	-0.81	V	$V_{EE} = -5.2V$ (25°C)	
Input low voltage	V_{INL}	-1.85	-1.475	V	$V_{EE} = -5.2V$ (25°C)	
Input low currents	I_{IL}	0.5		μA	25°C	
Input high current						
Clock and MS	I_H		400	μA	$V_{IN} = -1.85V$ (25°C)	
PE1 and PE2	I_H		250	μA	$V_{IN} = -0.8V$ (25°C)	

ELECTRICAL CHARACTERISTICS - ECL OPERATION (CONT.)

Characteristics	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Propagation delay CP to Q4	t_{PHL}		4	ns	Load = 100Ω to -2V (25°C)	Note 5
	t_{PLH}		3	ns		
Propagation delay MS to Q4	t_{PLH}		6	ns	25°C	Note 5
Mode control set-up time	t_s	4		ns	25°C	Note 5
Mode control release time	t_r	4		ns	25°C	Note 5
ECL output rise time (20 % - 80 %)	t_{TLH}		2	ns	25°C	Note 5
ECL output fall time (80 % - 20 %)	t_{THL}		2	ns	25°C	Note 5

NOTES
1. Unless otherwise stated, the electrical characteristics are guaranteed over specified supply, frequency and temperature range.
2. The temperature coefficient of V_{OH} = +1.2mV/°C, V_{OL} = +0.24mV/°C and of V_{IN} = +0.8mV/°C but these are not tested.
3. The test configuration for dynamic testing is shown in Fig.6.
4. Tested at 25°C and +125°C only.
5. Guaranteed but not tested.

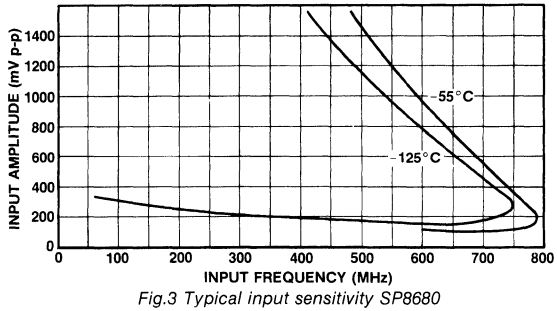
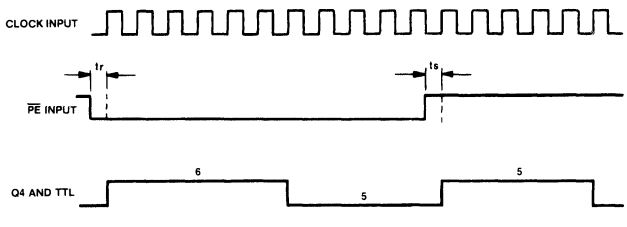


Fig.3 Typical input sensitivity SP8680



MS	CLOCK INH.	PE1	PE2	OUTPUT RESPONSE
H	X	X	X	ALL OUTPUTS SET HIGH
L	H	X	X	HOLD
L	L	L	L	÷11
L	L	H	L	÷10
L	L	L	H	÷10
L	L	H	H	÷10

X = DON'T CARE

Fig.4 Truth table and timing diagram SP8680

NOTE:
The set-up time t_s is defined as minimum time that can elapse between L→H transition of control input and the next L→H clock pulse transition to ensure that the ÷10 mode is obtained.
The release time t_r is defined as the minimum time that can elapse between a H→L transition of control input and the next L→H clock pulse transition to ensure that the ÷11 mode is obtained.

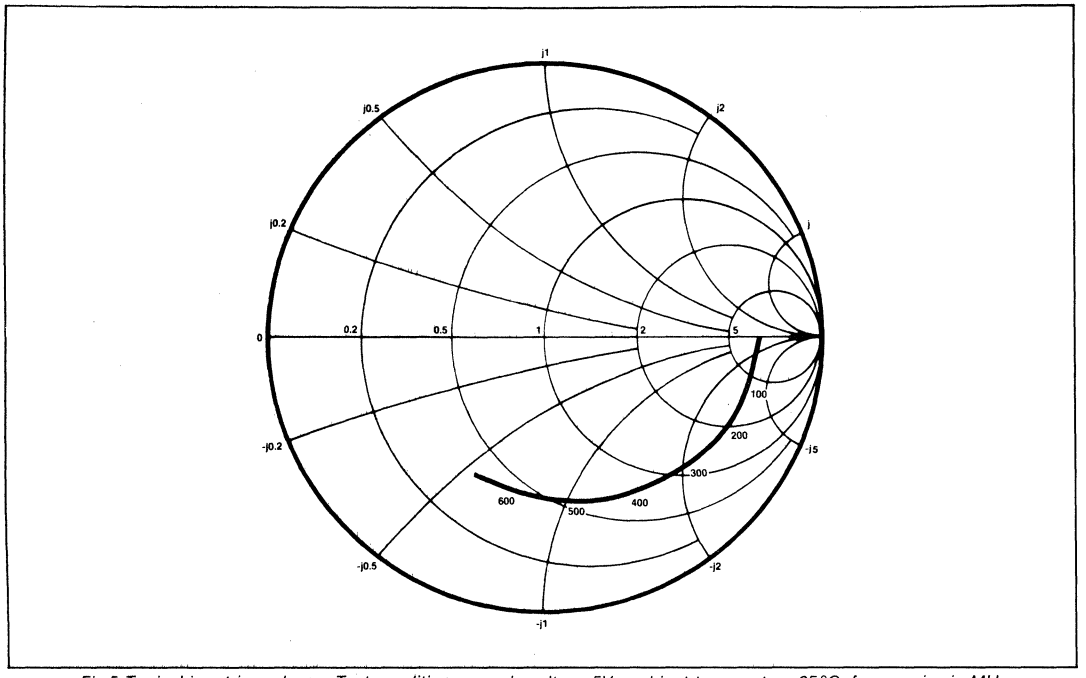


Fig.5 Typical input impedance. Test conditions: supply voltage 5V, ambient temperature 25°C, frequencies in MHz, impedances normalised to 50 ohms.

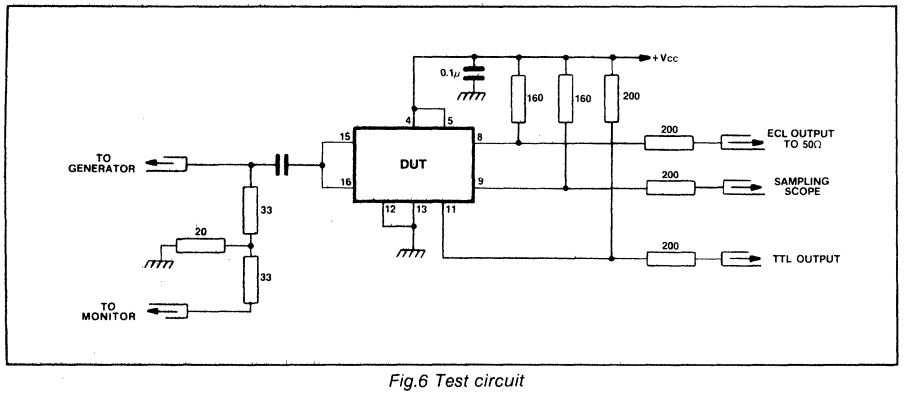


Fig.6 Test circuit

OPERATING NOTES

1. The clock input, which is ECL 10K compatible throughout the temperature range, can also be directly coupled to TTL as shown in Fig.9. The clock can also be capacitively coupled to the signal source (see Fig.7). Connecting the internally-generated bias voltage to the clock input, i.e. pin 15 to pin 16 centres the clock input about the switching threshold (see Fig.8).
2. The two complementary outputs are ECL 10K compatible but internal pulldown resistors are not included, and thus an external resistor to V_{EE} is required.
3. The TTL totem pole output operates with the same supply and is powered up by connecting V_{EE} (pin 12) to TTL V_{EE} (pin 13). If the TTL output is not required then the TTL V_{EE} (pin 13) should be left open-circuit reducing the power consumption by 20mW.
4. Both control inputs (PE1 and PE2) are ECL 10K compatible throughout the temperature range. Each control input is provided with a pull up resistor, the remote ends of which are connected to pins 6 and 7. This allows the pull up resistors to be unused if so desired, or to be used to interface from TTL (see Fig.9). If interfacing to ECL is required then pins 6 and 7 should be left open circuit: alternatively they can be connected to V_{EE} to act as pull-down resistors. When high, the master set input sets the counter to the eleventh state, is asynchronous, and overrides the clock input.
5. All the inputs have an internal pull-down resistor of 50k.
6. The device will operate down to DC but input slew rate must be better than 20V/μs.
7. Input impedance is a function of frequency. See Fig.5.

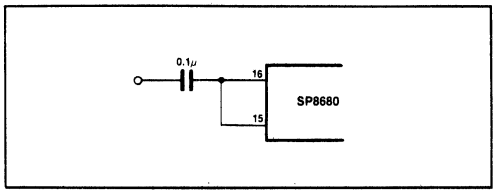


Fig.7 AC coupled input

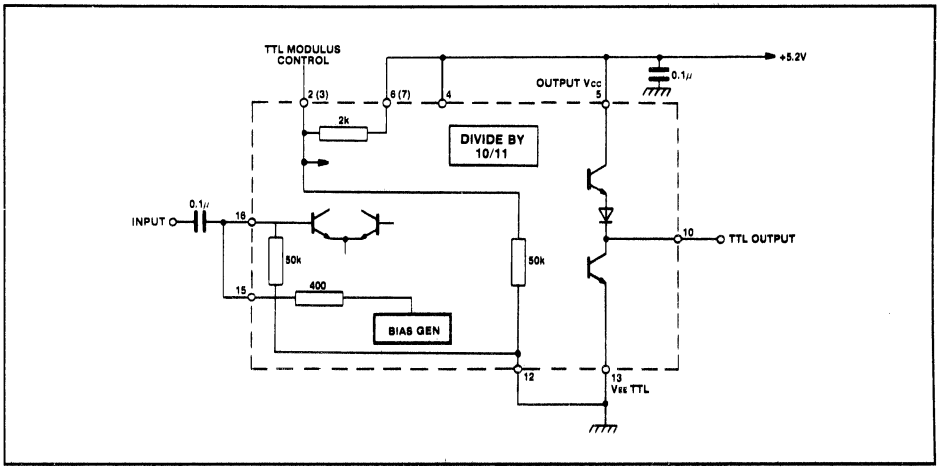


Fig.8 Typical application showing interfacing

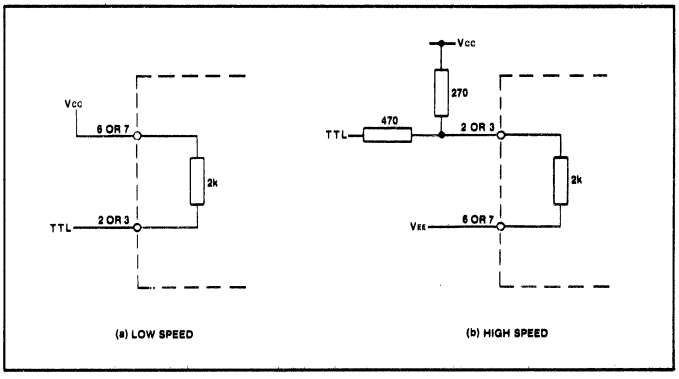


Fig.9 TTL interface to PE1 and PE2

PLESSEY
Semiconductors

SP8680B

600MHz ÷ 10/11

The SP8680 is an ECL counter with both ECL 10K and TTL compatible outputs. The circuit can operate from either ECL or TTL supplies. The division ratio is controlled by two control inputs (PE1 and PE2) which are ECL compatible. The counter will divide by 10 when either control input is in the high state and by 11 when both inputs are low. The counter can also be set to the eleventh state by applying a high level to the master set input.

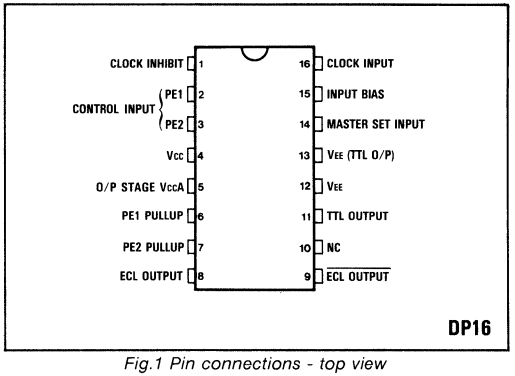


Fig.1 Pin connections - top view

FEATURES

- Very High Speed - 650MHz Typ.
- ECL and TTL Compatible Outputs
- DC or AC Clocking
- Clock Enable
- Divide By 10 or 11
- Asynchronous master set
- Equivalent to Fairchild 11C90

QUICK REFERENCE DATA

- Supply Voltage: 5V +0.5V -0.25V
  or -5V -0.5V +0.25V
- Power Consumption: 420mW
- Temperature: -40°C to +85°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage	8V
ECL output source current	50mA
Storage temperature range	-55°C to +125°C
Max. junction temperature	+175°C
TTL output sink current	30mA
Max. clock I/P voltage	2.5V p-p

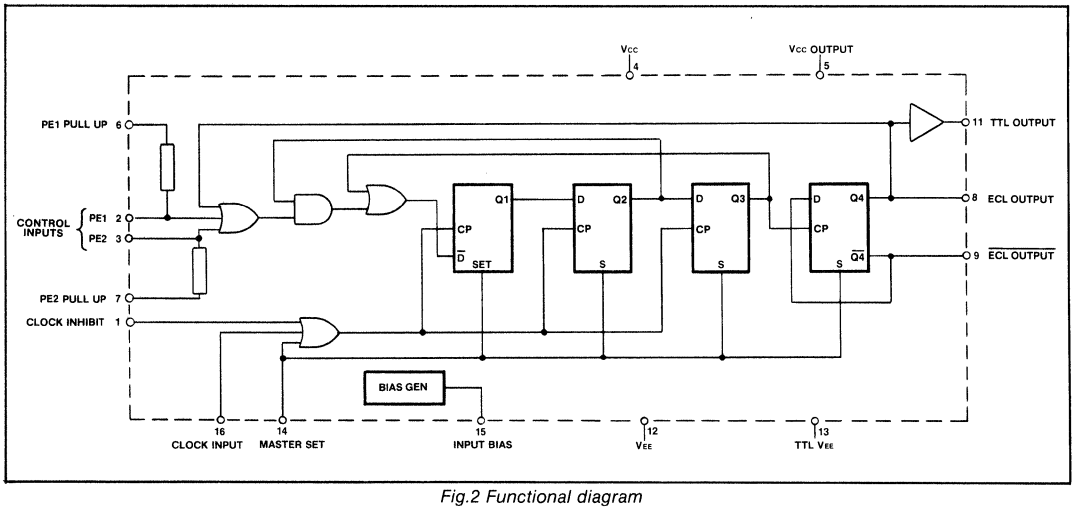


Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS
TTL OPERATION
Test conditions (unless otherwise stated):
T_{amb} = -40°C to +85°C Supply voltage: $V_{CC} = V_{CCA}$ = 4.75 to 5.5V V_{EE} = 0V

Characteristics	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency sinewave input	f_{max}		575	MHz	Clock input AC coupled = 350mV p-p	
Minimum frequency sinewave input	f_{min}	10		MHz	Clock input AC coupled = 600mV p-p	Note 4
Power supply current	I_{EE}		105	mA	$V_{CC} = V_{CC}$ max. Pins 6,7,13 open circuit	
Power supply current including TTL stage	I_{EE}		111	mA	$V_{CC} = V_{CC}$ max. Pins 6,7 open circuit	
TTL output high voltage	V_{OH}	2.3		V	$V_{CC} = V_{CC}$ min. I_{OH} = -640μA	
TTL output low voltage	V_{OL}		0.5	V	$V_{CC} = V_{CC}$ max. I_{OL} = -20mA	
Input high voltage PE1 and PE2 inputs	V_{INH}	3.9		V	V_{CC} = 5.0V (25°C)	
Input low voltage PE1 and PE2 inputs	V_{INL}		3.5	V	V_{CC} = 5.0V (25°C)	
Input low current PE1 and PE2 inputs	I_{IL}	-4		mA	$V_{CC} = V_{CC}$ max. (25°C) Pins 6,7 = V_{CC} V_{IN} = 0.4V	
Propagation delay CP to Q TTL	t_{pHL} t_{pLH}	6	14	ns	V_{CC} = 5.0V (25°C)	Note 4
Propagation delay MS to Q TTL	t_p		17	ns	V_{CC} = 5.0V (25°C)	Note 4
Mode control set-up time	t_s	4		ns	V_{CC} = 5.0V (25°C)	Note 4
Mode control release time	t_r	4		ns	V_{CC} = 5.0V (25°C)	Note 4
TTL output rise time (20 % - 80 %)	t_{TLH}		5	ns	V_{CC} = 5.0V (25°C)	Note 4
TTL output fall time (80 % - 20 %)	t_{THL}		5	ns	V_{CC} = 5.0V (25°C)	Note 4

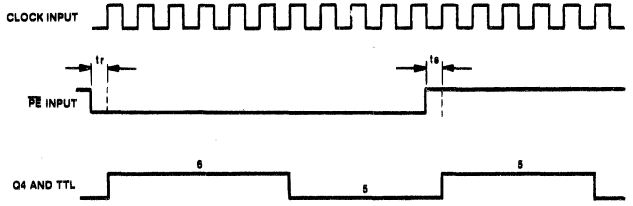
ELECTRICAL CHARACTERISTICS
ECL OPERATION
Test conditions (unless otherwise stated):
T_{amb} = -40°C to +85°C Supply Voltage: V_{EE} = -4.75V to -5.5V V_{CC} = 0V

Characteristics	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency sinewave input	f_{max}		575	MHz	Clock input AC coupled = 350mV p-p	
Minimum frequency sinewave input	f_{min}	10		MHz	Clock input AC coupled = 600mV p-p	Note 4
Power supply current	I_{EE}		105	mA	$V_{CC} = V_{CC}$ max. Pins 6,7,13 open circuit	
ECL output high voltage	V_{OH}	-0.93	-0.78	V	V_{EE} = -5.2V (25°C) Load = 100Ω to -2V	
ECL output low voltage	V_{OL}	-1.85	-1.62	V	V_{EE} = -5.2V (25°C) Load = 100Ω to -2V	
Input high voltage	V_{INH}	-1.095	-0.81	V	V_{EE} = -5.2V (25°C)	
Input low voltage	V_{INL}	-1.85	-1.475	V	V_{EE} = -5.2V (25°C)	

ELECTRICAL CHARACTERISTICS - ECL OPERATION (CONT.)

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Input low currents	I_{IL}	0.5		μA	25° C	
Input high current						
Clock and MS	I_H		400	μA	V_{IN} = -1.85V(25° C)	
PE1 and PE2	I_H		250	μA	V_{IN} = -0.8V(25° C)	
Propagation delay CP to Q4	t_{pLH}		3	ns	Load = 100Ω to -2V(25° C)	Note 4
Propagation delay MS to Q4	t_{pLH}		6	ns	25° C	Note 4
Mode control set-up time	t_s	4		ns	25° C	Note 4
Mode control release time	t_r	4		ns	25° C	Note 4
ECL output rise time (20 % - 80 %)	t_{TLH}		2	ns	25° C	Note 4
ECL output fall time (80 % - 20 %)	t_{THL}		2	ns	25° C	Note 4

NOTES
1. Unless otherwise stated, the electrical characteristics are guaranteed over specified supply, frequency and temperature range.
2. The temperature coefficient of V_{OH} = +1.2mV/ °C, V_{OL} = +0.25mV/ °C and of V_{IN} = +0.8mV/ °C but these are not tested.
3. The test configuration for dynamic testing is shown in Fig.5
4. Guaranteed but not tested.



MS	CLOCK INH.	PE1	PE2	OUTPUT RESPONSE
H	X	X	X	ALL OUTPUTS SET HIGH
L	H	X	X	HOLD
L	L	L	L	+11
L	L	H	L	+10
L	L	L	H	+10
L	L	H	H	+10

X = DON'T CARE

Fig.3 Truth table and timing diagram SP8680

NOTE:
The set-up time t_s is defined as minimum time that can elapse between L→H transition of control input and the next L→H clock pulse transition to ensure that the ÷10 mode is obtained.
The release time t_r is defined as the minimum time that can elapse between a H→L transition of control input and the next L→H clock pulse transition to ensure that the ÷11 mode is obtained.

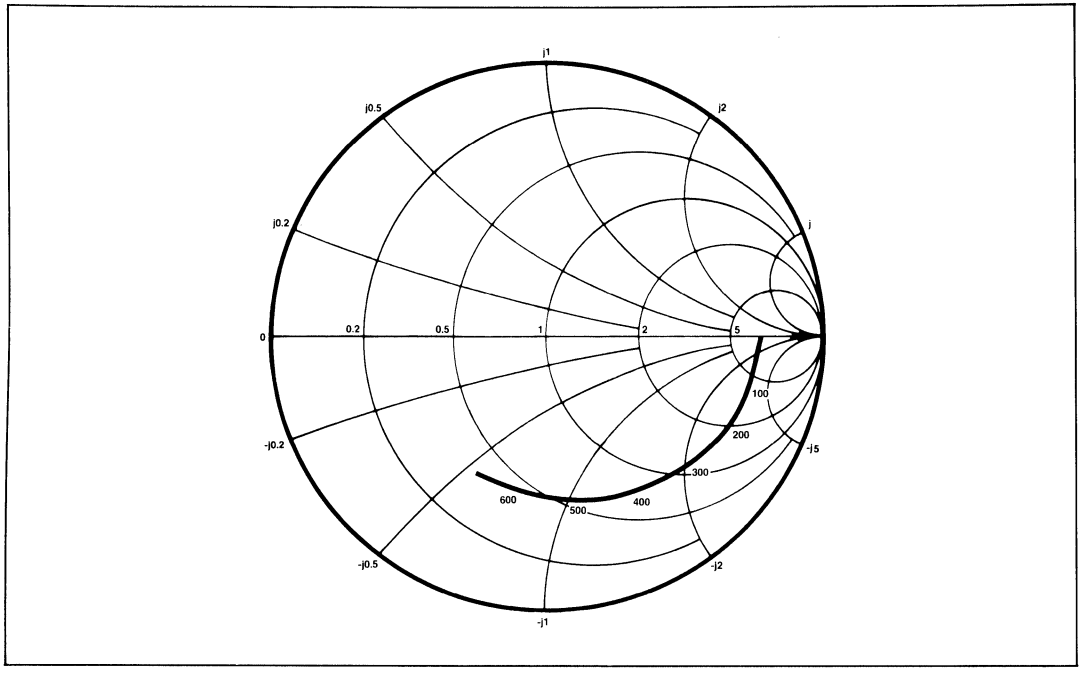


Fig.4 Typical input impedance. Test conditions: supply voltage 5V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

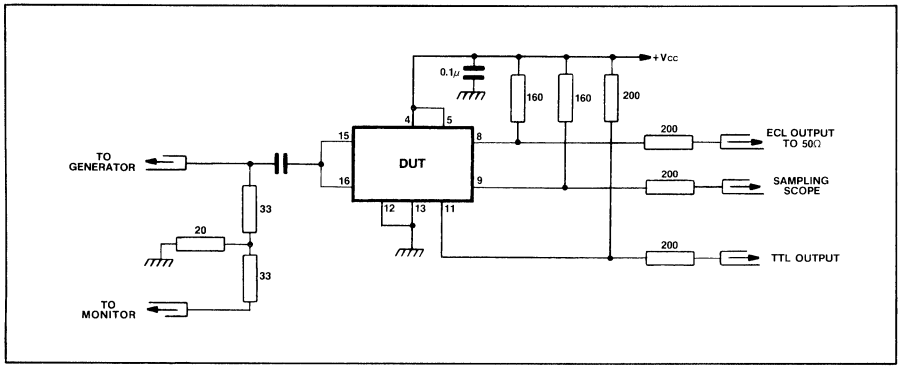


Fig.5 Test circuit

OPERATING NOTES

1. The clock input, which is ECL 10K compatible throughout the temperature range, can also be directly coupled to TTL as shown in Fig.8. The clock can also be capacitively coupled to the signal source (see Fig.6). Connecting the internally-generated bias voltage to the clock input, i.e. pin 15 to pin 16 centres the clock input about the switching threshold (see Fig.7).
2. The two complementary outputs are ECL 10K compatible but internal pulldown resistors are not included, and thus an external resistor to V_{EE} is required. The outputs are capable of driving a 50 ohm load to -2V over the temperature range -40° C to +85° C. The output high level will typically be reduced by 50mV.
3. The TTL totem pole output operates with the same supply and is powered up by connecting V_{EE} (pin 12) to TTL V_{EE} (pin 13). If the TTL output is not required then the TTL V_{EE} (pin 13) should be left open-circuit reducing the power consumption by 20mV.
4. Both control inputs (PE1 and PE2) are ECL 10K compatible throughout the temperature range. Each control input is provided with a pull up resistor, the remote ends of which are connected to pins 6 and 7. This allows the pull up resistors to be unused if so desired, or to be used to interface from TTL (see Fig.8). If interfacing to ECL is required then pins 6 and 7 should be left open circuit: alternatively they can be connected to V_{EE} to act as pull-down resistors. When high, the master set input sets the counter to the eleventh state, is asynchronous, and overrides the clock input.
5. All the inputs have an internal pull-down resistor of 50k.
6. The device will operate down to DC but input slew rate must be better than 20V/μs.
7. Input impedance is a function of frequency. See Fig.4.

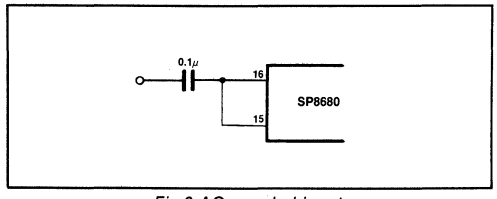


Fig.6 AC coupled input

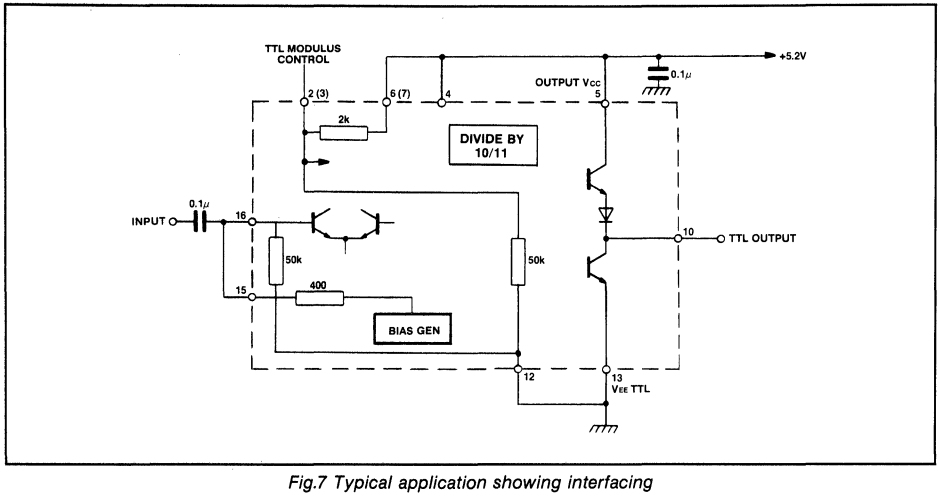


Fig.7 Typical application showing interfacing

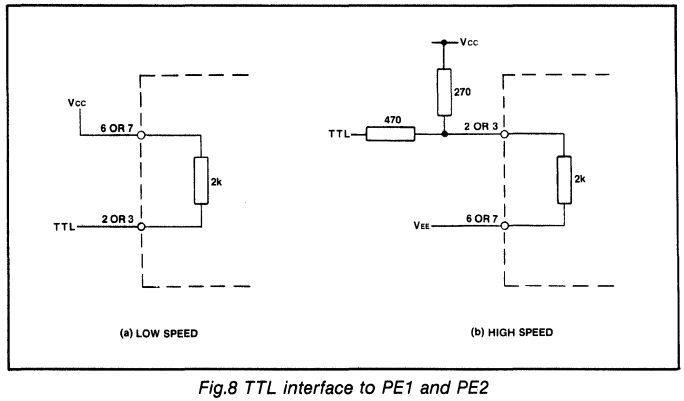


Fig.8 TTL interface to PE1 and PE2

SP8685A&B

500MHz ÷ 10/11

The SP8685 is an ECL variable modulus divider, with ECL 10K compatible outputs. It divides by 10 when either of the ECL control inputs, $\overline{PE1}$ or $\overline{PE2}$, is in the high state and by 11 when both are low (or open circuit).

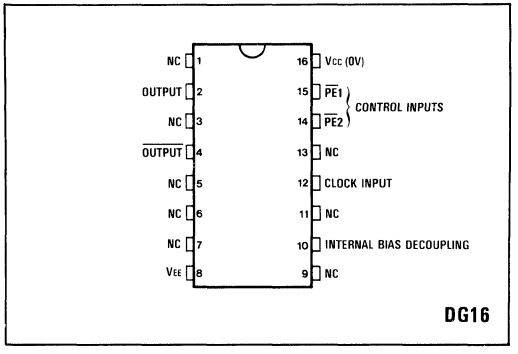


Fig.1 Pin connections - top view

FEATURES

- Divides by 10 and 11
- AC Coupled Input (Internal Bias)
- ECL Compatible Output

QUICK REFERENCE DATA

- Supply Voltage: -5.2V
- Power Consumption: 300mW
- Temperature Range:
  -55°C to +125°C (A Grade)
  -30°C to +70°C (B Grade)

ABSOLUTE MAXIMUM RATINGS

Supply voltage	-8V
Output current	20mA
Storage temperature range	-55°C to +150°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p

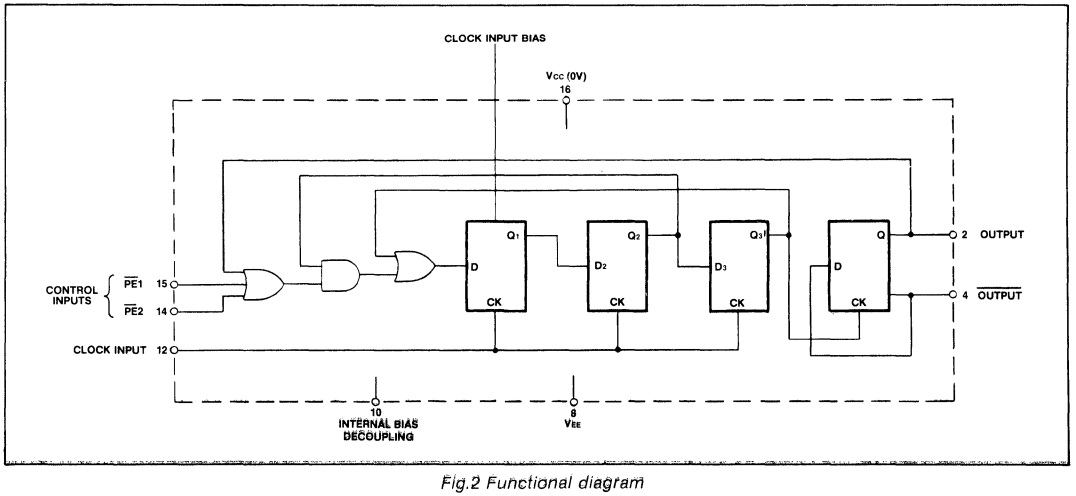


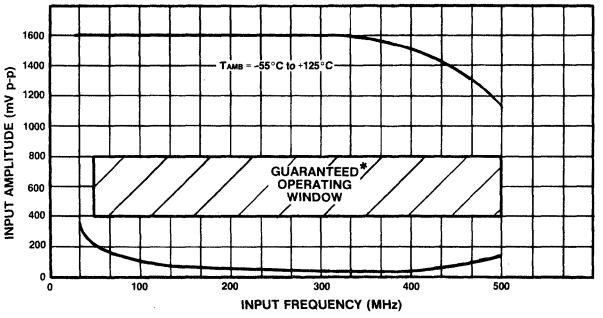
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply Voltage: V_{CC} = 0V V_{EE} = -5.2V ± 0.25V
Temperature: A Grade T_{amb} = -55°C to +125°C
B Grade T_{amb} = -30°C to +70°C

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{max}	500		MHz	Input = 400-800mV p-p	
Minimum frequency (sinewave input)	f_{min}		50	MHz	Input = 400-800mV p-p	Note 6
Power supply current	I_{EE}		70	mA	V_{EE} = -5.2V	Note 6
Output high voltage	V_{OH}	-0.87	-0.7	V	V_{EE} = -5.2V (25°C)	
Output low voltage	V_{OL}	-1.8	-1.5	V	V_{EE} = -5.2V (25°C)	
$\overline{PE}$ input high voltage	V_{INH}	-0.93		V	V_{EE} = -5.2V (25°C)	
$\overline{PE}$ input low voltage	V_{INL}		-1.62	V	V_{EE} = -5.2V (25°C)	
Clock to output delay	t_p		6	ns		Note 7
Set-up time	t_s	2		ns		Note 7
Release time	t_r	2		ns		Note 7

NOTES
1. Unless otherwise stated, the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The temperature coefficient of V_{OH} = +1.63mV/°C, V_{OL} = +0.94mV/°C and of V_{IN} = +1.22mV/°C but these are not tested.
3. The test configuration for dynamic testing is shown in Fig.6.
4. The set up time t_s is defined as minimum time that can elapse between L ⟶ H transition of control input and the next L ⟶ H clock pulse transition to ensure that ÷10 is obtained.
5. The release time t_r is defined as the minimum time that can elapse between H ⟶ L transition of the control input and the next L ⟶ H clock pulse transition to ensure that the ÷11 mode is obtained.
6. Tested at 25°C only.
7. Guaranteed but not tested.



*Tested as specified in table of Electrical Characteristics

Fig.3 Typical input characteristic SP8685A

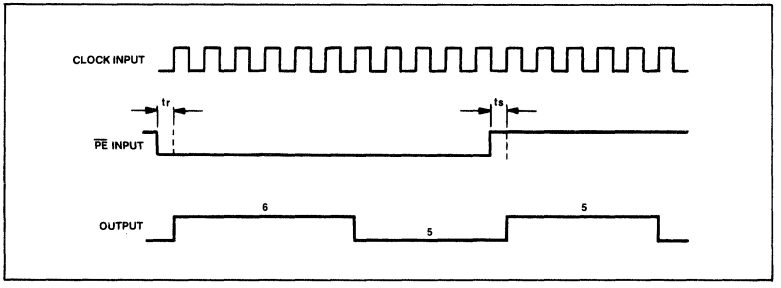


Fig.4 Timing diagram

OPERATING NOTES

1. The clock input is biased internally and is coupled to the signal source with a suitable capacitor. The input signal path is completed by an input reference decoupling capacitor which is connected to earth.
2. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 15k resistor from clock input (Pin 12) to V_{EE}. This will reduce the input sensitivity by approximately 100mV.
3. The circuit will operate down to DC but slew rate must be better than 100V/µs.
4. The outputs are compatible with ECL II but can be interfaced to ECL 10K as shown in Fig.7.
5. The $\overline{PE}$ inputs are ECL III/10K compatible and include a 4.3k internal pulldown resistor. Unused inputs can therefore be left open.

TRUTH TABLE FOR CONTROL INPUTS

$\overline{PE1}$	$\overline{PE2}$	Division Ratio
L	L	11
H	L	10
L	H	10
H	H	10

6. Input impedance is a function of frequency. See Fig. 5.
7. All components should be suitable for the frequency in use.

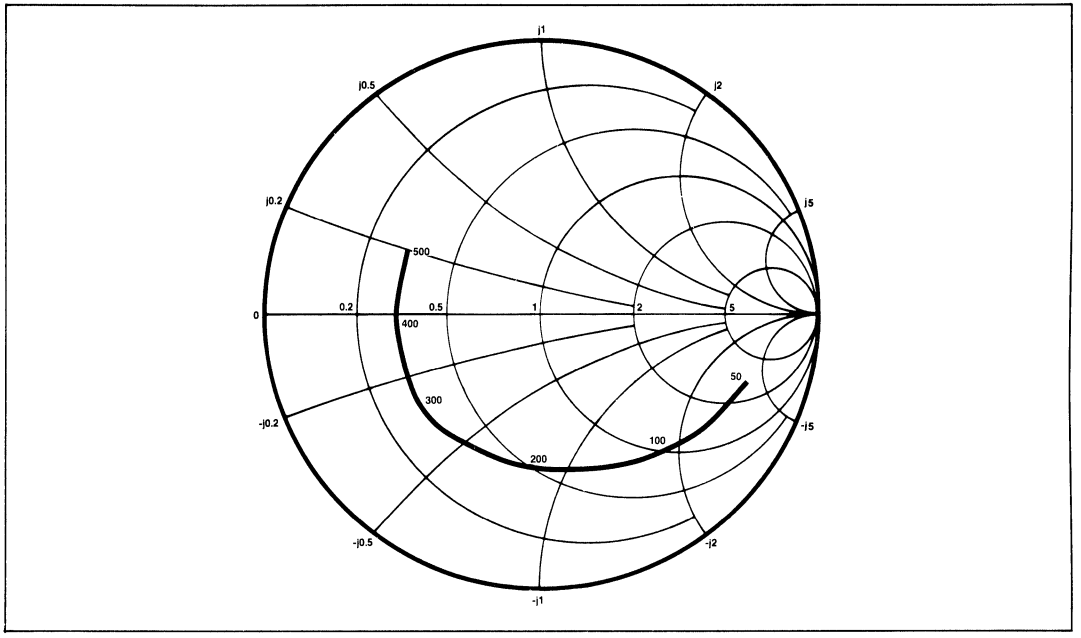


Fig.5 Typical input impedance. Test conditions: supply voltage -5.2V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

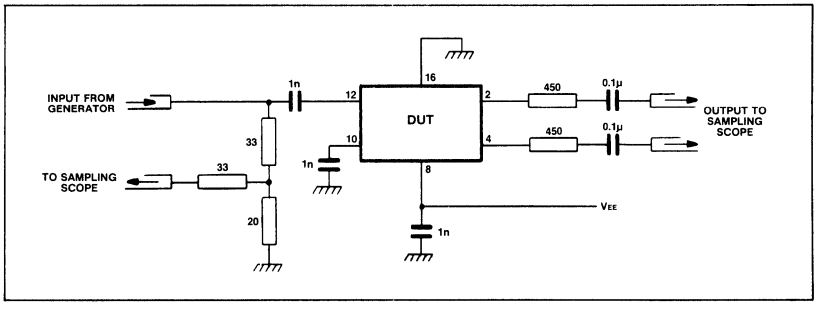


Fig.6 Test circuit

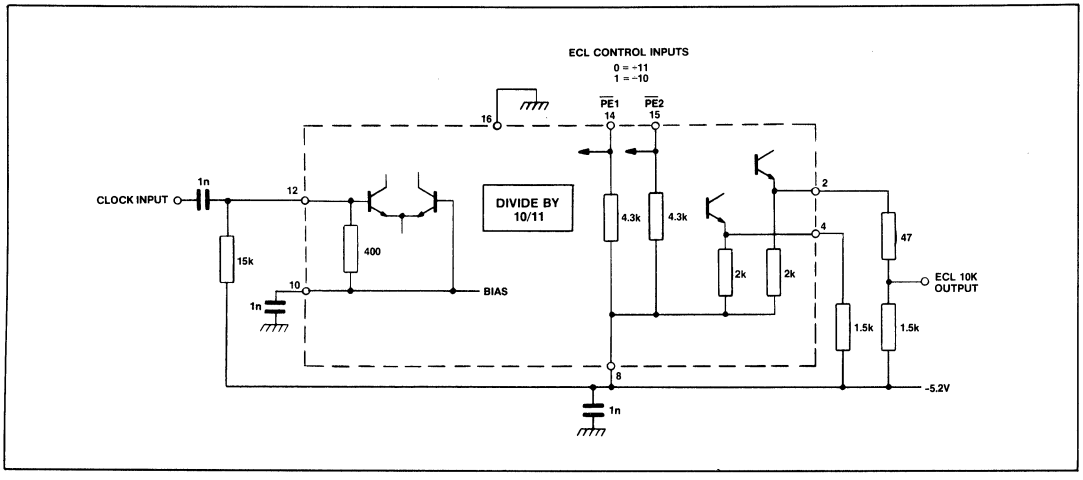


Fig.7 Typical application showing interfacing

SP8690A&B 200MHz ÷ 10/11
SP8691A&B 200MHz ÷ 8/9

The SP8690 and SP8691 are low power ECL counters with both ECL 10K and TTL compatible outputs. They divide by the lower division ratio when either control input is in the 'high' state and by the higher ratio when both are 'low' (or open circuit).

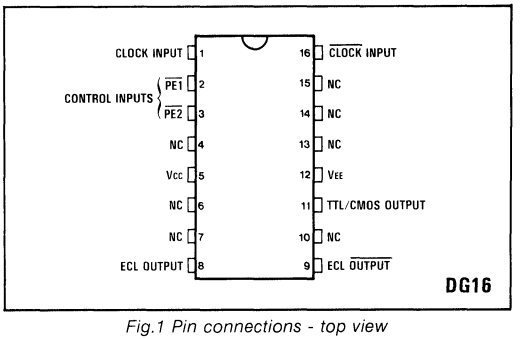


Fig.1 Pin connections - top view

FEATURES

- ECL and TTL/CMOS Output
- AC Coupled Input
- Control Inputs ECL Compatible

QUICK REFERENCE DATA

- Supply Voltage: 5V
- Power Consumption: 70mW
- Temperature Range:
  - A Grade: -55°C to +125°C
  - B Grade: -30°C to +70°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage	-8V
Output ECL current	10mA
Storage temperature range	-55°C to +150°C
Max. junction temperature	+175°C
TTL output	+12V
Input voltage	2.5V p-p
Max. open collector current	15mA

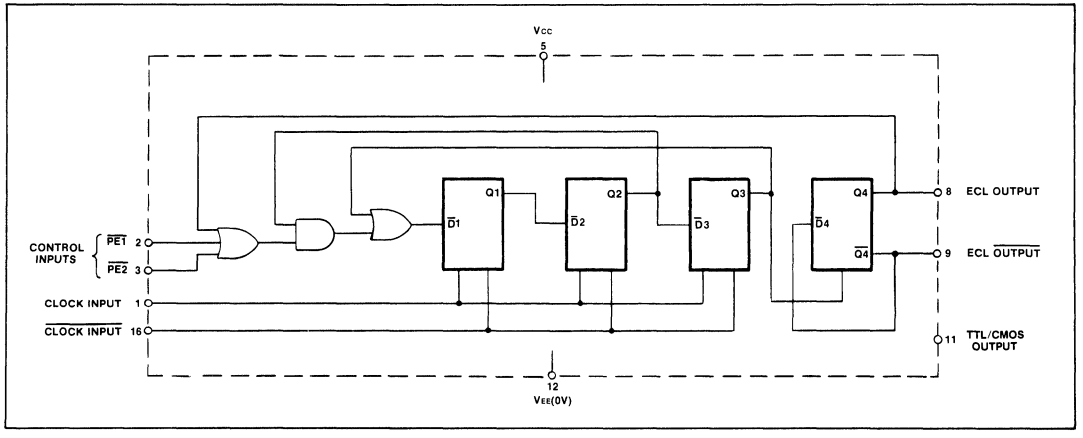


Fig.2 Functional diagram (SP8690)

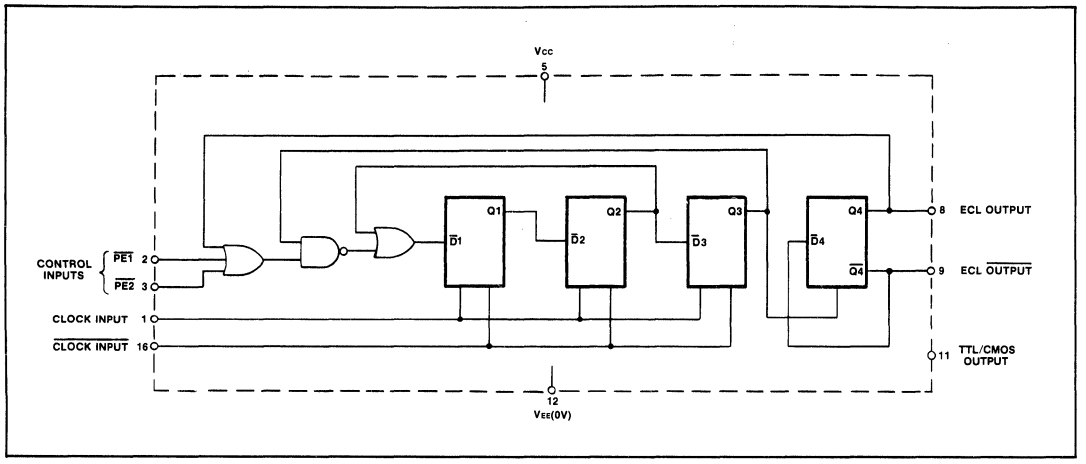


Fig.3 Functional diagram (SP8691)

ELECTRICAL CHARACTERISTICS

TTL OPERATION

Supply Voltage: V_{CC} = 5.0 ± 0.25V V_{EE} = 0V
Temperature: A Grade T_{amb} = -55°C to +125°C
B Grade T_{amb} = -30°C to +70°C

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency sinewave input	f_{max}	200		MHz	Input =400 - 800mV p-p	Note 3
Minimum frequency sinewave input	f_{min}		40	MHz	Input =400 - 800mV p-p	Note 3
Power supply current	I_{EE}		21	mA	V_{CC}= 5.0V	Note 3
TTL output high voltage	V_{OH}	3.75		V	V_{CC} = 5V RL = 560Ω	Note 3, 5
TTL output low voltage	V_{OL}		0.5	V	RL = 560Ω	Note 3, 5
Clock to TTL output delay (positive going)	t_{pLH}		32	ns	RL = 560Ω	Note 4
Clock to TTL output delay (negative going)	t_{pHL}		18	ns	RL = 560Ω	Note 4
Set-up time	t_s		3	ns		Note 4
Release time	t_r		8	ns		Note 4

NOTES
1. Unless otherwise stated, the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The temperature coefficient of V_{OH} = +1.63mV/°C, V_{OL} = +0.94mV/°C and of V_{IN} = +1.22mV/°C but these are not tested.
3. SP8690/1B tested at 25°C only.
4. Guaranteed but not tested.
5. Open collector output not recommended for use above 15MHz output frequency. $C_{load} \leqslant 5pF$.

ELECTRICAL CHARACTERISTICS

ECL OPERATION

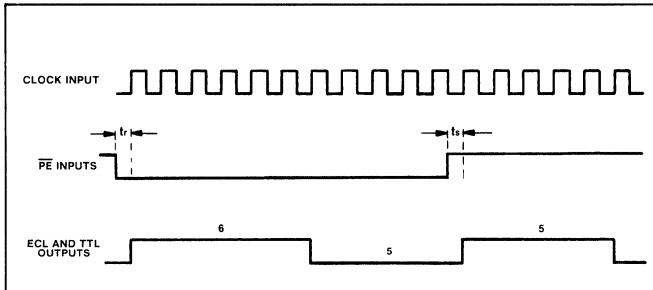
Supply Voltage: V_{EE} = -5.2 ± 0.25V V_{CC} = 0V
Temperature: A Grade T_{amb} = -55°C to +125°C
B Grade T_{amb} = -30°C to +70°C

Characteristics	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency sinewave input	f_{max}	200		MHz	Input = 400-800mV p-p	Note 3
Minimum frequency sinewave input	f_{min}		40	MHz	Input = 400-800mV p-p	Note 3
Power supply current	I_{EE}		21	mA	V_{EE} = -5.0V	Note 3

ELECTRICAL CHARACTERISTICS (CONTINUED)
ECL OPERATION

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
ECL output high voltage	V_{OH}	-0.85	-0.7	V	V_{EE} = -5.2V(25° C)	
ECL output low voltage	V_{OL}	-1.8	-1.5	V	V_{EE} = -5.2V(25° C)	
PE input high voltage	V_{INH}	-0.93		V	V_{EE} = -5.2V(25° C)	
PE input low voltage	V_{INL}		-1.62	V	V_{EE} = -5.2V(25° C)	
Clock to ECL output delay	t_p		9	ns		Note 4
Set-up time	t_s	3		ns		Note 4
Release time	t_r	8		ns		Note 4

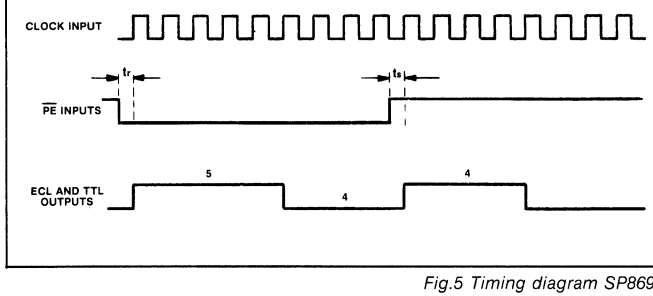
NOTES
1. Unless otherwise stated, the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The temperature coefficient of V_{OH} = +1.63mV/°C, V_{OL} = +0.94mV/°C and of V_{IN} = +1.22mV/°C but these are not tested.
3. SP8690/1B tested at 25°C only.
4. Guaranteed but not tested.



TRUTH TABLE FOR CONTROL INPUTS

$\overline{PE1}$	$\overline{PE2}$	Division Ratio
L	L	11
H	L	10
L	H	10
H	H	10

Fig.4 Timing diagram SP8690

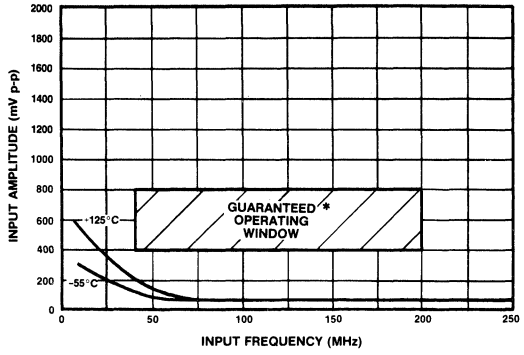


TRUTH TABLE FOR CONTROL INPUTS

$\overline{PE1}$	$\overline{PE2}$	Division Ratio
L	L	9
H	L	8
L	H	8
H	H	8

Fig.5 Timing diagram SP8691

NOTE:
The set-up time t_s is defined as minimum time that can elapse between L⟶H transition of control input and the next L⟶H clock pulse transition to ensure that the ÷10 or 8 mode is obtained.
The release time t_r is defined as the minimum time that can elapse between a H⟶L transition of a control input and the next L⟶H clock pulse transition to ensure that the ÷11 or 9 mode is obtained.



*Tested as specified in table of Electrical Characteristics

Fig.6 Typical input characteristics SP86790/1

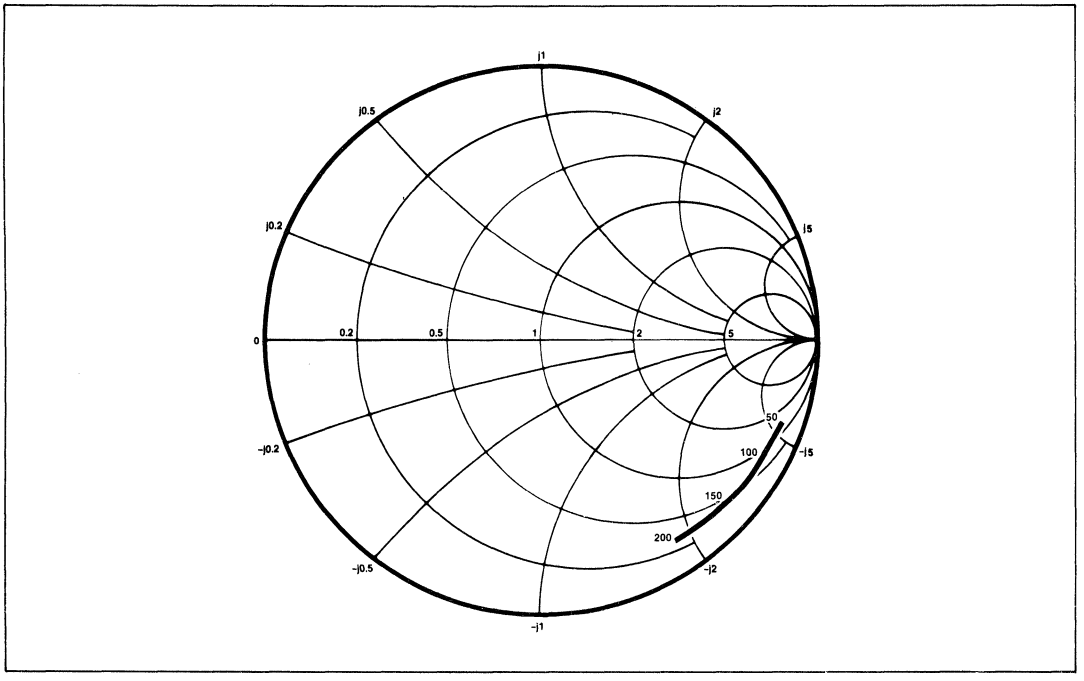


Fig.7 Typical input impedance. Test conditions: supply voltage 5.0V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

OPERATING NOTES

1. The clock inputs can be single or differentially driven. The clock input is biased internally and is coupled to the signal source with a suitable capacitor. The input signal path is completed by an input reference decoupling capacitor which is connected to earth.
2. In the absence of a signal the device will self-oscillate. If this is undesirable it may be prevented by connecting a 68k resistor from the input to V_{EE} (i.e. Pin 1 or 16 to Pin 12). This reduces input sensitivity by approximately 100mV.
3. The circuit will operate down to DC but slew rate must be better than 100V/µs.
4. The Q_4 and $\overline{Q_4}$ outputs are compatible with ECL II but can be interfaced to ECL 10K as shown in Fig.9.
5. The PE inputs are ECL III/10K compatible and include a 10k internal pulldown resistor. Unused inputs can therefore be left open circuit.
6. The input impedance of the SP8690/1 varies as a function of frequency. See Fig. 7.
7. The TTL/CMOS output has a free collector and the high state output voltage will depend on the supply that the collector load is taken too. This should not exceed 12V.
8. The rise/fall time of the open collector output waveform is directly proportional to load capacitance and load resistor value. Therefore load capacitance should be minimised and the load resistor kept to a minimum compatible with system power requirements. In the test configuration of Fig. 8 the output rise time is approximately 10ns and fall time is 7ns typically.

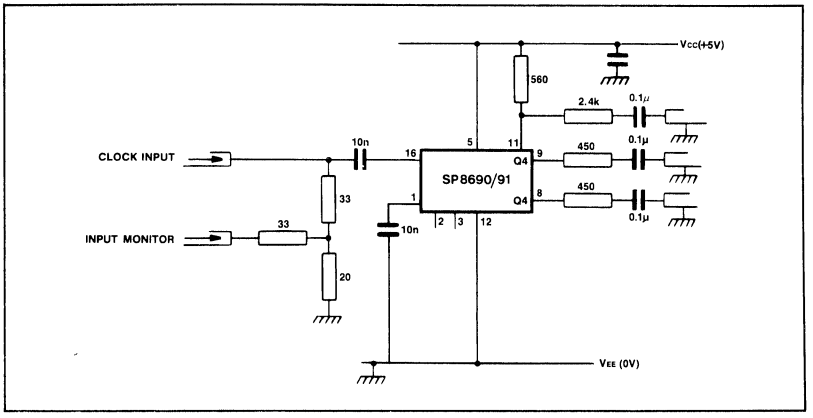


Fig.8 Test circuit for dynamic measurements

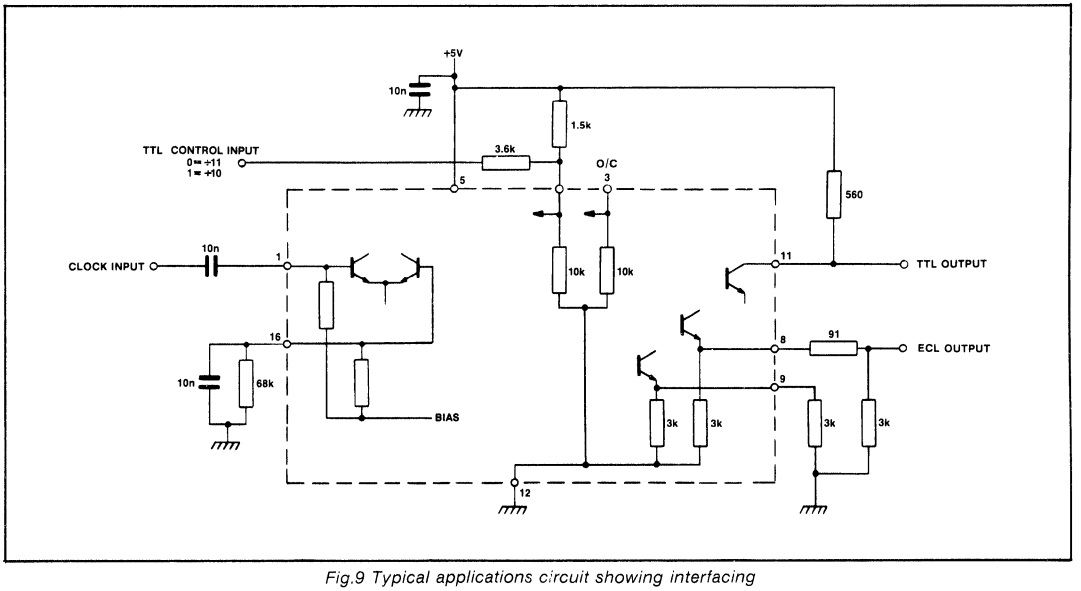


Fig.9 Typical applications circuit showing interfacing

SP8695A&B

200MHz ÷ 10/11

The SP8695 is a low power ECL counter with both ECL 10K and TTL compatible outputs. They divide by 10 when either control input in the 'high' state and by 11 when both are 'low' (or open circuit). The inputs are ECL II compatible but can also be AC coupled. An open collector output is provided for interfacing to TTL or CMOS.

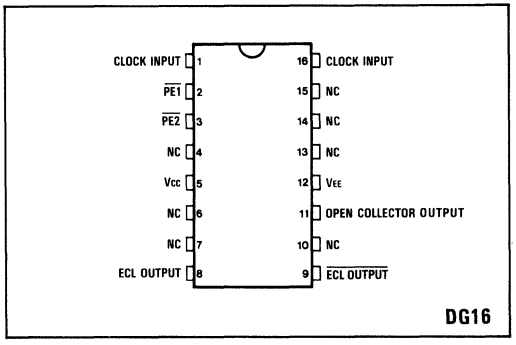


Fig.1 Pin connections - top view

FEATURES

- Low Frequency Operation
- ECL and TTL/CMOS Outputs
- DC or AC Coupled Input
- Temperature Ranges:
  - A Grade: -55°C to +125°C
  - B Grade: -30°C to +70°C

QUICK REFERENCE DATA

- Supply Voltage: +5.0V
- Power Consumption: 80mW
- Maximum Input Frequency: 200MHz

ABSOLUTE MAXIMUM RATINGS

Supply voltage	-8V
Output ECL current	10mA
Storage temperature range	-55°C to +150°C
Max. junction temperature	+175°C
Max. input voltage	2.5V p-p
Max. open collector output voltage	+12V
Max. open collector current	15mA

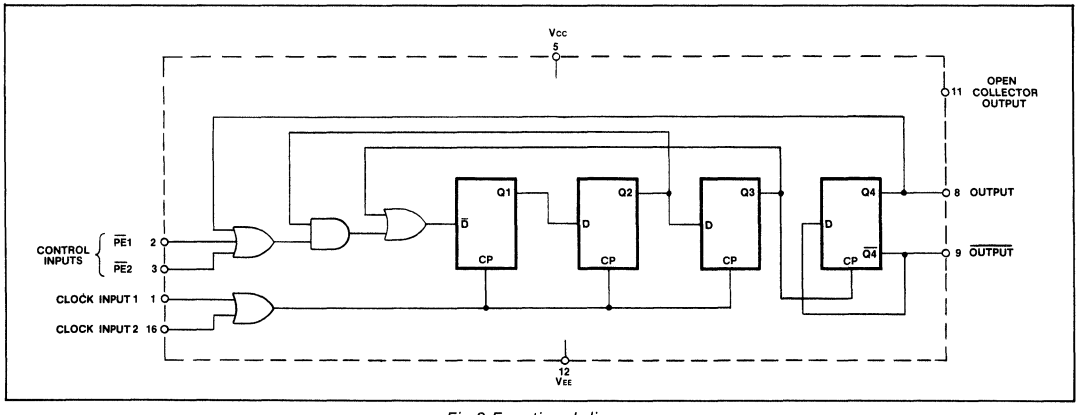


Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

ECL OPERATION

Supply Voltage: V_{EE} = -5.2V ± 0.25V V_{CC} = 0V
Temperature: A grade T_{amb} = -55°C to +125°C
B grade: T_{amb} = -30°C to +70°C

Characteristics	Symbol	Value		Units	Conditions	Temperature
		Min.	Max.			
Maximum frequency sinewave input	f_{max}	200		MHz	Input = 400-800mV p-p	Note 3
Minimum frequency sinewave input	f_{min}		2	MHz	Input = 400-800mV	Note 4
Power supply current	I_{EE}		21	mA	V_{EE} = -5.0V	Note 3
ECL output low voltage	V_{OH}	-0.85	-0.7	V	V_{EE} = -5.2V (25°C)	
ECL output high voltage	V_{OL}	-1.8	-1.5	V	V_{EE} = -5.2V (25°C)	
$\overline{PE}$ input high voltage	V_{INH}	-0.93		V	V_{EE} = -5.2V (25°C)	
$\overline{PE}$ input low voltage	V_{INL}		-1.62	V	V_{EE} = -5.2V (25°C)	
Clock to ECL output delay	t_p		9	ns		Note 4
Set-up time	t_s	3		ns		Note 4
Release time	t_r	8		ns		Note 4

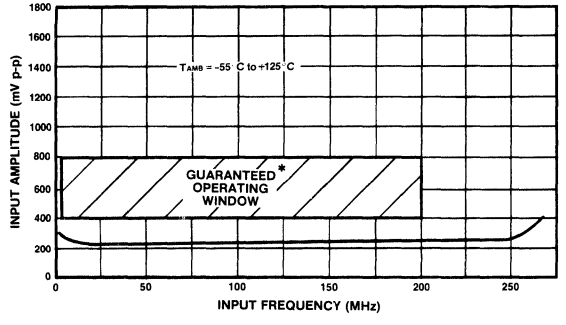
NOTES
1. Unless otherwise stated, the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The temperature coefficient of V_{OH} = +1.63mV/°C, V_{OL} = +0.94mV/°C and of V_{IN} = +1.22mV/°C but these are not tested.
3. SP8695B tested at 25°C only.
4. Guaranteed but not tested.
5. TTL output not recommended for use above 15MHz output frequency. $C_{load} \leq 5pF$.

ELECTRICAL CHARACTERISTICS

TTL OPERATION

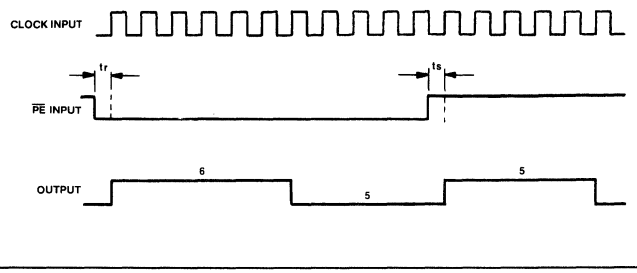
Supply Voltage: V_{CC} = 5.0 ± 0.25V V_{EE} = 0V
Temperature: A grade T_{amb} = -55°C to +125°C
B grade T_{amb} = -30°C to +70°C

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency sinewave input	f_{max}	200		MHz	Input =400 - 800mV p-p	Note 3
Minimum frequency sinewave input	f_{min}		2	MHz	Input =400 - 800mV p-p	Note 4
Power supply current	I_{EE}		21	mA	V_{CC}= 5.0V	Note 3
TTL output high voltage	V_{OH}	3.75		V	V_{CC}= 5V RL = 560Ω	Note 3, 5
TTL output low voltage	V_{OL}		0.5	V	RL = 560Ω	Note 3
Clock to TTL output delay (positive going)	t_{pLH}		32	ns	RL = 560Ω	Note 4
Clock to TTL output delay (negative going)	t_{pHL}		18	ns	RL = 560Ω	Note 4
Set-up time	t_s	3		ns		Note 4
Release time	t_r	8		ns		Note 4



*Tested as specified in table of Electrical Characteristics

Fig.3 Typical input characteristics SP8695A



CONTROL INPUT TRUTH TABLE

$\overline{PE1}$	$\overline{PE2}$	Division Ratio
L	L	11
H	L	10
L	H	10
H	H	10

Fig.4 Timing diagram SP8695

NOTES

The set-up time t_s is defined as minimum time that can elapse between L→H transition of control input and the next L→H clock pulse transition to ensure that the ÷10 mode is obtained.

The release time t_r is defined as the minimum time that can elapse between a H→L transition of control input and the next L→H clock pulse transition to ensure that the ÷11 mode is obtained.

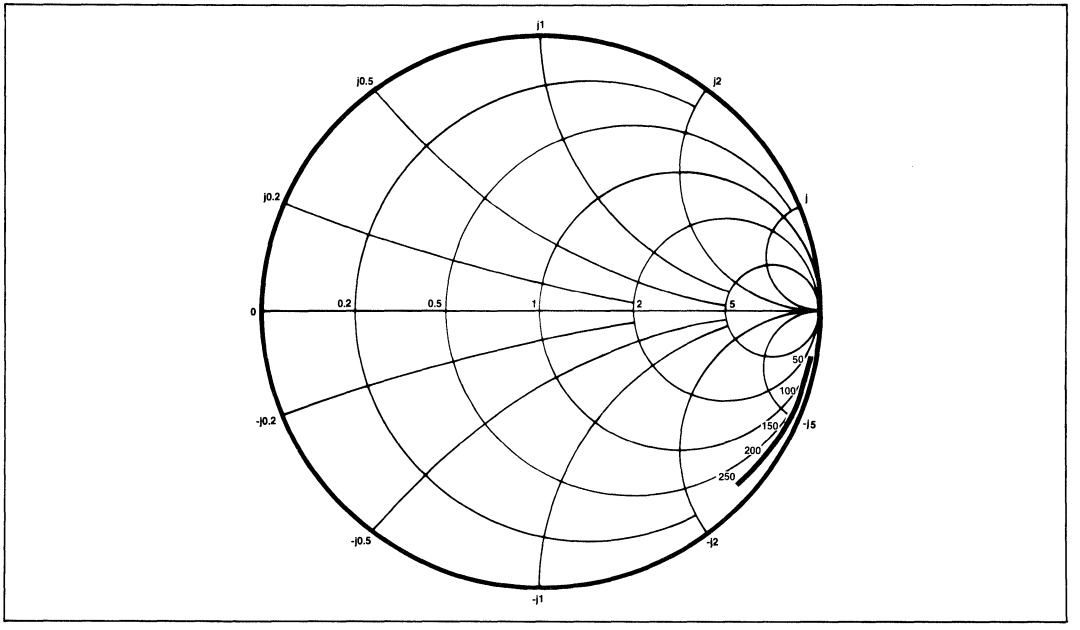


Fig.5 Typical input impedance. Test conditions: supply voltage 5.0V, ambient temperature 25°C, frequencies in MHz, impedances normalised to 50 Ohms.

OPERATING NOTES

1. The clock inputs can be driven from ECL II, III and 10K. The input reference voltage (-3.8V at 25°C) is compatible with ECL II, III and 10K over the specified temperature range. The inputs can also be capacitively coupled by addition of external bias as shown in Fig. 6. Each input has an internal pull-down resistor of 10k, and unused inputs can therefore be left open circuit. They should by bypassed to RF where maximum noise immunity is required.
2. The PE control inputs are similarly ECL III/10K compatible and also have an internal 10k pull-down resistor, allowing unused inputs to be left open circuit if required.
3. The Q_4 and $\overline{Q_4}$ ECL outputs have internal circuitry equivalent to a 14k pull-down resistor on each output and are ECL II compatible: they can however be interfaced to ECL III/10K as shown in Fig. 8.
4. The circuit will operate down to DC but slew rate must be better than 5V/µs.
5. The input impedance of SP8695 varies as a function of frequency. See Fig. 5.
6. The TTL/CMOS output has a free collector and the high state output voltage will depend on the supply that the collector load is taken to. This should not exceed 12V. The rise and fall time of the open collector output waveform is directly proportional to load capacitance and load resistance value. Therefore load capacitance should be kept to a minimum and the load resistor kept to a minimum compatible with system power requirements. In the test configuration of Fig. 6 the output rise time is approximately 10ns and fall time is 7ns typically.

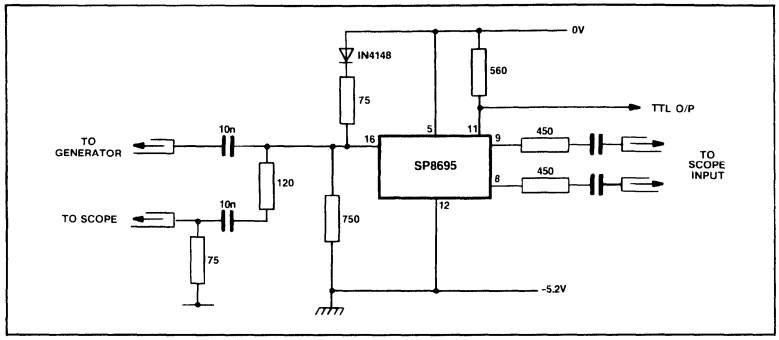


Fig.6 Test circuit

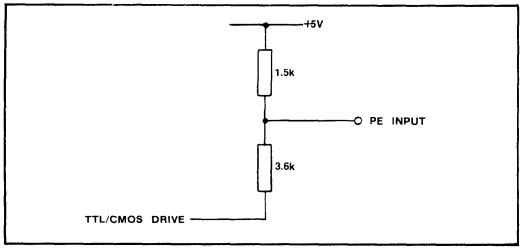


Fig.7 Interfacing TTL/CMOS to PE inputs

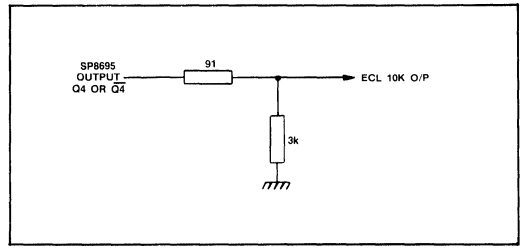


Fig.8 Interfacing to SP8695 output to ECL 10K

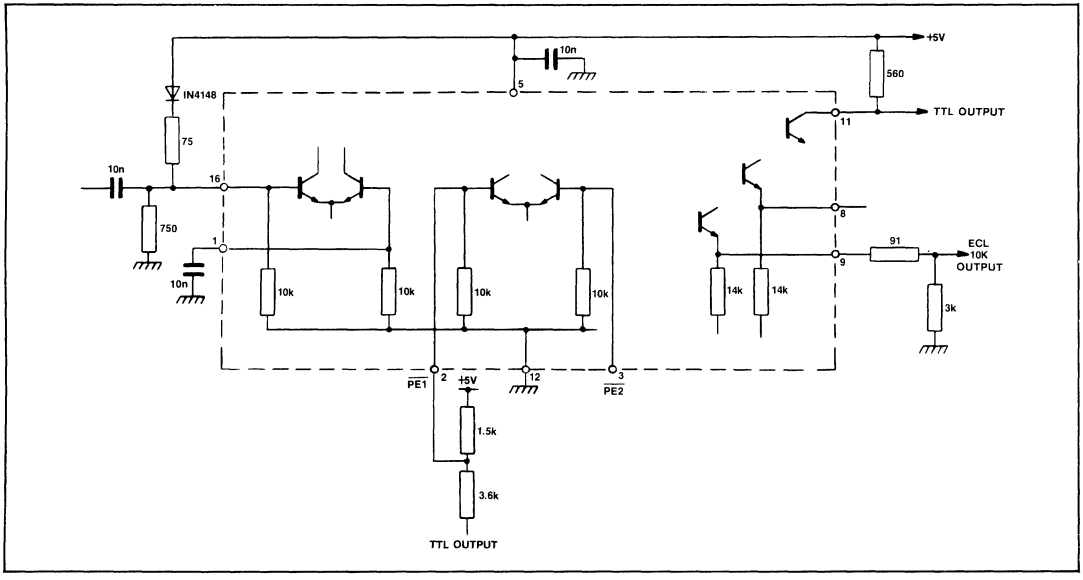


Fig.9 Typical application showing interfacing

SP8703

1GHz LOW CURRENT TWO-MODULUS DIVIDER

The SP8703 is a divide by 128/9 programmable divider with a maximum specified operating frequency of 1GHz.

The signal (clock) inputs are biased internally and require to be capacitor coupled.

The output stage is CMOS compatible only, the 0 to 1 output edge giving best loop delay performance.

A unique 'power-down' feature is included to minimise power consumption.

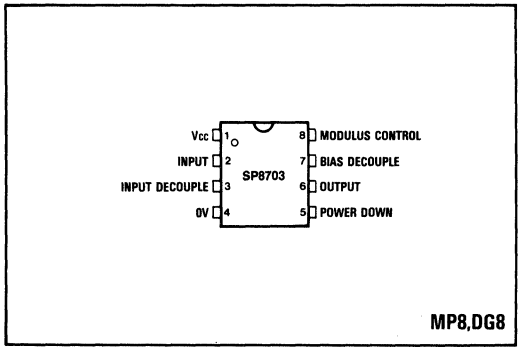


Fig.1 Pin connections - top view

FEATURES

- DC to 1GHz Operation
- -30° to +70°C Temperature Range
- Unique Power-Down Feature
- CMOS Compatible

QUICK REFERENCE DATA

- Supply Voltage 5.0V ± 0.25V
- Supply Current 30mA Typical

ABSOLUTE MAXIMUM RATINGS

Supply voltage	6V
Storage temperature range	-30°C to +150°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p

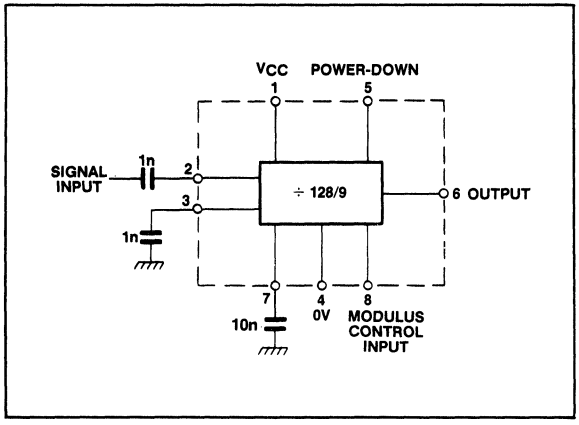


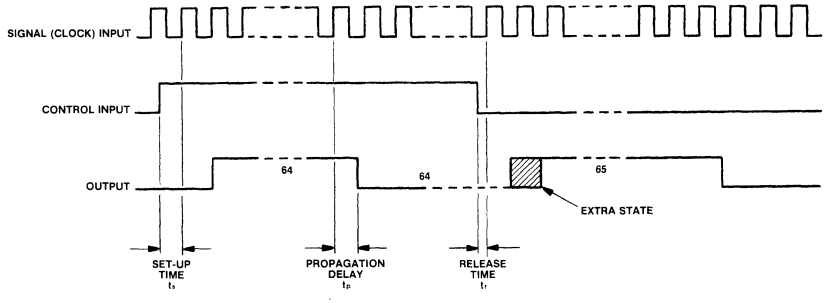
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{CC} = +4.75V to 5.25V, T_{amb} = -30°C to +70°C

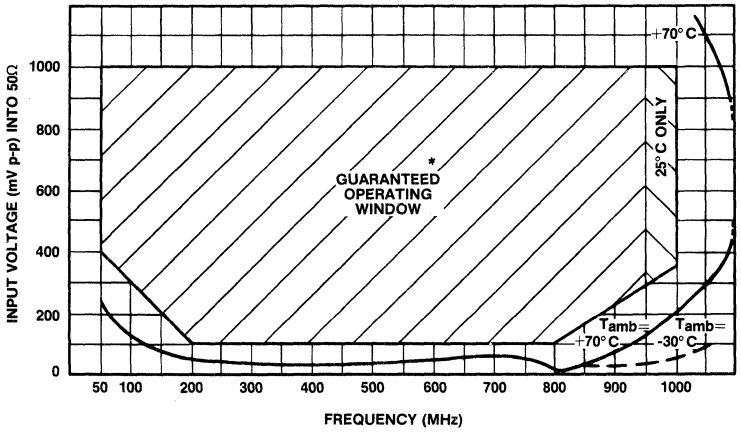
Characteristics	Value		Units	Conditions	Notes
	Min.	Max.			
Maximum frequency	1000		MHz	T_{amb} = 25°C	Note 1,2,4
Maximum frequency	950		MHz		Note 1,2,3
Minimum frequency (sinewave)		50	MHz		Note 1,2,3
Power supply current		40	mA	Power-up	Note 3
Power supply current		3	mA	Power-down	Note 3
Output high voltage	3.2	V_{CC}	V	IL = -0.2mA	Note 3
Output low voltage	0	1.7	V	IL = 0.2mA	Note 3
Control input high voltage	3.2	V_{CC}	V	Divide by 128	Note 3
Control input low voltage	0	1.7	V	Divide by 129	Note 3
Control input high current		50	μA	Input = V_{CC}	Note 3
Control input low current	-10		μA	Input = 0V	Note 3
Power-down high voltage	3.2	V_{CC}	V	Power-down	Note 3
Power-down low voltage	0	1.7	V	Power-up	Note 3
Power-down high current		10	μA	Input = V_{CC}	Note 3
Power-down low current	-2		μA	Input = 0V	Note 3
Clock to output delay		30	ns	CL = 10pF	Note 5
Set-up time		15	ns	CL = 10pF	Note 5
Release time		15	ns	CL = 10pF	Note 5

NOTES
1. See Fig.4 for guaranteed operating window.
2. See Fig.5 for input voltage measurement method.
3. Tested at 25°C and +70°C only.
4. Tested at 25°C only.
5. Guaranteed but not tested.



NOTE
The set-up time t_s is defined as the minimum time that can elapse between a L→H transition of the control input and the next L→H clock pulse transition to ensure that the ÷128 mode is obtained.
The release time t_r is defined as the minimum time that can elapse between a H→L transition of the control input and the next L→H clock pulse transition to ensure that the ÷129 mode is obtained.

Fig.3 Timing diagram



*Tested as specified in table of Electrical Characteristics

Fig.4 Typical input characteristics

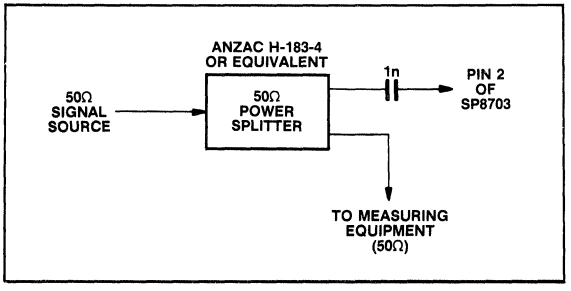


Fig.5 Input voltage measurement method

OPERATING NOTES

1. The inputs are biased internally and coupled to a signal source with suitable capacitors.
2. If no signal is present the devices will self-oscillate. If this is undesirable it may be prevented by connecting a 15k resistor from one input to pin 4 (ground). This will reduce the sensitivity.
3. The circuits will operate down to DC but slew rate must be better than 100V/μs.
4. The output stage is of an unusual design and is intended to interface with CMOS. External pull-up resistors or circuits must not be used.

PLESSEY
Semiconductors

SP8704

950MHz VERY LOW CURRENT MULTI-MODULUS DIVIDER

The SP8704 is a switchable divide by 128/129, 64/65 programmable divider with a maximum specified operating frequency of 950MHz.

The signal (clock) inputs are biased internally and require to be capacitor coupled.

The SP8704 will operate from any supply from 3V to 5V and features full electrostatic discharge protection.

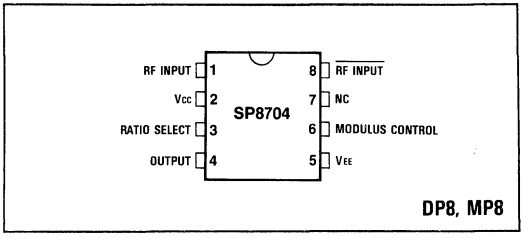


Fig.1 Pin connections - top view

FEATURES

- DC to 950MHz Operation
- -40°C to +85°C Temperature Range
- Operation from 3V to 5V Supply
- ESD Protection on all Pins

QUICK REFERENCE DATA

- Supply Voltage 3V to 5V
- Supply Current 10mA - Including Output Emitter Follower

ABSOLUTE MAXIMUM RATINGS

Supply voltage	7V
Storage temperature range	-55°C to +125°C
Junction temperature	+175°C
Input voltage	2.5V p-p

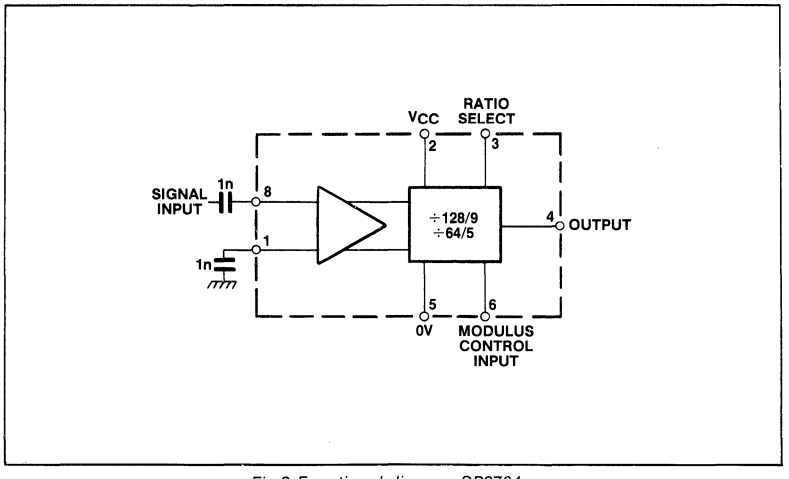


Fig.2 Functional diagram SP8704

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = -40°C to 85°C, V_{CC} = +2.75V to +5.5V

Characteristic		Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current			10		mA	Including output emitter follower
Input sensitivity	10MHz			150	mV rms	Sinewave input into 50Ω
	80MHz			25		
	150MHz			15		
	850MHz			15		
	950MHz			50		
Input overload		300			mV rms	
Input impedance			50		Ω	
			2		pF	
Output			1		V pk-pk	Emitter follower output current source = 0.75mA
Ratio select (pin 3)	LO			1	V	128/129 selected
	HI *	V_{CC}			V	64/65 selected
Modulus control (pin 6)	LO	1			V	65 or 129 selected
	HI *			2	V	64 or 128 selected
Clock to output delay			8		ns	
Set up time			16		ns	
Release time			16		ns	

*Or pin open circuit

TRUTH TABLE

Pin 3	Pin 6	Division ratio
L	L	129
L	H	128
H	L	65
H	H	64

SP8710A & B

225MHz LOW POWER TWO MODULUS DIVIDER ÷ 100/101

The SP8710 is a Low Power Two Modulus Divider with a divide by 100 ratio when the modulus control input is high and 101 when the input is low. The device also features a power down mode and will operate with a 3V power supply.The 'A' Grade device is characterised over the full military temperature range of -55°C to +125°C, the 'B' Grade over the industrial range of -40°C to +85°C.

FEATURES

- Low Power High Speed
- Power Down Mode
- CMOS Compatible Output Capability
- Ideal for Decade Synthesisers
- 3V Supply Operation

QUICK REFERENCE DATA

- Supply Voltage Range 3V to 10V
- Full Military Temperature Range: -55°C to 125°C (SP8710A)

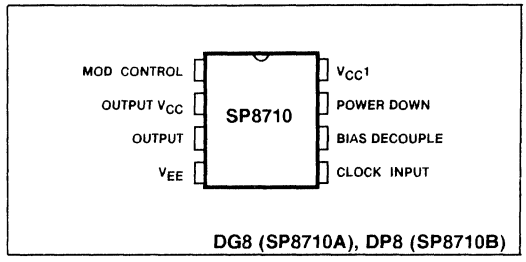


Fig.1 Pin connections - top view

ABSOLUTE MAXIMUM RATINGS

Supply voltage	12V
Clock input level	2.5V p-p
Junction temperature	+175°C
Storage temperature range	
SP8710A	-55°C to +150°C
SP8710B	-55°C to +125°C

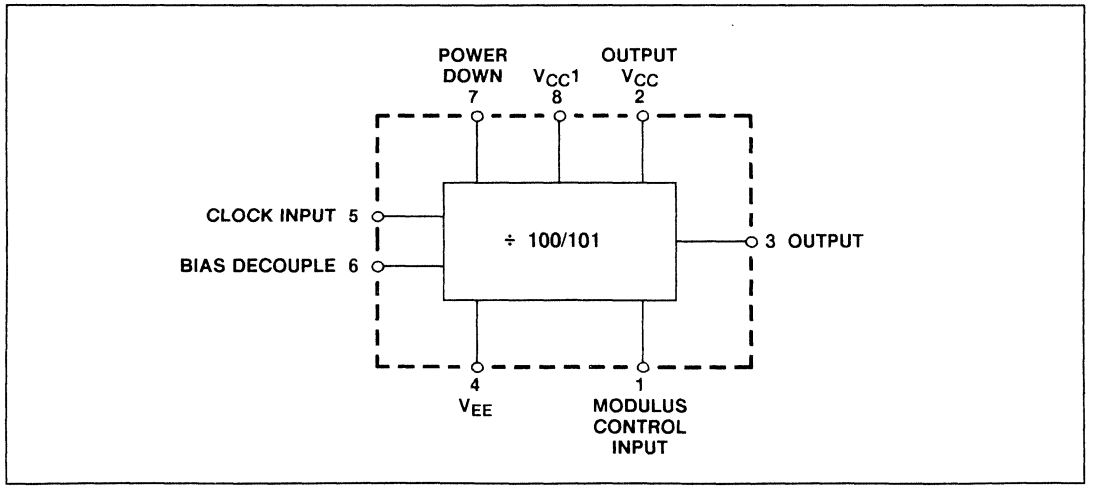


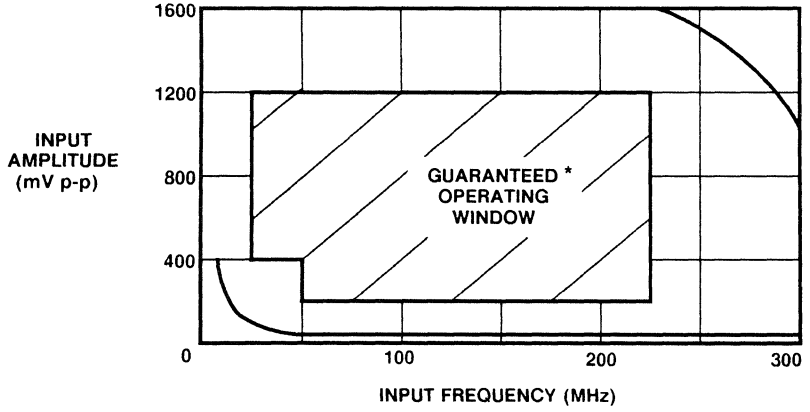
Fig.2 SP8710 functional diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

T_{amb} = SP8710A -55°C to +125°C, SP8710B -40°C to +85°C, V_{CC} = +3V to +10V

Characteristic	Pin	Value		Units	Conditions
		Min.	Max.		
Max. sinewave input frequency	5	225		MHz	Input = 200mV - 1200mV p-p
Min. sinewave input frequency	5		20	MHz	Input = 400mV - 1200mV p-p
Min. slew rate for LF operation	5		100	V/µs	
Power supply current I_{EE}	8		8	mA	Power up V_{CC} = 5V
			8.5	mA	Power up V_{CC} = 10V
			1	mA	Power down
Output low voltage	3	0	0.5	V	Load = 10pF//100k
Output high voltage		V_{CC}-0.9	V_{CC}	V	Load = 10pF//100k, V_{CC} = 5V
		V_{CC}-0.95	V_{CC}	V	Load = 10pF//100k,V_{CC} = 10V
Modulus control input high voltage	1	0	V_{CC}	V	
Modulus control input low voltage	1		0.4V_{CC}	V	
Modulus control input high current	1		20	µA	Input = V_{CC}
Modulus control input low current	1		-10	µA	Input = 0V
Clock to output propagation delay	5,6,7		80	ns	
Set up time	1		10	ns	
Release time	1		10	ns	
Power down input high voltage	7	0.6V_{CC}	V_{CC}	V	
Power down input low voltage	7	0	0.4V_{CC}	V	
Power down input high current	7		1	µA	
Power down input low current	7		-1	µA	



* As specified in Table of Electrical Characteristics

Fig.2 Typical input characteristics SP8710

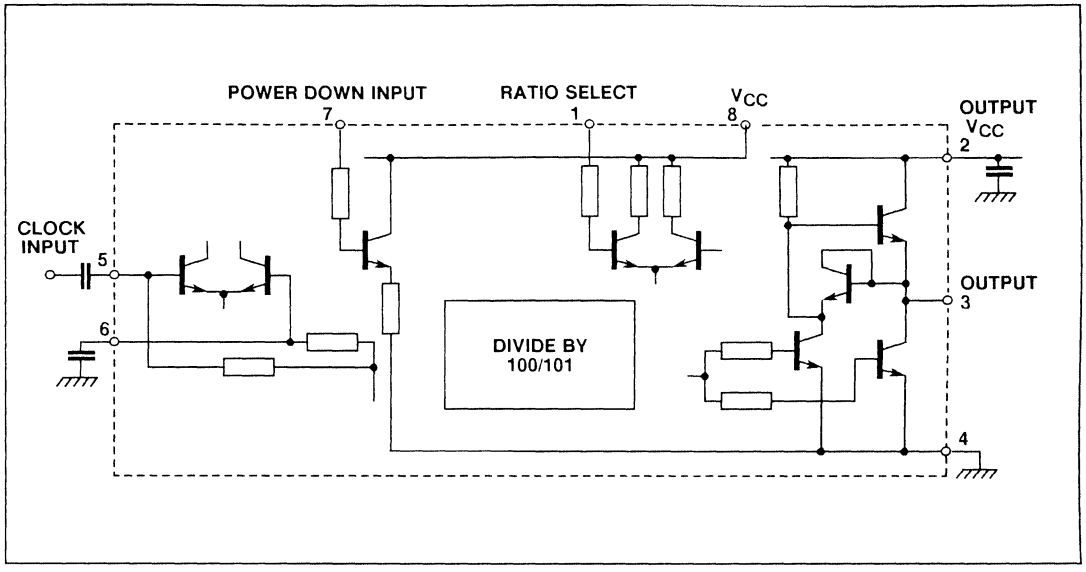


Fig.3 Typical application showing interfacing

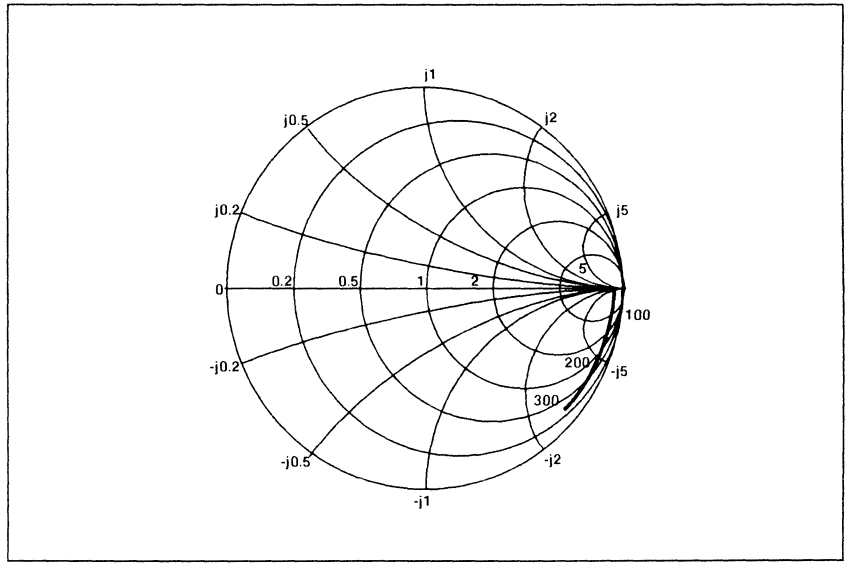


Fig.4 Typical Input Impedance. Test conditions:supply voltage 5V, ambient temperature 25°C, frequencies in MHz, impedances normalised to 50 Ohms

SP8712B

2400MHz ÷ 4

The SP8712B is an asynchronous emitter coupled logic counter which provides ECL 10K compatible outputs and can drive 100 ohm lines. It operates from a -6.8V supply or split supplies of +5V and -1.8V. Otherwise it is similar to the SP8610 and SP8611.

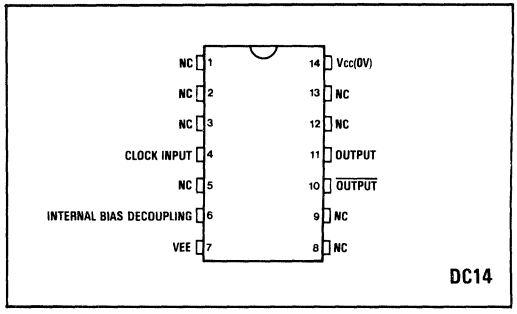


Fig.1 Pin connections - top view

FEATURES

- ECL Compatible Output
- AC Coupled Input (Internal Bias)
- Typical Operating Frequency 2.5GHz

QUICK REFERENCE DATA

- Supply Voltage: -6.8V
- Power Consumption: 630mW typ.
- Output Voltage Swing 800mV typ.

ABSOLUTE MAXIMUM RATINGS

Supply voltage (V_{CC} - V_{EE})	8V
Output current	15mA
Storage temperature range	-55°C to +150°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p

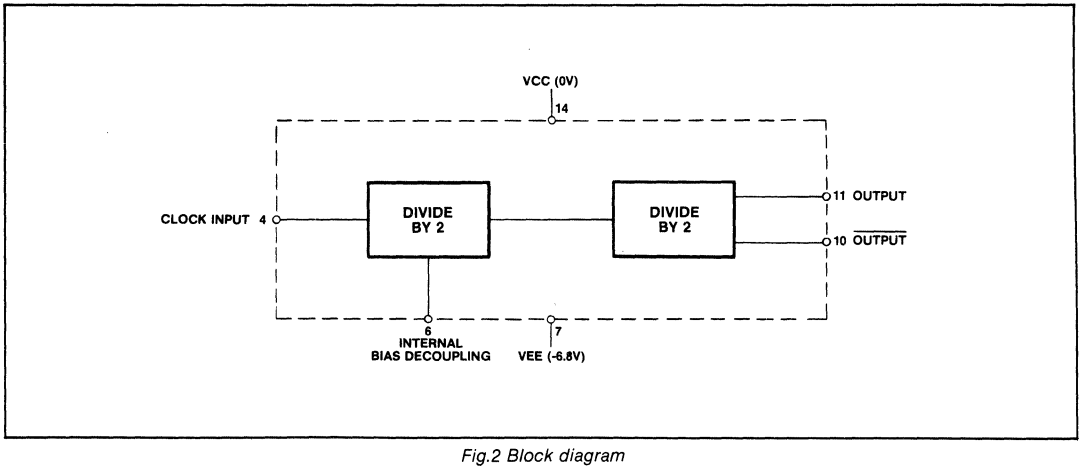


Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage: V_{CC} = 0V, V_{EE} = -6.8V ± 0.35V
Temperature: T_{amb} = 0°C to +70°C

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency sinewave input	f_{max}	2.4		GHz	Input = 600mV pk-pk	Note 4
Minimum frequency sinewave input	f_{min}		500	MHz	Input = 400mV pk-pk	Note 5
Power supply current	I_{EE}		110	mA	Outputs unloaded V_{EE} = -7.15V	Note 5
Output low voltage	V_{OL}	-0.93	-0.7	V	Outputs loaded with 620Ω to V_{EE} = -6.8V (25°C)	
Output high voltage	V_{OH}	-1.9	-1.6	V	Outputs loaded with 620Ω to V_{EE} = -6.8V (25°C)	
Minimum output swing	V_{OUT}	0.7		V	Outputs loaded with 620Ω to V_{EE} = -6.8V	Note 5

NOTES
1. Unless otherwise stated the electrical characteristics are guaranteed over specified supply, frequency and temperature range.
2. The temperature coefficients of V_{OH} = +1.2mV/°C and V_{OL} = +0.24mV/°C but these are not tested.
3. The test configuration for dynamic testing is shown in Fig.5.
4. Tested at +70°C only.
5. Tested at 25°C only.

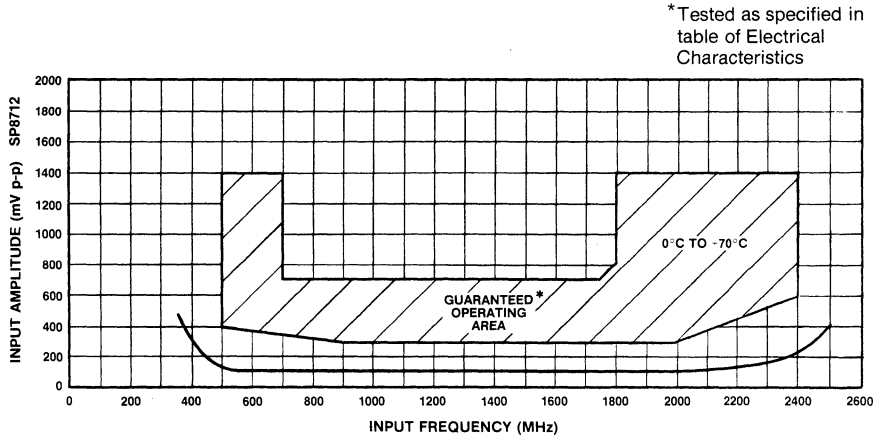


Fig.3 Typical input characteristics SP8712

OPERATING NOTES

1. The clock input (pin 4) should be capacitively coupled to the signal source. The input signal path is completed by connecting a capacitor from the internal bias decoupling pin (6) to ground.
2. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 10k resistor from the input to V_{EE} (i.e. pin 4 to pin 7). This reduces sensitivity by approximately 100mV.
3. The input can be operated at very low frequencies but slew rate must be better than 200V/μs.
4. The input impedance of the SP8712 is a function of frequency. See Fig.4.
5. The emitter follower outputs require external load resistors. These should not be less than 330 ohms, and a value of 620 ohms is recommended. Interfacing to ECL III/10K is shown in Fig.7.
6. These devices may be used with split supply lines by means of the circuit of Fig.6. Some improvement in the upper frequency of operation may be obtained under these conditions, but suitable circuit layout must be employed to achieve this improvement.
7. To obtain the best performance from these devices, good RF construction techniques must be employed: the use of leadless chip capacitors is recommended.

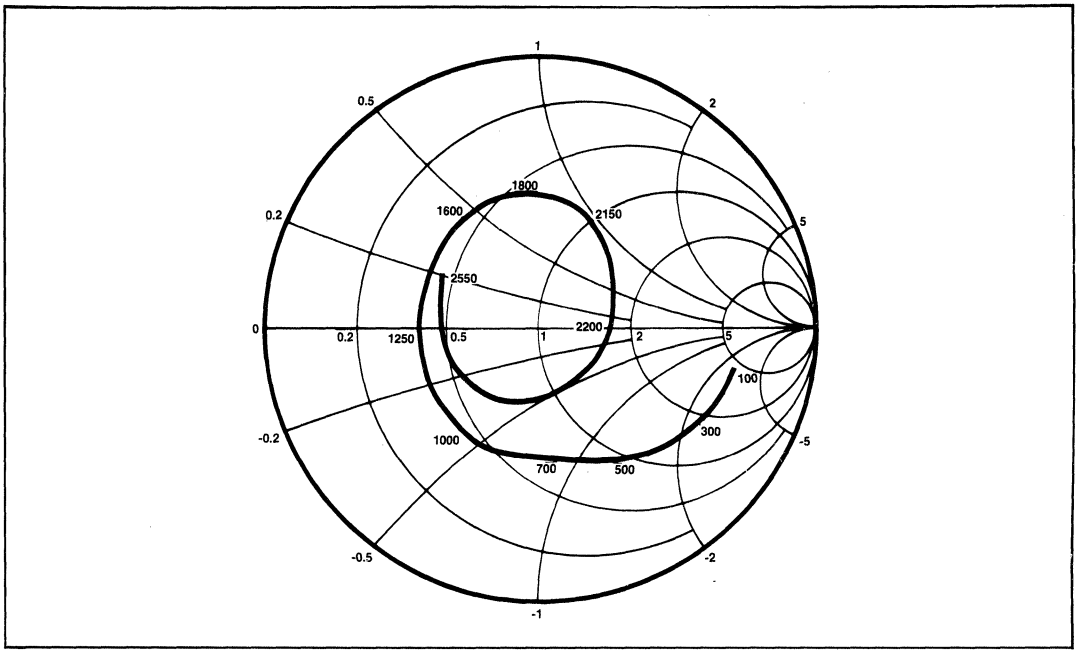


Fig.4 Typical input impedance. Test conditions: supply voltage -6.8V, ambient temperature 25° C. Frequencies in MHz, impedances normalised to 50 ohms.

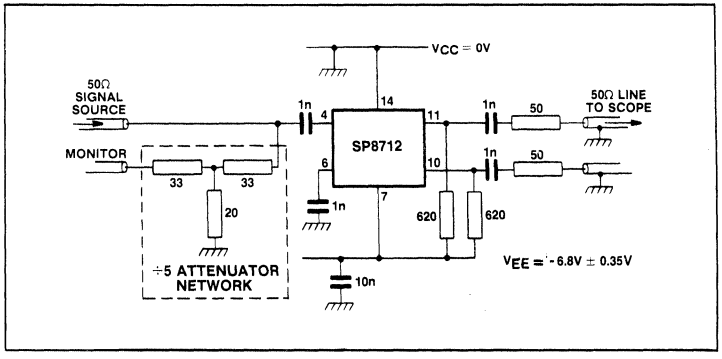


Fig.5 Toggle frequency test circuit

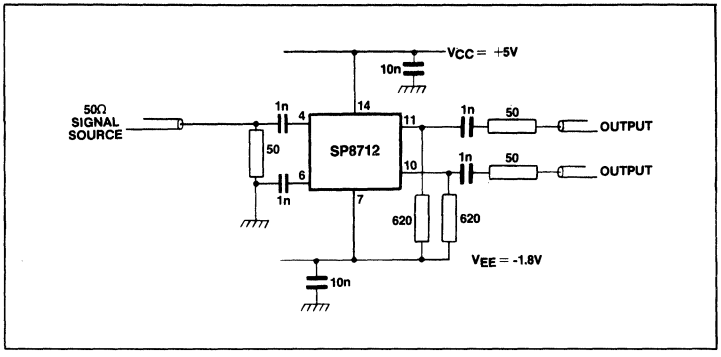


Fig.6 Operation on split supply voltages

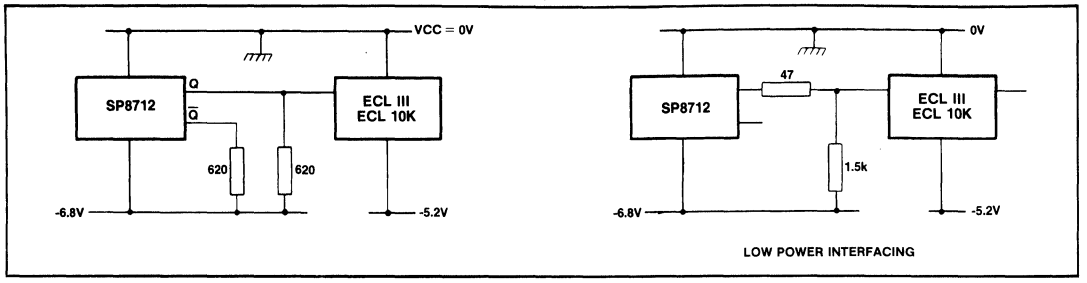


Fig.7 Interfacing SP8712 series to ECL 10K and ECL III

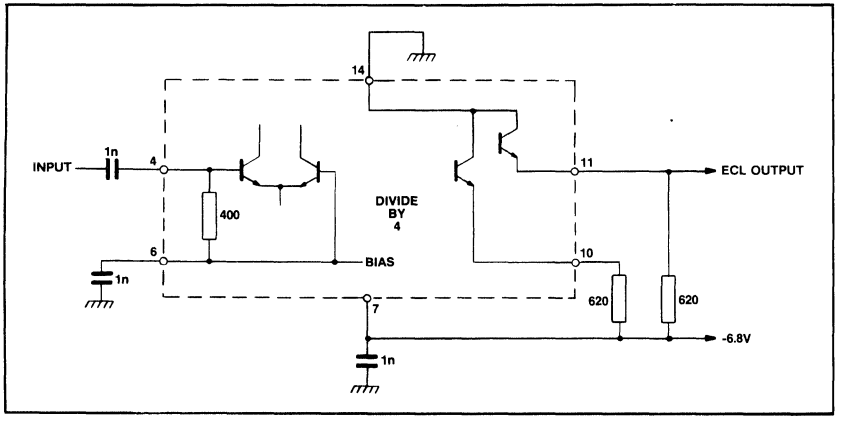


Fig.8 Typical application showing interfacing

SP8716/8/9

520MHz ULTRA LOW CURRENT TWO MODULUS DIVIDERS

SP8716 ÷ 40/41, SP8718 ÷ 64/65, SP8719 ÷ 80/81 are 50mW programmable dividers with a maximum specified operating frequency of 520MHz over the temperature range -40°C to +85°C.

The signal (clock) inputs are biased internally and require to be capacitor coupled. The output stage is of an unusual low power design featuring dynamic pull-up, and optimised for driving CMOS. The 0 to 1 output edge should be used to give the best loop delay performance.

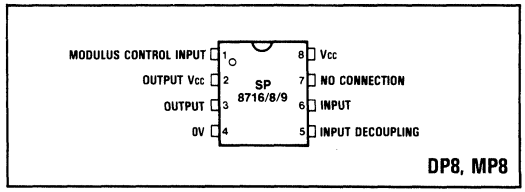


Fig.1 Pin connections - top view

FEATURES

- DC to 520MHz Operation
- -40°C to +85°C Temperature Range
- Control Inputs and Outputs are CMOS Compatible

QUICK REFERENCE DATA

- Supply Voltage 5.2V ± 0.25V
- Supply Current 10.5mA typ.

ABSOLUTE MAXIMUM RATING

Supply voltage (pin 2 or 8):	8V
Storage temperature range:	-55°C to +150°C
Max. junction temperature:	+175°C
Max. clock input voltage:	2.5V p-p

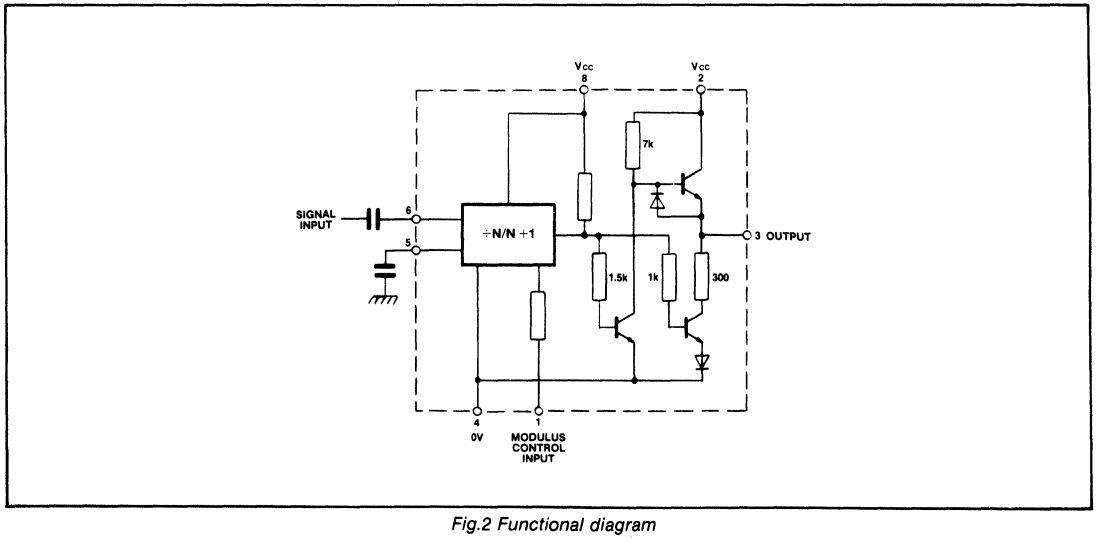


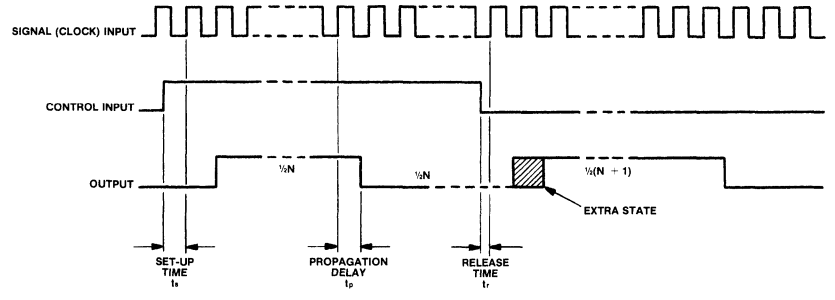
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage: V_{CC} = +4.95 to 5.45V, Temperature: T_{amb} = -40°C to +85°C

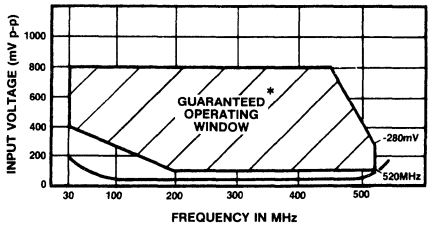
Characteristics	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Max. frequency	f_{max}	520		MHz	Input 100-280mV p-p	1
Min. frequency (sinewave input)	f_{min}		30	MHz	Input 400-800mV p-p	2
Power supply current	I_{CC}		11.9	mA	C_L = 3pF; pins 2, 8 linked	1
Output high voltage	V_{OH}	(V_{CC} -1.2)		V	I_L = -0.2mA	1
Output low voltage	V_{OL}		1	V	I_L = 0.2mA	1
Control input high voltage	V_{INH}	3.3	8	V	÷N	1
Control input low voltage	V_{INL}	0	1.7	V	÷N + 1	1
Control input high current	I_{INH}		0.41	mA	V_{INH} = 8V	1
Control input low current	I_{INL}	-0.20		mA	V_{INL} = 0V	1
Clock to output delay	t_p		28	ns	C_L = 10pF	2
Set-up time	t_s	10		ns	C_L = 10pF	2
Release time	t_r	10		ns	C_L = 10pF	2

NOTES
1. Tested at 25°C only.
2. Guaranteed but not tested.



NOTE
The set-up time t_s is defined as the minimum time that can elapse between a L→H transition of the control input and the next L→H clock pulse transition to ensure that the ÷N mode is obtained.
The release time t_r is defined as the minimum time that can elapse between a H→L transition of the control input and the next L→H clock pulse transition to ensure that the ÷(N + 1) mode is obtained.

Fig.3 Timing diagram



*Tested as specified in table of Electrical Characteristics

Fig.4 Typical input characteristics

OPERATING NOTES

1. The inputs are biased internally and coupled to a signal source with suitable capacitors.
2. If no signal is present the devices will self-oscillate. If this is undesirable it may be prevented by connecting a 15k resistor from one input to pin 4 (ground). This will reduce the sensitivity.
3. The circuits will operate down to DC but slew rate must be better than 100V/µs.
4. The output stage is of an unusual design and is intended to interface with CMOS. External pull-up resistors or circuits must not be used.
5. This device is NOT suitable for driving TTL or its derivatives.

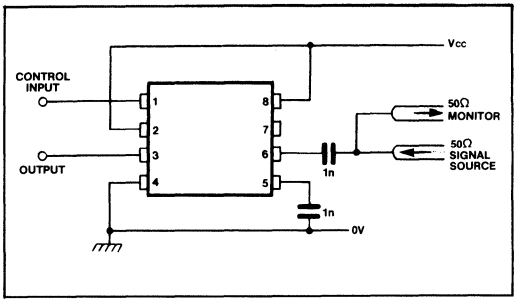


Fig.5 Toggle frequency test circuit

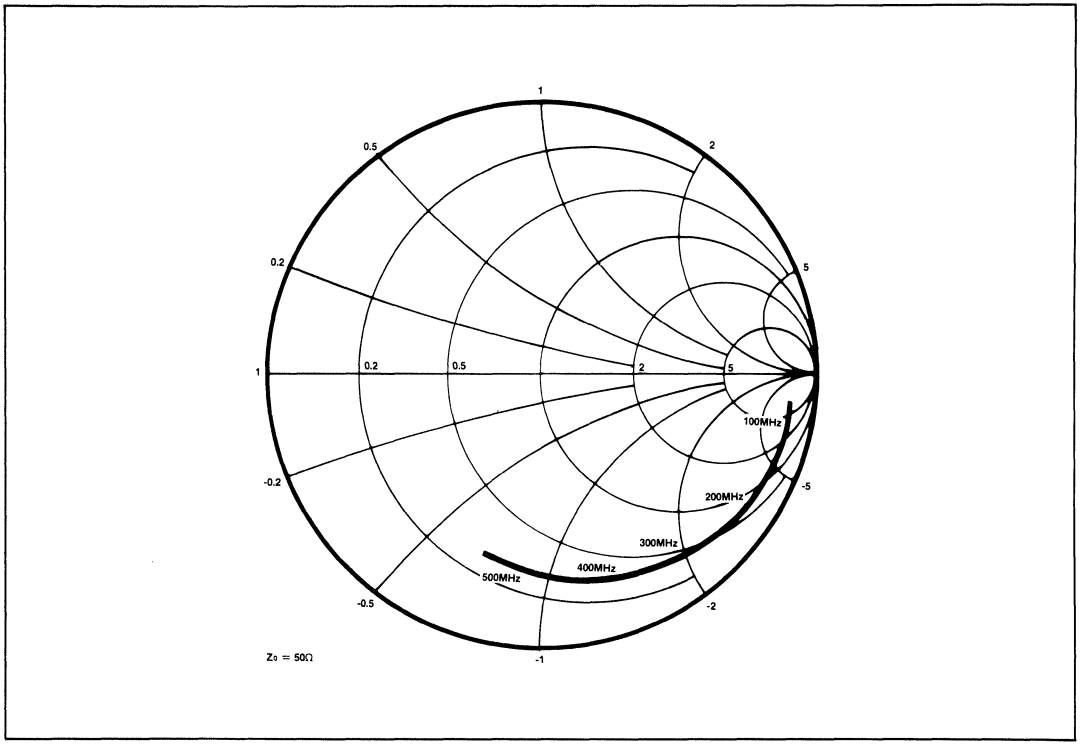


Fig.6 Typical input impedance

PLESSEY
Semiconductors

SP8716/8/9A

520MHz ULTRA LOW CURRENT TWO MODULUS DIVIDERS

The SP8716A ÷ 40/41, SP8718A ÷ 64/65 and SP8719A ÷80/81 are 50mW programmable dividers with a maximum specified operating frequency of 520MHz over the temperature range -55°C to +125°C.

The signal (clock) inputs are biased internally and require to be capacitor coupled. The output stage is of an unusual low power design featuring dynamic pull-up, and optimised for driving CMOS. The 0 to 1 output edge should be used to give the maximum loop delay.

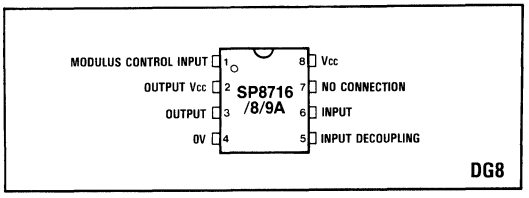


Fig.1 Pin connections - top view

FEATURES

- DC to 520MHz Operation
- -55°C to +125°C Temperature Range
- Control Inputs and Outputs are CMOS Compatible

QUICK REFERENCE DATA

- Supply Voltage 5.2V ± 0.25V
- Supply Current 10.5mA typ.

ABSOLUTE MAXIMUM RATING

Supply voltage (pin 2 or 8):	8V
Storage temperature range:	-55°C to +150°C
Max. junction temperature:	+175°C
Max. clock input voltage:	2.5V p-p

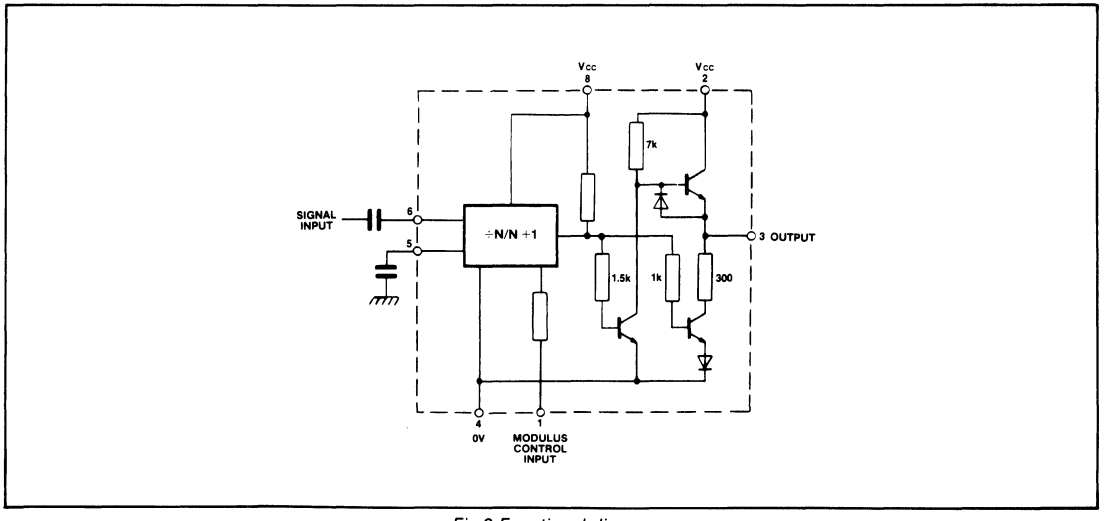


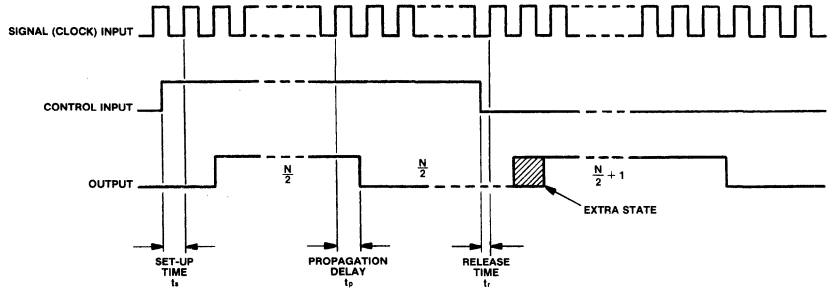
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage: V_{CC} = +4.95 to 5.45V, Temperature: T_{amb} = -55°C to +125°C

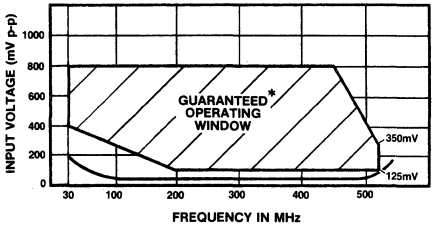
Characteristics	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Max. frequency	f_{max}	520		MHz	Input 125-350mV p-p	1
Min. frequency (sinewave input)	f_{min}		30	MHz	Input 400-800mV p-p	2
Power supply current	I_{CC}		11.9	mA	C_L = 3pF; pins 2, 8 linked	1
Output high voltage	V_{OH}	(V_{CC} -1.2)	1.2	V	I_L = -0.2mA	1
Output low voltage	V_{OL}		1	V	I_L = 0.2mA	1
Control input high voltage	V_{INH}	3.3	8	V	÷N	1
Control input low voltage	V_{INL}	0	1.7	V	÷N + 1	1
Control input high current	I_{INH}		0.41	mA	V_{INH} = 8V	1
Control input low current	I_{INL}	-0.20		mA	V_{INL} = 0V	1
Clock to output delay	t_p		28	ns	C_L = 10pF	2
Set-up time	t_s	10		ns	C_L = 10pF	2
Release time	t_r	10		ns	C_L = 10pF	2

NOTES
1. Tested at 25°C only.
2. Guaranteed but not tested.



NOTE
The set-up time t_s is defined as the minimum time that can elapse between a L→H transition of the control input and the next L→H clock pulse transition to ensure that the ÷N mode is obtained.
The release time t_r is defined as the minimum time that can elapse between a H→L transition of the control input and the next L→H clock pulse transition to ensure that the ÷(N + 1) mode is obtained.

Fig.3 Timing diagram



*Tested as specified in table of Electrical Characteristics

Fig.4 Typical input characteristics

OPERATING NOTES

1. The inputs are biased internally and coupled to a signal source with suitable capacitors.
2. If no signal is present the devices will self-oscillate. If this is undesirable it may be prevented by connecting a 15k resistor from one input to pin 4 (ground). This will reduce the sensitivity.
3. The circuits will operate down to DC but slew rate must be better than 100V/µs.
4. The output stage is of an unusual design and is intended to interface with CMOS. External pull-up resistors or circuits must not be used.
5. This device is NOT suitable for driving TTL or its derivatives.

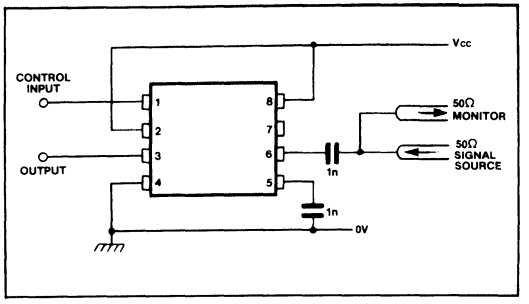


Fig.5 Toggle frequency test circuit

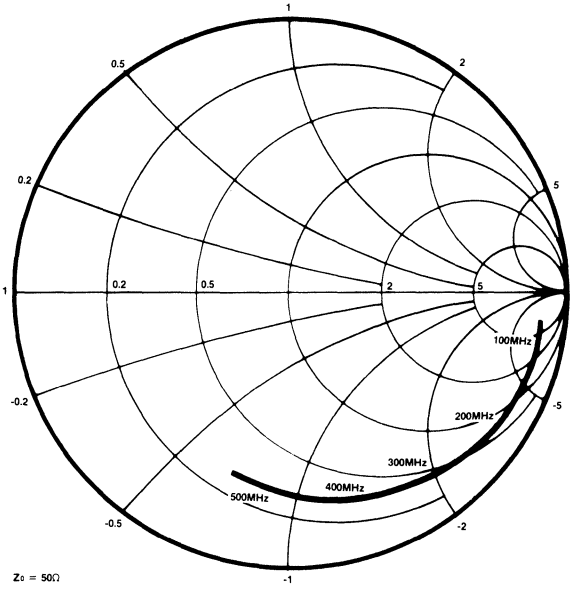


Fig.6 Typical input impedance

SP8720A&B

300MHz ÷ 3/4

The SP8720 is an ECL counter with ECL 10K compatible outputs. It divides by 3 when either control input is in the high state and by 4 when both inputs are low (or open circuit). An AC coupled input of 600mV p-p is required.

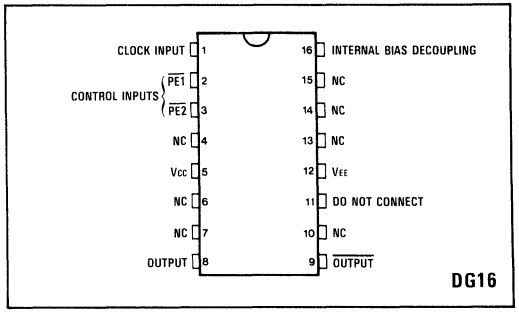


Fig.1 Pin connections - top view

FEATURES

- ECL Compatible Outputs
- AC Coupled Input (Internal Bias)
- Control Inputs ECL III/10K Compatible

QUICK REFERENCE DATA

- Supply Voltage: -5.2V
- Power Consumption: 240mW
- Temperature Range:
  - A Grade: -55°C to +125°C
  - B Grade: -30°C to +70°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage	-8V
Output current	20mA
Storage temperature range	-55°C to +150°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p

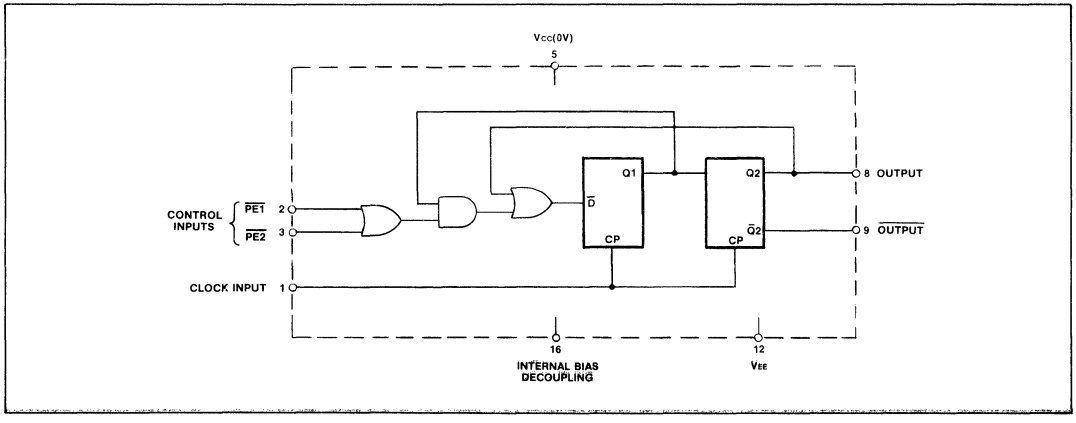


Fig.2 Functional diagram

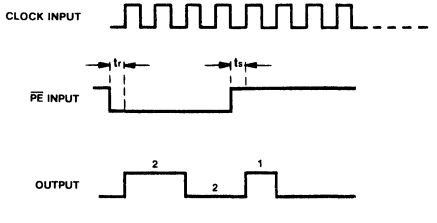
ELECTRICAL CHARACTERISTICS

ECL OPERATION

Supply Voltage: V_{EE} = -5.2 ± 0.25V V_{CC} = 0V
Temperature: A Grade T_{amb} = -55°C to +125°C
B Grade T_{amb} = -30°C to +70°C

Characteristics	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency sinewave input	f_{max}	300		MHz	Input = 400-800mV p-p	Note 3
Minimum frequency sinewave input	f_{min}		40	MHz	Input = 400-800mV p-p	Note 3
Power supply current	I_{EE}		65	mA	V_{EE} = -5.2V	Note 3
ECL output high voltage	V_{OH}	-0.85	-0.7	V	V_{EE} = -5.2V (25° C)	
ECL output low voltage	V_{OL}	-1.8	-1.5	V	V_{EE} = -5.2V (25° C)	
$\overline{PE}$ input high voltage	V_{INH}	-0.93		V	V_{EE} = -5.2V (25° C)	
$\overline{PE}$ input low voltage	V_{INL}		-1.62	V	V_{EE} = -5.2V (25° C)	
Clock to ECL output delay	t_p		6	ns		Note 4
Set-up time	t_s		2.5	ns		Note 4
Release time	t_r		3	ns		Note 4

NOTES
1. Unless otherwise stated the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The temperature coefficients of V_{OH} = +1.63mV/°C, V_{OL} = +0.94mV/°C and of V_{IN} = +1.22mV/°C but these are not tested.
3. SP8720B tested at 25°C only.
4. Guaranteed but not tested.

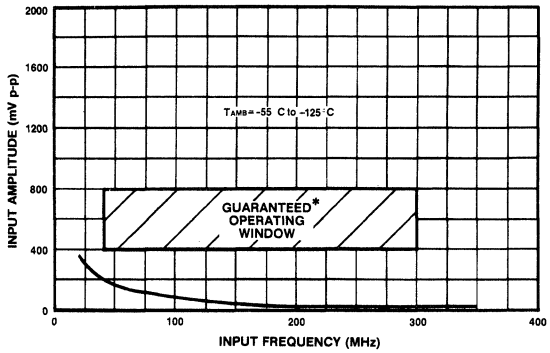


TRUTH TABLE FOR CONTROL INPUTS

$\overline{PE1}$	$\overline{PE2}$	Division Ratio
L	L	4
H	L	3
L	H	3
H	H	3

Fig.3 Timing diagram

NOTE:
The set-up time t_s is defined as minimum time that can elapse between L⟶H transition of control input and the next L⟶H clock pulse transition to ensure that the ÷3 mode is obtained.
The release time t_r is defined as the minimum time that can elapse between a H⟶L transition of a control input and the next L⟶H clock pulse transition to ensure that the ÷4 mode is obtained.



*Tested as specified in table of Electrical Characteristics

Fig.4 Typical input characteristics SP8720A

OPERATING NOTES

1. The clock input is biased internally and is coupled to the signal source with a suitable capacitor. The input signal path is completed by an input reference decoupling capacitor which is connected to earth.
2. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 15k resistor from the input to V_{EE} (i.e. Pin 1 to Pin 12). This will reduce the input sensitivity by approximately 100mV.
3. The circuit will operate down to DC but slew rate must be better than 100V/μs.
4. The Q and $\overline{Q}$ outputs are compatible with ECL II but can be interfaced to ECL 10K as shown in Fig. 7. There is an internal circuit equivalent to a load of 2k pulldown resistor at each output.
5. The PE inputs are ECL III/10K compatible and include a 4.3k internal pulldown resistor. Unused inputs can therefore be left open circuit.
6. The input impedance of the SP8720 varies as a function of frequency. See Fig. 5.

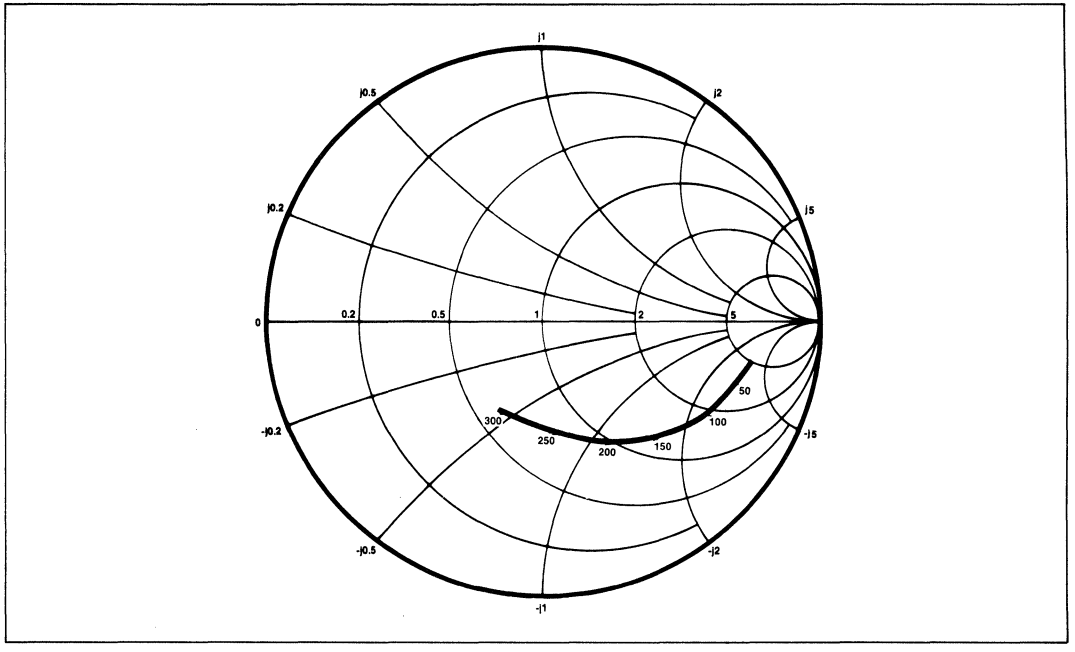


Fig.5 Typical input impedance. Test conditions: supply voltage -5.2V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

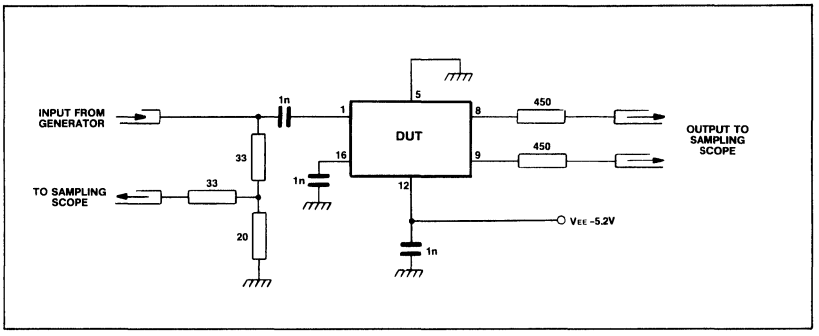


Fig.6 Test circuit

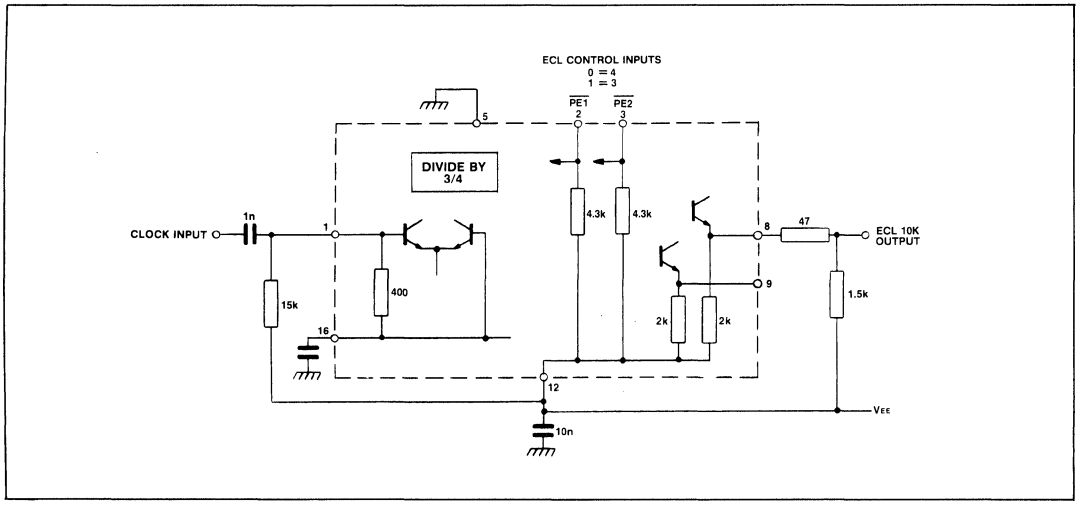


Fig.7 Typical applications circuit showing interfacing

SP8740A&B 300MHz ÷ 5/6
SP8741A&B 300MHz ÷ 6/7

The SP8740 and SP8741 are ECL counters with ECL 10K compatible output. The SP8740/SP8741 divide by 5 and 6 respectively when either control input is in the high state and by 6 and 7 respectively when both inputs are in the low state (or open circuit). An AC coupled input of 600mV is required.

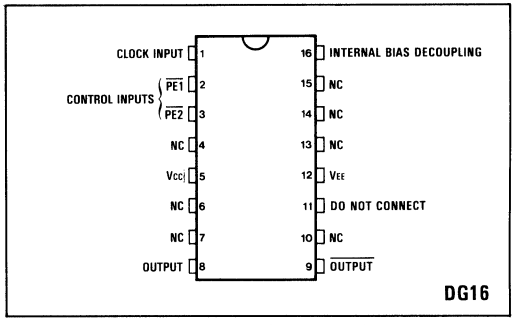


Fig.1 Pin connections - top view

FEATURES

- ECL Compatible Outputs
- ECL Compatible Control Inputs
- AC Coupled Inputs (Internal Bias)

QUICK REFERENCE DATA

- Supply Voltage: -5.2V
- Power Consumption: 240mW
- Temperature Range:
  - A Grade: -55°C to +125°C
  - B Grade: -30°C to +70°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage	-8V
Output current	20mA
Storage temperature range	-55°C to +150°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p

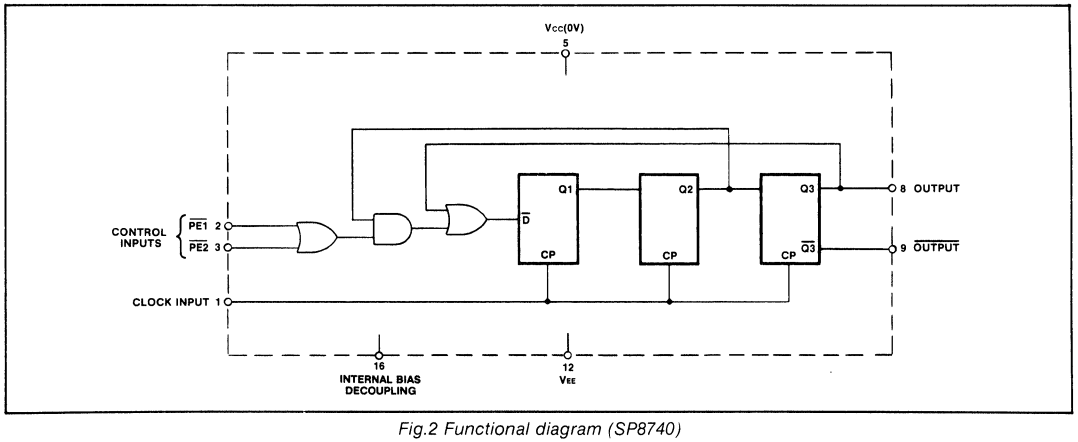


Fig.2 Functional diagram (SP8740)

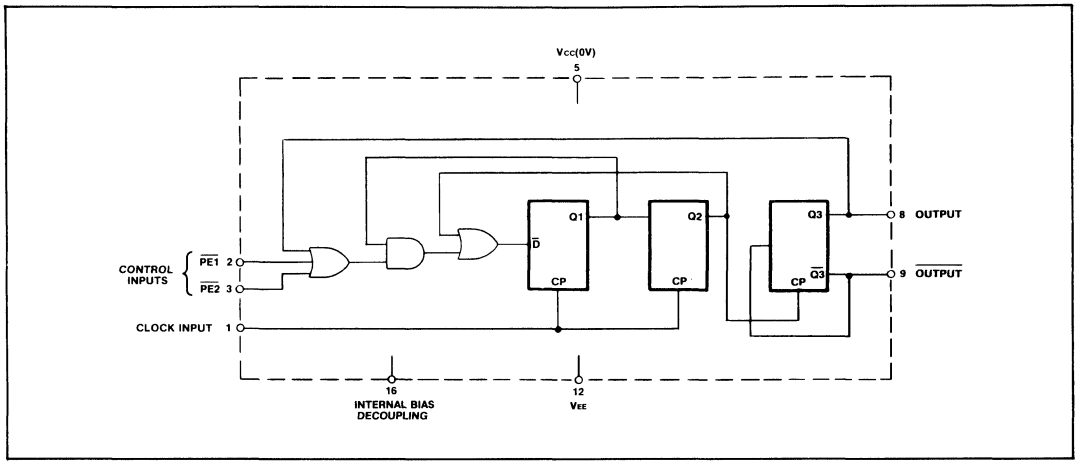


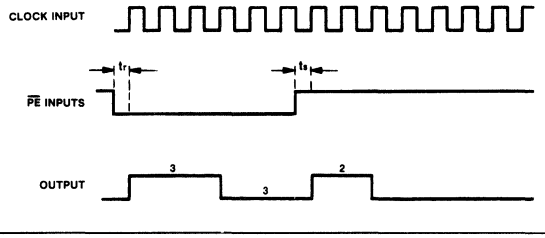
Fig.3 Functional diagram (SP8741)

ELECTRICAL CHARACTERISTICS

Supply Voltage: V_{EE} = -5.2 ± 0.25V V_{CC} = 0V
Temperature: A Grade T_{amb} = -55°C to +125°C
B Grade T_{amb} = -30°C to +70°C

Characteristics	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency sinewave input	f_{max}	300		MHz	Input = 400-800mV p-p	Note 3
Minimum frequency sinewave input	f_{min}		40	MHz	Input = 400-800mV p-p	Note 3
Power supply current	I_{EE}		60	mA		Note 3
ECL output high voltage	V_{OH}	-0.85	-0.7	V	V_{EE}=-5.2V(25° C)	
ECL output low voltage	V_{OL}	-1.8	-1.5	V	V_{EE}=-5.2V(25° C)	
PE input high voltage	V_{INH}	-0.93		V	V_{EE}=-5.2V(25° C)	
PE input low voltage	V_{INL}		-1.62	V	V_{EE}=-5.2V(25° C)	
Clock to ECL output delay	t_p		6	ns		Note 4
Set-up time	t_s		2.5	ns		Note 4
Release time	t_r		3	ns		Note 4

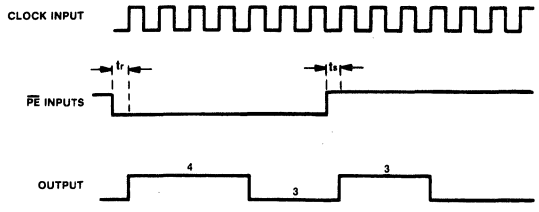
NOTES
1. Unless otherwise stated the electrical characteristics shown above are guaranteed over the full specified supply, frequency and temperature range of both SP8740 and SP8741.
2. The temperature coefficients of V_{OH} = +1.63mV/°C, V_{OL} = +0.94mV/°C and V_{IN} = +1.22mV/°C but these are not tested.
3. SP8740/1B tested at 25°C only.
4. Guaranteed but not tested.



TRUTH TABLE FOR CONTROL INPUTS

$\overline{PE1}$	$\overline{PE2}$	Division Ratio
L	L	6
H	L	5
L	H	5
H	H	5

Fig.4 Timing diagram SP8740



TRUTH TABLE FOR CONTROL INPUTS

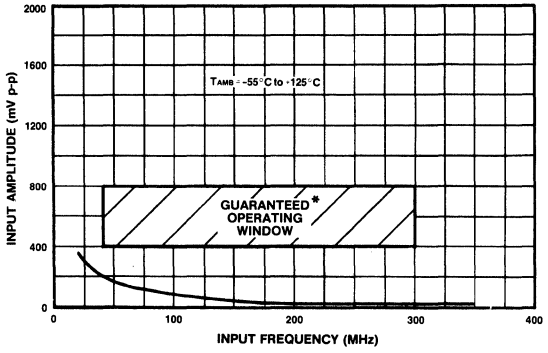
$\overline{PE1}$	$\overline{PE2}$	Division Ratio
L	L	7
H	L	6
L	H	6
H	H	6

Fig.5 Timing diagram SP8741

NOTE:

The set-up time t_s is defined as minimum time that can elapse between L⟶H transition of control input and the next L⟶H clock pulse transition to ensure that the ÷5 or 6 mode is obtained.

The release time t_r is defined as the minimum time that can elapse between a H⟶L transition of a control input and the next L⟶H clock pulse transition to ensure that the ÷6 or 7 mode is obtained.



*Tested as specified in table of Electrical Characteristics

Fig.6 Typical input characteristics SP8740/1A

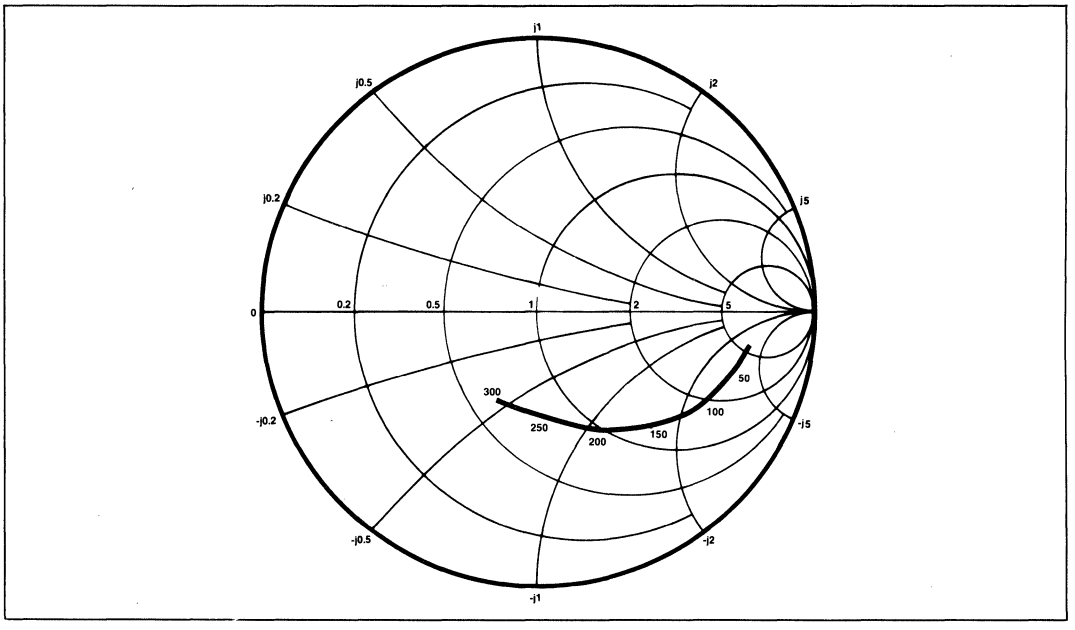


Fig.7 Typical input impedance. Test conditions: supply voltage -5.2V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

OPERATING NOTES

1. The clock input is biased internally and is coupled to the signal source with a suitable capacitor. The input signal path is completed by an input reference decoupling capacitor which is connected to earth.
2. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 15k resistor from the input to V_{EE} (i.e. Pin 1 to Pin 12). This will reduce the input sensitivity by approximately 100mV.
3. The circuit will operate down to DC but slew rate must be better than 100V/us.
4. The Q and $\overline{Q}$ outputs are compatible with ECL II but can be interfaced to ECL 10K as shown in Fig. 9. There is an internal circuit equivalent to a load of 2k pulldown resistor at load output.
5. The PE inputs are ECL III/10K compatible and include a 4.3k internal pulldown resistor. Unused inputs can therefore be left open circuit.
6. The input impedance of the SP8740/1 varies as a function of frequency. See Fig. 7.
7. The SP8740 is not suitable for use in a fixed divide by 6 mode.

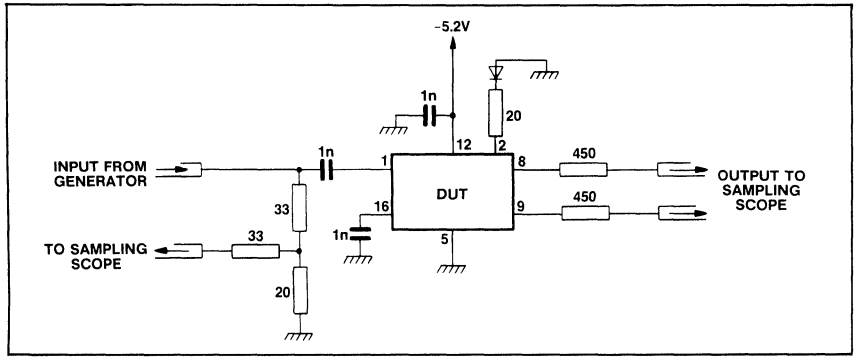


Fig.8 Test circuit

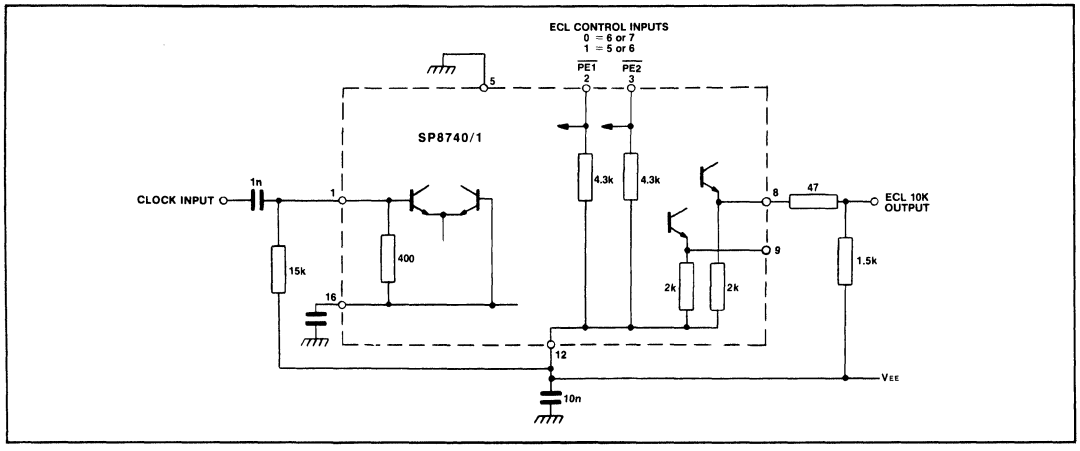


Fig.9 Typical applications circuit showing interfacing

SP8735B

600MHz ÷ 8 (BINARY OUTPUTS)

The SP8735 is an ECL counter with binary outputs. In addition, carry outputs are provided in TTL and ECL. The AC coupled input requires 600mV p-p, and the outputs are open collectors. A TTL compatible reset is provided, making this device ideal for instrumentation applications.

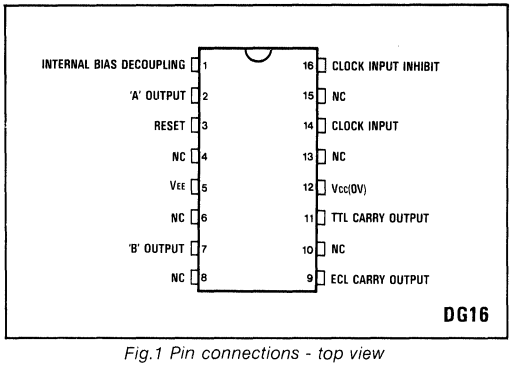


Fig.1 Pin connections - top view

FEATURES

- Binary Outputs to Open Collectors
- Reset Input TTL Compatible
- AC Coupled Input
- Clock Inhibit ECL Compatible
- TTL and ECL Compatible Carry Outputs

QUICK REFERENCE DATA

- Supply Voltage: 5.2V
- Power Consumption: 400mW
- Temperature Range: 0 to +70°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage	-8V
Binary ourput voltage	V_{EE} +11V
Storage temperature range	-55°C to +150°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p

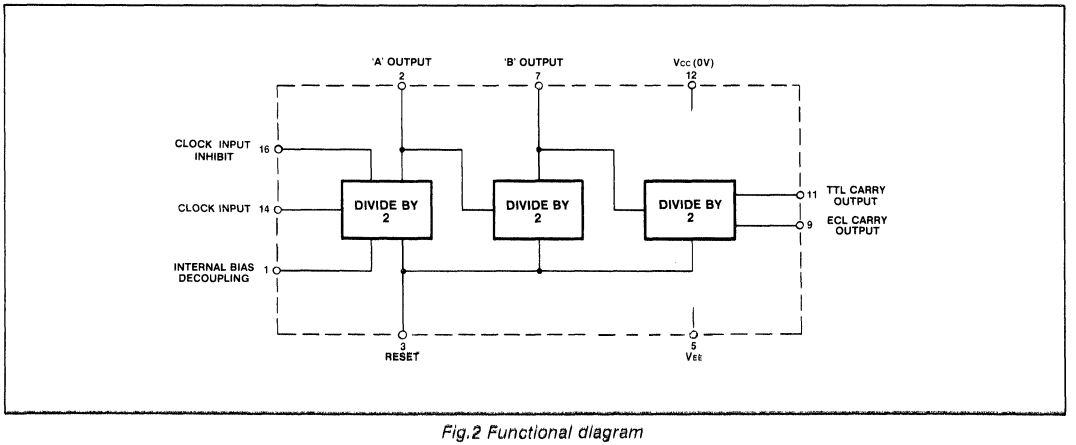


Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply Voltage: V_{CC} = 0V V_{EE} = -5.2V ± 0.25V
Temperature: T_{amb} = 0°C to +70°C

Characteristics	Symbol	Value Min.	Value Max.	Units	Conditions	Notes
Maximum frequency (sinewave input)	f_{max}	600		MHz	Input = 400-800mV p-p	Note 5
Minimum frequency (sinewave input)	f_{min}		40	MHz	Input = 400-800mV p-p	Note 7
Power supply current	I_{EE}		90	mA	V_{EE} = -5.2V	Note 6
Clock inhibit high voltage	V_{INH}	-0.96		V	V_{EE} = -5.2V (25°C)	
Clock inhibit low voltage	V_{INL}		-1.65	V	V_{EE} = -5.2V (25°C)	
TTL output high voltage (pin 2,7)	V_{OH}	2.4		V	10kΩ from TTL output to +5V	Note 6
TTL output low voltage (pin 2,7)	V_{OL}		0.4	V	10k from TTL output to +5V	Note 6
TTL carry high voltage (pin 11)	V_{OH}	2.4		V	5kΩ from TTL output to +5V	Note 6
TTL carry low voltage (pin 11)	V_{OL}		0.4	V	5kΩ from TTL output to +5V	Note 6
ECL carry high voltage (pin 9)	V_{OH}	-0.9	-0.7	V	V_{EE} = -5.2V (25°C)	
ECL carry low voltage (pin 9)	V_{OL}	-1.8	-1.5	V	V_{EE} = -5.2V (25°C)	
Edge speed for correct operation at maximum frequency	t_E		2.5	ns	10% to 90%	Note 7
Reset on time for correct operation	t_{ON}	100		ns		Note 7
Reset input high voltage	V_{INH}	2.4		V		Note 6
Reset input low voltage	V_{INL}		0.5	V		Note 6

NOTES
1. Unless otherwise stated the electrical characteristics are guaranteed over specified supply, frequency and temperature range.
2. The temperature coefficient of V_{OH} (ECL) = +1.3mV/°C and V_{OL} = +0.5mV/°C but these are not tested.
3. The temperature coefficient of inhibited threshold voltage = +0.24mV/°C but this is not tested.
4. The test configuration for dynamic testing is shown in Fig.8.
5. Tested at 0°C and +70°C only.
6. Tested at +25°C only.
7. Guaranteed but not tested.

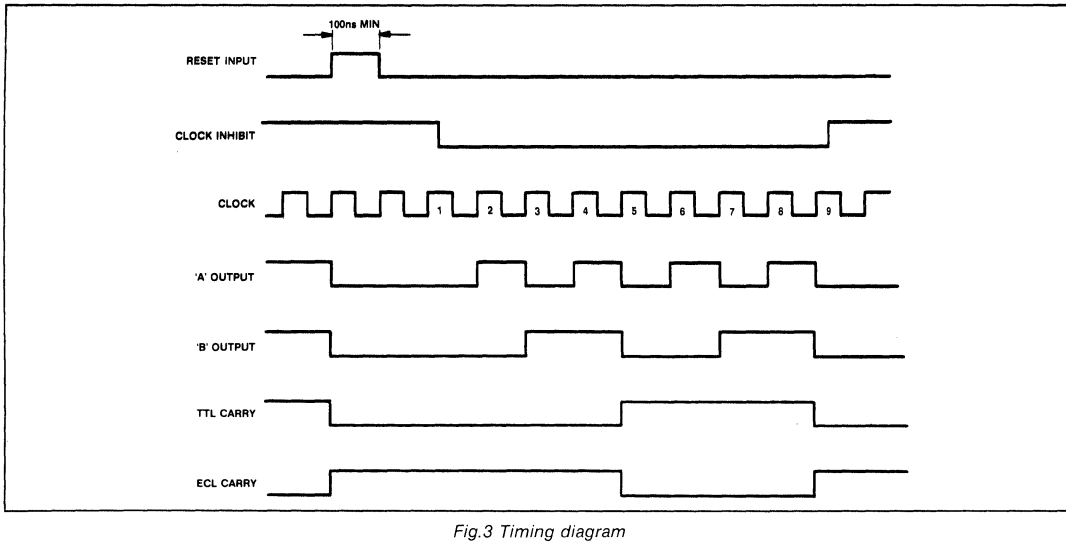
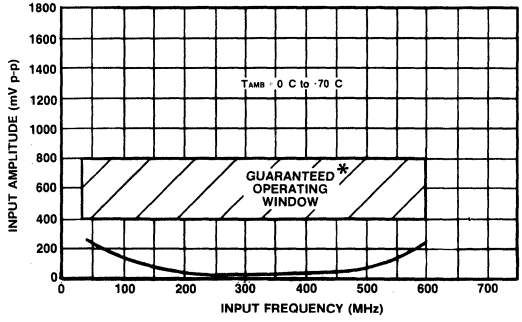


Fig.3 Timing diagram



*Tested as specified above.

Fig.4 Typical input characteristics SP8735

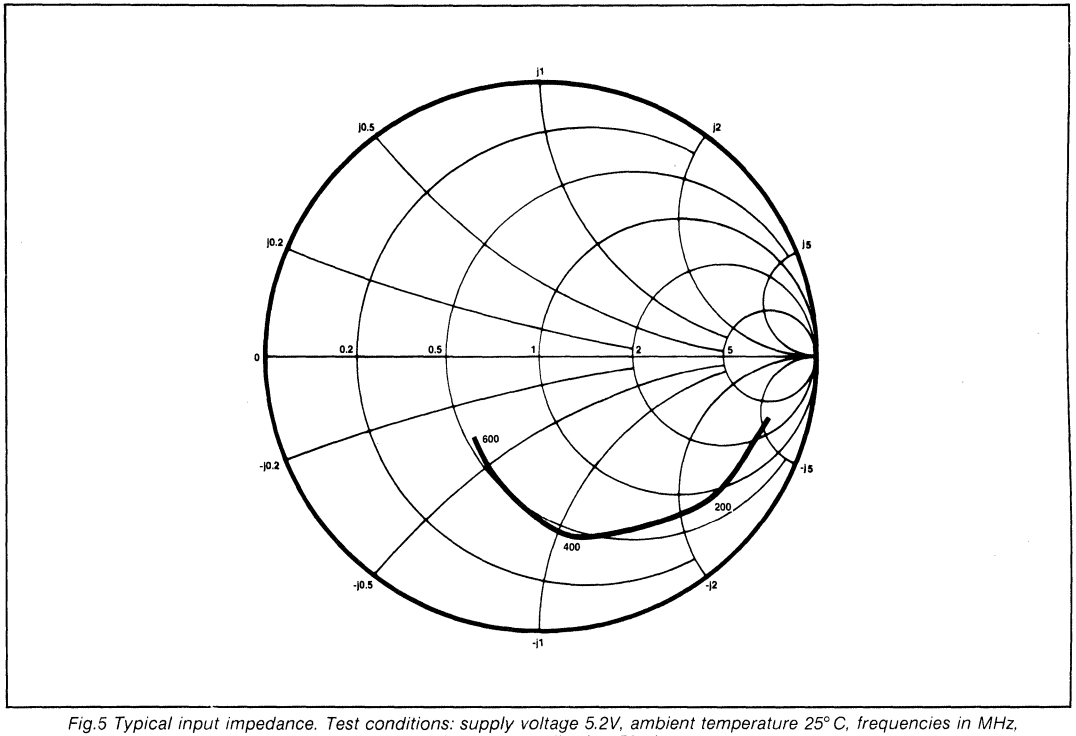


Fig.5 Typical input impedance. Test conditions: supply voltage 5.2V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

OPERATING NOTES

1. The clock input (pin 14) should be capacitively coupled to the signal source. The input signal path is completed by connecting a capacitor from the internal bias decoupling, pin 1 to ground.
2. In the absence of a signal the devices will self-oscillate. This can be prevented by connecting a 68k resistor between the clock input and the negative supply (pin 5).
3. The device will operate down to DC but the input slew rate must be better than 100V/µs.
4. The ECL Carry output (pin 9) is ECL II compatible but can be interfaced ECL III/10K by the inclusion of two resistors. See Fig.7.
5. The clock inhibit is compatible with ECL III/10K throughout the temperature range.
6. The 'A', 'B' and TTL Carry outputs are current sources and require the addition of 10k (pins 2 and 7) and 5k (pin 11) to +5V for TTL compatibility. See Fig. 6. This gives a fan-out = 1. The fan-out can be increased by buffering the output with a PNP emitter follower, see Fig. 9.
7. It is important to note that a positive going transition on either the clock or clock inhibit will clock the device provided of course that each input is in the low state.
8. Input impedance is a function of frequency. See Fig. 5.

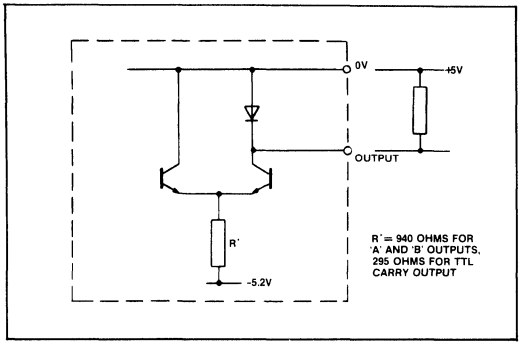


Fig.6 TTL output circuit

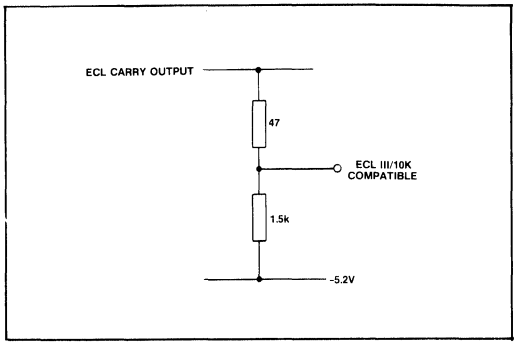


Fig.7 ECL II to ECL III/10K interface

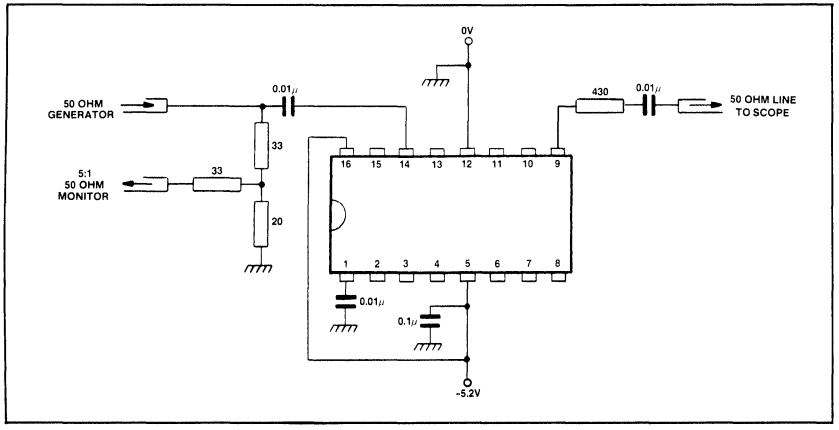


Fig.8 SP8735 high frequency test circuit

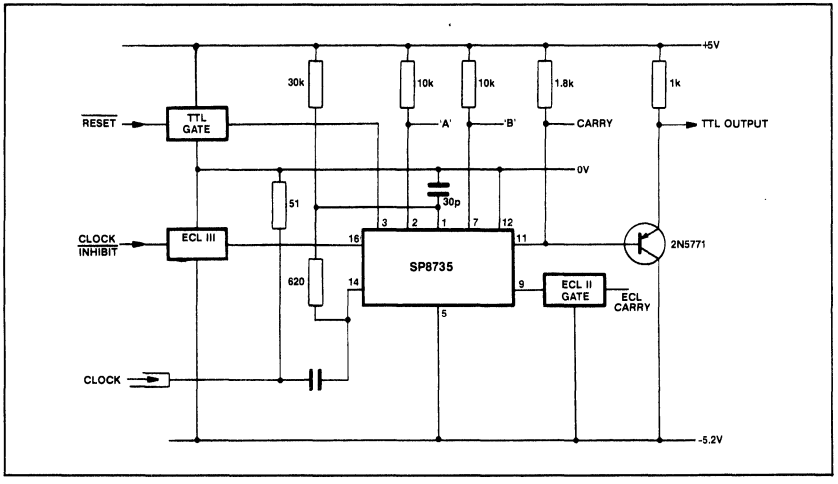


Fig.9 Typical application showing interfacing

SP8743A 450MHz ÷ 8/9
SP8743B 500MHz ÷ 8/9

The SP8743 is an ECL counter with ECL 10K compatible outputs. It divides by 8 when either control input is in the high state and by 9 when both inputs are low (or open circuit). An AC coupled input of 600mV p-p is required.

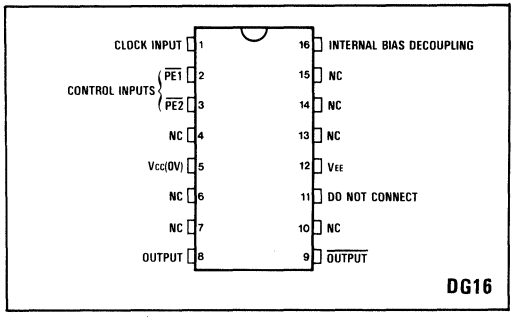


Fig.1 Pin connections - top view

FEATURES

- ECL Compatible Outputs
- ECL Compatible Control Inputs
- AC Coupled Input (Internal Bias)

QUICK REFERENCE DATA

- Supply Voltage: -5.2V
- Power Consumption: 240mW
- Temperature Range:
  - A Grade: -55°C to +125°C
  - B Grade: -30°C to +70°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage	-8V
Output current	20mA
Storage temperature range	-55°C to +150°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p

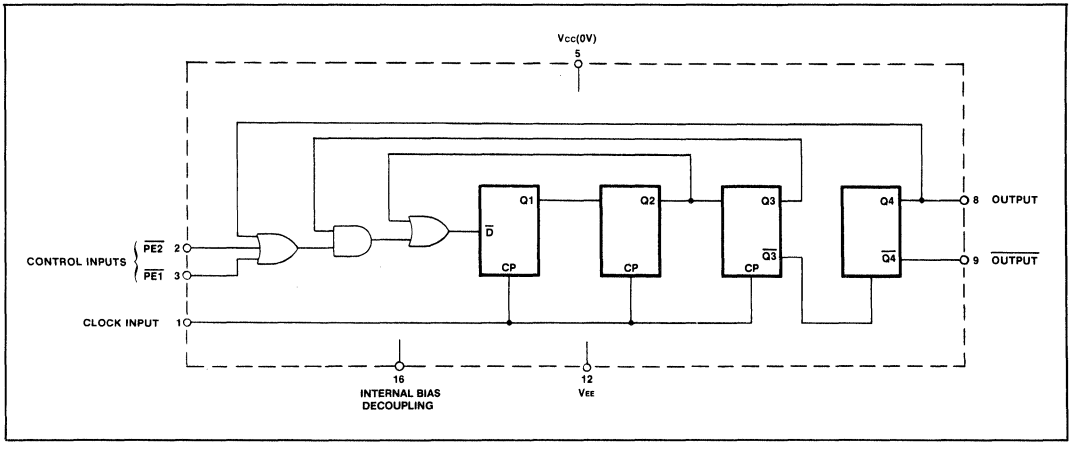


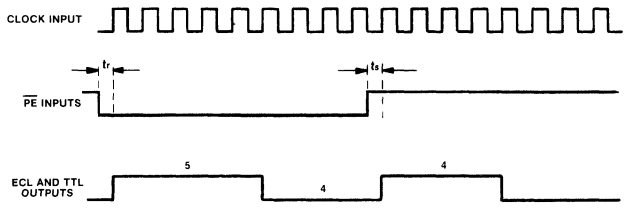
Fig.2 Function diagram

ELECTRICAL CHARACTERISTICS

Supply Voltage: V_{EE} = -5.2 ± 0.25V V_{CC} = 0V
Temperature: A Grade T_{amb} = -55°C to +125°C
B Grade T_{amb} = -30°C to +70°C

Characteristic	Symbol	Value		Units	Grade	Conditions	Notes
		Min.	Max.				
Maximum frequency	f_{max}	450		MHz	A	Input = 400 - 800mV p-p	Note 4
sinewave input		500		MHz	B	Input = 400 - 800mV p-p	Note 4
Minimum frequency	f_{min}		40	MHz	Both	Input = 400 - 800mV p-p	Note 5
sinewave input							
Power supply current	I_{EE}		60	mA	Both	V_{EE} = -5.2V	Note 6
ECL output high voltage	V_{OH}	-0.85	-0.7	V	Both	V_{EE} = -5.2V(25° C)	
ECL output low voltage	V_{OL}	-1.8	-1.5	V	Both	V_{EE} = -5.2V(25° C)	
PE input high voltage	V_{INH}	-0.93		V	Both	V_{EE} = -5.2V(25° C)	
PE input low voltage	V_{INL}		-1.62	V	Both	V_{EE} = -5.2V(25° C)	
Clock to ECL output delay	t_p		6	ns	Both		Note 5
Set-up time	t_s	1		ns	Both		Note 5
Release time	t_r	2.5		ns	Both		Note 5

NOTES
1. Unless otherwise stated the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The temperature coefficients of V_{OH} = +1.63mV/°C, V_{OL} = +0.94mV/°C and of V_{IN} = +1.22mV/°C.
3. The test configuration for dynamic testing is shown in Fig.6.
4. Tested at low and high temperature only (not at 25°C)
5. Guaranteed but not tested.
6. Tested at 25°C only.

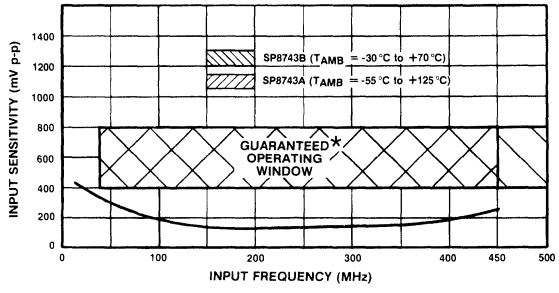


TRUTH TABLE FOR CONTROL INPUTS

$\overline{PE1}$	$\overline{PE2}$	Division Ratio
L	L	9
H	L	8
L	H	8
H	H	8

Fig.3 Timing diagram

NOTE:
The set-up time t_s is defined as minimum time that can elapse between L⟶H transition of control input and the next L⟶H clock pulse transition to ensure that the ÷8 mode is obtained.
The release time t_r is defined as the minimum time that can elapse between a H⟶L transition of a control input and the next L⟶H clock pulse transition to ensure that the ÷9 mode is obtained.



* Tested as specified in Table of Electrical Characteristics

Fig.4 Typical input characteristics of SP8743

OPERATING NOTES

1. The clock input is biased internally and is coupled to the signal source with a suitable capacitor. The input signal path is completed by an input reference decoupling capacitor which is connected to earth.
2. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 15k resistor from the input to V_{EE} (i.e. Pin 1 to Pin 12). This will reduce the input sensitivity by approximately 100mV.
3. The circuit will operate down to DC but slew rate must be better than 100V/μs.
4. The Q and $\overline{Q}$ outputs are compatible with ECL II but can be interfaced to ECL 10K as shown in Fig. 7. There is an internal circuit equivalent to a load of 2k pulldown resistor at each output.
5. The PE inputs are ECL III/10K compatible and include a 4.3k internal pulldown resistor. Unused inputs can therefore be left open circuit.
6. The input impedance of the SP8743 varies as a function of frequency. See Fig. 5.

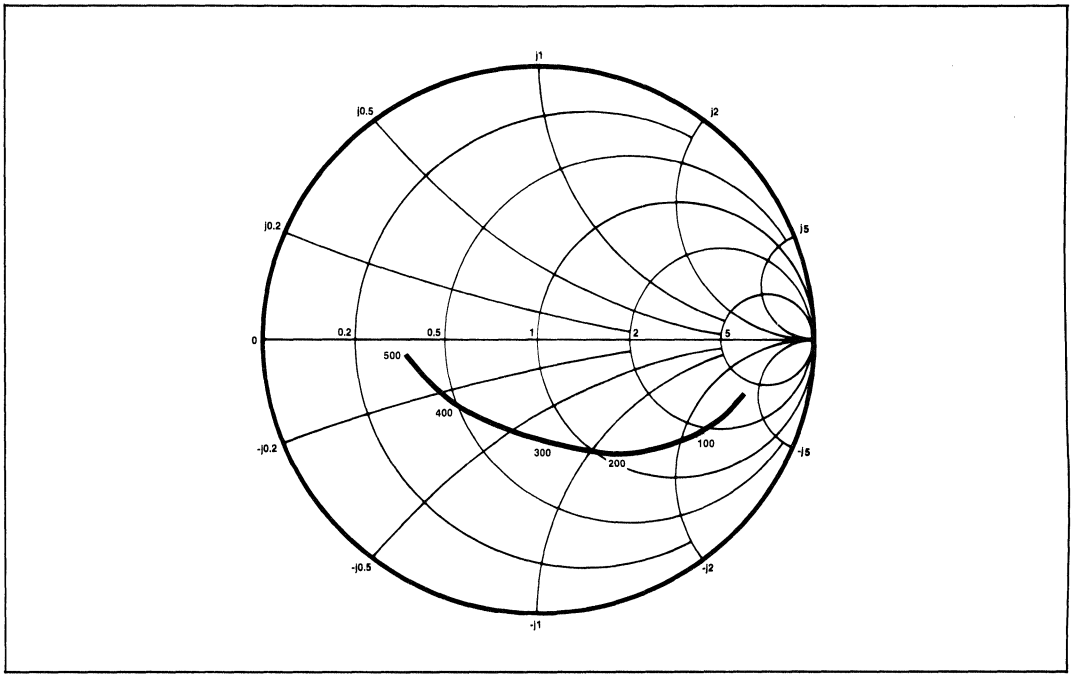


Fig.5 Typical input impedance. Test conditions: supply voltage -5.2V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

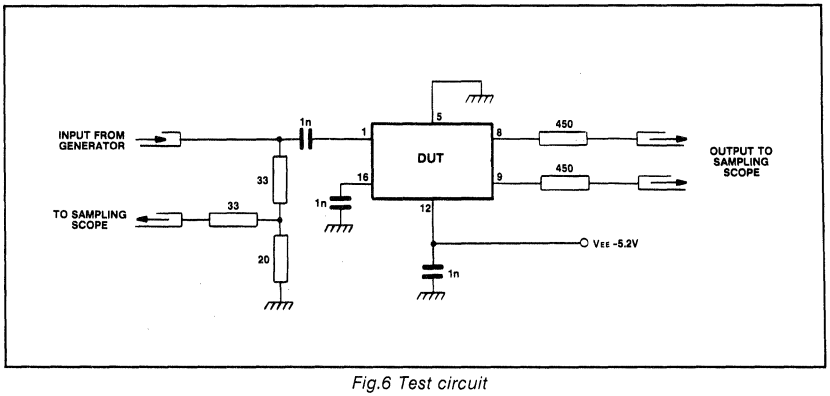


Fig.6 Test circuit

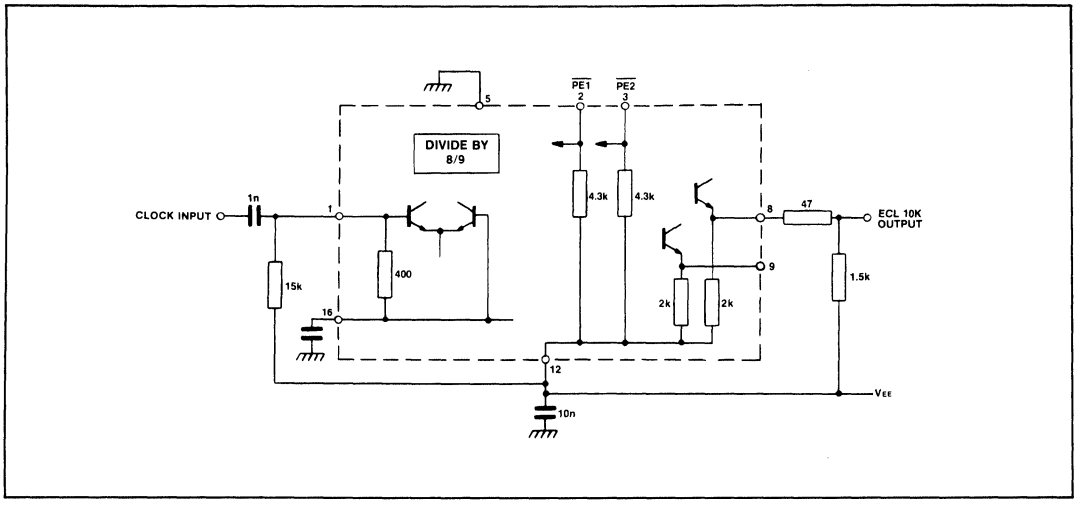


Fig.7 Typical applications circuit showing interfacing

SP8755A&B

1200MHz ÷ 64

The SP8755 is a divide by 64 prescaler which operates from a standard 5V TTL supply and will drive TTL directly. The SP8755A operates over the full military temperature range (-55°C to +125°C).

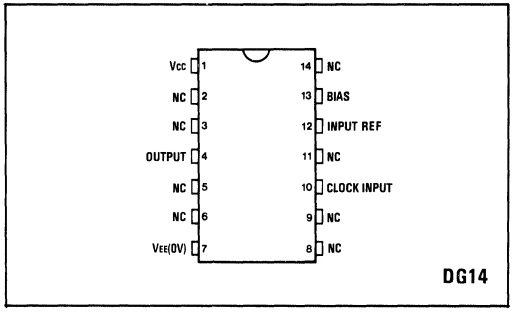


Fig.1 Pin connections - top view

FEATURES

- TTL Compatible Output
- AC Coupled Input (Internal Bias)

QUICK REFERENCE DATA

- Supply Voltage: 5V
- Power Consumption: 270mW
- Temperature Range:
  - A Grade: -55°C to +125°C
  - B Grade: -30°C to +70°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage	8V
Output current	±30mA
Storage temperature range	-55°C to +150°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p

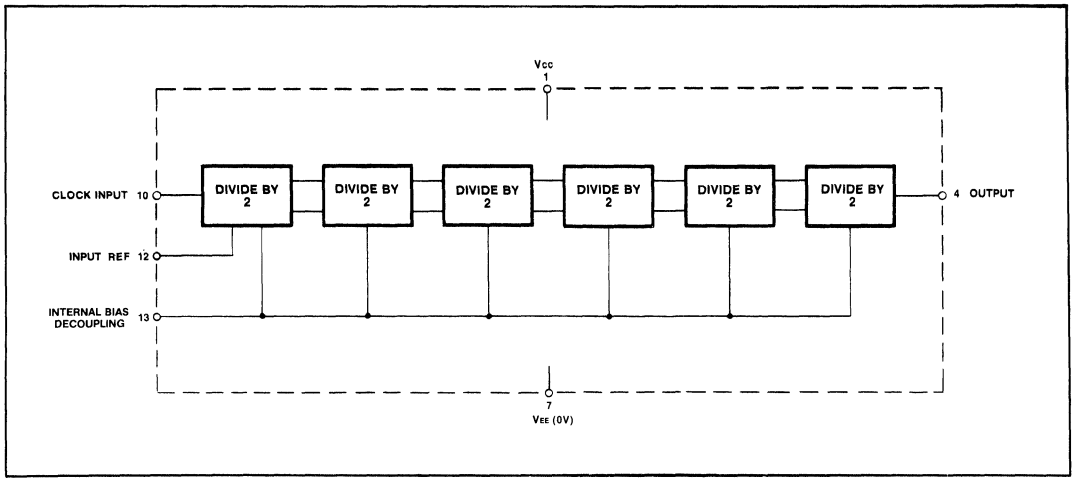


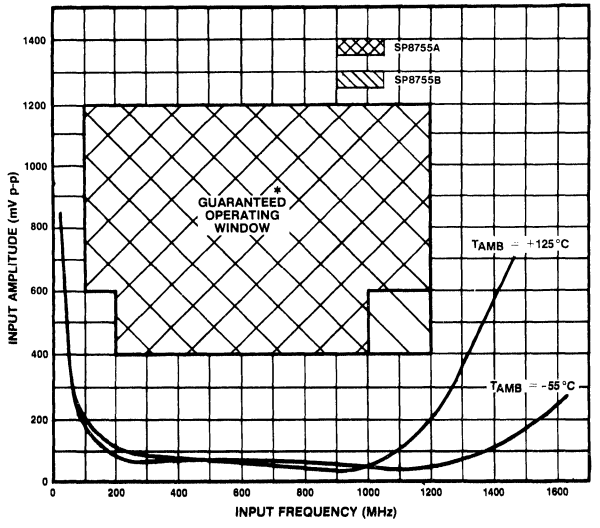
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply Voltage: V_{CC} = 5.0 ± 0.25V V_{EE} = 0V
Temperature: A grade T_{amb} = -55°C to +125°C
B grade T_{amb} = -30°C to +70°C

Characteristics	Symbol	Value		Units	Grade	Conditions
		Min.	Max.			
Maximum frequency sinewave input	f_{max}	1.2		GHz	SP8755A	Input = 600-1200mV p-p
		1.2		GHz	SP8755B	Input = 400-1200mV p-p
Minimum frequency sinewave input	f_{min}		100	MHz	Both	Input = 600-1200mV p-p
Power supply current	I_{EE}		75	mA	Both	
Output high voltage	V_{OH}	2.5		V	Both	
Output low voltage	V_{OL}		0.45	V	Both	Sink current = 5mA

NOTES
1. Unless otherwise stated,the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The test configuration for dynamic testing is shown in Fig.5.
3. Above characteristics are not tested at 25°C (tested at low and high temperature only).



*Tested as specified in table of Electrical Characteristics

Fig.3 Typical input characteristics SP8755A/B

OPERATING NOTES

1. The clock input is biased internally and is connected to the signal source via a capacitor. The input signal path is completed by an input reference decoupling capacitor which is connected to earth.
2. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting an 18k resistor between input and V_{EE} (i.e. Pin 10 to Pin 7). This will reduce sensitivity by approximately 100mV.
3. The device will operate down to DC but input slew rate must be better than 100V/μs.
4. The output stage is a standard totem pole TTL and can therefore be interfaced directly to TTL.

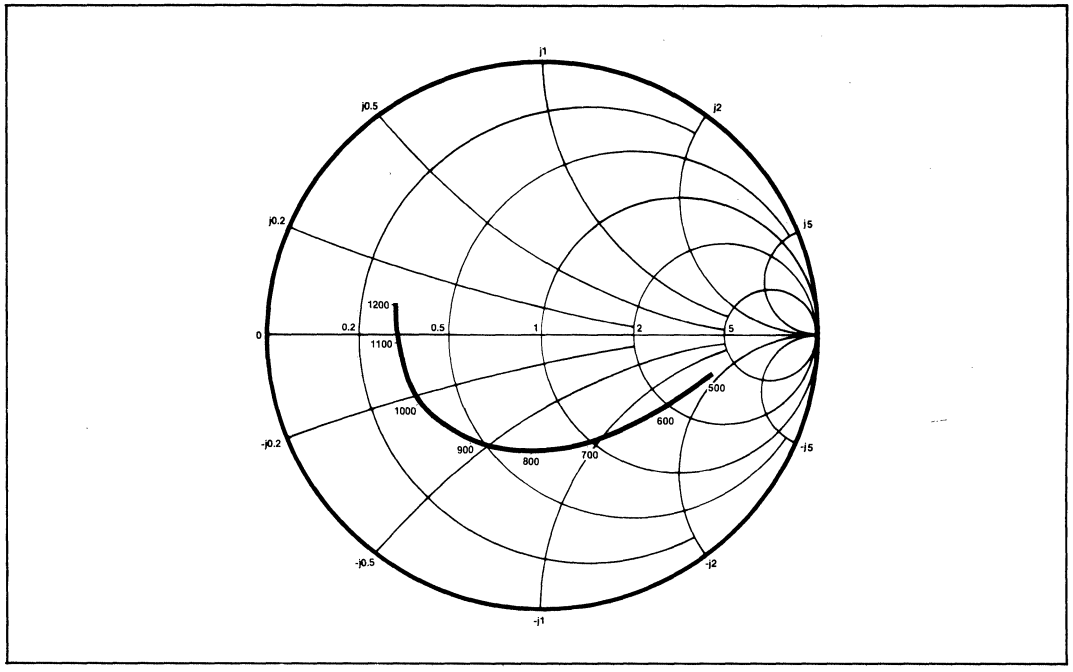


Fig.4 Typical input impedance. Test conditions: supply voltage 5V, ambient temperature 25°C. Frequencies in MHz, impedances normalised to 50 ohms.

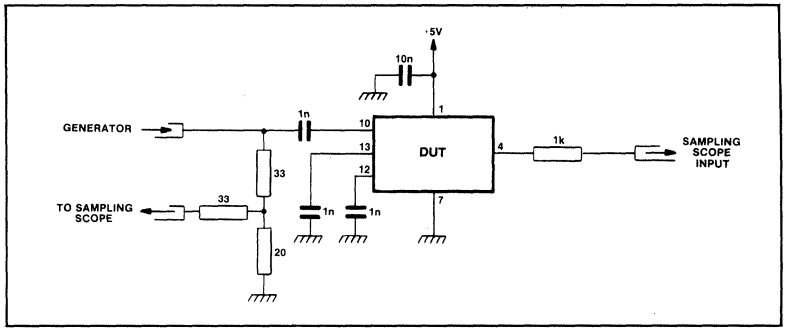


Fig.5 Test circuit

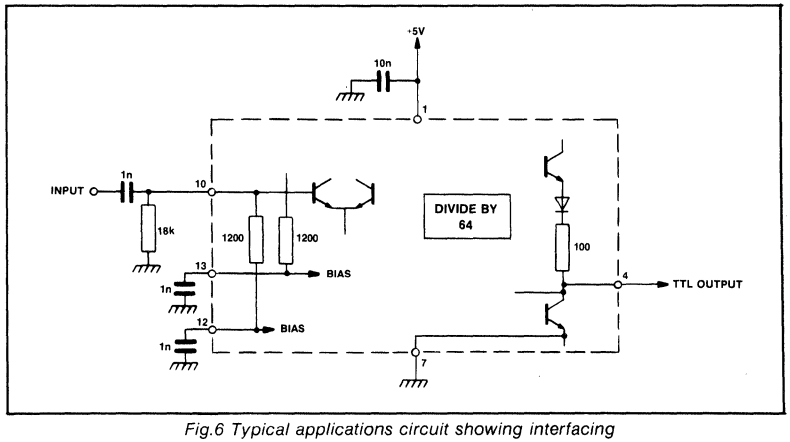


Fig.6 Typical applications circuit showing interfacing

PLESSEY
Semiconductors

SP8782A & B

1GHz ÷ 16/17, 32/33 MULTI-MODULUS DIVIDER

The SP8782 is a 1GHZ multi modulus divider which divides by 16/17 when the Ratio select pin is low and 32/33 when this pin is high. The Modulus control pin selects either a divide by 16 or 32 when the pin is high or 17 or 33 when the pin is low. The device uses resynchronisation techniques to reduce the effects of propagation delays in frequency synthesis. The 'A' Grade device is characterised over the full military temperature range of -55°C to +125°C, the 'B' Grade over the industrial range of -40°C to +85°C.

FEATURES

- Advanced Resynchronising Techniques to Negate Loop Delay Effects
- CMOS Compatible Output Capability
- Multi-Modulus Division

QUICK REFERENCE DATA

- Supply Voltage Range: 4V to 6V
- Full Military Temperature Range:-55°C to +125°C

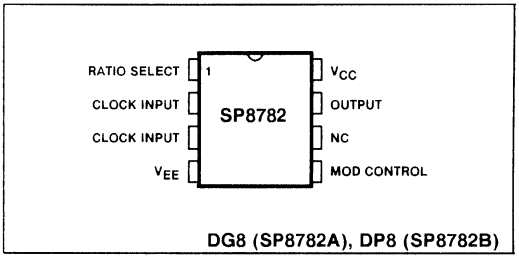


Fig.1 Pin connections - top view

ABSOLUTE MAXIMUM RATINGS

Supply voltage	6V
Clock input level	2.5V p-p
Junction temperature	+175°C
Storage temperature range	
SP8782A	-55°C to +150°C
SP8782B	-55°C to +125°C

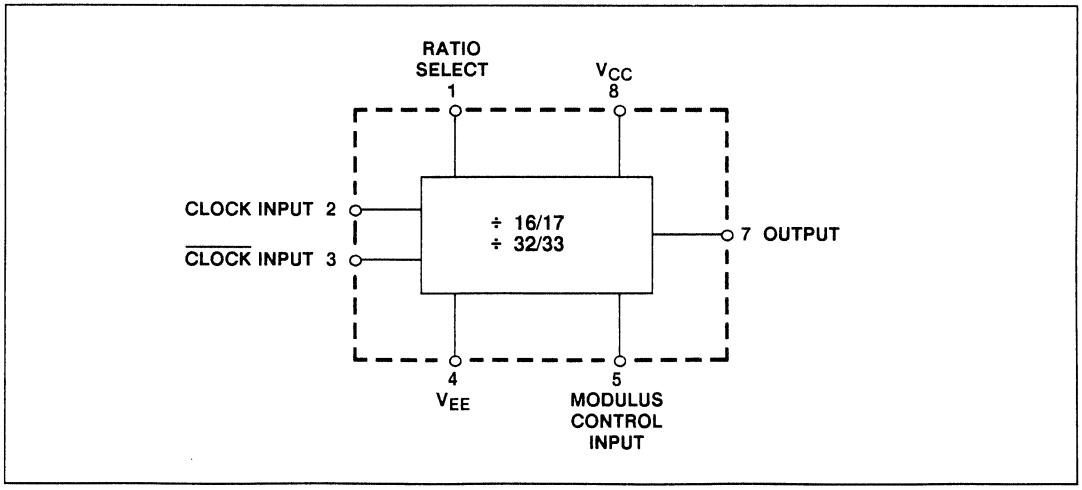


Fig.2 SP8782 functional diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
T_{amb} = SP8782A: -55°C to +125°C, SP8782B -40°C to +85°C, V_{CC} = +4V to +6V

Characteristic	Pin	Value		Units	Conditions
		Min.	Max.		
Max. sinewave input frequency	2,3	1		GHz	Input = 200mV - 1200mV p-p
Min. sinewave input frequency	2,3		50	MHz	Input = 400mV - 1200mV p-p
Min. slew rate for LF operation	2,3		100	V/µs	
Power supply current I_{EE}	8		40	mA	Outputs unloaded
Output low voltage	7	0	1.7	V	
Output high voltage	7	3.2	V_{CC}	V	
Modulus control input high voltage	5	$0.7V_{CC}$	V_{CC}	V	At driver end of 3k resistor
Modulus control input low voltage	5	0	$0.4V_{CC}$	V	At driver end of 3k resistor
Modulus control input high current	5	0.6	0.9	mA	Via 3k to V_{CC}
Modulus control input low current	5	-0.6	-0.9	mA	Via 3k to 0V
Ratio select input high voltage	1	$0.6V_{CC}$	V_{CC}	V	
Ratio select input low voltage	1	0	$0.3V_{CC}$	V	
Ratio select input current	1	-10	10	µA	
Clock to output propagation delay	2,3,7		3	ns	
Set up time	5		1	ns	
Release time	5		1	ns	

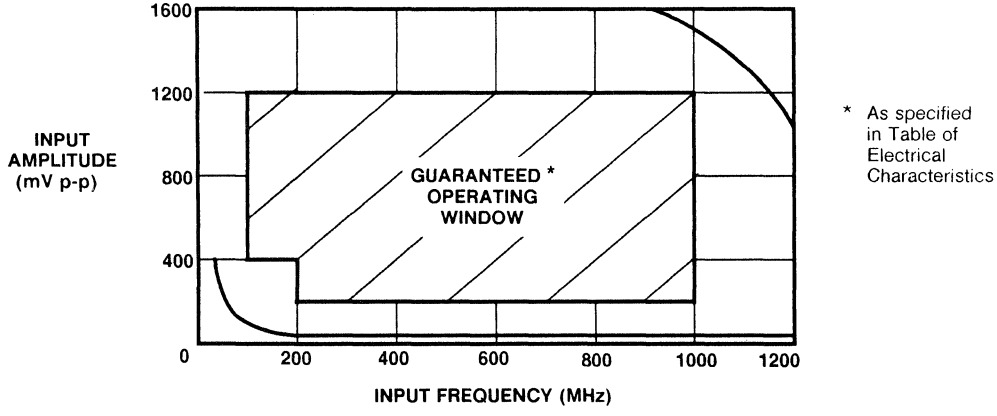


Fig.2 Typical input characteristics SP8782

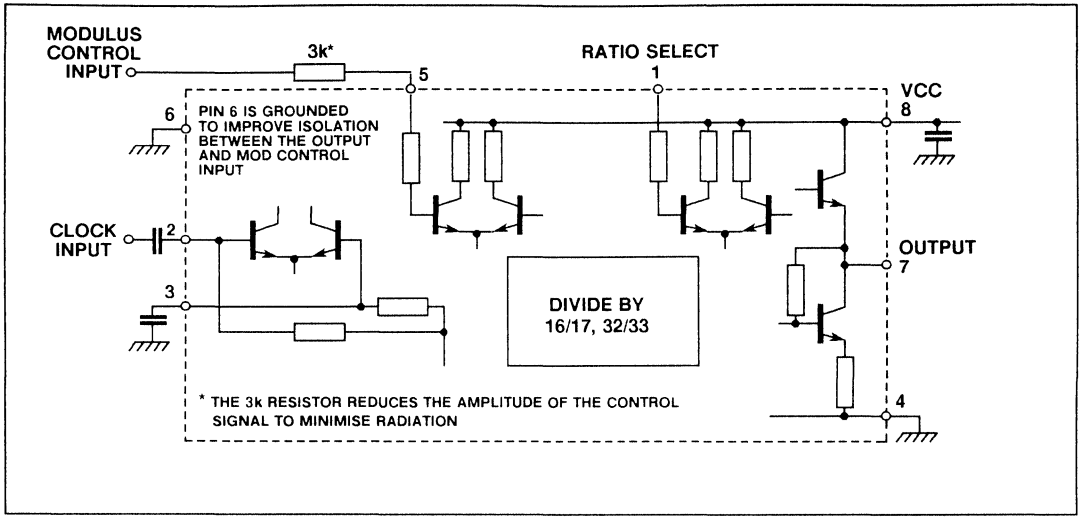


Fig.3 Typical applications showing interfacing

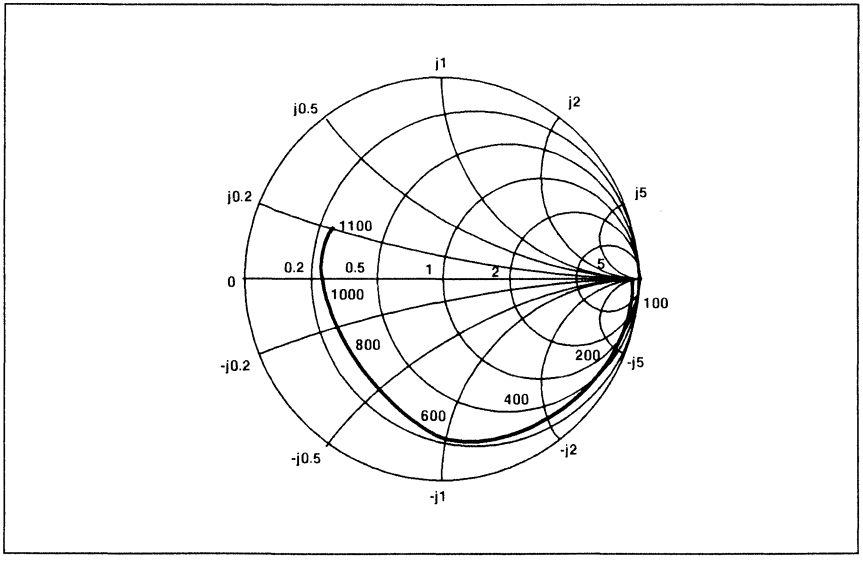


Fig.4 Typical input Impedance. Test conditions: supply voltage 5V, ambient temperature 25°C, frequencies in MHz, impedancies normalised to 50 Ohms

SP8785A&B 1000MHz ÷ 20/22
SP8786A&B 1300MHz ÷ 20/22

The SP8785 and SP8786 are high speed 2 modulus counters for use up to 1.0 and 1.3GHz respectively. They feature ECL compatible control inputs and outputs and are available in either the -30°C to +70°C (B Grade) or -55°C to +125°C (A Grade) temperature ranges.

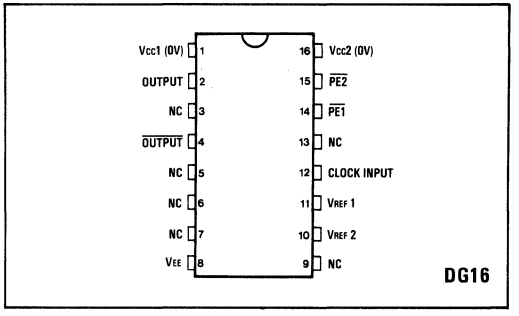


Fig.1 Pin connections - top view

FEATURES

- ECL Compatible Outputs
- AC Coupled Input
- Control Inputs ECL Compatible

QUICK REFERENCE DATA

- Supply Voltage: -5.2V
- Power Consumption: 450mW (Typ.)
- Temperature Range:
  - A Grade: -55°C to +125°C
  - B Grade: -30°C to +70°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage	-8V
Output current	20mA
Storage temperature range	-55°C to +150°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p

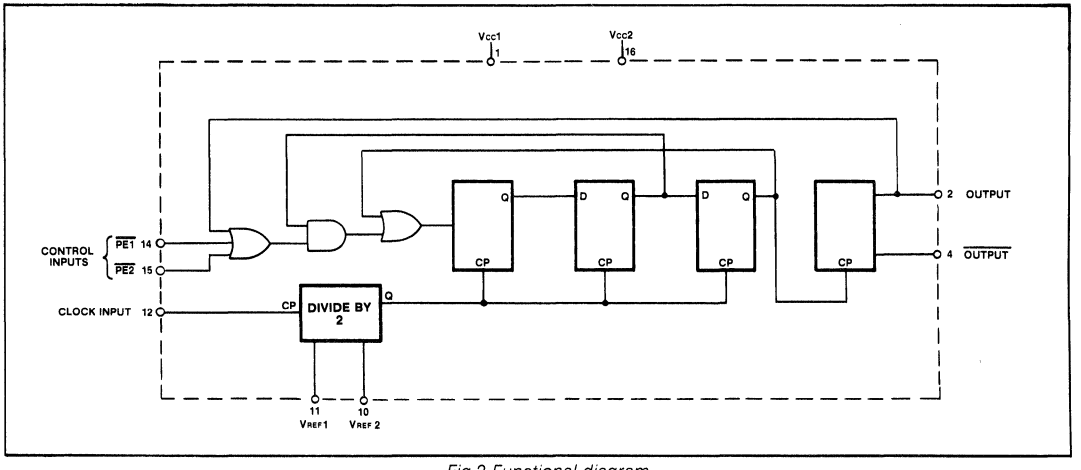


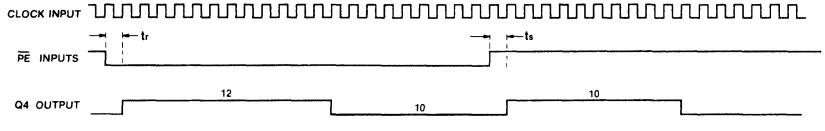
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply Voltage: V_{CC} = 0V V_{EE} = -5.2V ± 0.25V
Temperature: A grade T_{case} = -55°C to +125°C (case temperature)
B grade T_{amb} = -30°C to +70°C

Characteristics	Symbol	Value		Units	Grade	Conditions	Notes
		Min.	Max.				
Maximum toggle frequency sinewave input	f_{max}	1.0		GHz	SP8785	Input = 400-1200mV p-p	Note 4
		1.3		GHz	SP8786	Input = 600-1200mV p-p	Note 4
		1.3		GHz	SP8786	Input = 400-1200mV p-p	Note 4
Minimum toggle frequency sinewave input	f_{min}		150	MHz	All	Input = 400-1200mV p-p	Note 5
Current consumption	I_{EE}		115	mA	All	V_{EE} = -5.2V outputs unloaded	Note 6
Output low voltage	V_{OL}	-1.85	-1.62	V	All	V_{EE} = -5.2V output load = 430Ω	
Output high voltage	V_{OH}	-0.93	-0.78	V	All	V_{EE}=-5.2V(25°C) output load = 430Ω	
Minimum output swing	V_{OUT}	500		mV	All	V_{EE}=-5.2V(25°C) output load = 430Ω	Note 4
Clock to output delay	t_p		4	ns	All	V_{EE} = -5.2V	Note 5
Set up time	t_s	1		ns	All	V_{EE} = -5.2V	Note 5
Release time	t_r	1		ns	All	V_{EE} = -5.2V	Note 5
PE input high voltage	V_{INH}	-0.93		V	All	V_{EE}=-5.2V(25°C)	
PE input low voltage	V_{INL}		-1.62	V	All	V_{EE}=-5.2V(25°C)	

NOTES
1. Unless otherwise stated the electrical characteristics are guaranteed over specified supply, frequency and temperature range.
2. The A grade devices must be used with a heat sink to maintain chip temperature below +175°C when operating at an ambient of +125°C.
3. The temperature coefficient of V_{INL} & V_{INH} = +0.8mV/°C, of V_{OH} = +1.2mV/°C but these are not tested.
4. Tested at low and high temperatures only.
5. Guaranteed but not tested.
6. Tested at 25°C only.

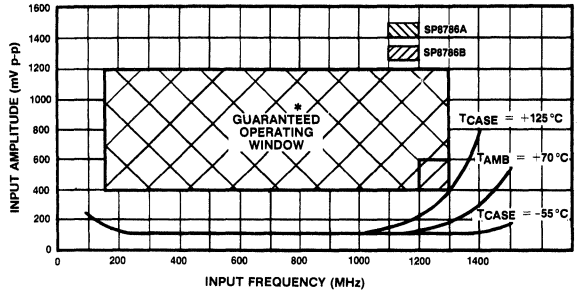


TRUTH TABLE FOR CONTROL INPUTS

$\overline{PE1}$	$\overline{PE2}$	Division Ratio
L	L	22
H	L	20
H	H	20
H	H	20

Fig.3 Timing diagram

NOTES
The set up time t_s is defined as minimum time that can elapse between L→H transition of control input and the next L→H clock pulse transition to ensure ÷20 mode is selected.
The release time t_r is defined as minimum time that can elapse between H→L transition of the control input and the next L→H clock pulse transition to ensure the ÷22 mode is selected.



*Tested as specified in table of Electrical Characteristics

Fig.4 Typical characteristics SP8786

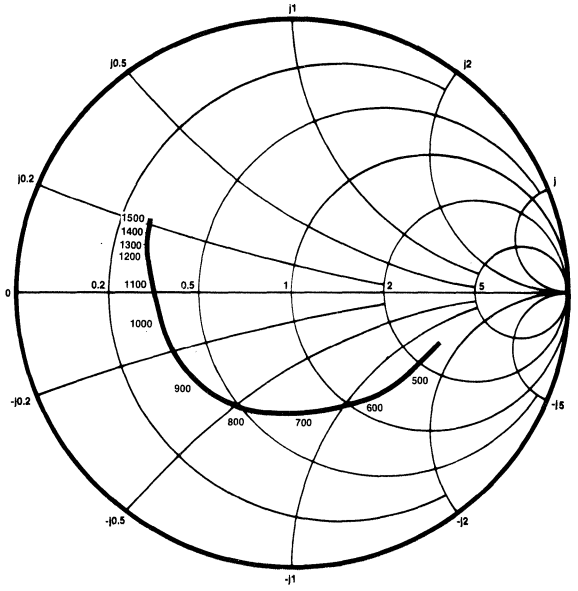


Fig.5 Typical input impedance. Test conditions: supply voltage 5.2V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

OPERATING NOTES

1. The clock input (pin 12) should be capacitively coupled to the signal source. The input signal path is completed by connecting a decoupling capacitor from $V_{REF}1$ (pin 11) to ground. $V_{REF}2$ (pin 10) should also be decoupled with a suitable capacitor, see Figs. 6 and 7.
2. If no signal is present the circuit device will self-oscillate. If this is undesirable it may be prevented by connecting a 10k resistor from the input to V_{EE} (i.e. pin 12 to pin 8).
3. The input can be operated at very low frequencies but slew rate must be better than 200V/µs.
4. The emitter follower outputs require a 430Ω pull-down resistor and are compatible with ECL III/10K. An equal load on an unused output will reduce distortion.
5. The PE inputs are ECL III/10K compatible and include a 4.3k pull-down resistor. Unused inputs can therefore be left open.
6. The input impedance of the SP8785/6 is a function of frequency, see Fig. 5. These impedance variations may give the effect of large variations in sensitivity because of the loading of the source by the device. For best results impedance matching should be used.
7. Note that all components should be suitable for the frequency in use.

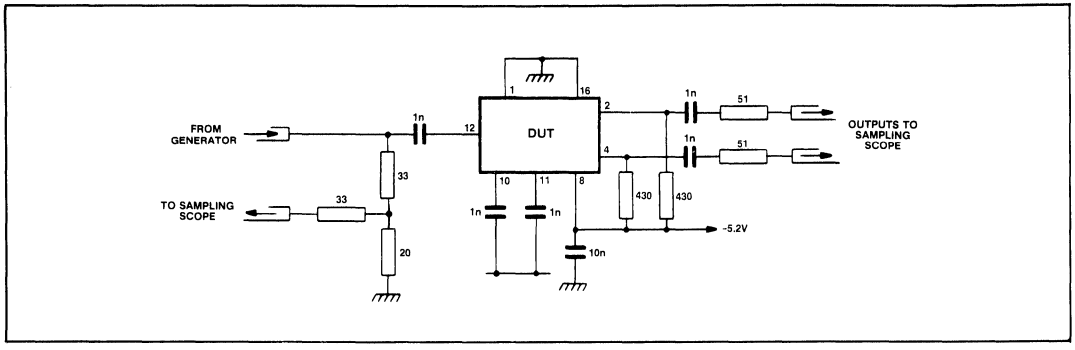


Fig.6 Toggle frequency test circuit

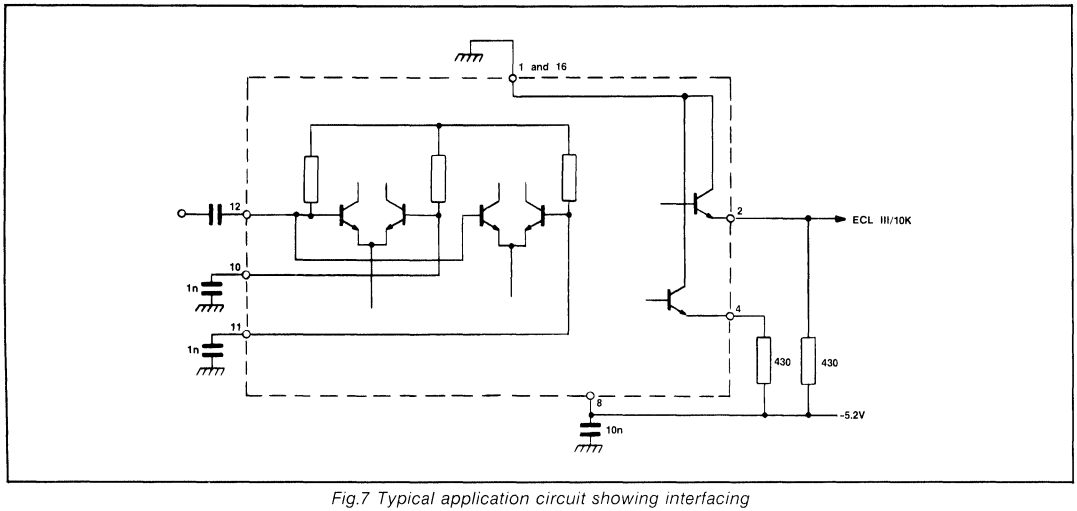


Fig.7 Typical application circuit showing interfacing

PLESSEY
Semiconductors

SP8789

225MHz ÷ 20/21 TWO MODULUS DIVIDER

The SP8789 is a low power programmable ÷20/21 counter.It divides by 20, when the control input is in the high state and by 21 when in the low state. An internal voltage regulator allows operation from a wide range of supply voltages.

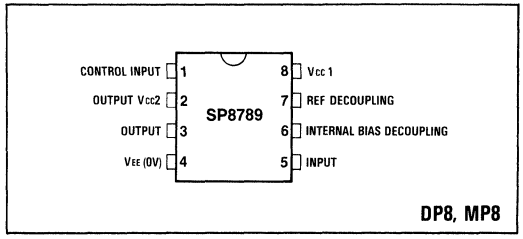


Fig.1 Pin connections - top view

FEATURES

- Very Low Power
- Control Input and Output CMOS/TTL Compatible
- AC Coupled Input
- Operation up to 9.5V using Internal Regulator

QUICK REFERENCE DATA

- Supply voltage: +5.2V or 6.8 to 9.5V
- Power consumption: 26mW Typical
- Temperature range: -40°C to +85°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage	6.0V pins 7 & 8 tied
Supply voltage	13.5V pin 8, pin 7 decoupled
Storage temperature range	-55°C to +125°C
Max. junction temperature	+175°C
Max. clock input voltage	2.5V p-p
$V_{CC}2$	Max. 10V

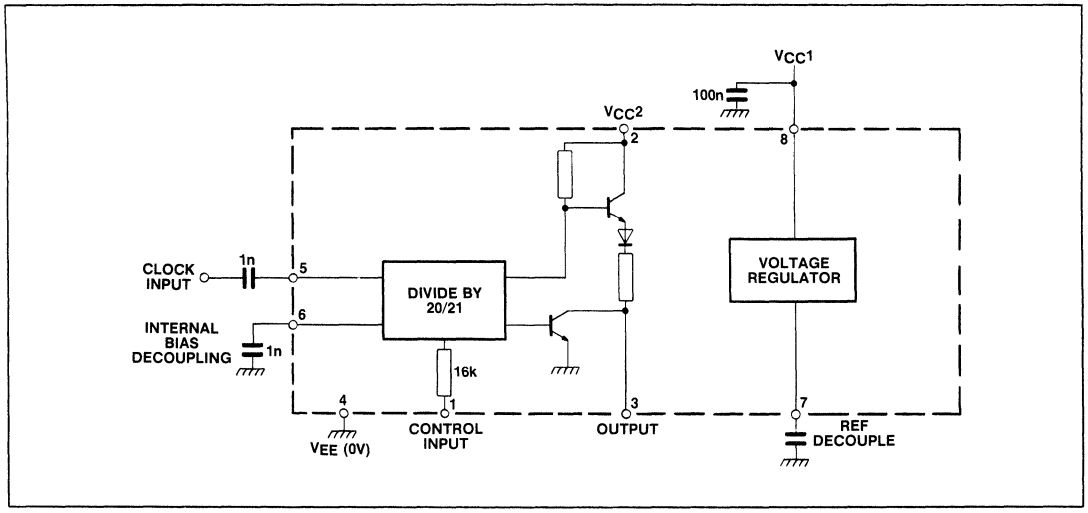


Fig.2 Functional diagram SP8789

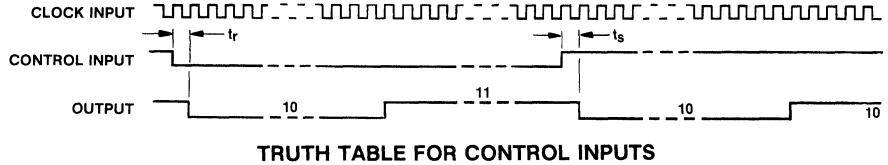
ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Supply voltage: V_{CC} 1 & 2 = 5.2V ± 0.25V or 6.8V to 9.5V (see Operating Note 7);
V_{EE} = 0V; Temperature T_{amb} = -40°C to +85°C

Characteristic	Symbol	Value		Units	Notes	Conditions
		Min.	Max.			
Maximum frequency (sinewave input)	f_{max}	225		MHz	Note 4	Input = 200-800mV p-p
Minimum frequency (sinewave input)	f_{min}		20	MHz	Note 4	Input = 400-800mV p-p
Power supply current	I_{EE}		7	mA	Note 4	
Control input high voltage	V_{INH}	4		V	Note 4	
Control input low voltage	V_{INL}		2	V	Note 4	
Output high voltage	V_{OH}	2.4		V	Note 4	Pins 2, 7 and 8 linked V_{CC} = 4.95V I_{OH} = 100μA
Output low voltage	V_{OL}		0.5	V	Note 4	Pin 2 linked to 8 and 7 I_{OL} = 1.6mA
Set up time	t_s	14		ns	Note 3	25°C
Release time	t_r	20		ns	Note 3	25°C
Clock to output propagation time	t_p		45	ns	Note 3	25°C

NOTES
1. Unless otherwise stated the electrical characteristics are guaranteed over full specified supply, frequency and temperature range.
2. The test configuration for dynamic testing is shown in Fig.6.
3. Guaranteed but not tested.
4. Tested only at 25°C.



TRUTH TABLE FOR CONTROL INPUTS

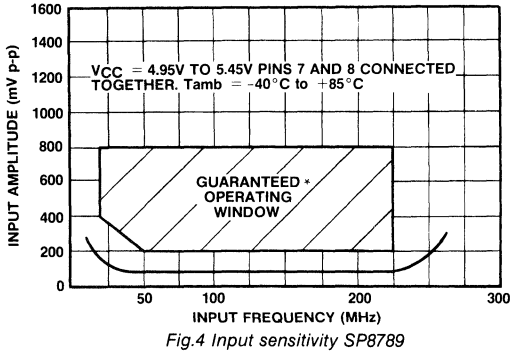
Control input	Division ratio
0	21
1	20

Fig.3 Timing diagram SP8789

NOTES

The set-up time t_s is defined as minimum time that can elapse between L→H transition of control input and next L→H clock pulse transition to ensure ÷20 mode is selected.

The release time t_r is defined as minimum time that can elapse between H→L transition of the control input and the next L→H clock pulse transition to ensure the ÷21 mode is selected.



*Tested as specified in table of Electrical Characteristics

Fig.4 Input sensitivity SP8789

OPERATING NOTES

1. The clock input (Pin 5) should be capacitively coupled to the signal source. The input signal path is completed by coupling a capacitor from the internal bias decoupling, Pin 6 to ground.
2. The output stage which is normally open collector (Pin 2 open circuit) can be interfaced to CMOS. The open collector can be returned to a +10V line via a 5k resistor but the output sink current should not exceed 2mA. If interfacing to TTL is required then Pins 2 and 7 should be connected together to give a fan-out = 1. This will increase supply current by approximately 2mA.
3. The circuit will operate down to DC but a slew rate of better than 20V/μs is required.
4. The mark space ratio of the output is approximately 1.2:1 at 200MHz.
5. Input impedance is a function of frequency. See Fig.5.
6. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 150k between unused input and ground. This reduces the input sensitivity by typically 50-100mV p-p.
7. The internal regulator has its input connected to Pin 8, while the internal reference voltage appears at Pin 7 and should be decoupled. For use from a 5.2V supply, Pins 7 and 8 should be connected together, and 5.2V applied to these pins. For operation from supply voltages in the range +6.8V to +9.5V, Pins 7 and 8 should be separately decoupled, and the supply voltage applied to Pin 8.

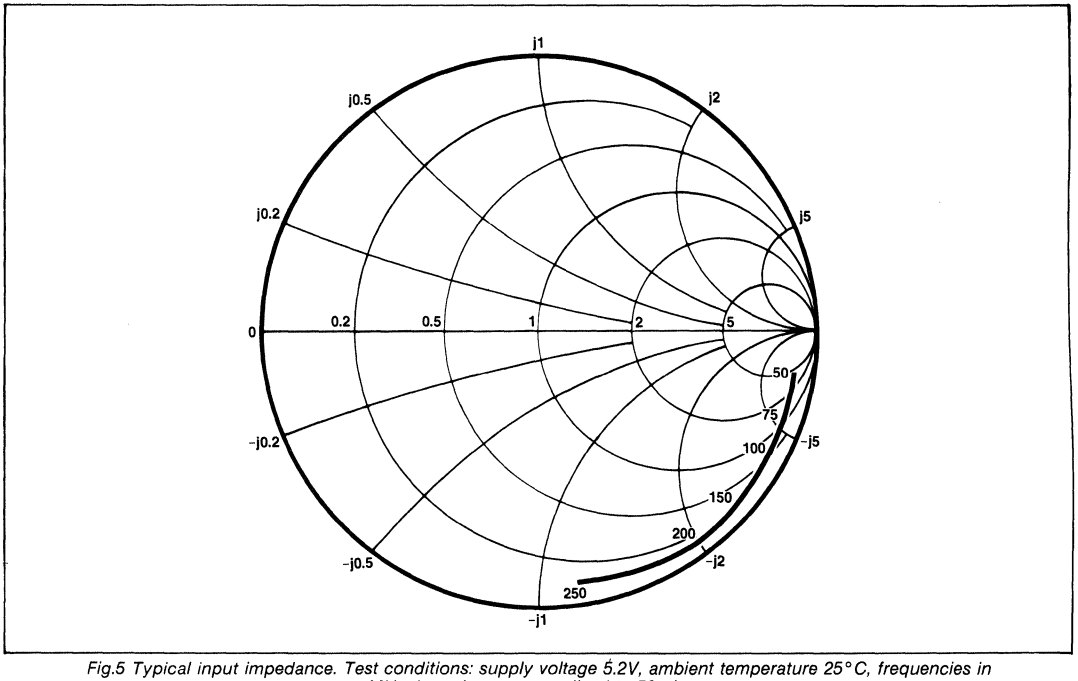


Fig.5 Typical input impedance. Test conditions: supply voltage 5.2V, ambient temperature 25°C, frequencies in MHz, impedances normalised to 50 ohms.

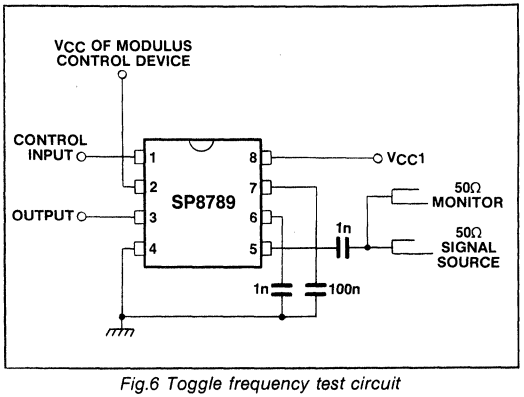


Fig.6 Toggle frequency test circuit

SP8789A

200MHz ÷ 20/21 TWO MODULUS DIVIDER

The SP8789A is a low power programmable ÷20/21 counter which operates over the full Military temperature range. It divides by 20 when the control input is in the high state and by 21 when in the low state.

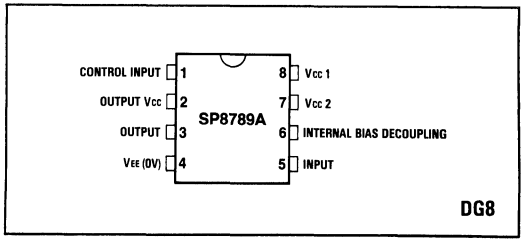


Fig.1 Pin connections - top view

FEATURES

- Very Low Power
- Control Input and Output CMOS/TTL Compatible
- AC Coupled Input

QUICK REFERENCE DATA

- Supply voltage: +5.2V
- Power consumption: 26mW Typical
- Temperature range: -55°C to +125°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage:	6.0V Pins 7 & 8 tied
Storage temperature range:	-55° C to +150° C
Max. junction temperature:	+175° C
Max. clock input voltage:	2.5V p-p

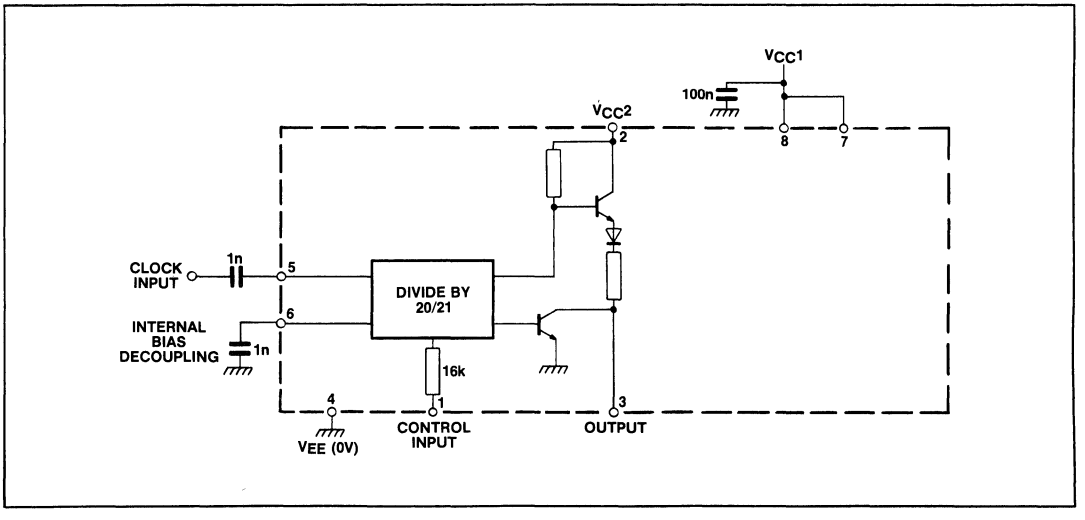


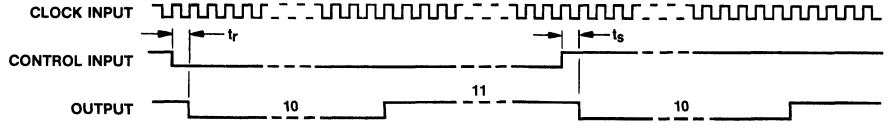
Fig.2 Function diagram SP8789A

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage: V_{CC} 1 & 2 = 5.2V ± 0.25V; V_{EE} = 0V; Temperature T_{amb} = -55°C to +125°C

Characteristic	Symbol	Value		Units	Notes	Conditions
		Min.	Max.			
Maximum frequency	f_{max}	200		MHz		Input = 200-400mV p-p
(sinewave input)		150		MHz	Note 3	Input = 200-800mV p-p
Minimum frequency	f_{min}		20	MHz	Note 3	Input = 400mV p-p
(sinewave input)			50	MHz		Input = 200mV p-p
Power supply current	I_{EE}		7	mA	Note 4	
Control input high voltage	V_{INH}	4	5.2	V	Note 4	
Control input low voltage	V_{INL}		2	V	Note 4	
Output high voltage	V_{OH}	2.4		V	Note 4	Pins 2, 7 and 8 linked V_{CC} = 4.95V I_{OH} = 100μA
Output low voltage	V_{OL}		0.5	V	Note 4	Pin 2 linked to 8 and 7 I_{OL} = 1.6mA
Set up time	t_s	14		ns	Note 3	25°C
Release time	t_r	20		ns	Note 3	25°C
Clock to output propagation time	t_p		45	ns	Note 3	25°C

NOTES
1. Unless otherwise stated the electrical characteristics are guaranteed over full specified supply, frequency and temperature range.
2. The test configuration for dynamic testing is shown in Fig.6.
3. Guaranteed but not tested.
4. Tested at 25°C only.

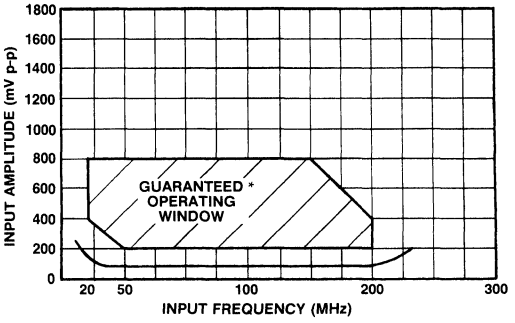


TRUTH TABLE FOR CONTROL INPUTS

Control inputs	Division ratio
0	21
1	20

Fig.3 Timing diagram SP8789A

NOTES
The set-up time t_s is defined as minimum time that can elapse between L→H transition of control input and next L→H clock pulse transition to ensure ÷20 mode is selected.
The release time t_r is defined as minimum time that can elapse between H→L transition of the control input and the next L→H clock pulse transition to ensure the ÷21 mode is selected.



*Tested as specified in table of Electrical Characteristics

Fig.4 Input sensitivity SP8789A

OPERATING NOTES

1. The clock input (Pin 5) should be capacitively coupled to the signal source. The input signal path is completed by coupling a capacitor from the internal bias decoupling, Pin 6 to ground.
2. The output stage which is normally open collector (Pin 2 open circuit) can be interfaced to CMOS. The open collector can be returned to a +10V line via a 5k resistor but the output sink current should not exceed 2mA. If interfacing to TTL is required then Pins 2 and 7 should be connected together to give a fan-out = 1. This will increase supply current by approximately 2mA.
3. The circuit will operate down to DC but a slew rate of better than 20V/μs is required.
4. The mark space ratio of the output is approximately 1.2:1 at 200MHz.
5. Input impedance is a function of frequency. See Fig.5.
6. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 150k between unused input and ground. This reduces the input sensitivity by typically 50-100mV p-p.
7. The supply voltage regulator which allows the SP8789 to be used at supply voltages up to 9.5V is *NOT* available for use in the A Grade device: the SP8789A is *ONLY* available for operation from 5.2V supply, and therefore Pins 7 and 8 should always be externally connected together.

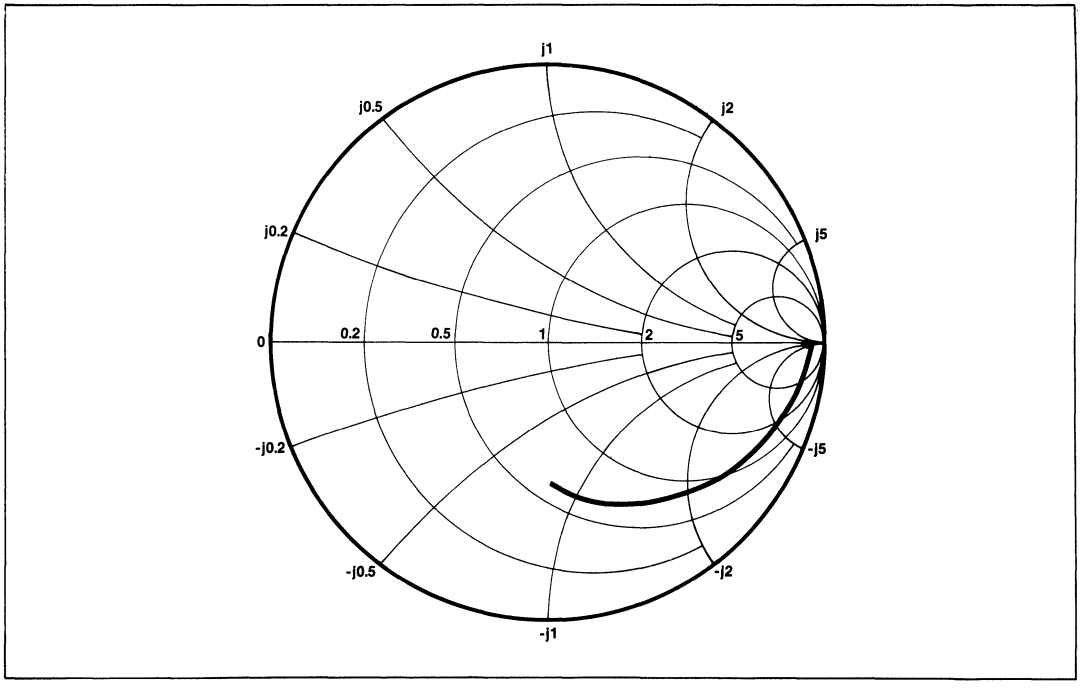


Fig.5 Typical input impedance. Test conditions: supply voltage 5.2V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

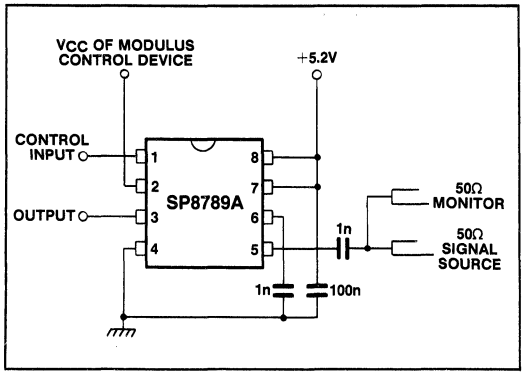


Fig.6 Toggle frequency test circuit

SP8790A&B

60MHz ÷ 4 (2-MODULUS EXTENDER)

The SP8790 is a divide-by-four counter designed for use with 2-modulus counters. It increases the minimum division ratio of the 2-modulus counter while retaining the same difference in division ratio. Suitable for low power frequency synthesis interfacing to CMOS or TTL.

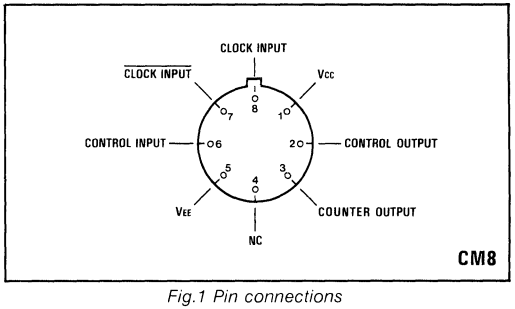


Fig.1 Pin connections

FEATURES

- Very Low Power
- Control Input and Counter Output will Interface Directly to TTL or CMOS
- Interfaces to SP8000 Programmable 2 Modulus Counters

QUICK REFERENCE DATA

- Supply Voltage: 5.0V
- Power Consumption: 40mW
- Temperature Range:
  - A Grade: -55°C to +125°C
  - B Grade: -30°C to +70°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage	8V
Open collector output	12V
Storage temperature range	-55°C to +150°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p
Output sink current	10mA

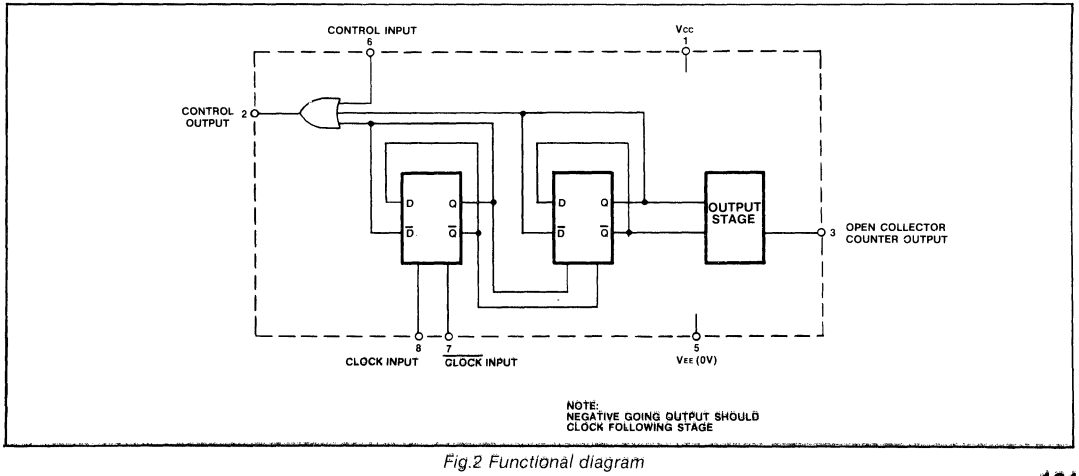


Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply Voltage: V_{CC} = 5V ± 0.25V V_{EE} = 0V
Temperature: A grade: -55°C to +125°C
B grade: -30°C to +70°C

Characteristics	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency sinewave input	f_{max}	60		MHz	Tested as a controller. See Fig.4	Note 3
Power supply current	I_{EE}		11	mA		Note 3
Control input high voltage	V_{INH}	3.5	10	V		Note 3
Control input low voltage	V_{INL}	0	1.5	V		Note 3
Output high voltage (pin 3)	V_{OH}	9		V	Pin 3 via 1.6k to +10V	Note 3
Output low voltage (pin 3)	V_{OL}		0.4	V	Pin 3 via 1.6k to +10V	Note 3
Output high voltage (pin 2)	V_{OH}	4.27	4.5	V	V_{CC} = 5.2V (25°C)	
Output low voltage (pin 2)	V_{OL}	3.28	3.7	V	V_{CC} = 5.2V (25°C)	
Clock to counter output -ve going delay	t_{pHL}		25	ns		Note 4
Clock to counter output +ve going delay	t_{pLH}		40	ns		Note 4
Clock to control output -ve going delay	t_{pLH}		15	ns	10kΩ pull-down on control O/P	Note 4
Clock to control output +ve going delay	t_{pHL}		26	ns	10kΩ pull-down on control O/P	Note 4
Control input to control output -ve going delay	t_{pLH}		12	ns	10kΩ pull-down on control O/P	Note 4
Control input to control output +ve going delay	t_{pHL}		16	ns	10kΩ pull-down on on control O/P	Note 4

NOTES
1. Unless otherwise stated the electrical characteristics are guaranteed over full supply, frequency and temperature range.
2. The test configuration for dynamic testing is shown in Fig.4.
3. Tested at low and high temperatures only.
4. Guaranteed but not tested.

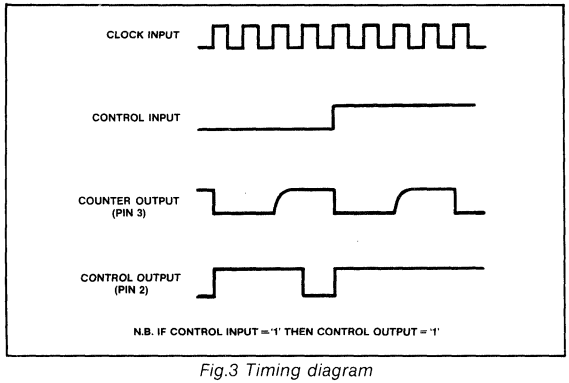


Fig.3 Timing diagram

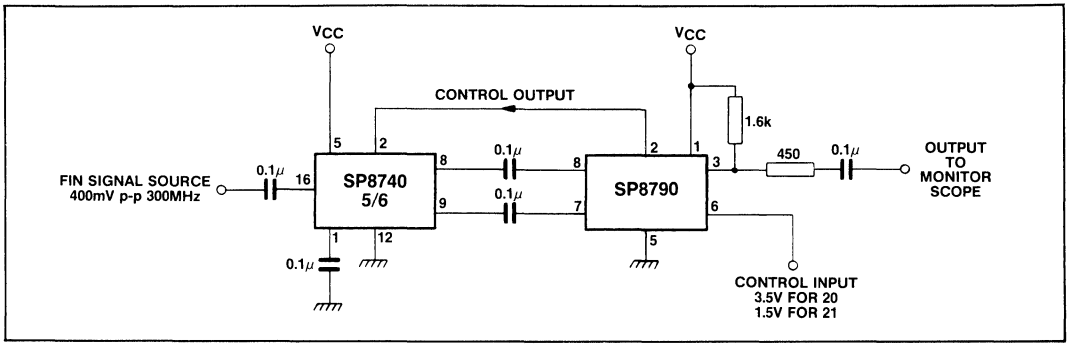


Fig.4 Test circuit

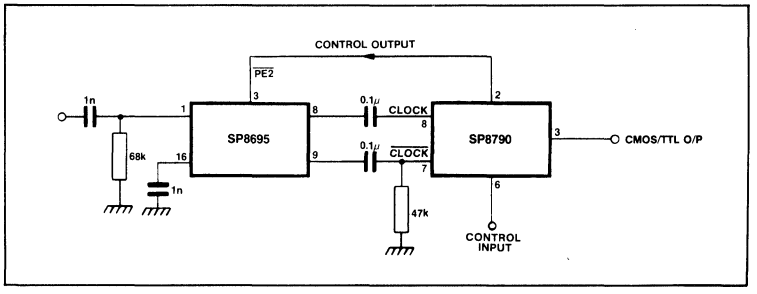


Fig.5 Typical interfacing to suppress self oscillation with no input signal

OPERATING NOTES

1. The device will normally be driven by capacitively coupling the inputs to outputs of a 2-modulus divider. See Figs. 4 and 5. The maximum frequency of the device when used as a controller is limited by the internal delays and will not operate above 60MHz. When used as a prescaler the device will operate in excess of 80MHz, the maximum frequency being limited by saturation of the counter output stage.
2. The device is normally driven from very fast edges of a 2-modulus divider and therefore there is no input slew rate problem.
3. The control input is TTL/CMOS compatible.
4. The counter output (pin 3) interfaces into CMOS/TTL by the addition of a pull-up resistor. For interconnecting to CMOS the output can be connected via a pull-up resistor to supply which should not exceed 12V.
5. When used as a controller the circuit will self-oscillate. This can be prevented by using one of the arrangements as shown in Fig. 5.
6. The control output, which includes an internal 16k pull-down resistor is ECL compatible and interfaced directly into, for example, SP8695. See Fig. 5.
7. The propagation delays stated are with a 10k pull-down resistor which is input pull-down of the SP8695. For interfacing into the SP8643/47 series which have 4.3k pull-downs, the propagation delays will be reduced.

PLESSEY
Semiconductors

SP8792 225MHz ÷ 80/81
SP8793 225MHz ÷ 40/41

WITH ON-CHIP VOLTAGE REGULATOR

The SP8792 and SP8793 are low power programmable ÷80/81 and ÷40/41 counters, temperature range: -40° C to +85° C. They divide by 80(40) when control input is in the high state and by 81(41) when in the low state. An internal voltage regulator allows operation from a wide range of supply voltages.

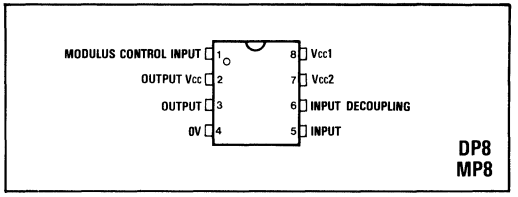


Fig.1 Pin connections - top view

FEATURES

- Very Low Power
- Control Input and Output CMOS/TTL Compatible
- AC Coupled Input
- Operation up to 9.5V using Internal Regulator

QUICK REFERENCE DATA

- Supply Voltage: +5.2V or 6.8V to 9.5V
- Power Consumption: 26mW

ABSOLUTE MAXIMUM RATINGS

Supply voltage	6.0V pins 7 & 8 tied
Supply voltage	13.5V pin 8, pin 7 decoupled
Storage temperature range	-40°C to +85°C
Max. junction temperature	+175°C
Max. clock input voltage	2.5V p-p
Vcc2 max	10V

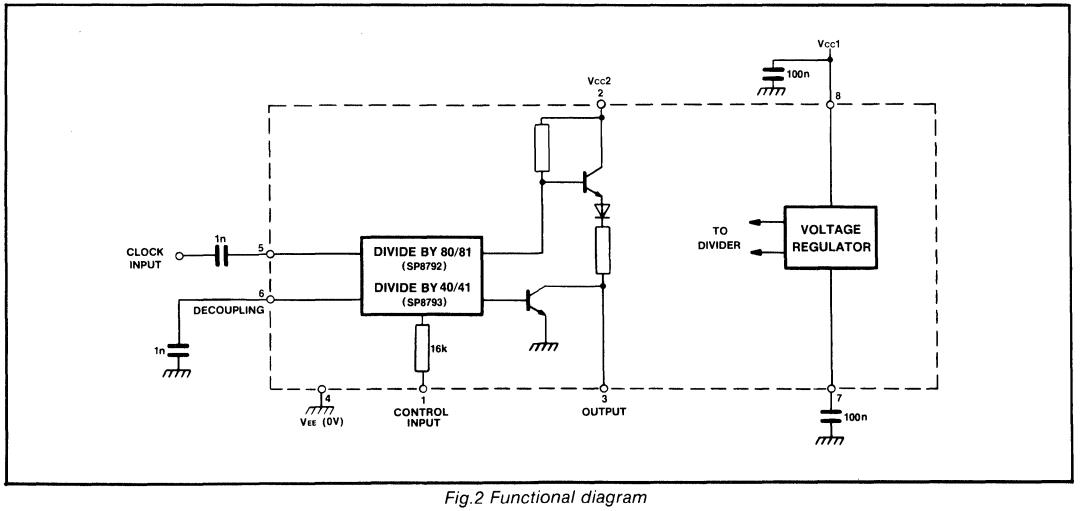


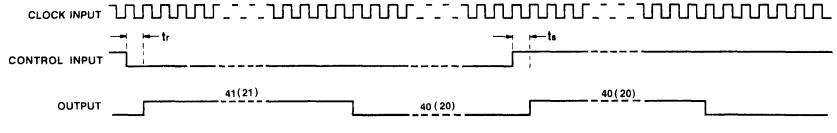
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply Voltage: V_{CC} = 5.2V ± 0.25V or 6.8-9.5V (See Operating Note 6) V_{EE} = 0V
Temperature: T_{amb} = -40°C to +85°C

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{max}	225		MHz	Input = 200-800mV p-p	Note 4
Minimum frequency (sinewave input)	f_{min}		20	MHz	Input = 400mV p-p	Note 4
Power supply current	I_{EE}		7	mA		Note 4
Control input high voltage	V_{INH}	4		V		Note 4
Control input low voltage	V_{INL}		2	V		Note 4
Output high voltage	V_{OH}	2.4		V	Pins 2,7 and 8 linked V_{CC} = 4.95V I_{OH} = 100µA	Note 4
Output low voltage	V_{OL}		0.5	V	Pin 2 open or linked to 8 and 7 I_{OL} = 1.6mA	Note 4
Set up time	t_s	14		ns	25°C	Note 3
Release time	t_r	20		ns	25°C	Note 3
Clock to output propagation time	t_p		45	ns	25°C	Note 3

NOTES
1. Unless otherwise stated the electrical characteristics are guaranteed over full specified supply, frequency and temperature range.
2. The test configuration for dynamic testing is shown in Fig.6.
3. Guaranteed but not tested.
4. Tested at 25°C only.

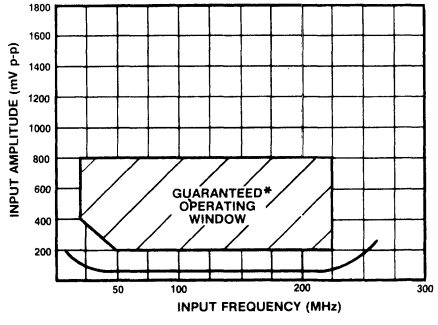


TRUTH TABLE FOR CONTROL INPUTS

Control Inputs	Division Ratio	
	SP8792	SP8793
0	81	41
1	80	40

Fig.3 Timing diagram SP8792/3

NOTES
The set-up time t_s is defined as minimum time that can elapse between L→H transition of control input and the next L→H clock pulse transition to ensure ÷80 or 40 mode is selected.
The release time t_r is defined as minimum time that can elapse between H→L transition of the control input and the next L→H clock pulse transition to ensure the ÷81 or 41 mode is selected.



*Tested as specified in table of Electrical Characteristics

Fig.4 Input sensitivity SP8792/SP8793

OPERATING NOTES

1. The clock input (pin 5) should be capacitively coupled to the signal source. The input signal path is completed by coupling a capacitor from the internal bias decoupling, pin 6, to ground.
2. The output stage which is normally open collector (pin 2 open circuit) can be interfaced to CMOS. The open collector can be returned to a +10V line via a 5k resistor but the output sink current should not exceed 2mA. If interfacing to TTL is required then pins 2 and 7 should be connected together to give a fan-out = 1. This will increase supply current by approximately 2mA.
3. The circuit will operate down to DC but a slew rate of better than 20V/µs is required.
4. The mark space ratio of output is approximately 1.2:1 at 200MHz.
5. Input impedance is a function of frequency. See Fig. 5.
6. The internal regulator has its input connected to pin 8, while the internal reference voltage appears at pin 7 and should be decoupled. For use from a 5.2V supply, pins 7 and 8 should be connected together, and 5.2V applied to these pins. For operation from supply voltages in the range +6.8V to +9.5V, pins 7 and 8 should be separately decoupled, and the supply voltage applied to pin 8.
7. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 150k between unused input and ground. This reduces the input sensitivity by typically 50-100mV p-p.

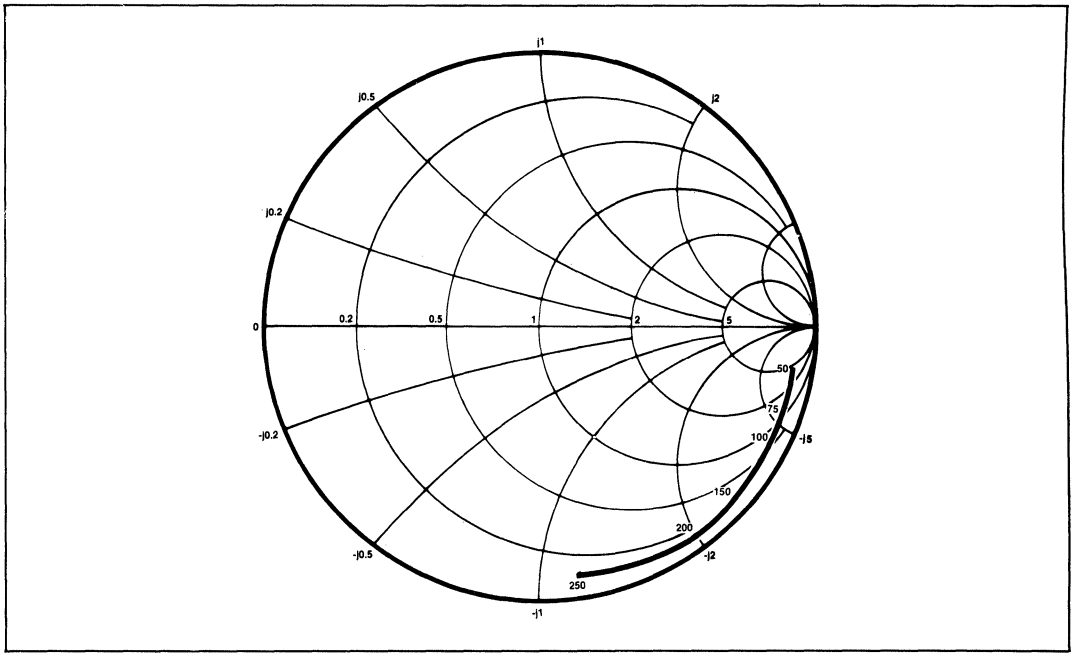


Fig.5 Typical input impedance. Test conditions: supply voltage 5.2V, ambient temperature 25°C, frequencies in MHz, impedances normalised to 50 ohms.

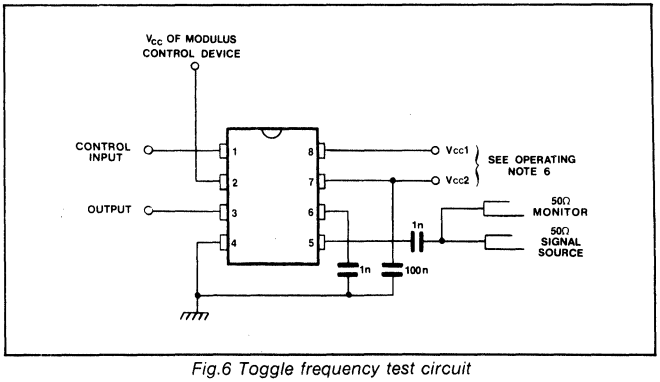


Fig.6 Toggle frequency test circuit

SP8792A 200MHz ÷ 80/81
SP8793A 200MHz ÷ 40/41

The SP8792A and SP8793A are low power programmable +80/81 and +40/41 counters which operate over the full Military temperature range. They divide by 80(40) when the control input is in the high state and by 81(41) when in the low state.

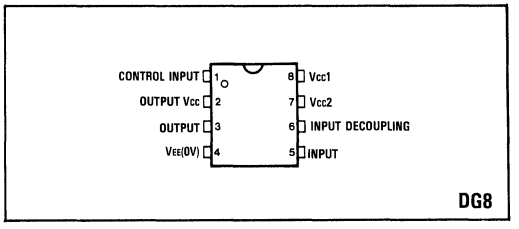


Fig.1 Pin connections - top view

FEATURES

- Very Low Power
- Control Input and Output CMOS/TTL Compatible
- AC Coupled Input

QUICK REFERENCE DATA

- Supply Voltage: +5.2V
- Power Consumption: 26mW typical
- Temperature Range: -55°C to +125°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage	6V pins 7 & 8 linked
Storage temperature range	-55°C to +150°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p

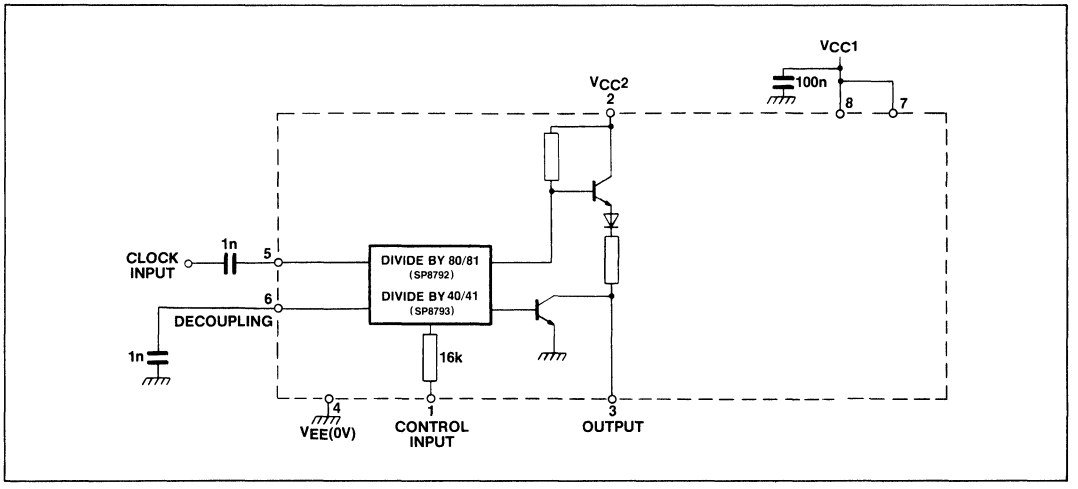


Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply Voltage: V_{CC} = 5.2V ± 0.25V V_{EE} = 0V
Temperature: T_{amb} = -55°C to +125°C

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{max}	200		MHz	Input =200 - 400mV p-p	
		150		MHz	Input =200 - 800mV p-p	Note 3
Minimum frequency (sinewave input)	f_{min}		20	MHz	Input =400mV p-p	
Power supply current	I_{EE}		7	mA		Note 4
Control input high voltage	V_{INH}	4		V		Note 4
Control input low voltage	V_{INL}		2	V		Note 4
Output high voltage	V_{OH}	2.4		V	Pins 2,7 and 8 linked V_{CC}= 4.95V I_{OH}= -100μA	Note 4
Output low voltage	V_{OL}		0.5	V	Pin 2 linked to 8 and 7 I_{OL} = 1.6mA	Note 4
Set-up time	t_s	14		ns	25° C	Note 3
Release time	t_r	20		ns	25° C	Note 3
Clock to output propagation time	t_p		45	ns	25° C	Note 3

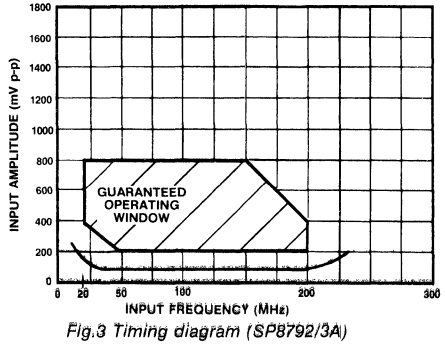
NOTES
1. Unless otherwise stated the electrical characteristics are guaranteed over full specified supply, frequency and temperature range.
2. The test configuration for dynamic testing is shown in Fig.6.
3. Guaranteed but not tested.
4. Tested at 25°C only.

TRUTH TABLE FOR CONTROL INPUTS

Control Inputs	Division Ratio	
	SP8792A	SP8793A
0	81	41
1	80	40

Fig.4 Input sensitivity (SP8792/3A)

NOTE
The set-up time t_s is defined as the minimum time that can elapse between a L → H transition of the control input and the next L→H clock pulse transition to ensure that the ÷80(40) mode is selected.
The release time t_r is defined as the minimum time that can elapse between a H→L transition of the control input and the next L→H clock pulse transition to ensure that the ÷81(41) mode is selected.



*Tested as specified in table of Electrical Characteristics

Fig.3 Timing diagram (SP8792/3A)

OPERATING NOTES

1. The clock input (pin 5) should be capacitively coupled to the signal source. The input signal path is completed by coupling a capacitor from the internal bias decoupling, pin 6 to ground.
2. The output stage which is normally open collector (pin 2 open circuit) can be interfaced to CMOS. The open collector can be returned to a +10V line via a 5k or greater resistor but the output sink current should not exceed 2mA. If interfacing to TTL is required then pin 2, 7, and 8 should be connected together to give a fan-out = 1. Alternatively, the open collector output may be used with a pull-up resistor.
3. The circuit will operate down to DC but a slew rate of better than 20V/μs is required.
4. The mark space ratio of the output is 1.2:1 at 200MHz.
5. Input impedance is a function of frequency. See Fig.5.
6. If no signal is present the circuit will self-oscillate. If this is undesirable it may be prevented by connecting a 150k between unused input and ground. This reduces the input sensitivity by typically 50-100mV p-p.
7. The supply voltage regulator which allows the SP8792/3 to be used at supply voltages up to 9.5V is NOT available for use in the A Grade device: the SP8792A and SP8793A are ONLY available for operation from 5.2V supply, and therefore pins 7 and 8 should always be externally connected together.

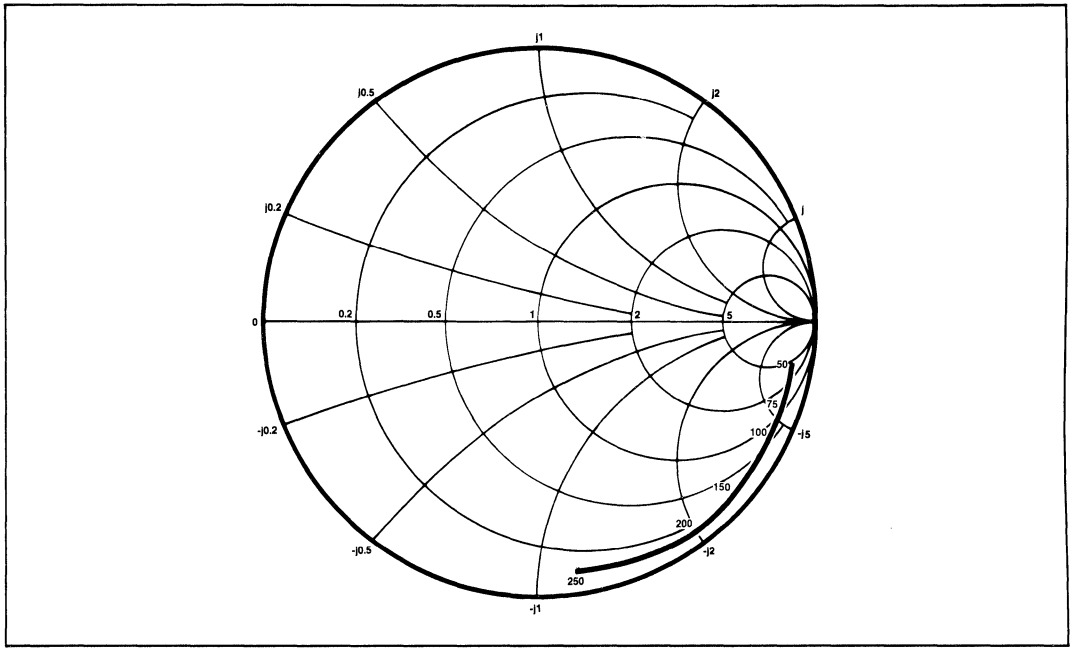


Fig.5 Typical input impedance. Test conditions: supply voltage 5.2V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

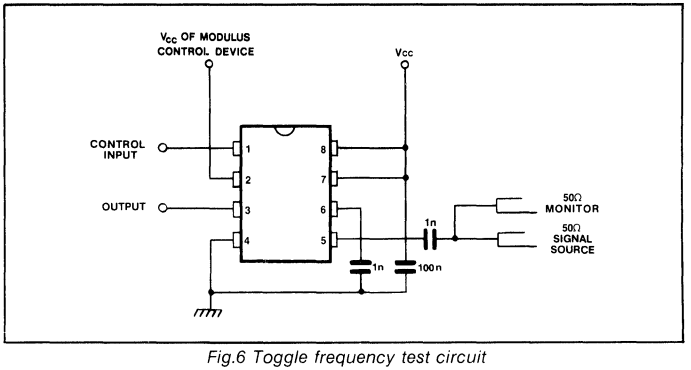


Fig.6 Toggle frequency test circuit

SP8794A&B

60MHz ÷ 8 (2-MODULUS EXTENDER)

The SP8794 is a divide-by-eight counter designed for use with 2-modulus counters. It increases the minimum division ratio of the 2-modulus counter while retaining the same difference in division ratio. Suitable for low power frequency synthesis interfacing to CMOS or TTL.

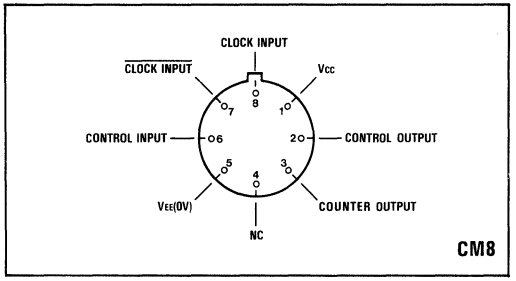


Fig.1 Pin connections - top view

FEATURES

- Very Low Power
- Control Input and Counter Output will Interface Directly to TTL or CMOS
- Interfaces to SP8000 Programmable 2-Modulus Counters

QUICK REFERENCE DATA

- Supply Voltage: 5.0V
- Power Consumption: 40mW
- Temperature Range:
  - A Grade: -55°C to +125°C
  - B Grade: -30°C to +70°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage	8V
Output collector output	12V
Storage temperature range	-55°C to +150°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p
Output sink current	10mA

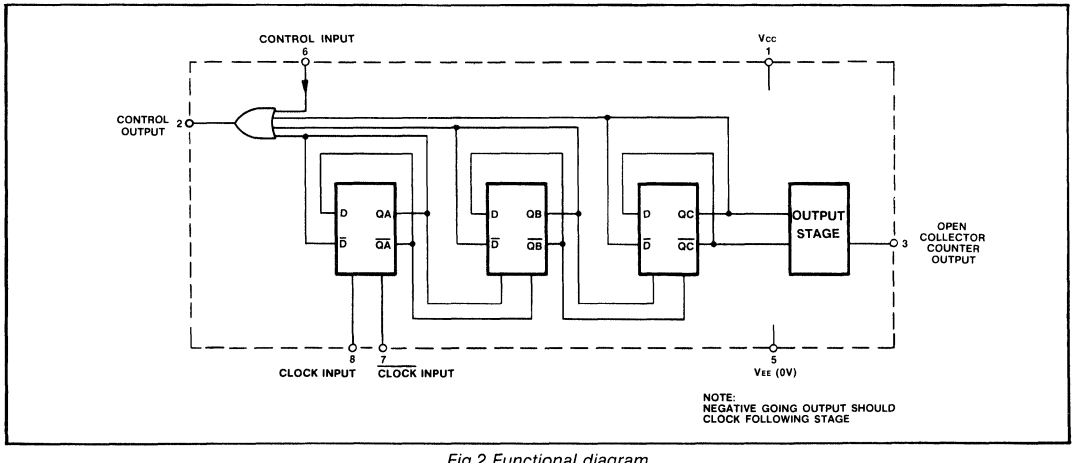


Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply Voltage: V_{CC} = 5V ± 0.25V V_{EE} = 0V
Temperature: A grade: -55°C to +125°C
B grade: -30°C to +70°C

Characteristics	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency sinewave input	f_{max}	60		MHz	Tested as a controller. See Fig. 4	Note 3
Power supply current	I_{EE}		11	mA		Note 3
Control input high voltage	V_{INH}	3.5	10	V		Note 3
Control input low voltage	V_{INL}	0	1.5	V		Note 3
Output high voltage (pin 3)	V_{OH}	9		V	Pin 3 via 1.6k to +10V	Note 3
Output low voltage (pin 3)	V_{OL}		0.4	V	Pin 3 via 1.6k to +10V	Note 3
Output high voltage (pin 2)	V_{OH}	4.27	4.5	V	V_{CC} = 5.2V(25° C)	
Output low voltage (pin 2)	V_{OL}	3.28	3.7	V	V_{CC} = 5.2V(25° C)	
Clock to counter output -ve going delay	t_{pHL}		27	ns		Note 4
Clock to counter output +ve going delay	t_{pLH}		48	ns		Note 4
Clock to control output -ve going delay	t_{pLH}		15	ns	10k pull-down on control O/P	Note 4
Clock to control output +ve going delay	t_{pHL}		26	ns	10k pull-down on control O/P	Note 4
Control input to control output -ve going delay	t_{pLH}		12	ns	10k pull-down on control O/P	Note 4
Control input to control output +ve going delay	t_{pHL}		16	ns	10k pull-down on on control O/P	Note 4

NOTES
1. Unless otherwise stated the electrical characteristics are guaranteed over full supply, frequency and temperature range.
2. The test configuration for dynamic testing is shown in Fig.4.
3. Tested at low and high temperatures only.
4. Guaranteed but not tested.

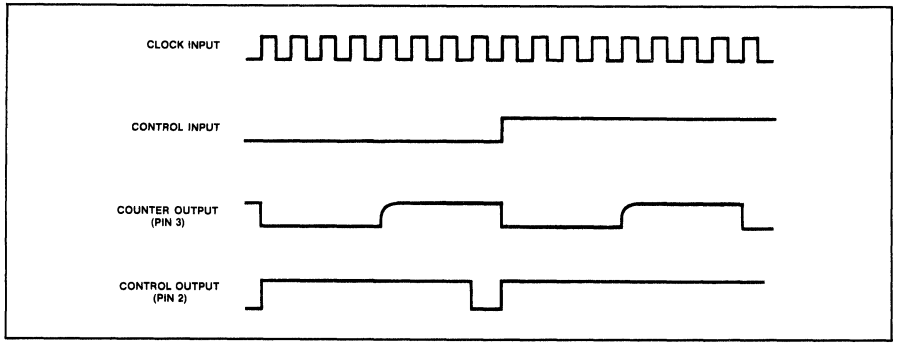


Fig.3 Timing diagram for SP8794

OPERATING NOTES

1. The device will normally be driven by capacitively coupling the clock inputs to the outputs of a 2-modulus divider. See Figs. 4 and 5. The maximum frequency of the device when used as a controller is limited by the internal delays and will not operate above 60MHz. When used as a prescaler the device will operate in excess of 120MHz, the maximum frequency being limited by saturation of the counter output stage.
2. The device is normally driven from the very fast edges of a 2-modulus divider and therefore there is no input slew rate problem.
3. The control input (pin 6) is TTL/CMOS compatible.
4. The counter output (pin 3) interfaces with CMOS/TTL by the addition of a pull-up resistor. For interconnecting to CMOS the output can be connected via a pull-up resistor to a supply which should not exceed 12V.
5. When used as a controller the circuit will self-oscillate in the absence of an input signal. This can be prevented by connecting a 47k resistor from pin 7 to ground, as shown in Fig. 5.
6. The control output which includes an internal 16k pull-down resistor, is ECL compatible and interfaced directly with, for example, the SP8695. See Fig. 5.
7. The propagation delays stated are with a 10k pull-down resistor which is the input pull-down of the SP8695. For interfacing with the SP8643/47 series, which have 4.3k input pull-downs, the propagation delays will be reduced.

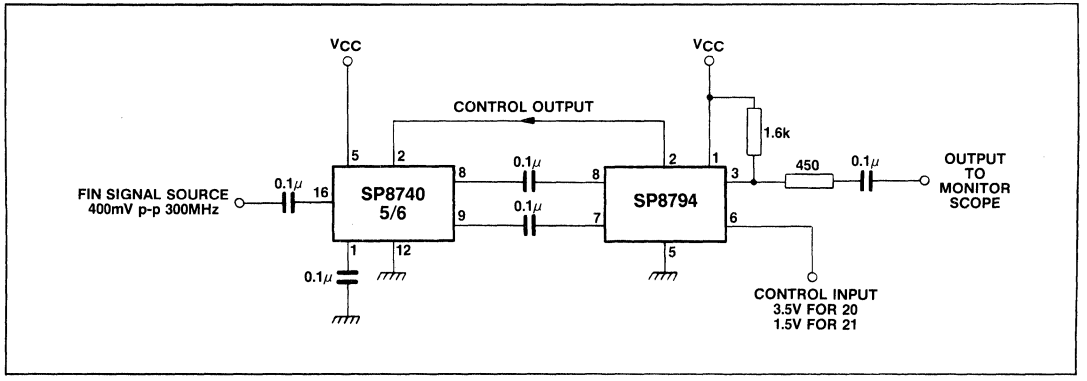


Fig.4 Test circuit

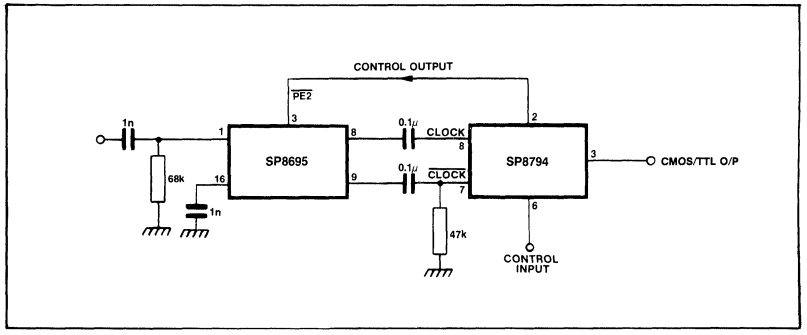


Fig.5 Typical interfacing to suppress self oscillation with no input signal

SP8795

225MHz ÷ 32/33 TWO MODULUS DIVIDER

The SP8795 is a low power programmable ÷32/33 counter.It divides by 32 when the control input is in the high state and by 33 when in the low state. An internal voltage regulator allows operation from a wide range of supply voltages.

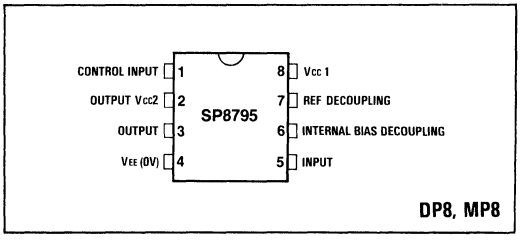


Fig.1 Pin connections - top view

FEATURES

- Very Low Power
- Control Input and Output CMOS/TTL Compatible
- AC Coupled Input
- Operation up to 9.5V using Internal Regulator

QUICK REFERENCE DATA

- Supply voltage: +5.2V or 6.8 to 9.5V
- Power consumption: 26mW Typical
- Temperature range: -40°C to +85°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage	6.0V Pins 7 & 8 tied
	13.5V Pin 8, Pin 7 decoupled
Storage temperature range	-55°C to +125°C
Max. junction temperature	+175°C
Max. clock input voltage	2.5V p-p
Vcc2	Max. 10V

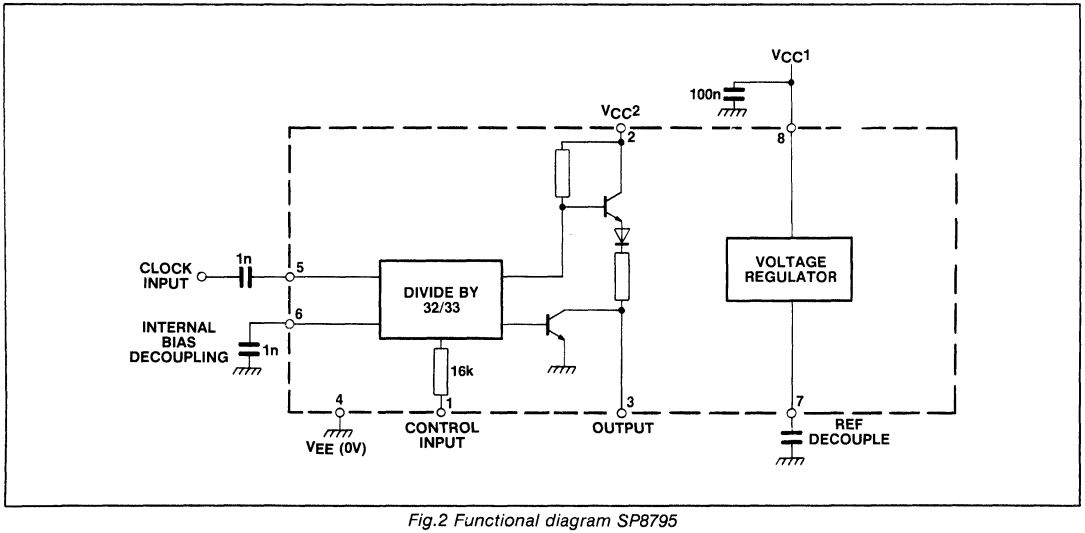


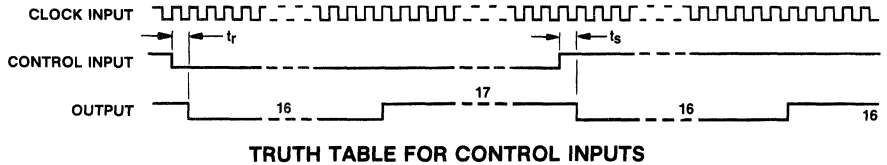
Fig.2 Functional diagram SP8795

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage: V_{CC} 1 & 2 = 5.2V ± 0.25V or 6.8V to 9.5V (see Operating Note 7);
V_{EE} = 0V; Temperature T_{amb} = -40°C to +85°C

Characteristic	Symbol	Value		Units	Notes	Conditions
		Min.	Max.			
Maximum frequency (sinewave input)	f_{max}	225		MHz	Note 4	Input = 200-800mV p-p
Minimum frequency (sinewave input)	f_{min}		20	MHz	Note 4	Input = 400-800mV p-p
Power supply current	I_{EE}		7	mA	Note 4	
Control input high voltage	V_{INH}	4		V	Note 4	
Control input low voltage	V_{INL}		2	V	Note 4	
Output high voltage	V_{OH}	2.4		V	Note 4	Pins 2, 7 and 8 linked V_{CC} = 4.95V I_{OH} = 100μA
Output low voltage	V_{OL}		0.5	V	Note 4	Pin 2 linked to 8 and 7 I_{OL} = 1.6mA
Set up time	t_s	14		ns	Note 3	25°C
Release time	t_r	20		ns	Note 3	25°C
Clock to output propagation time	t_p		45	ns	Note 3	25°C

NOTES
1. Unless otherwise stated the electrical characteristics are guaranteed over full specified supply, frequency and temperature range.
2. The test configuration for dynamic testing is shown in Fig.6.
3. Guaranteed but not tested.
4. Tested only at 25°C.

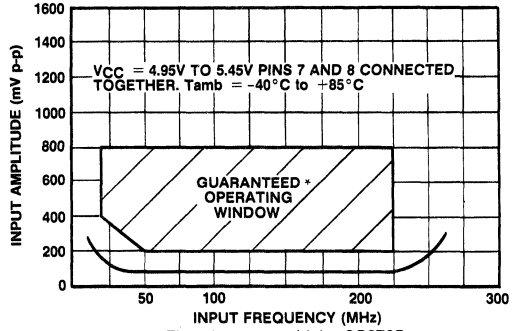


TRUTH TABLE FOR CONTROL INPUTS

Control input	Division ratio
0	33
1	32

Fig.3 Timing diagram SP8795

NOTES
The set-up time t_s is defined as minimum time that can elapse between L→H transition of control input and next L→H clock pulse transition to ensure ÷32 mode is selected.
The release time t_r is defined as minimum time that can elapse between H→L transition of the control input and the next L→H clock pulse transition to ensure the ÷33 mode is selected.



*Tested as specified in table of Electrical Characteristics

Fig.4 Input sensitivity SP8795

OPERATING NOTES

1. The clock input (Pin 5) should be capacitively coupled to the signal source. The input signal path is completed by coupling a capacitor from the internal bias decoupling, Pin 6 to ground.
2. The output stage which is normally open collector (Pin 2 open circuit) can be interfaced to CMOS. The open collector can be returned to a +10V line via a 5k resistor but the output sink current should not exceed 2mA. If interfacing to TTL is required then Pins 2 and 7 should be connected together to give a fan-out = 1. This will increase supply current by approximately 2mA.
3. The circuit will operate down to DC but a slew rate of better than 20V/μs is required.
4. The mark space ratio of the output is approximately 1.2:1 at 200MHz.
5. Input impedance is a function of frequency. See Fig.5.
6. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 150k between unused input and ground. This reduces the input sensitivity by typically 50-100mV p-p.
7. The internal regulator has its input connected to Pin 8, while the internal reference voltage appears at Pin 7 and should be decoupled. For use from a 5.2V supply, Pins 7 and 8 should be connected together, and 5.2V applied to these pins. For operation from supply voltages in the range +6.8V to +9.5V, Pins 7 and 8 should be separately decoupled, and the supply voltage applied to Pin 8.

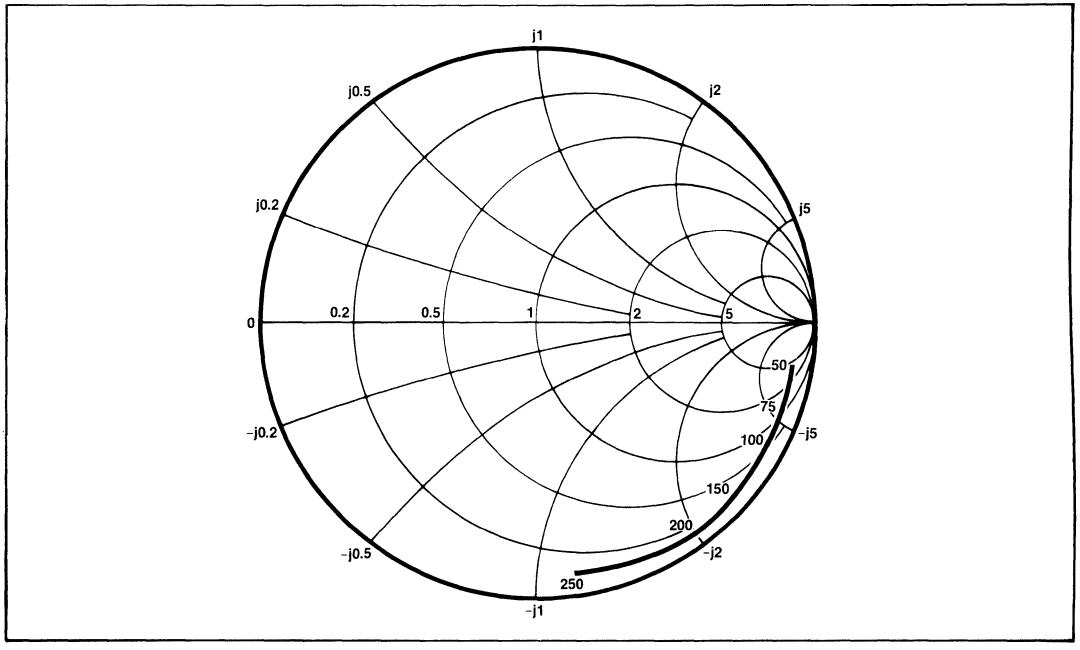


Fig.5 Typical input impedance. Test conditions: supply voltage 5.2V, ambient temperature 25°C, frequencies in MHz, impedances normalised to 50 ohms.

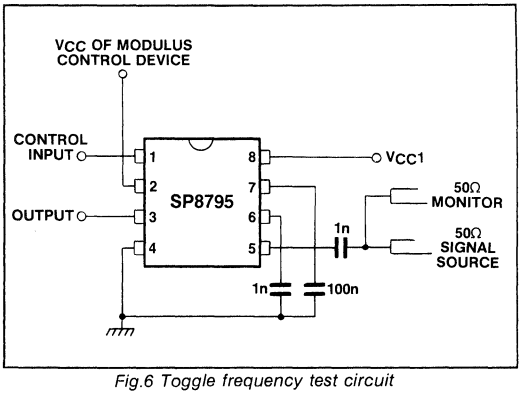


Fig.6 Toggle frequency test circuit

SP8795A

200MHz ÷ 32/33 TWO MODULUS DIVIDER

The SP8795A is a low power programmable ÷32/33 counter which operates over the full Military temperature range. It divides by 32 when the control input is in the high state and by 33 when in the low state.

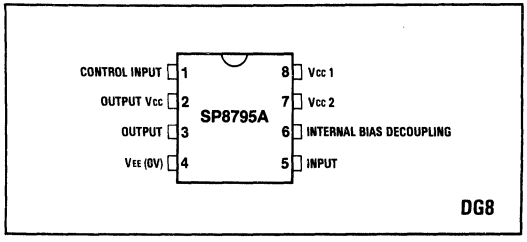


Fig.1 Pin connections - top view

FEATURES

- Very Low Power
- Control Input and Output CMOS/TTL Compatible
- AC Coupled Input

QUICK REFERENCE DATA

- Supply voltage: +5.2V
- Power consumption: 26mW typical
- Temperature range: -55°C to +125°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage:	6.0V Pins 7 & 8 tied
Storage temperature range:	-55°C to +150°C
Max. junction temperature:	+175°C
Max. clock input voltage:	2.5V p-p

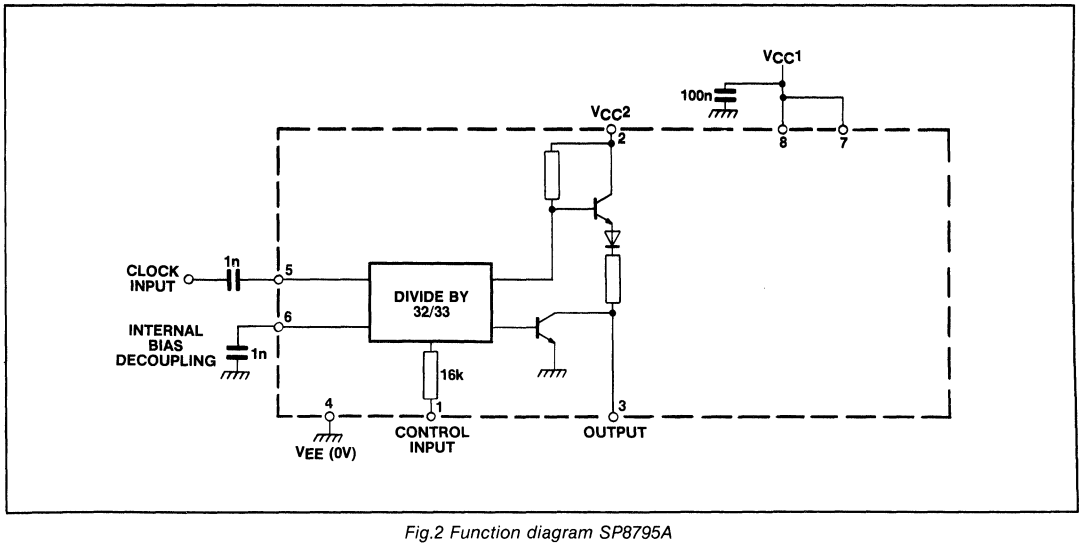


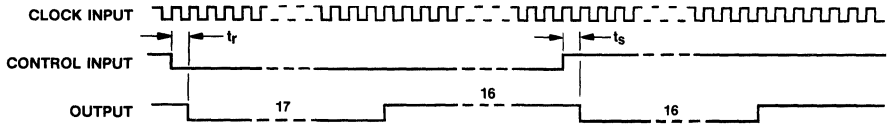
Fig.2 Function diagram SP8795A

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage: V_{CC} 1 & 2 = 5.2V ± 0.25V; V_{EE} = 0V; Temperature T_{amb} = -55°C to +125°C

Characteristic	Symbol	Value		Units	Notes	Conditions
		Min.	Max.			
Maximum frequency	f_{max}	200		MHz		Input = 200-400mV p-p
(sinewave input)		150		MHz	Note 3	Input = 200-800mV p-p
Minimum frequency	f_{min}		20	MHz	Note 3	Input = 400mV p-p
(sinewave input)			50	MHz		Input = 200mV p-p
Power supply current	I_{EE}		7	mA	Note 4	
Control input high voltage	V_{INH}	4	5.2	V	Note 4	
Control input low voltage	V_{INL}		2	V	Note 4	
Output high voltage	V_{OH}	2.4		V	Note 4	Pins 2, 7 and 8 linked V_{CC} = 4.95V I_{OH} = 100μA
Output low voltage	V_{OL}		0.5	V	Note 4	Pin 2 linked to 8 and 7 I_{OL} = 1.6mA
Set up time	t_s	14		ns	Note 3	25°C
Release time	t_r	20		ns	Note 3	25°C
Clock to output propagation time	t_p		45	ns	Note 3	25°C

NOTES
1. Unless otherwise stated the electrical characteristics are guaranteed over full specified supply, frequency and temperature range.
2. The test configuration for dynamic testing is shown in Fig.6.
3. Guaranteed but not tested.
4. Tested at 25°C only.

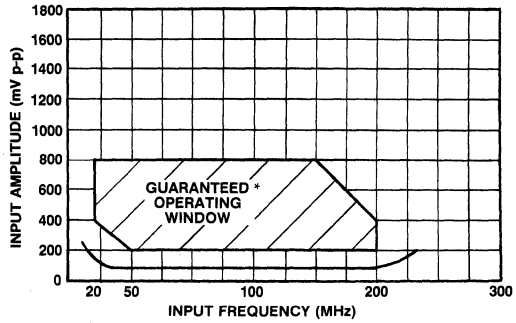


TRUTH TABLE FOR CONTROL INPUTS

Control inputs	Division ratio
0	33
1	32

Fig.3 Timing diagram SP8795A

NOTES
The set-up time t_s is defined as minimum time that can elapse between L→H transition of control input and next L→H clock pulse transition to ensure ÷32 mode is selected.
The release time t_r is defined as minimum time that can elapse between H→L transition of the control input and the next L→H clock pulse transition to ensure the ÷33 mode is selected.



*Tested as specified in table of Electrical Characteristics

Fig.4 Input sensitivity SP8795A

OPERATING NOTES

1. The clock input (Pin 5) should be capacitively coupled to the signal source. The input signal path is completed by coupling a capacitor from the internal bias decoupling, Pin 6 to ground.
2. The output stage which is normally open collector (Pin 2 open circuit) can be interfaced to CMOS. The open collector can be returned to a +10V line via a 5k resistor but the output sink current should not exceed 2mA. If interfacing to TTL is required then Pins 2 and 7 should be connected together to give a fan-out = 1. This will increase supply current by approximately 2mA.
3. The circuit will operate down to DC but a slew rate of better than 20V/μs is required.
4. The mark space ratio of the output is approximately 1.2:1 at 200MHz.
5. Input impedance is a function of frequency. See Fig.5.
6. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 150k between unused input and ground. This reduces the input sensitivity by typically 50-100mV p-p.
7. The supply voltage regulator which allows the SP8795 to be used at supply voltages up to 9.5V is *NOT* available for use in the A Grade device: the SP8795A is *ONLY* available for operation from 5.2V supply, and therefore Pins 7 and 8 should always be externally connected together.

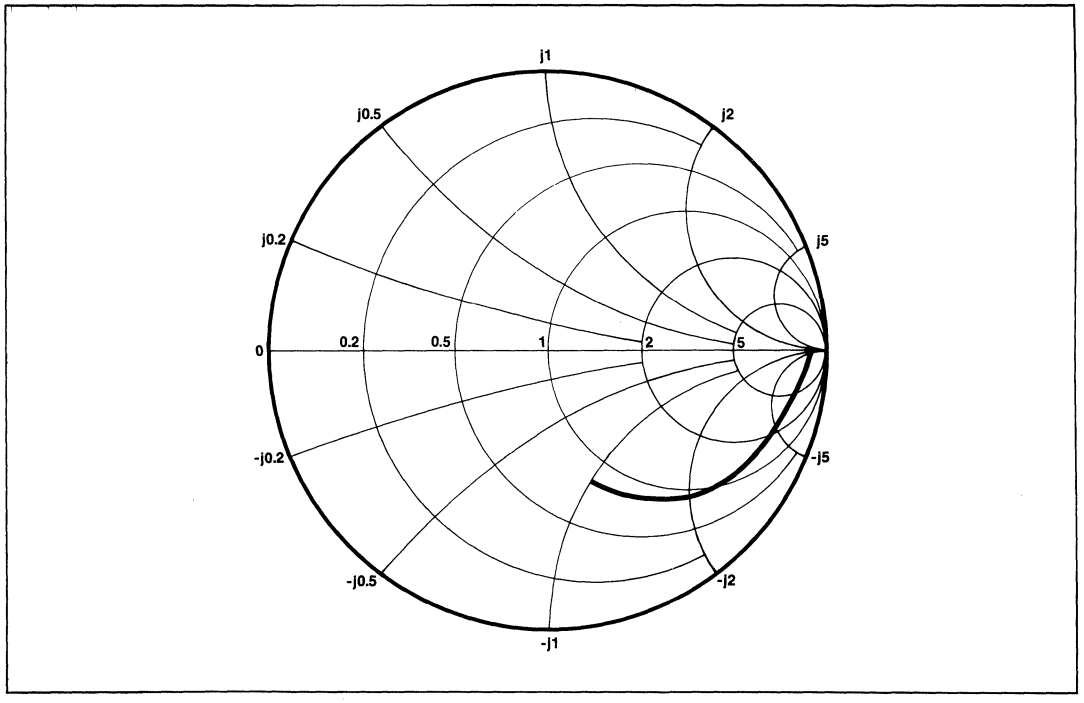


Fig.5 Typical input impedance. Test conditions: supply voltage 5.2V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

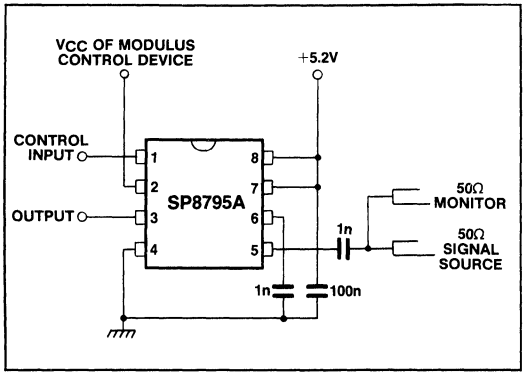


Fig.6 Toggle frequency test circuit

SP8799

225MHz ÷ 10/11 TWO MODULUS DIVIDER

The SP8799 is a low power programmable ÷10/11 counter.It divides by 10 when the control input is in the high state and by 11 when in the low state. An internal voltage regulator allows operation from a wide range of supply voltages.

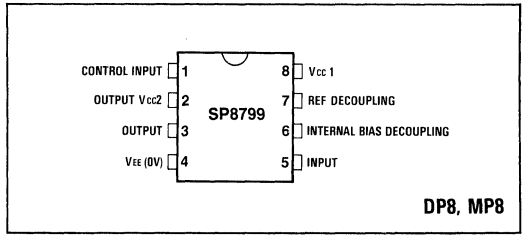


Fig.1 Pin connections - top view

FEATURES

- Very Low Power
- Control Input and Output CMOS/TTL Compatible
- AC Coupled Input
- Operation up to 9.5V using Internal Regulator

QUICK REFERENCE DATA

- Supply voltage: +5.2V or 6.8 to 9.5V
- Power consumption: 26mW Typical
- Temperature range: -40°C to +85°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage	6.0V Pins 7 & 8 tied
	13.5V Pin 8, Pin 7 decoupled
Storage temperature range	-55°C to +125°C
Max. junction temperature	+175°C
Max. clock input voltage	2.5V p-p
Vcc2	Max. 10V

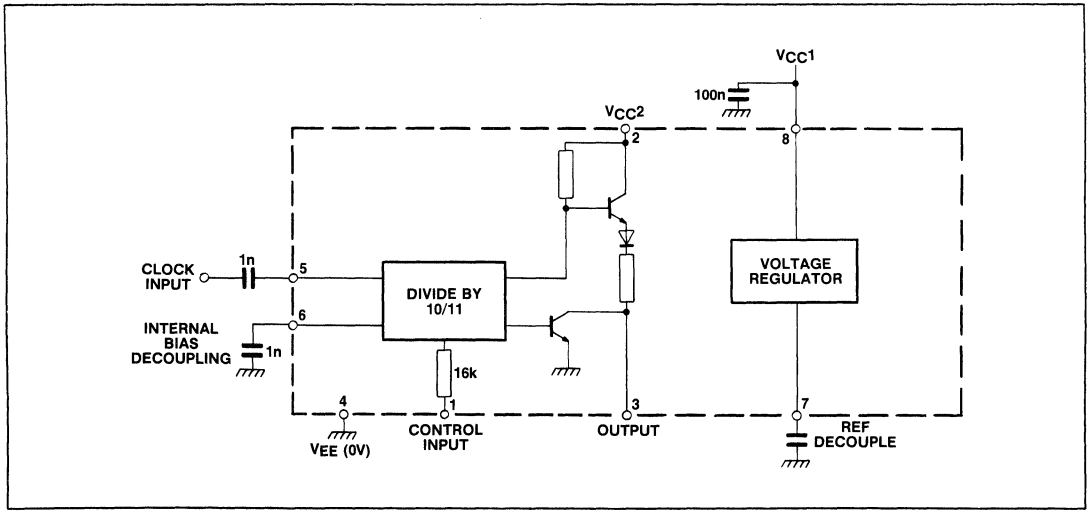


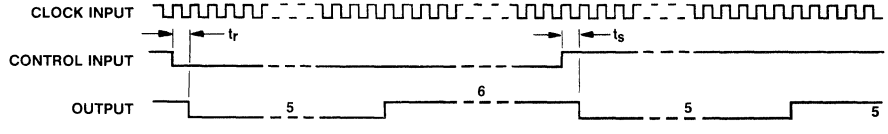
Fig.2 Functional diagram SP8799

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage: V_{CC} 1 & 2 = 5.2V ± 0.25V or 6.8V to 9.5V (see Operating Note 7);
V_{EE} = 0V; Temperature T_{amb} = -40°C to +85°C

Characteristic	Symbol	Value		Units	Notes	Conditions
		Min.	Max.			
Maximum frequency (sinewave input)	f_{max}	225		MHz	Note 4	Input = 200-800mV p-p
Minimum frequency (sinewave input)	f_{min}		20	MHz	Note 4	Input = 400-800mV p-p
Power supply current	I_{EE}		7	mA	Note 4	
Control input high voltage	V_{INH}	4		V	Note 4	
Control input low voltage	V_{INL}		2	V	Note 4	
Output high voltage	V_{OH}	2.4		V	Note 4	Pins 2, 7 and 8 linked V_{CC} = 4.95V I_{OH} = 100μA
Output low voltage	V_{OL}		0.5	V	Note 4	Pin 2 linked to 8 and 7 I_{OL} = 1.6mA
Set up time	t_s	14		ns	Note 3	25°C
Release time	t_r	20		ns	Note 3	25°C
Clock to output propagation time	t_p		45	ns	Note 3	25°C

NOTES
1. Unless otherwise stated the electrical characteristics are guaranteed over full specified supply, frequency and temperature range.
2. The test configuration for dynamic testing is shown in Fig.6.
3. Guaranteed but not tested.
4. Tested only at 25°C.



TRUTH TABLE FOR CONTROL INPUTS

Control input	Division ratio
0	11
1	10

Fig.3 Timing diagram SP8799

NOTES
The set-up time t_s is defined as minimum time that can elapse between L→H transition of control input and next L→H clock pulse transition to ensure ÷10 mode is selected.
The release time t_r is defined as minimum time that can elapse between H→L transition of the control input and the next L→H clock pulse transition to ensure the ÷11 mode is selected.

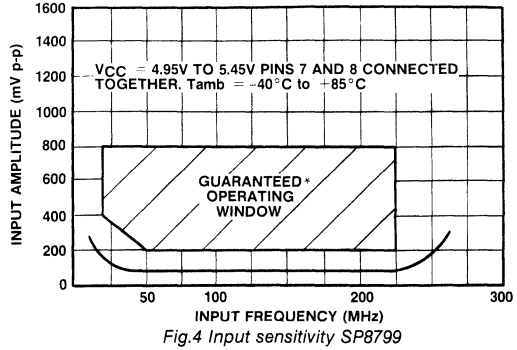


Fig.4 Input sensitivity SP8799

*Tested as specified in table of Electrical Characteristics

OPERATING NOTES

1. The clock input (Pin 5) should be capacitively coupled to the signal source. The input signal path is completed by coupling a capacitor from the internal bias decoupling, Pin 6 to ground.
2. The output stage which is normally open collector (Pin 2 open circuit) can be interfaced to CMOS. The open collector can be returned to a +10V line via a 5k resistor but the output sink current should not exceed 2mA. If interfacing to TTL is required then Pins 2 and 7 should be connected together to give a fan-out = 1. This will increase supply current by approximately 2mA.
3. The circuit will operate down to DC but a slew rate of better than 20V/μs is required.
4. The mark space ratio of the output is approximately 1.2:1 at 200MHz.
5. Input impedance is a function of frequency. See Fig.5.
6. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 150k between unused input and ground. This reduces the input sensitivity by typically 50-100mV p-p.
7. The internal regulator has its input connected to Pin 8, while the internal reference voltage appears at Pin 7 and should be decoupled. For use from a 5.2V supply, Pins 7 and 8 should be connected together, and 5.2V applied to these pins. For operation from supply voltages in the range +6.8V to +9.5V, Pins 7 and 8 should be separately decoupled, and the supply voltage applied to Pin 8.

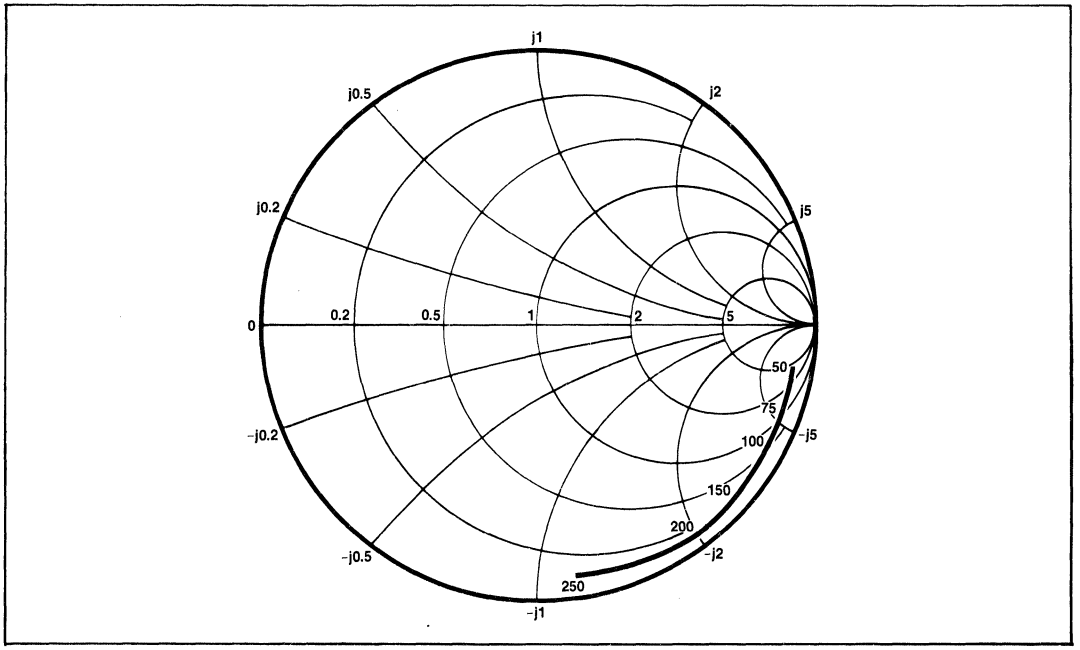


Fig.5 Typical input impedance. Test conditions: supply voltage 5.2V, ambient temperature 25°C, frequencies in MHz, impedances normalised to 50 ohms.

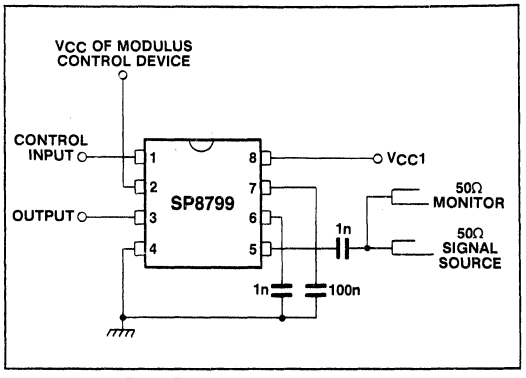


Fig.6 Toggle frequency test circuit

SP8799A

200MHz ÷ 10/11 TWO MODULUS DIVIDER

The SP8799A is a low power programmable ÷10/11 counter which operates over the full Military temperature range. It divides by 10 when the control input is in the high state and by 11 when in the low state.

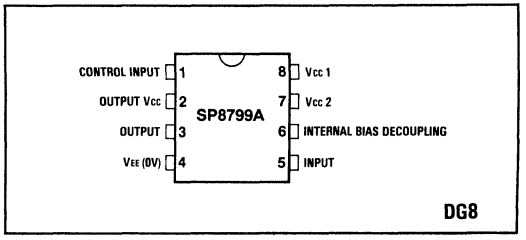


Fig.1 Pin connections - top view

FEATURES

- Very Low Power
- Control Input and Output CMOS/TTL Compatible
- AC Coupled Input

QUICK REFERENCE DATA

- Supply voltage: +5.2V
- Power consumption: 26mW typical
- Temperature range: -55°C to +125°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage:	6.0V Pins 7 & 8 tied
Storage temperature range:	-55°C to +150°C
Max. junction temperature:	+175°C
Max. clock input voltage:	2.5V p-p

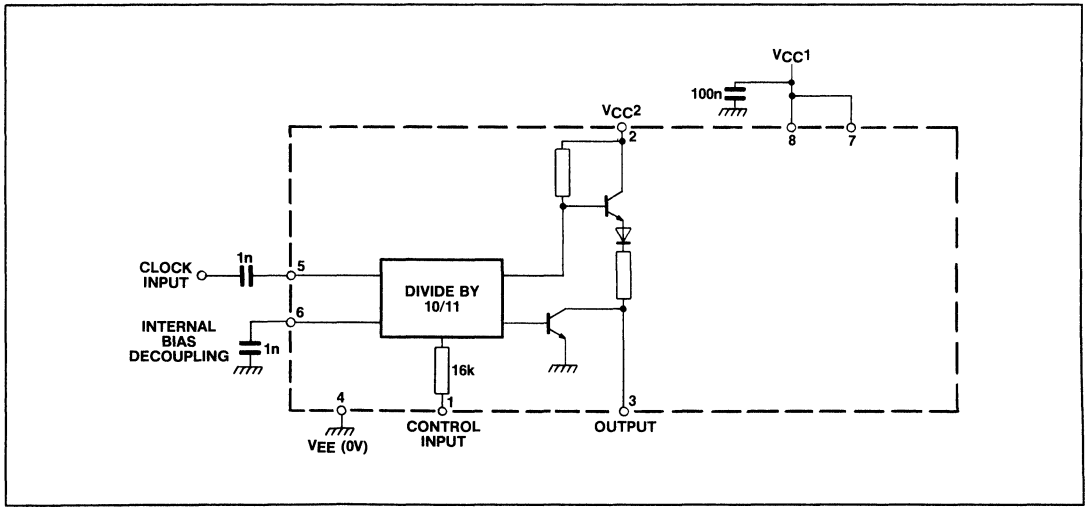


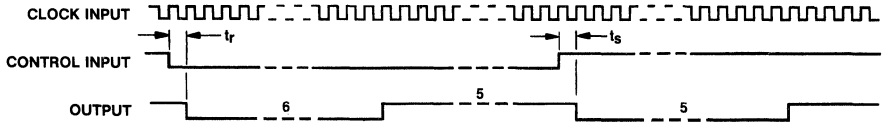
Fig.2 Function diagram SP8799A

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage: V_{CC} 1 & 2 = 5.2V ± 0.25V; V_{EE} = 0V; Temperature T_{amb} = -55°C to +125°C

Characteristic	Symbol	Value		Units	Notes	Conditions
		Min.	Max.			
Maximum frequency	f_{max}	200		MHz		Input = 200-400mV p-p
(sinewave input)		150		MHz	Note 3	Input = 200-800mV p-p
Minimum frequency	f_{min}		20	MHz	Note 3	Input = 400mV p-p
(sinewave input)			50	MHz		Input = 200mV p-p
Power supply current	I_{EE}		7	mA	Note 4	
Control input high voltage	V_{INH}	4	5.2	V	Note 4	
Control input low voltage	V_{INL}		2	V	Note 4	
Output high voltage	V_{OH}	2.4		V	Note 4	Pins 2, 7 and 8 linked V_{CC} = 4.95V I_{OH} = 100μA
Output low voltage	V_{OL}		0.5	V	Note 4	Pin 2 linked to 8 and 7 I_{OL} = 1.6mA
Set up time	t_s	14		ns	Note 3	25°C
Release time	t_r	20		ns	Note 3	25°C
Clock to output propagation time	t_p		45	ns	Note 3	25°C

NOTES
1. Unless otherwise stated the electrical characteristics are guaranteed over full specified supply, frequency and temperature range.
2. The test configuration for dynamic testing is shown in Fig.6.
3. Guaranteed but not tested.
4. Tested at 25°C only.

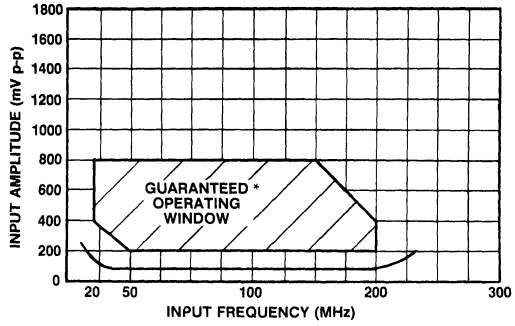


TRUTH TABLE FOR CONTROL INPUTS

Control inputs	Division ratio
0	11
1	10

Fig.3 Timing diagram SP8799A

NOTES
The set-up time t_s is defined as minimum time that can elapse between L→H transition of control input and next L→H clock pulse transition to ensure ÷10 mode is selected.
The release time t_r is defined as minimum time that can elapse between H→L transition of the control input and the next L→H clock pulse transition to ensure the ÷11 mode is selected.



*Tested as specified in table of Electrical Characteristics

Fig.4 Input sensitivity SP8799A

OPERATING NOTES

1. The clock input (Pin 5) should be capacitively coupled to the signal source. The input signal path is completed by coupling a capacitor from the internal bias decoupling, Pin 6 to ground.
2. The output stage which is normally open collector (Pin 2 open circuit) can be interfaced to CMOS. The open collector can be returned to a +10V line via a 5k resistor but the output sink current should not exceed 2mA. If interfacing to TTL is required then Pins 2 and 7 should be connected together to give a fan-out = 1. This will increase supply current by approximately 2mA.
3. The circuit will operate down to DC but a slew rate of better than 20V/μs is required.
4. The mark space ratio of the output is approximately 1.2:1 at 200MHz.
5. Input impedance is a function of frequency. See Fig.5.
6. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 150k between unused input and ground. This reduces the input sensitivity by typically 50-100mV p-p.
7. The supply voltage regulator which allows the SP8799 to be used at supply voltages up to 9.5V is *NOT* available for use in the A Grade device: the SP8799A is *ONLY* available for operation from 5.2V supply, and therefore Pins 7 and 8 should always be externally connected together.

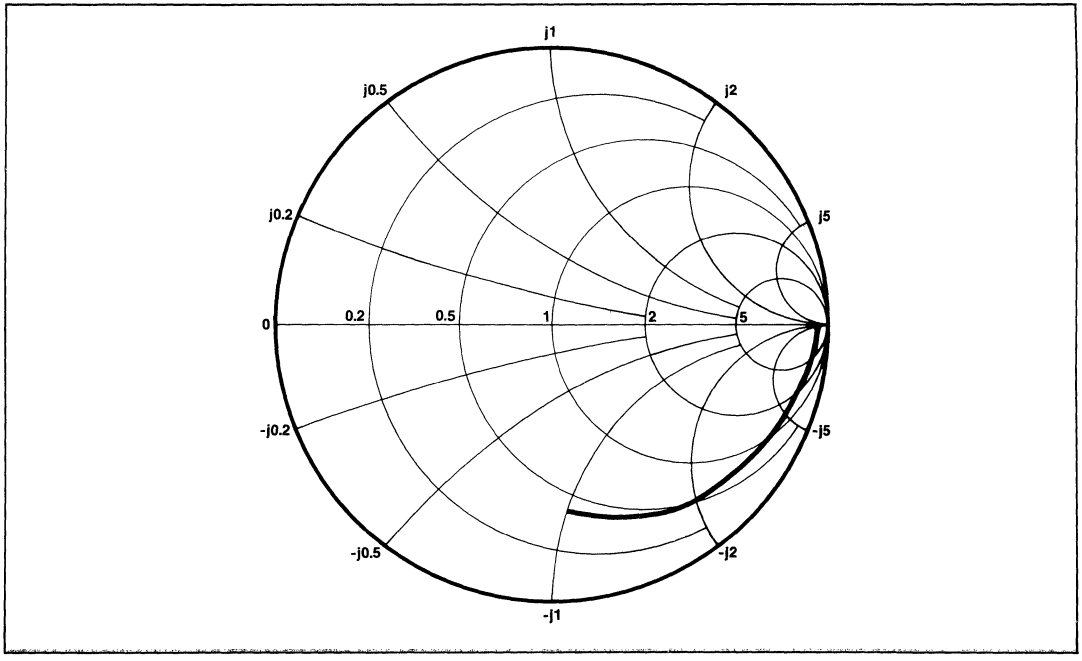


Fig.5 Typical input impedance. Test conditions: supply voltage 5.2V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

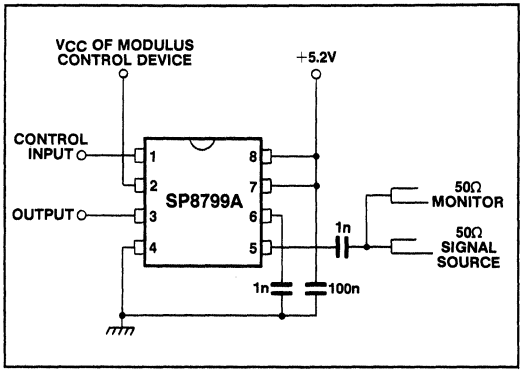


Fig.6 Toggle frequency test circuit

PLESSEY
Semiconductors

SP8802A

3.3GHz ÷ 2 FIXED MODULUS DIVIDER

The SP8802A is one of a range of very high speed low power prescalers for professional and military applications. The device features a complementary output stage with on chip current sources for the emitter follower outputs.

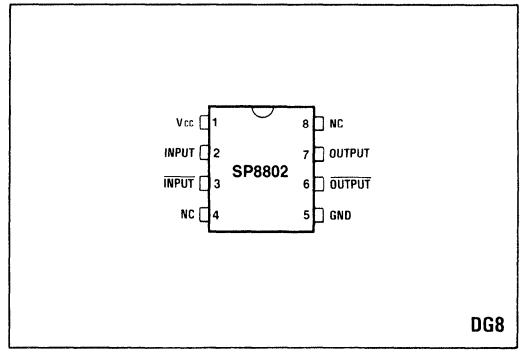


Fig.1 Pin connections - top view

FEATURES

- Very High Speed Operation 3.3GHz
- Silicon Technology for Low Phase Noise (Typically better than -140dBc/Hz at 10kHz
- Specified over the Full Military Temperature Range
- Low Power Dissipation 420mW (Typ.)
- 5V Single Supply Operation
- High Input Sensitivity
- Very Wide Operating Frequency Range

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	6.5V
Clock input voltage	2.5V p-p
Storage temperature range	-55°C to +150°C
Junction temperature	+175°C

THERMAL CHARACTERISTICS

θ_{JA} = 150°C/W

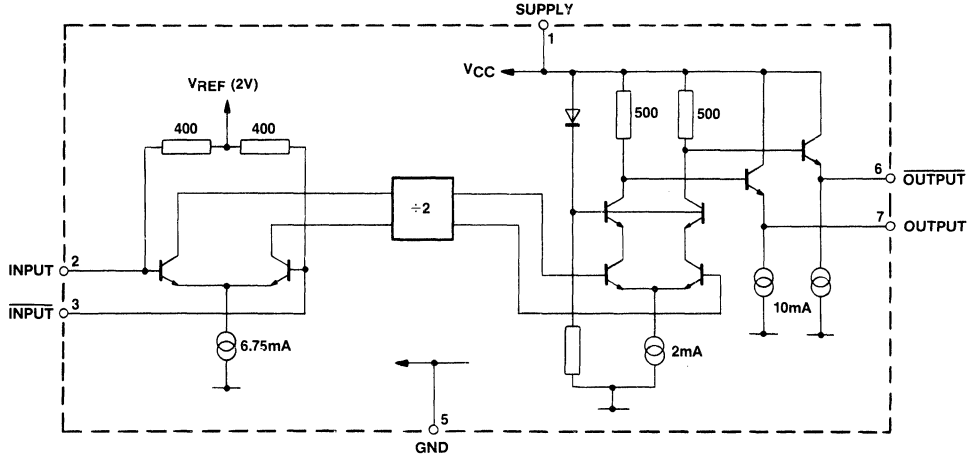


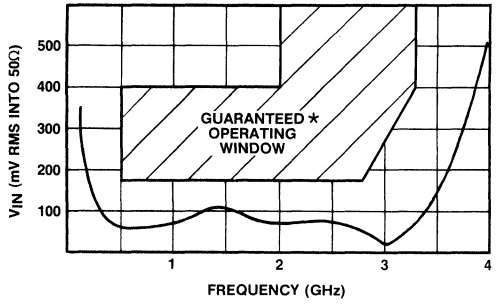
Fig.2 SP8802A block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = -55°C to +125°C, V_{CC} = 4.75V to 5.25V (See Note)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	1		84	100	mA	V_{CC} = 5V
Input sensitivity	2,3					RMS sinewave
0.5GHz to 2.8GHz				175	mV	Measured in 50Ω
3.3GHz				400	mV	system. See Figs. 3 & 4
Input impedance (series equivalent)	2,3		50		Ω	
			2		pF	
Output voltage with f_{in} = 1000MHz	6,7	0.8	1		V p-p	V_{CC} = 5V
Output voltage with f_{in} = 3GHz	6,7		0.35		V p-p	V_{CC} = 5V load as Fig.4

NOTE
Devices must be used with a suitable heatsink to maintain chip temperature below 175°C when operating at T_{amb} > 100°C.



* Tested as specified in Table of Electrical Characteristics

Fig.3 Typical input sensitivity

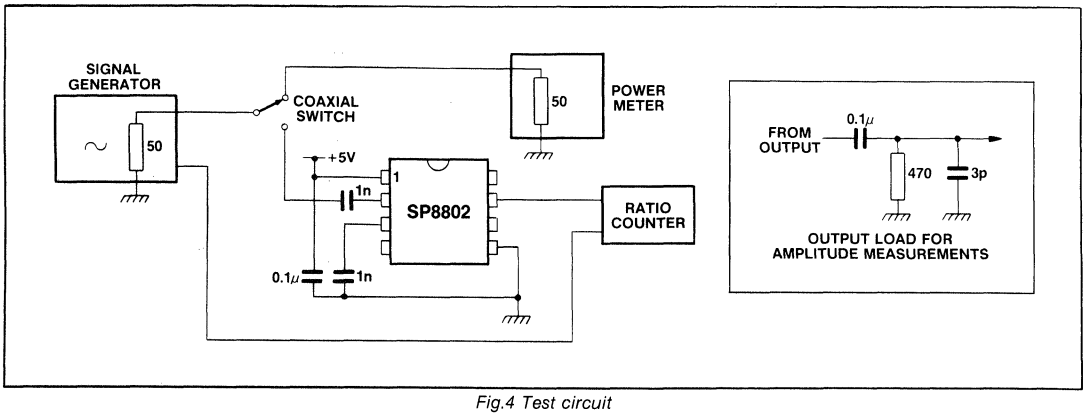


Fig.4 Test circuit

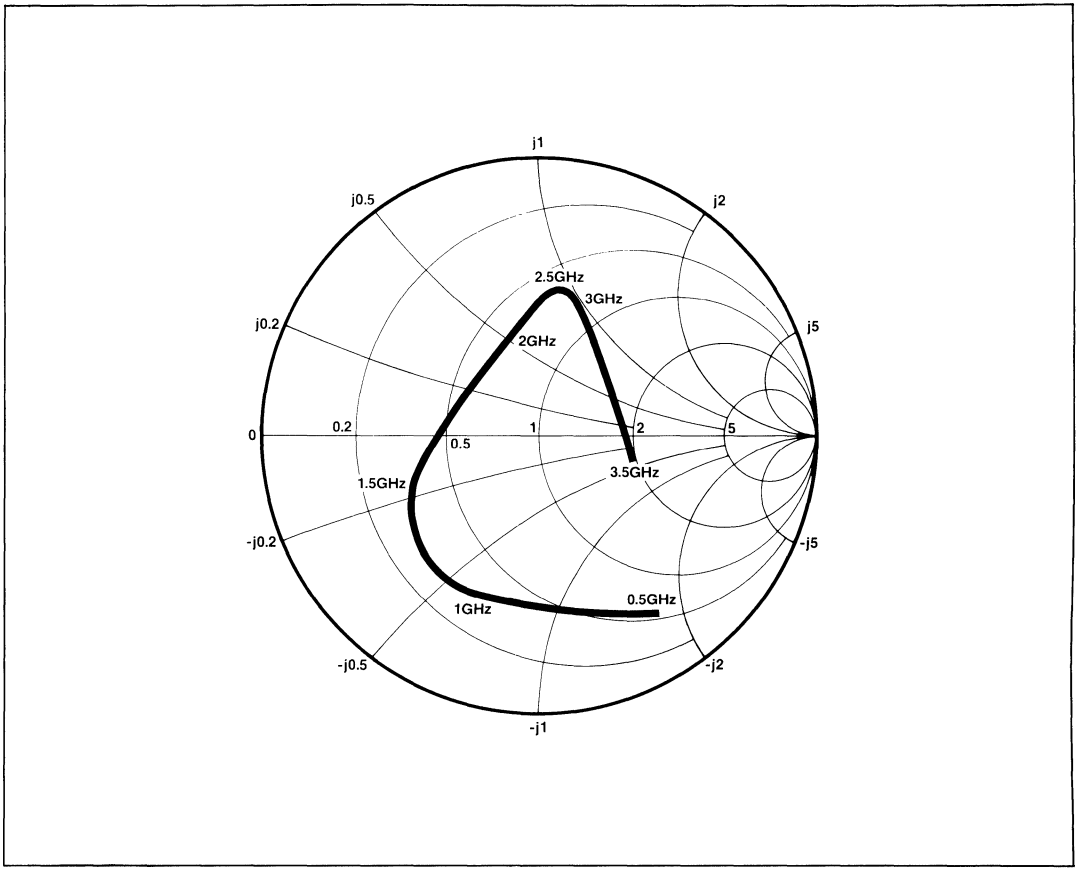


Fig.5 Typical input impedance

SP8804A

3.3GHz ÷ 4 FIXED MODULUS DIVIDER

The SP8804A is one of a range of very high speed low power prescalers for professional and military applications. The device features a complementary output stage with on chip current sources for the emitter follower outputs.

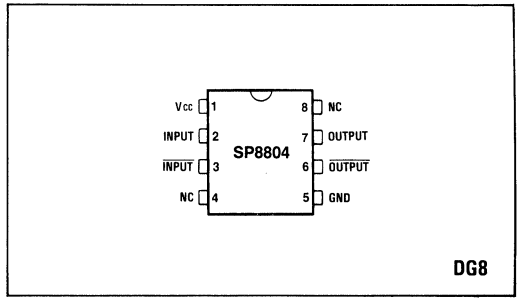


Fig.1 Pin connections - top view

FEATURES

- Very High Speed Operation 3.3GHz
- Silicon Technology for Low Phase Noise (Typically better than -140dBc/Hz at 10kHz
- Specified over the Full Military Temperature Range
- Low Power Dissipation 370mW (Typ.)
- 5V Single Supply Operation
- High Input Sensitivity
- Very Wide Operating Frequency Range

ABSOLUTE MAXIMUM RATINGS

Supply voltage Vcc	6.5V
Clock input voltage	2.5V p-p
Storage temperature range	-55°C to +150°C
Junction temperature	+175°C

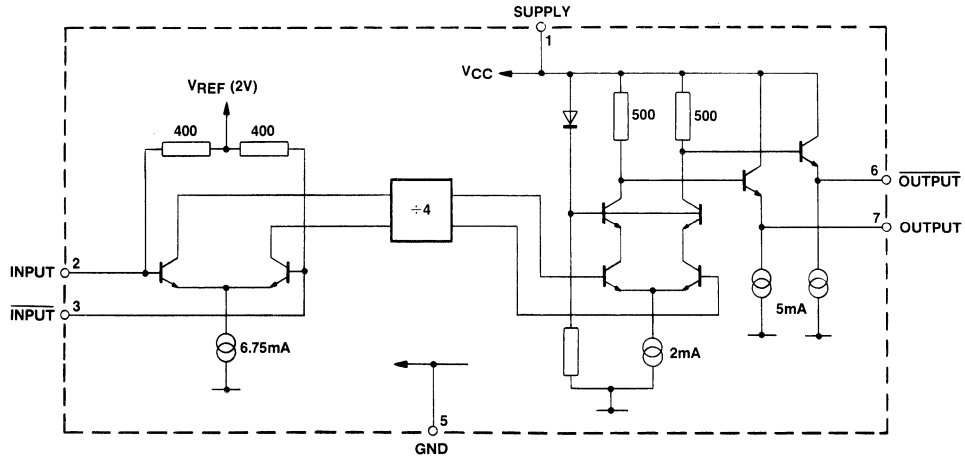


Fig.2 SP8804A block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = -55°C to +125°C, V_{CC} = 4.75V to 5.25V (See Note)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	1		74	90	mA	V_{CC} = 5V
Input sensitivity	2,3					RMS sinewave
0.5GHz to 2.8GHz				175	mV	Measured in 50Ω
3.3GHz				400	mV	system. See Figs. 3 & 4
Input impedance (series equivalent)	2,3		50		Ω	
			2		pF	
Output voltage with f_{in} = 1000MHz	6,7	0.8	1		V p-p	V_{CC} = 5V
Output voltage with f_{in} = 3GHz	6,7		0.25		V p-p	V_{CC} = 5V load as Fig.4

NOTE
Devices must be used with a suitable heatsink to maintain chip temperature below 175°C when operating at T_{amb} >105°C.

THERMAL CHARACTERISTICS

θ_{JA} = 150°C/W

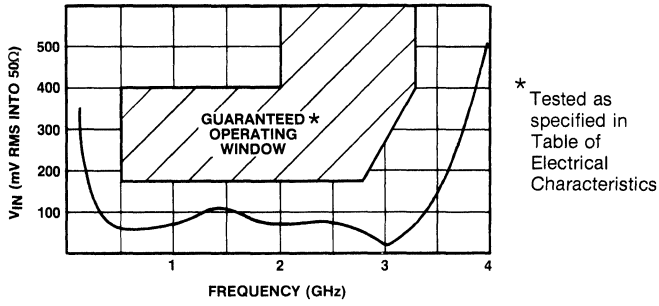


Fig.3 Typical input sensitivity

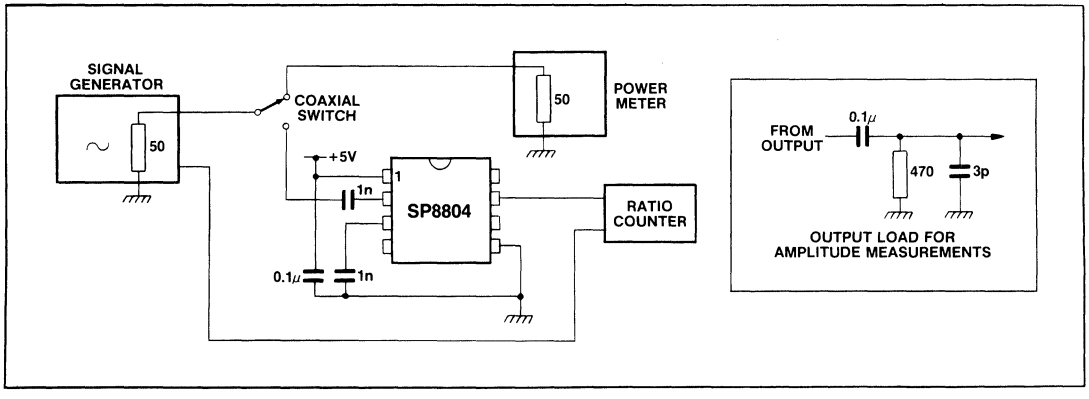


Fig.4 Test circuit

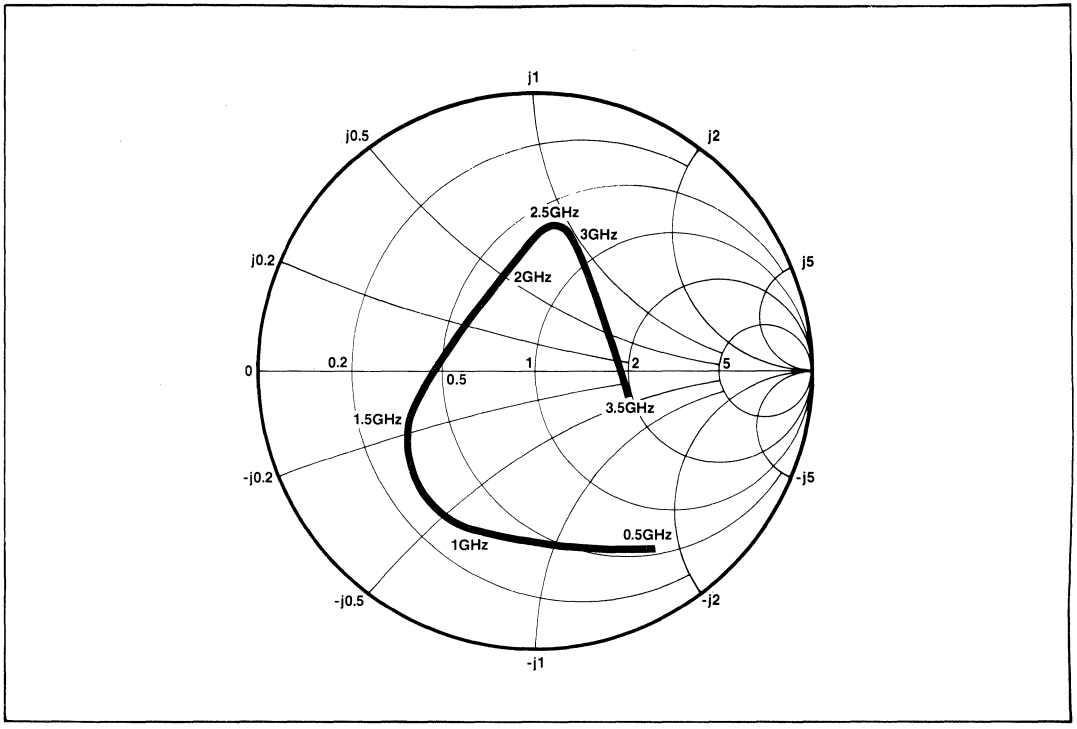


Fig.5 Typical input impedance

PLESSEY
Semiconductors

SP8808A

3.3GHz ÷ 8 FIXED MODULUS DIVIDER

The SP8808A is one of a range of very high speed low power prescalers for professional and military applications. The device features a complementary output stage with on chip current sources for the emitter follower outputs.

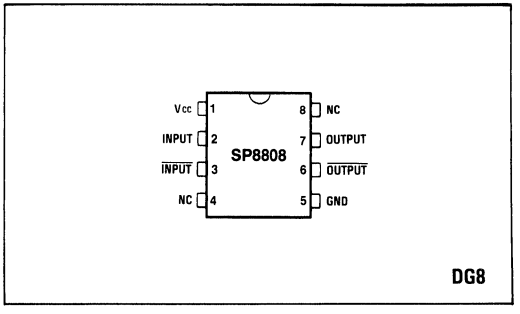


Fig.1 Pin connections - top view

FEATURES

- Very High Speed Operation 3.3GHz
- Silicon Technology for Low Phase Noise (Typically better than -140dBc/Hz at 10kHz
- Specified over the Full Military Temperature Range
- Low Power Dissipation 345mW (Typ.)
- 5V Single Supply Operation
- High Input Sensitivity
- Very Wide Operating Frequency Range

ABSOLUTE MAXIMUM RATINGS

Supply voltage Vcc	6.5V
Clock input voltage	2.5V p-p
Storage temperature range	-55°C to +150°C
Junction temperature	+175°C

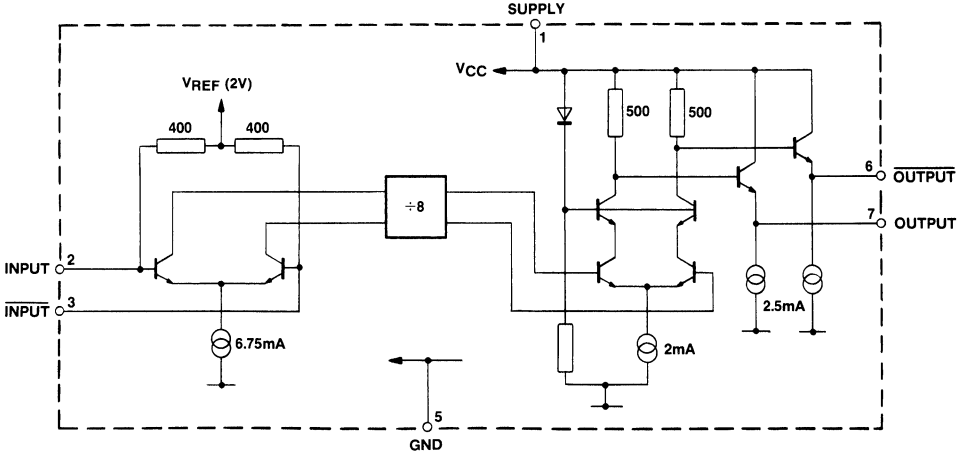


Fig.2 SP8808A block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = -55°C to +125°C, V_{CC} = 4.75V to 5.25V (See Note)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	1		69	85	mA	V_{CC} = 5V
Input sensitivity	2,3					RMS sinewave
0.5GHz to 2.8GHz				175	mV	Measured in 50Ω
3.3GHz				400	mV	system. See Figs. 3 & 4
Input impedance (series equivalent)	2,3		50		Ω	
			2		pF	
Output voltage with f_{in} = 1000MHz	6,7	0.8	1		V p-p	V_{CC} = 5V
Output voltage with f_{in} = 3GHz	6,7		0.4		V p-p	V_{CC} = 5V load as Fig.4

NOTE
Devices must be used with a suitable heat sink to maintain chip temperature below 175°C when operating at T_{amb} >110°C.

THERMAL CHARACTERISTICS

θ_{JA} = 150°C/W

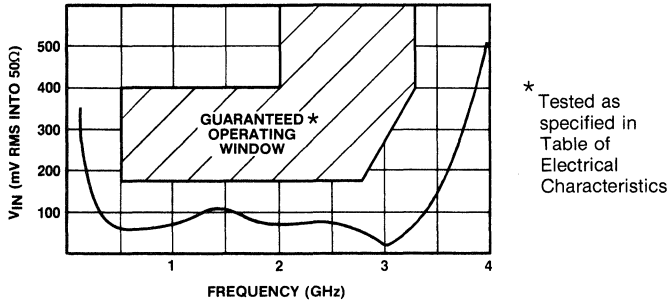


Fig.3 Typical input sensitivity

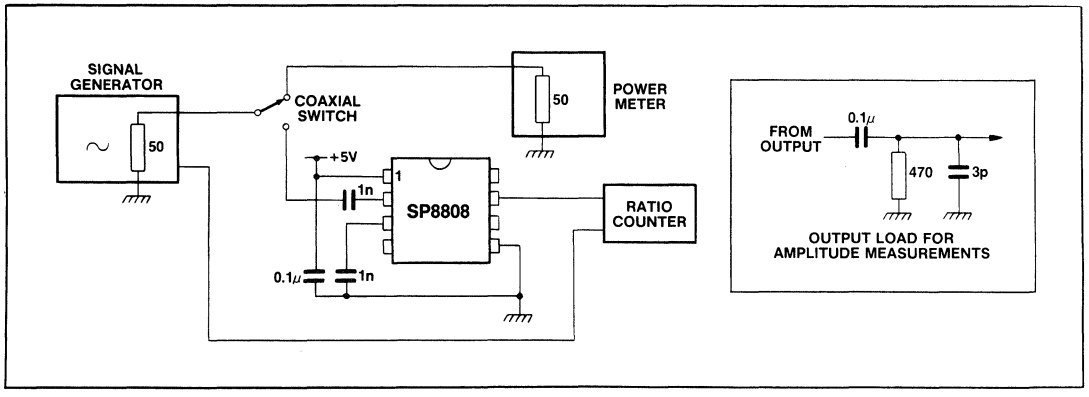


Fig.4 Test circuit

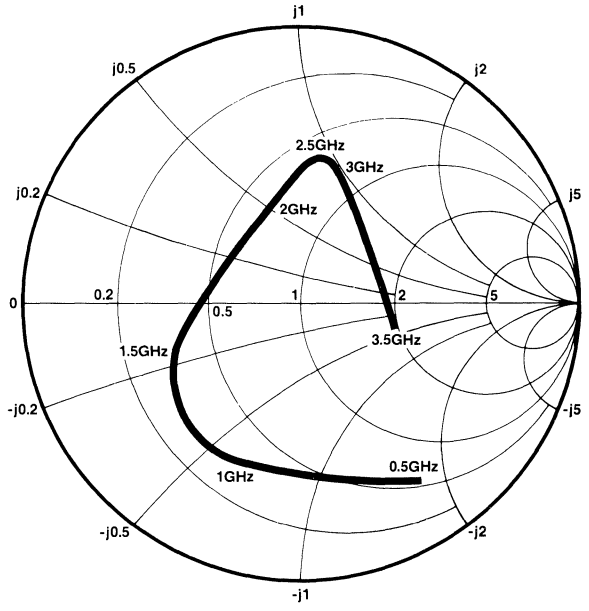


Fig.5 Typical input impedance

SP8812A & B

2.4GHz ÷ 2 FIXED MODULUS DIVIDER

The SP8812 is one of a range of very high speed low power prescalers for professional and military applications. The device features a complementary output stage with on chip current sources for the emitter follower outputs.

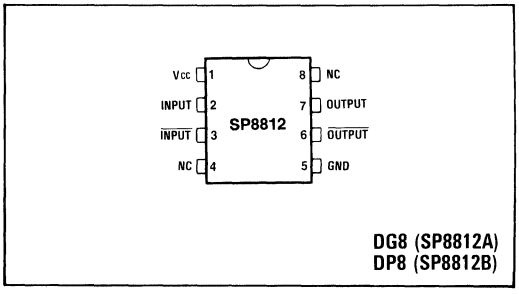


Fig.1 Pin connections - top view

FEATURES

- High Speed Operation 2.4GHz
- Silicon Technology for Low Phase Noise (Typically better than -140dBc/Hz at 10kHz
- Very Low Power Dissipation 250mW (Typ.)
- 5V Single Supply Operation
- High Input Sensitivity
- Very Wide Operating Frequency Range
- Temperature Range:
  -55°C to +125°C (A Grade)
  -40°C to +85°C (B Grade)

ABSOLUTE MAXIMUM RATINGS

Supply voltage Vcc	6.5V
Clock input voltage	2.5V p-p
Storage temperature range	-55°C to +150°C
Junction temperature	+175°C

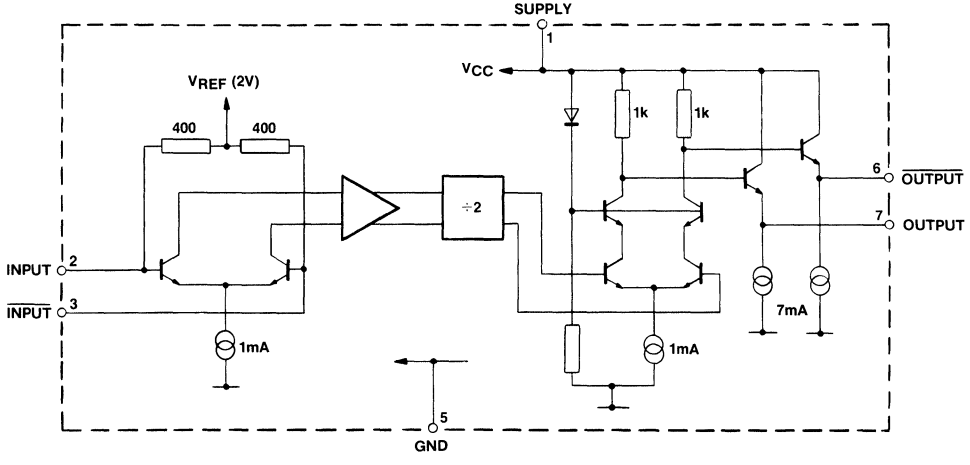
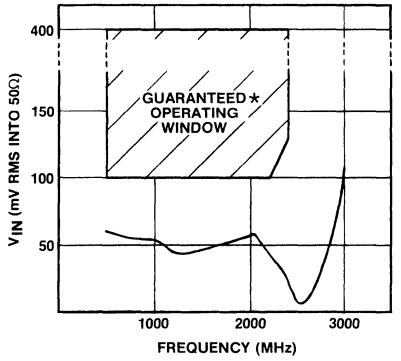


Fig.2 SP8812 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = A Grade -55°C to +125°C, B Grade -40°C to +85°C, V_{CC} = +4.75V to +5.25V

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	1		50	65	mA	V_{CC} = 5V
Input sensitivity	2,3					RMS sinewave
500MHz to 2200MHz				100	mV	Measured in 50Ω
2400MHz				125	mV	system. See Figs. 3 & 4
Input impedance (series equivalent)	2,3		50 2		Ω pF	See Fig.5
Output voltage with f_{in} = 500MHz	6,7	0.8	1		V p-p	V_{CC} = 5V
Output voltage with f_{in} = 2400MHz	6,7		0.13		V p-p	V_{CC} = 5V load as Fig.4



* Tested as specified in Table of Electrical Characteristics

Fig.3 Typical input sensitivity

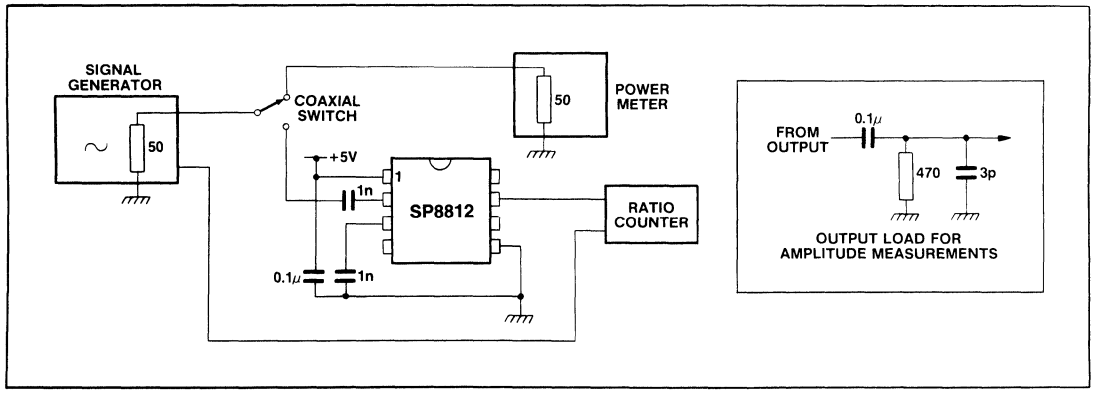


Fig.4 Test circuit

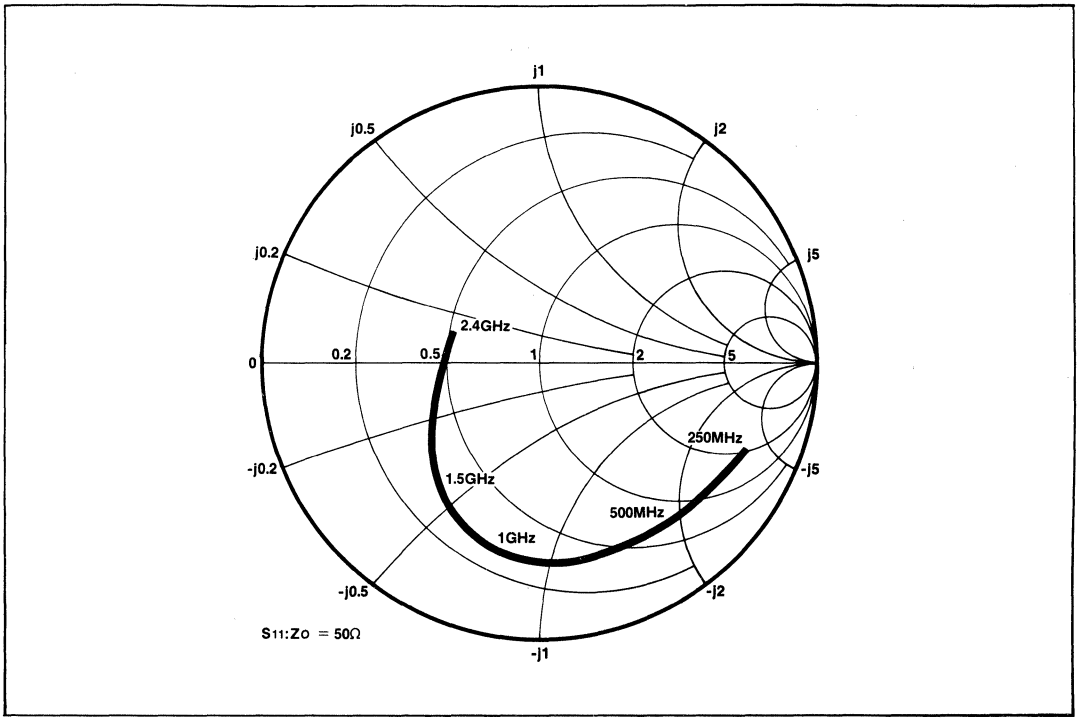


Fig.5 Typical input impedance

SP8814A & B

2.4GHz ÷ 4 FIXED MODULUS DIVIDER

The SP8814 is one of a range of very high speed low power prescalers for professional and military applications. The device features a complementary output stage with on chip current sources for the emitter follower outputs.

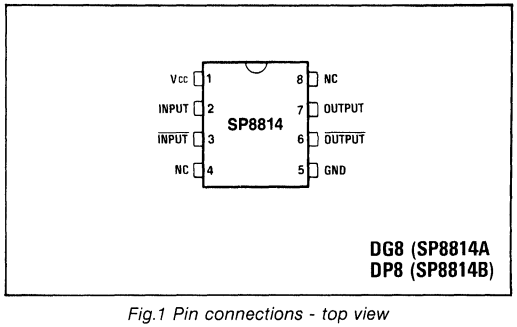


Fig.1 Pin connections - top view

FEATURES

- High Speed Operation 2.4GHz
- Silicon Technology for Low Phase Noise (Typically better than -140dBc/Hz at 10kHz
- Very Low Power Dissipation 220mW (Typ.)
- 5V Single Supply Operation
- High Input Sensitivity
- Very Wide Operating Frequency Range
- Temperature Range:
  -55°C to +125°C (A Grade)
  -40°C to +85°C (B Grade)

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	6.5V
Clock input voltage	2.5V p-p
Storage temperature range	-55°C to +150°C
Junction temperature	+175°C

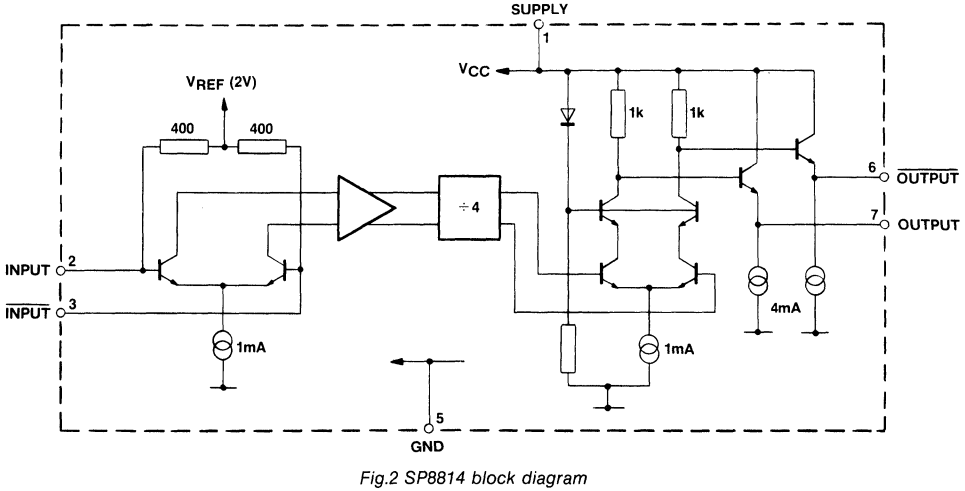
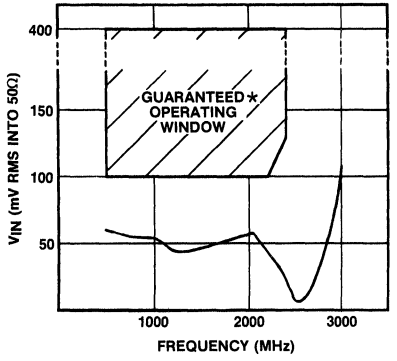


Fig.2 SP8814 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = A Grade -55°C to +125°C, B Grade -40°C to +85°C, V_{CC} = +4.75V to +5.25V

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	1		44	52	mA	V_{CC} = 5V
Input sensitivity	2,3					RMS sinewave
500MHz to 2200MHz				100	mV	Measured in 50Ω
2400MHz				125	mV	system. See Figs. 3 & 4
Input impedance (series equivalent)	2,3		50		Ω	
			2		pF	
Output voltage with f_{in} = 500MHz	6,7	0.8	1		V p-p	V_{CC} = 5V
Output voltage with f_{in} = 2400MHz	6,7		0.13		V p-p	V_{CC} = 5V load as Fig.4



*Tested as specified in Table of Electrical Characteristics

Fig.3 Typical input sensitivity

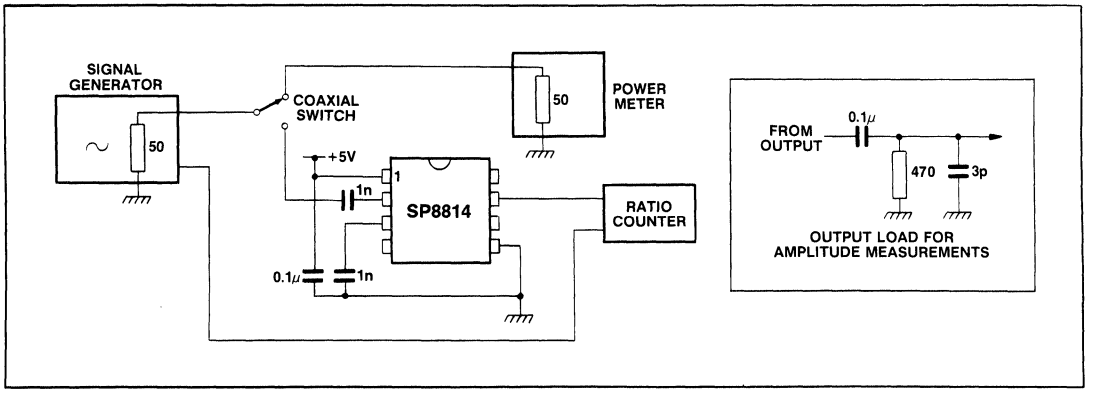


Fig.4 Test circuit

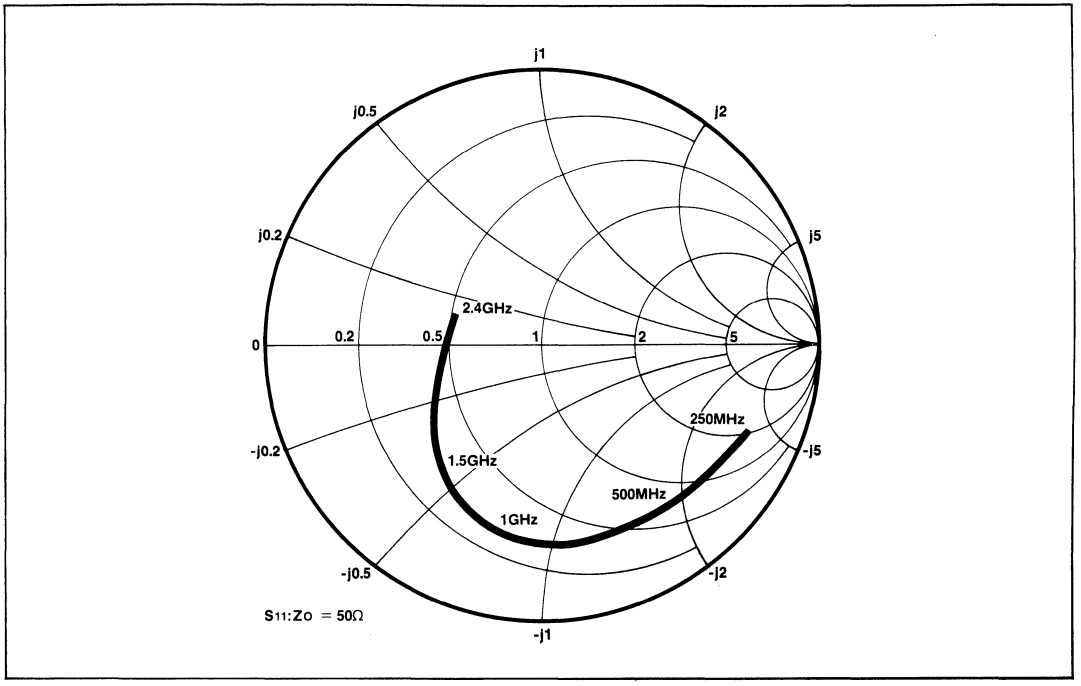


Fig.5 Typical input impedance

SP8818A & B

2.4GHz ÷ 8 FIXED MODULUS DIVIDER

The SP8818 is one of a range of very high speed low power prescalers for professional and military applications. The device features a complementary output stage with on chip current sources for the emitter follower outputs.

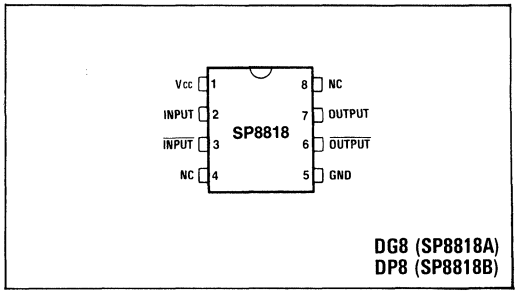


Fig.1 Pin connections - top view

FEATURES

- High Speed Operation 2.4GHz
- Silicon Technology for Low Phase Noise (Typically better than -140dBc/Hz at 10kHz
- Very Low Power Dissipation 200mW (Typ)
- 5V Single Supply Operation
- High Input Sensitivity
- Very Wide Operating Frequency Range
- Temperature Range:
  -55°C to +125°C (A Grade)
  -40°C to +85°C (B Grade)

ABSOLUTE MAXIMUM RATINGS

Supply voltage Vcc	6.5V
Clock input voltage	2.5V p-p
Storage temperature range	-55°C to +150°C
Junction temperature	+175°C

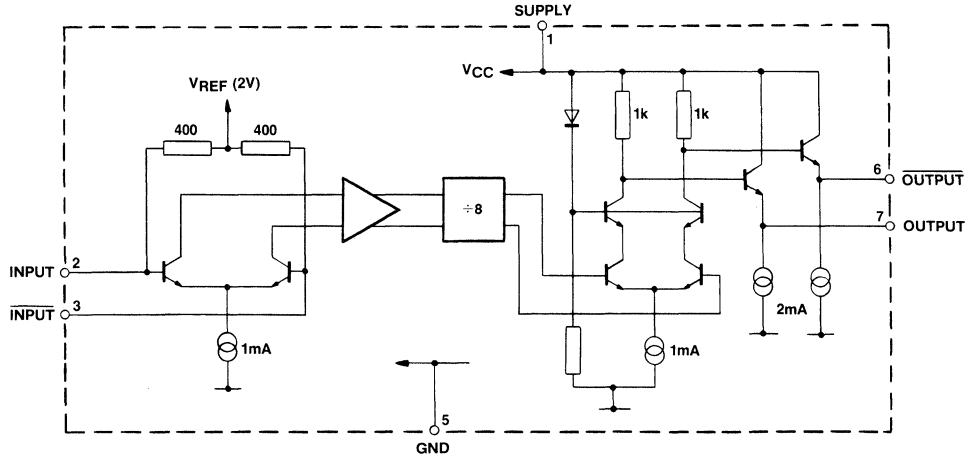


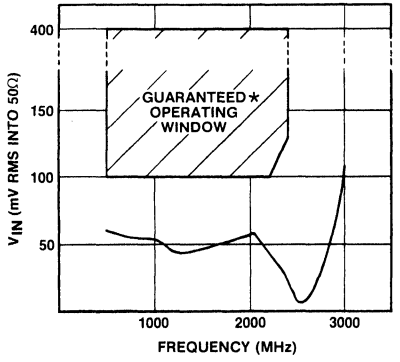
Fig.2 SP8818 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} = A Grade -55°C to +125°C, B Grade -40°C to +85°C, V_{CC} = +4.75V to +5.25V

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	1		40	48	mA	V_{CC} = 5V
Input sensitivity	2,3					RMS sinewave
500MHz to 2200MHz				100	mV	Measured in 50Ω
2400MHz				125	mV	system. See Figs. 3 & 4
Input impedance (series equivalent)	2,3		50		Ω	
			2		pF	
Output voltage with f_{in} = 500MHz	6,7	0.8	1		V p-p	V_{CC} = 5V
Output voltage with f_{in} = 2400MHz	6,7		0.13		V p-p	V_{CC} = 5V load as Fig.4



* Tested as specified in Table of Electrical Characteristics

Fig.4 Test circuit

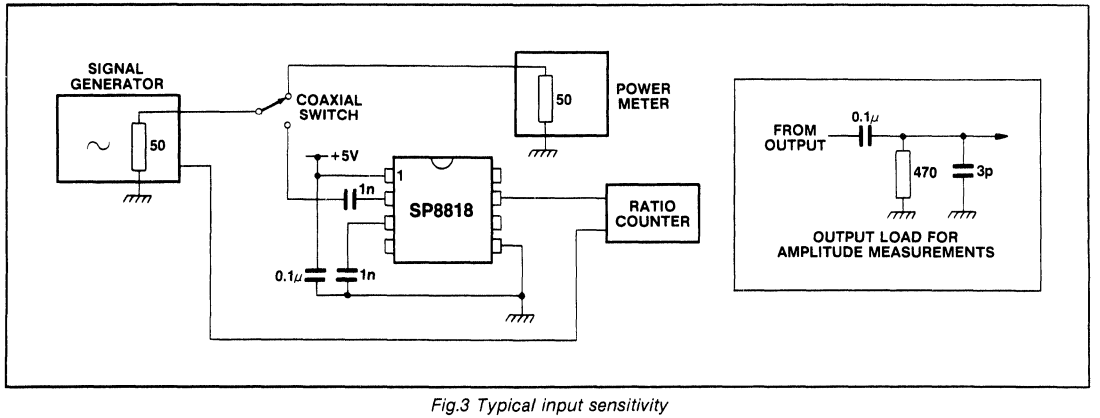


Fig.3 Typical input sensitivity

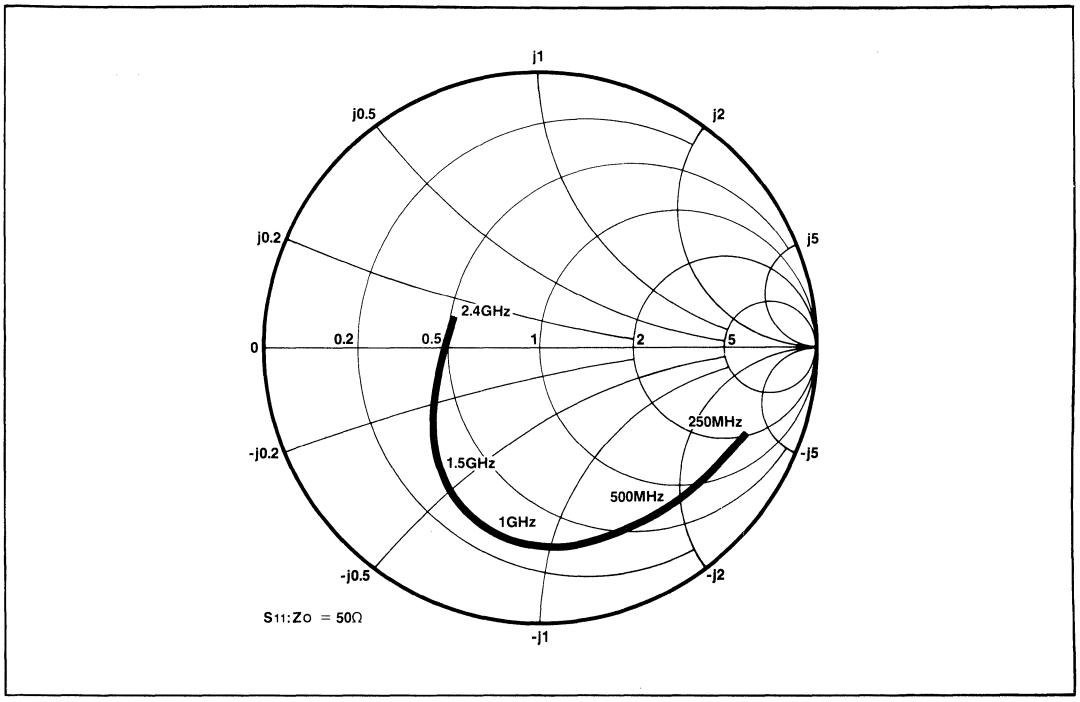


Fig.5 Typical input impedance

SP8822A & B

1.8GHz ÷ 2 FIXED MODULUS DIVIDER

The SP8822 is one of a range of very high speed low power prescalers for professional and military applications. The device features a complementary output stage with on chip current sources for the emitter follower outputs.

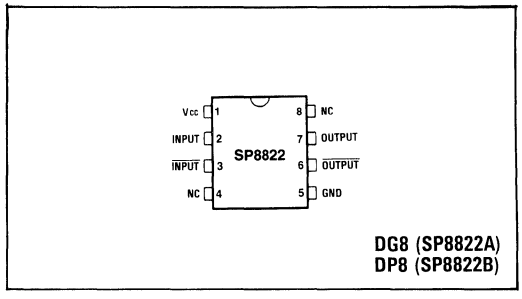


Fig.1 Pin connections - top view

FEATURES

- High Speed Operation 1.8GHz
- Silicon Technology for Low Phase Noise (Typically better than -140dBc/Hz at 10kHz
- Very Low Power Dissipation 215mW (Typ.)
- 5V Single Supply Operation
- High Input Sensitivity
- Very Wide Operating Frequency Range
- Temperature Range:
  -55°C to +125°C (A Grade)
  -40°C to +85°C (B Grade)

ABSOLUTE MAXIMUM RATINGS

Supply voltage Vcc	6.5V
Clock input voltage	2.5V p-p
Storage temperature range	-55°C to +150°C
Junction temperature	+175°C

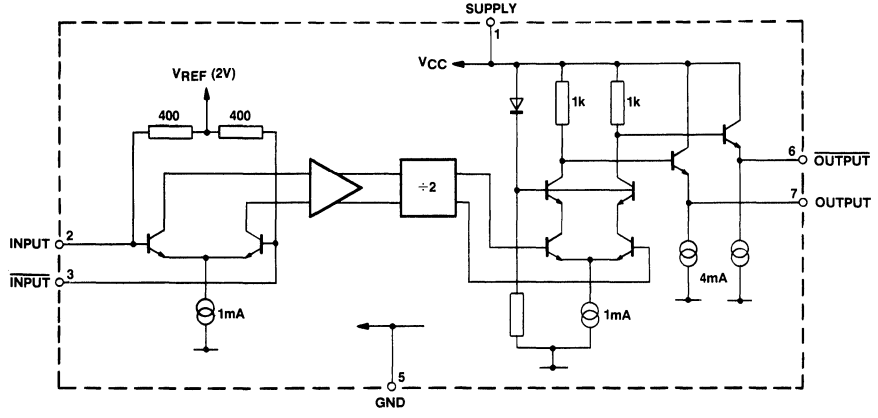
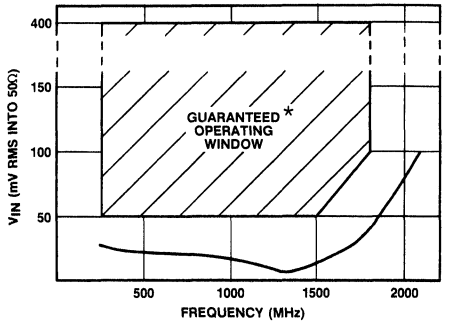


Fig.2 SP8822 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = A Grade -55°C to +125°C, B Grade -40°C to +85°C, V_{CC} = +4.75V to +5.25V

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	1		43	53	mA	V_{CC} = 5V
Input sensitivity	2,3					RMS sinewave
200MHz to 1500MHz				50	mV	Measured in 50Ω
1800MHz				100	mV	system. See Figs. 3 & 4
Input impedance (series equivalent)	2,3		50		Ω	See Fig.5
			2		pF	
Output voltage with f_{in} = 250MHz	6,7	0.8	1		V p-p	V_{CC} = 5V
Output voltage with f_{in} = 1800MHz	6,7		0.13		V p-p	V_{CC} = 5V load as Fig.4



* Tested as specified in Table of Electrical Characteristics

Fig.3 Typical input sensitivity

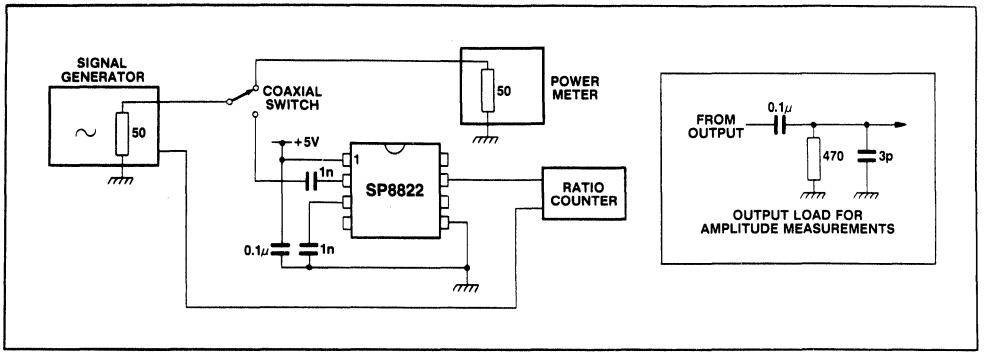


Fig.4 Test circuit

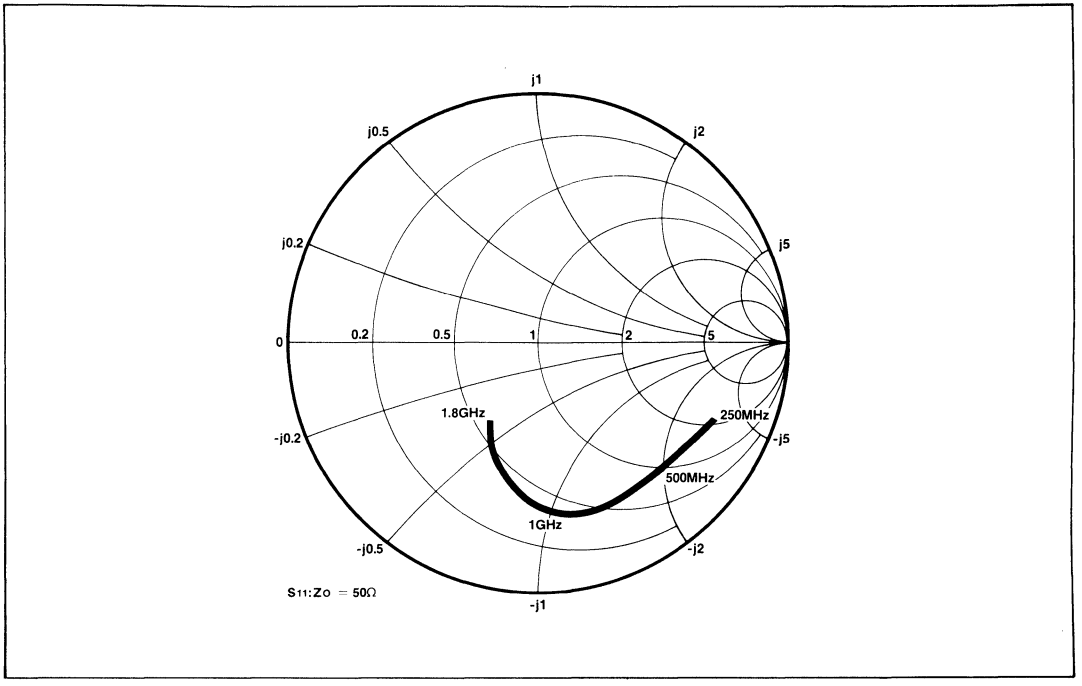


Fig.5 Typical input impedance

SP8824A & B

1.8GHz ÷ 4 FIXED MODULUS DIVIDER

The SP8824 is one of a range of very high speed low power prescalers for professional and military applications. The device features a complementary output stage with on chip current sources for the emitter follower outputs.

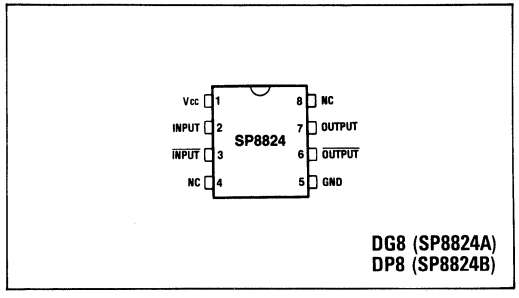


Fig.1 Pin connections - top view

FEATURES

- High Speed Operation 1.8GHz
- Silicon Technology for Low Phase Noise (Typically better than -140dBc/Hz at 10kHz
- Very Low Power Dissipation 190mW (Typ.)
- 5V Single Supply Operation
- High Input Sensitivity
- Very Wide Operating Frequency Range
- Temperature Range:
  -55°C to +125°C (A Grade)
  -40°C to +85°C (B Grade)

ABSOLUTE MAXIMUM RATINGS

Supply voltage Vcc	6.5V
Clock input voltage	2.5V p-p
Storage temperature range	-55°C to +150°C
Junction temperature	+175°C

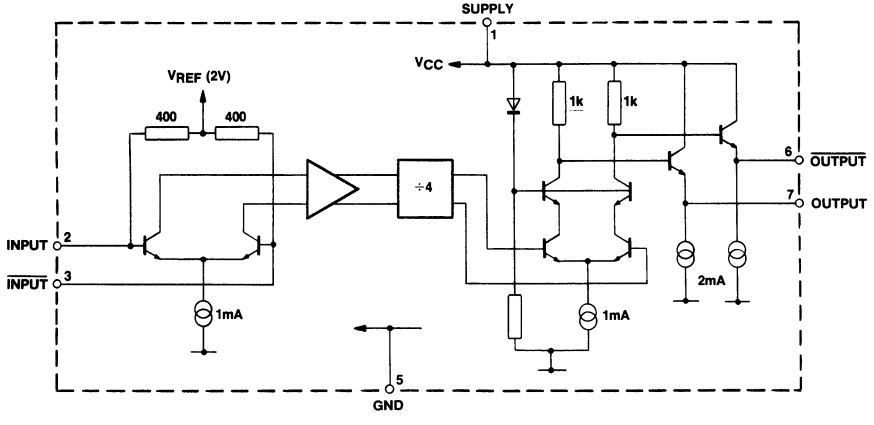


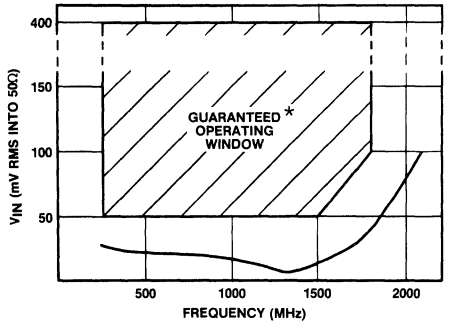
Fig.2 SP8824 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} = A Grade -55°C to +125°C, B Grade -40°C to +85°C, V_{CC} = +4.75V to +5.25V

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	1		38	48	mA	V_{CC} = 5V
Input sensitivity	2,3					RMS sinewave
200MHz to 1500MHz				50	mV	Measured in 50Ω
1800MHz				100	mV	system. See Figs. 3 & 4
Input impedance (series equivalent)	2,3		50		Ω	
			2		pF	
Output voltage with f_{in} = 250MHz	6,7	0.8	1		V p-p	V_{CC} = 5V
Output voltage with f_{in} = 1800MHz	6,7		0.15		V p-p	V_{CC} = 5V load as Fig.4



* Tested as specified in Table of Electrical Characteristics

Fig.3 Typical input sensitivity

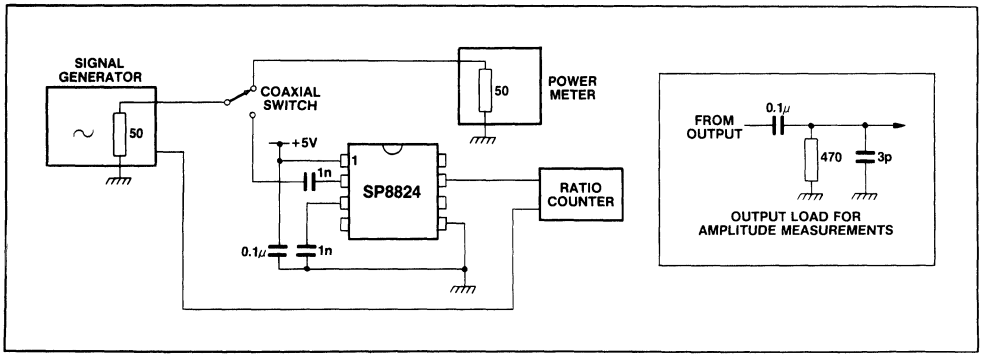


Fig.4 Test circuit

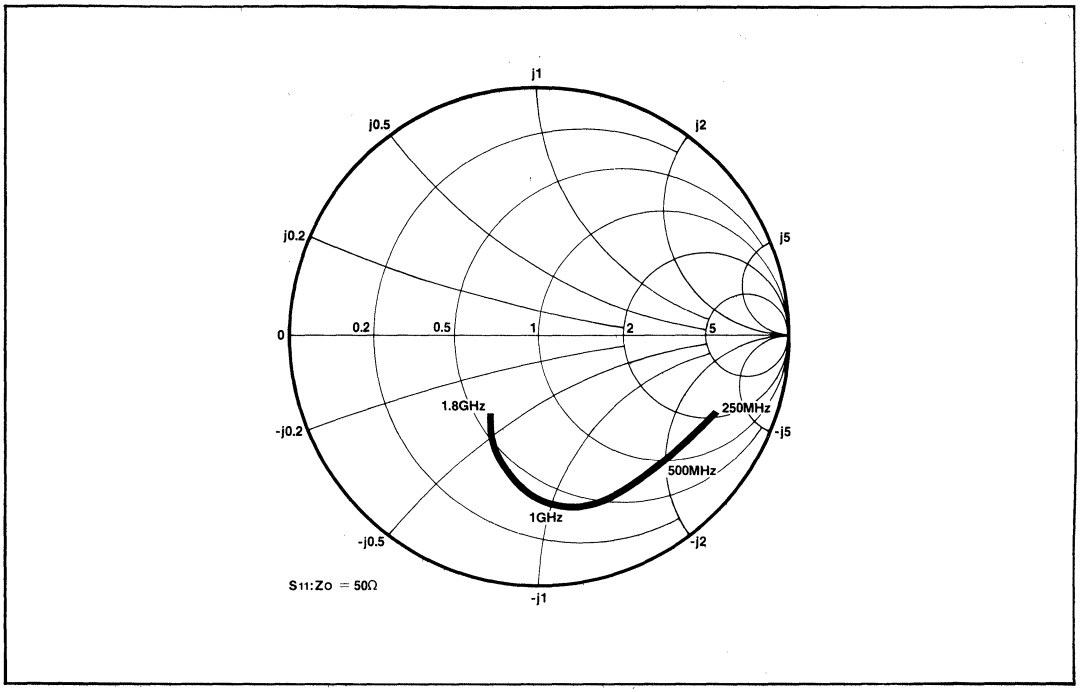


Fig.5 Typical input impedance

SP8828A & B

1.8GHz ÷ 8 FIXED MODULUS DIVIDER

The SP8828 is one of a range of very high speed low power prescalers for professional and military applications. The device features a complementary output stage with on chip current sources for the emitter follower outputs.

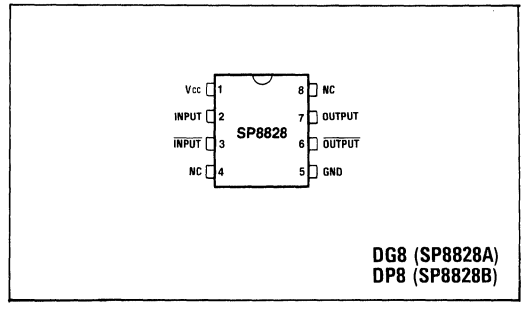


Fig.1 Pin connections - top view

FEATURES

- High Speed Operation 1.8GHz
- Silicon Technology for Low Phase Noise (Typically better than -140dBc/Hz at 10kHz
- Very Low Power Dissipation 175mW (Typ.)
- 5V Single Supply Operation
- High Input Sensitivity
- Very Wide Operating Frequency Range
- Temperature Range:
  -55°C to +125°C (A Grade)
  -40°C to +85°C (B Grade)

ABSOLUTE MAXIMUM RATINGS

Supply voltage Vcc	6.5V
Clock input voltage	2.5V p-p
Storage temperature range	-55°C to +150°C
Junction temperature	+175°C

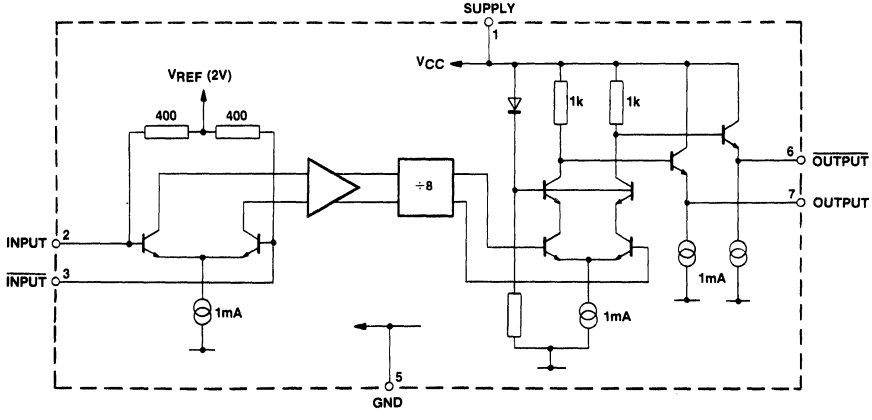


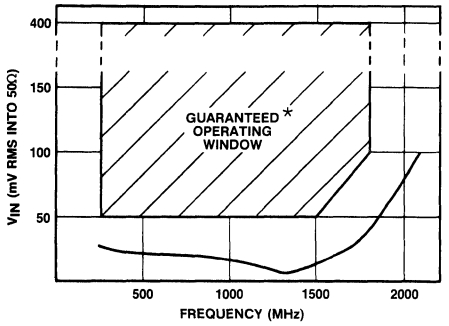
Fig.2 SP8828 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} = A Grade -55°C to +125°C, B Grade -40°C to +85°C, V_{CC} = +4.75V to +5.25V

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	1		35	45	mA	V_{CC} = 5V
Input sensitivity	2,3					RMS sinewave
200MHz to 1500MHz				50	mV	Measured in 50Ω
1800MHz				100	mV	system. See Figs. 3 & 4
Input impedance (series equivalent)	2,3		50		Ω	
			2		pF	
Output voltage with f_{in} = 250MHz	6,7	0.8	1		V p-p	V_{CC} = 5V
Output voltage with f_{in} = 1800MHz	6,7		0.15		V p-p	V_{CC} = 5V load as Fig.4



* Tested as specified in Table of Electrical Characteristics

Fig.3 Typical input sensitivity

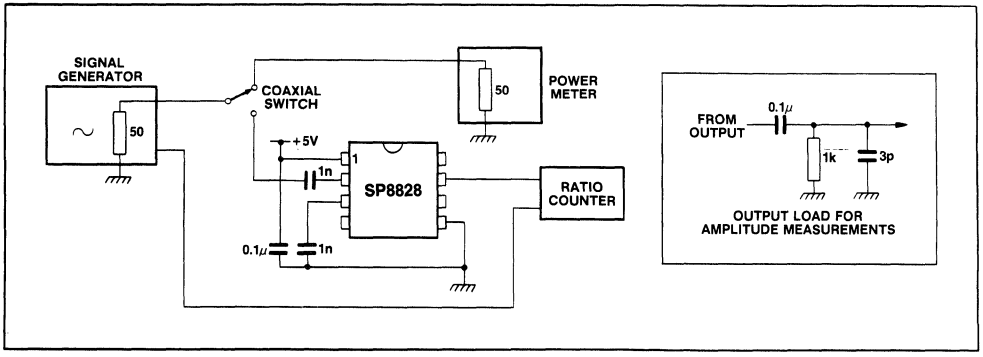


Fig.4 Test circuit

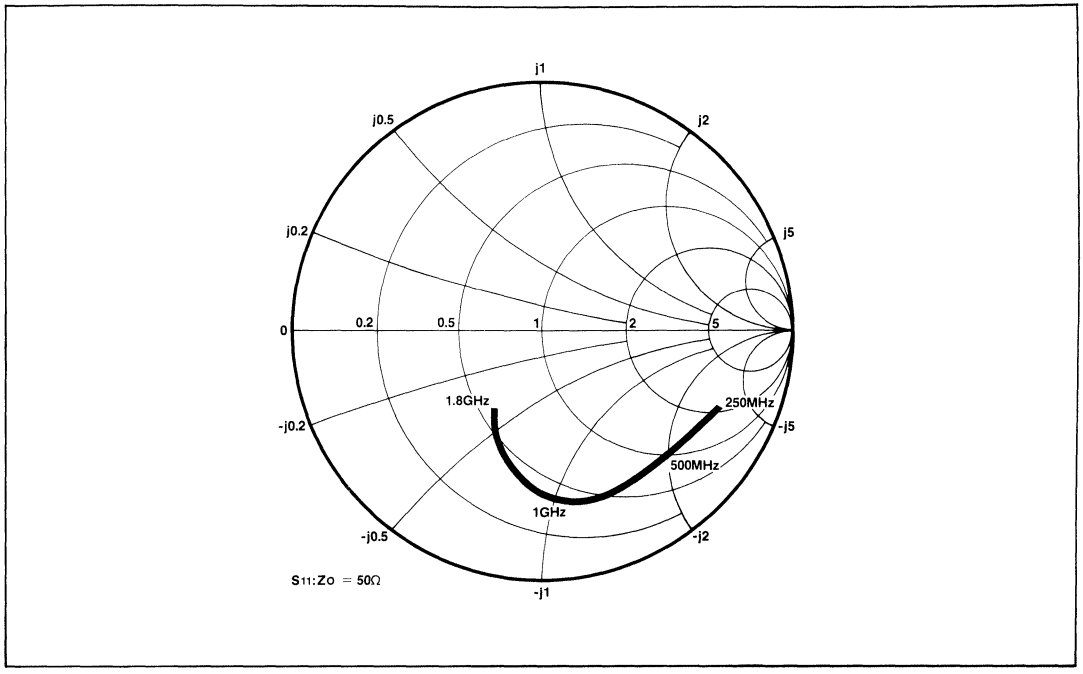


Fig.5 Typical input impedance

SP8830A & B

1.5GHz ÷ 10 FIXED MODULUS DIVIDER

The SP8830 is one of a range of very high speed low power prescalers for professional and military applications. The device features a complementary output stage with on chip current sources for the emitter follower outputs.

FEATURES

- High Speed Operation 1.5GHz
- Silicon Technology for Low Phase Noise (Typically better than -140dBc/Hz at 10kHz
- Very Low Power Dissipation 200mW (Typ.)
- 5V Single Supply Operation
- High Input Sensitivity
- Very Wide Operating Frequency Range
- Temperature Range:
  -55°C to +125°C (A Grade)
  -40°C to +85°C (B Grade)

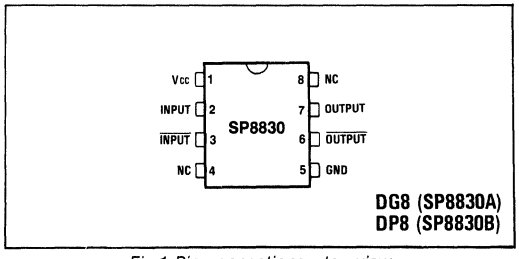


Fig.1 Pin connections - top view

ABSOLUTE MAXIMUM RATINGS

Supply voltage Vcc	6.5V
Clock input voltage	2.5V p-p
Storage temperature range	-55°C to +150°C
Junction temperature	+175°C

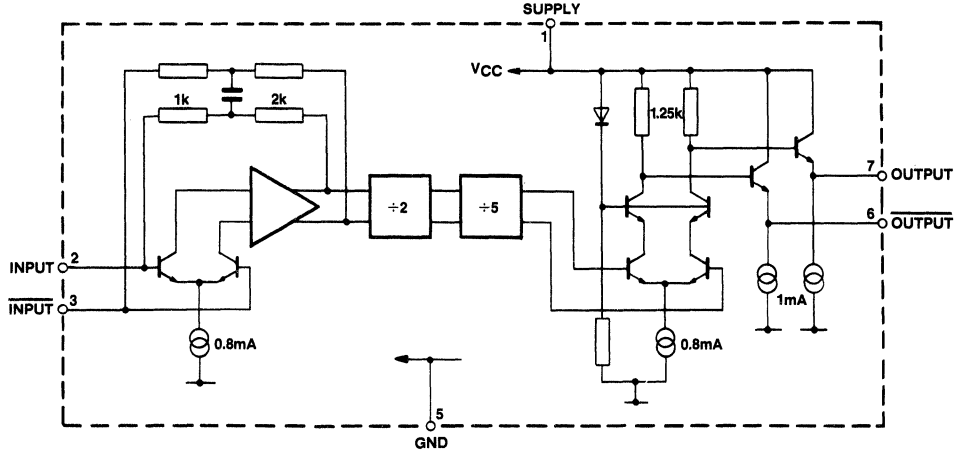


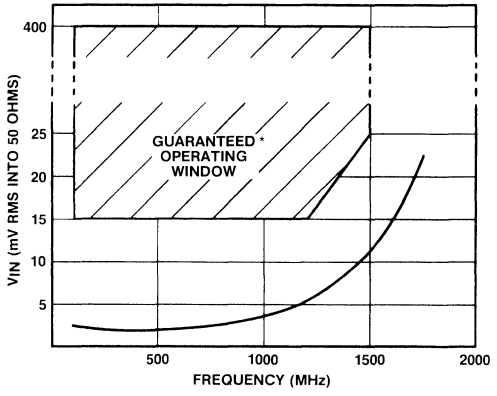
Fig.2 SP8830 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} = A Grade -55°C to +125°C, B Grade -40°C to +85°C, V_{CC} = +4.75V to +5.25V

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	1		40	50	mA	V_{CC} = 5V
Input sensitivity	2,3					RMS sinewave
100MHz to 1200MHz				15	mV	Measured in 50Ω
1.5GHz				25	mV	system. See Figs. 3 & 4
Input impedance (series equivalent)	2,3		50		Ω	
			2		pF	
Output voltage with f_{in} = 100MHz	6,7	0.8	1		V p-p	V_{CC} = 5V
Output voltage with f_{in} = 1500MHz	6,7		0.4		V p-p	V_{CC} = 5V load as Fig.4



*Tested as specified in table of Electrical Characteristics

Fig.3 Typical input sensitivity

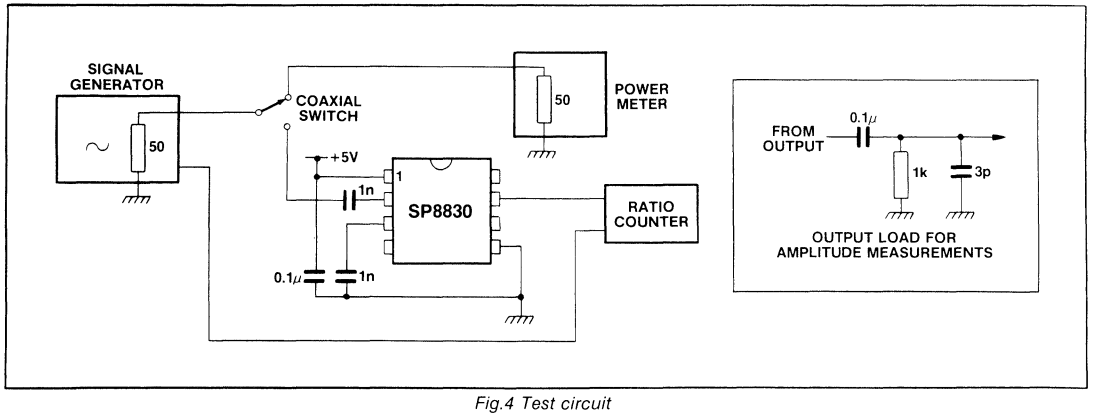


Fig.4 Test circuit

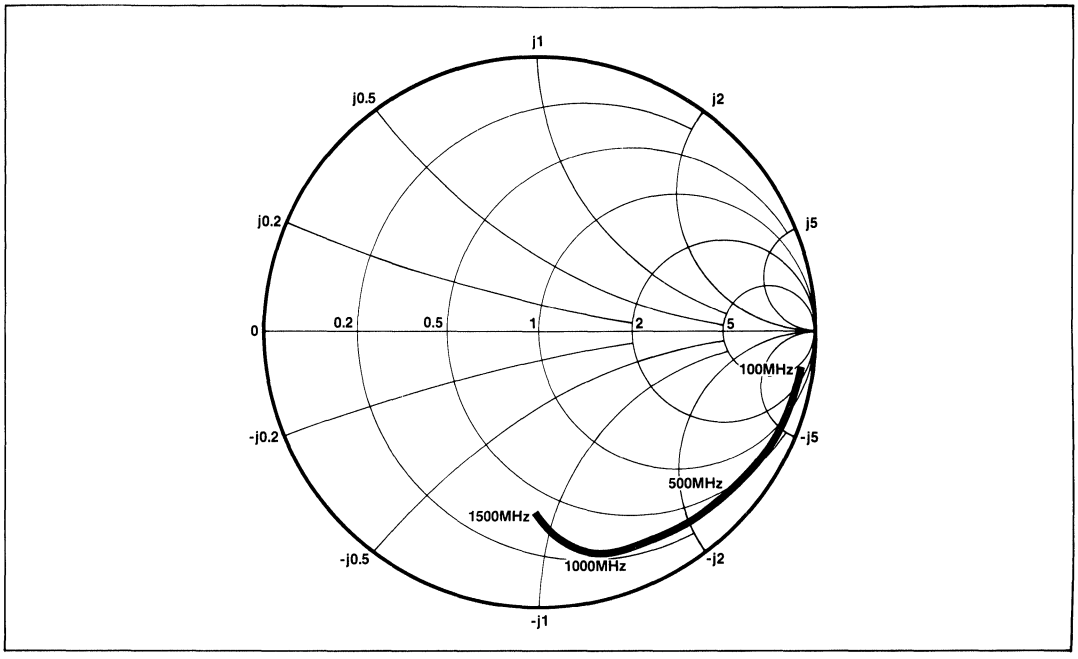


Fig.5 Typical input impedance

SP8832B

3.5GHz ÷ 2 FIXED MODULUS DIVIDER

The SP8832B is one of a range of very high speed low power prescalers for professional applications. The device features a complementary output stage with on chip current sources for the emitter follower outputs.

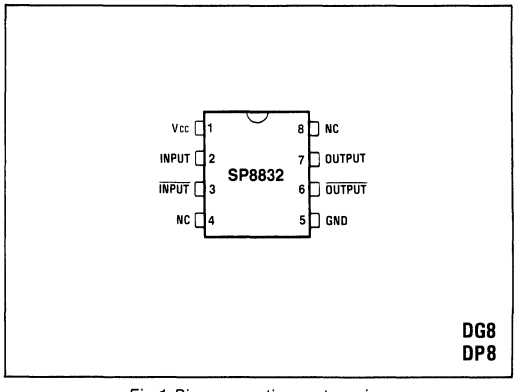


Fig.1 Pin connections - top view

FEATURES

- Very High Speed Operation 3.5GHz
- Silicon Technology for Low Phase Noise (Typically better than -140dBc/Hz at 10kHz
- Low Power Dissipation 420mW (Typ.)
- 5V Single Supply Operation
- High Input Sensitivity
- Very Wide Operating Frequency Range

ABSOLUTE MAXIMUM RATINGS

Supply voltage Vcc	6.5V
Clock input voltage	2.5V p-p
Storage temperature range	-55°C to +150°C
Junction temperature	+175°C

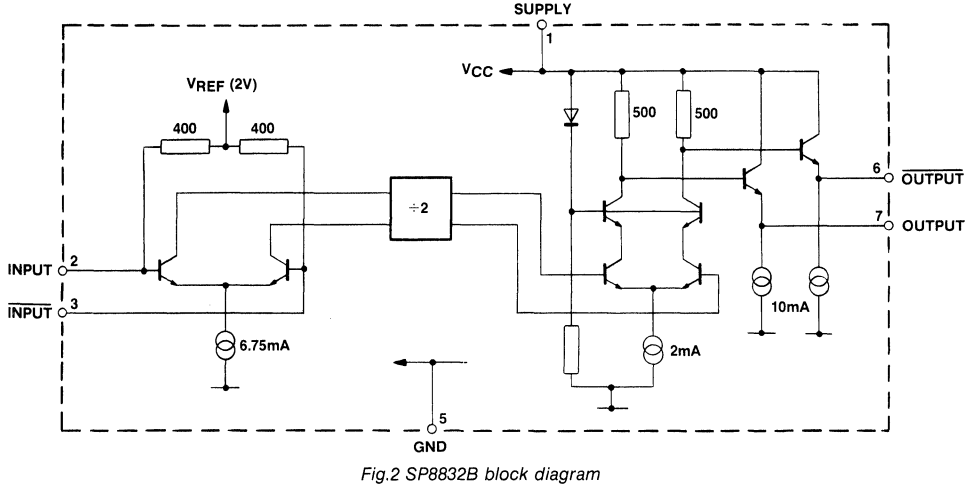
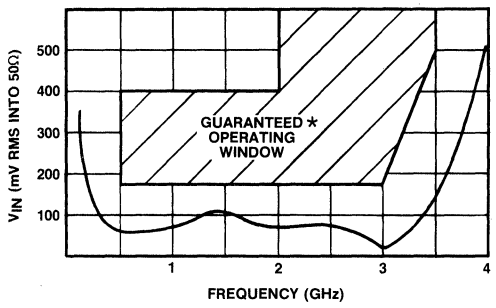


Fig.2 SP8832B block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = -40°C to +85°C, V_{CC} = +4.75V to +5.25V

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	1		84	100	mA	V_{CC} = 5V
Input sensitivity	2,3					RMS sinewave
0.5GHz to 2.8GHz				175	mV	Measured in 50Ω
3.5GHz				500	mV	system. See Figs. 3 & 4
Input impedance (series equivalent)	2,3		50		Ω	
			2		pF	
Output voltage with f_{in} = 1000MHz	6,7	0.8	1		V p-p	V_{CC} = 5V
Output voltage with f_{in} = 3GHz	6,7		0.35		V p-p	V_{CC} = 5V load as Fig.4



* Tested as specified in Table of Electrical Characteristics

Fig.3 Typical input sensitivity

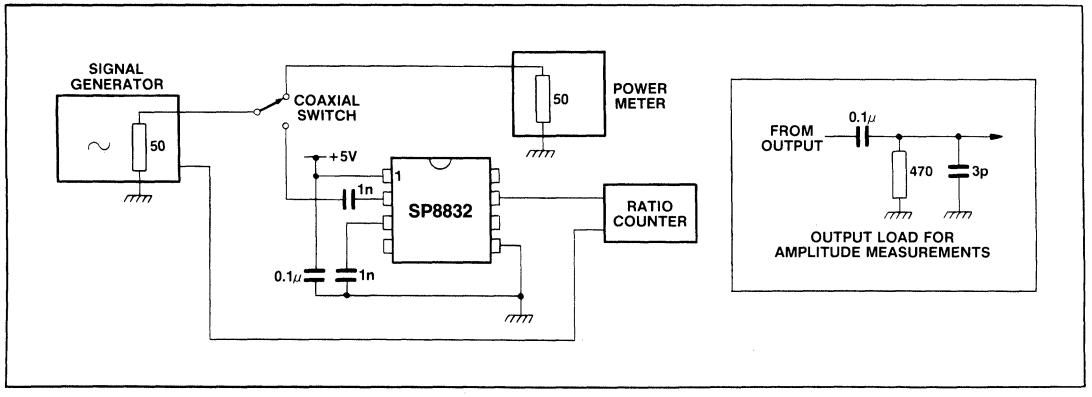


Fig.4 Test circuit

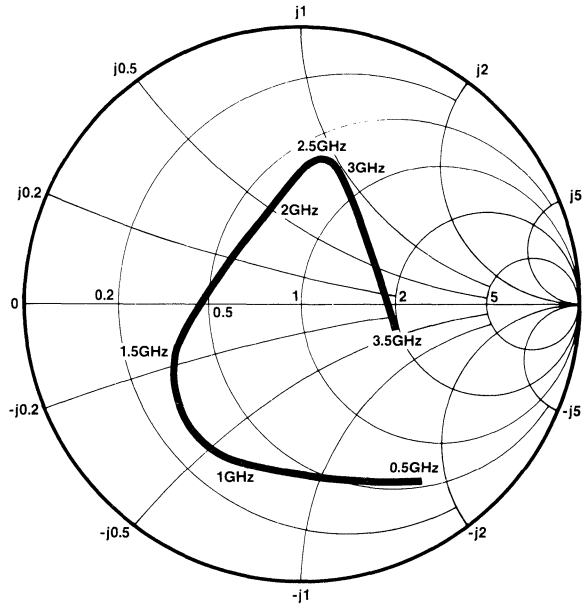


Fig.5 Typical input impedance

SP8835B

3.5GHz ÷ 4 FIXED MODULUS DIVIDER

The SP8835B is one of a range of very high speed low power prescalers for professional applications. The device features a complementary output stage with on chip current sources for the emitter follower outputs.

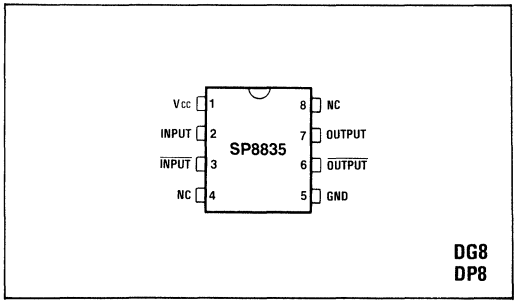


Fig.1 Pin connections - top view

FEATURES

- Very High Speed Operation 3.5GHz
- Silicon Technology for Low Phase Noise (Typically better than -140dBc/Hz at 10kHz
- Low Power Dissipation 370mW (Typ.)
- 5V Single Supply Operation
- High Input Sensitivity
- Very Wide Operating Frequency Range

ABSOLUTE MAXIMUM RATINGS

Supply voltage Vcc	6.5V
Clock input voltage	2.5V p-p
Storage temperature range	-55°C to +150°C
Junction temperature	+175°C

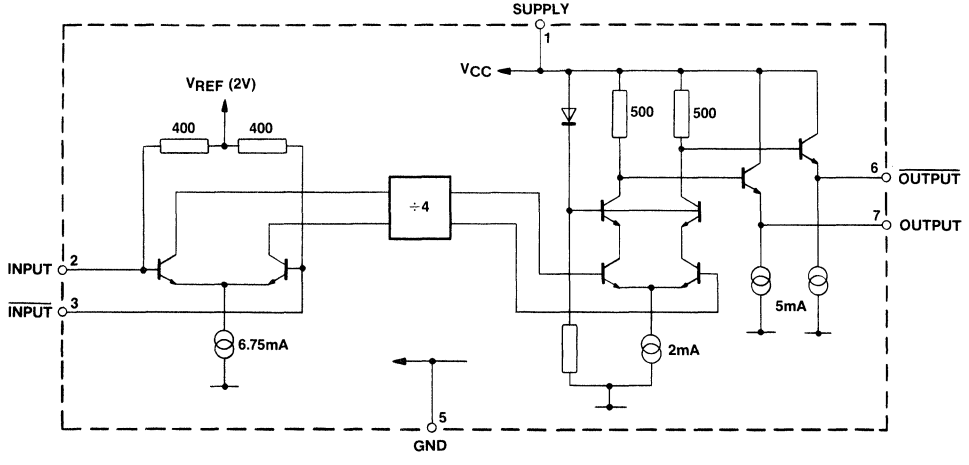
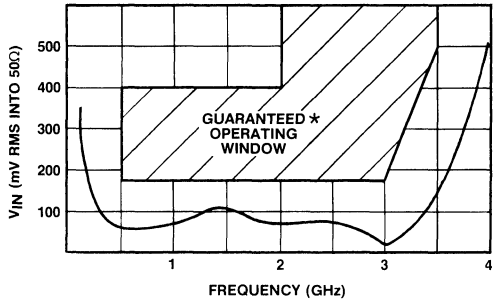


Fig.2 SP8834B block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = -40°C to +85°C, V_{CC} = +4.75V to +5.25V

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	1		74	90	mA	V_{CC} = 5V
Input sensitivity	2,3					RMS sinewave
0.5GHz to 2.8GHz				175	mV	Measured in 50Ω
3.5GHz				500	mV	system. See Figs. 3 & 4
Input impedance (series equivalent)	2,3		50		Ω	
			2		pF	
Output voltage with f_{in} = 1000MHz	6,7	0.8	1		V p-p	V_{CC} = 5V
Output voltage with f_{in} = 3GHz	6,7		0.25		V p-p	V_{CC} = 5V load as Fig.4



* Tested as specified in Table of Electrical Characteristics

Fig.3 Typical input sensitivity

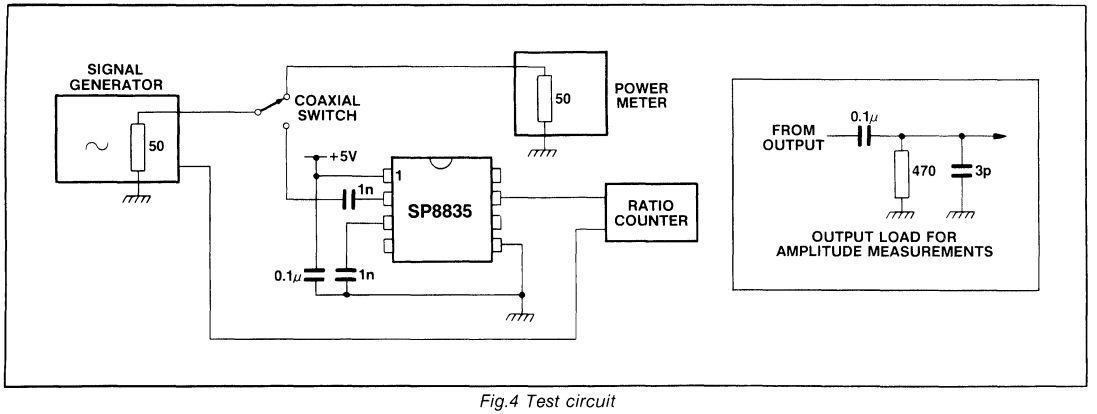


Fig.4 Test circuit

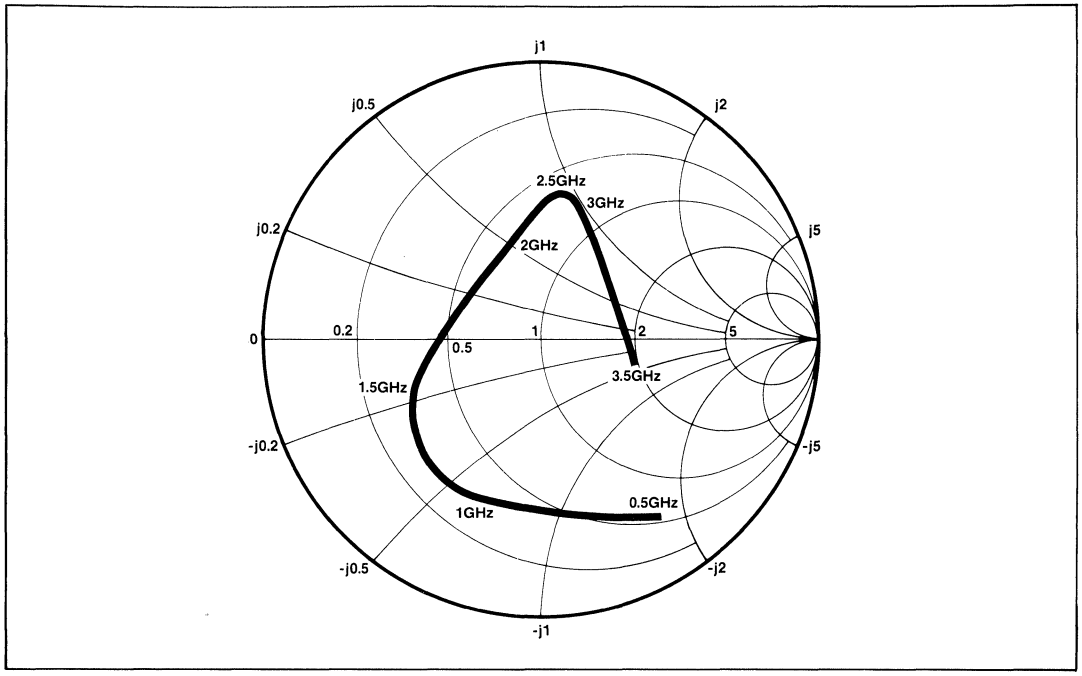


Fig.5 Typical input impedance

SP8838B

3.5GHz ÷ 8 FIXED MODULUS DIVIDER

The SP8838B is one of a range of very high speed low power prescalers for professional applications. The device features a complementary output stage with on chip current sources for the emitter follower outputs.

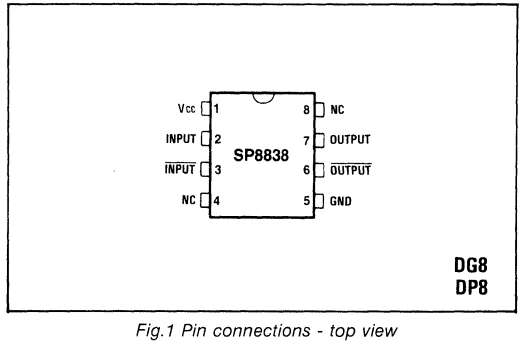


Fig.1 Pin connections - top view

FEATURES

- Very High Speed Operation 3.5GHz
- Silicon Technology for Low Phase Noise (Typically better than -140dBc/Hz at 10kHz
- Low Power Dissipation 345mW (Typ.)
- 5V Single Supply Operation
- High Input Sensitivity
- Very Wide Operating Frequency Range

ABSOLUTE MAXIMUM RATINGS

Supply voltage Vcc	6.5V
Clock input voltage	2.5V p-p
Storage temperature range	-55°C to +150°C
Junction temperature	+175°C

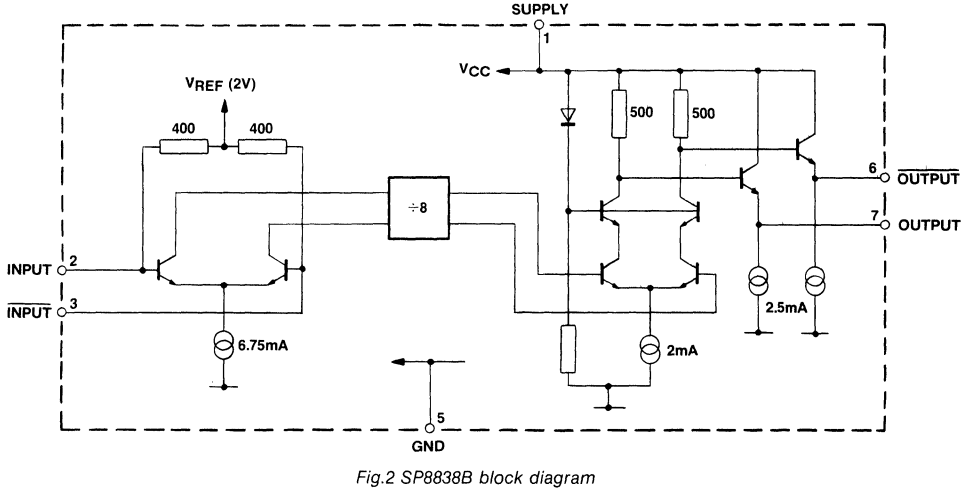


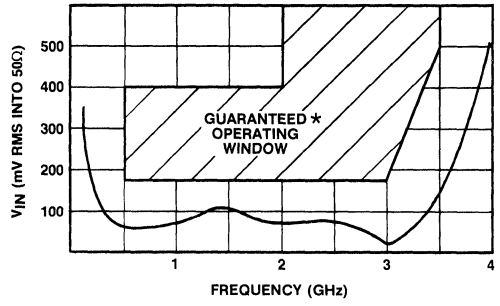
Fig.2 SP8838B block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} = -40°C to +85°C, V_{CC} = +4.75V to +5.25V

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	1		69	85	mA	V_{CC} = 5V
Input sensitivity	2,3					RMS sinewave
0.5GHz to 2.8GHz				175	mV	Measured in 50Ω
3.5GHz				500	mV	system. See Figs. 3 & 4
Input impedance (series equivalent)	2,3		50		Ω	
			2		pF	
Output voltage with f_{in} = 1000MHz	6,7	0.8	1		V p-p	V_{CC} = 5V
Output voltage with f_{in} = 3GHz	6,7		0.4		V p-p	V_{CC} = 5V load as Fig.4



* Tested as specified in Table of Electrical Characteristics

Fig.3 Typical input sensitivity

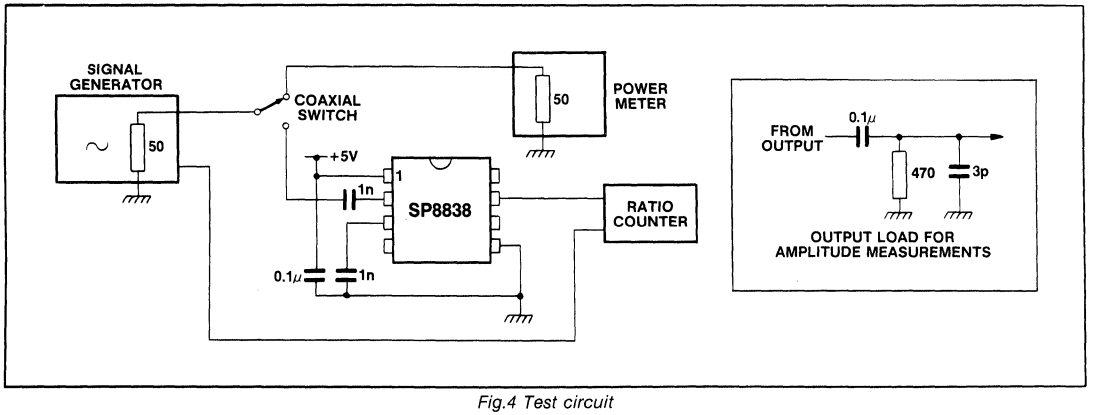


Fig.4 Test circuit

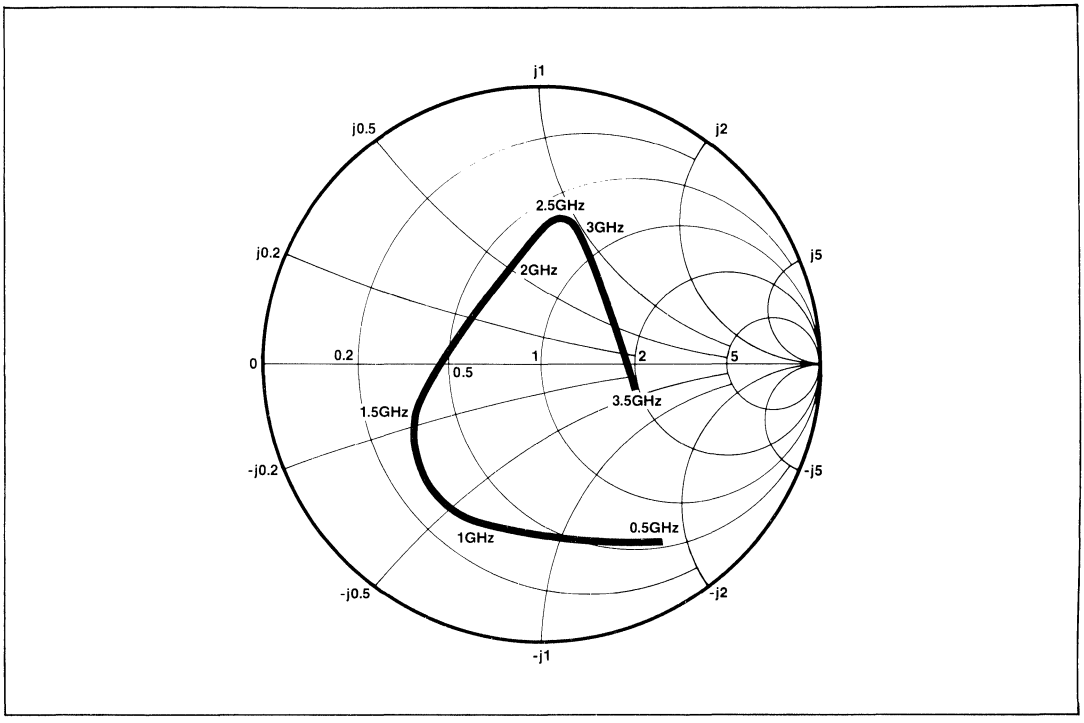


Fig.5 Typical input impedance

Technical Data

2. Frequency synthesisers

PLESSEY
Semiconductors

NJ8820, NJ8820B

FREQUENCY SYNTHESISER (PROM INTERFACE)

The NJ8820/NJ8820B is a synthesiser circuit fabricated on the Plessey 5-micron CMOS process and is capable of achieving high sideband attenuation and low noise performance. The circuit contains a reference oscillator, 11-bit programmable reference divider, digital and sample-and-hold phase comparators, 10-bit programmable 'M' counter, 7-bit programmable 'A' counter and the necessary control and latch circuitry for accepting and latching the input data.

Data is presented as eight 4-bit words read from an external memory with the necessary timing signals generated internally.

It is intended to be used in conjunction with a two-modulus prescaler such as the SP8710 series to produce a universal binary coded synthesiser.

The NJ8820 is available in Plastic DIL (DP) and Miniature Plastic DIL (MP) packages, both with operating temperature range of -30°C to +70°C. The NJ8820B is available only in Ceramic DIL package with operating temperature range of -40°C to +85°C.

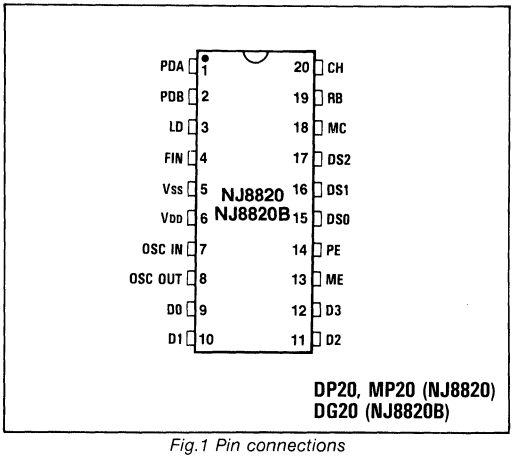


Fig.1 Pin connections

FEATURES

- Low Power Consumption
- Direct Interface to ROM or PROM
- High Performance Sample and Hold Phase Detector
- >10MHz Input Frequency

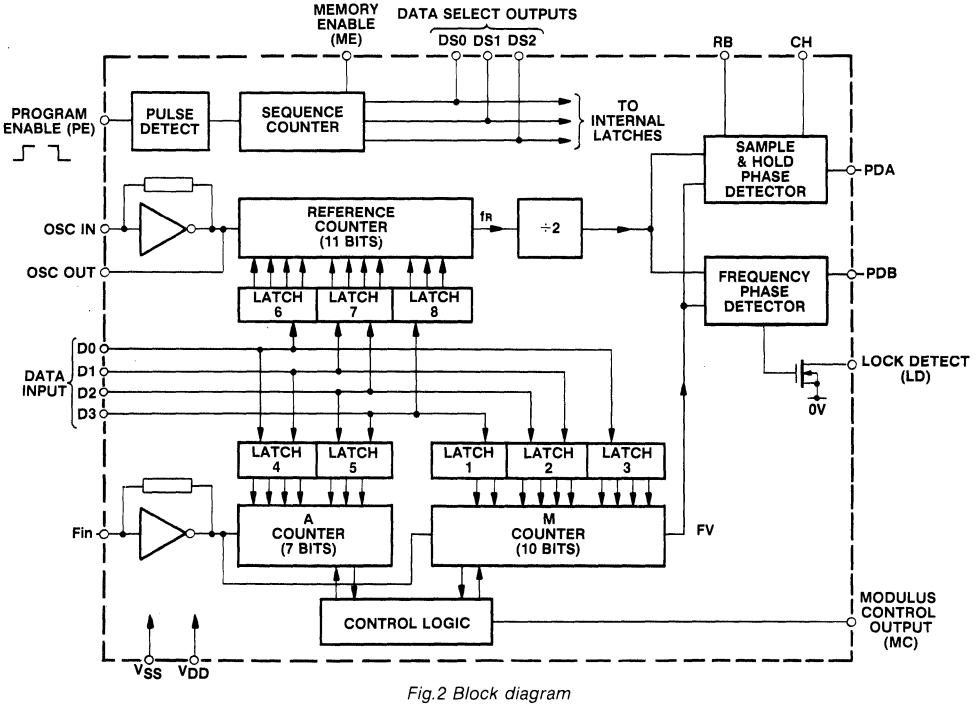


Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{DD}-V_{SS} 5V ± 0.5V, Temperature range NJ8820: -30°C to +70°C, NJ8820B: -40°C to +85°C

DC Characteristics at V_{DD} = 5V

Characteristics	Value Min.	Value Typ.	Value Max.	Units	Conditions
Supply current		3.5	5.5	mA	FOSC, FIN = 10MHz } 0 to 5V square wave
		0.7	1.5	mA	FOSC, FIN = 1.0MHz }
OUTPUT LEVELS					
ME output					
Low level			0.4	V	I_{sink} 4mA
Open drain pull-up voltage			8	V	
DS OUTPUTS					
High level	4.6			V	I_{source} 1mA
Low level			0.4	V	I_{sink} 2mA
MODULUS CONTROL OUT					
High level	4.6			V	I_{source} 1mA
Low level			0.4	V	I_{sink} 1mA
LOCK DETECT OUT					
Low level			0.4	V	I_{sink} 4mA
Open drain pull-up voltage			8	V	
PDB Output					
High level	4.6			V	I_{source} 5mA
Low level			0.4	V	I_{sink} 5mA
3-state leakage			±0.1	μA	
INPUT LEVELS					
Data Inputs					
High level	4.25			V	TTL compatible
Low level			0.75	V	See note 1
Program Enable Input (PE)					
Trigger level	V_{bias} ±100mV			V	V_{bias} = self bias point of PE (nominally V_{DD}/2)

AC Characteristics

Characteristics	Value Min.	Value Typ.	Value Max.	Units	Conditions
FIN/OSC inputs	200			mV RMS	10MHz AC coupled sinewave
Max. operating freq. OSC/FIN inputs	10.6			MHz	V_{DD} = 5V, Input squarewave V_{DD}-V_{SS} Note 5
Propagation delay, clock to modulus control		30	50	ns	Note 2
Program enable pulse length, t_W	5			μs	Pulse to V_{SS} or V_{DD}
Data set-up time, t_{SI}	1			μs	
Data hold time, t_{HI}	10			ns	
Digital phase detector propagation delay		500		ns	
Gain programming resistor, RB	5			kΩ	See Fig.7
Hold capacitor, CH			1	nF	Note 3
Output resistance PDA			5	kΩ	
Digital phase detector gain		1		V/Rad	
Power supply rise time	100			μs	10 % to 90 %. Note 4

NOTES
1. Data inputs have internal 'pull-up' resistors to enable them to be driven from TTL outputs. 2. All counters have outputs directly synchronous with their respective clock rising edges. 3. Finite output resistance of internal voltage follower and 'on' resistance of sample switch driving this pin will add a finite time-constant to the loop. A 1nF hold capacitor will give a maximum time-constant of 5 microseconds. 4. To ensure correct operation of power-on programming. 5. Operation at up to 15MHz is possible with a full logic swing but is not guaranteed.

PIN DESIGNATION

Pin No.	Name	Description
1	PDA	Analog output from the sample and hold phase comparator for use as a 'fine' error signal. Output at (V_{DD}-V_{SS})/2 when in lock. Voltage increases as FV phase lead increases and decreases as FR phase lead increases. Output is linear over only a narrow phase window determined by gain programmed by RB.
2	PDB	Three-state output from the phase/frequency detector for use as a 'coarse' error signal. FV > FR or FV leading: positive pulses FV < FR or FR leading: negative pulses FV = FR and phase error within PDA window: high impedance
3	LD	An open drain lock detect output at low level when phase error within PDA window (in lock). High impedance at all other times.
4	FIN	The input to the main counters normally driven from a prescaler which may be AC coupled or when a full logic swing is available may be DC coupled.
5	V_{SS}	Negative supply (normally ground)
6	V_{DD}	Positive supply
7,8	OSC.IN/ OSC.OUT	These pins form an on-chip reference oscillator when a parallel resonant crystal is connected across them. Capacitors of an appropriate value are also required between each end of the crystal and ground to provide the necessary additional phase shift. An external crystal-generated reference signal may alternatively be applied to OSC.IN. This may be a low-level signal AC coupled into OSC.IN or if a full logic swing is available it may be DC coupled. The program range of the reference counter is 6-4094 in steps of 2, with the division ratio being twice the programmed number.
9,10,11,12	D0-D3	Information on these inputs is transferred to the internal latches during the appropriate data read time slot. D3 MSB, D0 LSB.
13	ME	An open-drain output for use in controlling the power supply to an external ROM or PROM. This output is low during the data read period and high impedance at other times.
14	PE	A positive or negative pulse or edge AC coupled into this pin initiates the single-shot data read procedure. Grounding this pin repeats the data read procedure in a cyclic manner.
15,16,17	DS0-DS2	Internally generated three-state data select outputs which may be used to address external memory.
18	MC	Signal for controlling an external dual-modulus prescaler. The modulus control level will be low at the beginning of a count cycle and will remain low until the 'A' counter completes its cycle. The modulus control then goes high and remains high until the 'M' counter completes its cycle at which point both counters are reset. This gives a total division ratio of M.N +A where N and N +1 represent the dual modulus prescale values. The program range of the 'A' counter is 0-127 and therefore can control prescalers with a division ratio up to and including ÷128/129. The program range of the 'M' counter is 3-1023 and for correct program operation M ≥A. Where every possible channel is required, the minimum division ratio should be N^2-N.
19	RB	An external sample and hold phase comparator gain programming resistor should be connected between this pin and V_{SS}.
20	CH	An external hold capacitor should be connected between this pin and V_{SS}.

ABSOLUTE MAXIMUM RATINGS

Supply voltage (V_{DD} - V_{SS})	-0.5V to 7V
Input voltage	
Open drain O/Ps (pins 3 and 13)	7V
All other pins	V_{SS} -0.3V to V_{DD} +0.3V
Storage temperature	-65°C to +150°C (DG package, NJ8820B)
Storage temperature	-55°C to +125°C (DP and MP packages, NJ8820)

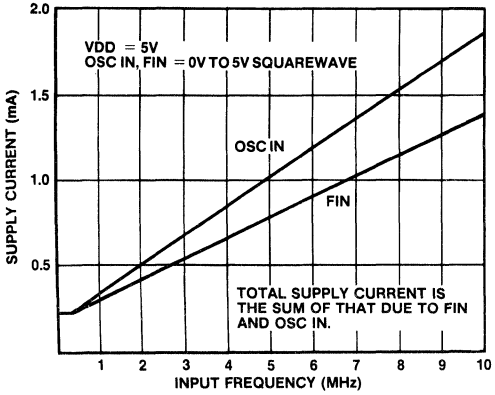


Fig.3 Typical supply current versus input frequency

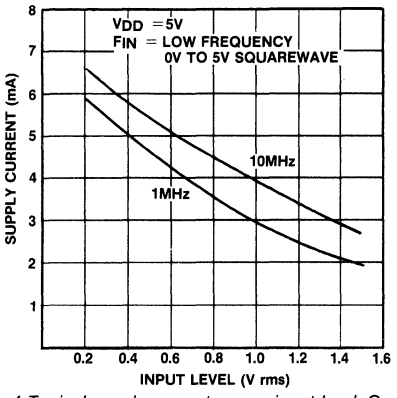


Fig.4 Typical supply current versus input level, Osc In

PROGRAMMING

Program information can be obtained from an external ROM or PROM under control of the NJ8820/NJ8820B. Twenty-eight data bits are required per channel arranged as eight 4-bit words leaving four redundant bits, two of which are available on the data bus driving the data-transfer time slot and may be used for external control purposes. A suitable PROM may be the 74S287 giving up to 32 channel capability as shown in Fig.5. Note that the choice of PNP transistor and supply bypass capacitor on the ROM should be such that the ROM will power up in time: for example, at 10MHz oscillator frequency, the ROM must be powered up in less than 25μs.

Reading of this data is normally done in a single shot mode with the data read cycle started by either a positive or negative pulse on the program enable pin. The data read cycle is generated from a program clock at 1/64th of the reference oscillator frequency. A memory enable signal is supplied to allow power-down of the memory when not in use. Data select outputs remain in a high-impedance state when the program cycle is completed to allow the address bus to be used for other functions if desired. The data map, data read cycle and timing diagram appears as Figs. 6 to 8. Data is latched internally during the shaded portions of the program cycle and all data is transferred to the counters and latched during the data transfer time slot.

Alternatively, the PE pin may be grounded causing the data read cycle to repeat in a cyclic manner to allow continuous up-dating of the program information. In this mode external memory will be enabled continuously, (ME low) and the data read cycle will repeat every sixteen cycles of the internal program clock, i.e. every 1024/fosc seconds. This programming method is not recommended because the higher power consumption and the possibilities of noise injection into the loop from the digital data lines.

Power-on programming On power-up the data read cycle is automatically initiated making it unnecessary to provide a PE pulse on power-up. The circuit detects the power supply rising above a threshold point, (nominally 1.5V) and after an internally generated delay to allow the supply to rise fully the circuit is programmed in the normal way. This delay is generated by counting reference oscillator pulses and is therefore dependent on the crystal used. The delay consists of 53248 reference oscillator cycles giving a delay of about 5ms at 10MHz.

To ensure correct operation of this function the power supply rise time should be less than 5ms, (at 10MHz) rising smoothly through the threshold point.

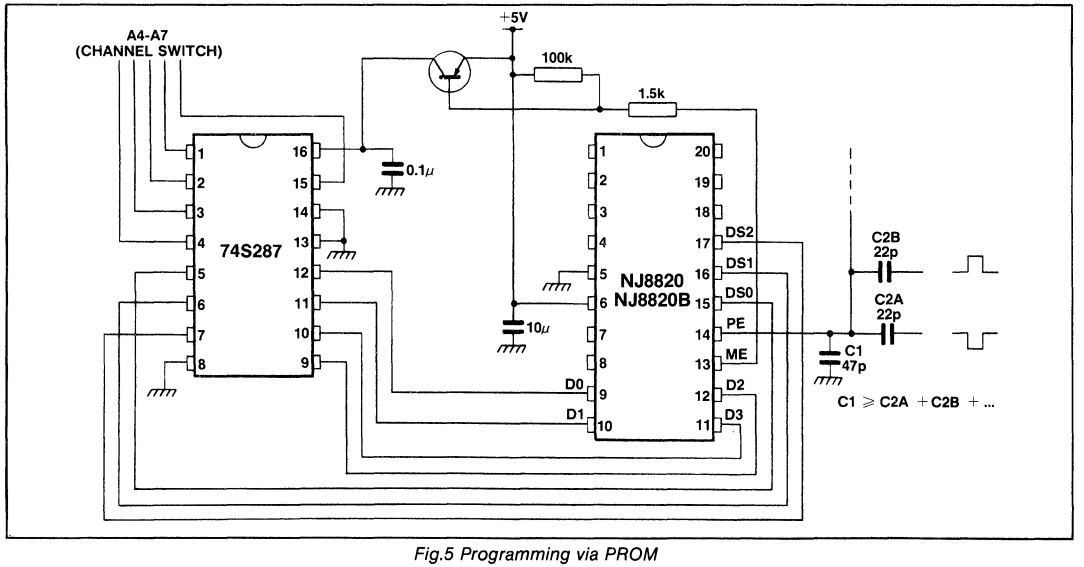


Fig.5 Programming via PROM

WORD	DS2	DS1	DS0	D3	D2	D1	D0
1	0	0	0	M1	M0	-	-
2	0	0	1	M5	M4	M3	M2
3	0	1	0	M9	M8	M7	M6
4	0	1	1	A3	A2	A1	A0
5	1	0	0	-	A6	A5	A4
6	1	0	1	R3	R2	R1	R0
7	1	1	0	R7	R6	R5	R4
8	1	1	1	-	R10	R9	R8

Fig.6 Data map

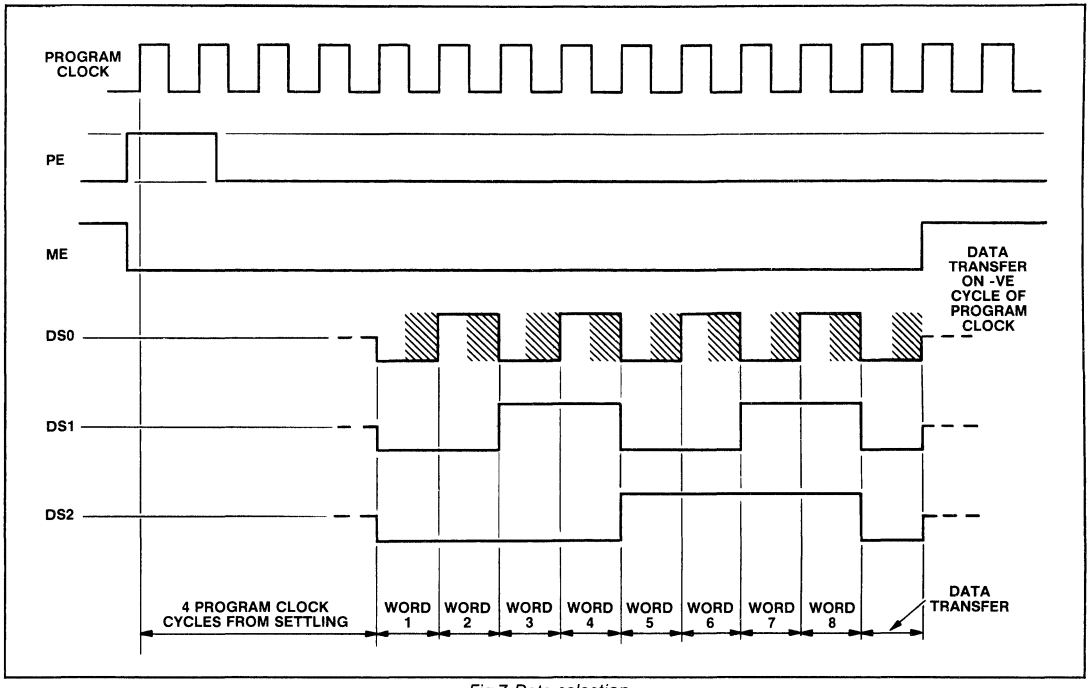


Fig.7 Data selection

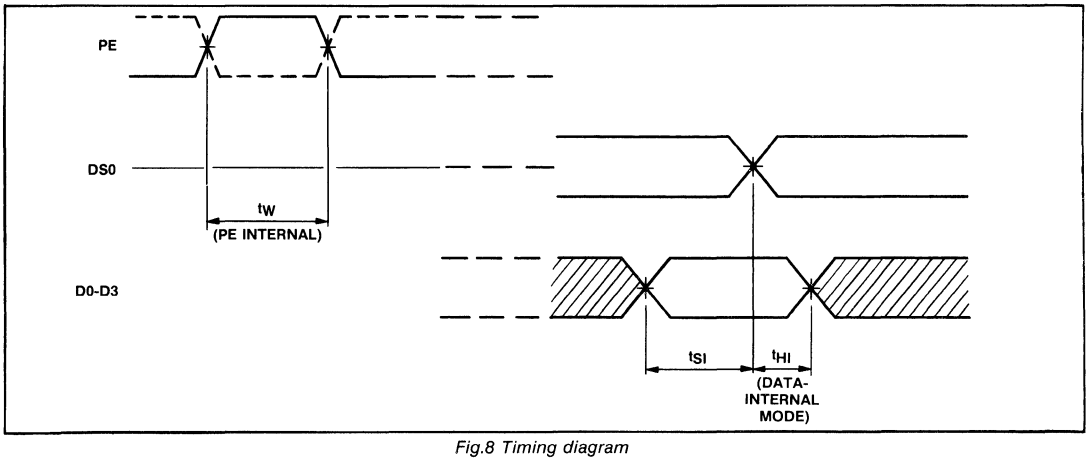


Fig.8 Timing diagram

PHASE COMPARATORS

A standard digital phase/frequency detector driving a three-state output provides a 'coarse' error signal to enable fast switching between channels. This output is active until the phase error is within the sample and hold phase detector window, when its output becomes high impedance. Phase-lock is indicated at this point with a low level on LD. The sample and hold phase detector provides a 'fine' error signal to give further phase adjustment and to hold the loop in lock.

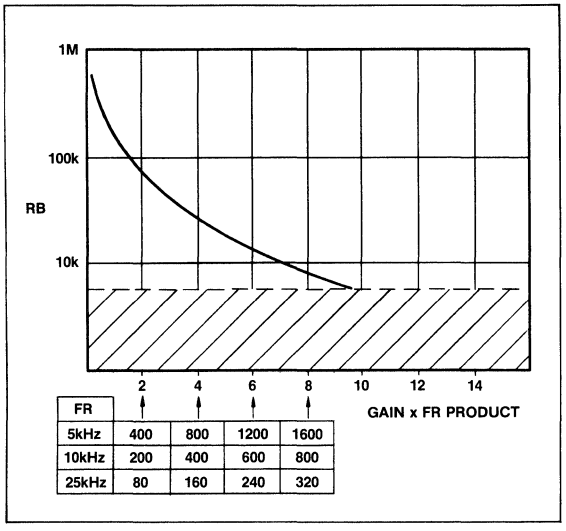
An internally generated ramp controlled by the digital output from both the reference and main divider chains is sampled at the reference frequency to give the fine error signal, PDA. When in phase lock this output would typically be at $(V_{DD}-V_{SS})/2$ and any offset from this would be proportional to phase error. The relationship between this offset voltage and the phase error is the phase-comparator gain which is programmable with an external resistor, RB. An internal 50pF capacitor is used in the sample and hold comparator.

This gain is typically:

$$\text{GAIN} = \frac{10\,[V_{DD}-V_{SS}-0.7-89(RB^{-½})]}{2 \times \pi \times 50\times10^{-12} \times RB \times FR}$$

The value of RB should be chosen to give the required gain at the reference frequency used. Fig.9 for example shows that to achieve a gain of 380V per radian at 10kHz requires approximately 39kΩ. A second external component is required; this is a hold capacitor of non-critical value which might typically be 470pF, a smaller value being sufficient if the sideband performance required is not high. Fig.9 shows the gain normalised to a 1Hz comparison frequency; to obtain the value for any other frequency, divide the value of gain frequency product by the desired frequency.

The output from these phase detectors should be combined and filtered to generate a single control voltage to drive the VCO as in Fig.8.



FR				
5kHz	400	800	1200	1600
10kHz	200	400	600	800
25kHz	80	160	240	320

Fig.9 RB versus gain and reference frequency

CRYSTAL OSCILLATOR

When using the internal oscillator, the stability may be enhanced at high frequencies by the use of an external resistor between Pin 8 and the other components. A value of 150-270Ω is advised.

PROGRAMMING/POWER UP

All data and signal input pins should have no input applied to them prior to the application of V_{DD}, as otherwise 'latch up' may occur.

APPLICATION EXAMPLE

An application example for a synthesiser for operation up to 520MHz is given in Fig.10. This gives up to 32 channels with a maximum supply current of 17mA, (typically 12mA) at 520MHz excluding the VCO. With careful construction the circuit is capable of providing sideband attenuation in excess of 90dB with lock-times of only a few milliseconds for a 1MHz frequency step.

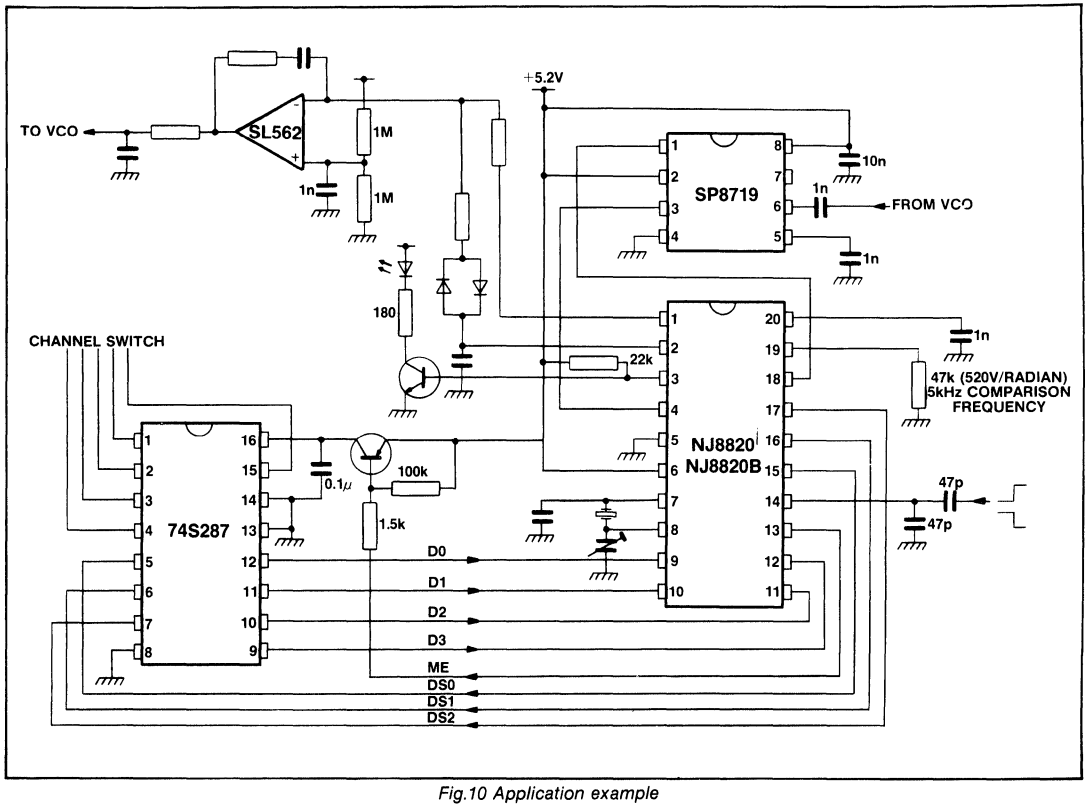


Fig.10 Application example

PLESSEY
Semiconductors

NJ8821, NJ8821B

FREQUENCY SYNTHESISER (MICROPROCESSOR INTERFACE) WITH RESETTABLE COUNTERS

The NJ8821/NJ8821B is a synthesiser circuit fabricated on the Plessey 5-micron CMOS process and is capable of achieving high sideband attenuation and low noise performance. The circuit contains a reference oscillator, 11-bit programmable reference divider, digital and sample-and-hold phase comparators, 10-bit programmable 'M' counter, 7-bit programmable 'A' counter and the necessary control and latch circuitry for accepting and latching the input data.

Data is presented as eight 4-bit words under external control from a suitable microprocessor.

It is intended to be used in conjunction with a two-modulus prescaler such as the SP8710 series to produce a universal binary coded synthesiser.

The NJ8821 is available in Plastic DIL (DP) and Miniature Plastic DIL (MP) packages, both with operating temperature range of -30°C to +70°C. The NJ8821B is available only in Ceramic DIL package with operating temperature range of -40°C to +85°C.

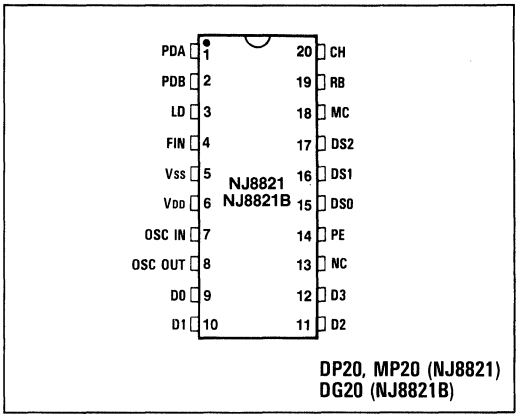


Fig.1 Pin connections

FEATURES

- Low Power Consumption
- High Performance Sample and Hold Phase Detector
- Microprocessor Compatible
- >10MHz Input Frequency

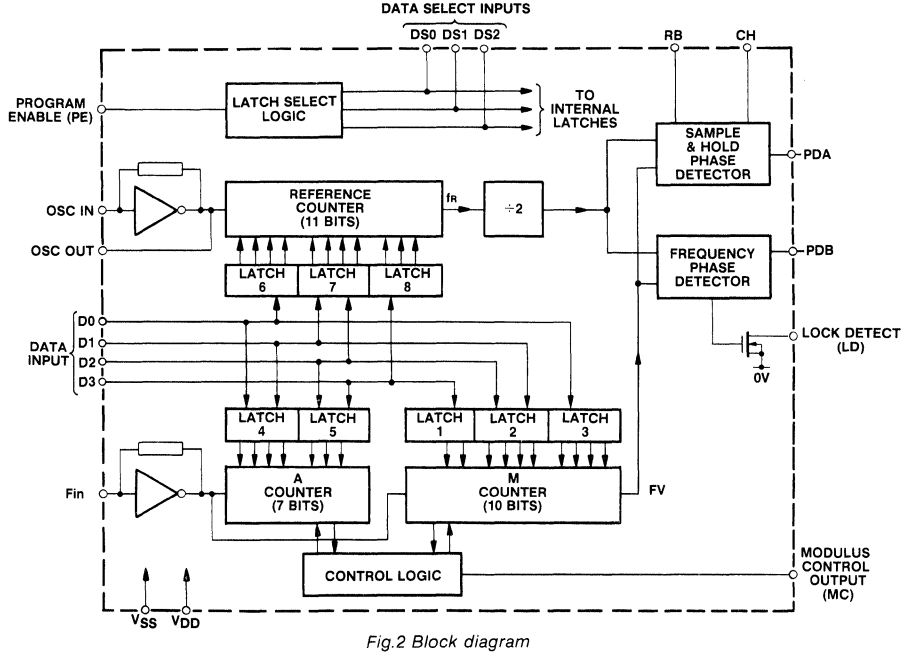


Fig.2 Block diagram

ELECTRICAL CONDITIONS

Test conditions (unless otherwise stated):

V_{DD}-V_{SS} 5V ± 0.5V

Temperature range NJ8821: -30°C to +70°C, NJ8821B: -40°C to +85°C

DC Characteristics at V_{DD} = 5V

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		3.5	5.5	mA	FOSC, FIN = 10MHz } 0 to 5V square wave
		0.7	1.5	mA	FOSC, FIN = 1.0MHz }
MODULUS CONTROL OUT					
High level	4.6			V	I_{source} 1mA
Low level			0.4	V	I_{sink} 1mA
LOCK DETECT OUT					
Low level			0.4	V	I_{sink} 4mA
Open drain pull-up voltage			8	V	
PDB Output					
High level	4.6			V	I_{source} 5mA
Low level			0.4	V	I_{sink} 5mA
3-state leakage			±0.1	μA	
INPUT LEVELS					
Data Inputs					
High level	4.25			V	TTL compatible
Low level			0.75	V	See note 1
Program Enable Input					
High level	4.25			V	
Low level			0.75	V	
DS INPUTS					
High level	4.25			V	
Low level			0.75	V	

AC Characteristics

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
FIN/OSC inputs	200			mV RMS	10MHz AC coupled sinewave
Max. operating freq. OSC/FIN inputs	10.6			MHz	V_{DD} = 5V, Input squarewave V_{DD}-Vss.Note 4
Propagation delay, clock to modulus control		30	50	ns	Note 2
Strobe pulse width external mode, $t_{w(ST)}$	2			μs	
Data set-up time, $t_{s(DATA)}$	1			μs	
Data hold time, $t_{H(DATA)}$	1			μs	
Address set-up time, t_{SE}	1			μs	
Address hold time, t_{HE}	1			μs	
Digital phase detector propagation delay		500		ns	
Gain programming resistor, RB	5			kΩ	See Fig.6
Hold capacitor, CH			1	nF	Note 3
Output resistance PDA			5	kΩ	
Digital phase detector gain		1		V/Rad	

NOTES

1. Data inputs have internal 'pull-up' resistors to enable them to be driven from TTL outputs.
2. All counters have outputs directly synchronous with their respective clock rising edges.
3. Finite output resistance of internal voltage follower and 'on' resistance of sample switch driving this pin will add a finite time-constant to the loop. A 1nF hold capacitor will give a maximum time-constant of 5 microseconds.
4. Operation at up to 15MHz is possible with a full logic swing but is not guaranteed.

PIN DESIGNATION

Pin No.	Name	Description
1	PDA	Analog output from the sample and hold phase comparator for use as a 'fine' error signal. Output at (V_{DD}-V_{SS})/2 when in lock. Voltage increases as FV phase lead increases and decreases as FR phase lead increases. Output is linear over only a narrow phase window determined by gain programmed by RB.
2	PDB	Three-state output from the phase/frequency detector for use as a 'coarse' error signal. FV > FR or FV leading: positive pulses FV < FR or FR leading: negative pulses FV = FR and phase error within PDA window: high impedance
3	LD	An open drain lock detect output at low level when phase error within PDA window (in lock). High impedance at all other times.
4	FIN	The input to the main counters normally driven from a prescaler which may be AC coupled or when a full logic swing is available may be DC coupled.
5	V_{SS}	Negative supply (normally ground)
6	V_{DD}	Positive supply
7,8	OSC.IN/ OSC.OUT	These pins form an on-chip reference oscillator when a parallel resonant crystal is connected across them. Capacitors of an appropriate value are also required between each end of the crystal and ground to provide the necessary additional phase shift. An external crystal-generated reference signal may alternatively be applied to OSC.IN. This may be a low-level signal AC coupled into OSC.IN or if a full logic swing is available it may be DC coupled. The program range of the reference counter is 6-4094 in steps of 2, with the division ratio being twice the programmed number.
9,10,11,12	D0-D3	Information on these inputs is transferred to the internal latches during the appropriate data read time slot. D3 MSB, D0 LSB.
14	PE	This pin is used as a strobe for the data. A logic high on this pin transfers data from the data pins to the internal latch selected by the address, (data select) lines, while a logic zero disables the data lines.
15,16,17	DS0-DS2	Data-select inputs to control the addressing of data latches.
18	MC	Signal for controlling an external dual-modulus prescaler. The modulus control level will be low at the beginning of a count cycle and will remain low until the 'A' counter completes its cycle. The modulus control then goes high and remains high until the 'M' counter completes its cycle at which point both counters are reset. This gives a total division ratio of M.N +A where N and N +1 represent the dual modulus prescale values. The program range of the 'A' counter is 0-127 and therefore can control prescalers with a division ratio up to and including ÷128/129. The program range of the 'M' counter is 3-1023 and for correct program operation M ≥A. Where every possible channel is required, the minimum division ratio should be N^2-N.
19	RB	An external sample and hold phase comparator gain programming resistor should be connected between this pin and V_{SS}.
20	CH	An external hold capacitor should be connected between this pin and V_{SS}.

ABSOLUTE MAXIMUM RATINGS

Supply voltage (V_{DD} - V_{SS})	-0.5V to 7V
Input voltage	
Open drain O/P (pin 3)	7V
All other pins	V_{SS} -0.3V to V_{DD} +0.3V
Storage temperature	-65°C to +150°C (DG Package, NJ8821B)
Storage temperature	-55°C to +125°C (DP and MP packages, NJ8821)

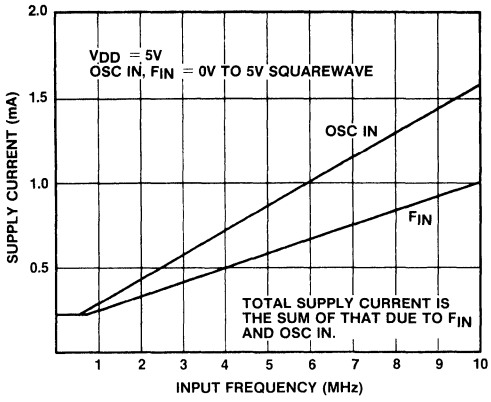


Fig.3 Typical supply current versus input frequency

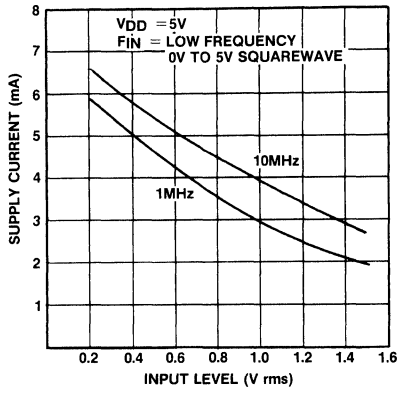


Fig.4 Typical supply current versus input level, Osc In

PROGRAMMING

Timing is generated externally, normally from a microprocessor, and allows the user to change the data in selected latches. The data map is Fig.5 with the PE pin used as a strobe for the data. Taking the PE pin high will transfer data from the data pins into the selected latch and taking this pin low will disable the data pins, retaining that data on the selected latch. Data transfer from all internal latches into the counters will occur simultaneously with the transfer of data into latch 1 and therefore this would normally be the final latch addressed during each channel change. Timing information for this mode of operation is given in Fig.6.

When re-programming, a reset to zero state is followed by reloading with the new counter values. This means the synthesiser loop lock up time will be well defined and less than 10msec. If shorter lock up times are required, when making only small changes in frequency, the non-resettable version NJ8823 should be considered.

WORD	DS2	DS1	DS0	D3	D2	D1	D0
1	0	0	0	M1	M0	-	-
2	0	0	1	M5	M4	M3	M2
3	0	1	0	M9	M8	M7	M6
4	0	1	1	A3	A2	A1	A0
5	1	0	0	-	A6	A5	A4
6	1	0	1	R3	R2	R1	R0
7	1	1	0	R7	R6	R5	R4
8	1	1	1	-	R10	R9	R8

Fig.5 Data map

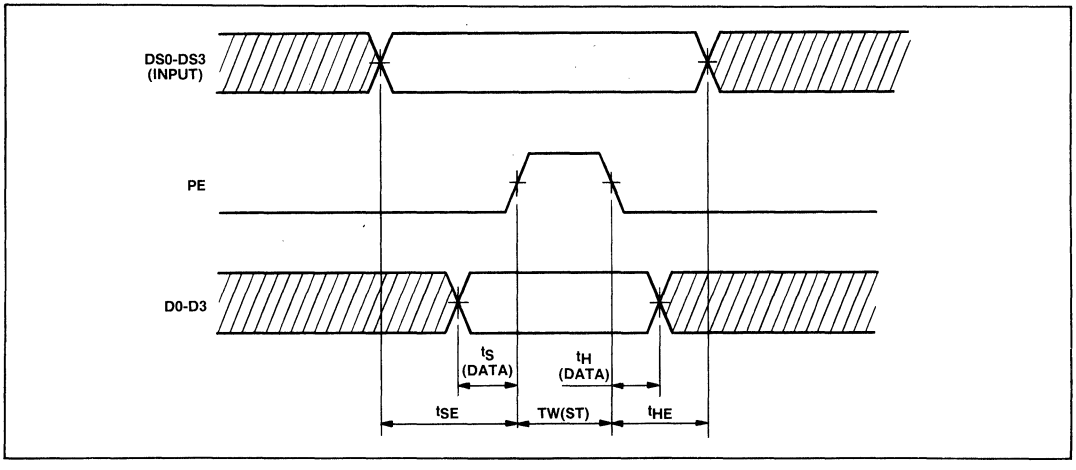


Fig.6 Timing diagram

PHASE COMPARATORS

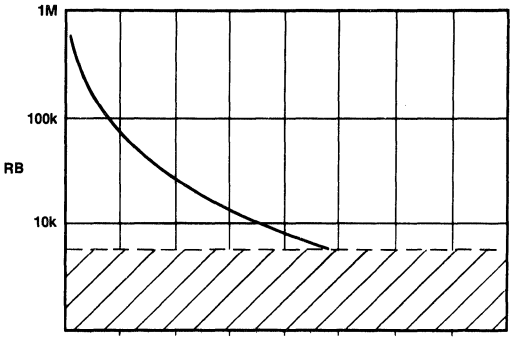
A standard digital phase/frequency detector driving a three-state output provides a 'coarse' error signal to enable fast switching between channels. This output is active until the phase error is within the sample and hold phase detector window, when its output becomes high impedance. Phase-lock is indicated at this point with a low level on LD. The sample and hold phase detector provides a 'fine' error signal to give further phase adjustment and to hold the loop in lock.

An internally generated ramp controlled by the digital output from both the reference and main divider chains is sampled at the reference frequency to give the fine error signal, PDA. When in phase lock this output would typically be at (V_{DD}-V_{SS})/2 and any offset from this would be proportional to phase error. The relationship between this offset voltage and the phase error is the phase-comparator gain which is programmable with an external resistor, RB. An internal 50pF capacitor is used in the sample and hold comparator.

This gain is typically:

$$\text{GAIN} = \frac{10\,[V_{DD}\text{-}V_{SS}\text{-}0.7\text{-}89(RB^{-½})]}{2 \times \pi\ 50\times10^{-12} \times RB\times FR}$$

The value of RB should be chosen to give the required gain at the reference frequency used. Fig.7 for example shows that to achieve a gain of 380V per radian at 10kHz requires approximately 39kΩ. A second external component is required; this is a hold capacitor of non-critical value which might typically be 470pF, a smaller value being sufficient if the sideband performance required is not high. Fig.7 shows the gain normalised to a 1Hz comparison frequency; to obtain the value for any other frequency, divide the value of Gain Frequency product by the desired frequency.



FR				
5kHz	400	800	1200	1600
10kHz	200	400	600	800
25kHz	80	160	240	320

Fig.7 RB versus gain and reference frequency

CRYSTAL OSCILLATOR

When using the internal oscillator, the stability may be enhanced at high frequencies by the use of an external resistor between Pin 8 and the other components. A value of 150-270Ω is advised.

PROGRAMMING/POWER UP

All data and signal input pins should have no input applied to them prior to the application of V_{DD}, as otherwise 'latch up' may occur.

NJ8821A

FREQUENCY SYNTHESISER (MICROPROCESSOR INTERFACE) WITH RESETTABLE COUNTERS

The NJ8821A is a synthesiser circuit fabricated on the Plessey 5-micron CMOS process and is capable of achieving high sideband attenuation and low noise performance. The circuit contains a reference oscillator, 11-bit programmable reference divider, digital and sample-and-hold phase comparators, 10-bit programmable 'M' counter, 7-bit programmable 'A' counter and the necessary control and latch circuitry for accepting and latching the input data.

Data is presented as eight 4-bit words under external control from a suitable microprocessor.

It is intended to be used in conjunction with a two-modulus prescaler such as the SP8710 series to produce a universal binary coded synthesiser.

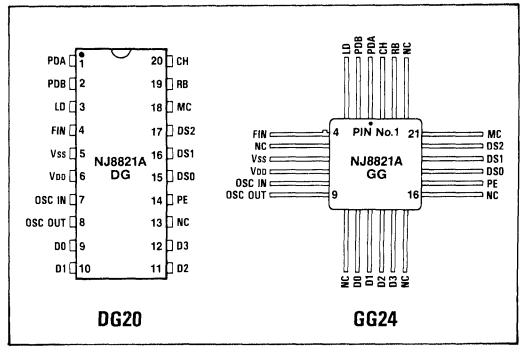


Fig.1 Pin connections

FEATURES

- Low Power Consumption
- High Performance Sample and Hold Phase Detector
- Microprocessor Compatible
- >10MHz Input Frequency
- Military Temperature Range (-55°C to +125°C)

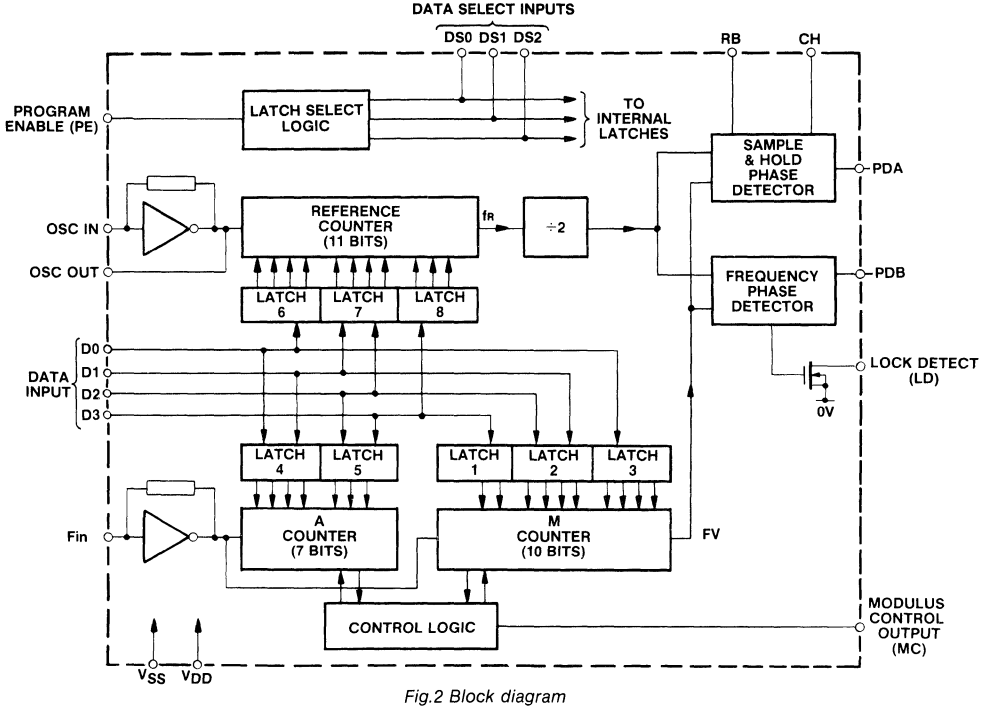


Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

V_{DD} - V_{SS} 5V ± 0.5V

Temperature range -55°C to +125°C

DC Characteristics at V_{DD} = 5V

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		3.5	7.0	mA	FOSC, FIN = 10MHz } 0 to 5V square wave
		0.7	2.0	mA	FOSC, FIN = 1.0MHz }
MODULUS CONTROL OUT					
High level	4.6			V	I_{source} 1mA
Low level			0.4	V	I_{sink} 1mA
LOCK DETECT OUT					
Low level			0.4	V	I_{sink} 4mA
Open drain pull-up voltage			8	V	
PDB Output					
High level	4.6			V	I_{source} 4mA
Low level			0.4	V	I_{sink} 4mA
3-state leakage			±0.1	μA	
INPUT LEVELS					
Data Inputs					
High level	4.25			V	TTL compatible
Low level			0.75	V	See note 1
Program Enable Input					
High level	4.25			V	
Low level			0.75	V	
DS INPUTS					
High level	4.25			V	
Low level			0.75	V	

AC Characteristics

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
FIN/OSC inputs	200			mV RMS	10MHz AC coupled sinewave
Max. operating freq. OSC/FIN inputs	10.6			MHz	V_{DD} = 5V, Input squarewave V_{DD}-V_{SS}. Note 4
Propagation delay, clock to modulus control		30	50	ns	Note 2
Strobe pulse width external mode, $t_{w(ST)}$	2			μs	
Data set-up time, $t_{s(DATA)}$	1			μs	
Data hold time, $t_{H(DATA)}$	1			μs	
Address set-up time, t_{SE}	1			μs	
Address hold time, t_{HE}	1			μs	
Digital phase detector propagation delay		500		ns	
Gain programming resistor, RB	5			kΩ	See Fig.7
Hold capacitor, CH			1	nF	Note 3
Output resistance PDA			5	kΩ	
Digital phase detector gain		1		V/Rad	

NOTES

1. Data inputs have internal 'pull-up' resistors to enable them to be driven from TTL outputs.
2. All counters have outputs directly synchronous with their respective clock rising edges.
3. Finite output resistance of internal voltage follower and 'on' resistance of sample switch driving this pin will add a finite time-constant to the loop. A 1nF hold capacitor will give a maximum time-constant of 5 microseconds.
4. Operation at up to 15MHz is possible with a full logic swing but is not guaranteed.

PIN DESIGNATION

Pin No. GG	Pin No. DG	Name	Description
1	1	PDA	Analogue output from the sample and hold phase comparator for use as a 'fine' error signal. Output at (V_{DD}-V_{SS})/2 when in lock. Voltage increases as FV phase lead increases and decreases as FR phase lead increases. Output is linear over only a narrow phase window determined by gain programmed by RB.
2	2	PDB	Three-state output from the phase/frequency detector for use as a 'coarse' error signal. FV > FR or FV leading: positive pulses FV < FR or FR leading: negative pulses FV = FR and phase error within PDA window: high impedance
3	3	LD	An open drain lock detect output at low level when phase error within PDA window (in lock). High impedance at all other times.
4	4	FIN	The input to the main counters normally driven from a prescaler which may be AC coupled or when a full logic swing is available may be DC coupled.
6	5	V_{SS}	Negative supply (normally ground)
7	6	V_{DD}	Positive supply
8,9	7,8	OSC.IN OSC.OUT	These pins form an on-chip reference oscillator when a parallel resonant crystal is connected across them. Capacitors of an appropriate value are also required between each end of the crystal and ground to provide the necessary additional phase shift. An external crystal-generated reference signal may alternatively be applied to OSC.IN. This may be a low-level signal AC coupled into OSC.IN or if a full logic swing is available it may be DC coupled. The programme range of the reference counter is 6-4094 in steps of 2, with the division ratio being twice the programmed number.
11,12,13,14	9,10,11,12	D0-D3	Information on these inputs is transferred to the internal latches during the appropriate data read time slot. D3 MSB, D0 LSB.
17	14	PE	This pin is used as a strobe for the data. A logic high on this pin transfers data from the data pins to the internal latch selected by the address, (data select) lines, while a logic zero disables the data lines
18,19,20	15,16,17	DS0-DS2	Data-select inputs to control the addressing of data latches.
21	18	MC	Signal for controlling an external dual-modulus prescaler. The modulus control level will be low at the beginning of a count cycle and will remain low until the 'A' counter completes its cycle. The modulus control then goes high and remains high until the 'M' counter completes its cycle at which point both counters are reset. This gives a total division ratio of M.N +A where N and N +1 represent the dual modulus prescale values. The programme range of the 'A' counter is 0-127 and therefore can control prescalers with a division ratio up to and including ÷128/129. The program range of the 'M' counter is 3-1023 and for correct program operation M ≥A. Where every possible channel is required, the minimum division ratio should be N^2-N.
23	19	RB	An external sample and hold phase comparator gain programming resistor should be connected between this pin and V_{SS}.
24	20	CH	An external hold capacitor should be connected between this pin and V_{SS}.

ABSOLUTE MAXIMUM RATINGS

Supply voltage (V_{DD} - V_{SS})	-0.5V to 7V
Input voltage	
Open drain O/P (pin 3)	7V
All other pins	V_{SS} -0.3V to V_{DD} +0.3V
Storage temperature	-65°C to +150°C

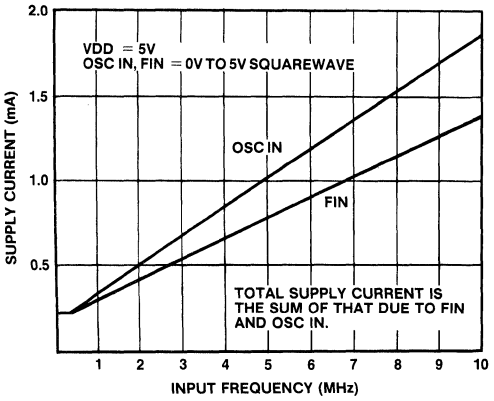


Fig.3 Typical supply current versus input frequency

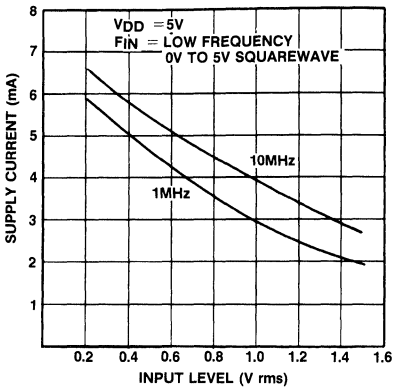


Fig.4 Typical supply current versus input level, Osc In

PROGRAMMING

Timing is generated externally, normally from a microprocessor, and allows the user to change the data in selected latches. The data map is Fig.5 with the PE pin used as a strobe for the data. Taking the PE pin high will transfer data from the data pins into the selected latch and taking this pin low will disable the data pins, retaining that data on the selected latch. Data transfer from all internal latches into the counters will occur simultaneously with the transfer of data into latch 1 and therefore this would normally be the final latch addressed during each channel change. Timing information is given in Fig.6.

When re-programming, a reset to zero state is followed by reloading with the new counter values. This means the synthesiser loop lock up time will be well defined and less than 10msec. If shorter lock up times are required, when making only small changes in frequency, the non-resettable version NJ8823 should be considered.

WORD	DS2	DS1	DS0	D3	D2	D1	D0
1	0	0	0	M1	M0	-	-
2	0	0	1	M5	M4	M3	M2
3	0	1	0	M9	M8	M7	M6
4	0	1	1	A3	A2	A1	A0
5	1	0	0	-	A6	A5	A4
6	1	0	1	R3	R2	R1	R0
7	1	1	0	R7	R6	R5	R4
8	1	1	1	-	R10	R9	R8

Fig.5 Data map

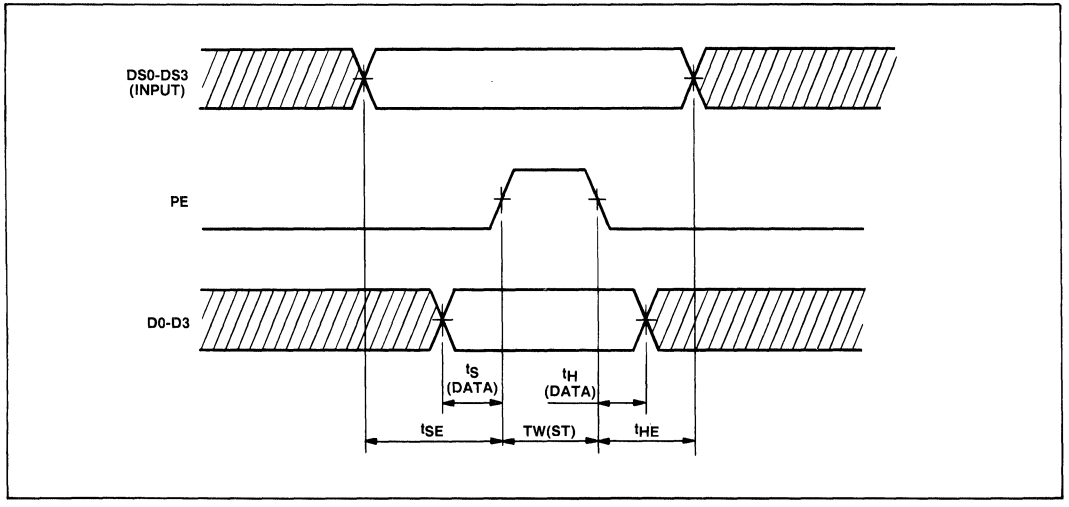


Fig.6 Timing diagram

PHASE COMPARATORS

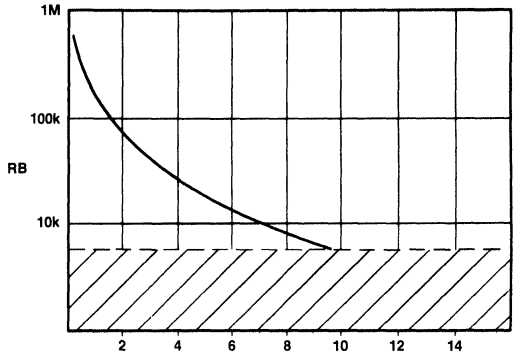
A standard digital phase/frequency detector driving a three-state output provides a 'coarse' error signal to enable fast switching between channels. This output is active until the phase error is within the sample and hold phase detector window, when its output becomes high impedance. Phase-lock is indicated at this point with a low level on LD. The sample and hold phase detector provides a 'fine' error signal to give further phase adjustment and to hold the loop in lock.

An internally generated ramp controlled by the digital output from both the reference and main divider chains is sampled at the reference frequency to give the fine error signal, PDA. When in phase lock this output would typically be at $(V_{DD}-V_{SS})/2$ and any offset from this would be proportional to phase error. The relationship between this offset voltage and the phase error is the phase-comparator gain which is programmable with an external resistor, RB. An internal 50pF capacitor is used in the sample and hold comparator.

This gain is typically:

$$\text{GAIN} = \frac{10\,[V_{DD}-V_{SS}-0.7-89(RB^{-½})]}{2 \times \pi\ 50\times10^{-12} \times RB\times FR}$$

The value of RB should be chosen to give the required gain at the reference frequency used. Fig.7 for example shows that to achieve a gain of 380V per radian at 10kHz requires approximately 39kΩ. A second external component is required; this is a hold capacitor of non-critical value which might typically be 470pF, a smaller value being sufficient if the sideband performance required is not high. Fig.7 shows the gain normalised to a 1Hz comparison frequency; to obtain the value for any other frequency, divide the value of Gain Frequency product by the desired frequency.



FR				
5kHz	400	800	1200	1600
10kHz	200	400	600	800
25kHz	80	160	240	320

Fig.7 RB versus gain and reference frequency

CRYSTAL OSCILLATOR

When using the internal oscillator, the stability may be enhanced at high frequencies by the use of an external resistor between Pin 8 and the other components. A value of 150-270Ω is advised.

PROGRAMMING/POWER UP

All data and signal input pins should have no input applied to them prior to the application of V_{DD}, as otherwise 'latch up' may occur.

NJ8822, NJ8822B

FREQUENCY SYNTHESISER (MICROPROCESSOR SERIAL INTERFACE) WITH RESETTABLE COUNTERS

The NJ8822 is a synthesiser circuit fabricated on the Plessey 5-micron CMOS process and is capable of achieving high sideband attenuation and low noise performance. It contains a reference oscillator, 11-bit programmable reference divider, digital and sample-and-hold phase comparators, 10-bit programmable 'M' counter, 7-bit programmable 'A' counter and the necessary control and latch circuitry for accepting and latching the input data.

Data is presented serially under external control from a suitable microprocessor. Although 28 bits of data are initially required to program all counters subsequent updating can be abbreviated to 17 bits when only the 'A' and 'M' counters require changing.

It is intended to be used in conjunction with a two-modulus prescaler such as the SP8710 or SP8704 series to produce a universal binary coded synthesiser for up to 950MHz operation.

FEATURES

- Low Power Consumption
- High Performance Sample and Hold Phase Detector
- Serial Input with Fast Update Feature
- >110MHz Input Frequency

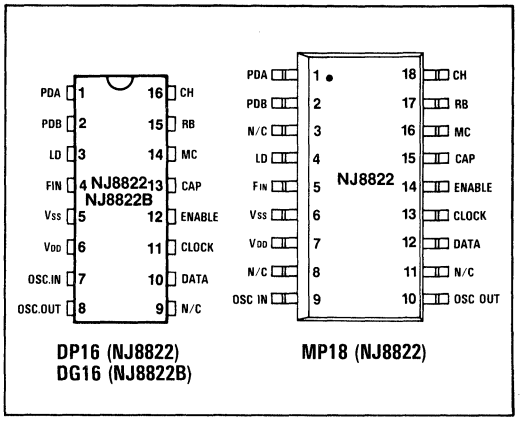


Fig. I Pin connections - top view, not to scale

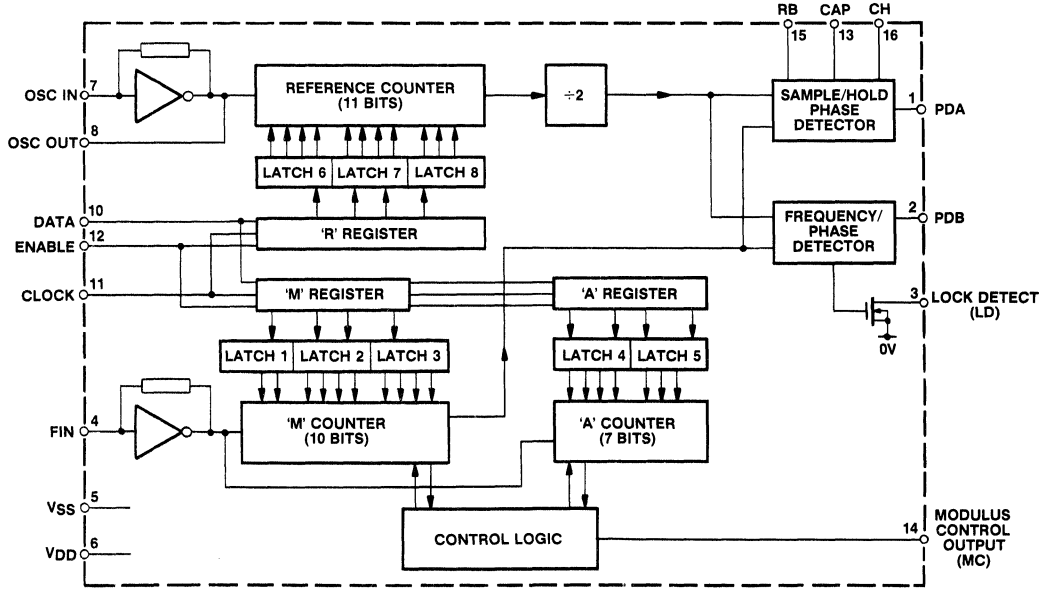


Fig.2 Block diagram. Pin numbers for MP package are shown in brackets.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{DD}-V_{SS} 5V ± 0.5V
Temperature range: NJ8822 -30°C to +70°C, NJ8822B -40°C to +85°C

DC Characteristics at V_{DD} = 5V

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current			5.5	mA	FOSC, FIN = 10MHz } 0 to 5V square wave
			1.5	mA	FOSC, FIN = 1MHz }
MODULUS CONTROL OUT					
High level	4.6			V	I_{source} 1mA
Low level			0.4	V	I_{sink} 1mA
LOCK DETECT OUT					
Low level			0.4	V	I_{sink} 4mA
Open drain pull-up voltage			8	V	
PDB OUTPUT					
High level	4.6			V	I_{source} 5mA
Low level			0.4	V	I_{sink} 5mA
3-state leakage			±0.1	μA	

AC Characteristics

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
FIN/OSC inputs	200			mV RMS	10MHz AC coupled sinewave
Max. operating freq. OSC/FIN inputs	10			MHz	V_{DD} = 5V, Input squarewave V_{DD}-V_{SS}, 25°C
Propagation delay, clock to modulus control		30	50	ns	Note 2
Programming inputs					
Clock high time, t_{CH}	0.5			μs	All timing periods are referenced to the negative transition of the clock waveform
Clock low time, t_{CL}	0.5			μs	
Enable set-up time, t_{ES}	0.2		t_{CH}	μs	
Enable hold time, t_{EH}	0.2			μs	
Data set-up time, t_{DS}	0.2			μs	
Data hold time, t_{DH}	0.2			μs	
Clock rise and fall times	0.2			μs	
Positive going threshold, V_T +	3			V	Note 1
Negative going threshold, V_T-			2	V	
Phase Detector					
Digital phase detector propagation delay		500		ns	
Gain programming resistor, RB	5			kΩ	
Hold capacitor, CH			1	nF	Note 3
Programming capacitor, CAP			1	nF	
Output resistance, PDA			5	kΩ	

NOTES
1. Data, Clock and Enable inputs are high impedance Schmitt buffers without ull up resistors. They are therefore not TTL compatible.
2. All counters have outputs directly synchronous with their respective clock rising edges.
3. The finite output resistance of the internal voltage follower and 'on' resistance of sample switch driving this pin will add a finite time-constant to the loop. A 1nF hold capacitor will give a maximum time-constant of 5 microseconds.
4. The inputs to the device should be at logic '0' when power is applied if latch up conditions are to be avoided. This includes the signal/osc. frequency inputs.

ABSOLUTE MAXIMUM RATINGS

Supply voltage (V_{DD}-V_{SS}) -0.5V to 7V
Input voltage
Open drain O/P (pin 3 (DG) pin 4 (MP)) 7V
All other pins V_{SS} -0.3V to V_{DD} +0.3V

Storage temperature -55°C to +125°C (DP and MP packages, NJ8822)
Storage temperature -65°C to +150°C (DG package, NJ8822B)

PIN DESIGNATION

Pin No. DG,DP	Pin No. MP	Name	Description
1	1	PDA	Analog output from the sample and hold phase comparator for use as a 'fine' error signal. Voltage increases as FV (FV is the output from the 'M' counter) phase lead increases and decreases as FR (FR is the output from the reference counter) phase lead increases. Output is linear over only a narrow phase window determined by gain (programmed by RB). In a type 2 loop, this pin is at (V_{DD} - V_{SS})/2 when the system is in lock.
-	3	N/C	Not connected.
2	2	PDB	Three-state output from the phase/frequency detector for use as a 'coarse' error signal. FV > FR or FV leading: positive pulses. FV < FR or FR leading: negative pulses. FV = FR and phase error within PDA window: high impedance.
3	4	LD	An open drain lock detect output at low level when phase error is within PDA window (in lock); high impedance at all other times.
4	5	FIN	The input to the main counters. It is normally driven from a prescaler which may be AC coupled or, when a full logic swing is available, may be DC coupled.
5	6	V_{SS}	Negative supply (ground).
6	7	V_{DD}	Positive supply (normally 5V).
-	8	N/C	Not connected.
7,8	9,10	OSC.IN/ OSC.OUT	These pins form an on-chip reference oscillator when a parallel resonant crystal is connected across them. Capacitors of an appropriate value are also required between each end of the crystal and ground to provide the necessary additional phase shift. The addition of a 220 ohm resistor between Pin 8 and the crystal will improve stability. An external reference signal may alternatively be applied to OSC.IN. This may be a low-level signal, AC coupled, or if a full logic swing is available it may be DC coupled. The program range of the reference counter is 3 to 2047 in steps of 1, with the division ratio being twice that programmed.
9	-	N/C	Not connected.
10	12	DATA	Information on this input is transferred to the internal latches during the appropriate data read time slot. Data is high for a '1' and low for a '0'. There are three data words which control the NJ8822, MSB is first in the order, 'A' - (7 bits), 'M' - (10 bits), 'R' - (11 bits).
11	13	CLK	Data is clocked in on the negative transition of the clock waveform. If less than 28 negative clock transitions have been received when the enable line goes low (i.e. only 'M' and 'A' will have been clocked in) then the 'R' counter latch will remain unchanged and only 'M' and 'A' will be transferred from the input shift register to the counter latches. This will protect the 'R' counter from being corrupted by any glitches on the clock line after only 'M' and 'A' have been loaded. If 28 negative transitions have been counted then the 'R' counter will be loaded with the new data.
12	14	ENABLE	When the enable is low the data and clock inputs are disabled internally. As soon as the enable is high the data and clock input are enabled and data may be clocked into the device. The data is transferred from the input shift register to the counter latches on the negative transition of the enable input and both inputs to the phase detector are synchronised to each other. Enable transitions only allowed when CLK is high.
13	15	CAP	This pin allows an external capacitor to be put in parallel with the ramp capacitor, and allows further programming of the device. (This capacitor is connected from CAP to V_{SS}).
14	16	MC	Output for controlling an external dual modulus prescaler. The modulus control level will be low at the beginning of a count cycle and will remain low until the 'A' counter completes its cycle. The modulus control then goes high and remains high until the 'M' counter completes its cycle at which point both counters are reset. This gives a total division ratio of M.N + A where N and N + 1 represent the dual modulus prescaler values. The program range of the 'A' counter is 0-127 and therefore can control prescalers with a division ratio up to and including ÷ 128/129. The programming range of the 'M' counter is 3-1023 and for correct program operation M $\geqslant$ A. Where every possible channel is required, the minimum division ratio should be $N^2 - N$.
15	17	RB	An external sample and hold phase comparator gain programming resistor should be connected between this pin and V_{SS}.
16	18	CH	An external hold capacitor should be connected between this pin and V_{SS}.

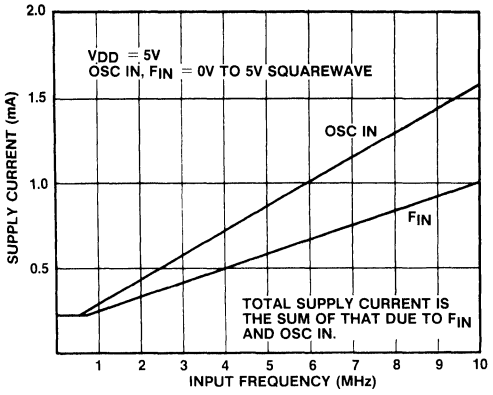


Fig.3 Typical supply current v. input frequency

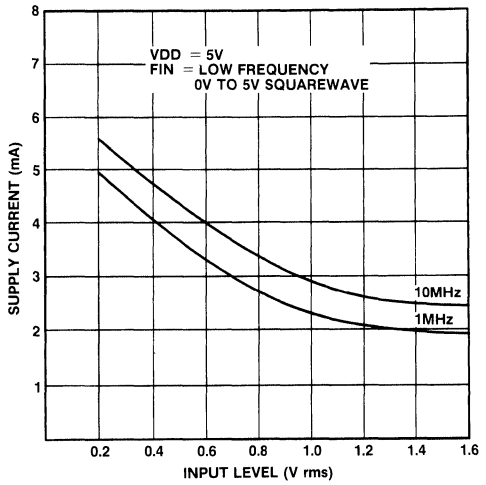


Fig.4 Typical supply current v. input level, Osc In

PROGRAMMING

Reference Divider Chain

The comparison frequency depends upon the crystal oscillator frequency and the division ratio of the R counter, which can be programmed in the range 3 to 2047.

$$R = \frac{fosc}{2 \times fcomp}$$

ie where *fcomp* = comparison frequency
fosc = oscillator frequency
R = R counter ratio

For example where crystal frequency = 10MHz and a channel spacing comparison frequency of 12.5kHz is required,

$$R = \frac{10^7}{2 \times 12.5 \times 10^3} = 400$$

Thus the R register would be programmed to 400 expressed in binary.
NB The total divider range is from 6 to 4094 in steps of 2.

VCO Divider Chain

The synthesised frequency of the voltage control oscillator (VCO) will depend on the division ratio of the M and A counters, the value of the external two modulus prescaler ($N/N + 1$) and the value of the comparison frequency *fcomp*.

The division ratio $P = NM + A$
where *M* is the ratio of the M counter in the range 3 to 1023 and *A* is the ratio of the A counter in the range 1 to 127.
Note $M \geqslant A$

$$\text{Also } P + \frac{fvco}{fcomp}$$

For example if the desired VCO frequency = 275MHz, the comparison frequency is 12.5kHz and a two modulus prescaler of ÷64/65 is being used, then:

$$P = \frac{275 \times 10^6}{12.5 \times 10^3} = 22 \times 10^3$$

Now $P = NM + A$
which can be rearranged to be $P/N = M + A/N$
In our example we have

$$\frac{22 \times 10^3}{64} = M + \frac{A}{6} \text{ therefore } 343.75 = M + \frac{A}{64}$$

M is programmed to the integer part = 343 and *A* is programmed to the fractional part times 64
ie $A = 0.75 \times 64 = 48$
NB The minimum ratio that can be used is $N^2 - N$
To check $P = 343 \times 64 + 48 = 22000$ which is the required divide ratio.

When re-programming, a reset to zero state is followed by reloading with the new counter values. This means the synthesiser loop lock up time will be well defined and less than 10msec. If shorter lock up times are required, when making only small changes in frequency, the non resettable version NJ8824 should be considered.

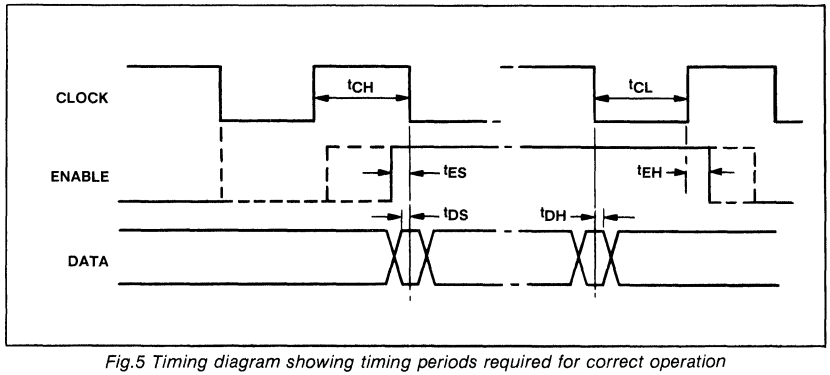


Fig.5 Timing diagram showing timing periods required for correct operation

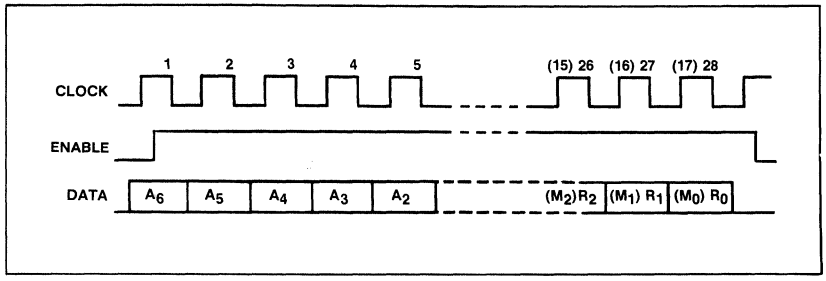


Fig.6 Timing diagram showing programming details

PHASE COMPARATORS

Noise output from a synthesiser loop is related to loop gain $K\Phi K v/P$, where $K\Phi$ is phase detector constant (volts/rad), $K v$ is the VCO constant (rad-secs/volt) and P is the overall loop division ratio. When P is large and the loop gain is low, noise may be reduced by employing a phase comparator with a high gain. The sample and hold phase detector within the NJ8822 has both a high gain and uses a double sampling technique to reduce spurious ouputs to a low level.

A standard digital phase/frequency detector driving a three-state output provides a 'coarse' error signal to enable fast switching between channels.

This output is active until the phase error is within the sample and hold phase detector window, when its output becomes high impedance. Phase-lock is indicated at this point with a low level on LD. The sample and hold phase detector provides a 'fine' error signal to give further phase adjustment and to hold the loop in lock.

An internally generated ramp controlled by the digital output from both the reference and main divider chains is sampled at the reference frequency to give the fine error signal, PDA. When in phase lock this output would typically be at $(V_{DD}-V_{SS})/2$ and any offset from this would be proportional to phase error.

The relationship between this offset voltage and the phase error is the phase-comparator gain which is programmable with an external resistor, RB and a capacitor, CAP.

An internal 50pF capacitor is used in the sample and hold comparator.

This gain is typically:

$$\text{GAIN} = \frac{10\,[V_{DD}-V_{SS}-0.7-89(RB^{-½})]}{2\pi\,[CAP + 50\times10^{-12}] \times RB \times FR}$$

The value of RB and CAP should be chosen to give the required gain at the reference frequency used. Fig.8 shows that to achieve a gain of 380V per radian at 10kHz requires RB to be approximately 39kΩ, CAP is zero. A hold capacitor (CH) of non-critical value which might be typically 470pF is connected from CH to V_{SS}. A smaller value is sufficient if the sideband performance required is not high.

The output from the sample/phase detector should be combined with that of the coarse phase/frequency detector and filtered to generate a single control voltage to drive the VCO.

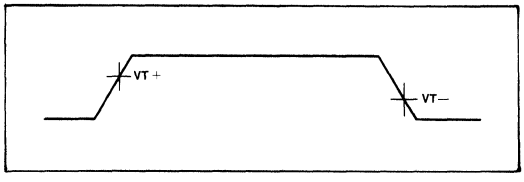


Fig.7 Timing diagram showing voltage thresholds

CRYSTAL OSCILLATOR

When using the internal oscillator, the stability may be enhanced at high frequencies by the use of an external resistor between Pin 8 and the other components. A value of 150-270Ω is advised.

PROGRAMMING/POWER UP

All data and signal input pins should have no input applied to them prior to the application of V_{DD}, as otherwise 'latch up' may occur.

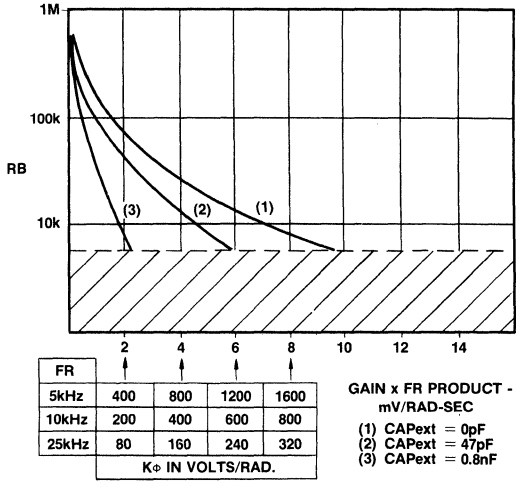


Fig.8 RB v. gain and reference frequency

PLESSEY
Semiconductors

NJ8822A

FREQUENCY SYNTHESISER (MICROPROCESSOR SERIAL INTERFACE) WITH RESETTABLE COUNTERS

The NJ8822A is a synthesiser circuit fabricated on the Plessey 5-micron CMOS process and is capable of achieving high sideband attenuation and low noise performance. It contains a reference oscillator, 11-bit programmable reference divider, digital and sample-and-hold phase comparators, 10-bit programmable 'M' counter, 7-bit programmable 'A' counter and the necessary control and latch circuitry for accepting and latching the input data.

Data is presented serially under external control from a suitable microprocessor. Although 28 bits of data are initially required to program all counters subsequent updating can be abbreviated to 17 bits when only the 'A' and 'M' counters require changing.

It is intended to be used in conjunction with a two-modulus prescaler such as the SP8710 series to produce a universal binary coded synthesiser for up to 950MHz operation.

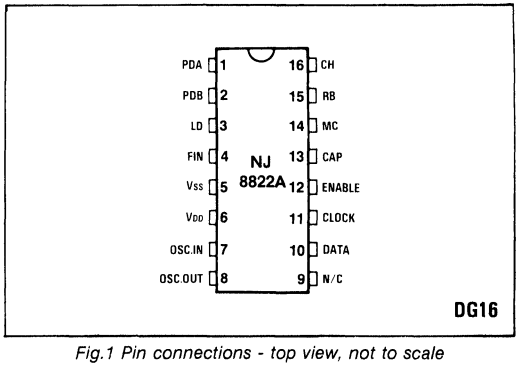


Fig.1 Pin connections - top view, not to scale

FEATURES

- Low Power Consumption
- High Performance Sample and Hold Phase Detector
- Serial Input with Fast Update Feature
- > 10MHz Input Frequency
- Military Temperature Range (-55°C to +125°C)

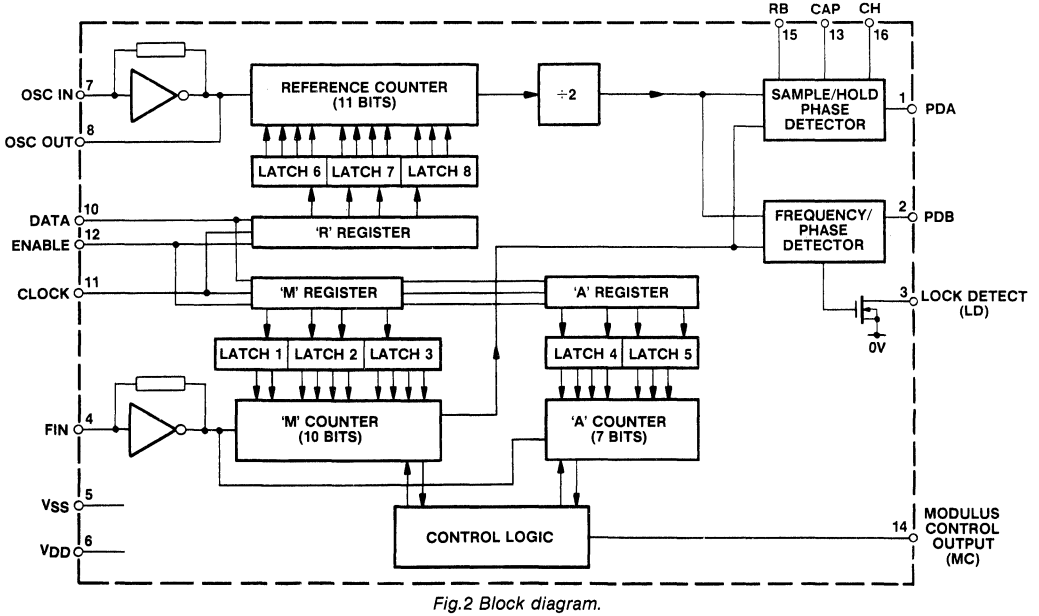


Fig.2 Block diagram.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{DD}-V_{SS} 5V ± 0.5V
Temperature range -55°C to +125°C

DC Characteristics at V_{DD} = 5V

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		6.3	7.0	mA	FOSC, FIN = 10MHz } 0 to 5V square wave
		0.7	2.0	mA	FOSC, FIN = 1MHz } 0 to 5V square wave
MODULUS CONTROL OUT					
High level	4.6			V	I_{source} 1mA
Low level			0.4	V	I_{sink} 1mA
LOCK DETECT OUT					
Low level			0.4	V	I_{sink} 4mA
Open drain pull-up voltage			8	V	
PDB OUTPUT					
High level	4.6			V	I_{source} 4mA
Low level			0.4	V	I_{sink} 4mA
3-state leakage			±0.1	μA	

AC Characteristics

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
FIN/OSC inputs	200			mV RMS	10MHz AC coupled sinewave
Max. operating freq. OSC/FIN inputs	10			MHz	V_{DD} = 5V, Input squarewave V_{DD}-V_{SS}, 25°C
Propagation delay, clock to modulus control		30	50	ns	Note 2
Programming inputs					
Clock high time, t_{cH}	0.5			μs	All timing periods are referenced to the negative transition of the clock waveform
Clock low time, t_{cL}	0.5			μs	
Enable set-up time, t_{ES}	0.2		t_{CH}	μs	
Enable hold time, t_{EH}	0.2			μs	
Data set-up time, t_{DS}	0.2			μs	
Data hold time, t_{DH}	0.2			μs	
Clock rise and fall times	0.2			μs	
Positive going threshold, V_T +	3			V	Note 1
Negative going threshold, V_T-			2	V	
Phase Detector					
Digital phase detector propagation delay		500		ns	
Gain programming resistor, RB	5			kΩ	
Hold capacitor, CH			1	nF	Note 3
Programming capacitor, CAP			1	nF	
Output resistance, PDA			5	kΩ	

NOTES
1. Data, Clock and Enable inputs are high impedance Schmitt buffers without pull up resistors. They are therefore not TTL compatible.
2. All counters have outputs directly synchronous with their respective clock rising edges.
3. The finite output resistance of the internal voltage follower and 'on' resistance of sample switch driving this pin will add a finite time-constant to the loop. A 1nF hold capacitor will give a maximum time-constant of 5 microseconds.
4. The inputs to the device should be at logic '0' when power is applied if latch up conditions are to be avoided. This includes the signal/osc. frequency inputs.

ABSOLUTE MAXIMUM RATINGS

Supply voltage (V_{DD}-V_{SS})	-0.5V to 7V
Input voltage	
Open drain O/P (pin 3)	7V
All other pins	V_{SS} -0.3V to V_{DD} +0.3V
Storage temperature	-65°C to +150°C

PIN DESIGNATION

Pin No.	Name	Description
1	PDA	Analog output from the sample and hold phase comparator for use as a 'fine' error signal. Voltage increases as FV (FV is the output from the 'M' counter) phase lead increases and decreases as FR (FR is the output from the reference counter) phase lead increases. Output is linear over only a narrow phase window determined by gain (programmed by RB). In a type 2 loop, this pin is at (V_{DD} - V_{SS})/2 when the system in in lock.
-	N/C	Not connected.
2	PDB	Three-state output from the phase/frequency detector for use as a 'coarse' error signal. FV > FR or FV leading: positive pulses. FV < FR or FR leading: negative pulses. FV = FR and phase error within PDA window: high impedance.
3	LD	An open drain lock detect output at low level when phase error is within PDA window (in lock); high impedance at all other times.
4	FIN	The input to the main counters. It is normally driven from a prescaler which may be AC coupled or, when a full logic swing is available, may be DC coupled.
5	V_{SS}	Negative supply (ground).
6	V_{DD}	Positive supply (normally 5V).
-	N/C	Not connected.
7,8	OSC.IN/ OSC.OUT	These pins form an on-chip reference oscillator when a parallel resonant crystal is connected across them. Capacitors of an appropriate value are also required between each end of the crystal and ground to provide the necessary additional phase shift. The addition of a 220 ohm resistor between Pin 8 and the crystal will improve stability. An external reference signal may alternatively be applied to OSC.IN. This may be a low-level signal, AC coupled, or if a full logic swing is available it may be DC coupled. The program range of the reference counter is 3 to 2047 in steps of 1, with the division ratio being twice that programmed.
9	N/C	Not connected.
10	DATA	Information on this input is transferred to the internal latches during the appropriate data read time slot. Data is high for a '1' and low for a '0'. There are three data words which control the NJ8822, MSB is first in the order, 'A' - (7 bits), 'M' - (10 bits), 'R' - (11 bits).
11	CLK	Data is clocked in on the negative transition of the clock waveform. If less than 28 negative clock transitions have been received when the enable line goes low (i.e. only 'M' and 'A' will have been clocked in) then the 'R' counter latch will remain unchanged and only 'M' and 'A' will be transferred from the input shift register to the counter latches. This will protect the 'R' counter from being corrupted by any glitches on the clock line after only 'M' and 'A' have been loaded. If 28 negative transitions have been counted then the 'R' counter will be loaded with the new data.
12	ENABLE	When the enable is low the data and clock inputs are disabled internally. As soon as the enable is high the data and clock input are enabled and data may be clocked into the device. The data is transferred from the input shift register to the counter latches on the negative transition of the enable input and both inputs to the phase detector are synchronised to each other. Enable transitions only allowed when CLK is high.
13	CAP	This pin allows an external capacitor to be put in parallel with the ramp capacitor, and allows further programming of the device. (This capacitor is connected from CAP to V_{SS}).
14	MC	Output for controlling an external dual modulus prescaler. The modulus control level will be low at the beginning of a count cycle and will remain low until the 'A' counter completes its cycle. The modulus control then goes high and remains high until the 'M' counter completes its cycle at which point both counters are reset. This gives a total division ratio of M.N + A where N and N + 1 represent the dual modulus prescaler values. The program range of the 'A' counter is 0-127 and therefore can control prescalers with a division ratio up to and including ÷ 128/129. The programming range of the 'M' counter is 3-1023 and for correct program operation M ⩾ A. Where every possible channel is required, the minimum division ratio should be N^2 - N.
15	RB	An external sample and hold phase comparator gain programming resistor should be connected between this pin and V_{SS}.
16	CH	An external hold capacitor should be connected between this pin and V_{SS}.

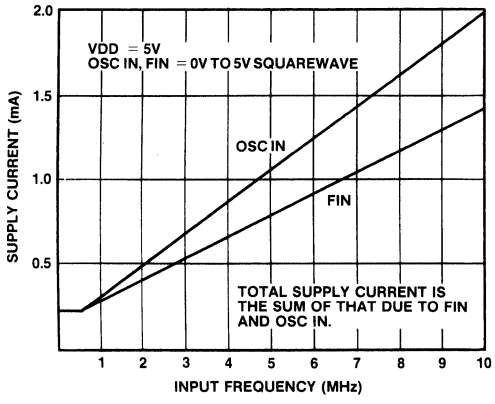


Fig.3 Typical supply current v. input frequency

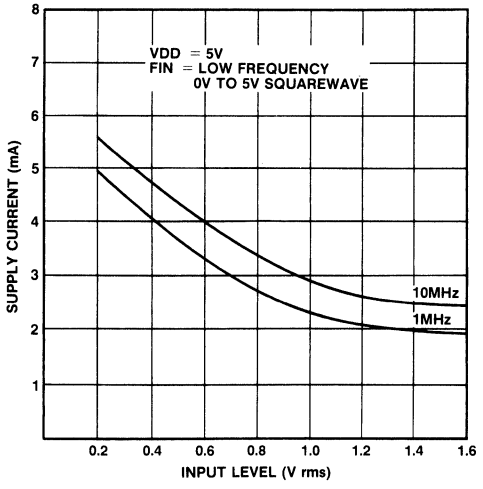


Fig.4 Typical supply current v. input level, Osc In

PROGRAMMING

Reference Divider Chain

The comparison frequency depends upon the crystal oscillator frequency and the division ratio of the R counter, which can be programmed in the range 3 to 2047.

$$R = \frac{fosc}{2 \times fcomp}$$

ie where *fcomp* = comparison frequency
fosc = oscillator frequency
R = R counter ratio

For example where crystal frequency = 10MHz and a channel spacing comparison frequency of 12.5kHz is required,

$$R = \frac{10^7}{2 \times 12.5 \times 10^3} = 400$$

Thus the R register would be programmed to 400 expressed in binary.
NB The total divider range is from 6 to 4094 in steps of 2.

VCO Divider Chain

The synthesised frequency of the voltage control oscillator (VCO) will depend on the division ratio of the M and A counters, the value of the external two modulus prescaler ($N/N + 1$) and the value of the comparison frequency *fcomp*.

The division ratio $P = NM + A$
where *M* is the ratio of the M counter in the range 3 to 1023 and *A* is the ratio of the A counter in the range 1 to 127.
Note $M \geqslant A$

$$\text{Also } P + \frac{fvco}{fcomp}$$

For example if the desired VCO frequency = 275MHz, the comparison frequency is 12.5kHz and a two modulus prescaler of ÷64/65 is being used, then:

$$P = \frac{275 \times 10^6}{12.5 \times 10^3} = 22 \times 10^3$$

Now $P = NM + A$
which can be rearranged to be $P/N = M + A/N$
In our example we have

$$\frac{22 \times 10^3}{64} = M + \frac{A}{6} \quad \text{therefore } 343.75 = M + \frac{A}{64}$$

M is programmed to the integer part = 343 and *A* is programmed to the fractional part times 64
ie $A = 0.75 \times 64 = 48$
NB The minimum ratio that can be used is $N^2 - N$
To check $P = 343 \times 64 + 48 = 22000$ which is the required divide ratio.

When re-programming, a reset to zero state is followed by reloading with the new counter values. This means the synthesiser loop lock up time will be well defined and less than 10msec. If shorter lock up times are required, when making only small changes in frequency, the non resettable version NJ8824 should be considered.

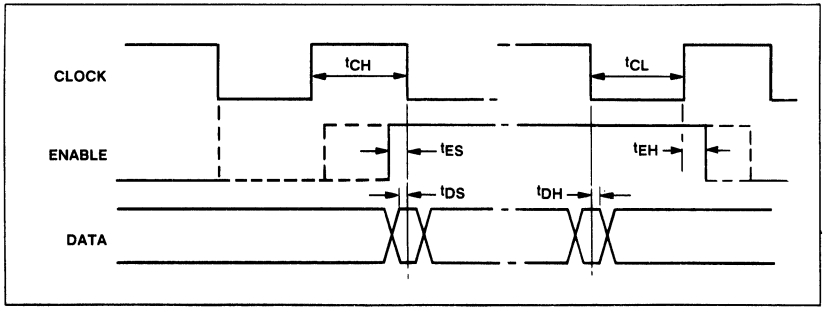


Fig.5 Timing diagram showing timing periods required for correct operation

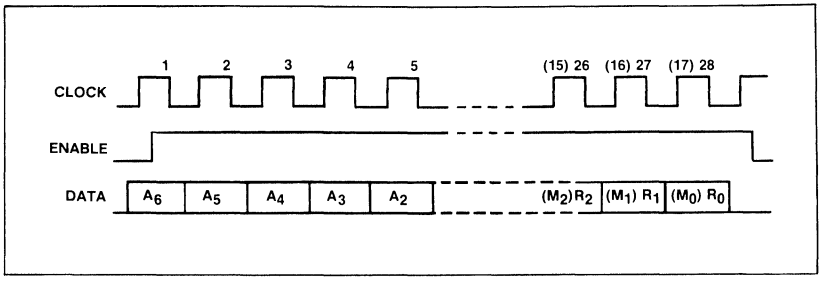


Fig.6 Timing diagram showing programming details

PHASE COMPARATORS

Noise output from a synthesiser loop is related to loop gain $K_\Phi K_V/P$, where K_Φ is phase detector constant (volts/rad), K_V is the VCO constant (rad-secs/volt) and P is the overall loop division ratio. When P is large and the loop gain is low, noise may be reduced by employing a phase comparator with a high gain. The sample and hold phase detector within the NJ8822 has both a high gain and uses a double sampling technique to reduce spurious ouputs to a low level.

A standard digital phase/frequency detector driving a three-state output provides a 'coarse' error signal to enable fast switching between channels.

This output is active until the phase error is within the sample and hold phase detector window, when its output becomes high impedance. Phase-lock is indicated at this point with a low level on LD. The sample and hold phase detector provides a 'fine' error signal to give further phase adjustment and to hold the loop in lock.

An internally generated ramp controlled by the digital output from both the reference and main divider chains is sampled at the reference frequency to give the fine error signal, PDA. When in phase lock this output would typically be at $(V_{DD}-V_{SS})/2$ and any offset from this would be proportional to phase error.

The relationship between this offset voltage and the phase error is the phase-comparator gain which is programmable with an external resistor, RB and a capacitor, CAP.

An internal 50pF capacitor is used in the sample and hold comparator.

This gain is typically:

$$\text{GAIN} = \frac{10\,[V_{DD}-V_{SS}-0.7-89(RB^{-1/2})]}{2\pi\,[CAP + 50\times10^{-12}] \times RB \times FR}$$

The value of RB and CAP should be chosen to give the required gain at the reference frequency used. Fig.8 shows that to achieve a gain of 380V per radian at 10kHz requires RB to be approximately 39kΩ, CAP is zero. A hold capacitor (CH) of non-critical value which might be typically 470pF is connected from CH to V_{SS}. A smaller value is sufficient if the sideband performance required is not high.

The output from the sample/phase detector should be combined with that of the coarse phase/frequency detector and filtered to generate a single control voltage to drive the VCO.

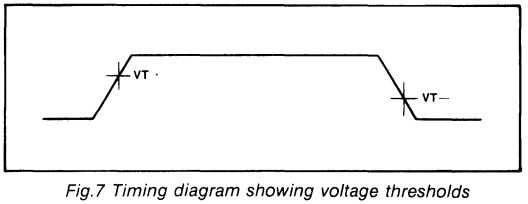


Fig.7 Timing diagram showing voltage thresholds

CRYSTAL OSCILLATOR

When using the internal oscillator, the stability may be enhanced at high frequencies by the use of an external resistor between Pin 8 and the other components. A value of 150-270Ω is advised.

PROGRAMMING/POWER UP

All data and signal input pins should have no input applied to them prior to the application of V_{DD}, as otherwise 'latch up' may occur.

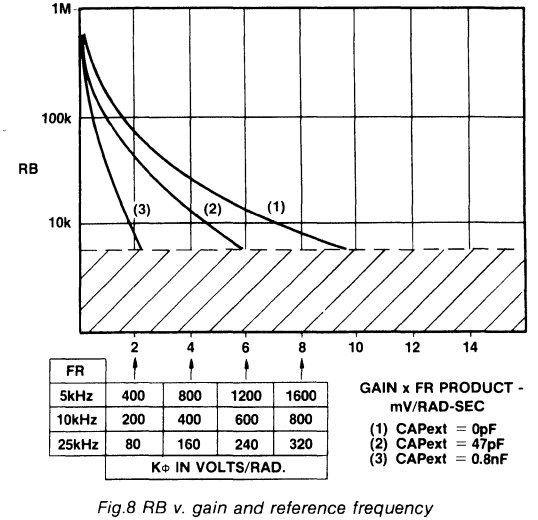


Fig.8 RB v. gain and reference frequency

NJ8823, NJ8823B

FREQUENCY SYNTHESISER (MICROPROCESSOR INTERFACE) WITH NON-RESETTABLE COUNTERS

The NJ8823/NJ8823B is a synthesiser circuit fabricated on the Plessey 5-micron CMOS process and is capable of achieving high sideband attenuation and low noise performance. The circuit contains a reference oscillator, 11-bit programmable reference divider, digital and sample-and-hold phase comparators, 10-bit programmable 'M' counter, 7-bit programmable 'A' counter and the necessary control and latch circuitry for accepting and latching the input data.

Data is presented as eight 4-bit words under external control from a suitable microprocessor.

The NJ8823 is available in Plastic DIL (DP) and Miniature Plastic DIL (MP) poackages, both with operating temperature range of -30°C to +70°C. The NJ8823B is available only in Ceramic DIL package with operating temperature range of -40°C to +85°C.

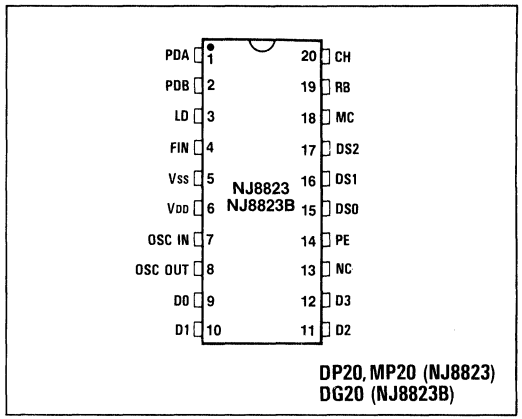


Fig.1 Pin connections

FEATURES

- Low Power Consumption
- High Performance Sample and Hold Phase Detector
- Microprocessor Compatible
- > 10MHz Input Frequency
- Fast Lock Up Time

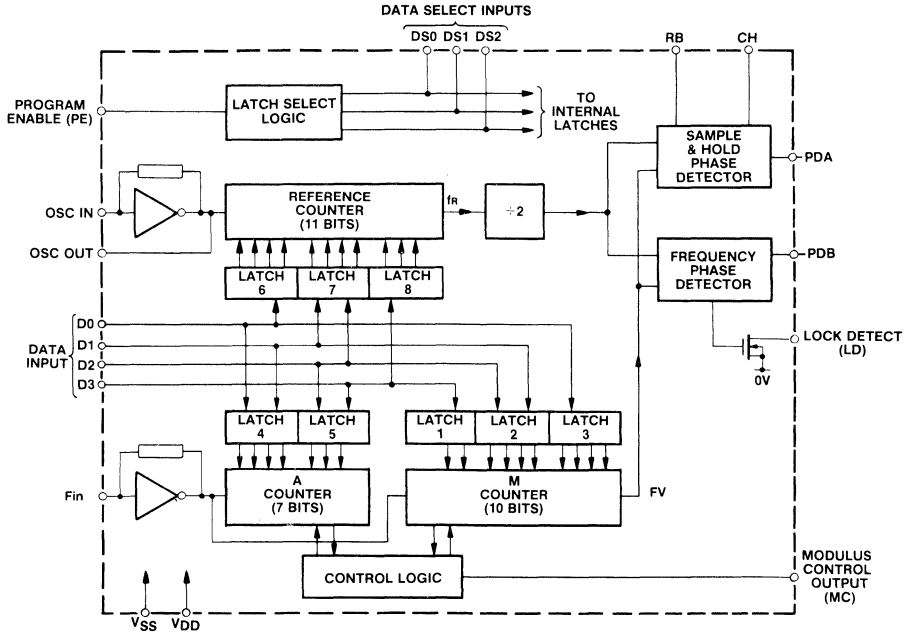


Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

V_{DD}-V_{SS} 5V ± 0.5V

Temperature range: NJ8823 -30°C to +70°C, NJ8823B -40°C to +85°C

DC Characteristics at V_{DD} = 5V

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		3.5	5.5	mA	FOSC, FIN = 10MHz } 0 to 5V square wave
		0.7	1.5	mA	FOSC, FIN = 1.0MHz }
MODULUS CONTROL OUT					
High level	4.6			V	I_{source} 1mA
Low level			0.4	V	I_{sink} 1mA
LOCK DETECT OUT					
Low level			0.4	V	I_{sink} 4mA
Open drain pull-up voltage			8	V	
PDB Output					
High level	4.6			V	I_{source} 5mA
Low level			0.4	V	I_{sink} 5mA
3-state leakage			±0.1	μA	
INPUT LEVELS					
Data Inputs					
High level	4.25			V	TTL compatible
Low level			0.75	V	See note 1
Program Enable Input					
High level	4.25			V	
Low level			0.75	V	
DS INPUTS					
High level	4.25			V	
Low level			0.75	V	

AC Characteristics

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
FIN/OSC inputs	200			mV RMS	10MHz AC coupled sinewave
Max. operating freq. OSC/FIN inputs	10.6			MHz	V_{DD} = 5V, Input squarewave V_{DD}-V_{SS}.Note 4
Propagation delay, clock to modulus control		30	50	ns	Note 2
Strobe pulse width external mode, $t_{w(ST)}$	2			μs	
Data set-up time, $t_{s(DATA)}$	1			μs	
Data hold time, $t_{H(DATA)}$	1			μs	
Address set-up time, t_{SE}	1			μs	
Address hold time, t_{HE}	1			μs	
Digital phase detector propagation delay		500		ns	
Gain programming resistor, RB	5			kΩ	See Fig.6
Hold capacitor, CH			1	nF	Note 3
Output resistance PDA			5	kΩ	
Digital phase detector gain		1		V/Rad	

NOTES

1. Data inputs have internal 'pull-up' resistors to enable them to be driven from TTL outputs.
2. All counters have outputs directly synchronous with their respective clock rising edges.
3. Finite output resistance of internal voltage follower and 'on' resistance of sample switch driving this pin will add a finite time-constant to the loop. A 1nF hold capacitor will give a maximum time-constant of 5 microseconds.
4. Operation at up to 15MHz is possible with a full logic swing but is not guaranteed.

PIN DESIGNATION

Pin No.	Name	Description
1	PDA	Analog output from the sample and hold phase comparator for use as a 'fine' error signal. Output at (V_{DD}-V_{SS})/2 when in lock. Voltage increases as FV phase lead increases and decreases as FR phase lead increases. Output is linear over only a narrow phase window determined by gain programmed by RB.
2	PDB	Three-state output from the phase/frequency detector for use as a 'coarse' error signal. FV > FR or FV leading: positive pulses FV < FR or FR leading: negative pulses FV = FR and phase error within PDA window: high impedance
3	LD	An open drain lock detect output at low level when phase error within PDA window (in lock). High impedance at all other times.
4	FIN	The input to the main counters normally driven from a prescaler which may be AC coupled or when a full logic swing is available may be DC coupled.
5	V_{SS}	Negative supply (normally ground)
6	V_{DD}	Positive supply
7,8	OSC.IN/ OSC.OUT	These pins form an on-chip reference oscillator when a parallel resonant crystal is connected across them. Capacitors of an appropriate value are also required between each end of the crystal and ground to provide the necessary additional phase shift. An external crystal-generated reference signal may alternatively be applied to OSC.IN. This may be a low-level signal AC coupled into OSC.IN or if a full logic swing is available it may be DC coupled. The program range of the reference counter is 6-4094 in steps of 2, with the division ratio being twice the programmed number.
9,10,11,12	D0-D3	Information on these inputs is transferred to the internal latches during the appropriate data read time slot. D3 MSB, D0 LSB.
14	PE	This pin is used as a strobe for the data. A logic high on this pin transfers data from the data pins to the internal latch selected by the address, (data select) lines, while a logic zero disables the data lines.
15,16,17	DS0-DS2	Data-select inputs to control the addressing of data latches.
18	MC	Signal for controlling an external dual-modulus prescaler. The modulus control level will be low at the beginning of a count cycle and will remain low until the 'A' counter completes its cycle. The modulus control then goes high and remains high until the 'M' counter completes its cycle at which point both counters are reset. This gives a total division ratio of M.N +A where N and N +1 represent the dual modulus prescale values. The program range of the 'A' counter is 0-127 and therefore can control prescalers with a division ratio up to and including ÷128/129. The program range of the 'M' counter is 3-1023 and for correct program operation M ⩾A. Where every possible channel is required, the minimum division ratio should be N^2-N.
19	RB	An external sample and hold phase comparator gain programming resistor should be connected between this pin and V_{SS}.
20	CH	An external hold capacitor should be connected between this pin and V_{SS}.

ABSOLUTE MAXIMUM RATINGS

Supply voltage (V_{DD} - V_{SS})	-0.5V to 7V
Input voltage	
Open drain O/P (pin 3)	7V
All other pins	V_{SS} -0.3V to V_{DD} +0.3V
Storage temperature	-65 °C to +150 °C (DG Package, NJ8823B)
Storage temperature	-55 °C to +125 °C (DP and MP Packages, NJ8823)

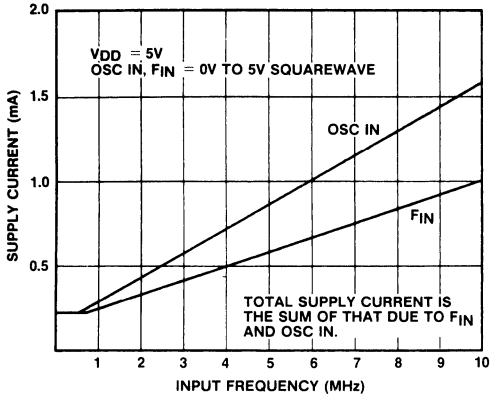


Fig.3 Typical supply current versus input frequency

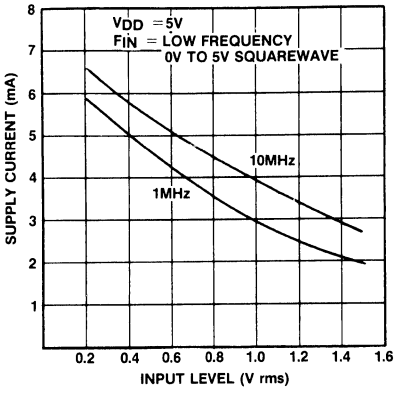


Fig.4 Typical supply current versus input level, Osc In

PROGRAMMING

Timing is generated externally, normally from a microprocessor, and allows the user to change the data in selected latches. The data map is Fig.5 with the PE pin used as a strobe for the data. Taking the PE pin high will transfer data from the data pins into the selected latch and taking this pin low will disable the data pins, retaining that data on the selected latch. Data transfer from all internal latches into the counters will occur simultaneously with the transfer of data into latch 1 and therefore this would normally be the final latch addressed during each channel change. Timing information for this mode of operation is given in Fig.6.

When re-programming, the counters are changed only when they reach a zero state. There is no reset to zero state. This means the synthesiser loop lock up time will be variable. For the case when only small changes in frequency are required, the non-resettable synthesiser should achieve the shortest loop lock up times.

WORD	DS2	DS1	DS0	D3	D2	D1	D0
1	0	0	0	M1	M0	-	-
2	0	0	1	M5	M4	M3	M2
3	0	1	0	M9	M8	M7	M6
4	0	1	1	A3	A2	A1	A0
5	1	0	0	-	A6	A5	A4
6	1	0	1	R3	R2	R1	R0
7	1	1	0	R7	R6	R5	R4
8	1	1	1	-	R10	R9	R8

Fig.5 Data map

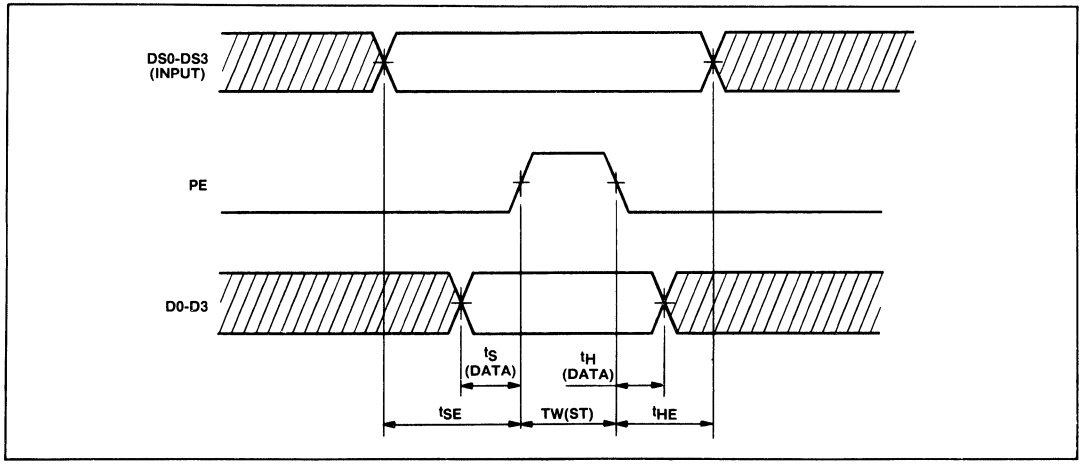


Fig.6 Timing diagram

PHASE COMPARATORS

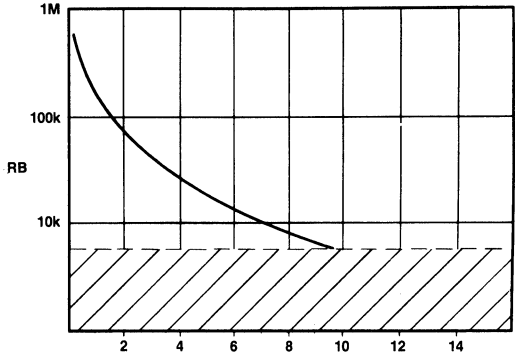
A standard digital phase/frequency detector driving a three-state output provides a 'coarse' error signal to enable fast switching between channels. This output is active until the phase error is within the sample and hold phase detector window, when its output becomes high impedance. Phase-lock is indicated at this point with a low level on LD. The sample and hold phase detector provides a 'fine' error signal to give further phase adjustment and to hold the loop in lock.

An internally generated ramp controlled by the digital output from both the reference and main divider chains is sampled at the reference frequency to give the fine error signal, PDA. When in phase lock this output would typically be at (V_{DD}-V_{SS})/2 and any offset from this would be proportional to phase error. The relationship between this offset voltage and the phase error is the phase-comparator gain which is programmable with an external resistor, RB. An internal 50pF capacitor is used in the sample and hold comparator.

This gain is typically:

$$\text{GAIN} = \frac{10\,[V_{DD}\text{-}V_{SS}\text{-}0.7\text{-}89(RB^{-\frac{1}{2}})]}{2 \times \pi\ 50\text{x}10^{-12} \times \text{RBxFR}}$$

The value of RB should be chosen to give the required gain at the reference frequency used. Fig.7 for example shows that to achieve a gain of 380V per radian at 10kHz requires approximately 39kΩ. A second external component is required; this is a hold capacitor of non-critical value which might typically be 470pF, a smaller value being sufficient if the sideband performance required is not high. Fig.7 shows the gain normalised to a 1Hz comparison frequency; to obtain the value for any other frequency, divide the value of Gain Frequency product by the desired frequency.



FR				
5kHz	400	800	1200	1600
10kHz	200	400	600	800
25kHz	80	160	240	320

Fig.7 RB versus gain and reference frequency

CRYSTAL OSCILLATOR

When using the internal oscillator, the stability may be enhanced at high frequencies by the use of an external resistor between Pin 8 and the other components. A value of 150-270Ω is advised.

PROGRAMMING/POWER UP

All data and signal input pins should have no input applied to them prior to the application of V_{DD}, as otherwise 'latch up' may occur.

PLESSEY
Semiconductors

NJ8824, NJ8824B

FREQUENCY SYNTHESISER (MICROPROCESSOR SERIAL INTERFACE) WITH NON-RESETTABLE COUNTERS

The NJ8824 is a synthesiser circuit fabricated on the Plessey 5-micron CMOS process and is capable of achieving high sideband attenuation and low noise performance. It contains a reference oscillator, 11-bit programmable reference divider, digital and sample-and-hold phase comparators, 10-bit programmable 'M' counter, 7-bit programmable 'A' counter and the necessary control and latch circuitry for accepting and latching the input data.

Data is presented serially under external control from a suitable microprocessor. Although 28 bits of data are initially required to program all counters subsequent updating can be abbreviated to 17 bits when only the 'A' and 'M' counters require changing.

It is intended to be used in conjunction with a two-modulus prescaler such as the SP8710 or SP8704 series to produce a universal binary coded synthesiser for up to 960MHz operation.

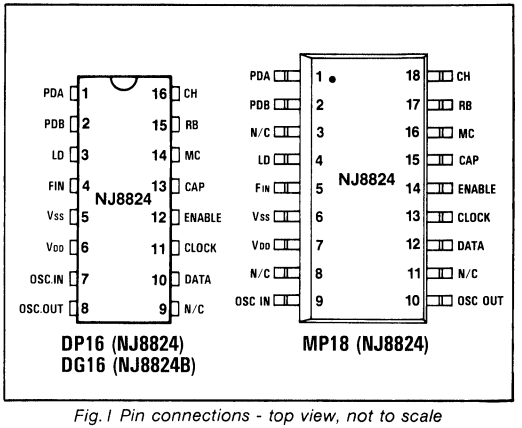


Fig. 1 Pin connections - top view, not to scale

FEATURES

- Low Power Consumption
- High Performance Sample and Hold Phase Detector
- Serial Input with Fast Update Feature
- >10MHz Input Frequency
- Fast Lock Up Time

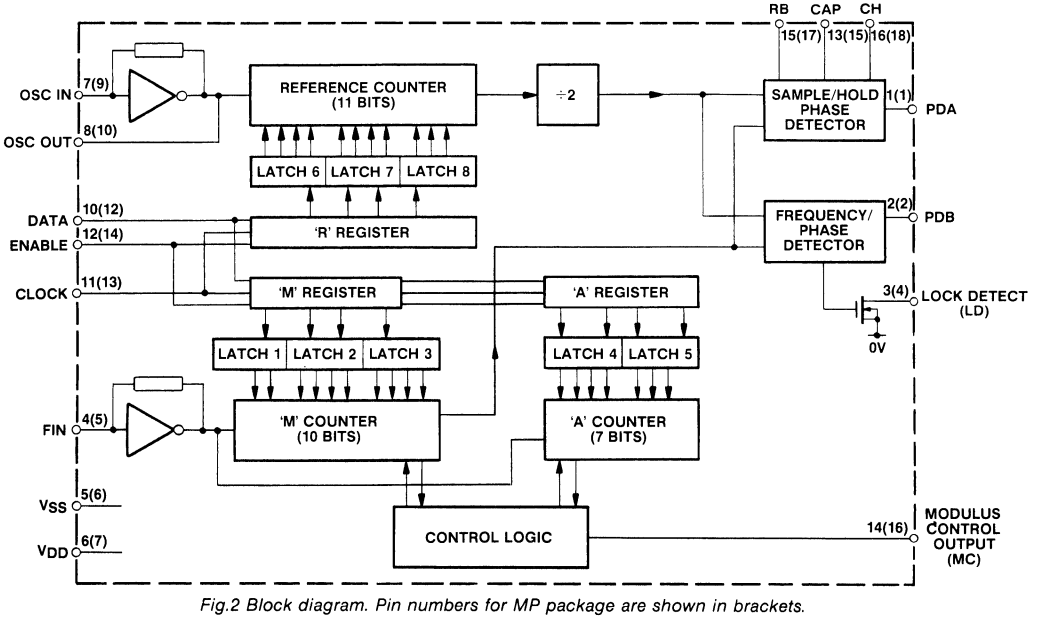


Fig.2 Block diagram. Pin numbers for MP package are shown in brackets.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{DD}-V_{SS} 5V ± 0.5V
Temperature range: NJ8824 -30°C to +70°C, NJ8824B -40°C to +85°C

DC Characteristics at V_{DD} = 5V

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current			5.5	mA	FOSC, FIN = 10MHz } 0 to 5V square wave
			1.5	mA	FOSC, FIN = 1MHz }
MODULUS CONTROL OUT					
High level	4.6			V	I_{source} 1mA
Low level			0.4	V	I_{sink} 1mA
LOCK DETECT OUT					
Low level			0.4	V	I_{sink} 4mA
Open drain pull-up voltage			8	V	
PDB OUTPUT					
High level	4.6			V	I_{source} 5mA
Low level			0.4	V	I_{sink} 5mA
3-state leakage			±0.1	μA	

AC Characteristics

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
FIN/OSC inputs	200			mV RMS	10MHz AC coupled sinewave
Max. operating freq. OSC/FIN inputs	10			MHz	V_{DD} = 5V, Input squarewave V_{DD}-V_{SS}, 25°C
Propagation delay, clock to modulus control		30	50	ns	Note 2
Programming inputs					
Clock high time, t_{cH}	0.5			μs	All timing periods are referenced to the negative transition of the clock waveform
Clock low time, t_{cL}	0.5			μs	
Enable set-up time, t_{ES}	0.2		t_{CH}	μs	
Enable hold time, t_{EH}	0.2			μs	
Data set-up time, t_{DS}	0.2			μs	
Data hold time, t_{DH}	0.2			μs	
Clock rise and fall times	0.2			μs	
Positive going threshold, V_T +	3			V	Note 1
Negative going threshold, V_T-			2	V	
Phase Detector					
Digital phase detector propagation delay		500		ns	
Gain programming resistor, RB	5			kΩ	
Hold capacitor, CH			1	nF	Note 3
Programming capacitor, CAP			1	nF	
Output resistance, PDA			5	kΩ	

NOTES
1. Data, Clock and Enable inputs are high impedance Schmitt buffers without pull up resistors. They are therefore not TTL compatible.
2. All counters have outputs directly synchronous with their respective clock rising edges.
3. The finite output resistance of the internal voltage follower and 'on' resistance of sample switch driving this pin will add a finite time-constant to the loop. A 1nF hold capacitor will give a maximum time-constant of 5 microseconds.
4. The inputs to the device should be at logic '0' when power is applied if latch up conditions are to be avoided. This includes the signal/osc. frequency inputs.

ABSOLUTE MAXIMUM RATINGS

Supply voltage (V_{DD}-V_{SS}) -0.5V to 7V
Input voltage
Open drain O/P (pin 3 (DG) pin 4 (MP)) 7V
All other pins V_{SS} -0.3V to V_{DD} +0.3V

Storage temperature -55°C to +125°C
(DP and MP packages, NJ8824)
Storage temperature -65°C to +150°C
(DG packages, NJ8824B)

PIN DESIGNATION

Pin No. DP	Pin No. MP	Name	Description
1	1	PDA	Analog output from the sample and hold phase comparator for use as a 'fine' error signal. Voltage increases as FV (FV is the output from the 'M' counter) phase lead increases and decreases as FR (FR is the output from the reference counter) phase lead increases. Output is linear over only a narrow phase window determined by gain (programmed by RB). In a type 2 loop, this pin is at (V_{DD} - V_{SS})/2 when the system is in lock.
-	3	N/C	Not connected.
2	2	PDB	Three-state output from the phase/frequency detector for use as a 'coarse' error signal. FV > FR or FV leading: positive pulses. FV < FR or FR leading: negative pulses. FV = FR and phase error within PDA window: high impedance.
3	4	LD	An open drain lock detect output at low level when phase error is within PDA window (in lock); high impedance at all other times.
4	5	FIN	The input to the main counters. It is normally driven from a prescaler which may be AC coupled or, when a full logic swing is available, may be DC coupled.
5	6	V_{SS}	Negative supply (ground).
6	7	V_{DD}	Positive supply (normally 5V).
-	8	N/C	Not connected.
7,8	9,10	OSC.IN/ OSC.OUT	These pins form an on-chip reference oscillator when a parallel resonant crystal is connected across them. Capacitors of an appropriate value are also required between each end of the crystal and ground to provide the necessary additional phase shift. The addition of a 220 ohm resistor between Pin 8 and the crystal will improve stability. An external reference signal may alternatively be applied to OSC.IN. This may be a low-level signal, AC coupled, or if a full logic swing is available it may be DC coupled. The program range of the reference counter is 3 to 2047 in steps of 1, with the division ratio being twice that programmed.
9	-	N/C	Not connected.
10	12	DATA	Information on this input is transferred to the internal latches during the appropriate data read time slot. Data is high for a '1' and low for a '0'. There are three data words which control the NJ8824, MSB is first in the order, 'A' - (7 bits), 'M' - (10 bits), 'R' - (11 bits).
11	13	CLK	Data is clocked in on the negative transition of the clock waveform. If less than 28 negative clock transitions have been received when the enable line goes low (i.e. only 'M' and 'A' will have been clocked in) then the 'R' counter latch will remain unchanged and only 'M' and 'A' will be transferred from the input shift register to the counter latches. This will protect the 'R' counter from being corrupted by any glitches on the clock line after only 'M' and 'A' have been loaded. If 28 negative transitions have been counted then the 'R' counter will be loaded with the new data.
12	14	ENABLE	When the enable is low the data and clock inputs are disabled internally. As soon as the enable is high the data and clock input are enabled and data may be clocked into the device. The data is transferred from the input shift register to the counter latches on the negative transition of the enable input and both inputs to the phase detector are synchronised to each other. Enable transitions only allowed when CLK is high.
13	15	CAP	This pin allows an external capacitor to be put in parallel with the ramp capacitor, and allows further programming of the device. (This capacitor is connected from CAP to V_{SS}).
14	16	MC	Output for controlling an external dual modulus prescaler. The modulus control level will be low at the beginning of a count cycle and will remain low until the 'A' counter completes its cycle. The modulus control then goes high and remains high until the 'M' counter completes its cycle at which point both counters are reset. This gives a total division ratio of M.N + A where N and N + 1 represent the dual modulus prescaler values. The program range of the 'A' counter is 0-127 and therefore can control prescalers with a division ratio up to and including ÷ 128/129. The programming range of the 'M' counter is 3-1023 and for correct program operation M $\geqslant$ A. Where every possible channel is required, the minimum division ratio should be N^2 - N.
15	17	RB	An external sample and hold phase comparator gain programming resistor should be connected between this pin and V_{SS}.
16	18	CH	An external hold capacitor should be connected between this pin and V_{SS}.

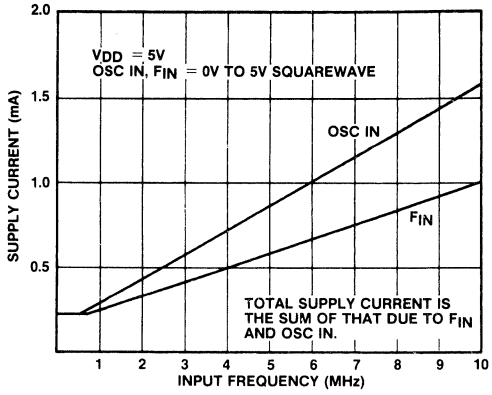


Fig.3 Typical supply current v. input frequency

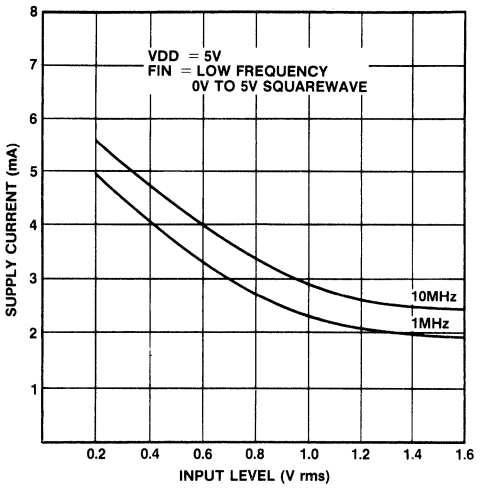


Fig.4 Typical supply current v. input level, Osc In

PROGRAMMING

Reference Divider Chain

The comparison frequency depends upon the crystal oscillator frequency and the division ratio of the R counter, which can be programmed in the range 3 to 2047.

$$R = \frac{fosc}{2 \times fcomp}$$

ie where *fcomp* = comparison frequency
fosc = oscillator frequency
R = R counter ratio

For example where crystal frequency = 10MHz and a channel spacing comparison frequency of 12.5kHz is required,

$$R = \frac{10^7}{2 \times 12.5 \times 10^3} = 400$$

Thus the R register would be programmed to 400 expressed in binary.
NB The total divider range is from 6 to 4094 in steps of 2.

VCO Divider Chain

The synthesised frequency of the voltage control oscillator (VCO) will depend on the division ratio of the M and A counters, the value of the external two modulus prescaler ($N/N + 1$) and the value of the comparison frequency *fcomp*.

The division ratio $P = NM + A$
where *M* is the ratio of the M counter in the range 3 to 1023 and *A* is the ratio of the A counter in the range 1 to 127.
Note $M \geqslant A$

$$\text{Also } P + \frac{fvco}{fcomp}$$

For example if the desired VCO frequency = 275MHz, the comparison frequency is 12.5kHz and a two modulus prescaler of ÷64/65 is being used, then:

$$P = \frac{275 \times 10^6}{12.5 \times 10^3} = 22 \times 10^3$$

Now $P = NM + A$
which can be rearranged to be $P/N = M + A/N$
In our example we have

$$\frac{22 \times 10^3}{64} = M + \frac{A}{6} \text{ therefore } 343.75 = M + \frac{A}{64}$$

M is programmed to the integer part = 343 and *A* is programmed to the fractional part times 64
ie $A = 0.75 \times 64 = 48$
NB The minimum ratio that can be used is $N^2 - N$
To check $P = 343 \times 64 + 48 = 22000$ which is the required divide ratio.

When re-programming, the counters are changed only when they reach a zero state. There is no reset to zero state. This means the synthesiser loop lock up time will be variable. For the case when only small changes in frequency are required, the non-resettable synthesiser should achieve the shortest loop lock up times.

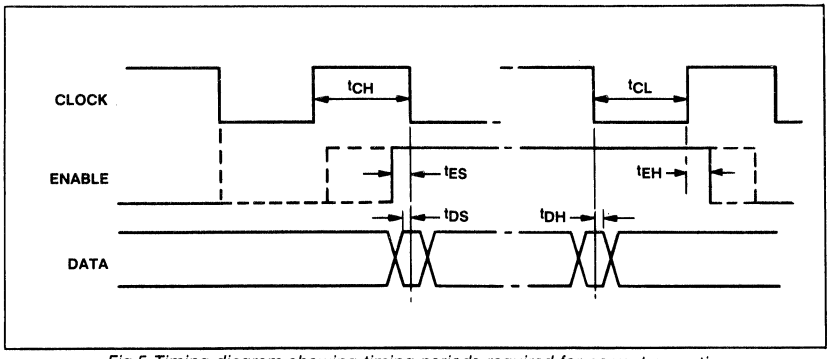


Fig.5 Timing diagram showing timing periods required for correct operation

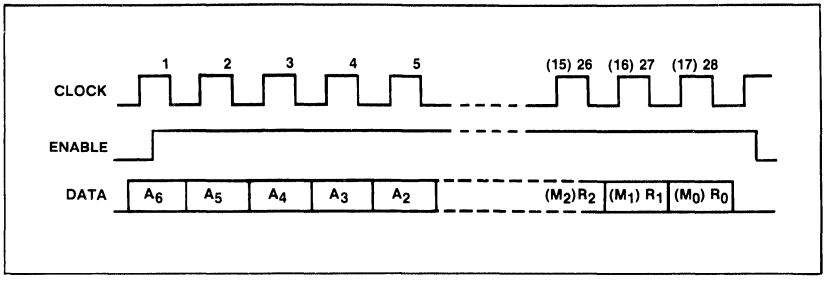


Fig.6 Timing diagram showing programming details

PHASE COMPARATORS

Noise output from a synthesiser loop is related to loop gain $K_\Phi K_V/P$, where K_Φ is phase detector constant (volts/rad), K_V is the VCO constant (rad-secs/volt) and P is the overall loop division ratio. When P is large and the loop gain is low, noise may be reduced by employing a phase comparator with a high gain. The sample and hold phase detector, within the NJ8824 has both a high gain and uses a double sampling technique to reduce spurious outputs to a low level.

A standard digital phase/frequency detector driving a three-state output provides a 'coarse' error signal to enable fast switching between channels.

This output is active until the phase error is within the sample and hold phase detector window, when its output becomes high impedance. Phase-lock is indicated at this point with a low level on LD. The sample and hold phase detector provides a 'fine' error signal to give further phase adjustment and to hold the loop in lock.

An internally generated ramp controlled by the digital output from both the reference and main divider chains is sampled at the reference frequency to give the fine error signal, PDA. When in phase lock this output would typically be at $(V_{DD}-V_{SS})/2$ and any offset from this would be proportional to phase error.

The relationship between this offset voltage and the phase error is the phase-comparator gain which is programmable with an external resistor, RB and a capacitor, CAP.

An internal 50pF capacitor is used in the sample and hold comparator.

This gain is typically:

$$\text{GAIN} = \frac{10\,[V_{DD}-V_{SS}-0.7-89(RB^{-1/2})]}{2\pi\,[CAP + 50\times10^{-12}] \times RB \times FR}$$

The value of RB and CAP should be chosen to give the required gain at the reference frequency used. Fig.8 shows that to achieve a gain of 380V per radian at 10kHz requires RB to be approximately 39kΩ, CAP is zero. A hold capacitor (CH) of non-critical value which might be typically 470pF is connected from CH to V_{SS}. A smaller value is sufficient if the sideband performance required is not high.

The output from the sample/phase detector should be combined with that of the coarse phase/frequency detector and filtered to generate a single control voltage to drive the VCO.

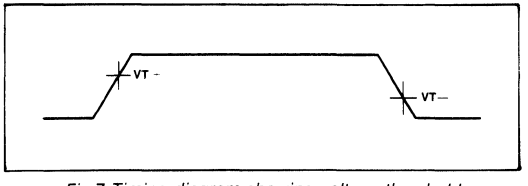


Fig.7 Timing diagram showing voltage thresholds

CRYSTAL OSCILLATOR

When using the internal oscillator, the stability may be enhanced at high frequencies by the use of an external resistor between Pin 8 and the other components. A value of 150-270Ω is advised.

PROGRAMMING/POWER UP

All data and signal input pins should have no input applied to them prior to the application of V_{DD}, as otherwise 'latch up' may occur.

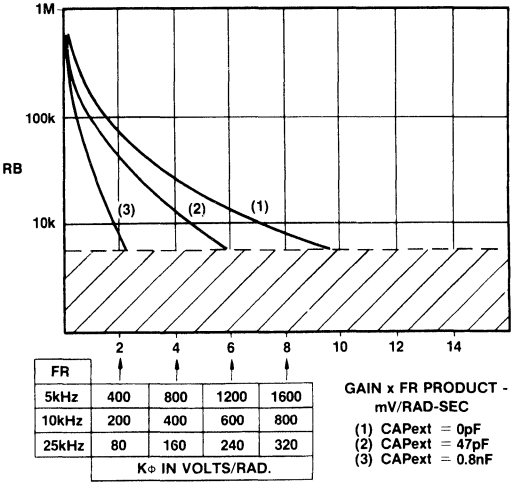


Fig.8 RB v. gain and reference frequency

PLESSEY
Semiconductors

NJ88C25

FREQUENCY SYNTHESISER (MICROPROCESSOR SERIAL INTERFACE)

The NJ88C25 is a synthesiser circuit fabricated on the 2-micron CMOS process and is capable of achieving high sideband attenuation and low noise performance. The circuit contains a reference oscillator, 11-bit programmable reference divider, digital and sample-and-hold phase comparators, 10-bit programmable 'M' counter, 7-bit programmable 'A' counter, latched and buffered Band 0 and Band 1 outputs and the necessary control and latch circuitry for accepting and latching the input data.

Data is presented serially under external control from a suitable microprocessor. Although thirty bits of data are initially required to program all counters, subsequent updating can be abbreviated to nineteen bits when only the 'A', 'M' and 'B' counters require changing.

It is intended to be used in conjunction with a two-modulus prescaler such as the SP8710 series to produce a universal binary coded synthesiser.

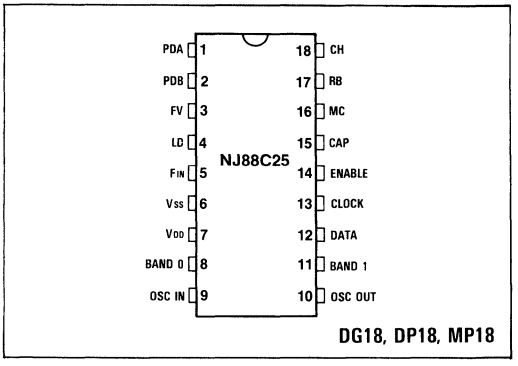


Fig.1 Pin connections - top view

FEATURES

- 3.0V to 5.0V Supply Range
- Low Power Consumption
- High Performance Sample and Hold Phase Detector
- Serial Input with Fast Update Feature
- > 20MHz Input Frequency

ABSOLUTE MAXIMUM RATINGS

Supply voltage (V_{DD} - V_{SS})	-0.5V to 7V
Input voltage	
Open drain O/Ps (pins 3 & 4)	7V
All other pins	V_{SS} -0.3V to V_{DD} +0.3V
Storage temperature	-65°C to +150°C

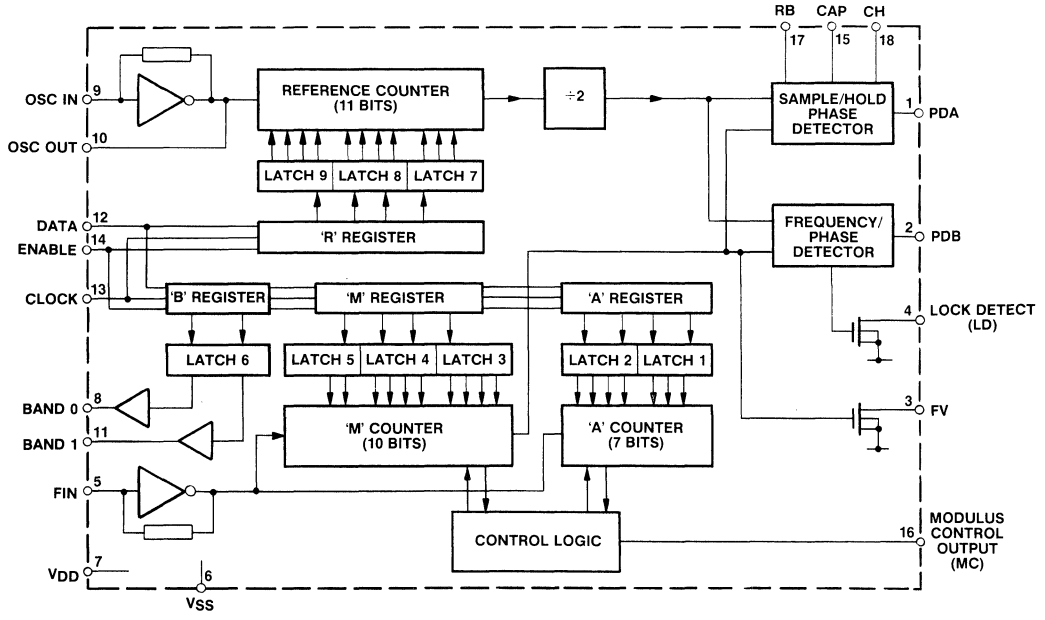


Fig.2 Block Diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{DD} - V_{SS} 2.7V to 5.5V, Temperature Range -30°C to +70°C

DC Characteristics at V_{DD} = 5.0V

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		5.5	TBA	mA	FOSC, FIN = 20MHz } 0 to 5V
		0.7	TBA	mA	FOSC, FIN = 1MHz } square
		3.7	TBA	mA	FOSC, FIN = 10MHz } wave
Modulus Control out, BAND 0, BAND 1					
High level	V_{DD}-0.4			V	I_{source} 1mA
Low level			0.4	V	I_{sink} 1mA
Lock Detect Out, FV					
Low level			0.4	V	I_{sink} 4mA
Open drain pull-up voltage			7	V	
PDB output					
High level	4.6			V	I_{source} 4mA
Low level			0.4	V	I_{sink} 4mA
3-state leakage			±0.1	μA	

AC Characteristics

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
FIN/OSC outputs	200			mV RMS	20MHz AC coupled sinewave
Max. operating freq. OSC/FIN inputs	20			MHz	V_{DD} = 5V, 0 to 5V square wave
Propagation delay, clock to modulus control		30	50	ns	Note 2
Programming inputs					
Clock high time, t_{CH}	0.5			μs	
Clock low time, t_{CL}	0.5			μs	
Enable set-up time, t_{ES}	0.2		t_{CH}	μs	Note 5
Enable hold time, t_{EH}	0.2			μs	
Data set-up time, t_{DS}	0.2			μs	
Data hold time, t_{DH}	0.2			μs	
Clock rise and fall times	0.2			μs	
Positive going threshold, V_{T+}	3			V	TTL compatible
Negative going threshold, V_{T-}			2	V	
Digital phase detector propagation delay		500		ns	
Gain programming resistor, RB	5			kΩ	
Hold capacitor, CH			1	nF	Note 3
Programming capacitor, CAP			1	nF	
Output resistance, PDA			5	kΩ	

NOTES
1. Data inputs have internal 'pull-up' resistors to enable them to be driven from TTL outputs.
2. All counters have outputs directly synchronous with their respective clock rising edges.
3. The finite output resistance of the internal voltage follower and 'on' resistance of sample switch driving this pin will add a finite time-constant to the loop. A 1nF hold capacitor will give a maximum time constant of 5 microseconds.
4. The inputs to the device should be at logic '0' when power is applied if latch up conditions are to be avoided. This includes the signal/osc. frequency inputs.
5. Clock to enable set up time is variable, dependent on frequency of OSC. IN, it needs to be specified in terms of OSC. IN frequency, clock high time (t_{CH}) and clock low time (t_{CL}). Enable set-up time, t_{ES} must meet following conditions: 4 x 1/OSC. IN $\leqslant t_{ES} < (t_{CH} + t_{CL})$.

PIN DESIGNATION

Pin No.	Name	Description
1	PDA	Analog output from the sample and hold phase comparator for use as a 'fine' error signal. Voltage increases as FV (FV is the output from the 'M' counter) phase lead increases and decreases as FR (FR is the output from the reference counter) phase lead increases. Output is linear over only a narrow phase window determined by gain (programmed by RB). In a type 2 loop, this pin is at (V_{DD} - V_{SS})/2 when the system is in lock.
2	PDB	Three-state output from the phase/frequency detector for use as a 'coarse' error signal. FV > FR or FV leading: positive pulses. FV < FR or FR leading: negative pulses. FV = FR and phase error within PDA window: high impedance.
3	FV	This pin is an open drain output from the 'M' counter.
4	LD	An open drain lock detect output at low level when phase error is within PDA window (in lock); high impedance at all other times.
5	FIN	The input to the main counters. It is normally driven from a prescaler which may be AC coupled or, when a full logic swing is available, may be DC coupled.
6	V_{SS}	Negative supply (ground).
7	V_{DD}	Positive supply (normally 5V).
9,10	OSC.IN/ OSC.OUT	These pins form an on-chip reference oscillator when a parallel resonant crystal is connected across them. Capacitors of an appropriate value are also required between each end of the crystal and ground to provide the necessary additional phase shift. The addition of a 220Ω resistor between Pin 8 and the crystal will improve stability. An external reference signal may alternatively be applied to OSC.IN. This may be a low-level signal, AC coupled, or if a full logic swing is available it may be DC coupled. The program range of the reference counter is 3 to 2047 in steps of 1, with the division ratio being twice that programmed.
8,11	BAND 0/1	Two latch outputs, providing an output of the data from the register 'B'.
12	DATA	Information on this input is transferred to the internal latches during the appropriate data read time slot. Data is high for a '1' and low for a '0'. There are four data words which control the NJ88C25, MSB is first in the order, 'A' - (7 bits), 'M' - (10 bits), 'B' (2 bits) and 'R' (11 bits).
13	CLOCK	Data is clocked in on the negative transition of the clock waveform. If less than 30 negative clock transitions have been received when the enable line goes low (ie only 'B', 'M' and 'A' have been clocked in) then the 'R' counter latch will remain unchanged and only 'B', 'M' and 'A' will be transferred from the input shift register to the counter latches. This will protect the 'R' counter from being corrupted by any glitches on the clock line after only 'B', 'M' and 'A' have been loaded. If 30 negative transitions have been counted then the 'R' counter will be loaded with the new data.
14	ENABLE	When the enable is low the data and clock inputs are disabled internally. As soon as the enable is high the data and clock inputs are enabled and data may be clocked into the device. The data is transferred from the input shift register to the counter latches on the negative transition of the enable input and both inputs to the phase detector are synchronised to each other. Enable transitions are only allowed when CLK is high.
15	CAP	This pin allows an external capacitor to be put in parallel with the ramp capacitor, and allows further programming of the device. (This capacitor is connected from CAP to V_{SS}.)
16	MC	Output for controlling an external dual modulus prescaler. The modulus control level will be low at the beginning of a count cycle and will remain low until the 'A' counter completes its cycle.The modulus control then goes high and remains high until the 'M' counter completes its cycle at which point both counters are reset. This gives a total division ratio of M.N + A where N and N + 1 represent the dual modulus prescaler values. The program range of the 'A' counter is 0-127 and therefore can control prescalers with a division ratio up to and including ÷128/129. The programming range of the 'M' counter is 3-1023 and for correct program operation M ⩾ A. Where every possible channel is required, the minimum division ratio should be N^2-N.
17	RB	An external sample and hold phase comparator gain programming resistor should be connected between this pin and V_{SS}.
18	CH	An external hold capacitor should be connected between this pin and V_{SS}.

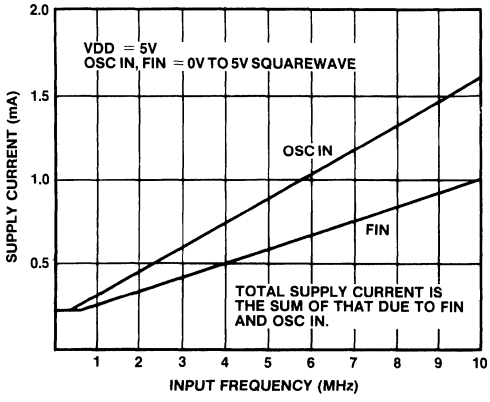


Fig.3 Typical supply current versus input frequency

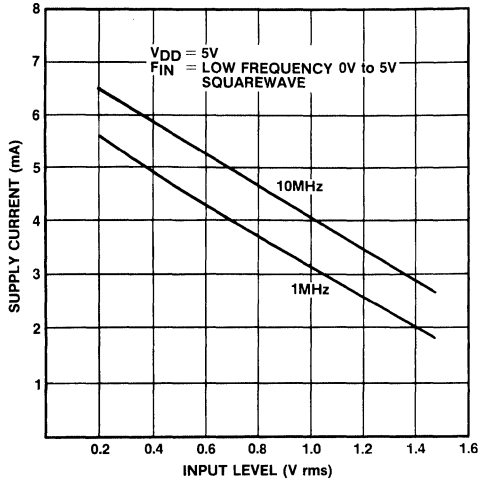


Fig.4 Typical supply current versus input level, Osc In

PROGRAMMING

Reference Divider Chain

The comparison frequency depends upon the crystal oscillator frequency and the division ratio of the R counter, which can be programmed in the range 3 to 2047.

$$R = \frac{fosc}{2 \times fcomp}$$

ie where *fcomp* = comparison frequency
fosc = oscillator frequency
R = R counter ratio

For example where crystal frequency = 10MHz and a channel spacing comparison frequency of 12.5kHz is required,

$$R = \frac{10^7}{2 \times 12.5 \times 10^3} = 400$$

Thus the R register would be programmed to 400 expressed in binary.
NB The total divider range is from 6 to 4094 in steps of 2.

VCO Divider Chain

The synthesised frequency of the voltage control oscillator (VCO) will depend on the division ratio of the M and A counters, the value of the external two modulus prescaler ($N/N + 1$) and the value of the comparison frequency *fcomp*.

The division ratio $P = NM + A$
where M is the ratio of the M counter in the range 3 to 1023 and *A* is the ratio of the A counter in the range 1 to 127
Note $M \geqslant A$

$$\text{Also } P = \frac{fvco}{fcomp}$$

For example if the desired VCO frequency = 275MHz, the comparison frequency is 12.5kHz and a two modulus prescaler of ÷64/65 is being used, then:

$$P = \frac{275 \times 10^6}{12.5 \times 10^3} = 22 \times 10^3$$

Now $P = NM + A$
which can be rearranged to be $P/N = M + A/N$
In our example we have

$$\frac{22 \times 10^3}{64} = M + \frac{A}{6} \text{ therefore } 343.75 = M + \frac{A}{64}$$

M is programmed to the integer part = 343 and *A* is programmed to the fractional part times 64
ie $A = 0.75 \times 64 = 48$
NB The minimum ratio that can be used is $N^2 - N$
To check $P = 343 \times 64 + 48 = 22000$ which is the required dividers ratio.

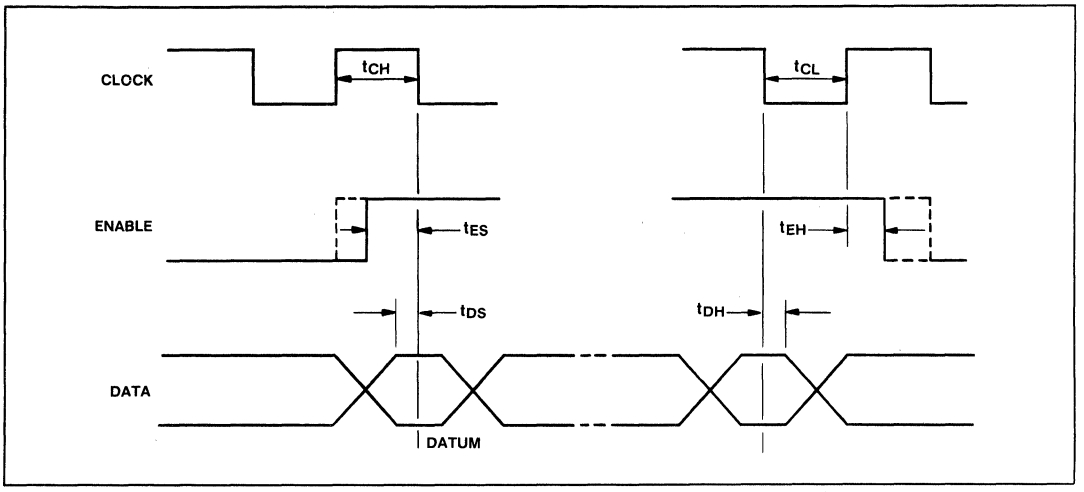


Fig.5 Timing diagram showing timing periods required for correct operation

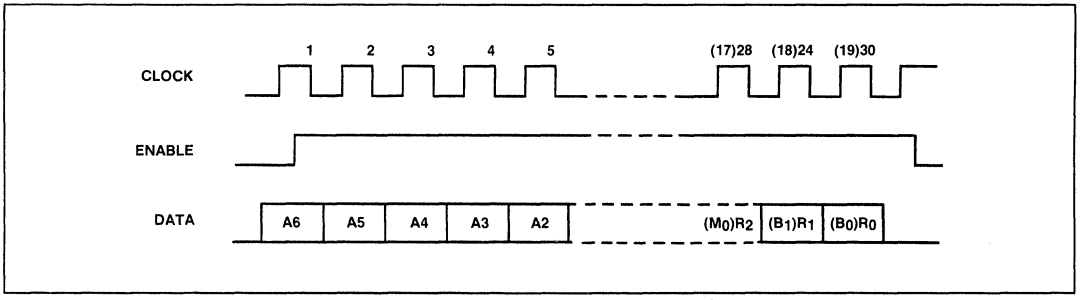


Fig.6 Timing diagram showing programming details

PHASE COMPARATORS

Noise output from a synthesiser loop is related to loop gain $K\Phi Kv/P$, where $K\Phi$ is phase detector constant (volts/rad), Kv is the VCO constant (rad-secs/volt) and P is the overall loop division ratio. When P is large and the loop gain is low, noise may be reduced by employing a phase comparator with a high gain. The sample and hold phase detector within the NJ88C25 has both a high gain and uses a double sampling technique to reduce spurious outputs to a low level.

A standard digital phase/frequency detetor driving a three-state output provides a 'coarse' error signal to enable fast switching between channels.

This output is active until the phase error is within the sample and hold phase detector window, when its output becomes high impedance. Phase-lock is indicated at this point with a low level on LD. The sample and hold phase detector provides a 'fine' error signal to give further phase adjustment and to hold the loop in lock.

An internally generated ramp controlled by the digital output from both the reference and main divider chains is sampled at the reference frequency to give the fine error signal, PDA. When in phase lock this output would typically be at $(V_{DD}-V_{SS})/2$ and any offset from this would be proportional to phase error.

The relationship between this offset voltage and the phase error is the phase-comparator gain which is programmable with an external resistor, RB and a capacitor, CAP.

An internal 50pF capacitor is used in the sample and hold comparator.

The gain is typically

$$GAIN = \frac{10\ |V_{DD} - V_{SS} - 0.7 - 89(RB^{-1/2})|}{2\pi\ |CAP + 50 \times 10^{-12}| \times RB \times FR}$$

The value of RB and CAP should be chosen to give the required gain at the reference frequency used.

Fig.8 shows that to achieve a gain of 380V per radian at 10kHz requires RB to be approximately 39kΩ, CAP is zero. A hold capacitor (CH) of non-critical value which might be typically 470pF is connected from CH to V_{SS}. A smaller value is sufficient if the sideband performance required is not high.

The output from the sample/phase detector should be combined with that of the coarse phase/frequency detector and filtered to generate a single control voltage to drive the VCO.

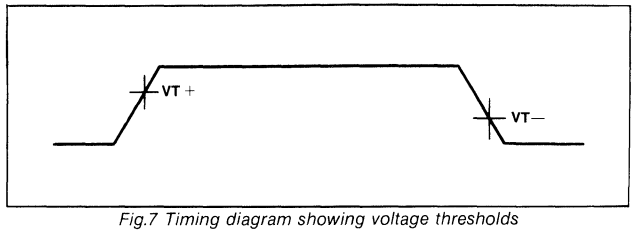
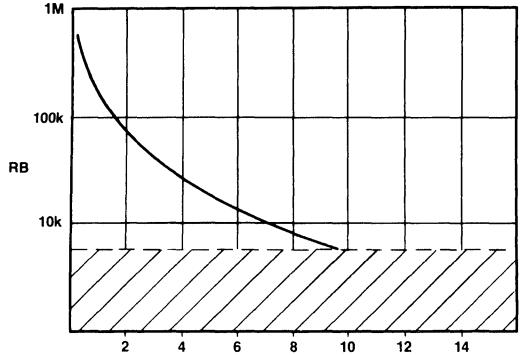


Fig.7 Timing diagram showing voltage thresholds



FR				
5kHz	400	800	1200	1600
10kHz	200	400	600	800
25kHz	80	160	240	320
	KΦ IN VOLTS/RAD.			

Fig.8 RB versus gain and reference frequency

NJ88C30

VHF SYNTHESISER

The NJ88C30 contains all the logic needed for a VHF PLL synthesiser and is fabricated on the Plessey high performance small geometry CMOS. The circuit contains a reference oscillator and divider, a two modulus prescaler and 4-bit control register, a 12-bit programmable divider, a phase comparator and the necessary data input and control logic.

FEATURES

- Low Power CMOS
- Easy to Use
- Low Cost
- Single Chip Synthesiser to VHF
- Lock Detect Output

APPLICATIONS

- Mobile Radios
- Hand Held Portable Radios
- Sonobuoys

ABSOLUTE MAXIMUM RATINGS

V_{DD}	-0.3V to +6V
Voltage on any pin	-0.3V to V_{DD} +0.3V
Operating temperature	-30°C to +70°C
Storage temperature	-55°C to +125°C

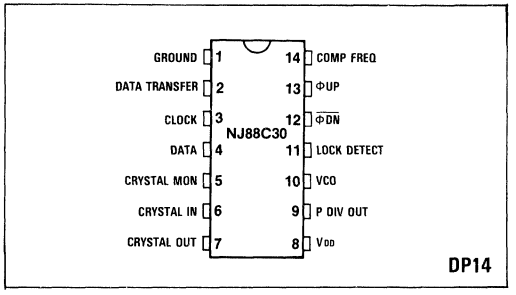


Fig.1 Pin connections (plastic DIL - top view)

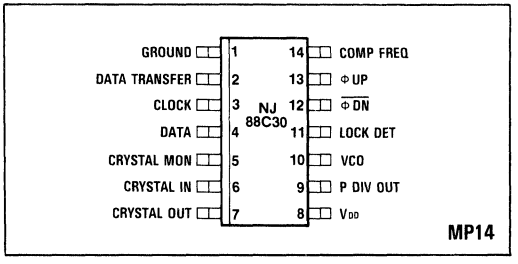


Fig.2 Pin connections (miniature plastic DIL - top view)

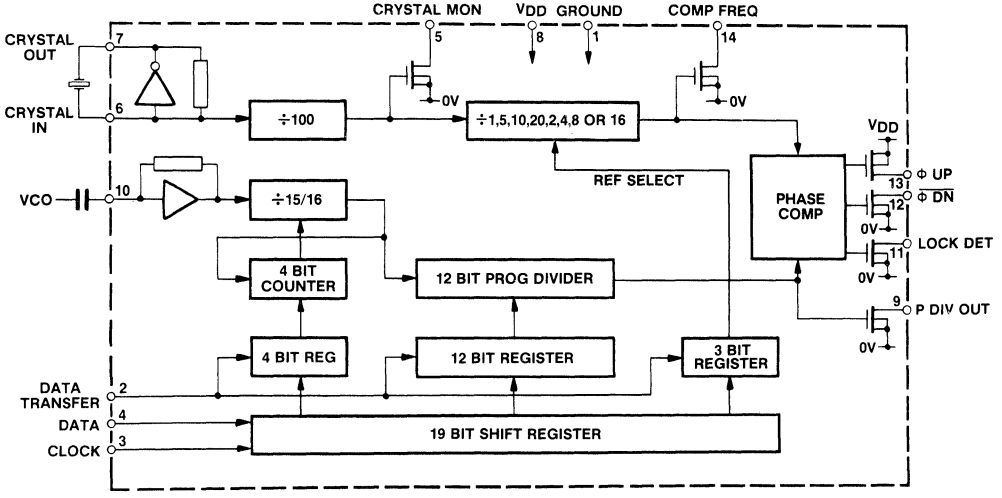
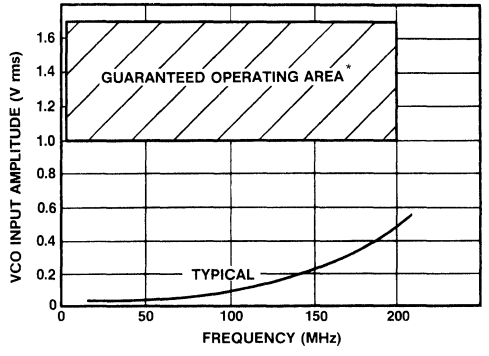


Fig.3 Functional block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = -30°C to +70°C, V_{DD} = 5V ± 0.5V

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply						
Supply current	8		4	7	mA	1V rms VCO input at 200MHz and f_{XTAL} = 10MHz
Crystal oscillator						
Frequency	6,7		10	15	MHz	Parallel resonant, fundamental crystal
External input level	6	1			V rms	AC coupled
High level	6	V_{DD}-1			V	DC coupled
Low level	6			1	V	DC coupled
VCO input						
VCO input sensitivity	10	1			V rms	At 200MHz, see Fig.4
Slew rate VCO input	10	4			V/μs	
VCO input impedance	10		5pF/10kΩ			
DATA, DATA TRANSFER, CLOCK inputs		V_{DD}-1				
High level	2,3,4				V	
Low level	2,3,4			1	V	
Rise, fall time	2,3			200	ns	
Data set up time	3,4	200			ns	See Fig.5
Clock frequency	3			2	MHz	
Transfer pulse width	2	500			ns	
Crystal monitor output						
Current sink	5	0.8			mA	V_{OUT} = 0.5V
Comp freq, LOCK DET, P DIV						
Current sink	9,11,14	1.6			mA	V_{OUT} = 0.5V
Φ UP/Φ DN						
Current sink	12	0.8			mA	V_{OUT} = 0.5V
Current source	13	0.8			mA	V_{OUT} = V_{DD} - 0.5V



*Tested as specified in table of Electrical Characteristics

Fig.4 Input sensitivity

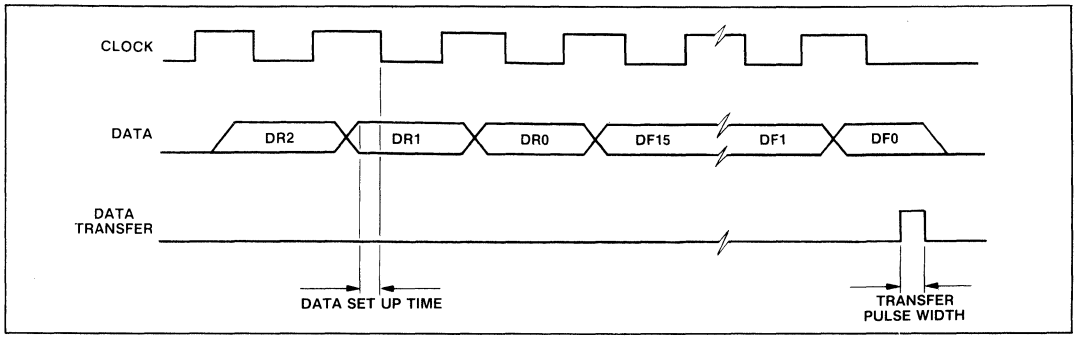


Fig.5 Input data timing diagram

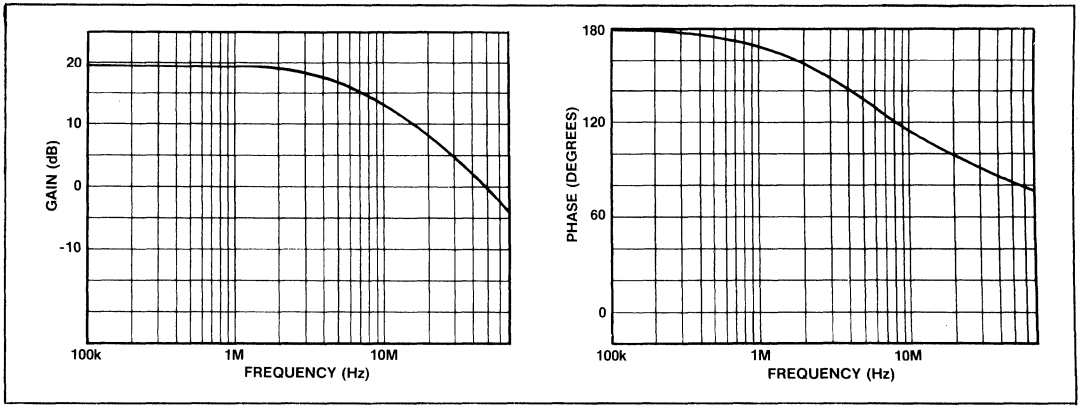


Fig.6 Gain phase characteristics of reference oscillator inverter

CIRCUIT DESCRIPTION

Crystal Oscillator and Reference Divider

The reference oscillator consists of a Pierce type oscillator intended for use with parallel resonant fundamental crystals. Typical gain and phase characteristics for the oscillator inverter are shown in Fig.6. An external reference oscillator may be used by either capacitively coupling a 1V rms sinewave into the CRYSTAL IN pin or if CMOS logic levels are available by connecting directly to CRYSTAL IN pin.

The reference oscillator drives a divider to produce a range of comparison frequencies which are selected by decoding the first three bits (DR2, DR1, DR0) of the input data. The possible division ratios and the comparison frequencies if a 10MHz crystal is used are shown in Fig.7.

DR2	DR1	DR0	Division Ratio	Comparison Frequency for 10MHz Ref. Osc.
0	0	0	1600	6.25kHz
0	0	1	800	12.5kHz
0	1	0	400	25kHz
0	1	1	200	50kHz
1	0	0	2000	5kHz
1	0	1	1000	10kHz
1	1	0	500	20kHz
1	1	1	100	100kHz

Fig.7 Reference divider division ratios

To assist in trimming the crystal, an open drain output at one hundredth of the reference oscillator frequency is provided on CRYSTAL MONITOR pin 1.

Programmable Divider

The programmable divider consits of a ÷15/16 two modulus prescaler with a 4-bit control register followed by a 12-bit programmable divider. A 1V rms sinewave should be capacitively coupled from the VCO to the divider input VCO pin.

The overall division ratio is selected by a single 16-bit word (DF 15 to 0) loaded through the serial data bus. A lower limit of 240 ensures correct prescaler operation; the upper limit is 65535. The VCO frequency in a locked system will be this division ratio multiplied by the comparison frequency.

Phase Comparator

The phase comparator consists of a digital type phase comparator with open drain Φ UP and $\overline{\Phi}$ DN outputs and an open drain lock detect output. Open drain outputs from the reference divider and programmable divider are provided for monitoring purposes or for use with an external phase comparator. Waveforms for all these outputs are shown in Fig.8. The duty cycle of Φ UP and $\overline{\Phi}$ DN versus phase difference are shown in Fig.9. The phase comparator is linear over a $\pm 2\pi$ range and if the phase gains or slips by more than 2π the phase comparator outputs repeat with a 2π period.

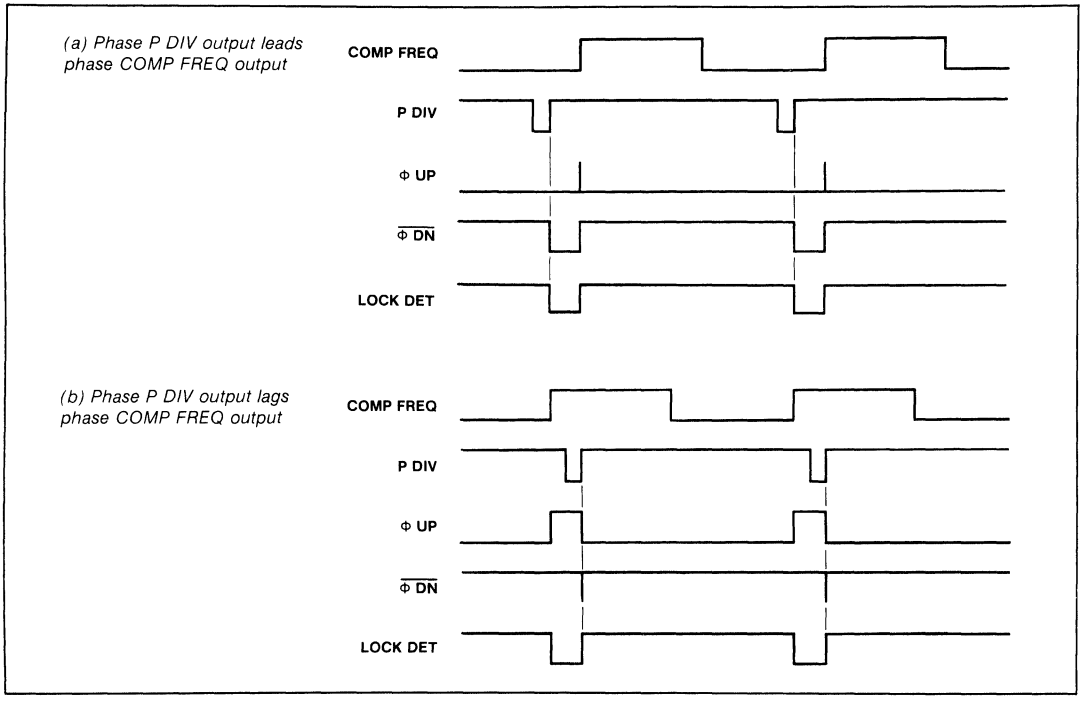


Fig.8 Phase comparator waveforms

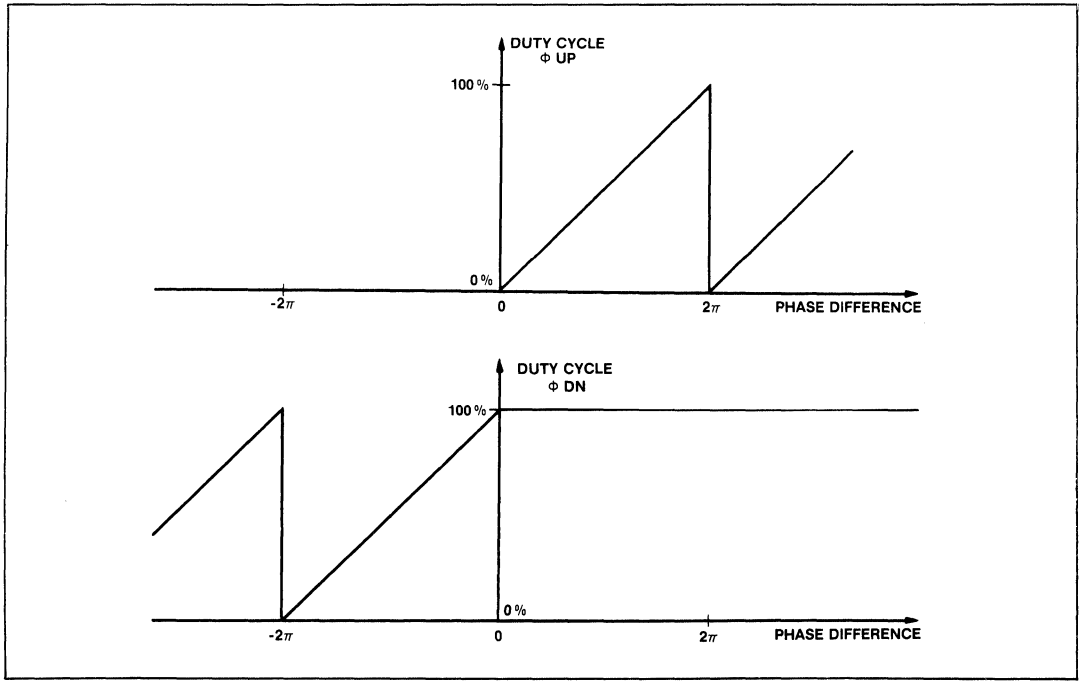


Fig.9 Phase comparator output characteristics

Once the phase difference exceeds 2π the comparator will gain or slip one cycle and then try to lock to the new zero phase difference. Note very narrow pulses may be seen on the inactive phase comparator output at the end of the pulse on the active output.

Data Input and Control Register

To control the synthesiser a simple three line serial input is used with Data, Clock and Data Transfer signals. The data consists of 19 bits, the first three DR2, DR1, DR0 control the reference divider, the next sixteen, DF15 to DF0, control the prescaler and programmable divider. Until the synthesiser receives the Data Transfer pulse it will use the previously loaded data; on receiving the pulse it will switch rapidly to the new data.

APPLICATIONS

A simplified circuit for a synthesiser intended for VHF broadcast receiver applications is shown in Fig.10. When the varicap line drive voltage necessary to tune the required band is greater than 5V, some form of level shifter such as the operational amplifier shown in Fig.10 is required. Pulses from the phase comparator are filtered by R_1, R_2 and C_1. Their values can be determined, given a required natural loop bandwidth ω_n and damping factor δ, by the following equations:

$$R_1C_1 = \frac{K}{\omega_n^2}, \quad R_2C_1 = \frac{2\delta}{\omega_n} \quad \text{and} \quad K = \frac{GK_0V_{CC}}{2\pi N}$$

where

ω - natural loop bandwidth (rad/s)
δ - damping factor
K_0 - VCO gain factor (rad/Vs)
V_{CC} - charge pump supply voltage (V)
N - division ratio = f_{OUT}/f_{COMP}
G - gain of amplifier

The values in Fig. 10 were calculated for:

ω_n = 3000 rad/s
δ = 0.707
K_0 = 18 Mrad/Vs
V_{CC} = 5V
f_{OUT} = 100MHz
f_{COMP} = 50kHz
G = 2

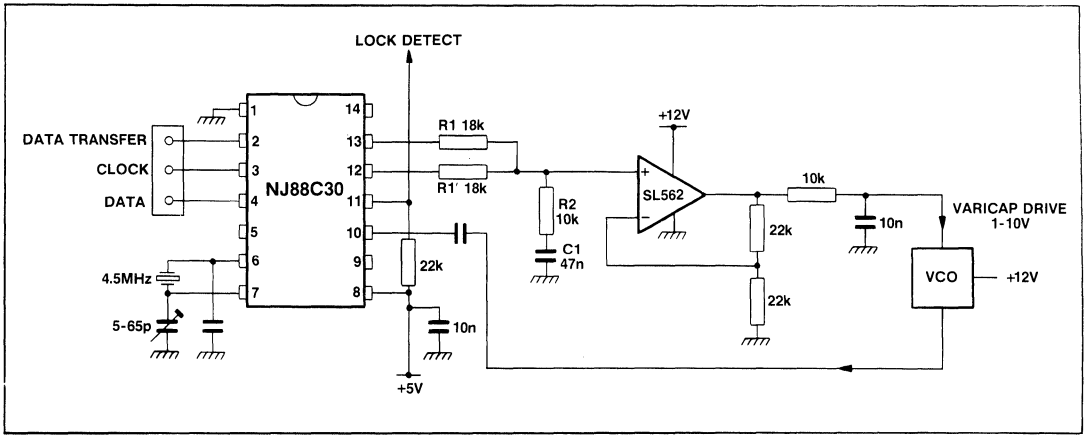


Fig.10 Typical application

Example of Programming

For a channel spacing (comparison frequency) of 5kHz when using a crystal oscillator of 10MHz the reference divider ratio will need to be 2000 (see Fig.7). This is programmed as binary 100 in the most significant three of the 19 bits (MSB programmed first).

To obtain the maximum VCO frequency of 200MHz the programmable divider ratio would be:

$$\frac{200 \times 10^6}{5 \times 10^3} = 40 \times 10^3 \text{ which is 9C40 Hex.}$$

The complete program word would then be:

	DR			DF															
	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Binary	1	0	0	1	0	0	1	1	1	0	0	0	1	0	0	0	0	0	0
Hex	4			9				C				4				0			

Using the same crystal and 5kHz channel spacing the minimum VCO frequency programmable would be 1.2MHz with the division ratio of 240 (= F0 Hex). The program word would then be:

	DR			DF															
	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Binary	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0
Hex	4			0				0				F				0			

PLESSEY
Semiconductors

NJ88C31

MF/VHF SYNTHESISER

The NJ88C31 contains all the logic needed for an MF/VHF PLL synthesiser and is fabricated on Plessey high performance small geometry CMOS. The circuit contains a reference oscillator and divider, a two modulus prescaler and 4-bit control register, a 12-bit programmable divider, a phase comparator and the necessary data input and control logic, and a 4.5MHz μP clock drive output.

FEATURES

- Low Power CMOS
- Easy To Use
- Low Cost
- Single Chip Synthesiser
- Lock Detect Output
- 4.5MHzμP Clock Output
- MF Band Prescaler Bypass Function
- Front End Disable for Very Low Power Standby
- Band Output to Switch Radio Between MF and VHF

APPLICATIONS

- AM/FM Radios
- Car Radios

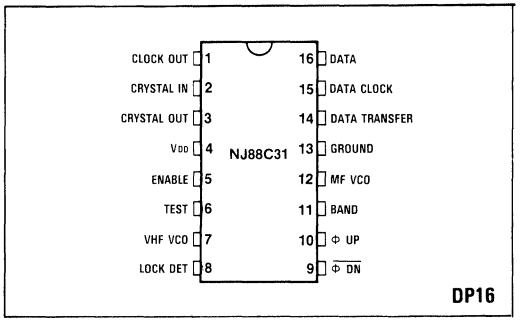


Fig.1 Pin connections (plastic DIL - top view)

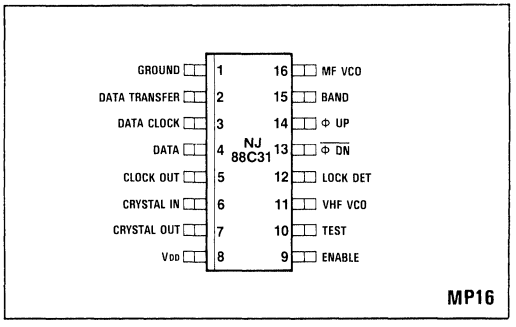


Fig.2 Pin connections (miniature plastic DIL - top view)

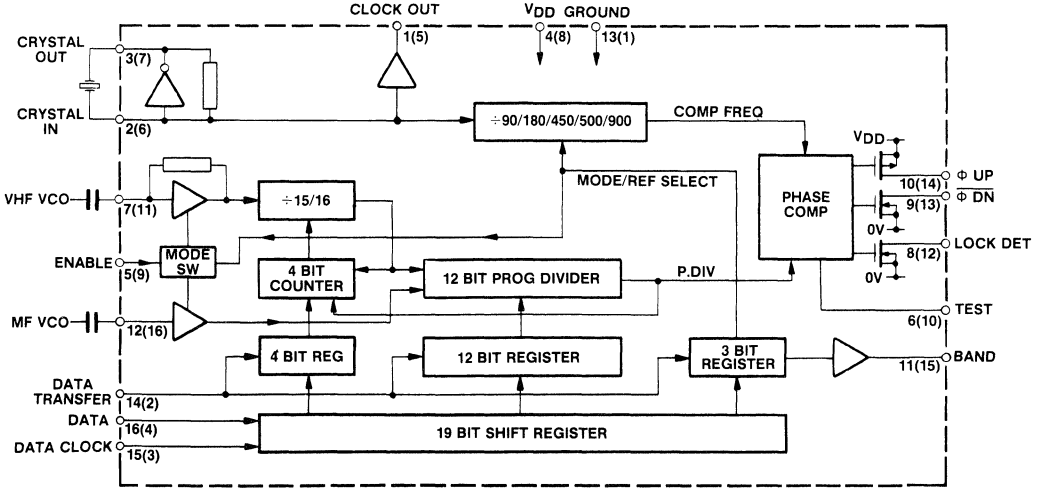


Fig.3 Functional block diagram. Pin numbers for MP package are shown in brackets.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = -30°C to +70°C, V_{DD} = 5V ± 0.5V

ABSOLUTE MAXIMUM RATINGS

V_{DD}	-0.3V to +6V
Voltage on any pin	-0.3V to V_{DD} +0.3V
Operating temperature	-30°C to +70°C
Storage temperature	-55°C to +125°C

Characteristic	Pin MP16	Pin DP16	Value Min.	Value Typ.	Value Max.	Units	Conditions
Supply							
Supply current	8	4		4	7	mA	1V rms VHF VCO input at 120MHz and f_{XTAL} = 4.5MHz
Supply current (Standby mode)					2	mA	f_{XTAL} = 4.5MHz, Enable low
Crystal oscillator							
Frequency	6,7	2,3		4.5	15	MHz	Parallel resonant, fundamental crystal
External input level	6	2	1			V rms	AC coupled
High level	6	2	V_{DD}-1			V	DC coupled
Low level	6	2			1	V	DC coupled
VCO inputs							
VHF VCO input sensitivity	13	7	0.3			V rms	At 50 to 125MHz, see Fig.4
MF VCO input sensitivity	16	12	0.3			V rms	At 0.1 to 2.5MHz
VCO input impedance	13,16	7,12		5pF/10kΩ			
DATA, DATA TRANSFER, DATA CLOCK, TEST and ENABLE inputs							
High level	2,3,4 9,10	5,6, 14,15,16	V_{DD}-1			V	
Low level	2,3,4, 9,10	5,6, 14,15,16			1	V	
Rise, fall time	2,3	14,15			200	ns	
Data set up time	3,4	15,16	200			ns	See Fig.5
Clock frequency	3	15			2	MHz	
Transfer pulse width	2	14	500			ns	
CLOCK OUT, BAND							
Current sink	5,15	1,11	0.8			mA	V_{OUT} = 0.5V
Current source	5,15	1,11	0.8			mA	V_{OUT} = V_{DD} -0.5V
LOCK DET							
Current sink	12	8	1.6			mA	V_{OUT} = 0.5V
Φ UP/$\overline{\Phi}$ DN, BAND							
Current sink	13	9	0.8			mA	V_{OUT} = 0.5V
Current source	14	10	0.8			mA	V_{OUT} = V_{DD} -0.5V

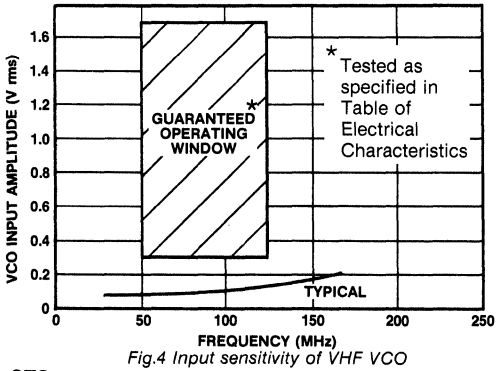


Fig.4 Input sensitivity of VHF VCO

CIRCUIT DESCRIPTION

Crystal Oscillator and Reference Divider

The reference oscillator consists of a Pierce type oscillator intended for use with parallel resonant fundamental crystals. Typical gain and phase characteristics for the oscillator inverter are shown in Fig.6. An external reference oscillator may be used by either capacitively coupling a 1V rms sinewave into the CRYSTAL IN pin or if CMOS logic levels are available by connecting directly to the CRYSTAL IN pin.

The reference oscillator drives a divider to produce a range of comparison frequencies which are selected by decoding the first three bits (DR2, DR1, DR0) of the input data. The possible division ratios and the comparison frequencies if a 4.5MHz crystal is used are shown in Fig.7.

There is a 4.5MHz μP clock drive output available on the CRYSTAL OUT pin.

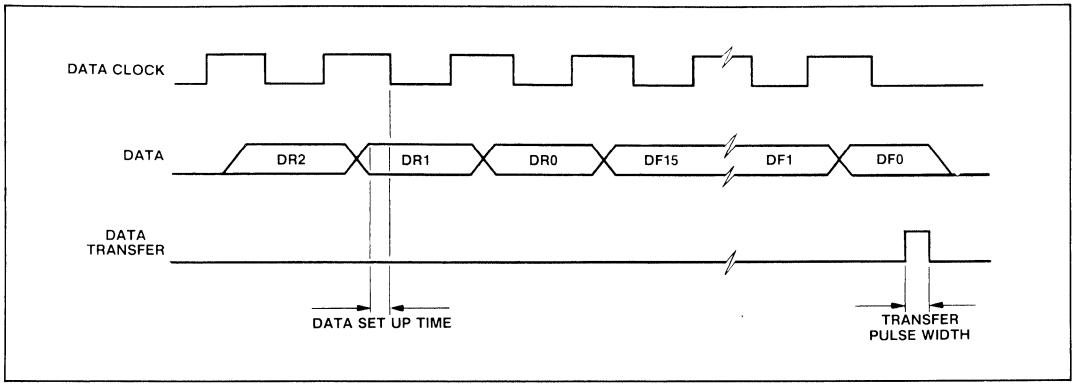


Fig.5 Input data timing diagram

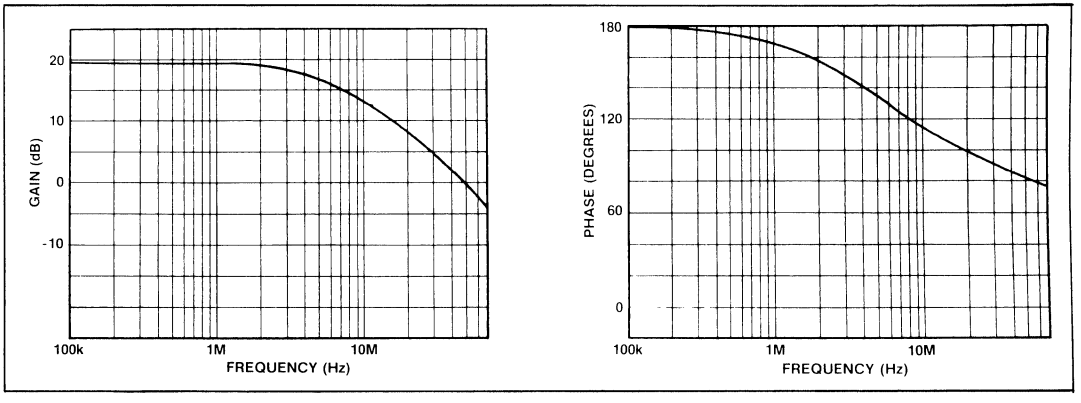


Fig.6 Gain phase characteristics of reference oscillator inverter

BAND Output

The programming bit DR2 is brought out as a BAND output, '1' for MF band and '0' for VHF.

DR2	DR1	DR0	Division Ratio	Comparison Frequency 4.5MHz XTAL	BAND
0	0	0	90	50kHz	VHF
0	0	1	180	25kHz	
0	1	0	450	10kHz	
1	0	0	450	10kHz	MF
1	0	1	500	9kHz	
1	1	0	900	5kHz	

Fig.7 Reference divider division ratios

Programmable Divider

The programmable divider consists of a 12-bit divider preceded on FM by a divide by 15/16 two modulus divider. The F/M input is fed through an amplifier to provide adequate sensitivity.

TEST Input

When the TEST pin is taken to a logic 1, the Φ UP pin is connected to the output of the reference chain divider (COMP FREQ) and the $\overline{\Phi \text{ DN}}$ pin is connected to the output of the 12-bit programmable signal chain divider (PROG DIV); this mode is normally only used in factory testing.

Phase Comparator

The digital phase comparator has three open drain outputs; Φ UP and $\overline{\Phi \text{ DN}}$ drive the charge pump and LOCK DETECT may be integrated to generate a MUTE signal. Waveforms for all these outputs are shown in Fig.8. The duty cycle of Φ UP and $\overline{\Phi \text{ DN}}$ versus phase difference are shown in Fig.9. The phase comparator is linear over a $\pm 2\pi$ range and if the phase gains or slips by more than 2π the phase comparator outputs repeat with a 2π period. Once the phase difference exceeds 2π the comparator will gain or slip one cycle and then try to lock to the new zero phase difference. Note very narrow pulses may be seen on the inactive phase comparator output at the end of the pulse on the active output.

ENABLE Input

When ENABLE is taken to logic '0' both VCO input buffers and the prescaler are switched off to save power. The crystal oscillator, CLOCK OUT and control registers continue working normally, such that when ENABLE is taken to a '1' the device will retune the last programmed frequency.

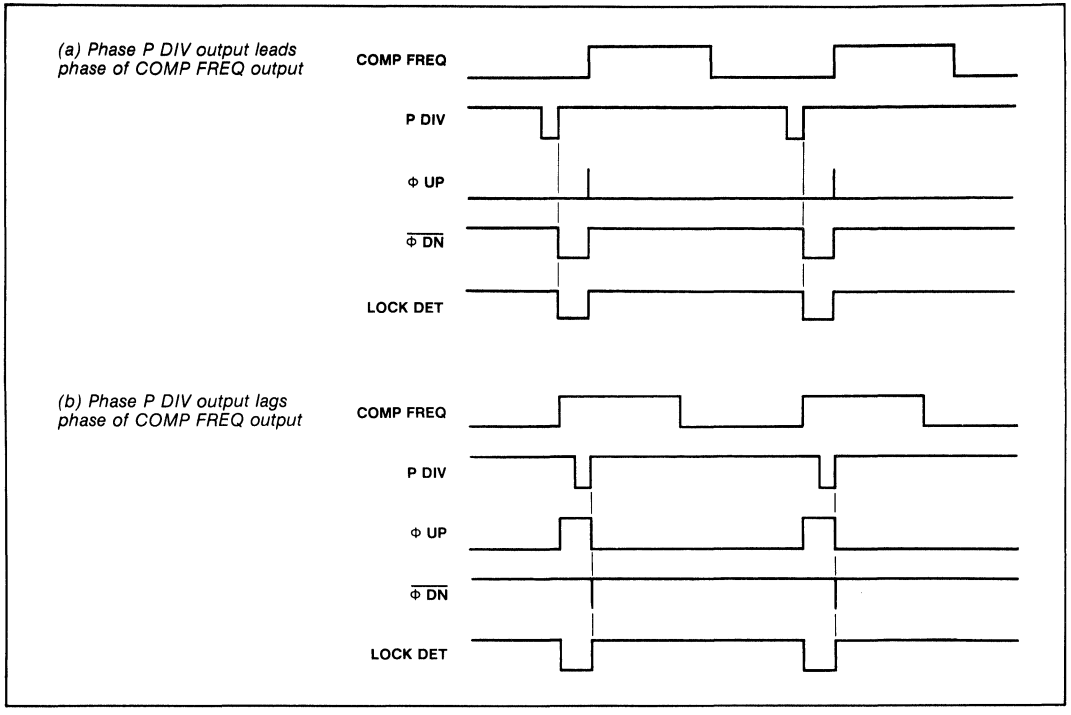


Fig.8 Phase comparator waveforms

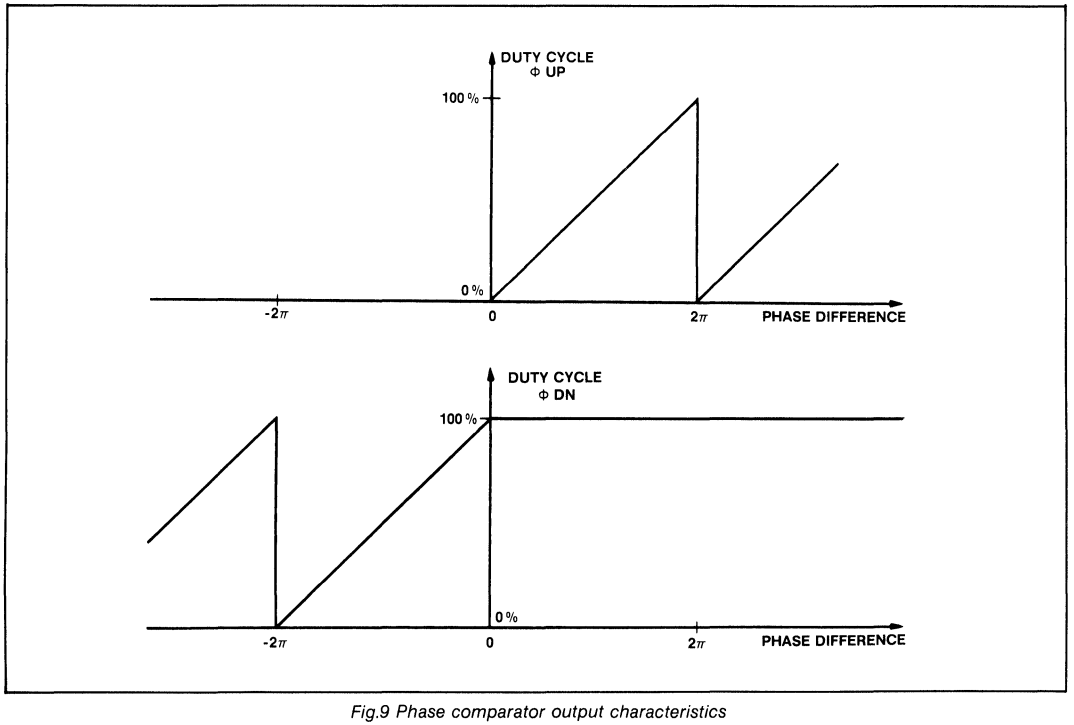


Fig.9 Phase comparator output characteristics

Data Input and Control Register

To control the synthesiser a simple three line serial input is used with Data, Clock and Data Transfer signals. The data consists of 19 bits, the first three DR2, DR1, DR0 control the reference divider, the next sixteen, DF15 to DF0, control the prescaler and programmable divider. Until the synthesiser receives the Data Transfer pulse it will use the previously loaded data; on receiving the pulse it will switch rapidly to the new data. See Fig.5.

APPLICATIONS

A simplified circuit for a synthesiser intended for VHF broadcast receiver applications is shown in Fig.10. When the varicap line drive voltage necessary to tune the required band is greater than 5V, some form of level shifter such as the operational amplifier shown in Fig.10 is required.Pulses from the phase comparator are filtered by R_1, R_2, and C_1. Their values can be determined, given a required natural loop bandwidth ω_n and damping factor δ, by the following equations:

$$R_1C_1 = \frac{K}{\omega_n^2}, \quad R_2C_1 = \frac{2\delta}{\omega_n} \quad \text{and} \quad K = \frac{K_0 \times V_{CC} \times G}{2\pi N}$$

where

ω - natural loop bandwidth (rad/s)
δ - damping factor
K_0 - VCO gain factor (rad/Vs)
V_{CC} - charge pump supply voltage (V)
N - division ratio = f_{OUT}/f_{COMP}
G - Gain of amplifier

The values in Fig.10 were calculated for:

ω = 3000 rad/s
δ = 0.707
K_0 = 18 Mrad/Vs
V_{CC} = 5V
f_{OUT} = 100MHz
f_{COMP} = 25kHz
G = 2

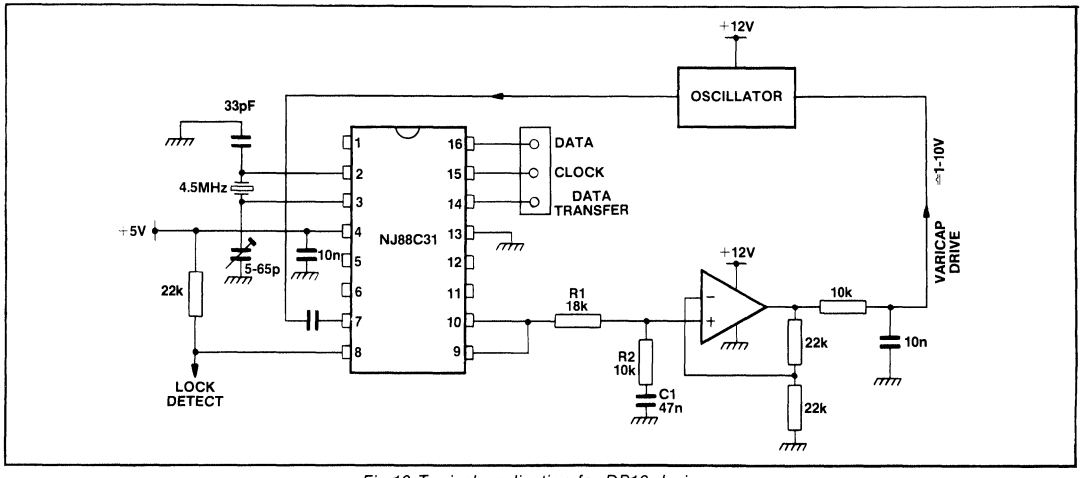


Fig.10 Typical application for DP16 device

Example of Programming

VHF section

For a channel spacing (comparison frequency) of 10kHz when using a crystal oscillator of 4.5MHz, the reference divider ratio will need to be 450 (see Fig.7). This is programmed as binary 010 in the most significant three bits of the 19 bit data word (MSB programmed first).

To obtain a VCO frequency of 125MHz the programmable divider ratio would be:

$$\frac{125 \times 10^6}{10 \times 10^3} = 12500 = 30D4 \text{ Hex.}$$

The programming word would be:

	DR			DF															
Bit No.	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Binary	0	1	0	0	0	1	1	0	0	0	0	1	1	0	1	0	1	0	0
Hex	2			3				0				D				4			

MF section

The four least significant bits of DF are not used in programming the programmable divider ratio, but nevertheless a total of 19 bits must be supplied.

For a channel spacing of 5kHz when using a crystal oscillator of 4.5MHz, the reference divider ratio will be 900 (see Fig.7). This is programmed as 110 in the most significant bits of the 19 bit word (MSB is programmed first).

To obtain a frequency of 2.5MHz the programmable divider ratio would need to be 500. The value programmed into the DP register must be the desired ratio minus one, i.e. in this case 499 which is 1F3 Hex.

The programming word would be:

	DR			DF															
Bit No.	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Binary	1	1	0	0	0	0	1	1	1	1	1	0	0	1	1	X	X	X	X
Hex	6			1				F				3				DON'T CARE			

PLESSEY
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This information is for sample evaluation only. Final specification will take account of market demands.

SP2001

DIRECT DIGITAL SYNTHESISER WITH 100MHz OUTPUT

The SP2001 Direct Digital Frequency Synthesiser (DDFS) is an ECL 100K compatible 'numerically controlled oscillator' i.e. it directly generates the DAC code required for an output sinewave anywhere within the output range 5kHz to 100 MHz. A block diagram of the full synthesiser is included in Fig 2.

FEATURES

- Maximum Clock Frequency >350MHz
- 16-Bit Resolution
- 8-Bit Parallel Cosine Output
- ECL 100K Compatible Inputs and Outputs
- 40-lead Sidebrazed Ceramic DIL Package
- Maximum Output Frequency >100MHz
- Useable with 5, 10, 15 or 30kHz Channel Spacing
- Useable with 3.125, 6.25, 12.5 or 25kHz Channel Spacing
- Asynchronous Data Load for Fast (17ns) Hop Time
- Low Power: 1.85W
- Very Low Close-to-Carrier Noise,-135dBc/Hz

APPLICATIONS

- Local Oscillator Transmitter Synthesis in VHF Low Band (30 - 100MHz)
- LO Synthesis in Frequency Agile Radio/Radar
- Wide Single - Range Sinewave Generator
- ECM/ECCM - e.g Follower Jammers or Fast Hoppers

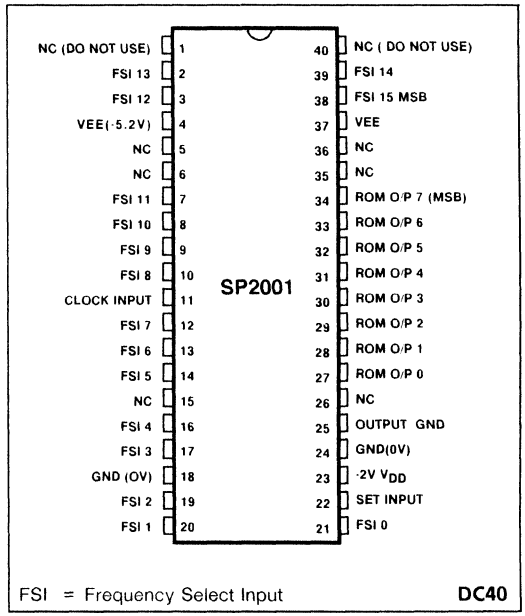


Fig.1 Pin connections - top view

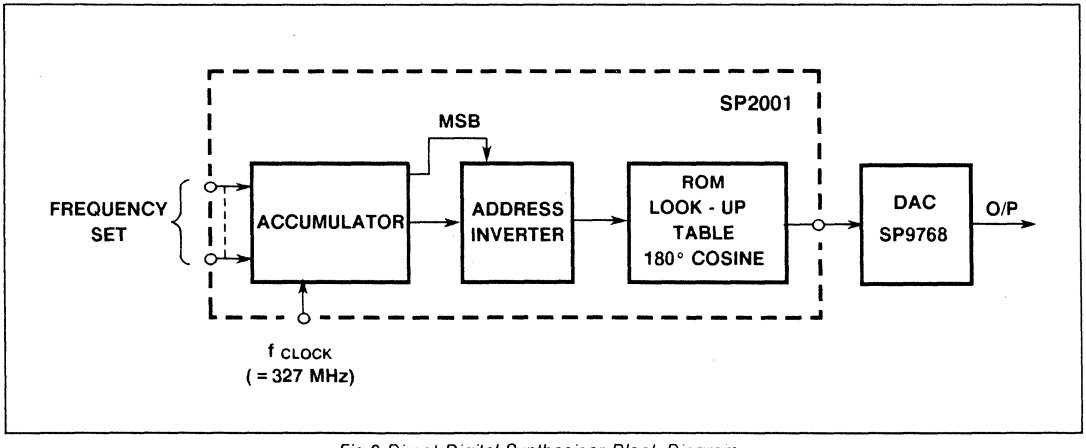


Fig.2 Direct Digital Synthesiser Block Diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

V_{EE} = -5.2V, V_{CC} = GND, V_{DD} = -2.0V, T_{case} = -10°C to + 85°C

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Input HIGH voltage		-1125		-880	mV	
Input LOW voltage		-1810		-1520	mV	
Output HIGH voltage		-1025	-955	-880	mV	Loaded with 50Ω to -2V
Output LOW voltage		-1810	-1705	-1620	mV	Loaded with 50Ω to -2V
I_{EE} supply current			310		mA	
I_{DD} supply current			125		mA	

ABSOLUTE MAXIMUM RATINGS

Storage temperature	-65°C to +150°C
Max. junction temperature	+150°C
Case temperature in operation	-55°C to +150°C
Max. voltage between V_{EE} & V_{CC}	-7.0V to +0.5V
Input voltage (DC)	V_{EE} to (V_{CC} +0.5)V
Output current at V_O = V_{OH}	-20mA
ECL termination supply	-1.75V to -2.25V

CIRCUIT DESCRIPTION

The SP2001 is a digital direct frequency synthesiser with an output frequency of 5Khz to 100 MHz, in a single range, at 5kHz channel spacing. Alternative clock frequencies will lead to different channel spacing. The circuit needs no reactive components at all (except power supply decoupling capacitors) and is under full digital control at all times, including during the phase-coherent frequency transitions. Frequency accuracy is set by an external clock oscillator; close-to-carrier noise levels on the synthesiser output are dominated by the clock performance.

The fully digital system does not contain control loops, so that 'hop' time between discrete output frequencies is limited in principle only by the digital to analog converter settling time of about 5ns. In practice, to simplify the logic, a further four clock periods of delay have been added; the resultant total of 17ns worst case is about five orders of magnitude faster than loop synthesisers. The block diagram (Fig.2) shows a full DDFS, including the recommended Plessey SP9768 Digital to Analog Converter.

The function of the blocks can be seen from Fig.2. To avoid the need for storage of a full 360 degrees in the ROM, the MSB output of the accumulator is used as a sign inverter, which with the LSBs, forms a digitised triangular number sequence. The ROM contains the data for 180 degrees, stored in a cosine sequence in this instance. ROM size is 1K bit (128 x 8 bits) and with the reflection about zero implicit in the 180° storage, this is equivalent to 256 words of data i.e. the storage density is equal to the word length.

The data passes through retiming latches at each stage including the output in order to provide accurate data at the high clock rate; pipeline delays are unimportant in a non-looped system.

Finally, the DAC constructs the output waveform, which consists of discrete points on the sinusoid. Interpolation could be carried out by low-pass filtering; in practice, no filters were used except the inherent low-pass action of the DAC.

Performance of the system is to some extent limited by the maximum update rate of the DAC used. The recommended SP9768 will typically update to ±½ LSB at over 200MHz. When the clock is running at 327.68MHz, the DAC achieves 5-6 bits accuracy but is otherwise unimpaired in operation. When the output is 100MHz, a spurious rejection of 32dBc is obtained. The largest spurs are at (327.68-3 × 100)MHz and (4 × 100-327- 68) MHz. At 10MHz output, using the same programme code, with 32.768MHz clock, the largest spur is at -38dBc, although this is a frequency which would be removed by low pass filtering. The true spur level is -46dBc, close to the theoretical limit for an 8-bit system. Close-to-carrier noise is very good and is dominated by the clock source; separate measurements indicate a noise floor of better than -135dBc/Hz at ±25kHz.

Measurement of close-to-carrier spurs involves the use of an extremely wide dynamic range receiver. This was achieved by using a Hewlett-Packard 3047A/11740A Microwave Phase Noise Measurement System, with a signal generator type HP8662A. Measurements are of course channel specific; the 'cleanest' channels occur when the channel selected is a whole binary number such as 00010000 0000 0000. Channels close to this, e.g. one channel away, contain small close-to-carrier components generally at a spacing dependent on the ratio between the output frequency and the clock. Typically, at $f_{OUT} = f_{CLOCK}/4$, and $f_{INCREMENT}$ = 5kHz, the spurs are at ±20kHz.

The 'SET' input (pin 22) provides a 'start from zero' as a test facility. It sets all accumulator latches to zero so that the output is the ROM zeros state.

The frequency equation is:

$$f_{OUT} = \frac{f_{CLOCK}}{2^{16}} \times \textit{Input Data}$$

e.g. For 5kHz increments , f_{CLOCK} = 327.68MHz.
For 3.125kHz increments , f_{CLOCK} = 204.8Hz.

TIMING

The channel selection data is parallel asynchronously loaded so timing is uncritical. Internal latching of the device pipelines the data, so there is a through delay of 4 clock periods plus 400ps from change of input data. Minimum channel re-selection time is therefore approximately 12ns plus DAC settling time. In a worst case, one further clock period should be allowed.

SP8850

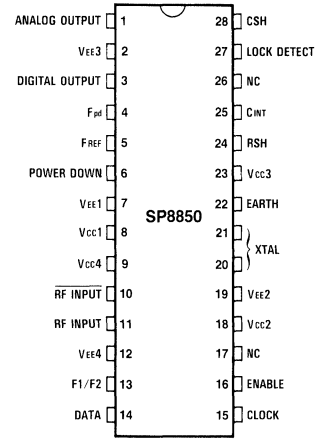
1.5GHz PROFESSIONAL SYNTHESISER

The SP8850 is a low power single chip synthesiser intended for professional radio communications containing all the elements (apart from the loop amplifier) to fabricate a PLL frequency synthesis loop.

The device is serially programmable by a three wire data highway and contains three independent buffers to store one reference divider word and two local oscillator divider words.

Analog and digital phase comparators are provided and both gain and output phase are programmable via the divider buffers. The preset tandem operation of the phase detectors can be overwritten or the comparison frequencies switched to output ports under control of the divider word. The dual modulus ratio and therefore operation range is also programmable through the same word.

A power down mode is incorporated as a battery economy feature.



Pin out

VCC1, VEE1 - ECL Supplies
VCC2, VEE2 - Oscillator Supplies
VCC3, VEE3 - Analog Detector Supplies
VCC4, VEE4 - Preamp and 16/17

DG28

Fig.1 Pin connections - top view

FEATURES

- Low Operating Power, Typically 125mW
- 1.5GHz Operating Frequency
- Complete Phase Locked Loop
- High Input Sensitivity
- Programmed through Three Wire Data Bus
- Wide Range of Reference Division Ratios
- Wide range of Local Oscillator Division Ratios
- Local Storage for Two Frequency Words giving Rapid Frequency Toggling
- Integrated Analog and Digital Phase Detectors
- Programmable Phase Detector Gain
- Power Down Mode
- ESD Protection on all Pins

ASBOLUTE MAXIMUM RATINGS

Supply voltage	-0.3V to 7V
Storage temperature	-55°C to +150°C
Operating temperature	-55°C to +125°C
Prescaler input voltage	2.5V p-p

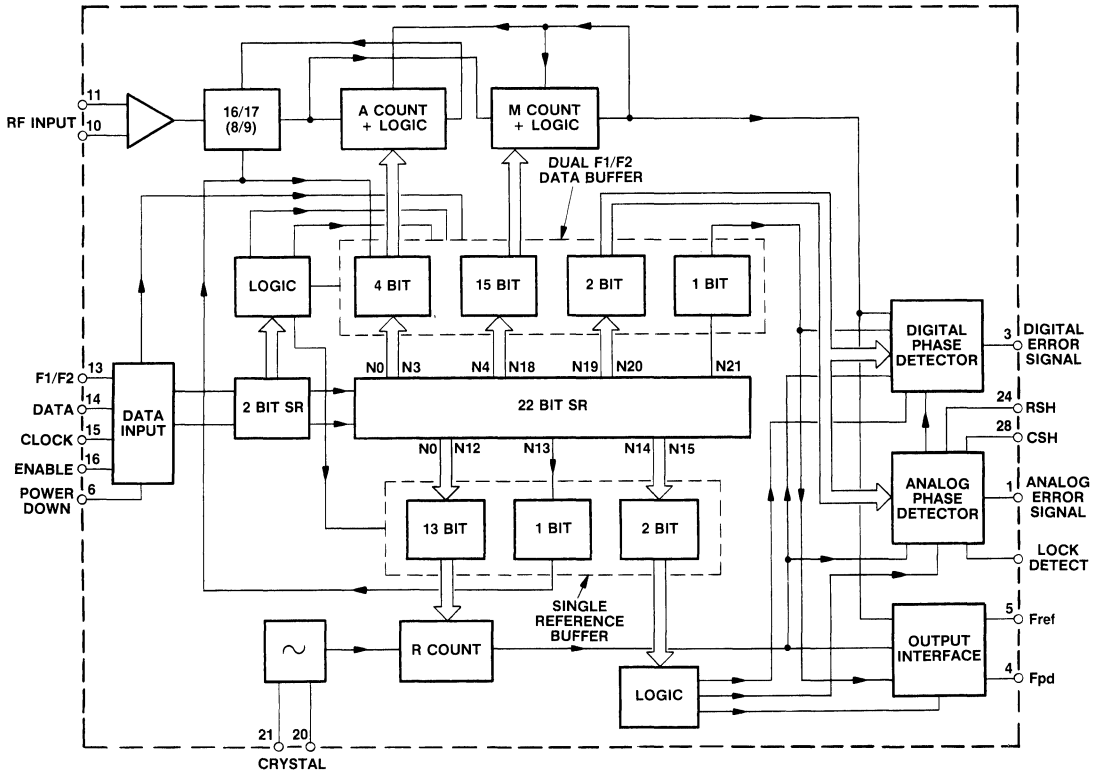


Fig.2 SP8850 block diagram

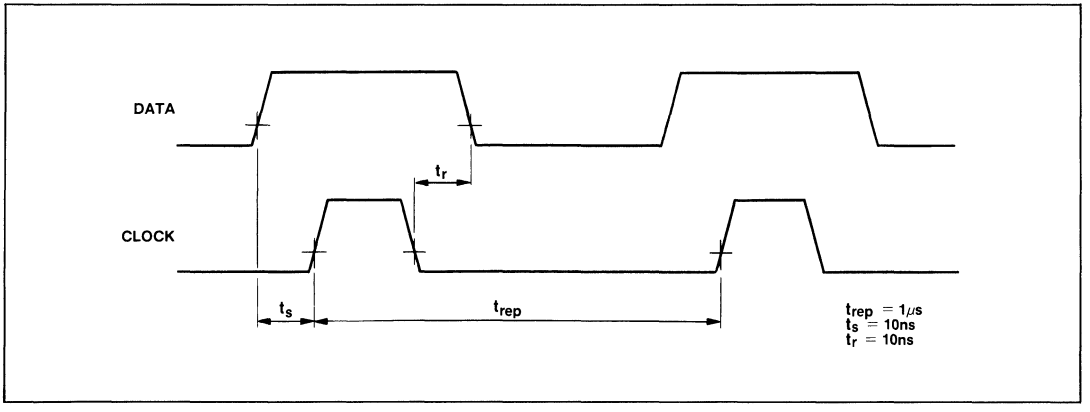


Fig.3 Clock and data timing requirements

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = -55°C to +125°C, V_{CC} = +4.75V to +5.25V

Characteristic		Pin	Value			Units	Conditions
			Min.	Typ.	Max.		
Supply current				25		mA	
Input sensitivity	80MHz			17.5		mV rms	
	150MHz			10		mV rms	
	0.9GHz			10		mV rms	
	1GHz			17.5		mV rms	
	1.5GHz			50		mV rms	
Input overload			300			mV rms	
Input impedance				50		Ohms	
				2		pF	
RF input division ratio			240		524303		With 16/17 selected
			56		262151		With 8/9 selected
Comparison frequency					2.5	MHz	
Reference oscillator			4		20	MHz	
Reference division ratio			2		8192		
Data clock repetition rate t_{rep}					1	μs	
Minimum set up time t_s			10			ns	
Minimum release time t_r			10			ns	
Data input	High		0.5 V_{CC}			V	
	Low				0.3 V_{CC}	V	
Data enable	High		0.5 V_{CC}			V	
	Low				0.3 V_{CC}	V	
F1/F2 input	High		0.5V cc			V	F1 buffer selected
	Low				0.3 V_{CC}	V	F2 buffer selected

DESCRIPTION

The programmable divider chain is of AM counter construction and therefore contains a dual modulus front end prescaler, an A counter which controls the dual modulus ratio and an M counter which performs the bulk multi-modulus division. A programmable divider of this construction has a division ratio of MN + A and a minimum integer steppable division ratio of N(N - 1).

In the SP8850 the dual modulus front end prescaler is a dual N ratio device capable of being statically switched between 16/17 and 8/9 ratios. The controlling A counter is of four bit design enabling a maximum count sequence of 15, (2^4 - 1) which begins with the start of the M counter sequence and stops when it has counted by the preloaded number of cycles. Whilst the A counter is counting the dual modulus prescaler is held in the N + 1 mode, then relaxes back to the N mode at the completion of the A sequence. The M counter is a 15-bit asynchronous divider which counts with a ratio set by a control word. In both A and M counters the controlling data from the F1/F2 buffer is loaded in sequence with every M count cycle. The N ratio of the dual modulus prescaler is selected by a one bit word in the reference divider buffer and, when a ratio of 8/9 is selected the A counter is automatically switched to three bits, having an impact on the frequency bit allocation as described in the data entry section.

Reference Source

The reference source in the SP8850 is obtained from an on board oscillator, frequency controlled by an external crystal. The oscillator can also function as a buffer amplifier allowing the use of an external reference source. In this mode the source is simply AC coupled into the oscillator.

The oscillator output is coupled to a programmable reference divider whose output is the reference source for the phase detector. The reference divider is a fully programmable 13-bit asynchronous design and can be set to any division ratio between 2 and 8192. The actual division ratio is controlled by a data word stored in the internal reference data buffer.

Phase Comparator

In order to improve performance in phase locked and unlocked conditions, the SP8850 is provided with both digital and analog phase comparators. The digital comparator is sensitive to both frequency and phase errors over a wide linear range and is designed to rapidly bring the loop close to phase lock. The analog sample and hold comparator brings the loop into final phase lock and holds it in this condition with minimum sideband generation. In normal operation the digital phase comparator is automatically disabled when the loop phase error is within the linear range of the analog comparator.

The automatic switching from digital to analog comparators may be overwritten by an internal two bit control word, stored in the reference divider buffer. Using this word, the loop can be switched to internal digital control only or both can be disabled and the local oscillator and reference divider signals switched to output pins allowing use of an external phase detector.

There are three further control bits associated with the phase detectors which are stored in the F1/F2 buffer. The

first bit controls the sense of the phase detector, allowing for inversions of control direction in the external loop. The other two bits are an internal gain control for the phase detectors allowing compensation for local oscillator control slope changes over the band, so maintaining close to optimum loop parameters (see Table 1).

MSB	LSB	Digital	Analog
0	0	50μA	1
0	1	75μA	1.5
1	0	125μA	2.5
1	1	200μA	4

Table 1

Note: **Digital** *is charge pump current,* **Analog** *is multiplication factor of externally set gain.*

The unit gain of the digital detector is controlled by the integration capacitor in the loop amplifier. The analog gain is set by an external resistor R and the hold time constant by the external capacitor C. In operation the two detectors will be summed into the loop amplifier and the ratio of the two gains set by the series resistance in the analog detector output. See the application circuit diagram.

A lock detect circuit gives an output when the analog phase comparator is within the linear range of operation.

Data Entry and Storage

The data section of the SP8850 consists of a data input interface, an internal data shift register and three internal data buffers.

Data is entered to the data input interface by a three wire data highway with data, clock and chip enable inputs. The input interface then routes this data to a 24-bit shift register with bus connections to three data buffers. Data entered via the serial bus is transferred to the appropriate data buffer on the negative transition of the chip enable input according to the two final data bits as shown in Table 2.

The dual F1/F2 buffer can receive two 22-bit words and controls the programmable divider A and M counters using 19-bits, the phase detector gain with two bits and the phase detector sense with one bit. A fourth input from the synthesiser control system selects the active buffer.

Output for RF phase lag		
Sense bit	**Digital detector**	**Analog detector**
0	Current source	+ve
1	Current sink	-ve

The third buffer contains only 16 bits, 13 being used to set the reference counter division ratio, and 2 to control the phase comparator enable logic. The remaining bit sets the dual modulus prescaler N ratio.

2 Bit S.R. Contents	Buffer Loaded
00	F1
01	F2
10	ACTIVE A*
11	REFERENCE

Table 2

** Transfer of A counter bits into buffer controlling the programmable counter.*

The data words may be entered in any individual or multiple sequence and the shift register can be updated whilst the data buffers retain control of the synthesiser with the previously loaded data. This enables four unique data words to be stored in the device, with three in the data buffers and a fourth in the shift register, whilst the chip is enabled. F1 word may also be updated whilst F2 is controlling the programmable divider and vice versa.

The dual F1/F2 buffer enables the device to be toggled between two frequencies using the F1/F2 select input at a rate determined by the comparison frequency and also enables random frequency hopping at a rate determined by a byte load period, since the loop can be locked to F1 whilst F2 is updated by entering new data via the shift register.

An F1 or F2 update cycle will consist of a byte containing 24 bits, whereas the reference byte will contain 18 bits. The device requires 3 bytes, each with a chip select sequence, totalling 66 bits to fully program.

When the dual modulus counter (A count) is set to ÷8/9, the data required to set the counter is reduced by one bit, leaving a redundant bit in the 22-bit F1/F2 buffer. Various programming sequences are shown in Fig.5.

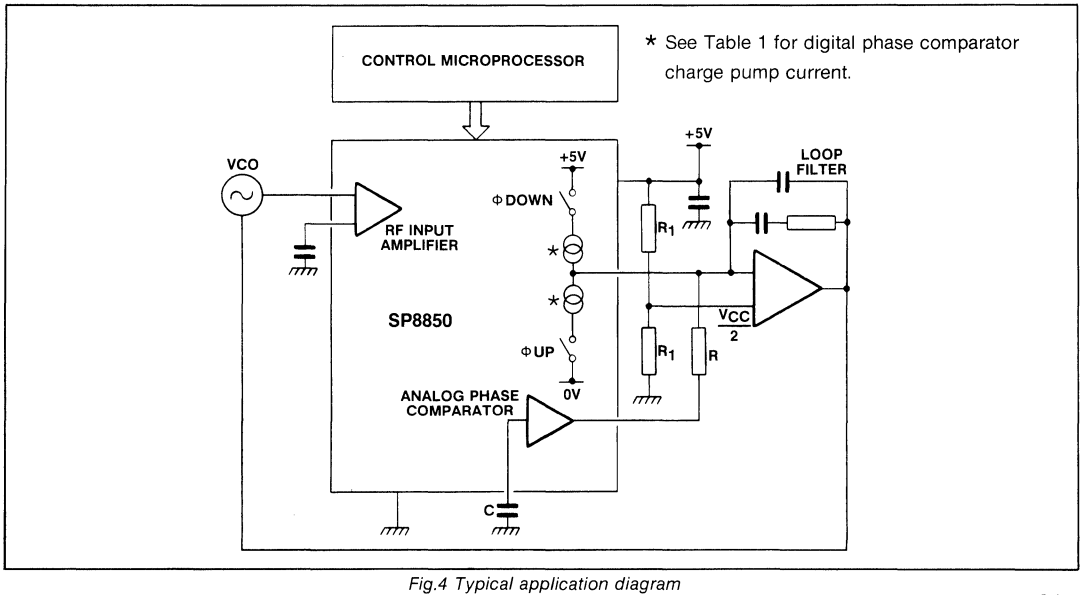


Fig.4 Typical application diagram

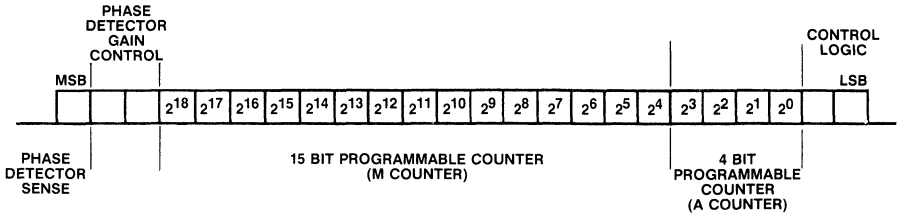


Fig.5(a) F1 or F2 word, bit allocation with 16/17 selected

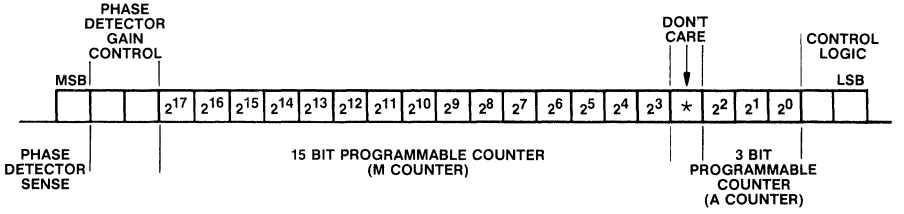


Fig.5(b) F1 or F2 word, bit allocation with 8/9 selected

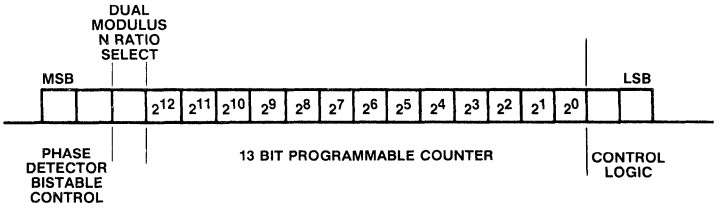


Fig.5(c) Reference word bit allocation

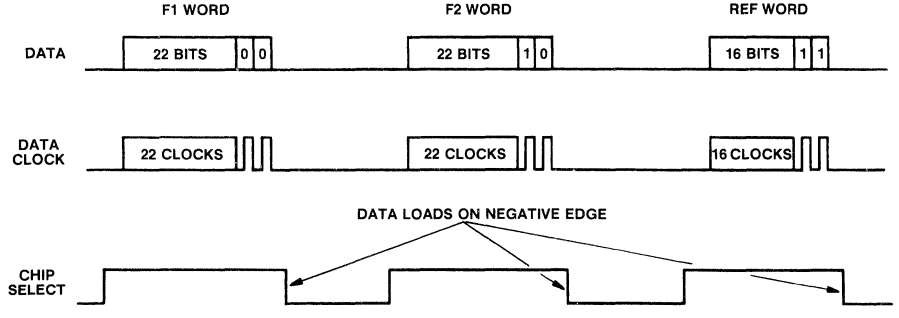


Fig.5(d) Typical data load sequence

Fig.5 Data format diagrams

Application Notes

Phase Noise Intermodulation and Dynamic Range

The radio receiver operates in a non-benign environment. It needs to pick out a very weak wanted signal from a background of noise at the same time as it rejects a large number of much stronger unwanted signals. These may be present either fortuitously, as in the case of the overcrowded radio spectrum, or because of deliberate action, as in the case of Electronic Warfare. In either case, the use of suitable devices may considerably influence the job of the equipment designer.

Dynamic range is a 'catch all' term, applied to limitations of intermodulation or phase noise: it has many definitions depending upon the application. Firstly, however, it is advisable to define those terms which limit the dynamic range of a receiver.

INTERMODULATION

This is described as the *'result of a non linear transfer characteristic'*. The mathematics have been exhaustively treated, and Ref.1 is recommended to those interested.

The effects of intermodulation are similar to those produced by mixing and harmonic production, insofar as the application of two signals of frequencies f_1 and f_2 produce outputs of $2f_2 - f_1$, $2f_1 - f_2$, $2f_1$, $2f_2$ etc. The levels of these signals are dependent upon the actual transfer function of the device and thus vary with device type. For example, a truly square law device, such as a perfect FET, produces no third order products ($2f_2 - f_1$, $2f_1 - f_2$). Intermodulation products are additional to the harmonics $2f_1$, $2f_2$, $3f_1$, $3f_2$ etc. Fig.1 shows intermodulation products diagrammatically.

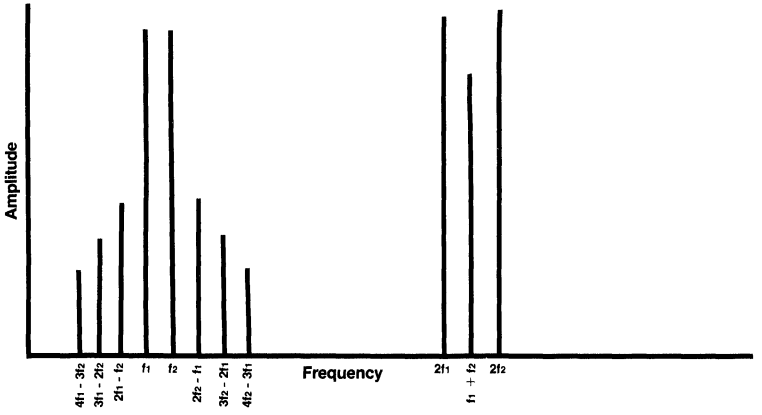


Fig.1 Intermodulation products

The effects of intermodulation are to produce unwanted signals, and these degrade the effective signal to noise ratio of the wanted signal. Consider firstly the discrete case of a weak wanted signal on 7.010MHz and two large unwanted signals on 7.020 and 7.030MHz. A third order product (2 x 7.02 - 7.03) falls on the wanted signal, and may completely drown it out. Fig.2 shows the total HF spectrum from 1.5 to 41.5MHz and Fig.3 shows the integrated power at the front end of a receiver tuned to 7MHz. It may be seen that just as white light is made up from all the colours of the spectrum, so the total power produced by so many signals approximates to a large wide band noise signal. Now, it has already been shown that two signals, f_1 and f_2, produce third order intermodulation products of $2f_1 - f_2$ and $2f_2 - f_1$. The signals will produce third order products somewhat greater in number, viz: $2f_1 - f_2$, $2f_1 - f_3$, $2f_2 - f_1$, $2f_2 - f_3$, $2f_3 - f_1$ and $2f_3 - f_2$. An increase in the number of input signals will multiply greatly the effects of intermodulation, and will manifest as a rise in the noise floor of the receiver.

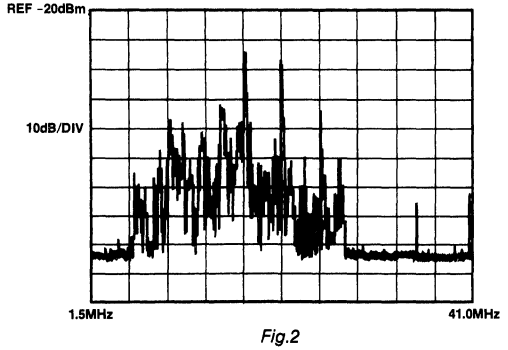


Fig.2

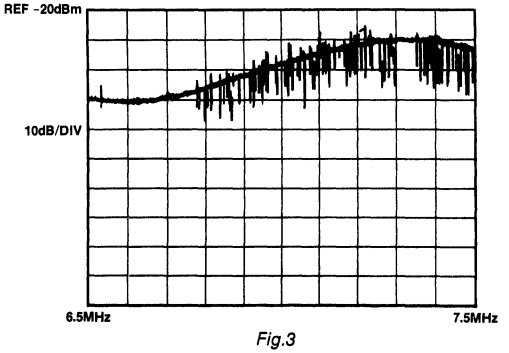


Fig.3

The amplitude relationships of the third order intermodulation products and the fundamental tones may be derived from Ref.1, where it is shown that the intermodulation product amplitude is proportional to the cube of the input signal level. Thus an increase of 3dB in input level will produce an increase of 9dB in the levels of the intermodulation products. Fig.4 shows this in graphic form, and the point where the graphs of fundamental power and intermodulation power cross is the *Third Order Intercept Point*.

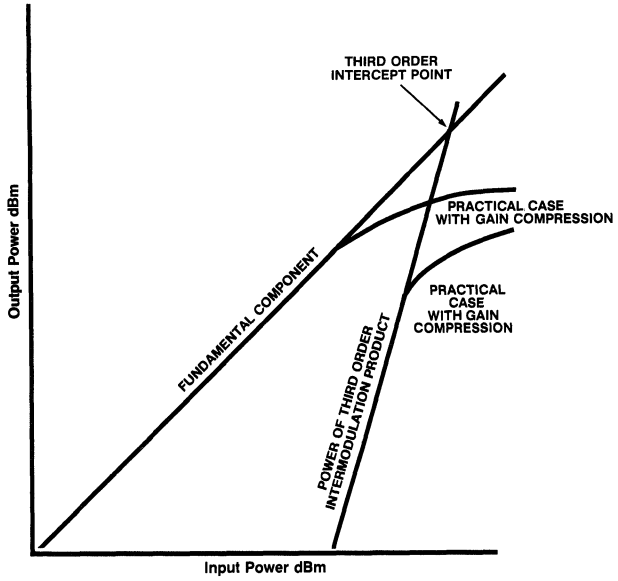


Fig.4 3rd order intercept

The third order intercept point is, however, a purely theoretical concept. This is because the worst possible intermodulation ratio is 13dB (Ref.2), so that in fact the two graphs never cross. In addition, the finite output power capability of the device leads to *Gain Compression*.

Thus, it is apparent that the intermodulation produced noise floor in a receiver is related to the intercept point. Figs.5, 6 and 7 show the noise floor produced by various intercept points, in a receiver fed from an antenna - a realistic test! Fig.5 shows that a large number of signals are below the noise floor and are thus lost; this represents a 0dBm intercept point. Fig.7 shows a +20dBm intercept noise floor, and it is obvious that many more signals may be received.

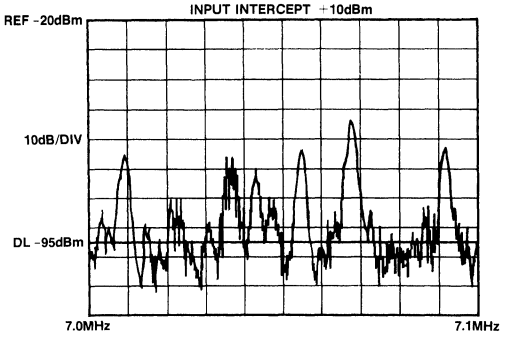


Fig.6

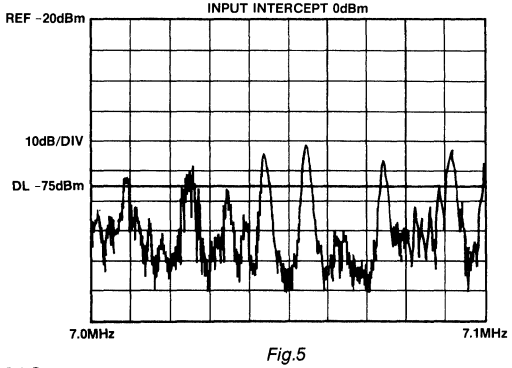


Fig.5

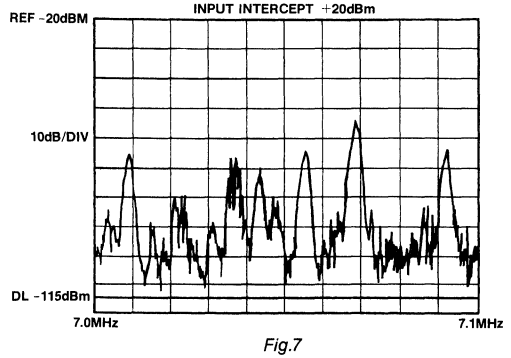


Fig.7

Because of the rate at which intermodulation products increase with input level (3dB on the intermodulation products for 1dB on the fundamental), the addition of an attenuator at the front end can improve the signal to noise ratio, as an increase in attenuation of 3dB will reduce the wanted signal by 3dB, but the intermodulation will decrease by 9dB. However, it is a fair comment that aerial attenuators are an admission of defeat, as suitable design does not require them!

The concept of dynamic range is often used when discussing intermodulation. Fig.8 shows total receiver dynamic range, which is defined as the spurious Free Dynamic Range. Obviously an intermodulation product lying below the receiver noise floor may be ignored. Thus the usable dynamic range is that input range between the noise floor and the input level at which the intermodulation product reaches the noise floor. In fact

$$DR = \frac{2}{3}(I_3 - NF) \quad \ldots (1)$$

Where DR is the dynamic range in dB
I_3 is the intermodulation input intercept point in dBm
NF is the noise floor in dBm.

Note that in any particular receiver, the noise floor is related to the bandwidth; dynamic range is similarly so related.

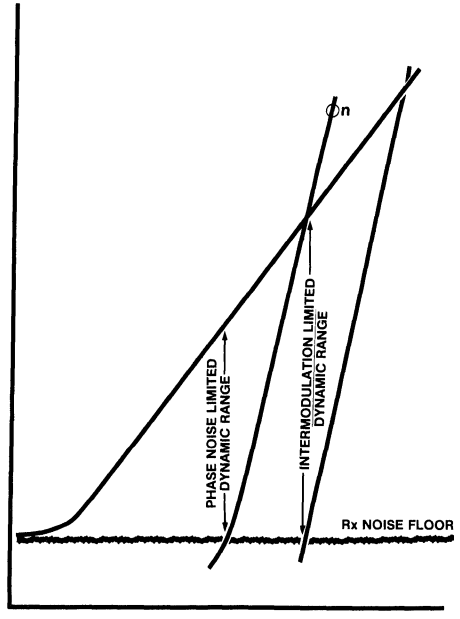


Fig.8

HF receivers will often require input intercept points of +20dBm or more. The usable noise factor of HF receivers is normally 10-12dB: exceptionally 7 or 8dB may be required when small whip antennas are used. An SSB bandwidth would have a dynamic range from (1) of 105.3dB. The same receiver with a 100Hz CW bandwidth would have a dynamic range of 114.6dB and thus dynamic range is quite often a confusing and imprecise term.

Appendix A defines a quantitive method of Intermodulation Noise Floor assessment, developed later than the data in Figs.5 to 7.

VHF receivers require noise figures of 1 or 2dB for most critical applications, and where co-sited transmitters are concerned, signals at 0dBm or more are not uncommon. However, such signals are usually separated by at least 5 % in frequency and filters can be provided. Close-in signals at levels of -20dBm are not uncommon, and dynamic ranges in SSB bandwidths of about 98dB are required.

The achievement of high input intercept points and low noise factors is not necessarily easy. The usual superhet architecture follows the mixer with some sort of filter, frequently a crystal filter, and the performance of this filter may well limit the performance. Crystal filters are not the linear reciprocal two-port networks that theory suggests, being neither linear nor reciprocal. It has been suggested that the IMD is produced by ferrite cored transformers, but experiments have shown that ladder filters with no transformers suffer similarly. Thus, although ferrite cored transformers can contribute, other mechanisms dominate in these components. The most probable is the failure of the piezo-electric material to follow Hooke's Law at high input levels, and possibly the use of crystal cuts other than AT could help insofar as the relative mechanical crystal distortion is reduced. The use of SAW filters is attractive, since they are not bulk wave devices and do not suffer to such an extent from IMD; however, it is necessary to use a resonant SAW filter to achieve the necessary bandwidths and low insertion losses.

The design of active components such as amplifiers is relatively straightforward. Amplifiers of low noise and high dynamic range are fairly easy to produce, especially with transformer feedback, although where high reverse isolation is required, care must be taken. Mixers are however, another matter.

Probably the most popular mixer is the diode ring (Fig.9). Although popular, this mixer does have some drawbacks, which have been well documented. These are:

Insertion loss (normally about 7dB)
High LO drive power (up to +27dBm)
Termination sensitive (needs a wideband 50Ω)
Poor interport isolation (40dB)

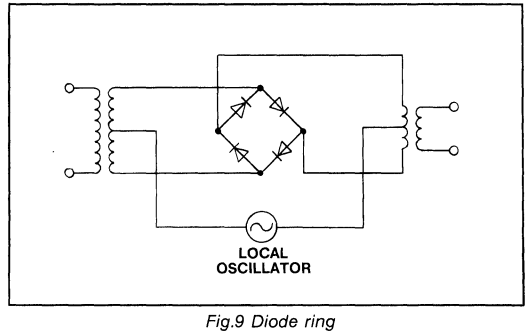


Fig.9 Diode ring

The insertion loss is a parameter which may be classed merely as annoying, although it does limit the overall noise figure of the receiving system. The high LO drive power means a large amount of DC is required, affecting power budgets in a disastrous way, while termination sensitivity may mean the full potential of the mixer cannot be realised.

For the diode ring to perform adequately, a good termination 'from DC to daylight' is required - definitely at the image frequency (LO ± sig. freq.) - and preferably at the harmonics as well. Finally, interport isolation of 40dB with a +27dBm LO still leaves -13dBm of LO radiation to be filtered or otherwise suppressed before reaching the antenna.

A further problem with the simple diode ring of this form is that the 'OFF' diodes are only off by the forward voltage drop of the ON diodes. Thus the application of an input which exceeds this OFF voltage leads to the diodes trying to turn ON, giving gain compression and reduced IMD performance.

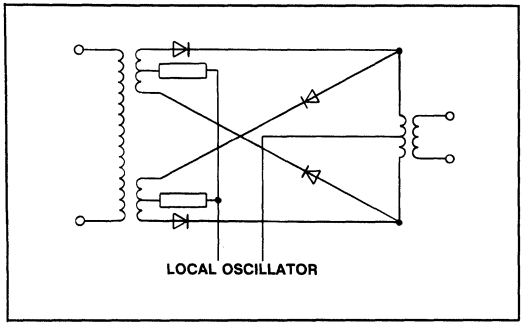


Fig.10 Resistive loaded high intercept point mixer

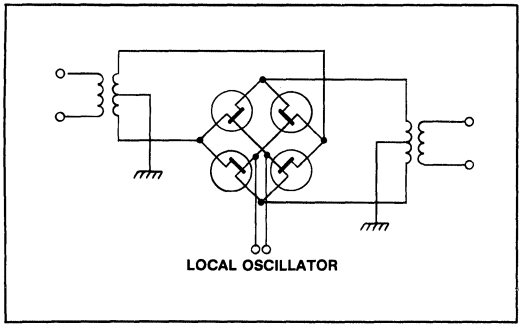


Fig.11 Quad MOSFET commutative mixer

Fig.10 shows a variation of this in which series resistors are added. The current flow through these resistors increases the reverse bias on the OFF diodes which gives a higher gain compression point: such a mixer can give +36dBm intercept points with a +30dBm of LO drive. Nevertheless, as is common to all commutative mixers, the intermodulation performance is related to the termination, and the LO radiation from the input port is relatively high.

Variations of this form of mixer include the Rafuse Quad MOSFET mixer of Fig.11, which suffers with many of the same problems. Fig.12 shows a dual VMOS mixer capable of good performance, but requiring a large amount of DC power and with limited isolation of the LO injection.

Many advantages accrue to the choice of the transistor tree type of approach (Fig.13). Here the input signal produces a current in the collectors of the lower transistors and this current is commutated by the upper set of switching transistors. Because the current is to a first order approximation independent of collector voltage, the transistor tree does not exhibit the sensitivity to load impedance that the diode ring does, and indeed, by the use of suitable load impedances, gain may be achieved. The non-linearity of the voltage to current conversion in the base emitter junctions of the bottom transistors is the major cause of intermodulation, but by using suitably large transistors and emitter degeneration, very high performances (+32dBm input intercept) can be achieved. The Plessey SL6440 has been described (Refs.3, 4, 5) and uses these techniques to achieve a high standard of performance (see Fig.16).

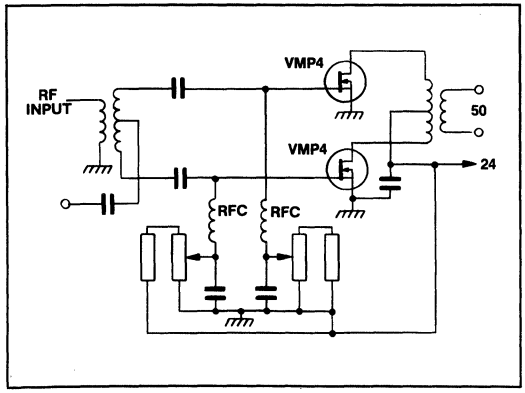


Fig.12 VMOS mixer

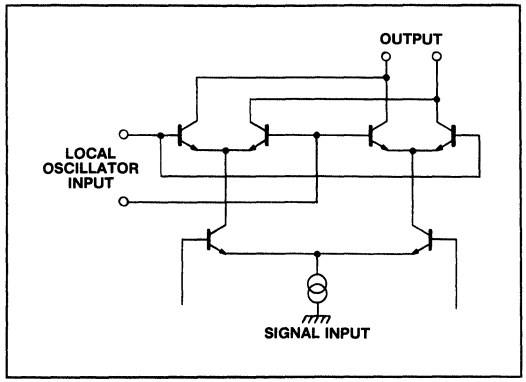


Fig.13 The transistor tree

PHASE NOISE

The mixing process for the superhet receiver is shown in Fig.14, where an incoming signal mixes with the local oscillator to produce the intermediate frequency. Fig.15 shows the effect of noise modulation on the LO, where the noise sidebands of the LO mix with a strong, off channel signal to produce the IF. This means that the phase noise performance of the LO affects the capability of the receiver to reject off channel signals, and thus the receiver selectivity is not necessarily defined by the signal path filters. This phenomena is referred to as *Reciprocal Mixing*, and has tended to become more prominent with the increased use of frequency synthesisers in equipments.

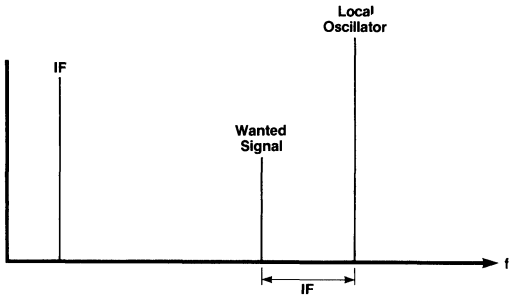


Fig.14 Superhet mixing

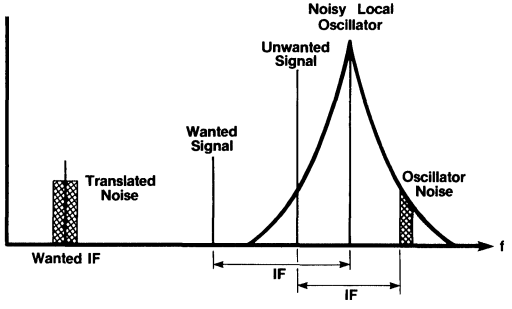


Fig.15 Reciprocal mixing

The performance level requirements of receivers is dependent upon the application. Some European mobile radio specifications call for 70dB of adjacent channel rejection, equating to some -122dBc/Hz, while an HF receiver requiring 60dB rejection in the adjacent sideband needs -94dBc/Hz at a 500Hz offset. The use of extremely high performance filters in the receiver can be completely negated if the phase noise is poor. For example, a receiver using a KVG XF9B filter with a rejection in the unwanted sideband of 80dB at 1.2kHz, would require a local oscillator with -114dBc/Hz phase noise at 1.2kHz if the filter performance was not to be degraded.

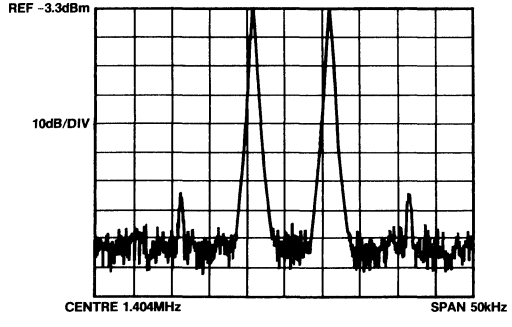


Fig.16 SL6440 intermodulation performance

To put these levels in perspective, relatively few signals generators are adequate to the task of being the LO in such a system. For example, 'Industry Standards' like the HP8640B are not specified to be good enough: neither are the HP8642, Marconi 2017/2018, or Racal 9082, all of which are modern, high performance signal generators.

All this suggests that it is very easy to over-specify a receiver in terms of selectivity, and simple synthesisers are not necessarily ideal in all situations.

The ability of the receiver to receive weak wanted signals in the presence of strong unwanted signals is therefore determined not only by the intermodulation capabilities of the receiver, but by phase noise and filter selectivity.

The usual approach to high performance synthesis has used multiple loops for good close-in performance. Notable exceptions are those equipments using fractional N techniques with a single loop. Nevertheless, such equipments not generally specified as highly as multi-loop synthesisers. A vital part of the synthesiser is still the low noise VCO, for which many approaches are possible. This VCO performance should not be degraded by the addition of the synthesiser: careful choice of technologies is therefore essential. For example, Gallium Arsenide dividers are much worse in phase noise production than silicon, and amongst the silicon technologies, TTL is better than ECL.

From equation (1)

$$DR = \frac{2}{3}(I_{p3} - NF) \text{ dB}$$

where I_{p3} = input intercept point dBm
NF = noise floor dBm

The phase noise governed dynamic range is given by

$$DR_{\Phi} = P_n + 10 \log_{10} B \; Db \qquad (2)$$

Where P_n is the phase noise spectral density in dBc/Hz at any offset and B is the IF bandwidth in Hz.

(N.B. This is not quite correct if B is large enough such that noise floor is not effectively flat inside the IF bandwidth).

Ideally the ratio

$$\frac{DR_{IM}}{DR_{\Phi}}$$

should be 1 in a well designed receiver - i.e. the dynamic range limited by phase noise is equal to the dynamic range limited by intermodulation.

Certain aspects of low noise synthesiser design have been touched upon and Ref.6 provides further information.

The performance of a receiver in terms of its capabilities to handle input signals widely ranging in input level is dependent upon the receiver capability in terms of intermodulation and phase noise. Neglect of either of these parameters leads to performance degradation, and it has been shown that specifications are not only often difficult to meet, but sometimes contradictory in their requirements.

This paper was first presented at the RF Technology Expo, Anaheim, Jan 1986.

P.E. Chadwick

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APPENDIX A

Intermodulation is caused by odd order curvature in the transfer characteristic of a device. If two signals f_1 and f_2 are applied to a device with third order term in its transfer characteristic, the products are given by:

$(\text{Cos}f_1 + \text{Cos}f_2)^3 = \text{Cos}^3f_1 + 3\text{Cos}^2f_1\,\text{Cos}f_2 + 3\text{Cos}f^2f_2\,\text{Cos}f_1 + \text{Cos}^3f_2$

from the trig identities Cos^3A, Cos^2A and CosACosB, this is

$\frac{1}{4}\text{Cos}^3f_1 + \frac{3}{4}\text{Cos}f_1 + \frac{3}{2}\text{Cos}^2f_1\text{Cos}f_2 + \frac{3}{2}\text{Cos}f_1\text{Cos}^2f_2 + \frac{3}{4}\text{Cos}f_2 + \frac{1}{4}\text{Cos}^3f_2 + \frac{3}{4}\text{Cos}f_2$

(where $f_1 = A$ and $f_2 = B$). Neglecting coefficients, the terms $\text{Cos}^2f_1\,\text{Cos}f_2$ and $\text{Cos}f_1\,\text{Cos}^2f_2$ are equal to

$\text{Cos}(2f_1 + f_2) + \text{Cos}(2f_1 - f_2)$ and
$\text{Cos}(2f_2 + f_1) + \text{Cos}(2f_2 - f_1)$

By inspection, it may be seen that frequencies of f_1, f_2, $3f_1$,$3f_2$, $(2f_1 \pm f_2)$ and $(2f_2 \pm f_1)$ are present in the output. Of these, only $2f_2 - f_1$, and $2f_1 - f_2$ are close to wanted frequencies f_1 and f_2.
The application of three signals f_1, f_2 and f_3, produces a similar answer, in that the resulting products are:

$3f_1$, $3f_2$, $3f_3$, $f_1 + f_2 + f_3$, $f_1 + f_2 - f_3$, $f_1 - f_2 + f_3$, $f_1 - f_2 - f_3$, $f_2 - f_1 + f_3$, $f_2 - f_1 - f_3$, $-f_1 - f_2 - f_3$, $-f_1 - f_2 + f_3$

in addition to the products

$2f_1 \pm f_2$, $2f_2 \pm f_1$, $2f_2 \pm f_3$, $2f_3 \pm f_2$, $2f_1 \pm f_3$, $2f_3 \pm f_1$

if a greater number of signals are applied such that the input may be represented by:

$\text{Cos}f_1 + \text{Cos}f_2 + \text{Cos}f_3 + \text{Cos}f_4 \ldots \text{Cos}f_n$

The result from third order curvature can be calculated from:

$(\text{Cos}f_1 + \text{Cos}f_2 + \text{Cos}f_3 + \text{Cos}f_4 \ldots \text{Cos}f_n)^3$

This expansion produces terms of

$\text{Cos}(f_1 \pm f_2 \pm f_3)$, $\text{Cos}(f_1 \pm f_2 \pm f_4)$, $\text{Cos}(f_1 \pm f_2 \pm f_n)$ etc from which it can be seen that the total number of products is:

$$\frac{n!}{3!(n-3)!} = 4 \times \tfrac{1}{6}n\,(n-1)(n-2)$$

(The factor of 4 appears because each term has four possible sign configuratons i.e. $\text{Cos}(f_1 + f_2 + f_3)$, $\text{Cos}(f_1 + f_2 - f_3)$ etc). This agrees with Ref A1.
By a similar reasoning, n signals produce:

$2n(n-1)$ products of the form $(2f_1 \pm f_2)$ $(2f_2 \pm f_1)$ etc and n 3rd harmonics.

Thus the total number of intermodulation products produced by third order distortion is:

$$n + 2n(n-) + \tfrac{2}{3}n\,(n-1)(n-2) \qquad (1)$$

Reduction of the input bandwidth of the receiver modifies this. Consider, for example, a receiver with sub-octave filters, rather than the 'wide-open' situation analysed above. In this case, the third harmonics produced by any input signals will not fall within the tune band, as will some of the products such as $f_1 + f_2 + f_3$, $f_1 - f_2 - f_3$, etc. In this case, the total number of intermoduation products is reduced. There are only three possible sets of products of the form f_1 $f_1 \pm f_2 \pm f_3$, i.e. $f_1 + f_2 - f_3$, $f_1 - f_2 + f_3$ and $f_3 - f_1 - f_2$ which can give products within the band. Note that for products to be considered, they must have an effective input frequency at the receiver mixer equivalent to an on-tune desired signal. In addition, products of the form $2f_1 + f_2$, $2f_2 + f_1$ etc are again out of band. Thus half of the $2n\,(n-1)$ products of this class are not able to cause problems and the total number of products to be considered is now:

$$n\,(n-1) + \tfrac{1}{2}n\,(n-1)(n-2) \qquad (2)$$

This result does not agree with Barrs (Ref A2) who uses the results in (1). The results in (2) are an absolute worst case, insofar as a number of the intermodulation products are out of band.

(For the purposes of this analysis, IMD in a mixer is assumed to produce an 'on tune' signal. Thus not all the possible intermodulation frequencies appearing in a half octave bandwidth will be able to interfere).

The same arguments apply to narrower front end bandwidths. However, the narrower the front end bandwidth, the higher is the probability that the distribution of signals will produce IMD products outside the band. For example, a receiver with ±2.5% front end bandwidth tuned to 10MHz will accept signals in a band from 9.75 to 10.25MHz. Signals capable of producing a product of the form $2f_1 - f_2$ must have one of the signals (f_1 or f_2) in the band 9.875 - 10.25 for a product to appear on tune. Thus the two signal apparent bandwidth is less than would be expected. Similar constraints apply to the $f_1 + f_2 - f_3$ product.

Similar arguments apply to other orders of curvature. Second order curvature, for example, will not produce any products in band for input bandwidths of less than 2:1 in frequency ratio.

The actual levels of intermodulation produced can be predicted from reference A1. In practice, the situation is that the input signals to a receiver are rarely all of equal unvarying amplitude and assumptions are made from the input intercept points and the input signal density.

If a series of amplitude cells are established for given frequency ranges, such as that in Table 1, then a prediction of the number of intermodulation products for any given number of input signals and amplitudes may be obtained, either from equation (1) or (2) (as applicable) or from Ref A1 (for higher orders). Where the input bandwidth of the receiver is deliberately minimised, the maximum cell size in the frequency domain should be equal to the input bandwidth.

The total input power in each cell is

$nPav$

where n is the number of signals and Pav is the average power of each signal.

A worst case situation is to assume that all signals in the cell are equal to the cell upper power limit boundary, e.g. if the cell amplitude range is from -40 to -30dBm, then an assumption that all signals in this cell are at -30dBm is a worst case.

If, however, it is assumed that signals will have a Gaussian distribution of input levels within a cell, then the total input power becomes:

$$Pt = 0.55nP$$

where Pt is the total power
n is the number of signals
P is the power level at the upper boundary of the cell

Because the total IMD power is the sum of all the IMD powers, the average input power is

$$Pav = \frac{0.55nP}{n}$$

The IMD power produced by third order curvature is:

$$10 \log_{10} [\tfrac{1}{3}n(2n^2 + 1)] \text{ Antilog } \tfrac{1}{10}[Pav - 3(I_3 - Pav)]dBm$$

where P_{IM} is the total power of the intermodulation products
I_3 is the third order input intercept point

Because the coefficients of the amplitudes of the intermodulation products are (depending on product)

a^3, a^2b, ab^2, abc, b^3

where a, b and c are approximately equal, the use of a^3 as the general coefficient is justified.

From equations (1) or (2) and (3), the total IMD power and number of products may be calculated. As 'n' increase in number, the number of products will mean that the resultant IMD tends more to a noise floor increase in the receiver, thus reducing the effective sensitivity.

The amount of this degradation is such that the noise floor is:

$$\frac{\frac{2}{3}(0.55nP)^3}{I_3} \times \frac{I_3}{(f_{max} - f_{min})} \times \Delta f$$

where $(f_{max} - f_{min})$ is the bandwidth prior to the first intermodulating stage. Δf is signal bandwidth in a linear system. The Gaussian Factor of 0.55 is somewhat arbitrary, since errors in this assumption are cubed.

The intermodulation Limited Dynamic Range is

$$\tfrac{2}{3}(I_3 + 174 - 10 \log_{10} \Delta f - NF)$$

where NF is the Noise Figure in dB.

The effects of Reciprocal Mixing are similar, except that signals may be taken one at a time. The performance is affected by the frequency separation between an 'off-tune' interfering signal and an 'on-tune' wanted signal unless the separation is such that the oscillator noise floor has been reached. Here again, reduction of front end bandwidth reduces the number of signals.

Generally speaking, the effects of reciprocal mixing are limited to close in effects - say within $\pm$50kHz, unless very poor synthesisers are used.

The response at some separation f_0 from the tune frequency is: $(L - 10 \log_{10} 10\Delta f)dB$ where L is phase noise spectral density in dBc/Hz and Δf is the IF bandwidth.

This assumes that the spectral density does not change within the receiver bandwidth: Ref A1 shows this to be generally applicable for narrow bandwidths.

The intermodulation free dynamic range is defined as:

$$\tfrac{2}{3}[I_3 - \text{noise floor}] = \tfrac{2}{3}[I_3 + 174 - 10 \log_{10} \Delta f - NF]dB$$

where I_3 is the input 3rd order intercept point in dBm
NF is the noise figure in dB
Δf is the IF bandwidth in Hz

It has been claimed that there is 6dB rejection of phase noise in diode commutative mixers. Thus the relationship between IMD and phase noise can be expressed as:

IMD dynamic range = phase noise dynamic range +6dB = (L - 10 $\log_{10}$ Δf) + 6dB

Thus at any offset, it is important to ensure that the two dynamic ranges are approximately equal if performance is not be be compromised.

A receiver for example with an input intercept point of +20dBm and input signals of -30dBm will produce an IMD product at -130dBm which, for an HF receiver with a noise factor of 8dB, will be just above the noise floor, in an SSB bandwidth. The noise floor of the LO will need to be such that the noise is at -133dBm if degradation is not to occur, and this will be produced by a noise floor of -137dBc/Hz in the synthesiser at the frequency separation of the signals in question. Thus the high intermodulation performance may well be compromised by poor phase noise.

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Radio Synthesiser Circuits
Loop Filter Design

LOOP BANDWIDTH

An important choice in the design of the Phase Locked Loop is the Loop Bandwidth. This determines parameters such as lock up time, noise and modulation capability, and generally is made as wide as possible in single loop synthesisers. There are conflicting requirements however, and single loop synthesisers are not always practicable - Refs. 1, 2.

The NJ8820 series use two phase detectors, a digital 'steering' detector and an analog high gain linear detector. This latter detector is a sample-and-hold type in which an internal 50pF capacitor is discharged at a constant current. This current is set by the gain programming resistor *RB*, and the voltage on the capacitor is sampled at the reference frequency. Thus the gain of the detector is fixed by the time available for the capacitor to be discharged. If the discharge current was constant, the phase detector would have a gain directly proportional to frequency and current, but the departure from constant current gives a correcting factor, and the gain is thus:

$$K\Phi = 10\,\frac{[V_{SUPPLY} - 0.7 - 89\,(RB)^{-\frac{1}{2}}]}{[2\pi \times (50 \times 10^{12} + CAP) \times RB \times FR]} \quad \text{...(1)}$$

where *RB* is the gain programming resistor and *FR* is the phase comparison frequency. The value of *CAP* is 0 for the NJ8820/1 and is fixed externally in the NJ8822.

The analog phase comparator has a very high gain and so can only operate over a narrow phase range. This phase window is given by:

$$\Delta\Phi = 4.5/K\Phi \text{ radian}$$

where $K\Phi$ is the phase detector constant (volts/radian).

When the analog phase detector is outside this range, the digital detector operates to provide steering. Inside the analog detector phase range, the digital output is in its 'Tri-State' high impedance condition.

When the loop filter consists of an integrator of the form of Fig.1 the digital output produces a voltage ramp given by:

$$-2.5\,\frac{R_3}{R_1} - \frac{2.5}{R1C} \text{ volts/sec} \quad \text{...(2)}$$

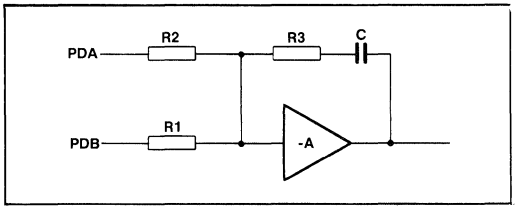

Fig.1 Augmenting integrator for loop filter

The figure of 2.5 is derived as follows:

A 2nd order loop has infinite DC gain and thus the analog phase detector output sits at a potential very close to the half supply voltage point. It is thus at 2.5V, and the maximum change in Vin is therefore 2.5V, and this input will appear whenever the digital phase detector operates.

This ramp results in a frequency sweep of approximately

$$2.5K_V \left(\frac{R_3}{R_1} + \frac{1}{R_1C_1}\right) \text{rads/sec}^2 \quad \text{...(3)}$$

Thus for a frequency step of $\Delta\omega$, the loop will slew to the new frequency in

$$\frac{\Delta\omega}{\frac{2.5K_V}{R_1}\left(R_3 + \frac{1}{C}\right)} \quad \text{...(4)}$$

where K_V is the VCO constant in rads/volts-sec.

Although the loop will lock eventually without the digital steering, the time taken is much longer. The time to attain frequency lock is given approximately by:

$$\frac{\Delta\omega R_2}{2.5K_V\left(R_3 + \frac{1}{C_1}\right)} \quad \text{...(5)}$$

This is derived from the slew rate at the output of the integration without the digital loop connected. Independent control of lock up time and loop bandwidth is therefore available by correct choice of R_1.

The 2nd order analog loop has a bandwidth and damping factor given by:

$$\omega_n = \sqrt{\frac{K\Phi K_V}{NR_2C}} \quad \text{...(6)}$$

$$D = \frac{R_3C}{2} \cdot \omega_n \quad \text{...(7)}$$

If the loop is slewed at too high a rate by the digital output, then a longer lock up time may result because of overshoot; in extreme cases, the loop will become unstable, because the VCO frequency will sweep too quickly.

$$CR_2 = \frac{2\pi\, K\Phi K_V}{\omega_n^2 N} \quad \text{...(8)}$$

$$\frac{R_2}{R_3} = \frac{\pi\, K\Phi K_V}{DN\,\omega_n} \quad \text{...(9)}$$

$$R_1 \geqslant 5R_2\,\frac{2D}{\omega_n} + 1 \quad \text{...(10)}$$

where ω_n = loop bandwidth in rads/sec
$K\Phi$ = analog phase detector gain in volts/rad
K_V = VCO sensitivity in Hz/volt
D = loop damping factor
N = divide ratio

The minimum value of R_1 can be determined as follows. The noise bandwidth, B_n, of a second order loop is:

$$B_n = \frac{K\Phi K_V\,\frac{R_3}{R_2} + \frac{1}{R_3C}}{4} \text{ Hz} \quad \text{...(11)}$$

and the maximum sweep rate is

$$\frac{d\angle\omega}{dt} = \frac{1}{2R_3C}\left(4B_n - \frac{1}{R_3C}\right) (B_n \text{ in radians}) \quad \text{...(12)}$$

Thus the maximum voltage sweep is

$$\frac{dV}{dt} = \frac{1}{2K_V R_3C}\left(4B_n - \frac{1}{R_3C}\right) \quad \text{...(13)}$$

which simplifies to

$$\frac{dV}{dt} = \frac{K\Phi}{2R_2C} \quad \text{...(14)}$$

The integrator gives an output (assuming $R_2 >> R_1$)

$$V = 2.5\left(\frac{R_3}{R_1} + \frac{1}{R_1C}\right) \text{ volts/sec} \quad \text{...(15)}$$

$$\text{therefore } 2.5\left(\frac{R3}{R1} + \frac{1}{R1C}\right) \leqslant \frac{K\Phi}{2R2C} \quad ...(16)$$

$$R3 = \frac{2D}{\omega_n D} \quad \text{and by substitution,}$$

$$R1 \geqslant \frac{5R2}{K\Phi}\left(\frac{2D}{\omega_n} + 1\right) \quad ...(17)$$

For $D > 0.5 < 1.0$
and $\omega_n > 10$ rads/sec
Then the approximation

$$R1 \geqslant \frac{5R2}{K\Phi} \quad ...(18)$$

is correct.

It is advisable to use a larger value than this: it is suggested that

$$R1 \text{ min} = \frac{6R2}{K\Phi} \quad ...(19)$$

The minimum usable values of $K\Phi$ occur at higher reference frequencies, where a wider loop bandwidth can be used. Wide loop bandwidths are good for reduction of VCO noise and freedom from microphony, while narrow loops minimise the effects of reference frequency noise.

The NJ8820 analog phase detector has an internal noise level of about 1 microvolt/$\sqrt{}$Hz at a frequency of 100Hz. This falls within increasing frequency, and decreasing phase detector gain.

VCO Noise

Phase noise of the VCO inside the loop bandwidth will be reduced by the loop, while outside the loop bandwidth it will be unaltered. The phase noise of the reference oscillator will add to the VCO noise at frequencies inside the loop bandwidth and this effect also influences the choice of loop bandwidth. For example, a loop with a 5kHz loop bandwidth operating at 900MHz with a reasonable 5MHz crystal oscillator noise floor (-125dBc/Hz at 1kHz oscillator) would have a noise power of some -80dBc/Hz at 1kHz offset at final frequency. For a further discussion of phase noise and other compromises see Ref. 2.

Where a high phase detector gain is used with a noisy oscillator, or with a high value of K_V, it may well happen that the analog phase detector is driven outside the phase window. This will lead to the digital output becoming active, and instability is likely to result.

Modulation Techniques

Modulation of the PLL may take place inside or outside the loops bandwidth. Modulation outside the loop bandwidth requires the loop bandwidth to be less than the lowest modulating frequency, and the amount of modulation will vary over the frequency range as K_V, the VCO constant varies.

Various techniques may be used to minimise the variation in modulation sensitivity, and probably the easiest in the use of a separate modulation diode. The variation in capacitance is very small for normal NBFM variations and thus the deviation may well remain sensibly constant over a wide range, e.g. +0.75kHz for 5kHz nominal deviation over an 18MHz range at VHF.

Modulation outside the loop bandwidth leads to a signal appearing at the phase detector output corresponding to the phase error between reference frequency and the divided VCO. Should this phase error be such as to lead to the phase detector being driven outside its phase window, then problems may occur, with reference frequency sidebands appearing and possibly even unlocking of the loop.

Avoidance of this condition may be achieved by limiting the phase deviation at the detector such that detector is operating within its linear range. For devices with programmable phase detector gain, such as NJ8820 series, this may be achieved by using a low gain and high deviation ratio.

Modulation index, m, is given by:

$$m = \frac{\text{frequency deviation}}{\text{modulating frequency}} \quad ...(20)$$

For a modulation index of 1 at the VCO, the phase variation is 1 radian. Thus an NBFM transmitter with a deviation of 2.5kHz and modulation frequency of 500Hz has a phase deviation of 5 radians.

In a 25kHz channelled system at 30MHz, the deviation at the detector would be 5/1200 rads or 0.24 degrees. Attempting to operate the NJ8820 at 800 volts/rad would give problems because of limiting in the analog phase detector.

Modulation inside the loop bandwidth avoids this problem, but care must be taken to ensure that the reference frequency sidebands do not become appreciable. In addition, the wideband noise of the phase detector and loop filter can cause problems when K_V, the oscillator constant in MHz/volt, is high.

Modulation of the reference oscillator is another possible technique of modulating inside the loop bandwidth. However, all modulation inside the loop bandwidth produces phase rather than frequency modulation and there are, in addition, limits on the frequency deviation and modulation frequency that can be accepted without the loop becoming unlocked. Generally, the modulation frequency must be much less than the loop bandwidth. Gardner (Ref.4) has derived the equation:

$$\Delta\omega = \frac{\omega_n^2}{\omega_m} \quad ...(21)$$

where $\Delta\omega$ = frequency deviation
ω_n = loop natural frequency (bandwidth)
ω_m = modulating frequency

This equation is only valid for $\omega_m \ll \omega_n$

In general, modulation outside the loop bandwidth is used, because the required bandwidth is greater than the reference frequency. The loop bandwidth is usually 1/5 and 1/10 of the lower modulating frequency.

Note that modulation applied such that

$$\frac{\Delta\omega}{dt} \geqslant \frac{K\Phi K_V}{R2C} \quad ...(22)$$

will cause the loop to unlock.

In addition, modulation such that the analog phase detector limits is not advisable. This will occur when

$$\Delta\Phi \geqslant 4.5N/K\Phi \text{ rads} \quad ...(23)$$

$\Delta\Phi$ is equivalent to m, the modulation index: when $m = 1$, $\Delta\Phi = 1$ radian.

Thus, a synthesiser operating at 145MHz with a 25kHz comparison frequency and a modulation index of 30 for the lowest modulating frequencies would need $K\Phi$ to be less than 870 volts/rad. Operation at lower frequencies are used. However, large amounts of LF phase noise can have appreciable phase deviations and thus low noise oscillators should be used.

Noise from the amplifier used in the loop filter should be minimised: the use of a low noise amplifier such as a Plessey SL562 is suggested. Filtering after the amplifier, such as in Fig.2, is advisable to minimise the noise modulation of the VCO, but care should be taken to ensure that the added phase shift does not cause the loop to become unstable.

Loop Stability

Calculation of loop stability may be carried out in a number of ways. It has been claimed (Ref.4) that a true 2nd order PLL does not exist because of strays. In addition, an extra section (at least) of RC filtering is generally required to minimise the effects of noise in the operational amplifier. Various computer programs exist in which such analysis can be undertaken, but it is possible to evaluate loop stability in a relatively easy manner using a programmable calculator.

For a 2nd order loop such as Fig.2, it may be shown that the transfer function is

$$\frac{AoK\Phi Kv}{N\omega} \cdot \frac{j\omega T2 + 1}{j(1-\omega^2 E) - \omega(F - \omega^2 D)} \quad ...(24)$$

where $D = T3To(T1 + T2)$
$E = T3(Ao\,T1 + To + T1 + T2) + To(T1 + T2)$
$F = Ao\,T1 + To + T1 + T2 + T3$

and Ao, $K\Phi$, Kv, N, ω, have the previously assigned definitions.

Ao = open loop amplifier gain
To = $1/fo$, amplifier open loop 3dB bandwidth
$T1$ = $R2C1$
$T2$ = $R3C1$
$T3$ = $R4C2$

The finite modulation bandwidth of the VCO is ignored in this analysis.

Evaluating the equation (24) in terms of gain and angle ($rL\theta$) at various frequencies allows the stability to be evaluated. An example of a frequency synthesiser design is given in the following section, where Table 1 lists a suitable program for Hewlett Packard Calculators using Reverse Polish Notation.

Frequency Synthesiser Design

A frequency synthesiser is required for a transmitter covering 144-148MHz. the supply voltage for the synthesiser is 10 volts, pre-emphasised frequency modulation is required with an upper limit of 3kHz, adjacent channel noise is required to be -70dB at 12.5kHz channel spacing and a 'lock-up' time of 25ms is required.

12.5kHz channel spacing systems use an IF bandwidth of 7.5kHz, which gives approximately 39dB more noise than a 1Hz bandwidth. Thus the VCO for this synthesiser must have a phase noise characteristic of -109dBc/Hz at 12.5kHz (see Ref.1) and from Refs. 2 and 3 this may be shown to be practical with a single loop synthesiser using a narrow bandwidth.

The choice of prescaler should be made from a consideration of programming - see the relevant data sheet.

The lowest modulation frequency is 300Hz and the transmitter will attenuate components below this frequency at 12dB/octave or more. Standard pre-emphasis rises at 6dB/octave from 300Hz to 2700Hz: thus the deviation at 300Hz is approximately 18dB down on that at 2.7kHz and at 50Hz will be about -45dB. With a deviation at 2.7kHz of 2.5kHz, the deviation at 50Hz will be about 15Hz.

At 144MHz, the divide ratio is 145000/12.5 = 11600. Thus the 15Hz deviation it caused by the 50Hz modulation becomes

$$15/50 \times 1/11600$$

radians at the phase detector, which is negligible. Thus the analog phase detetor will operate inside its window at low frequencies. Even at 300Hz where the modulation index is 8.33, the phase deviation at the phase detector is only 0.041 degrees.

Since a 10V supply is available, a VCO control line swing of 8 volts may be assumed. Allowing overlap, the VCO will cover 143-149MHz, giving Kv (the VCO constant) as 0.75MHz/volt. This gives a residual deviation caused by the phase detector noise of about 0.75Hz.

A loop bandwidth of 50Hz is well below the lowest modulating frequency and values may be readily calculated. $K\Phi$, the phase detector gain, is an independent variable; a reasonable mid-range value of 320 volts/rad gives a phase window of 0.89 degrees.

From these constants, values of $R1$, $R2$, $R3$ and C in Fig.1 may be calculated.

$$CR2 = \frac{2\pi K\Phi Kv}{\omega_n^2 N} \quad ...(25)$$

$$\frac{R2}{R3} = \frac{\pi K\Phi Kv}{DN\omega_n} \quad ...(26)$$

$$R1 \text{ min} = \frac{6R2}{K\Phi} \quad ...(27)$$

Thus, at the mid-band frequency of 146MHz, where N = 11680:

$$CR2 = \frac{2\pi \times 320 \times 0.75 \times 10^6}{(2\pi \times 50)^2 \times 11680} = 1.3 \quad ...(28)$$

$$\frac{R2}{R3} = \frac{\pi \times 320 \times 0.75 \times 10^6}{0.7 \times 11680 \times 2\pi \times 50} = 293 \quad ...(29)$$

$$R1 \geqslant \frac{5R2}{K\Phi}\left(\frac{2D}{\omega_n}\right) + 1 \quad ...(30)$$

The use of high values of resistance leads to greater noise generation in the loop filter because of KTB noise, while low values lead to larger current swings, which can give slew rate limiting in the op-amp. If $R3$ is set to 2200Ω, thus preventing slew rate limiting,

$R2 = 664k\Omega$ (use $680k\Omega$)
$C1 = 1.9\mu F$ (use $2.2\mu F$)

From these standard values

$$\omega_n = \sqrt{\frac{K\Phi Kv}{NCR2}} = 293.3 \text{rads/sec} \equiv 46.7\text{Hz} \quad ...(31)$$

$$\text{and } D = \frac{R3C}{2} \cdot \omega_n = 0.71$$

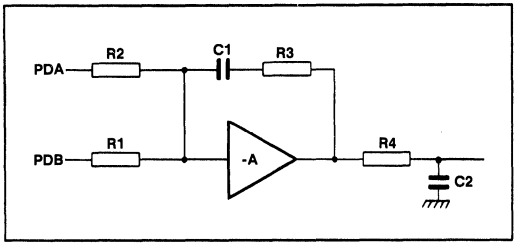

Fig.2 Augmenting integrator amplifier with filtering

$$R1 \text{ min} = \left(\frac{5 \times 680k\Omega}{320}\right)\left(\frac{2 \times 0.71}{2\pi \times 46.7} + 1\right) = 10.7k\Omega \quad ...(32)$$

(use 12kΩ or 15kΩ).

A further section of filtering may be added as in Fig.2, and the cut-off frequency may be arbitrarily set at 500Hz. Again, a reasonable compromise is required on *CR* values for the same reasons. The added filter section reduces noise from the op-amp and resistors, and so is a useful addition.

Let $R = 10k\Omega$ and $C = 0.33\mu F$

Using the program in Table 1, the stability may be calculated. (Assume a Plessey SL562 op-amp, where *fo*, the open loop 3dB frequency is 250Hz and *Ao*, the open loop gain = 30000).

$T0 = 1/fo = 4 \times 10^{-3}$
$T1 = R2C1 = 1.496$
$T2 = R3C1 = 4.84 \times 10^{-3}$
$T3 = R4C2 = 330 \times 10^{-6}$
$N = 11680$
$K\Phi = 320$
$Kv = 0.75$MHz/volt (4.7×10^6 rads/volt)

The results of the program are:

Frequency (Hz)	Loop Gain	Phase Margin (Degrees)
1	2200	-178
10	23	-164
50	1.59	-119
100	0.69	-128

From this analysis, it may be seen that the loop is stable. Increasing the time constant of *T3* is thus practicable from a loop stability point of view.

The lock up time *t* may be calculated from

$$\frac{\Delta\omega}{2.5Kv}\left(\frac{1}{R1R3} + CR1\right) \quad ...(33)$$

so for a 600kHz change,
$t = 8.5$ms to achieve frequency lock.
as opposed to 476ms without the digital steering (see equation (5)).

Note that these lock up times assume that the major factors affecting loop bandwidth are the values of the time constant *R2C*. In practice, this simplification is not completely justified, and, for example, increasing the value of *C2R4* to give *T3* = 5ms would increase lock up time while having little effect on loop stability.

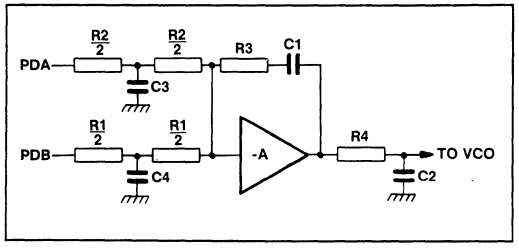

Fig.3 Loop filter with input sections

In cases where the operational amplifier 'locks up' because of overdrive, the circuit of Fig.3 may be used, often with success. The time constants *C3R2/2* should be about *10/fn* where *fn* is the loop bandwidth. It should be noted that the capacitor *C1 must* be of the non-polarised variety, as the voltage across it can reverse. Similarly, the external capacitor provided in the phase detector of the NJ8820 should be a low leakage type, such as polystyrene: ceramic capacitors are not generally good enough.

Bypassing the gain setting resistor of the NJ8820 series with a large capacitor may reduce noise derived from this resistor.

Loop Stability Program for HP Calculators

Enter

STO0	T0
STO1	T1
STO2	T2
STO3	T3
STO4	Ao
STO5	KΦ
STO6	Kv
STO7	N

(*T0* = 1/*fo*, the 3dB point of the op amp 'open loop' bandwidth, *T1* = *R2C1*, *T2* = *R3C*, *T3* = *R4C2*, *Ao* = open loop gain, *KΦ* = phase detector gain in volts/rad for the analog phase detector, *Kv* = VCO constant in rads/volt-sec, *N* = divide ratio).

Line	Function	Line	Function	Line	Function
001	hLBLA		+		RCL.0
	Enter		RCL0		$(g)x^2$
	2		x	075	+
	x	040	STO.0		(h)1/x
005	$(h)\pi$		RCL4		RCL.1
	x		RCL1		x
	STO8		x		STO.1
	RCL1		RCL0	080	RCL8
	RCL2		+	081	RCL2
010	+	046	RCL1		x
	RCL0		+		RCL.0
	x		RCL2		x
	RCL3		+	085	RCL9
	x	050	RCL3		-
015	RCL8		x		RCL.1
	$(g)x^2$		RCL.0		x
	x		+		STO.2
	STO9		RCL8	090	RCL8
	RCL4	055	$(g)x^2$		RCL2
020	RCL1		x		x
	x		CHS		RCL9
	RCL0		1		x
	+		+	095	RCL.0
	RCL1	060	STO.0		+
025	+		RCL4		CHS
	RCL2		RCL5		RCL.1
	+		x		x
	RCL3		RCL6	100	STO.3
	+	065	x		Enter
030	RCL9		RCL7		RCL.2
	-		÷		(g)P
	RCL8		RCL8		(h)PSE
	x		÷	105	(h)PSE
	STO9	070	STO.1		(g)R
035	RCL1		RCL9		(h)RTN
	RCL2		$(g)x^2$		

Table 1 Loop stability program

To use, enter the frequency in Hz, and press R/S. The display will show the loop gain, flash twice and display the phase margin in degrees.

Note that HP calculators provide angular information up to ±180 degrees only. Thus a change from -179 degrees to -181 degrees would show as -179 to +179 degrees.

Multimodulus Division

Phase Locked Loop Frequency Synthesisers of the form shown in Fig.4 suffer from the problems inherent in producing fully programmable dividers required to operate at appreciable frequencies while not consuming excessive power. Although advances in small geometry integrated circuit technology make any figures obsolete, guaranteed operation above about 50MHz requires relatively high power.

The use of fixed prescaling, as in Fig.5, is widely used, but for a division ratio of N in the prescaler and a channel spacing of f kHz, the phase comparison frequency of Fig.4 has been reduced by the factor f/N. This lower frequency necessitates a lower bandwidth in the phase locked loop, and thus a greater susceptibility to microphonics etc., and, generally speaking, a longer lock up time.

The alternatives to fixed division are mixing, as in Fig.6 or 'multimodulus division' ('pulse swallowing') as in Fig.7. The use of mixers requires great care in the choice of frequencies if spurious products are not to be a problem and although widely used, is certainly more complicated than multimodulus division in terms of its physical realisation, requirements for 'adjust-on-test' parts, and its susceptibility to layout problems.

The multimodulus divider system is shown in Fig.7. It is built up from a number of blocks:

1. A two-modulus divider which will divide by one of two numbers N or $N + 1$ (e.g., 10/11, 64/65 etc.).

2. An A counter which is programmable and the output of which controls the modulus of the divider.

3. An M counter which is programmable, is clocked in parallel with the A counter, and the output of which resets both itself and the A counter.

The counters may count 'down' to zero from the programmed input, or count 'up' from zero.

The principle of operation is as follows:

The A counter is programmed to a smaller number than the M counter and assuming the counters to be empty, the system starts with the divider ($N/N + 1$) dividing by $N + 1$. This continues until the A counter reaches its programmed value, whereupon the divider divides by N until the M counter is full. As the M counter has received A pulses, this counter overflows after (M - A) pulses, corresponding to $N(M - A)$ input pulses to the divider. Thus the total division ratio P is given by:

$$P = (N + 1)A + N(M - A)$$
$$= NM + A$$

Obviously, A must be equal to or less than M for the system to work, while for every possible channel to be available, the minimum total divide ratio is $N(N - 1)$ while the maximum total divide ratio is $M(N + 1)$. A_{max} should be equal to or greater than N.

Although deceptively simple in theory, there are a few points which require consideration in the design of such a divider system. Of these probably the most important is Loop Delay.

Consider the counter chain at the instant that the $(N + 1)$th pulse appears at the two modulus divider input. After some time $tp1$ the output produces a pulse, which clocks the A and M counters. Assume that the A counter is filled by the pulse, and so after a time $tp2$ (determined by the propagation delay of the A counter) an output is produced to set the dual modulus divider ratio to N. After a set-up time ts, the dual modulus divider will divide by N. But if $tp1 + tp2 + ts$ is greater than N cycles of input frequency, the divider will not be set to divide by N until after N pulses have appeared, and the system will fail. Thus

$$\frac{N}{fin} > \text{total loop delay}$$

Design in this region is critical: worst case tolerances *MUST* be used if the reproducibility and reliability of the design under temperature and voltage extremes is not to be compromised.

The value of N must also be large enough that the output frequency from the divider does not exceed the maximum input frequency of the following circuitry. In single chip MOS controllers, this may well be as high as 50MHz under some conditions, but under others, such as high temperature and low voltage, much lower. Generally, however, the limitation on such circuits is the loop delay rather than input frequency.

The loop delay is affected by the edge of the waveform on which the divider and the A and M counters trigger. If the edges are opposite then the loop delay may be increased by large amount, and if in these circumstances, the use of an inverter at the output of the divider is justified.

The minimum value of N is therefore settled by these constraints, but the actual choice of N may be determined by the ease of programming. This may be seen by considering a synthesiser with a 25kHz phase comparison frequency and 25kHz channelling, using a 40/41 divider.

At 156MHz:

$$P = \frac{156}{0.025} = 6240$$

therefore $NM + A = 6240$
therefore $40M + 0 = 6240$ ($A = 0$ for the lowest channel)
therefore $M = 156$

In general, where

$$fN = 1 \text{ or } 10 \text{ or } 100$$

$$M = f, \frac{f}{10}, \frac{f}{100} \text{ etc.}$$

and similarly for binary divide ratios.

The choice of prescaler is therefore fixed by

1. Total allowable loop delay.

$$\frac{N}{fin} > \text{controller delays}$$

2. Output frequency within the controller input frequency band.

3. Programming ease.

REFERENCE FREQUENCY DIVISION RATIO (R)

The value of R is set by the input frequency and the phase comparison frequency. Higher input frequencies require greater power and offer lower stability, while lower frequencies (below 4MHz) generally require larger physical crystal case sizes. Normally, a frequency between 4 and 10.7MHz is used, especially as in double conversion equipments commonality of oscillators may be possible.
e.g. for a 2.5kHz comparison frequency and 10.245MHz 2nd local oscillator frequency,

$$R = \frac{10.245 \times 10^6}{2.5 \times 10^3} = 4098$$

Note that R is *always* an even number.

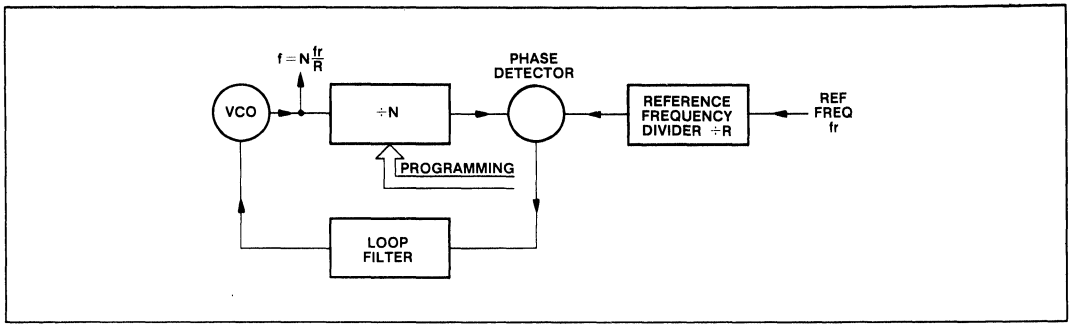

Fig.4 Direct division

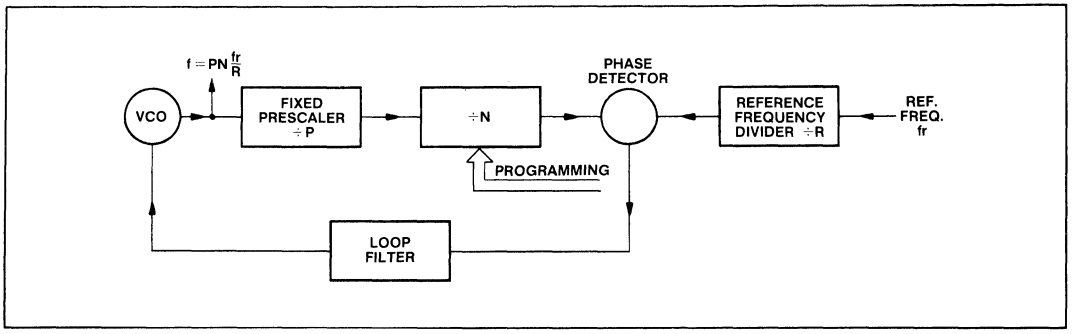

Fig.5 Fixed prescaling

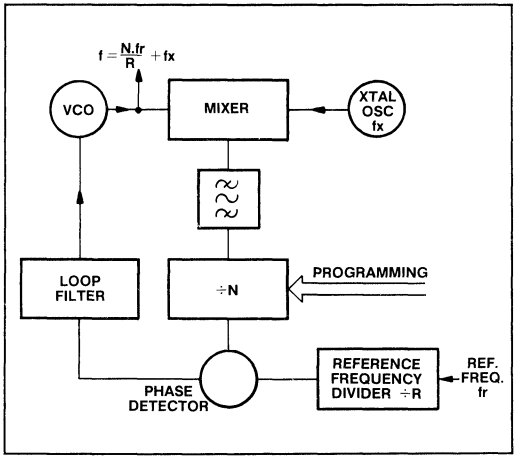

Fig.6 Mixing in the loop

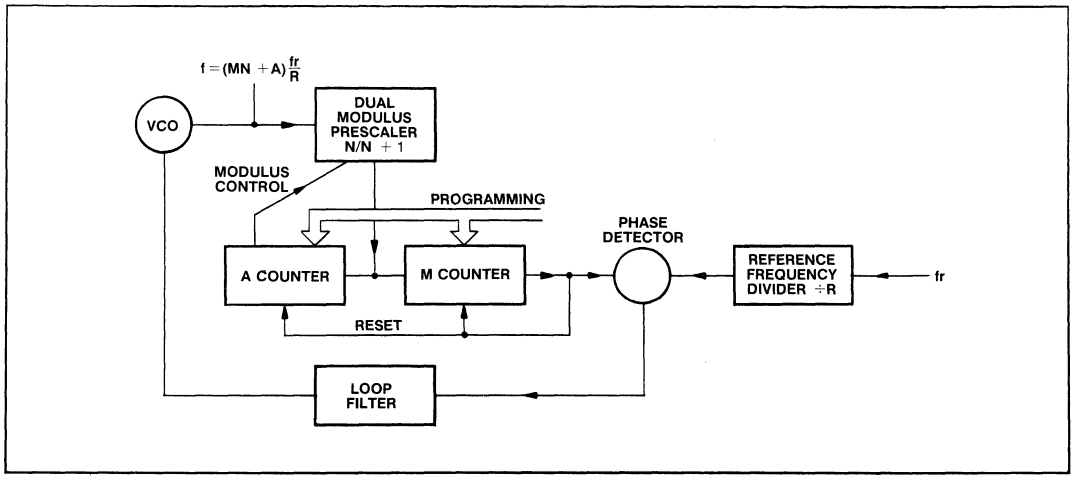

Fig.7 Dual modulus prescaling

Programming the NJ8820 and NJ8821/23

The NJ8820 and NJ8821/23 are versatile high performance CMOS frequency synthesiser controllers. The differences between devices lies in hardware programming methods.

The basic system of a single loop frequency synthesiser is shown in Fig.8, where a 2-modulus prescaler is used to divide the VCO frequency down to a suitable range for use in the CMOS device. The NJ8820/1/3 is programmed by 8 of 4 bit words on the data inputs: the addresses for these words may be obtained internally or externally and appear on the Data Select inputs/outputs. To program any frequency, it is necessary to program the *A* counter, the *M* counter and the reference or *R* counter: these counters are respectively, 7, 10, and 11 bits long.

ADDRESSING

Addressing is by one of three modes: These are:

A. Self Programming Internal Mode

Here the reference oscillator (either an internal crystal oscillator or from an external source) signal is divided in the reference counter by 64 and a DATA READ cycle commences every 1024/fosc seconds.

In this DATA READ cycle, the MEMORY ENABLE pin is pulled low, and the DATA SELECT outputs DS0, 1 and 2 count in binary from 0 to 7. This provides addresses for the DATA on D0, 1, 2 and 3, the data being transferred to internal latches on the trailing edge of the DATA SELECT pulses -see Fig.9. Note that the Program Clock is internally derived and is at a frequency of fosc/64. The PE (Program enable) pin is grounded, and the cycle continuously repeats. This mode is not recommended, as noise may be picked up by the phase locked loop.

B. Single Shot Internal Mode

In this mode, the PE pin is provided with a pulse input. This pulse initiates a data read cycle as outlined above, and at the end of the cycle, the ME (Memory Enable - NJ8820 and NJ8820HG only) pin goes high and thus system power consumption is minimised. 'Power-on' initiation is used, in which the application of power to the device is sensed and a programming cycle initiated. In order to avoid corruption of the data, a delay of 53248 cycles of reference oscillator frequency is provided before the programming cycle occurs. This delay is approximately 5ms for a 10MHz reference frequency.

C. External Mode

The address is presented to DS0, 1 and 2, and a pulse is applied to the PE pin to transfer data to the internal latches. The data is transferred from the latches to the counters simultaneously with the transfer of data into Latch 1: thus this word should be the last one entered.

WORD VALUES

For any particular set of conditions, viz operating frequency, prescaler ratio, comparison frequency and input frequency from the reference oscillator, a unique set of programming words exist.

Reference Divider

This divider produces the comparison frequency required by the synthesiser. It is programmable from 6 to 4094 in steps of 2. The division ratio is twice the programmed number. Therefore, if for example a 10MHz crystal is used, and a 12.5kHz reference required, this counter would be programmed to give a ratio of 100000/12.5 = 800. The actual programming would then be 400, which would be entered in binary according to the data map, Table 3.

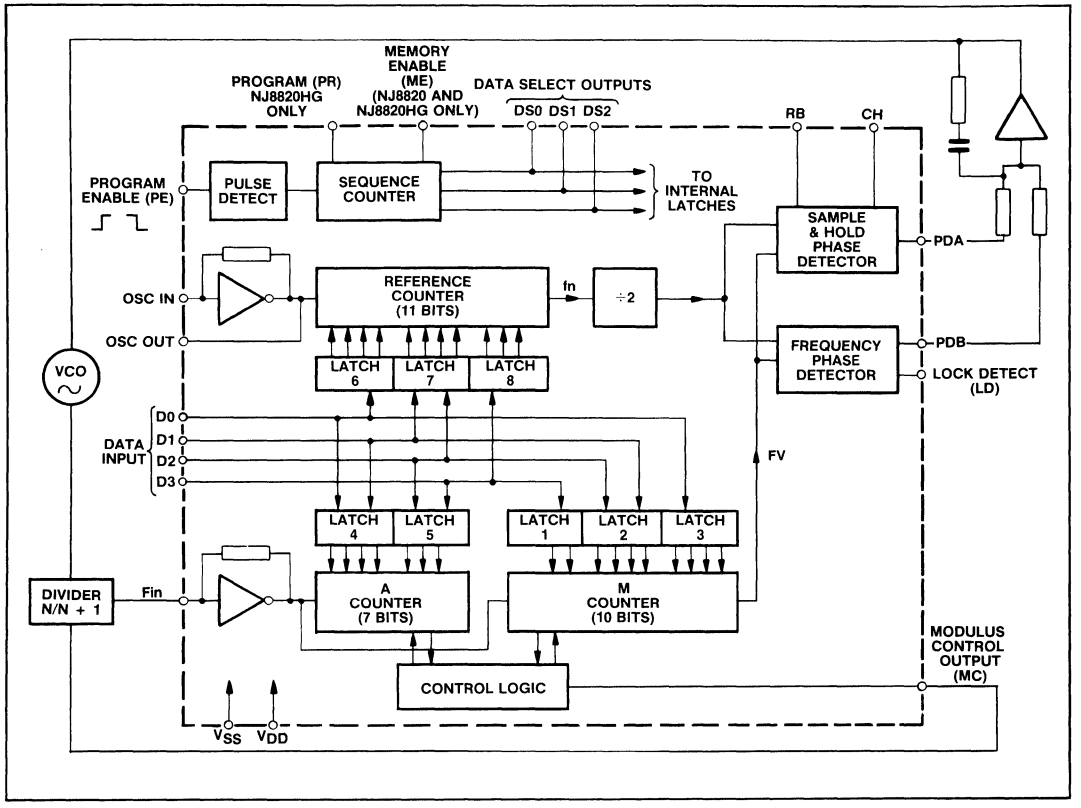

Fig.8 The phase lock loop

A and N Dividers

The *A* counter is a 7-bit counter and the *M* counter is a 10-bit counter. The programming calculations are as follows:

1. The *A* counter should contain *x* bits such that $2^x = M$.

2. If more bits are included in the *A* counter, these should be programmed to zero.

e.g. $M = 64 = 6$ bits
$A = 10$ bits
then the 4 MSB are programmed to zero.

3. The *M* and *A* counters are treated as being combined so that the MSB of the *M* counter is the MSB of the total and LSB of the *A* counter is the LSB of the total.

e.g. A synthesiser operating from 430-440MHz in 25kHz steps uses a 64/65 divider, and the control circuit uses binary counters.
P = f/fref and fref = channel spacing = 25kHz
$Pmin = 430/0.025 = 17200$
$Pmax = 440/0.025 = 17600$

Minimum possible divide ratio is $N^2 - N = 4032$
where N is two modulus divider ratio

$$\text{maximum allowable loop delay} = \frac{64}{440 \times 106} = 145\text{ns}$$

Total divide ratio, P, is given by
$P = NM + A$
$N = 64$, as a 64/65 divider is used
$Pmin$ from above is 17200

Therefore $17200 = 64M + A$
And $M \geqslant A$
Let $A = 0$ Then $Mmin = \frac{17200}{64} = 268.75$

$= 268$
and $Mmax = \frac{17600}{64} = 275.0$

Thus the *M* counter must be programmable from 268 to 275 as required: the *M* counter must have at least 9 bits.
For a frequency of 433.975MHz

$P = 433.97/0.025 = 17359$

$$\text{therefore} \quad M = \frac{17359}{64} = 271.2343$$

The *A* counter is programmed for the remainder i.e.

$$0.2343 \times 64 = 15$$

From this, the *A* counter is programmed to 15 and the *M* counter to 271. The output frequency can bow be checked.

$P = NM + A$
$= 271 \times 64 + 15 = 17359$
and this is the required divider ratio.

Repeated calculations for memory programming may be easily evaluated using a programmable calculator. The program listed in Table 2 is suitable for most Hewlett Packard calculators.

Line	Function	Display
001	hLBLA	25 13 11
002	ENTER	31
003	RCL0	24 0
004	-	71
005	STO2	23 2
006	RCL1	24 1
007	-	71
008	STO3	23 3
009	hFRAC	25 33
010	ENTER	31
011	RCL1	24 1
012	X	61
013	STO4	23 4
014	RCL3	24 3
015	ENTER	31
016	RCL3	24 3
017	hFRAC	25 33
018	-	41
019	STO3	23 3
020	hPSE	25 74
021	hPSE	25 74
022	RCL4	25 4
023	hRTN	25 12

Table 2 Calculator program for values of M and A

To use the program, enter the comparison frequency in STO0, and the dual-modulus prescaler ratio in STO1 (this is the value of N in an $N/N + 1$ divider).

Enter the frequency to be synthesised in Hz and press the R/S button. The calculator will flash twice and display the decimal value of M: pressing R/S again will display the value for the A counter. The M counter value is in STO3: the A counter value is in STO4.

WORD	DS2	DS1	DS0	D3	D2	D1	D0
1	0	0	0	M1	M0	-	-
2	0	0	1	M5	M4	M3	M2
3	0	1	0	M9	M8	M7	M6
4	0	1	1	A3	A2	A1	A0
5	1	0	0	-	A6	A5	A4
6	1	0	1	R3	R2	R1	R0
7	1	1	0	R7	R6	R5	R4
8	1	1	1	-	R10	R9	R8

Table 3 Data map

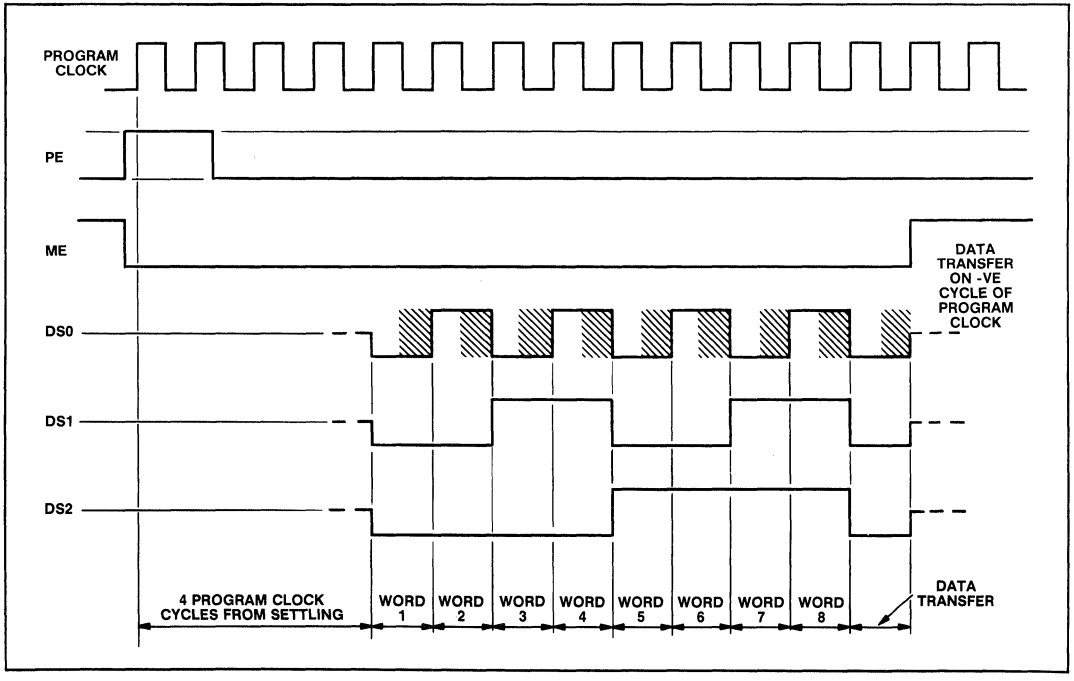

Fig.9 Data selection

NJ8820/1 SYNTHESISER DESIGN SUMMARY

1. Choose a suitable prescaler

- Check that input frequency range is suitable.
- $\frac{fin}{N} < 10.7\text{MHz}$
- $\frac{N}{fin} > 50\text{ns} + tr + tp$

  (tr is 'set-up' or 'release' time - whichever is longer; tp is propagation delay).
- Minimum division ratio is $N^2 - N$.

2. Choose the crystal frequency and value of R

- The phase comparison frequency should be as high as possible - usually the channel spacing.
- Higher crystal frequencies use more current and are less stable, but frequencies below 4MHz need larger case styles.
- R *must* be an even number.

3. Set values for A and M

- A is between 0 and 127.
- A is always equal to or less than M.
- Total division ratio is $NM + A$.
- M is between 3 and 1023.

4. Set loop values

- Choose the loop bandwidth ω_n rads/sec - normally less than $\frac{fx \,.\, 2\pi}{10R}$ (fx = crystal frequency)
- Choose the Damping Factor D - normally 0.7.
- Choose phase comparator gain such that at the lowest modulation frequency the phase deviation

$$\frac{\text{Modulation index}}{(MN + A)} < \frac{4.5}{K_\Phi}\text{ rads}$$

5. Calculate the values:

- $$CR2 = \frac{2\pi K_\Phi K_V}{\omega_n^2 \,.\, (NM + A)}$$

  (K_Φ in volts/rad)
  (K_V in rads/volt-sec)
  (ω_n in rads/sec)
- $$\frac{R2}{R3} = \frac{\pi K_\Phi K_V}{D(NM + A)\,\omega_n}$$
- $$R1 > \frac{6R2}{K_\Phi}$$
- $$\frac{1}{R4C2} \geqslant \frac{10\,\omega_n}{2\pi}$$

6. Check the time to reach a new frequency

- $$t = \frac{\Delta\omega}{2.5K_V}\left(\frac{1}{R1R3} + CR1\right)$$

  ($\Delta\omega$ is the frequency step in rads/sec).

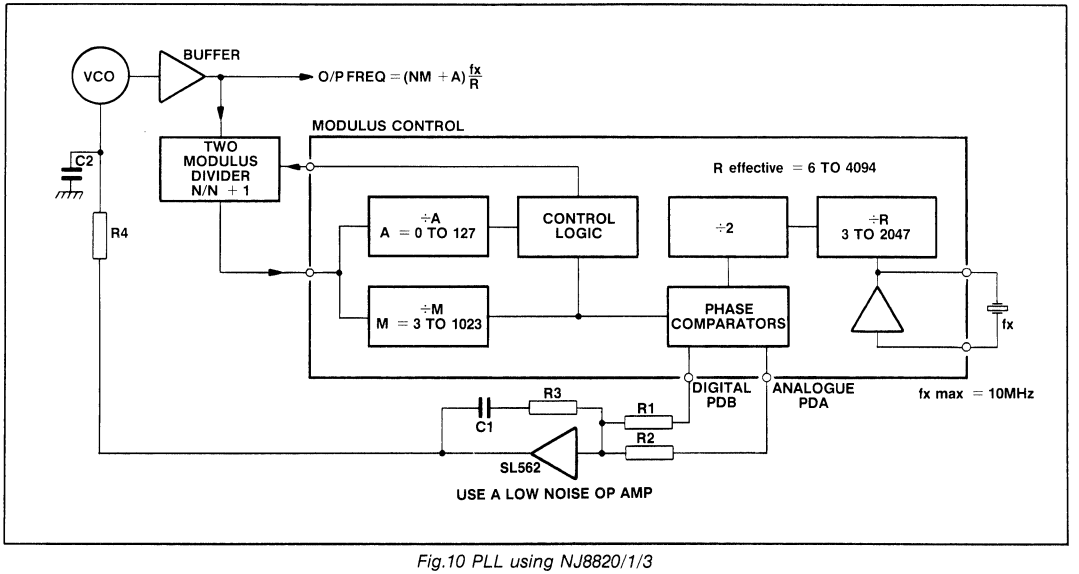

Fig.10 PLL using NJ8820/1/3

7. Check the loop stability using Bode or Nyquist plots - or use the calculator program listed in Table 1. (Page 4).

8. Derive the program numbers for the *A* and *M* counters - or use the calculator program listed in Table 2. (Page 9).

9. An example

A synthesiser is to operate from 430 to 440MHz in 25kHz steps (the channel spacing is 25kHz):

- **Choose the divider** The SP8718 is one choice. Since it divides by 64/65 then $N = 64$.
- **Choose the reference frequency** 25kHz is the channel spacing and is the best choice in this case.
- **Choose the crystal frequency** 2.5MHz is one possibility. The value of *R* can now be calculated:

  Crystal frequency = Reference frequency x *R* x 2
  So $R = 50$
- **Calculate the division ratio** (the ratio between the VCO output frequency and reference frequency)
  This is 17200 to 17600 in steps of 1.
- **Calculate values for A and M** The division ratio $NM + A$ is 17200 to 17600.

  So for the **minimum** frequency: $64M + A = 17200$
  If $A = 0$, $M = 268.75$
  This is not possible (it must be an integer) so this must be **decreased** to make *Mmin* = 268.
- **Draw up a table** for the required values of *A* and *M*

  Division ratio $(P) = NM + A$
  $= 64M + A$

  or use the calculator program listed in Table 2.

M	A	Division ratio	Output frequency (MHz)
268	48	17200	430.000
..	49	17201	430.025
..	50	17202	430.050
..	..	..	..
..	..	..	..
..	..	..	..
268	63	17215	430.375
269	0	17216	430.400
..	..	..	..
..	..	..	..
..	..	..	..
..	..	..	..
274	63	17599	439.975
275	0	17600	440.000

Table 4 Decimal values of A and M

These figures are acceptable:

$$N \geqslant A$$
$$P > M^2 - M$$

The values of *M*, *A* and *R* must be fed into the NJ8820/1 for each value of frequency required. (In this example the value of *R* is constant). The values must first be converted into BINARY format as shown in Table 5.

M (decimal	M (10 bit binary)									
	M9	M8	M7	M6	M5	M4	M3	M2	M1	M0
268	0	1	0	0	0	0	1	1	0	0
268										
268										
..										
..										
..										
..										
..										
..										
..										
..										
274	0	1	0	0	0	1	0	0	1	0
275	0	1	0	0	0	1	0	0	1	1

Table 5a Binary values for M

A (decimal)	A (7 bit binary)						
	A6	A5	A4	A3	A2	A1	A0
48	0	1	1	0	0	0	0
49	0	1	1	0	0	0	1
50	0	1	1	0	0	1	0
..							
..							
..							
..							
..							
..							
..							
..							
63	0	1	1	1	1	1	1
0	1	0	0	0	0	0	0

Table 5b Binary values for A

R (decimal)	R (11 bit binary)										
	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0
50	0	0	0	0	0	1	1	0	0	1	0
50											
50											
..											
..											
..											
..											
..											
..											
..											
..											
50											
50											

Table 5c Binary values for R

In each case the LSB is identified by the heading *M*0, *A*0 or *R*0.

The NJ8820 and NJ8821/23 require 32 bits of data to be transferred for each value of frequency. These 32 bits are composed of the 28 bits above (10 + 7 + 11) plus 4 redundant bits. The method of transferring this data is different for the two device types.

NJ8820 - data obtained from a PROM

NJ8821/23 - data obtained from a Microprocessor.

USING THE NJ8820

The NJ8820 operates with an external 4 bit wide PROM. Information is transferred automatically from the PROM to the NJ8820 when the *PE* pin is activated. A 1024 bit PROM (256 x 4) will store 32 channels because each channel requires the transfer of 8 words (32 bits) of data. A 256 x 4 PROM has 8 address lines (*A*0 to *A*7) of which the NJ8820 can address 3 (*A*0 to A2, connected to *DS*0 to *DS*2). The remaining 5 address lines allow the unique identification of the channel required (32 channels in this case) as shown in Table 6, so for each channel number there are 8 words, each of four bits. The composition of these words is as shown in Table 7. The '-' symbol indicates that this is not read - normally the 8 bit value is 0.

The value of the bits *D*3, *M*1, etc. can be either 0 or 1 and can be found from the tables in the previous section. For example, when $M = 268$ then $M1 = 0$, $M0 = 0$ and WORD 1 is 0000.

USING THE NJ8821/23 IN A PARALLEL MODE

The NJ8821/23 operates with an asynchronous stream of data supplied from a microprocessor. When used in a 4-bit parallel mode it requires the transfer of 8 words (32 bits) of data. Word numbers 1 to 3 control the '*M*' counter, 4 and 5 the '*A*' counter, 6 to 8 the '*R*' counter. It is not necessary to transfer all the words every time; WORD 1 indicates to the NJ8821/23 that the data should be transferred from all latches to counters and so WORD 1 must always be sent last. There are 8 data connections between the microprocessor and NJ8821/23:

- *DS*0, *DS*1 and *DS*2 to select the correct word
- *D*0, *D*1, *D*2 and *D*3 are the input data for *A*, *M* and *R* counters
- *PE* is the strobe

To enter channel information follow the sequence listed below:

1. Ensure the *PE* (strobe) is 0.
2. Select any word (except word 1)...(*DS*0 to *DS*2) and the relevant input data (*D*0 to *D*3).
3. Wait for 1 microsecond or more.
4. Pulse the strobe (to 1) for 2 microseconds or more and return to 0.
5. Wait for 1 microsecond or more.
6. Repeat (2) to (5) as required.
7. Repeat (2) to (5) for word 1.

The composition of the data words is identical to that for the NJ8820.

USING THE NJ8821/23 IN A SERIAL MODE

When used in a serial mode (using a single external shift register) the NJ8821/23 requires the transfer of 8 words, each of 7 bits (56 bits) of data to program the *A*, *M* and *R* counters but only 5 words (35 bits) subsequently to reprogram the *A* and *M* counters. There are thus only 3 data inputs from the microprocessor: DATA, CLOCK and STROBE, as shown in Fig.11.

	ADDRESS LINES								
	A7	A6	A5	A4	A3	A2	A1	A0	
CHANNEL NUMBER 0					0	0	0	0	word 1
					0	0	0	1	word 2
					0	0	1	0	word 3
					0				..
					0				..
					0	1	1	1	word 8
CHANNEL NUMBER 1	0	0	0	0	1	0	0	0	word 1
					1	0	0	1	word 2
					1	0	1	0	word 3
					1				..
					1				..
					1	1	1	1	word 8

Table 6 Channel identification

ADDRESS LINES					DATA LINES				WORD
-	-	A2	A1	A0	D3	D2	D1	D0	
		0	0	0	M1	M0	-	-	1
		0	0	1	M5	M4	M3	M2	2
		0	1	0	M9	M8	M7	M6	3
		0	1	1	A3	A2	A1	A0	4
		1	0	0	-	A6	A5	A4	5
		1	0	1	R3	R2	R1	R0	6
		1	1	0	R7	R6	R5	R4	7
		1	1	1	-	R10	R9	R8	8

Table 7 Channel number composition

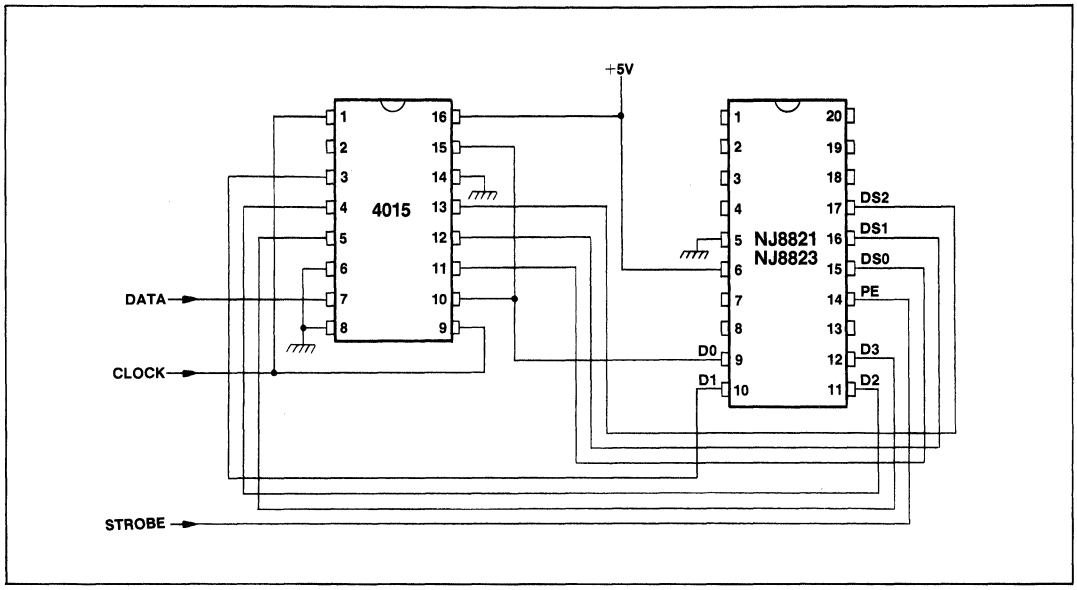

Fig.11 NJ8821/23 serial mode connections

The composition and entry sequence of the data words is identical to that of the NJ8820 except that the data is transmitted serially.

Once again, there is no need to transfer all the words every time provided that WORD 1 is always sent last.

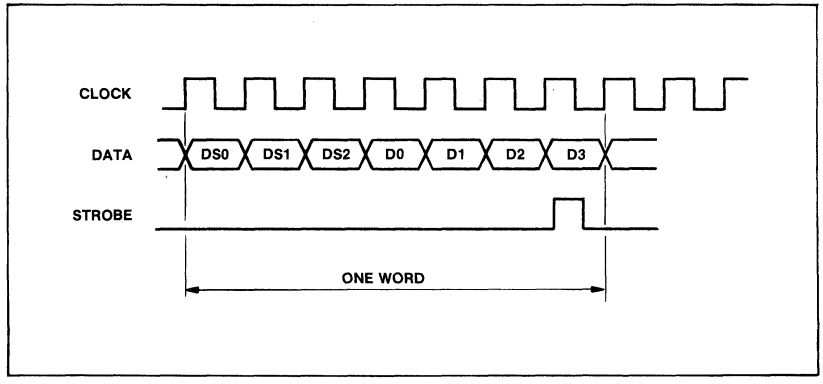

Fig.12 Serial data timing

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1. "Design Compromise in Single Loop Frequency Synthesisers" P.E. Chadwick, RF Design Expo, Anaheim, Ca. Jan 1985
2. Frequency Synthesisers, Theory and Design, V. Manassewitsch, Wiley, 1980, ISBN 0-471-07917-0
3. Digital PLL Frequency Synthesisers, U.L. Rohde, Prentice Hall, 1983, ISBN 0-13-214239-2
4. Phaselock Techniques, F.M. Gardner, Wiley 1979, ISBN 0-471-04294-3

A Serially Programmable VHF Frequency Synthesiser

This demonstration circuit uses three Plessey Devices - the NJ8822 single chip synthesiser, the SP8793 dual-modulus prescaler and the SL562 low noise op-amp in the configuration shown in Fig.1. The NJ8822 is programmed via a serial microprocessor interface.

The VCO is a FJET oscillator using a transmission line as the resonator. This VCO is modulated by applying the audio signal to the cathode of a reversed biased PIN diode as shown in the circuit diagram. The loop filter uses the SL562 which with the values shown has a loop bandwidth of 60Hz and a damping factor of 0.6. This filter is followed by a low pass pole at 3.7kHz to attenuate the 12.5kHz reference sidebands. The lock up time for a 1MHz change in frequency is 80ms (determined empirically). The output frequency range is 144-146MHz and the level is +3dBm into 50Ω.

The output spectra at 12.5kHz reference frequency is shown in Fig.2, and Fig.3 is a graph of modulating frequency against percentage distortion at several values of deviation. The circuit performs normally at a supply voltage of 5V ± 0.5V and within a temperature range of -30°C to +70°C. the only observable effect of varying the temperature was a frequency drift of 3kHz between the temperature extremes due to the uncompensated reference oscillator.

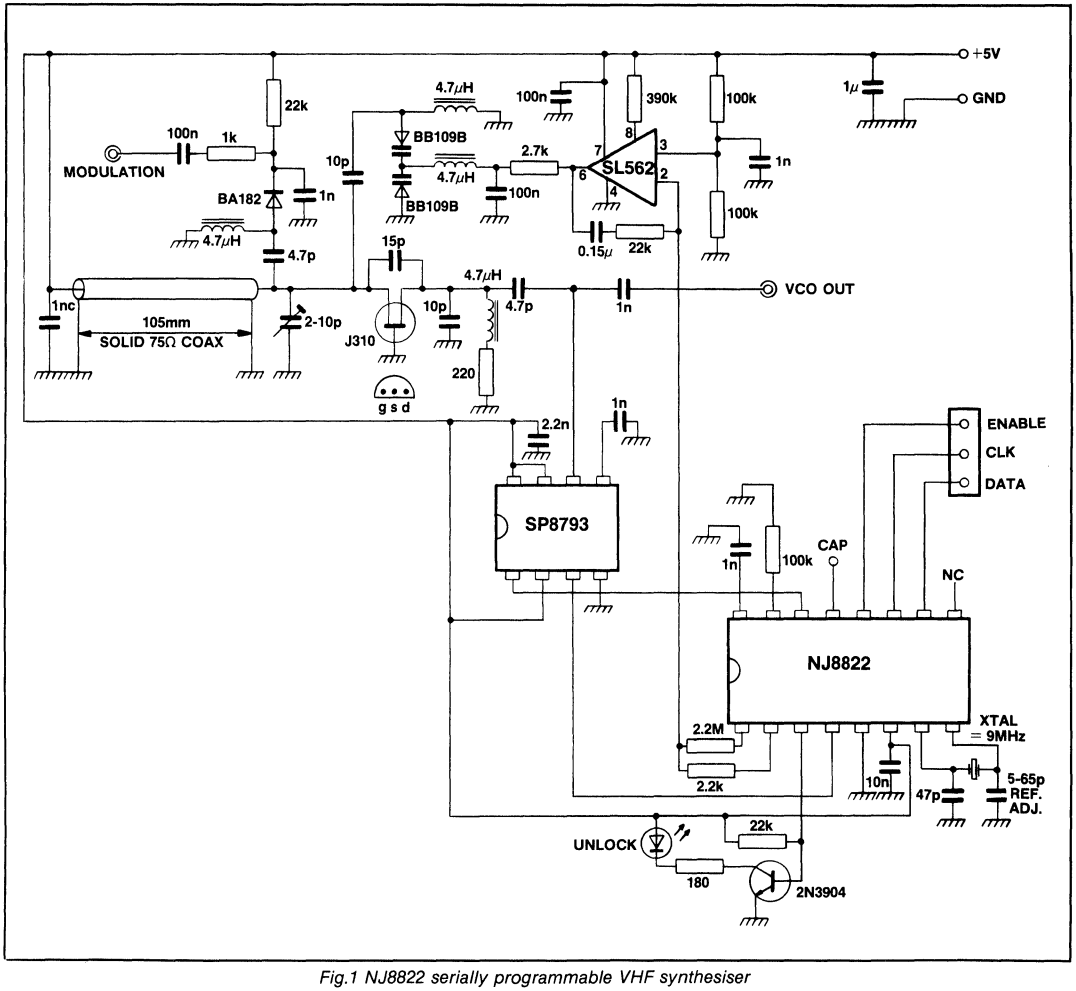
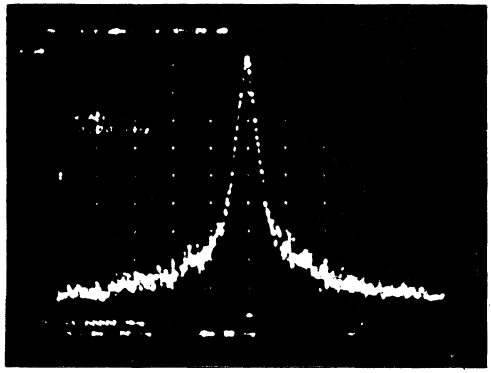
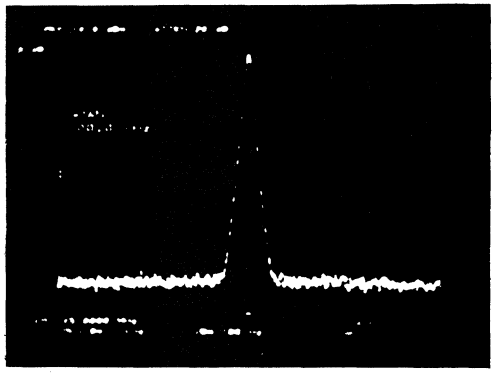


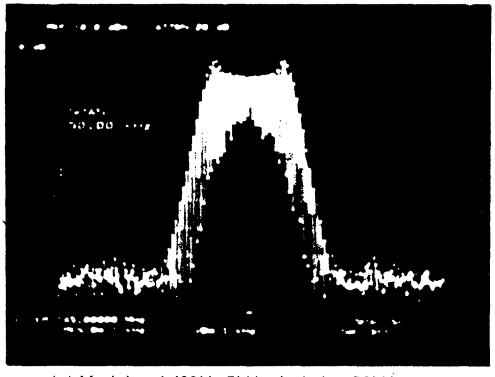
Fig.1 NJ8822 serially programmable VHF synthesiser



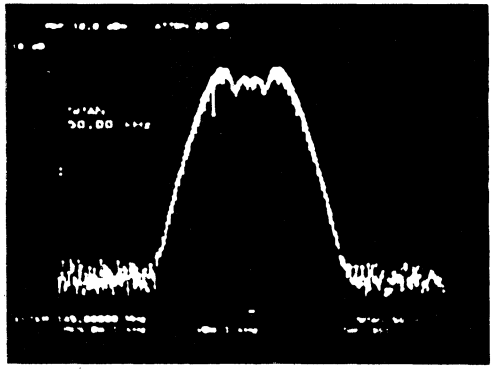
(a) Unmodulated 10kHz span



(b) Unmodulated 100kHz span



(c) Modulated 400Hz 5kHz deviation 50kHz span



(d) Modulated 1kHz 5kHz deviation 50kHz span

Fig.2 NJ8822 frequency synthesiser spectral performance

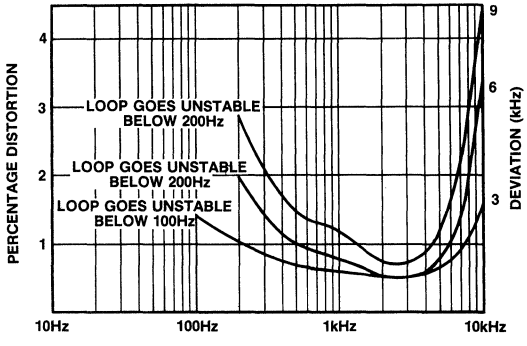


Fig.3 Graph of distortion against modulating frequency at various deviations for the NJ8822 VHF frequency synthesiser

Design Compromises in Single Loop Frequency Synthesisers

The single loop frequency synthesiser is justly popular as an approach to frequency synthesis. It has the merit of simplicity, and because of this, low cost, especially as a large amount of the circuitry is easily produced in monolithic integrated circuit form.

Certain performance parameters of the synthesiser are defined by the equipment performance. For example, a marine VHF radio frequency synthesiser has requirements for phase noise and discrete spurious outputs defined by the adjacent channel specification, and the phase noise performance may well need to be several dB better than would at first be expected. If the adjacent channel rejection is 70dB for example, then a single sideband phase noise level in the receiver bandwidth must be more than 70dB, see Fig.1. In fact, the translated noise level should be reduced by an amount dependent upon the performance of other areas of the equipment and these specification levels are typically determined by the system architect. Frequently, however, during design of a project, some modifications in architecture become apparent, but an understanding of practical limitations is vital at an early stage if delay and consequent expense is to be avoided. For further details on the effects of phase noise on receiver performance, see Ref.1.

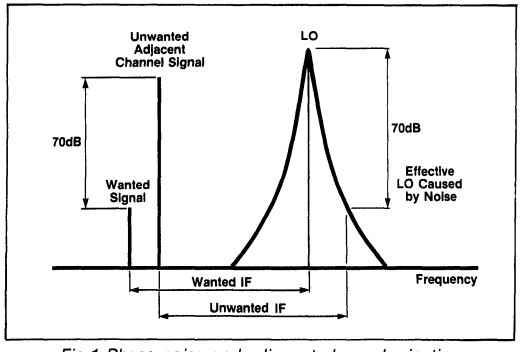


Fig.1 Phase noise and adjacent channel rejection

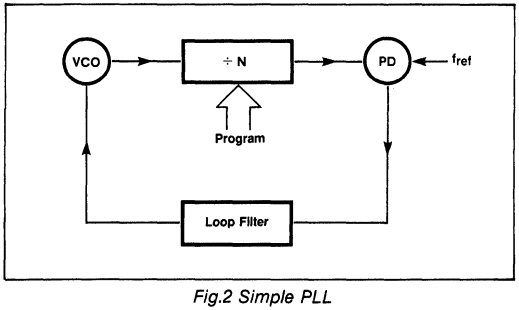


Fig.2 Simple PLL

DIVIDERS

Single loop synthesisers using direct division as in Fig.2 suffer from certain limitations. Fully programmable dividers are not generally available for frequencies above about 50MHz without high power consumptions, and even CMOS dividers currently available are limited in applications at low (5V) supply voltages and extreme temperatures. Newer devices are appearing, however, and experimental 250MHz operation has been observed.

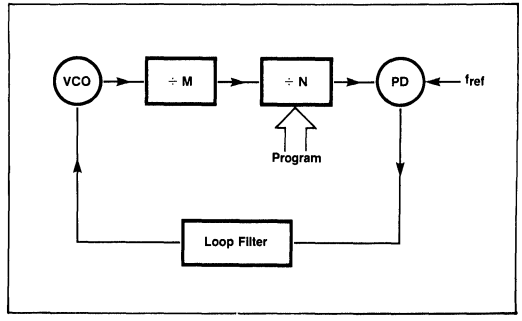


Fig.3 Use of a fixed prescaler

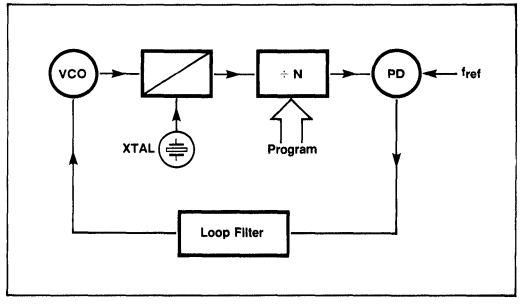


Fig.4 Mixing in the loop

Early synthesisers used fixed prescalers to divide the VCO down to a suitable frequency for the programmable counter as in Fig.3, or used mixing techniques as in Fig.4. Indeed, a large number of CB radios use the mixing technique, but this system can suffer from spurious products unless carefully designed in choice of frequencies, input levels and particular mixers used, see Refs. 2,3,4 and 5. In addition, the large variation in subsequent division ratio may give problems with loop dynamic performance.

A major area of conflict lies in the choice of reference frequency. In synthesisers such as Fig.3, the output frequency step size is *M* times, the reference frequency, where *M* is the prescale ratio. In a system where every channel is used, the problem is then that the reference frequency has to be decreased by a factor of *M*, and as a result, the bandwidth of the feedback loop must decrease. The bandwidth and damping factor of the loop filter are vitally important parameters in determining such loop characteristics as lock up time as well as the phase noise characteristics. (The effects of loop bandwidth on phase noise will be discussed later.) In general, the widest possible loop bandwidth is required to minimise lock up time and to confer the greatest immunity to shock and vibration. However, the loop bandwidth cannot be greater than the reference frequency and so the use of a fixed prescaler is obviously somewhat limited. The alternative is the widely used 'Two Modulus' or 'Pulse Swallowing' prescaler system, illustrated in Fig.5. In this method, the prescaler is able to divide by two integers *N* and *N* + 1. The two counters *A* and

M are programmable and are clocked in parallel, the divider being set initially to the $N + 1$ ratio. When the A counter is full, the divider is set to divide by N until the M counter is full, giving a total division ratio of $MN + A$. This system is limited to a minimum division ratio of $N^2 - N$ if every value of N is to be achieved (no 'skipped' channels) and the M counter must always be programmed to a bigger number than the A counter. Within these limitations, however, a fully programmable divider is achieved and so f_{ref} can now equal the channel spacing.

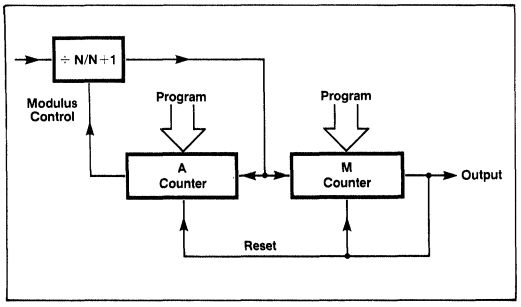


Fig.5 Two modulus divider

Another and more subtle limitation is in the delay times of the various components within the loop. When the circuit (Fig.5) has counted down so that the M counter has been filled, the whole system is reset, and quite obviously, must achieve this in a time equal to $N + 1$ cycles of the input frequency e.g. in a ÷64/65 prescaler, at 1GHz, the reset of the M and A counters must be achieved in 65 cycles or in this case, 65ns. This means that the propagation delays plus set up/release times plus reset delays must not exceed 65ns and it is this area where trouble can often be expected, especially at temperature extremes. Although a 1GHz synthesiser with a 64/65 divider only sees an input frequency of 15MHz for 1GHz input, the set up/release time and delays may well easily reach 85-90ns and the system will thus fail.

If the propagation through the divider $= t_d$
the set up time $= t_s$
the release time $= t_r$
the propagation delay through the A and M counters $= t_c$

then

$$f_{max} = \frac{N}{(t_d + t_s + t_c)} \text{ or } \frac{N}{(t_d + t_r + t_c)}$$

whichever is least.

One of the areas in which an increase in loop delay time can inadvertently occur is if the A and M counters trigger from a different edge to the dual modulus prescaler. This can cause a major diminution in available loop delay, as can an attempt to physically separate the divider and control circuits. Other deleterious affects have been noted, such as radiation of the divider output to the VCO, producing high frequency sidebands, so practical synthesisers are best produced with little physical spacing between divider and control circuit.

The control circuit is a practical device in a number of technologies, although modern devices exclusively use CMOS to minimise power consumption. Prescalers are still mainly exemplified by bipolar technology, advances in which have seen major reductions in power consumptions in recent years - for example from 65mA at 5V for a divide by 10/11 operating at 250MHz in 1976 to 4mA at 5V for a divide by 40/41 operating at 225MHz today. Some equipments still build up the A and M counters from discrete ICs and then add phase detectors, reset circuitry and so on, but such equipments are by now obsolete in design and extremely expensive to manufacture. Nevertheless, the lessons of tolerancing delays necessary in such designs should not be forgotten just because the majority of circuitry is now hidden inside a block of silicon.

The choice of prescaler ratio is governed by a number of factors. Discussed so far have been minimum ratio and loop delay. However, the output frequency of the divider must be low enough for the A and M counters to function. Summarising

1. $f_{in} \leqslant N\, f_{max\ control}$
   where N is the divider ratio
   $f_{max\ control}$ is control circuit maximum operating frequency.
2. $f_{min} \leqslant \dfrac{N}{\text{total loop delay}}$
3. $P_{min} = N^2 - N$
   where P_{min} is the minimum divide ratio.
   N is the dual modulus divider ratio.

Various values for N exist in proprietary devices. These range from 3/4 to 128/129: binary values (32/33, 64/65, 128/129) are popular for ease of programming from ROMs and microprocessors, while decimal and BCD are used for thumbwheel switch programming.

Programming is a straightforward exercise for binary division and the following method is recommended.

1. The A counter should contain x bits such that
   $$2^x = N$$
2. If more bits are included in the A counter, these should be programmed to zero.

e.g.
$N = 64 = 6$ bits
$A = 10$ bits
then the 4 MSB are programmed to zero.

3. The M and A counters are treated as being combined so that the MSB of the M counter is the MSB of the total and LSB of the A counter is the LSB of the total.

e.g.
A synthesiser operating from 430-440MHz in 25kHz steps uses a 64/65 divider, and the control circuit uses binary counters.
$P = f/f_{ref}$ and f_{ref} = channel spacing = 25kHz
$P_{min} = 430/0.025 = 17200$
$P_{max} = 440/0.025 = 17600$

Minimum possible divide ratio is $N^2 - N = 4032$
where N is two modulus divider ratio

Maximum allowable loop delay $= \dfrac{64}{440 \times 106} = 145\text{ns}$

Total divide ratio, P, is given by
$P = NM + A$
$N = 64$, as a 64/65 divider is used
P_{min} from above is 17200
Therefore $17200 = 64M + A$
And $M \geqslant A$

Let $A = 0$ Then $M_{min} = \dfrac{17200}{64} = 268.75$

$= 268$

and $M_{max} = \dfrac{17600}{64} = 275.0$

Thus the M counter must be programmable from 268 to 275 as required: the M counter must have at least 9 bits.

For a frequency of 433.975MHz

$$P = 433.97/0.025 = 17359$$

therefore

$$M = \frac{17359}{64} = 271.2343$$

The A counter is programmed for the remainder i.e.

$$0.2343 \times 64 = 15$$

From this, the A counter is programmed to 15 and the N counter to 271. The output frequency can now be checked.

$P = NM + A$
$= 271 \times 64 + 15 = 17359$
and this is the required divider ratio.

The two modulus prescaler is therefore able to offer the advantages of producing a programmable divider operating at a very high frequency, but consuming a fraction of the power of such a divider. This enables the reference frequency to equal the channel spacing, thus allowing maximisation of loop bandwidth with its concomitant faster lock up time. It is limited by total loop delay, maximum operating frequencies of dividers and counters, and in minimum count values, but is nevertheless a powerful tool for the synthesiser designer.

The limitation on the value of P_{min}, the minimum ratio can be avoided by the use of three and four modulus dividers. The use of a four modulus counter allows a very wide frequency range to be covered with one device, but at the expense of a much higher power dissipation. Typical of such devices are the Plessey SP8901 and SP8906. Power consumptions for 2-modulus dividers typically range from 4mA at 200MHz (Plessey SP8792/3) through 11mA at 520MHz (Plessey SP8716/8/9) to 25mA at 1GHz (Plessey SP8703).

LOOP BANDWIDTH AND PHASE NOISE

As stated earlier, phase noise is a very important parameter in frequency synthesisers. Too many early synthesisers suffered from phase noise problems which manifested themselves as poor equipment performance in such areas as multiple signal selectivity and ultimate signal to noise ratio. The performance of the synthesiser may be degraded or improved by changing the loop bandwidth, depending upon the characteristics and parameters involved.

The general characteristics of a phase locked loop (PLL) are that for signals injected into the loop it acts as a low pass filter for signals inside the loop bandwidth, and as a high pass filter for signals outside the loop bandwidth. To analyse the performance, consider modulation of the VCO at very low frequencies. The output of the phase detector will be a low frequency signal of phase such as to attempt to remove the modulation imposed on the VCO. As the modulation frequency increases, the error component of the phase detector output is not passed by the loop filter, and so the modulation is not removed by the loop. Note that the modulation is phase modulation (PM) up to the filter break point, and frequency modulation (FM) thereafter. In the 'in-between' range, some interesting distortion effects can occur, especially when excessive group delay exists in the loop filter.

The relationship of loop filter bandwidth to phase noise is now apparent. Phase noise from the oscillator corresponding to frequencies below the filter bandwidth will be removed by the loop, while phase noise components outside the loop bandwidth will be unaffected by the loop. Under these circumstances then, the VCO output spectrum will be cleaned up by the loop. However, for frequencies inside the loop bandwidth, other factors enter. Variations in the reference frequency cause variations in output frequency from the synthesiser, and phase noise components at the reference frequency are purely the frequency domain transforms of time domain frequency instability (Refs. 6,7 and 8). These phase noise effects are multiplied in the loop by the divider ratio. An example (admittedly using gross instability for demonstration) is shown.

If the 430MHz synthesiser has an instability of +1Hz in the 25kHz reference frequency, this is multiplied by P.

i.e. for operation at 433MHz
$P = 433/0.025 = 17320$

Therefore IF +1Hz at 25kHz gives +17.32kHz at final frequency.

Phase noise at the reference frequency is derived from two sources:

(a) the system standard oscillator
(b) the reference chain divider

Oscillators for standards are available with very low phase noise characteristics, and -130 to -170dBc/Hz at 1kHz offset covers the usual range. This phase noise is modified by the reference divider and multiplied by the division ratio as explained above. Of course, phase noise at any offset is reduced by division until the phase noise floor of the divider is reached. Little has been published on the causes of phase noise in dividers, although various measurements have been made (Ref. 9). It has been suggested that TTL and CMOS dividers are better than ECL and CMOS is better at low (10-20Hz) offsets. At a 1kHz offset, ECL levels of about -155 to -165dBc/Hz appear usual. The explanations for the occurence of phase noise is intuitively regarded as being jitter in the transition point of the signal: on this basis, one would not expect CMOS to be so good as TTL insofar as the rise and fall times will be somewhat slower. Regrettably, the difficulty and cost of making meaningful measurements is an inhibiting factor: data on the phase noise performance of Gallium Arsenide dividers would be of considerable interest, especially at small frequency offsets.

From the above discussion, a phase noise floor of some -150dBc/Hz can be expected at the end of the reference frequency divider chain if a good frequency standard is used, while a low cost one may well be at about -130dBc/Hz. In our 430MHz synthesiser, a degradation at 1kHz (if the loop is wide enough) of some 84dB will be seen, so inside the loop bandwidth, the noise performance will be limited to $-130 + 84 = -46$dBc/Hz. At lower offset frequencies, the phase noise of dividers and frequency standards is worse, so the phase noise performance is now being defined by the loop, rather than the VCO. These are worst case figures, but the ultimate signal to noise ratio of an FM receiver can clearly be seen to be easily limited at UHF by multiplied phase noise. Fortunately, the noise enhancement by the loop is such that pre-emphasis of the modulation provides major improvements in signal to noise ratio.

Nevertheless, it is obvious that the choice of loop bandwidth is compromised by the ultimate signal to noise level required by the system and that such factors as reference oscillator noise level and divider noise cannot be totally disregarded. Operation in the usual cellular radio bands at 800 or 900MHz makes the situation some 6dB worse than that analysed above and the use of a psophometric audio weighting in the equipment is advisable. Sub audible tones may well need fairly high deviation if signal to noise performance is not to be severely limited on them, although modern decoders will work with a negative signal to noise ratio (Ref.10).

In the single loop synthesiser, the phase noise in adjacent channels, which determines the adjacent channel performance, is, to a first order, unaffected by the loop and its parameters. Second order effects such as noise modulation

by such loop components as high value resistors and operational amplifiers may be negated by the use of a passive low pass filter prior to the VCO. Phase noise in the oscillator is discussed below.

Even where the effects of multiplied phase noise may be ignored, such as where the reference divider chain noise is sufficiently low, certain other problems occur in the loop filter design. Many of these are associated with the phase detector employed, which in many areas has been a digital phase/frequency detector. Various types of detector have been used over the years, from an OR gate producing a variable mark space ratio to the well known 2 D type detector. The first of these used integration of the variable mark-space ratio to produce the required output, while the latter (Fig.6) produces minimal width pulses on both Φu and ΦD when in the zero phase error condition. Unfortunately, the zero phase error state exists for a degree of phase error dependent upon the propagation of the gates and a phase error/output voltage characteristic such as Fig.7 is achieved. The performance in the central flat portion of the characteristic means that the loop gain falls to zero when the phase error reaches some small but finite value, and this leads to an increase in the low frequency phase noise of the loop. This phenomenon is of course related to the reference frequency of the loop, being worse at high comparison frequencies.

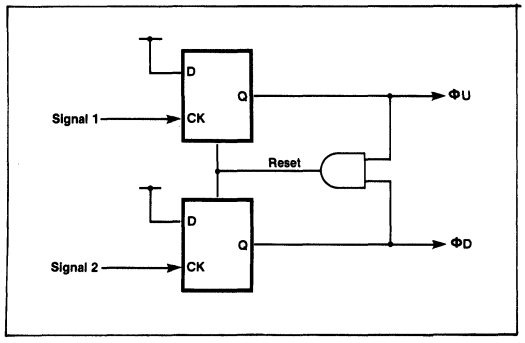


Fig.6 Dual D type phase discriminator

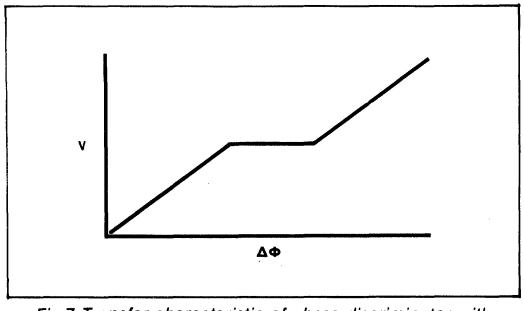


Fig.7 Transfer characteristic of phase discriminator with a charge pump

Although a number of approaches have been made to minimise this problem, including the provision of a leakage path across the VCO control line (Ref. 16), the better approach is to use a linear phase detector of high gain to 'fill in' the gap in the response. An additional benefit of this method is that if the digital phase detector has a 'tri-state' output for the area in which the dead zone occurs and the linear phase detector operates, then the phase detector output at comparison frequency is reduced, allowing either a wider loop bandwidth for the same comparison frequency sideband rejection, or increased rejection, or to some extent, both. The analog phase detector may easily be given a very high gain and narrow range of operation - say a 2 degree range with a gain of 600 volts/radians, but only a limited lock range. It is however, essential to ensure that saturation of this detector, and indeed of the loop filter/amplifier is minimised, as under channel change conditions, the control line and thus the filter amplifiers can be driven hard into saturation. A long recovery time here may well make a mockery of any lock up time calculations. It is this approach which has been adopted in the NJ8820 series of CMOS control circuits from Plessey with a large degree of success.

The choice of loop bandwidth is also governed by the time to change channel, and here again, compromise is often necessary. For example, a lock up time of 1ms and a loop bandwidth of 100Hz are apparently mutually incompatible. By using the two detector approach outlined above however, the loop bandwidth for the digital detector may be made much wider than the analogue detector, thus providing a form of adaptive filtering. The basic loop equation for a type 2 2nd order loop is

$$\omega_n = \sqrt{\frac{K_0 K_v}{N t_1}}$$

where ω_n = loop natural frequency, K_v = VCO gain in Rad/S-v, K_0 = phase detector gain in volts/rad, N = division ratio and t_1 = integrator time constant, shows the dependence of ω_n, the loop natural frequency on N. It should be noted the 3dB bandwidth of the loop and the natural frequency ω_n, are not identical - except for a damping factor, $D = 3.02$.

It was stated earlier that noise caused by the phase detector and loop filter is easily filtered to avoid noise in adjacent channels and the use of low-noise components in loop filters (NOT a 741!) is advisable. Where possible, time constants should use large capacitors and small resistors to minimise KTBR noise. $1/f$ noise can be a problem with operational amplifiers, and where loop bandwidth is high, slew rate is important if the dynamic loop bandwidth is to beary any relationship to the small signal case.

To summarise, the choice of loop bandwidth affects close in phase noise and lock up time. Phase noise is produced by dividers, phase detectors and filters, and when multiplication ratios are high, the reference frequency phase noise can be dominant when multiplied. To minimise this effect, the loop bandwidth can be narrowed, since noise outside the loop bandwidth is determined soley by the VCO. Typical divider phase noises of -150 or -160dBc/Hz can be expected, so low cost reference oscillators can dominate the noise performance.

VOLTAGE CONTROLLED OSCILLATORS

Many engineers consider VCO design to be a black art, and although some art is occasionally involved, VCOs are amenable to analysis.

In the single loop synthesiser, the phase noise performance outside the loop bandwidth is dominated by the VCO, with the noise generation by passive components in the loop filter generally being of lesser importance.

Scherer, Leeson (Ref.12) and Robins (Ref.13) have analysed oscillator phase noise performance and Scherer (Ref.14) has demonstrated the applicability of Leeson's equations and uses the equation

$$L_{(f)} = \tfrac{1}{8} \left[\frac{FkT}{P_s}\right] \frac{(f_o)^2}{(f)} \left[\frac{1}{Q} + \frac{P_o}{\tfrac{1}{2}CV^2 2\pi f.}\right]^2 \quad \text{Eq. 1}$$

where $L_{(f)}$ is the SSB phase noise at an offset F
F is the Noise Figure of the amplifier in the oscillator
k is Boltzmann's Constant
T is the Temperature
P_s is the available signal power
f_o is operating frequency
f is the offset at which the power is to be calculated
Q is working Q of the tuned circuit
C is tank capacity
V is tank current peak voltage
P_o is rf output power

By inspection of Eq. 1, it may be seen that the phase noise is proportional to Q^{-2} and also to (frequency offset)$^{-2}$. This means that for each octave decrease in the offset frequency, the noise power will increase by 4 times or at 6dB/octave. As the frequency offset decreases 1/f or flicker noise becomes important: this 'break' frequency can be as high as 50MHz with GaAs devices. From Eq. 1, it may be determined that a low phase noise oscillator will have a large voltage swing, a high working Q and provide little output power to the load. There is of course a limit as to the level of power required, as the noise of any subsequent buffer amplifiers will degrade the oscillator.

A major compromise in the design of equipment is the choice of VCO frequency. If, for example, a 800MHz cellular radio type of receiver is considered, some fairly straightforward calculations will serve to act as a guide. Starting with the receiver parameters, we will assume that a 70dB rejection of a signal two channels (60kHz) away is required. A numbr of receiver sub system parameters are involved.

(a) Synthesiser phase noise
(b) IF filter performance
(c) Co-channel rejection ratio
(d) Gain compression of stages before the main IF selectivity.

Of these parameters, (c) is the least obvious in its applicability. Ref.1 showed how oscillator noise was mixed onto a wanted signal by a strong unwanted signal. The degradation of a wanted signal by this noise obviously depends upon the relative levels of signal and noise, and because the noise is on the same frequency, the Co-channel rejection. Typically, this means that a noise level within the IF passband of some 8dB less than the signal is required. Thus for the 70dB rejection, oscillator noise at -78dB is required, and 80dB would thus be the design aim.

Conversion of this level to dBc/Hz is not straightforward because of the non linear slope of the phase noise. However, for narrow bandwidths at large offsets, little error is obtained by approximating the phase noise slope to a straight line. This may be illustrated as follows:

From Eq. 1, the power spectrum at an offset beyond the flicker noise knee is given by:

$$P_o = Kf^{-2}$$

where P is the noise power
K is a constant
f is the offset

For a frequency band bounded by f_{lower} and f_{upper}, the noise power is:

$$P_t = \int_{f_L}^{f_U} Kf^{-2}\,df = \left[-Kf^{-1}\right]_{f_L}^{f_U}$$

$$= K(f_L^{-1} - f_U^{-1})$$

Therefore

$$K = \frac{P_t}{(f_L^{-1} - f_U^{-1})}$$

P_t has been defined as the phase noise in the band = -80dB therefore

$$K = \left[\frac{10^{-8}}{\frac{1}{53.5 \times 10^3} - \frac{1}{67.5 \times 10^3}}\right] = 2.58 \times 10^{-3}$$

To find the phase noise in a 1Hz bandwidth at an offset f

$$P = Kf^{-2}$$

so at 53.5kHz

$$P = \frac{2.58 \times 10^{-3}}{(53.5 \times 10^3)^2} = 0.901 \times 10^{-15}$$

$$= -120.5\text{dBc/Hz}$$

At 60kHz

$$P = -121.4\text{dBc/Hz}$$

and at 67.5kHz

$$P = -122.5\text{dBc/Hz}$$

If the 'break point' for 1/f noise is above 60kHz, then the spectral density is determined by noise rising at f^{3}. Similar procedures are followed:

$$P_o = K'f^{-3}$$

$$P_t = \int_{f_L}^{f_U} K'f^{-3}\,df = -K'\left[\frac{f^{-2}}{2}\right]_{f_L}^{f_U}$$

$$= \frac{-K'}{2}(f_U^{-2} - f_L^{-2})$$

$$= \frac{K'}{2}(f_L^{-2} - f_U^{-2})$$

Using similar figures, the performance required is:

53.5kHz	-120.0dBc/Hz
60.0kHz	-121.5dBc/Hz
67.5kHz	-123.0dBc/Hz

The error by assuming a linear relationship is given by:

IF bandwidth = 15kHz
therefore noise power is 10 log$_{10}$15 x 10^{3}dB greater than in a 1Hz bandwidth
which is 41.8dB
therefore if the noise power is 80dB down on the signal, total carrier to noise power ratio is -121.8dBc/Hz at 60kHz.

This in fact gives a requirement some 0.4dB higher than previously calculated and in 120dB is obviously negligible.

Having decided upon the level of allowable oscillator noise, it is now possible to calculate the best methods of achieving this level. Using Scherer's figures from Ref.13 for a 400MHz oscillator which will be doubled, using parameters of:

Q = 200
C = 23pF
V = 10V pk
$\frac{FKT}{P^5} = \left[\frac{6nV}{1V}\right]^2$ where 6nV is the noise voltage and 1V is the input before limiting.

The noise power P at a 30kHz offset is, from Eq. 1, -135dBc/Hz.

So far flicker noise has been ignored. Flicker noise is a low frequency phenomonen which causes problems by intermodulation with the carrier frequency to produce noise sidebands. The 'break point' at which flicker noise becomes dominant varies but a UHF VCO of the type under consideration would probably have a break point at about 50-150kHz offset from the carrier. Eq. 1 needs some

modification to include this factor and a multiplicand of

$$\frac{(1 + f_e)}{f}$$

may be used, where f_e is the 1/f noise corner frequency.

The previously calculated noise will now be degraded by about 8dB under these conditions, (assuming $f_e = 150$kHz) and will now be -127dBc/Hz. This is about 5dB inside the previously calculated requirement. Note that calculations have been made on the basis of a 30kHz offset to allow for doubling the oscillator frequency.

Considering an oscillator with a fundamental frequency of 800MHz, a number of problems appear. Ignoring for the time being the increased noise figure of the device, the available Q of components is considerably less - for example high quality chip capacitors can offer Q's of about 200, leading to working Q of about 100. Calculating noise levels for a 60kHz offset with all other parameters constant except tank capacity which is 12pF (half the 400MHz oscillator) the noise at 60kHz is -105dBc/Hz or about 17dB outside the requirement. Obviously, these figures are no more than a guide, but the suggestion is that the doubled 400MHz oscillator will meet requirements, while the 800MHz oscillator will not (see Fig.8).

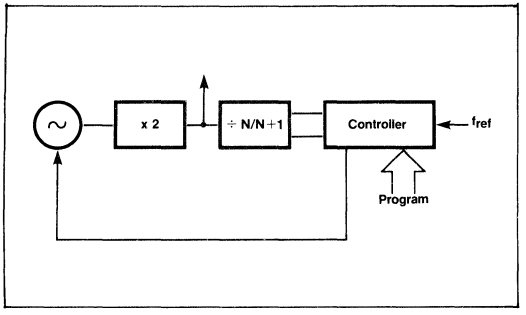


Fig.8 Use of a lower frequency oscillator for improved phase noise

Flicker noise can be reduced by the inclusion of local DC negative feedback, such as an unbypassed emitter resistor, but a major requirement is to choose a suitable device. In general a low phase noise oscillator will run at high power, using a device with both low flicker noise and low high frequency noise, and with high gain and minimum damping on the tuned circuit. In fact, in many applications, the thermionic tube is attractive! Q should be as high as possible, and where VCOs are concerned, the MHz/V should be minimised. This is because of the effects of noise - at 10MHz/V, 1 microvolt of noise will produce 10Hz of FM deviation.

Where relatively wide frequency ranges are concerned, the variation in loop bandwidth may cause problems.

$$\omega_n = \sqrt{\frac{K_o K_v}{N t_1}}$$

where ω_n = natural loop frequency
K_o = VCO constant
K_v = phase detector constant
N = divider ratio
t_1 = integrator time constant

ω_n varies with N, and where desirable to maintain equal lock up times and loop bandwidth, K_v may be designed to vary with N. Several methods exist, but the use of a transmission line VCO can prove useful, as the effective inductance increases with frequency. The use of a suitable length of transmission line can provide an oscillator tuneable from 130 to 190MHz with a coarse tuning trimmer, and electrically tuneable over 6MHz at the bottom of the band to 8.75MHz at the top, thus maintaining ω_n sensibly constant. The use of PIN diodes to switch capacitors is possible, although care must be taken not to degrade Q e.g. a 10pF capacitor at 150MHz has $X_c = 106\Omega$. A PIN diode with an ON resistance of 0.5Ω will give $Q_{MAX} = 212$, assuming a perfect capacitor, and as considered earlier, this can have disastrous effects on phase noise performance.

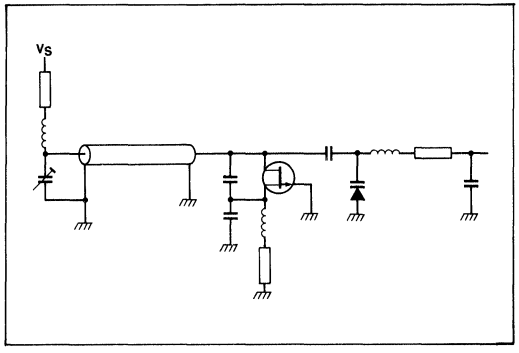


Fig.9 Transmission line VCO using the line as an impedance inverter

An initially attractive method of realising the transmission line VCO is shown in Fig.9, where a length of line is used as a reactance inverter, changing the capacity into an inductance. The use of a Smith Chart will, however, show that the resulting inductance will have a low reactance unless the terminating capacitor is large and the line relatively long (greater than ⅛ wavelength). This leads to a low Q circuit as the resistance of the line is constant, and measurements made using a 16cm rigid coax 75Ω line with a loss of 4dB/100ft at 150MHz gave a Q of less than 100. This line was terminated with an air spaced trimmer. The same line as a shortened capacitively loaded resonator as in Fig.10 had a Q of over 250.

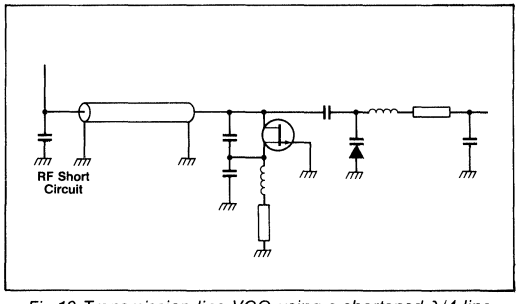


Fig.10 Transmission line VCO using a shortened λ/4 line capacitively loaded

SUMMARY

The compromises in the synthesiser design are now apparent: a narrow bandwidth is required to minimise multiplied reference noise, but a wide bandwidth is needed to minimise lock up time. A high oscillator frequency may be required to avoid spurious outputs and multiplier chains, while a low frequency and multiplier chain give the best performance on system phase noise and possibly power consumption. The classical way to minimise these problems is the two loop synthesiser, but cost is a determining factor effecting the compromise finally reached. Power consumption is always a problem and unfortunately is more demanding at high frequencies while increasing channel occupancy will lead to ever tighter performance requirements in terms of phase noise and switching time.

Modern integrated circuits help the designer by providing better phase detectors and faster lower power dividers. Nevertheless, the single loop synthesiser has been shown to involve a number of compromises in its design, and in some cases, these compromises may limit the final equipment performance level. The single loop synthesiser is very useful, but is not universally applicable.

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The care and feeding of High Speed Dividers

Circuit design and layout for high speed dividers operating at frequencies up to 2GHz owe much more to analog RF design techniques than normal digital ones and the limitations on flexibility and component choice inherent in UHF RF design are of paramount importance in successful designs.

PRACTICAL DESIGN CONSIDERATIONS

High speed divider applications require the printed circuit boards to be mechanically designed with two considerations in mind:

(1) Electrical performance
(2) Mechanical and thermal performance.

These two considerations are inter-related; for example, the use of 1/16 inch thick fibreglass PC board may be desirable mechanically, but a 50Ω stripline on this thickness of board is about 5/32 inch wide, and is thus too wide to pass between the pins of an IC.

Most of the heat conducted from a dual-in-line IC package is removed from the bottom of the package. Less than 10 % is conducted out by the leads, and because of the cavity between the chip and lid, relatively little through the top of the package.

For this reason, the use of a double-layer PC board layout is recommended, with a ground plane top surface. Where 1/32 inch thick material is used, a top surface ground plane will add substantially to the heat dissipation capabilities of the board.

For use at very high frequencies, consideration must be given to the type of component used. Carbon composition resistors are more nearly resistive at high frequencies than either carbon or metal film types, and are available in very small sizes. Bypass capacitors need to be chosen carefully if they are to act as low impedances, as series inductance leads to an increasing impedance with frequency above the series resonant frequency of the device. As a guide, a 1000pF disc ceramic capacitor with 1/4 inch leads will be self resonant at about 75MHz, and will appear as an inductive impedance of about 22Ω at 800MHz. The use of chip capacitors is recommended above 500MHz, although leaded monolithic ceramic capacitors with suitably short leads are often acceptable.

The use of a ground plane for RF decoupling purposes is often recommended, and can be helpful. However, the danger is that the ground current paths in the plane are not defined very well, and because of this lack of definition, the ground plane can cause unsatisfactory operation. Probably the best method is to return all the bypass capacitors to a single point (as in Fig.1) and return this point to the ground plane.

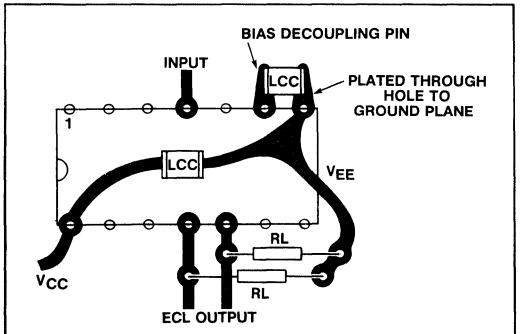


Fig.1 Single point grounding

Also note that in Fig.1 the output load resistors have their grounded ends connected together and a common return used. Because the currents in the resistors are in antiphase, cancellation of the inductive effects taken place, and the path followed by the relatively large output currents is controlled. Defining the ground current path is more important in applications like frequency synthesis, where a relatively large part of the system may be on one PCB.

It is well known that the effect of mismatching a transmission line is to cause variations in the voltage along the line. Standard practice at Plessey Semiconductors has been to use a 5:1 attenuator manufactured from 'microdot' resistors as an attenuator feeding a 50Ω sampling oscilloscope or a power meter. Although a high VSWR will exist on the line from the generator to the test fixture, the theory is that the line from the power meter to the attenuator will be a matched line, and so the power measured is 14dB lower than the power at the device input pin. This method has been proved very successful, even if simple, and offers some advantages over the use of hybrids or directional couplers.

The use of a matched 50Ω system can help, and using microstrip techniques, a track with a defined impedance is reasonably practical. The impedance of a microstrip line is given by:

$$Z_O = 377\ (L/w)\ (1/\varepsilon_r)$$

Where L = dielectric thickness, w = width of track and ε_r is the relative permeability of the board material.

Some correction factors have to be applied, and typically, on 1/16 inch glass fibre epoxy board, the following sizes provide a guide to track width

100Ω - 1mm
75Ω - 2mm
50Ω - 4mm

These impedances rely on the ground plane on the obverse of the board being complete, and where boards are wave soldered, it may be necessary to make arrangements to prevent blistering.

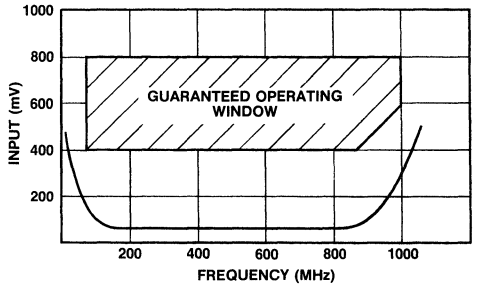


Fig.2 Example of input sensitivity curves

The input level of a divider should be maintained within the guaranteed operating window shown on its data sheet (Fig.2). Excessive input can vary in its effects, from causing permanent damage to miscounting, especially when cold. Running the device at too low a level can cause problems, even though the level is within the 'typical' performance line of the device. An ECL output signal on pin 6 of the device in

Fig.3 can couple 60mV of signal to the input shown on Fig.2 at 500MHz. Such a level of coupling can lead to divider jitter if the input signal is low, and it becomes very necessary to keep the inputs and outputs well separated at the higher frequencies. This includes ECL lines to modulus control pins on two modulus dividers.

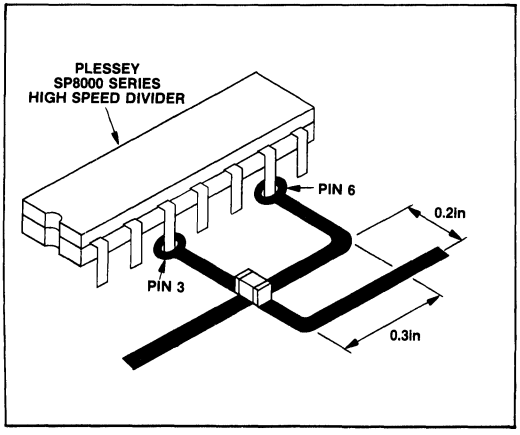


Fig.3 Coupling between parallel tracks

Most dividers are edge triggered, and although they are specified over a frequency range with sine wave input, they will operate to lower frequencies provided a suitably high slew rate is provided on the input signal. This is generally of the order of 100 to 200 volts/microsecond. This should be achieved by shaping of the input signal, for example by limiting, rather than by overdriving the device.

The outputs of devices may be of the following forms:

(1) ECL
(2) Open collector TTL
(3) TTL
(4) CMOS

Of these, the ECL output is well defined; some devices require external load resistors and the data sheet should be consulted. Where these external resistors are required, suitable interconnection techniques should be used between them and the device; the resistors should be carefully chosen for their non-inductive properties when output frequencies are very high. Where an ECL output divider drives another divider it is best to AC couple, since few dividers are strictly ECL-compatible on their inputs.

Open collector TTL outputs are relatively slow. Although the negative edge is limited in speed by the turn-on time of the output transistor, the rising edge is limited by the external load resistor and capacitance to ground. In practice this means that short narrow tracks are required to the following device, and a minimum 'fan-in' load provided. In addition, open collector TTL should not be used above about 10MHz output frequency.

True TTL outputs are not so limited, because of the active pull-up. Nevertheless, the use of such outputs at frequencies above about 25-30MHz is not recommended, especially into capactive loads. Loads of more than 30pF should not be driven faster than about 15MHz. Note that the current drawn by true TTL outputs increases with increasing load capacitance.

CMOS outputs are, on the face of it, TTL-compatible. However, investigation will show that the outputs are not guaranteed to meet TTL levels at TTL currents and it is not recommended that CMOS output devices be used to directly drive TTL. Where an interface of this sort is required, an active transistor interface should be used.

Fig.4 shows a circuit for an ECL-TTL interface, using a line receiver. Simple circuits using one or two transistors cannot be guaranteed to work over all the tolerances of ECL output voltages and temperature ranges.

Interfacing to dividers is not difficult if a few simple rules are obeyed. These are:

(1) Observe the input requirements - guaranteed input operating area, and slew rate.
(2) Do not use open collector outputs above 10MHz.
(3) Do not use CMOS outputs to drive TTL.
(4) Use a sensible layout with good components, and sensible values - 0.1 microfarad ceramic capacitors are NOT bypasses at 1.5GHz.

Treating dividers as RF linear devices is probably the best way to ensure successful applications at high frequencies. There is no magic in HF design, only intelligent layout and sensible component choice.

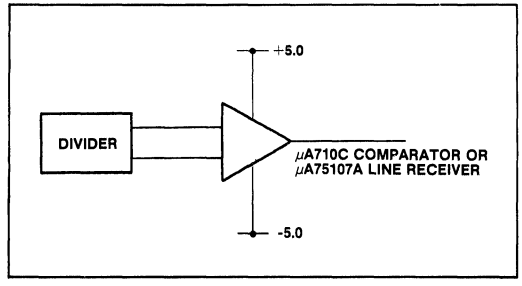


Fig.4 ECL/TTL interface

Impedance Matching

The use of microstrip techniques has been mentioned already. However, in itself this will not produce a matched network and various possibilities exist to improve the matching at the input of a device. These include Tchebycheff impedance transforming networks, narrow band 'L' matching networks, and at high enough frequencies, the use of transmission lines. Wideband matching is often difficult, and attempts should be made to use networks that have the lowest possible working Q. This is for two reasons: firstly a high Q network will not only be narrow band, but will have the capability of increasing the losses, and secondly, a low Q network is generally more tolerant of component variations.

The greater losses in high Q circuits occur because of the greater circulating current: the loss power is I^2R, so that if the Q is doubled with all else constant, the power loss is increased by 4 times.

The easiest method of determining matching components is by means of the Smith Chart.

THE SMITH CHART

The input impedance of SP8000-series high speed dividers varies as a function of frequency and is therefore specified on the datasheets by means of Smith Charts. The following information is included in this handbook as a guide to their interpretation and use.

Construction of the chart

The chart is constructed with two sets of circles, one set comprising circles of CONSTANT RESISTANCE (Fig. 5) and the other circles of CONSTANT REACTANCE (Fig. 6). The values on these circles are normalised to the characteristic impedances of the system by dividing the actual value of resistance or reactance by the characteristic impedance e.g. in a 50Ω system, a resistance of 100Ω is normalised to a value of 2.0.

By combining Figs. 5 and 6 to form Fig. 7, a chart is produced in which any normalised impedance has a unique position on the chart, and the variation of this impedance with frequency or other parameters may be plotted.

A further series of circles may be plotted on the chart: these are circles of constant VSWR, and represent the degree of mismatch in a system. The VSWR is the ratio of the device impedance to the characteristic impedance, and is always expressed as a ratio greater than 1: thus a 25Ω device in a 50Ω system gives rise to a 2:1 VSWR. These circles of constant VSWR have been added in Fig. 7.

Any point can be represented on the Smith Chart: for example an impedance of 150-*j*75Ω can be represented by a normalised impedance (in a 50 Ω system) of 3-*j*1.5 and this point is plotted in Fig. 7 as point A.

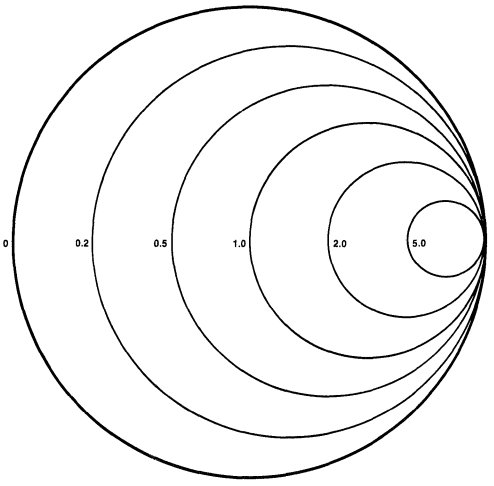


Fig.5 Constant resistance circles

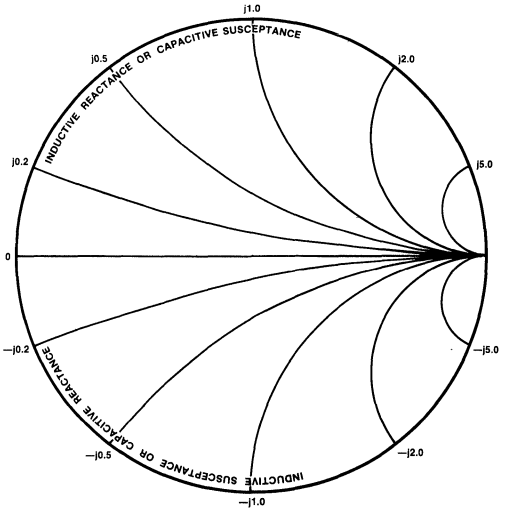


Fig.6 Constant reactance circles

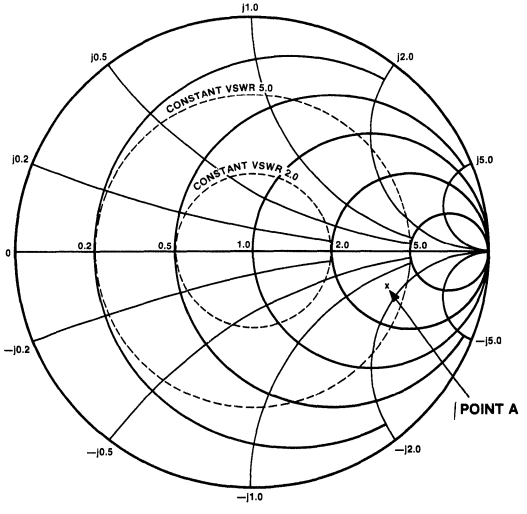


Fig.7 The complete chart

Network calculations

The main application for Smith Charts with integrated circuits is in the design of matching networks. Although these can be calculated by use of the series to parallel (and vice-versa) transforms, followed by the application of Kirchoff's Laws, the method can be laborious. Although the Smith Chart as a graphical method cannot necessarily compete in terms of overall accuracy, it is nevertheless more than adequate for the majority of problems, especially when the errors inherent in practical components are taken into account.

Any impedance can be represented at a fixed frequency by a shunt conductance and susceptance (impedances as series reactance and resistance in this context). By transferring a point on the Smith Chart to a point at the same diameter but 180° away, this transformation is automatically made (see Fig. 8) where A and B are the series and parallel equivalents.

It is often easier to change a series RC network to its equivalent parallel network for calculation purposes. This is because as a parallel network of admittances, a shunt admittance can be directly added, rather than the tortuous calculations necessary if the series form is used. Similar arguments apply to parallel networks, so in general it is best to deal with admittances for shunt components and reactances for series components.

Admittances and impedances can be easily added on the Smith Chart (see Fig. 9). Where a series inductance is to be added to an admittance (i.e. parallel R and C), the admittance should be turned into a series impedance by the method outlined above and in Fig. 8. The series inductance can then be added as in Fig. 9 (see also Fig. 10).

Point A is the starting admittance consisting of a shunt capacitance and resistance. The equivalent capacitive impedance is shown at point B. The addition of a series inductor moves the impedance to point C. The value of this inductor is defined by the length of the arc BC, and in Fig. 10 is $-j0.5$ to $j0.43$ i.e. a total of $j0.93$. This reactance must of course be denormalised before evaluation. Point C represents an inductive impedance which is equivalent to the admittance shown at Point D. The addition of shunt reactance moves the input admittance to the centre of the chart, and has a value of $-j2.0$. Point D should be chosen such that it lies on unity impedance/conductance circle: thus a locus of points for point C exists.

This procedure allows for design of the matching at any one frequency. Wide band matching is more difficult and other techniques are needed. Of these, one of the most powerful is to absorb the reactance into a low pass filter form of ladder network: if the values are suitably chosen, the resulting input impedance is dependent upon the reflection coefficient of the filter.

At frequencies above about 400MHz, it becomes practical to use sections of transmission line to provide the necessary reactances, and reference to one of the standard works on the subject is recommended.

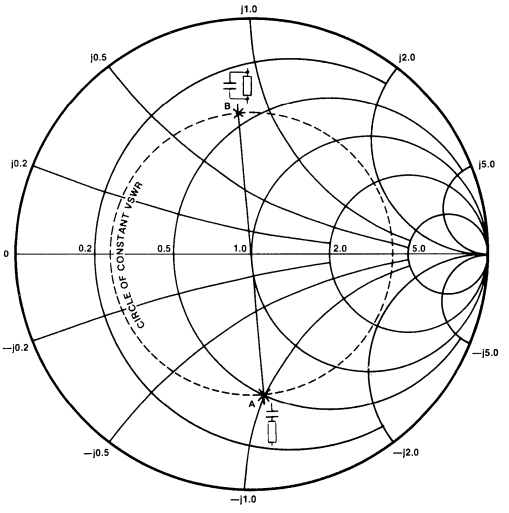


Fig.8 Series reactance to parallel admittance conversion

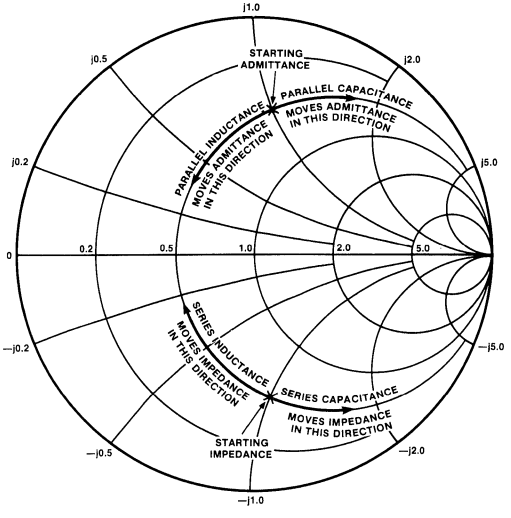


Fig.9 Effects of series and shunt reactance

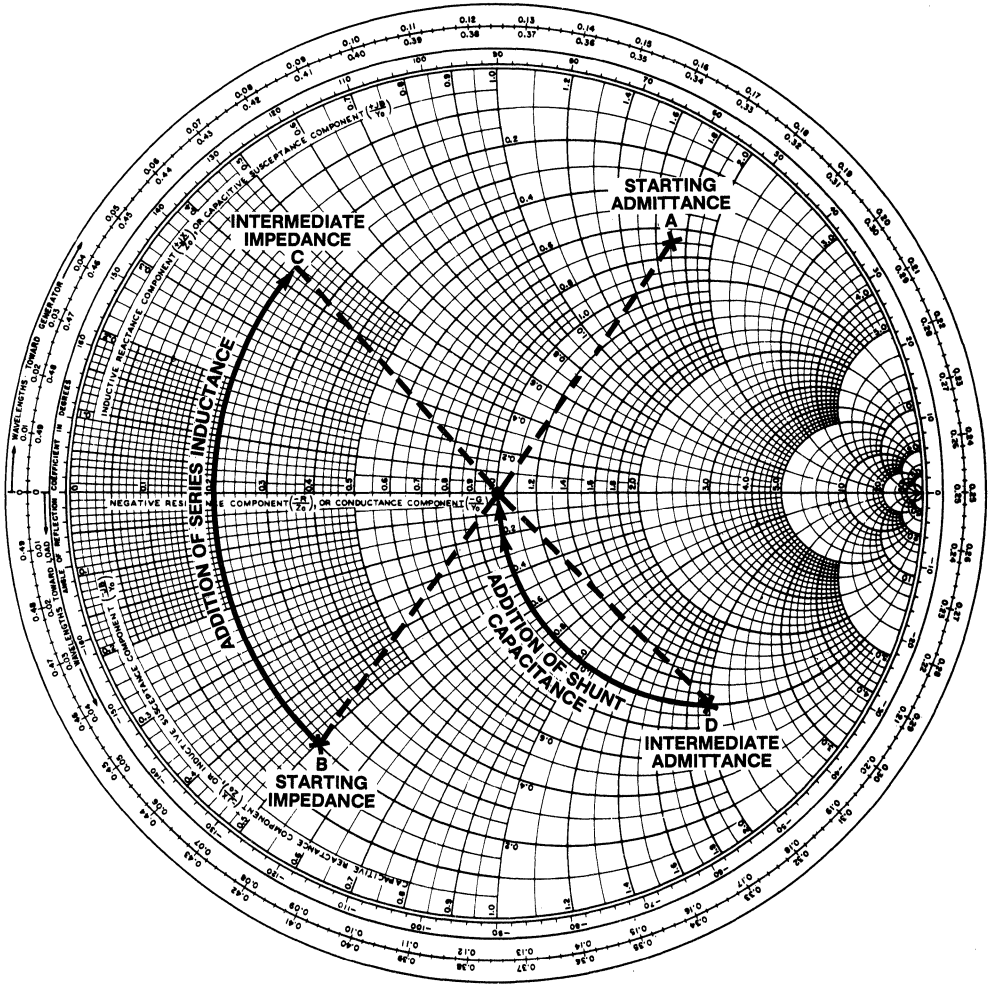


Fig.10 Matching design using the Smith Chart

PHASE NOISE AND DIVIDERS

Phase noise is becoming increasingly important in systems and it is necessary to minimise its effects. First, however, phase noise must be defined.

A spectrally pure signal of a given frequency would appear on a perfect spectrum analyser display as a single straight line as in Fig.11. If the signal is frequency modulated with a discrete modulation frequency, the result will be a comb of frequencies as in Fig.12, while modulation with noise will produce an output spectrum as in Fig.13. Note that the noise density decreases as the offset from the carrier increases. This effect is the result of the effectively lower modulation index *m*. In the case of a Voltage Controlled Oscillator modulated by white noise, a similar effect will be seen, because for a given deviation *f*, the modulation index *m*, (= 1/*fmod*) is greater for lower frequencies than for higher frequencies. Thus the number of sidebands is greater for lower frequencies, and the noise spectral density increases as the carrier is approached.

The causes of phase noise in dividers are not well understood, but the effects of internal noise on the switching point of the various flip-flops cannot be ignored. The 1/*f* noise will obviously inter-relate to the phase noise if this is so, and it is interesting to note that various measurements of Gallium Arsenide dividers suggest performances 20 to 30dB worse than for ECL dividers. Rohde (ref. 4) suggests that TTL and CMOS are much better than ECL, although little work has been published in this field, possibly because of the measurement difficulties.

The non-saturating nature of ECL, the fact that the transistors are designed and processed for high speed rather than low noise, and the smaller signal swings than TTL or CMOS, lead intuitively to the conclusion that ECL should be worse than either of these other two logic families. This appears to be the case, while the high 1/*f* noise knee of Gallium Arsenide devices leads to the high relatively close in phase noise.

Devices with slow output edges, such as open collector TTL output stages may also be expected to be worse, which is again born out in practice.

Minimisation of phase noise requires the use of well-filtered supplies, correct input levels and minimisation of noise in level changing circuitry.

Fig.11 Spectrally pure signal

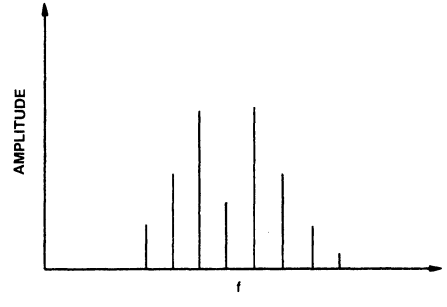


Fig.12 Spectrally pure signal, frequency modulated with single tone

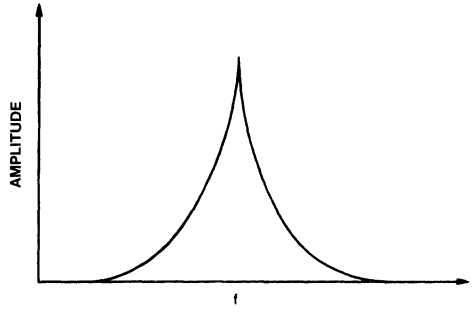


Fig.13 Spectrally pure signal, frequency modulated by noise

REFERENCES

1. Electronic Applications of the Smith Chart, Philip H. Smith, McGraw Hill, 1969.
2. Microwave Filters, Impedance - Matching Networks and Coupling Structures, Matthei, Young, Jones, Artech House 1980. SBN 0890060991.
3. Tables of Chebyshev Impedance Transforming Networks of Low Pass Filter Form, Matthei G.L., Proc IEEE August 1964 pp 939 - 963.
4. Digital PLL Frequency Synthesis Theory and Design V.L. Rohde, Prentice Hall 1983 ISBN 0-13-214239-2.

Universal Programmer for Plessey Synthesiser ICs

The programmer described in this application note will provide the data required to program any of the Plessey NJ8820 or NJ88C30 series of Synthesiser ICs. This circuit can be made from readily available CMOS logic ICs and a single 2K byte eprom (type 2516), and requires only a +5V supply.

BRIEF CIRCUIT DESCRIPTION

The program cycle is initiated by pressing the momentary switch S1. This generates a pulse which clocks the 4013 D-latch which in turn resets the 4040 counter; the same clock pulse is passed to the output buffer as a program enable signal for the NJ8820 or NJ8821/23.

The Q2 to Q7 outputs of the counter then sequentially address 64 locations in the eprom, the start address of which is determined by Hex switch S2 which is used to set bits A9 to A6 of the eprom address. The data outputs of the eprom D6-D4 are used to generate data select signals DS2-DS0 (NJ8821/23) and to provide a 3-bit address to the 4051 multiplexer which in turn selects one of the eight hex switches S3-S10.

The MSB of switch S2 selects, via the 74HC157 multiplexer, either the data bits D6-D4 from the eprom or the data select signals DS2-DS0 from input buffers (NJ8820).

Data output D3-D0 (NJ8820/21/23) from the output buffer is determined by setting the 8 hex switches S3-S10. The serial data output is derived from D3-D0, via a 74HC153 multiplexer, which is in turn controlled by data bits D3 and D2 from the eprom.

Eprom data output D1 and D0 generate the clock and enable signals respectively.

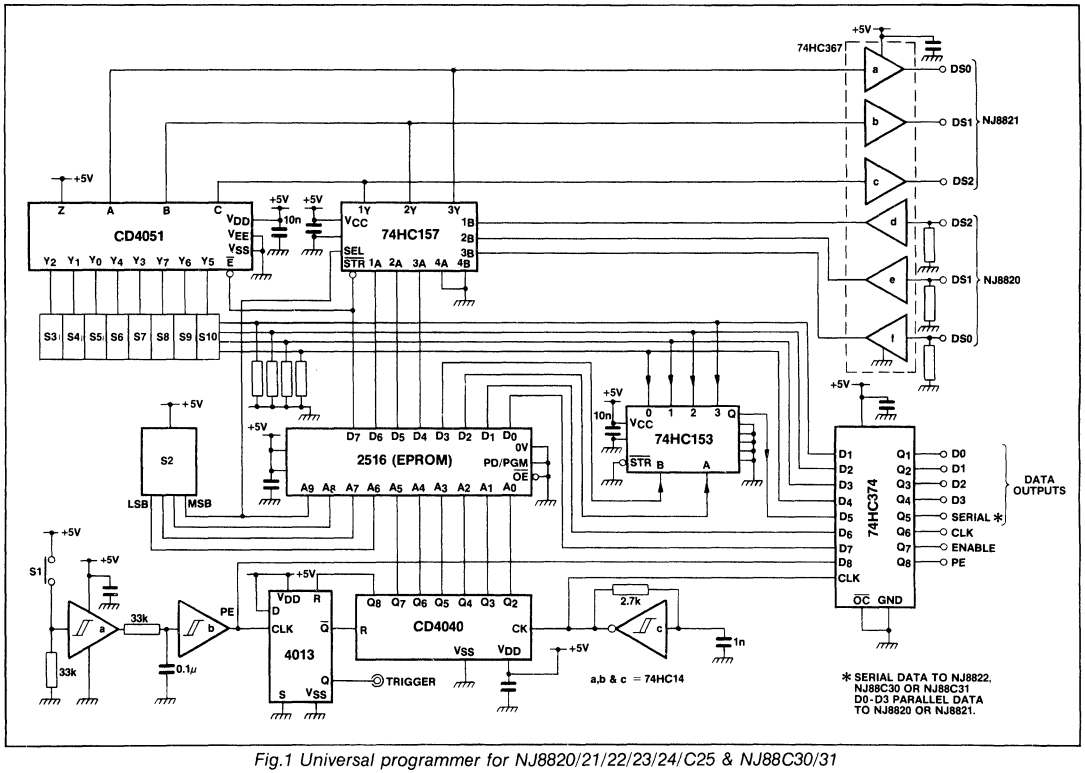


Fig.1 Universal programmer for NJ8820/21/22/23/24/C25 & NJ88C30/31

Switch	2				1				0				4			
	MSB			LSB	MSB			LSB	MSB			LSB	MSB			LSB
NJ8820/1/2/3/4	M9	M8	M7	M6	M5	M4	M3	M2	M1	M0	-	-	-	A6	A5	A4
NJ88C30/31	-	R2	R1	R0	-	-	-	-	-	-	-	-	-	-	-	-

Switch	3				7				6				5			
	MSB			LSB	MSB			LSB	MSB			LSB	MSB			LSB
NJ8820/1/2/3/4	A3	A2	A1	A0	-	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0
NJ88C30/31	F15	F14	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	F0

NOTE:
When entering the data for the NJ8820 series of devices it is necessary to multiply the M divide ratio by 4 prior to conversion to hexadecimal. It is necessary to divide the R divide ratio by 2 prior to conversion to hexadecimal to take into account the fixed divide by 2 in the reference chain.

Table 1 Switch settings for various synthesiser types

A_9	A_8	A_7	A_6	Synthesiser Type
0	0	0	0	**NJ8821/3**
0	0	0	1	**NJ8822/4 (17 Bits)**
0	0	1	0	**NJ8822/4 (28 Bits)**
0	0	1	1	**NJ88C30/31**
0	1	0	0	**NJ88C25 (19 Bits)**
0	1	0	1	**NJ88C25 (30 Bits)**
1	0	0	0	**NJ8820**

Table 2 Eprom addressing

A5 to A0 is determined by the 4040 counter outputs Q7-Q2 to give 64 timing slots per synthesiser type. Start addresses A9 to A6 are set by switch S2.

Table 4 is an example of the eprom data for the NJ8822. The start address 0040 is set by hex switch S2.

It can be seen how the data generates the clock and enable signals, the control signals for the parallel to serial conversion in the 74HC153 Mux and the selection of the switches S3-S10. In this case S6 and S7 are selected, these contain the data for the 'A' counter which is the first to be sent to the device.

A complete memory map of the eprom is given in Table 5.

D7	0	DS0-DS2 and Data outputs enabled
	1	DS0-DS2 and Data outputs disabled
D6	**D5**	**D4**	**Switch selected**
0	0	0	S5
0	0	1	S4
0	1	0	S3 LHS switch
0	1	1	S7
1	0	0	S6
1	0	1	S10 RHS switch
1	1	0	S9
1	1	1	S8
D3	**D2**	**Serial data**
0	0	MSB D3
0	1	D2
1	0	D1
1	1	LSB D0
D1		Clock O/P
D0		Enable O/P

Table 3 Eprom data

			Switch Select			Parallel to Serial		CK	EN
Address	**Data**	**O/P Enable**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
040	80	1	0	0	0	0	0	0	0
041	02	0	0	0	0	0	0	1	1
042	47	0	1	0	0	0	1	1	1
043	45	0	1	0	0	0	1	0	1
044	4B	0	1	0	0	1	0	1	1
045	49	0	1	0	0	1	0	0	1
046	4F	0	1	0	0	1	1	1	1
047	4D	0	1	0	0	1	1	0	1
048	33	0	0	1	1	0	0	1	1
049	31	0	0	1	1	0	0	0	1
04A	37	0	0	1	1	0	1	1	1
04B	35	0	0	1	1	0	1	0	1
04C	3B	0	0	1	1	1	0	1	1
04D	39	0	0	1	1	1	0	0	1
04E	3F	0	0	1	1	1	1	1	1
04F	3D	0	0	1	1	1	1	0	1

Table 4 Example of eprom data organization

		Eprom Start Addr (Hex)	Switch No.
NJ8821/3	80 00 01 01 00 10 11 11 10 20 21 21 20 30 31 31 30 40 41 41 40 50 51 51 50 60 61 61 60 70 71 71 70 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80	00	0
NJ8822/4 17 Bit	80 02 47 45 4B 49 4F 4D 33 31 37 35 3B 39 3F 3D 23 21 27 25 2B 29 2F 2D 13 11 17 15 1B 19 1F 1D 03 01 07 01 07 02 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80	40	1
NJ8822/4 28 Bit	80 02 47 45 4B 49 4F 4D 33 31 37 35 3B 39 3F 3D 23 21 27 25 2B 29 2F 2D 13 11 17 15 1B 19 1F 1D 03 01 07 05 77 75 7B 79 7F 7D 63 61 67 65 6B 69 6F 6D 53 51 57 55 5B 59 5F 5D 5F 5E 80 80 80 80	80	2
NJ88C30/31	80 26 24 2A 28 2E 2C 32 30 36 34 3A 38 3E 3C 72 70 76 74 7A 78 7E 7C 62 60 66 64 6A 68 6E 6C 52 50 56 54 5A 58 5E 5C 5D 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80	C0	3
NJ88C25 19 Bit	80 02 47 45 4B 49 4F 4D 33 31 37 35 3B 39 3F 3D 23 21 27 25 2B 29 2F 2D 13 11 17 15 1B 19 1F 1D 03 01 07 05 0B 09 0F 0D 8F 8D 8F 8E 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80	100	4
NJ88C25 30 Bits	80 02 47 45 4B 49 4F 4D 33 31 37 35 3B 39 3F 3D 23 21 27 25 2B 29 2F 2D 13 11 17 15 1B 19 1F 1D 03 01 07 05 0B 09 0F 0D 77 75 7B 79 7F 7D 63 61 67 65 6B 69 6F 6D 53 51 57 55 5B 59 5F 5D 5F 5E	140	5
	80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80		6
	80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80 80		7
NJ8820	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	200	8

Table 5 Eprom memory map

Using the SP8835 in 3.5GHz Synthesisers

Until recently, prescalers have only been available (at reasonable consumer prices) for frequencies up to about 1GHz. Now, with the rapid improvement of silicon technology, Plessey Semiconductors has developed a range of dividers for frequencies for up to 3.5GHz.

The following application note explains how one of these devices can easily be used with two standard integrated synthesisers. The first example is of a 3.5GHz synthesiser using the SP8835 ÷ 4 (3.5GHz) together with the SP5000 (1GHz synthesiser chip). The second example is again a 3.5GHz synthesiser, but using the SP8835 ÷ 4 with an SP8704 ÷ 128/9 (dual modulus divider 1GHz) and the NJ8820. This second example can be programmed to give a smaller frequency step size than the first example, but requires more components.

High speed dividers are primarily used in frequency synthesisers, either phase locked loops or frequency locked loops. Synthesisers incorporate a voltage controlled oscillator which is controlled via a feedback network so that it oscillates at a predetermined frequency. In most cases, this synthesised frequency can be altered (by external programming) to tune the oscillator over a range of frequencies (band). The prescaler is used in such a system to reduce the oscillator's frequency to one that can be compared with a standard known reference frequency (usually obtained from a crystal oscillator and divider). This frequency comparison can be made in several ways, for example a phase comparison using a phase detector (PLL) or a frequency comparison using a frequency counter (μPC) in a frequency locked loop.

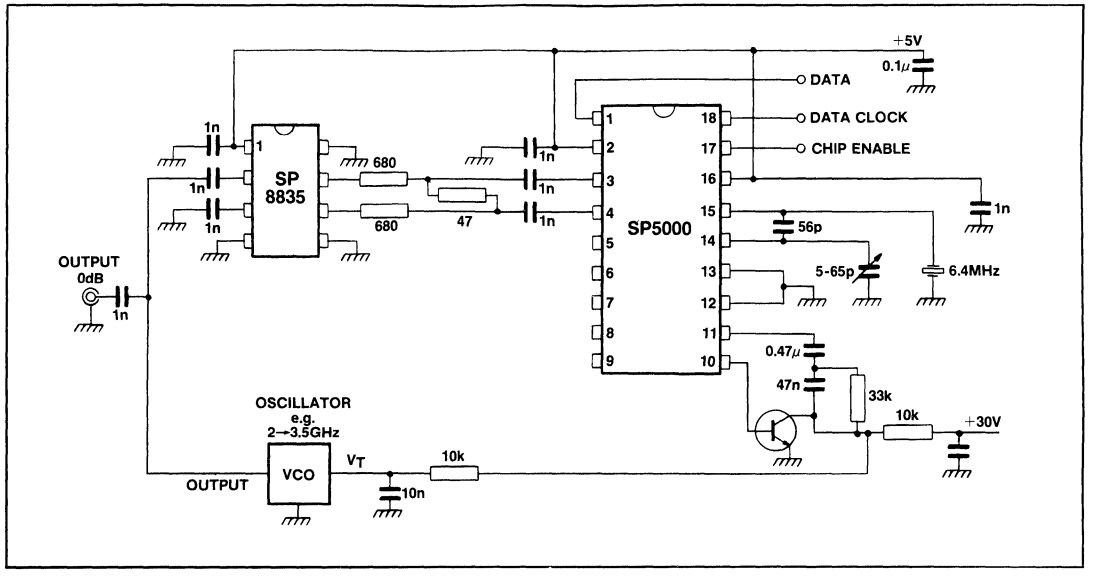


Fig.1 SP8835 and SP5000 - 3.5GHz synthesiser

3.5GHz SYNTHESISER USING SP8835 AND SP5000

The SP8835 (÷4) interfaces very easily with the SP5000 (see Fig.1). The only interface circuit used is an attenuator so that the output from the SP8835 does not overload the input of the SP5000 (the SP5000 has very good sensitivity for TV applications). The rest of this application circuit is identical to the standard application circuits of the two devices as shown in their relevant data sheets. With a 4MHz crystal used in the reference oscillator, a synthesiser can be programmed to synthesise frequencies up to 3.5GHz with a minimum frequency step size of 500kHz. The range of frequencies over which the synthesiser will synthesise is determined by the voltage controlled oscillator used.

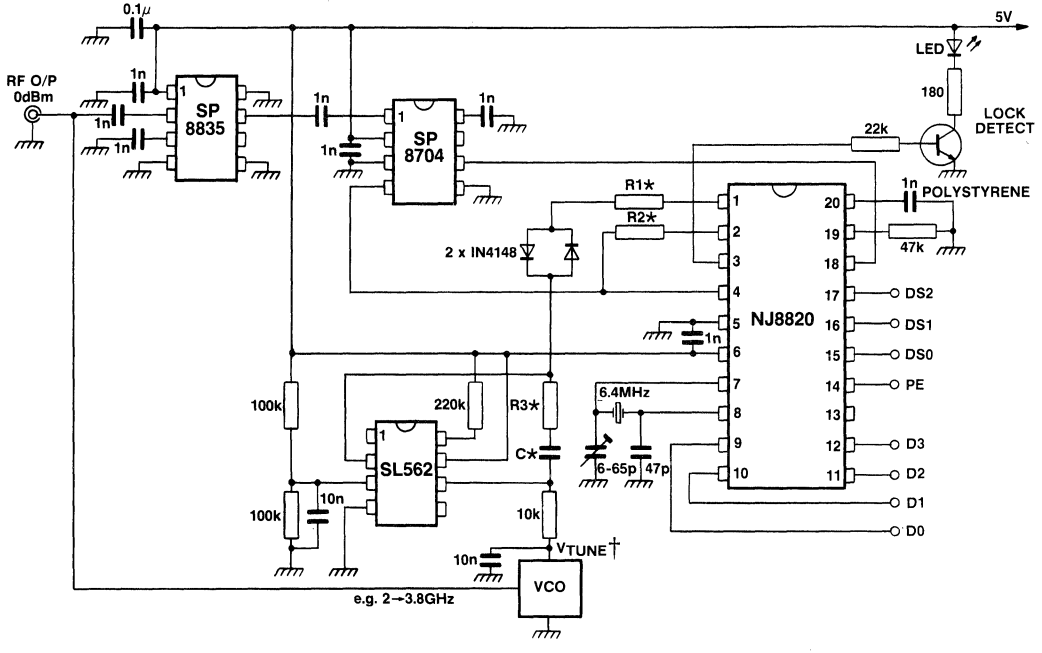
When laying out the PCB for this application, a board with an earth plane should be used, all decoupling capacitors should be placed as near as possible to the devices and all high frequency links should be 50Ω track.

3.5GHz SYNTHESISER USING SP8835, SP8704, NJ8820 AND SL562

If the SP8835 is used in conjunction with an SP8704 (÷128/129) and an NJ8820 with loop filter amplifier (SL562), a synthesiser with a minimum frequency step size of 100kHz can be constructed (using a 6.4MHz crystal, see Fig.2). The devices interface to each other very easily as shown in the circuit diagram. No attenuation or amplfication is needed to match input and output levels. The only section of the synthesiser that needs careful design is the loop filter which is dependent on the type of oscillator used and the phase noise requirements. With a small frequency step size of 100kHz, which is a very small percentage of the synthesised frequency, a low loop bandwidth is required for adequate sideband suppression. A 200Hz loop filter gives adequate sideband suppression for a 3.5GHz synthesiser for use in a satellite TV reception system (C band direct conversion). The loop filter component calculations are explained in the 'Radio Synthesiser Circuits' applcation booklet.

PCB layout techniques are the same as the previous example.

These are just a few examples of applications for high speed dividers. They can very easily be used in conjunction with a larger modulus, lower frequency divider to produce a frequency low enough for a microprocessor to be able to count and can therefore be used in a frequency locked loop. This is useful if a microprocessor is already used in the system.



NOTES

† V_{TUNE} approximately 0 to 5V. If a greater voltage range is required, the supply to the SL562 may be increased to a maximum of 20V. Pin 3 of the SL562 should be maintained at 2.5V.

* Values for the loop filter components R1, R2, R3 and C can be calculated as described in the Loop Filter Design application note.

Fig.2 3.5GHz synthesiser using SP8835, SP8703, NJ8820 and SL562

Thermal Design

The temperature of any semiconductor device has an important effect upon its long term reliability. For this reason, it is important to minimise the chip temperature; and in any case, the maximum junction temperature should not be exceeded.

Electrical power dissipated in any device is a source of heat. How quickly this heat can be dissipated is directly related to the rise in chip temperature: if the heat can only escape slowly, then the chip temperature will rise further than if the heat can escape quickly. To use an electrical analogy: energy from a constant voltage source can be drawn much faster by using a low resistance load than by using a high resistance load.

The thermal resistance to the flow of heat from the semiconductor junction to the ambient temperature air surrounding the package is made up of several elements. These are the thermal resistance of the junction-to-case, case-to-heatsink and heatsink-to-ambient interfaces. Of course, where no heatsink is used, the case-to-ambient thermal resistance is used.

These thermal resistances may be represented as

$\theta_{JA} = \theta_{JC} + \theta_{CH} + \theta_{HA}$

where θ_{JA} is thermal resistance junction-to-ambient °C/W
θ_{JC} is thermal resistance junction-to-case °C/W
θ_{CH} is thermal resistance case-to-heatsink °C/W
θ_{HA} is thermal resistance heatsink-to-ambient °C/W

The temperature of the junction is also dependent upon the amount of power dissipated in the device — so the greater the power, the greater the temperature.

Just as Ohm's Law is applied in an electrical circuit, a similar relationship is applicable to heatsinks.

$T_j = T_{amb} + P_D (\theta_{JA})$,

where T_j = junction temperature
T_{amb} = ambient temperature
P_D = dissipated power

From this equation, junction temperature may be calculated, as in the following examples.

Example 1

An SP8785B is to be used at an ambient temperature of +50 °C. θ_{JA} for the DG16 package with a chip of approximately 1mm sq is 110 °C/W; from the datasheet, P_D max = 598mW and T_j max = 175 °C.

$T_j = T_{amb} + P_D \theta_{JA}$
$= 50 + (0.598 \times 110)$
$= +11.8$ °C

Where operation in a higher ambient temperature is necessary, the maximum junction temperature can easily be exceeded unless suitable measures are taken:

Example 2

An SP8785A is to be used at an ambient temperature of +120 °C. Again, θ_{JA} = 110 °C/W, P_D max = 598mW.

$$T_j = 120 + (0.598 \times 110)$$
$$= +185.8\,°C$$

This clearly exceeds the maximum permissible junction temperature and therefore some means of decreasing the junction-to-ambient thermal resistance is required.

As stated earlier, θ_{JA} is the sum of the individual thermal resistances; of these, θ_{JC} is fixed by the design of device and package and so only the case-to-ambient thermal resistance, θ_{CA}, can be reduced.

If θ_{CA}, and therefore θ_{JA}, is reduced by the use of a suitable heatsink, then the maximum T_{amb} can be increased:

Example 3

Assume that an IERC LIC14A2U dissipator and DC000080B retainer are used. This device is rated as providing a θ_{JA} of 55 °C/W for the DG16 package. Using this heatsink with the SP8785A operated as in Example 2 would result in a junction temperature given by:

$$T_j = 120 + (0.598 \times 55)$$
$$= +153\,°C$$

Nevertheless, it should be noted that these calculations are not necessarily exact. This is because factors such as θ_{JC} may vary from device type to device type, and the efficacy of the heatsink may vary according to the air movement in the equipment.

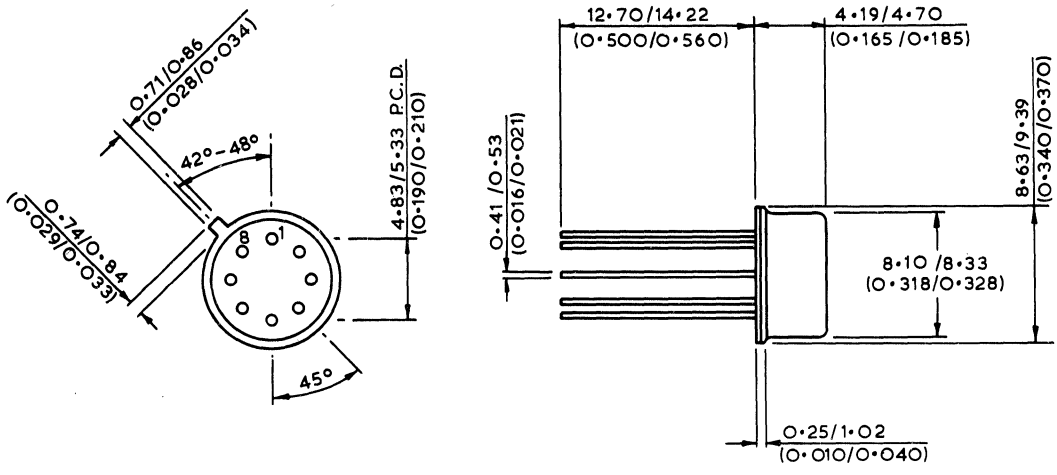
In addition, the assumption has been made that chip temperature and junction temperature are the same thing. This is not strictly so, as not only can hot spots occur on the chip, but the thermal conductivity of silicon is a variable with temperature, and thus the θ_{JC} is in fact a function of chip temperature. Nevertheless, the method outlined above is a practical method which will give adequate answers for the design of equipment.

It is possible to improve the dissipating capability of the package by the use of heat dissipating bars under the package, and various proprietary items exist for this purpose.

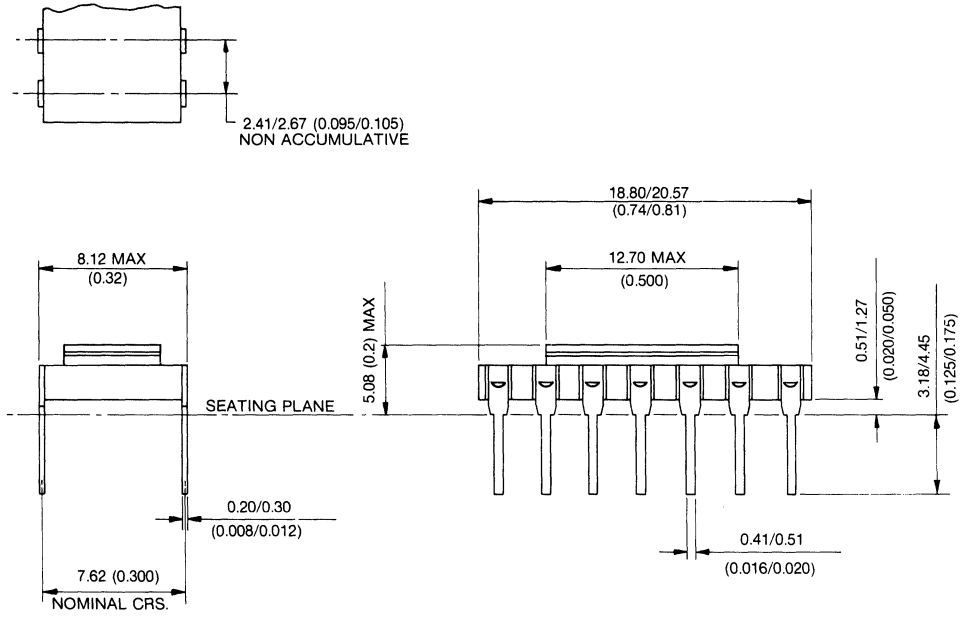
Under certain circumstances, forced air cooling can become necessary, and although the simple approach outlined above is useful, more factors must be taken into account.

Package Outlines

Ordering Information



8-LEAD METAL CAN - CM8



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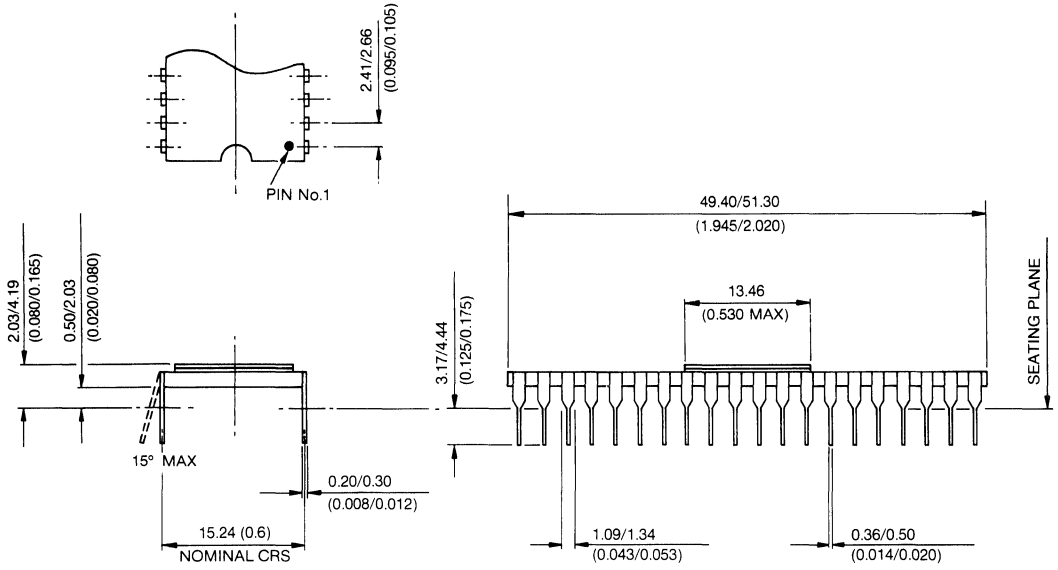

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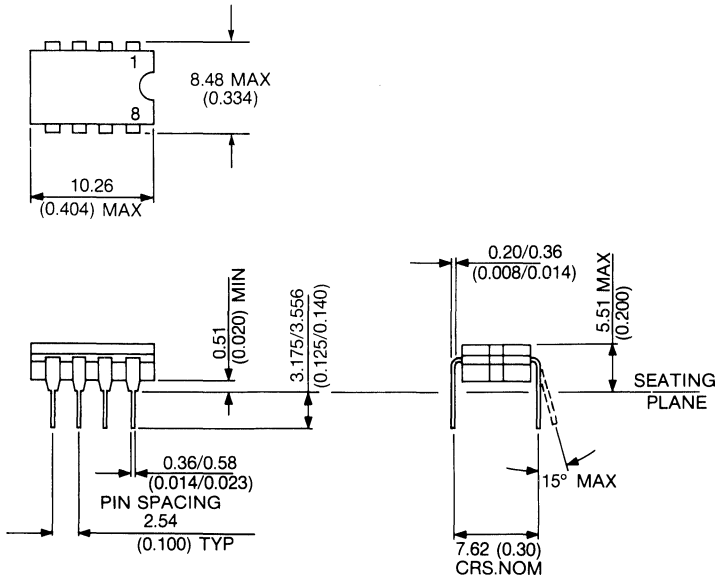

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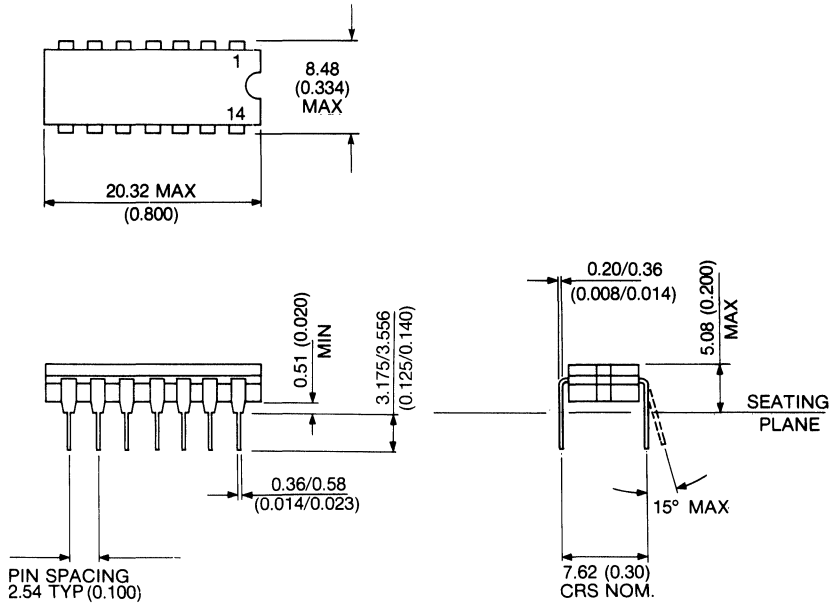

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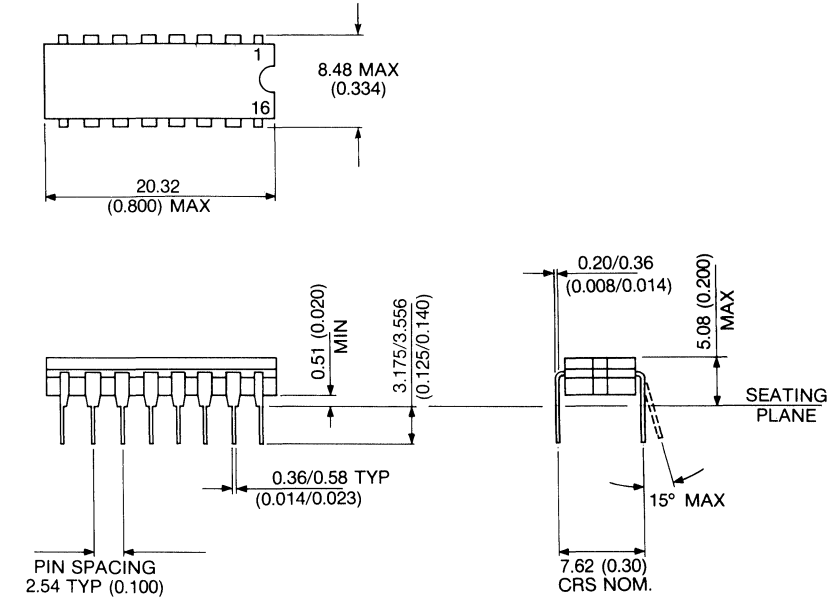

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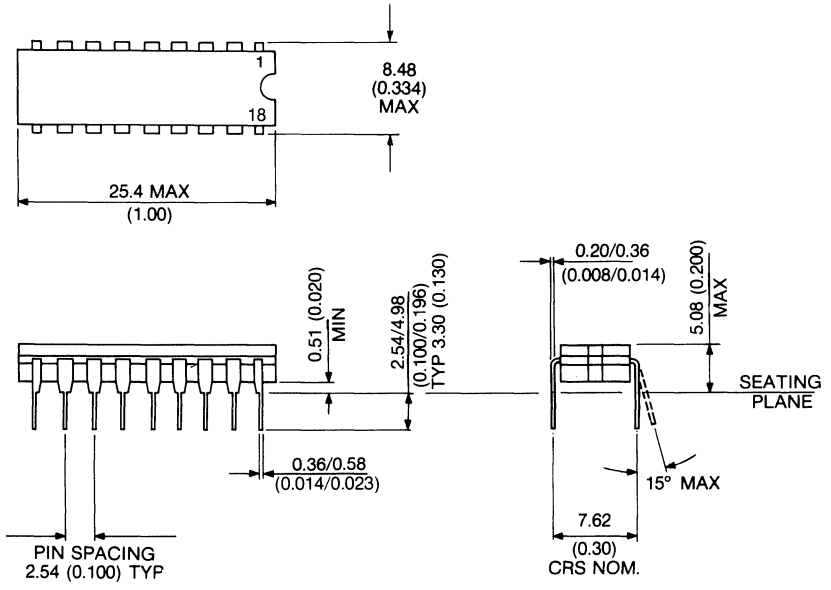

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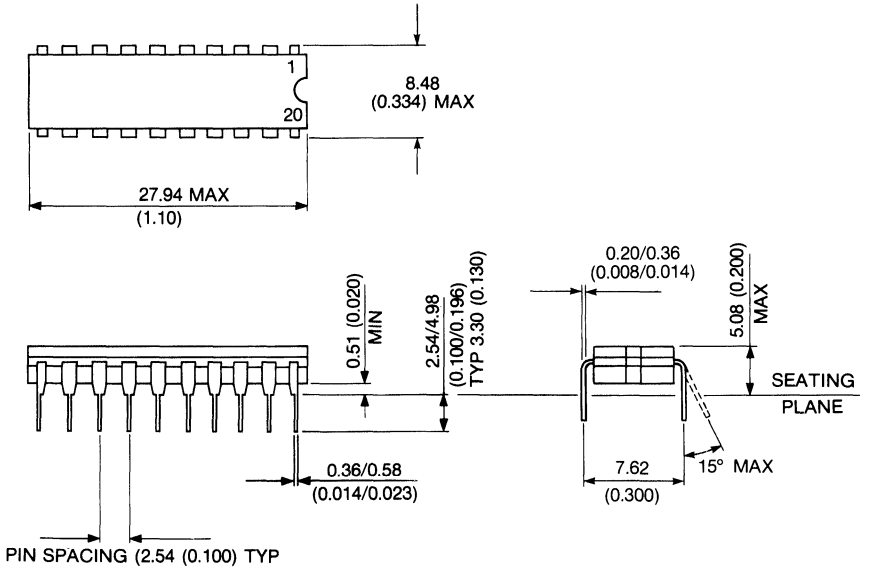

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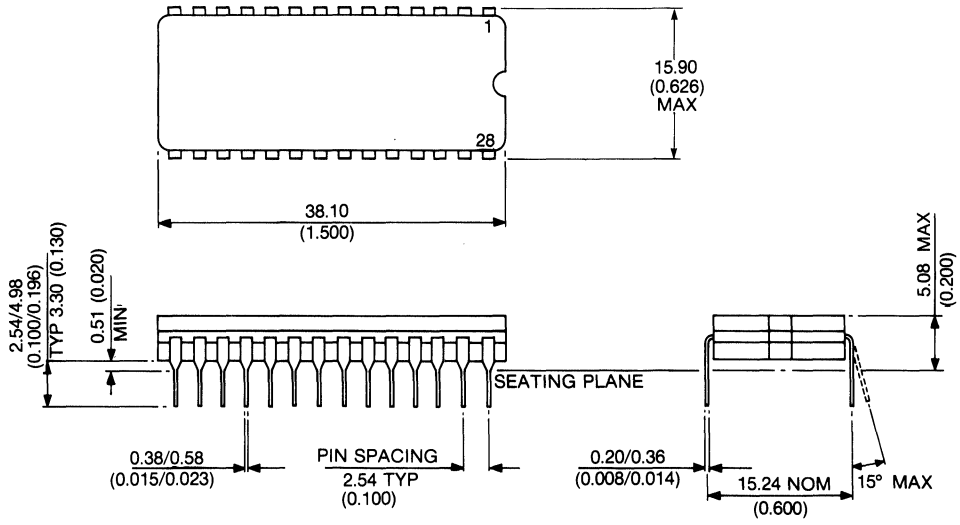

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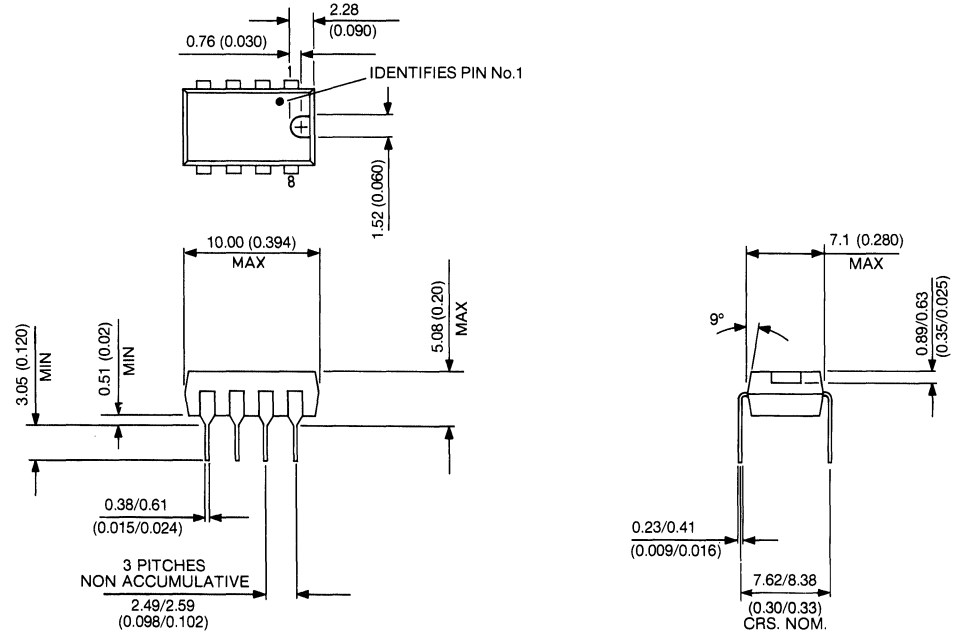

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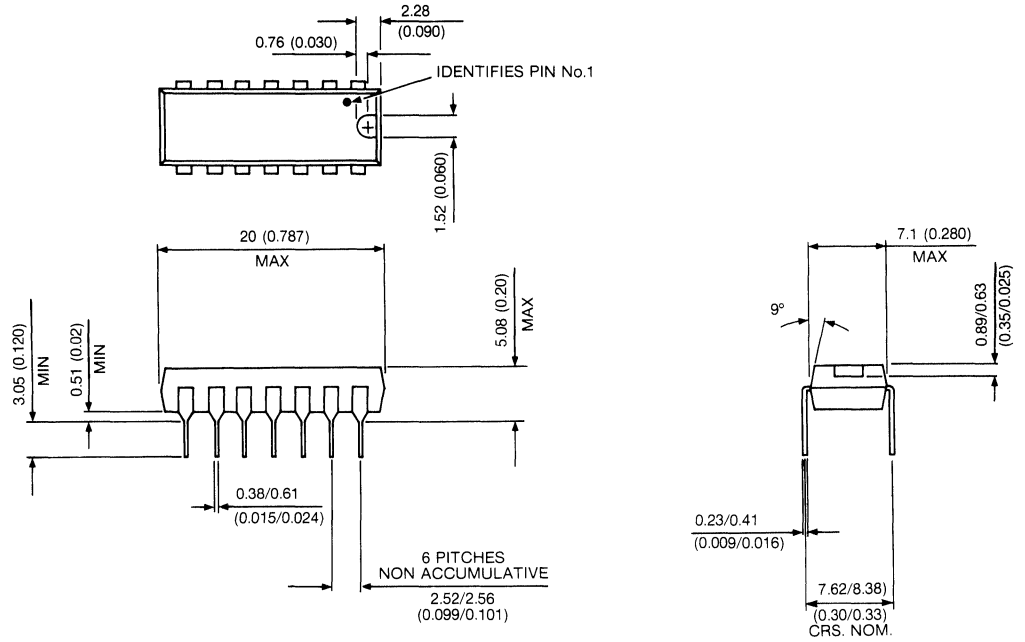

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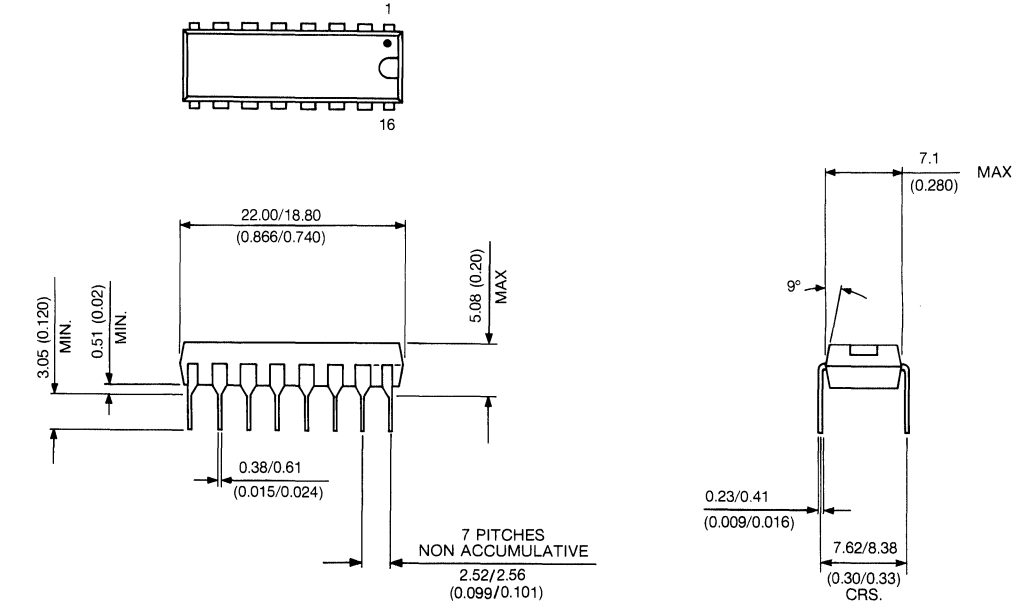

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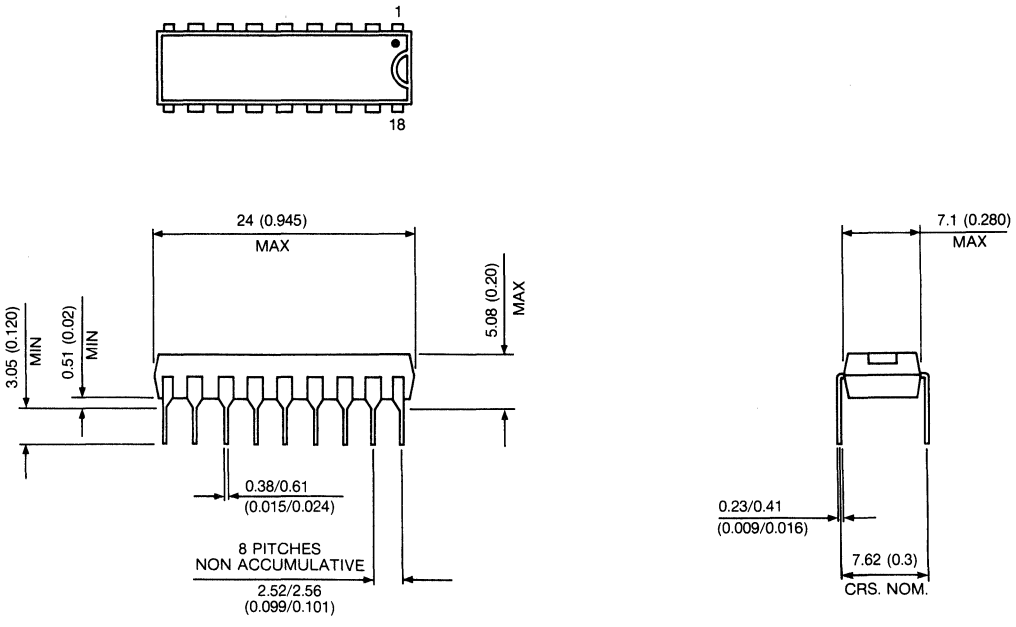

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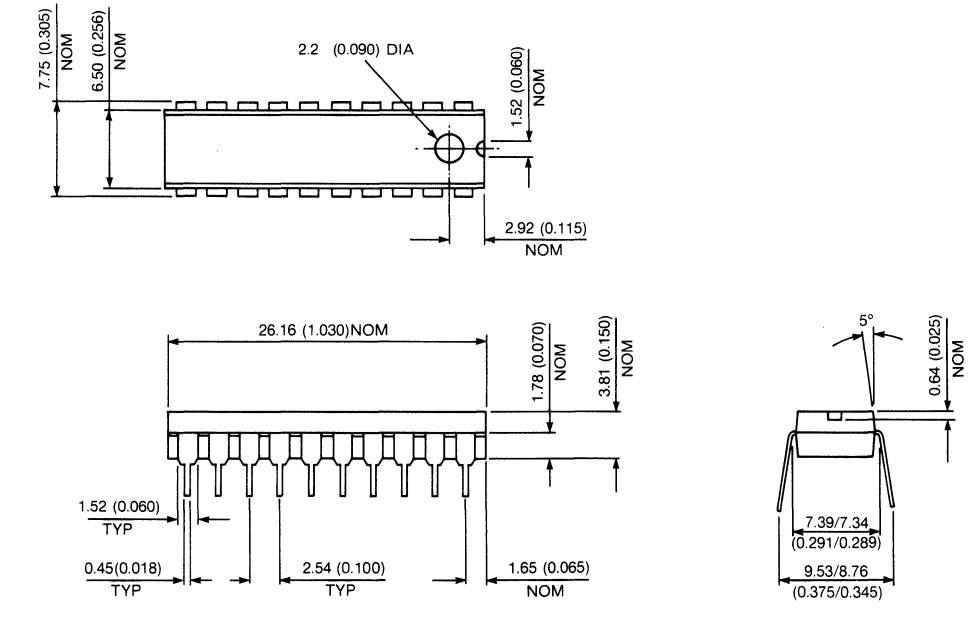

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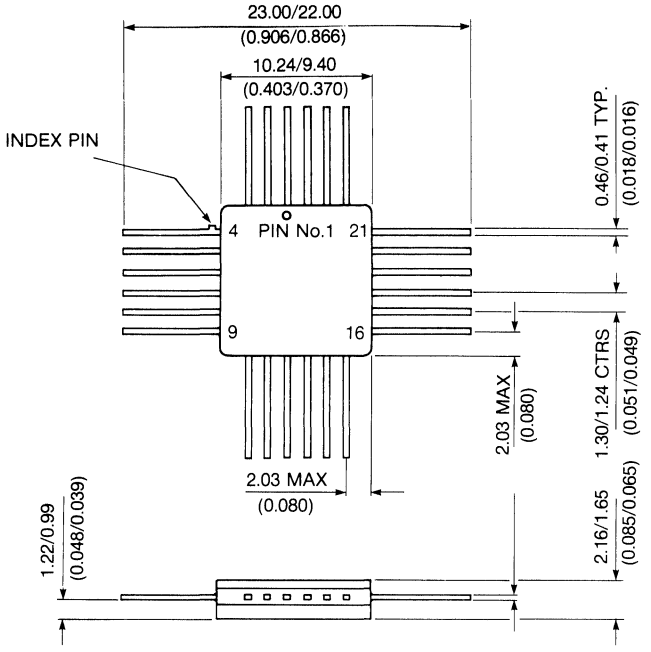
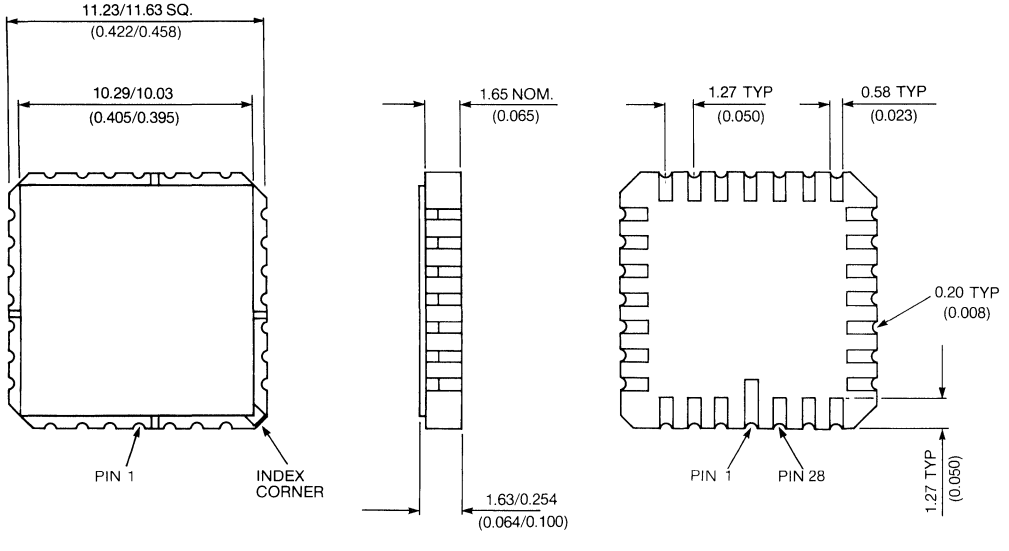
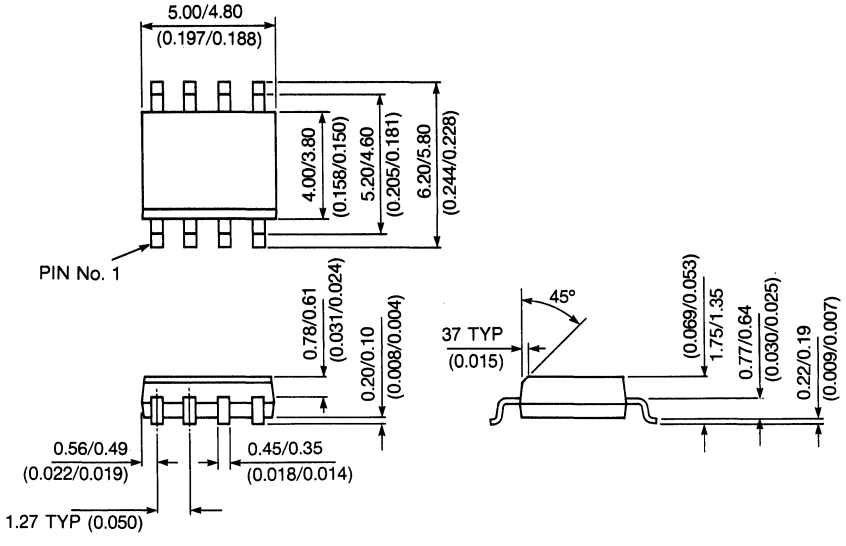


24 LEAD FLATPACK - GG24



28-PIN LEADLESS CHIP CARRIER - LC28
(HERMETIC)



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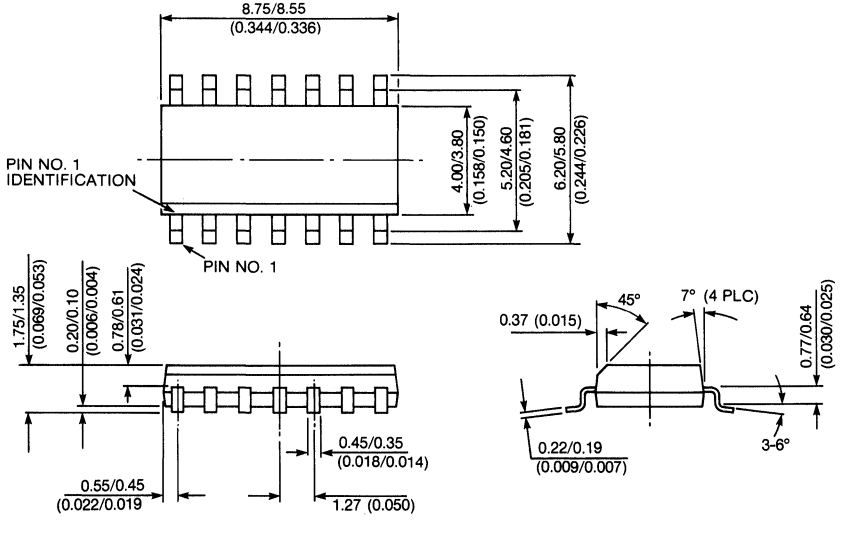

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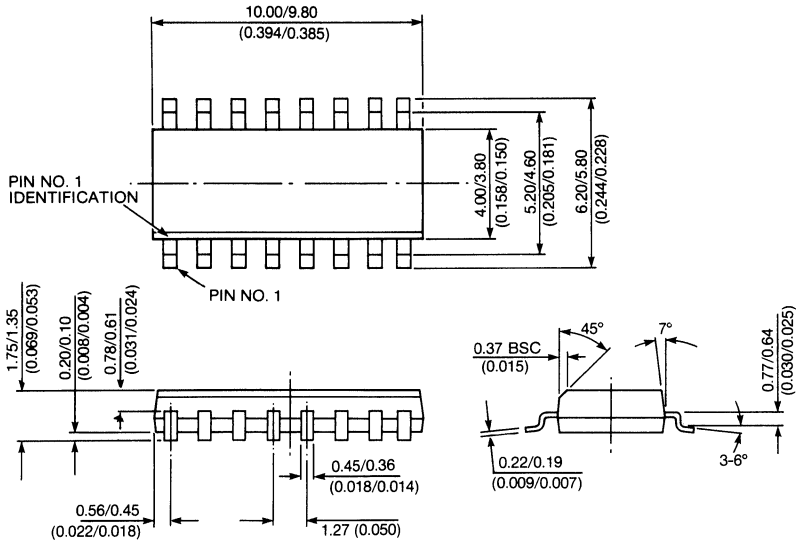

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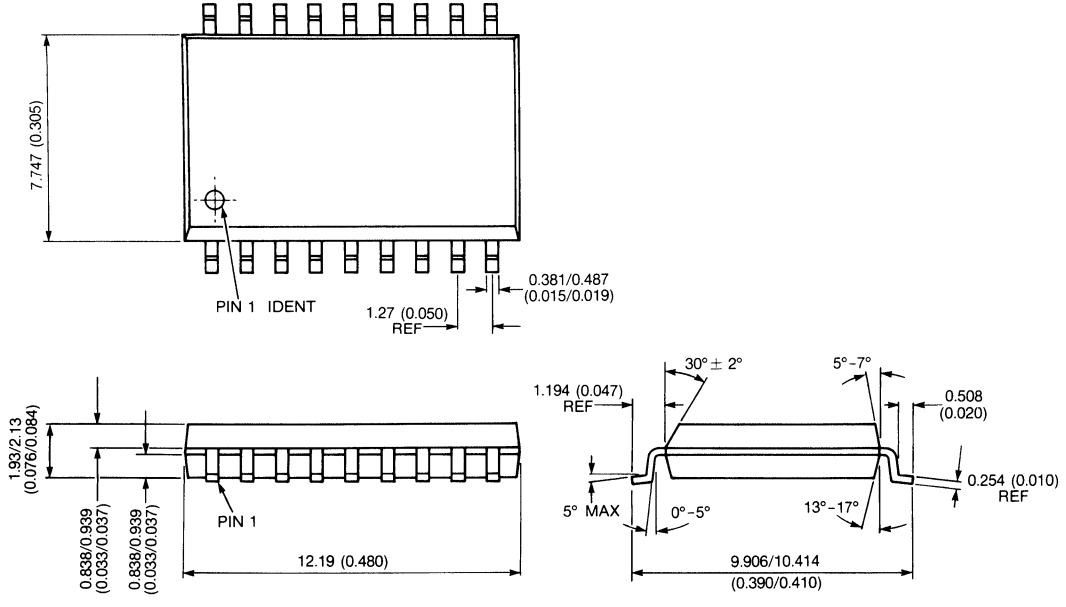

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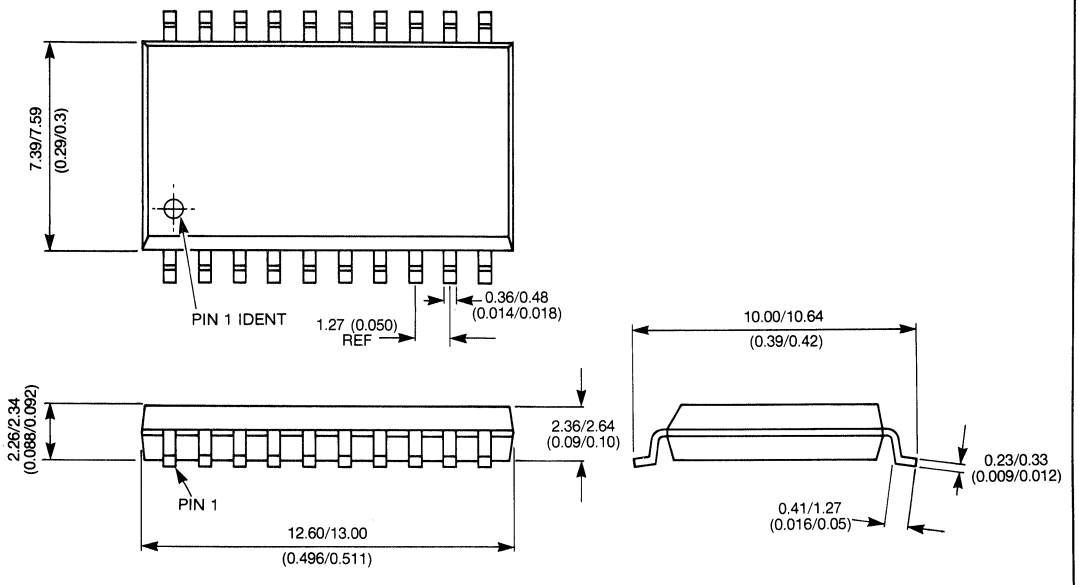

20-LEAD MINIATURE PLASTIC DIL - MP20

Ordering Information

The coding block for an SP8000 device with an explanation of the meaning of each segment is explained here.

SP 8XXX Y Z PT

Y - Identifies the maximum operating temperature.

A = -55°C to +125°C
B = -40°C to +85°C
-30°C to +70°C
0°C to +70°C
} Refer to data sheet

NOTE: Some devices do not have a suffix letter in this position; please consult relevant data sheet for temperature range.

Z - Identifies the screening level required.

B = is for product screened to Plessey HI-REL B condition.
C = is for product screened to MIL-STD-883C Class B condition.
S = is for product screened to MIL-STD-883C Class S condition.
BSS2 = is for product screened to BS9400 Level S2 condition.

PT - Identifies the package types:

DG - Dual-in-Line in a Glass Ceramic package.
DP - Dual-in-Line in Plastic package.
DC - Dual-in-Line in a Metal Ceramic package.
MP - Miniature Plastic package.
LC - Leadless Chip Carriers in a Metal Ceramic 3 Layer package.
GG - Glass Sealed Ceramic Leaded Chip Carrier.

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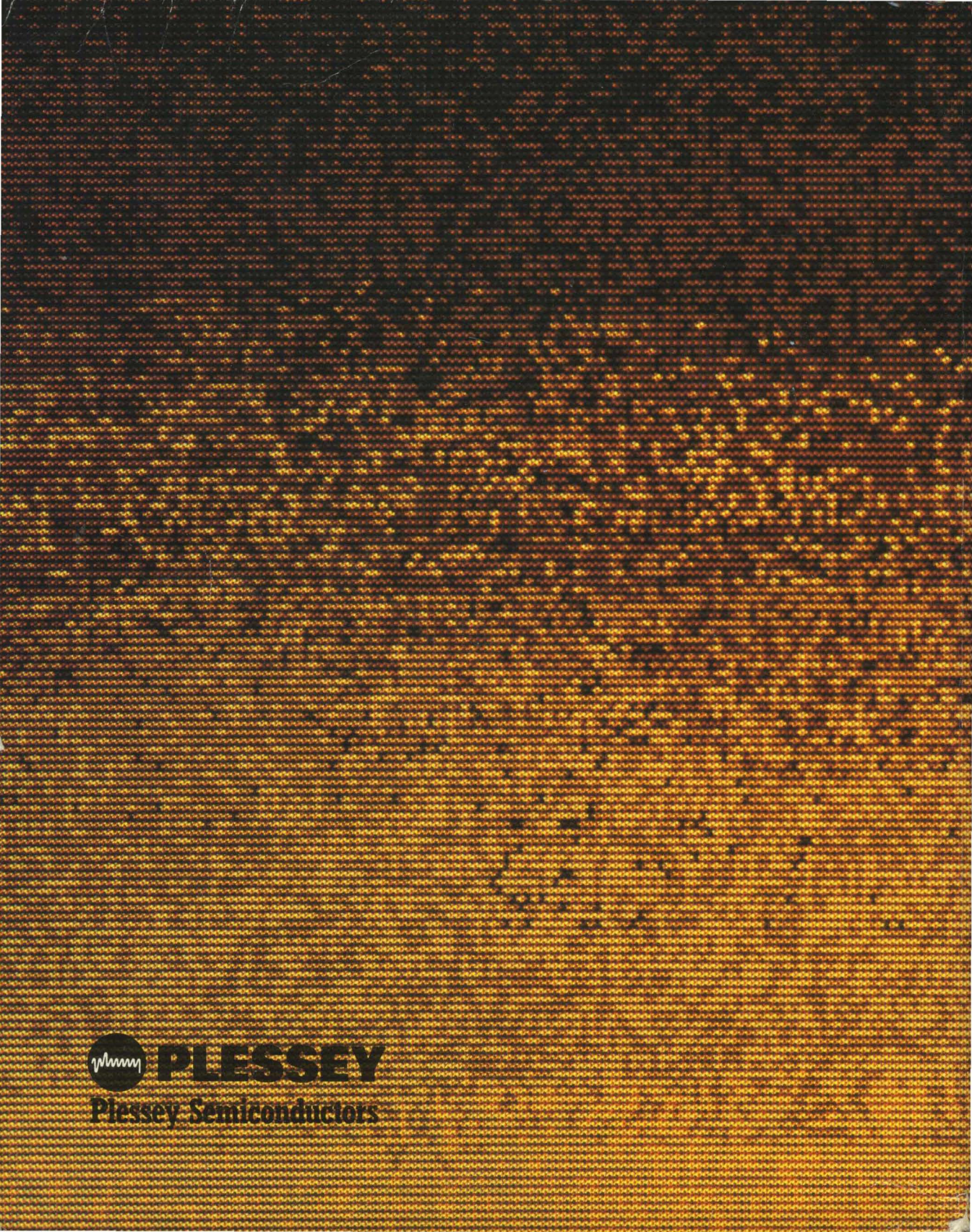
Publication No. P.S.1937 February 1988

Supersedes the *SP8000 Series High Speed Dividers Integrated Circuit Handbook,* August 1985

PWC 1984/2007 2/88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