## Components and materials

Book C1 1985

## PLC modules

PC20 modules

## PROGRAMMABLE CONTROLLER MODULES

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ELECTRON TUBES BLUE

SEMICONDUCTORS
RED

INTEGRATED CIRCUITS
PURPLE

COMPONENTS AND MATERIALS
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The data handbooks contain all pertinent data available at the time of publication, and each is revised and reissued periodically.
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Instrument tubes, monitor and display tubes, C.R. tubes for special applications

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Photo and electron multipliers
Photomultiplier tubes, phototubes, single channel electron multipliers, channel electron multiplier plates

T10 Camera tubes and accessories
T11 Microwave semiconductors and components
T12 Vidicons and Newvicons
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S4a Low-frequency power transistors and hybrid modules
S4b High-voltage and switching power transistors
S5 Field-effect transistors
S6 R.F. power transistors and modules
S7 Surface mounted semiconductors
S8 Devices for optoelectronics
Photosensitive diodes and transistors, light-emitting diodes, displays, photocouplers, infrared sensitive devices, photoconductive devices.

S9 Power MOS transistors
S10 Wideband transistors and wideband hybrid IC modules
S11 Microwave semiconductors (to be published in this series in 1985)
All present available.in Handbook T11
S12 Surface acoustic wave devices

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## EXISTING SERIES

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IC2 Bipolar ICs for video equipment
IC3 ICs for digital systems in radio, audio and video equipment
IC4 Digital integrated circuits
CMOS HE4000B family

IC5 Digital integrated circuits - ECL
ECL10000 (GX family), ECL100000 (HX family), dedicated designs

IC6 Professional analogue integrated circuits
IC7 Signetics bipolar memories
IC8 Signetics analogue circuits
IC9 Signetics TTL logic
IC10 Signetics Integrated Fuse Logic (IFL)
IC11 Microprocessors, microcomputers and peripheral circuitry

## NEW SERIES

IC01N Radio, audio and associated systems
Bipolar, MOS
IC02N Video and associated systems
Bipolar, MOS
IC03N Telephony equipment
Bipolar, MOS
IC04N HE4000B logic family CMOS

IC05N HE4000B logic family uncased integrated circuits
(published 1984)

IC06N PC54/74HC/HCU/HCT logic families HCMOS

IC07N PC54/74HC/HCU/HCT uncased integrated circuits HCMOS

IC08N 10K and 100K logic family
(published 1984)
ECL
IC09N Logic series (published 1984)

IC10N Memories
MOS, TTL, ECL
IC11N Analogue - industrial
IC12N Semi-custom gate arrays \& cell libraries
ISL, ECL, CMOS

IC13N Semi-custom integrated fuse logic IFL series 20/24/28

IC14N Microprocessors, microcontrollers \& peripherals Bipolar, MOS

IC15N Logic series FAST TTL
(published 1984)
Note
Books available in the new series are shown with their date of publication.

## COMPONENTS AND MATERIALS (GREEN SERIES)

The green series of data handbooks comprises:
C1 Programmable controller modules PLC modules, PC20 modules
C2 Television tuners, video modulators, surface acoustic wave filters
C3 Loudspeakers
C4 Ferroxcube potcores, square cores and cross cores
C5 Ferroxcube for power, audio/video and accelerators
C6 Synchronous motors and gearboxes
C7 Variable capacitors
C8 Variable mains transformers
C9 Piezoelectric quartz devices
Quartz crystal units, temperature compensated crystal oscillators, compact integrated oscillators, quartz crystal cuts for temperature measurements

## C10 Connectors

C11 Non-linear resistors
Voltage dependent resistors (VDR), light dependent resistors (LDR), negative temperature coefficient thermistors (NTC), positive temperature coefficient thermistors (PTC)

C12 Variable resistors and test switches
C13 Fixed resistors
C14 Electrolytic and solid capacitors
C15 Ceramic capacitors*
C16 Permanent magnet materials
C17 Stepping motors and associated electronics
C18 D.C. motors
C19 Piezoelectric ceramics
C20 Wire-wound components for TVs and monitors
C21 Assemblies for industrial use
HNIL FZ/30 series, NORbits 60-, 61-, 90 -series, input devices

* Film capacitors are included in Data Handbook C22 which will be published in 1985. The September 1982 edition of C15 should be retained until C22 is issued.

PLC MODULES

## MODULES FOR PROGRAMMABLE LOGIC CONTROLLERS

## INTRODUCTION

The programmable logic controller (PLC) is used for the controlling of machines or processes. It can be easily programmed and re-programmed as required.
The modular design of the PLC enables a user to build a PLC which is 'tailor-made' for his control task. By specifying the number and the types of PLC modules that he requires, he avoids purchasing more of the expensive electronic capability than he needs.
The PLC modules are formed on standard double Eurocards. Optically coupled interface circuits, specifically designed for an industrial environment, provide excellent noise immunity and a high degree of isolation. The internationally accepted machine signal level of 24 V is used and generous tolerances on operational margins and thresholds ease compatibility headaches.
Besides the PLC modules, the PLC comprises back panels, a frame (19 in rack) and a standard power supply. The frame must conform to IEC297 or DIN41494 (for racks) and IEC130-14 or DIN41612 (for connectors). The adoption of these standards means that the frame and the power supply should be easily obtainable.

The following PLC modules are available.

| type | description | catalogue no. | page |
| :---: | :---: | :---: | :---: |
| CP10 | central processor, 32 registers | 432202790420 | 7 |
| CP11 | central processor, without registers | 432202790390 | 7 |
| IM10 | input module, 16 inputs, 24 V d.c. | 432202790434 | 17 |
| IM11 | input module, 16 inputs, 24 V a.c. | 432202790403 | 17 |
| LX10 | load external interface module | 432202791600 | 23 |
| MM10 | program memory module, 1 k , non-volatile core RAM | 432202791400 | 31 |
| MM11 | program memory module, non-volatile, UV-erasable PROMs. 1 k 13 or 2 k 13 capacity; for program copying or read-out | 432202791630 | 37 |
| MM12 | program memory module, non-volatile. UV-erasable PROMs, 1 k 13 or 2 k 13 capacity; for read-out only | 432202791640 | 45 |
| OM10 | output module, 16 outputs, max. $0,1 \mathrm{~A}$ each, 24 V d.c. | 432202790440 | 51 |
| OM12 | output module, 8 outputs max. 2 A each, 24 V d.c. | 936001150112 | 57 |
| Pl10* | punch and teletype interface module | 822241241572 | 63 |
| PU10 | programming unit | 432202790410 | 71 |
| BP11 to BP16 | back panels | 9390269.0112 | 79 |

[^0]The diagram shows, in a simplified form, the function of each of the PLC modules. In operation the PLC cycles continuously through a data input/output cycle and a data processing cycle.


The input module converts the signals from the plant into a binary form acceptable to the central processor.

The central processor reads the data from the input module, performs logic equations on it in accordance with the program instructions and transfers the results to the output module.

The output module converts the binary data from the central processor to electrical signals suitable for the control of the plant.

The program memory is the store in which the set of instructions that comprise the program are stored. These instructions dictate the actions which must be taken in response to the condition of each input.

The programming unit is the means by which an operator can write a program, or changes to a program, into the program memory. The unit is portable and thus one may be used to serve any number of PLCs. It is also sufficiently inexpensive to make the permanent location of one in each PLC for monitoring or test purposes, a realistic and useful proposition.

## GENERAL CHARACTERISTICS

Operating temperature range
Storage temperature range
Dimensions

Supply voltage (d.c.)
Maximum number of input + output signals
Maximum program length
Cycle time

0 to $+60{ }^{\circ} \mathrm{C}$
-40 to $+70^{\circ} \mathrm{C}$
$160 \mathrm{~mm} \times 233 \mathrm{~mm}$ (double Eurocard) according to IEC297 or DIN41494
$\mathrm{V}_{\mathrm{P}}=5 \mathrm{~V} \pm 5 \% ; \frac{\mathrm{dV} \mathrm{P}}{\mathrm{dt}} \leq 5 \mathrm{~V} / \mathrm{ms}$ 512
$4 \times 1024$ words
$0,029\left(n_{\mathrm{IM}}+\mathrm{nOM}_{\mathrm{O}}\right)+1,85 \mathrm{n}_{\mathrm{MM}} \mathrm{ms}$
$\mathrm{n}_{\mathrm{IM}}=$ number of input modules
$\mathrm{n}_{\mathrm{OM}}=$ number of output modules
$\mathrm{n}_{\mathrm{MM}}=$ number of memory modules

## TESTS AND REQUIREMENTS

All modules are designed to meet the tests below.
Vibration test
IEC68-2, test method Fc: 5 to 55 Hz , amplitude $1,5 \mathrm{~mm}$ or 5 g (whichever is less).

## Shock test

IEC68-2, test method Ea: 3 shocks in 6 directions, pulse duration 11 ms , peak acceleration 50 g .

Rapid change of temperature test
IEC68-2, test method Na: 5 cycles of 2 h at $-40^{\circ} \mathrm{C}$ and 2 h at $+70^{\circ} \mathrm{C}$.
Damp heat test
IEC68-2, test method $\mathrm{Ca}: 21$ days at $40^{\circ} \mathrm{C}$, R.H. 90 to $95 \%$.

## CENTRAL PROCESSORS

## DESCRIPTION

These central processors are modules intended for use in combination with the input module IM10 (or IM11), memory module MM10 (or MM11 or MM12), output module OM10 (or OM12) and programming unit PU10 to assemble a programmable logic controller (PLC). The central processor is the heart of the logic controller; it asks the input modules for data and the program memory for instructions, processes the data according to these instructions, and applies the result to the output modules. It also generates the internal timing of the controller.
The processor actions take place in two distinct cycles: an input/output cycle and a data processing cycle.
During the input/output cycle the processor addresses each input stage in turn (counter/ buffer register) and transfers the present data to the corresponding scratch-pad memory location, see Fig. 1. In the same cycle the processed data of the previous data processing cycle are clocked out from the scratch-pad memory into the latch flip-flops of the output modules. As the scratch-pad memory can hold up 512 bits of data the central processor can handle a maximum combination of 512 inputs, outputs, and intermediate results. Provision is made to prevent loss of information of the scratch-pad memory in the case of power failure.
During the data processing cycle the processor applies an address and a cycle initiate signal to the program memory, which in turn then apply a program word to the processor. The program word contains an instruction and an address, which comprise 13 data bits. An instruction consists of 4 bits of data; these are applied to the logic processing unit and the register processing unit. ${ }^{1}$ ) The other 9 bits of data form the scratch-pad memory address and are used to select the data bit at this memory location, and also one of the 328 -bit registers. ${ }^{1}$ ) The logic processing unit only processes data from the scratch-pad memory. The register processing unit processes the data stored in one of the 8 -bits registers, in conjunction with a working register (A-register). Due to the fact that a register is always selected when a scratch-pad memory address is selected, the results of register processing will be stored in the corresponding scratch-pad memory location (condition register). Data for the registers can be supplied by the program memory or by an external source. These data are stored in the registers during the data processing cycle.

[^1]

Fig. 1. Simplified block diagram of the central processor. Blocks drawn with broken lines are only extant in the CP10.

The central processor is built on an epoxy-glass printed-wiring board of $233,4 \mathrm{~mm} x$ 160 mm (Euro-card system). The board is provided with two F068-I connectors (board parts); the corresponding panel parts are available under catalogue number 242202589288 (pins for wire wrap), 242202589298 (pins for dip soldering) or 242202589326 (solder tags) ${ }^{1}$ ). The board has a metal screen at the components side, which is connected to the 0 V line.

[^2]
## ELECTRICAL DATA

## Supply

Supply voltage (d.c.)
$\mathrm{V}_{\mathrm{P}} \quad 5 \mathrm{~V} \pm 5 \%$
current
Ip max. $2,1 \mathrm{~A}$
typ. 1,9 A
Battery back-up requirements to save contents of the scratch-pad memory in case of power failure.

Battery voltage
Battery current ( $\mathrm{V}_{\mathrm{P}}=0 \mathrm{~V}$ )
VB 4,5 to $7,5 \mathrm{~V}$
Trickle charge current $\left(\mathrm{V}_{\mathrm{P}}=5 \mathrm{~V}\right)$
$\mathrm{I}_{\mathrm{B}} \quad$ typ. $3,5 \mathrm{~mA}$ at $\mathrm{V}_{\mathrm{B}}=5 \mathrm{~V}$
typ. 2 mA at $\mathrm{V}_{\mathrm{B}}=5 \mathrm{~V}$

Input data
All inputs meet the standard TTL specifications.

| input | function | load | terminations (Fig. 4) |  |
| :---: | :---: | :---: | :---: | :---: |
|  |  |  | connector 1 | connector 2 |
| $\mathrm{PBMCP}_{0}$ <br> PBMCP $_{1}$ <br> $\mathrm{PBMCP}_{2}$ <br> $\mathrm{PBMCP}_{3}$ <br> PBMCP $_{4}$ <br> PBMCP $_{5}$ <br> ${ }^{\text {PBMCP }} 6$ <br> $\mathrm{PBMCP}_{7}$ <br> $\mathrm{PBMCP}_{8}$ <br> $\mathrm{PBMCP}_{9}$ <br> PBMCP 10 <br> PBMCP $_{11}$ <br> PBMCP $_{12}$ | Program word bits from program memory. | $\begin{aligned} & 1 \mathrm{TTL} \\ & 1 \mathrm{TTL} \\ & 1 \text { TTL } \\ & 1 \text { TTL } \\ & 1 \text { TTL } \\ & 1 \text { TTL } \\ & 1 \text { TTL } \\ & 1 \text { TTL } \\ & 1 \text { TTL } \\ & 1 \text { TTL } \\ & 1 \text { TTL } \\ & 1 \text { TTL } \\ & 1 \text { TTL } \end{aligned}$ |  | a2, c2 <br> a3, c3 <br> a4, c 4 <br> a5, c5 <br> a6, c6 <br> a7, c7 <br> a8, c8 <br> a9, c9 <br> a10, c 10 <br> a11, cll <br> a12, c 12 <br> a13, c 13 <br> a14, c14 |
| MICC | Memory identification signal; this signal is connected to one of the four ENCMoutputs of the central processor. | 2 TTL | a5 |  |
| SCPC | Store command from programming unit; initiates SCCM (see output data) when the central processor is in a data processing cycle. | 2 TTL |  | a 15, c15 |
| DBIC | Data bit from input stage; data is stored in scratch-pad memory during input/ output cycle. | 3 TTL | c20 |  |
| CLCP | Clear signal from external source. When CLCP is LOW the central processor is kept in the start position of an input/output cycle; when CLCP is HIGH the central processor is running (see also SPCE). | 2 TTL | a20 |  |


| input | function | load | terminations (Fig. 4) |  |
| :--- | :--- | :--- | :--- | :--- |
|  |  |  |  | connector 1 |
|  | Scratch-pad clear enable line from ex- <br> ternal source. When SPCE is HIGH and <br> CLCP goes from LOW to HIGH all <br> scratch-pad places (except those which <br> are addressed as an input) are set to zero <br> in the first input/output cycle; when SPCE <br> is LOW and CLCP goes from LOW to <br> HIGH the central processor starts with a <br> normal input/output cycle. | 2 TTL | a22 |  |
| SPCE |  |  |  |  |

Output data
All outputs meet the standard TTL specifications.

| output | function | loadability | terminations (Fig. 4) |  |
| :---: | :---: | :---: | :---: | :---: |
|  |  |  | connector 1 | connector 2 |
| $\mathrm{ABCIO}_{0}$ | Address bits to input and output modules. $\mathrm{ABCIO}_{0-3}$ select the input or output stage, $\mathrm{ABCIO}_{4-8}$ select the input or output modules. | 32 TTL | c2 |  |
| $\mathrm{ABCIO}_{1}$ |  | 32 TTL | c4 |  |
| $\mathrm{ABCIO}_{2}$ |  | 32 TTL | c6 |  |
| $\mathrm{ABCIO}_{3}$ |  | 32 TTL | c 8 |  |
| $\mathrm{ABCIO}_{4}$ |  | 32 TTL | c 10 |  |
| $\mathrm{ABCIO}_{5}$ |  | 32 TTL | c 12 |  |
| $\mathrm{ABCIO}_{6}$ |  | 32 TTL | c 14 |  |
| $\mathrm{ABCIO}_{7}$ |  | 32 TTL | c16 |  |
| $\mathrm{ABCIO}_{8}$ |  | 32 TTL | c18 |  |


| output | function | loada- <br> bility | terminations (Fig. 4) |  |
| :---: | :---: | :---: | :---: | :---: |
|  |  |  | connector 1 | connector 2 |
| $\mathrm{ABCM}_{0}$ $\mathrm{ABCM}_{1}$ $\mathrm{ABCM}_{2}$ $\mathrm{ABCM}_{3}$ $\mathrm{ABCM}_{4}$ $\mathrm{ABCM}_{5}$ $\mathrm{ABCM}_{6}$ $\mathrm{ABCM}_{7}$ $\mathrm{ABCM}_{8}$ $\mathrm{ABCM}_{9}$ | Address bits to program memory, initiated by program address counter. | 10 TTL 10 TTL 10 TTL 10 TTL 10 TTL 10 TTL 10 TTL 10 TTL 10 TTL 10 TTL |  | a20, c20 <br> a21, c21 <br> a22, c22 <br> a23, c23 <br> a24, c24 <br> a25, c25 <br> a26, c26 <br> a27, c27 <br> a28, c28 <br> a29, c29 |
| $\mathrm{ENCM}_{1}$ <br> $\mathrm{ENCM}_{2}$ <br> $\mathrm{ENCM}_{3}$ <br> $\mathrm{ENCM}_{4}$ | Enable signal to program memory; four lines are necessary when program memory capacity is extended to 4 k | $\begin{array}{\|l} 8 \text { TTL } \\ 8 \text { TTL } \\ 8 \text { TTL } \\ 8 \text { TTL } \end{array}$ | $\begin{array}{ll} \text { a1, c1 } \\ \text { a2 } & \\ \text { a3 } & \\ \text { a4 } & \end{array}$ |  |
| SCCM | Store command to program memory; level determines whether a program word is read out from program memory to central processor (LOW) or a new program word is written into the program memory (HIGH). SCCM $=\overline{\text { SCPC }}$. | 10 TTL |  | a17, c17 |
| $\frac{\mathrm{CICM}}{\overline{\mathrm{CICM}}}$ | Cycle initiate signal to program memory; depending on the level of SCCM, CICM starts read/restore or clear/write cycle (bipolar to reduce noise sensitivity). | 9 TTL |  | $\begin{array}{ll} \text { a 19, c19 } \\ \text { a 18, c18 } \end{array}$ |
| $\overline{\mathrm{CL}}_{23}$ | Inverted clock signal to programming unit. | 10 TTL | a 15 |  |
| CLCO | Clock signal to output module, stores data on DBCO into output stage during input/output cycle. | $\begin{aligned} & 32 \times \\ & \text { OM } 10 \end{aligned}$ | a28 |  |
| DBCO | Data bit to output module; data is stored in output stage by CLCO. | 31 TTL | c22 |  |
| SBCP | Status bit to programming unit; clocked by $\phi_{57}$ it indicates " 1 " or " 0 " at selected scratch-pad memory address. | 1 TTL | a 16 |  |
| LDCP | Synchronization signal to programming unit, synchronizes auxiliary address counter in programming unit with address counter in central processor. | 10 TTL | a 14 |  |
| ${ }^{\text {¢ }}$ 57 | Clock signal for state indication on programming unit; occurs only during data processing cycle. | 10 TTL |  | a 16, c 16 |

Alarm output (a26 of connector 1) : open collector output, which indicates a LOW level when $\mathrm{V}_{\mathrm{P}}<4,75 \mathrm{~V} . \mathrm{V}_{\text {alarm }}$, LOW level $<0,4 \mathrm{~V}$ at $\mathrm{I}_{\mathrm{c}}=3 \mathrm{~mA}$.

## Time data

Scan time per input or output module
Read time per 1 k memory module
Total cycle time
$0,029 \mathrm{~ms}$
$1,85 \mathrm{~ms}$
$0,029\left(\mathrm{n}_{\mathrm{IM}}+\mathrm{n}_{\mathrm{OM}}\right)+1,85 \mathrm{n}_{\mathrm{MM}} \mathrm{ms}$
$\mathrm{n}_{\mathrm{IM}}=$ number of input modules
$\mathrm{n}_{\mathrm{OM}}=$ number of output modules
$\mathrm{n}_{\mathrm{MM}}=$ number of memory modules
Note - By removing a wire jump, marked " A ", on the central processor board the scan time per input or output module is set to $7,4 \mathrm{~ms}$.


Fig.2. Timing diagram of data processing cycle.


Fig. 3. Timing diagram of input/output cycle.


Fig. 4

Mass
400 g

Terminal location
connector 1

| row c |  | row a |
| :---: | :---: | :---: |
| $\mathrm{ENCM}_{1}$ | 1 | $\mathrm{ENCM}_{1}$ |
| $\mathrm{ABCIO}_{0}$ | 2 | $\mathrm{ENCM}_{2}$ |
| n.c. | 3 | ENCM3 |
| $\mathrm{ABCIO}_{1}$ | 4 | $\mathrm{ENCM}_{4}$ |
| n.c. | 5 | MICC |
| $\mathrm{ABClO}_{2}$ | 6 | $\mathrm{LEX}_{0}$ |
| n.c. | 7 | $\mathrm{LEX}_{1}$ |
| $\mathrm{ABCIO}_{3}$ | 8 | $\mathrm{LEX}_{2}$ |
| $\mathrm{n} . \mathrm{c}$. | 9 | $\mathrm{LEX}_{3}$ |
| $\mathrm{ABCIO}_{4}$ | 10 | $\mathrm{LEX}_{4}$ |
| n.c. | 11 | $\mathrm{LEX}_{5}$ |
| $\mathrm{ABCIO}_{5}$ | 12 | LEX $_{6}$ |
| n.c. | 13 | $\mathrm{LEX}_{7}$ |
| $\mathrm{ABClO}_{6}$ | 14 | LDCP |
| n.c. | 15 | $\overline{\mathrm{CL}}_{23}$ |
| $\mathrm{ABCIO}_{7}$ | 16 | SBCP |
| n.c. | 17 | n.c. |
| $\mathrm{ABCIO}_{8}$ | 18 | n.c. |
| n.c. | 19 | n.c. |
| DBIC | 20 | CLCP |
| n.c. | 21 | n.c. |
| DBCO | 22 | SPCE |
| n.c. | 23 | n.c. |
| IDIC | 24 | n.c. |
| n.c. | 25 | n.c. |
| IDLC | 26 | alarm |
| n.c. | 27 | n.c. |
| $0 \mathrm{~V}^{\mathbf{1}}$ ) | 28 | CLCO |
| n.c. | 29 | n.c. |
| n.c. | 30 | n.c. |
| $\mathrm{V}_{\mathrm{P}}$ | 31 | Vp |
| 0 V | 32 | 0 V |

connector 2

| row c |  | row a |
| :---: | :---: | :---: |
| i. c. | 1 | i.c. |
| $\mathrm{PBMCP}_{0}$ | 2 | $\mathrm{PBMCP}_{0}$ |
| $\mathrm{PBMCP}_{1}$ | 3 | $\mathrm{PBMCP}_{1}$ |
| $\mathrm{PBMCP}_{2}$ | 4 | $\mathrm{PBMCP}_{2}$ |
| PBMCP 3 | 5 | $\mathrm{PBMCP}_{3}$ |
| PBMCP 4 | 6 | $\mathrm{PBMCP}_{4}$ |
| PBMCP5 | 7 | $\mathrm{PBMCP}_{5}$ |
| $\mathrm{PBMCP}_{6}$ | 8 | PBMCP6 |
| $\mathrm{PBMCP}_{7}$ | 9 | $\mathrm{PBMCP}_{7}$ |
| $\mathrm{PBMCP}_{8}$ | 10 | $\mathrm{PBMCP}_{8}$ |
| PBMCP9 | 11 | $\mathrm{PBMCP}_{9}$ |
| PBMCP 10 | 12 | PBMCP 10 |
| $\mathrm{PBMCP}_{11}$ | 13 | $\mathrm{PBMCP}_{11}$ |
| $\mathrm{PBMCP}_{12}$ | 14 | $\mathrm{PBMCP}_{12}$ |
| SCPC | 15 | SCPC |
| ¢ 57 | 16 | \$ 57 |
| SCCM | 17 | SCCM |
| CICM | 18 | CICM |
| CICM | 19 | CICM |
| $\mathrm{ABCM}_{0}$ | 20 | $\mathrm{ABCM}_{0}$ |
| $\mathrm{ABCM}_{1}$ | 21 | $\mathrm{ABCM}_{1}$ |
| $\mathrm{ABCM}_{2}$ | 22 | $\mathrm{ABCM}_{2}$ |
| $\mathrm{ABCM}_{3}$ | 23 | $\mathrm{ABCM}_{3}$ |
| $\mathrm{ABCM}_{4}$ | 24 | $\mathrm{ABCM}_{4}$ |
| $\mathrm{ABCM}_{5}$ | 25 | $\mathrm{ABCM}_{5}$ |
| $\mathrm{ABCM}_{6}$ | 26 | $\mathrm{ABCM}_{6}$ |
| $\mathrm{ABCM}_{7}$ | 27 | $\mathrm{ABCM}_{7}$ |
| $\mathrm{ABCM}_{8}$ | 28 | $\mathrm{ABCM}_{8}$ |
| ABCM9 | 29 | ABCM9 |
| $\mathrm{V}_{\mathrm{B}}$ | 30 | $\mathrm{V}_{\mathrm{B}}$ |
| $\mathrm{V}_{\mathrm{p}}$ | 31 | $\mathrm{V}_{\mathrm{P}}$ |
| 0 V | 32 | 0 V |

n. c. = not connected.
i. c. = internal connection.

[^3]
## INPUT MODULES

## DESCRIPTION

These input modules are intended for use in combination with the central processor CP10 (or CP11), memory module MM10 (or MM11 or MM12), output module OM10 (or OM12) and programming unit PU10 to assemble a programmable logic controller (PLC).
The IM10 and IM11 are identical in many respects, but the IM10 is designed for d.c. inputs, whereas the IM11 is designed for a.c. and unsmoothed rectified inputs. Each input module contains 16 addressable input stages, equipped with photocouplers to obtain electrical isolation between external and internal circuitry (Fig. 1). All inputs are floating with respect to each other. Each input stage has a LED for status indication: it is lit when the input is active. A delay circuit (symmetrical delay time typ. 1 ms ) is incorporated in each input stage of the IM 10 , to increase the noise immunity. The delay time can be increased by adding extra capacitance (approx. $0,068 \mu \mathrm{~F} / \mathrm{ms}$ ). A rectifying and smoothing circuit is incorporated in each input stage of the IM11.


Fig. 1a Circuit diagram of an input stage (IM10).


Fig. 1b Circuit diagram of an input stage (IM11).

Each input module has nine address inputs ( $\mathrm{ABCIO}_{0-8}$ ) and five module identification inputs ( $\overline{\mathrm{MID}}_{0-4}$ ), which are accessible on the connectors at the rear (Fig. 2).
The circuit is built on an epoxy-glass printed-wiring board of $233,4 \mathrm{~mm} \times 160 \mathrm{~mm}$ (Euro-card system). The board is provided with two F068-1 connectors (board parts); the corresponding rack parts are available on the back panels BP11 to BP16 or separately under catalogue number 242202589291 (pins for wire wrapping), 242202589299 (pins for dip soldering) or 242202589327 (solder tags).*


Fig. 2 Block diagram of the input modules.

[^4]
## ELECTRICAL DATA

## Supply

Supply voltage (d.c.)
current

$$
\begin{array}{ll}
\mathrm{V} P & 5 \mathrm{~V} \pm 5 \% \\
\mathrm{lp} & \max .0,5 \mathrm{~A} \\
& \text { typ. 0,45 A }
\end{array}
$$

## Input data

The data inputs are $\mathrm{DI}_{\mathrm{XYO}}$ to $\mathrm{DI}_{\mathrm{XY7}}$ and $\mathrm{DI}_{\mathrm{XZO}}$ to $\mathrm{DI}_{\mathrm{XZ7}}$. They are accessible on connector 2, see "Terminal location".

Active voltage ( $\mathrm{V}_{\mathrm{a}-\mathrm{c}}$ )*
Non-active voltage ( $\mathrm{V}_{\mathrm{a}-\mathrm{c}}$ )*
Input current, active at $\mathrm{V}_{\mathrm{a}-\mathrm{c}}=5 \mathrm{~V}$ or 24 V resp.

| 5 V level** | 24 V level |
| :--- | :--- |
| 3,5 to $6 \mathrm{~V} \mathrm{\Delta}$ | 17 to $30 \mathrm{~V} \mathrm{\Delta}$ |
| 0 to $0,8 \mathrm{~V}$ or floating | 0 to 7 V or floating |
| typ. 10 mA | typ. 10 mA |

The inputs mentioned below meet the standard TTL specifications.

| input | function | load | terminations of connector 1 (Fig. 3) |
| :---: | :---: | :---: | :---: |
| $\mathrm{ABClO}_{0}$ <br> $\mathrm{ABClO}_{1}$ <br> $\mathrm{ABClO}_{2}$ <br> $\mathrm{ABClO}_{3}$ <br> $\mathrm{ABClO}_{4}$ <br> $\mathrm{ABClO}_{5}$ <br> $\mathrm{ABClO}_{6}$ <br> $\mathrm{ABClO}_{7}$ <br> $\mathrm{ABClO}_{8}$ | Address bits from central processor; $\mathrm{ABCIO}_{0-3}$ select the input stage, $\mathrm{ABClO}_{4-8}$ selection the input module. | 1 TTL <br> 1 TTL <br> 1 TTL <br> 1 TTL <br> 1 TTL <br> 1 TTL <br> 1 TTL <br> 1 TTL <br> 1 TTL | a2, c2 <br> a4, c4 <br> a6, c6 <br> a8, c8 <br> a10 <br> a12 <br> a14 <br> a16 <br> a18 |
| MIN | Module inhibit signal from external source; a low level applied to this input inhibits data on DBIC to be stored in the scratchpad memory of the central processor. | 2 TTL | c26 |
| $\begin{aligned} & \overline{\mathrm{MID}}_{0} \\ & \overline{\mathrm{MID}}_{1} \\ & \overline{\mathrm{MID}}_{2} \\ & \overline{\mathrm{MID}}_{3} \end{aligned}$ | Module identification inputs; provide module with individual identity. | $\begin{aligned} & 2 \text { TTL } \\ & 2 \text { TTL } \\ & 2 ~ T T L \\ & 2 ~ T T L \\ & 2 ~ T T L \end{aligned}$ | $\begin{aligned} & \text { c10 } \\ & \text { c12 } \\ & \text { c14 } \\ & \text { c16 } \\ & \text { c18 } \end{aligned}$ |

* Voltage between terminal of row a and terminal of row cof connector 2.
${ }^{* *}$ By short-circuiting terminals B1 and B2 (see Figs 1a and 1b).
$\Delta$ D.C. (for IM10) or a.c. values (for IM11).


## Output data

All outputs (open collector) meet the standard TTL specifications.

| output | function | loadability | terminations of <br> connector 1 (Fig. 3) |
| :--- | :--- | :--- | :---: |
| DBIC | Data bit to central processor; data is <br> stored in scratch-pad memory of <br> central processor. | 10 TTL | a 20 |
| IDIC | Identification signal to central processor <br> (active LOW); prepares central pro- <br> cessor for data on DBIC to be written in <br> the scratch-pad memory. | 10 TTL | c24 |
| IDLC | Identification signal from last input <br> module to central processor (active <br> HIGH); only the IDLC output of the last <br> input module has to be connected with <br> the IDLC input of the central processor. | 2 TTL | a26 |

## Outlines



Fig. 3.
Mass $\quad 250 \mathrm{~g}$

Terminal location
connector 1

| row c |  | row a |
| :--- | :--- | :--- |
| $\mathrm{ABCIO}_{0}$ | 2 | $\mathrm{ABCIO}_{0}$ |
| $\mathrm{ABCIO}_{1}$ | 4 | $\mathrm{ABCIO}_{1}$ |
| $\mathrm{ABCIO}_{2}$ | 6 | $\mathrm{ABCIO}_{2}$ |
| $\mathrm{ABCIO}_{3}$ | 8 | $\mathrm{ABCIO}_{3}$ |
| $\overline{\mathrm{MID}}_{0}$ | 10 | $\mathrm{ABCIO}_{4}$ |
| $\overline{\mathrm{MID}}_{1}$ | 12 | $\mathrm{ABCIO}_{5}$ |
| $\overline{\mathrm{MID}}_{2}$ | 14 | $\mathrm{ABCIO}_{6}$ |
| $\overline{\mathrm{MID}}_{3}$ | 16 | $\mathrm{ABCIO}_{7}$ |
| $\overline{\mathrm{MID}} 4^{0 V^{*}}$ | 18 | $\mathrm{ABCIO}_{8}$ |
| 0 V | 20 | DBIC |
| $I D I C$ | 22 | n.c. |
| MIN | 24 | n.c. |
| $\mathrm{n.c}$. | 26 | $I D L C$ |
| V | 28 | n.c. |
| 0 V | 30 | VP |
|  | 32 | 0 V |

connector 2

| row c |  | row a |
| :--- | :--- | :--- |
| DIXYO | 2 | DIXY0 |
| DIXY1 | 4 | DIXY1 |
| DIXY2 | 6 | DIXY2 |
| DIXY3 | 8 | DIXY3 |
| DIXY4 | 10 | DIXY4 |
| DIXY5 | 12 | DIXY5 |
| DIXY6 | 14 | DIXY6 |
| DIXY7 | 16 | DIXY7 |
| DIXZ0 | 18 | DIXZ0 |
| DIXZ1 | 20 | DIXZ1 |
| DIXZ2 | 22 | DIXZ2 |
| DIXZ3 | 24 | DIXZ3 |
| DIXZ4 | 26 | DIXZ4 |
| DIXZ5 | 28 | DIXZ5 |
| DIXZ6 | 30 | DIXZ6 |
| DIXZ7 | 32 | DIXZ7 |

n.c. $=$ not connected.

* No supply line; only to be used for coding of the $\overline{\mathrm{MID}_{0-4}}$ lines.


## LOAD EXTERNAL INTERFACE

## DESCRIPTION

This load external interface is intended for use in combination with the central processor CP10, input module IM10 or IM11, output module OM10 or OM12, memory module MM10, MM11 or MM12 and programming unit PU10 to assemble a programmable logic controller (PLC). The module can be used as an interface between the load external inputs $\mathrm{LEX}_{0}$ to $\mathrm{LEX}_{7}$ on the CP 10 and a number of 8 -bit data sources. The data outputs of the different data sources have to be connected to one 8 -bit data bus. The LX10 has 16 enable outputs $\overline{E N}_{0}$ to $\overline{E N}_{17}$, which are to enable the different data sources. The 8 -bit data bus has to be connected to the data inputs $\mathrm{DB}_{0}$ to $\mathrm{DB}_{7}$. The data applied to the data inputs can be inverted on the LX10 by activating the data bit invert input DBI (see the truth table on the next page). The applied data can have a 5 V or a 24 V level. A block diagram is given in Fig. 1. The data inputs and enable outputs are electrically isolated from the 5 V logic circuitry by means of photocouplers. All data inputs are floating with respect to each other. Reading data from the data sources will only occur during the input/output cycle. The data are then stored in a $16 \times 8$ randomaccess memory (RAM) on the LX10. The data can be read out of the RAM during the data processing cycle. Storing data into the RAM can be inhibited by applying a 0 V level to the module inhibit input (MIN). Reading data out of the RAM cannot be inhibited. The module has 6 address inputs $\mathrm{ABCIO}_{3}$ to $\mathrm{ABClO}_{8}$. This means that a total number of 64 data sources of 8 -bits can be connected to the PLC system via 4 LX10 modules. Therefore the module is provided with 2 module identification inputs ( $\overline{\mathrm{MID}}_{3}, \overline{\mathrm{MID}}_{4}$ ) which are accessible on the connector. Irrespective of the number of LX10 modules used, a complete input/output cycle of $0,924 \mathrm{~ms}$ will occur.


Fig. 1.

## Truth Table

| data inputs <br> $\mathrm{DB}_{0}$ to $\mathrm{DB}_{7}$ | data input <br> DBI | data ouput <br> $\mathrm{LEX}_{0}$ to $\mathrm{LEX}_{7}$ |
| :--- | :--- | :---: |
| active | active | 0 |
| non-active | active | 1 |
| active | non-active | 1 |
| non-active | non-active | 0 |

## ELECTRICAL DATA

## Supply

Logic supply voltage (d.c.)
Logic supply current (d.c.)
Supply voltage (d.c.) to drive enable outputs
Supply current (d.c.) to drive enable outputs

VP $5 \mathrm{~V} \pm 5 \%$
Ip $\begin{aligned} & \text { max. 0,7 A } \\ & \text { typ. } 0,6 \mathrm{~A}\end{aligned}$
typ. 0,6 A
$5 \mathrm{~V} \pm 5 \%$
$24 \mathrm{~V} \pm 25 \%$
max. 3 mA
typ. $2,5 \mathrm{~mA}$

## Input data

The data inputs are $\mathrm{DB}_{0}$ to $\mathrm{DB}_{7}$ and DBI. They are accessible on connector 2 (see "Terminal location" and Fig. 2 for connection).

Active voltage ( $\mathrm{V}_{\mathrm{a}-\mathrm{c}}$ )*

| 5 V level | 24 V level |
| :--- | :--- |
| 3,5 to 6 V | 18 to 30 V |
| 0 to $0,8 \mathrm{~V}$ | 0 to $0,8 \mathrm{~V}$ |
| typ. 10 mA | typ. 10 mA |

Connector 2
row a, terminals $1,3,5,7,9,11,13,15,17$
row a, terminals $2,4,6,8,10,12,14,16,18$
row $c$, terminals $(1,2),(3,4),(5,6),(7,8)$,
$(9,10),(11,12),(13,14)$, $(15,16),(17,18)$


Fig. 2 Input circuit DB0 to $\mathrm{DB}_{7}$ and DBI.

All other inputs are connected to the CP10 and meet the standard TTL specification except the CLCO-input.

[^5]| input | function | load | terminations (Fig. 4) |  |
| :---: | :---: | :---: | :---: | :---: |
|  |  |  | connector 1 | connector 2 |
| $\mathrm{ABClO}_{3}$ <br> $\mathrm{ABClO}_{4}$ <br> $\mathrm{ABClO}_{5}$ <br> $\mathrm{ABClO}_{6}$ <br> $\mathrm{ABClO}_{7}$ <br> $\mathrm{ABClO}_{8}$ | Address bits from central processor. | $\begin{aligned} & 1 \text { TTL } \\ & 1 \mathrm{TTL} \\ & 1 \mathrm{TTL} \\ & 1 \mathrm{TTL} \\ & 1 \mathrm{TTL} \\ & 1 \mathrm{TTL} \end{aligned}$ | a8 <br> a10 <br> a12 <br> a14 <br> a16 <br> a18 |  |
| LDCP | Signal from central processor indicating the beginning of data processing cycle. | 2 TTL | c15 |  |
| MICC | Signal from central processor; trailing edge indicates the end of the data processing cycle. | 1 TTL | c5 |  |
| MIN | Module inhibit signal from external source; a LOW level applied to this input inhibits data on $\mathrm{DB}_{0}$ to $\mathrm{DB}_{7}$ to be stored in the RAM on the LX10. | 2 TTL | c26 |  |
| $\begin{aligned} & \overline{\mathrm{MID}}_{3} \\ & \overline{\mathrm{MID}}_{4} \end{aligned}$ | Module identification inputs. | $\begin{aligned} & 2 \text { TTL } \\ & 2 \text { TTL } \end{aligned}$ | $\begin{aligned} & \mathrm{c} 16 \\ & \mathrm{c} 18 \end{aligned}$ |  |
| CLCO * | Clock signal from central processor. | * | a28 |  |

* Input with relatively high input resistance (typ. $40 \mathrm{k} \Omega$ ).

CLCO-input, LOW level: max. 1 V ;
HIGH level: min. 2,4 V.

## Output data

The enable outputs are $\overline{E N}_{0}$ to $\overline{E N}_{17}$; they are open-collector outputs.
Output voltage LOW, with respect to COMMON

$$
\text { at } \mathrm{I} \overline{\mathrm{EN}}=80 \mathrm{~mA} \quad \leqslant 0,5 \mathrm{~V}
$$

Output voltage HIGH
$\leqslant 30 \mathrm{~V}$

| output | function | loada- <br> bility | terminations (Fig. 4) |  |
| :---: | :---: | :---: | :---: | :---: |
|  |  |  | connector 1 | connector 2 |
| LEX $_{0}$ <br> LEX 1 <br> $\mathrm{LEX}_{2}$ <br> $\mathrm{LEX}_{3}$ <br> LEX $_{4}$ <br> LEX $_{5}$ <br> LEX $_{6}$ <br> $\mathrm{LEX}_{7}$ | Data outputs to be connected to $\mathrm{LEX}_{0}$ to $\mathrm{LEX}_{7}$ inputs of CP10. | 10 TTL 10 TTL 10 TTL 10 TTL 10 TTL 10 TTL 10 TTL 10 TTL | $\begin{array}{ll} \text { a7 } & \\ \text { a9 } & \mathrm{c} 9 \\ \mathrm{a} 11 & \mathrm{c} 9 \\ \mathrm{a} 13 & \mathrm{c} 11 \\ & \mathrm{c} 13 \end{array}$ |  |
| IDLC | Identification signal from the LX10 to the CP10. This connection forces a complete input/output cycle. This terminal is direct connected to 0 V on the LX10. |  | a25 |  |

## Time data

Time that a data source is enabled
when CP10 is used with non-extended
input/output cycle $\quad \mathrm{t}_{\mathrm{en}} \quad 58 \mu \mathrm{~s}$
when CP10 is used with extended
input/output cycle $\quad t_{e n} 14,8 \mathrm{~ms}$
Time that data have to be present on $\mathrm{DB}_{0}$ to $\mathrm{DB}_{7}$
before end of enable signal
with non-extended input/output cycle $\quad t_{d s} 12 \mu \mathrm{~s}$
with extended input/output cycle
$t_{d s} \quad 2 \mathrm{~ms}$


Fig. 3.

MECHANICAL DATA
Dimensions in mm
Outlines


Fig. 4.

Terminal location

|  | conne | or 1 |  |  | connector |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | row c |  | row a | row c |  |  | row a |  |
|  | n.c. | 1 | n.c. | (note 4) | $\mathrm{DB}_{0}$ | 1 | $\mathrm{DB}_{0}(5 \mathrm{~V})$ |  |
|  | n.c. | 2 | n.c. | (note 4) | $\mathrm{DB}_{0}$ | 2 | $\mathrm{DB}_{0}(24 \mathrm{~V})$ |  |
|  | n.c. | 3 | n.c. |  | DB1 | 3 | DB1 |  |
|  | n.c. | 4 | n.c. | (note 4) | DB1 | 4 | DB1 |  |
|  | MICC | 5 | n.c. |  | $\mathrm{DB}_{2}$ | 5 | $\mathrm{DB}_{2}$ |  |
|  | n.c. | 6 | n.c. | (note 4) | $\mathrm{DB}_{2}$ | 6 | $\mathrm{DB}_{2}$ |  |
|  | LEX 1 | 7 | $\mathrm{LEX}_{0}$ | (note 4) | $\mathrm{DB}_{3}$ | 7 | $\mathrm{DB}_{3}$ |  |
|  | n.c. | 8 | $\mathrm{ABCIO}_{3}$ | (note 4) | $\mathrm{DB}_{3}$ | 8 | $\mathrm{DB}_{3}$ |  |
|  | $\mathrm{LEX}_{3}$ | 9 | $\mathrm{LEX}_{2}$ |  | $\mathrm{CBH}_{4}$ | 9 | $\mathrm{DB}_{4}$ |  |
|  | n.c. | 10 | $\mathrm{ABClO}_{4}$ | (note 4) | $\mathrm{DB}_{4}$ | 10 | $\mathrm{DB}_{4}$ |  |
|  | LEX $_{5}$ | 11 | $\mathrm{LEX}_{4}$ | (note 4) | $\mathrm{DB}_{5}$ | 11 | $\mathrm{DB}_{5}$ |  |
|  | n.c. | 12 | $\mathrm{ABClO}_{5}$ | (note 4) | $\mathrm{DB}_{5}$ | 12 | $\mathrm{DB}_{5}$ |  |
|  | $\mathrm{LEX}_{7}$ | 13 | $\mathrm{LEX}_{6}$ | (note 4) | ${ }^{\text {d }} \mathrm{DB}_{6}$ | 13 | $\mathrm{DB}_{6}$ |  |
|  | n.c. | 14 | $\mathrm{ABCIO}_{6}$ | (note 4) | $\mathrm{DB}_{6}$ | 14 | $\mathrm{DB}_{6}$ |  |
|  | LDCP | 15 | n.c. | (note 4) | $\mathrm{DB}_{7}$ | 15 | $\mathrm{DB}_{7}$ |  |
|  | $\overline{\mathrm{MID}}_{3}$ | 16 | $\mathrm{ABClO}_{7}$ | (note 4) | $\mathrm{DB}_{7}$ | 16 | $\mathrm{DB}_{7}$ |  |
|  | n.c. | 17 | n.c. | (note 4) | DBI | 17 | DBI (5V) |  |
|  | $\overline{\mathrm{MID}}_{4}$ | 18 | $\mathrm{ABCIO}_{8}$ | (note 4) | DBI | 18 | DBI (24 V) |  |
|  | n.c. | 19 | n.c. |  | n.c. | 19 | n.c. |  |
|  | $0 \vee$ (note 1) | 20 | n.c. |  | $\overline{E N} 0$ | 20 | $\overline{E N}_{1}$ |  |
|  | n.c. | 21 | n.c. |  | $\overline{E N}_{2}$ | 21 | $\mathrm{EN}_{3}$ |  |
|  | 0 V (note 1) | 22 | n.c. |  | $\overline{E N}_{4}$ | 22 | $\overline{E N}_{5}$ |  |
|  | n.c. | 23 | n.c. |  | $\overline{E N}_{6}$ | 23 | $\overline{E N}_{7}$ |  |
|  | n.c. | 24 | n.c. |  | $\overline{E N}_{10}$ | 24 | EN 11 |  |
|  | n.c. | 25 | IDLC |  | $\overline{E N}_{12}$ | 25 | $\overline{E N}_{13}$ |  |
|  | MIN | 26 | n.c. |  | $\overline{E N}_{14}$ | 26 | $\overline{E N}_{15}$ |  |
|  | n.c. | 27 | n.c. |  | $\overline{\mathrm{EN}}_{16}$ | 27 | $\overline{E N}_{17}$ |  |
|  | 0 V (note 2) | 28 | CLCO |  | n.c. | 28 | n.c. |  |
|  | n.c. | 29 | n.c. |  | n.c. | 29 | n.c. |  |
|  | n.c. | 30 | n.c. |  | 24 V | 30 | 24 V |  |
| (note 3) | $\left\{\begin{array}{l}5 \mathrm{~V}\end{array}\right.$ | 31 | 5 V (note 3) | (note 5) | 5 V | 31 | 5 V | (note 5) |
| (note 3) | 10 V | 32 | 0 V ) (note 3) | - | COMMON | 32 | COMMON |  |

## Notes

1. No supply line; only to be used for coding of the $\overline{\mathrm{MID}}_{3,4}$ lines.
2. No supply line; only to be used as a ground connection for CLCO.
3. Logic supply.
4. Interconnected.
5. Enable output drive.

## MEMORY MODULE

## DESCRIPTION

This memory module is intended for use in combination with the central processor CP10 (or CP11), input module IM10, output module OM10 (or OM12) and programming unit PU10 to assemble a programmable logic controller (PLC). The control program is stored in the memory module.

The memory module is a random access magnetic core memory system with a basic capacity of 1024 words of 13 bits ( 1 k 13 ) and a cycle time of $1 \mu \mathrm{~s}$. The memory is complete in itself; it consists of a $3 \mathrm{D}, 3$-wire stack, timing selecting andinhibit circuitry, address and data registers, and a memory retention circuit including the 5 V sensing.

The memory module is built on three epoxy-glass printed-wiring boards. The module is provided with two F068-I connectors (board parts, Euro-card system); the corresponding panel parts are available under catalogue number 242202589288 (pins for wire wrap), 242202589298 (pins for dip soldering) or 242202589326 (solder tags) ${ }^{1}$ ).

## ELECTRICAL DATA

Supply
Supply voltage (d.c.)
current (cycle time $1,8 \mu \mathrm{~s}$ )

$$
\begin{array}{ll}
\mathrm{V}_{\mathrm{P}} & 5 \mathrm{~V} \pm 5 \% \\
\mathrm{I}_{\mathrm{P}} & \text { operating max. } \\
& \\
& \text { typ. } 1 \mathrm{~A} . \\
& \text { standby } \\
& \max .3,6 \mathrm{~A} \\
& \text { typ. } 3,3 \mathrm{~A}
\end{array}
$$

Note: The memory is in standby position when ENCM is LOW.

## Cooling

An air velocity of $0,2 \mathrm{~m} / \mathrm{s}$ is required.

[^6]Input data
All inputs meet the standard TTL specifications.

| input | function | load | terminations (Fig. 3) <br> connector 1 | connector 2 |
| :--- | :--- | :--- | :--- | :--- |

Output data
All outputs meet the standard TTL specifications.

| output | function | loadability | terminations (Fig. 3) |  |
| :---: | :---: | :---: | :---: | :---: |
|  |  |  | connector 1 | connector 2 |
| $\mathrm{PBMCP}_{0}$ |  | 9 TTL |  | a2, c2 |
| $\mathrm{PBMCP}_{1}$ |  | 9 TTL |  | a3, c3 |
| $\mathrm{PBMCP}_{2}$ |  | 9 TTL |  | a4, c4 |
| $\mathrm{PBMCP}_{3}$ |  | 9 TTL |  | a5, c5 |
| $\mathrm{PBMCP}_{4}$ |  | 9 TTL |  | a6, c6 |
| $\mathrm{PBMCP}_{5}$ | Program word bits from program memory | 9 TTL |  | a7, c7 |
| $\mathrm{PBMCP}_{6}$ | to central processor and programming unit. | 9 TTL |  | a8, c8 |
| $\mathrm{PBMCP}_{7}$ | Open collector output with pull-up resistor | 9 TTL |  | a9, c9 |
| $\mathrm{PBMCP}_{8}$ | (3,9 k 2 ). | 9 TTL |  | a10, c10 |
| PBMCP9 |  | 9 TTL |  | al1, c11 |
| $\mathrm{PBMCP}_{10}$ |  | 9 TTL |  | a12, c12 |
| $\mathrm{PBMCP}_{11}$ |  | 9 TTL |  | a13, c13 |
| $\mathrm{PBMCP}_{12}$ |  | 9 TTL |  | a14, c14 |
| $\overline{\text { PBMCP }}_{0}$ |  | 10TTL | c17 |  |
| $\overline{\text { PBMCP }}_{1}$ |  | 10TTL | c18 |  |
| $\overline{\text { PBMCP }}_{2}$ |  | 10TTL | c19 |  |
| $\overline{\mathrm{PBMCP}}_{3}$ |  | 10TTL | c20 |  |
| $\overline{\text { PBMCP }}_{4}$ |  | 10TTL | c21 |  |
| $\overline{\text { PBMCP }}_{5}$ |  | 10TTL | c22 |  |
| $\overline{\text { PBMCP }} 6$ | Inverted $\mathrm{PBMCP}_{0-12}$ enabled by ENPB | 10TTL | c23 |  |
| $\overline{\text { PBMCP }}_{7}$ | (three-state outputs). | 10TTL | c24 |  |
| $\overline{\text { PBMCP }}_{8}$ |  | 10TTL | c25 |  |
| $\overline{\text { PBMCP }}^{\text {PB }}$ |  | 10TTL | c26 |  |
| $\overline{\text { PBMCP }}^{10}$ |  | 10TTL | c27 |  |
| $\overline{\text { PBMCP }}_{11}$ |  | 10TTL | c28 |  |
| $\overline{\mathrm{PBMCP}}_{12}$ |  | 10TTL | c29 |  |
| DA | Data available signal. This signal becomes LOW max. 150 ns after CICM (or CICM), and goes HIGH as soon as the data become available at the outputs (max. 500 ns after CICM or CICM). Open collector output with pull-up resistor ( $3,9 \mathrm{k} \Omega$ ). | 9 TTL |  | a16, c16 |

## Time data

The relationship between the different input and output signals are given when the memory module is operating in a programmable logic controller system.


Fig. 1. Timing of read/restore mode.


Fig. 2. Timing of clear/write mode.

## MECHANICAL DATA

## Outlines



Fig. 3

Mass
780 g

Terminal location
connector 1

| ow c |  | row |
| :---: | :---: | :---: |
| $\mathrm{PBPM}_{0}$ | 1 | $\mathrm{ENCM}_{1}$ |
| $\mathrm{PBPM}_{1}$ | 2 | $\mathrm{ENCM}_{2}$ |
| $\mathrm{PBPM}_{2}$ | 3 | $\mathrm{ENCM}_{3}$ |
| $\mathrm{PBPM}_{3}$ | 4 | $\mathrm{ENCM}_{4}$ |
| $\mathrm{PBPM}_{4}$ | 5 | n.c. |
| $\mathrm{PBPM}_{5}$ | 6 | ENPB |
| $\mathrm{PBPM}_{6}$ | 7 | n.c. |
| $\mathrm{PBPM}_{7}$ | 8 | n.c. |
| $\mathrm{PBPM}_{8}$ | 9 | n.c. |
| $\mathrm{PBPM}_{9}$ | 10 | n.c. |
| $\mathrm{PBPM}_{10}$ | 11 | n.c. |
| $\mathrm{PBPM}_{11}$ | 12 | n.c. |
| $\mathrm{PBPM}_{12}$ | 13 | n.c |
| n.c. | 14 | n.c. |
| n.c. | 15 | n.c. |
| n.c. | 16 | n.c. |
| $\overline{\mathrm{PBMCP}}_{0}$ | 17 | n.c. |
| $\mathrm{PBMCP}_{1}$ | 18 | n. |
| $\overline{\text { PBMCP }}_{2}$ | 19 | n.c. |
| $\mathrm{PBMCP}_{3}$ | 20 | n. |
| ${ }^{\text {PBMCP }} 4$ | 21 | n.c. |
| $\overline{\text { PBMCP }}_{5}$ | 22 | n.c. |
| $\stackrel{\text { PBMCP }}{ }_{6}$ | 23 | n.c. |
| $\stackrel{\text { PBMCP }}{ } 7^{7}$ | 24 | n.c |
| $\overline{\text { PBMCP }}^{8}$ | 25 | n.c. |
| $\overline{\text { PBMCP }}^{\text {P }} 9$ | 26 | n.c. |
| $\mathrm{PBMCP}_{10}$ | 27 | n.c. |
| $\overline{\text { PBMCP }}_{11} 1$ | 28 | n.c. |
| $\overline{\text { PBMCP }}_{12}$ | 29 | n.c. |
| n.c. | 30 | n.c. |
| $\mathrm{V}_{\mathrm{P}}$ | 31 | $\mathrm{V}_{\mathrm{P}}$ |
| 0 V | 32 | 0 V |

connector 2

| row c |  | row a |
| :---: | :---: | :---: |
| n.c. | 1 | n.c. |
| $\mathrm{PBMCP}_{0}$ | 2 | PBMCP0 |
| $\mathrm{PBMCP}_{1}$ | 3 | $\mathrm{PBMCP}_{1}$ |
| $\mathrm{PBMCP}_{2}$ | 4 | $\mathrm{PBMCP}_{2}$ |
| $\mathrm{PBMCP}_{3}$ | 5 | $\mathrm{PBMCP}_{3}$ |
| $\mathrm{PBMCP}_{4}$ | 6 | $\mathrm{PBMCP}_{4}$ |
| $\mathrm{PBMCP}_{5}$ | 7 | $\mathrm{PBMCP}_{5}$ |
| $\mathrm{PBMCP}_{6}$ | 8 | $\mathrm{PBMCP}_{6}$ |
| $\mathrm{PBMCP}_{7}$ | 9 | $\mathrm{PBMCP}_{7}$ |
| $\mathrm{PBMCP}_{8}$ | 10 | $\mathrm{PBMCP}_{8}$ |
| $\mathrm{PBMCP}_{9}$ | 11 | $\mathrm{PBMCP}_{9}$ |
| $\mathrm{PBMCP}_{10}$ | 12 | $\mathrm{PBMCP}_{10}$ |
| $\mathrm{PBMCP}_{11}$ | 13 | $\mathrm{PBMCP}_{11}$ |
| $\mathrm{PBMCP}_{12}$ | 14 | $\mathrm{PBMCP}_{12}$ |
| i.c. | 15 | i.c. |
| DA | 16 | DA |
| SCCM | 17 | SCCM |
| CICM | 18 | CICM |
| CICM | 19 | CICM |
| $\mathrm{ABCM}_{0}$ | 20 | $\mathrm{ABCM}_{0}$ |
| $\mathrm{ABCM}_{1}$ | 21 | $\mathrm{ABCM}_{1}$ |
| $\mathrm{ABCM}_{2}$ | 22 | $\mathrm{ABCM}_{2}$ |
| $\mathrm{ABCM}_{3}$ | 23 | $\mathrm{ABCM}_{3}$ |
| $\mathrm{ABCM}_{4}$ | 24 | $\mathrm{ABCM}_{4}$ |
| $\mathrm{ABCM}_{5}$ | 25 | ABCM5 |
| $\mathrm{ABCM}_{6}$ | 26 | $\mathrm{ABCM}_{6}$ |
| $\mathrm{ABCM}_{7}$ | 27 | $\mathrm{ABCM}_{7}$ |
| $\mathrm{ABCM}_{8}$ | 28 | $\mathrm{ABCM}_{8}$ |
| $\mathrm{ABCM}_{9}$ | 29 | ABCM9 |
| i.c. | 30 | i.c. |
| $\mathrm{V}_{P}$ | 31 | $\mathrm{V}_{\mathrm{P}}$ |
| 0 V | 32 | 0 V |

n.c. = not connected.
i.c. = internal connection.

## MEMORY MODULE

## DESCRIPTION

The memory module MM11 is intended for use in the PLC system as a program memory or as an auxiliary unit for programming EPROMs (2708); see also Remark below. It contains 4 IC sockets in which 4 UV-erasable EPROMs can be plugged. The MM11 also contains an address buffer, output buffers, and 3 d.c./d.c. converters ( 5 V to $12 \mathrm{~V}, 5 \mathrm{~V}$ to -5 V and 5 V to 27 V ).
The MM11 has three operation modes which can be selected by two mode-selection inputs $\mathrm{MSI}_{1}$ and $\mathrm{MSI}_{2}$ (see also truth table under "Input data"):

- Read mode (RD): the module can be used as a read only memory (ROM), that is the situation when the module is used in an operating PLC system.
- Write into master mode (WIM) : data from MM10, MM11 or MM12* can brogram the EPROMs in the IC sockets.
- Write into RAM mode (WIR): the contents of the EPROMs on the MM11 can be written into an MM10*.

The last two modes will be started after pressing a push button, to be connected between terminal 24a of connector 1 and 0 V , or by applying a LOW level to that terminal.
When the MM11 is in the WIM mode the data flow will be as follows:

- the MM11 sends an address ( $\mathrm{ABCM}_{0}$ to $A B C M g$ ), an enable signal ( $E N C M_{1}$ or $E N C M_{2}$ ) and a cycle initiate signal (CICM/ $\overline{\mathrm{CICM}}$ ) to the data source which may be an MM10, MM11 or MM12 (the MM12 does not need a CICM signal);
- the data source will send the data to be programmed into the EPROMs on the MM11.

When the MM11 is in the WIR mode the data flow will be:

- the MM11 sends an address ( $\mathrm{ABCM}_{0}$ to $A B C M g$ ), an enable signal ( $E N C M_{1}$ or $E N C M_{2}$ ), a cycle initiate signal (CICM/ $\overline{\mathrm{CICM}}$ ) and a store command to the MM10;
- data from MM11 will go via PBPM ${ }_{0}$ to PBPM $_{12}$ to the MM10 and be stored into the MM10.

The MM11 has a capacity of 1 k 13 or 2 k 13 depending on whether there are 2 or 4 EPROMs on the module.

The enable input $\mathrm{ENCM}_{1}$ or $\mathrm{ENCM}_{3}$ (addresses 0000 to 1777 and 4000 to 5777 respectively) corresponds with the EPROMs in sockets 1 A and 1 B . The enable input $\mathrm{ENCM}_{2}$ or $\mathrm{ENCM}_{4}$ (addresses 2000 to 3777 and 6000 to 7777 respectively) corresponds with the EPROMs in sockets 2A and 2B. This means that one program word is stored into 2 EPROMs, $A$ and B, of which EPROMs A contain the instruction and the most significant digit of the address (address part of the program word), and EPROMs $B$ contain the remaining two digits.
The MM11 is supplied with two empty EPROMs 2708.

## Remark

Correct programming of EPROMs is only guaranteed, when completely erased EPROMs are used; for the correct erase procedure consult the relevant data sheet of the 2708 EPROMs.

[^7]
## ELECTRICAL DATA

## Supply

Supply voltage (d.c.)
Supply current

| $V_{p}$ | $5 \mathrm{~V} \pm 5 \%$ |
| :--- | :--- |
|  | max. $2,4 \mathrm{~A}$ <br> typ. $\quad 2 \mathrm{~A}$ |

## Remark

There are several terminals on the connectors which act as inputs or outputs depending on the mode in which the MM11 is operating (see below). These terminals are described under "Input data" and "Output data".

|  | operation mode |  |  |
| :--- | :--- | :---: | :---: |
| terminal | WIM | WIR | RD |
| CICM/ $\overline{\mathrm{CICM}}$ | output | output | input |
| ENCM $_{1}$ to $\mathrm{ENCM}_{4}$ | output | output | input |
| ABCMO $_{0}$ to $\mathrm{ABCMg}_{9}$ | output | output | input |
| PBMCPO $_{0}$ to PBMCP $_{12}$ | input | output | output |

## Input data

All inputs meet the standard TTL specifications.

| input | function | load | terminations (Fig.1) |  |
| :---: | :---: | :---: | :---: | :---: |
|  |  |  | connector 1 | connector 2 |
| $\mathrm{ABCM}_{0}$ |  | 1 TTL |  | a20, c20 |
| $\mathrm{ABCM}_{1}$ |  | 1 TTL |  | a21, c21 |
| $\mathrm{ABCM}_{2}$ |  | 1 TTL |  | a22, c22 |
| $\mathrm{ABCM}_{3}$ |  | 1 TTL |  | a23, 223 |
| $\mathrm{ABCM}_{4}$ |  | 1 TTL |  | a24, c24 |
| $\mathrm{ABCM}_{5}$ | Address inputs (RD mode). | 1 TTL |  | a25, 225 |
| $\mathrm{ABCM}_{6}$ |  | 1 TTL |  | a26, c26 |
| $\mathrm{ABCM}_{7}$ |  | 1 TTL |  | a27, 227 |
| ABCM8 |  | 1 TTL |  | a28, 228 |
| $\mathrm{ABCM}_{9}$ |  | 1 TTL |  | a29, c29 |
| CICM | Cycle initiate signal; bipolar to reduce | 2 TTL |  | a19, c19 |
| $\overline{\text { CICM }}$ | noise sensitivity (RD mode). | 2 TTL |  | a18, c18 |
| $\mathrm{ENCM}_{1}$ |  | 2 TTL | a1 |  |
| $\mathrm{ENCM}_{2}$ | Enable inputs; memory is enabled | 2 TTL | a2 |  |
| $\mathrm{ENCM}_{3}$ | when ENCM is HIGH (RD mode). | 2 TTL | a3 |  |
| $\mathrm{ENCM}_{4}$ |  | 2 TTL | a4 |  |
| $\mathrm{PBMCP}_{0}$ |  | 1 TTL |  | a2, c2 |
| $\mathrm{PBMCP}_{1}$ |  | 1 TTL |  | a3, c3 |
| $\mathrm{PBMCP}_{2}$ | Data inputs for data to be programmed | 1 TTL |  | a4, c4 |
| $\mathrm{PBMCP}_{3}$ | into the EPROMs (WIM mode). | 1 TTL |  | a5, c5 |
| $\mathrm{PBMCP}_{4}$ |  | 1 TTL |  | a6, c6 |
| $\mathrm{PBMCP}_{5}$ |  | 1 TTL |  | a7, c7 |


| input | function | load | terminations (Fig.1) |  |
| :---: | :---: | :---: | :---: | :---: |
|  |  |  | connector 1 | connector 2 |
| $\mathrm{PBMCP}_{6}$ <br> $\mathrm{PBMCP}_{7}$ <br> $\mathrm{PBMCP}_{8}$ <br> PBMCP9 <br> PBMCP $_{10}$ <br> PBMCP 11 <br> PBMCP 12 | Data inputs for data to be programmed into the EPROMs (WIM mode). | 1 TTL <br> 1 TTL <br> 1 TTL <br> 1 TTL <br> 1 TTL <br> 1TTL <br> 1 TTL |  | $\begin{aligned} & \text { a8, c8 } \\ & \text { a9, c9 } \\ & \text { a10, c10 } \\ & \text { a11, c11 } \\ & \text { a12, c12 } \\ & \text { a13, c13 } \\ & \text { a14, c14 } \end{aligned}$ |
| START | Input to start the WIM or the WIR mode (active LOW). | 2 TTL | a24 |  |
| REST | Input to restart the stopped WIM or WIR mode (active LOW) | 1 TTL | a19 |  |
| INH | Inhibit and stop input; when LOW the start input is inoperative. | 2 TTL | a25 |  |
| $\begin{aligned} & \mathrm{MSI}_{1} \\ & \mathrm{MSI}_{2} \end{aligned}$ | Mode selection inputs. | $\begin{aligned} & 6 \text { TTL } \\ & 6 \text { TTL } \end{aligned}$ | $\begin{aligned} & \text { a26 } \\ & \text { a27 } \end{aligned}$ |  |

Operation mode truth table

| mode | mode selection inputs |  |
| :---: | :---: | :---: |
|  | $\mathrm{MSI}_{1}$ | $\mathrm{MSI}_{2}$ |
| RD | HIGH <br> (floating) | HIGH <br> (floating) |
| WIM | active LOW | arbitrary level |
| WIR | HIGH <br> (floating) | active LOW |

Output data
All outputs meet the standard TTL specifications.


| output | function | loadability | terminations (Fig. 1) |  |
| :---: | :---: | :---: | :---: | :---: |
|  |  |  | connector 1 | connector 2 |
| $\mathrm{PBPM}_{0}$ |  | 10 TTL | c1 |  |
| $\mathrm{PBPM}_{1}$ |  | 10 TTL | c2 |  |
| $\mathrm{PBPM}_{2}$ |  | 10 TTL | c3 |  |
| $\mathrm{PBPM}_{3}$ |  | 10 TTL | c4 |  |
| $\mathrm{PBPM}_{4}$ |  | 10 TTL | c5 |  |
| $\mathrm{PBPM}_{5}$ |  | 10 TTL | c6 |  |
| $\mathrm{PBPM}_{6}$ | Program word bits to MM10 (WIR mode). | 10 TTL | c7 |  |
| $\mathrm{PBPM}_{7}$ | These three-state outputs are only | 10 TTL | c8 |  |
| $\mathrm{PBPM}_{8}$ | active in the WIR mode. | 10 TTL | c9 |  |
| PBPM9 |  | 10 TTL | c10 |  |
| $\mathrm{PBPM}_{10}$ |  | 10 TTL | c11 |  |
| $\mathrm{PBPM}_{11}$ |  | 10 TTL | c12 |  |
| $\mathrm{PBPM}_{12}$ |  | 10 TTL | c13 |  |

## Time data

## RD mode

Time between leading edges of $\mathrm{CICM} / \overline{\mathrm{CICM}}$ and data valid PBMCP $_{0}$ to PBMCP $_{12}$
max. 550 ns
Time between address changes on $\mathrm{ABCM}_{0}$ to ABCM 9 and leading edges of $\mathrm{CICM} / \mathrm{CICM}$ $\min . \quad 0 \mathrm{~ns}$

## WIM mode

Time to program 1 k or 2 k EPROM memory

## WIR mode

Time to read-out MM11 and store into MM10
$\max .18 \min$
typ. 15 min
max. 4,2 s
typ. $3,5 \mathrm{~s}$

## MECHANICAL DATA

Dimensions in mm

## Outlines



Fig. 1.

[^8]Terminal location

| connector 1 |  |  | connector 2 |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| row c |  | row a | row c |  | row a |
| $\mathrm{PBPM}_{0}$ | 1 | $\mathrm{ENCM}_{1}$ | n.c. | 1 | n.c. |
| $\mathrm{PBPM}_{1}$ | 2 | $\mathrm{ENCM}_{2}$ | $\mathrm{PBMCP}_{0}$ | 2 | $\mathrm{PBMCP}_{0}\left(\mathrm{O}_{54}{ }^{*}\right)$ |
| $\mathrm{PBPM}_{2}$ | 3 | $\mathrm{ENCM}_{3}$ | $\mathrm{PBMCP}_{1}$ | 3 | $\mathrm{PBMCP}_{1}\left(\mathrm{O}_{6 A}\right)$ |
| $\mathrm{PBPM}_{3}$ | 4 | $\mathrm{ENCM}_{4}$ | $\mathrm{PBMCP}_{2}$ | 4 | $\mathrm{PBMCP}_{2}\left(\mathrm{O}_{7 A}\right)$ |
| $\mathrm{PBPM}_{4}$ | 5 | n.c. | $\mathrm{PBMCP}_{3}$ | 5 | $\mathrm{PBMCP}_{3}\left(\mathrm{O}_{8 A}\right)$ |
| $\mathrm{PBPM}_{5}$ | 6 | n.c. | $\mathrm{PBMCP}_{4}$ | 6 | $\mathrm{PBMCP}_{4}\left(\mathrm{O}_{1 \mathrm{~B}}\right)$ |
| $\mathrm{PBPM}_{6}$ | 7 | n.c. | $\mathrm{PBMCP}_{5}$ | 7 | $\mathrm{PBMCP}_{5}\left(\mathrm{O}_{2} \mathrm{~B}\right)$ |
| $\mathrm{PBPM}_{7}$ | 8 | n.c. | PBMCP $_{6}$ | 8 | PBMCP $_{6}\left(\mathrm{O}_{3 \mathrm{~B}}\right)$ |
| $\mathrm{PBPM}_{8}$ | 9 | n.c. | $\mathrm{PBMCP}_{7}$ | 9 | $\mathrm{PBMCP}_{7}\left(\mathrm{O}_{58}\right)$ |
| PBPM9 | 10 | n.c. | PBMCP8 | 10 | $\mathrm{PBMCP}_{8}\left(\mathrm{O}_{6 \mathrm{~B}}\right)$ |
| $\mathrm{PBPM}_{10}$ | 11 | n.c. | PBMCP9 | 11 | PBMCP9 $\left(\mathrm{O}_{7 \mathrm{~B}}\right)$ |
| PBPM 11 | 12 | n.c. | PBMCP 10 | 12 | $\mathrm{PBMCP}_{10}\left(\mathrm{O}_{14}\right)$ |
| $\mathrm{PBPM}_{12}$ | 13 | n.c. | PBMCP 11 | 13 | $\mathrm{PBMCP}_{11}\left(\mathrm{O}_{2} \mathrm{~A}\right)$ |
| n.c. | 14 | n.c. | PBMCP 12 | 14 | $\mathrm{PBMCP}_{12}\left(\mathrm{O}_{3 A}\right)$ |
| n.c. | 15 | n.c. | n.c. | 15 | n.c. |
| n.c. | 16 | n.c. | n.c. | 16 | n.c. |
| n.c. | 17 | n.c. | SCCM | 17 | SCCM |
| n.c. | 18 | n.c. | $\overline{\text { CICM }}$ | 18 | $\overline{\text { CICM }}$ |
| n.c. | 19 | REST | CICM | 19 | CICM |
| n.c. | 20 | n.c. | $\mathrm{ABCM}_{0}$ | 20 | $\mathrm{ABCM}_{0}$ |
| n.c. | 21 | n.c. | $\mathrm{ABCM}_{1}$ | 21 | $\mathrm{ABCM}_{1}$ |
| n.c. | 22 | n.c. | $\mathrm{ABCM}_{2}$ | 22 | $\mathrm{ABCM}_{2}$ |
| n.c. | 23 | PRB | $\mathrm{ABCM}_{3}$ | 23 | $\mathrm{ABCM}_{3}$ |
| n.c. | 24 | START | $\mathrm{ABCM}_{4}$ | 24 | $\mathrm{ABCM}_{4}$ |
| n.c. | 25 | INH | $\mathrm{ABCM}_{5}$ | 25 | $\mathrm{ABCM}_{5}$ |
| n.c. | 26 | $\mathrm{MSI}_{1}$ | $\mathrm{ABCM}_{6}$ | 26 | $\mathrm{ABCM}_{6}$ |
| n.c. | 27 | $\mathrm{MSI}_{2}$ | $\mathrm{ABCM}_{7}$ | 27 | $\mathrm{ABCM}_{7}$ |
| n.c. | 28 | n.c. | $\mathrm{ABCM}_{8}$ | 28 | $\mathrm{ABCM}_{8}$ |
| n.c. | 29 | n.c. | ABCM9 | 29 | ABCM9 |
| n.c. | 30 | n.c. | n.c. | 30 | n.c. |
| $V_{P}$ | 31 | $V p$ | $V_{P}$ | 31 | $V_{P}$ |
| 0 V | 32 | 0 V | 0 V | 32 | 0 V |

n.c. $=$ not connected

[^9]
## MEMORY MODULE

## DESCRIPTION

The memory module MM12 is intended for use in the PLC system as a program memory. It contains 4 IC sockets in which 4 UV-erasable PROMs (2708) can be plugged. The MM12 also contains 10 buffered address inputs, 4 enable inputs, 16 buffered outputs and 2 d.c./d.c. converters ( 5 V to 12 V and 5 V to -5 V ).
The MM12 has a capacity of 2 k 16 . Although the PLC system operates with program words of 13 bits, the remaining 3 bits are also brought out ( $\mathrm{O}_{4 \mathrm{~A}}, \mathrm{O}_{4 \mathrm{~B}}, \mathrm{O}_{8 \mathrm{~B}}$ ), so that the module can be used in other applications which require 16 bits.
The enable input ENCM 1 or ENCM 3 (addresses 0000 to 1777 and 4000 to 5777 respectively) corresponds with the EPROMs in sockets 1 A and 1 B . The enable input $\mathrm{ENCM}_{2}$ or $\mathrm{ENCM}_{4}$ (addresses 2000 to 3777 and 6000 to 7777 respectively) corresponds with the EPROMs in sockets 2A and 2B. This means that one program word is stored into 2 EPROMs, $A$ and $B$, of which EPROMs $A$ contain the instruction and the most significant digit of the address (address part of the program word), and EPROMs B contain the remaining two digits.
Programming of the EPROMs cannot be done on the MM12: this has to be done on the MM11or by existing programming equipment.
The MM12 is supplied with two empty EPROMs 2708.

## ELECTRICAL DATA

## Supply

| Supply voltage (d.c.) | $V_{P}$ | $5 \mathrm{~V} \pm 5 \%$ |
| :---: | :---: | :---: |
| Supply current | ${ }^{\text {I }}$ | max. 1,2 A |

## Input data

All inputs meet the standard TTL specifications.

| input | function | load | terminations (Fig. 2) |  |
| :---: | :---: | :---: | :---: | :---: |
|  |  |  | connector 1 | connector 2 |
| $\mathrm{ABCM}_{0}$ <br> $\mathrm{ABCM}_{1}$ <br> $\mathrm{ABCM}_{2}$ <br> $\mathrm{ABCM}_{3}$ <br> $\mathrm{ABCM}_{4}$ <br> $\mathrm{ABCM}_{5}$ <br> $\mathrm{ABCM}_{6}$ <br> $\mathrm{ABCM}_{7}$ <br> $\mathrm{ABCM}_{8}$ <br> ABCM9 | Address bits from central processor | $\begin{aligned} & 1 \mathrm{TTL} \\ & 1 \mathrm{TTL} \\ & 1 \mathrm{TTL} \\ & 1 \mathrm{TTL} \\ & 1 \mathrm{TTL} \\ & 1 \mathrm{TTL} \\ & 1 \mathrm{TTL} \\ & 1 \mathrm{TTL} \\ & 1 \mathrm{TTL} \\ & 1 \mathrm{TTL} \end{aligned}$ |  | $\begin{aligned} & \text { a20, c20 } \\ & \text { a21, c21 } \\ & \text { a22, c22 } \\ & \text { a23, c23 } \\ & \text { a24, c24 } \\ & \text { a25, c25 } \\ & \text { a26, c26 } \\ & \text { a27, c27 } \\ & \text { a28, c28 } \\ & \text { a29, c29 } \end{aligned}$ |
| $\mathrm{ENCM}_{1}$ <br> $\mathrm{ENCM}_{2}$ <br> $\mathrm{ENCM}_{3}$ <br> $\mathrm{ENCM}_{4}$ | Enable inputs from central processor | $\begin{aligned} & 1 \mathrm{TTL} \\ & 1 \mathrm{TTL} \\ & 1 \mathrm{TTL} \\ & 1 \mathrm{TTL} \end{aligned}$ | $\begin{aligned} & \text { a1 } \\ & \text { a2 } \\ & \text { a3 } \\ & \text { a4 } \end{aligned}$ |  |

## Output data

All outputs are three-state outputs and meet the standard TTL specifications.

| output | function | loadability | terminations (Fig. 2) |  |
| :---: | :---: | :---: | :---: | :---: |
|  |  |  | connector 1 | connector 2 |
| PBMCPO <br> PBMCP $_{1}$ <br> $\mathrm{PBMCP}_{2}$ <br> $\mathrm{PBMCP}_{3}$ <br> $\mathrm{PBMCP}_{4}$ <br> PBMCP $_{5}$ <br> PBMCP $_{6}$ <br> $\mathrm{PBMCP}_{7}$ <br> PBMCP8 <br> PBMCP9 <br> PBMCP $_{10}$ <br> PBMCP 11 <br> PBMCP $_{12}$ | Program word bits from memory module to central processor | 10 TTL 10 TTL 10 TTL 10 TTL 10 TTL 10 TTL 10 TTL 10 TTL 10 TTL 10 TTL 10 TTL 10 TTL 10 TTL |  | a2, c2 <br> a3, c3 <br> a4, c4 <br> a5, c5 <br> a6, c6 <br> a7, c7 <br> a8, c8 <br> a9, c9 <br> a10, c10 <br> a11, c11 <br> a12, c12 <br> a13, c13 <br> a14, c14 |
| $\mathrm{O}_{4 \mathrm{~A}}$ | Buffered output from output 04 of EPROM A. | 10 TTL |  | a1, c1 |
| $\mathrm{O}_{4 \mathrm{~B}}$ | Buffered output from output 04 of EPROM B. | 10 TTL |  | a15, c15 |
| $\mathrm{O}_{88}$ | Buffered output from output O8 of EPROM B. | 10 TTL |  | a16, c16 |

## Time data

The relationship between the different input and output signals are given when the memory module is operating in the PLC system.


Fig. 1.

## MECHANICAL DATA

Dimensions in mm

## Outlines



Fig. 2.

[^10]Terminal location

| connector 1 |  |  | connector 2 |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| row c |  | row a | row c |  | row a |
| n.c. | 1 | $\mathrm{ENCM}_{1}$ | $\mathrm{O}_{4 A}$ | 1 | $\mathrm{O}_{4 \mathrm{~A}}\left(\mathrm{O}_{4 \mathrm{~A}}{ }^{*}\right)$ |
| n.c. | 2 | $\mathrm{ENCM}_{2}$ | $\mathrm{PBMCP}_{0}$ | 2 | $\mathrm{PBMCP}_{0}\left(\mathrm{O}_{5} \mathrm{~A}\right)$ |
| n.c. | 3 | $\mathrm{ENCM}_{3}$ | $\mathrm{PBMCP}_{1}$ | 3 | PBMCP $1_{1}\left(\mathrm{O}_{6 A}\right)$ |
| n.c. | 4 | $\mathrm{ENCM}_{4}$ | $\mathrm{PBMCP}_{2}$ | 4 | $\mathrm{PBMCP}_{2}\left(\mathrm{O}_{7 A}\right)$ |
| n.c. | 5 | n.c. | $\mathrm{PBMCP}_{3}$ | 5 | $\mathrm{PBMCP}_{3}\left(\mathrm{O}_{8 A}\right)$ |
| n.c. | 6 | n.c. | $\mathrm{PBMCP}_{4}$ | 6 | $\mathrm{PBMCP}_{4}\left(\mathrm{O}_{1 \mathrm{~B}}\right)$ |
| n.c. | 7 | n.c. | $\mathrm{PBMCP}_{5}$ | 7 | $\mathrm{PBMCP}_{5}\left(\mathrm{O}_{2 \mathrm{~B}}\right)$ |
| n.c. | 8 | n.c. | $\mathrm{PBMCP}_{6}$ | 8 | $\mathrm{PBMCP}_{6}\left(\mathrm{O}_{3 \mathrm{~B}}\right)$ |
| n.c. | 9 | n.c. | $\mathrm{PBMCP}_{7}$ | 9 | $\mathrm{PBMCP}_{7}\left(\mathrm{O}_{58}\right)$ |
| n.c. | 10 | n.c. | PBMCP8 | 10 | $\mathrm{PBMCP}_{8}\left(\mathrm{O}_{6 \mathrm{~B}}\right)$ |
| n.c. | 11 | n.c. | PBMCP9 | 11 | PBMCPg $\left(\mathrm{O}_{7 \mathrm{~B}}\right)$ |
| n.c. | 12 | n.c. | PBMCP 10 | 12 | $\mathrm{PBMCP}_{10}\left(\mathrm{O}_{14}\right)$ |
| n.c. | 13 | n.c. | PBMCP 11 | 13 | $\mathrm{PBMCP}_{11}\left(\mathrm{O}_{2} \mathrm{~A}\right)$ |
| n.c. | 14 | n.c. | $\mathrm{PBMCP}_{12}$ | 14 | $\mathrm{PBMCP}_{12}\left(\mathrm{O}_{3} \mathrm{~A}\right)$ |
| n.c. | 15 | n.c. | $\mathrm{Q}_{4 B}$ | 15 | $\mathrm{O}_{4 \mathrm{~B}}\left(\mathrm{O}_{4 \mathrm{~B}}\right)$ |
| n.c. | 16 | n.c. | $\mathrm{Q}_{8 B}$ | 16 | $\mathrm{C}_{88}\left(\mathrm{O}_{8 B}\right)$ |
| n.c. | 17 | n.c. | n.c. | 17 | n.c. |
| n.c. | 18 | n.c. | n.c. | 18 | n.c. |
| n.c. | 19 | n.c. | n.c. | 19 | n.c. |
| n.c. | 20 | n.c. | $\mathrm{ABCM}_{0}$ | 20 | $\mathrm{ABCM}_{0}$ |
| n.c. | 21 | n.c. | $\mathrm{ABCM}_{1}$ | 21 | $\mathrm{ABCM}_{1}$ |
| n.c. | 22 | n.c. | $\mathrm{ABCM}_{2}$ | 22 | $\mathrm{ABCM}_{2}$ |
| n.c. | 23 | n.c. | $\mathrm{ABCM}_{3}$ | 23 | $\mathrm{ABCM}_{3}$ |
| n.c. | 24 | n.c. | $\mathrm{ABCM}_{4}$ | 24 | $\mathrm{ABCM}_{4}$ |
| n.c. | 25 | n.c. | $\mathrm{ABCM}_{5}$ | 25 | $\mathrm{ABCM}_{5}$ |
| n.c. | 26 | n.c. | $\mathrm{ABCM}_{6}$ | 26 | $\mathrm{ABCM}_{6}$ |
| n.c. | 27 | n.c. | $\mathrm{ABCM}_{7}$ | 27 | $\mathrm{ABCM}_{7}$ |
| n.c. | 28 | n.c. | $\mathrm{ABCM}_{8}$ | 28 | $\mathrm{ABCM}_{8}$ |
| n.c. | 29 | n.c. | $\mathrm{ABCM}_{9}$ | 29 | $\mathrm{ABCM}_{9}$ |
| n.c. | 30 | n.c. | n.c. | 30 | n.c. |
| $V_{P}$ | 31 | $V_{p}$ | Vp | 31 | $V_{P}$ |
| 0 V | 32 | 0 V | 0 V | 32 | 0 V |

n.c. $=$ not connected.

[^11]
## OUTPUT MODULE

## DESCRIPTION

The output module is intended for use in combination with the central processor CP10 ( or CP11), input module IM10 ( or IM11 or LX10), memory module MM10 (or MM11 or MM12) and programming unit PU10 to assemble a programmable logic controller (PLC).

The output module contains 16 addressable output stages, equipped with photocouplers to obtain electrical isolation between external and internal circuitry (Fig. 1). All outputs are floating with respect to each other.
Each output stage has a suppressor diode, to allow it to switch inductive loads. Each output stage also has a LED for status indication: it is lit when the output transistor is conducting.


Fig. 1. Circuit diagram of an output stage.
The output module has nine address inputs $\left(\mathrm{ABCIO}_{0-8}\right)$ and five module identification inputs ( $\overline{\mathrm{MID}}_{0-4}$ ), which are accessible on the connectors at the rear (Fig. 2).

The circuit is built on an epoxy-glass printed-wiring board of $233,4 \mathrm{~mm} \times 160 \mathrm{~mm}$ (Euro-card sytem). The board is provided with two F068-I connectors (board parts); the corresponding panel parts are available under catalogue number 242202589291 (pins for wire wrap), 242202589299 (pins for dip soldering) or 242202589327 (solder tags) ${ }^{1}$ ).

[^12]

Fig. 2. Block diagram of the output module.

## ELECTRICAL DATA

Supply
Supply voltage (d.c.)
$\mathrm{V}_{\mathrm{P}}$
Ip
$5 \mathrm{~V} \pm 5 \%$
current
Ip
max. 1 A (all stages "ON")
typ. 0, 75 A ( 8 stages "ON", 8 stages "OFF")

Input data
All inputs meet the standard TTL specification except the CLCO-input.

| input | function | load | terminations of connector 1 (Fig.3) |
| :---: | :---: | :---: | :---: |
| $\mathrm{ABCIO}_{0}$ |  | 1 TTL | a2, c2 |
| $\mathrm{ABCIO}_{1}$ |  | 1 TTL | a4, c4 |
| $\mathrm{ABCIO}_{2}$ |  | 1 TTL | a6, c6 |
| $\mathrm{ABCIO}_{3}$ | Address bits from central processor; | 1 TTL | a8, c 8 |
| $\mathrm{ABCIO}_{4}$ | $\mathrm{ABCIO}_{0-3}$ select the output stage, | 1 TTL | a 10 |
| $\mathrm{ABCIO}_{5}$ | $\mathrm{ABCIO}_{4-8}$ select the output module. | 1 TTL | a12 |
| $\mathrm{ABCIO}_{6}$ |  | 1 TTL | a14 |
| $\mathrm{ABCIO}_{7}$ |  | 1 TTL | a16 |
| $\mathrm{ABCIO}_{8}$ |  | 1 TTL | a18 |
| DBCO | Data bit from central processor; data is stored in output stage by CLCO. | 1 TTL | a22 |
| MIN | Module inhibit signal from external source; a low level applied to this input inhibits data on DBCO to be stored in the output stage. | 2 TTL | c26 |
| REO | Reset output module line; a low level on this input will reset all output latches (output transistor non-conducting). | 1 TTL | a24 |
| $\overline{\text { MID }}$ |  | 2 TTL | c10 |
| $\overline{\text { MID }}$ |  | 2 TTL | c12 |
| $\overline{\text { MID }}$ | module with individual identity. | 2 TTL | c14 |
| $\overline{\overline{M I D}}$ |  | 2 TTL | c16 |
| $\overline{\mathrm{MID}} 4$ |  | 2 TTL | c 18 |
| CLCO* | Clock signal from central processor to output module, stores data on DBCO into output stage during input/output cycle. | * | a28 |

*) Input with relatively high input resistance (typ. $40 \mathrm{k} \Omega$ ).
CLCO-input, LOW level:max. 1 V :
HIGH level: min. 2, 4 V .

## Output data

The data outputs are $\mathrm{DOXY}_{\mathrm{X}}$ to $\mathrm{DO}_{\mathrm{XY}} 7$ and $\mathrm{DO}_{\mathrm{XZ} 0}$ to $\mathrm{DOXZ7}$. They are accessible on connector 2, see "Terminal location".
Output transistor conducting : output current $=\max .100 \mathrm{~mA}$ at $\left.\mathrm{V}_{\mathrm{a}-\mathrm{c}}{ }^{1}\right)=\max .1,5 \mathrm{~V}$
Output transistor non-conducting: output current $=\max .10 \mu \mathrm{~A}$ at $\mathrm{V}_{\mathrm{a}-\mathrm{c}}{ }^{1}$ ) $=\max .30 \mathrm{~V}$
Each data output has a suppressor diode, which allows the switching of loads with an inductance of max. 10 H .


The output (open collector) below meets the standard TTL specifications.

| output | function | loada- <br> bility | terminations of <br> connector 1 (Fig. 3) |
| :---: | :---: | :---: | :---: |
| IDLC | Identification signal from last output <br> module to central processor (active <br> HIGH); only the IDLC output of the last <br> output module has to be connected with <br> the IDLC input of the central processor. | 2 TTL | a26 |

## MECHANICAL DATA

Outlines


Fig. 3

Mass $\quad 230 \mathrm{~g}$

Terminal location
connector 1

| row c |  | row |
| :---: | :---: | :---: |
| $\mathrm{ABCIO}_{0}$ | 2 | $\mathrm{ABCIO}_{0}$ |
| $\mathrm{ABCIO}_{1}$ | 4 | $\mathrm{ABCIO}_{1}$ |
| $\mathrm{ABCIO}_{2}$ | 6 | $\mathrm{ABCIO}_{2}$ |
| $\mathrm{ABCIO}_{3}$ | 8 | $\mathrm{ABCIO}_{3}$ |
| $\overline{\text { MID }}$ | 10 | $\mathrm{ABClO}_{4}$ |
| $\overline{\mathrm{MID}_{1}}$ | 12 | $\mathrm{ABCIO}_{5}$ |
| $\overline{\text { MID } 2}$ | 14 | $\mathrm{ABClO}_{6}$ |
| $\overline{\text { MID }}$ | 16 | $\mathrm{ABCIO}_{7}$ |
| $\mathrm{MID}_{4}$ | 18 | $\mathrm{ABCIO}_{8}$ |
| $0 \mathrm{~V}^{1}$ ) | 20 | n.c. |
| $0 \mathrm{~V}^{1}$ ) | 22 | DBCO |
| n.c. | 24 | REO |
| MIN | 26 | IDLC |
| $0 \mathrm{~V}^{2}$ ) | 28 | CLCO |
| $\mathrm{V}_{\mathrm{p}}$ | 30 | Vp |
| 0 V | 32 | 0 V |

n.c. = not connected.
connector 2

| row c |  | row a |
| :--- | :--- | :--- |
| DOXY0 | 2 | DOXXY0 |
| DOXY1 | 4 | DOXY1 |
| DOXY2 | 6 | DOXY2 |
| DOXY3 | 8 | DOXY3 |
| DOXY4 | 10 | DOXY4 |
| DOXY5 | 12 | DOXY5 |
| DOXY6 | 14 | DOXY6 |
| DOXY7 | 16 | DOXY7 |
| DOXZ0 | 18 | DOXZ0 |
| DOXZ1 | 20 | DOXZ1 |
| DOXZ2 | 22 | DOXZ2 |
| DOXZ3 | 24 | DOXZ3 |
| DOXZ4 | 26 | DOXZ4 |
| DOXZ5 | 28 | DOXZ5 |
| DOXZ6 | 30 | DOXZ6 |
| DOXZ7 | 32 | DOXZ7 |

[^13]
## OUTPUT MODULE

## DESCRIPTION

The output module is intended for use in combination with the central processor CP10 (or CP11), input module IM10 (or IM11 or LX10), memory module MM10 (or MM11 or MM12) and programming unit PU10 to assemble a programmable logic controller (PLC).
The output module contains 8 addressable output stages, equipped with photocouplers to obtain electrical isolation between external and internal circuitry (Fig. 1). All outputs are open-collector outputs. Each output stage has a suppressor diode, to allow it to switch inductive loads. Each output stage also has a LED for status indication: it is lit when the output transistor is conducting.
The output stages feature electronic short-circuit protection which can only be de-activated by resetting the input signal. Short-circuit indication is provided by the lower row of LEDs on the front panel. If the status indicator LED and the short-circuit indicator LED with the same number are both lit, these output stages are working correctly. If the former LED is lit and the latter extinguished, this will indicate a short-circuit condition.


Fig. 1 Circuit diagram of an output stage.

The output module has 9 address inputs ( $\mathrm{ABClO} \mathrm{O}_{0-8}$ ) and 5 module identification inputs ( $\overline{\mathrm{MID}}_{0-4}$ ) at the rear, for selecting 16 addresses. Because 8 are used as output stages (with even second digit e.g. 162), the remaining 8 addresses can be used as internal places (with odd second digit e.g. 172).


Fig. 2 Block diagram of the output module.
The circuit is built on an epoxy-glass printed-wiring board of $233,4 \mathrm{~mm} \times 160 \mathrm{~mm}$ (Euro-card system). The board is provided with two F068-I connectors (board parts), the corresponding panel parts are available too, but should be ordered additionally: 242202589291 (with wire-wrap pins), 2422025 89299 (with dip-solder pins), or 242202589327 (with solder tags). For a general description of the Euro-card system see IEC 297 or DIN 41494 for 19-in racks and IEC 130-14 or DIN 41612 for connectors.

## ELECTRICAL DATA

## Supply

| Supply voltage (d.c.) | logic | $V_{P}$ | $5 \mathrm{~V} \pm 5 \%$ |
| :---: | :---: | :---: | :---: |
| Supply current |  | IP | typ 0,75 A |
| Supply voltage (d.c.) | for | $\mathrm{v}_{\text {S }}$ | $24 \mathrm{~V} \pm 25 \%$ |
| Supply current (excluding load current) | output circuitry | Is | typ 0,1 A |

## Input data

All inputs meet the standard TTL specification except the CLCO-input.

| input | function | load | terminations of connector 1 (Fig.3) |  |
| :---: | :---: | :---: | :---: | :---: |
| $\mathrm{ABCIO}_{0}$ |  | 1 TTL | a2, | c2 |
| $\mathrm{ABCIO}_{1}$ |  | 1 TTL | a4, | c4 |
| $\mathrm{ABCIO}_{2}$ |  | 1 TTL | a6, | c6 |
| $\mathrm{ABCIO}_{3}$ | address bits from central processor; | 1 TTL | a8, | c8 |
| $\mathrm{ABClO}_{4}$ | $A B C 1 O_{0-3}$ select the output stage, | 1 TTL | a10 |  |
| $\mathrm{ABCIO}_{5}$ | $\mathrm{ABClO}_{4-8}$ select the output module. | 1 TTL | a12 |  |
| $\mathrm{ABCIO}_{6}$ |  | 1 TTL | a14 |  |
| $\mathrm{ABCIO}_{7}$ |  | 1 TTL | a16 |  |
| $\mathrm{ABCIO}_{8}$ |  | 1 TTL | a18 |  |
| DBCO | Data bit from central processor; data are stored in output stage by CLCO. | 1 TTL | a22 |  |
| MIN | Module inhibit signal from external source; a low level applied to this input inhibits data on DBCO to be stored in the output stage. | 2 TTL |  | c26 |
| REO | Reset output module line; a low level on this input will reset all output latches (output transistor non-conducting). | 1 TTL | a24 |  |
| $\overline{\mathrm{MID}} 0$ |  | 2 TTL |  | c10 |
| MID 1 |  | 2 TTL |  | c12 |
| $\overline{\mathrm{MID}}{ }_{2}$ | module with individual identity. | 2 TTL |  | c14 |
| $\overline{\mathrm{MID}}_{3}$ |  | 2 TTL |  | c16 |
| $\overline{\mathrm{MID}} 4$ |  | 2 TTL |  | c18 |
| CLCO * | Clock signal from central processor to output module, stores data on DBCO into output stage during input/output cycle. | * | a28 |  |

[^14]
## Output data

The data outputs are $\mathrm{DO}_{\mathrm{XY}}$ to $\mathrm{DO}_{\mathrm{XY7}}$ ( Y is always even). They are accessible on connector 2, see terminal location.
Output transistor conducting: $\mathrm{V}_{\mathrm{a}-\mathrm{c}}{ }^{*}=\max .2,53 \mathrm{~V}$ at output current $\left(\mathrm{I}_{\mathrm{O}}\right)$ is 2 A .
Output transistor non-conducting: $\mathrm{I}_{\mathrm{O}}=\max .10 \mu \mathrm{~A}$ at $\mathrm{V}_{\mathrm{a}-\mathrm{c}}{ }^{*}$ is 30 V .
Maximum load inductance ( $L_{\text {max }}$ )
Maximum switching frequency at maximum output current (I Omax)

Table 1

| $\mathrm{O}_{\mathrm{O}}$ | $\mathrm{L}_{\text {max }}$ <br> mH |
| :---: | ---: |
| 2,0 | 50 |
| 1,8 | 60 |
| 1,6 | 80 |
| 1,4 | 100 |
| 1,2 | 140 |
| 1,0 | 200 |
| 0,8 | 310 |
| 0,6 | 560 |
| 0,4 | 1300 |
| 0,2 | 5000 |
| 0,1 | 20000 |

Output current at operation with forced air cooling of $1 \mathrm{~m} / \mathrm{s}$, for all stages
max. 2 A per stage
Output current at operation without forced air cooling
for all stages max. 0,915 A per stage
for maximum 4 stages
Short-circuit protection trip level
max. 2 A per stage
2,16 A

The output (open collector) meets the standard TTL specifications

| output | function | loadability | terminations of <br> connector 1 (Fig.3) |
| :--- | :--- | :--- | :--- |
| IDLC | Identification signal from last output module <br> to central processor (active HIGH); only the <br> IDLC output of the last output module has <br> to be connected with the IDLC input of the <br> central processor. | 2 TTL | a26 |

[^15]
## MECHANICAL DATA

## Outlines



Fig. 3 The LEDs identified with * are for status indication, those identified with ** are for shortcircuit indication.

[^16]Terminal location
connector 1

| row c |  | row a |
| :---: | :---: | :---: |
| $\mathrm{ABCIO}_{0}$ | 2 | $\mathrm{ABCIO}_{0}$ |
| $\mathrm{ABCIO}_{1}$ | 4 | $\mathrm{ABCIO}_{1}$ |
| $\mathrm{ABCIO}_{2}$ | 6 | $\mathrm{ABClO}_{2}$ |
| $\mathrm{ABCIO}_{3}$ | 8 | $\mathrm{ABClO}_{3}$ |
| $\mathrm{MID}_{0}$ | 10 | $\mathrm{ABClO}_{4}$ |
| $\overline{\mathrm{MID}} 1$ | 12 | $\mathrm{ABCIO}_{5}$ |
| $\overline{\mathrm{MID}}_{2}$ | 14 | $\mathrm{ABCIO}_{6}$ |
| $\overline{\mathrm{MID}}_{3}$ | 16 | $\mathrm{ABClO}_{7}$ |
| $\overline{\mathrm{MID}}_{4}$ | 18 | $\mathrm{ABCIO}_{8}$ |
| 0 V (note 1) | 20 | n.c. |
| 0 V (note 1) | 22 | DBCO |
| n.c. | 24 | REO |
| MIN | 26 | IDLC |
| 0 V (note 2) | 28 | CLCO |
| $V_{p}$ | 30 | $V_{p}$ |
| 0 V | 32 | 0 V |

connector 2

| row c |  |  | row a |
| :---: | :---: | :---: | :---: |
| 0 V |  | 2 | DOXYO |
| 0 V |  | 4 | DOXY1 |
| 0 V |  | 6 | DOXY2 |
| 0 V | (note 3) | 8 | DOXY3 |
| 0 V | (note 3) | 10 | DOXY4 |
| 0 V |  | 12 | DOXY5 |
| 0 V |  | 14 | DOXY6 |
| 0 V |  | 16 | DOXY7 |
| i.c. |  | 18 | i.c. |
| i.c. |  | 20 | i.c. |
| i.c. |  | 22 | i.c. |
| n.c. |  | 24 | n.c. |
| i.c. |  | 26 | n.c. |
| n.c. |  | 28 | n.c. |
| n.c. |  | 30 | n.c. |
| $\mathrm{V}_{\mathrm{S}}$ |  | 32 | $\mathrm{V}_{S}$ |

n.c. $=$ not connected.
i.c. $=$ internally connected.

## Notes

1. No supply line; only to be used for coding of the $\overline{\mathrm{MID}_{0}-4 \text { lines. }}$
2. No supply line; only to be used as a ground connection for CLCO.
3. 0 -line of $\mathrm{V}_{\mathrm{S}}$.

## PUNCH AND TELETYPE INTERFACE MODULE

## DESCRIPTION

This punch and teletype interface module is intended for use in a PLC system to enable the user to make a hard copy of the program.
For this purpose, the CP10 or CP11 central processor module must be replaced by the PI10 in the operating PLC system. Connections to the hard copy equipment can de done via two F161 connectors in the front panel. The upper (connector 4, female, 25 pins) is for the TTY which supplies data in a serial form including start and stop bits according to standard RS232C. The lower (connector 3, female, 15 pins) is for the punch which supplies data in a parallel form (TTL-level). Both data are in ASCII code including parity-bit. The module is also provided with "start" and "reset" pushbuttons and a "ready" indication. The latter is ON as soon as the power supply is switched-on. When "start" is pushed it extinguishes and relights as soon as the read-out has been completed or when "reset" is pushed.
Data output is approx. 9 characters per second, adjusted for normal TTY operation. If higher speeds are required, e.g. for a fast punch, a resistor Rp can be inserted between two solder-pins on the board, marked "a" and "b" (see Fig. 3; maximum 29 characters/s possible).
The punch and teletype interface module is built on an epoxy glass printed-wiring board of $233,4 \mathrm{~mm}$ $\times 160 \mathrm{~mm}$ (Eurocard system). The board is provided with two F068-I connectors (board parts) to fit in the place of a CP10 or CP11.

## ELECTRICAL DATA

## Supply

Voltage (d.c.) $\quad V_{P} 5 \mathrm{~V} \pm 5 \%$
Current
Ip typ. 1,5 A

## Input data

All inputs meet the standard TTL-specifications.


## Output data

Outputs to PLC system (rear side).
All outputs meet the standard TTL specifications.

| output | function | loadability | terminations (Fig. 5) |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | connector 1 | connector 2 |  |
| $\mathrm{ABCM}_{0}$ $\mathrm{ABCM}_{1}$ <br> $\mathrm{ABCM}_{2}$ <br> $\mathrm{ABCM}_{3}$ <br> $\mathrm{ABCM}_{4}$ <br> $\mathrm{ABCM}_{5}$ <br> $\mathrm{ABCM}_{6}$ <br> $\mathrm{ABCM}_{7}$ <br> $\mathrm{ABCM}_{8}$ <br> ABCM9 | Address bits to program memory. | 9 TTL 9 TTL 9 TTL 9 TTL 9 TTL 9 TTL 9 TTL 9 TTL 9 TTL 9 TTL |  | $\begin{aligned} & \text { a20, } \\ & \text { a21, } \\ & \text { a22, } \\ & \text { a23, } \\ & \text { a24, } \\ & \text { a25, } \\ & \text { a26, } \\ & \text { a27, } \\ & \text { a28, } \\ & \text { a29, } \end{aligned}$ | $\begin{aligned} & \mathrm{c} 20 \\ & \mathrm{c} 21 \\ & \mathrm{c} 22 \\ & \mathrm{c} 23 \\ & \mathrm{c} 24 \\ & \mathrm{c} 25 \\ & \mathrm{c} 26 \\ & \mathrm{c} 27 \\ & \mathrm{c} 28 \\ & \mathrm{c} 29 \end{aligned}$ |
| ENCM 1 <br> $\mathrm{ENCM}_{2}$ <br> $\mathrm{ENCM}_{3}$ <br> $\mathrm{ENCM}_{4}$ | Enable signal to program memory; four lines are necessary when program memory capacity is extended to 4 k . | $\begin{aligned} & 10 \mathrm{TTL} \\ & 10 \mathrm{TTL} \\ & 10 \mathrm{TTL} \\ & 10 \mathrm{TTL} \end{aligned}$ | $\begin{aligned} & \text { a1 } \\ & \text { a2 } \\ & \text { a3 } \\ & \text { a4 } \end{aligned}$ |  |  |
| SCCM | Store command to program memory. This terminal is directly connected to 0 V on punch/teletype interface, forcing the program memory into "read" operation. |  |  | a17, | c17 |
| $\frac{\mathrm{CICM}}{\mathrm{CICM}}$ | Cycle initiate signal to program memory (bipolar to reduce noise sensitivity). | $\begin{array}{\|c\|} \hline 10 \mathrm{TTL} \\ 9 \mathrm{TTL} \end{array}$ |  | $\begin{aligned} & \text { a19, } \\ & \text { a18, } \end{aligned}$ | $\begin{aligned} & \text { c19 } \\ & \text { c18 } \end{aligned}$ |

## Output data (continued)

Outputs to hard copy equipment (front panel).
All outputs of connector 3 meet the standard TTL specifications. The output of connector 4 meets the standard RS232C specification.

| output | function | loadability | termination (Fig. 5) |  |
| :---: | :---: | :---: | :---: | :---: |
|  |  |  | connector 3 | connector 4 |
| $\begin{aligned} & \mathrm{TB}_{1} \\ & \mathrm{~TB}_{2} \\ & \mathrm{~TB}_{3} \\ & \mathrm{~TB}_{4} \\ & \mathrm{~TB}_{5} \\ & \mathrm{~TB}_{6} \end{aligned}$ | Tape bits performing ASCII code. | 10 TTL 10 TTL 10 TTL 10 TTL 10 TTL 10 TTL | $\begin{aligned} & 1 \\ & 2 \\ & 3 \\ & 4 \\ & 5 \\ & 6 \end{aligned}$ |  |
| TB7 | Directly connected to 0 V . |  | 7 |  |
| TB8 | Parity bit *. | 10 TTL | 8 |  |
| $\begin{aligned} & \text { STROBE } \\ & \hline \text { STROBE } \end{aligned}$ | Start signal to punch (data on $\mathrm{TB}_{1-8}$ ready). | $\begin{aligned} & 10 \mathrm{TTL} \\ & 10 \mathrm{TTL} \end{aligned}$ | $\begin{array}{r} 9 \\ 10 \end{array}$ |  |
| HIGH | Constant HIGH level (directly connected to $\mathrm{V}_{\mathrm{p}}$ ). |  | 12 |  |
| 0 V | Signal ground (directly connected to 0 V ). |  | 15 |  |
| DO | Data output (RS232C). |  |  | 3 |
| 0 V | Signal ground (directly connected to 0 V ). |  |  | 7 |

[^17]TIME DATA
Parallel output

$t_{1}$ STROBE pulse duration
$t_{2}$ DATA valid before STROBE pulse
$t_{3}$ depending on $R_{P}$
$2 \mathrm{~ms} \pm 20 \%$
$\min .10 \mu \mathrm{~s}$
9 characters/s $\left(R_{p}=\infty\right)$
29 characters/s $\left(R_{p}=8 \mathrm{k} \Omega\right)$

Fig. 1.

## Serial output



Fig. 2.
approx. 9 characters/s $\left(R_{p}=\infty\right)$


Fig. 3 Required $R_{p}$ as a function of print/punch speed (number of characters per second).

## APPLICATION INFORMATION

If the user wants to have only a part of the program dumped, he can preset the starting point by means of three switches on the PC board; see Figs 4 and 5. Termination of the read-out can be achieved by pressing the "reset" button.

| start with <br> line number | preset switch |  |  |
| :---: | :---: | :---: | :---: |
|  | 4 | 2 | 1 |
| 0000 | L | L | L |
| 1000 | L | L | H |
| 2000 | H | L |  |
| 300 | H | H |  |
| 4000 | H | L | L |
| 5000 | H | L | H |
| 6000 | H | H | L |
| 7000 | H | H | H |



Fig. 4.

## Punch format

After pressing the "start" button, the module will generate "tape feed" 56 times. Hereafter, the line number followed by "space", the program word, "enter", 'step", 'carriage return" and 'line feed" will be punched. This cycle, consisting of 14 characters, is repeated, starting with the next line number. After the addresses 1777, 3777, 5777 and 7777, other sections of 56 times "tape-feed" will be inserted.

## Teletype format

The same characters as mentioned above are sent to the TTY, producing the following print out:

|  | (line) | (space) | (program word) | (enter) | (step) |
| :---: | :---: | :---: | :---: | :---: | :---: |
| e.g. | 3271 |  | 1.401 | $>$ | $<$ |
|  | 3272 |  | $* 2.130$ | $>$ | $<$ |
|  | 3273 |  | $* 0.740$ | $>$ | $<$ |



Fig. 5.

Punch and teletype interface module

Terminal location

| connector 1 |  |  | connector 2 |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| row c |  | row a | row c |  | row a |
| n.c. | 1 | $\mathrm{ENCM}_{1}$ | n.c. | 1 | n.c. |
| n.c. | 2 | $\mathrm{ENCM}_{2}$ | PBMCP0 | 2 | $\mathrm{PBMCP}_{0}$ |
| n.c. | 3 | $\mathrm{ENCM}_{3}$ | $\mathrm{PBMCP}_{1}$ | 3 | $\mathrm{PBMCP}_{1}$ |
| n.c. | 4 | $\mathrm{ENCM}_{4}$ | $\mathrm{PBMCP}_{2}$ | 4 | $\mathrm{PBMCP}_{2}$ |
| n.c. | 5 | MICC | $\mathrm{PBMCP}_{3}$ | 5 | $\mathrm{PBMCP}_{3}$ |
| n.c. | 6 | n.c. | $\mathrm{PBMCP}_{4}$ | 6 | $\mathrm{PBMCP}_{4}$ |
| n.c. | 7 | n.c. | $\mathrm{PBMCP}_{5}$ | 7 | $\mathrm{PBMCP}_{5}$ |
| n.c. | 8 | n.c. | $\mathrm{PBMCP}_{6}$ | 8 | $\mathrm{PBMCP}_{6}$ |
| n.c. | 9 | n.c. | $\mathrm{PBMCP}_{7}$ | 9 | $\mathrm{PBMCP}_{7}$ |
| n.c. | 10 | n.c. | PBMCP8 | 10 | PBMCP8 |
| n.c. | 11 | n.c. | PBMCP9 | 11 | PBMCP9 |
| n.c. | 12 | n.c. | PBMCP10 | 12 | PBMCP 10 |
| n.c. | 13 | n.c. | PBMCP11 | 13 | PBMCP 11 |
| n.c. | 14 | n.c. | PBMCP 12 | 14 | PBMCP 12 |
| n.c. | 15 | n.c. | n.c. | 15 | n.c. |
| n.c. | 16 | n.c. | n.c. | 16 | n.c. |
| n.c. | 17 | n.c. | SCCM | 17 | SCCM |
| n.c. | 18 | n.c. | $\overline{\text { CICM }}$ | 18 | $\overline{\text { CICM }}$ |
| n.c. | 19 | n.c. | CICM | 19 | CICM |
| n.c. | 20 | n.c. | $\mathrm{ABCM}_{0}$ | 20 | $\mathrm{ABCM}_{0}$ |
| n.c. | 21 | n.c. | $\mathrm{ABCM}_{1}$ | 21 | $\mathrm{ABCM}_{1}$ |
| n.c. | 22 | n.c. | $\mathrm{ABCM}_{2}$ | 22 | $\mathrm{ABCM}_{2}$ |
| n.c. | 23 | n.c. | $\mathrm{ABCM}_{3}$ | 23 | $\mathrm{ABCM}_{3}$ |
| n.c. | 24 | n.c. | $\mathrm{ABCM}_{4}$ | 24 | $\mathrm{ABCM}_{4}$ |
| n.c. | 25 | n.c. | $\mathrm{ABCM}_{5}$ | 25 | $\mathrm{ABCM}_{5}$ |
| n.c. | 26 | n.c. | $\mathrm{ABCM}_{6}$ | 26 | $\mathrm{ABCM}_{6}$ |
| n.c. | 27 | n.c. | $\mathrm{ABCM}_{7}$ | 27 | $\mathrm{ABCM}_{7}$ |
| n.c. | 28 | n.c. | $\mathrm{ABCM}_{8}$ | 28 | $\mathrm{ABCM}_{8}$ |
| n.c. | 29 | n.c. | ABCMg | 29 | $\mathrm{ABCM}_{9}$ |
| n.c. | 30 | n.c. | n.c. | 30 | n.c. |
| $V_{p}$ | 31 | $V_{p}$ | $V_{P}$ | 31 | $V_{P}$ |
| 0 V | 32 | 0 V | 0 V | 32 | 0 V |

n.c. $=$ not connected

Terminal location (continued)

connector 4

|  |  | $\bullet$ | 13 | n.c. |
| :--- | :--- | :--- | :--- | :--- |
| n.c. | 25 | $\bullet$ | 12 | n.c. |
| n.c. | 24 | $\bullet$ | 11 | n.c. |
| n.c. | 23 | $\bullet$ | 10 | n.c. |
| n.c. | 22 | $\bullet$ | 9 | n.c. |
| n.c. | 21 | $\bullet$ | n.c. |  |
| n.c. | 20 | $\bullet$ | 7 | 0 V |
| n.c. | 19 | $\bullet$ | n.c. |  |
| n.c. | 18 | $\bullet$ | 5 | n.c. |
| n.c. | 17 | $\bullet$ | 4 | n.c. |
| n.c. | 16 | $\bullet$ | 3 | DO |
| n.c. | 15 | $\bullet$ | 2 | n.c. |
| n.c. | 14 | $\bullet$ | 1 | n.c. |

n.c. $=$ not connected

* No supply line, only to be used as signal ground.
** No supply line, only to be used as fixed HIGH level.


## PROGRAMMING UNIT

## DESCRIPTION

The programming unit is intended for use in combination with the central processor CP10 (or CP11), input module IM10 (or IM11 or LX10), memory module MM10 (or MM11 or MM12) and output module OM10 (or OM12) to assemble a programmable logic controller (PLC). The control program is written into the program memory with the aid of this unit, by means of the built-in keyboard, or from a punched tape.
The unit can also be used to read the contents of the program memory: eight seven-segments LED displays show the program line number (memory address) and the program word belonging to it. Each program word contains a scratch-pad memory address; the content of this address ( 1 or 0 ) is indicated by the status indicator LED.

Programming a system by means of the keyboard (or a punched tape) is only possible when the key switch of the programming unit is set to the on position. The key switch determines the authority of the unit: with a key the user has the complete command of the PLC, without a key he can only monitor its actions.

The keyboard comprises 13 keys (Fig. 3) :

- 9 keys, marked 0 to 7 and $*$, with which the program word is typed in;
- 1 key, marked ENTER; by pressing this key the displayed program word is transferred to the program memory. As soon as the key is released the program memory is set to the read mode; the programming unit reads the contents of the program memory and the program word is again displayed as a check that it is written correctly into the program memory.
- 1 key marked STEP; by pressing this key the next memory address is selected. Each time this key is pressed the line number is incremented by one.
- 1 key, marked CIRC, a repetitive STEP key; by pressing this key the line number is incremented continuously with a frequency of approx. 50 Hz .
- 1 key, marked DECR; by pressing this key simultaneously with either the STEP or CIRC keys, the line number is decremented by one or continuously respectively.

When the key switch is in the off position only the STEP, CIRC and DECR keys are operative. When selecting a particular address by means of these keys, the program word is displayed and the status of the scratch-pad memory address specified in the program word is indicated. In this way the PLC can be monitored without disrupting the working system.

If a punched tape is used, it must be coded according to the ASCII code. The characters to be used for the ENTER and the STEP commands are > and < respectively.
The unit is so constructed that it can be plugged into the PLC; after loading the program into the memory module the PU10 can be removed to be used in another PLC system.


Fig. 1. Simplified block diagram of the programming unit.
The circuit is built on two epoxy-glass printed-wiring boards, mounted in a metal housing, which fits into the Euro-card system. The unit is provided with two F068-I connectors (board parts); the corresponding panel parts are available under catalogue number 2422 02589291 (pins for wire wrap), 242202589299 (pins for dip soldering) or 242202589327 (solder tags) ${ }^{1}$ ).

[^18]
## ELECTRICAL DATA

Supply
Supply voltage (d.c.)
current

$$
\begin{array}{ll}
\mathrm{V}_{\mathrm{p}} & 5 \mathrm{~V} \pm 5 \% \\
\mathrm{I}_{\mathrm{p}} & \text { max. } 2 \mathrm{~A} \\
& \text { typ. } 1,8 \mathrm{~A}
\end{array}
$$

Input data
All inputs meet the standard TTL specifications.

| input | function | load | terminations (Fig. 2) |  |
| :---: | :---: | :---: | :---: | :---: |
|  |  |  | connector 1 | connector 2 |
| $\mathrm{PBMCP}_{0}$ <br> $\mathrm{PBMCP}_{1}$ <br> $\mathrm{PBMCP}_{2}$ <br> $\mathrm{PBMCP}_{3}$ <br> $\mathrm{PBMCP}_{4}$ <br> $\mathrm{PBMCP}_{5}$ <br> PBMCP $_{6}$ <br> $\mathrm{PBMCP}_{7}$ <br> $\mathrm{PBMCP}_{8}$ <br> $\mathrm{PBMCP}_{9}$ <br> PBMCP $_{10}$ <br> PBMCP $_{11}$ <br> PBMCP $_{12}$ | Program word bits from program memory. | $\begin{array}{ll} 1 & \mathrm{TTL} \\ 1 & \mathrm{TTL} \\ 1 & \mathrm{TTL} \\ 1 & \mathrm{TTL} \\ 1 & \mathrm{TTL} \\ 1 & \mathrm{TTL} \\ 1 & \mathrm{TTL} \\ 1 & \mathrm{TTL} \\ 1 & \mathrm{TTL} \\ 1 & \mathrm{TTL} \\ 1 & \mathrm{TTL} \\ 1 & \mathrm{TTL} \\ 1 & \mathrm{TTL} \end{array}$ |  | a2 c 2 <br> a 4 c 4 <br> a 6 c 6 <br> a 8 c 8 <br> a 10 c 10 <br> a 12 c 12 <br>  c 14 |
| LDCP | Synchronization input from central processor; synchronizes auxiliary address counter in programming unit with address counter in central processor. | 1 TTL | a 14 |  |
| $\overline{\mathrm{CL}}_{2} 3$ | Inverted clock input from central processor. | 1 TTL | cl6 |  |
| $\phi 57$ | Clock signal for status indication from central processor. | 1 TTL |  | c 16 |
| SBCP | Status bit from central processor; clocked by $\phi_{57}$ it indicates state 1 or 0 at selected scratch-pad memory address. | 1 TTL | a 16 |  |
| $\begin{aligned} & \mathrm{TB}_{1} \\ & \mathrm{~TB}_{2} \\ & \mathrm{~TB}_{3} \\ & \mathrm{~TB}_{4} \\ & \mathrm{~TB}_{5} \\ & \mathrm{~TB}_{6} \\ & \mathrm{~TB} 7 \end{aligned}$ | Tape bits (ASCII code) from tape reader | 2 TTL |   <br> a18 c18 <br> a20 c20 <br> a22 c22 <br>  c24 |  |


| input | function | load | terminations (Fig. 2) |  |
| :--- | :--- | :---: | :---: | :---: |
|  |  |  | connector 1 | connector 2 |
| STROBE | Signal from tape-reader sprocket. | 2 TTL | a24 |  |
| SLTP | Selection signal from tape reader or <br> external switch; if tape reader is <br> used the input must be connected to <br> the logic LOW level. | 2 TTL |  |  |

Output data
All outputs meet the standard TTL specifications.

| output | function | loadability | terminations (Fig. 2) |  |
| :---: | :---: | :---: | :---: | :---: |
|  |  |  | connector 1 | connector 2 |
| $\mathrm{PBPM}_{0}$ $\mathrm{PBPM}_{1}$ $\mathrm{PBPM}_{2}$ $\mathrm{PBPM}_{3}$ $\mathrm{PBPM}_{4}$ $\mathrm{PBPM}_{5}$ $\mathrm{PBPM}_{6}$ $\mathrm{PBPM}_{7}$ $\mathrm{PBPM}_{8}$ $\mathrm{PBPM}_{9}$ PBPM $_{10}$ PBPM $_{11}$ PBPM $_{12}$ | Program word bits to program memory, | 9 TTL <br> 9 TTL <br> 9 TTL <br> 9 TTL <br> 9 TTL <br> 9 TTL <br> 9 TTL <br> 9 TTL <br> 9 TTL <br> 9 TTL <br> 9 TTL <br> 9 TTL <br> 9 TTL | a2 c 2 <br> a4 c 4 <br> a6 c 6 <br> a8 c 8 <br> a 10 c 10 <br> a 12 c 12 <br>  c 14 |  |
| $\begin{aligned} & \overline{\mathrm{ABP}}_{0} \\ & \overline{\mathrm{ABP}}_{1} \\ & \overline{\mathrm{ABP}}_{2} \\ & \overline{\mathrm{ABP}}_{3} \\ & \overline{\mathrm{ABP}}_{4} \\ & \overline{\mathrm{ABP}}_{5} \\ & \overline{\mathrm{ABP}}_{6} \\ & \overline{\mathrm{ABP}}_{7} \\ & \overline{\mathrm{ABP}}_{8} \\ & \overline{\mathrm{ABP}}_{9} \mathrm{ABP}_{10} \\ & \overline{\mathrm{ABPP}}_{11} \end{aligned}$ | Inverted address bits (line number bits to external printer). | 10 TTL 10 TTL 10 TTL 10 TTL 10 TTL 10 TTL 10 TTL 10 TTL 10 TTL 10 TTL 10 TTL 10 TTL |  |  c18 <br> a18 c20 <br> a20  <br> a22 c22 <br> a24 c24 <br> a26 c26 <br> a28 c28 |
| READY | Signal indicating that contents of program memory address counter agrees with line number. | 10 TTL |  | a16 |


| output | function | loada- <br> bility | terminations (Fig. 2) |  |
| :--- | :--- | :--- | :--- | :--- |
|  |  |  | connector 1 | connector 2 |
| SCPC | Store command to central processor. | 10 TTL |  | al4 |
| BSP | Busy signal to external tape reader; <br> the output becomes LOW when a <br> correct code has been recognized, <br> and becomes HIGH when this code <br> has been stored. | 10 TTL | c 26 |  |
| $\overline{\overline{\mathrm{BSP}}}$ | Inverted BSP. | 10 TTL | a 26 |  |

Time data
If a tape reader is used for loading the control program into the program memory the following considerations have to be taken in account.

Delay time between the level
changes on TB 1-7 and strobe signal
Delay time between leading edge of strobe pulse and code recognition on BSP
Strobe pulse duration
$\mathrm{t}_{1} \min .0 \mathrm{~ns}$
$\mathrm{t}_{2} \max .500 \mathrm{~ns}$
$\mathrm{t}_{\mathrm{s}} \quad \min .2 \mu \mathrm{~s}$
$\max . \quad 10 \mathrm{~ms}$

BSP becomes LOW when a correct code has been recognized and HIGH when this code has been stored. At this moment the tape reader can be started to give the next code.


Fig. 2


REAR VIEW


Fig. 3

Mass
Terminal location
connector 1

| row c |  | row a |
| :---: | :---: | :---: |
| $\mathrm{PBPM}_{0}$ | 2 | $\mathrm{PBPM}_{1}$ |
| $\mathrm{PBPM}_{2}$ | 4 | $\mathrm{PBPM}_{3}$ |
| $\mathrm{PBPM}_{4}$ | 6 | PBPM 5 |
| $\mathrm{PBPM}_{6}$ | 8 | $\mathrm{PBPM}_{7}$ |
| $\mathrm{PBPM}_{8}$ | 10 | PBPM9 |
| $\mathrm{PBPM}_{10}$ | 12 | $\mathrm{PBPM}_{11}$ |
| $\mathrm{PBPM}_{12}$ | 14 | LDCP |
| $\mathrm{CL}_{2} 3$ | 16 | SBCP |
| TB1 | 18 | TB2 |
| TB3 | 20 | TB4 |
| TB5 | 22 | TB6 |
| $\mathrm{TB}_{7}$ | 24 | STROBE |
| BSP | 26 | $\overline{\mathrm{BSP}}$ |
| SLTP | 28 | n.c. |
| Vp | 30 | Vp |
| 0 V | 32 | 0 V |

connector 2

| row c |  | row a |
| :--- | :--- | :--- |
| $\mathrm{PBMCP}_{0}$ | 2 | $\mathrm{PBMCP}_{1}$ |
| $\mathrm{PBMCP}_{2}$ | 4 | $\mathrm{PBMCP}_{3}$ |
| $\mathrm{PBMCP}_{4}$ | 6 | $\mathrm{PBMCP}_{5}$ |
| $\mathrm{PBMCP}_{6}$ | 8 | $\mathrm{PBMCP}_{7}$ |
| $\mathrm{PBMCP}_{8}$ | 10 | $\mathrm{PBMCP}_{9}$ |
| $\mathrm{PBMCP}_{10}$ | 12 | $\mathrm{PBMCP}_{11}$ |
| $\mathrm{PBMCP}_{12}$ | 14 | $\mathrm{SCPC}^{2}$ |
| $\phi_{57}$ | 16 | READY |
| $\overline{\mathrm{ABP}}_{0}$ | 18 | $\overline{\mathrm{ABP}}_{1}$ |
| $\overline{\mathrm{ABP}}_{2}$ | 20 | $\overline{\mathrm{ABP}}_{3}$ |
| $\overline{\mathrm{ABP}}_{4}$ | 22 | $\overline{\mathrm{ABP}} 5_{5}^{\mathrm{ABP}} 6$ |

n.c. = not connected.

## BACK PANELS

## APPLICATION

Back panels BP11 to BP16 are designed for use as mother boards in 19 -inch racks in the PLC system. Use of these panels removes the work of wiring separate connectors to receive the modules. The range avoids system redundancy and allows the rack space to be fully utilized.

## DESCRIPTION

The back panels are equipped with female connectors, matching the male counterparts of the PLC modules. They have solder bridges for determining the addresses of an input/output/LX10 module (MID), the addresses of the MM modules (ENCM), the last IM/OM module or cycle time (IDLC), the last MM module (MICC), and connecting blocks for external connections.
Types BP11 to BP14 each consist of two back panels. The upper panel provides the required interconnections for connector 1 of each PLC module. The lower panel provides the interconnections for connector 2 of each MM, PU and CP module (see Figs 1 to 4). External connections are made to the lower connectors of the IM, OM and LX10 modules; these must be received by the separately mounted female connectors.

As the layout of the panels depends on the number of MM modules used, four different types have been developed. Table 1 surveys the various back panels and the type and number of each module which can be placed in the rack. Since a greater number of MM modules generally requires a greater number of IM/OM modules, need will be felt for an extension rack to accommodate these extra modules. Two back panel types are available for this purpose: the BP15 is for $15 \mathrm{IM} / \mathrm{OM}$ modules; the BP16 is for 21. These, of course, are only upper back panels.

Table 1 Back panels

| no. of <br> MM <br> modules | no. of <br> IM/OM/LX* <br> modules | no. of <br> CP <br> modules | no. of <br> PU <br> modules | type of <br> back <br> panel | catalogue <br> number |
| :--- | :--- | :--- | :--- | :--- | :--- |
| 1 | 13 | 1 | 1 | BP11 | 30112 |
| 2 | 11 | 1 | 1 | BP12 | 40112 |
| 3 | 9 | 1 | 1 | BP13 | 50112 |
| 4 | 7 | 1 | 1 | BP14 | 60112 |
| - | $21^{* *}$ | - | - | BP15 | 70112 |
| - | - | - | BP16 | 80112 |  |

The back panels are screwed to the rack by M2,5 screws, using threaded rails and isolation strips.

[^19]

Fig. 1 Back panel BP11.
IM = input module
OM = output module
LX = load external interface module
CP = central processor
PU = programming unit
$M M=$ program memory module
$\left.\begin{array}{ll}+ & =+5 \mathrm{~V} \pm 5 \% \\ - & =0 \mathrm{~V}\end{array}\right\}$ supply voltage
$\mathrm{V}_{\mathrm{B}}=+4,5 \mathrm{~V}$ to $+7,5 \mathrm{~V}$ (battery voltage)
Data bus cable is only used for connecting a BP15 or BP16 panel.



Fig. 2 Back panel BP12.
IM = input module
OM = output module
LX = load external interface module
CP = central processor
PU = programming unit
MM = program memory module
$\left.\begin{array}{ll}+=+5 \mathrm{~V} \pm 5 \% \\ -\quad=0 \mathrm{~V}\end{array}\right\}$ supply voltage
$\mathrm{V}_{\mathrm{B}}=+4,5 \mathrm{~V}$ to $+7,5 \mathrm{~V}$ (battery voltage)
Data bus cable is only used for connecting a BP15 or BP16 panel.

| $\bigcirc$ | $\bigcirc$ | $\bigcirc$ | $\bigcirc$ |
| :---: | :---: | :---: | :---: |
| - | $\bullet$ | $\bullet$ | - |
| : | -• | ! | ! |
| ! |  |  | ! |
| ! ! | - |  | ! ! |
| ! |  |  | ! |
| : | - |  |  |
| ! |  |  |  |
| ! |  |  |  |
| ! |  |  |  |
| ! |  |  |  |
|  |  |  |  |
| $\bigcirc$ | $\bigcirc$ | $\bigcirc$ | $\bigcirc$ |

Fig. 3 Back panel BP13.
IM = input module
OM = output module
LX = load external interface module
CP = central processor
PU = programming unit
$\mathrm{MM}=$ program memory module
$\left.\begin{array}{l}+=+5 \mathrm{~V} \pm 5 \% \\ -\quad=0\end{array}\right\}$ supply voltage

$\mathrm{V}_{\mathrm{B}}=+4,5 \mathrm{~V}$ to $+7,5 \mathrm{~V}$ (battery voltage)
Data bus cable is only used for connecting a BP15 or BP16 panel.


Fig. 4 Back panel BP14.
IM = input module
OM = output module
LX = load external interface module
CP = central processor
$\mathrm{PU}=$ programming unit
$\mathrm{MM}=$ program memory module
$\left.\begin{array}{ll}+\quad=+5 \mathrm{~V} \pm 5 \% \\ - & =0 \mathrm{~V}\end{array}\right\}$ supply voltage
$\mathrm{V}_{\mathrm{B}}=+4,5 \mathrm{~V}$ to $+7,5 \mathrm{~V}$ (battery voltage)
Data bus cable is only used for connecting a BP15 or BP16 panel.




Each of the IM and OM modules has a discrete address so that the central processor can address each in turn during an input/output cycle. This address is formed by bridging the appropriate MID pad ( $\overline{\mathrm{MID}}_{0-4}$ ) and the adjacent 0 V pad (connected to connector 1, pin c22). Table 2 gives the address codes for the IM and OM modules. The $\overline{M I D}_{5}$ pad is not used.
If no LX modules are used, it is important to assign the $\overline{M I D}$ addresses to the IM and OM modules, so that the spare addresses, if any, are of a higher order than the used addresses. If this is not done, the input/output cycle will take longer than necessary. If no LX modules are inserted, the IDLC pad of the last IM/OM module (the one with the highest address) must be bridged to the adjacent r or n -shaped pad. If output modules are inserted at places IM/OM/LX2 and IM/OM/LX3, for instance, a logic LOW level applied via wires, connected to $\mathrm{REO}_{2}$ and $\mathrm{REO}_{3}$ of the connector block between places IM/OM/LX2 and IM/OM/LX1, will reset all the output latches in the relevant modules. Consequently the output transistors are driven in the non-conductive state. A logic LOW (inhibit) applied via wires connected to MIN $_{1}$ or MIN $_{2}$ of the same connector block, causes data from input modules (IM/LX) inserted at places IM/OM/LX1 or IM/OM/LX2 respectively, to be ignored by the central processor. It also prevents data stored during the preceding input/output cycle in output modules, inserted in the same places, from changing. If one or more LX modules are inserted, pin a25 automatically connects the IDLC line of the central processor to zero (maximum cycle time of $0,924 \mathrm{~ms}$ ). Removal of all LX modules will affect the $0,924 \mathrm{~ms}$ cycle time. As the maximum number of $L X$ modules in any one PLC system is 4 , only two MID pads are used for addressing (see Table 3).


Fig. 7 Detail of back panels BP11 to BP16. Note: $\overline{\mathrm{MID}}_{5}$ is normally not used.

Table 2 IM and OM module address codes

| $\overline{\mathrm{MID}} 0$ | $\overline{\mathrm{MID}}_{1}$ | $\overline{\mathrm{MID}}_{2}$ | $\overline{\mathrm{MID}}_{3}$ | $\overline{\mathrm{MID}}_{4}$ | input/output stage address - scratch-pad locations |
| :---: | :---: | :---: | :---: | :---: | :---: |
| - | - | - | - | - | 000 to 017 |
| 0 V | - | - | - | - | 020 to 037 |
| - | 0 V | - | - | - | 040 to 057 |
| 0 V | 0 V | - | - | - | 060 to 077 |
| - | - | 0 V | - | - | 100 to 117 |
| 0 V | - | 0 V | - | - | 120 to 137 |
| - | 0 V | 0 V | - | - | 140 to 157 |
| 0 V | 0 V | 0 V | - | - | 160 to 177 |
| - | - | - | 0 V | - | 200 to 217 |
| 0 V | - | - | 0 V | - | 220 to 237 |
| - | 0 V | - | 0 V | - | 240 to 257 |
| 0 V | 0 V | - | 0 V | - | 260 to 277 |
| - | - | 0 V | 0 V | - | 300 to 317 |
| 0 V | - | 0 V | 0 V | - | 320 to 337 |
| - | 0 V | 0 V | 0 V | - | 340 to 357 |
| 0 V | 0 V | 0 V | 0 V | - | 360 to 377 |
| - | - | - | - | 0 V | 400 to 417 |
| 0 V | - | - | - | 0 V | 420 to 437 |
| - | 0 V | - | - | 0 V | 440 to 457 |
| 0 V | 0 V | - | - | 0 V | 460 to 477 |
| - | - | 0 V | - | 0 V | 500 to 517 |
| OV | - | 0 V | - | 0 V | 520 to 537 |
| - | 0 V | 0 V | - | 0 V | 540 to 557 |
| 0 V | 0 V | 0 V | - | 0 V | 560 to 577 |
| - | - | - | 0 V | 0 V | 600 to 617 |
| 0 V | - | - | 0 V | 0 V | 620 to 637 |
| - | 0 V | - | 0 V | 0 V | 640 to 657 |
| 0 V | 0 V | - | 0 V | 0 V | 660 to 677 |
| - | - | 0 V | 0 V | 0 V | 700 to 717 |
| 0 V | - | 0 V | 0 V | 0 V | 720 to 737 |
| - | 0 V | 0 V | 0 V | 0 V | 740 to 757 |
| 0 V | OV | 0 V | 0 V | 0 V | 760 to 777 |

Table 3 LX module address codes

| $\overline{\mathrm{MID}}_{3}$ | $\overline{\mathrm{MID}}_{4}$ | address of eight-bit data source |
| :--- | :--- | :---: |
| $\overline{0}$ | - | $00 \circ$ to 17 o |
| $\overline{\mathrm{V}}$ | - | 20 o to 37 o |
| $\overline{0} \mathrm{~V}$ | OV | 40 o to 57 o |

Notes to Tables 2 and 3.

1. 0 V indicates that the $\overline{\text { MID }}$ terminal is connected to connector 1 , pin c22 $(0 \mathrm{~V})$.
2.     - indicates that the $\overline{\text { MID }}$ terminal is floating.
3. The least significant digit of each LX address is always 0 , e.g. 00 o to 170 in the table signifies addresses 00 o, 01o, 02o, 03 o etc., up to 17 o .

## Back panels

Fig. 8 shows the connector blocks on the back panels BP11 to BP14. The left-hand block contains connections for the $\mathrm{REO}_{1}$ wire and the MIN wire with the number of the highest IM/OM place $(13,11$, 9 or 7). A CLCP wire can be connected to the upper terminal, carrying a disable signal from external source (switch) to central processor (active LOW). The operation of this signal in combination with. the SPCE signal, carried by a wire connected to the lower terminal, is given in Table 4.
The right-hand connector block contains the output connection ALARM, which will become LOW when the supply voltage drops below $4,75 \mathrm{~V}$. The tape reader connections $\mathrm{TB}_{1}$ to $\mathrm{TB}_{7}$ and STROBE can be connected to the corresponding tape bit outputs of a tape reader. Connection BSP or $\overline{\mathrm{BSP}}$ must then be connected to the start/stop input of the tape reader. Connection SLTP must be switched to 0 V during tape reader programming and left floating during keyboard programming.

Fig. 8 Detail of back panels BP11 to BP14.

Table 4 Operation of CLCP and SPCE

| CLCP | SPCE | operation |
| :---: | :--- | :--- |
| 0 | $\mathrm{X}^{*}$ | The central processor is held at the <br> beginning of an input/output cycle. |
| $0 \rightarrow 1$ | 1 | The central processor is running. <br> The central processor starts running <br> at the beginning of an input/output <br> cycle. All scratch-pad locations, <br> except those corresponding to <br> inputs are reset to '0' during the <br> first input/output cycle. <br> All outputs from the PLC output <br> modules are passive after the first <br> input/output cycle. |
| $0 \rightarrow 1$ | 0 | The central processor starts running <br> at the beginning of an input/output <br> cycle. Any data existing in the <br> scratch-pad locations corresponding <br> to outputs determine the state of <br> the output stages in the output <br> modules during the first input/output <br> cycle. |



[^20]

Fig. 9 Detail of back panels BP12 to BP14.
$A=P R B ; B=S T A R T ; C=I N H ; D=M S I_{1} ; E=M S I_{2} ; F=+5 V, \pm 5 \% ; G=+5 V, \pm 5 \%$;
$\mathrm{H}=0 \mathrm{~V} ; \mathrm{I}=0 \mathrm{~V}$.
Pads 11 and 12 and connections $A$ to $E$ are used for program copying with the MM11 module.
ENCM $_{1-4}=$ enable signal from central processor to program memory;
MICC = memory identification signal derived from MM module in highest position;
PRB = program busy output signal to external equipment;
INH = inhibit input, when LOW the start input is inoperative;
MSI = mode selection inputs (see data sheets MM11).

Table 5 MM module address codes

| total byte content | number and type of MM modules | MM module position |  |  |  | pad pairs to be bridged |  | module position in which a ${ }_{1}$ must be connected with $\mathrm{a}_{2}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | 1 | 2 | 3 | 4 | MICC | ENCM |  |
| 1k | 1 MM10 |  |  |  |  | 1 |  |  |
|  | 1 MM12 |  |  |  |  | 1 |  |  |
| 2k | 2 MM10 |  |  |  |  | 2 | 6 |  |
|  | 2 MM12 |  |  |  |  | 2 | 6 | 12 |
|  | 1 MM12 |  |  |  |  | 2 | 5 |  |
| 3k | $3 \mathrm{MM10}$ |  |  |  |  | 3 | 68 |  |
|  | 3 MM12 |  |  |  |  | 3 | 68 | 123 |
|  | 2 MM12 |  |  |  |  | 3 | 579 |  |
| 4k | 4 MM10 |  |  |  |  | 4 | 6810 |  |
|  | 4 MM12 |  |  |  |  | 4 | 6810 | 1234 |
|  | 2 MM12 |  |  |  |  | 4 | 579 |  |

Note
$=$ MM12 equipped with 1 k only (PROMs in position 1 A and $1 B$ ).
$=$ MM12 equipped with 2 k .
$\vdots$
$\vdots$
$\vdots$
$\cdots$

$\rightarrow$


## MODULES FOR PROGRAMMABLE CONTROLLERS

## GENERAL

The programmable controller PC20 is used for controlling machines and/or processes. It can be easily programmed and re-programmed.
The modular design of the PC2O enables a user to build a programmable controller which is 'tailormade' for his control task. By specifying the number and the types of PC20 modules that he requires he only has to purchase the electronic capability he needs.

The PC20 modules are on standard double Eurocards.* Optically isolated interface circuits, specifically designed for an industrial environment, provide excellent noise immunity and a high degree of isolation. The internationally accepted machine signal level of 24 V is used and generous tolerances on operational margins and thresholds ensures good compatibility.
Besides these modules, the PC20 comprises back panels, frames (19 in racks), input and output cables, and a standard power supply. The frames and modules conform to IEC 297 or DIN 41494 (for racks) and IEC 130-14 or DIN 41612 (for connectors). For smaller controllers the special frame SC20 and power supply SO20 are available.
The microcontroller MC2O is suited for controlling small systems. This controller is based on the same principles as the PC20 system, however it is built on a single printed board** with sufficient inputs and outputs for the general run of machine tool and process controls.
Software modules are available e.g. for communication in hierarchical systems.
Tables 1 to 5 give a survey of the available modules, accessories and cables.

[^21]Table 1 Modules

| type | description | catalogue number | page |
| :--- | :--- | :--- | :--- |
| AD20 | analogue to digital module | 432202794200 | 153 |
| CI20* | computer interface | 432202794630 |  |
| CP20 | central processor with program memory (2 k (E) PROM) | 432202792040 | 99 |
| CP21** | central processor with program memory (1 k RAM) | 432202792050 | 109 |
| CP22 | central processor without program memory | 432202792060 | 119 |
| CP24 | central processor with program memory (2 k RAM) | 432202794140 | 129 |
| DA20 | digital to analogue module | 432202794210 | 197 |
| IM20 | input module (16 inputs, 24 V) | 432202792000 | 139 |
| IM22 | input module (32 inputs, 24 V) | 432202794660 | 147 |
| IM23 | input module (16 inputs, 48 V) | 432202794610 | 139 |
| MM20 | program memory module (8 k (E) PROM) | 432202792070 | 161 |
| MM21 | program memory module (8 k RAM) | 432202792080 | 167 |
| MM22 | program memory module (4 k RAM) | 432202794160 | 167 |
| OM20 | output module (16 x0,5 A; 24 V) | 432202792010 | 173 |
| OM21 | output module ( $8 \times 2$ A; 24 V) | 432202792020 | 179 |
| OM22 | output module (32 $\times 0,1 \mathrm{~A} ; 24 \mathrm{~V}$ ) | 432202794100 | 185 |
| OM23* | output module (16 x 0,5 A; 24/48 V) | 432202794700 |  |
| RP20 | bidirectional parallel interface | 432202792170 | 205 |
| RS20 | bidirectional serial interface | 432202792180 | 215 |
| SO20 | supply and output module (8 x 0,5 A) | 432202792030 | 191 |
| VI20 | bidirectional serial interface | 432202792200 | 223 |
| MC20 | microcontroller | 432202723000 | 233 |

Table 2 Programming aids

| type | descriptión | catalogue number | page |
| :--- | :--- | :--- | :--- |
| MI20 | microcontroller interface for MC20 | 432202794190 | 241 |
| PU20/2 | programming unit for PC20 and MC20 | 432202792090 | 247 |
| PU23 | programming unit interface for PC20 and MC20 | 432202794180 | 253 |

[^22]Table 3 Accessories

| type | description | catalogue number | page |
| :--- | :--- | :--- | :--- |
| BP22 | terminal strip for inputs/outputs in controller cabinet SC20 | 432202792140 | 267 |
| BP23 | back panel for main Eurorack | 432202794010 | 261 |
| BP25 | back panel for half extension rack | 432202794030 | 261 |
| BP26 | back panel for full extension rack | 432202794040 | 261 |
| BP27 | terminal strip for output module OM22 in controller |  |  |
|  | cabinet SC20 | 432202793950 | 267 |
| FP20 | front plate, 15 mm width, in controller cabinet SC20 | 432202792150 | 269 |
| FP21 | front plate, 20 mm width (standard module width) | 432202792160 | 269 |
| MB20 | mounting clip for microcontroller MC20 | 432202723080 | 238 |
| RA23 | main rack assembly | 939029410000 |  |
| RA25 | half extension rack assembly (for 15 I/O modules) | 939029420000 |  |
| RA26 | full extension rack assembly (for 21 I/O modules) | 939029430000 |  |
| SC20 | small controller cabinet | 432202792110 | 267 |
|  | CP front panel kit (one LED hole) | 432202791440 |  |
|  | IM/OM front panel kit (16 LED holes) | 432202791450 |  |
| fM20* | supply module | 432202791460 |  |

Table 4 Cables

| type | description | catalogue number | page |
| :--- | :--- | :--- | :--- |
| BI21 | bus extension cable for one I/O extension rack <br> bus extension cable with bus interface for two | 432202737910 | 266 |
| BI22 | 432202737920 | 266 |  |
| BI23 | l/O extension racks <br> bus extension cable with bus interface for three | 432202737930 | 266 |
| I/O extension racks | 939029350000 |  |  |
| CC20 | connecting cable for module OM21 | 939029360000 |  |
| CC21 | connecting cable for module SO20 | 939029370000 |  |
| CC22 | connecting cable for modules IM20/IM23 | 939029380000 |  |
| CC23 | connecting cable for modules IM20/IM23 and OM20/OM23 | 9390 |  |

Table 5 Software modules

| type | description | catalogue number | page |
| :--- | :--- | :--- | :--- |
| PVI1 | message program | 432202799011 | 230 |
| PVI2 | data terminal program | 432202799021 | 230 |
| PVI3 | mass memory program | 432202799031 |  |
| PVI4 | communication program A | 432202799041 | 230 |
| PVI5 | communication program B | 432202799051 | 230 |
| PVI7 | communication program C | 432202799071 | 230 |
| PVI8 | PID control loop | 432202799081 | 230 |
| PDS2 | program development system $n$ | 432202799921 |  |

[^23]

Fig. 1 Diagram of PC20 system.

Figure 1 shows, in a simplified form, the function of each of the PC20 modules. In operation the PC20 cycles continuously through a data input/output cycle and a data processing cycle.

The input module converts the signals from the plant into a binary form acceptable to the central processor.
The central processor reads the data from the input module, performs logic equations on it in accordance with the program instructions and transfers the results to the output module.
The output module converts the binary data from the central processor to electrical signals suitable for the control of the plant.
The program memory is the store in which the set of instructions that comprise the program are stored. These instructions dictate the actions which must be taken in response to the condition of each input.
The programming unit PU20/2 is the means by which an operator can write a program, or changes to a program, into the program memory. The unit is a portable desk-top apparatus so that only one is required to serve any number of PC20 systems. It is connected to the PC20 system via the programming unit interface PU23, which is not too expensive to leave in the PC20 system.
For programming and monitoring the MC20 system, the same programming unit (PU20/2) as for the PC20 system is used, however this unit has to be used in conjunction with microcontroller interface MI20 and programming unit interface PU23, see Fig. 2.


Fig. 2 Diagram of MC2O system.

## PROGRAMMABLE CONTROLLERS

## GENERAL CHARACTERISTICS

Operating temperature range
Storage temperature range
Dimensions

Supply voltage (d.c.)
Number of input + output signals
Maximum program length
Cycle time

0 to $+60^{\circ} \mathrm{C}$ ( 0 to $\left.+45^{\circ} \mathrm{C}^{*}\right)$
-40 to $+70^{\circ} \mathrm{C}$
$160 \mathrm{~mm} \times 233 \mathrm{~mm}$ (double Eurocard) according to IEC 297 or DIN 41494**
$\mathrm{V}=10 \mathrm{~V} \pm 10 \% ; 24 \mathrm{~V} \pm 25 \%^{*} *$ 2000

8 k instructions
1 ms for a typical program of 1 k instructions

## TESTS AND REQUIREMENTS

All modules are designed to meet the tests below.

## Vibration test

IEC 68-2-6, test method Fc ; 10 to 55 Hz , amplitude $0,75 \mathrm{~mm}$ ( $0,35 \mathrm{~mm}^{*}$ ) or 5 g (whichever is less).

## Shock test

IEC 68-2-27, test method Ea; 3 shocks in 6 directions, pulse duration 11 ms , peak acceleration $50 \mathrm{~g}(30 \mathrm{~g}$ ) .

## Rapid change of temperature test

IEC 68-2-14, test method Na : 5 cycles of 2 h at $-40^{\circ} \mathrm{C}$ and 2 h at $+85^{\circ} \mathrm{C}$.
Damp heat test
IEC 68-2-3, test method Ca: 21 days at $40^{\circ} \mathrm{C}$, R.H. 90 to $95 \%$.

## Note

For detailed information refer to the PC20 User Manual, catalogue number 939860960011.

* Valid for PU20/2.
** For PU20/2 and MC20 see the relevant data sheet.


## CENTRAL PROCESSOR

## DESCRIPTION

The central processor CP20 is for use with other PC20 modules, to assemble a programmable controller. The central processor is the heart of the PC20 controller; it requests data from the input modules, processes the data according to the instructions written in the program memory, and applies the results to the output modules. It also generates clock pulses for the controller.
The central processor block diagram is given in Fig. 1. The data processor controls the system and the complete timing. It includes the instruction decoder, the 1 -bit logic processor, the 4 -bit arithmetic processor and the data control.
The address processor generates addresses for the program memory under program control. It also generates addresses for the input and output modules.
The program memory consists of 2 EPROMs 2716 (2k), for which 2 sockets (A and B, Fig. 5) are provided. The CP20 is supplied with 2 empty EPROMs, which can be programmed on the programming unit PU20/2.
The capacity of the scratchpad memory is $1 / 4 \mathrm{k} 4$. Depending on the instruction, the scratchpad memory can be addressed word by word (addresses run from 000 to 255) or bit by bit (addresses run from 000.0 to 255.3 ). In the latter case the address notation is, for example, 147.2 or 076.0 . The CP20 has no on-board battery back-up; provisions for an external battery for data retention in the scratchpad memory are present.
The UDC-circuit (Up-Date and Check) controls the switch-on/off procedure; it informs the system of power failures. It also controls the access of the programming unit to the system memories.
The reset scratchpad memory circuit allows the central processor to set all scratchpad memory locations to zero, dependent on the RSME level, immediately after switch-on of the system.
The timer clock circuit provides 5 crystal-controlled timer clocks: $10 \mathrm{~ms}, 100 \mathrm{~ms}, 1 \mathrm{~s}, 10 \mathrm{~s}, 1 \mathrm{~min}$ (50\% duty factor).


Fig. 1 Block diagram.
Figure 2 illustrates the system operation. The system operates in four phases, which are continuously repeated. The phases, indicated by levels on outputs $\mathrm{PHC}_{0}$ and $\mathrm{PHC}_{1}$, are:

- up-date and check phase (UDC): $\quad \mathrm{PHC}_{0}=0, \mathrm{PHC}_{1}=0$;
- reset scratchpad memory (RSM): $\quad \mathrm{PHC}_{0}=1, \mathrm{PHC}_{1}=0$;
- data processing (DP):
- up-date input/output (I/O):
$P C_{0}=0 ; \mathrm{PHC}_{1}=1 ;$
$\mathrm{PHC}_{0}=1, \mathrm{PHC}_{1}=1$.
Each central processor is built on an epoxy-glass printed-wiring board of $233,4 \mathrm{~mm} \times 160 \mathrm{~mm}$ (double Euro-card*). The board has two F068-I connectors (male parts); the corresponding female parts are on the back panels.

[^24]Fig. 2 Flow chart. The UDC-phase and RSM-phase are only executed if required.


## ELECTRICAL DATA

## Supply

| Supply voltage (d.c.) | $\mathrm{Vp}_{\mathrm{P}}$ | $10 \mathrm{~V} \pm 10 \%$ |
| :--- | :--- | :--- |
| current | Ip | $\max$. |

Requirements of the external battery to retain the contents of the scratchpad memory during power failure.

| Battery voltage | $V_{B}$ | 3 to 4,5 V |  |
| :---: | :---: | :---: | :---: |
| Battery current ( $\mathrm{V}_{P}=0 \mathrm{~V}$ ) | ${ }^{\prime} \mathrm{B}$ | max. | 2 mA |
| Trickle charge current ( $\mathrm{V}_{\mathrm{P}}=10 \mathrm{~V}$ ) |  | typ. | -6 mA |

## Input and output data

The voltage levels of inputs and outputs are in accordance with standard LOCMOS specifications.

|  | function | terminations (Fig. 5) |  |
| :--- | :--- | ---: | ---: |
|  | connector 1 | connector 2 |  |

## BI-DIRECTIONAL BUSSES



|  | function | terminations (Fig. 5) |  |
| :--- | :--- | :--- | :--- |
|  |  | connector 1 | connector 2 |
| INS $_{0}$ |  | a1, | c1 |
|  |  |  |  |
| INS $_{1}$ | Instruction bus, interconnected with PU23; |  |  |
| INS $_{2}$ | commanded by PDBE. | c2 |  |
| INS $_{3}$ |  | a3, | c3 |
| INS $_{4}$ |  | a4, | c4 |

INPUTS

| ALI | Alarm input for internal use. Active HIGH: input current $=2 \mathrm{~mA}$. | a29, c29 |  |
| :---: | :---: | :---: | :---: |
| CPSD | Central processor slow down; input commanded by PU23. |  | a3, c3 |
| CPSI | Central processor stop initiate; command from PU23 stops central processor in UDC-phase (active HIGH). |  | a4, c4 |
| DEF | Data exchange finished; signal from output modules indicating that data from central processor has been stored. | a25 |  |
| HOLD | Command from PU23 to stop central processor in DP-phase (active LOW). |  | a6, c6 |
| PABE | Program memory address bus enable; active during UDC-phase. When LOW APM bus functions as input. |  | a1, c1 |
| PDBE | Program memory data bus enable; active during UDC-phase. When LOW, INS and ADD-bus function as inputs. |  | a2, c2 |
| PRF | Preparation input/output modules finished. | a24 |  |
| $\overline{\mathrm{RCP}}$ | Reset central processor; resets data processor, address processor, UDC circuitry, RSM circuitry and timer clocks. Active LOW: input current $=2 \mathrm{~mA}$. |  | a12, c12 |
| RSME | Reset scratchpad memory enable. When HIGH or floating a reset of the scratchpad memory will occur during the first RSM-phase after switching on. When LOW (input current $=2 \mathrm{~mA}$ ) the RSMphase is only effective for the scratchpad memory addresses 0 to 2 inclusive. |  | a10, c10 |




Fig. 3 Location of RCO points.


Fig. 4 Circuit diagram of SRI output. Transistor conducting: $I_{\mathrm{Q}}=\max .100 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CE}}<1,5 \mathrm{~V}$; transistor non-conducting: $I_{Q}=\max .10 \mu \mathrm{~A} ; \mathrm{V}_{\mathrm{CE}} \leqslant 30 \mathrm{~V}$; in case of system stop the output stage switches on and off with a cycle time of $0,4 \mathrm{~s}$.

Fixed scratchpad memory addresses

| address | description |
| :--- | :--- |
| 000.0 | Overflow bit for arithmetic operations. |
| 000.1 | Constant "1" level. |
| 000.2 | 24 V alarm output (becomes 1 if $\mathrm{V}_{\mathrm{S}} \leqslant 17,5 \mathrm{~V}$ ). |
| 000.3 | Timer clock 10 ms. |
| 001.0 | Timer clock 100 ms. |
| 001.1 | Timer clock 1 s. |
| 001.2 | Timer clock 10 s. |
| 001.3 | Timer clock 1 min. |

## MECHANICAL DATA

Dimensions in mm

## Outlines



Fig. 5.

## Mass

 approx. 270 gCentral processor

Terminal location

| row c |  | row a |
| :---: | :---: | :---: |
| $\mathrm{INS}_{0}$ | 1 | $\mathrm{INS}_{0}$ |
| $\mathrm{INS}_{1}$ | 2 | $\mathrm{INS}_{1}$ |
| $\mathrm{INS}_{2}$ | 3 | $\mathrm{INS}_{2}$ |
| $\mathrm{INS}_{3}$ | 4 | $\mathrm{INS}_{3}$ |
| $\mathrm{INS}_{4}$ | 5 | $\mathrm{INS}_{4}$ |
| $\mathrm{ADD}_{0}$ | 6 | $\mathrm{ADD}_{0}$ |
| $\mathrm{ADD}_{1}$ | 7 | $\mathrm{ADD}_{1}$ |
| $\mathrm{ADD}_{2}$ | 8 | $\mathrm{ADD}_{2}$ |
| $\mathrm{ADD}_{3}$ | 9 | $\mathrm{ADD}_{3}$ |
| $\mathrm{ADD}_{4}$ | 10 | $\mathrm{ADD}_{4}$ |
| $\mathrm{ADD}_{5}$ | 11 | $\mathrm{ADD}_{5}$ |
| $\mathrm{ADD}_{6}$ | 12 | $\mathrm{ADD}_{6}$ |
| $\mathrm{ADD}_{7}$ | 13 | $\mathrm{ADD}_{7}$ |
| $\mathrm{ADD}_{8}$ | 14 | $\mathrm{ADD}_{8}$ |
| $\mathrm{ADD}_{9}$ | 15 | ADD9 |
| ADD 10 | 16 | ADD 10 |
| PB1 | 17 | $\mathrm{PB}_{0}$ |
| RR | 18 | RR |
| $\mathrm{DIO}_{0}$ | 19 | $\mathrm{DIO}_{0}$ |
| $\mathrm{DIO}_{1}$ | 20 | $\mathrm{DIO}_{1}$ |
| $\mathrm{DIO}_{2}$ | 21 | $\mathrm{DiO}_{2}$ |
| $\mathrm{DIO}_{3}$ | 22 | $\mathrm{DIO}_{3}$ |
| $\mathrm{PHC}_{0}$ | 23 | $\mathrm{PHC}_{1}$ |
| R/WSM | 24 | PRF |
| O V * | 25 | DEF |
| SBI | 26 | APF |
| $\overline{\mathrm{RCO}}$ | 27 | n.c. |
| WEPC | 28 | n.c. |
| ALI | 29 | ALI |
| SRI - | 30 | SRI + |
| $V_{p}$ | 31 | $V_{p}$ |
| 0 V | 32 | 0 V |

connector 2

| row c |  | row a |
| :---: | :---: | :---: |
| PABE | 1 | PABE |
| PDBE | 2 | PDBE |
| CPSD | 3 | CPSD |
| CPSI | 4 | CPSI |
| CPSC | 5 | CPSC |
| HOLD | 6 | HOLD |
| CLOCK | 7 | CLOCK |
| n.c. | 8 | n.c. |
| n.c. | 9 | n.c. |
| RSME | 10 | RSME |
| n.c. | 11 | n.c. |
| $\overline{\mathrm{RCP}}$ | 12 | $\overline{\mathrm{RCP}}$ |
| WPSM | 13 | WPSM |
| n.c. | 14 | n.c. |
| n.c. | 15 | n.c. |
| $\mathrm{APM}_{0}$ | 16 | $\mathrm{APM}_{0}$ |
| $\mathrm{APM}_{1}$ | 17 | $\mathrm{APM}_{1}$ |
| $\mathrm{APM}_{2}$ | 18 | $\mathrm{APM}_{2}$ |
| $\mathrm{APM}_{3}$ | 19 | $\mathrm{APM}_{3}$ |
| $\mathrm{APM}_{4}$ | 20 | $\mathrm{APM}_{4}$ |
| $\mathrm{APM}_{5}$ | 21 | $\mathrm{APM}_{5}$ |
| $\mathrm{APM}_{6}$ | 22 | $\mathrm{APM}_{6}$ |
| $\mathrm{APM}_{7}$ | 23 | $\mathrm{APM}_{7}$ |
| APM8 | 24 | APM $_{8}$ |
| APM9 | 25 | APM9 |
| APM 10 | 26 | $A^{\text {APM }} 10$ |
| $\mathrm{APM}_{11}$ | 27 | $A^{\text {APM }} 11$ |
| $\mathrm{APM}_{12}$ | 28 | $\mathrm{APM}_{12}$ |
| n.c. | 29 | n.c. |
| VB | 30 | VB |
| $V_{p}$ | 31 | $V_{p}$ |
| 0 V | 32 | 0 V |

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## CENTRAL PROCESSOR

## DESCRIPTION

The central processor CP21 is for use with other PC20 modules, to assemble a programmable controller.
The central processor is the heart of the PC2O controller; it requests data from the input modules, processes the data according to the instructions written in the program memory, and applies the results to the output modules. It also generates clock pulses for the controller.
The central processor block diagram is given in Fig. 1. The data processor controls the system and the complete timing. It includes the instruction decoder, the 1 -bit logic processor, the 4 -bit arithmetic processor and the data control.
The address processor generates addresses for the program memory under program control. It also generates addresses for the input and output modules.
The program memory is a C-MOS RAM ( 1 k 16 ). The CP21 has on-board battery back-up and a provision to connect an external battery for longer memory retention.
The capacity of the scratchpad memory is $1 / 4 \mathrm{k} 4$. Depending on the instruction, the scratchpad memory can be addressed word by word (addresses run from 000 to 255) or bit by bit (addresses run from 000.0 to 255.3 ). In the latter case, the address notation is, for example, 147.2 or 076.0. The on-board battery for data retention in the program memory RAM, is also used for data retention of the scratchpad memory.
The UDC-circuit (Up-Date and Check) controls the switch-on/off procedure; it informs the system of power failures. It also controls the access of the programming unit to the system memories.
The reset scratchpad memory circuit allows the central processor to set all scratchpad memory locations to zero, dependent on the RSME level, immediately after switch-on of the system.
The timer clock circuit provides 5 crystal-controlled timer clocks: $10 \mathrm{~ms}, 100 \mathrm{~ms}, 1 \mathrm{~s}, 10 \mathrm{~s}, 1 \mathrm{~min}$ (50\% duty factor).


Fig. 1 Block diagram.
Figure 2 illustrates the system operation. The system operates in four phases, which are continuously repeated. The phases, indicated by levels on outputs $\mathrm{PHC}_{0}$ and $\mathrm{PHC}_{1}$, are:

- up-date and check phase (UDC):
- reset scratchpad memory (RSM):
- data processing (DP):
- up-date input/output (I/O):
$\mathrm{PHC}_{0}=0, \mathrm{PHC}_{1}=0 ;$
$\mathrm{PHC}_{0}=1, \mathrm{PHC}_{1}=0$.
$\mathrm{PHC}_{0}=0, \mathrm{PHC}_{1}=1$.
$\mathrm{PHC}_{0}=1, \mathrm{PHC}_{1}=1$.

Each central processor is built on an epoxy-glass printed-wiring board of $233,4 \mathrm{~mm} \times 160 \mathrm{~mm}$ (double Euro-card*). The board has two F068-I connectors (male parts); the corresponding female parts are on the back panels.

* For a general description of the Euro-card system see IEC 297 or DIN 41494 for 19-in racks and IEC 130-14 or DIN 41612 for connectors.

Fig. 2 Flow chart. The UDC-phase and RSM-phase are only executed if required.


## ELECTRICAL DATA

Supply

| Supply voltage (d.c.) | $V_{P}$ | $10 \mathrm{~V} \pm 10 \%$ |
| :---: | :--- | :--- |
| current | $I_{P}$ | $\max .160 \mathrm{~mA}$ |

Requirements of the external battery to retain the contents of the program memory and the scratchpad memory during power failure.
Battery voltage
Battery current ( $\mathrm{V}_{\mathrm{P}}=0 \mathrm{~V}$ )
Trickle charge current ( $\mathrm{V} P=10 \mathrm{~V}$ )
Data retention with on-board battery at $40^{\circ} \mathrm{C}$

## Input and output data

The voltage levels of inputs and outputs are in accordance with standard LOCMOS specifications.

|  | function | terminations (Fig. 4) |  |
| :--- | :--- | :--- | :--- |
|  |  | connector 1 | connector 2 |

BI-DIRECTIONAL BUSSES

| $\begin{aligned} & \mathrm{ADD}_{0} \\ & \mathrm{ADD}_{1} \\ & \mathrm{ADD}_{2} \\ & \rightarrow \mathrm{ADD}_{3} \\ & \mathrm{ADD}_{4} \\ & \mathrm{ADD}_{5} \\ & \mathrm{ADD}_{6} \\ & \mathrm{ADD}_{7} \\ & \mathrm{ADD}_{8} \\ & \mathrm{ADD}_{9} \\ & \mathrm{ADD}_{10} \\ & \hline \end{aligned}$ | Address bus interconnected with PU23 and input and output modules; commanded by PDBE; during DP-phase address bits for the scratchpad memory; during I/O-phase address bits for the input and output modules. | a6, c6 <br> a7, c7 <br> a8, c8 <br> a9, c9 <br> a10, c10 <br> a11, c11 <br> a12, c12 <br> a13, c13 <br> a14, c14 <br> a15, c15 <br> a16, c16 |  |
| :---: | :---: | :---: | :---: |
| $A P M_{0}$ APM ${ }_{1}$ APM ${ }_{2}$ $\mathrm{APM}_{3}$ $\mathrm{APM}_{4}$ APM 5 APM $_{6}$ $\mathrm{APM}_{7}$ $\mathrm{APM}_{8}$ APM9 APM 10 | Program memory address bus; APM act as inputs when PABE is LOW (only during UDC-phase). |  | a16, c 16 <br> a17, c 17 <br> a18, c 18 <br> a19, c 19 <br> a20, c 20 <br> a21, c 21 <br> a22, c 22 <br> a23, c 23 <br> a24, c 24 <br> a25, c 25 <br> a26, c 26 |
| APM 11 APM 12 | Pseudo address bits connected via resistor to 0 V . |  | $\begin{array}{ll} \text { a27, } & \text { c27 } \\ \text { a28, } & \text { c28 } \end{array}$ |
| $\rightarrow \begin{aligned} & \mathrm{DIO}_{0} \\ & \mathrm{DIO}_{1} \\ & \mathrm{DIO}_{2} \\ & \mathrm{DIO}_{3} \\ & \hline \end{aligned}$ | Data bus; receives data for scratchpad memory from input modules and PU23, transmits data from scratchpad memory to output modules and PU23; data bus is controlled by WEPC or by R/WSM. | a19, c19 <br> a20, c20 <br> a21, c21 <br> a22, c22 |  |


|  | function | terminations (Fig. 4) |  |  |
| :---: | :---: | :---: | :---: | :---: |
|  |  | con | tor 1 | connector 2 |
| $\mathrm{INS}_{0}$ | Instruction bus, interconnected with PU23; commanded by PDBE, | a1, |  |  |
| $\mathrm{INS}_{1}$ |  |  | c2 |  |
| $\mathrm{INS}_{2}$ |  |  | c3 |  |
| $\mathrm{INS}_{3}$ |  |  | c4 |  |
| $\mathrm{INS}_{4}$ |  |  | c5 |  |

INPUTS

| ALI | Alarm input for internal use. Active HIGH: input current $=2 \mathrm{~mA}$. | a29, c29 |  |
| :---: | :---: | :---: | :---: |
| CPSD | Central processor slow down; input commanded by PU 23. |  | a3, c3 |
| CPSI | Central processor stop initiate; command from PU23 stops central processor in UCD-phase (active HIGH). |  | a4, c4 |
| DEF | Data exchange finished; signal from output modules indicating that data from central processor has been stored. | a25 |  |
| HOLD | Command from PU23 to stop central processor in DP-phase (active LOW). |  | a6, c6 |
| PABE | Program memory address bus enable; active during UDC-phase. When LOW APM bus functions as input. |  | a1, c1 |
| PDBE | Program memory data bus enable; active during UDC-phase. When LOW, INS and ADD-bus function as inputs. |  | a2, c2 |
| PRF | Preparation input/output modules finished. | a24 |  |
| $\overline{\mathrm{RCP}}$ | Reset central processor; resets data processor, address processor, UDC circuitry, RSM circuitry and timer clocks. Active LOW: input current $=2 \mathrm{~mA}$. |  | a12, c12 |
| RSME | Reset scratchpad memory enable. When HIGH or floating a reset of the scratchpad memory will occur during the first RSM-phase after switching on. When LOW (input current $=2 \mathrm{~mA}$ ) the RSMphase is only effective for the scratchpad memory addresses 0 to 2 inclusive. |  | a10, c10 |
| $\overline{\mathrm{R}} / \mathrm{WPM}$ | Write signal from PU23 to CP21, to store data in program memory (active HIGH). |  | a14, c14 |


|  | function | terminations (Fig. 4) |  |
| :--- | :--- | ---: | ---: |
| R/WSM |  | c24 |  |
| WEPC | Write enable signal from PU23; prepares central <br> processor to store data from PU23 into scratch- <br> pad memory. | c28 | connector 2 |
| WPSM | Write pulse for scratchpad memory; signal from <br> PU23 to store data on DIO <br> O-3 into scratchpad <br> memory. | a13, c13 |  |

## OUTPUTS




Fig. 3 Location of RCO points and switch (jumper A) of on-board battery.

Fixed scratchpad memory addresses

| address | description |
| :--- | :--- |
| 000.0 | Overflow bit for arithmetic operations. |
| 000.1 | Constant '1' level. |
| 000.2 | 24 V alarm output (becomes 1 if $\mathrm{V}_{\mathrm{S}} \leqslant 17,5 \mathrm{~V}$ ). |
| 000.3 | Timer clock 10 ms. |
| 001.0 | Timer clock 100 ms. |
| 001.1 | Timer clock 1 s. |
| 001.2 | Timer clock 10 s. |
| 001.3 | Timer clock 1 min. |

MECHANICAL DATA
Dimensions in mm
Outlines


Fig. 4.
Mass
approx. 270 g

## Notes

1. At delivery of the central processor the on-board battery is switched off (jumper A, Figs 3 and 4, in off-position).
2. If the central processor is removed from the rack, ensure that it is put on an insulated surface to prevent short-circuiting of the on-board battery.

Terminal location
connector 1

| row c |  | row a |
| :---: | :---: | :---: |
| $\mathrm{INS}_{0}$ | 1 | $\mathrm{INS}_{0}$ |
| $\mathrm{INS}_{1}$ | 2 | $\mathrm{INS}_{1}$ |
| $\mathrm{INS}_{2}$ | 3 | $\mathrm{INS}_{2}$ |
| $\mathrm{INS}_{3}$ | 4 | $\mathrm{INS}_{3}$ |
| $\mathrm{INS}_{4}$ | 5 | $\mathrm{INS}_{4}$ |
| $\mathrm{ADD}_{0}$ | 6 | $\mathrm{ADD}_{0}$ |
| $\mathrm{ADD}_{1}$ | 7 | $\mathrm{ADD}_{1}$ |
| $\mathrm{ADD}_{2}$ | 8 | $\mathrm{ADD}_{2}$ |
| $\mathrm{ADD}_{3}$ | 9 | $\mathrm{ADD}_{3}$ |
| $\mathrm{ADD}_{4}$ | 10 | $\mathrm{ADD}_{4}$ |
| $\mathrm{ADD}_{5}$ | 11 | $\mathrm{ADD}_{5}$ |
| $\mathrm{ADD}_{6}$ | 12 | $\mathrm{ADD}_{6}$ |
| $\mathrm{ADD}_{7}$ | 13 | $\mathrm{ADD}_{7}$ |
| ADD8 | 14 | $\mathrm{ADD}_{8}$ |
| ADD9 | 15 | ADD9 |
| ADD 10 | 16 | ADD10 |
| $\mathrm{PB}_{1}$ | 17 | $\mathrm{PB}_{0}$ |
| RR | 18 | RR |
| $\mathrm{DIO}_{0}$ | 19 | $\mathrm{DIO}_{0}$ |
| $\mathrm{DIO}_{1}$ | 20 | $\mathrm{DIO}_{1}$ |
| $\mathrm{DIO}_{2}$ | 21 | $\mathrm{DIO}_{2}$ |
| $\mathrm{DIO}_{3}$ | 22 | $\mathrm{DIO}_{3}$ |
| $\mathrm{PHC}_{0}$ | 23 | $\mathrm{PHC}_{1}$ |
| R/酲SM | 24 | PRF |
| 0 V * | 25 | DEF |
| SBI | 26 | APF |
| $\overline{\mathrm{RCO}}$ | 27 | n.c. |
| WEPC | 28 | n.c. |
| ALI | 29 | ALI |
| n.c. | 30 | n.c. |
| $V_{p}$ | 31 | $V_{p}$ |
| 0 V | 32 | 0 V |

connector 2
row c

| PABE | 1 | PABE |
| :---: | :---: | :---: |
| PDBE | 2 | PDBE |
| CPSD | 3 | CPSD |
| CPSI | 4 | CPSI |
| CPSC | 5 | CPSC |
| HOLD | 6 | HOLD |
| CLOCK | 7 | CLOCK |
| n.c. | 8 | n.c. |
| n.c. | 9 | n.c. |
| RSME | 10 | RSME |
| n.c. | 11 | n.c. |
| $\overline{\mathrm{RCP}}$ | 12 | $\overline{\mathrm{RCP}}$ |
| WPSM | 13 | WPSM |
| $\overline{\mathrm{R}} / \mathrm{WPM}$ | 14 | $\overline{\mathrm{R}} / \mathrm{WPM}$ |
| n.c. | 15 | n.c. |
| $\mathrm{APM}_{0}$ | 16 | $\mathrm{APM}_{0}$ |
| $\mathrm{APM}_{1}$ | 17 | $\mathrm{APM}_{1}$ |
| $\mathrm{APM}_{2}$ | 18 | $\mathrm{APM}_{2}$ |
| $\mathrm{APM}_{3}$ | 19 | $\mathrm{APM}_{3}$ |
| $\mathrm{APM}_{4}$ | 20 | $\mathrm{APM}_{4}$ |
| $\mathrm{APM}_{5}$ | 21 | $\mathrm{APM}_{5}$ |
| APM $_{6}$ | 22 | $\mathrm{APM}_{6}$ |
| $\mathrm{APM}_{7}$ | 23 | $\mathrm{APM}_{7}$ |
| $\mathrm{APM}_{8}$ | 24 | $\mathrm{APM}_{8}$ |
| APM9 | 25 | APM9 |
| $\mathrm{APM}_{10}$ | 26 | APM $_{10}$ |
| APM 11 | 27 | APM $_{11}$ |
| APM 12 | 28 | $\mathrm{APM}_{12}$ |
| n.c. | 29 | n.c. |
| VB | 30 | VB |
| $V_{p}$ | 31 | $V_{p}$ |
| 0 V | 32 | 0 V |

n.c. $=$ not connected

[^25]
## CENTRAL PROCESSOR

## DESCRIPTION

The central processor CP22 is for use with other PC20 modules, to assemble a programmable controller. The central processor is the heart of the PC2O controller; it requests data from the input modules, processes the data according to the instructions written in the program memory, and applies the results to the output modules. It also generates the clock pulses for the controller.
The central processor block diagram is given in Fig. 1.


Fig. 1 Block diagram.
The data processor performs the control of the system and the complete timing. It includes the instruction decoder, the logic processor, the arithmetic processor and the control of the internal data traffic.
The address processor generates addresses for the program memory. It also generates addresses for the input and output modules. It has an address range for an 8 k program memory.
In the scratchpad memory the data from the inputs are stored as are the processed data for transfer to the outputs; for this purpose the inputs and outputs each have their own, individual place in the scratchpad. The capacity of the scratchpad memory, including the page register, is 2 k 4 , divided in 4 pages of 512 words each; for details see para. "Organization of scratchpad memory and page register". The CP22 has provisions for an external battery for data retention in the scratchpad memory.
The UDC-circuit (Up-Date and Check) controls the switch-on/off procedure; it informs the system about power failures. It also controls the access of the programming unit to the system memories.
The reset scratchpad memory circuit provides the central processor with the possibility to set all scratchpad memory locations to zero, dependent on the RSME level, immediately after the switch-on of the system.
The timer clock circuit provides 5 crystal-controlled timer clocks: $10 \mathrm{~ms}, 100 \mathrm{~ms}, 1 \mathrm{~s}, 10 \mathrm{~s}$, 1 min ( $50 \%$ duty factor).

Figure 2 illustrates the system operation. The system operates in four phases, which are continuously repeated. The phases, indicated by levels on outputs $\mathrm{PHC}_{0}$ and $\mathrm{PHC}_{1}$, are:

- up-date and check phase (UDC): $\quad \mathrm{PHC}_{0}=0, \mathrm{PHC}_{1}=0$.
- reset scratchpad memory (RSM): $\quad \mathrm{PHC}_{0}=1, \mathrm{PHC}_{1}=0$.
- data processing (DP): $P H C_{0}=0, \mathrm{PHC}_{1}=1$.
- up-date input/output (I/O): $\quad \mathrm{PHC}_{0}=1, \mathrm{PHC}_{1}=1$.

Each central processor is built on an epoxy-glass printedwiring board of $233,4 \mathrm{~mm} \times 160 \mathrm{~mm}$ (double Euro-card*). The board is provided with two F068-I connectors (male parts); the corresponding female parts are on the back panels.


Fig. 2 Flow chart. The UDC-phase
and RSM-phase are only executed
Fig. 2 Flow chart. The UDC-phase
and RSM-phase are only executed if required.

* For a general description of the Euro-card system see IEC 297 or DIN 41494 for 19-in racks and IEC 130-14 or DIN 41612 for connectors.


## Central processor

## ELECTRICAL DATA

## Supply

Supply voltage (d.c.)
current

| $V_{P}$ | $10 \mathrm{~V} \pm 10 \%$ |
| :--- | :--- |
| $\mathrm{I}_{\mathrm{P}}$ | typ. $\quad 90 \mathrm{~mA}$ |
| max. | 110 mA |

Requirements of the external battery to retain the contents of the scratchpad memory during power failure.

Battery voltage
Battery current ( $\mathrm{V}_{\mathrm{P}}=0 \mathrm{~V}$ )
Trickle charge current ( $\mathrm{V}_{\mathrm{P}}=10 \mathrm{~V}$ )
$V_{B} 3$ to $4,5 \mathrm{~V}$
$\mathrm{I}_{\mathrm{B}} \quad$ typ. $1,5 \mathrm{~mA}$
typ. -5 mA

## Input and output data

The voltage levels of inputs and outputs are in accordance with standard LOCMOS specifications

|  | function | terminations (Fig. 7) |  |
| :---: | :---: | :---: | :---: |
|  |  | connector 1 | connector 2 |
| BI-DIRECTIONAL BUSSES |  |  |  |
| $\begin{aligned} & \mathrm{ADD}_{0} \\ & \mathrm{ADD}_{1} \\ & \mathrm{ADD}_{2} \\ & \mathrm{ADD}_{3} \\ & \mathrm{ADD}_{4} \\ & \mathrm{ADD}_{5} \\ & \mathrm{ADD}_{6} \\ & \mathrm{ADD}_{7} \\ & \mathrm{ADD}_{8} \\ & \mathrm{ADD}_{9} \\ & \mathrm{ADD}_{10} \end{aligned}$ | Address bus interconnected with PU23 and input and output modules; commanded by PDBE; during DP-phase address bits for the scratchpad memory; during I/O-phase address bits for the input and output modules. | a6, a7, <br> a8, <br> a9, <br> a10, <br> a11, <br> a12, <br> a13, <br> a14, <br> a15, <br> a16, |  |
| APM0 <br> APM 1 <br> $\mathrm{APM}_{2}$ <br> $\mathrm{APM}_{3}$ <br> $\mathrm{APM}_{4}$ <br> APM ${ }_{5}$ <br> APM ${ }_{6}$ <br> APM $_{7}$ <br> APM8 <br> APM9 <br> APM 10 <br> APM 11 <br> APM 12 | Program memory address bus; APM act as inputs when PABE is LOW (only during UDC-phase). |  | a16, c16 <br> a17, c17 <br> a18, c18 <br> a19, c19 <br> a20, c20 <br> a21, c21 <br> a22, c22 <br> a23, c23 <br> a24, c24 <br> a25, c25 <br> a26, c26 <br> a27, c27 <br> a28, c28 |
| $\begin{aligned} & \mathrm{DIO}_{0} \\ & \mathrm{DIO}_{1} \\ & \mathrm{DIO}_{2} \\ & \mathrm{DIO}_{3} \end{aligned}$ | Data bus; receives data for scratchpad memory from input modules and PU23, transmits data from scartchpad memory to output modules and PU23; data bus is controlled by WEPC or by R/WSM. | a19, c19 <br> a20, c20 <br> a21, c21 <br> a22, c22 |  |


|  | function | terminations (Fig. 7) |  |
| :--- | :--- | :--- | :--- |
|  |  | connector 1 | connector 2 |
| INS $_{0}$ |  | $a 1$ |  |
| INS $_{1}$ | Instruction bus, interconnected with PU23; | a2 |  |
| INS $_{2}$ | commanded by PDBE. | a3 |  |
| INS $_{3}$ |  | $a 4$ |  |
| INS $_{4}$ |  | a5 |  |

INPUTS

| ALI | Alarm input for internal use. Active HIGH: input current $=2 \mathrm{~mA}$. | a29, c29 |  |
| :---: | :---: | :---: | :---: |
| CPSI | Central processor stop initiate; command from PU23 stops central processor in UDC-phase (active HIGH). |  | a4, c4 |
| DEF | Data exchange finished; signal from output modules indicating that data from central processor has been stored. | a25 |  |
| HOLD | Command from PU23 to stop central processor in DP-phase (active LOW). |  | a6, c6 |
| PABE | Program memory address bus enable; active during UDC-phase. When LOW APM bus is in highimpedance state. |  | a1, c1 |
| PDBE | Program memory data bus enable; active during UDC-phase. When LOW, ADD-bus function as input, and INS-bus is in high-impedance state. |  | a2, c2 |
| $\mathrm{PMB}_{0}$ <br> PMB ${ }_{1}$ <br> $\mathrm{PMB}_{2}$ <br> $\mathrm{PMB}_{3}$ <br> $\mathrm{PMB}_{4}$ <br> $\mathrm{PMB}_{5}$ <br> PMB6 <br> $\mathrm{PMB}_{7}$ <br> PMB8 <br> PMB9 <br> PMB 10 <br> PMB 11 <br> PMB 12 <br> PMB 13 <br> PMB14 <br> PMB15 | Program memory bits from memory module. | c1 <br> c2 <br> c3 <br> c4 <br> c5 <br> c6 <br> c7 <br> c8 <br> c9 <br> c10 <br> c11 <br> c12 <br> c13 <br> c14 <br> c15 <br> c16 |  |


|  | function | terminations (Fig. 7) |  |
| :---: | :---: | :---: | :---: |
|  |  | connector 1 | connector 2 |
| PRF | Preparation input/output module finished. | a24 |  |
| PRFP | Preparation memory module finished. | a27 |  |
| $\overline{\mathrm{RCP}}$ | Reset central processor; resets data processor, address processor, UDC circuitry, RSM circuitry and timer clocks. Active LOW: input current $=2 \mathrm{~mA}$ |  | a12, c12 |
| RSME | Reset scratchpad memory enable. When HIGH or floating a reset of the scratchpad memory will occur during the first RSM-phase after switching on. When LOW (input current $=2 \mathrm{~mA}$ ) the RSMphase is only effective for the scratchpad memory locations 002.2 and 002.3. |  | a10, c10 |
| R/W̄SM | Read-write level from input and output modules; only effective during l/O-phase. | c24 |  |
| WEPC | Write enable signal from PU23; prepares central processor to store data from PU23 into scratchpad memory. | c28 |  |
| WPSM | Write pulse for scratchpad memory; signal from PU 23 to store data on $\mathrm{DIO}_{0-3}$ into scartchpad memory |  | a13, c13 |

## OUTPUTS

| APF | Address processing for input and output modules <br> finished. | a 26 |  |
| :--- | :--- | :--- | :--- |
| APFP | Address processing for memory modules finished. | a 28 |  |
| CLOCK | Clock output to PU23. | $\mathrm{a7}, \quad \mathrm{c7}$ |  |
| CPSC | Central processor stop completed; command <br> (HIGH) to PU23 indicating that central processor <br> has been stopped in UDC-phase. | a5, $\quad$ c5 |  |
| $\mathrm{PB}_{0}$ <br> $\mathrm{~PB}_{1}$ | Page bits, contents of page register, interconnected <br> with PU23. | a17 | c17 |


|  | function | terminations (Fig. 7) |  |  |
| :---: | :---: | :---: | :---: | :---: |
|  |  | connector 1 |  | connector 2 |
| RR | Result Register, interconnected with PU23. | a18, | c18 |  |
| SBI | Storage command to store data on data bus into output modules and PU23. |  | c26 |  |
| $\begin{aligned} & \text { SRI + } \\ & \text { SRI - } \end{aligned}$ | System run indication; Darlington transistor output, galvanically isolated by means of opto coupler. SRI + = collector, SRI - = emitter. When the system runs the transistor is non conducting; when the system stops the transistor switches on and off (see for circuit diagram, Fig. 4). | a30 | c30 |  |



Fig. 3 Location of RCO points.


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Fig. 4 Circuit diagram of SRI output. Transistor conducting: $\mathrm{I}_{\mathrm{Q}}=\max .100 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CE}}<1,5 \mathrm{~V}$; transistor non-conducting: $\mathrm{I}_{\mathrm{Q}}=$ max. $10 \mu \mathrm{~A} ; \mathrm{V}_{\mathrm{CE}} \leqslant 30 \mathrm{~V}$; in case of system stop the output stage switches on and off with a cycle time of $0,4 \mathrm{~s}$.

## Organization of scratchpad memory and page register

The capacity of the scratchpad memory is $2 k 4$, divided into 4 pages of 512 words each, see Fig. 5. Depending on the instruction the scratchpad memory is addressed word by word or bit by bit. The page numbers run from 0 to 3 and the addresses within a page from 000 to 511 . When addressing word by word the address notation is 0000 to 0511,1000 to 1511,2000 to 2511 or 3000 to 3511. When addressing bit by bit the addresses run from 000.0 to 511.3 . This bit by bit addressing can, basically, only be done on page 0 ; addressing on other pages is possible by using the page register. This register, which has the fixed address 0002, is connected in parallel with the scratchpad memory and is enabled by inserting a wire jump between points PBE on the module, see Fig. 6. When a number 1,2 or 3 has been stored in this register, the succeeding bit by bit addressing is then carried out on the page indicated by the contents of the page register.
At the end of a DP-phase the contents of the page register is always set to zero, independent of whether the wire jump PBE has been inserted or not.


Fig. 5 Schematic presentation of the scratchpad memory.


Fig. 6 Location of PBE points.
Fixed scratchpad memory addresses

| address | description |
| :--- | :--- |
| 000.0 | Overflow bit for arithmetic operations. |
| 000.1 | Constant "1" level. |
| 000.2 | 24 V alarm output (becomes 1 if $\mathrm{V}_{\mathrm{S}} \leqslant 17,5 \mathrm{~V}$ ). |
| 000.3 | Timer clock 10 ms. |
| 001.0 | Timer clock 100 ms. |
| 001.1 | Timer clock 1 s. |
| 001.2 | Timer clock 10 s. |
| 001.3 | Timer clock 1 min. |
| 002.0 | Page register. |
| 002.1 |  |

## MECHANICAL DATA

Dimensions in mm

## Outlines



Fig. 7.

Mass
approx. 270 g

Terminal location
connector 1

| row c |  | row a |
| :---: | :---: | :---: |
| $\mathrm{PMB}_{0}$ | 1 | $\mathrm{INS}_{0}$ |
| $\mathrm{PMB}_{1}$ | 2 | $\mathrm{INS}_{1}$ |
| $\mathrm{PMB}_{2}$ | 3 | $\mathrm{INS}_{2}$ |
| $\mathrm{PMB}_{3}$ | 4 | $\mathrm{INS}_{3}$ |
| $\mathrm{PMB}_{4}$ | 5 | $\mathrm{INS}_{4}$ |
| $\mathrm{PMB}_{5}$ | 6 | $\mathrm{ADD}_{0}$ |
| $\mathrm{PMB}_{6}$ | 7 | $\mathrm{ADD}_{1}$ |
| $\mathrm{PMB}_{7}$ | 8 | $\mathrm{ADD}_{2}$ |
| $\mathrm{PMB}_{8}$ | 9 | $\mathrm{ADD}_{3}$ |
| PMB9 | 10 | $\mathrm{ADD}_{4}$ |
| PMB 10 | 11 | $\mathrm{ADD}_{5}$ |
| PMB11 | 12 | $\mathrm{ADD}_{6}$ |
| $\mathrm{PMB}_{12}$ | 13 | $\mathrm{ADD}_{7}$ |
| PMB13 | 14 | $\mathrm{ADD}_{8}$ |
| $\mathrm{PMB}_{14}$ | 15 | ADD9 |
| PMB 15 | 16 | ADD 10 |
| $\mathrm{PB}_{1}$ | 17 | $\mathrm{PB}_{0}$ |
| RR | 18 | RR |
| $\mathrm{DIO}_{0}$ | 19 | $\mathrm{DIO}_{0}$ |
| $\mathrm{DIO}_{1}$ | 20 | $\mathrm{DIO}_{1}$ |
| $\mathrm{DIO}_{2}$ | 21 | $\mathrm{DIO}_{2}$ |
| $\mathrm{DIO}_{3}$ | 22 | $\mathrm{DIO}_{3}$ |
| PHC0 | 23 | $\mathrm{PHC}_{1}$ |
| R/WSM | 24 | PRF |
| 0 V * | 25 | DEF |
| SBI | 26 | APF |
| $\overline{\mathrm{RCO}}$ | 27 | PRFP |
| WECP | 28 | APFP |
| ALI | 29 | ALI |
| SRI - | 30 | SRI + |
| $V_{p}$ | 31 | $V_{p}$ |
| 0 V | 32 | 0 V |

connector 2

| row c |  | row a |
| :---: | :---: | :---: |
| PABE | 1 | PABE |
| PDBE | 2 | PDBE |
| n.c. | 3 | n.c. |
| CPSI | 4 | CPSI |
| CPSC | 5 | CPSC |
| HOLD | 6 | HOLD |
| CLOCK | 7 | CLOCK |
| n.c. | 8 | n.c. |
| n.c. | 9 | n.c. |
| RSME | 10 | RSME |
| n.c. | 11 | n.c. |
| $\overline{\mathrm{RCP}}$ | 12 | $\overline{\mathrm{RCP}}$ |
| WPSM | 13 | WPSM |
| n.c. | 14 | n.c. |
| n.c. | 15 | n.c. |
| $\mathrm{APM}_{0}$ | 16 | APM $_{0}$ |
| $\mathrm{APM}_{1}$ | 17 | $\mathrm{APM}_{1}$ |
| $\mathrm{APM}_{2}$ | 18 | $\mathrm{APM}_{2}$ |
| $\mathrm{APM}_{3}$ | 19 | $\mathrm{APM}_{3}$ |
| $\mathrm{APM}_{4}$ | 20 | $\mathrm{APM}_{4}$ |
| $\mathrm{APM}_{5}$ | 21 | $\mathrm{APM}_{5}$ |
| $\mathrm{APM}_{6}$ | 22 | APM $_{6}$ |
| $\mathrm{APM}_{7}$ | 23 | $\mathrm{APM}_{7}$ |
| APM8 | 24 | APM $_{8}$ |
| APM9 | 25 | APM9 |
| $\mathrm{APM}_{10}$ | 26 | $\mathrm{APM}_{10}$ |
| $\mathrm{APM}_{11}$ | 27 | $\mathrm{APM}_{11}$ |
| $\mathrm{APM}_{12}$ | 28 | APM 12 |
| n.c. | 29 | n.c. |
| VB | 30 | VB |
| $V_{p}$ | 31 | $V_{p}$ |
| 0 V | 32 | 0 V |

n.c. $=$ not connected

[^26]
## CENTRAL PROCESSOR

## DESCRIPTION

The central processor CP24 is for use with other PC20 modules, to assemble a programmable controller. The central processor is the heart of the PC20 controller; it requests data from the input modules, processes the data according to the instructions written in the program memory, and applies the results to the output modules. It also generates clock pulses for the controller.
The central processor block diagram is given in Fig. 1. The data processor controls the system and the complete timing. It includes the instruction decoder, the 1 -bit logic processor, the 4 -bit arithmetic processor and the data control.
The address processor generates addresses for the program memory under program control. It also generates addresses for the input and output modules.
The program memory is a C-MOS RAM (2k16). The CP24 has on-board battery back-up and a provision to connect an external battery for longer memory retention.
The capacity of the scratchpad memory is $1 / 1 / k 4$. Depending on the instruction the scratchpad memory can be addressed word by word (addresses run from 000 to 255) or bit by bit (addresses run from 000.0 to 255.3 ). In the latter case the address notation is, for example, 147.2 or 076.0. The on-board battery for data retention in the program memory RAM, is also used for data retention of the scratchpad memory.
The UDC-circuit (Up-Date and Check) controls the switch-on/off procedure; it informs the system of power failures. It also controls the access of the programming unit to the system memories.
The reset scratchpad memory circuit allows the central processor to set all scratchpad memory locations to zero, dependent on the RSME level, immediately after switch-on of the system.
The timer clock circuit provides 5 crystal-controlled timer clocks: $10 \mathrm{~ms}, 100 \mathrm{~ms}, 1 \mathrm{~s}, 10 \mathrm{~s}, 1 \mathrm{~min}$ (50\% duty factor).


Fig. 1 Block diagram.
Figure 2 illustrates the system operation. The system operates in four phases, which are continuously repeated. The phases, indicated by levels on outputs $\mathrm{PHC}_{0}$ and $\mathrm{PHC}_{1}$, are:

- up-date and check phase (UDC): $\mathrm{PHC}_{0}=0, \mathrm{PHC}_{1}=0$;
- reset scratchpad memory (RSM): $\mathrm{PHC}_{0}=1, \mathrm{PHC}_{1}=0$;
- data processing (DP): $\quad P \mathrm{PHC}_{0}=0, \mathrm{PHC}_{1}=1$;
- up-date input/output (I/O): $\quad \mathrm{PHC}_{0}=1, \mathrm{PHC}_{1}=1$.

Each central processor is built on an epoxy-glass printed-wiring board of $233,4 \mathrm{~mm} \times 160 \mathrm{~mm}$ (double Euro-card*). The board has two F068-I connectors (male parts); the corresponding female parts are on the back panels.

* For a general description of the Euro-card system see IEC297 or DIN41494 for 19-in racks and IEC 130-14 or DIN41612 for connectors.


Fig. 2 Flow chart. The UDC-phase and RSM-phase are only executed if required.

## ELECTRICAL DATA

## Supply

Supply voltage (d.c.)
current

$$
\begin{array}{ll}
V_{P} & 10 \mathrm{~V} \pm 10 \% \\
I_{P} & \max .250 \mathrm{~mA}
\end{array}
$$

Requirements of the external battery to retain the contents of the program memory and the scratchpad memory during power failure.

## Battery voltage

Battery current ( $\mathrm{V}_{\mathrm{P}}=0 \mathrm{~V}$ )
Trickle charge current ( $\mathrm{V}_{\mathrm{P}}=10 \mathrm{~V}$ )
Data retention with on-board battery at $40^{\circ} \mathrm{C}$

## Input and output data

The voltage levels of inputs and outputs are in accordance with standard LOCMOS specifications.

|  | function | terminations (Fig. 5) |  |
| :--- | :--- | :--- | :---: |
|  |  | connector 1 | connector 2 |

BI-DIRECTIONAL BUSSES


|  | function | terminations (Fig. 5) |  |  |
| :--- | :--- | :--- | :--- | :--- |
|  |  | connector 1 | connector 2 |  |
| INS $_{0}$ |  | $a 1$, | c1 |  |
| INS $_{1}$ | Instruction bus, interconnected with PU23; | $a 2$, | c2 |  |
| INS $_{2}$ | commanded by PDBE. | $a 3$, | c3 |  |
| INS $_{3}$ |  | $a 4$, | $c 4$ |  |
| INS $_{4}$ |  | a5, | c5 |  |

INPUTS

| ALI | Alarm input for internal use. Active HIGH: input current $=2 \mathrm{~mA}$. | a29, c29 |  |
| :---: | :---: | :---: | :---: |
| CPSD | Central processor slow down; input commanded by PU23. |  | a3, c3 |
| CPSI | Central processor stop initiate; command from PU23 stops central processor in UDC-phase (active HIGH). |  | a4, c4 |
| DEF | Data exchange finished; signal from output modules indicating that data from central processor has been stored (input current $=-5 \mathrm{~mA}$ ). | a25 |  |
| HOLD | Command from PU23 to stop central processor in DP-phase (active LOW). |  | a6, c6 |
| PABE | Program memory address bus enable; active during UDC-phase. When LOW APM bus functions as input. |  | a1, c1 |
| PDBE | Program memory data bus enable; active during UDC-phase. When LOW, INS and ADD-bus function as inputs. |  | a2, c2 |
| PRF | Preparation input/output modules finished. | a24 |  |
| $\overline{\mathrm{RCP}}$ | Reset central processor; resets data processor, address processor, UDC circuitry, RSM circuitry and timer clocks. Active LOW: input current $=4 \mathrm{~mA}$. |  | a12, c12 |
| RSME | Reset scratchpad memory enable. When HIGH or floating a reset of the scratchpad memory will occur during the first RSM-phase after switching on. When LOW (input current $=2 \mathrm{~mA}$ ) the RSM-phase is only effective for the scratchpad memory addresses 0 to 2 inclusive. |  | a10, c10 |
| $\overline{\mathrm{R}} / \mathrm{WPM}$ | Write signal from PU23 to central processor, to store data in program memory (active HIGH). |  | a14, c14 |


|  | function | terminations (Fig. 5) |  |
| :---: | :---: | :---: | :---: |
|  |  | connector 1 | connector 2 |
| R/WSM | Read-write level from input and output modules; only effective during I/O-phase. | c24 |  |
| WEPC | Write enable signal from PU23; prepares central processor to store data from PU23 into scratchpad memory. | c28 |  |
| WPSM | Write pulse for scratchpad memory; signal from PU23 to store data on $\mathrm{DIO}_{0-3}$ into scratchpad memory. |  | a13, c13 |
| OUTPUTS |  |  |  |
| APF | Address processing for input and output modules finished; address stable. | a26 |  |
| CLOCK | Clock output to PU23. |  | a7, c7 |
| CPSC | Central processor stop completed; command (HIGH) to PU23 indicating that central processor has been stopped in UDC-phase. |  | a5, c5 |
| $\begin{aligned} & \mathrm{PB}_{0} \\ & \mathrm{~PB}_{1} \end{aligned}$ | Page bits, connected to 0 V . | $\begin{aligned} & \text { a17 } \quad \text { c17 } \end{aligned}$ |  |
| $\begin{aligned} & \mathrm{PHC}_{0} \\ & \mathrm{PHC}_{1} \end{aligned}$ | Phase control to PU23 and input and output modules. | a23 c23 |  |
| $\overline{\mathrm{RCO}}$ | Reset output to output modules; becomes LOW during switch-on of the system, or if $\overline{\mathrm{RCP}}$ is LOW. When a wire jump has been inserted between the RCO points on the module (Fig. 3), $\overline{\mathrm{RCO}}$ output will also become LOW if $\mathrm{V}_{\mathrm{P}}<9 \mathrm{~V}$ or $>11 \mathrm{~V}$. | c27 |  |
| RR | Result Register, interconnected with PU23. | a18, c18 |  |
| SBI | Storage command to store data on data bus into output modules and PU23. | c26 |  |
| $\begin{aligned} & \text { SRI + } \\ & \text { SRI - } \end{aligned}$ | System run indication; Darlington transistor output, galvanically isolated by means of opto-coupler. SRI + = collector, SRI - = emitter. <br> When the system runs the transistor is non conducting; when the system stops the transistor switches on and off (see for circuit diagram, Fig. 4). | a30 c30 |  |

Fig. 3 Location of RCO points and jumper $A$ of the on-board battery.


Fig. 4 Circuit diagram of SRI output. Transistor conducting: $I_{Q}=\max .100 \mathrm{~mA}$, $\mathrm{V}_{\mathrm{CE}}<1,5 \mathrm{~V}$; transistor non-conducting: $\mathrm{I}_{\mathrm{Q}}=\max .10 \mu \mathrm{~A} ; \mathrm{V}_{\mathrm{CE}} \leqslant 30 \mathrm{~V}$; in case of system stop the output stage switches on and off with a cycle time of $0,4 \mathrm{~s}$.

Fixed scratchpad memory addresses

| address | description |
| :--- | :--- |
| 000.0 | Overflow bit for arithmetic operations. |
| 000.1 | Constant "1" level. |
| 000.2 | 24 V alarm output (becomes 1 if $\mathrm{V}_{\mathrm{S}} \leqslant 17,5 \mathrm{~V}$ ). |
| 000.3 | Timer clock 10 ms. |
| 001.0 | Timer clock 100 ms. |
| 001.1 | Timer clock 1 s. |
| 001.2 | Timer clock 10 s. |
| 001.3 | Timer clock 1 min. |

MECHANICAL DATA

## Outlines



Fig. 5.
Mass
approx. 270 g

## Notes

1. At delivery of the central processor the on-board battery is switched off (jumper A, Fig. 3, in offposition).
2. If the central processor is removed from the rack, ensure that it is put on an insulated surface to prevent short-circuiting of the on-board battery.

Terminal location

|  | ne |  |
| :---: | :---: | :---: |
| row c |  | row a |
| $\mathrm{INS}_{0}$ | 1 | $\mathrm{INS}_{0}$ |
| $\mathrm{INS}_{1}$ | 2 | $\mathrm{INS}_{1}$ |
| $\mathrm{INS}_{2}$ | 3 | $\mathrm{INS}_{2}$ |
| $\mathrm{INS}_{3}$ | 4 | $\mathrm{INS}_{3}$ |
| $\mathrm{INS}_{4}$ | 5 | $\mathrm{INS}_{4}$ |
| $\mathrm{ADD}_{0}$ | 6 | $\mathrm{ADD}_{0}$ |
| $\mathrm{ADD}_{1}$ | 7 | $\mathrm{ADD}_{1}$ |
| $\mathrm{ADD}_{2}$ | 8 | $\mathrm{ADD}_{2}$ |
| $\mathrm{ADD}_{3}$ | 9 | $\mathrm{ADD}_{3}$ |
| $\mathrm{ADD}_{4}$ | 10 | $\mathrm{ADD}_{4}$ |
| $\mathrm{ADD}_{5}$ | 11 | $\mathrm{ADD}_{5}$ |
| $\mathrm{ADD}_{6}$ | 12 | $\mathrm{ADD}_{6}$ |
| $\mathrm{ADD}_{7}$ | 13 | $\mathrm{ADD}_{7}$ |
| $\mathrm{ADD}_{8}$ | 14 | $\mathrm{ADD}_{8}$ |
| ADD9 | 15 | ADD9 |
| ADD10 | 16 | ADD 10 |
| $\mathrm{PB}_{1}$ | 17 | $\mathrm{PB}_{0}$ |
| RR | 18 | RR |
| $\mathrm{DIO}_{0}$ | 19 | $\mathrm{DIO}_{0}$ |
| $\mathrm{DIO}_{1}$ | 20 | $\mathrm{DIO}_{1}$ |
| $\mathrm{DIO}_{2}$ | 21 | $\mathrm{DIO}_{2}$ |
| $\mathrm{DIO}_{3}$ | 22 | $\mathrm{DIO}_{3}$ |
| $\mathrm{PHC}_{0}$ | 23 | $\mathrm{PHC}_{1}$ |
| R/WSM | 24 | PRF |
| 0 V * | 25 | DEF |
| SBI | 26 | APF |
| $\overline{\mathrm{RCO}}$ | 27 | n.c. |
| WEPC | 28 | n.c. |
| ALI | 29 | ALI |
| SRI- | 30 | SRI + |
| $V_{p}$ | 31 | $V_{p}$ |
| 0 V | 32 | 0 V |

connector 2
row c row a

| PABE | 1 | PABE |
| :---: | :---: | :---: |
| PDBE | 2 | PDBE |
| CPSD | 3 | CPSD |
| CPSI | 4 | CPSI |
| CPSC | 5 | CPSC |
| HOLD | 6 | HOLD |
| CLOCK | 7 | CLOCK |
| n.c. | 8 | n.c. |
| n.c. | 9 | n.c. |
| RSME | 10 | RSME |
| n.c. | 11 | n.c. |
| $\overline{\mathrm{RCP}}$ | 12 | $\overline{\mathrm{RCP}}$ |
| WPSM | 13 | WPSM |
| $\overline{\mathrm{R}} / \mathrm{WPM}$ | 14 | $\overline{\mathrm{R}} / \mathrm{WPM}$ |
| n.c. | 15 | n.c. |
| $\mathrm{APM}_{0}$ | 16 | $\mathrm{APM}_{0}$ |
| $\mathrm{APM}_{1}$ | 17 | $\mathrm{APM}_{1}$ |
| $\mathrm{APM}_{2}$ | 18 | $\mathrm{APM}_{2}$ |
| $\mathrm{APM}_{3}$ | 19 | $\mathrm{APM}_{3}$ |
| $\mathrm{APM}_{4}$ | 20 | $\mathrm{APM}_{4}$ |
| $\mathrm{APM}_{5}$ | 21 | $\mathrm{APM}_{5}$ |
| APM $_{6}$ | 22 | $\mathrm{APM}_{6}$ |
| $\mathrm{APM}_{7}$ | 23 | $\mathrm{APM}_{7}$ |
| APM 8 | 24 | $\mathrm{APM}_{8}$ |
| APM9 | 25 | APM9 |
| APM 10 | 26 | $\mathrm{APM}_{10}$ |
| $\mathrm{APM}_{11}$ | 27 | $\mathrm{APM}_{11}$ |
| $\mathrm{APM}_{12}$ | 28 | $\mathrm{APM}_{12}$ |
| n.c. | 29 | n.c. |
| VB | 30 | VB |
| $V_{p}$ | 31 | $V_{p}$ |
| 0 V | 32 | 0 V |

* No supply line; is used as return line for control signals.


## INPUT MODULES

## DESCRIPTION

These input modules are used with the other PC20 modules to assemble a programmable controller. The IM20 and IM23 are for 24 V and 48 V input levels resp.; both modules can be adapted to drive from 5 V input levels.
The modules contain 16 addressable input stages, with photo-isolators between external and internal circuitry (Fig. 1). All inputs are floating with respect to each other. Each input stage has a LED for status indication: it is lit when the input is active. Furthermore, to limit power consumption, these LEDs can be switched-off. A delay circuit (symmetrical delay time typ. 1 ms ) is incorporated in each input stage to increase the noise immunity. The delay time can be increased by adding extra capacitance.


Fig. 1 Circuit diagram of an input stage.

Each input module has 11 address inputs ( $A D D D_{0-10}$ ) and 9 module identification inputs ( $\mathrm{MID}_{2-10}$ ), which are accessible on the connectors at the rear (Fig. 2).


Fig. 2 Block diagram of the input module.
The circuit is built on an epoxy-glass printed-wiring board of $233,4 \mathrm{~mm} \times 160 \mathrm{~mm}$ (double Eurocard). The board has two F068-I connectors (board parts); the corresponding rack part of connector 1 (Fig. 4) is available on the back panels, that of connector 2 (external connections) is separately available under catalogue number 242202589291 (pins for wire wrapping), 242202589299 (pins for dip-soldering) or 242202589327 (solder tags).*

* For a general description of the Eurocard system see IEC 297 or DIN 41494 for 19-in racks and IEC 130-14 or DIN 41612 for connectors.


## ELECTRICAL DATA

## Supply

Supply voltage (d.c.)
current
$V_{p} \quad 10 \mathrm{~V} \pm 10 \%$
typ. 45 mA (all inputs inactive)
Ip typ. 175 mA (all inputs active) max. 200 mA (all inputs active)

## Input data

The data inputs are $\mathrm{Dl}_{\mathrm{W} .0}$ to $\mathrm{Dl}_{\mathrm{W} .3} \mathrm{DI}_{\mathrm{X} .0}$ to $\mathrm{DI}_{\mathrm{X} .3}$, $\mathrm{Dl}_{\mathrm{Y} .0}$ to $\mathrm{Dl}_{\mathrm{Y} .3}$ and $\mathrm{DI}_{\mathrm{Z.} .0}$ to $\mathrm{DI}_{\mathrm{Z.3}}$. They are accessible on connector 2 , see "Terminal location".
$\left.\begin{array}{l}\text { Active voltage }\left(\mathrm{V}_{\mathrm{a}-\mathrm{c}}\right) \\ \text { Non-active voltage }\left(\mathrm{V}_{\mathrm{a}-\mathrm{c}}\right)\end{array}\right\}$ note 1

Input current, active

| IM20 | IM23 | 5 V level (note 2) |
| :--- | :--- | :--- |
| 17 to 30 V | 35 to 60 V | 3,5 to 6 V |
| 0 to 7 V or | 0 to 10 V or | 0 to $0,8 \mathrm{~V}$ or |
| floating | floating | floating |
| typ. 10 mA | typ. $5,5 \mathrm{~mA}$ | typ. 10 mA |
| (at $\mathrm{V}_{\mathrm{a}-\mathrm{c}}=24 \mathrm{~V}$ ) | (at $\mathrm{V}_{\mathrm{a}-\mathrm{c}}=48 \mathrm{~V}$ ) | (at $\mathrm{V}_{\mathrm{a}-\mathrm{c}}=5 \mathrm{~V}$ ) |

The delay time of the deiay circuit can be increased by inserting capacitors (approx. 0,015 $\mu \mathrm{F} / \mathrm{ms}$ ) between connecting points B and $\mathrm{B}^{\prime}$ (Fig. 3).

## Notes

1. $\mathrm{V}_{\mathrm{a}-\mathrm{c}}$ is the voltage between terminal of row a and terminal of row c of connector 2.
2. For 5 V -level operation a resistor of $360 \Omega \pm 5 \%$, style CR25, has to be connected to each input stage between connecting points $A$ and $A^{\prime}$ (Fig. 3).


Fig. 3 Part of the printed-wiring board, showing the connecting points for the additional delay capacitors and the resistors for 5 V -level operation.

The inputs mentioned below meet the standard LOCMOS specifications.

| input | function | terminations of connector 1 (Fig. 4) |
| :---: | :---: | :---: |
| $\begin{aligned} & \mathrm{ADD}_{0} \\ & \mathrm{ADD}_{1} \\ & \mathrm{ADD}_{2} \\ & \mathrm{ADD}_{3} \\ & \mathrm{ADD}_{4} \\ & \mathrm{ADD}_{5} \\ & \mathrm{ADD}_{6} \\ & \mathrm{ADD}_{7} \\ & \mathrm{ADDD}_{8} \\ & \mathrm{ADDD}_{9} \\ & \mathrm{ADD}_{10} \end{aligned}$ | Address bits from central processor: ADD $_{0-1}$ select a group of 4 input stages, $A_{2-10}$ select the input module. | a11 $c 11$ <br> a12 $c 12$ <br> a13 $c 13$ <br> a14 $c 14$ <br> a15 $c 15$ <br>  $c 16$ |
| APF | Handshake signal; input/output address correct. | a26 |
| $\overline{\text { ILD }}$ | Indication LED disable; input current LOW: 0,1 mA | c28 |
| $\mathrm{MID}_{2}$ <br> MID3 <br> MID4 <br> $\mathrm{MID}_{5}$ <br> $\mathrm{MID}_{6}$ <br> $\mathrm{MID}_{7}$ <br> MID8 <br> MID9 <br> MID10 | Module identification inputs; provide module with individual identity. | $\begin{aligned} & \mathrm{c} 2 \\ & \mathrm{c} 3 \\ & \mathrm{c} 4 \\ & \mathrm{c5} \\ & \mathrm{c} 6 \\ & \mathrm{c} 7 \\ & \mathrm{c} 8 \\ & \mathrm{c} 9 \\ & \mathrm{c} 10 \end{aligned}$ |
| $\begin{aligned} & \mathrm{PHC}_{0} \\ & \mathrm{PHC}_{1} \end{aligned}$ | Phase control signals. | a23 c23 |

## Output data

All outputs meet the standard LOCMOS specifications, except the R/W and PRF outputs.

| output | function | terminations of <br> connector 1 (Fig. 4) |  |
| :--- | :--- | :--- | :--- |
| $\mathrm{DIO}_{0}$ <br> $\mathrm{DIO}_{1}$ <br> $\mathrm{DIO}_{2}$ <br> $\mathrm{DIO}_{3}$ | Data bits to central processor; data is stored <br> in scratchpad memory of central processor. | c21 |  |
| PRF | Preparation of input module finished (open collector <br> output). | a24 | c22 |
| $\mathrm{R} / \overline{\mathrm{W}}$ | Signal to central processor (active LOW); <br> prepares central processor for data on DIO <br> to be written in the scratchpad memory <br> (open collector output). | c24 |  |

Outlines


Fig. 4.
Mass $\quad 250 \mathrm{~g}$

Terminal location

| connector 1 |  |  |  | connector 2 |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| row c | row a |  |  | row c |  | row a |
| n.c. | 1 | HIGH level |  | DIW. 0 | 2 | DIW. 0 |
| MID2 | 2 | HIGH level |  | DIW. 1 | 4 | DIW. 1 |
| MID3 | 3 | HIGH level |  | DIW. 2 | 6 | DIW. 2 |
| MID4 | 4 | HIGH level |  | DIW. 3 | 8 | DIW. 3 |
| MID5 | 5 | HIGH level | ** | DIX. 0 | 10 | DIX. 0 |
| MID6 | 6 | HIGH level |  | DIX. 1 | 12 | DIX. 1 |
| MID7 | 7 | HIGH level |  | DIX. 2 | 14 | DIX. 2 |
| MID8 | 8 | HIGH level |  | DIX. 3 | 16 | DIX. 3 |
| MID9 | 9 | HIGH level |  | DIY. 0 | 18 | DIY. 0 |
| MID10 | 10 | HIGH level |  | Dly. 1 | 20 | DIY. 1 |
| $\mathrm{ADD}_{0}$ | 11 | $\mathrm{ADD}_{1}$ |  | DIY. 2 | 22 | DIY. 2 |
| $\mathrm{ADD}_{2}$ | 12 | $\mathrm{ADD}_{3}$ |  | DIY. 3 | 24 | Dly. 3 |
| $\mathrm{ADD}_{4}$ | 13 | $\mathrm{ADD}_{5}$ |  | DIZ.0 | 26 | DIZ.0 |
| $\mathrm{ADD}_{6}$ | 14 | $\mathrm{ADD}_{7}$ |  | DIZ. 1 | 28 | DIZ. 1 |
| $\mathrm{ADD}_{8}$ | 15 | ADD9 |  | DIZ. 2 | 30 | DIZ. 2 |
| ADD10 | 16 | n.c. |  | DIZ.3 | 32 | DIZ.3 |
| n.c. | 17 | n.c. |  |  |  |  |
| n.c. | 18 | n.c. |  |  |  |  |
| n.c. | 19 | n.c. |  |  |  |  |
| n.c. | 20 | n.c. |  |  |  |  |
| $\mathrm{DIO}_{0}$ | 21 | $\mathrm{DIO}_{1}$ |  |  |  |  |
| $\mathrm{DIO}_{2}$ | 22 | $\mathrm{DIO}_{3}$ |  |  |  |  |
| PHCO | 23 | $\mathrm{PHC}_{1}$ |  |  |  |  |
| R/W | 24 | PRF |  |  |  |  |
| $0 \mathrm{~V}^{*}$ | 25 | n.c. |  |  |  |  |
| n.c. | 26 | APF |  |  |  |  |
| n.c. | 27 | n.c. |  |  |  |  |
| ILD | 28 | n.c. |  |  |  |  |
| n.c. | 29 | n.c. |  |  |  |  |
| n.c. | 30 | n.c. |  |  |  |  |
| $V_{P}$ | 31 | $V_{p}$ |  |  |  |  |
| 0 V | 32 | 0 V |  |  |  |  |

n.c. $=$ not connected.

* No supply line; is used as return line for control signals.
** For coding MID lines.


## INPUT MODULE

## DESCRIPTION

This input module is used with the other PC20 modules to assemble a programmable controller.
The input module contains 32 addressable input stages, with photo-isolators between external and internal circuitry (Fig. 1). All inputs are floating with respect to each other. The module has 16 LEDs for status indication; with the switch on the front panel they can be connected whether to the 16 inputs with the lowest addresses or to the 16 inputs with the highest addresses. The LEDs are lit when the input stage is active. When the switch is in its middle position all LEDs are switched-off.

A delay circuit (symmetrical delay time typ. 1 ms ) is incorporated in each input stage to increase the noise immunity.


Fig. 1 Circuit diagram of an input stage.

The input module has 11 address inputs ( $\mathrm{ADD}_{0-10}$ ) and 8 module identification inputs ( $\mathrm{MID}_{3-10}$ ), which are accessible on the connectors at the rear (Fig. 2).


Fig. 2 Block diagram of the input module.
The circuit is built on an epoxy-glass printed-wiring board of $233,4 \mathrm{~mm} \times 160 \mathrm{~mm}$ (double Eurocard).
The board has two F068-I connectors (board parts); the corresponding rack part of connector 1 (Fig. 4) is available on the back panels, that of connector 2 (external connections) is separately available under catalogue number 242202589288 (pins for wire wrapping), 242202589298 (pins for dip-soldering) or 242202589326 (solder tags).*

## ELECTRICAL DATA

supply

Supply voltage (d.c.)
Supply current

Vp $\quad 10 \mathrm{~V} \pm 10 \%$
Ip typ. 3 mA (all inputs inactive) typ. 140 mA (all inputs active) max. 175 mA (all inputs active)

## Input data

 $\mathrm{DI}_{\mathrm{X} .0}$ to $\mathrm{DI}_{\mathrm{X} .3 \text {, }} \mathrm{DI}_{\mathrm{Y} .0}$ to $\mathrm{Dl}_{\mathrm{Y} .3}$ and $\mathrm{DI}_{\mathrm{Z} .0}$ to $\mathrm{DI}_{\mathrm{Z} .3}$. They are accessible on connector 2, see "Terminal location".

| $\left.\begin{array}{l}\text { Active voltage }\left(\mathrm{V}_{\mathrm{a}-\mathrm{c}}\right) \\ \text { Non-active voltage }\left(\mathrm{V}_{\mathrm{a}-\mathrm{c}}\right)\end{array}\right\}^{* *}$ | 17 to 30 V <br> Input current, active at $\mathrm{V}_{\mathrm{a}-\mathrm{c}}=24 \mathrm{~V}$ |
| :--- | :--- |
| 0 to 7 V or floating <br> typ. 10 mA |  |

* For a general description of the Eurocard system see IEC 297 or DIN 41494 for 19-in racks and IEC 130-14 or DIN 41612 for connectors.
** $\mathrm{V}_{\mathrm{a}-\mathrm{c}}$ is the voltage between terminal of row a and terminal of row c of connector 2.

The inputs mentioned below meet the standard LOCMOS specifications.

| input | function | terminations of connector 1 (Fig. 3) |
| :---: | :---: | :---: |
|  | Address bits from central processor; ADD $_{0-2}$ select a group of 4 input stages, ADD $_{3-10}$ select the input module. | a11 c11 <br> a12 c12 <br> a13 c13 <br> a14 c 14 <br> a15 c 15 <br>  c 16 |
| APF | Handshake signal; input/output address correct. | a26 |
| $\mathrm{MID}_{3}$ <br> $\mathrm{MID}_{4}$ <br> MID $_{5}$ <br> MID $_{6}$ <br> MID7 <br> $\mathrm{MID}_{8}$ <br> MID9 <br> MID $_{10}$ | Module identification inputs; provide module with individual identity. | c3 <br> c4 <br> c5 <br> c6 <br> c7 <br> c8 <br> c9 <br> c10 |
| $\begin{aligned} & \mathrm{PHC}_{0} \\ & \mathrm{PHC}_{1} \\ & \hline \end{aligned}$ | Phase control signals. | a23 c23 |

## Output data

All outputs meet the standard LOCMOS specifications, except the R/W and PRF outputs.

| output | function | terminations of connector 1 (Fig. 3) |
| :---: | :---: | :---: |
| $\begin{aligned} & \mathrm{DIO}_{0} \\ & \mathrm{DIO}_{1} \\ & \mathrm{DIO}_{2} \\ & \mathrm{DIO}_{3} \end{aligned}$ | Data bits to central processor; data is stored in scratchpad memory of central processor. |  c21 <br> a21 c22 <br> a22  |
| PRF | Preparation of input module finished (open collector output). | a24 |
| $\mathrm{R} / \mathrm{W}$ | Signal to central processor (active LOW); prepares central processor for data on $\mathrm{DIO}_{0-3}$ to be written in the scratchpad memory (open collector output). | c24 |

MECHANICAL DATA
Dimensions in mm

## Outlines



Fig. 3.

[^27]Terminal location

n.c. $=$ not connected.

* No supply line; is used as return line for control signals.
** For coding MID lines.


## ANALOGUE TO DIGITAL MODULE

## DESCRIPTION

This analogue input module is for use with other PC20 modules to assemble a programmable controller. With this module 8 analogue input signals can be processed in a PC20 system.

Analogue to digital conversion is achieved by a 10 -bit $\mathrm{A} / \mathrm{D}$ converter, using the successive approximation technique.
The module converts analogue voltages from 0 to 10 V and currents from 0 to 20 mA or 4 to 20 mA into 312 -digit BCD values from 0000 to 1000 , representing 0 to $1000 \%$ of the input range. The most significant digit of the values is represented by 1 bit (13th bit). To store these values into the scratchpad memory of the central processor 4 addresses per input channel have to be reserved (see Fig. 1), that means an address area of max. 32 addresses for 8 inputs. The module has 3 channel select inputs $\left(\mathrm{CHS}_{0}, 1,2\right)$ with which the number of analogue inputs to be scanned can be selected. See Table 1 for connection of the CHS inputs and the influence on the address range of the module.

|  | $m$ | $m+1$ | $m+2$ | $m+3$ |  |
| :--- | :---: | :---: | :---: | :---: | :--- |
| 3 |  |  |  |  |  |
| 2 |  |  |  |  |  |
| 1 |  |  |  |  |  |
| 0 | MSB |  |  |  |  |
|  |  | MSD |  | LSD |  |

Fig. 1.
$m=$ multiple of 4
$\mathrm{m}_{0}=$ MSB (13th bit)
$\mathrm{m}_{1}=0$ no assignment
$\mathrm{m}_{2}=1$ if analogue voltage $<10 \mathrm{mV}$ (out of range indication)
$m_{3}=1$ if analogue voltage $>10,2 \mathrm{~V}$ (out of range indication)
Table 1

| channel to be <br> scanned | $\mathrm{CHS}_{0}$ <br> $\left(\mathrm{SClO}_{0}\right)^{*}$ | $\mathrm{CHS}_{1}$ <br> $\left(\mathrm{SClO}_{1}\right)^{*}$ | $\mathrm{CHS}_{2}$ <br> $\left(\mathrm{SClO}_{2}\right)^{*}$ | address range of AD 20 <br> 32 .n $+\ldots$ (see below) |
| :--- | :---: | :---: | :---: | :---: |
| 0 to 7 | 0 | 0 | 0 | 0 to 31 |
| 1 to 7 | 1 | 0 | 0 | 4 to 31 |
| 2 to 7 | 0 | 1 | 0 | 8 to 31 |
| 3 to 7 | 1 | 1 | 0 | 12 to 31 |
| 4 to 7 | 0 | 0 | 1 | 16 to 31 |
| 5 to 7 | 1 | 0 | 1 | $n=1$ to 7 for CP20, CP21, CP24; |
| 6 and 7 | 0 | 1 | 1 | 20 to 31 |
| 7 | 1 | 1 | 1 | 28 to 31 |

[^28]The address range is determined by the coding on the module identification inputs $\mathrm{MID}_{5-10}$. If less then 8 analogue input channels are used, the module must be regarded as a complete module for the MID-coding; the addresses which are not used may be occupied by other input/output modules.
The analogue input circuit contains a double-pole multiplexer with 8 inputs, an operational amplifier with 3 gain settings ( 1,10 and 12,5), a $-2,5 \mathrm{~V}$ reference voltage, and an A/D converter, see Fig. 2.
Resistors ( $50 \Omega$ ) are provided for each input to be connected in parallel with the input terminals (terminals $\mathrm{Al}_{0-7}$ + to be connected to terminals $\mathrm{R}_{0-7}$ ), to obtain both input ranges 0 to 20 mA and 4 to 20 mA . Jumpers are provided for adjustment of the module to the required range; see ADJUSTMENTS FOR OPERATION.


Fig. 2.
The operational amplifier needs a return path for the bias currents, which can be established by connecting terminal AG of the module to the common or earth terminal of the voltage/current input source. An example is shown in Fig. 3.


Fig. 3.
The analogue part is electrically isolated from the logic part by means of optocouplers. A d.c./d.c. converter with electrical isolation is provided on the module to generate the required supply voltages for the analogue part, providing complete isolation of the analogue part from both input circuit supply ( $\mathrm{V}_{\mathrm{S}}$ ) and logic supply ( $\mathrm{V}_{\mathrm{p}}$ ).

After the AD20 (in a PC20 system) has been switched on the module starts scanning the analogue input with the lowest number, dependent on the selection made on the CHS inputs, and stores the value in a buffer memory. The module continues scanning the other channels, and after channel 7 has been scanned it switches over to data exchange with the scratchpad memory of the central processor. When the data exchange has been finished a new scanning of the analogue inputs starts.

The scanning time per channel is $100 \mu \mathrm{~s}$. When the time between end of scanning and data exchange exceeds 100 ms the module automatically starts a new scanning.
The module has a 3-digit display that enables monitoring of the inputs; channel selection is done with the thumbwheel switch. The display gives a 3-digit number without a decimal point. As the AD20 handles analogue input voltages up to $10,23 \mathrm{~V}(31 / 2$-digit) the $1 / 2$ digit is represented by 3 decimal points, so values greater than 999 are displayed as x.x.x.

The whole circuitry is built on an epoxy printed-wiring board of $233,4 \mathrm{~mm} \times 160 \mathrm{~mm}$ (double Eurocard). The board has two F068-I connectors (board parts); the corresponding rack part of connector 1 (Fig. 5) is available on the back panels, that of connector 2 (external connections) is separately available under catalogue number 242202589288 (pins for wire wrapping), 242202589298 (pins for dip-soldering) or 242202589326 (solder tags).*

## ELECTRICAL DATA

|  | $\begin{aligned} & \mathrm{V}_{\mathrm{S}} \\ & \mathrm{I}_{\mathrm{S}} \end{aligned}$ | $\begin{aligned} & 24 \mathrm{~V} \pm 25 \% \\ & \max .90 \mathrm{~mA} \end{aligned}$ |
| :---: | :---: | :---: |
| $\left.\begin{array}{l}\text { Supply voltage (d.c.) } \\ \text { Supply current }\end{array}\right\}$ logic,$~$ | $\begin{aligned} & V_{p} \\ & I_{p} \end{aligned}$ | $\begin{aligned} & 10 \mathrm{~V} \pm 10 \% \\ & \max .120 \mathrm{~mA} \end{aligned}$ |
| Current input (input impedance $50 \Omega \pm 0,1 \%$ ) | 0 to 20 mA or 4 to 20 mA |  |
| Voltage input (input impedance $\geqslant 10 \mathrm{M} \Omega$ ) | 0 to 10 V |  |
| Accuracy | max. error | max. temp. coefficient |
| 0 to 10 mV range | $\pm 0,1 \%$ | $+30 \times 10^{-6} / \mathrm{K}$ |
| 0 to 20 mA range | $\pm 0,4 \%$ | $+60 \times 10^{-6} / \mathrm{K}$ |
| 4 to 20 mA range | $\pm 0,4 \%$ | $+60 \times 10^{-6} / \mathrm{K}$ |
| differential non-linearity | max. 0,1\% |  |
| Maximum voltage between inputs and analogue ground (terminal AG) | $\pm 15 \mathrm{~V}$ |  |

[^29]
## Input and output data

All inputs and outputs, except the PRF and R/WTSM outputs meet the standard LOCMOS specifications.

|  | function | terminations of <br> connector 1 (Fig. 5) |
| :--- | :--- | :--- |

INPUTS

| $\mathrm{ADD}_{0}$ | Address bits from central processor. |  | c11 |
| :---: | :---: | :---: | :---: |
| $\mathrm{ADD}_{1}$ |  | a11 |  |
| $\mathrm{ADD}_{2}$ |  |  | c12 |
| $\mathrm{ADD}_{3}$ |  | a12 |  |
| $\mathrm{ADD}_{4}$ |  |  | c13 |
| $\mathrm{ADD}_{5}$ |  | a13 |  |
| $\mathrm{ADD}_{6}$ |  |  | c14 |
| $\mathrm{ADD}_{7}$ |  | a14 |  |
| $\mathrm{ADD}_{8}$ |  |  | c15 |
| ADD9 |  | a15 |  |
| ADD 10 |  |  | c16 |
| APF | Handshake signal, indicates that addresses are correct. | a26 |  |
| $\mathrm{CHS}_{0}$ |  |  | c17 |
| $\mathrm{CHS}_{1}$ | Channel select inputs. |  | c18 |
| $\mathrm{CHS}_{2}$ |  |  | c19 |
| MID ${ }_{5}$ |  |  | c5 |
| MID 6 |  |  | c6 |
| $\mathrm{MID}_{7}$ | Module identification inputs; provide module with |  | c7 |
| MID8 | individual identity. |  | c8 |
| MID9 |  |  | c9 |
| MID 10 |  |  | c10 |
| $\begin{aligned} & \mathrm{PHC}_{0} \\ & \mathrm{PHC}_{1} \end{aligned}$ | Phase control signals. | a23 | c23 |
| $\overline{\mathrm{RCO}}$ | Reset from central processor |  | c27 |

OUTPUTS

| $\mathrm{DIO}_{0}$ <br> $\mathrm{DIO}_{1}$ <br> $\mathrm{DIO}_{2}$ <br> $\mathrm{DIO}_{3}$ | Data bits to central processor. | $\begin{aligned} & \text { a21 } \\ & \text { a22 } \end{aligned}$ | $\begin{aligned} & \text { c21 } \\ & \text { c22 } \end{aligned}$ |
| :---: | :---: | :---: | :---: |
| PRF | Preparation of addressing AD20 finished (open collector output). | a24 |  |
| R//WSM | Read-write level for central processor (open collector output). | a26 |  |

AD20

|  | function | terminations of <br> connector 2 (Fig. 5) |
| :--- | :--- | :--- |

ANALOGUE INPUTS

| $\begin{aligned} & \mathrm{Al}_{0}+ \\ & \mathrm{Al}_{0}- \\ & \mathrm{R}_{0} \\ & \mathrm{AG} \end{aligned}$ | Positive terminal <br> Negative terminal <br> $50 \Omega$ input resistor terminal <br> Analogue ground | $\begin{aligned} & \text { a10 } \\ & \text { a9 } \end{aligned}$ | $\begin{aligned} & \text { c10 } \\ & \text { c8/c9 } \end{aligned}$ |
| :---: | :---: | :---: | :---: |
| $\begin{aligned} & \mathrm{Al}_{1}+ \\ & \mathrm{Al}_{1}- \\ & \mathrm{R1} \\ & \mathrm{AG} \end{aligned}$ | Positive terminal <br> Negative terminal <br> $50 \Omega$ input resistor terminal <br> Analogue ground | a12 <br> a11 | c12 <br> c11 |
| $\begin{aligned} & \mathrm{Al}_{2}{ }^{+} \\ & \mathrm{Al}_{2}- \\ & \mathrm{R2} \\ & \mathrm{AG} \end{aligned}$ | Positive terminal <br> Negative terminal <br> $50 \Omega$ input resistor terminal <br> Analogue ground | a14 <br> a13 | c14 $\mathrm{c} 13$ |
| $\begin{aligned} & \mathrm{Al}_{3}+ \\ & \mathrm{Al}_{3}- \\ & \mathrm{R} 3 \\ & \mathrm{AG} \end{aligned}$ | Positive terminal <br> Negative terminal <br> $50 \Omega$ input resistor terminal <br> Analogue ground | a16 <br> a15 | $\begin{aligned} & \text { c16 } \\ & \text { c15 } \end{aligned}$ |
| $\begin{aligned} & \mathrm{Al}_{4}+ \\ & \mathrm{Al}_{4}- \\ & \mathrm{R4} \\ & \mathrm{AG} \end{aligned}$ | Positive terminal <br> Negative terminal <br> $50 \Omega$ input resistor terminal <br> Analogue ground | a18 <br> a17 | c18 c17 |
| $\mathrm{Al}_{5}{ }^{+}$ <br> $\mathrm{Al}_{5}$ - <br> R5 <br> AG | Positive terminal <br> Negative terminal <br> $50 \Omega$ input resistor terminal <br> Analogue ground | $\begin{aligned} & \text { a20 } \\ & \text { a19 } \end{aligned}$ | c20 c19 |
| $\begin{aligned} & \mathrm{Al}_{6}{ }^{+} \\ & \mathrm{Al}_{6}- \\ & \mathrm{R} 6 \\ & \mathrm{AG} \end{aligned}$ | Positive terminal <br> Negative terminal <br> $50 \Omega$ input resistor terminal <br> Analogue ground | $\begin{aligned} & \text { a22 } \\ & \text { a21 } \end{aligned}$ | $\begin{aligned} & \text { c22 } \\ & \text { c21 } \end{aligned}$ |
| $\begin{aligned} & \mathrm{Al}_{7}+ \\ & \mathrm{Al}_{7}- \\ & \mathrm{R} 7 \\ & \mathrm{AG} \end{aligned}$ | Positive terminal <br> Negative terminal <br> $50 \Omega$ input resistor terminal <br> Analogue ground | $\begin{aligned} & \text { a24 } \\ & \text { a23 } \end{aligned}$ | $\begin{aligned} & \text { c24 } \\ & \text { c23/c26 } \end{aligned}$ |

## ADJUSTMENTS FOR OPERATION

The input range can be selected by positioning the jumpers $A$ and $B$ (Fig. 4) as shown below.

| input range | position of jumpers A | position of jumper B | relation between measured value and data (D) stored in scratchpad memory |
| :---: | :---: | :---: | :---: |
| 0 to 10 V | $\begin{array}{\|l\|l\|} \hline 0 \\ 0 & 0 \\ 0 \end{array}$ |  | $\mathrm{D}=100 \mathrm{Vi}$ |
| 0 to 20 mA | 0 0 |  | $\mathrm{D}=50 \mathrm{li}$ |
| 4 to 20 mA | 0 0 | 0 | $D=62,5(1 i-4)$ |

830718-20-01

Fig. 4 Location of jumpers for adjustment of input range.


## MECHANICAL DATA

Dimensions in mm

## Outlines



Fig. 5.

Terminal location

| connector 1 |  |  |  | connector 2 |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| row c | row a |  |  | row c |  | row a |
| n.c. | 1 | n.c. |  | n.c. | 1 | n.c. |
| n.c. | 2 | n.c. |  | n.c. | 2 | n.c. |
| n.c. | 3 | n.c. |  | n.c. | 3 | n.c. |
| n.c. | 4 | n.c. |  | n.c. | 4 | n.c. |
| MID5 | 5 | HIGH level |  | n.c. | 5 | n.c. |
| MID6 | 6 | HIGH level |  | n.c. | 6 | n.c. |
| $\mathrm{MID}_{7}$ | 7 | HIGH level | * | n.c. | 7 | n.c. |
| $\mathrm{MID}_{8}$ | 8 | HIGH level |  | AG | 8 | n.c. |
| MIDg | 9 | HIGH level |  | AG | 9 | $\mathrm{R}_{0}$ |
| MID 10 | 10 | HIGH level |  | $\mathrm{Al}_{0}-$ | 10 | $\mathrm{Al}_{0}+$ |
| $\mathrm{ADD}_{0}$ | 11 | $\mathrm{ADD}_{1}$ |  | AG | 11 | $\mathrm{R}_{1}$ |
| $\mathrm{ADD}_{2}$ | 12 | $\mathrm{ADD}_{3}$ |  | $\mathrm{Al}_{1}-$ | 12 | $\mathrm{Al}_{1}{ }^{+}$ |
| $\mathrm{ADD}_{4}$ | 13 | $\mathrm{ADD}_{5}$ |  | AG | 13 | $\mathrm{R}_{2}$ |
| $\mathrm{ADD}_{6}$ | 14 | $\mathrm{ADD}_{7}$ |  | $\mathrm{Al}_{2}$ - | 14 | $\mathrm{Al}_{2}{ }^{+}$ |
| $\mathrm{ADD}_{8}$ | 15 | ADDg |  | AG | 15 | $\mathrm{R}_{3}$ |
| $\mathrm{ADD}_{10}$ | 16 | n.c. |  | $\mathrm{Al}_{3}^{-}$ | 16 | $\mathrm{Al}_{3}+$ |
| $\mathrm{CHS}_{0}$ | 17 | HIGH level |  | AG | 17 | $\mathrm{R}_{4}$ |
| $\mathrm{CHS}_{1}$ | 18 | HIGH level | - | $\mathrm{Al}_{4}^{-}$ | 18 | $\mathrm{Al}_{4}{ }^{+}$ |
| $\mathrm{CHS}_{2}$ | 19 | HIGH level |  | AG | 19 | $\mathrm{R}_{5}$ |
| n.c. | 20 | n.c. |  | $\mathrm{Al}_{5}^{-}$ | 20 | $\mathrm{Al}_{5}+$ |
| $\mathrm{DIO}_{0}$ | 21 | $\mathrm{DIO}_{1}$ |  | AG | 21 | $\mathrm{R}_{6}$ |
| $\mathrm{DIO}_{2}$ | 22 | $\mathrm{DiO}_{3}$ |  | $\mathrm{Al}_{6}-$ | 22 | $\mathrm{Al}_{6}+$ |
| $\mathrm{PHC}_{0}$ | 23 | $\mathrm{PHC}_{1}$ |  | AG | 23 | $\mathrm{R}_{7}$ |
| R/WSM | 24 | PRF |  | $\mathrm{Al}_{7}-$ | 24 | $\mathrm{Al}_{7}+$ |
| 0 V * | 25 | n.c. |  | n.c. | 25 | n.c. |
| n.c. | 26 | APF |  | AG | 26 | n.c. |
| $\overline{\mathrm{RCO}}$ | 27. | n.c. |  | n.c. | 27 | n.c. |
| n.c. | 28 | n.c. |  | n.c. | 28 | n.c. |
| n.c. | 29 | n.c. |  | n.c. | 29 | n.c. |
| n.c. | 30 | n.c. |  | n.c. | 30 | n.c. |
| $V_{p}$ | 31 | $V_{p}$ |  | 0 V | 31 | $V_{S}$ |
| 0 V | 32 | 0 V |  | n.c. | 32 | n.c. |

n.c. $=$ not connected.

* No supply line, is used as return line for control signals.
** For coding MID lines.
- For coding CHS lines.


## PROGRAM MEMORY MODULE

## DESCRIPTION

This memory module is for use with central processor CP22 and other PC20 modules to assemble a programmable controller.
The MM20 is an 8 k 16 EPROM memory. It is supplied with 8 empty EPROMs, type 2716 , which can be programmed on the programming unit PU20.

The 8 IC-sockets for the EPROMs are marked $0-1,2-3,4-5$, or 6-7, for $A$ and $B$ type EPROMs, indicating the address range of the socket.
EPROMs should be inserted into the sockets as follows:
EPROMs ( $A$ and $B$ ) with addresses 0000 to 2047 into sockets 0-1 ( $A$ and $B$ );
EPROMs ( $A$ and $B$ ) with addresses 2048 to 4095 into sockets $2-3$ ( $A$ and $B$ );
EPROMs ( $A$ and $B$ ) with addresses 4096 to 6143 into sockets $4-5$ ( $A$ and $B$ );
EPROMs ( $A$ and $B$ ) with addresses 6144 to 8191 into sockets 6-7 ( $A$ and $B$ ).
The memory module is built on a glass-epoxy double Euro-card* ( $233,4 \mathrm{~mm} \times 160 \mathrm{~mm}$ ) with two F068-1 connectors (male parts) ; the corresponding female parts are on the back panels.

## ELECTRICAL DATA

## Supply

Supply voltage (d.c.) current
$V_{p} \quad 10 \mathrm{~V} \pm 10 \%$
Ip max. 550 mA (module filled with 8 EPROMs)

* For a general description of the Euro-card system see IEC 297 or DIN41494 for 19 -in racks and IEC 130-14 or DIN41612 for connectors.


## Input and output data

The voltage levels of inputs and outputs are in accordance with standard LOCMOS specifications.

| function | terminations (Fig. 2) |  |  |
| :--- | :--- | :--- | :--- |
|  |  | connector 1 | connector 2 |

INPUTS

| APFP | Address processing finished; when LOW addresses may change. | a28 |  |
| :---: | :---: | :---: | :---: |
| APM 0 <br> APM ${ }_{1}$ <br> APM 2 <br> APM 3 <br> APM 4 <br> APM ${ }_{5}$ <br> APM 6 <br> APM 7 <br> APM 8 <br> APM9 <br> APM 10 <br> APM 11 <br> APM 12 | Address bits for program memory. |  | a16, c16 <br> a17, c17 <br> a18, c18 <br> a19, c19 <br> a20, c20 <br> a21, c21 <br> a22, c22 <br> a23, c23 <br> a24, c24 <br> a25, c25 <br> a26, c26 <br> a27, c27 <br> a28, c28 |
| $\mathrm{PHC}_{0}$ | Phase control line. | c23 |  |



Time data


Fig. 1 Read-out of program memory during DP-phase.

Preparation time
Access time

| $t_{\text {pr }}$ | max. | 350 ns |
| :--- | :--- | :--- |
| $t_{\text {acc }}$ | max. | 525 ns |

## MECHANICAL DATA

Dimensions in mm
Outlines


Mass approx. 310 g

Terminal location

| connector 1 |  |  | connector 2 |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| row c |  | row a | row c |  | row a |
| $\mathrm{PMB}_{0}$ | 1 | n.c. | n.c. | 1 | n.c. |
| PMB1 | 2 | n.c. | n.c. | 2 | n.c. |
| $\mathrm{PMB}_{2}$ | 3 | n.c. | n.c. | 3 | n.c. |
| $\mathrm{PMB}_{3}$ | 4 | n.c. | n.c. | 4 | n.c. |
| $\mathrm{PMB}_{4}$ | 5 | n.c. | n.c. | 5 | n.c. |
| $\mathrm{PMB}_{5}$ | 6 | n.c. | n.c. | 6 | n.c. |
| $\mathrm{PMB}_{6}$ | 7 | n.c. | n.c. | 7 | n.c. |
| $\mathrm{PMB}_{7}$ | 8 | n.c. | n.c. | 8 | n.c. |
| $\mathrm{PMB}_{8}$ | 9 | n.c. | n.c. | 9 | n.c. |
| PMB9 | 10 | n.c. | n.c. | 10 | n.c. |
| PMB10 | 11 | n.c. | n.c. | 11 | n.c. |
| PMB11 | 12 | n.c. | n.c. | 12 | n.c. |
| $\mathrm{PMB}_{12}$ | 13 | n.c. | n.c. | 13 | n.c. |
| PMB13 | 14 | n.c. | n.c. | 14 | n.c. |
| PMB 14 | 15 | n.c. | n.c. | 15 | n.c. |
| PMB15 | 16 | n.c. | $\mathrm{APM}_{0}$ | 16 | $\mathrm{APM}_{0}$ |
| n.c. | 17 | n.c. | $\mathrm{APM}_{1}$ | 17 | $\mathrm{APM}_{1}$ |
| n.c. | 18 | n.c. | $\mathrm{APM}_{2}$ | 18 | $\mathrm{APM}_{2}$ |
| n.c. | 19 | n.c. | $\mathrm{APM}_{3}$ | 19 | $\mathrm{APM}_{3}$ |
| n.c. | 20 | n.c. | $\mathrm{APM}_{4}$ | 20 | $\mathrm{APM}_{4}$ |
| n.c. | 21 | n.c. | $\mathrm{APM}_{5}$ | 21 | $\mathrm{APM}_{5}$ |
| n.c. | 22 | n.c. | APM $_{6}$ | 22 | $\mathrm{APM}_{6}$ |
| $\mathrm{PHC}_{0}$ | 23 | n.c. | $\mathrm{APM}_{7}$ | 23 | $\mathrm{APM}_{7}$ |
| n.c. | 24 | n.c. | APM $_{8}$ | 24 | $\mathrm{APM}_{8}$ |
| n.c. | 25 | n.c. | APM9 | 25 | APM9 |
| n.c. | 26 | n.c. | $\mathrm{APM}_{10}$ | 26 | $\mathrm{APM}_{10}$ |
| n.c. | 27 | PRFP | $\mathrm{APM}_{11}$ | 27 | $\mathrm{APM}_{11}$ |
| n.c. | 28 | APFP | $\mathrm{APM}_{12}$ | 28 | $\mathrm{APM}_{12}$ |
| n.c. | 29 | n.c. | n.c. | 29 | n.c. |
| n.c. | 30 | n.c. | n.c. | 30 | n.c. |
| $V_{p}$ | 31 | $V_{p}$ | $V_{p}$ | 31 | $V_{p}$ |
| 0 V | 32 | 0 V | 0 V | 32 | 0 V |

n.c. $=$ not connected.

## PROGRAM MEMORY MODULES

## DESCRIPTION

These memory modules are for use with central processor CP22 and other PC20 modules to assemble a programmable controller.

The two modules are identical, except for the program memory capacity: 8 k 16 C-MOS RAM for the MM21, 4 k 16 C-MOS RAM for the MM22. The modules have an on-board battery for data retention ( 30 h ) in case the supply voltage is switched off. An external battery can be connected for longer memory retention.

Each module is built on a glass-epoxy double Euro-card* ( $233,4 \mathrm{~mm} \times 160 \mathrm{~mm}$ ) with two F068-I connectors (male parts) ; the corresponding female parts are on the back panels.

## ELECTRICAL DATA

Supply
Supply voltage (d.c.)
current

| $V_{P}$ | $10 \mathrm{~V} \pm 10 \%$ |
| :--- | :--- |
| $\mathrm{I}_{\mathrm{P}}$ | typ. 110 mA |
|  | $\max .150 \mathrm{~mA}$ |

Requirements of the back-up battery
Battery voltage
Battery current ( $\mathrm{V}_{\mathrm{P}}=0 \mathrm{~V}$ )
Trickle charge current ( $\mathrm{V} P=10 \mathrm{~V}$ )
Data retention with on-board battery at $40^{\circ} \mathrm{C}$
$V_{B} 3$ to $4,5 \mathrm{~V}$
IB typ. 1,5 mA typ. -5 mA typ. 30 h , provided the module has been in operation for at least 20 h .

## Note

When the supply voltage drops below 7 V the C-MOS RAM memory is automatically switched to the stand-by position, so that the battery can take over the supply of the memory as soon as $V_{p}$ falls below $\mathrm{V}_{\mathrm{B}}$.

[^30]
## Input and output data

The voltage levels of inputs and outputs are in accordance with standard LOCMOS specifications.

|  | function | terminations (Fig. 3) |  |
| :--- | :--- | :--- | :--- |
|  |  | connector 1 | connector 2 |

INPUTS

| APFP | Address processing finished; when LOW addresses may change, when goes HIGH address on APM $0-12$ is clocked into the address latch in the RAM (active when $\mathrm{PHC}_{0}$ is LOW). | a28 |  |
| :---: | :---: | :---: | :---: |
| APM $_{0}$ <br> APM 1 <br> $\mathrm{APM}_{2}$ <br> $\mathrm{APM}_{3}$ <br> APM $_{4}$ <br> APM $_{5}$ <br> APM 6 <br> $\mathrm{APM}_{7}$ <br> APM 8 <br> APM9 <br> APM 10 <br> APM11 <br> APM 12 | Address bits for program memory. |  | a16, c16 <br> a17, c17 <br> a18, c18 <br> a19, c19 <br> a20, c20 <br> a21, c21 <br> a22, c22 <br> a23, c23 <br> a24, c24 <br> a25, c25 <br> a26, c26 <br> a27, c27 <br> a28, c28 |
| PABE | Input to clock address on $\mathrm{APM}_{0-12}$ into the address latch in the RAM. |  | a1, c1 |
| $\begin{aligned} & \mathrm{PHC}_{0} \\ & \mathrm{PHC}_{1} \end{aligned}$ | Phase control lines | $\mathrm{a} 23 \quad \mathrm{c} 23$ |  |
| $\mathrm{PMBI}_{0}$ <br> $\mathrm{PMBI}_{1}$ <br> $\mathrm{PMBI}_{2}$ <br> $\mathrm{PMBl}_{3}$ <br> $\mathrm{PMBI}_{4}$ <br> $\mathrm{PMBI}_{5}$ <br> ${ }^{\text {PMBI }} 6$ <br> $\mathrm{PMBI}_{7}$ <br> $\mathrm{PMBI}_{8}$ <br> PMBIg <br> PMBI 10 <br> $\mathrm{PMBI}_{11}$ <br> $\mathrm{PMBI}_{12}$ <br> PMBI $_{13}$ <br> PMBI 14 <br> PMBI 15 | Data inputs for program memory bits. | a1 <br> a2 <br> a3 <br> a4 <br> a5 <br> a6 <br> a7 <br> a8 <br> a9 <br> a10 <br> a11 <br> a12 <br> a13 <br> a14 <br> a15 <br> a16 |  |
| $\overline{\mathrm{R}} / \mathrm{W}$ | Read/write input. When HIGH data on $\mathrm{PMBI}_{0-15}$ is written into the RAM only when $\mathrm{PHC}_{0}$ and $\mathrm{PHC}_{1}$ are LOW. |  | a14, c14 |


|  | function | terminations (Fig. 3) |  |
| :---: | :---: | :---: | :---: |
|  |  | connector 1 | connector 2 |
| OUTPUTS |  |  |  |
| $\mathrm{PMB}_{0}$ $\mathrm{PMB}_{1}$ <br> PMB2 PMB3 PMB4 PMB5 PMB6 PMB7 PMB8 PMB9 PMB10 PMB11 PMB12 PMB13 PMB14 PMB15 | Data output of program memory. <br> The output stage is built-up with transistor drive circuit with pull-up resistor ( $2,2 \mathrm{k} \Omega$ ). <br> The sink capability is max. 3 mA . | c1 <br> c2 <br> c3 <br> c4 <br> c5 <br> c6 <br> c7 <br> c8 <br> c9 <br> c10 <br> c11 <br> c12 <br> c13 <br> c14 <br> c15 <br> c16 |  |
| PRFP | Output indicating that preparation for reading data has been finished and data is available on outputs $\mathrm{PMB}_{0-15}$ (active when $\mathrm{PHC}_{0}$ is LOW). | a27 |  |

Time data $\mathrm{PHC}_{0}$


Fig. 1 Read/write cycle during UDC-phase.
Pulse width for RAM address latch
Address setting time
Access time
Write pulse width
Data stable
$\min . \quad 50 \mathrm{~ns}$
$\mathrm{t}_{\text {as }}$ max. 200 ns
tacc max. $1 \mu \mathrm{~s}$
$\mathrm{t}_{\mathrm{wp}} \quad \mathrm{min} .600 \mathrm{~ns}$
$\mathrm{t}_{\mathrm{ds}} \quad \mathrm{min} .500 \mathrm{~ns}$
$\mathrm{PHC}_{0}$ $\qquad$

$\bar{R} / W$


Fig. 2 Read cycle during DP-phase.

Address setting time
Preparation time
Access time

| $\mathrm{t}_{\text {as }}$ | min. | 0 ns |
| :--- | :--- | ---: |
| $\mathrm{t}_{\mathrm{pr}}$ | max. | 350 ns |
| $\mathrm{t}_{\mathrm{acc}}$ | max. | 600 ns |

MECHANICAL DATA


REAR VIEW


Fig. 3.
7289354


FRONT VIEW

Mass approx. 270 g

## Notes

1. When the program memory module is delivered, the on-board battery is switched off (jumper A, Fig. 4).
2. If the program memory module is removed from the rack, ensure that it is placed on an insulated surface to prevent short-circuiting of the on-board battery.


Fig. 4.

Terminal location

| row c | connector 1 |  | connector 2 |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | row a | row c |  | row a |
| $\mathrm{PMB}_{0}$ | 1 | $\mathrm{PMBI}_{0}$ | PABE | 1 | PABE |
| $\mathrm{PMB}_{1}$ | 2 | $\mathrm{PMBI}_{1}$ | n.c. | 2 | n.c. |
| $\mathrm{PMB}_{2}$ | 3 | $\mathrm{PMBI}_{2}$ | n.c. | 3 | n.c. |
| $\mathrm{PMB}_{3}$ | 4 | $\mathrm{PMBl}_{3}$ | n.c. | 4 | n.c. |
| $\mathrm{PMB}_{4}$ | 5 | $\mathrm{PMBI}_{4}$ | n.c. | 5 | n.c. |
| $\mathrm{PMB}_{5}$ | 6 | $\mathrm{PMBI}_{5}$ | n.c. | 6 | n.c. |
| $\mathrm{PMB}_{6}$ | 7 | $\mathrm{PMBI}_{6}$ | n.c. | 7 | n.c. |
| $\mathrm{PMB}_{7}$ | 8 | $\mathrm{PMBI}_{7}$ | n.c. | 8 | n.c. |
| PMB8 | 9 | $\mathrm{PMBl}_{8}$ | n.c. | 9 | n.c. |
| $\mathrm{PMB}_{9}$ | 10 | PMBI9 | n.c. | 10 | n.c. |
| PMB10 | 11 | PMBI 10 | n.c. | 11 | n.c. |
| $\mathrm{PMB}_{11}$ | 12 | PMBI 11 | n.c. | 12 | n.c. |
| $\mathrm{PMB}_{12}$ | 13 | PMBI 12 | n.c. | 13 | n.c. |
| PMB13 | 14 | PMBI 13 | $\bar{R} / W$ | 14 | $\bar{R} / W$ |
| PMB14 | 15 | PMBI 14 | n.c. | 15 | n.c. |
| PMB15 | 16 | PMBI 15 | $\mathrm{APM}_{0}$ | 16 | $\mathrm{APM}_{0}$ |
| n.c. | 17 | n.c. | $\mathrm{APM}_{1}$ | 17 | $\mathrm{APM}_{1}$ |
| n.c. | 18 | n.c. | $\mathrm{APM}_{2}$ | 18 | $\mathrm{APM}_{2}$ |
| n.c. | 19 | n.c. | $\mathrm{APM}_{3}$ | 19 | $\mathrm{APM}_{3}$ |
| n.c. | 20 | n.c. | $\mathrm{APM}_{4}$ | 20 | $\mathrm{APM}_{4}$ |
| n.c. | 21 | n.c. | $\mathrm{APM}_{5}$ | 21 | $\mathrm{APM}_{5}$ |
| n.c. | 22 | n.c. | APM $_{6}$ | 22 | $\mathrm{APM}_{6}$ |
| $\mathrm{PHC}_{0}$ | 23 | $\mathrm{PHC}_{1}$ | ${ }^{\text {APM }} 7$ | 23 | $\mathrm{APM}_{7}$ |
| n.c. | 24 | n.c. | $\mathrm{APM}_{8}$ | 24 | APM8 |
| n.c. | 25 | n.c. | $\mathrm{APM}_{9}$ | 25 | $\mathrm{APM}_{9}$ |
| n.c. | 26 | n.c. | APM $_{10}$ | 26 | APM 10 |
| n.c. | 27 | PRFP | $\mathrm{APM}_{11}$ | 27 | $\mathrm{APM}_{11}$ |
| n.c. | 28 | APFP | $\mathrm{APM}_{12}$ | 28 | $\mathrm{APM}_{12}$ |
| n.c. | 29 | n.c. | n.c. | 29 | n.c. |
| n.c. | 30 | n.c. | VB | 30 | VB |
| $V_{p}$ | 31 | $V_{p}$ | $V_{p}$ | 31 | $V_{p}$ |
| 0 V | 32 | 0 V | 0 V | 32 | 0 V |

## OUTPUT MODULE

## DESCRIPTION

This output module is used with the other PC20 modules to assemble a programmable controller.
The output module contains 16 addressable output stages, with photo-isolators between external and internal circuitry (Fig. 1). All outputs have grounded loads. Each output stage has a flywheel diode, to allow it to switch inductive loads. Each output stage also has a LED for status indication: it is lit when the output transistor is conducting.
The output stages have electronic short-circuit protection with automatic reset.


Fig. 1 Circuit diagram of an output stage.

The output module has 11 address inputs ( $\mathrm{ADD}_{0-10}$ ) and 9 module identification inputs ( $\mathrm{MID}_{2-10}$ ), which are accessible on the connectors at the rear (Fig. 2).


Fig. 2 Block diagram of the output module.
The circuit is built on an epoxy-glass printed-wiring board of $233,4 \mathrm{~mm} \times 160 \mathrm{~mm}$ (double Eurocard).
The board has two F068-I connectors (board parts); the corresponding rack part of connector 1 (Fig. 3) is available on the back pànels, that of connector 2 (external connections) is separately available under catalogue number 242202589288 (pins for wire wrapping), 242202589298 (pins for dip-soldering) or 242202589326 (solder tags).*

## ELECTRICAL DATA

## Supply

| Supply voltage (d.c.) Supply current | logic | $\begin{aligned} & V_{p} \\ & I_{P} \end{aligned}$ | $10 \mathrm{~V} \pm 10 \%$ <br> typ. 120 mA (all stages ON ) <br> max. 150 mA (all stages ON) <br> typ. $\quad 25 \mathrm{~mA}$ (all stages OFF) |
| :---: | :---: | :---: | :---: |
| Supply voltage (d.c.) | for | $\mathrm{V}_{S}$ | $24 \pm 25 \% * *$ |
| Supply current (excluding load current) | output circuitry | Is | typ. $\quad 75 \mathrm{~mA}$ (all stages ON) max. 110 mA (all stages ON) typ. $\quad 50 \mathrm{~mA}$ (all stages OFF) |

* For a general description of the Eurocard system see IEC 297 or DIN 41494 for 19-in racks and IEC 130-14 or DIN 41612 for connectors.
** If $\mathrm{V}_{\mathrm{S}}$ drops below 16 V , all output stages are forced into the non-conducting state for protection of the output circuitry.

Output module

Input data
All inputs meet the standard LOCMOS specifications.

| input | function | terminations of connector 1 (Fig. 3) |
| :---: | :---: | :---: |
|  | Address bits from central processor; $A D D_{0-1}$ select a group of four output stages, $A D D_{2-10}$ select the output module. | a11 $c 11$ <br> a12 $c 12$ <br> a13 c 13 <br> a14 c 14 <br> a15 c 15 <br>  c 16 |
| $\mathrm{DIO}_{0}$ <br> DIO1 <br> $\mathrm{DIO}_{2}$ <br> $\mathrm{DIO}_{3}$ | Data bits from central processor; data are stored in output stages by SBI. | a21 c21 <br> a22 c22 |
| $\overline{\mathrm{REO}}$ | Reset output module input; a low level on this input will reset all output latches (output transistor non-conducting); input current LOW: 10 mA . | a27 |
| $\overline{\mathrm{RCO}}$ | Reset from central processor (low level) during switch-on. | c27 |
| $M_{1 D} 2$ <br> $\mathrm{MID}_{3}$ <br> MID4 <br> MID $_{5}$ <br> MID6 <br> $\mathrm{MID}_{7}$ <br> $\mathrm{MID}_{8}$ <br> MID9 <br> MID 10 | Module identification inputs; provide module with individual identity. | $\begin{aligned} & \mathrm{c} 2 \\ & \mathrm{c} 3 \\ & \mathrm{c} 4 \\ & \mathrm{c} 5 \\ & \mathrm{c} 6 \\ & \mathrm{c} 7 \\ & \mathrm{c} 8 \\ & \mathrm{c} 9 \\ & \mathrm{c} 10 \end{aligned}$ |
| SBI | Cloc̣k signal from central processor to output module, stores data on $\mathrm{DIO}_{0-3}$ into output stages during input/output cycle. | c26 |
| $\begin{aligned} & \mathrm{PHC}_{0} \\ & \mathrm{PHC}_{1} \end{aligned}$ | Phase control signals. | a23 c23 |
| APF | Handshake signal; input/output address correct. | a26 |
| $\overline{O S D}$ | Output stage disable for all stages; input current LOW: 10 mA . | a28 |

## Output data

The data outputs are $\mathrm{DO}_{\mathrm{W} .0}$ to $\mathrm{DO}_{\mathrm{W} .3}, \mathrm{DO}_{\mathrm{X} .0}$ to $\mathrm{DO}_{\mathrm{X} .3}, \mathrm{DO}_{\mathrm{Y} .0}$ to $\mathrm{DO}_{\mathrm{Y} .3}$ and $\mathrm{DO}_{\mathrm{Z} .0}$ to $\mathrm{DO}_{\mathrm{Z} .3}$. They are accessible on connector 2, see "Terminal location".
Minimum load resistance $R_{L}=48 \Omega$.
Output transistor conducting: $\mathrm{R}_{\mathrm{L}}=48 \Omega ; \mathrm{V}_{\mathrm{a}-\mathrm{c}}{ }^{*}=\min . \mathrm{V}_{\mathrm{S}}-1,5 \mathrm{~V}$.
Output transistor non-conducting: $\mathrm{I}_{\mathrm{O}}=\max .2 \mathrm{~mA}$ at $\mathrm{V}_{\mathrm{S}}=30 \mathrm{~V}$.
The outputs are continuously tested for short-circuiting. As soon as the short-circuiting is removed, the output stage is automatically reset to normal operation.
Output current (limited to 6A per module)
for all stages
max. $0,375 \mathrm{~A}$ per stage
for maximum 12 stages
max. 0,5 A per stage

Logic outputs (open collector)

| output | function | terminations of <br> connector 1 (Fig. 3) |
| :--- | :--- | :--- |
| PRF | Preparation of output module finished. | a 24 |
| DEF | Data exchange finished. | a 25 |

* Voltage between terminal of row a and terminal of row cof connector 2.

Output module

MECHANICAL DATA
Dimensions in mm

## Outlines



Fig. 3.
Mass
230 g

Terminal location

| connector 1 |  |  |  | connector 2 |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| row c |  | row a |  | row c |  | row a |
| n.c. | 1 | HIGH level |  | 0 V | 1 | $\mathrm{V}_{S}$ |
| $\mathrm{MID}_{2}$ | 2 | HIGH level |  | 0 V | 2 | DOW.0 |
| $\mathrm{MID}_{3}$ | 3 | HIGH level |  | 0 V | 3 |  |
| $\mathrm{MID}_{4}$ | 4 | HIGH level |  | 0 V | 4 | DOW. 1 |
| MID5 | 5 | HIGH level | ** | 0 V | 5 | $\mathrm{V}_{\text {S }}$ |
| MID6 | 6 | HIGH level |  | 0 V | 6 | $\mathrm{DO}_{\text {W. } 2}$ |
| MID7 | 7 | HIGH level |  | 0 V | 7 |  |
| MID8 | 8 | HIGH level |  | 0 V | 8 | DOW. 3 |
| MID9 | 9 | HIGH level |  | 0 V | 9 | $\mathrm{V}_{\text {S }}$ |
| MID10 | 10 | HIGH level |  | 0 V | 10 | DOX. 0 |
| ADD 0 | 11 | $\mathrm{ADD}_{1}$ |  | 0 V | 11 | $\mathrm{V}_{S}$ |
| $\mathrm{ADD}_{2}$ | 12 | $\mathrm{ADD}_{3}$ |  | 0 V | 12 | DOX. 1 |
| $\mathrm{ADD}_{4}$ | 13 | $\mathrm{ADD}_{5}$ |  | 0 V | 13 | $\mathrm{V}_{\mathrm{S}}$ |
| $\mathrm{ADD}_{6}$ | 14 | $\mathrm{ADD}_{7}$ |  | 0 V | 14 | ${ }_{\text {DOX. }} 2$ |
| $\mathrm{ADD}_{8}$ | 15 | ADD9 |  | 0 V | 15 | $\mathrm{V}_{\mathrm{S}}$ |
| ADD 10 | 16 | n.c. |  | 0 V | 16 | DOX. 3 |
| n.c. | 17 | n.c. |  | 0 V | 17 | $\mathrm{V}_{S}$ |
| n.c. | 18 | n.c. |  | 0 V | 18 | DOY. 0 |
| n.c. | 19 | n.c. |  | 0 V | 19 | $V_{S}$ |
| n.c. | 20 | n.c. |  | 0 V | 20 | DOY. 1 |
| $\mathrm{DIO}_{0}$ | 21 | $\mathrm{DIO}_{1}$ |  | 0 V | 21 | $\mathrm{V}_{S}$ |
| $\mathrm{DIO}_{2}$ | 22 | $\mathrm{DIO}_{3}$ |  | 0 V | 22 | DOY. 2 |
| $\mathrm{PHC}_{0}$ | 23 | $\mathrm{PHC}_{1}$ |  | 0 V | 23 | $\mathrm{V}_{\mathrm{S}}$ |
| n.c. | 24 | PRF |  | 0 V | 24 | DOY. 3 |
| $0 V^{*}$ | 25 | DEF |  | 0 V | 25 | $\mathrm{V}_{\mathrm{S}}$ |
| SBI | 26 | APF |  | 0 V | 26 | $\mathrm{DO}_{\text {z. }}$ |
| RCO | 27 | REO |  | 0 V | 27 | $\mathrm{V}_{\mathrm{S}}$ |
| n.c. | 28 | OSD |  | 0 V | 28 | $\mathrm{DO}_{\text {Z. } 1}$ |
| n.c. | 29 | n.c. |  | 0 V | 29 | $\mathrm{V}_{\mathrm{S}}$ |
| n.c. | 30 | n.c. |  | 0 V | 30 | $\mathrm{DO}_{\text {Z. } 2}$ |
| $V_{p}$ | 31 | $V_{P}$ |  | 0 V | 31 | $\mathrm{V}_{\mathrm{S}}{ }^{2}$ |
| 0 V | 32 | 0 V |  | 0 V | 32 | $\mathrm{DO}_{\mathrm{z} .3}$ |

n.c. $=$ not connected.

## Note

Supply-voltage lines $\left(V_{S}\right)$ have to be connected to each group of 4 outputs.

[^31]** For coding MID lines.

## OM21

## OUTPUT MODULE

## DESCRIPTION

This output module is used with the other PC20 modules to assemble a programmable controller.
The output module contains 8 addressable output stages, with photo-isolators between external and internal circuitry (Fig. 1). All outputs are grounded load outputs. Each output stage has a voltage regulator diode, to allow it to switch inductive loads. Each output stage also has a LED for status indication: it is lit when the output transistor is conducting.
The output stages feature electronic short-circuit protection, i.e. when a short circuit occurs the relevant output stage is switched off automatically, and is indicated via the short-circuit indication output (SCI). After removing the short circuit the output stage can be reactivated via the REO input.


Fig. 1 Circuit diagram of an output stage.

The output module has 11 address inputs ( $A D D D_{0-10}$ ) and 10 module identification inputs ( $\mathrm{MID}_{1-10}$ ) which are accessible on the connectors at the rear (Fig. 2).


Fig. 2 Block diagram of the output module.
The circuit is built on an epoxy-glass printed-wiring board of $233,4 \mathrm{~mm} \times 160 \mathrm{~mm}$ (double Eurocard). The board has two F068-I connectors (board parts); the corresponding rack part of connector 1 (Fig. 4) is available on the back panels, that of connector 2 (external connections) is separately available under catalogue number 242202589288 (pins for wire wrapping), 242202589298 (pins for dip-soldering) or 242202589326 (solder tags).*

## ELECTRICAL DATA

## Supply



[^32]
## Input data

All inputs meet the standard LOCMOS specifications.

| input | function | terminations of connector 1 (Fig. 4) |  |
| :---: | :---: | :---: | :---: |
| $\mathrm{ADD}_{0}$ | Address bits from central processor; ADD $_{0}$ select a group of four output stages, ADD $_{1-10}$ select the output module. |  | c11 |
| $\mathrm{ADD}_{1}$ |  | a11 |  |
| $\mathrm{ADD}_{2}$ |  |  | c12 |
| $\mathrm{ADD}_{3}$ |  | a12 |  |
| $\mathrm{ADD}_{4}$ |  |  | c13 |
| $\mathrm{ADD}_{5}$ |  | a13 |  |
| $\mathrm{ADD}_{6}$ |  |  | c14 |
| $\mathrm{ADD}_{7}$ |  | a14 |  |
| $\mathrm{ADD}_{8}$ |  |  | c15 |
| $\mathrm{ADD}_{9}$ |  | a15 |  |
| $\mathrm{ADD}_{10}$ |  |  | c16 |
| $\mathrm{DIO}_{0}$ | Data bits from central processor; data are stored in output stages by SBI. |  | c21 |
| $\mathrm{DIO}_{1}$ |  | a21 |  |
| $\mathrm{DIO}_{2}$ |  |  | c22 |
| $\mathrm{DIO}_{3}$ |  | a22 |  |
| $\overline{\text { REO }}$ | Reset output module input; a low level on this input will reset all output latches and the shortcircuit protection circuitry (output transistor non-conducting; input current LOW: 10 mA ). | a27 |  |



| $\mathrm{PHC}_{0}$ |
| :--- | :--- | :---: |
| $\mathrm{PHC}_{1}$ |$|$ Phase control signals. $\quad$ a23 $\quad$ c23

## Output data

The data outputs are $\mathrm{DO}_{\mathrm{Y} .0}$ to $\mathrm{DO}_{\mathrm{Y} .3}$ and $\mathrm{DO}_{\mathrm{Z} .0}$ to $\mathrm{DO}_{\mathrm{Z} .3}$.
They are accessible on connector 2, see "Terminal location".
Minimum load resistance $R_{L}=12 \Omega$.
Output transistor conducting: $\mathrm{R}_{\mathrm{L}}=12 \Omega ; \mathrm{V}_{\mathrm{a}-\mathrm{c}}{ }^{*}=\min . \mathrm{V}_{\mathrm{S}}-1,5 \mathrm{~V}$.
Output transistor non-conducting: $I_{0}=\max .2 \mathrm{~mA}$ at $\mathrm{V}_{\mathrm{S}}=30 \mathrm{~V}$.
For load inductance, see Fig. 3.
Output current (limited to 8 A per module)
for all stages
for maximum 4 stages
max. 1 A per stage
max. 2 A per stage

Output SCI is an open-collector output; drive capability max. 20 mA . In case of a short circuit in one of the output stages, the output transistor is conducting: $\mathrm{V}_{\mathrm{SCI}}=$ max. $0,5 \mathrm{~V}$ (with respect to 0 V - line); transistor non-conducting: $\mathrm{V}_{\mathrm{SCI}}=30 \mathrm{~V}$.

Logic outputs (open collector)

| output | function | terminations of <br> connector 1 (Fig. 4) |
| :--- | :--- | :--- |
| PRF | Preparation of output module finished. | a 24 |
| DEF | Data exchange finished. | a 25 |



Fig. 3 Maximum duty factor ( $\delta$ ) as a function of switching frequency at different $L_{L} L^{\prime}$ - products ( $L_{L}=$ load inductance; $I_{L}=$ load current).

[^33]
## Outlines



Fig. 4.

[^34]Terminal location

|  | nector |  |  |  | nect |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| row c |  | row a |  | row c |  | row a |
| MID 1 | 1 | HIGH level |  | 0 V | 1 | $v_{S}$ |
| $\mathrm{MID}_{2}$ | 2 | HIGH level |  | 0 V | 2 | SCI |
| $\mathrm{MID}_{3}$ | 3 | HIGH level |  | 0 V | 3 | $\mathrm{V}_{\mathrm{S}}$ |
| $\mathrm{MID}_{4}$ |  | HIGH level |  | 0 V | 4 | DOY. 0 |
| $\mathrm{MID}_{5}$ | 5 | HIGH level | ** | 0 V | 5 | $\mathrm{V}_{\mathrm{S}}$ |
| $\mathrm{MID}_{6}$ | 6 | HIGH level |  | 0 V | 6 | ${ }^{\text {DO }} \mathrm{Y} .1$ |
| $\mathrm{MID}_{7}$ |  | HIGH level |  | 0 V | 7 |  |
| $\mathrm{MID}_{8}$ | 8 | HIGH level |  | 0 V | 8 | ${ }^{\text {DO }} \mathrm{Y} .1$ |
| MID9 | 9 | HIGH level |  | 0 V | 9 | $\mathrm{V}_{\mathrm{S}}$ |
| MID 10 | 10 | HIGH level |  | 0 V | 10 | $\mathrm{DO}_{\mathrm{Y} .2}$ |
| $\mathrm{ADD}_{0}$ | 11 | $\mathrm{ADD}_{1}$ |  | 0 V | 11 | $\mathrm{V}_{\mathrm{S}}$ |
| $\mathrm{ADD}_{2}$ | 12 | $\mathrm{ADD}_{3}$ |  | 0 V | 12 | $\mathrm{DO}_{\mathrm{Y} .2}$ |
| $\mathrm{ADD}_{4}$ | 13 | $\mathrm{ADD}_{5}$ |  | 0 V | 13 | $\mathrm{V}_{\mathrm{S}}$ |
| $\mathrm{ADD}_{6}$ | 14 | $\mathrm{ADD}_{7}$ |  | 0 V | 14 | ${ }^{\text {DO }} \mathrm{Y} .3$ |
| $\mathrm{ADD}_{8}$ | 15 | ADD9 |  | 0 V | 15 | $\mathrm{V}_{\mathrm{S}}$ |
| $\mathrm{ADD}_{10}$ | 16 | n.c. |  | 0 V | 16 | ${ }_{\text {DO }}^{\text {Y }} 3$ |
| n.c. | 17 | n.c. |  | 0 V | 17 | $\mathrm{V}_{S}$ |
| n.c. | 18 | n.c. |  | 0 V | 18 | $\mathrm{DO}_{\mathrm{z} .0}$ |
| n.c. | 19 | n.c. |  | 0 V | 19 | $\mathrm{V}_{\mathrm{S}}$ |
| n.c. | 20 | n.c. |  | 0 V | 20 | $\mathrm{DO}_{\mathrm{Z} .0}$ |
| $\mathrm{DIO}_{0}$ | 21 | $\mathrm{DIO}_{1}$ |  | 0 V | 21 | $\mathrm{V}_{S}$ |
| $\mathrm{DIO}_{2}$ | 22 | $\mathrm{DIO}_{3}$ |  | 0 V | 22 | $\mathrm{DO}_{\mathrm{z} .1}$ |
| $\mathrm{PHC}_{0}$ | 23 | $\mathrm{PHC}_{1}$ |  | 0 V | 23 | $\mathrm{v}_{\mathrm{S}}$ |
| n.c. | 24 | PRF |  | 0 V | 24 | $\mathrm{DO}_{\mathrm{Z} .1}$ |
| OV* | 25 | DEF |  | 0 V | 25 | $\mathrm{V}_{S}$ |
| SBI | 26 | APF |  | 0 V | 26 | $\mathrm{DO}_{\mathrm{Z} .2}$ |
| RCO | 27 | $\overline{\text { REO }}$ |  | 0 V | 27 | $\mathrm{V}_{\mathrm{S}}$ |
| n.c. | 28 | $\overline{\text { OSD }}$ |  | 0 V | 28 | $\mathrm{DO}_{\mathrm{z.} 2}$ |
| n.c. | 29 | n.c. |  | 0 V | 29 | $V_{S}$ |
| n.c. | 30 | n.c. |  | 0 V | 30 | $\mathrm{DO}_{\text {Z. } 3}$ |
| $V_{P}$ | 31 | $V_{P}$ |  | 0 V | 31 | $\mathrm{V}_{\text {S }}$ |
| OV | 32 | 0 V |  | 0 V | 32 | $\mathrm{DO}_{\mathrm{z.} 3}$ |
| n.c. $=$ not connected. |  |  |  |  |  |  |

Note
Supply-voltage lines ( $\mathrm{V}_{\mathrm{S}}$ ) have to be connected to each output.

[^35]
## OUTPUT MODULE

## DESCRIPTION

This output module is used with the other PC20 modules to assemble a programmable controller.
The output module contains 32 addressable output stages, with photo-isolators between external and internal circuitry (Fig. 1). All outputs are floating with respect to each other. Each output stage has a suppressor diode, to allow it to switch inductive loads.


Fig. 1 Circuit diagram of an output stage.
To obtain a pull-down facility for the first 16 output stages, e.g. to drive TTL circuitry, the module has two 16 -pin sockets ( $S_{3}$ and $\mathrm{S}_{4}$, Fig. 5), to provide insertion of adapter headers to which pull-down resistors are soldered. (See also Output Data.)

The output module has 11 address inputs ( $\mathrm{ADD}_{0-10}$ ) and 8 module identification inputs ( $\mathrm{MID}_{3-10}$ ), which are accessible on the connectors at the rear (Fig. 2).


7289788

Fig. 2 Block diagram of the output module.
The circuit is built on an epoxy-glass printed-wiring board of $233,4 \mathrm{~mm} \times 160 \mathrm{~mm}$ (double Eurocard). The board has two F068-I connectors (board parts); the corresponding rack part of connector 1 (Fig. 3) is available on the back panels, that of connector 2 (external connections) is separately available under catalogue number 242202589288 (pins for wire wrapping), 242202589298 (pins for dip-soldering) or 242202589326 (solder tags).*

## ELECTRICAL DATA

Supply

| Supply voltage (d.c.) | logic | $V_{p}$ | $10 \mathrm{~V} \pm 10 \%$ |
| :---: | :---: | :---: | :---: |
| Supply current | logic | Ip | typ. 340 mA (all stages ON) |
|  |  |  | max. 400 mA (all stages ON) |
|  |  |  | typ. 1 mA (all stages OFF) |

[^36]
## Input data

All inputs meet the standard LOCMOS specifications.

| input | function | terminations of connector 1 (Fig. 5) |
| :---: | :---: | :---: |
|  | Address bits from central processor; $A D D_{0-2}$ select a group of four output stages, $A D D_{3-10}$ select the output module. | a11 c11 <br> a12 c 12 <br> a13 c 13 <br> a14 c 14 <br> a15 c 15 <br>  c 16 |
| APF | Handshake signal; input/output address correct. | a26 |
| $\mathrm{DIO}_{0}$ <br> $\mathrm{DIO}_{1}$ <br> $\mathrm{DIO}_{2}$ <br> $\mathrm{DIO}_{3}$ | Data bits from central processor; data are stored in output stages by SBI. | a21 c21 <br> a22 c22 |
| $\mathrm{MID}_{3}$ <br> $\mathrm{MID}_{4}$ <br> $\mathrm{MID}_{5}$ <br> MID $_{6}$ <br> $\mathrm{MID}_{7}$ <br> $\mathrm{MID}_{8}$ <br> MID9 <br> MID $_{10}$ | Module identification inputs; provide module with individual identity. | c3 c4 c5 c6 c7 c8 c9 c10 |
| $\overline{\text { OSD }}$ | Output stage disable for all stages; input current LOW: 10 mA . | a28 |
| $\begin{aligned} & \mathrm{PHC}_{0} \\ & \mathrm{PHC}_{1} \end{aligned}$ | Phase control signals. | a23 c23 |
| $\overline{\mathrm{RCO}}$ | Reset from central processor (low level) during switch-on. | c27 |
| $\overline{\text { REO }}$ | Reset output module input; a low level on this input will reset all outputs latches (output transistor non-conducting); input current LOW: 10 mA . | a27 |
| SBI | Clock signal from central processor to output module, stores data in $\mathrm{DIO}_{0-3}$ into output stages during input/output cycle. | c26 |

## Output data

The data outputs are $\mathrm{DO}_{\mathrm{S} .0}$ to $\mathrm{DO}_{\mathrm{S} .3}, \mathrm{DO}_{\mathrm{T} .0}$ to $\mathrm{DO}_{\mathrm{T} .3}, \mathrm{DO}_{\mathrm{U} .0}$ to $\mathrm{DO}_{\mathrm{U} .3}, \mathrm{DO}_{\mathrm{V} .0}$ to $\mathrm{DO}_{\mathrm{V} .3}$, ${ }^{\text {DO }} \mathrm{W} .0$ to DOW. $3, \mathrm{DO}_{\mathrm{X} .0}$ to $\mathrm{DO}_{\mathrm{X} .3}, \mathrm{DO}_{\mathrm{Y} .0}$ to $\mathrm{DO}_{\mathrm{Y} .3}$ and $\mathrm{DO}_{\mathrm{Z} .0}$ to $\mathrm{DO}_{\mathrm{Z} .3}$. They are accessible on connector 2, see Terminal location.
Output transistor conducting: output current $=\max .100 \mathrm{~mA}$ at $\mathrm{V}_{\mathrm{a}-\mathrm{c}}{ }^{*}=\max .1,5 \mathrm{~V}$. Output transistor non-conducting: output current $=\max .10 \mu \mathrm{~A}$ at $\mathrm{V}_{\mathrm{a}-\mathrm{c}}{ }^{*}=\max .30 \mathrm{~V}$.
Each output has a suppressor diode, which allows the switching of loads with an inductance of max. 10 H .

Note: If a supply voltage of 5 V is required, e.g. to drive TTL circuitry, pull-down resistors (R, Figs 3 and 4) must be used. These resistors can be soldered to adapter headers, which have to be inserted into sockets $\mathrm{S}_{3}$ and $\mathrm{S}_{4}$ (Figs 3 and 5). The emitter-output on terminal c31 of connector 2 must be connected to the 0 V -line of the external supply voltage $\mathrm{V}_{\mathrm{S}}$ (Fig. 4); this output can then only be used in common emitter configuration.


7289787
Fig. 3.
Fig. 4.
Logic outputs (open collector)

| output | function | terminations of <br> connector 1 (Fig. 5) |
| :--- | :--- | :--- |
| DEF | Data exchange finished. | a 25 |
| PRF | Preparation of output module finished. | a 24 |

Output module
OM22

MECHANICAL DATA
Dimensions in mm
Outlines


Fig. 5.
Mass
approx. 230 g

Terminal location

| row c | connector 1 |  |  | connector 2 |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | row a |  | row c |  | row a |
| n.c. | 1 | HIGH level |  | $\mathrm{DO}_{\text {S } .0}$ | 1 | $\mathrm{DO}_{\text {S. } 0}$ |
| n.c. | 2 | HIGH level |  | $\mathrm{DO}_{\mathrm{S} .1}$ | 2 | DOs. 1 |
| $\mathrm{MID}_{3}$ | 3 | HIGH level |  | $\mathrm{DO}_{\mathrm{S} .2}$ | 3 | $\mathrm{DO}_{\text {S. } 2}$ |
| $\mathrm{MID}_{4}$ | 4 | HIGH level |  | $\mathrm{DO}_{5.3}$ | 4 | DOS. 3 |
| MID 5 | 5 | HIGH level | ** | ${ }^{\text {DO }}$ T. 0 | 5 | $\mathrm{DO}_{\text {T. } 0}$ |
| $\mathrm{MID}_{6}$ | 6 | HIGH level |  | ${ }^{\text {DOT }}$ T. 1 | 6 | DOT. 1 |
| $\mathrm{MID}_{7}$ | 7 | HIGH level |  | ${ }^{\text {DOT. } 2}$ | 7 | DOT. 2 |
| $\mathrm{MID}_{8}$ | 8 | HIGH level |  | ${ }^{\text {DOT. }} 3$ | 8 | DOT. 3 |
| MID9 | 9 | HIGH level |  | DOU.0 | 9 | DOU. 0 |
| MID10 | 10 | HIGH level |  | DOU. 1 | 10 | DOU. 1 |
| $\mathrm{ADD}_{0}$ | 11 | $\mathrm{ADD}_{1}$ |  | DOU. 2 | 11 | DOU. 2 |
| $\mathrm{ADD}_{2}$ | 12 | $\mathrm{ADD}_{3}$ |  | $\mathrm{DO}_{\mathrm{U} .3}$ | 12 | DOU. 3 |
| $\mathrm{ADD}_{4}$ | 13 | $\mathrm{ADD}_{5}$ |  | DOV. 0 | 13 | DOV. 0 |
| $\mathrm{ADD}_{6}$ | 14 | $\mathrm{ADD}_{7}$ |  | DOV. 1 | 14 | DOV. 1 |
| $\mathrm{ADD}_{8}$ | 15 | ADD9 |  | DOV. 2 | 15 | DOV. 2 |
| $\mathrm{ADD}_{10}$ | 16 | n.c. |  | DOV. 3 | 16 | DOV. 3 |
| n.c. | 17 | n.c. |  | DOw. 0 | 17 | DOw. 0 |
| n.c. | 18 | n.c. |  | DOw. 1 | 18 | DOW. 1 |
| n.c. | 19 | n.c. |  | DOw. 2 | 19 | DOw. 2 |
| n.c. | 20 | n.c. |  | DOw. 3 | 20 | DOw. 3 |
| $\mathrm{DIO}_{0}$ | 21 | $\mathrm{DIO}_{1}$ |  | DOX. 0 | 21 | DOX. 0 |
| $\mathrm{DIO}_{2}$ | 22 | $\mathrm{DIO}_{3}$ |  | DOX. 1 | 22 | DOX. 1 |
| $\mathrm{PHC}_{0}$ | 23 | $\mathrm{PHC}_{1}$ |  | DOX. 2 | 23 | DOX. 2 |
| n.c. | 24 | PRF |  | ${ }^{\text {DO }} \times$. 3 | 24 | DOX. 3 |
| 0 V* | 25 | DEF |  | DOY. 0 | 25 | DOY. 0 |
| SBI | 26 | APF |  | DOY. 1 | 26 | DOY. 1 |
| RCO | 27 | REO |  | DOY. 2 | 27 | DOY. 2 |
| n.c. | 28 | OSD |  | DOY. 3 | 28 | DOY. 3 |
| n.c. | 29 | n.c. |  | DOz. $^{\text {d }}$ | 29 | $\mathrm{DO}_{\mathrm{Z} .0}$ |
| n.c. | 30 | n.c. |  | $\mathrm{DO}_{\mathrm{z} .1}$ | 30 | DOZ. 1 |
| Vp | 31 | $V_{p}$ |  | $\mathrm{DO}_{\text {z. } 2}(0 \mathrm{~V}){ }^{\text {® }}$ | 31 | $\mathrm{DO}_{\text {z. } 2}$ |
| 0 V | 32 | 0 V |  | $\mathrm{DO}_{\mathrm{Z} .3}$ | 32 | $\mathrm{DO}_{\mathrm{z} .3}$ |

n.c. $=$ not connected.

* No supply line; is used as return line for control signals.
** For coding MID lines.
A 0 -line of $\mathrm{V}_{\mathrm{S}}$ when pull-down resistors are used.


## SUPPLY AND OUTPUT MODULE

## DESCRIPTION

This supply and output module is used with the other PC20 modules to assemble a programmable controller.
The module contains 8 addressable output stages, a $24 \mathrm{~V} / 10 \mathrm{~V}$ d.c.-d.c. converter and an alarm circuit for the 24 V supply. The output stages have photo-isolators between external and internal circuitry (Fig. 1). All outputs have a grounded load. Each output stage has a flywheel diode, to allow it to switch inductive loads. Each output stage also has a LED for status indication: it is lit when the output transistor is conducting.

The output stages have electronic short-circuit protection with automatic reset.
The $24 \mathrm{~V} / 10 \mathrm{~V}$ d.c.-d.c. converter provides the logic supply voltage for a small controller system with galvanic isolation from the external 24 V supply. Furthermore, it is short-circuit protected and two or more of these modules may be connected in parallel for higher current demands in larger systems.
The alarm circuit monitors the 24 V supply ( $\mathrm{V}_{\mathrm{ic}}$ ), providing two alarm outputs. One of these is accessible for external use (hardware); the other can be used internally for processing (software). Furthermore, a LED on the front panel indicates that $\mathrm{V}_{\mathrm{ic}}$ is above its minimum specified level.


Fig. 1 Circuit diagram of an output stage.

The output part has 11 address inputs ( $\mathrm{ADD}_{0-10}$ ) and 10 module identification inputs ( $\mathrm{MID}_{1-10}$ ), which are accessible on the connectors at the rear (Fig. 2).


Fig. 2 Block diagram of the output part.
The circuits are built on an epoxy-glass printed-wiring board of $233,4 \mathrm{~mm} \times 160 \mathrm{~mm}$ (double Eurocard). The board has two F068-I connectors (board parts); the corresponding rack part of connector 1 (Fig. 3) is available on the back panels, that of connector 2 (external connections) is separately available under catalogue number 242202589288 (pins for wire wrapping), 242202589298 (pins for dip-soldering) or 242202589326 (solder tags).*

## ELECTRICAL DATA

## Supply

| Supply voltage (d.c.) | for | $\mathrm{V}_{\mathrm{S}}$ | $24 \mathrm{~V} \pm 25 \%^{* *}$ |
| :---: | :---: | :---: | :---: |
| Supply current (excluding load current) | output circuitry | IS | typ. 50 mA (all stages (ON) max. 60 mA (all stages ON) typ. 30 mA (all stages OFF) |
| Supply voltage (d.c.) | for | $V_{\text {ic }}$ | $24 \mathrm{~V} \pm 25 \%$ |
| Supply current, at $\mathrm{V}_{\text {ic }}=24 \mathrm{~V}$ and output current $I_{p}=1,7 \mathrm{~A}$ | $\left\{\begin{array}{l} 24 \mathrm{~V} / 10 \mathrm{~V} \\ \text { d.c.-d.c. } \\ \text { converter } \end{array}\right.$ | $l_{\text {ic }}$ | typ. 1,1 A |

[^37]
## Input data

All inputs meet the standard LOCMOS specifications.

| input | function | terminations of connector 1 (Fig. 3) |  |
| :---: | :---: | :---: | :---: |
| $\begin{aligned} & \mathrm{ADD}_{0} \\ & \mathrm{ADD}_{1} \\ & \mathrm{ADD}_{2} \\ & \mathrm{ADD}_{3} \\ & \mathrm{ADD}_{4} \\ & \mathrm{ADD}_{5} \\ & \mathrm{ADD}_{6} \\ & \mathrm{ADD}_{7} \\ & \mathrm{ADD}_{8} \\ & \mathrm{ADD}_{9} \\ & \mathrm{ADD}_{10} \end{aligned}$ | Address bits from central processor; $A D D_{0}$ selects a group of four output stages, ADD $1-10$ select the (output) module. | a11 <br> a12 <br> a13 <br> a14 <br> a15 | c11 <br> c12 <br> c13 <br> c14 <br> c15 <br> c16 |
| $\mathrm{DIO}_{0}$ <br> $\mathrm{DIO}_{1}$ <br> $\mathrm{DIO}_{2}$ <br> $\mathrm{DIO}_{3}$ | Data bits from central processor; data are stored in output stages by SBI. | a21 <br> a22 | $\begin{aligned} & \mathrm{c} 21 \\ & \mathrm{c} 22 \end{aligned}$ |
| REO | Reset output module input; a low level on this input will reset all output latches (output transistor non-conducting); input current LOW: 10 mA . | a27 |  |
| RCO | Reset from central processor (low level) during switch-on. |  | c27 |
| MID1 <br> MID2 <br> $\mathrm{MID}_{3}$ <br> MID4 <br> MID5 <br> MID6 <br> MID7 <br> MID8 <br> MID9 <br> MID10 | Module identification inputs; provide module with individual identity. |  | c1 $c 2$ $c 3$ $c 4$ $c 5$ $c 6$ $c 7$ $c 8$ $c 9$ $c 10$ |
| SBI | Clock signal from central processor to output module, stores data on $\mathrm{DIO}_{0-3}$ into output stages during input/output cycle. |  | c26 |
| $\begin{aligned} & \mathrm{PHC}_{0} \\ & \mathrm{PHC}_{1} \end{aligned}$ | Phase control signals. | a23 | c23 |
| APF | Handshake signal; input/output address correct. | a26 |  |
| $\overline{\text { OSD }}$ | Output stage disable for all stages; input current LOW: 0,1 mA. | a28 |  |

## Output data

The data outputs are DOY. 0 to $\mathrm{DO}_{\mathrm{Y} .3}$ and $\mathrm{DO}_{\mathrm{Z} .0}$ to $\mathrm{DO}_{\mathrm{Z} .3}$. They are accessible on connector 2, see "Terminal location".

Minimum load resistance $R_{L}=48 \Omega$.
Output transistor conducting: $\mathrm{R}_{\mathrm{L}}=48 \Omega ; \mathrm{V}_{\mathrm{a}-\mathrm{c}}{ }^{*}=\mathrm{min} . \mathrm{V}_{\mathrm{S}}-1,5 \mathrm{~V}$.
Output transistor non-conducting: $\mathrm{I}_{\mathrm{O}}=\mathrm{max} .2 \mathrm{~mA}$ at $\mathrm{V}_{\mathrm{S}}=30 \mathrm{~V}$.
The outputs are continuously tested for short-circuiting. As soon as the short-circuiting is removed, the output stage is automatically reset to normal operation.
Output current (limited to 3 A per module)
for all stages
max. $0,375 \mathrm{~A}$ per stage
for maximum 6 stages
max. 0,5 A per stage

Logic outputs (open collector)

| output | function | terminations of <br> connector 1 (Fig. 3) |
| :--- | :--- | :--- |
| PRF | Preparation of output module finished. | a24 |
| DEF | Data exchange finished. | a25 |
| ALI | Alarm internal; active LOW as long as $\mathrm{V}_{\text {ic }}$ is <br> above 17,5 V ; with opto-coupler isolation <br> between internal and external supply. | a29 |

The external alarm output ALE (connector 2, a2) has a similar function as ALI. It is an open collector output and can sink a current of $10 \mathrm{~mA}\left(\mathrm{~V}_{\text {ALE }}\right.$ LOW $\left.=1,3 \mathrm{~V}\right)$.

## Converter output

Output voltage
Output current
$V_{p}$
Ip
$\mathrm{V}_{\mathrm{p}}$ : on terminals a31, c31 of connector 1
0 V : on terminals a32, c32 of connector 1
$10 \mathrm{~V} \pm 10 \%$
max. 1,7 A; short-
circuit proof **

[^38]MECHANICAL DATA
Dimensions in mm

## Outlines



Fig. 3.
Mass $\quad 400 \mathrm{~g}$

Terminal location

| connector 1 |  |  |  | connector 2 |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| row c |  | row a |  | row c |  | row a |
| MID1 | 1 | HIGH level |  | n.c. | 1 | n.c. |
| $\mathrm{MID}_{2}$ | 2 | HIGH level |  | 0 V * | 2 | ALE |
| MID3 | 3 | HIGH level |  | n.c. | 3 | n.c. |
| MID4 | 4 | HIGH level |  | O V* | 4 | $V$ ic |
| MID5 | 5 | HIGH level | ** | n.c. | 5 | n.c. |
| MID6 | 6 | HIGH level | * | O V* | 6 | $V \mathrm{ic}$ |
| MID7 | 7 | HIGH level |  | n.c. | 7 | n.c. |
| MID8 | 8 | HIGH level |  | 0 V * | 8 | $V_{\text {ic }}$ |
| MID9 | 9 | HIGH level |  | 0 V | 9 | $V_{S}$ |
| MID10 | 10 | HIGH level |  | 0 V | 10 | n.c. |
| $\mathrm{ADD}_{0}$ | 11 | $\mathrm{ADD}_{1}$ |  | 0 V | 11 | $V_{S}$ |
| $\mathrm{ADD}_{2}$ | 12 | $\mathrm{ADD}_{3}$ |  | 0 V | 12 | n.c. |
| $\mathrm{ADD}_{4}$ | 13 | $\mathrm{ADD}_{5}$ |  | 0 V | 13 | $V_{S}$ |
| $\mathrm{ADD}_{6}$ | 14 | $\mathrm{ADD}_{7}$ |  | 0 V | 14 | n.c. |
| $\mathrm{ADD}_{8}$ | 15 | ADD9 |  | 0 V | 15 | $V_{S}$ |
| ADD $_{10}$ | 16 | n.c. |  | 0 V | 16 | n.c. |
| n.c. | 17 | n.c. |  | 0 V | 17 | $\mathrm{V}_{S}$ |
| n.c. | 18 | n.c. |  | 0 V | - 18 | DOY. 0 |
| n.c. | 19 | n.c. |  | 0 V | 19 | $\mathrm{V}_{S}$ |
| n.c. | 20 | n.c. |  | 0 V | 20 | DOY. 1 |
| $\mathrm{DIO}_{0}$ | 21 | $\mathrm{DIO}_{1}$ |  | 0 V | 21 | $\mathrm{V}_{\mathrm{S}}$ |
| $\mathrm{DIO}_{2}$ | 22 | $\mathrm{DIO}_{3}$ |  | 0 V | 22 | DOY. 2 |
| $\mathrm{PHCO}_{0}$ | 23 | $\mathrm{PHC}_{1}$ |  | 0 V | 23 | $\mathrm{V}_{\mathrm{S}}$ |
| n.c. | 24 | PRF |  | 0 V | 24 | DOY. 3 |
| $0 \mathrm{~V}^{* * *}$ | 25 | DEF |  | 0 V | 25 | $\mathrm{V}_{\mathrm{S}}$ |
| SBI | 26 | APF |  | OV | 26 | $\mathrm{DO}_{\mathrm{Z} .0}$ |
| RCO | 27 | REO |  | 0 V | 27 | $\mathrm{V}_{S}$ |
| n.c. | 28 | $\overline{\text { OSD }}$ |  | 0 V | 28 | $\mathrm{DO}_{\mathrm{Z} .1}$ |
| ALI | 29 | ALI |  | 0 V | 29 | $\mathrm{V}_{S}$ |
| n.c. | 30 | n.c. |  | 0 V | 30 | $\mathrm{DO}_{\mathrm{Z} .2}$ |
| $V_{p}$ | 31 | $V_{p}$ |  | 0 V | 31 | $\mathrm{V}_{S}$ |
| 0 V | 32 | OV |  | 0 V | 32 | $\mathrm{DO}_{\mathrm{Z} .3}$ |

Note
Supply-voltage lines $\left(V_{S}\right)$ have to be connected to each group of 4 outputs.

* $\quad 0 V$ for $V_{\text {ic. }}$
** For coding MID-lines.
*** No supply line; is used as return line for control signals.


## DIGITAL TO ANALOGUE MODULE

This output module is for use in PC20 programmable controllers if an analogue voltage or current output level is required. The module contains four 3-decade D/A converters, which accept 3-digit BCD data from the scratchpad memory of the central processor in the PC20 system. Each converter has a voltage output ( 0 to $9,99 \mathrm{~V}$ ) and a current output ( 0 to 20 mA or 4 to 20 mA ) in a grounded load configuration ( 0 to $500 \Omega$ ). The output current range is selected by means of jumper connectors on the module.

Four addresses in the scratchpad memory are reserved for each output (Fig. 1), that means an address area of 16 addresses for 4 outputs. The address range is determined by the coding on the module identification inputs MID4-10.
When the module is switched on in the PC20 system all data latches on the DA20 are set to 0 .
The module has a 3-digit display that enables monitoring of the outputs; channel selection is done with the thumbwheel switch.

|  | $m$ | $m+1$ | $m+2$ | $m+3$ |  |
| :--- | :--- | :--- | :--- | :--- | :--- |
| 3 |  |  |  |  |  |
| 2 |  |  |  |  |  |
| 1 |  |  |  |  |  |
| 0 |  |  |  |  |  |
|  | MSD |  | LSD |  |  |

Fig. 1 Address arrangement in the scratchpad memory.
The addresses $m+3$ are not used.
$m=$ multiple of 4 .


Fig. 2 Block diagram.
The whole circuitry is built on an epoxy printed-wiring board of $233,4 \mathrm{~mm} \times 160 \mathrm{~mm}$ (double Eurocard). The board has two F068-I connectors (board parts); the corresponding rack part of connector 1 (Fig. 4) is available on the back panels, that of connector 2 (external connections) is separately available under catalogue number 242202589288 (pins for wire wrapping), 242202589298 (pins for dipsoldering) or 242202589326 (solder tags).*

[^39]Digital to analogue module

## ELECTRICAL DATA

| Supply voltage (d.c.) for input circuitry |
| :--- | :--- |
| Supply current |

Supply voltage (d.c.)
Supply current logic
Output current ranges
Maximum output impedance of current output
Output voltage range
Minimum output impedance of voltage output
Non-linearity of D/A converters

| $V_{S}$ | $24 \mathrm{~V} \pm 25 \%$ |  |
| :--- | :--- | :--- |
| $\mathrm{I}_{\mathrm{S}}$ | $\max .250 \mathrm{~mA}$ |  |
| $\mathrm{~V}_{\mathrm{P}}$ | $10 \mathrm{~V} \pm 10 \%$ |  |
| $\mathrm{I}_{\mathrm{P}}$ | $\max .60 \mathrm{~mA}$ |  |
|  | 0 to 20 mA | selectable |
|  | 4 to 20 mA | by jumper |

Accuracy of voltage to current conversion (current output is derived from voltage output)
$500 \Omega$
0 to $9,99 \mathrm{~V}$
$2 \mathrm{k} \Omega$
$\pm 1 \mathrm{LSB}$
$\pm 0,25 \%$

## Input and output data

All inputs meet the standard LOCMOS specifications.

|  | function | terminations <br> connector 1 (Fig. 4) |
| :---: | :---: | :---: |
| INPUTS |  |  |
|  | Address bits from central processor. | a11 c 11 <br> a 12 c 12 <br> a 13 c 13 <br> a 14 c 14 <br> a 15 c 15 <br>  c 16 |
| APF | Handshake signal, indicates that addresses are correct. | a26 |
| $\mathrm{DIO}_{0}$ <br> $\mathrm{DIO}_{1}$ <br> $\mathrm{DIO}_{2}$ <br> $\mathrm{DIO}_{3}$ | Data bits from central processor. | a21 c21 <br> a22 c22 |
| $\mathrm{MID}_{4}$ <br> $\mathrm{MID}_{5}$ <br> MID $_{6}$ <br> $\mathrm{MID}_{7}$ <br> $\mathrm{MID}_{8}$ <br> $\mathrm{MID}_{9}$ <br> MID 10 | Module identification inputs; provide module with individual identity. | c4 <br> c5 <br> c6 <br> c7 <br> c8 <br> c9 <br> c10 |
| $\begin{aligned} & \mathrm{PHC}_{0} \\ & \mathrm{PHC}_{1} \end{aligned}$ | Phase control signals. | a23 c23 |
| $\overline{\text { RCO }}$ | Reset signal from central processor, to reset all data latches. | c27 |
| SBI | Clock signal from central processor to clock data into latches. | c26 |

Digital to analogue module

|  | function | terminations of <br> connector 1 (Fig. 4) |
| :--- | :--- | :--- |

OUTPUTS

| DEF | Data exchange finished (open collector output). | a25 |
| :--- | :--- | :--- |
| PRF | Preparation of addressing DA20 finished <br> (open collector output). | a24 |


|  | function | terminations of <br> connector 2 (Fig. 4) |
| :--- | :--- | :--- |

ANALOGUE OUTPUTS

| $\mathrm{VO}_{0}$ <br> $\mathrm{CO}_{0}$ <br> COM | Voltage output of channel 0 Current output of channel 0 Common | $\begin{aligned} & \mathrm{a} 4 \\ & \mathrm{a} 2 \end{aligned}$ | c2/c4 |
| :---: | :---: | :---: | :---: |
| $\mathrm{VO}_{1}$ $\mathrm{CO}_{1}$ COM | Voltage output of channel 1 Current output of channel 1 Common | $\begin{aligned} & \text { a8 } \\ & \text { a6 } \end{aligned}$ | c6/c8 |
| $\begin{aligned} & \mathrm{VO}_{2} \\ & \mathrm{CO}_{2} \\ & \mathrm{COM} \end{aligned}$ | Voltage output of channel 2 Current output of channel 2 Common | $\begin{aligned} & \text { a12 } \\ & \text { a10 } \end{aligned}$ | c10/c12 |
| $\mathrm{VO}_{3}$ <br> $\mathrm{CO}_{3}$ <br> COM | Voltage output of channel 3 Current output of channel 3 Common | $\begin{aligned} & \text { a16 } \\ & \text { a14 } \end{aligned}$ | c14/c16 |

## ADJUSTMENTS FOR OPERATION

For the 4 channels the output current range can be selected by positioning the jumpers $\mathbf{0 , 1 , 2}$ and 3 (Fig. 3) as shown below.

| output current range | position of the relative jumper* |
| :--- | :---: |
| 0 to 20 mA | 0 0 <br>  0 |
| 4 to 20 mA | 0 |

* Module in position as shown in Fig. 3.

Fig. 3 Location of jumpers for adjustment of output current range.


Digital to analogue module

## MECHANICAL DATA

Dimensions in mm

## Outlines



Fig. 4.

Mass
approx. 270 g

## Terminal location

| connector 1 |  |  | connector 2 |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| row c |  | row a | row c |  | row a |
| n.c. | 1 | n.c. | n.c. | 1 | n.c. |
| n.c. | 2 | n.c. | COM | 2 | $\mathrm{CO}_{0}$ |
| n.c. | 3 | n.c. | n.c. | 3 | n.c. |
| $\mathrm{MID}_{4}$ | 4 | HIGH level | COM | 4 | $\mathrm{VO}_{0}$ |
| MID5 | 5 | HIGH level | n.c. | 5 | n.c. |
| MID6 | 6 | HIGH level | COM | 6 | $\mathrm{CO}_{1}$ |
| $\mathrm{MID}_{7}$ | 7 | HIGH level $\}^{* *}$ | n.c. | 7 | n.c. |
| $\mathrm{MID}_{8}$ | 8 | HIGH level | COM | 8 | $\mathrm{VO}_{1}$ |
| MID9 | 9 | HIGH level | n.c. | 9 | n.c. |
| MID10 | 10 | HIGH level | COM | 10 | $\mathrm{CO}_{2}$ |
| $\mathrm{ADD}_{0}$ | 11 | $\mathrm{ADD}_{1}$ | n.c. | 11 | n.c. |
| $\mathrm{ADD}_{2}$ | 12 | $\mathrm{ADD}_{3}$ | COM | 12 | $\mathrm{VO}_{2}$ |
| $\mathrm{ADD}_{4}$ | 13 | $\mathrm{ADD}_{5}$ | n.c. | 13 | n.c. |
| $\mathrm{ADD}_{6}$ | 14 | $\mathrm{ADD}_{7}$ | COM | 14 | $\mathrm{CO}_{3}$ |
| $\mathrm{ADD}_{8}$ | 15 | ADD9 | n.c. | 15 | n.c. |
| ADD10 | 16 | n.c. | COM | 16 | $\mathrm{VO}_{3}$ |
| n.c. | 17 | n.c. | n.c. | 17 | n.c. |
| n.c. | 18 | n.c. | n.c. | 18 | n.c. |
| n.c. | 19 | n.c. | n.c. | 19 | n.c. |
| n.c. | 20 | n.c. | n.c. | 20 | n.c. |
| $\mathrm{DIO}_{0}$ | 21 | $\mathrm{DIO}_{1}$ | n.c. | 21 | n.c. |
| $\mathrm{DIO}_{2}$ | 22 | $\mathrm{DIO}_{3}$ | n.c. | 22 | n.c. |
| $\mathrm{PHC}_{0}$ | 23 | $\mathrm{PHC}_{1}$ | n.c. | 23 | n.c. |
| n.c. | 24 | PRF | n.c. | 24 | n.c. |
| $0 \mathrm{~V}^{*}$ | 25 | DEF | n.c. | 25 | n.c. |
| SBI | 26 | APF | n.c. | 26 | n.c. |
| $\overline{\mathrm{RCO}}$ | 27 | n.c. | n.c. | 27 | n.c. |
| n.c. | 28 | n.c. | n.c. | 28 | n.c. |
| n.c. | 29 | n.c. | n.c. | 29 | n.c. |
| n.c. | 30 | n.c. | n.c. | 30 | n.c. |
| $V_{P}$ | 31 | $V_{p}$ | 0 V | 31 | $V_{S}$ |
| 0 V | 32 | 0 V | n.c. | 32 | n.c. |

* No supply line, is used as return line for control signals.
** For coding MID lines.


## BIDIRECTIONAL PARALLEL INTERFACE

## DESCRIPTION

The RP20 is intended for use as an interface between a PC20-system and data input and output devices, e.g. thumbwheel switches, seven-segment displays, etc.

The module has 16 enable outputs, each of which can select an eight-bit input or output device, so it has a capacity of $16 \times 8$ bits and therefore it occupies 32 four-bit places in the input/output field. When an enable output selects an input device, this device will put 8 bits of information on the data lines. This data information is stored in the buffer memory of the RP20. When an output device is selected, data is transferred from the buffer memory to this device. The lower enable lines always select outputs; inputs are selected by the remaining lines. Separation between these two groups is done by means of the SCIO inputs, which determine the number of outputs that are scanned.
Enabling always starts at $E N_{0}$ and finishes at $E N_{15}$. The scanning rate can be chosen by means of switches on the module.
After having activated successively all enable outputs the RP20 stops scanning, activates its $\overline{\text { READY }}$ output and enables the central processor to get access to the buffer memory. Data exchange between central processor and RP20 takes place during the I/O-phase in which the RP20 is scanned. As soon as the central processor finishes this I/O-phase, the RP2O disables the central processor access to its memory and starts scanning the inputs and outputs, provided the START input is at the high level. If the START input is at the low level, scanning is postponed until this level is high again. During scanning the RP20 ignores the addressing of the central processor; this does not influence the cycle time of the PC20-system.
The start procedure is initiated by a low level on the RCO input. First all buffer memory locations of the RP20 are set to 0 , then there will be a data exchange between the scratchpad memory of the central processor and the buffer memory of the RP20. At the moment central processor finishes the I/O-phase, the RP20 starts scanning the input and output devices.
Data lines, enable lines, $\overline{\text { READY }}$ output and START input are electrically isolated from the PC20 circuitry by means of photocouplers.
Although the system is designed for use in combination with input and output devices requiring 24 V supply, the RP20 can be adapted for use with devices for 5 V supply by means of a jumper on the printed-wiring board.
The RP20 is built on an epoxy-glass printed-wiring board of $233,4 \mathrm{~mm} \times 160 \mathrm{~mm}$ (double Euro-card). The board has two F068-I connectors (board parts); the corresponding rack part of connector 1 (Fig. 7) is available on the back panels, that of connector 2 (external connections) is separately available under catalogue number 242202589288 (pins for wire wrapping), 242202589298 (pins for dip-soldering) or 242202589326 (solder tags).*

[^40]
## ELECTRICAL DATA

## Supply

| Supply voltage (d.c.) |  | $V_{p}$ | $10 \mathrm{~V} \pm 10 \%$ |
| :---: | :---: | :---: | :---: |
| Supply current |  | Ip | $\max .150 \mathrm{~mA}\left(\mathrm{~V}_{\mathrm{P}}=10 \mathrm{~V}\right.$, all outputs used, all data 0 ) |
| Supply voltage (d.c.) | for | $\mathrm{V}^{*}{ }^{*}$ | $24 \mathrm{~V} \pm 25 \%$ |
| Supply current | output circuitry | IS | max. 250 mA (all data lines at low level) min. 20 mA (all data lines at high level) |
| Supply voltage (d.c.) | for | $\mathrm{V}_{\mathrm{S}}{ }^{*}$ | $5 \mathrm{~V} \pm 5 \%^{* *}$ |
| Supply current | output circuitry | IS | max. 250 mA (all data lines and inverting inputs at low level, 4 enable lines inverted) <br> min. 20 mA (all data lines at high level) |

* The value of $V_{S}$ depends on the supply voltage and signal levels required for the input and output devices.
** To be adjusted by means of a jumper; see 'ADJUSTMENTS'.


## Input and output data

The inputs at connector 1 meet the standard LOCMOS specifications; the inputs and outputs at connector 2 are electrically isolated from the logic part by means of photocouplers.

|  | function | terminations (Fig. 7) |  |
| :--- | :--- | :--- | :--- |
|  |  | connector 1 | connector 2 |

INPUTS

| $\mathrm{ADD}_{0}$ $\mathrm{ADD}_{1}$ $\mathrm{ADD}_{2}$ $\mathrm{ADD}_{3}$ $\mathrm{ADD}_{4}$ $\mathrm{ADD}_{5}$ $A^{A D D} 6$ $\mathrm{ADD}_{7}$ ADD8 $\mathrm{ADD}_{9}$ ADD $_{10}$ | Address bits from central processor; <br> $A D D_{0-4}$ select the memory position on the module, $A D D_{5-10}$ select the module. |  $c 11$ <br> a11 c12 <br> a12 c13 <br> a13 c14 <br> a14 c15 <br> a15 c16 |  |
| :---: | :---: | :---: | :---: |
| APF | Handshake signal, indicates that addresses are correct. | a26 |  |
| INVI | Input that inverts input information; input current LOW: 10 mA . |  | a24 |
| INVO | Input that inverts output information; input current LOW: 10 mA . |  | c24 |
| MID $_{5}$ <br> $\mathrm{MID}_{6}$ <br> $\mathrm{MID}_{7}$ <br> $\mathrm{MID}_{8}$ <br> MID9 <br> MID $_{10}$ | Module identification inputs; provide module with individual identity. | c5 $c 6$ $c 7$ $c 8$ $c 9$ $c 10$ |  |
| $\begin{aligned} & \mathrm{PHC}_{0} \\ & \mathrm{PHC}_{1} \\ & \hline \end{aligned}$ | Phase control signals from central processor. | $\text { a23 } \mathrm{c} 23$ |  |
| $\overline{\mathrm{RCO}}$ | Reset from central processor (low level) during switch-on. | c27 |  |
| $\mathrm{SClO}_{0}$ <br> $\mathrm{SClO}_{1}$ <br> $\mathrm{SClO}_{2}$ <br> $\mathrm{SClO}_{3}$ | Input/output separation code inputs, control the $\mathrm{R} / \overline{\mathrm{W}}$ line to central processor, and determine whether data is received or sent on $\mathrm{DB}_{0-7}$. | $\begin{aligned} & \mathrm{c} 17 \\ & \mathrm{c} 18 \\ & \mathrm{c} 19 \\ & \mathrm{c} 20 \end{aligned}$ |  |
| START | A high level ( 24 V ) starts a scanning cycle of the RP20; if this input is kept HIGH permanently, scanning starts immediately after the I/O cycle during which data was exchanged; input current high: 10 mA . For 5 V-level operation, see 'ADJUSTMENTS'. |  | c20 |


|  | function | terminations (Fig. 7) |  |
| :---: | :---: | :---: | :---: |
|  |  | connector 1 | connector 2 |
| BI-DIRECTIONAL BUSES |  |  |  |
| $\mathrm{DIO}_{0}$ <br> $\mathrm{DIO}_{1}$ <br> $\mathrm{DIO}_{2}$ <br> $\mathrm{DIO}_{3}$ | Data bits to and from central processor. | $\begin{array}{ll}  & \mathrm{c} 21 \\ \mathrm{a} 21 & \\ \text { a22 } & \mathrm{c} 22 \end{array}$ |  |
| $\begin{aligned} & \mathrm{DB}_{0} \\ & \mathrm{DB}_{1} \\ & \mathrm{DB}_{2} \\ & \mathrm{DB}_{3} \\ & \mathrm{DB}_{4} \\ & \mathrm{DB}_{5} \\ & \mathrm{DB} 6 \\ & \mathrm{DB} 7 \end{aligned}$ | These external data bus terminals form outputs when the enable outputs of the first group are activated, and inputs during activation of the second group. $A$ " 1 " in the scratchpad memory of the central processor will be represented as a high level at these outputs, provided $\overline{\mathrm{INVO}}$ input is at high level (or floating). If $\overline{\text { NVO }}$ input is at low level a " 1 " will be represented as a low level. <br> A high level at these inputs will be represented in the scratchpad memory as a " 0 " when the INVI input is at the high level (or floating). <br> A low level of the INVI input causes a high level to become a " 1 ". <br> $\mathrm{DB}_{0-7}$ occupy two four-bit places in the scratchpad memory; $\mathrm{DB}_{0-3}$ occupy the lower place, $\mathrm{DB}_{4-7}$ occupy the higher place. <br> Input current low ( $\mathrm{I}_{\mathrm{i}} \mid$ ): 10 mA ; output current low ( $\mathrm{I}_{\mathrm{ol}}$ ): max. 15 mA ; see Fig. 1. |  | a26  <br> c28 c26 <br> a30 c28 <br> a32 c30 <br>  c32 |

## OUTPUTS

| $\overline{\mathrm{EN}}$ |  | a2 |  |
| :---: | :---: | :---: | :---: |
| $\mathrm{EN}_{1}$ |  |  | c2 |
| EN2 | Enable outputs (open collector); select an input or | a4 |  |
| $\mathrm{EN}_{3}$ | output device. |  | c4 |
| $\mathrm{EN}_{4}$ | During the scanning period of the RP20, these outputs | a6 |  |
| $\mathrm{EN}_{5}$ | go successively to the low level, enabling an input |  | c6 |
| $\mathrm{EN}_{6}$ | device to put its information on $\mathrm{DB}_{0}^{-7} 7$, or an output | a8 |  |
| $\mathrm{EN}_{7}$ | device to store the information from this bus. |  | c8 |
| $\mathrm{EN}_{8}$ | For devices requiring a high level for enabling, see | a10 |  |
| $\overline{\mathrm{EN}} 9$ | 'ADJUSTMENTS'. |  | c10 |
| EN10 | Each enable output corresponds with two four-bit | a12 |  |
| EN11 | places; the lower enable lines refer to the lower |  | c12 |
| EN12 | scratchpad places. Output current: max. 120 mA at | a14 |  |
| EN13 | 0,5 V. |  | c14 |
| EN14 |  | a16 |  |
| $\overline{E N}_{15}$ |  |  | c16 |


| function | terminations (Fig. 7) |  |  |
| :--- | :--- | :--- | :--- |
|  |  | connector 1 | connector 2 |
| DEF | Data exchange finished (open collector output) | a 25 |  |
| PRF | Preparation of RP20 finished (open collector output) | a 24 | a 20 |
| READY | A low level indicates that RP20 finished I/O scanning <br> (open collector output); output current low: max. <br> 20 mA at 0,5 V. |  | c 24 |
| R/W | A low level indicates that the central processor has to <br> receive data (open collector output). |  |  |



Fig. 1 External data bus circuit. Points $A$ to be bridged for 5 V supply, see "ADJUSTMENTS".

Time data (see also Figs 2 and 3)

Scanning time for one input or output
Time that scanning pulse is active
Time that input information must become stable
Time between two scanning pulses
Time between enable output active and output data valid
Time that output data remains valid
Total scanning time

$$
\begin{aligned}
& \mathrm{t}_{\mathrm{o}} \\
& \mathrm{t}_{\mathrm{sc}}=0,8 \mathrm{t}_{\mathrm{o}} \\
& \mathrm{t}_{\mathrm{v}}=\max \cdot 0,7 \mathrm{t}_{\mathrm{o}}-50 \mu \mathrm{~s} \\
& \mathrm{t}_{1}=0,2 \mathrm{t}_{\mathrm{o}} \\
& \mathrm{t}_{2}=\max \cdot 40 \mu \mathrm{~s} \\
& \mathrm{t}_{3}=0,1 \mathrm{t}_{\mathrm{o}} \\
& \mathrm{t}_{\mathrm{s}}=16 \mathrm{t}_{\mathrm{o}}
\end{aligned}
$$

To be adjusted with switches on the module, see 'ADJUSTMENTS'.

| $\mathrm{t}_{\mathrm{s}}$ <br> ms | $\mathrm{t}_{\mathrm{o}}$ |
| ---: | ---: |
| $\mu \mathrm{s}$ |  |, | +12 | 320 |
| ---: | ---: |
| 10,24 | 640 |
| 20,48 | 1280 |
| 40,96 | 2560 |



Fig. 2.


Fig. 3.

Bidirectional parallel interface

## ADJUSTMENTS

Adjustment for use with devices requiring 5 V supply
If the input and output devices require 5 V levels, the supply voltage $\left(\mathrm{V}_{\mathrm{S}}\right)$ should be 5 V . By bridging the points A (Figs 1 and 5 ) with a jumper, the module is adapted for 5 V supply.

## Adjustment for 5 V level operation on START input

For 5 V level operation on the START input, a resistor of $360 \Omega$ should be connected between the points $B$ (Figs. 4 and 5 ).


7Z86308.1

Fig. 4.


Fig. 5.

## Adjustment for use with devices requiring a high level for enabling

For devices which require a high level for enabling, it is necessary to invert the outputs $\overline{E N}_{0}, \overline{E N}_{1}, \overline{E N}_{14}$ and $\overline{\mathrm{EN}}_{15}$ by means of switches on the printed-wiring board (Fig. 6). The following points have to be connected:
point 1 to point 16: $\mathrm{EN}_{14}$ is inverted;
point 2 to point 15: $E N_{1}$ is inverted;
point 3 to point 14: $\mathrm{EN}_{15}$ is inverted;
point 4 to point 13: $E N_{0}$ is inverted.
Proper functioning is only possible if the 5 V -jumper is used (Fig. 5).
For inverting purposes a transistor BC337 with common emitter and a resistor of $4700 \Omega$ between base and emitter have been added; the collector has been connected to output CT (termination c18, connector 2 ), the base to input BT (termination a18, connector 2 ).

## Adjustment of scanning time

The total scanning time ( $\mathrm{t}_{\mathrm{s}}$, Fig. 3) can be adjusted with switches on the printed-wiring board (Fig. 6). A choice can be made of the following connections:
point 5 to point $12: \mathrm{t}_{\mathrm{s}}=40,96 \mathrm{~ms}$;
point 6 to point $11: \mathrm{t}_{\mathrm{s}}=10,24 \mathrm{~ms}$;
point 7 to point 10 : $\mathrm{t}_{\mathrm{s}}=20,48 \mathrm{~ms}$;
point 8 to point $9: \mathrm{t}_{\mathrm{s}}=5,12 \mathrm{~ms}$.
Note: Only one connection should be made.


Fig. 6.

## MECHANICAL DATA

Dimensions in mm

## Outlines



Fig. 7.

Mass approx. 270 g

Terminal location

| connector 1 |  |  | connector 2 |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| row c |  | row a | row c |  | row a |
| n.c. | 1 | n.c. | n.c. | 1 | n.c. |
| n.c. | 2 | n.c. | $\overline{E N}_{1}$ | 2 | $\overline{E N}_{0}$ |
| n.c. | 3 | n.c. | n.c. | 3 | n.c. |
| n.c. | 4 | n.c. | $\overline{E N}_{3}$ | 4 | $\overline{E N}_{2}$ |
| MID 5 | 5 | HIGH level | n.c. | 5 | n.c. |
| MID 6 | 6 | HIGH level | $\overline{E N}_{5}$ | 6 | $\overline{E N}_{4}$ |
| $\mathrm{MID}_{7}$ | 7 | HIGH level | n.c. | 7 | n.c. |
| $\mathrm{MID}_{8}$ | 8 | HIGH level | $\overline{E N}_{7}$ | 8 | $\overline{E N}_{6}$ |
| MID9 | 9 | HIGH level | n.c. | 9 | n.c. |
| MID10 | 10 | HIGH level | $\overline{E N}_{9}$ | 10 | $\overline{E N}_{8}$ |
| $\mathrm{ADD}_{0}$ | 11 | $\mathrm{ADD}_{1}$ | n.c. | 11 | n.c. |
| $\mathrm{ADD}_{2}$ | 12 | $\mathrm{ADD}_{3}$ | $\overline{E N}_{11}$ | 12 | $\mathrm{EN}_{10}$ |
| $\mathrm{ADD}_{4}$ | 13 | $\mathrm{ADD}_{5}$ | n.c. | 13 | n.c. |
| $\mathrm{ADD}_{6}$ | 14 | $\mathrm{ADD}_{7}$ | $\overline{E N}_{13}$ | 14 | $\mathrm{EN}_{12}$ |
| $\mathrm{ADD}_{8}$ | 15 | ADD9 | n.c. | 15 | n.c. |
| ADD10 | 16 | n.c. | $\mathrm{EN}_{15}$ | 16 | EN14 |
| $\mathrm{SClO}_{0}$ | 17 | HIGH level | n.c. | 17 | n.c. |
| $\mathrm{SCIO}_{1}$ | 18 | HIGH level | CT | 18 | BT |
| $\mathrm{SClO}_{2}$ | 19 | HIGH level | n.c. | 19 | n.c. |
| $\mathrm{SClO}_{3}$ | 20 | HIGH level | START | 20 | READY |
| $\mathrm{DIO}_{0}$ | 21 | $\mathrm{DIO}_{1}$ | n.c. | 21 | n.c. |
| $\mathrm{DIO}_{2}$ | 22 | $\mathrm{DIO}_{3}$ | n.c. | 22 | n.c. |
| $\mathrm{PHC}_{0}$ | 23 | $\mathrm{PHC}_{1}$ | n.c. | 23 | n.c. |
| R/ $\bar{W}$ | 24 | PRF | $\overline{\text { INVO }}$ | 24 | INVI |
| 0 V | 25 | DEF | n.c. | 25 | n.c. |
| SBI | 26 | APF | DB1 | 26 | $\mathrm{DB}_{0}$ |
| $\overline{\mathrm{RCO}}$ | 27 | n.c. | n.c. | 27 | n.c. |
| n.c. | 28 | n.c. | $\mathrm{DB}_{3}$ | 28 | $\mathrm{DB}_{2}$ |
| n.c. | 29 | n.c. | OV | 29 | $V_{S}{ }^{*}$ |
| n.c. | 30 | n.c. | $\mathrm{DB}_{5}$ | 30 | $\mathrm{DB}_{4}$ |
| V | 31 | $V_{p}$ | OV | 31 | $\mathrm{V}_{\mathrm{S}}{ }^{*}$ |
| 0 V | 32 | 0 V | $\mathrm{DB}_{7}$ | 32 | $\mathrm{DB}_{6}$ |

[^41]
## BIDIRECTIONAL SERIAL INTERFACE

The RS20 is for remote control of input and output modules of a PC2O-system (passive slave). Furthermore it allows two PC20-systems to be connected to each other in a master/slave configuration, for data exchange between the systems (active slave); see Fig. 1.

Both master and slave station must have an RS20 module and they must be connected to each other via a coaxial cable or a shielded twisted pair of wires.
The RS20 performs three modes of operation, which are selected by the levels on inputs BMS and CMS, as shown in Table INPUTS, paragraph ELECTRICAL DATA.

Mode A (master mode): when used in the master PC20-system for communication with one slave station.

Mode B (active slave mode) : when used in the slave PC20-system with a central processor.
Mode C (passive slave mode): when used in the slave PC20-system, which includes only input and output modules, to transfer data without further processing.


Fig. 1.

Master/slave communication takes place via the 256-bit RAM buffer memories of the RS20 modules. The data transfer rate is 256 bits in $0,75 \mathrm{~ms}$. Within this time all control and data is transferred and checked.
Whether data are handled as inputs or outputs is established by the setting of the SCIO coding inputs. Error detection is accomplished by Cyclic Redundancy Checking. The $\overline{\text { ERROR }}$ output is set to 0 if an error has been detected on received data at either or both ends of the external data line. This output is also set to 0 during the first 120 ms after switching on the supply voltage, and after 60 ms if no communication has taken place. During this period continuous testing takes place to restore communication. If the ERROR output is set to 0 , the LED at the front of the module is lit.
After data exchange between the PC20-systems, the $\overline{\text { READY }}$ output is set to 0 , and the RS20 is ready for internal data exchange between its buffer memory and the scratchpad memory of the PC20-system of which it forms part, or the connected input and output modules. This internal data exchange takes place during the I/O phase in which the RS2O is scanned. The sequence of the various data flows is shown in Fig. 2.


Fig. 2.
The RS20 is built on an epoxy-glass printed-wiring board of $233,4 \mathrm{~mm} \times 160 \mathrm{~mm}$ (double Euro-card). The board has two F068-I connectors (board parts); the corresponding rack part of connector 1 (Fig. 7) is available on the back panels, that of connector 2 (external connections) is separately available under catalogue number 242202589288 (pins for wire wrapping), 242202589298 (pins for dip-soldering) or 242202589326 (solder tags).*

* For a general description of the Euro-card system see IEC 297 or DIN 41494 for 19 in racks and IEC 130-14 or DIN 41612 for connectors.


## ELECTRICAL DATA

| Supply voltage (d.c.) | logic | $V_{P}$ | $10 \mathrm{~V} \pm 10 \%$ |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Supply current |  | $\mathrm{I}_{\mathrm{p}}$ | typ. |  | mA |
| Supply voltage (d.c.) | for input/output | $\mathrm{V}_{\text {S }}$ | $24 \mathrm{~V} \pm 25 \%$ |  |  |
| Supply current | circuitry | Is | typ. |  | mA |
| Output voltage between $\mathrm{TR}_{1}$ and $\mathrm{TR}_{3}{ }^{*}$ |  | $V_{o(p-p)}$ | min. | 5,66 | V |
| Input voltage between $\mathrm{TR}_{1}$ and $\mathrm{TR}_{3}{ }^{*}$ |  | $V_{i(p-p)}$ | min. | 4,24 | V |
| Input impedance between $\mathrm{TR}_{1}$ and $\mathrm{TR}_{3}{ }^{*}$ |  | $z_{i}$ | approx. | 75 | $\Omega$ |
| Data transfer rate |  |  |  | 400 | kbaud |

## Connection between master and slave station

For distances up to 250 m a shielded twisted pair of wires, max. loop resistance $50 \Omega$, with polythene insulation can be used (Fig. 4). For larger distances a coaxial cable has to be used (Fig. 3), e.g. COAX-12** for max. 750 m , or BAMBOO-SIX** for max. 2000 m .


Fig. 3 Connection of bidirectional busses via a coaxial cable.


Fig. 4 Connection of bidirectional busses, via a shielded twisted pair of wires.

[^42]
## Input and output data

All inputs and outputs meet the standard LOCMOS specifications, unless otherwise specified.

|  | function | terminations (Fig. 7) |  |
| :--- | :--- | :--- | :---: |
|  |  | connector 1 | connector 2 |

BI-DIRECTIONAL DATA BUSSES

| $\mathrm{ADD}_{0}$ |  | c11 |  |
| :---: | :---: | :---: | :---: |
| $\mathrm{ADD}_{1}$ |  |  |  |
| $\mathrm{ADD}_{2}$ |  | c12 |  |
| $\mathrm{ADD}_{3}$ |  | a12 |  |
| $\mathrm{ADD}_{4}$ | Address bits. | c13 |  |
| $\mathrm{ADD}_{5}$ | Inputs in A and B modes, outputs in C mode. |  |  |
| $\mathrm{ADD}_{6}$ |  | c14 |  |
| $\mathrm{ADD}_{7}$ |  | a14 |  |
| $\mathrm{ADD}_{8}$ |  | c15 |  |
| $\mathrm{ADD}_{9}$ |  | $\text { a } 15$ |  |
| $\mathrm{ADD}_{10}$ |  |  |  |
| APF | Handshake signal, indicates that addresses are correct. Input in A and B modes, output in C mode. | a26 |  |
| $\mathrm{DIO}_{0}$ |  | c21 |  |
| $\mathrm{DIO}_{1}$ | Data exchange between RS20 and PC20 system. | a21 |  |
| $\mathrm{DIO}_{2}$ |  | c22 |  |
| $\mathrm{DIO}_{3}$ |  | a22 |  |
| $\begin{aligned} & \mathrm{PHC}_{0} \\ & \mathrm{PHC}_{1} \end{aligned}$ | Phase control. <br> Inputs in A and B modes, outputs in C mode. | $\mathrm{a}^{\mathrm{c} 3}{ }^{\mathrm{c} 23}$ |  |
| SBI | Store command; <br> Stores data in buffer memory during I/O cycle. Input in A and B modes, output in C mode. | c26 |  |
| $\begin{aligned} & \mathrm{TR}_{1} \\ & \mathrm{TR}_{2} \\ & \mathrm{TR}_{3} \end{aligned}$ | Transmit/receive terminals for connection of external data line ( $\mathrm{TR}_{2}$ common); via transformer coupled to the inner ceircuitry of the RS20, (Figs 3 and 4). |  | $\begin{aligned} & \text { c26 } \\ & \text { c28 } \\ & \text { c30 } \end{aligned}$ |


|  | function | terminations (Fig. 7) |  |
| :---: | :---: | :---: | :---: |
|  |  | connector 1 | connector 2 |
| INPUTS |  |  |  |
| $\begin{aligned} & \text { BMS } \\ & \text { CMS } \end{aligned}$ | Mode select inputs. <br> Mode A: BMS and CMS are LOW. <br> Mode B: BMS is HIGH, CMS is LOW. <br> Mode C: BMS is HIGH or LOW, CMS is HIGH. | $\begin{aligned} & c 1 \\ & c 2 \end{aligned}$ |  |
| $\mathrm{MID}_{6}$ <br> $\mathrm{MID}_{7}$ <br> MID8 <br> MID9 <br> MID 10 | Module identification inputs; provide module with individual identity. | $\begin{aligned} & \text { c6 } \\ & \text { c7 } \\ & \text { c8 } \\ & \text { c9 } \\ & \text { c10 } \end{aligned}$ |  |
| $\mathrm{SCIO}_{0}$ <br> $\mathrm{SCIO}_{1}$ <br> $\mathrm{SClO}_{2}$ <br> $\mathrm{SClO}_{3}$ | Input/output separation coding inputs. Numbers smaller than code are outputs (seen from PC20 master system); other numbers are inputs. | $\begin{aligned} & \mathrm{c} 17 \\ & \mathrm{c} 18 \\ & \mathrm{c} 19 \\ & \mathrm{c} 20 \end{aligned}$ |  |
| START | Enables external data exchange. Input is isolated from the internal circuitry with photo-isolator (Fig. 5), to be connected to an OM20 output. <br> LOW input level: 0 to 7 V ; HIGH input level: 18 to 30 V . |  | c20 |



Fig. 5 Circuit diagram of START input.
(1) For 5 V -level operation a resistor of $360 \Omega \pm 5 \%$, style CR25, has to be connected.

| function | terminations (Fig. 7) |  |  |
| :--- | :---: | :---: | :---: |
|  |  | connector 1 | connector 2 |

OUTPUTS

| DEF | Signal to central processor, indicating that data from central processor has been stored. | a25 |  |
| :---: | :---: | :---: | :---: |
| $\overline{\mathrm{DER}}$ * | Detected error output, indicating an error has been detected on data received from the other RS20 module. |  | c14 |
| $\overline{\text { ERROR }}{ }^{*}$ | Error output, indicating data exchange along the external data line did not happen errorless or did not happen at all |  | c16 |
| PRF | Preparation of RS2O finished (open collector output) | a24 |  |
| $\overline{\text { READY }}{ }^{*}$ | Output, indicating RS2O has finished external data exchange. |  | a20 |
| R/W | Read-write level PC20-system. Only active during I/O-phase. | c24 |  |
| $\overline{\mathrm{TER}}$ * | Transmitted error output, indicating the RS-20 at the other side of the external data line has detected an error on the received data. |  | c12 |

* Open-collector output; isolated from the internal circuitry with photo-isolator (Fig. 6). To be connected to IM20 inputs.
Maximum sink current: 25 mA ; maximum collector voltage in off-position: 30 V .


Fig. 6 Circuit diagram of $\overline{\text { ERROR }}, \overline{D E R}, \overline{T E R}$ and $\overline{\text { READY }}$ outputs.

MECHANICAL DATA
Outlines


Fig. 7.

Terminal location
connector 1

| row c |  | row a |
| :---: | :---: | :---: |
| BMS | 1 | HIGH level |
| CMS | 2 | HIGH level |
| n.c. | 3 | n.c. |
| n.c. | 4 | n.c. |
| n.c. | 5 | n.c. |
| MID6 | 6 | HIGH level |
| $\mathrm{MID}_{7}$ | 7 | HIGH level |
| MID8 | 8 | HIGH level |
| MID9 | 9 | HIGH level |
| MID 10 | 10 | HIGH level |
| $\mathrm{ADD}_{0}$ | 11 | $\mathrm{ADD}_{1}$ |
| $\mathrm{ADD}_{2}$ | 12 | $\mathrm{ADD}_{3}$ |
| $\mathrm{ADD}_{4}$ | 13 | $\mathrm{ADD}_{5}$ |
| $\mathrm{ADD}_{6}$ | 14 | $\mathrm{ADD}_{7}$ |
| $\mathrm{ADD}_{8}$ | 15 | ADD9 |
| ADD 10 | 16 | n.c. |
| $\mathrm{SClO}_{0}$ | 17 | HIGH level |
| $\mathrm{SClO}_{1}$ | 18 | HIGH level |
| $\mathrm{SClO}_{2}$ | 19 | HIGH level |
| $\mathrm{SClO}_{3}$ | 20 | HIGH level |
| $\mathrm{DIO}_{0}$ | 21 | $\mathrm{DIO}_{1}$ |
| $\mathrm{DIO}_{2}$ | 22 | $\mathrm{DIO}_{3}$ |
| $\mathrm{PHC}_{0}$ | 23 | $\mathrm{PHC}_{1}$ |
| $\mathrm{R} / \overline{\mathrm{W}}$ | 24 | PRF |
| 0 V * | 25 | DEF |
| SBI | 26 | APF |
| n.c. | 27 | n.c. |
| n.c. | 28 | n.c. |
| n.c. | 29 | n.c. |
| n.c. | 30 | n.c. |
| $V_{p}$ | 31 | $V_{p}$ |
| 0 V | 32 | 0 V |

connector 2
row c

| n.c. | 1 | n.c. |
| :---: | :---: | :---: |
| n.c. | 2 | n.c. |
| n.c. | 3 | n.c. |
| n.c. | 4 | n.c. |
| n.c. | 5 | n.c. |
| n.c. | 6 | n.c. |
| n.c. | 7 | n.c. |
| n.c. | 8 | n.c. |
| n.c. | 9 | n.c. |
| n.c. | 10 | n.c. |
| n.c. | 11 | n.c. |
| $\overline{\text { TER }}$ | 12 | n.c. |
| n.c. | 13 | n.c. |
| $\overline{\text { DER }}$ | 14 | n.c. |
| n.c. | 15 | n.c. |
| $\overline{\text { ERROR }}$ | 16 | n.c. |
| n.c. | 17 | n.c. |
| n.c. | 18 | n.c. |
| n.c. | 19 | n.c. |
| START | 20 | $\overline{\text { READY }}$ |
| n.c. | 21 | n.c. |
| n.c. | 22 | n.c. |
| n.c. | 23 | n.c. |
| 0 V | 24 | n.c. |
| n.c. | 25 | n.c. |
| TR1 | 26 | n.c. |
| n.c. | 27 | n.c. |
| $\mathrm{TR}_{2}$ | 28 | n.c. |
| 0 V | 29 | Vs |
| $\mathrm{TR}_{3}$ | 30 | n.c. |
| 0 V | 31 | Vs |
| 0 V | 32 | n.c. |

n.c. $=$ not connected

[^43]
## BIDIRECTIONAL SERIAL INTERFACE

The VI20 bidirectional serial interface is used in PC20 systems to communicate with TTYs, VDUs, minicomputers and other equipment handling serial data. It has V24/RS232C/RS423 and current-loop inputs and outputs for this purpose. Furthermore, the VI2O can be used to advantage as a satellite processor for handling complex and time-consuming operations thus maintaining rapidity of system response. Its address and data processors are identical to those used in the PC20 central processor modules. Having a 2 k 16 EPROM program memory* and a $1 / 2 \mathrm{k} 4$ data memory it resembles most the CP20 central processor; see Fig. 1. Figure 8 shows the location of the two type 2716 EPROMs (sockets A and B). As with all other I/O modules the VI2O uses photo-isolators between its logic circuitry and the outside world.
For communication with the PC20, the VI2O has a 16 -bit ( $4 \times 4$ bits) control register to exchange control data, and a 128 -bit ( $32 \times 4$ bits) buffer register (part of data memory) to transfer process data. The control register is identified in the PC20 scratchpad memory using the MID ${ }_{2-9}$ code on the back panel: hardware addressing. The buffer register is identified by six bits, $\mathrm{A}_{5-10}$, generated in the PC20 program and accumulated in the control register: software addressing. Utmost flexibility is achieved through free selection of the software addressing code allowing the entire area of a 2 k 4 scratchpad memory to be covered for storing and retrieving the process data.
In contrast to the PC20 system, the VI20 is intermittent in operation. When started by the PC20 it completes one data processing phase (active state) then stops and waits until the next start signal (idle state). During the processing phase the VI2O inputs and outputs are directly accessible.
Basically, there are three PC2O I/O operations (Fig. 2):

- for communication between the PC20 and its process (marked '1' in Fig. 2);
- for communication between the PC20 and the VI20 via the control register (marked ' 2 ');
- for transfer of process data between PC20 scratchpad memory and buffer register (hatched).

Transfer of process data occurs upon request; the Vi20 must be in the idle state to allow this.
The VI20 instruction set is identical to that of the PC20 system. Intermittent operation of the VI20 is clear from the flow chart, Fig. 3. Upon switch-on or reset the CONDITION is set to ' 1 ' level. Also, in the first cycle after switch-on or reset, all 4-bit data memory locations are set to 1001.
The VI20 has been built on an epoxy-glass printed-wiring board of $233,4 \mathrm{~mm} \times 160 \mathrm{~mm}$ (double Eurocard). The board has two F068-I connectors (board parts). The corresponding rack part of connector 1 (Fig. 8) is available on the back panel. That of connector 2 (external connections) is separately available under catalogue number 242202589288 (pins for wire wrapping), 242202589298 (pins for dip-soldering) or 242202589326 (solder tags). **

[^44]

Fig. 1 Block diagram.


Fig. 2 Basic PC2O I/O operations and VI2O states.

The $4 \times 4$-bit control register, Fig. 4, contains four outputs (one-bit places) to and ten inputs (one-bit places) from the PC2O scratchpad memory. Addressing of the control register can only occur on pages 0 and 1 of the CP22 scratchpad (MID 10 internally connected to 0 V ).


Fig. 4 Control Register.
The control register bit functions are:
VIR $\quad$ VIR $=1:$ VI20 in idle state; VIR $=0$ : VI20 in active state.
$\mathrm{Cl}_{0,1,2}$ General-purpose control bits originating in VI20 program.
XX No assignment.
$\mathrm{CO}_{0,1} \quad$ General-purpose control bits originating in PC20 program.
VIS Provided VIR $=1$ (VI2O idle) a positive change of this bit will cause the VI2O to become active and start with line 0000 of its program; VI20 will not become active before the end of the PC2O I/O phase in which the positive transition of VIS has been detected.
$\mathrm{I} / \overline{\mathrm{O}}=0$ : data transfer from scratchpad memory to buffer register;
Fig. 3 Flow chart.

A5-10 program ( $A_{5}=$ least significant bit; $A_{10}=$ most significant bit).

In the table below the occupation of the data memory is specified. Locations 0 to 215 are free for storing data generated in the VI20 program. Locations 216 and 217 form the eight-bit register that can be loaded by the LSTIO instruction only. The highest locations, 224 to 255 , form the buffer register.

The bit-rate generator is used in asynchronous data transmission. It can be adjusted to a variety of bit rates by means of jumpers (S, Fig. 5) on the printed-wiring board; see table below.
Mark/space ratio is $1: 1$ ( $50 \%$ duty factor). Reset to start of LOW phase is done using the 'STRD 221' execute instruction.

Bit-rate selection. Upper jumper position = 1, lower jumper position = 0. Jumper positioning shown in Fig. 5 for 300 bits/s.

Assignment of data memory addresses.

| address | function | bits/s | jumper positions |
| :---: | :---: | :---: | :---: |
| 0 to 215 | no assignment |  |  |
| 216, 217 | read-only eight-bit register | 50 | $\square \square \square \square$ |
| 218.0/.1/.2/.3 | V24 inputs | 75 | - |
| 219.0/. 1 | $\mathrm{CO}_{0}, 1$ control bits | 110 | 므믐 |
| 219.2 | arithmetic overflow | 150 | 믐ㅁ |
| 219.3 | bit-rate generator output | 300 | 믐 |
| 220.0/.1/.2/.3 | V24 outputs | 600 | - |
| 221 | reset bit-rate generator | 1200 | 므믐 |
| 222.0/.1/.2 | $\mathrm{Cl}_{0,1,2}$ control bits | 2400 | 므ㅁㅡㅡㅔ |
| 223 | no assignment | 4800 | 므므ํ |
| 224 to 255 | buffer register | 9600 | ㅁロㅁ |

## ELECTRICAL DATA

## Supply



## Inputs

Data inputs. The data inputs $I_{0}(218.0), I_{1}(218.1), I_{2}(218.2)$ and $I_{3}(218.3)$ are zener-diode protected and meet V 24 standards. The bit level is ' 1 ' when input voltage $\mathrm{V}_{\mathrm{i}} \leqslant-1 \mathrm{~V}$ and ' 0 ' when $\mathrm{V}_{\mathrm{i}} \geqslant+1 \mathrm{~V}$. They are accessible via connector 2 ; see 'Terminal location'. The inputs are commoned through $V_{c}$. Input resistance
Max. permissible input voltage (positive or negative)
$\mathrm{R}_{\mathbf{i}}$
see Fig. 6
$V_{i \max } 30 \mathrm{~V}$

The first input (corresponding to address 218.0) can be made to act as a 20 mA current loop by changing the position of two jumpers (A, Fig. 5) on the printed-wiring board. Current flow is from $C L I_{0}$ to $C L I_{1}$, see Fig. 6 . The bit level is ' 1 ' when input current $l_{i} \leqslant 0,1 \mathrm{~mA}$ and ' 0 ' when $I_{i} \geqslant 10 \mathrm{~mA}$. Max. permissible input current
$l_{i \max } \quad 20 \mathrm{~mA}$

[^45]Individual reset. The VI2O can either be reset via $\overline{\mathrm{RCO}}$ together with the PC 20 system using the $\overline{\mathrm{RCP}}$ input to the central processor or it can be individually reset using input $\overline{\mathrm{RVI}}$ (table below).
Individual reset.

| $\overline{\mathrm{RVI}}$ | voltage | typ current |
| :--- | :--- | :--- |
| active <br> not active | 0 V to +1 V <br> +10 V or floating | $0,5 \mathrm{~mA}$ |



Fig. 5 Vì20 adjustments.


Fig. 6 Circuit diagram for input 218.0; for jumpers A see Fig. 5.

| input | function | termination of connector 1 (Fig. 8) |
| :---: | :---: | :---: |
| $\begin{aligned} & \mathrm{ADD}_{0} \\ & \mathrm{ADD}_{1} \\ & \mathrm{ADD}_{2} \\ & \mathrm{ADD}_{3} \\ & \mathrm{ADD}_{4} \\ & \mathrm{ADD}_{5} \\ & \mathrm{ADD}_{6} \\ & \mathrm{ADD}_{7} \\ & \mathrm{ADD}_{8} \\ & \mathrm{ADD}_{9} \\ & \mathrm{ADD}_{10} \\ & \hline \end{aligned}$ | Address bits from central processor. <br> Control register <br> $A D D_{0-1}$ select a group of four bits in the control register. <br> ADD 2-9 select the control register. <br> Buffer register <br> ADD ${ }_{0-4}$ address both the buffer register and its address field in the scratchpad memory. <br> $A D D_{5-10}$ select the buffer register. | a11 $c 11$ <br> a12 c12 <br> a13 c13 <br> a14 c14 <br> a15 c15 <br>  c16 |
| APF | Handshake signal indicating that address for VI20 is stable. | a26 |
| $\begin{aligned} & \mathrm{DIO}_{0}{ }^{*} \\ & \mathrm{DIO}_{1}^{*} \\ & \mathrm{DIO}_{2}^{*} \\ & \mathrm{DIO}_{3}{ }^{*} \\ & \hline \end{aligned}$ | Data bits from and to central processor. | a21 c21 <br> a22 c22 |
| $\mathrm{MID}_{2}$ <br> $\mathrm{MID}_{3}$ <br> $\mathrm{MID}_{4}$ <br> $\mathrm{MID}_{5}$ <br> $\mathrm{MID}_{6}$ <br> $\mathrm{MID}_{7}$ <br> MID8 <br> MID9 | Control register identification inputs; provide control register with individual identity. | $\begin{aligned} & \mathrm{c} 2 \\ & \mathrm{c} 3 \\ & \mathrm{c} 4 \\ & \mathrm{c5} \\ & \mathrm{c} 6 \\ & \mathrm{c} 7 \\ & \mathrm{c} 8 \\ & \mathrm{c} 9 \end{aligned}$ |
| $\begin{aligned} & \mathrm{PHC}_{0} \\ & \mathrm{PHC}_{1} \\ & \hline \end{aligned}$ | Phase control signals from central processor. | a23 c23 |
| $\overline{\mathrm{RCO}}$ | Reset from central processor during switch-on (active LOW) | c27 |
| 人VII | Individual VI20 reset (active LOW) | a27 |
| SBI | Store command to store data from central processor in control register or buffer register. | c26 |



7289768
Fig. 7 Circuit diagram for output 220.0.

[^46]
## Outputs

Data outputs. The data outputs $\mathrm{O}_{0}(220.0), \mathrm{O}_{1}(220.1), \mathrm{O}_{2}(220.2)$ and $\mathrm{O}_{3}$ (220.3) conform to V 24 standards. The bit level is ' 1 ' when output voltage $\mathrm{V}_{\mathrm{O}}$ is -4 to -6 V and ' 0 ' when $\mathrm{V}_{\mathrm{O}}$ is +4 to +6 V . Access is via connector 2; see 'Terminal location'. All outputs are commoned through $\mathrm{V}_{\mathrm{c}}$.

Min. permissible load resistance
$R_{\text {Lmin }} \quad 450 \Omega$

Output $\mathrm{O}_{0}$ (address 220.0 ) drives 20 mA current-loop outputs $\mathrm{CLO}_{0}$ and $\mathrm{CLO}_{1}$ for two-line and four-line transmission (open collector outputs): see Fig. 7. Current flow is from $\mathrm{CLO}_{0}$ to $\mathrm{V}_{\mathrm{c}}$ (NPN transistor) and from $\mathrm{V}_{\mathrm{c}}$ to $\mathrm{CLO}_{1}$ (PNP transistor) respectively.
Specifications of current-loop outputs $\mathrm{CLO}_{0}$ and $\mathrm{CLO}_{1}$.

| bit level in data <br> memory address <br> 220.0 | NPN transistor <br> between <br> $\mathrm{CLO}_{0}$ and $\mathrm{V}_{\mathrm{c}}$ | PNP transistor <br> between <br> $\mathrm{V}_{\mathrm{c}}$ and $\mathrm{CLO}_{1}$ |
| :--- | :--- | :--- |
| $\prime^{\prime}$ | not conducting <br> conducting | conducting <br> not conducting |

Max. permissible collector current
Collector-emitter voltage
Max. permissible collector-emitter voltage
Collector-emitter leakage current

| $I_{\text {Cmax }}$ | 30 mA |
| :--- | :--- |
| $\mathrm{~V}_{\text {CE }}$ | $\leqslant 0,5 \mathrm{~V}$ at $\mathrm{I}_{\text {Cmax }}$ |
| $\mathrm{V}_{\text {CEmax }}$ | 30 V |
| ${ }^{\text {CEO }}$ | $\leqslant 100 \mu \mathrm{~A}$ at $\mathrm{V}_{\text {CEmax }}$ |

Reference outputs. Reference outputs $\mathrm{V}_{+}$and $\mathrm{V}_{-}$are available ( +12 V and -12 V ) to bias any one of the inputs. These outputs are commoned via $\mathrm{V}_{\mathrm{c}}$.
Minimum permissible load resistance is $1 \mathrm{k} \Omega$ for each output.

| output | function | termination of <br> connector 1 (Fig. 8) |
| :--- | :--- | :--- |
| DEF | Data exchange - scratchpad memory to buffer register - finished <br> (open collector output). | a25 |
| PRF | Preparation of VI20-addressing finished (open collector output). | a24 |
| R $\bar{W}$ | Signal to central processor (active LOW); prepares central <br> processor for data on DIO $0-3$ <br> to be written in scratchpad <br> memory (open collector output). | c24 |

Note: All V24 inputs and outputs as well as $\mathrm{V}_{+}$and $\mathrm{V}_{-}$are commoned to $\mathrm{V}_{\mathrm{c}}$ and floating with respect to $\mathrm{V}_{\mathrm{P}}$ and $\mathrm{V}_{\mathrm{S}}$.

## Software modules

Standard programs are available, which come as software modules, each consisting of two pre-programmed type 2716 EPROMs. These modules have to be ordered separately. The following software modules are available:
PVI1 - message program: provides a framework to assemble messages of any nature; catalogue number 432202799011.
PVI2 - data terminal program: a TTY or VDU with keybaard is used to write data in or read data from the central processor scratchpad memory; catalogue number 432202799021.
PVI4 - communication program A: for communication between a master station and slave stations (VI20 modules); the four-bit data are embedded in seven-bit ASCII characters; catalogue number 432202799041.
PVI5 - communication program B: for communication between a master station and a PC20 system via a VI20 module (slave); eight bits of data are transferred as asynchronous eight-bit characters; catalogue number 432202799051.

PVI7 - communication program C: for communication between a master station and slave stations (VI20 modules); the slave stations can take initiative for communication. The four-bit data are embedded in seven-bit ASCII characters; catalogue number 432202799071.
PVI8 - twelve channel PID controller, to be used in conjunction with analogue input and output modules AD20 and DA20; catalogue number 432202799081.

## MECHANICAL DATA

## Outlines



Fig. 8.
Mass approx. 300 g

Terminal location

| row c | connector 1 |  |  | connector 2 |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | row a |  | row c |  | row a |
| n.c. | 1 | n.c. |  | n.c. | 1 | n.c. |
| $\mathrm{MID}_{2}$ | 2 | HIGH level |  | $V_{c}$ | 2 | ${ }^{1} 0$ |
| $\mathrm{MID}_{3}$ | 3 | HIGH level |  | n.c. | 3 | n.c. |
| $\mathrm{MID}_{4}$ | 4 | HIGH level |  | $\mathrm{V}_{\mathrm{c}}$ | 4 | $\mathrm{I}_{1}$ |
| MID5 | 5 | HIGH level | * | n.c. | 5 | n.c. |
| $\mathrm{MID}_{6}$ | 6 | HIGH level |  | $V_{c}$ | 6 | $\mathrm{I}_{2}$ |
| $\mathrm{MID}_{7}$ | 7 | HIGH level |  | n.c. | 7 | n.c. |
| MID8 | 8 | HIGH level |  | $V_{c}$ | 8 | 13 |
| MID9 | 9 | HIGH level |  | n.c. | 9 | n.c. |
| n.c. | 10 | n.c. |  | $\mathrm{CLI}_{1}$ | 10 | $\mathrm{CLI}_{0}$ |
| $\mathrm{ADD}_{0}$ | 11 | $\mathrm{ADD}_{1}$ |  | n.c. | 11 | n.c. |
| $\mathrm{ADD}_{2}$ | 12 | $\mathrm{ADD}_{3}$ |  | n.c. | 12 | n.c. |
| $\mathrm{ADD}_{4}$ | 13 | $\mathrm{ADD}_{5}$ |  | n.c. | 13 | n.c. |
| $\mathrm{ADD}_{6}$ | 14 | $\mathrm{ADD}_{7}$ |  | $\mathrm{V}_{+}$ | 14 | n.c. |
| $\mathrm{ADD}_{8}$ | 15 | ADD9 |  | n.c. | 15 | n.c. |
| ADD10 | 16 | n.c. |  | $\mathrm{V}_{-}$ | 16 | n.c. |
| n.c. | 17 | n.c. |  | n.c. | 17 | n.c. |
| n.c. | 18 | n.c. |  | $V_{c}$ | 18 | $\mathrm{O}_{0}$ |
| n.c. | 19 | n.c. |  | n.c. | 19 | n.c. |
| n.c. | 20 | n.c. |  | $\mathrm{V}_{\mathrm{c}}$ | 20 | $\mathrm{O}_{1}$ |
| $\mathrm{DIO}_{0}$ | 21 | $\mathrm{DIO}_{1}$ |  | n.c. | 21 | n.c. |
| $\mathrm{DIO}_{2}$ | 22 | $\mathrm{DIO}_{3}$ |  | $\mathrm{V}_{\mathrm{c}}$ | 22 | $\mathrm{O}_{2}$ |
| $\mathrm{PHC}_{0}$ | 23 | $\mathrm{PHC}_{1}$ |  | n.c. | 23 | n.c. |
| R/W | 24 | PRF |  | $V_{c}$ | 24 | $\mathrm{O}_{3}$ |
| 0 V ** | 25 | DEF |  | 0 V | 25 | $V_{S}$ |
| SBI | 26 | APF |  | $\mathrm{V}_{\mathrm{c}}$ | 26 | $\mathrm{CLO}_{0}$ |
| $\overline{\mathrm{RCO}}$ | 27 | $\overline{\mathrm{RVI}}$ |  | 0 V | 27 | $\mathrm{V}_{\mathrm{S}}$ |
| n.c. | 28 | n.c. |  | $\mathrm{V}_{\mathrm{c}}$ | 28 | $\mathrm{CLO}_{1}$ |
| n.c. | 29 | n.c. |  | 0 V | 29 | $V_{S}$ |
| n.c. | 30 | n.c. |  | n.c. | 30 | n.c. |
| Vp | 31 | $V_{P}$ |  | 0 V | 31 | $\mathrm{V}_{\mathrm{S}}$ |
| 0 V | 32 | 0 V |  | n.c. | 32 | n.c. |

* For coding MID lines only.
** No supply line; is used as return line for control signals.


## MICROCONTROLLER

The MC2O is a programmable controller for small systems. It uses the same address and data processors as the PC20 system.
The controller is on one printed-wiring board, and contains the following functions:

- 32 inputs;
- 20 outputs;
- 2k16 EPROM program memory;
- $1 / 2 k 4$ scratchpad memory;
- 8 adjustments for software timers/counters;
- 5 internal clock references;
$-24 \mathrm{~V} / 5 \mathrm{~V}$ d.c.-d.c. converter;
- automatic reset when power switched-on.

The microcontroller is protected by a plastic cover. External connections are made via screw terminals. The controller can be mounted to a panel by means of screws, or to Euro-rails (DIN 46277, Blatt 3) by means of mounting clips (see "Accessories").

## Inputs

The 32 inputs are arranged in 8 groups of 4, each input being galvanically isolated by photo-isolators (Fig. 1). A delay circuit (delay time typ. 1 ms ) is incorporated in each input to increase noise immunity.

Active voltage (' 1 ' level)
Non-active voltage (' 0 ' level)
Input current, active at 24 V

16 to 30 V
0 to 7 V
typ. 10 mA

The input terminals are marked 8.0 to 15.3 , in accordance with their fixed addresses in the scratchpad memory.

## Outputs

The 20 outputs are arranged according to Fig. 2.
Supply voltage, $\mathrm{V}_{\mathrm{S} 2}$
18 to 30 V
Minimum load resistance, $R_{L}$
$120 \Omega$
Maximum output current at 24 V
200 mA
The output terminals are marked 3.0 to 7.3 , in accordance with their fixed addresses in the scratchpad memory.

## NOTE

Since the inputs and outputs have fixed addresses 3 to 15 in the scratchpad memory, the relevant I/O-phase should only be specified within this field (to be programmed as LST1015, END3).


Fig. 2 Configuration of output stages.

Fig. 1 Configuration of input stages.

## Program memory

Two empty EPROMs (2716) are supplied with the MC20 (inside the cover) having a capacity of 2048 instructions. For programming instructions, see "Programming and monitoring".
The programmed EPROMs (A and B) should be inserted into the sockets as shown in Fig. 3.

## Scratchpad memory

The scratchpad memory has a capacity of $1 / 2 k 4$ ( 512 words of 4 bits).
Fixed scratchpad memory addresses are:
0.0 - overflow bit
0.1 - constant ' 1 ' level
0.2 - alarm supply voltage ( $\mathrm{V}_{\mathrm{S} 1}<18 \mathrm{~V}$ )
0.3 - timer clock 10 ms
1.0 - timer clock 100 ms
1.1 - timer clock 1 s
1.2 - timer clock 10 s
1.3 - timer clock 1 ms
3.0 to 7.3 - outputs
8.0 to 15.3 - inputs

240 to 255 - potentiometer settings
No battery back-up is provided for the scratchpad memory.

## Adjustments of software timers

Eight potentiometers ( $\mathrm{P}, \mathrm{Fig} .3$ ) provide adjustment of software timers. The potentiometer setting is converted into a two-decade BCD-value ( 0 to 99 ), and stored in the scratchpad memory at two consecutive addresses when the system is in the UDC-phase. The potentiometer settings are scanned sequentially and each time a conversion is completed and the system is in the UDC-phase the scratchpad memory is updated. The conversion of one potentiometer setting takes a maximum of $0,5 \mathrm{~ms}$.
The results of the conversions are stored at the scratchpad memory addresses 240 to 255; the setting of potentiometer 1 being stored at the two lowest number addresses 240 and 241 (LSD).

## Internal clock periods

The MC20 has 5 crystal-controlled timer clocks, which are accessible at fixed scratchpad memory addresses 0.3 to 1.3.

## 24 V/5 V d.c.-d.c. converter

The logic part of the controller has a supply voltage of 5 V . To allow the controller to be directly operated in a machine control system with a supply of 24 V , the MC 20 has a $24 \mathrm{~V} / 5 \mathrm{~V}$ d.c.-d.c. converter. If the supply voltage to the converter, $\mathrm{V}_{\mathrm{S} 1}(24 \mathrm{~V})$, falls below 18 V the alarm input (scratchpad memory address 0.2 ) becomes ' 1 '.

## Automatic reset

When the supply voltage is switched on, the control system generates an automatic reset. This resets the whole system, including setting all locations in the scratchpad memory to ' 0 '. A system reset also occurs if the supply voltage $\left(\mathrm{V}_{\mathrm{S} 1}\right)$ falls below 16 V .

The system has a pushbutton (R, Fig. 3) for manual reset (cover to be removed).

## System speed

The system execute time depends on the types of instructions used. The execute time of read instructions and all conditional instructions of which the condition is false is $2,5 \mu \mathrm{~s} /$ instruction. For an average program of 1 k instructions the cycle time is typically 3 ms .


Fig. 3 Microcontroller; cover removed.

## Supply

$\left.\begin{array}{l}\text { Supply voltage } \\
\text { Supply current }\end{array}\right\}$ for $24 \mathrm{~V} / 5 \mathrm{~V}$ d.c.-d.c. converter
$\left.\begin{array}{l}\text { Supply voltage } \\
\text { Supply current }\end{array}\right\}$ for output circuitry, exclusive load current

| $\mathrm{V}_{\mathrm{S} 1}$ | $24 \mathrm{~V} \pm 25 \%$ <br> typ. 100 mA |
| :--- | :--- |
| $\mathrm{I}_{\mathrm{S} 1}$ | max. 130 mA |
| $\mathrm{~V}_{\mathrm{S} 2}$ | $24 \mathrm{~V} \pm 25 \%$ |
|  | $\mathrm{I}_{\mathrm{S} 2}$ |
| max. 250 mA |  |



Fig. 4 Connection of supply voltages.

## Programming and monitoring

Programming unit PU20, in conjunction with microcontroller interface MI20, can be used to program and monitor the MC20. The MI20 contains an RI20 module ( 2 k 16 CMOS RAM + interface) and a PU23* module. The MC2O can be connected to the RI20 with a 50 -core flat cable.
The program can also be developed with a PC20-system.
Note that an MC20-program in the EPROMs cannot be monitored when the PU20 is in the EDIT-mode, or in the MONITOR CONT-mode when the UDC-key is operated.


Fig. 5 Programming/monitoring MC20.

[^47]
## MECHANICAL DATA

## Outlines



Fig. 6 The holes marked $(1)$ are for mounting clips MB20, see 'Accessories'.

## ACCESSORIES

For mounting the microcontroller to Euro-rails, snap-on mounting clips MB2O can be supplied;
catalogue number of set of 4 clips: 432202723080.

## ENVIRONMENTAL DATA

Operating temperature range
0 to $+60^{\circ} \mathrm{C}$
Storage temperature range

$$
-40 \text { to }+70^{\circ} \mathrm{C}
$$

## TESTS AND REQUIREMENTS

The MC20 is designed to meet the tests below.
Vibration test
IEC 68-2-6, test method Fc: 10 to 55 Hz , amplitude $0,75 \mathrm{~mm}$ or 5 g (whichever is less).

## Shock test

IEC 68-2-27, test method Ea: 3 shocks in 6 directions, pulse duration 11 ms , peak acceleration 50 g .

## Rapid change of temperature test

IEC 68-2-14, test method $\mathrm{Na}: 5$ cycles of 2 h at $-40^{\circ} \mathrm{C}$ and 2 h at $+85^{\circ} \mathrm{C}$.

## Damp heat test

IEC 68-2-3, test method Ca: 21 days at $40^{\circ}$ C, R.H. 90 to $95 \%$.

## MICROCONTROLLER INTERFACE

This microcontroller interface is used between an MC20 system and the programming unit PU20. Via this interface the PU20 obtains access to the system for programming and monitoring.

The MI20 is a metal housing, containing a RAM/interface unit RI20 and a programming unit interface PU23; the PU23 has to be ordered separately under catalogue number 432202794180 . The RI20 forms an interface between the PU23 and the MC20; it has a 2 k 16 C-MOS RAM program memory for programming the MC20 system.
The metal housing MI20 can be fitted to the MC20 by means of a quick-coupling system. A 50-pole male header F303 at the front of the RI20 provides electrical connection to the MC20 via a 50-core flat cable, which is supplied with the MI20.

The M120 performs two modes of operation for programming and monitoring the MC20 system, which are indicated by LEDs at the front panel of the RI20.
PROM mode (PROM LED is on): for the MC20 system, operating on a program that is stored in its EPROM memory. The MI20 is automatically set to this mode when the system is switched on.
RAM mode (RAM LED in on): for the MC20 system, operating on a program that is stored in the program memory of the RI20. The MI20 is set to this mode by pushing the button at the front of the RI20; the actual setting takes place when the MC20 comes in the UDC phase.


Fig. 1.

In the PROM mode an MC20 program cannot be monitored when the PU20 is in the EDIT mode, or in the MONITOR CONT $n \bullet$ de when the UDC key is operated. In the latter case the END instruction also cannot be monitored.

When the EPROM sockets on the MC20 are empty and a program has to be written into the RAMs of the MI20 the following procedure has to be followed.

- Switch on the PU20, select EDIT mode and line number 0, and push ENTER key.
- Switch on the MC20/MI20 system; the PROM LED on the front plate of the RI20 lights and the PU20 displays 270000.
.-. Push the button on the front plate of the RI20; the RAM LED lights and the system is ready for RAM programming.


## ELECTRICAL DATA

\(\left.$$
\begin{array}{l}\left.\begin{array}{l}\text { Supply voltage } \\
\text { Supply current }\end{array}\right\} \quad \text { from MC20 via flat cable }\end{array}
$$ $$
\begin{array}{ll}V_{P} \\
I_{P}\end{array}
$$ \quad \begin{array}{l}5 \mathrm{~V}+5 \% <br>

typ. 80 \mathrm{~mA}\end{array}\right]\)| min. 7 days, provided the module is |
| :--- |
| in operation for at least 10 h. |

## Input and output data

|  | function | terminations of male header <br> at the front of RI20 |
| :--- | :--- | :--- |

BI-DIRECTIONAL BUSSES

| ADD $_{0}$ |  | 21 |
| :--- | :--- | :--- |
| ADD $_{1}$ |  | 22 |
| ADD $_{2}$ |  | 29 |
| ADD $_{3}$ |  | 30 |
| ADD $_{4}$ | Scratchpad memory address bus. | 31 |
| ADD $_{5}$ |  | 32 |
| ADD $_{6}$ |  | 33 |
| ADD $_{7}$ |  | 20 |
| ADD $_{8}$ |  | 19 |
| ADD $_{9}$ |  | 18 |
| ADD $_{10}$ |  | 34 |
| APM $_{0}$ |  | 36 |
| APM $_{1}$ |  | 37 |
| APM $_{2}$ |  | 38 |
| APM $_{3}$ |  | 39 |
| APM $_{4}$ |  | 40 |
| APM $_{5}$ |  | 41 |
| APM $_{6}$ |  | 42 |
| APM $_{7}$ |  | 43 |
| APM $_{8}$ |  | 44 |
| APM $_{9}$ |  | 45 |
| APM $_{10}$ |  | 46 |


|  | function | terminations of male header <br> at the front of RI20 |
| :--- | :--- | :---: |
| DIO $_{0}$ |  | 9 |
| DIO | Scratchpad memory data bus. | 8 |
| DIO |  | 10 |
| DIO $_{3}$ |  | 11 |
| INS $_{0}$ |  | 14 |
| INS $_{1}$ |  | 13 |
| INS $_{2}$ | Instruction bus | 12 |
| INS $_{3}$ |  | 16 |
| INS $_{4}$ |  | 17 |

INPUTS

| APF | Timing signal from MC20 to PU23 | 1 |
| :--- | :--- | :---: |
| CLOCK | Clock signal to PU23 | 48 |
| CPSI | Signal from PU23 to stop MC20 in UDC phase | 4 |
| PHC $_{0}$ | Phase control outputs from MC20 | 7 |
| PHC $_{1}$ | Reset output from MC20 (active low). | 6 |
| $\overline{\text { RESET }}$ | Output Result Register from MC20. | 23 |
| RR | Clock signal from MC20 to RI20 and PU23. | 35 |
| SBI | 15 |  |

OUTPUTS

| CPDC | Timing pulse to clock data in program <br> memory data latch on MC20 during <br> UDC phase. | 2 |
| :--- | :--- | :---: |
| CPSC | Signal from MC20 to PU23 indicating that <br> MC20 has been stopped. | 50 |
| HOLD | Signal from PU23 to hold MC20. | 5 |
| PDLE | Program memory data latch enable. | 49 |
| WDSM | Signal from PU23 to write data on DIO <br> bus into scratchpad memory. | 47 |



Fig. 2.

Mass: $1,5 \mathrm{~kg}$

## TERMINAL LOCATION

Terminations of male header at the front of R120

| APF | 1 | 2 | CPDC |
| :--- | ---: | ---: | :--- |
| n.c. | 3 | 4 | CPSI |
| HOLD | 5 | 6 | $\mathrm{PHC}_{1}$ |
| $\mathrm{PHC}_{0}$ | 7 | 8 | $\mathrm{DIO}_{1}$ |
| $\mathrm{DIO}_{0}$ | 9 | 10 | $\mathrm{DIO}_{2}$ |
| $\mathrm{DIO}_{3}$ | 11 | 12 | $\mathrm{INS}_{2}$ |
| $\mathrm{INS}_{1}$ | 13 | 14 | $\mathrm{NS}_{0}$ |
| $\mathrm{SBI}^{2}$ | 15 | 16 | $\mathrm{INS}_{3}$ |
| $\mathrm{INS}_{4}$ | 17 | 18 | $\mathrm{ADD}_{9}$ |

$\mathrm{ADD}_{8} 19$
$A D D_{0} 21$
RESET 23
OV 25
$V_{p} \quad 27$
$\mathrm{ADD}_{2} 29$
$\mathrm{ADD}_{4} 31$
$A D D \quad 33$
RR 35
APM $_{1} \quad 37$
$\mathrm{APM}_{3} 39$
APM $_{5} 41$
$\mathrm{APM}_{7} 43$
APM9 45
WDSM 47
PDLE 49
$20 \quad \mathrm{ADD}_{7}$
22 ADD $_{1}$
24 n.c.
26 OV
28 VP
$30 \quad \mathrm{ADD}_{3}$
$32 \quad \mathrm{ADD}_{5}$
34 ADD 10
$36 \quad$ APM 0
$38 \quad \mathrm{APM}_{2}$
$40 \quad$ APM $_{4}$
$42 \quad \mathrm{APM}_{6}$
44 APM8
$46 \quad$ APM $_{10}$
48 CLOCK
50 CPSC
n.c. $=$ not connected.

# PROGRAMMING UNIT 

## DESCRIPTION

This mains-powered programming unit is for loading, checking, dumping and monitoring the control program of the PC20-system. It provides access to the program memory and the scratchpad memory. The programming unit is a desk-top apparatus. The program is written into the program memory via the keyboard (Fig. 1) or other sources e.g. tape readers, cassette recorders, program developing systems. The program is monitored by the display or, for example, by an external VDU.
The programming unit must be used in conjunction with the programming unit interface PU21/PU23 (placed in the PC rack), to which it is connected via an 8-core cable. The circuits of the PU20/2 and the PU21/PU23 are galvanically isolated from each other by means of photo-isolators. The data transport via the data-in and data-out lines is serial.
After loading the program into the program memory, the programming unit can be removed to be used in another PC-system. If necessary, for monitoring purposes for example, it is very easy to connect the PU20/2 to the system again.

The programming unit is provided with two sockets for EPROMs, type 2716 (2k bytes). Programming of the EPROMs is done in such a way that each program word is distributed over two EPROMs, A and $B$ (Fig. 1). EPROM A contains the instruction and the most significant digit of the address and EPROM $B$ contains the remaining digits. The programmed EPRONis can be used in central processor CP20, program memory module MM20 and microcontroller MC20.
The programming unit has the following 10 modes of operation.

1. EDIT: creating a new program or changing an existing program.
2. MONITOR CONT: continuous monitoring the PC20-system in operation; on-line change facilities.
3. MONITOR CYCLE: monitoring the PC20-system, which operates on command for one cycle.
4. MONITOR STEP: monitoring the PC20-system, which executes on command one program line.
5. PROM PROG: dumping the program from the PC20-system into the EPROMs in the sockets of the programming unit.
6. DUMP CASS: dumping the program from the PC 20 -system onto cassette tape.
7. DUMP RS449/423: dumping the program from the PC 20 -system into peripheral equipment with EIA-standard specification RS449/423.
8. LOAD PROM SOCK: loading the program from the EPROMs in the sockets of the programming unit into the PC20-system.
9. LOAD CASS: loading the program from cassette tape into the PC20-system.
10. LOAD RS449/423: loading the program from peripheral equipment with EIA-standard specification RS449/423 into the PC20-system.
A keyswitch is provided. Without the key a user can only monitor system operation and check the states of scratchpad memory locations; a user with a key has full command over all functions.

MECHANICAL DATA
Dimensions
Mass
approx. $6,3 \mathrm{~kg}$

## ENVIRONMENTAL DATA

| Operating temperature range | 0 to $45{ }^{\circ} \mathrm{C}$ |
| :--- | :--- |
| Storage temperature range | -40 to $+70{ }^{\circ} \mathrm{C}$ |

Storage temperature range
-40 to $+70^{\circ} \mathrm{C}$


Fig. 2 Outline dimensions (in mm).

## ELECTRICAL DATA

Mains voltage
Mains frequency
Fusing
for 110 or 127 V mains
for 220 or 240 V mains
Power consumption
$110,127,220$ or 240 V ; tolerance $+10 \%,-15 \%$
46 to 65 Hz

200 mA (delayed action fuse)
100 mA (delayed action fuse)
20 VA

On delivery the programming unit is adjusted to 220 V mains voltage. If the local voltage is different, the switch at the rear must be set to the required position and the fuse must be replaced.

## CONNECTING FACILITIES (see Fig. 4)

- Fixed mains cable (1) with plug with side earth-contact; length $2,4 \mathrm{~m}$.
- Fixed 8-core cable (2) with 9-pole female plug F161, for connection to programming unit interface PU21/PU23; length 2,5 m. For terminal location see Table 1.
- EIA-standard interface connector plug (3), according to RS449/423, for connecting data terminal equipment (DTE), like CRT terminals, punchers, printers, readers. The pins 4, 6, 9, and 19 are operational. For detailed information Table 2 should be consulted.

Note: The programming unit is data communication equipment (DCE).

- DIN-socket (4) for connecting a normal audio cassette recorder (see also Fig. 3). To avoid drop-outs it is recommended that C60 Super Quality Ferrochromium cassette tape be used.
- Two sockets for EPROMs, type 2716 (2k bytes) or 2758 (1k bytes).

Note: At the rear of the programming unit provisions (5) are made for stowage of the mains cable and the 8-core cable during transport.


Fig. 3 DIN audio socket.


Fig. 4 Rear view.
Table 1 Terminal location of connecting cable to PU21/PU23

| terminal | function |
| :--- | :--- |
| 1. | connected to terminal 6 |
| 2. $\overline{\text { CLDT }}$ | clock signal for data transfer between PU20/2 and PU21/PU23 |
| 3. $\overline{\text { TRANSFER }}$ | data transfer required by PU20/2 |
| 4. $\overline{\text { SSE }}$ | system stop enable |
| 5. | $+5 \mathrm{~V}^{*}$ |
| 6. | connected to terminal 1 |
| 7. $\overline{\text { DPI }}$ | data from PU20/2 to PU21/PU23 |
| 8. DIP | data from PU21/PU23 to PU20/2 |
| 9. READY | ready signal to PU20/2, indicating that PU21/PU23 is available for data transfer |

[^48]Table 2 Terminal location of RS449/423 plug

| terminal | function | operational | dummy <br> ON | dumm <br> OFF | jumper <br> 1 | jumper <br> 2 |
| :---: | :--- | :---: | :---: | :---: | :---: | :---: |
| 2 | SI - signalling route indicator |  | X |  |  |  |
| 4 | SD - send data | X |  |  |  |  |
| 6 | RD - receive data | X |  |  |  |  |
| 9 | CS - clear to send | $\mathrm{X}^{*}$ |  |  |  | $\mathrm{X}^{* *}$ |
| 11 | DM - data mode |  |  |  |  | X |
| 12 | TR - terminal ready |  |  |  |  | X |
| 13 | RR - receiver ready |  |  |  |  | X |
| 15 | IC - incoming call |  |  | X |  |  |
| 18 | TM - test mode |  |  | X |  |  |
| 19 | SG - signal ground | X |  |  | X |  |
| 20 | RC - receive common |  |  |  | X |  |
| 33 | SQ - signal quality |  | X |  |  |  |
| 36 | SB - stand-by indicator |  |  | X |  |  |
| 37 | SC - send common |  |  |  | X |  |

* Not applicable to the former type PU2O.
** Only applicable to the former type PU20.
The PU20/2 has an input (pin 9 of connector plug (3), Fig. 4) which enables interruption of the data transfer from the PU20/2 to peripheral equipment with RS449/423 or RS232 input specification. When this input goes to the 'OFF' condition ( -5 V ) the data transfer is stopped. When this input goes to the ' ON ' condition ( +5 V ) or is left floating, the data transfer is started again.
(a)


Fig. 5 Time relation between data stream (a) and stop signal (b); $\mathrm{t}_{\mathrm{d}}=\min .0 ;$ max. $\frac{2}{\text { bit rate }} \mathrm{s}$.

## PROGRAMMING UNIT INTERFACES

## DESCRIPTION

The programming unit interface can be used between a PC2O-system or MC2O-system (in conjunction with microcontroller interface MI2O) and the programming unit PU20/2 which obtains access to the system via this interface*. The programming unit interface does not form an essentail part of an operating system which can function normally without it.
Figure 1 is a block diagram of the programming unit interface which has direct access to the data, address and control lines of the PC20/MC20-system. Furthermore it is connected to the PU20/2 via an 8 -core cable, which contains a data-in, transfer, clock, ready, system stop enable and a common line. These lines are galvanically isolated from the PU21/PU23 circuitry by photo-isolators. The data transport via the data-in and data-out lines is serial. All actions to be executed are commanded by the PU20/2 through a 4-bit function mode code. This code is transmitted, with the other data to the programming unit interface, in both normal and inverted form so that correct reception can be verified.
The circuit is built on an epoxy-glass printed-wiring board of $233,4 \mathrm{~mm} \times 160 \mathrm{~mm}$ (double Euro-card**). The board has two F068-I connectors (male parts); the corresponding female parts are on the back panels. At the front of the unit a 9-pole male connector F161 allows connection of the cable from the programming unit.

* The PU21 can only be used with a PC20-system.
** For a general description of the Euro-card system see IEC 297 or DIN41494 for 19-in racks and IEC 130-14 or DIN41612 for connectors.


Fig. 1 Simplified block diagram.

## ELECTRICAL DATA

## Supply

Supply voltage (d.c.) current

|  | PU21 | PU23 |
| :--- | :--- | :--- |
| $V_{p}$ <br> $I_{p}$ | Pax. 20 mA | 5 or $10 \mathrm{~V} \pm 10 \%$ <br> $\max .20 \mathrm{~mA}$ |

## Input and output data

All inputs and outputs meet the standard LOCMOS specifications.

|  | function | terminations (Fig. 2) |  |
| :---: | :---: | :---: | :---: |
|  |  | connector 1 | connector 2 |
| BI-DIRECTIONAL DATA BUSSES |  |  |  |
| APM0 <br> APM 1 <br> APM 2 <br> APM 3 <br> APM 4 <br> APM 5 <br> APM 6 <br> APM 7 <br> APM8 <br> APM9 <br> APM ${ }_{10}$ <br> APM 11 <br> APM 12 | Program memory address bus; APM $_{0-12}$ act as outputs when PABE is LOW (only during UDC-phase). |  | a16, c16 <br> a17, c17 <br> a18, c18 <br> a19, c19 <br> a20, c20 <br> a21, c21 <br> a22, c22 <br> a23, c23 <br> a24, c24 <br> a25, c25 <br> a26, c26 <br> a27, c27 <br> a28, c28 |
| $\mathrm{DIO}_{0}$ <br> $\mathrm{DIO}_{1}$ <br> $\mathrm{DIO}_{2}$ <br> $\mathrm{DiO}_{3}$ | Data to or from scratchpad memory, controlled by WEPC. | a19, c19 <br> a20, c20 <br> a21, c21 <br> a22, c22 |  |


| INPUTS |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| $\mathrm{ADD}_{0}$ | Program memory data bits from central processor (address bus). | a6 |  |  |
| $\mathrm{ADD}_{1}$ |  | a7 |  |  |
| $\mathrm{ADD}_{2}$ |  | a8 |  |  |
| $\mathrm{ADD}_{3}$ |  | a9 |  |  |
| $\mathrm{ADD}_{4}$ |  | a10 |  |  |
| $\mathrm{ADD}_{5}$ |  | a11 |  |  |
| $\mathrm{ADD}_{6}$ |  | a12 |  |  |
| $\mathrm{ADD}_{7}$ |  | a13 |  |  |
| $\mathrm{ADD}_{8}$ |  | a14 |  |  |
| ADD9 |  | a15 |  |  |
| ADD10 |  | a16 |  |  |
| CLOCK | Clock input from central processor for timing purposes. |  | a7, | c7 |
| CPSC | Input that indicates that the central processor has been stopped (HIGH) in the UDC-phase. |  | a5, | c5 |
| $\mathrm{INS}_{0}$ |  | a1 |  |  |
| $\mathrm{INS}_{1}$ |  | a2 |  |  |
| $!\mathrm{NS}_{2}$ | processor (instruction bus). | a3 |  |  |
| $\mathrm{INS}_{3}$ |  | a4 |  |  |
| $\mathrm{INS}_{4}$ |  | a5 |  |  |



OUTPUTS


[^49]|  | function | terminations (Fig. 2) |  |
| :--- | :--- | :--- | :--- |
|  |  | connector 1 | connector 2 |
| R/WPM | Write signal to CP21/CP24, M21/M22 or RI20* <br> to store data in program memory (active HIGH). |  | a14, c14 |
| WEPC | Write enable signal to central processor; <br> prepares central processor to store data <br> on DIO <br> LOW, in scratchpad memory (active | c28 |  |
| WPSM during UDC-phase). |  |  |  |

Connection to programming unit PU20

| line | function | terminations (Fig. 2) <br> connector 3 |
| :--- | :--- | :---: |
| $\overline{\text { CLDT }}$ | clock signal for data transfer between PU20/2 <br> and PU21/PU23. | 2 |
| DIP | data from PU21/PU23 to PU20/2. | 8 |
| $\overline{\text { DPI }}$ | data from PU20/2 to PU21/PU23. | 7 |
| READY | ready signal to PU20/2, indicating that PU21/PU23 <br> is available for data transfer. | 9 |
| $\overline{\text { SSE }}$ | system stop enable. | 4 |
| $\overline{\text { TRANSFER }}$ | data transfer required by PU20/2. | 3 |

[^50]
## MECHANICAL DATA

## Outlines



Fig. 2.
Mass approx. 270 g

| row c | connector 1 |  | connector 2 |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | row a | row c |  | row a |
| INSS $_{0}$ | 1 | $\mathrm{INS}_{0}$ | PABE | 1 | PABE |
| $\mathrm{INSS}_{1}$ | 2 | INS ${ }_{1}$ | PDBE | 2 | PDBE |
| $\mathrm{INSS}_{2}$ | 3 | $\mathrm{INS}_{2}$ | CPSD | 3 | CPSD |
| $\mathrm{INSS}_{3}$ | 4 | $\mathrm{INS}_{3}$ | CPSI | 4 | CPSI |
| $\mathrm{INSS}_{4}$ | 5 | $\mathrm{INS}_{4}$ | CPSC | 5 | CPSC |
| $\mathrm{ADDS}_{0}$ | 6 | $\mathrm{ADD}_{0}$ | $\overline{\text { HOLD }}$ | 6 | HOLD |
| $\mathrm{ADDS}_{1}$ | 7 | $\mathrm{ADD}_{1}$ | CLOCK | 7 | CLOCK |
| $\mathrm{ADDS}_{2}$ | 8 | $\mathrm{ADD}_{2}$ | n.c. | 8 | n.c. |
| $\mathrm{ADDS}_{3}$ | 9 | $\mathrm{ADD}_{3}$ | n.c. | 9 | n.c. |
| $\mathrm{ADDS}_{4}$ | 10 | $\mathrm{ADD}_{4}$ | n.c. | 10 | n.c. |
| $\mathrm{ADDS}_{5}$ | 11 | $\mathrm{ADD}_{5}$ | n.c. | 11 | n.c. |
| $\mathrm{ADDS}_{6}$ | 12 | $\mathrm{ADD}_{6}$ | n.c. | 12 | n.c. |
| $\mathrm{ADDS}_{7}$ | 13 | $\mathrm{ADD}_{7}$ | WPSM | 13 | WPSM |
| $\mathrm{ADDS}_{8}$ | 14 | $\mathrm{ADD}_{8}$ | $\bar{R} /$ WPM | 14 | $\bar{R} / W P M$ |
| ADDS9 | 15 | ADD9 | n.c. | 15 | n.c. |
| ADDS $_{10}$ | 16 | ADD 10 | $\mathrm{APM}_{0}$ | 16 | $\mathrm{APM}_{0}$ |
| $\mathrm{PB}_{1}$ | 17 | $\mathrm{PB}_{0}$ | APM ${ }_{1}$ | 17 | APM $_{1}$ |
| RR | 18 | RR | APM 2 | 18 | APM ${ }_{2}$ |
| $\mathrm{DIO}_{0}$ | 19 | $\mathrm{DIO}_{0}$ | APM 3 | 19 | APM3 |
| $\mathrm{DIO}_{1}$ | 20 | $\mathrm{DIO}_{1}$ | $\mathrm{APM}_{4}$ | 20 | $\mathrm{APM}_{4}$ |
| $\mathrm{DIO}_{2}$ | 21 | $\mathrm{DIO}_{2}$ | APM ${ }_{5}$ | 21 | APM ${ }_{5}$ |
| $\mathrm{DIO}_{3}$ | 22 | $\mathrm{DIO}_{3}$ | $\mathrm{APM}_{6}$ | 22 | $\mathrm{APM}_{6}$ |
| $\mathrm{PHC}_{0}$ | 23 | $\mathrm{PHC}_{1}$ | $\mathrm{APM}_{7}$ | 23 | $\mathrm{APM}_{7}$ |
| n.c. | 24 | n.c. | APM8 | 24 | APM8 |
| n.c. | 25 | n.c. | APM9 | 25 | APM9 |
| SBI | 26 | n.c. | APM ${ }_{10}$ | 26 | APM 10 |
| n.c. | 27 | n.c. | APM 11 | 27 | APM 11 |
| WEPC | 28 | n.c. | APM 12 | 28 | APM ${ }_{12}$ |
| n.c. | 29 | n.c. | n.c. | 29 | n.c. |
| n.c. | 30 | n.c. | n.c. | 30 | n.c. |
| $V_{p}$ | 31 | $V_{p}$ | $\mathrm{V}_{\mathrm{p}}$ | 31 | $V_{p}$ |
| 0 V | 32 | 0 V | 0 V | 32 | 0 V |

Connector 3 (front panel)
1
2
3
4
$5-5$
6

7

> | $\frac{\text { i.c. }}{\text { CLDT }}$ |
| :--- |
| $\frac{\text { TRANSFER }}{\text { SSE }}$ |
| $+5 V^{*}$ |
| $\frac{\text { i.c. }}{\overline{D P I}}$ |

8 DIP
9 READY
n.c. $=$ not connected
i.c. $=$ internal connected

* No supply line; is used as a common line for the control signals.


## BACK PANELS

## APPLICATION

These back panels are for use in 19 inch racks, to accommodate the modules of the PC20 system. Use of these panels eliminates the need to wire separate connectors to receive the modules.

## DESCRIPTION

The back panels incorporate female connectors which mate with the male counterparts of the PC20 modules. Type BP23 consists of two back panels. The upper panel (BP23A) provides the required interconnections for connector 1 of a PU21/PU23, MM module, CP module and of eighteen input/ output modules. It has solder pads for allocation of the addresses of the input/output modules. The lower panel (BP23B) provides the interconnections for connector 2 of a PU21/PU23, MM module and CP module. External connections to the lower connectors of the input/output modules must be made individually; for this purpose connecting cables are available, see Table 1. Back panels BP25 and BP26 are used in extension racks to accommodate additional input/output modules. Type BP25 is for 15 input/output modules, type BP26 for 21 . These types, of course, are only upper back panels.
The back panels carry a four-terminal block for external connection of the 10 V supply. Interconnection between the panels can be made via a ribbon cable (see Table 2); for this purpose, the panels incorporate an F303 male header.
The back panels are fixed to the rack with M2,5 $\times 10$ screws, using threaded rails and isolation strips.
Table 1 Connecting cables

| type | description | catalogue number |
| :--- | :--- | :--- |
| CC20 | connecting cable for module OM21 | 939029350000 |
| CC21 | connecting cable for module SO20 | 939029360000 |
| CC22 | connecting cable for module IM20 | 939029370000 |
| CC23 | connecting cable for modules IM20 and OM20 | 939029380000 |

Table 2 Bus extension cables (see also Fig. 5)

| type | description | catalogue number |
| :--- | :--- | :--- |
| BI21 | bus extension cable for one I/O extension rack | 432202737910 |
| BI22 | bus extension cable with bus interface for two I/O extension racks | 432202737920 |
| BI23 | bus extension cable with bus interface for three I/O extension racks | 432202737930 |

Fig. 1 Back panels BP23A (upper) and BP23B (lower), seen from rear of rack.
CP = central processor
$\mathrm{MM}=$ memory module;
PU = programming unit interface (PU21/PU23).
For terminal location of the male header, see last page of this data sheet.




## Connection of control signals and external battery

Control signals can be connected to the connecting points on the rear side of the back panels (see
Figs 1, 2 and 3. The functions of the control signals are indicated in the table below.
RCP and RSME signals are only applicable to panel BP23A.

| connecting <br> points | function |
| :--- | :--- |
| $\overline{\overline{L D D}}$ | Indication LED disable; input current low: $0,1 \mathrm{~mA}$. |
| $\overline{\mathrm{REO}}$ | Reset output module input; a low level on this input will reset all output latches <br> (output transistor non-conducting); input current low: $0,1 \mathrm{~mA}$. |
| $\overline{\mathrm{OSD}}$ | Output stage disable for all stages; input current low: 10 mA. |
| $\overline{\mathrm{RCP}}$ | Reset central processor; resets data processor, address processor, UDC circuitry, <br> RSM circuitry and timer clocks. Active low: input current $=2 \mathrm{~mA}$. |
| RSME | Reset scratchpad memory enable. When high or floating a reset of the scratchpad <br> memory will occur during the first RSM-phase after switching on. When low (input <br> current is 2 mA ) the RSM-phase is only effective for the scratchpad memory <br> addresses 0 to 2 inclusive. |
| VB | External battery connection for saving the contents of the program memory and/or <br> the scratchpad memory, in case of power failure. If central processor CP21/CP24 or <br> memory module MM21/MM22 is used, this battery is parallel to the on-board battery <br> and the retention time is lengthened. |

## Allocation of addresses of input/output modules

Each group of four inputs and outputs of an input/output module has a discrete address in the scratchpad memory of the central processor. This address is allocated by bridging the appropriate MID-pads ( MID $_{1}$ to MID 10 ) on the back panels.

## Separation of inputs and outputs of modules RP20 and RS20

Inputs and outputs are separated by bridging the appropriate SCIO -pads ( $\mathrm{SClO}_{0}$ to $\mathrm{SClO}_{3}$ ) on the back panels.

## Connection for logic supply voltage

The logic voltage $\left(V_{p}\right)$ is $10 \mathrm{~V} \pm 10 \%$. It can be connected to the four-terminal connecting block on the back panels. This connection is only applicable if there is no SO20 module provided.

Note: For full information see PC20 user manual.

Terminal location of F303 male header


Fig. 4 Male header, seen from rear of rack.


Fig. 5 Bus extension cables for I/O extension racks.


BI 21


BI22
BI23
7285949

## SMALL CONTROLLER CABINET

## APPLICATION

This cabinet is designed for accommodating PC20 modules, for easy assembling of small controller systems.

## DESCRIPTION

This metal cabinet houses a programming unit interface PU21/PU23, a central processor CP20 or CP21/CP24, a supply and output module SO20 and six input/output modules.
The cabinet has back panels, so the work of wiring separate connectors to receive the male connectors of the modules is eliminated.
The upper panel BP20 provides the required interconnections for connector 1 of a PU21/PU23, CP20 or CP21/CP24 and an SO20 module, and of six input/output modules. It has solder bridges for allocating the addresses of the input/output modules.

The lower panel BP21 provides the interconnections for connector 2 of a PU21/PU23, CP20 or CP21/ CP24 and an SO20 module; type BP22 provides for connector 2 of an input/output module, type BP27 provides for connector 2 of output module OM22 or input module IM22. These panels have connecting blocks with screw terminals for connection of supply voltages and input and output circuits. Furthermore, panel BP21 has connecting points for the control signals.
The cabinet is supplied with one panel BP22 but space is provided for another five BP22 or BP27 panels, which must be ordered separately.
The connections to the outside world are protected by the sloping cover on the lower part of the cabinet. Openings in the underside provide entry of the input/output cables. The cabinet is intended for wall mounting.

Note: For larger controller systems, back panels BP23, BP25 and BP26 are available, to be used in 19 inch racks; see the relevant data sheet.

MECHANICAL DATA

## Outlines



Dimensions in mm

Fig. 1 Small controller cabinet.

| Cabinet, material <br> colour | steel <br> black |
| :--- | :--- |
| Mass | $5,2 \mathrm{~kg}$ |

## ENVIRONMENTAL DATA

Maximum permissible temperature, measured 5 cm above the cabinet

## MOUNTING OF THE CABINET

Four mounting brackets can be fitted to the cabinet (Fig. 1). They are supplied with bolts and washers with the cabinet.
The cabinet can be fixed to a wall with M6 bolts. In some cases, e.g. if the wall is not flat, it is sufficient to use three mounting brackets (one at the top and two at the bottom of the cabinet).
The cabinet must be positioned so that air has free access.

## MOUNTING OF ADDITIONAL BACK PANELS BP22 AND BP27

The back panel BP22 or BP27 has to be positioned through the openings in the bottom of the cabinet, to avoid bending of the panel. It is fitted to the mounting strip in the cabinet by means of the four M2,5 $\times 10$ screws, which are supplied with the cabinet. Two of these screws also secure the female connector. Before tightening the screws, the panel has to be aligned. To this end an input/output module has to be slid carefully into the cabinet, so that its connectors are fully mated with their counterparts on the back panel. The lower two screws can then be tightened and, after removing the module, the fixing screws of the connector can be tightened.
Catalogue number of back panel BP22: 432202792140.
Catalogue number of back panel BP27: 432202793950.

## ACCESSORIES

To give sufficient space for connection of the input/output cables to the connecting blocks on back panels BP22 and BP27, the various input/output modules in the cabinet are 15 mm apart. To cover these spaces front plates FP20 are available.
Unused module spaces, can be covered with a front plate FP21.
Catalogue number of front plate FP20 ( 15 mm width): 432202792150.
Catalogue number of front plate FP21 ( 20 mm width): 432202792160.

## INSTALLATION

## Connection of control signals and external battery

Control signals can be connected to the connecting points on the lower end of back panel BP21
(see Fig. 2). The functions of the control signals are indicated in the table below.
Note: Use of control signals $\overline{\mathrm{ILD}}, \overline{\mathrm{REO}}$ and $\overline{\mathrm{OSD}}$ requires interconnections between back panels BP2O and BP21 (see Fig. 2).

| connecting points | function |
| :---: | :---: |
| $\overline{\text { ILD }}$ | Indication LED disable; input current low: 0,1 mA. |
| $\overline{\mathrm{REO}}$ | Reset output module input; a low level on this input will reset all output latches (output transistor non-conducting); input current low: 10 mA . |
| $\overline{\text { OSD }}$ | Output stage disable for all stages; input current low: 10 mA . |
| RCP | Reset central processor; resets data processor, address processor, UDC circuitry, RSM circuitry and timer clocks. Active low: input current $=2 \mathrm{~mA}$. |
| RSME | Reset scratchpad memory enable. When high or floating a reset of the scratchpad memory will occur during the first RSM-phase after switching on. When low (input current $=2 \mathrm{~mA}$ ) the RSM-phase is only effective for the scratchpad memory addresses 0 to 2 inclusive. |
| $\pm$ BATT | External battery connection for saving the contents of the program/scratchpad memories, in case of power failure. If central processor CP21/CP24 is used, this battery is parallel to the on-board battery and the retention time is lengthened. |
| ALE | Alarm external; active low as long as $\mathrm{V}_{\text {ic }}$ is above $17,5 \mathrm{~V}$; with photo-isolator between internal and external supply. |



Fig. 2 Back panel arrangement. See also note at the top of the next page.

Note to Fig. 2 on the preceding page: If all outputs of the OM22 are used in grounded load configuration, an interconnection between the two connecting points of the small connecting block of back panel BP27 has to be used (indicated with a dashed line). This interconnection has not to be made if the first 16 output stages of the OM22 are used with pull-down resistors, e.g. to drive TTL circuitry. See also data sheet OM22.

## Allocation of addresses of input/output modules

Each group of four inputs and outputs of an input/output module has a discrete address in the scratchpad memory of the central processor. This address is allocated by bridging the appropriate MID-pads ( MID $_{1}$ to MID $_{10}$ ) on back panel BP20, see Fig. 2.

## Coding of inputs and outputs on modules RP20 and RS20

The coding of inputs and outputs is done by bridging the appropriate SClO -pads ( $\mathrm{SClO}_{0}$ to $\mathrm{SClO}_{3}$ ) on back panel BP20, see Fig. 2.

## Connection of input and output circuits

The input circuits of the input modules and the output circuits of the output modules should be connected to the large connecting blocks on back panel(s) BP22, with the exception of the modules IM22, OM22, SO20:

- the input circuits of IM22 and output circuits of OM22 to be connected to the large connecting blocks on back panel(s) BP27,
- the output circuits of SO20 to be connected to the large connecting block on back panel BP21, see Fig. 2.


## Connection of supply voltage for $24 \mathrm{~V} / 10 \mathrm{~V}$ d.c.-d.c. converter of module SO2O

The supply voltage for the converter $\left(\mathrm{V}_{\mathrm{ic}}\right)$ is $24 \mathrm{~V} \pm 25 \%$. It should be connected to the terminals of the small connecting block on back panel BP21, see Fig. 2. A fuse ( $I_{\mathrm{n}}=1,6 \mathrm{~A}$, delayed action) protects the supply against short-circuit in the converter.

## Connection of supply voltage for output modules

The supply voltage for the output modules ( $\mathrm{V}_{\mathrm{S}}$ ) is $24 \mathrm{~V} \pm 25 \%$. It should be connected to the double connecting block on back panel BP21 and the small connecting block on the panel(s) BP22 and BP27 (only + connection), see Fig. 2.

Note: For full information see PC20 Manual.

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[^0]:    * Obsolescent type.

[^1]:    ${ }^{1}$ ) Only present in the CP10.

[^2]:    ${ }^{1}$ ) For a general description of the Euro-card system see IEC 297 or DIN 41494 for 19-in racks and IEC 130-14 or DIN 41612 for connectors.

[^3]:    ${ }^{1}$ ) No supply line; only to be used as a ground connection for CLCO.

[^4]:    * For a general description of the Euro-card system see IEC 297 or DIN 41494 for 19-in racks and IEC 130-14 or DIN 41612 for connectors.

[^5]:    * Voltage between terminal of row a and terminal of row cof connector 2.

[^6]:     in racks and IEC 130-14 or DIN 41612 for connectors.

[^7]:    * The connections between these modules have to be done in a separate module set-up, outside the system. No special programming apparatus is required.

[^8]:    Mass
    350 g

[^9]:    * Corresponding output number of EPROM.

[^10]:    Mass
    290 g

[^11]:    * Corresponding output number of EPROM.

[^12]:    1) For a general description of the Euro-card system see IEC297 or DIN41494 for 19-in racks and IEC 130-14 or DIN41612 for connectors.
[^13]:    ${ }^{1}$ ) No supply line; only to be used for coding of the $\overline{\mathrm{MID}}_{0-4}$ lines.
    ${ }^{2}$ ) No supply line; only to be used as a ground connection for CLCO.

[^14]:    * Input with relatively high input resistance (typical $40 \mathrm{k} \Omega$ ). CLCO-input: LOW level, maximum 1 V ; HIGH level, minimum $2,4 \mathrm{~V}$.

[^15]:    * Voltage between terminal of row a and terminal of row c of connector 2.

[^16]:    Mass
    260 g

[^17]:    * When points " $c$ " and " $d$ " on the PC board are not interconnected (see Fig. 5), the module supplies an even parity. With a short-circuit bridge across these points an odd parity occurs.

[^18]:    1) For a general description of the Euro-card system see IEC 297 or DIN 41494 for 19 -in racks and IEC 130-14 or DIN 41612 for connectors.
[^19]:    * A maximum of 4 LX modules can be inserted at positions IM/OM1 to IM/OM4. If an extension rack is used, one place in each rack must be reserved for data bus cable, thus the number of modules is one less than the number stated in this column.
    ** Back panels type BP15 and BP16 are extension panels for use in a second rack to accommodate additional IM/OM modules.

[^20]:    * X indicates either 0 or 1 .

[^21]:    * Except programming unit PU20, which is a desk-top apparatus.
    ** Different from standard Eurocards.

[^22]:    * Under development.
    ** Obsolescent type.

[^23]:    * Under development.

[^24]:    * For a general description of the Euro-card system see IEC 297 or DIN 41494 for 19-in racks and IEC 130-14 or DIN 41612 for connectors.

[^25]:    * No supply line; is used as return line for control signals.

[^26]:    * No supply line; is used as return line for control signals.

[^27]:    Mass $\quad 250 \mathrm{~g}$

[^28]:    * 1 if SCIO pads on back panel are bridged;

    0 if SCIO pads on back panel are not bridged.

[^29]:    * For a general description of the Eurocard system see IEC 297 or DIN 41494 for 19-in racks and IEC 130-14 or DIN 41612 for connectors.

[^30]:    * For a general description of the Euro-card system see IEC 127 or DIN 41494 for 19-in racks and IEC 130-14 or DIN 41612 for connectors.

[^31]:    * No supply line; is used as return line for control signals.

[^32]:    * For a general description of the Eurocard system see IEC 297 or DIN 41494 for 19-in racks and IEC 130-14 or DIN 41612 for connectors.
    ** If $\mathrm{V}_{\mathrm{S}}$ drops below 16 V , all output stages are forced into the non-conducting state for protection of the output circuitry.

[^33]:    * Voltage between terminal of row a and terminal of row cof connector 2.

[^34]:    Mass
    230 g

[^35]:    * No supply line; is used as return line for control signals.
    ** For coding MID lines.

[^36]:    * For a general description of the Eurocard system see IEC 297 or DIN 41494 for 19-in racks and IEC 130-14 or DIN 41612 for connectors.

[^37]:    * For a general description of the Eurocard system see IEC 297 or DIN 41494 for 19-in racks and IEC 130-14 or DIN 41612 for connectors.
    ** If $\mathrm{V}_{\mathrm{S}}$ drops below 16 V , all output stages are forced into the non-conducting state for protection of the output circuitry.

[^38]:    * Voltage between terminal of row a and terminal of row c of connector 2.
    ** If two or more modules are connected in parallel the output current per module is max. 1,5 A.

[^39]:    * For a general description of the Eurocard system see IEC 297 or DIN 41494 for 19-in racks and IEC 130-14 or DIN 41612 for connectors.

[^40]:    * For a general description of the Euro-card system see IEC 297 or DIN 41494 for 19-in racks and IEC 130-14 or DIN 41612 for connectors.

[^41]:    * $\mathrm{V}_{\mathrm{S}}=24 \mathrm{~V}$ : points A (Fig. 5) not bridged;
    $\mathrm{V}_{\mathrm{S}}=5 \mathrm{~V}$ : points A to be bridged with a jumper.

[^42]:    * Bidirectional busses for the external data line.
    ** Trade name of NKF (Nederlandse Kabel Fabrieken).

[^43]:    * No supply line; is used as return line for control signals.

[^44]:    * Standard programs are available, see paragraph "Software modules".
    ** For a general description of the Eurocard system see IEC 297 or DIN 41494 for 19-inch racks and IEC 130-14 or DIN 41612 for connectors.

[^45]:    * Used to supply V24 interface circuitry.

[^46]:    * Either input or output.

[^47]:    * To be ordered separately.

[^48]:    * No supply line; is used as a common line for the control signals.

[^49]:    * Not for PU21.

[^50]:    * Not for PU21.

