1.0 Introduction

The 82C602A is the newest generation of OPTi's 82C602 Buffer Device. This enhanced version of the 82C602 has numerous modes which enable the system designer to reduce the amount of required TTL logic and increase the performance of their systems.

This document is supplemental information and must be used with the existing 82C601/82C602 Data Book (Document No. 912-3000-025, Revision 1.0, November 1994). This document lists information on the various modes and OPTi chipsets that the 82C602A is capable of working in/with. All changes and additions to the 82C602 will be listed in this document. It is therefore implied that all changes not discussed in this document and are present in the current 82C602, retain their functionality as outlined in the existing 82C601/82C602 Data Book.

2.0 Modes/Chipset Support

The 82C602A must follow the strapping table below. The 82C602A will sense the XD[7:0] bits during reset to determine which mode it will enter. In order to achieve a '0' value during reset, the system designer needs to place a 2.2K ohm pull-down resistor on the appropriate XD lines. In order to achieve a '1' value, no external pull-up resistors are needed since the 82C602A contains internal pull-up resistors on the XD[7:0] bus.

In the Viper NBB Mode, the XD bus does not exist, but the straps are sampled on BSA[7:0] pins.

The 82C602A is available by default in a 100-pin PQFP (plastic quad flat pack). It is also available in a 100-pin TQFP (thin quad flat pack) by special order for all notebook modes.

Table 2-1 82C602A Mode Strap Options

XD7 (Pin 97)	XD6 (Pin 96)	XD5 (Pin 95)	XD4 (Pin 94)	XD3 (Pin 93)	XD2 (Pin 92)	XD1 (Pin 89)	XD0 (Pin 88)	Mode/Chipset Supported
0	1	1	0	1	1	1	1	802G Mode / 82C802G
1	0	1	0	1	1	1	1	Blackhawk / 82C802GP & 82C832
1	1	1	0	1	1	0	1	486 Notebook Mode / 82C465MV
0	0	1	0	1	1	1	1	Viper Desktop Mode A (VDTA) / 82C556/557/558
0	0	0	0	1	1	1	1	Viper Desktop Mode B (VDTB) / 82C556/557/558
1	1	1	0	1	1	1	0	Viper Notebook Mode A (VNBA) / 82C556/557/558N
1	1	0	0	1	1	1	0	Viper Notebook Mode B (VNBB) / 82C556/557/558N

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3.0 Signal Definitions

Figure 3-1 802G Mode Pin Diagram (100-Pin PQFP)

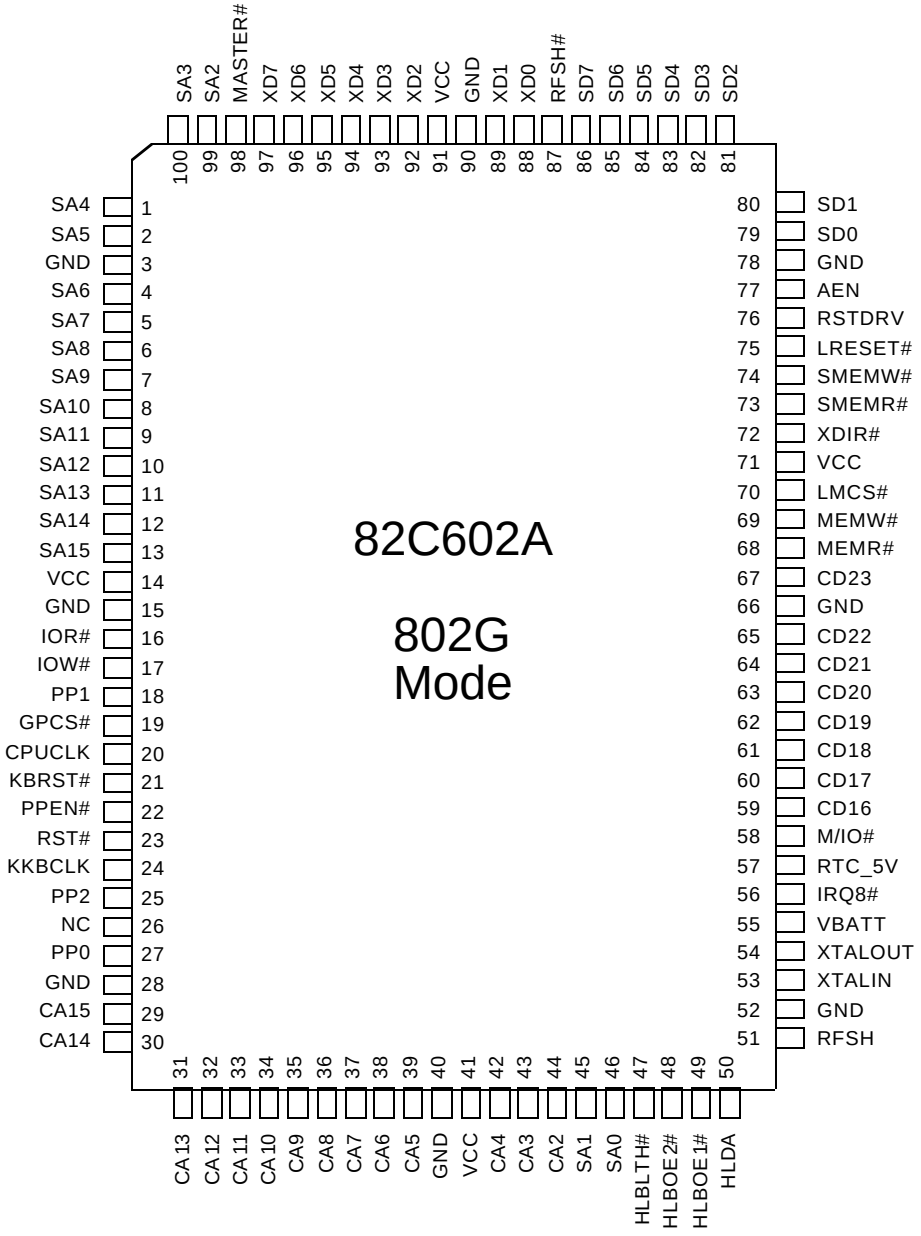

Table 3-1 802G Mode - Numerical Pin Cross-Reference List

	Pin Name	Pin Type	Pin #	Pin Name	Pin Type	Pin #	Pin Name	Pin Type	Pin #	Pin Name	Pin Type
	SA4	I/O	26	NC		51	RFSH	O	76	RSTDRV	O
2	SA5	I/O	27	PP0	O	52	GND	G	77	AEN	O
3	GND	G	28	GND	G	53	XTALIN	I	78	GND	G
4	SA6	I/O	29	CA15	I/O	54	XTALOUT	O	79	SD0	I/O
5	SA7	I/O	30	CA14	I/O	55	VBATT	I	80	SD1	I/O
6	SA8	I/O	31	CA13	I/O	56	IRQ8#	O	81	SD2	I/O
7	SA9	I/O	32	CA12	I/O	57	RTC_5V	I	82	SD3	I/O
8	SA10	I/O	33	CA11	I/O	58	M/IO#	I	83	SD4	I/O
9	SA11	I/O	34	CA10	I/O	59	CD16	I/O	84	SD5	I/O
10	SA12	I/O	35	CA9	I/O	60	CD17	I/O	85	SD6	I/O
11	SA13	I/O	36	CA8	I/O	61	CD18	I/O	86	SD7	I/O
12	SA14	I/O	37	CA7	I/O	62	CD19	I/O	87	RFSH#	I
13	SA15	I/O	38	CA6	I/O	63	CD20	I/O	88	XD0	I/O
14	VCC	P	39	CA5	I/O	64	CD21	I/O	89	XD1	I/O
15	GND	G	40	GND	G	65	CD22	I/O	90	GND	G
16	IOR#	I	41	VCC	P	66	GND	G	91	VCC	P
17	IOW#	I	42	CA4	I/O	67	CD23	I/O	92	XD2	I/O
18	PP1	O	43	CA3	I/O	68	MEMR#	I	93	XD3	I/O
19	GPCS#	O	44	CA2	I/O	69	MEMW#	I	94	XD4	I/O
20	CPUCLK	I	45	SA1	I/O	70	LMCS#	I	95	XD5	I/O
21	KBCLK	I	46	SA0	I/O	71	VCC	P	96	XD6	I/O
22	PPEN#	I	47	HLBLTH#	I	72	XDIR#	I	97	XD7	I/O
23	RST#	I	48	HLBOE2#	I	73	SMEMR#	O	98	MASTER#	I
24	KKBCLK	O	49	HLBOE1#	I	74	SMEMW#	O	99	SA2	I/O
25	PP2	O	50	HLDA	I	75	LRESET#	O	100	SA3	I/O

Table 3-2 802G Mode - Alphabetical Pin Cross-Reference List

Pin Name	Pin #	Pin Type	Pin Name	Pin #	Pin Type	Pin Name	Pin #	Pin Type	Pin Name	Pin #	Pin Type
AEN	77	O	GND	15	G	PP1	18	O	SD1	80	I/O
CA2	44	I/O	GND	28	G	PP2	25	O	SD2	81	I/O
CA3	43	I/O	GND	40	G	PPEN#	22	I	SD3	82	I/O
CA4	42	I/O	GND	52	G	RFSH	51	O	SD4	83	I/O
CA5	39	I/O	GND	66	G	RFSH#	87	I	SD5	84	I/O
CA6	38	I/O	GND	78	G	RST#	23	I	SD6	85	I/O
CA7	37	I/O	GND	90	G	RSTDRV	76	O	SD7	86	I/O
CA8	36	I/O	GPCS#	19	O	RTC_5V	57	I	SMEMR#	73	O
CA9	35	I/O	HLBLTH#	47	I	SA0	46	I/O	SMEMW#	74	O
CA10	34	I/O	HLBOE2#	48	I	SA1	45	I/O	VBATT	55	I
CA11	33	I/O	HLBOE1#	49	I	SA2	99	I/O	VCC	14	P
CA12	32	I/O	HLDA	50	I	SA3	100	I/O	VCC	41	P
CA13	31	I/O	IOR#	16	I	SA4	1	I/O	VCC	71	P
CA14	30	I/O	IOW#	17	I	SA5	2	I/O	VCC	91	P
CA15	29	I/O	IRQ8#	56	O	SA6	4	I/O	XD0	88	I/O
CD16	59	I/O	KBCLK	21	I	SA7	5	I/O	XD1	89	I/O
CD17	60	I/O	KKBCLK	24	O	SA8	6	I/O	XD2	92	I/O
CD18	61	I/O	LMCS#	70	I	SA9	7	I/O	XD3	93	I/O
CD19	62	I/O	LRESET#	75	O	SA10	8	I/O	XD4	94	I/O
CD20	63	I/O	MASTER#	98	I	SA11	9	I/O	XD5	95	I/O
CD21	64	I/O	MEMR#	68	I	SA12	10	I/O	XD6	96	I/O
CD22	65	I/O	MEMW#	69	I	SA13	11	I/O	XD7	97	I/O
CD23	67	I/O	M/IO#	58	I	SA14	12	I/O	XDIR#	72	I
CPUCLK	20	I	NC	26		SA15	13	I/O	XTALIN	53	I
GND	3	G	PP0	27	O	SD0	79	I/O	XTALOUT	54	O

3.1 802G Mode Signal Descriptions

3.1.1 Clock and Reset Interface Signals

Signal Name	Pin No.	Signal Type	Signal Description
CPUCLK	20	I	***CPU Clock:*** This pin is an input from the processor 1X clock signal.
RST#	23	I	***Reset:*** PWRGD input from the power supply.
RSTDRV	76	O	***Reset Drive:*** An active high reset output to the AT bus.
LRESET#	75	O	***Local Reset:*** An active low reset output to the VESA local bus.

3.1.2 CPU Interface Signals

Signal Name	Pin No.	Signal Type	Signal Description
M/IO#	58	I	***CPU Memory / I/O Status:*** This signal is driven by the CPU cycle after ADS# is asserted and defines the bus cycle along with D/C# and W/R#.
HLDA	50	I	***Hold Acknowledge:*** This input from the CPU informs the system that the CPU has given control to another local bus master.

3.1.3 Address Bus Interface Signals

Signal Name	Pin No.	Signal Type	Signal Description
SA[15:0]	13:4, 2, 1, 100, 99, 45, 46	I/O	***System Address AT Bus Lines 15 through 0.***
CA[15:2]	29:39, 42:44	I/O	***CPU Address Lines 15 through 2.***

3.1.4 Data Bus and Control Interface Signals

Signal Name	Pin No.	Signal Type	Signal Description
SD[7:0]	86:79	I/O	***System Data AT Bus Lines 7 through 0.***
XD[7:0]	97:92, 89, 88	I/O	***XD Bus Data Lines 7 through 0:*** XD7 and XD4 must be sampled low during reset to enter the 802G Mode. A 2.2K pull-down resistor is recommended on these lines. All XD lines on the 82C602A have internal weak pull-up resistors and do not require any external pull-up resistors.
XDIR#	72	I	***XD Bus Direction:*** A direction control signal for the SD bus to/from the XD bus. When active, will allow the XD bus to flow onto the SD bus.
CD[23:16]	67, 65:59	I/O	***CPU Data Bus Lines 23 through 16.***
HLBOE1#	49	I	***Output enable for CD[23:16l to SD[7:0]:*** This signal is the HD bus low byte enable control from the chipset to the 82C602A.
HLBOE2#	48	I	***Output enable for SD[7:0] to CD[23:16]*** latch from the chipset to the 82C602A.

802G Mode Signal Descriptions (cont.)

Signal Name	Pin No.	Signal Type	Signal Description
HLBLTH#	47	I	***Latch control for SD[7:0] to CD[23:16]*** for the 82C802G.

3.1.5 AT Bus Command/Control Interface Signals

Signal Name	Pin No.	Signal Type	Signal Description
IOR#	16	I	***AT I/O Read Command:*** This input is tied to IOR# of the chipset.
IOW#	17	I	***AT I/O Write Command:*** This input signal is tied to IOW# of the chipset.
MEMR#	68	I	***Memory Read Command:*** This input signal is tied to MEMR# of the chipset.
MEMW#	69	I	***Memory Write Command:*** This input signal is tied to MEMW# of the chipset.
SMEMR#	73	O	***AT Memory Read Low 1 Meg Command:*** This output is the ORed combination of MEMR# and LMCS#.
SMEMW#	74	O	***AT Memory Write Low 1 Meg Command:*** This output is the ORed combination of MEMW# and LMCS#.
LMCS#	70	I	***Low 1 Meg Memory Chip Select:*** This input from the chipset is active for memory cycle below 1MB.
MASTER#	98	I	***Master:*** This master cycle indication signal is used to control the CA/SA buffer direction.
RFSH#	87	I	***Refresh:*** This refresh cycle indication signal is used to: 1) Enable the refresh address from internal address counter. 2) Tristate the CA/SA buffer.
RFSH	51	O	***Refresh:*** This is the inverted output of pin 87.
AEN	77	O	***Address Enable:*** When high, the DMA controller has control of the address lines, data lines, MEMR#, MEMW#, IOR#, and IOW#. This signal is connected to AEN of the AT bus.

3.1.6 Real-Time Clock Interface Signals

Signal Name	Pin No.	Signal Type	Signal Description
IRQ8#	56	O	***Interrupt Request Bit 8:*** The alarm output interrupt signal generated by the internal real-time clock.
RTC_5V	57	I	***Real-time Clock 5.0V:*** This pin must be connected to +5V. This input will prevent the lithium battery from being accessed during power-on.
VBATT	55	I	***Voltage Battery:*** This input pin is connected to a 3 volt lithium battery. It is used to power the internal NVM and RTC during power off.
KBCLK	21	I	***Keyboard Clock Input:*** This input signal is from the keyboard controller.
KKBCLK	24	O	***Keyboard Clock Output:*** This signal outputs clock information to the keyboard.
XTALIN	53	I	***Crystal Oscillator Input:*** 32.768KHz XTAL output.
XTALOUT	54	O	***Crystal Oscillator Output:*** 32.768KHz XTAL output.

802G Mode Signal Descriptions (cont.)

3.1.7 Miscellaneous Interface Signals

Signal Name	Pin No.	Signal Type	Signal Description
PP[2:0]	25, 18, 27	O	***Power Port Bits 2 through 0:*** These output pins are the latched power port output pins. These pins are used to signal a low power state to the components in the system.
PPEN#	22	I	***Power Port Enable:*** This input pin from the 82C802G latches power port data on the SD[2:0] bus onto the PP[2:0] output pins.
NC	26		***No Connect:*** This pin should be left unconnected.
GPCS#	19	O	***General Purpose Chip Select:*** This output is controlled by Index F7h-F9h. (Refer to the 82C601/602 Data Book.)

3.1.8 Power and Ground Pins

Signal Name	Pin No.	Signal Type	Signal Description
VCC	14, 41, 71, 91	P	Power Connection
GND	3, 15, 28, 40, 52, 66, 78, 90	G	Ground Connection

Legend:

G	Ground
I/O	Input/Output
G	Ground
OD	Open Drain
I/O	Input/Output
P	Power
Sch	Schmitt-trigger

Figure 3-2 Blackhawk Mode Pin Diagram (100-Pin PQFP)

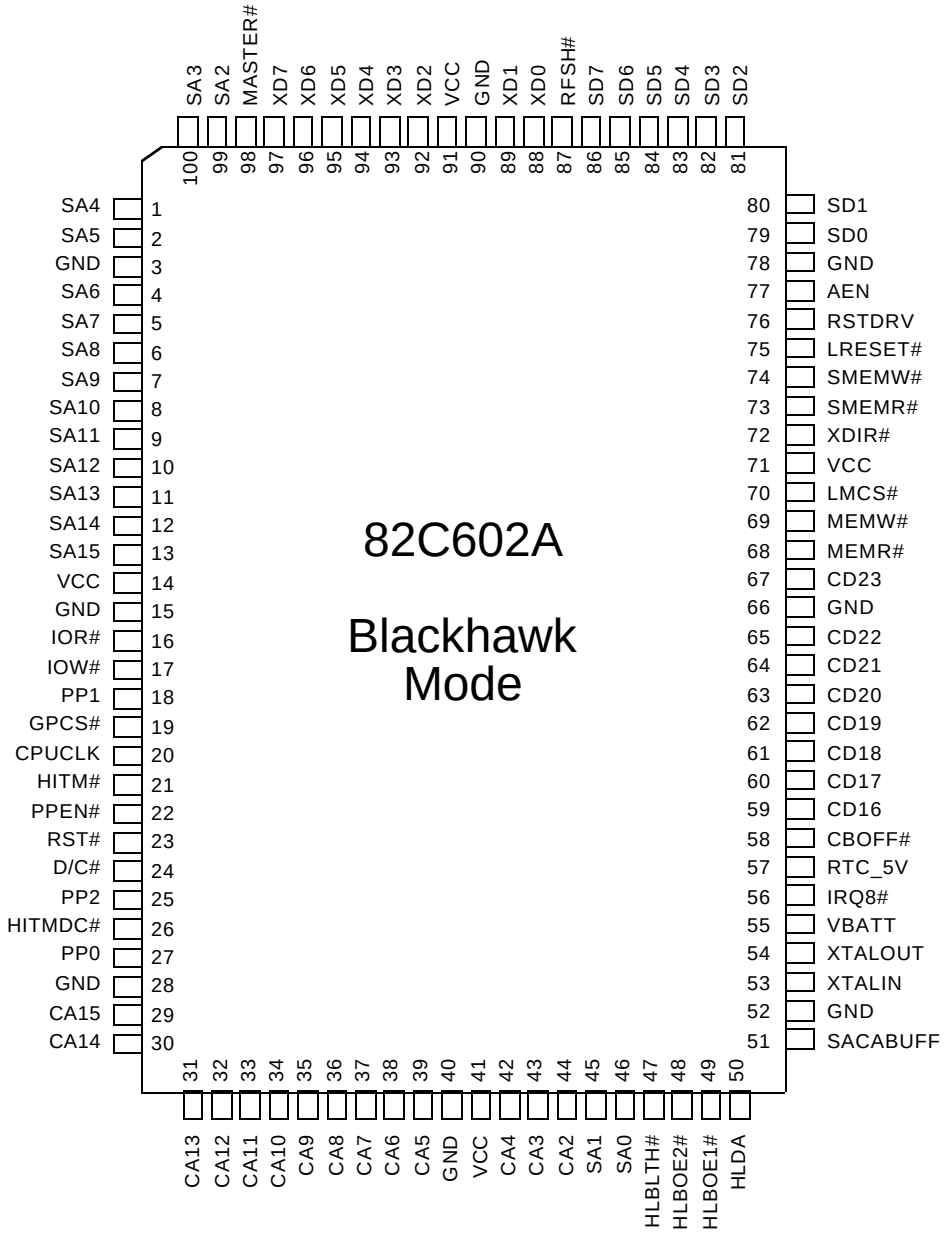

Table 3-3 Blackhawk Mode - Numerical Pin Cross-Reference List

Pin #	Pin Name	Pin Type
1	SA4	I/O
2	SA5	I/O
3	GND	G
4	SA6	I/O
5	SA7	I/O
6	SA8	I/O
7	SA9	I/O
8	SA10	I/O
9	SA11	I/O
10	SA12	I/O
11	SA13	I/O
12	SA14	I/O
13	SA15	I/O
14	VCC	P
15	GND	G
16	IOR#	I
17	IOW#	I
18	PP1	O
19	GPCS#	O
20	CPUCLK	I
21	HITM#	I
22	PPEN#	I
23	RST#	I
24	D/C#	I
25	PP2	O
26	HITMDC#	O
27	PP0	O
28	GND	G
29	CA15	I/O
30	CA14	I/O
31	CA13	I/O
32	CA12	I/O
33	CA11	I/O
34	CA10	I/O
35	CA9	I/O
36	CA8	I/O
37	CA7	I/O
38	CA6	I/O
39	CA5	I/O
40	GND	G
41	VCC	P
42	CA4	I/O
43	CA3	I/O
44	CA2	I/O
45	SA1	I/O
46	SA0	I/O
47	HLBLTH#	I
48	HLBOE2#	I
49	HLBOE1#	I
50	HLDA	I
51	SACABUFF	O
52	GND	G
53	XTALIN	I
54	XTALOUT	O
55	VBATT	I
56	IRQ8#	O
57	RTC_5V	I
58	CBOFF#	I
59	CD16	I/O
60	CD17	I/O
61	CD18	I/O
62	CD19	I/O
63	CD20	I/O
64	CD21	I/O
65	CD22	I/O
66	GND	G
67	CD23	I/O
68	MEMR#	I
69	MEMW#	I
70	LMCS#	I
71	VCC	P
72	XDIR#	I
73	SMEMR#	O
74	SMEMW#	O
75	LRESET#	O
76	RSTDRV	O
77	AEN	O
78	GND	G
79	SD0	I/O
80	SD1	I/O
81	SD2	I/O
82	SD3	I/O
83	SD4	I/O
84	SD5	I/O
85	SD6	I/O
86	SD7	I/O
87	RFSH#	I
88	XD0	I/O
89	XD1	I/O
90	GND	G
91	VCC	P
92	XD2	I/O
93	XD3	I/O
94	XD4	I/O
95	XD5	I/O
96	XD6	I/O
97	XD7	I/O
98	MASTER#	I
99	SA2	I/O
100	SA3	I/O

Table 3-4 Blackhawk Mode - Alphabetical Pin Cross-Reference List

Pin Name	Pin #	Pin Type
AEN	77	O
CA2	44	I/O
CA3	43	I/O
CA4	42	I/O
CA5	39	I/O
CA6	38	I/O
CA7	37	I/O
CA8	36	I/O
CA9	35	I/O
CA10	34	I/O
CA11	33	I/O
CA12	32	I/O
CA13	31	I/O
CA14	30	I/O
CA15	29	I/O
CD16	59	I/O
CD17	60	I/O
CD18	61	I/O
CD19	62	I/O
CD20	63	I/O
CD21	64	I/O
CD22	65	I/O
CD23	67	I/O
CBOFF#	58	I
CPUCLK	20	I
D/C#	24	I
GND	3	G
GND	15	G
GND	28	G
GND	40	G
GND	52	G
GND	66	G
GND	78	G
GND	90	G
GPCS#	19	O
HITM#	21	I
HITMDC#	26	O
HLBLTH#	47	I
HLBOE2#	48	I
HLBOE1#	49	I
HLDA	50	I
IOR#	16	I
IOW#	17	I
IRQ8#	56	O
LMCS#	70	I
LRESET#	75	O
MASTER#	98	I
MEMR#	68	I
MEMW#	69	I
PP0	27	O
PP1	18	O
PP2	25	O
PPEN#	22	I
RFSH#	87	I
RST#	23	I
RSTDRV	76	O
RTC_5V	57	I
SA0	46	I/O
SA1	45	I/O
SA2	99	I/O
SA3	100	I/O
SA4	1	I/O
SA5	2	I/O
SA6	4	I/O
SA7	5	I/O
SA8	6	I/O
SA9	7	I/O
SA10	8	I/O
SA11	9	I/O
SA12	10	I/O
SA13	11	I/O
SA14	12	I/O
SA15	13	I/O
SACABUFF	51	O
SD0	79	I/O
SD1	80	I/O
SD2	81	I/O
SD3	82	I/O
SD4	83	I/O
SD5	84	I/O
SD6	85	I/O
SD7	86	I/O
SMEMR#	73	I/O
SMEMW#	74	I/O
VBATT	55	I
VCC	14	P
VCC	41	P
VCC	71	P
VCC	91	P
XD0	88	I/O
XD1	89	I/O
XD2	92	I/O
XD3	93	I/O
XD4	94	I/O
XD5	95	I/O
XD6	96	I/O
XD7	97	I/O
XDIR#	72	I
XTALIN	53	I
XTALOUT	54	O

3.2 Blackhawk Mode Signal Descriptions

3.2.1 Clock and Reset Interface Signals

Signal Name	Pin No.	Signal Type	Signal Description
CPUCLK	20	I	***CPU Clock:*** This pin is an input from the processor 1X clock signal. It is used for holding RESET active for 64 clocks.
RST#	23	I	***Reset:*** PWRGD input from the power supply.
RSTDRV	76	O	***Reset Drive:*** An active high reset output to the AT bus.
LRESET#	75	O	***Local Reset:*** An active low reset output to the VESA local bus.

3.2.2 CPU Interface Signals

Signal Name	Pin No.	Signal Type	Signal Description
HITM#	21	I	***Hit Modified:*** This input from the CPU indicates a write-back of a dirty line from the primary L1 cache is necessary to service the current memory cycle.
HITMDC#	26	O	***Hit Modified and Data / Control:*** This output is the ANDed combination of pins 21 and 24. The 82C802GP uses this output to multiplex between HITM# and D/C#.
CBOFF#	58	I	***Cache Module Back-off:*** This input is from the cache module to indicate that a write-back of a dirty line from the secondary cache is necessary to service the cur-rent memory cycle and all other devices must back-off from the CPU bus so that the cache can take control.
D/C#	24	I	***Data / Control:*** This input pin is ANDed with pin 21 to create a combined out-put on pin 26. The purpose is to allow the 82C802GP one pin to multiplex between HITM# and D/C#.
HLDA	50	I	***Hold Acknowledge:*** Hold acknowledge output signal from the CPU.

3.2.3 Address Bus Interface Signals

Signal Name	Pin No.	Signal Type	Signal Description
SA[15:0]	13:4, 2, 1, 100, 99, 45, 46	I/O	***System Address AT Bus Lines 15 through 0.***
CA[15:2]	29:39, 42:44	I/O	***CPU Address Lines 15 through 2.***

3.2.4 Data Bus and Control Interface Signals

Signal Name	Pin No.	Signal Type	Signal Description
SD[7:0]	86:79	I/O	***System Data AT Bus Lines 7 through 0.***

Blackhawk Mode Signal Descriptions (cont.)

Signal Name	Pin No.	Signal Type	Signal Description
XD[7:0]	97:92, 89, 88	I/O	***XD Bus Data Lines 7 through 0:*** XD6 and XD4 must be sampled low during reset to enter the Blackhawk Mode. A 2.2K pull-down resistor is recommended on these lines. All XD lines on the 82C602A have internal weak pull-up resistors and do not require any external pull-up resistors.
XDIR#	72	I	***XD Bus Direction:*** A direction control signal for the SD bus to/from the XD bus. When active, will allow the XD bus to flow onto the SD bus.
CD[23:16]	67, 65:59	I/O	***CPU Data Bus Lines 23 through 16.***
HLBOE1#	49	I	***Output enable for CD[23:16l to SD[7:0]:*** This signal is the HD bus low byte enable control from the chipset to the 82C602A.
HLBOE2#	48	I	***Output enable for SD[7:0] to CD[23:16]*** latch from the chipset to the 82C602A.
HLBLTH#	47	I	***Latch control for SD[7:0] to CD[23:16]*** for the 82C802G.
SACABUFF	51	O	***SA Bus to CA Bus Buffer Control:*** The buffer will be disabled if either RFSH# or CBOFF# are active.

3.2.5 AT Bus Command/Control Interface Signals

Signal Name	Pin No.	Signal Type	Signal Description
IOR#	16	I	***AT I/O Read Command:*** This input is tied to IOR# of the chipset.
IOW#	17	I	***AT I/O Write Command:*** This input signal is tied to IOW# of the chipset.
MEMR#	68	I	***Memory Read Command:*** This input signal is tied to MEMR# of the chipset.
MEMW#	69	I	***Memory Write Command:*** This input signal is tied to MEMW# of the chipset.
SMEMR#	73	O	***AT Memory Read Low 1 Meg Command:*** This output is the ORed combination of MEMR# and LMCS#.
SMEMW#	74	O	***AT Memory Write Low 1 Meg Command:*** This output is the ORed combination of MEMW# and LMCS#.
LMCS#	70	I	***Low 1 Meg Memory Chip Select:*** This input from the chipset is active for memory cycles below 1MB.
MASTER#	98	I	***Master:*** This master cycle indication signal is used to control the CA/SA buffer direction.
RFSH#	87	I	***Refresh:*** This refresh cycle indication signal is used to: 1) Enable the refresh address from internal address counter. 2) Tristate the CA/SA buffer.
AEN	77	O	***Address Enable:*** When high, the DMA controller has control of the address lines, data lines, MEMR#, MEMW#, IOR#, and IOW#. This signal is connected to AEN of the AT bus.

Blackhawk Mode Signal Descriptions (cont.)

3.2.6 Real-Time Clock Interface Signals

Signal Name	Pin No.	Signal Type	Signal Description
IRQ8#	56	O	***Interrupt Request Bit 8:*** The alarm output interrupt signal generated by the internal real-time clock.
RTC_5V	57	I	***Real-time Clock 5.0V:*** This pin must be connected to +5V. This input will prevent the lithium battery from being accessed during power-on.
VBATT	55	I	***Voltage Battery:*** This input pin is connected to a 3 volt lithium battery. It is used to power the internal NVM and RTC during power off.
XTALIN	53	I	***Crystal Oscillator Input:*** 32.768KHz XTAL output.
XTALOUT	54	O	***Crystal Oscillator Output:*** 32.768KHz XTAL output.

3.2.7 Miscellaneous Interface Signals

Signal Name	Pin No.	Signal Type	Signal Description
PP[2:0]	25, 18, 27	O	***Power Port Bits 2 through 0:*** These output pins are the latched power port output pins. These pins are used to signal a low power state to the components in the system.
PPEN#	22	I	***Power Port Enable:*** This input pin from the Blackhawk Chipset latches power port data onto the PP[2:0] output pins.
GPCS#	19	O	***General Purpose Chip Select:*** This output is controlled by Index F7h-F9h. (Refer to the 82C601/602 Data Book.)

3.2.8 Power and Ground Pins

Signal Name	Pin No.	Signal Type	Signal Description
VCC	14, 41, 71, 91	P	Power Connection
GND	3, 15, 28, 40, 52, 66, 78, 90	G	Ground Connection

Legend:

G	Ground
I/O	Input/Output
G	Ground
OD	Open Drain
I/O	Input/Output
P	Power
Sch	Schmitt-trigger

Figure 3-3 486 NB Mode Pin Diagram (100-Pin PQFP)

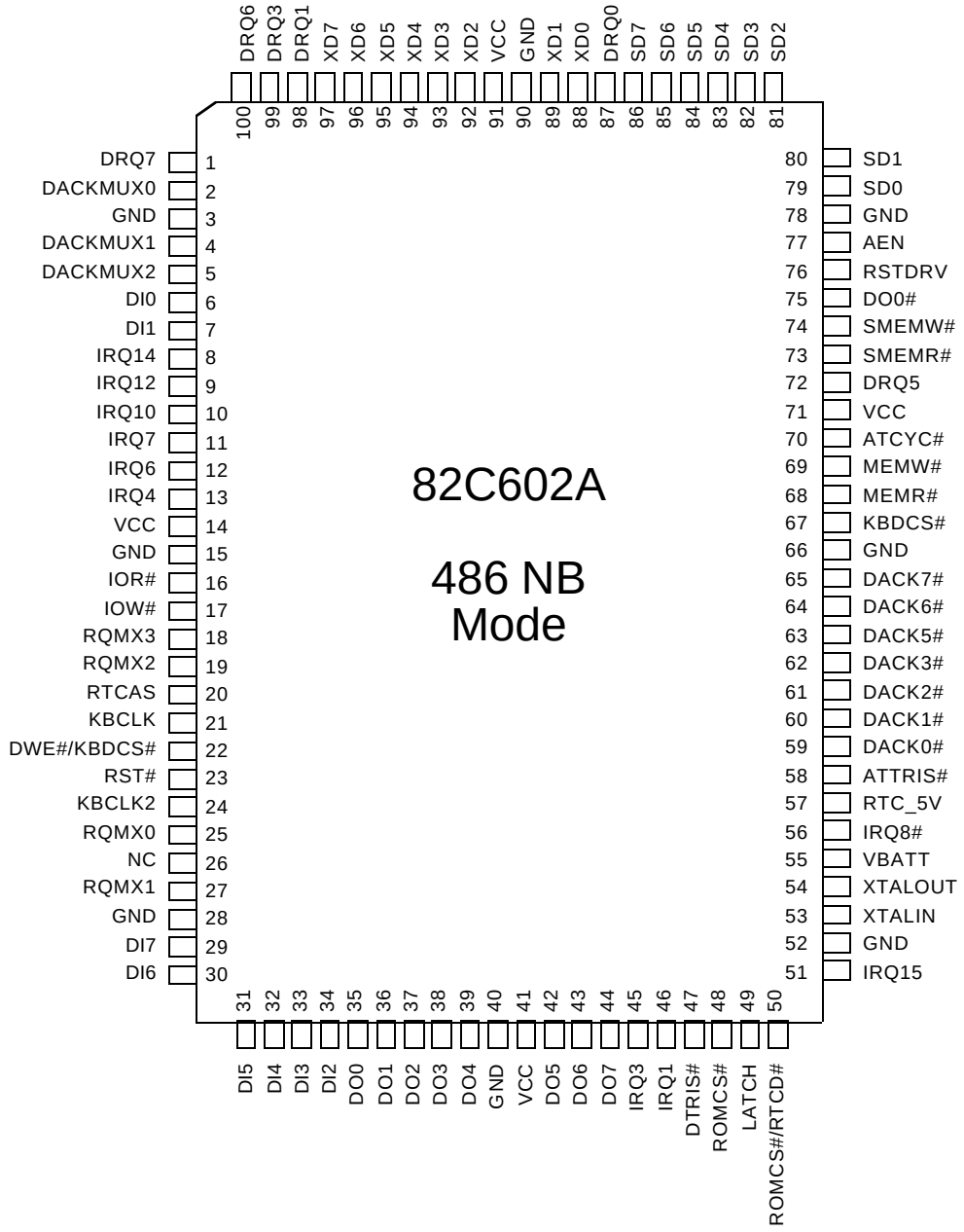

Figure 3-4 486 NB Mode Pin Diagram (100-Pin TQFP)

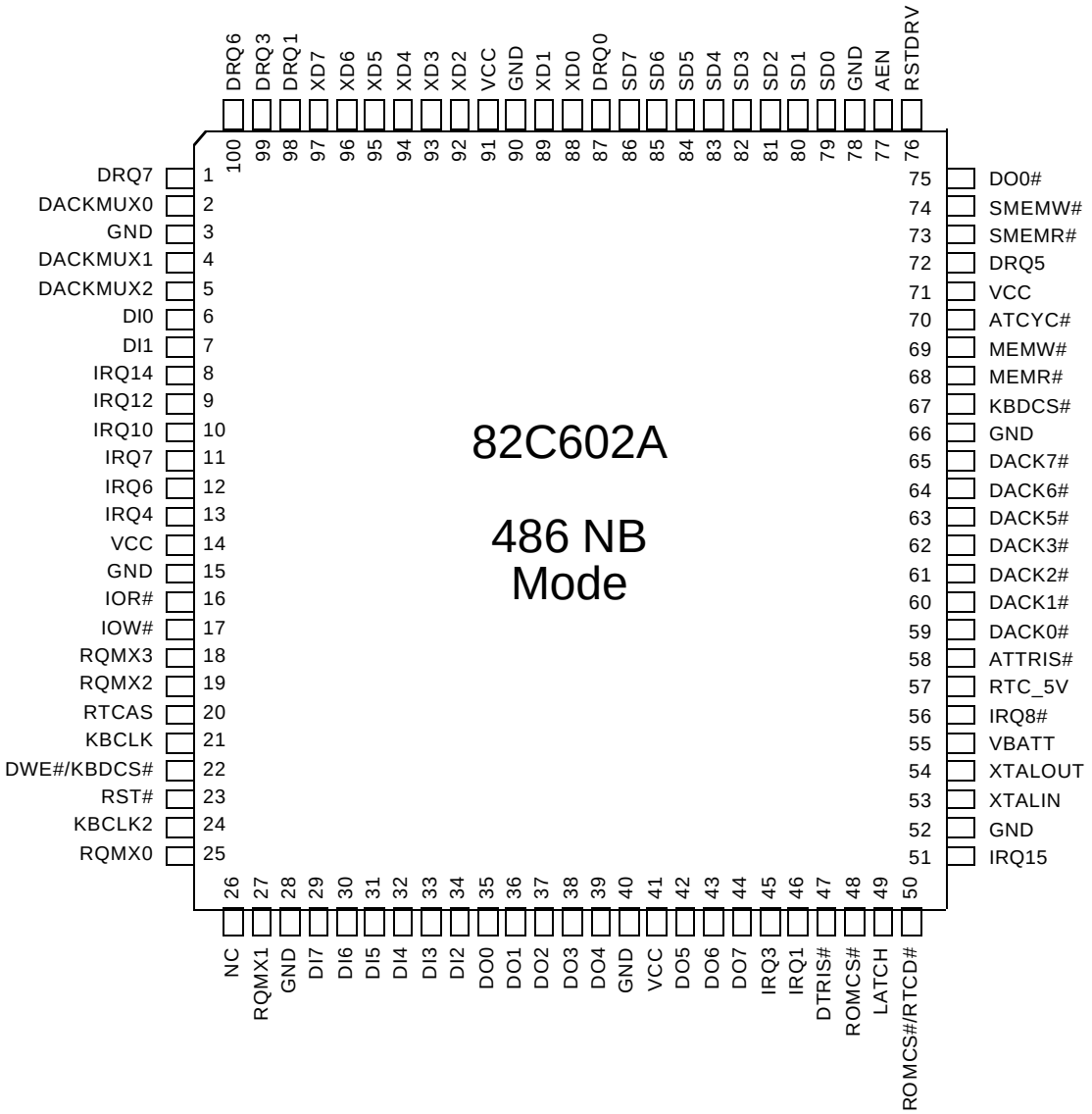

Table 3-5 486 NB Mode - Numerical Pin Cross-Reference List

Pin #	Pin Name	Pin Type	Pin #	Pin Name	Pin Type	Pin #	Pin Name	Pin Type	Pin #	Pin Name	Pin Type
1	DRQ7	I	26	NC		51	IRQ15	I	76	RSTDRV	O
2	DACKMUX0	I	27	RQMX1	O	52	GND	G	77	AEN	O
3	GND	G	28	GND	G	53	XTALIN	I	78	GND	G
4	DACKMUX1	I	29	DI7	I	54	XTALOUT	O	79	SD0	I/O
5	DACKMUX2	I	30	DI6	I	55	VBATT	I	80	SD1	I/O
6	DI0	I	31	DI5	I	56	IRQ8#	O	81	SD2	I/O
7	DI1	I	32	DI4	I	57	RTC_5V	I	82	SD3	I/O
8	IRQ14	I	33	DI3	I	58	ATTRIS#	I	83	SD4	I/O
9	IRQ12	I	34	DI2	I	59	DACK0#	O	84	SD5	I/O
10	IRQ10	I	35	DO0	O	60	DACK1#	O	85	SD6	I/O
11	IRQ7	I	36	DO1	O	61	DACK2#	O	86	SD7	I/O
12	IRQ6	I	37	DO2	O	62	DACK3#	O	87	DRQ0	I
13	IRQ4	I	38	DO3	O	63	DACK5#	O	88	XD0	I/O
14	VCC	P	39	DO4	O	64	DACK6#	O	89	XD1	I/O
15	GND	G	40	GND	G	65	DACK7#	O	90	GND	G
16	IOR#	I	41	VCC	P	66	GND	G	91	VCC	P
17	IOW#	I	42	DO5	O	67	KBDCS#	O	92	XD2	I/O
18	RQMX3	O	43	DO6	O	68	MEMR#	I	93	XD3	I/O
19	RQMX2	O	44	DO7	O	69	MEMW#	I	94	XD4	I/O
20	RTCAS	I	45	IRQ3	I	70	ATCYC#	I	95	XD5	I/O
21	KBCLK	I	46	IRQ1	I	71	VCC	P	96	XD6	I/O
22	DWE#/KBDCS#	I	47	DTRIS#	I	72	DRQ5	I	97	XD7	I/O
23	RST#	I	48	ROMCS#	I	73	SMEMR#	O	98	DRQ1	I
24	KBCLK2	I	49	LATCH	I	74	SMEMW#	O	99	DRQ3	I
25	RQMX0	O	50	ROMCS#/RTCD#	I	75	DO0#	O	100	DRQ6	I

Table 3-6 486 NB Mode - Alphabetical Pin Cross-Reference List

Pin Name	Pin #	Pin Type	Pin Name	Pin #	Pin Type	Pin Name	Pin #	Pin Type	Pin Name	Pin #	Pin Type
AEN	77	O	DO3	38	O	IRQ4	13	I	SD0	79	I/O
ATCYC#	70	I	DO4	39	O	IRQ6	12	I	SD1	80	I/O
ATTRIS#	58	I	DO5	42	O	IRQ7	11	I	SD2	81	I/O
DACK0#	59	O	DO6	43	O	IRQ8#	56	O	SD3	82	I/O
DACK1#	60	O	DO7	44	O	IRQ10	10	I	SD4	83	I/O
DACK2#	61	O	DRQ0	87	I	IRQ12	9	I	SD5	84	I/O
DACK3#	62	O	DRQ1	98	I	IRQ14	8	I	SD6	85	I/O
DACK5#	63	O	DRQ3	99	I	IRQ15	51	I	SD7	86	I/O
DACK6#	64	O	DRQ5	72	I	KBCLK	21	I	SMEMR#	73	O
DACK7#	65	O	DRQ6	100	I	KBCLK2	24	I	SMEMW#	74	O
DACKMUX0	2	I	DRQ7	1	I	KBDCS#	67	O	VBATT	55	I
DACKMUX1	4	I	DTRIS#	47	I	LATCH	49	I	VCC	14	P
DACKMUX2	5	I	DWE#/KBDCS#	22	I	MEMR#	68	I	VCC	41	P
DI0	6	I	GND	3	G	MEMW#	69	I	VCC	71	P
DI1	7	I	GND	15	G	NC	26		VCC	91	P
DI2	34	I	GND	28	G	ROMCS#	48	I	XTALIN	53	I
DI3	33	I	GND	40	G	ROMCS#/RTCD#	50	I	XTALOUT	54	O
DI4	32	I	GND	52	G	RQMX0	25	O	XD0	88	I/O
DI5	31	I	GND	66	G	RQMX1	27	O	XD1	89	I/O
DI6	30	I	GND	78	G	RQMX2	19	O	XD2	92	I/O
DI7	29	I	GND	90	G	RQMX3	18	O	XD3	93	I/O
DO0#	75	O	IOR#	16	I	RTCAS	20	I	XD4	94	I/O
DO0	35	O	IOW#	17	I	RST#	23	I	XD5	95	I/O
DO1	36	O	IRQ1	46	I	RSTDRV	76	O	XD6	96	I/O
DO2	37	O	IRQ3	45	I	RTC_5V	57	I	XD7	97	I/O

3.3 486 NB Mode Signal Descriptions

Refer to the 486 NB internal circuitry schematic in Section 4.0 for complete details.

3.3.1 Clock and Reset Interface Signals

Signal Name	Pin No.	Signal (Drive) Type	Signal Description
RST#	23	I-S	***Reset:*** Reset input to the 82C602A logic.
RSTDRV	76	O (24mA)	***Reset Drive:*** Inverted RST#.

3.3.2 Interrupt/Control Interface Signals

Signal Name	Pin No.	Signal (Drive) Type	Signal Description
IRQ1, IRQ3, IRQ4, IRQ6, IRQ7	46, 45, 13, 12, 11	I	***Interrupt Request Bits 1, 3, 4, 6, and 7.***
IRQ10, IRQ12, IRQ14, IRQ15	10, 9, 8, 51	I	***Interrupt Request Bits 10, 12, 14, and 15.***
IOR#	16	I	***I/O Read***
IOW#	17	I	***I/O Write***
MEMR#	68	I	***Memory Read***
MEMW#	69	I	***Memory Write***
SMEMR#	73	O (24mA)	***SMEMR# with tristate control.***
SMEMW#	74	O (24mA)	***SMEMW# with tristate control.***

3.3.3 ISA DMA Arbiter Interface Signals

Signal Name	Pin No.	Signal (Drive) Type	Signal Description
DRQ[7:5] DRQ3, DRQ1, DRQ0	1, 100, 72, 99, 98, 87	I	***DMA Request bits 7 through 5, 3, 1, and 0.***
DACK[7:5]#, DACK[3:0]#	65:63, 62:59	O (6mA)	***DMA Acknowledge bits 7 through 5, and 3 through 0.***
DACKMUX[2:0]	5, 4, 2	I	***Encoded DACKs***
RQMX3	18	O (6mA)	***Mux of DRQ1, DRQ3, DRQ6, DRQ7***
RQMX2	19	O (6mA)	***Mux of IRQ10, IRQ15, DRQ05***

486 NB Mode Signal Descriptions (cont.)

Signal Name	Pin No.	Signal (Drive) Type	Signal Description
RQMX1	27	O (4mA)	***Mux of IRQ4, IRQ6, IRQ8#, IRQ12***
RQMX0	25	O (4mA)	***Mux of IRQ1, IRQ3, IRQ7, IRQ14***
DWE#/KBDCS#	22	i	***DRAM Write Enable or Keyboard Chip Select***

3.3.4 Bus Interface Signals

Signal Name	Pin No.	Signal (Drive) Type	Signal Description
DI[7:0]	29:34, 7, 6	I	***Data Buffer Inputs 7 through 0***
DO[7:0]	44:42, 39:35	O (4mA)	***Data Buffer Outputs 7 through 0***
DO0#	75	O (8mA)	***Inverted Data Buffer Output 0***
DTRIS#	47	I	***Data Buffer Tristate Control:*** When active, will tristate the data buffer.
ROMCS#	48	I	***ROM Chip Select:*** This signal, when active, will allow ROM on the XD bus to put information on the SD bus.
ROMCS#/RTCD#	50	I	***ROM Chip Select and RTC Command Line:*** This signal is used to enable accesses to the ROM and RTC from the 82C465MV.
SD[7:0]	86:79	I/O (24mA)	***SD Bus Lines 7 through 0***
XD[7:0]	97:92, 89, 88	I/O (6mA)	***XD Bus Data Lines 7 through 0:*** XD4 and XD1 must be sampled low during reset to enter the 486 Notebook Mode. A 2.2K pull-down resistor is recommended on these lines. All XD lines in the 82C602A have internal weak pull-up resistors and do not require any external pull-up resistors.
ATTRIS#	58	I	***Tristates AT Bus Outputs:*** This is used to tristate the AT bus during low power mode.
ATCYC	70	I	***AT Cycle Indication***

3.3.5 Real-Time Clock and Keyboard Interface Signals

Signal Name	Pin No.	Signal (Drive) Type	Signal Description
RTCAS	20	I	***Real-time Clock Address Strobe:*** RTCAS is used to demultiplex the address/data bus. The falling edge of AS latches the address on XD[7:0].
RTC_5V	57	I	***Real-time Clock 5.0V:*** This pin must be connected to +5V. This input will prevent the lithium battery from being accessed during power-on.
VBATT	55	I	***Voltage Battery:*** This pin is connected to the CMOS and RTC battery.

486 NB Mode Signal Descriptions (cont.)

Signal Name	Pin No.	Signal (Drive) Type	Signal Description
IRQ8#	56	O	***Interrupt Request Bit 8:*** The alarm output interrupt generated by the internal RTC.
XTALIN	53	I	***Crystal Oscillator Input:*** 32.768KHz XTAL input.
XTALOUT	54	O	***Crystal Oscillator Output:*** 32.768KHz XTAL output.
KBCLK	21	I	***Keyboard Clock:*** This input is used for demuxing interrupts and DMA requests.
KBCLK2	24	I	***Keyboard Clock / 2:*** This input is used for demuxing interrupts and DMA requests.
KBDCS#	67	O (6mA)	***KBDCS# qualified with AEN:*** Allows the system to access the keyboard controller.

3.3.6 Miscellaneous Interface Signals

Signal Name	Pin No.	Signal Type	Signal Description
NC	26		***No Connection:*** This pin should be left unconnected.
LATCH	49	I	***Data Buffer Latch:*** This signal controls the latching of information on the data bus.
AEN	77	I	***Address Enable:*** This input is used to ensure that the system has access to the real-time clock.

3.3.7 Power and Ground Pins

Signal Name	Pin No.	Signal Type	Signal Description
VCC	14, 41, 71, 91	P	***Power Connection***
GND	3, 15, 28, 40, 52, 66, 78, 90	G	***Ground Connection***

Legend:

G	Ground
I/O	Input/Output
G	Ground
OD	Open Drain
I/O	Input/Output
P	Power
Sch	Schmitt-trigger

Figure 3-5 Viper DTA Mode Pin Diagram (100-Pin PQFP)

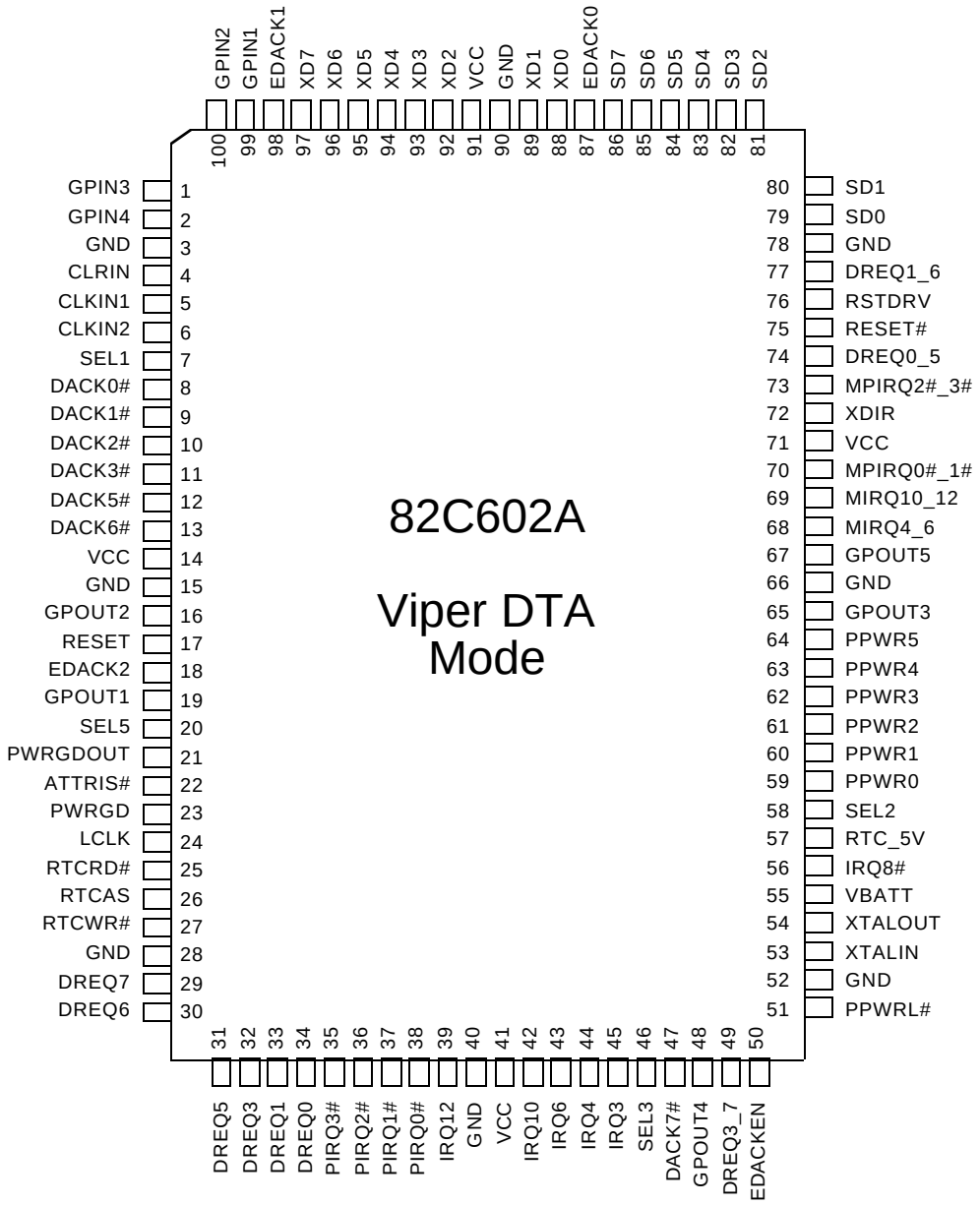

Table 3-7 Viper DTA Mode - Numerical Pin Cross-Reference List

Pin #	Pin Name	Pin Type	Pin #	Pin Name	Pin Type	Pin #	Pin Name	Pin Type	Pin #	Pin Name	Pin Type
1	GPIN3	I	26	RTCAS	I	51	PPWRL#	I	76	RSTDRV	O
2	GPIN4	I	27	RTCWR#	I	52	GND	G	77	DREQ1_6	O
3	GND	G	28	GND	G	53	XTALIN	I	78	GND	G
4	CLRIN	I	29	DREQ7	I	54	XTALOUT	O	79	SD0	I/O
5	CLKIN1	I	30	DREQ6	I	55	VBATT	I	80	SD1	I/O
6	CLKIN2	I	31	DREQ5	I	56	IRQ8#	O	81	SD2	I/O
7	SEL1	I	32	DREQ3	I	57	RTC_5V	I	82	SD3	I/O
8	DACK0#	O	33	DREQ1	I	58	SEL2	I	83	SD4	I/O
9	DACK1#	O	34	DREQ0	I	59	PPWR0	O	84	SD5	I/O
10	DACK2#	O	35	PIRQ3#	I	60	PPWR1	O	85	SD6	I/O
11	DACK3#	O	36	PIRQ2#	I	61	PPWR2	O	86	SD7	I/O
12	DACK5#	O	37	PIRQ1#	I	62	PPWR3	O	87	EDACK0	I
13	DACK6#	O	38	PIRQ0#	I	63	PPWR4	O	88	XD0	I/O
14	VCC	P	39	IRQ12	I	64	PPWR5	O	89	XD1	I/O
15	GND	G	40	GND	G	65	GPOUT3	O	90	GND	G
16	GPOUT2	O	41	VCC	P	66	GND	G	91	VCC	P
17	RESET	I	42	IRQ10	I	67	GPOUT5	O	92	XD2	I/O
18	EDACK2	I	43	IRQ6	I	68	MIRQ4_6	O	93	XD3	I/O
19	GPOUT1	O	44	IRQ4	I	69	MIRQ10_12	O	94	XD4	I/O
20	SEL5	I	45	SEL3	I	70	MPIRQ0#_1#	O	95	XD5	I/O
21	PWRGDOUT	O(OD)	46	SEL4	I	71	VCC	P	96	XD6	I/O
22	ATTRIS#	I	47	DACK7#	O	72	XDIR	I	97	XD7	I/O
23	PWRGD	I-S	48	GPOUT4	O	73	MPIRQ2#_3#	O	98	EDACK1	I
24	LCLK	I	49	DREQ3_7	O	74	DREQ0_5	O	99	GPIN1	I
25	RTCRD#	I	50	EDACKEN	I	75	RESET#	O	100	GPIN2	I

Table 3-8 Viper DTA Mode - Alphabetical Pin Cross-Reference List

Pin Name	Pin #	Pin Type	Pin Name	Pin #	Pin Type	Pin Name	Pin #	Pin Type	Pin Name	Pin #	Pin Type
ATTRIS#	22	I	GND	15	G	MPIRQ2#_3#	73	O	SD4	83	I/O
CLKIN1	5	I	GND	28	G	PIRQ0#	38	I	SD5	84	I/O
CLKIN2	6	I	GND	40	G	PIRQ1#	37	I	SD6	85	I/O
CLRIN	4	I	GND	52	G	PIRQ2#	36	I	SD7	86	I/O
DACK0#	8	O	GND	66	G	PIRQ3#	35	I	SEL1	7	I
DACK1#	9	O	GND	78	G	PPWR0	59	O	SEL2	58	I
DACK2#	10	O	GND	90	G	PPWR1	60	O	SEL3	45	I
DACK3#	11	O	GPIN1	99	I	PPWR2	61	O	SEL4	46	I
DACK5#	12	O	GPIN2	100	I	PPWR3	62	O	SEL5	20	I
DACK6#	13	O	GPIN3	1	I	PPWR4	63	O	VBATT	55	I
DACK7#	47	O	GPIN4	2	I	PPWR5	64	O	VCC	14	P
DREQ0	34	I	GPOUT1	19	O	PPWRL#	51	I	VCC	41	P
DREQ0_5	74	O	GPOUT2	16	O	PWRGD	23	I-S	VCC	71	P
DREQ1	33	I	GPOUT3	65	O	PWRGDOUT	21	O(OD)	VCC	91	P
DREQ1_6	77	O	GPOUT4	48	O	RESET	17	I	XD0	88	I/O
DREQ3	32	I	GPOUT5	67	O	RESET#	75	O	XD1	89	I/O
DREQ3_7	49	O	IRQ4	44	I	RSTDRV	76	O	XD2	92	I/O
DREQ5	31	I	IRQ6	43	I	RTC_5V	57	I	XD3	93	I/O
DREQ6	30	I	IRQ8#	56	O	RTCRD#	25	I	XD4	94	I/O
DREQ7	29	I	IRQ10	42	I	RTCAS	26	I	XD5	95	I/O
EDACK0	87	I	IRQ12	39	I	RTCWR#	27	I	XD6	96	I/O
EDACK1	98	I	LCLK	24	I	SD0	79	I/O	XD7	97	I/O
EDACK2	18	I	MIRQ4_6	68	O	SD1	80	I/O	XDIR	72	I
EDACKEN	50	I	MIRQ10_12	69	O	SD2	81	I/O	XTALIN	53	I
GND	3	G	MPIRQ0#_1#	70	O	SD3	82	I/O	XTALOUT	54	O

3.4 Viper DTA Mode Signal Descriptions

Refer to the Viper DTA internal circuitry schematic in Section 4.0 for complete details.

3.4.1 Clock and Reset Interface Signals

Signal Name	Pin No.	Signal Type	Signal Description
RESET	17	I	***Reset:*** Reset input from the Viper Desktop Chipset.
RESET#	75	O	***Reset:*** The inverted output of pin 17. This signal is also used to reset the internal real-time clock.
RSTDRV	76	O	***Reset Drive:*** This signal is the buffered output of pin 17 and is an active high reset output to the AT bus.
LCLK	24	I	***Local Bus Clock:*** The Viper Desktop Chipset demultiplexes its multiplexed signals based on either the LCLK or the 14.318MHz clock. This input to the 82C602A goes to the select input of the multiplexers internal to the 82C602A and is used to multiplex the IRQs and DREQs to the Viper Desktop Chipset.
PWRGD	23	I-Sch	***Power Good:*** The PWRGD input signal from the power supply.
PWRGDOUT	21	O (OD)	***Power Good Output:*** An open drain output signal to the Viper Desktop Chipset.

3.4.2 Interrupt/Control Interface Signals

Signal Name	Pin No.	Signal Type	Signal Description
IRQ4	44	I	***Interrupt Request Bit 4:*** This input is from the ISA bus. It is used as a multiplexed pin with IRQ6 to the Viper Desktop Chipset.
IRQ6	43	I	***Interrupt Request Bit 6:*** This input is from the ISA bus. It is used as a multiplexed pin with IRQ4 to the Viper Desktop Chipset.
IRQ10	42	I	***Interrupt Request Bit 10:*** This input is from the ISA bus. It is used as a multiplexed pin with IRQ12 to the Viper Desktop Chipset.
IRQ12	39	I	***Interrupt Request Bit 12:*** This input is from the ISA bus. It is used as a multiplexed pin with IRQ10 to the Viper Desktop Chipset.
PIRQ[3:0]#	35:38	I	***PCI Interrupt Request Bits 3 through 0:*** These inputs are PCI interrupt requests. They are multiplexed internally and output to the Viper Desktop Chipset.
MIRQ4_6	68	O	***Multiplexed Interrupt Request Bit 4 and 6:*** This signal is the multiplexed output of IRQ4 and IRQ6. When LCLK is high, the output is IRQ4. When LCLK is low, the output is IRQ6. This output is demultiplexed in the Viper Desktop Chipset.
MIRQ10_12	69	O	***Multiplexed Interrupt Request Bit 10 and 12:*** This signal is the multiplexed output of IRQ10 and IRQ12. When LCLK is high, the output is IRQ10. When LCLK is low, the output is IRQ12. This output is demultiplexed in the Viper Desktop Chipset.
MPIRQ0#_1#	70	O	***Multiplexed PCl Interrupt Request Bit 0 and 1:*** This signal is the multiplexed output of PIRQ0# and PIRQ1#. When LCLK is high, the output is PIRQ0#. When LCLK is low, the output is PIRQ1#. This output is demultiplexed in the Viper Desktop Chipset.

Viper DTA Mode Signal Descriptions (cont.)

Signal Name	Pin No.	Signal Type	Signal Description
MPIRQ2#_3#	73	O	***Multiplexed PCI Interrupt Request Bit 2 and 3:*** This signal is the multiplexed output of PIRQ2# and PIRQ3#. When LCLK is high, the output is PIRQ2#. When LCLK is low, the output is PIRQ3. This output is demultiplexed in the Viper Desktop Chipset.

3.4.3 ISA DMA Arbiter Interface Signals

Signal Name	Pin No.	Signal Type	Signal Description
DRQ[7:5] DRQ3, DRQ1, DRQ0	29:31, 32, 33, 34	I	***DMA Request bits 7 through 5, 3, 1, and 0:*** These inputs are DMA request signals directly from the ISA bus. They are internally multiplexed and output to the Viper Desktop Chipset.
DREQ3_7	49	O	***DMA Request Bit 3 and 7:*** This output is the multiplexed output of DMA request 3 and 7. When LCLK is high, the output is DREQ3. When LCLK is low, the output is DREQ7. This output is demultiplexed in the Viper Desktop Chipset.
DREQ1_6	77	O	***DMA Request Bit 1 and 6:*** This output is the multiplexed output of DMA request 1 and 6. When LCLK is high, the output is DREQ1. When LCLK is low, the output is DREQ6. This output is demultiplexed in the Viper Desktop Chipset.
DREQ0_5	74	O	***DMA Request Bit 0 and 5:*** This output is the multiplexed output of DMA request 0 and 5. When LCLK is high, the output is DREQ0. When LCLK is low, the output is DREQ5. This output is demultiplexed in the Viper Desktop Chipset.
DACK[7:0]#	47, 13:8	O	***DMA Acknowledge Bits 7 through 0:*** These output signals are directly connected to the ISA bus. They are derived from the EDACK[2:0] and EDACKEN inputs from the Viper Desktop Chipset.
EDACK[2:0]	18, 98, 87	I	***Encoded DMA Acknowledge Bits 2 through 0:*** These encoded inputs give a 3-to-8 decode for the DMA acknowledge.
EDACKEN	50	I	***Encoded DMA Acknowledge Enable:*** This active high input enables the DACKs to be decoded. **Note:** The EDACKEN signal from the Viper Desktop Chipset is active low and therefore it needs to be inverted before coming to the 82C602A.

3.4.4 Data Bus and Control Interface Signals

Signal Name	Pin No.	Signal Type	Signal Description
SD[7:0]	86:79	I/O	***System Data AT Bus Lines 7 through 0***
XD[7:0]	97:92, 89, 88	I/O	***XD Bus Data Lines 7 through 0:*** XD7, XD6, and XD4 must be sampled low during reset to enter the Viper DTA Mode. A 2.2K pull-down resistor is recommended on these lines. All XD lines in the 82C602A have internal weak pull-up resistors and do not require any external pull-up resistors.

Viper DTA Mode Signal Descriptions (cont.)

Signal Name	Pin No.	Signal Type	Signal Description
XDIR	72	I	***XD Bus Direction:*** A direction control signal for the SD bus to/from the XD bus.
ATTRIS#	22	I	***Tristate XD Buffer Control:*** When this signal is asserted, it allows the XD bus buffer to transfer data between (to or from) the XD to the SD bus. When negated, it will not allow any transfers to or from the XD/SD bus.
CLRIN	4	I	***Clear Input Pin:*** This input clears the flip flops which control the general purpose output pins GPOUT3 and GPOUT4.

3.4.5 Power Management Interface Signals and General Purpose Logic

Signal Name	Pin No.	Signal Type	Signal Description
PPWRL#	51	I	***Peripheral Power Latch Control:*** This input from the Viper Desktop Chipset will latch power control information. The Viper Desktop Chipset puts out the power control information on the SD bus and that information is latched into the power control latch by this signal.
PPWR[5:0]	64:59	O	***Peripheral Power Latches 5 through 0:*** These six outputs are the power control signals used to put the system into a low power state.
GPOUT[5:1]	67, 48, 65, 16, 19	O	***General Purpose Outputs 5 through 1:*** These five output signals are a function of the GPIN pins and the SEL[5:1] inputs. (Refer to the schematics in Section 4.0.)
GPIN[4:1]	2, 1, 100, 99	I	***General Purpose Inputs 4 through 1:*** These four input signals along with the SEL[5: 1] inputs determine the output on the GPOUT pins. (Refer to the schematics in Section 4.0.)
SEL[5:1]	20, 46, 45, 58, 7	I	***Selection bits 5 through 1:*** The SEL[5:1] inputs along with the GPIN[4:1] inputs determine the output on the GPOUT pins. (Refer to the schematics in Section 4.0.)
CLKIN1	5	I	***Clock Input 1:*** This input pin will clock the GPOUT1 signal (pin 19) and output the GPOUT3 signal (pin 65).
CLKIN2	6	I	***Clock Input 2:*** This input pin will clock the GPOUT5 signal (pin 67) and output the GPOUT4 signal (pin 48).

3.4.6 Real-Time Clock Interface Signals

Signal Name	Pin No.	Signal Type	Signal Description
RTCRD#	25	I	***Real-time Clock Read Command:*** This is the data strobe input. The falling edge of this strobe is used to enable the outputs during a read cycle.
RTCWR#	27	I	***Real-time Clock Write Command:*** The rising edge of this input latches data in the internal real-time clock.
RTCAS	26	I	***Real-time Clock Address Strobe:*** RTCAS is used to demultiplex the address/data bus. The falling edge of AS latches the address on XD[7:0].
RTC_5V	57	I	***Real-time Clock 5.0V:*** This pin must be connected to +5V. This input will prevent the lithium battery from being accessed during power-on.

Viper DTA Mode Signal Descriptions (cont.)

Signal Name	Pin No.	Signal Type	Signal Description
VBATT	55	I	***Voltage Battery:*** This pin is connected to the CMOS and RTC battery. This input pin should be connected to a 3 volt lithium battery.
XTALIN	53	I	***Crystal Oscillator Input:*** 32.768KHz XTAL input.
XTALOUT	54	O	***Crystal Oscillator Output:*** 32.768KHz XTAL output.
IRQ8#	56	O	***Interrupt Request Bit 8:*** The alarm output interrupt generated by the internal RTC.

3.4.7 Power and Ground Pins

Signal Name	Pin No.	Signal Type	Signal Description
VCC	14, 41, 71, 91	P	***Power Connection***
GND	3, 15, 28, 40, 52, 66, 78, 90	G	***Ground Connection***

Legend:

G	Ground
I/O	Input/Output
G	Ground
OD	Open Drain
I/O	Input/Output
P	Power
Sch	Schmitt-trigger

Figure 3-6 Viper DTB Mode Pin Diagram (100-Pin PQFP)

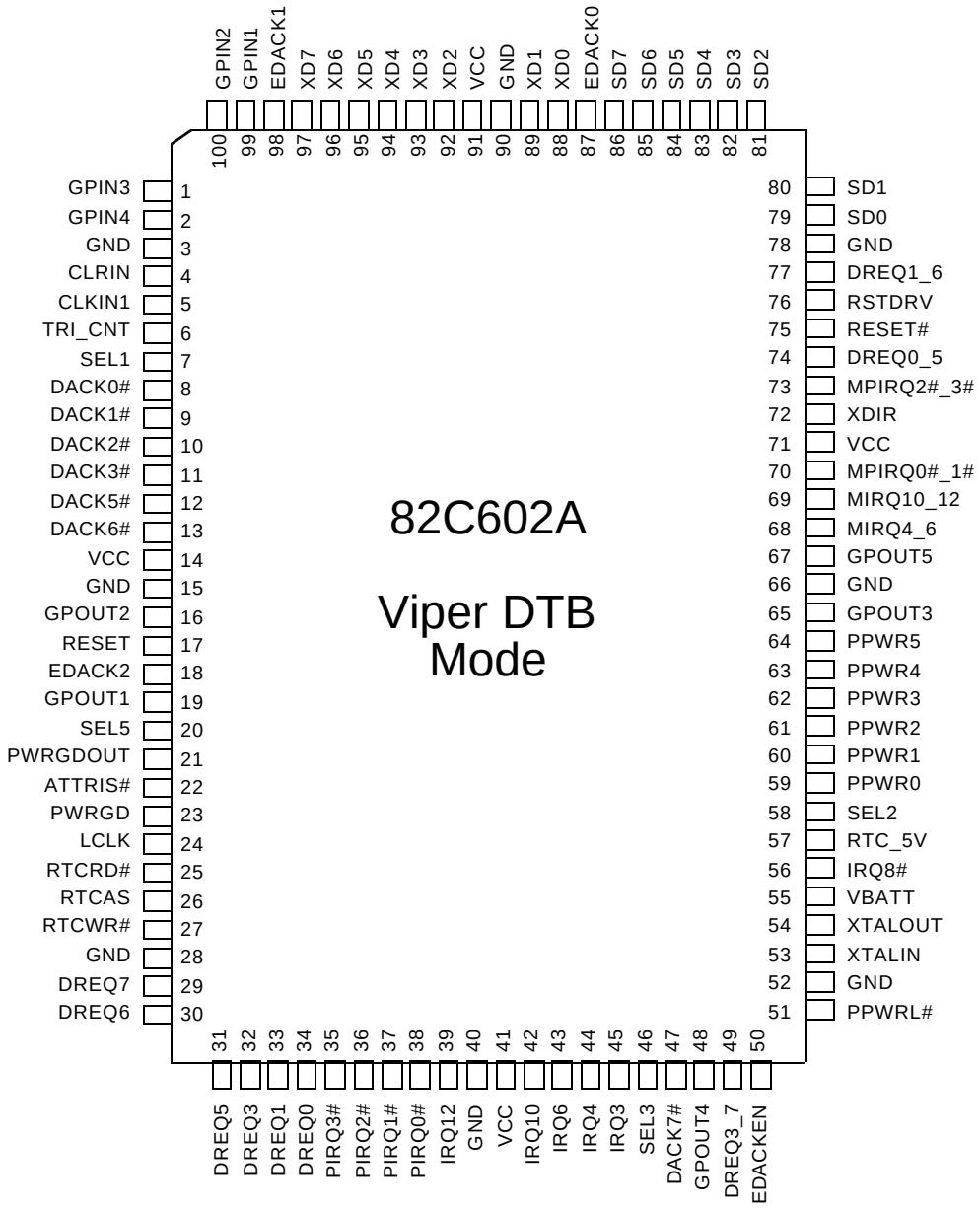

Table 3-9 Viper DTB Mode - Numerical Pin Cross-Reference List

Pin #	Pin Name	Pin Type	Pin #	Pin Name	Pin Type	Pin #	Pin Name	Pin Type	Pin #	Pin Name	Pin Type
1	GPIN3	I	26	RTCAS	I	51	PPWRL#	I	76	RSTDRV	O
2	GPIN4	I	27	RTCWR#	I	52	GND	G	77	DREQ1_6	O
3	GND	G	28	GND	G	53	XTALIN	I	78	GND	G
4	CLRIN	I	29	DREQ7	I	54	XTALOUT	O	79	SD0	I/O
5	CLKIN1	I	30	DREQ6	I	55	VBATT	I	80	SD1	I/O
6	TRI_CNT	I	31	DREQ5	I	56	IRQ8#	O	81	SD2	I/O
7	SEL1	I	32	DREQ3	I	57	RTC_5V	I	82	SD3	I/O
8	DACK0#	O	33	DREQ1	I	58	SEL2	I	83	SD4	I/O
9	DACK1#	O	34	DREQ0	I	59	PPWR0	O	84	SD5	I/O
10	DACK2#	O	35	PIRQ3#	I	60	PPWR1	O	85	SD6	I/O
11	DACK3#	O	36	PIRQ2#	I	61	PPWR2	O	86	SD7	I/O
12	DACK5#	O	37	PIRQ1#	I	62	PPWR3	O	87	EDACK0	I
13	DACK6#	O	38	PIRQ0#	I	63	PPWR4	O	88	XD0	I/O
14	VCC	P	39	IRQ12	I	64	PPWR5	O	89	XD1	I/O
15	GND	G	40	GND	G	65	GPOUT3	O	90	GND	G
16	GPOUT2	O	41	VCC	P	66	GND	G	91	VCC	P
17	RESET	I	42	IRQ10	I	67	GPOUT5	O	92	XD2	I/O
18	EDACK2	I	43	IRQ6	I	68	MIRQ4_6	O	93	XD3	I/O
19	GPOUT1	O	44	IRQ4	I	69	MIRQ10_12	O	94	XD4	I/O
20	SEL5	I	45	SEL3	I	70	MPIRQ0#_1#	O	95	XD5	I/O
21	PWRGDOUT	O(OD)	46	SEL4	I	71	VCC	P	96	XD6	I/O
22	ATTRIS#	I	47	DACK7#	O	72	XDIR	I	97	XD7	I/O
23	PWRGD	I-S	48	GPOUT4	O	73	MPIRQ2#_3#	O	98	EDACK1	I
24	LCLK	I	49	DREQ3_7	O	74	DREQ0_5	O	99	GPIN1	I
25	RTCRD#	I	50	EDACKEN	I	75	RESET#	O	100	GPIN2	I

Table 3-10 Viper DTB Mode - Alphabetical Pin Cross-Reference List

Pin Name	Pin #	Pin Type	Pin Name	Pin #	Pin Type	Pin Name	Pin #	Pin Type	Pin Name	Pin #	Pin Type
ATTRIS#	22	I	GND	28	G	PIRQ0#	38	I	SD5	84	I/O
CLKIN1	5	I	GND	40	G	PIRQ1#	37	I	SD6	85	I/O
CLRIN	4	I	GND	52	G	PIRQ2#	36	I	SD7	86	I/O
DACK0#	8	O	GND	66	G	PIRQ3#	35	I	SEL1	7	I
DACK1#	9	O	GND	78	G	PPWR0	59	O	SEL2	58	I
DACK2#	10	O	GND	90	G	PPWR1	60	O	SEL3	45	I
DACK3#	11	O	GPIN1	99	I	PPWR2	61	O	SEL4	46	I
DACK5#	12	O	GPIN2	100	I	PPWR3	62	O	SEL5	20	I
DACK6#	13	O	GPIN3	1	I	PPWR4	63	O	TRI_CNT	6	I
DACK7#	47	O	GPIN4	2	I	PPWR5	64	O	VBATT	55	I
DREQ0	34	I	GPOUT1	19	O	PPWRL#	51	I	VCC	14	P
DREQ0_5	74	O	GPOUT2	16	O	PWRGD	23	I-S	VCC	41	P
DREQ1	33	I	GPOUT3	65	O	PWRGDOUT	21	O(OD)	VCC	71	P
DREQ1_6	77	O	GPOUT4	48	O	RESET	17	I	VCC	91	P
DREQ3	32	I	GPOUT5	67	O	RESET#	75	O	XD0	88	I/O
DREQ3_7	49	O	IRQ4	44	I	RSTDRV	76	O	XD1	89	I/O
DREQ5	31	I	IRQ6	43	I	RTC_5V	57	I	XD2	92	I/O
DREQ6	30	I	IRQ8#	56	O	RTCRD#	25	I	XD3	93	I/O
DREQ7	29	I	IRQ10	42	I	RTCAS	26	I	XD4	94	I/O
EDACK0	87	I	IRQ12	39	I	RTCWR#	27	I	XD5	95	I/O
EDACK1	98	I	LCLK	24	I	SD0	79	I/O	XD6	96	I/O
EDACK2	18	I	MIRQ4_6	68	O	SD1	80	I/O	XD7	97	I/O
EDACKEN	50	I	MIRQ10_12	69	O	SD2	81	I/O	XDIR	72	I
GND	3	G	MPIRQ0#_1#	70	O	SD3	82	I/O	XTALIN	53	I
GND	15	G	MPIRQ2#_3#	73	O	SD4	83	I/O	XTALOUT	54	O

3.5 Viper DTB Mode Signal Descriptions

Refer to the Viper DTB internal circuitry schematic in Section 4.0 for complete details.

3.5.1 Clock and Reset Interface Signals

Signal Name	Pin No.	Signal Type	Signal Description
RESET	17	I	***Reset:*** Reset input from the Viper Desktop Chipset.
RESET#	75	O	***Reset:*** The inverted output of pin 17. This signal is also used to reset the internal real-time clock.
RSTDRV	76	O	***Reset Drive:*** This signal is the buffered output of pin 17 and is an active high reset output to the AT bus.
LCLK	24	I	***Local Bus Clock:*** The Viper Desktop Chipset demultiplexes its multiplexed signals based on either the LCLK or the 14.318MHz clock. This input to the 82C602A goes to the select input of the multiplexers internal to the 82C602A and is used to multiplex the IRQs and DREQs to the Viper Desktop Chipset.
PWRGD	23	I-Sch	***Power Good:*** The PWRGD input signal from the power supply.
PWRGDOUT	21	O (OD)	***Power Good Output:*** An open drain output signal to the Viper Desktop Chipset.

3.5.2 Interrupt/Control Interface Signals

Signal Name	Pin No.	Signal Type	Signal Description
IRQ4	44	I	***Interrupt Request Bit 4:*** This input is from the ISA bus. It is used as a multiplexed pin with IRQ6 to the Viper Desktop Chipset.
IRQ6	43	I	***Interrupt Request Bit 6:*** This input is from the ISA bus. It is used as a multiplexed pin with IRQ4 to the Viper Desktop Chipset.
IRQ10	42	I	***Interrupt Request Bit 10:*** This input is from the ISA bus. It is used as a multiplexed pin with IRQ12 to the Viper Desktop Chipset.
IRQ12	39	I	***Interrupt Request Bit 12:*** This input is from the ISA bus. It is used as a multiplexed pin with IRQ10 to the Viper Desktop Chipset.
PIRQ[3:0]#	35:38	I	***PCI Interrupt Request Bits 3 through 0:*** These inputs are PCI interrupt requests. They are multiplexed internally and output to the Viper Desktop Chipset.
MIRQ4_6	68	O	***Multiplexed Interrupt Request Bit 4 and 6:*** This signal is the multiplexed output of IRQ4 and IRQ6. When LCLK is high, the output is IRQ4. When LCLK is low, the output is IRQ6. This output is demultiplexed in the Viper Desktop Chipset.
MIRQ10_12	69	O	***Multiplexed Interrupt Request Bit 10 and 12:*** This signal is the multiplexed output of IRQ10 and IRQ12. When LCLK is high, the output is IRQ10. When LCLK is low, the output is IRQ12. This output is demultiplexed in the Viper Desktop Chipset.
MPIRQ0#_1#	70	O	***Multiplexed PCl Interrupt Request Bit 0 and 1:*** This signal is the multiplexed output of PIRQ0# and PIRQ1#. When LCLK is high, the output is PIRQ0#. When LCLK is low, the output is PIRQ1#. This output is demultiplexed in the Viper Desktop Chipset.

Viper DTB Mode Signal Descriptions (cont.)

Signal Name	Pin No.	Signal Type	Signal Description
MPIRQ2#_3#	73	O	***Multiplexed PCI Interrupt Request Bit 2 and 3:*** This signal is the multiplexed output of PIRQ2# and PIRQ3#. When LCLK is high, the output is PIRQ2#. When LCLK is low, the output is PIRQ3. This output is demultiplexed in the Viper Desktop Chipset.

3.5.3 ISA DMA Arbiter Interface Signals

Signal Name	Pin No.	Signal Type	Signal Description
DRQ[7:5] DRQ3, DRQ1, DRQ0	29:31, 32, 33, 34	I	***DMA Request bits 7 through 5, 3, 1, and 0:*** These inputs are DMA request signals directly from the ISA bus. They are internally multiplexed and output to the Viper Desktop Chipset.
DREQ3_7	49	O	***DMA Request Bit 3 and 7:*** This output is the multiplexed output of DMA request 3 and 7. When LCLK is high, the output is DREQ3. When LCLK is low, the output is DREQ7. This output is demultiplexed in the Viper Desktop Chipset.
DREQ1_6	77	O	***DMA Request Bit 1 and 6:*** This output is the multiplexed output of DMA request 1 and 6. When LCLK is high, the output is DREQ1. When LCLK is low, the output is DREQ6. This output is demultiplexed in the Viper Desktop Chipset.
DREQ0_5	74	O	***DMA Request Bit 0 and 5:*** This output is the multiplexed output of DMA request 0 and 5. When LCLK is high, the output is DREQ0. When LCLK is low, the output is DREQ5. This output is demultiplexed in the Viper Desktop Chipset.
DACK[7:0]#	47, 13:8	O	***DMA Acknowledge Bits 7 through 0:*** These output signals are directly connected to the ISA bus. They are derived from the EDACK[2:0] and EDACKEN inputs from the Viper Desktop Chipset.
EDACK[2:0]	18, 98, 87	I	***Encoded DMA Acknowledge Bits 2 through 0:*** These encoded inputs give a 3-to-8 decode for the DMA acknowledge.
EDACKEN	50	I	***Encoded DMA Acknowledge Enable:*** This active high input enables the DACKs to be decoded. **Note:** The EDACKEN signal from the Viper Desktop Chipset is active low and therefore it needs to be inverted before coming to the 82C602A.

3.5.4 Data Bus and Control Interface Signals

Signal Name	Pin No.	Signal Type	Signal Description
SD[7:0]	86:79	I/O	***System Data AT Bus Lines 7 through 0***
XD[7:0]	97:92, 89, 88	I/O	***XD Bus Data Lines 7 through 0:*** XD7, XD6, XD5, and XD4 must be sampled low during reset to enter the Viper DTB Mode. A 2.2K pull-down resistor is recommended on these lines. All XD lines in the 82C602A have internal weak pull-up resistors and do not require any external pull-up resistors.

Viper DTB Mode Signal Descriptions (cont.)

Signal Name	Pin No.	Signal Type	Signal Description
XDIR	72	I	***XD Bus Direction:*** A direction control signal for the SD bus to/from the XD bus.
ATTRIS#	22	I	***Tristate XD Buffer Control:*** When this signal is asserted, it allows the XD bus buffer to transfer data between (to or from) the XD to the SD bus. When negated, it will not allow any transfers to or from the XD/SD bus.
CLRIN	4	I	***Clear Input Pin:*** This input clears the flip flops which control the general purpose output pins GPOUT3 and GPOUT4.

3.5.5 Power Management Interface Signals and General Purpose Logic

Signal Name	Pin No.	Signal Type	Signal Description
PPWRL#	51	I	***Peripheral Power Latch Control:*** This input from the Viper Desktop Chipset will latch power control information. The Viper Desktop Chipset puts out the power control information on the SD bus and that information is latched into the power control latch by this signal.
PPWR[5:0]	64:59	O	***Peripheral Power Latches 5 through 0:*** These six outputs are the power control signals used to put the system into a low power state.
TRI_CNT	6	I	***Tristate Control for GPOUT3 and GPOUT4:*** This signal, when low, will allow latched information to be output on the GPOUT3 and GPOUT4 outputs. When high, it tristates these outputs.
GPOUT[5:1]	67, 48, 65, 16, 19	O	***General Purpose Outputs 5 through 1:*** These five output signals are a function of the GPIN pins and the SEL[5:1] inputs. (Refer to the schematics in Section 4.0.)
GPIN[4:1]	2, 1, 100, 99	I	***General Purpose Inputs 4 through 1:*** These four input signals along with the SEL[5: 1] inputs determine the output on the GPOUT pins. (Refer to the schematics in Section 4.0.)
SEL[5:1]	20, 46, 45, 58, 7	I	***Selection bits 5 through 1:*** The SEL[5:1] inputs along with the GPIN[4:1] inputs determine the output on the GPOUT pins. (Refer to the schematics in Section 4.0.)
CLKIN1	5	I	***Clock Input 1:*** This input pin will clock the GPOUT1 signal (pin 19) and output the GPOUT3 signal (pin 65).

3.5.6 Real-Time Clock Interface Signals

Signal Name	Pin No.	Signal Type	Signal Description
RTCRD#	25	I	***Real-time Clock Read Command:*** This is the data strobe input. The falling edge of this strobe is used to enable the outputs during a read cycle.
RTCWR#	27	I	***Real-time Clock Write Command:*** The rising edge of this input latches data in the internal real-time clock.
RTCAS	26	I	***Real-time Clock Address Strobe:*** RTCAS is used to demultiplex the address/data bus. The falling edge of AS latches the address on XD[7:0].

Viper DTB Mode Signal Descriptions (cont.)

Signal Name	Pin No.	Signal Type	Signal Description
RTC_5V	57	I	***Real-time Clock 5.0V:*** This pin must be connected to +5V. This input will prevent the lithium battery from being accessed during power-on.
VBATT	55	I	***Voltage Battery:*** This pin is connected to the CMOS and RTC battery. This input pin should be connected to a 3 volt lithium battery.
XTALIN	53	I	***Crystal Oscillator Input:*** 32.768KHz XTAL input.
XTALOUT	54	O	***Crystal Oscillator Output:*** 32.768KHz XTAL output.
IRQ8#	56	O	***Interrupt Request Bit 8:*** The alarm output interrupt generated by the internal RTC.

3.5.7 Power and Ground Pins

Signal Name	Pin No.	Signal Type	Signal Description
VCC	14, 41, 71, 91	P	***Power Connection***
GND	3, 15, 28, 40, 52, 66, 78, 90	G	***Ground Connection***

Legend:

G	Ground
I/O	Input/Output
G	Ground
OD	Open Drain
I/O	Input/Output
P	Power
Sch	Schmitt-trigger

Figure 3-7 Viper NBA Mode Pin Diagram (100-Pin PQFP)

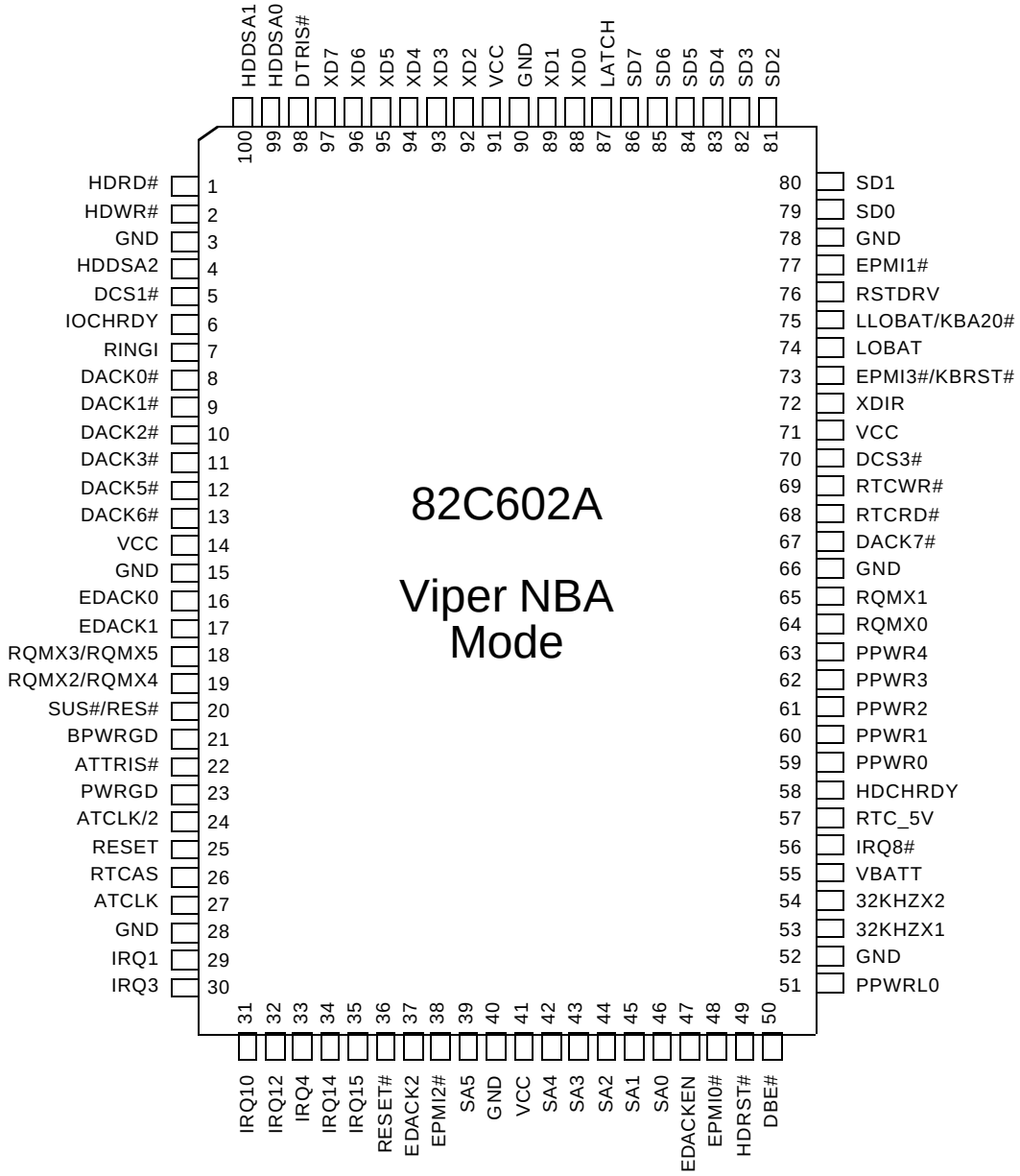

Figure 3-8 Viper NBA Mode Pin Diagram (100-Pin TQFP)

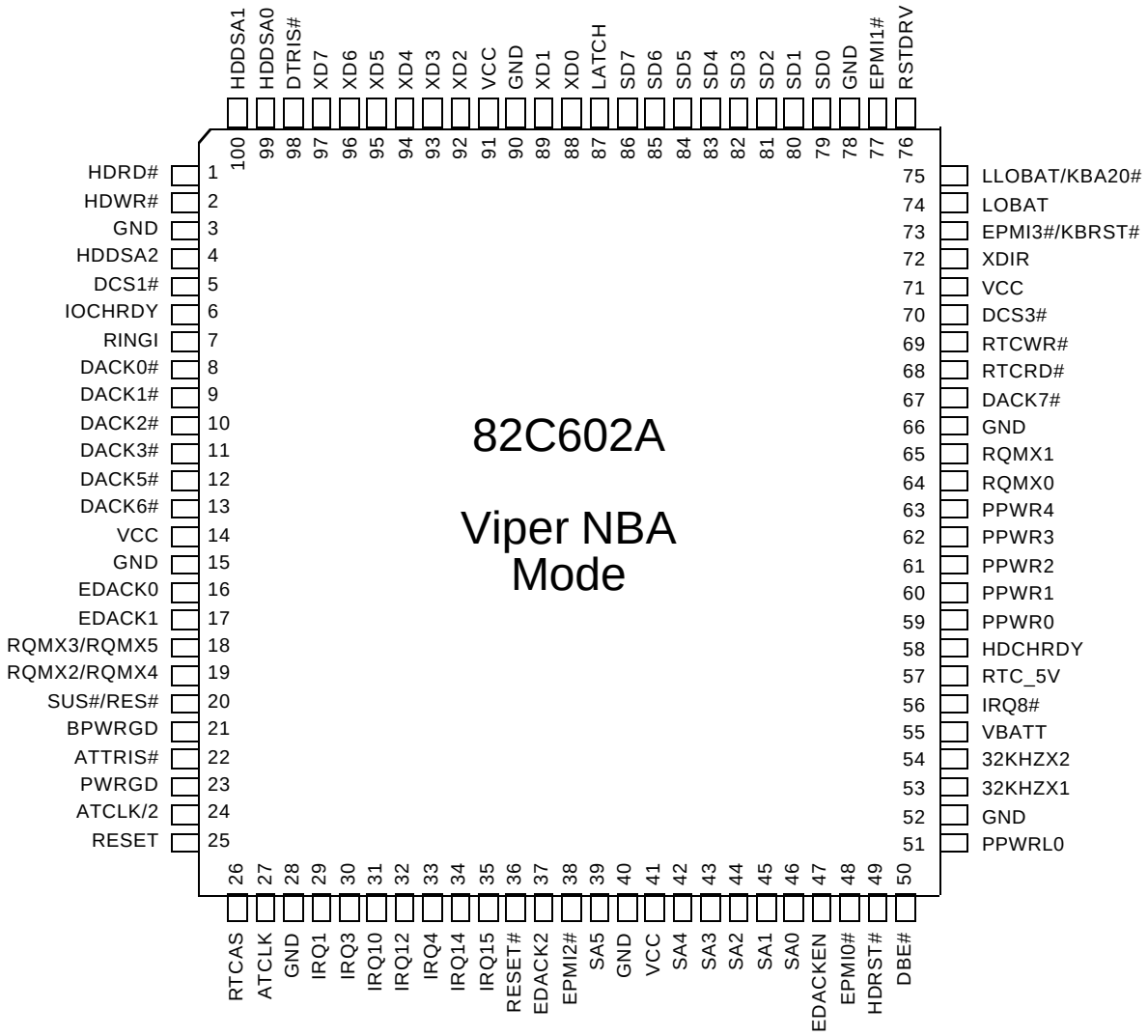

Table 3-11 Viper NBA Mode - Numerical Pin Cross-Reference List

Pin #	Pin Name	Pin Type	Pin #	Pin Name	Pin Type	Pin #	Pin Name	Pin Type	Pin #	Pin Name	Pin Type
1	HDRD#	O	26	RTCAS	I	51	PPWRL0	I	76	RSTDRV	O
2	HDWR#	O	27	ATCLK	I	52	GND	G	77	EPMI1#	I
3	GND	G	28	GND	G	53	32KHZX1	I	78	GND	G
4	HDDSA2	O	29	IRQ1	I	54	32KHZX2	O	79	SD0	I/O
5	DCS1#	O	30	IRQ3	I	55	VBATT	I	80	SD1	I/O
6	IOCHRDY	O	31	IRQ10	I	56	IRQ8#	O(OD)	81	SD2	I/O
7	RINGI	I	32	IRQ12	I	57	RTC_5V	I	82	SD3	I/O
8	DACK0#	O	33	IRQ4	I	58	HDCHRDY	I	83	SD4	I/O
9	DACK1#	O	34	IRQ14	I	59	PPWR0	O	84	SD5	I/O
10	DACK2#	O	35	IRQ15	I	60	PPWR1	O	85	SD6	I/O
11	DACK3#	O	36	RESET#	O	61	PPWR2	O	86	SD7	I/O
12	DACK5#	O	37	EDACK2	I	62	PPWR3	O	87	LATCH	I
13	DACK6#	O	38	EPMI2#	I	63	PPWR4	O	88	XD0	I/O
14	VCC	P	39	SA5	I	64	RQMX0	O	89	XD1	I/O
15	GND	G	40	GND	G	65	RQMX1	O	90	GND	G
16	EDACK0	I	41	VCC	P	66	GND	G	91	VCC	P
17	EDACK1	I	42	SA4	I	67	DACK7#	O	92	XD2	I/O
18	RQMX3/RQMX5	O	43	SA3	I	68	RTCRD#	I	93	XD3	I/O
19	RQMX2/RQMX4	O	44	SA2	I	69	RTCWR#	I	94	XD4	I/O
20	SUS#/RES#	I	45	SA1	I	70	DCS3#	O	95	XD5	I/O
21	BPWRGD	O(OD)	46	SA0	I	71	VCC	P	96	XD6	I/O
22	ATTRIS#	I	47	EDACKEN	I	72	XDIR	I	97	XD7	I/O
23	PWRGD	I-Sch	48	EPMI0#	I	73	EPMI3#/KBRST#	I	98	DTRIS#	I
24	ATCLK/2	I	49	HDRST#	O	74	LOBAT	I	99	HDDSA0	O
25	RESET	I	50	DBE#	I	75	LLOBAT/KBA20#	I	100	HDDSA1	O

Table 3-12 Viper NBA Mode - Alphabetical Pin Cross-Reference List

Pin Name	Pin #	Pin Type	Pin Name	Pin #	Pin Type	Pin Name	Pin #	Pin Type	Pin Name	Pin #	Pin Type
ATCLK	27	I	GND	28	G	PPWR0	59	O	SD0	79	I/O
ATCLK/2	24	I	GND	40	G	PPWR1	60	O	SD1	80	I/O
ATTRIS#	22	I	GND	52	G	PPWR2	61	O	SD2	81	I/O
BPWRGD	21	O(OD)	GND	66	G	PPWR3	62	O	SD3	82	I/O
DACK0#	8	O	GND	78	G	PPWR4	63	O	SD4	83	I/O
DACK1#	9	O	GND	90	G	PPWRL0	51	I	SD5	84	I/O
DACK2#	10	O	HDCHRDY	58	I	PWRGD	23	I-Sch	SD6	85	I/O
DACK3#	11	O	HDDSA0	99	O	RESET	25	I	SD7	86	I/O
DACK5#	12	O	HDDSA1	100	O	RESET#	36	O	SUS#/RES#	20	I
DACK6#	13	O	HDDSA2	4	O	RINGI	7	I	VBATT	55	I
DACK7#	67	O	HDRD#	1	O	RQMX0	64	O	VCC	14	P
DBE#	50	I	HDRST#	49	O	RQMX1	65	O	VCC	41	P
DCS1#	5	O	HDWR#	2	O	RQMX2/RQMX4	19	O	VCC	71	P
DCS3#	70	O	IOCHRDY	6	O	RQMX3/RQMX5	18	O	VCC	91	P
DTRIS#	98	I	IRQ1	29	I	RSTDRV	76	O	XD0	88	I/O
EDACK0	16	I	IRQ3	30	I	RTCAS	26	I	XD1	89	I/O
EDACK1	17	I	IRQ4	33	I	RTC_5V	57	I	XD2	92	I/O
EDACK2	37	I	IRQ8#	56	O(OD)	RTCRD#	68	I	XD3	93	I/O
EDACKEN	47	I	IRQ10	31	I	RTCWR#	69	I	XD4	94	I/O
EPMI0#	48	I	IRQ12	32	I	SA0	46	I	XD5	95	I/O
EPMI1#	77	I	IRQ14	34	I	SA1	45	I	XD6	96	I/O
EPMI2#	38	I	IRQ15	35	I	SA2	44	I	XD7	97	I/O
EPMI3#/KBRST#	73	I	LATCH	87	I	SA3	43	I	XDIR	72	I
GND	3	G	LLOBAT/KBA20#	75	I	SA4	42	I	32KHZX1	53	I
GND	15	G	LOBAT	74	I	SA5	39	I	32KHZX2	54	O

3.6 Viper NBA Mode Signal Descriptions

Refer to the Viper NBA internal circuitry schematic in Section 4.0 for complete details.

3.6.1 Clock and Reset Interface Signals

Signal Name	Pin No.	Signal Type	Signal Description
RESET	25	I	***Reset:*** Reset input from the Viper Notebook Chipset.
RESET#	36	O	***Reset:*** The inverted output of RESET (pin 25). This signal is also used to reset the internal real-time clock.
RSTDRV	76	O	***Reset Drive:*** An active high reset output to the AT bus.
PWRGD	23	I-Sch	***Power Good:*** The PWRGD input signal from the power supply. A rising edge on this input is used to sample the strap information.
BPWRGD	21	O (OD)	***Buffered Power Good:*** An open drain output signal to the Viper Notebook Chipset.

3.6.2 Interrupt Control Interface Signals

Signal Name	Pin No.	Signal Type	Signal Description
IRQ1, IRQ3, IRQ10, IRQ12	29, 30, 31, 32	I	***Interrupt Request bits 1, 3, 10, and 12:*** Interrupt request inputs from the ISA bus. These inputs are output serially to the Viper Notebook Chipset on RQMX0. A low pulse on any of these inputs is internally extended by one ATCLK.
IRQ4, IRQ14, IRQ15	33, 34, 35	I	***Interrupt Request bits 4, 14, and 15:*** Interrupt request inputs from the ISA bus. These inputs are output serially to the Viper Notebook Chipset along with IRQ8# on RQMX1. A low pulse on any of these inputs is internally extended by one ATCLK.
RQMX[1:0]	65, 64	O	***Serial Outputs 1 and 0:*** These outputs are sent to the Viper Notebook Chipset. The Viper Notebook Chipset will demultiplex these lines to decode interrupt and power management information.

3.6.3 ISA DMA Arbiter Interface Signals

Signal Name	Pin No.	Signal Type	Signal Description
DACK[7:0]#	67, 13:8	O	***DMA Acknowledge bits 7 through 0:*** These output signals are directly connected to the ISA bus. They are derived from the EDACK[2:0] and EDACKEN inputs from the Viper Notebook Chipset.
EDACK[2:0]	37, 17, 16	I	***Encoded DMA Acknowledge bits 2 through 0:*** These encoded inputs give a 3-to-8 decode for the DMA acknowledge.
EDACKEN	47	I	***Encoded DMA Acknowledge Enable:*** This active high input allows the DACKs to be decoded.

Viper NBA Mode Signal Descriptions (cont.)

3.6.4 Data Bus and Control Interface Signals

Signal Name	Pin No.	Signal Type	Signal Description
SD[7:0]	86:79	I/O	***System Data AT Bus Lines 7 through 0***
XD[7:0]	97:92, 89, 88	I/O	***XD Bus Data Lines 7 through 0:*** XD4 and XD0 must be sampled low driving reset to enter the Viper NBA Mode. A 4.7K pull-down resistor is recommended on these lines. All the XD lines on the 82C602A have internal pull-up resistors and do not require any external pull-up resistors.
XDIR	72	I	***XD Bus Direction:*** A direction control signal for the SD bus to/from the XD bus.
ATTRIS#	22	I	***AT Tristate Control:*** When this signal is high, the 82C602A will drive the DACK lines; the SD-XD buffer is also enabled. When low, the DACK lines are tristated and so is the SD-XD buffer.

3.6.5 Power Management Interface Signals

Signal Name	Pin No.	Signal Type	Signal Description
DTRIS#	98	I	***Power Control Output Port Enable:*** This signal, when active, will tristate the power port. When disabled, it will allow output to the power port.
PPWRL0	51	I	***Peripheral Power Latch Control:*** This signal, when active, will latch the power control information on the SA bus and output it to the power control output pins.
PPWR[4:0]	63:59	O	***Peripheral Power Bits 4 through 0:*** These power control outputs can be used to control power to various peripherals.
SUS#/RES#	20	I	***Suspend / Resume:*** A power control input that is monitored by the Viper Notebook Chipset.
LOBAT	74	I	***Low Battery:*** A power control input that is monitored by the Viper Notebook Chipset.
LLOBAT/KBA20#	75	I	***Low Low Battery or Keyboard ControllerA20#:*** This input can be either LLOBAT (a power control input) or KBA20# from the keyboard controller. When the input is LLOBAT, pin 18 is RQMX3. If the input is KBA20#, pin 18 becomes RQMX5.
ATCLK	27	I	***AT Bus Clock:*** AT bus clock input from the Viper Notebook Chipset. This input along with ATCLK/2 will serially output interrupts and power management inputs to the Viper Notebook Chipset.
ATCLK/2	24	I	***AT Bus Clock Divide by 2:*** AT bus clock divide by 2 input from the Viper Notebook Chipset.
EPMI3#/KBRST#	73	I	***External Power Management Input Bit 3 or Keyboard Reset:*** This input can be either EPMI3# (power management input) or KBRST# from the keyboard controller. When the input is EPMI3#, pin 19 becomes RQMX2. When it is KBRST#, pin 19 becomes RQMX4.
EPMI[2:0]#	38, 77, 48	I	***External Power Management Input Bits 2 through 0:*** These three inputs and EPMI3# will signal the Viper Notebook Chipset that an external power management event has occurred.

Viper NBA Mode Signal Descriptions (cont.)

Signal Name	Pin No.	Signal Type	Signal Description
RINGI	7	I	***Ring Indicator:*** A power control input that is monitored by the Viper Notebook Chipset.
RQMX2/RQMX4	19	O	***Multiplexed Power Management Output:*** RQMX2/RQMX4 is a multiplexed output of RINGI, EPMI2#, EPMI3#/KBRST#, and LOBAT. These inputs are multiplexed using ATCLK and ATCLK/2.
RQMX3/RQMX5	18	O	***Multiplexed Power Management Output:*** RQMX3/RQMX5 is a multiplexed output of SUS#/RES#, EMPI0#, EPMI1#, and LLOBAT/KBA20#. These inputs are multiplexed using ATCLK and ATCLK/2.

3.6.6 Real-Time Clock Interface Signals

Signal Name	Pin No.	Signal (Drive) Type	Signal Description
RTCRD#	68	I	***Real-time Clock Read Command:*** This is the data strobe input. The falling edge of this strobe is used to enable the outputs during a read cycle.
RTCWR#	69	I	***Real-time Clock Write Command:*** The rising edge of this input latches data in the internal real-time clock.
RTCAS	26	I	***Real-time Clock Address Strobe:*** RTCAS is used to demultiplex the address/ data bus. The falling edge of AS latches the address on XD[7:0].
RTC_5V	57	I	***Real-time Clock 5.0V:*** This pin must be connected to +5V. This input will prevent the VBATT from being accessed during power-on.
VBATT	55	I	***Voltage Battery:*** This pin is connected to the CMOS and RTC battery.
IRQ8#	56	O (OD)	***Interrupt Request Bit 8:*** The alarm output interrupt generated by the internal real-time clock. This pin needs an external pull-up.
32KHZX1	53	I	***Crystal Oscillator Input:*** 32.768KHz XTAL input.
32HKZX2	54	O	***Crystal Oscillator Output:*** 32.768KHz XTAL output.

3.6.7 IDE Interface Signals

Signal Name	Pin No.	Signal Type	Signal Description
DBE#	50	I	***Data Buffer Enable:*** This signal, when active, will allow information to pass to the IDE drive.
DCS1#, DCS3#	5, 70	O	***Drive Chip Select 1 and 3:*** These chip select signals decoded from the host address bus are used to select the Command and Control Block Registers.
HDCHRDY	58	I	***Drive I/O Channel Ready:*** This signal is negated to extend the host transfer cycle of any host register access (read or write) when the drive is not ready to respond to a data transfer request. When HDCHRDY is not negated, HDCHRDY is in a high impedance state.
HDDSA[2:0]	4, 100, 99	O	***Drive Address Lines 2 through 0:*** This is the 3-bit binary coded address asserted by the host to access a register or data port in the drive.

Viper NBA Mode Signal Descriptions (cont.)

Signal Name	Pin No.	Signal Type	Signal Description
HDRD#	1	O	***Drive I/O Read:*** This is the read strobe signal. The low level of HDRD# enables data from a register or the data port of the drive onto the data bus.
HDRST#	49	O	***Drive Reset:*** This signal is asserted for at least 25msec after voltage levels have stabilized during power-on and negated thereafter unless some event requires that the drive(s) be reset following power-on.
HDWR#	2	O	***Drive I/O Write:*** This is the write strobe signal. The rising edge of DWR# samples data from the data bus into a register or the data port of the drive.
IOCHRDY	6	O	***I/O Channel Ready:*** This signal to the AT bus is used to extend the current cycle for non-zero wait state operations.
SA[5:0]	39, 42:46	I	***System Address Bus Lines 5 through 0:*** These AT bus address lines supply information to the IDE and power latch.
LATCH	87	I	***IDE Latch Enable:*** The input must be high if the internal buffer is used for IDE control. If IDE control is not obtained from the 82C602A, this input may be connected to PPWRL1 of the 82C558N IPC to obtain PPWR[13:8] on pins 5, 1, 2, 4,100, and 99 respectively.

3.6.8 Power and Ground Pins

Signal Name	Pin No.	Signal Type	Signal Description
VCC	14, 41, 71, 91	P	***Power Connection***
GND	3, 15, 28, 40, 52, 66, 78, 90	G	***Ground Connection***

Legend:

G	Ground
I/O	Input/Output
G	Ground
OD	Open Drain
I/O	Input/Output
P	Power
Sch	Schmitt-trigger

Figure 3-9 Viper NBB Mode Pin Diagram (100-Pin PQFP)

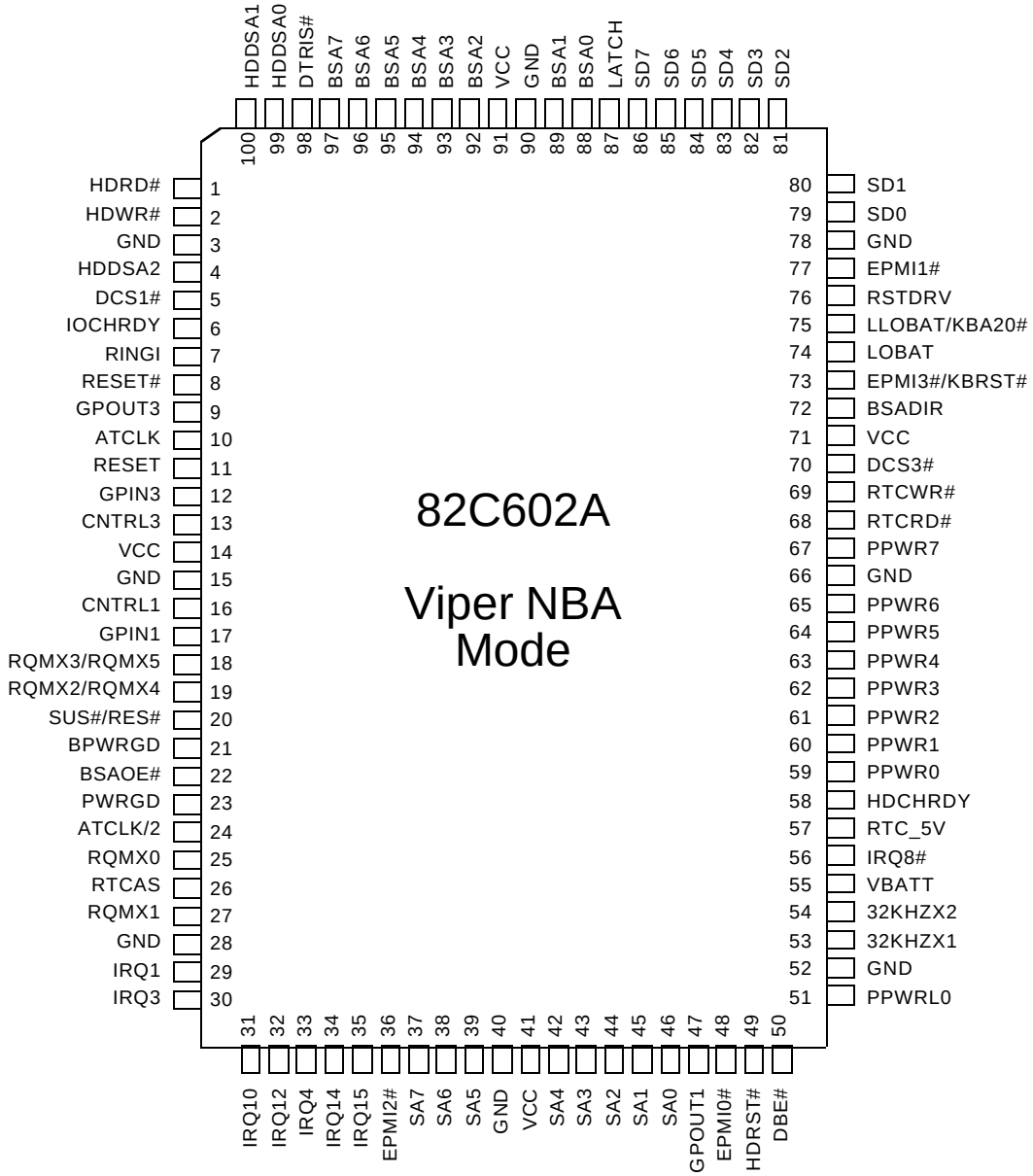

Figure 3-10 Viper NBB Mode Pin Diagram (100-Pin TQFP)

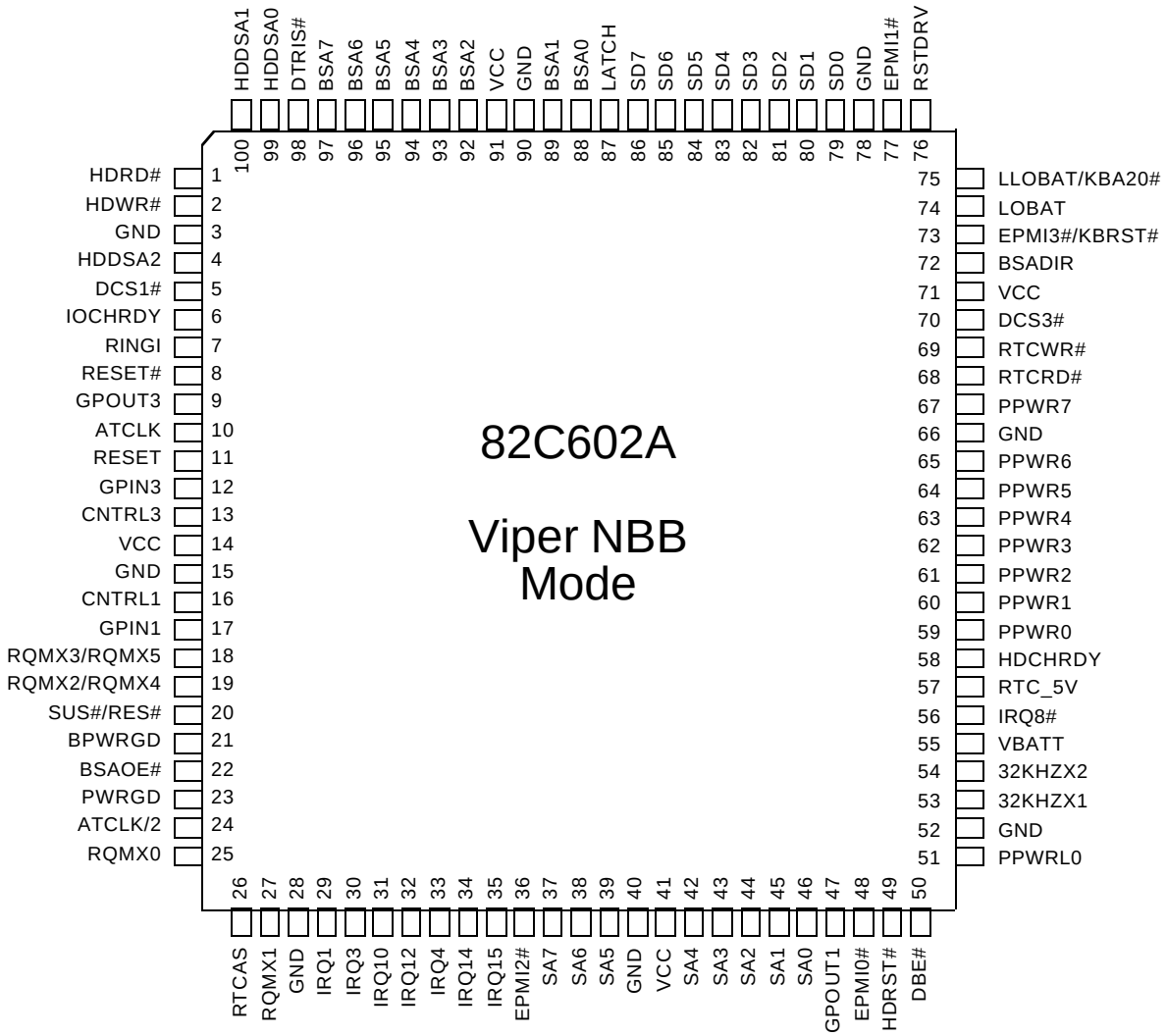

Table 3-13 Viper NBB Mode - Numerical Pin Cross-Reference List

Pin #	Pin Name	Pin Type	Pin #	Pin Name	Pin Type	Pin #	Pin Name	Pin Type	Pin #	Pin Name	Pin Type
1	HDRD#	O	26	RTCAS	I	51	PPWRL0	I	76	RSTDRV	O
2	HDWR#	O	27	RQMX1	O	52	GND	G	77	EPMI1#	I
3	GND	G	28	GND	G	53	32KHZX1	I	78	GND	G
4	HDDSA2	O	29	IRQ1	I	54	32KHZX2	O	79	SD0	I/O
5	DCS1#	O	30	IRQ3	I	55	VBATT	I	80	SD1	I/O
6	IOCHRDY	O	31	IRQ10	I	56	IRQ8#	O(OD)	81	SD2	I/O
7	RINGI	I	32	IRQ12	I	57	RTC_5V	I	82	SD3	I/O
8	RESET#	O	33	IRQ4	I	58	HDCHRDY	I	83	SD4	I/O
9	GPOUT3	O	34	IRQ14	I	59	PPWR0	O	84	SD5	I/O
10	ATCLK	I	35	IRQ15	I	60	PPWR1	O	85	SD6	I/O
11	RESET	I	36	EPMI2#	I	61	PPWR2	O	86	SD7	I/O
12	GPIN3	I	37	SA7	I/O	62	PPWR3	O	87	LATCH	I
13	CNTRL3	I	38	SA6	I/O	63	PPWR4	O	88	BSA0	I/O
14	VCC	P	39	SA5	I/O	64	PPWR5	O	89	BSA1	I/O
15	GND	G	40	GND	G	65	PPWR6	O	90	GND	G
16	CNTRL1	I	41	VCC	P	66	GND	G	91	VCC	P
17	GPIN1	I	42	SA4	I/O	67	PPWR7	O	92	BSA2	I/O
18	RQMX3/RQMX5	O	43	SA3	I/O	68	RTCRD#	I	93	BSA3	I/O
19	RQMX2/RQMX4	O	44	SA2	I/O	69	RTCWR#	I	94	BSA4	I/O
20	SUS#/RES#	I	45	SA1	I/O	70	DCS3#	O	95	BSA5	I/O
21	BPWRGD	O(OD)	46	SA0	I/O	71	VCC	P	96	BSA6	I/O
22	BSAOE#	I	47	GPOUT1	O	72	BSADIR	I	97	BSA7	I/O
23	PWRGD	I-Sch	48	EPMI0#	I	73	EPMI3#/KBRST#	I	98	DTRIS#	I
24	ATCLK/2	I	49	HDRST#	O	74	LOBAT	I	99	HDDSA0	O
25	RQMX0	O	50	DBE#	I	75	LLOBAT/KBA20#	I	100	HDDSA1	O

Table 3-14 Viper NBB Mode - Alphabetical Pin Cross-Reference List

Pin Name	Pin #	Pin Type	Pin Name	Pin #	Pin Type	Pin Name	Pin #	Pin Type	Pin Name	Pin #	Pin Type
ATCLK	27	I	GND	28	G	IRQ15	35	I	RTC_5V	57	I
ATCLK/2	24	I	GND	40	G	LATCH	87	I	SA0	46	I/O
BPWRGD	21	O(OD)	GND	52	G	LLOBAT/KBA20#	75	I	SA1	45	I/O
BSA0	88I	I/O	GND	66	G	LOBAT	74	I	SA2	44	I/O
BSA1	89	I/O	GND	78	G	PPWR0	59	O	SA3	43	I/O
BSA2	92	I/O	GND	90	G	PPWR1	60	O	SA4	42	I/O
BSA3	93	I/O	GPIN1	17	I	PPWR2	61	O	SA5	39	I/O
BSA4	94	I/O	GPIN3	12	I	PPWR3	62	O	SA6	38	I/O
BSA5	95	I/O	GPOUT1	47	O	PPWR4	63	O	SA7	37	I/O
BSA6	96	I/O	GPOUT3	9	O	PPWR5	64	O	SD0	79	I/O
BSA7	97	I/O	HDCHRDY	58	I	PPWR6	65	O	SD1	80	I/O
BSAOE#	22	I	HDDSA0	99	O	PPWR7	67	O	SD2	81	I/O
BSADIR	72	I	HDDSA1	100	O	PPWRL0	51	I	SD3	82	I/O
CNTRL1	16	I	HDDSA2	4	O	PWRGD	23	I-Sch	SD4	83	I/O
CNTRL3	13	I	HDRD#	1	O	RESET	11	I	SD5	84	I/O
DBE#	50	I	HDRST#	49	O	RESET#	8	O	SD6	85	I/O
DCS1#	5	O	HDWR#	2	O	RINGI	7	I	SD7	86	I/O
DCS3#	70	O	IOCHRDY	6	O	RQMX0	25	O	SUS#/RES#	20	I
DTRIS#	98	I	IRQ1	29	I	RQMX1	27	O	VBATT	55	I
EPMI0#	48	I	IRQ3	30	I	RQMX2/RQMX4	19	O	VCC	14	P
EPMI1#	77	I	IRQ4	33	I	RQMX3/RQMX5	18	O	VCC	41	P
EPMI2#	36	I	IRQ8#	56	O(OD)	RSTDRV	76	O	VCC	71	P
EPMI3#/KBRST#	73	I	IRQ10	31	I	RTCAS	26	I	VCC	91	P
GND	3	G	IRQ12	32	I	RTCRD#	68	I	32KHZX1	53	I
GND	15	G	IRQ14	34	I	RTCWR#	69	I	32KHZX2	54	O

3.7 Viper NBB Mode Signal Descriptions

Refer to the Viper NBB internal circuitry schematic in Section 4.0 for complete details.

3.7.1 Clock and Reset Interface Signals

Signal Name	Pin No.	Signal Type	Signal Description
RESET	11	I	***Reset:*** Reset input from the Viper Notebook Chipset.
RESET#	8	O	***Reset:*** The inverted output of RESET (pin 25). This signal is also used to reset the internal real-time clock.
RSTDRV	76	O	***Reset Drive:*** An active high reset output to the AT bus.
PWRGD	23	I-Sch	***Power Good:*** The PWRGD input signal from the power supply. A rising edge on this input is used to sample the strap information.
BPWRGD	21	O (OD)	***Buffered Power Good:*** An open drain output signal to the Viper Notebook Chipset.

3.7.2 Interrupt Control Interface Signals

Signal Name	Pin No.	Signal Type	Signal Description
IRQ1, IRQ3, IRQ10, IRQ12	29, 30, 31, 32	I	***Interrupt Request bits 1, 3, 10, and 12:*** Interrupt request inputs from the ISA bus. These inputs are output serially to the Viper Notebook Chipset on RQMX0. A low pulse on any of these inputs is internally extended by one ATCLK.
IRQ4, IRQ14, IRQ15	33, 34, 35	I	***Interrupt Request bits 4, 14, and 15:*** Interrupt request inputs from the ISA bus. These inputs are output serially to the Viper Notebook Chipset along with IRQ8# on RQMX1. A low pulse on any of these inputs is internally extended by one ATCLK.
RQMX[1:0]	65, 64	O	***Serial Outputs 1 and 0:*** These outputs are sent to the Viper Notebook Chipset. The Viper Notebook Chipset will demultiplex these lines to decode interrupt and power management information.

3.7.3 Data Bus and Control Interface Signals

Signal Name	Pin No.	Signal Type	Signal Description
SD[7:0]	86:79	I/O	***System Data AT Bus Lines 7 through 0:*** In this mode, the RTC data pins are connected to these signals.

3.7.4 Power Management Interface Signals

Signal Name	Pin No.	Signal Type	Signal Description
DTRIS#	98	I	***Power Control Output Port Enable:*** This signal, when active, will tristate the power port. When disabled, it will allow output to the power port.
PPWRL0	51	I	***Peripheral Power Latch Control:*** This signal, when active, will latch the power control information on the SA bus and output it to the power control output pins.

Viper NBB Mode Signal Descriptions (cont.)

Signal Name	Pin No.	Signal Type	Signal Description
PPWR[7:0]	67:59	O	***Peripheral Power Bits 4 through 0:*** These power control outputs can be used to control power to various peripherals. Note that --WR7 is used internally to control access to the upper 128 bytes of the CMOS SRAM. When PPWR7 is low, the lower 128 bytes are accessed. When high, the upper 128 bytes are accessed.
SUS#/RES#	20	I	***Suspend / Resume:*** A power control input that is monitored by the Viper Notebook Chipset.
LOBAT	74	I	***Low Battery:*** A power control input that is monitored by the Viper Notebook Chipset.
LLOBAT/KBA20#	75	I	***Low Low Battery or Keyboard ControllerA20#:*** This input can be either LLOBAT (a power control input) or KBA20# from the keyboard controller. When the input is LLOBAT, pin 18 is RQMX3. If the input is KBA20#, pin 18 becomes RQMX5.
RINGI	7	I	***Ring Indicator:*** A power control input that is monitored by the Viper Notebook Chipset.
ATCLK	27	I	***AT Bus Clock:*** AT bus clock input from the Viper Notebook Chipset. This input along with ATCLK/2 will serially output interrupts and power management inputs to the Viper Notebook Chipset.
ATCLK/2	24	I	***AT Bus Clock Divide by 2:*** AT bus clock divide by 2 input from the Viper Notebook Chipset.
EPMI3#/KBRST#	73	I	***External Power Management Input Bit 3 or Keyboard Reset:*** This input can be either EPMI3# (power management input) or KBRST# from the keyboard controller. When the input is EPMI3#, pin 19 becomes RQMX2. When it is KBRST#, pin 19 becomes RQMX4.
EPMI[2:0]#	36, 77, 48	I	***External Power Management Input Bits 2 through 0:*** These three inputs and EPMI3# will signal the Viper Notebook Chipset that an external power management event has occurred.
RQMX2/RQMX4	19	O	***Multiplexed Power Management Output:*** RQMX2/RQMX4 is a multiplexed output of RINGI, EPMI2#, EPMI3#/KBRST#, and LOBAT. These inputs are multiplexed using ATCLK and ATCLK/2.
RQMX3/RQMX5	18	O	***Multiplexed Power Management Output:*** RQMX3/RQMX5 is a multiplexed output of SUS#/RES#, EMPI0#, EPMI1#, and LLOBAT/KBA20#. These inputs are multiplexed using ATCLK and ATCLK/2.

3.7.5 Real-Time Clock Interface Signals

Signal Name	Pin No.	Signal (Drive) Type	Signal Description
RTCRD#	68	I	***Real-time Clock Read Command:*** This is the data strobe input. The falling edge of this strobe is used to enable the outputs during a read cycle.
RTCWR#	69	I	***Real-time Clock Write Command:*** The rising edge of this input latches data in the internal real-time clock.

Viper NBB Mode Signal Descriptions (cont.)

Signal Name	Pin No.	Signal (Drive) Type	Signal Description
RTCAS	26	I	***Real-time Clock Address Strobe:*** RTCAS is used to demultiplex the address/ data bus. The falling edge of AS latches the address on XD[7:0].
RTC_5V	57	I	***Real-time Clock 5.0V:*** This pin must be connected to +5V. This input will prevent the VBATT from being accessed during power-on.
VBATT	55	I	***Voltage Battery:*** This pin is connected to the CMOS and RTC battery.
IRQ8#	56	O (OD)	***Interrupt Request Bit 8:*** The alarm output interrupt generated by the internal real-time clock. This pin needs an external pull-up.
32KHZX1	53	I	***Crystal Oscillator Input:*** 32.768KHz XTAL input.
32HKZX2	54	O	***Crystal Oscillator Output:*** 32.768KHz XTAL output.

3.7.6 IDE Interface Signals

Signal Name	Pin No.	Signal Type	Signal Description
DBE#	50	I	***Data Buffer Enable:*** This signal, when active, will allow information to pass to the IDE drive.
DCS1#, DCS3#	5, 70	O	***Drive Chip Select 1 and 3:*** These chip select signals decoded from the host address bus are used to select the Command and Control Block Registers.
HDCHRDY	58	I	***Drive I/O Channel Ready:*** This signal is negated to extend the host transfer cycle of any host register access (read or write) when the drive is not ready to respond to a data transfer request. When HDCHRDY is not negated, HDCHRDY is in a high impedance state.
HDDSA[2:0]	4, 100, 99	O	***Drive Address Lines 2 through 0:*** This is the 3-bit binary coded address asserted by the host to access a register or data port in the drive.
HDRD#	1	O	***Drive I/O Read:*** This is the read strobe signal. The low level of HDRD# enables data from a register or the data port of the drive onto the data bus DD[7:0] or DD[15:0].
HDRST#	49	O	***Drive Reset:*** This signal is asserted for at least 25msec after voltage levels have stabilized during power-on and negated thereafter unless some event requires that the drive(s) be reset following power-on.
HDWR#	2	O	***Drive I/O Write:*** This is the write strobe signal. The rising edge of DWR# samples data from the data bus DD[7:0] or DD[15:0] into a register or the data port of the drive.
IOCHRDY	6	O	***I/O Channel Ready:*** This signal to the AT bus is used to extend the current cycle for non-zero wait state operations.
SA[7:0]	37:39, 42:46	I/O	***System Address Bus Lines 7 through 0:*** These AT bus address lines supply information to the IDE and power latch.
LATCH	87	I	***IDE Latch Enable:*** The input must be tied high if the internal buffer is used. If the internal buffer is not used, this input may be tied to PPWRL1 of the 82C558N IPC to obtain PPWR[13:8] on pins 5, 1, 2, 4,100, and 99 respectively.

Viper NBB Mode Signal Descriptions (cont.)

Signal Name	Pin No.	Signal Type	Signal Description
BSA[7:0]	97:92, 89, 88	I/O	***Buffered SA Bus:*** This output buffers the address bus to the ISA bus. These also function as strap inputs during reset. BSA5, BSA4, and BSA0 must have a 4.7K pull-down resistor. BSA[7:6] and BSA[3:1] do not need pull-ups for strap sampling, but since these lines are connected to the ISA bus, they need to be pulled up. Note that ISA address lines 0, 4, and 5 have to be pulled low with 4.7K ohm resistors. There should be no pull-ups on these lines.
BSAOE#	22	I	***SA Buffer Enable:*** When enabled, this signal will allow the address to be sent/ received from the SA[7:0] lines and the BSA[7:0] lines.
BSADIR	72	I	***SA Buffer Direction Control:*** When low, this signal will allow an ISA master to drive addresses through the buffer to the 82C558N IPC on the SA[7:0] lines. When high, this signal will allow the 82C558N to drive an address onto the BSA[7:0] lines from SA[7:0].
CNTRL1	16	I	***Control 1:*** This signal, when asserted, will tristate the GPOUT1 signal.
CNTRL3	13	I	***Control 3:*** This signal, when asserted, will tristate the GPOUT3 signal.
GPIN1	17	I	***General Purpose Input 1:*** This general purpose input will be inverted and output on GPOUT1.
GPIN3	12	I	***General Purpose Input 3:*** This general purpose input will be inverted and output on GPOUT1.
GPOUT1	47	O	***General Purpose Output 1:*** This general purpose output signal is controlled by CNTRL1.
GPOUT3	9	O	***General Purpose Output 3:*** This general purpose output signal is controlled by CNTRL3.

3.7.7 Power and Ground Pins

Signal Name	Pin No.	Signal Type	Signal Description
VCC	14, 41, 71, 91	P	***Power Connection***
GND	3, 15, 28, 40, 52, 66, 78, 90	G	***Ground Connection***

Legend:

G	Ground
I/O	Input/Output
G	Ground
OD	Open Drain
I/O	Input/Output
P	Power
Sch	Schmitt-trigger