17K 4-BIT MICROCONTROLLER DATA BOOK

NEC

1992
17K 4-BIT MICROCONTROLLER DATA BOOK

20043

Table of Contents

General information

Section 1 - General Information

NEC's consumer ICs include a variety of devices which are built into the electronic equipment found nowadays in most homes. They are used to control audio and video systems, transmit and display information, store data, drive clocks and for many other functions.
Infrared remote controllers for home entertainment like VCR, TV and audio equipment are extremly popular. Their use is spreading to household appliances and new application fields like car locks, security systems, burglar alarms and air-conditioning systems.

The NEC consumer data book is divided into the following sections:

1. General Information. This section gives a general overview of NEC's consumer devices and the structure of the data book.

2. μPD17K-Family. In this section you will find all devices of our μPD17K-Family separated into 5 main groups:
- the μPD170xx series (digital tuning systems)
- the μPD171xx series (consumer specific microcomputers)
- the μPD172xx series (remote controllers)
- the μPD173xx series (home automation controllers)
- the μPD174xx series (special consumer applications)

3. Instruction Manual of the μPD17K-Family. This section provides you with information about the architecture and the instruction set of this device family.

μPD17K-Family

Section 2 - μPD17K-Family

17K-Family

- One machine-cycle instruction execution
- General Register Machine not just Accu based CPU
- 16 bit instruction length

170xx

- Digital tuning systems
- Serial interface
- A/D –D/A-converters
- IF-counter
- LCD-driver
- Image display controller
- PLL

171xx

- White goods controllers
- Low power consumption
- General purpose
- Serial interface
- A/D-converter
- Timer
- Low voltage operation

172xx

- Remote controller
- Low voltage operation
- Carrier frequency generation
- Low voltage detection circuit
- Constant LCD voltage circuit
- Learning remote controller
- Built-in preamplifier
- Large static RAM

170xx – Overview

	DTS (TUNERS)					LCD-TV/VCR		Portable TV; Voltage synthesizer		
	17001	17003A	17005	17010	17006	17002	17008	17051	17052	17053
ROM (words)	3836	3836	7932		12288	3968	16256	8192		12288
RAM (words)	224	320	432		896	336	672	448		672
Stack levels	7			9	7	6	7	6		7
Minimum instruction execution time	4.44µs/4.5MHz				1.78µs/ 4.5MHz	2µs/8MHz				
ADCs	6 x 6 bit				6 x 8 bit	6 x 4 bit	8 x 4 bit			
DACs (PWM)	3 x 8 bit				3 x 9 bit	4 x 6 bit	9 x 8 bit 6 x 6 bit	3 x 6 bit	4 x 6 bit	
Amplifiers	1			–		–				
Int./ext. interrupts	3/1	3/2		4/2		–/1				
Serial interface	1 channel 3 wires 1 channel 2 wires	2 channels 3 wires 1 channels 2 wires				1 channel 3 wires 1 channel 2 wires				
I/O-Ports	12	16			48	15	16	15	20	
Input-Ports	8					4				
Output-Ports	12	9			11	8	25	12	20	
LCD Driver	–	30 segments / 2 common			–	–				
IDC charact. on screen						99	200	97	99	199
IDC different types						120	248	128	128	256
Counter	16 bit IF counter					Vsync-; Hsync- counter				
PLL/voltage synthesizer	150 MHz PLL	250 MHz PLL	150 MHz PLL			15 MHz PLL (ext. prescaler required)		14 bit D/A (PWM) Voltage synthesizer		
Pins Package	48 QFP	80 QFP				48 SDIP/QFP	64 SDIP	48 SDIP	64 SDIP	
OTP	17P001	17P005		17P010	17P006	No OTP version	17P008	No OTP version		

171xx - Overview

	17102	17106	17103 (L)*	17104 (L)*	17107(L)*	17108 (L)*	17134A	17136A	17135A	17137A
ROM (words)	2048	4096	512				1024	2048	1024	2048
RAM (words)	222	178	16				112			
Stack levels	3	7	1				5			
Minimum instruction execution time	2 µs / 8 MHz		STD: V_{DD} 4.5 - 6V 2 µs /8 MHz		STD: V_{DD} 4.5 - 6 V 8 µs /1 MHz		8 µs / 1MHz		2 µs / 8MHz	
			L: V_{DD} 1.8 - 3.6 V 8 µs /2 MHz		L: V_{DD} 1.5 - 3.6 V 40 µs /200kHz					
ADCs	6 bits 4 channels	–					1 x 8 bit / 4 channel			
DACs (PWM)	1 x 6 bit	–								
Timers	8 bit 2 channels	–					8 bit / 2 channels + watchdog			
Zero-Cross Detectors	1	–					1			
Int./ext. interrupts	2/3	2/1	–				4/1			
Serial interface	1channel 3 wires	2 channels 2 and 3 wires	–				1channel 3 wires			
LCD-Driver	48 segments	176 segments	–							
I/O-Ports	16	5	11	16	11	16	21			
Input-Ports	8	4	–							
Output-Ports	14	–								
Amplifiers	2	–								
Clock Generator	Ceramic resonator				RC oscillator				Ceramic resonator	
Pins Package	52 QFP	64 QFP	16 DIP 16 SOP	22 SDIP 24 QFP	16 DIP 16 SOP	22 SDIP 24 SOP	28 SDIP 28 SOP			
OTP	No OTP version	17P106	17P103	17P104	17P107	17P108	17P136A		17P137A	

* L: Low voltage version

172xx - Overview

	17201A	17207	17202A	17203A	17204
ROM (words)	3072	4096	2048	4096	7936
RAM (words)	336		112	336 + 4096 SRAM	336 + 2048 SRAM
Stack levels	5				7
Instr.exec. time	4µs/4MHz				
ADCs	4 x 8 bit		–		
Timers	8 bit + watchdog			8 bit / 10 bit / 16 bit + watchdog	
Ext. interrupt	1				
Serial interface	1		–	1	
I/O-Ports	19		16	28	
LCD-Drivers	34 segments + 4 common		24 segments + 4 common	–	
Pins Package	80 QFP		64 QFP	52 QFP	
OTP	17P207		17P202A	17P203A	17P204

Common features:
- Low voltage operation (2.0V)
- Low voltage detection circuit

BUILT-IN PRESCALER

μPD17001 is a 4 bits CMOS microcomputer for Digital Tuning System implemented prescaler (operational frequency up to 150 MHz), PLL frequency synthesizer and IF counter on chip.

CPU applies μPD17000 architecture which operates data memory directly without accumulater, and it realizes effective programming.

All instructions consist of 16 bits one word.

As PLL frequency synthesizer can apply pulse swallow method, high performance tuner is easily constructed by selecting high reference frequency like 50 kHz or 100 kHz.

In addition, station detect is realized by counting intermediate frequency of tuner using built-in 16 bits IF counter.

As system development support tools of μPD17001, IE-17K (In Circuit Emulator) and AS17K (assembler) are prepared.

FEATURES

- 4 bits microcomputer for Digital Tuning System
- program memory (ROM)
  : 8 K bytes (16 bits x 3836 steps)
- data memory (RAM)
  : 224 words (4 bits x 224 words)
- stack level: 7
- 35 types of simple instruction
- decimal operation
- instruction execution time: 4.44 μs
  (with 4.5 MHz crystal oscillator)
- built-in PLL frequency synthesizer and 150 MHz prescaler
- 12 types of reference frequencies can be selected by software.
  1, 1.25, 2.5, 3, 5, 6.25, 9, 10, 12.5, 25, 50, 100 kHz
- built-in amplifier for LPF (Low pass filter)
- built-in IF counter (AMIFC, FMIFC)
- built-in 8 bits serial interface
  1 system 2 channels: 3 wire or 2 wire system
- built-in D/A converter: 8 bits x 3 (PWM output)
- built-in A/D converter: 6 bits x 6
- built-in discharge detection circuit and power on reset circuit
- interrupt
  external interrupt: 2 channels
  internal interrupt: 3 channels
- various I/O ports
  input/output ports: 12 lines
  input ports : 8 lines
  output ports : 12 lines
- built-in CGP (Clock Generator Port)
- single power supply (5 V±10 %)
- CMOS low power consumption
- 48-pin plastic QFP

Notes on Serial interface:

The 2-wire mode corresponds to the I2C-Bus specification from Philips.

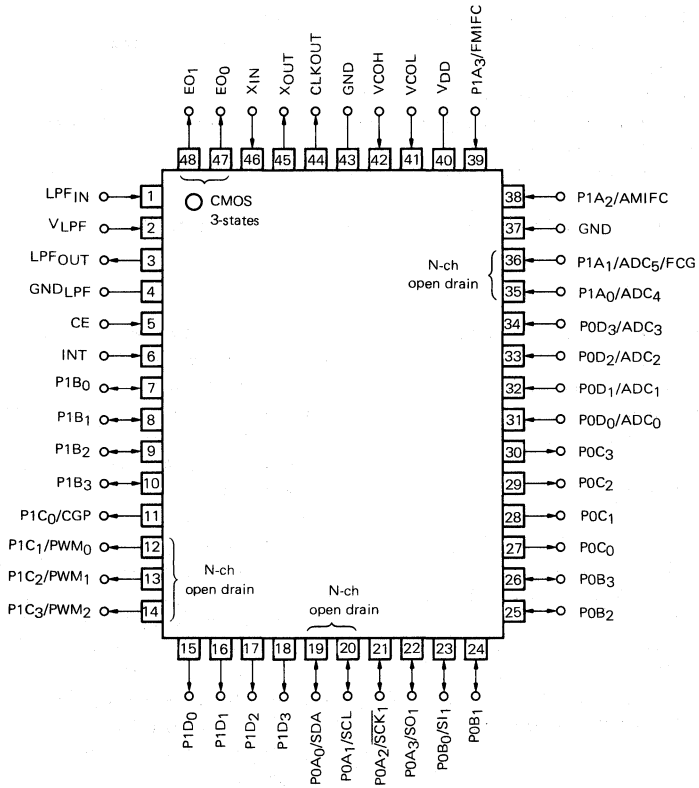
In case of using this interface mode note the following:

Duties when using I2C bus system

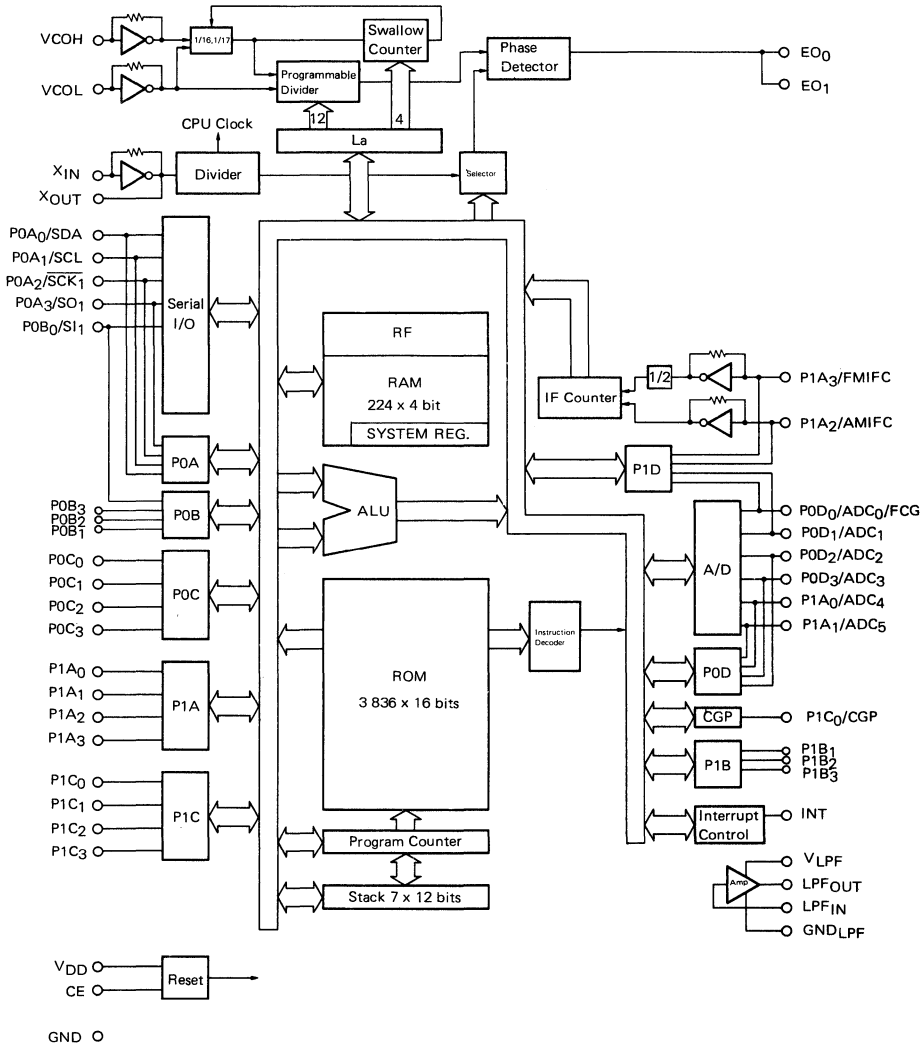
Purchase of NEC's I2C bus system hardware components conveys a license under the Philips I2C patents rights to use this components in an I2C system, provided that the system conforms the I2C standard specifications as defined by Philips.

Consequently for all ROM based components with I2C hardware circuits the user is kindly requested to notify the use of the I2C bus interface at the ROM code verification stage.

PIN CONFIGURATION (Top View)



BLOCK DIAGRAM



BUILT-IN EPROM, PRESCALER

μPD17P001 is a 4 bits CMOS microcomputer for Digital Tuning System implemented EPROM, prescaler (operational frequency up to 150 MHz), PLL frequency synthesizer and IF counter on chip.

CPU applies μPD17000 architecture which operates data memory directly without accumulater, and it realizes effective programming.

All instructions consist of 16 bits one word.

As PLL frequency synthesizer can apply pulse swallow method, high performance tuner is easily constructed by selecting high reference frequency like 50 kHz or 100 kHz.

In addition, station detect is realized by counting intermediate frequency of tuner using built-in 16 bits IF counter.

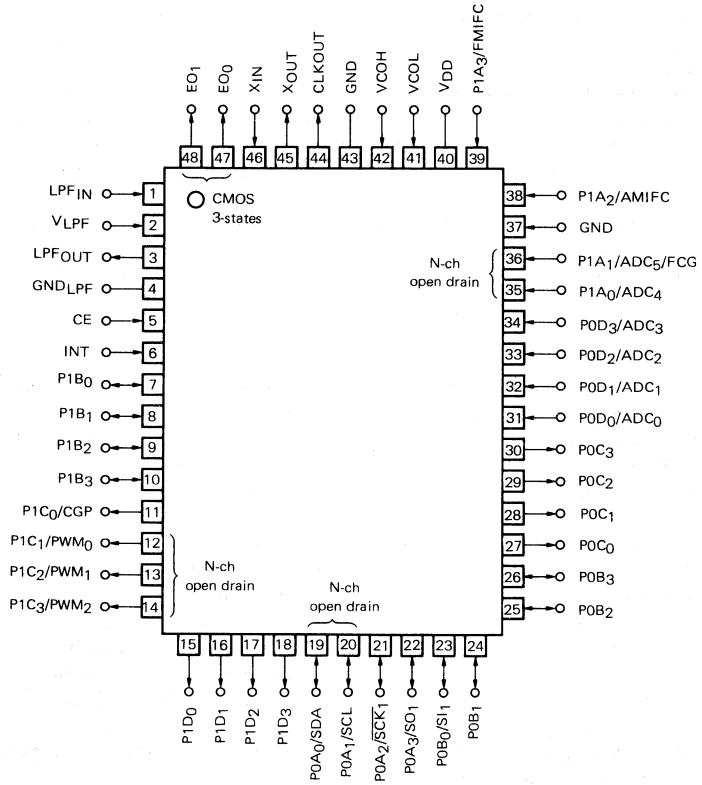
μPD17P001 is the most suitable for evaluating the program of μPD17001 or for producing a few products because μPD17P001 is built-in EPROM.

As system development support tools of μPD17P001, IE-17K (In Circuit Emulator) and AS17K (assembler) are prepared.

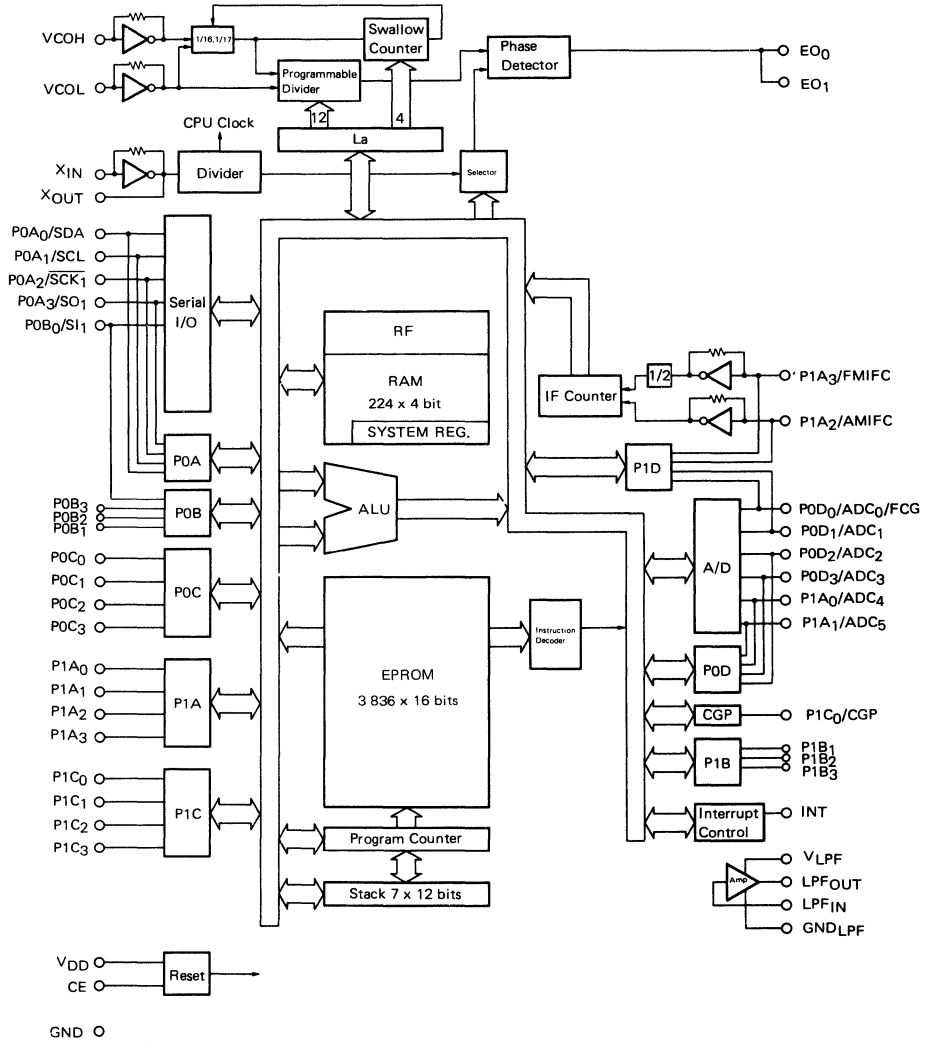
FEATURES

- 4 bits microcomputer for Digital Tuning System
- program memory (EPROM)
  : 8 K bytes (16 bits x 3836 steps)
- data memory (RAM)
  : 224 words (4 bits x 224 words)
- stack level: 7
- 35 types of simple instruction sets
- decimal operation
- instruction execution time: 4.44 μs
  (with 4.5 MHz crystal oscillator)
- built-in PLL frequency synthesizer and 150 MHz prescaler
- 12 types of reference frequencies can be selected by software.
  1, 1.25, 2.5, 3, 5, 6.25, 9, 10, 12.5, 25, 50, 100 kHz
- built-in amplifier for LPF (Low pass filter)
- built-in IF counter (AMIFC, FMIFC)
- built-in 8 bits serial interface
  1 system 2 channels: 3 wire or 2 wire system
- built-in D/A converter: 8 bits x 3 (PWM output)
- built-in A/D converter: 6 bits x 6
- built-in discharge detection circuit and power on reset circuit
- interrupt
  external interrupt: 2 channels
  internal interrupt: 3 channels
- various I/O ports
  input/output ports: 12 lines
  input ports : 8 lines
  output ports : 12 lines
- built-in CGP (Clock Generator Port)
- single power supply (5 V±10 %)
- CMOS low power consumption
- Product of mask ROM version: μPD17001
- 48-pin plastic QFP

PIN CONFIGURATION (Top View)



BLOCK DIAGRAM



DIGITAL TUNING SYSTEM HARDWARE BUILT-IN 4-BIT SINGLE CHIP MICRO CONTROLLER

μPD17003A is a 4-bit single chip CMOS micro controller which contains digital tuning system hardware.

17K architecture is used for CPU, data and memory manipulations and various types of operations, and peripheral hardware control can be performed directly by one instruction.

Peripheral hardware devices include a prescaler which operates up to 250 MHz, PLL frequency synthesizer, LPF (Low Pass Filter) amplifier, and frequency counter for digital tuning in addition to various types of input/output ports, LCD controller/driver, A/D converter, D/A converter (PWM output), and clock generator ports.

Consequently, a high performance digital tuning system with a variety of functions can be constructed using only one chip. μPD17005 (note) is available as the product which is pin-compatible with μPD17003A and whose memory size (ROM) is extended. One-time PROM version μPD17P005 (note) is available as μPD17005, and μPD17P005 can be used for program evaluation of μPD17003A at small volume production.

FEATURES

- Using 17K architecture
- Program memory (ROM)
  8K bytes (3836 steps x 16 bits)
- General purpose data memory (RAM)
  320 nibble (320 words x 4 bits)
- Instruction execution time
  4.44 μs (using 4.5 MHz quarts oscillator)
- Decimal operation enabled
- Table reference enabled
- Built-in PLL frequency synthesizer hardware
- Dual modules prescaler (250 MHz Max.), programmable divider, phase comparator, charge pump, and LPF amplifier
- Various types of peripheral hardware
  General purpose input/output ports, LCD controller/driver, serial interface, A/D converter, D/A converter (PWM output), clock generator, ports, and frequency counter
- Various types of interrupt
  External interrupt : 2 channels
  Internal interrupt : 3 channels
- Power On Reset, resetting by a CE pin, and built-in blackout detection circuit
- CMOS low power consumption
- Power supply voltage 5 V ±10%

ORDERING INFORMATION

Order Code	Package
μPD17003AGF-XXX-3B9	80-pin plastic QFP (14 x 20)

Notes on Serial interface:

The 2-wire mode corresponds to the I2C-Bus specification from Philips.

In case of using this interface mode note the following:

Duties when using I2C bus system

Purchase of NEC's I2C bus system hardware components conveys a license under the Philips I2C patents rights to use this components in an I2C system, provided that the system conforms the I2C standard specifications as defined by Philips.

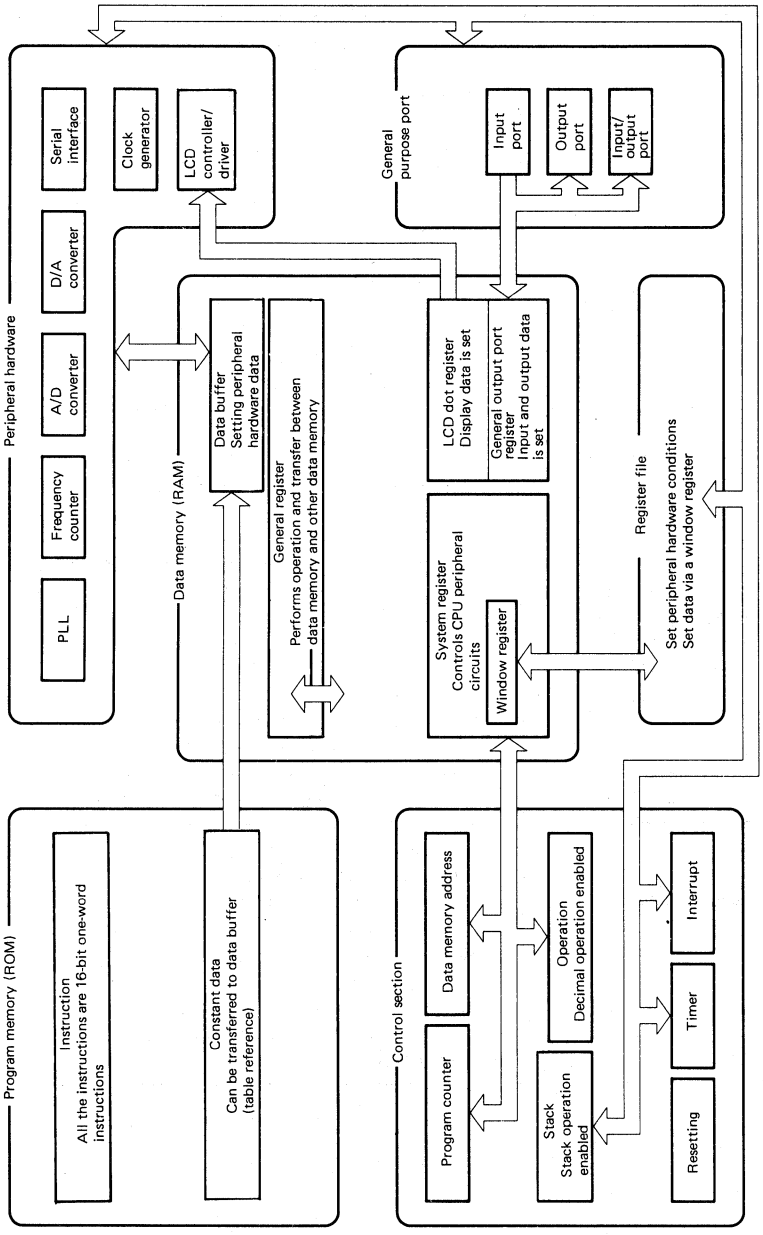
Consequently for all ROM based components with I2C hardware circuits the user is kindly requested to notify the use of the I2C bus interface at the ROM code verification stage.

μPD17003A FUNCTION OUTLINE

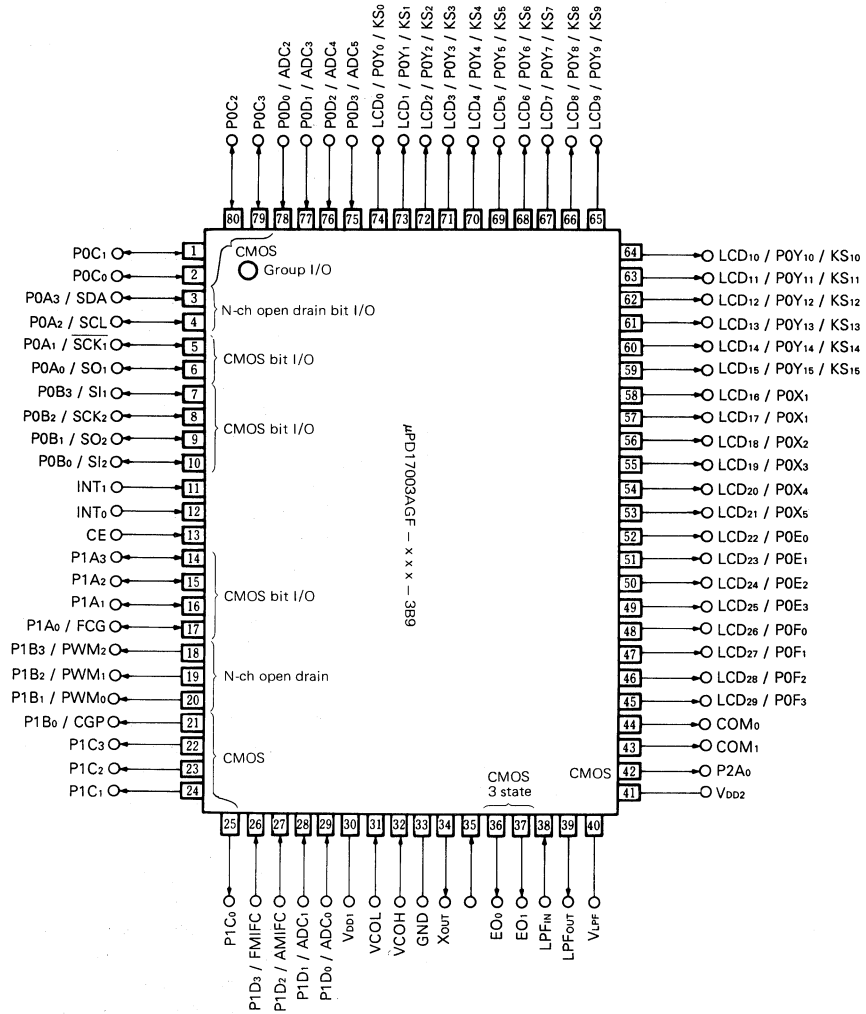
Item	Function
Program memory (ROM)	• 8K bytes (3836 steps x 16 bits) Table reference area: up to 256 steps x 16 bits
General data memory (RAM)	• 320 nibble (320 words x 4 bits) Data buffer: 4 nibbles General register: 16 nibbles
System register	• 12 nibbles
Register file	• 33 nibbles (control register)
General port register (including LCD dot data register)	• 24 nibbles
Instruction execution time	• 4.44 μs (using 4.5 MHz quarts oscillator)
Stack level	• 7 levels (stack operation enabled)
General purpose port	• Input/output port: 16 • Input ports: 8 • Output ports: 9 (+30: LCD segment pin)
Clock generator port (CGP)	• 1 VDP (Variable Duty Pulse) and SG (Signal Generator) functions
LCD controller/driver	• 30 segments, 2 common 1/2 duty, 1/2 bias, frame frequency 250 Hz, driving voltage V_{DD}, segment pin used also for key source: 16 ports All of the 30 ports can be used as output ports (4 ports, 4 ports, 6 ports, and 16 ports can be set independently)
Serial interface	• Two types (3 channels) 8-bit 3-wire system: 2 channels 8-bit 2-wire system: 1 channel
D/A converter	• 8 bits x 3 (PWM output and output resisting pressure 16 V Max.)

Item		Function
A/D converter		• 6 bits x 6 (consecutive comparison method by software)
Interrupt		• 5 channels (maskable interrupt) External interrupt: 2 channels (INT_0 pin and INT_1 pin) Internal interrupt: 3 channels (timer, serial interface 1, and frequency counter)
Timer		• Two types Timer carry FF (1, 5, 100, 250 ms) Timer interrupt (1, 5, 10, 250 ms)
Reset		• Power On Reset (at power supply connection) • Resetting by CE pin (CE pin Low – High) • Blackout detection function
PLL frequency synthesizer	Division method	• 2 types Direct division method (VCOL pin 20 MHz Max.) Pulse swallow method (VCOL pin 40 MHz Max.) (VCOH pin 250 MHz Max.)
	Reference frequency	• 12 types are selected by the program 1, 1.25, 2.5, 3, 5, 6.25, 9, 10, 12.5, 25, 50, 100 kHz
	Charge pump	• Two independent error output
	Phase comparator	• Unlocking can be detected by a program Unlocking FF delay time can selected
	LPF amplifier	• CMOS operation amplifier output resisting pressure 16 V Max.
Frequency counter		• Frequency test $P1D_3$ / FMIFC pin 5 to 15 MHz $P1D_2$ / AMIFC pin 0.1 to 1 MHz • External gate width test $P0A_1$ / FCG pin
Power supply voltage		5 V ±10%
Package		80-pin plastic QFP

CONCEPT OF μPD17003A



PIN CONFIGURATION (Top View)



1. PIN FUNCTIONS

1.1 EXPLANATION ON EACH PIN FUNCTION

PIN NO.	SYMBOL	INPUT/ OUTPUT	OUTPUT MODE	PIN NAME	FUNCTION
79 80 1 2	$P0C_3$ $P0C_2$ $P0C_1$ $P0C_0$	Input/ Output	CMOS Push-Pull	Port 0C	4-bit general purpose output port. Can be specified as an input or output port in 4-bit units (group I/O). Input/ output is specified by the P0CGPIO register (address 27H) of a register file. The P0C register (address 27H of BANK0) of the port register is used for reading input data and setting output data. At Power On Reset, Clock Stop instruction execution, or CE Reset, these pins are specified as input ports.
3 4 5 6	$P0A_3$ / SDA $P0A_2$ / SCL $P0A_1$ / $\overline{SCK_1}$ $P0A_0$ / SO_1	Input/ Output	N-ch open drain CMOS Push-Pull	Port 0A	Used as a 4-bit general purpose input/ output port and also for serial interface. A general purpose input/output port and serial interface is switched by the SIO1MODE register (address 08H) and SIO2MODE register (address 02H) of the SIO1MODE register of the register file. **(1) When the pin is used as a 4-bit general purpose input/output port** The port can be specified as an input or output port in bit units (bit I/O). Input or output is specified by the P0ABIO register (address 35H) of the register file. The P0A register (address 70H of BANK0) is used for reading input data and output data and setting the port register. Since $P0A_3$ / SDA, and $P0A_2$ / SCL pins are N-ch open drain output, pull-up resistance is required in the external section.

<table>
<tr><th>PIN NO.</th><th>SYMBOL</th><th>INPUT/ OUTPUT</th><th>OUTPUT MODE</th><th>PIN NAME</th><th>FUNCTION</th></tr>
<tr><td>3
4
5
6</td><td>P0A3 / SDA
P0A2 / SCL
P0A1 / $\overline{SCK_1}$
P0A0 / SO1</td><td>Input/ Output</td><td>N-ch open drain
CMOS Push-Pull</td><td>Port 0A</td><td>(2) When the pins are used for serial interface
Two types of serial interfaces are available, serial interface 1 and serial interface 2 including Port 0B (pin numbers 7 to 10).
Serial interface 1 and serial interface 2 can be used concurrently.
Two channels of a 2-wire system and 3-wire system can be used for serial interface 1 and one channel of a 3-wire system can be used for serial interface 2.
When using serial interface 1, specify pins from the SIO1MODE register of the register file and when using serial interface 2, specify pins using SIO2MODE register.
The function of each pin is listed below.</td></tr>
</table>

Pin name	Function	Operating mode	
P0A3 / SDA	Data input/ output	2-wire	Serial interface 1
P0A2 / SCL	Clock input/ output		
P0A1 / $\overline{SCK_1}$	Clock input/ output	3-wire	
P0A0 / SO1	Data output		
P0B3 / SI1	Data input		

<table>
<tr><th>PIN NO.</th><th>SYMBOL</th><th>INPUT/ OUTPUT</th><th>OUTPUT MODE</th><th>PIN NAME</th><th>FUNCTION</th></tr>
<tr><td>3
4
5
6</td><td>P0A3 / SDA
P0A2 / SCL
P0A1 / $\overline{SCK_1}$
P0A0 / SO1</td><td>Input/ Output</td><td>N-ch open drain
CMOS Push-Pull</td><td>Port 0A</td><td>
<table>
<tr><th>Pin name</th><th>Function</th><th colspan="2">Operating mode</th></tr>
<tr><td>P0B2 / $\overline{SCK_2}$</td><td>Clock input/ output</td><td rowspan="3">3-wire</td><td rowspan="3">Serial interface 2</td></tr>
<tr><td>P0B1 / SO2</td><td>Data output</td></tr>
<tr><td>P0B0 / SI2</td><td>Data input</td></tr>
</table>
Since pins P0A3 / SDA and P0A2 / SCL are N-ch open drain, Pull-Up resistance is required externally.
At Power On Reset, Clock Stop instruction execution, and CE Reset, all of these pins are specified as input ports of general purpose input/output ports.
</td></tr>
<tr><td>7
8
9
10</td><td>P0B3 / SI1
P0B2 / $\overline{SCK_2}$
P0B1 / SO2
P0B0 / SI2</td><td>Input/ Output</td><td>CMOS Push-Pull</td><td>Port 0B</td><td>Used for 4-bit general purpose input/ output ports and also for serial interface
The SIO1MODE register (address 08H) or SIO2MODE register (address 02H) of the register file are used for switching the function as general purpose input/ output port to serial interface or vice versa.
(1) When using the pins as 4-bit general purpose input/output ports
The pins can be specified as input or output ports in bit units (bit I/O).
Input or output is specified by the P0BBIO register (address 35H) of the register file.
The P0B register (address 71H of BANK0) of the port register is used for reading input data and setting output data.</td></tr>
</table>

PIN NO.	SYMBOL	INPUT/ OUTPUT	OUTPUT MODE	PIN NAME	FUNCTION
7 8 9 10	$P0B_3$ / SI_1 $P0B_2$ / $\overline{SCK_2}$ $P0B_1$ / SO_2 $P0B_0$ / SI_2	Input/ Output	CMOS Push-Pull	Port 0B	(2) **When the pins are used for serial interface** Two types of serial interface can be used including Port 0A (addresses 3 to 6), serial interface 1 and serial interface 2. See the explanation on Port 0A for the function of each pin. At Power On Reset, Clock Stop instruction execution, and CE Reset, all of these pins are specified as input ports of general purpose input/output ports.
11 12	INT_1 INT_0	Input	–	Interrupt	External interrupt request input pin. An interrupt request is issued from the input signal rising edge or falling edge of the input signal added to the pin. A rising edge and a falling edge can be specified by the INTEDGE register (address 1FH) of the register file using INT_0 pin and INT_1 pin independently. Even if an interrupt request is issued, interrupt cannot be accepted unless it is permitted (maskable interrupt). Types of interrupt permission include permission of all the interrupts by the EI instruction and permission of the interrupt of each INT_0 pin and INT_1 pin. Permission of interrupt for each pin is specified by the INTPM2 register (address 2FH) of the register file. When interrupt is permitted and when an interrupt request is issued, the interrupt is accepted. When interrupt is accepted, control of the program is passed to address 0005H in the case of interrupt by the INT_0 pin and address 0004H in the case of interrupt by the INT_1 pin. When interrupts for both INT_0 pin and INT_1 pin are allowed and when interrupts for both pins are issued, priority is given to the interrupt by INT_0 pin.

PIN NO.	SYMBOL	INPUT/ OUTPUT	OUTPUT MODE	PIN NAME	FUNCTION
11 12	INT_1 INT_0	Input	–	Interrupt	Even if an interrupt is not permitted, the issuing of an interrupt request can be checked using the INTREQ2 register (address 3FH) of the register file. When an interrupt function is not used, the input level of each pin can be detected by the INTJDG register (address 0FH) of the register file, and the pin can be used as a general purpose input port. At Power On Reset, Clock Stop Instruction execution, or CE Reset, the interrupt permission and interrupt request are reset.
13	CE	Input	–	Chip Enable	Input pins for device operation selection signal and reset signal. Device operation selection is to select the operation of the PLL frequency synthesizer and standby status as described below. (1) **Device operation selection** When the CE pin is at a High level, the PLL frequency synthesizer section can be operated. When the CE pin is at a Low level, the PLL frequency synthesizer section sets to a Disable state (operation prohibited) automatically in the device internal section. When the CE pin is at a Low level, the operation of quartz oscillation circuits in the internal section and CPU can be stopped by executing a Clock Stop instruction and data memory can be kept under a low consumption current (15 μA or less) (at CE pin = High level, the Clock Stop instruction operates as the NOP instruction). At execution of a Clock Stop instruction, the LCD controller/driver is set to a Display Off mode (LCD_0 to LCD_{29}, COM_0, COM_1 pin are Low level

PIN NO.	SYMBOL	INPUT/ OUTPUT	OUTPUT MODE	PIN NAME	FUNCTION
13	CE	Input	–	Chip Enable	output) and general purpose input-output ports (Port 0A, Port 0B, Port 0C, and Port 1A) are used as input ports. (2) **Reset signal input** When the CE pin is changed from a Low level to High level, the device is reset by synchronizing with the Timer Carry FF of the internal section (CE Reset). When the device is reset, the program starts from address 0. In this case, the general purpose input/output ports are used as input ports. Since four types of internal Timer Carry FF, 1, 5, 100, and 250 ms can be selected, the time elapsing from when the pin is changed from the Low level to High level until the device is reset can be selected. However, if a Clock Stop instruction has been executed, the device is reset about 100 ms after the CE pin is changed to a High level. This pin does not accept a Low level or High level of less than 100 to 165 μs to prevent operation error due to noise. By using the CEJDG register (address 07H) of the register file, the input signal level of this pin can be detected. In this case also, the contents of the CEJDG register do not change at a Low level or High level of less than 110 to 165 μs. Shumit Trigger input with hysterisis feature is used for this pin. Note that a voltage higher than that of V_{DD} pin must not be supplied at power connection.

PIN NO.	SYMBOL	INPUT/ OUTPUT	OUTPUT MODE	PIN NAME	FUNCTION
14 15 16 17	$P1A_3$ $P1A_2$ $P1A_1$ $P1A_0$ / FCG	Input Output	CMOS Push- Pull	Port 1A	Used as a 4-bit general purpose input/ output port and also as an external gate counter ($P1A_0$ / FCG pin). The switching between the general purpose input/output port and an external gate counter is performed by the IFCMODE register (address 12H) of the register file. (1) **When the port is used as a 4-bit general purpose input/output port** The port can be specified as an input or output port in bit units (bit I/O). Input or output is specified by the P1A register (address 35H) of the register file. The P1ABIO register (address 70H of BANK1) of the port register is used for reading input data and setting output data. (2) **When the port is used as an external gate counter (FCG) ($P1A_0$ / FCG pin)** The counter counts the time from one rising edge to the next rising edge of the signal sent to the $P1A_0$ / FCG pin. A reference frequency (1 kHz, 100 kHz, 900 kHz) of the internal section is counted by a 16-bit counter. The external gate counter is specified by the IFCMODE register (address 12H) and IFCCONT register (address 23H) of the register file. The PIA_0 / FCG pin must be specified as the input port by the P1ABIO register (address 35H). Since the IFCMODE register and IFCCONT register control the frequency conter ($P1D_3$ / FMIFC and $P1D_2$ / AMIFC pins) and a clock

PIN NO.	SYMBOL	INPUT/ OUTPUT	OUTPUT MODE	PIN NAME	FUNCTION
14 15 16 17	$P1A_3$ $P1A_2$ $P1A_1$ $P1A_0$ / FCG	Input Output	CMOS Push-Pull	Port 1A	generator port ($P1B_0$ / CGP pin) also, an external gate counter, frequency counter, and a lock generator port cannot be used concurrently. At Power On Reset, execution of a Clock Stop instruction, and CE Reset, all of these pins are specified for input ports of the general input/output ports.
18 19 20 21	$P1B_3$ / PWM_2 $P1B_2$ / PWM_1 $P1B_1$ / PWM_0 $P1B_0$ / CGP	Output	N-ch open drain CMOS Push-Pull	Port 1B	Used as a 4-bit general output port, D/A converter ($P1B_2$ / PWM_2, $P1B_2$ / PWM_1, $P1B_1$ / PWN_0 pins), and a clock generator port ($P1B_0$ / CGP pin). The PWMMODE register (address 13H) of the register file is used for switching the general output port, D/A converter and a clock generator port. (1) **When the port is used as a 4-bit general purpose output port** The P1B register (address 71H of BANK1) of the port register is used for setting output data. The pins PIB_3 / PWM_2, PIB_2 / PWM_1, and PIB_0 / PWM_0 require Pull-UP resistance for N-ch open drain output. (Resisting pressure 16 V Max.) (2) **When the port is used as a D/A converter (PWM output) (pins $P1B_3$/ PWM_2, $P1B_2$ / PWM_1, and $P1B_1$ / PWM_0)** Each of pins $P1B_3$ / PWM_2, $P1B_2$ / PWM_1, and $P1B_1$ / PWM_0 can output an independent signal. A pulse width modulation (PWM) method is used as the output method, the frequency is 878.9 Hz (225 kHz/256) and duty is 0.25/256–255.25/256. (256 stages)

<table>
<tr><th>PIN NO.</th><th>SYMBOL</th><th>INPUT/ OUTPUT</th><th>OUTPUT MODE</th><th>PIN NAME</th><th>FUNCTION</th></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td>The duty must be set below the PWMR0 to PWMR2 registers (addresses from 05H to 07H) via a data buffer.
<table><tr><th>Function</th><th>Frequency</th><th>Duty</th></tr><tr><td>D/A converter</td><td>878.9 Hz</td><td>$\frac{0.25 + X}{256} \times 100\%$
X = 0 – 255</td></tr></table></td></tr>
<tr><td>18
19
20</td><td>P1B3 / PWM2
P1B2 / PWM1
P1B1 / PWM0</td><td>Output</td><td>N-ch open drain</td><td>Port 1B</td><td>These three pins are N-ch open drain output and the resisting pressure is 16 V Max.</td></tr>
<tr><td>21</td><td>P1B0 / CGP</td><td></td><td>CMOS Push-Pull</td><td></td><td>(3) When the port is used as a clock generator port (CGP) (P1B0 / CGP pin)
The P1B0 / CGP pin is set to a CGP mode by the PWMMODE register (address 13H) and IFCMODE register (address 12H) of the register file.
Two functions are available for a CGP mode, VDP (Variable Duty Pulse) and SG (Signal Generator).
The VDP function produces output in 64 stages, duty 2/67 – 65/67 at frequency 269 Hz.
The SG function produces output by dividing with the value of 4 to 130 (64 stages) using frequency 18 kHz as the reference frequency.
Both the VDP and SG functions set data as follows using the CGPR register (address 20H) via a data buffer.</td></tr>
</table>

<table>
<tr><th>PIN NO.</th><th>SYMBOL</th><th>INPUT/ OUTPUT</th><th>OUTPUT MODE</th><th>PIN NAME</th><th>FUNCTION</th></tr>
<tr><td>18
19
20

21</td><td>P1B3 / PWM2
P1B2 / PWM1
P1B1 / PWM0

P1B0 / CGP</td><td>Output</td><td>N-ch open drain

CMOS Push-Pull</td><td>Port 1B</td><td>
<table>
<tr><th>Function</th><th>Frequency</th><th>Duty</th></tr>
<tr><td>VDP</td><td>269 Hz</td><td>$\frac{2+X}{67}$ x 100%
X = 0 – 63</td></tr>
<tr><td>SG</td><td>$\frac{18}{2(2+X)}$ kHz
X = 0 – 63</td><td>50%</td></tr>
</table>
At Power On Reset, execution of a Clock Stop instruction, these pins are specified as general purpose output ports.
At Power On Reset, undefined data is output. At execution of a Clock Stop instruction, the value of the general purpose output port is retained. At CE reset, the statuses (general purpose output port, A/D converter, CGP) which are set at that time are retained.
</td></tr>
<tr><td>22
23
24
24
25</td><td>P1C3
P1C2
P1C1
P1C0
P1C0</td><td>Output</td><td>CMOS Push–Pull</td><td>Port 1C</td><td>4-bit general purpose output port.
Output data is set via the P1C register (address 72H of BANK1) of the port register.
At Power On Reset, Undefined data is output.
At execution of a Clock Stop instruction or CE reset, the value which was output previously is kept.</td></tr>
<tr><td>26
27
28
29</td><td>P1D3 / FMIFC
P1D2 / AMIFC
P1D1 / ADC1
P1D0 / ADC0</td><td>Input</td><td>–</td><td>Port 1D</td><td>Used as a 4-bit general purpose input port, frequency counter (pins P1D3 / FMIFC and P1D2 / AMIFC), and also A/D converter (pins PID1 / ADC1 and PID0 / ADC0).
The IFCMODE register (address 12H) of the register file is used for switching the general purpose input port and A/D converter.</td></tr>
</table>

<table>
<tr><th>PIN NO.</th><th>SYMBOL</th><th>INPUT/ OUTPUT</th><th>OUTPUT MODE</th><th>PIN NAME</th><th>FUNCTION</th></tr>
<tr><td>26
27
28
29</td><td>P1D3 / FMIFC
P1D2 / AMIFC
P1D1 / ADC1
P1D0 / ADC0</td><td>Input</td><td>–</td><td>Port 1D</td><td>
The ADCCH register (address 14H) of the register file is used for switching the general input port and A/D converter.

(1) When the port is used as a 4-bit general purpose input port
The P1D register (address 73H of BANK1) of the port register is used for reading input data.
(2) When the port is used as a frequency counter (P1D3 / FMIFC and P1D2 / AMIFC)
Using the IFCMODE register of the register file, pins P1D3 / FMIFC and P1D2 / AMIFC can be used as frequency test pins. The following frequencies can be tested.

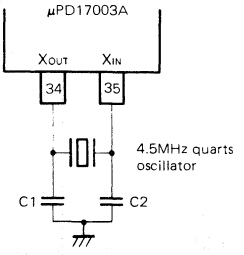
<table>
<tr><th>Input pin</th><th>Input frequency</th><th>Input oscillation</th></tr>
<tr><td>P1D3 / FMIFC</td><td>5 to 15 MHZ</td><td>0.3 Vp-p</td></tr>
<tr><td>P1D2 / AMIFC</td><td>0.1 to 1 MHz</td><td>0.3 Vp-p</td></tr>
</table>
As the test method, the frequency input within the gate time (1 ms, 4 ms, 8 ms, open) is counted by a 16-bit counter. However, the value divided by 2 is counted for the P1D3 / FMIFC pin.
At termination of the test (when the gate is closed), an interrupt request can be issued.
These functions can be used at detection of broadcast station by counting the intermediate frequency.
When the port is used as a frequency counter, cut the direct current section of the input signal with a condenser because an alternate current amplifier is used for input.
</td></tr>
</table>

PIN NO.	SYMBOL	INPUT/ OUTPUT	OUTPUT MODE	PIN NAME	FUNCTION
26 27 28 29	$P1D_3$ / FMIFC $P1D_2$ / AMIFC $P1D_1$ / ADC_1 $P1D_0$ / ADC_0	Input	–	Port 1D	The pin which was selected is used as an intermediate electric potential (about 1/2 V_{DD}). Pins which are not selected can be used as a general purpose input port. The alternate current ampilfier must be initialized by a program as required because it is not set to Disabled (prohibited state) even if the CE pin (pin number 13) is set to a Low level (if the amplifier is operating, the current consumed may increase the noise factor). Since the IFCMODE register also specifies an external gate counter ($P1A_0$ / FCG pin) and clock generator port ($P1B_0$ / CGP pin), the frequency counter, external gate counter, and clock generator port cannot be used concurrently. (3) **When the port is used as an A/D converter (pins $P1D_1$ / ADC_1 and $P1D_0$ / ADC_0)** The port can be used as an A/D converter of 6 bits by the ADCCH register (address 14H) of the register file. The A/D converter can use six channels by switching pins POD_3 / ADC_5 to POD_0 / ADC_2 (pin numbers from 75 to 78) in addition to pins $P1D_1$ / ACD_1 and $P1D_0$ / ACD_0. A consecutive comparison type is used as the conversion method and the reference voltage is created by dividing power supply voltage V_{DD} using the R string method.

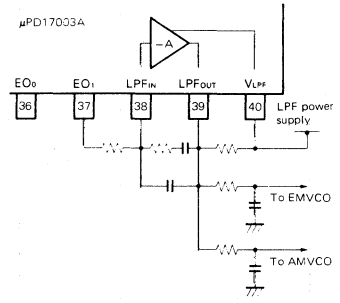
PIN NO.	SYMBOL	INPUT/ OUTPUT	OUTPUT MODE	PIN NAME	FUNCTION
26 27 28 29	P1D3 / FMIFC P1D2 / AMIFC P1D1 / ADC1 P1D0 / ADC0	Input	–	Port 1D	At Power On Reset, execution of a Clock Stop instruction, all these pins are specified as a general purpose input ports. At CE reset, the statuses (general purpose input port, frequency counter, and A/D converter) set at that time are retained.
30 41	V_{DD1} V_{DD2}	–	–	Power supply	Device power supply pin Voltage of 5 V ±10% is supplied at operation of CPU and peripheral functions. When only CPU is operating, the voltage can be reduced to 3.5 V. When the CE pin (pin number 13) is at a Low level and when a Clock Stop instruction is executed, oscillation of the quartz oscillator stops and a data set backup state is set. During the clock stop state, the voltage can be reduced to 2.2 V. When the voltage rises from 0 V to 4.5 V or when the voltage rises to 4.5 V again after decreasing to a degree less than 3.5 V (less than 2.2 V at clock stop), Power On reset is performed for the device. When Power On Reset is performed, the peripheral circuits, system registers, and register files are initialized and the program starts from address 0. The time spent from the voltage 0 V to 4.5 V must be within 500 ms. Resetting by a CE pin (CE Pin Reset) is also available in addition to Power On Reset described above for resetting a device. Since the values of timer carry FF if the register file differs between Power On Reset and CE Reset, blackout can be detected by detecting the timer carry FF.

<table>
<tr><th>PIN NO.</th><th>SYMBOL</th><th>INPUT/ OUTPUT</th><th>OUTPUT MODE</th><th>PIN NAME</th><th>FUNCTION</th></tr>
<tr><td>30
41</td><td>V_{DD1}
V_{DD2}</td><td>–</td><td>–</td><td>Power supply</td><td>A voltage higher than that of the V_{DD} pin must not be supplied to all the pins other than V_{DD} pins (V_{DD1} and V_{DD2}). In particular, care is necessary when the V_{DD} pin and the CE pin are started simultaneously. Latch-Up may occur. The V_{DD1} pin and V_{DD2} pin must be connected to an electrical potential. The V_{DD2} pin is used to supply power to quartz oscillation circuits (pins X_{IN} and X_{OUT}), error out circuits (pins EO_0 and EO_1), and low path filter circuits (pin LPF_{IN}). Pin V_{DD1} is used for supplying power to other sections.</td></tr>
<tr><td>31
32</td><td>VCOL
VCOH</td><td>Input</td><td>–</td><td>Local oscillation Low input

Local oscillation High input</td><td>Used for inputting local oscillation (VCO) frequency of PLL.
A direct division method (MF mode) and pulse swallow method (HF mode and VHF mode) are available as division methods and the method is specified by the PLLMODE register (address 21H) of the register file. The input pin, input frequency and division ratio by each division method are as follows.
<table>
<tr><th>Division method</th><th>Input pin</th><th>Input frequency (MHz)</th><th>Input voltage (Vp-p)</th><th>Division ratio</th></tr>
<tr><td>Direct division</td><td>VCOL</td><td>0.5 to 30</td><td>0.3</td><td>16 to $2^{16}-1$</td></tr>
<tr><td>Pulse swallow (HF)</td><td>VCOL</td><td>5 to 40</td><td>0.3</td><td>256 to $2^{16}-1$</td></tr>
<tr><td rowspan="2">Pulse swallow (VHF)</td><td rowspan="2">VCOH</td><td>9 to 150</td><td>0.3</td><td rowspan="2">256 to $2^{16}-1$</td></tr>
<tr><td>9 to 250</td><td>0.5</td></tr>
</table>
Since alternate current amplifier is used for input of these pins, the direct current section of the input signal must be cut using a condenser.
The pin specified by the PLLMODE register is used as an intermediate electrical potential (about 1/2 V_{DD}).</td></tr>
</table>

PIN NO.	SYMBOL	INPUT/ OUTPUT	OUTPUT MODE	PIN NAME	FUNCTION
31 32	VCOL VCOH	Input	–	Local oscillation Low input Local oscillation High input	Pins which are not specified are pulled down in the internal section of the device. When PLL is disabled or when the CE pin is at a Low level, these pins are pulled down in the internal section of the device. At Power On Reset or execution of a Clock Stop instruction, a PLL Disabled state is set. At CE reset, the state specified by the PLLMODE register is set.
33	GND	–	–	Ground	Ground pin of the device
34 35	X_{OUT} X_{IN}	Output Input	CMOS –	Quartz oscillator	Quartz oscillator connection pin Connects a 4.5 MHz quarts oscillator as shown below.  The values of C1 and C2 are determined by the quartz oscillator which is used. When the values of C1 and C2 are increased to values which are too high, the oscillation activation feature may deteriorate or current consumption may increase. In general, the adjustment range of a trimmer condenser for oscillation frequency adjustment increases when the oscillator is connected to the X_{IN}

PIN NO.	SYMBOL	INPUT/ OUTPUT	OUTPUT MODE	PIN NAME	FUNCTION
34 35	X_{OUT} X_{IN}	Output Input	CMOS –	Quartz oscillator	pin. However, the quartz oscillator which is actually used, including oscillation stabilizer, must be used for evaluation. An oscillation frequency cannot be adjusted accurately because of the problem at capacity, etc., if a probe is connected to the X_{OUT} pin or X_{IN} pin. Consequently, the frequency must be tested while testing the LCD driving wave form (125 Hz) or VCO oscillation frequency. Since the reference frequency of the timer of the internal section or PLL is used by dividing 4.5 MHz, if the value is shifted from 4.5 MHz, the values of the timer and reference frequency also shift in the same proportion.
36 37	EO_1 EO_0	Output	CMOS 3 states	Error out	Used as charge pump output pins of a PLL frequency synthesizer. When the value producing by dividing the local oscillation (VCO) frequency which is input to the VCOL pin (pin number 31) or VCOH pin (pin number 32) is higher than the reference frequency, a High level is output from these pins and when the value is lower than the reference frequency, a Low level is output. When the values match, floating occurs. A PLL frequency synthesizer can be structured by adding output of these pins to VCO (Voltage Controlled Oscillator) via LPF (Low Pass Filter). Either of the pins EO_1 and EO_2 can be used because the same signal is output. At a PLL Disabled state, these pins are set floating. That is, when the CE pin (pin number 13) is at a Low level or at Power On Reset, floating occurs.

PIN NO.	SYMBOL	INPUT/ OUTPUT	OUTPUT MODE	PIN NAME	FUNCTION
36 37	EO_1 EO_0	Output	CMOS 3 states	Error out	The PLL frequency synthesizer can detect a PLL unlocked state by the PLLULJDG register (address 05H) of the register file. Four types of time (0.5 μs, 1 μs, 2 μs, and Disable) can be selected as the delay time for detecting the PLL unlocated state using the PLULDLY register (address 15H) of the register file.
38 39 40	LPF_{IN} LPF_{OUT} V_{LPF}	Input Output –	– N-ch open drain –	LPF Amplifier	Pins for a built-in CMOS operation amplifier for LPF (Low Pass Filter) Examples of an internal equivalent circuit of each pin and application of circuit are shown below. 

PIN NO.	SYMBOL	INPUT/ OUTPUT	OUTPUT MODE	PIN NAME	FUNCTION
38	LPF_{IN}	Input	–	LPF Amplifier	Pull-Up resistance is required for the LPF_{OUT} pin because of N-ch open drain output. The resisting pressure is 16 V Max. A voltage higher than that of the LPF_{OUT} pin must be supplied to the V_{LPF} pin (16 V Max). At a PLL Disabled State, the LPF_{IN} pin is pulled up in the device internal section.
39	LPF_{OUT}	Output	N-ch open drain		
40	V_{LPF}	–	–		
42	$P2A_0$	Output	CMOS Push-Pull	Port 2A	1-bit general purpose output port. Output data is set via the P2A register (address 70H of BANK2) of the port register. At Power On Reset, undefined data is output. At execution of a Clock Stop instruction or CE reset, the value which was output previously is kept.
43 44	COM_1 COM_0	Output	CMOS 3-value output	Common signal	Common signal output pins of the LCD controller/driver. The duty, bias, frame frequency, and driving voltage of the LCD controller/ driver are 1/2, 1/2, 250 Hz, and V_{DD} respectively. Display of up to 60 dots can be performed by the matrix with pins LCD_0 / $P0Y_0$ / KS_0 to LCD_{29} / $P0F_3$. Three types of voltages, 0, 1/2 V_{DD}, and V_{DD} are output from these pins. The light of the dot from which a potential difference of $\pm V_{DD}$ is produced between these pins and pins LCD_0 / $P0Y_0$ / KS_0 to LCD_{29} / $P0F_3$ comes on. When a Display Off mode is set by the LCDMODE register (address 10H of the LCDMODE register of the register file), a Low level is output at Power On Reset or execution of a Clock Stop instruction. At CE Reset, the state is kept if the mode is a Display On mode.

PIN NO.	SYMBOL	INPUT/ OUTPUT	OUTPUT MODE	PIN NAME	FUNCTION
45 to 48	LCD_{29} / $P0F_3$ to LCD_{26} / $P0F_C$	Output	CMOS Push-Pull	LCD segment signal	Used for segment signal output (pins LCD_{29} / $P0F_3$ to LCD_0 / $P0Y_0$ / KS_0) of a LCD controller/driver, key source signal output (pins LCD_{15} / $P0Y_{15}$ / KS_{15} to LCD_0 / $P0Y_0$ / KS_0), and also as a general output port (LCD_{29} / $P0F_3$ to LCD_0 / $P0Y_0$ / KS_0). The LCDMODE register (address 10H) and LCDPORT register (address 11H) are used for outputting segment signals and key source signals, and switching general purpose output ports. (1) **When the pins are used for segment signal output of a LCD controller/driver (pins LCD_{29} / $P0F_3$ to LCD_0 / $P0Y_0$ / KS_0)** The duty, bias, and frame frequency (segment signal output 125 Hz) of a LCD controller/driver are 1/2, 1/2, and 250 Hz respectively. Display of up to 60 dots is enabled by using a matrix of these segment signal output pins, the COM_0 pin, and COM_1 pin (numbers 43 and 44). The light of the dot from which a potential difference of $\pm V_{DD}$ is produced between these segment signal output pins, and COM_0 and COM_1 pins comes on. Display data of an LCD controller/driver is set via LCD dot registers (addresses 60H to 6EH of BANK0). Data can also be set by LCD group registers (addresses 08H to 0FH) via a data buffer. A Display On mode and Display Off mode of a LCD controller/driver is set by the LCDMODE register of the register file.
49 to 52	LCD_{25} / $P0E_3$ to LCD_{22} / $P0E_0$				
53 to 58	LCD_{21} / $P0X_5$ to LCD_{16} / $P0X_0$				
59 to 74	LCD_{15} / $P0Y_{15}$ / KS_{15} to LCD_0 / $P0Y_0$ / KS_0				

PIN NO.	SYMBOL	INPUT/ OUTPUT	OUTPUT MODE	PIN NAME	FUNCTION
45 to 48	LCD_{29} / $P0F_3$ to LCD_{26} / $P0F_0$	Output	CMOS Push-Pull	LCD segment signal	In Display Off mode, these segment signal output pins output a Low level. However, for pins which are specified for a general purpose output port by the LCDPORT register of the register file, data of the output port is output regardless of the display mode, On or Off. Sixteen pins from LCD_{15} / $P0Y_{15}$ / KS_{15} to LCD_0 / $P0Y_0$ / KS_0 are also used for key source signal output of a key matrix as described in (2) and an LCD segment signal and a key source signal can be output concurrently. (2) **When the pins are used as a key source signal of a key matrix (pins LCD_{15} / $P0Y_{15}$ / KS_{15} to LCD_0 / $P0Y_0$ / KS_0)** Using the LCDMODE register of the register file, sixteen pins from LCD_{15} / $P0Y_{15}$ / KS_{15} to LCD_0 / $P0Y_0$ / KS_0 can be used as a key source output signal. A key source signal is output with a LCD segment signal in time sharing mode (key source signal output time 220 μs). When a key source signal is used, pins $P0D_3$ / ADC_5 to $P0D_0$ / ADC_2 (pin numbers 75 to 78) are used as the return signal input pins. Consequently, a key matrix of 16 key sources and 4 key input (up to 64) can be structured. A key source signal is output every 4 ms. Output data of a key source signal is set by the KSR register (address 42H) via a data buffer.
49 to 52	LCD_{25} / $P0E_3$ to LCD_{22} / $P0E_0$				
53 to 58	LCD_{21} / $P0X_5$ to LCD_{16} / $P0X_0$				
59 to 74	LCD_{15} / $P0Y_{15}$ / KS_{15} to LCD_0 / $P0Y_0$ / KS_0				

PIN NO.	SYMBOL	INPUT/ OUTPUT	OUTPUT MODE	PIN NAME	FUNCTION
45 to 48	LCD_{29} / $P0F_3$ to LCD_{26} / $P0F_0$	Output	CMOS Push-Pull	LCD segment signal	When the LCD controller/driver is in Display Off mode (segment signal output = Low level) and when these pins are specified for a general purpose output port, a key source signal is not output. (3) **When the pins are used for a general purpose output port** Each pin can be specified for an output port as listed in the following table using the LCDPORT register (address 11H) of the register file.
49 to 52	LCD_{25} / $P0E_3$ to LCD_{22} / $P0E_0$				
53 to 58	LCD_{21} / $P0X_5$ to LCD_{16} / $P0X_0$				
59 to 74	LCD_{15} / $P0Y_{15}$ / KS_{15} to LCD_0 / $P0Y_0$ / KS_0				

Pin number	Pin name	Port name	Number bit
45 to 48	LCD_{29} / $P0F_3$ to LCD_{26} / $P0F_0$	Port 0F	4 bits
49 to 52	LCD_{25} / $P0E_3$ to LCD_{22} / $P0E_0$	Port 0E	4 bits
53 to 58	LCD_{21} / $P0X_5$ to LCD_{16} / $P0X_0$	Port 0X	6 bits
59 to 74	LCD_{15} / $P0Y_{15}$ / KS_{15} to LCD_0 / $P0Y_0$ / KS_0	Port 0Y	16 bits

Port 0F, Port 0E, Port 0X, and Port 0Y can be specified as general purpose output ports individually. Pins which are not specified for a general purpose output port can be used as LCD segment signal output pins.
Output data of each output port is set as listed below.

<table>
<tr><th>PIN NO.</th><th>SYMBOL</th><th>INPUT/ OUTPUT</th><th>OUTPUT MODE</th><th>PIN NAME</th><th>FUNCTION</th></tr>
<tr>
<td>45
to
48

49
to
52

53
to
58

59
to
74</td>
<td>LCD_{29} / $P0F_3$
to
LCD_{26} / $P0F_0$

LCD_{25} / $P0E_3$
to
LCD_{22} / $P0E_0$

LCD_{21} / $P0X_5$
to
LCD_{16} / $P0X_0$

LCD_{15} / $P0Y_{15}$ / KS_{15}
to
LCD_0 / $P0Y_0$ / KS_0</td>
<td>Output</td>
<td>CMOS Push-Pull</td>
<td>LCD segment signal</td>
<td>
<table>
<tr><th>Port name</th><th>Setting output data</th></tr>
<tr><td>Port 0F</td><td>• P0F register (address 6DH of BANK0)
Used also for the LCDD13 register of the LCD dot register</td></tr>
<tr><td>Port 0E</td><td>• P0E register (Address 6BH of BANK0)
Used also for the LCDD11 register of the LCD dot register</td></tr>
<tr><td>Port 0X</td><td>• P0XH and P0XL registers (Addresses 69H and 68H of BANK0)
Used also for the LCDD9 and LCDD8 registers of the LCD dot register
• Set by the P0X group register (0CH) via a data buffer</td></tr>
<tr><td>Port 0Y</td><td>• Set by a 0Y group register (42H) via a data buffer</td></tr>
</table>

At Power On Reset or execution of Clock Stop instruciton, all of these pins are specified for segment signal output and set to a Display Off mode. Consequently a Low level is output from all these pins.
At CE Reset, the statuses (segment signal output, key source signal output, and general purpose output port) which are set at that time are retained.
</td>
</tr>
</table>

PIN NO.	SYMBOL	INPUT/ OUTPUT	OUTPUT MODE	PIN NAME	FUNCTION
75 76 77 78	$P0D_3$ / ADC_5 $P0D_2$ / ADC_4 $P0D_1$ / ADC_3 $P0D_0$ / ADC_2	Input	(Pull-Down Input with resistance)	Port 0D	Used for a 4-bit general purpose input port and also LCD segment key source signal return input, and also A/D converter input. The ADCCH register (address 14H) of the register file is used for switching the general purpose port and A/D converter. The pins $P0D_3$ / ADC_5 to $P0D_0$ / ADC_2 contain pull-down resistance so that they can be used as key return signal input pins of a key matrix. (1) **When the pins are used for general purpose input ports** Input data is read via the P0D register (address 72H of BANK0) of the port register. When pins are used for a general input port, the built-in pull down resistance is always set to ON. (2) **When the pins are used for key source signal return input of an LCD segment** When an LCD segment pins is used for key source, the built-in pull down resistance is set to ON only during output of a key source signal (220 μs) and the resistance is set to OFF during output of an LCD segment signal. The signals which were input to these pins during output of key source signals are fetched as key input data. Consequently, these pins must be used when a LCD segment signal output is used as the key source signal.

PIN NO.	SYMBOL	INPUT/ OUTPUT	OUTPUT MODE	PIN NAME	FUNCTION
75 76 77 78	P0D3 / ADC5 P0D2 / ADC4 P0D1 / ADC3 P0D0 / ADC2	Input	(Pull-Down Input with resistance)	Port 0D	(3) **When pins are used as an A/D converter** By the ADCCH register (address 14H) of the register file, the port can be used as a 6-bit A/D converter. A consecutive comparison method by a program is used as the A/D converter conversion method and the reference voltage is created by dividing power supply voltage V_{DD} using the R string method. An A/D converter can be used by switching six channels, pins P1D1 / ADC1 and P1D0 / ADC0 (pin numbers 28 and 29) in addition to pins from P0D3 / ADC5 to P0D0 / ADC2. The channel used is specified by the ADCCH register of the register file. The other five channels which are not specified for the A/D converter can be used as a general purpose input port. For the built-in pull-down resistance, only the pin which was set is set to OFF when it is set to A/D converter input by the ADCCH register. At Power On Reset or execution of a Clock Stop instruction, the pins are specified for a general purpose input port. At CE Reset, the status (general purpose input port, LCD segment key source, return input, and A/D converter) which are set at that point are retained.

1.2 NOTES ON USING A GENERAL PURPOSE PORT

1.2.1 Port Register Data Set

The port registers (registers P0A to P2A) on data memory are used for reading input data or setting output data of each of the ports, Port 0A, Port 0B, Port 0C, Port 0D, Port 1A, Port 1B, Port 1C, and Port 2A.

In this case, the $P0A_3$ pin of Port 0A corresponds to the highest bit of port register P0A and the $P0A_0$ pin corresponds to the lowest bit.

These apply also to Port 0B, Port 0C, Port 0D, Port 1A, Port 1B, Port 1C, Port 1D, and Port 2A. Output data of Port 0E, Port 0F, Port 0X, and Port 0Y is set by the LCD group register via the LCD dot register or a data buffer on the data memory.

1.2.2 Input/Output Ports (Port 0A, Port 0B, Port 0C, and Port 1A)

(1) When each port is specified as an input port

By executing an instruction (the address of the port register is specified for m of SKT m, #i, or ADD r, m) for reading the contents of each port register in the data memory, the status of each port pin is used as the value of the port register.

When an instruction (specified for r of MOV m, #i or ADD r, m) for writing data to each port register is executed, the value is written to the output data latch circuit.

(2) When each port is specified as an output port

When an instruction for writing data to each port register is executed, the value is written to the output data latch circuit and is output from each pin.

When an instruction for reading the contents of each port register is executed, the content of output data latch are used as the value of the port register. However, for pins P0A3/SDA and P0A2/SCL, the pin status is read as it is when the contents of the port register are read and the status may be different from the output data.

At Power On Reset, CE Reset, or execution of a Clock Stop instruction, all of these pins are set for input ports.

Since the contents of the output data latch circuit are undefined at Power On Reset, a Write instruction must be executed for the port register before setting data to the output port. Otherwise, undefined data is output. At CE Reset or execution of a Clock Stop instruction, the contents of the output data latch circuit do not change.

1.2.3 Output Ports (Port 1B, Port 1C, Port 0F, Port 0E, Port 0X, and Port 0Y)

An output port is used for writing the value of the port register to the output data latch circuit by executing an instruction for writing data in a port register and outputting data from each pin.

When a Read instruction is executed for a port register value, the port register value is set as the status of the output data latch circuit.

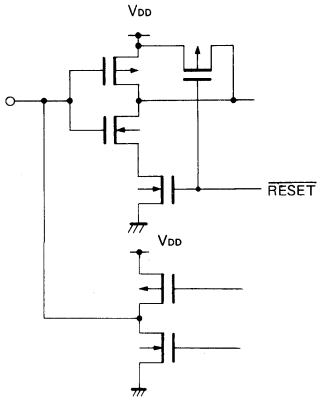
At Power On Reset, undefined data is output.

At CE Reset, the previous output data is kept at execution of a Clock Stop instruction. However, Port 0E, Port 0F, Port 0X, and Port 0Y output a Low level automatically at Power On Reset and at execution of a Clock Stop instruction.

1.3 PIN EQUIVALENT CIRCUITS

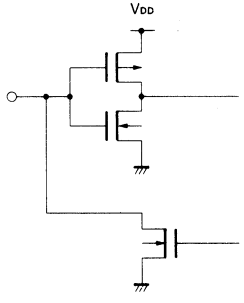
1.3.1 P0A ($P0A_1$ / $\overline{SCK_1}$, $P0A_0$ / SO_1)
P0B ($P0B_3$ / SI_1, POB_2 / $\overline{SCK_2}$, POB_1 / SO_2, $P0B_0$ / SI_2)
P0C ($P0C_3$, $P0C_2$, $P0C_1$, $P0C_0$) (*1)
P1A ($P1A_3$, $P1A_2$, $P1A_1$, and $P1A_0$)

(Input/output)

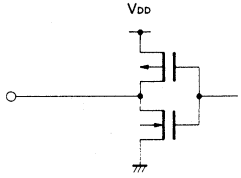


*1: The $\overline{RESET}$ signal is not provided to P0C.

1.3.2 P0A ($P0A_3$ / SDA and $P0A_2$ / SCL) (Input/Output)

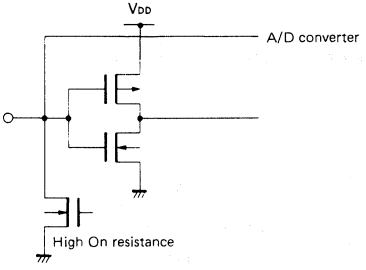


1.3.3 P1B ($P1B_0$ / CGP)
P1C ($P1C_3$, $P1C_2$, $P1C_1$, and $P1C_0$)
P2A ($P2A_0$)
LCD_0 / $P0Y_0$ / KS_0 to LCD_{29} / $P0F_3$ } (Output)

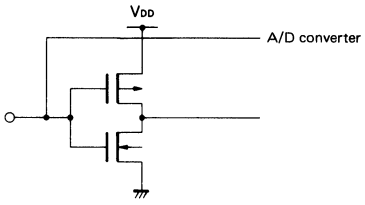


1.3.4 P1B ($P1B_3$ / PWM_2 and $P1B_2$ / PWM_1, and $P1B_1$ / PWM_0) (Output)

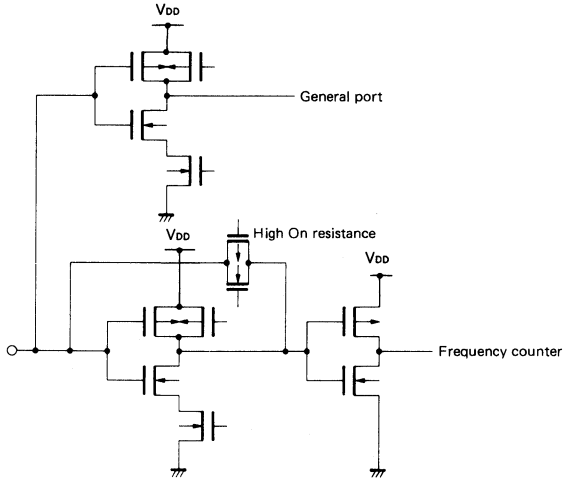
1.3.5 P0D ($P0D_3$ / ADC_5, $P0D_2$ / ADC_4, $P0D_1$ / ADC_3, and $P0D_0$ / ADC_2) (Input)



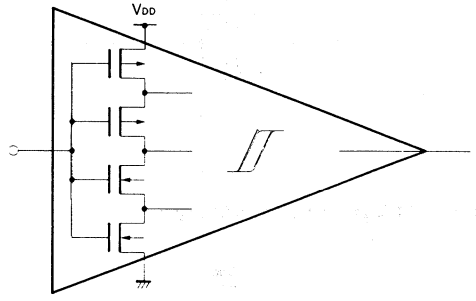
1.3.6 P1D (P1D1 / ADC1 and P1D0 / ADC0) (Input)



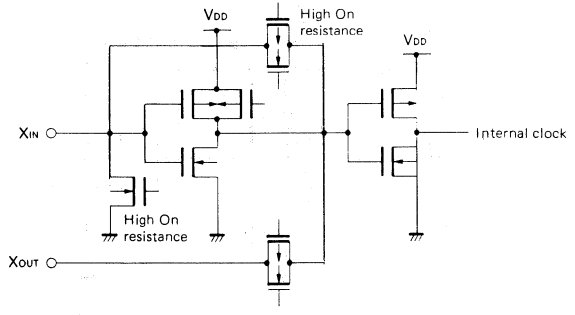
1.3.7 P1D (P1D3 / FMIFC, and P1D2 / AMIFC) (Input)



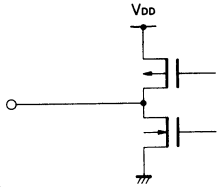
1.3.8 **CE**
INT_1 } **(Schmit trigger input)**
INT_0



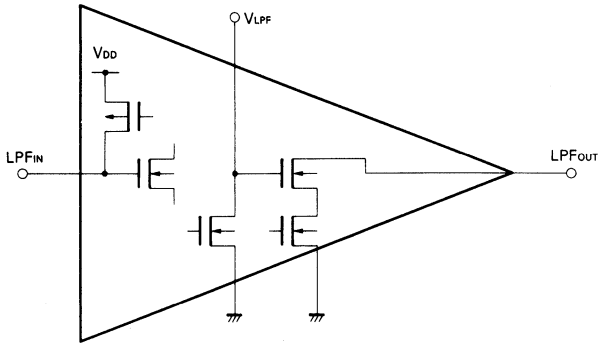
1.3.9 **X_{OUT} (output) and X_{IN} (input)**



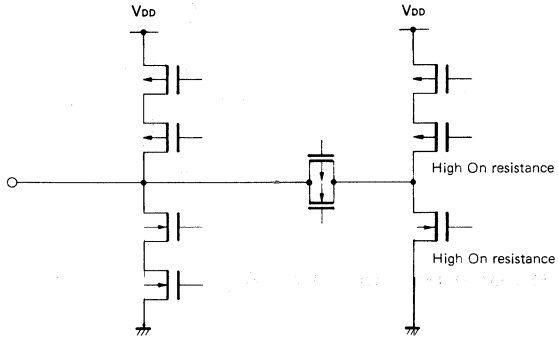
1.3.10 EO_1, EO_0 (Output)



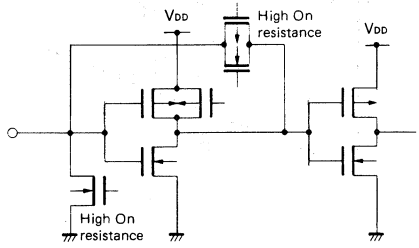
1.3.11 LPF_{IN} (input), LPF_{OUT} (output), and V_{LPF}



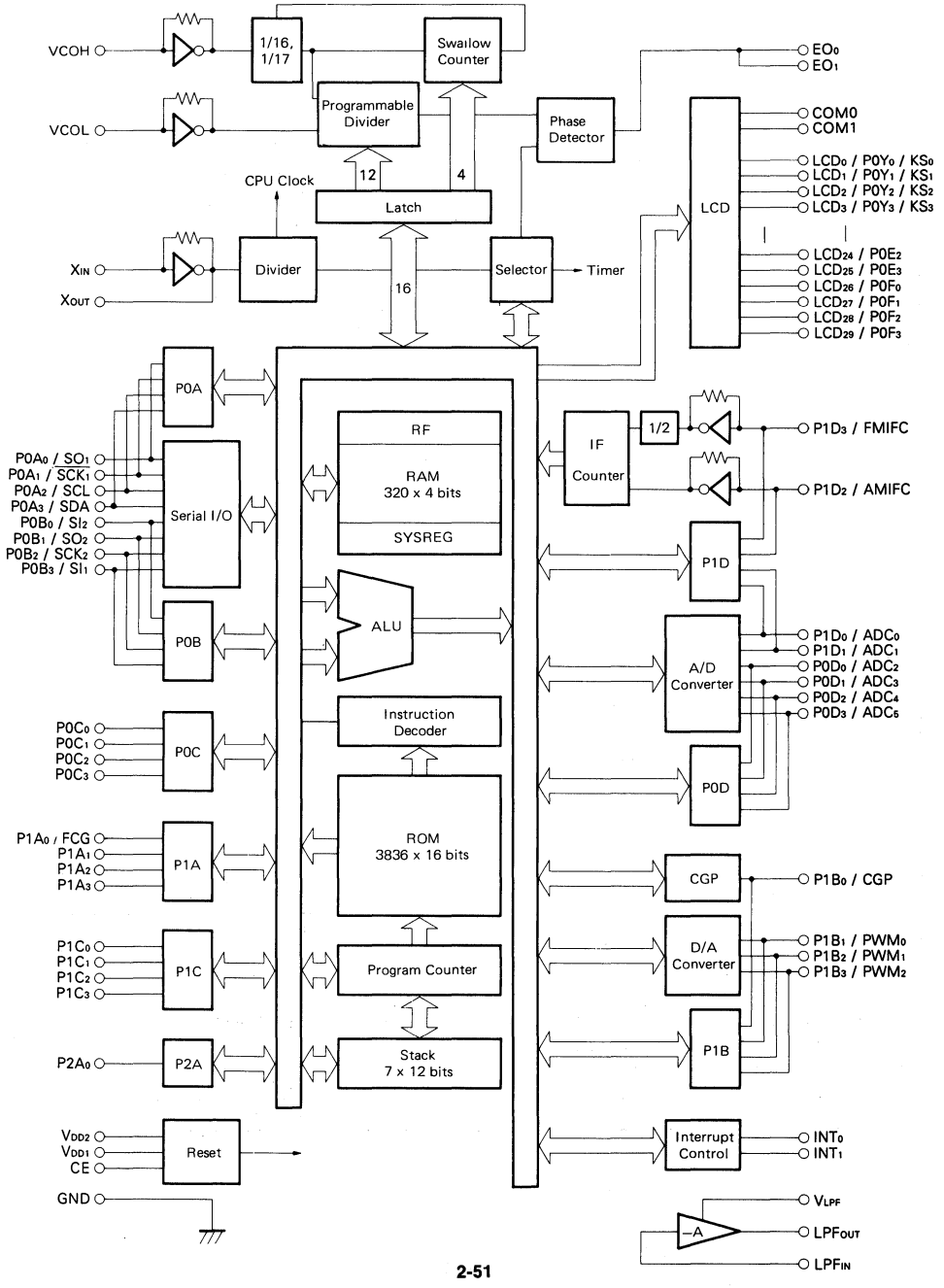
1.3.12 **COM1 / COM0** **(Output)**



1.3.13 **VCOH / VCOL** **(Input)**



2. BLOCK DIAGRAM



μPD17003A INSTRUCTIONS

INSTRUCTION SET

b_{14} b_{13} b_{12} b_{11}	b_{15}	0	1
0 0 0 0	0	ADD r, m	ADD m, #i
0 0 0 1	1	SUB r, m	SUB m, #i
0 0 1 0	2	ADDC r, m	ADDC m, #i
0 0 1 1	3	SUBC r, m	SUBC m, #i
0 1 0 0	4	AND r, m	AND m, #i
0 1 0 1	5	XOR r, m	XOR m, #i
0 1 1 0	6	OR r, m	OR m, #i
0 1 1 1	7	INC AR INC IX MOVT DBF, @AR BR @AR CALL @AR RET RETSK EI DI RETI PUSH AR POP AR GET DBF, p PUT p, DBF PEEK WR, rf POKE rf, WR RORC r STOP 0 HALT h NOP	
1 0 0 0	8	LD r, m	ST m, r
1 0 0 1	9	SKE m, #i	SKGE m, #i
1 0 1 0	A	MOV @r, m	MOV m, @r
1 0 1 1	B	SKNE m, #i	SKLT m, #i
1 1 0 0	C	BR addr (page0)	CALL addr (page0)
1 1 0 1	D	BR addr (page1)	MOV m, #i
1 1 1 0	E		SKT m, #n
1 1 1 1	F		SKF m, #n

LIST OF INSTRUCTIONS

Legends	:	
M	:	Data memory address
m	:	Data memory address excluding bank
m_H	:	Data memory row address
m_L	:	Data memory column address
R	:	General register address
r	:	General register column address
RP	:	General register pointer
RF	:	Register file
rf	:	Register file address
rf_H	:	Register file address (upper 3 bits)
rf_L	:	Register file address (lower 3 bits)
AR	:	Address register
IX	:	Index register
IXE	:	Index enable flag
DBF	:	Data buffer
WR	:	Window register
MP	:	Data memory row address pointer
MPE	:	Memory pointer enable flag
PE	:	Peripheral register
P	:	Peripheral address
P_H	:	Peripheral address (upper 3 bits)
P_L	:	Peripheral address (lower 4 bits)
PC	:	Program memory counter
SP	:	Stack pointer
STACK	:	Stack value indicated by stack pointer
$STACK_{PC}$	:	Program counter value indicated by stack pointer
BANK	:	Bank register
$(ROM)_{PC}$	:	Program memory data indicated by program memory counter
INTEF	:	Interrupt enable flag
SGR	:	Program memory segment register
i	:	Immediate data (4 bits)
n	:	Bit position (4 bits)
addr	:	Program memory address (11 bits)
CY	:	Carry flag
c	:	Carry
b	:	Borrow
h	:	Halt canceling condition
[ ]	:	Data memory or register address
( )	:	Data memory or register value

Instruction	Mnemonic	Operand	Operation	Machine code			
				Operation code			
Add instruction	ADD	r, m	(R) ← (R) + (M)	00000	m_H	m_L	r
		m, #i	(M) ← (M) + i	10000	m_H	m_L	i
	ADDC	r, m	(R) ← (R) + (M) + (CY)	00010	m_H	m_L	r
		m, #i	(M) ← (M) + i + (CY)	10010	m_H	m_L	i
	INC	AR	(AR) ← (AR) + 1	00111	000	1001	0000
		IX	(IX) ← (IX) + 1	00111	000	1000	0000
Subtract instruction	SUB	r, m	(R) ← (R) − (M)	00001	m_H	m_L	r
		m, #i	(M) ← (M) − i	10001	m_H	m_L	i
	SUBC	r, m	(R) ← (R) − (M) − (CY)	00011	m_H	m_L	r
		m, #i	(M) ← (M) − i − (CY)	10011	m_H	m_L	i
Compare instruction	SKE	m, #i	(M) − i, skip if zero	01001	m_H	m_L	i
	SKGE	m, #i	(M) − i, skip if not borrow	11001	m_H	m_L	i
	SKLT	m, #i	(M) − i, skip if borrow	11011	m_H	m_L	i
	SKNE	m, #i	(M) − i, skip if not zero	01011	m_H	m_L	i
Logical instruction	AND	m, #i	(M) ← (M) AND i	10100	m_H	m_L	i
		r, m	(R) ← (R) AND (M)	00100	m_H	m_L	r
	OR	m, #i	(M) ← (M) OR i	10110	m_H	m_L	i
		r, m	(R) ← (R) OR (M)	00110	m_H	m_L	r
	XOR	m, #i	(M) ← (M) XOR i	10101	m_H	m_L	i
		r, m	(R) ← (R) XOR (M)	00101	m_H	m_L	r
Transfer instruction	LD	r, m	(R) ← (M)	01000	m_H	m_L	r
	ST	m, r	(M) ← (R)	11000	m_H	m_L	r
	MOV	@r, m	if MPE = 1 : [(MP), (R)] ← (M) if MPE = 0 : [(m_H), (R)] ← (M)	01010	m_H	m_L	r
		m, @r	if MPE = 1 : (M) ← [(MP), (R)] if MPE = 0 : (M) ← [(m_H), (R)]	11010	m_H	m_L	r
		m, #i	(M) ← i	11101	m_H	m_L	i
	MOVT	DBF, @AR	($STACK_{PC}$) ← (PC), (PC) ← (AR) (DBF) ← (ROM_{PC}), (PC) ← ($STACK_{PC}$)	00111	000	0001	0000
	PUSH	AR	(SP) ← (SP) − 1, ($STACK_{PC}$) ← (AR)	00111	000	1101	0000
	POP	AR	(AR) ← ($STACK_{PC}$), (SP) ← (SP) + 1	00111	000	1100	0000
	PEEK	WR, rf	(WR) ← (RF)	00111	rf_H	0011	rf_L
	POKE	rf, WR	(RF) ← (WR)	00111	rf_H	0010	rf_L
	GET	DBF, p	(DBF) ← (PE)	00111	p_H	1011	p_L
	PUT	p, DBF	(PE) ← (DBF)	00111	p_H	1010	p_L
Decision instruction	SKT	m, #n	if $(M)_n$ = all "1", then skip	11110	m_H	m_L	n
	SKF	m, #n	if $(M)_n$ = all "0", then skip	11111	m_H	m_L	n
Branch instruction	BR	addr	(PC) ← addr, $(PC)_{\pm 11}$ ← 0	01100	addr (11 bits)		
			(PC) ← addr, $(PC)_{\pm 11}$ ← 1	01101			
		@AR	(PC) ← (AR)	00111	000	0100	0000

Instruction	Mnemonic	Operand	Operation	Machine code			
				Operation code			
Shift	RORC	r	(CY) ← (R)$_{b3}$ → (R)$_{b2}$ → (R)$_{b1}$ → (R)$_{b0}$ → (CY)	00111	000	0111	r
Subroutine instruction	CALL	addr	(SP) ← (SP) − 1, (STACK$_{PC}$) ← ((PC) + 1), (PC)$_{\#11}$ ← 0, (PC) ← addr	11100	addr (11 bits)		
		@AR	(SP) ← (SP) − 1, (STACK$_{PC}$) ← ((PC) + 1), (PC) ← (AR)	00111	000	0101	0000
	RET		(PC) ← (STACK$_{PC}$), (SP) ← (SP) + 1	00111	000	1110	0000
	RETSK		(PC) ← (STACK$_{PC}$), (SP) ← (SP) + 1, skip	00111	001	1110	0000
	RETI		(PC), (BANK), (IXE) ← (STACK), (SP) ← (SP) + 1	00111	100	1110	0000
Interrupt	EI		INTEF ← 1	00111	000	1111	0000
	DI		INTEF ← 0	00111	001	1111	0000
Others	STOP	0	stop clock if CE = low	00111	010	1111	0000
	HALT	h	halt	00111	011	1111	h
	NOP		No operation	00111	100	1111	0000

ASSEMBLER (AS17K) BUILT-IN MACRO INSTRUCTION

Legend

flag	:	**One of flag1-flagn**
flag1-flagn	:	**Flag names indicated by reserved words**
n	:	**Number**
< >	:	**Omission allowed**

	Mnemonic	Operand	n	Operation
	SKTn	flag1, ···flagn	1 ≦ n ≦ 4	if (flag1) ~ (flagn) = all "1", then skip
	SKFn	flag1, ···flagn	1 ≦ n ≦ 4	if (flag1) ~ (flagn) = all "0", then skip
	SETn	flag1, ···flagn	1 ≦ n ≦ 4	(flag1) ~ (flagn) ← 1
	CLRn	flag1, ···flagn	1 ≦ n ≦ 4	(flag1) ~ (flagn) ← 0
	NOTn	flag1, ···flagn	1 ≦ n ≦ 4	if (flag) = "0", then (flag) ← 1 & if (flag) = "1", then (flag) ← 0
	INITFLG	<NOT>flag1, ···<NOT>flagn		if description = NOT flag, (flag) ← 0 if description = flag, (flag) ← 1
	BANKn		0 ≦ n ≦ 2	(BANK) ← n, 0 ≦ n ≦ 2

μPD17003A RESERVED WORDS

LIST OF RESERVED WORDS

System Register (SYSREG)

Reserved word	Type	Address	Read/ Write	Function
AR3	MEM	0.74H	R	Address register bit b_{15}-b_{12}
AR2	MEM	0.75H	R	Address register bit b_{11}-b_8
AR1	MEM	0.76H	R/W	Address register bit b_7-b_4
AR0	MEM	0.77H	R/W	Address register bit b_3-b_0
WR	MEM	0.78H	R/W	Window register
BANK	MEM	0.79H	R/W	Bank register
IXH	MEM	0.7AH	R/W	Index register high
MPH	MEM	0.7AH	R/W	Memory pointer high
MPE	FLG	0.7AH.3	R/W	Memory pointer enable flag
IXM	MEM	0.7BH	R/W	Index register middle
MPL	MEM	0.7BH	R/W	Memory pointer low
IXL	MEM	0.7CH	R/W	Index register low
RPH	MEM	0.7DH	R/W	General register pointer high
RPL	MEM	0.7EH	R/W	General register pointer low
PSW	MEM	0.7FH	R/W	Program status word
BCD	FLG	0.7EH.0	R/W	BCD flag
CMP	FLG	0.7FH.3	R/W	Compare flag
CY	FLG	0.7FH.2	R/W	Carry flag
Z	FLG	0.7FH.1	R/W	Zero flag
IXE	FLG	0.7FH.0	R/W	Index enable flag

26.1.2 Data buffer (DBF)

Reserved word	Type	Address	Read/ Write	Function
DBF3	MEM	0.0CH	R/W	DBF bit b_{15} to b_{12}
DBF2	MEM	0.0DH	R/W	DBF bit b_{11} to b_8
DBF1	MEM	0.0EH	R/W	DBF bit b_7 to b_4
DBF0	MEM	0.0FH	R/W	DBF bit b_3 to b_0

LCD dot data register

Reserved word	Type	Address	Read/ Write	Function
LCDD0	MEM	0.60H	R/W	LCD data register
LCDD1	MEM	0.61H	R/W	LCD data register
LCDD2	MEM	0.62H	R/W	LCD data register
LCDD3	MEM	0.63H	R/W	LCD data register
LCDD4	MEM	0.64H	R/W	LCD data register
LCDD5	MEM	0.65H	R/W	LCD data register
LCDD6	MEM	0.66H	R/W	LCD data register
LCDD7	MEM	0.67H	R/W	LCD data register
LCDD8	MEM	0.68H	R/W	LCD data register
LCDD9	MEM	0.69H	R/W	LCD data register
LCDD10	MEM	0.6AH	R/W	LCD data register
LCDD11	MEM	0.6BH	R/W	LCD data register
LCDD12	MEM	0.6CH	R/W	LCD data register
LCDD13	MEM	0.6DH	R/W	LCD data register
LCDD14	MEM	0.6EH	R/W	LCD data register

General port register

Reserved word	Type	Address	Read/ Write	Function
P0A3	FLG	0.70H.3	R/W	Port 0A bit b_3
P0A2	FLG	0.70H.2	R/W	Port 0A bit b_2
P0A1	FLG	0.70H.1	R/W	Port 0A bit b_1
P0A0	FLG	0.70H.0	R/W	Port 0A bit b_0
P0B3	FLG	0.71H.3	R/W	Port 0B bit b_3
P0B2	FLG	0.71H.2	R/W	Port 0B bit b_2
P0B1	FLG	0.71H.1	R/W	Port 0B bit b_1
P0B0	FLG	0.71H.0	R/W	Port 0B bit b_0
P0C3	FLG	0.72H.3	R/W	Port 0C bit b_3
P0C2	FLG	0.72H.2	R/W	Port 0C bit b_2
P0C1	FLG	0.72H.1	R/W	Port 0C bit b_1
P0C0	FLG	0.72H.0	R/W	Port 0C bit b_0
P0D3	FLG	0.73H.3	R	Port 0D bit b_3
P0D2	FLG	0.73H.2	R	Port 0D bit b_2
P0D1	FLG	0.73H.1	R	Port 0D bit b_1
P0D0	FLG	0.73H.0	R	Port 0D bit b_0
P0XL3	FLG	0.68H.3	R/W	Port 0X bit b_1
P0XL2	FLG	0.68H.2	R/W	Port 0X bit b_0
P0XL1	FLG	0.68H.1	R/W	Dummy
P0XL0	FLG	0.68H.0	R/W	Dummy
P0XH3	FLG	0.69H.3	R/W	Port 0X bit b_5
P0XH2	FLG	0.69H.2	R/W	Port 0X bit b_4
P0XH1	FLG	0.69H.1	R/W	Port 0X bit b_3
P0XH0	FLG	0.69H.0	R/W	Port 0X bit b_2
P0E3	FLG	0.6BH.3	R/W	Port 0E bit b_3
P0E2	FLG	0.6BH.2	R/W	Port 0E bit b_2
P0E1	FLG	0.6BH.1	R/W	Port 0E bit b_1
P0E0	FLG	0.6BH.0	R/W	Port 0E bit b_0
P0F3	FLG	0.6DH.3	R/W	Port 0F bit b_3
P0F2	FLG	0.6DH.2	R/W	Port 0F bit b_2
P0F1	FLG	0.6DH.1	R/W	Port 0F bit b_1
P0F0	FLG	0.6DH.0	R/W	Port 0F bit b_0
P1A3	FLG	1.70H.3	R/W	Port 1A bit b_3
P1A2	FLG	1.70H.2	R/W	Port 1A bit b_2
P1A1	FLG	1.70H.1	R/W	Port 1A bit b_1
P1A0	FLG	1.70H.0	R/W	Port 1A bit b_0

Reserved word	Type	Address	Read/ Write	Function
P1B3	FLG	1.71H.3	R/W	Port 1B bit b_3
P1B2	FLG	1.71H.2	R/W	Port 1B bit b_2
P1B1	FLG	1.71H.1	R/W	Port 1B bit b_1
P1B0	FLG	1.71H.0	R/W	Port 1B bit b_0
P1C3	FLG	1.72H.3	R/W	Port 1C bit b_3
P1C2	FLG	1.72H.2	R/W	Port 1C bit b_2
P1C1	FLG	1.72H.1	R/W	Port 1C bit b_1
P1C0	FLG	1.72H.0	R/W	Port 1C bit b_0
P1D3	FLG	1.73H.3	R/W	Port 1D bit b_3
P1D2	FLG	1.73H.2	R/W	Port 1D bit b_2
P1D1	FLG	1.73H.1	R/W	Port 1D bit b_1
P1D0	FLG	1.73H.0	R/W	Port 1D bit b_0
P2A3	FLG	2.70H.3	R/W	Port 2A bit b_3
P2A2	FLG	2.70H.2	R/W	Port 2A bit b_2
P2A1	FLG	2.70H.1	R/W	Port 2A bit b_1
P2A0	FLG	2.70H.0	R/W	Port 2A bit b_0

Register file (Control register)

Reserved word	Type	Address	Read/ Write	Function
SP	MEM	0.81H	R/W	Stack pointer
SIO2TS	FLG	0.82H.3	R/W	SIO_2 start flag
SIO2HIZ	FLG	0.82H.2	R/W	$SO_2/P0B_1$ select flag
SIO2CK1	FLG	0.82H.1	R/W	SIO_2 clock select bit b_1
SIO2CK0	FLG	0.82H.0	R/W	SIO_2 clock select bit b_0
IFCG	FLG	0.84H.0	R	IF counter gate status flag
PLLUL	FLG	0.85H.0	R	PLL unlock FF flag
ADCCMP	FLG	0.86H.0	R	ADC judge flag
CE	FLG	0.87H.0	R	CE pin status flag
SIO1CH	FLG	0.88H.3	R/W	SIO_1 mode select flag
SB	FLG	0.88H.2	R/W	SB/SBI select flag
SIO1MS	FLG	0.88H.1	R/W	SIO_1 clock mode select flag
SIO1TX	FLG	0.88H.0	R/W	SIO_1 TX/RX select flag
TMMD3	FLG	0.89H.3	R/W	Timer interrupt mode select flag
TMMD2	FLG	0.89H.2	R/W	Timer interrupt mode select flag
TMMD1	FLG	0.89H.1	R/W	Timer carry FF mode select flag
TMMD0	FLG	0.89H.0	R/W	Timer carry FF mode select flag
INT1	FLG	0.8FH.1	R	INT_1 pin status flag
INT0	FLG	0.8FH.0	R	INT_0 pin status flag
KSEN	FLG	0.90H.1	R/W	Key source decoder enable flag
LCDEN	FLG	0.90H.0	R/W	LCD driver enable flag
P0YON	FLG	0.91H.3	R/W	Port 0Y enable flag
P0XON	FLG	0.91H.2	R/W	Port 0X enable flag
P0EON	FLG	0.91H.1	R/W	Port 0E enable flag
P0FON	FLG	0.91H.0	R/W	Port 0F enable flag
IFCMD1	FLG	0.92H.3	R/W	IF counter mode select flag
IFCMD0	FLG	0.92H.2	R/W	IF counter mode select flag
IFCCK1	FLG	0.92H.1	R/W	IF counter clock select flag
IFCCK0	FLG	0.92H.0	R/W	IF counter clock select flag
PWM2ON	FLG	0.93H.3	R/W	PWM2 enable flag
PWM1ON	FLG	0.93H.2	R/W	PWM1 enable flag
PWM0ON	FLG	0.93H.1	R/W	PWM0 enable flag
CGPON	FLG	0.93H.0	R/W	CGP enable flag
ADCCH3	FLG	0.94H.3	R	AD mode select flag (Dummy : 0)
ADCCH2	FLG	0.94H.2	R/W	AD mode select flag
ADCCH1	FLG	0.94H.1	R/W	AD mode select flag
ADCCH0	FLG	0.94H.0	R/W	AD mode select flag

Reserved word	Type	Address	Read/ Write	Function
PLULDLY3	FLG	0.95H.3	R	PLL unlock time select flag (Dummy : 0)
PLULDLY2	FLG	0.95H.2	R	PLL unlock time select flag (Dummy : 0)
PLULDLY1	FLG	0.95H.1	R/W	PLL unlock time select flag
PLULDLY0	FLG	0.95H.0	R/W	PLL unlock time select flag
KEYJ	FLG	0.96H.0	R	Key input judge flag
TMCY	FLG	0.97H.0	R	Timer carry FF status flag
SBACK	FLG	0.98H.3	R/W	SB acknowledge flag
SIO1NWT	FLG	0.98H.2	R/W	SIO_1 not wait flag
SIO1WRQ1	FLG	0.98H.1	R/W	SIO_1 wait mode flag
SIO1WRQ0	FLG	0.98H.0	R/W	SIO_1 wait mode flag
IEG1	FLG	0.9FH.1	R/W	INT_1 interrupt edge select flag
IEG0	FLG	0.9FH.0	R/W	INT_0 interrupt edge select flag
PLLMD3	FLG	0.0A1H.3	R	PLL mode select flag (Dummy : 0)
PLLMD2	FLG	0.0A1H.2	R	PLL mode select flag (Dummy : 0)
PLLMD1	FLG	0.0A1H.1	R/W	PLL mode select flag
PLLMD0	FLG	0.0A1H.0	R/W	PLL mode select flag
IFCSTRT	FLG	0.0A3H.1	W	IF counter start flag
IFCRES	FLG	0.0A3H.0	W	IF counter reset flag
P0CGIO	FLG	0.0A7H.0	R/W	Port 0C I O select flag
SIO1SF8	FLG	0.0A8H.3	R/W	SIO_1 clock counter status flag
SIO1SF9	FLG	0.0A8H.2	R/W	SIO_1 clock counter status flag
SBSTT	FLG	0.0A8H.1	R/W	SB start condition status flag
SBBSY	FLG	0.0A8H.0	R/W	SB start stop condition status flag
IPIFC	FLG	0.0AEH.0	R/W	IF counter interrupt permission flag
IPSIO1	FLG	0.0AFH.3	R/W	SIO_1 interrupt permission flag
IPTM	FLG	0.0AFH.2	R/W	Timer interrupt permission flag
IP1	FLG	0.0AFH.1	R/W	INT_1 interrupt permission flag
IP0	FLG	0.0AFH.0	R/W	INT_0 interrupt permission flag
PLLRFMD3	FLG	0.0B1H.3	R/W	PLL reference clock select flag
PLLRFMD2	FLG	0.0B1H.2	R/W	PLL reference clock select flag
PLLRFMD1	FLG	0.0B1H.1	R/W	PLL reference clock select flag
PLLRFMD0	FLG	0.0B1H.0	R/W	PLL reference clock select flag
P1ABIO3	FLG	0.0B5H.3	R/W	$P1A_3$ I O select flag
P1ABIO2	FLG	0.0B5H.2	R/W	$P1A_2$ I O select flag
P1ABIO1	FLG	0.0B5H.1	R/W	$P1A_1$ I O select flag
P1ABIO0	FLG	0.0B5H.0	R/W	$P1A_0$ I O select flag
P0BBIO3	FLG	0.0B6H.3	R/W	$P0B_3$ I O select flag
P0BBIO2	FLG	0.0B6H.2	R/W	$P0B_2$ I O select flag
P0BBIO1	FLG	0.0B6H.1	R/W	$P0B_1$ I O select flag
P0BBIO0	FLG	0.0B6H.0	R/W	$P0B_0$ I O select flag

Reserved word	Type	Address	Read/ Write	Function
P0ABIO3	FLG	0.0B7H.3	R/W	$P0A_3$ I/O select flag
P0ABIO2	FLG	0.0B7H.2	R/W	$P0A_2$ I/O select flag
P0ABIO1	FLG	0.0B7H.1	R/W	$P0A_1$ I/O select flag
P0ABIO0	FLG	0.0B7H.0	R/W	$P0A_0$ I/O select flag
SIO1IMD3	FLG	0.0B8H.3	R	SIO_1 interrupt mode select flag (Dummy : 0)
SIO1IMD2	FLG	0.0B8H.2	R	SIO_1 interrupt mode select flag (Dummy : 0)
SIO1IMD1	FLG	0.0B8H.1	R/W	SIO_1 interrupt mode select flag
SIO1IMD0	FLG	0.0B8H.0	R/W	SIO_1 interrupt mode select flag
SIO1CK3	FLG	0.0B9H.3	R	SIO_1 shift clock select flag (Dummy : 0)
SIO1CK2	FLG	0.0B9H.2	R	SIO_1 shift clock select flag (Dummy : 0)
SIO1CK1	FLG	0.0B9H.1	R/W	SIO_1 shift clock select flag
SIO1CK0	FLG	0.0B9H.0	R/W	SIO_1 shift clock select flag
IRQIFC	FLG	0.0BEH.0	R/W	IF counter interrupt request flag
IRQSIO1	FLG	0.0BFH.3	R/W	SIO_1 interrupt request flag
IRQTM	FLG	0.0BFH.2	R/W	Timer interrupt request flag
IRQ1	FLG	0.0BFH.1	R/W	INT_1 interrupt request flag
IRQ0	FLG	0.0BFH.0	R/W	INT_0 interrupt request flag

Peripheral hardware address

Reserved word	Type	Address	Read/ Write	Function
DBF	DAT	0FH	R/W	Data buffer address of GET/PUT instruction
IX	DAT	01H	R/W	Index register address of INC instruction
ADCR	DAT	02H	R/W	A D converter VREF data register
SIO2SFR	DAT	03H	R/W	SIO_2 presettable shift register
SIO1SFR	DAT	04H	R/W	SIO_1 presettable shift register
PWMR0	DAT	05H	R/W	PWM0 data register
PWMR1	DAT	06H	R/W	PWM1 data register
PWMR2	DAT	07H	R/W	PWM2 data register
LCDR0	DAT	08H	W	LCD group data register 0
LCDR1	DAT	09H	W	LCD group data register 1
LCDR2	DAT	0AH	W	LCD group data register 2
LCDR3	DAT	0BH	W	LCD group data register 3
LCDR4	DAT	0CH	W	LCD group data register 4
P0X	DAT	0CH	W	Port 0X data register
LCDR5	DAT	0DH	W	LCD group data register 5
LCDR6	DAT	0EH	W	LCD group data register 6
LCDR7	DAT	0FH	W	LCD group data register 7
CGPR	DAT	20H	R/W	CGP data register
AR	DAT	40H	R/W	Address register address of GET PUT PUSH CALL BR MOVT INC instruction
PLLR	DAT	41H	R/W	PLL data register
KSR	DAT	42H	R/W	Key source data register
P0Y	DAT	42H	R/W	Port 0Y data register
IFC	DAT	43H	R	IF counter data register

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (Unless otherwise specified, T_a = 25 ± 2 °C)

Source voltage	V_{DD}		−0.3 to +6.0	V
Input voltage	V_I		−0.3 to V_{DD} + 0.3	V
Output voltage	V_O	Excluding $P1B_1$, to $P1B_3$, $P0A_2$, $P0A_3$ and LPF_{OUT}	−0.3 to V_{DD} +0.3	V
Output withstand voltage	V_{BDS1}	$P1B_1$ to $P1B_3$, LPF_{OUT}	18.0	V
Output withstand voltage	V_{BDS2}	$P0A_2$, $P0A_3$	V_{DD} +0.3	V
Output absorbing current	I_O		10.0	mA
Operating temperature	T_{opt}		−40 to +85	°C
Storage temperature	T_{stg}		−55 to +125	°C

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Source voltage	V_{DD1}	4.5	5.0	5.5	V	PLL and CPU are operating
Source voltage	V_{DD2}	3.5	5.0	5.5	V	PLL is OFF and CPU is operating
Data holding voltage	V_{DDR}	2.2		5.5	V	Quartz oscillator OFF
Source voltage rise time	T_{rise}			500	ms	V_{DD} = 0 4.5 V
Input amplitude	V_{in1}	0.5		V_{DD}	V_{P-P}	VCOL, V COH
Input amplitude	V_{in2}	0.5		V_{DD}	V_{P-P}	AMIFC, FMIFC
Output withstand voltage	V_{BDS}			16.0	V	P_1B_1 to $P1B_3$, LPF_{OUT}
Operating temperature	T_{opt}	−40		+85	°C	

DC CHARACTERISTICS (UNLESS OTHERWISE SPECIFIED, T_a = −40 to + 85 °C, V_{DD} = 4.5 to 5.5 V)

CHARACTERISTICS	SYMBOL	STANDARD VALUE				CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Source voltage	V_{DD1}	4.5	5.0	5.5	V	CPU and PLL are operating
Source voltage	V_{DD2}	3.5	5.0	5.5	V	CPU is operating and PLL is OFF.
Source current	I_{DD1}		1.2	2.4	mA	CPU is operating and PLL is OFF XIn pin Sinc wave Input (fin = 4.5 MHz, Vin, V_{DD}), T_a=25 °C
Source current	I_{DD2}		0.45	0.90	mA	CPU is operating, PLL is OFF, and HALT Instruction is used (20 Instructions executed per 1 ms). X↘ pin Sinc wave input fin 4.5 MHz, Vin = V_{DD}, T_a = 25°C
Data holding voltage	V_{DDR1}	3.5		5.5	V	Power failure detection by timer FF, quartz oscillator oscillating
Data holding voltage	V_{DDR2}	2.2		5.5	V	Power failure detection by timer FF, quartz oscillator not oscillating
Data holding voltage	V_{DDR3}	2.0		5.5	V	Data memory (RAM) holding
Data holding current	I_{DDR1}		2	15	μA	Quartz oscillator not oscillating T_a = 25°C
Data Holding current	I_{DDR2}		2	10	μA	Quartz oscillator not oscillating V_{DD} = 5.0 V T_a 25 °C
Intermediate level output voltage	V_{OM1}	2.3	2.5	2.7	V	COM_0 CGM_1 V_{DD} 5 V
High level input voltage	V_{IH1}	0.8 V_{DD}		V_{DD}	V	$P0A_0$, to PCA_3, $P0B_0$ to $P0B_3$, $P0C_0$ to $P0C_3$, $P1A_0$, to $P1B_3$, $P1O_0$, to $P1O_3$, CE, INT_0, INT_1
High level input voltage	V_{IH2}	0.6 V_{DD}		V_{DD}	V	$P0D_0$ to $P0O_3$
Low level input voltage	V_{IL}	0		0.2 V_{DD}	V	POA_0 to POA_3, POB_0 to POB_3, POC_0 to POC_3, POD_0, to POD_3, POA_0, to $P1C_3$, $P1D_0$ to $P1D_3$, CE, INT_0, INT_1
High level output current	I_{OH1}	−1.0	−5.0		mA	$P0A_0$ to $P0A_3$, $P0B_0$ to $P0B_3$, $P0C_0$ to $P0C_3$, $P0D_0$ to $P0D_3$, $P1C_0$ to $P1A_3$, $P1B_0$ to $P1A_3$, V_{OH} = V_{DD} −1V
High level output current	I_{OH2}	−1.0	−4.0		mA	LOD_0 to LCI_{29} EO_0 EO_1 V_{OH} = V_{DD} − 1V
Low level output current	I_{OL1}	1.0	7.0		mA	$P0A_0$ to $P0A_3$, $P0B_0$, to $P0B_3$, $P0C_0$ to $P0C_3$, $P1A_0$, to $P1A_3$, $P1C_0$, to $P1C_3$, $P1B_0$, $P2A_0$ V_{OL} 1V
Low level output current	I_{OL2}	1.0	3.5		mA	LCD_0 to LCO_{29} EO_0 = $EI0_1$ V_{OL} 1 V
Low level output current	I_{OL3}	1.0	2.0		mA	$P1B_1$ to $P1B_3$ V_{OL} 1 V
Low level output current	I_{OL4}	1.0	10.0		mA	$P0A_2$ $P0A_3$ V_{OL} 1 V
High level output current	I_{IH1}	0.1	0.8		mA	VCOH pull-down V_{IH} = V_{DD}
High level input current	I_{IH2}	0.1	0.8		mA	VCOL pull-down V_{IH} = V_{DD}
High level input current	I_{IH3}	0.1	1.3		mA	P↘ pull-down V_{IH} = V_{DD}

CHARACTERISTICS	SYMBOL	STANDARD VALUE				CONDITION
		MIN.	TYP.	MAX.	UNIT	
High Level input current	I_{IH4}	0.05	0.13	0.30	mA	$P0D_0$ to $P0D_3$ pull-down $V_{IH}=V_{DD}$
Output off leak current	I_{L1}			500	nA	$P0A_2$, $P0A_3$ $V_{OH}=V_{DD}$
Output off leak current	I_{L2}			500	nA	$P1B_1$ to $P1B_3$, LPF_{OUT} $V_{OH}=16$ V
Output off leak current	I_{L3}			±100	nA	EO_0, EO_1 $V_{OH}=V_{DD1}$ $V_{OL}=0$V

AC CHARACTERISTICS (Unless otherwise specified, T_a = −40 to +85 °C, V_{DD} = 4.5 to 5.5 V)

CHARACTERISTICS	SYMBOL	STANDARD VALUE				CONDITION
		MIN.	TYP.	MAX.	UNIT	
Operating frequency	f_{in1}	0.5		30	MHz	VCOL MF mode, sine wave input $V_{in}=0.3\ V_{P-P}$
Operating frequency	f_{in2}	5		40	MHz	VCOL MF mode, sine wave input $V_{in}=0.3\ V_{P-P}$
Operating frequency	f_{in3}	9		150	MHz	VCOL, sine wave input $V_{in}=0.3\ V_{P-P}$
Operating frequency	f_{in4}	9		250	MHz	VCOL, sine wave input $V_{in}=0.3\ V_{P-P}$
Operating frequency	f_{in5}	0.1		1	MHz	AMIFC, sine wave input $V_{in}=0.3\ V_{P-P}$
Operating frequency	f_{in6}	5		15	MHz	FMIFC, sine wave input $V_{in}=0.3\ V_{P-P}$
AD converting resolution				6	bit	
Absolute accuracy of AD conversion			±1	±1.5	LSB	T_a= + 10 to + 50°C

REFERENCE CHARACTERISTICS

CHARACTERISTICS	SYMBOL	STANDARD VALUE				CONDITION
		MIN.	TYP.	MAX.	UNIT	
Source current	I_{DD3}		15		mA	CPU and PLL are operating VCOL sine wave Input f_{in}=150 MHz V_{in}=0.5 VP-P V_{DD}=5 V T_a=25°C
High level output current	I_{OH4}		−0.2		mA	COM_0, COM_1 $V_{OH}=V_{DD}-1$ V
Intermediate level output current	I_{OM1}		−20		μA	COM_0, COM_1 $V_{OM}=V_{DD}+1$ V
Intermediate level output current	I_{OM2}		20		μA	COM_0, COM_1 $V_{OM}=1$ V
Low level output current	I_{OL5}		0.2		mA	COM_0, COM_1 $V_{OL}=1$ V

RECOMMENDED SOLDERING CONDITIONS

The following conditions (see table below) must be met when soldering this product.

Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

TYPES OF SURFACE MOUNT DEVICE

For more details, refer to our document "SMT MANUAL" (IEI-1207).

μPD17003AGF

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak package's surface temperature: 230 °C or below, Reflow time: 30 seconds or below (210 °C or higher), Number of reflow process: 1, Exposure limit*: None	IR30-00
VPS	Peak package's surface temperature: 215 °C or below, Reflow time: 40 seconds or below (200 °C or higher), Number of reflow process: 1, Exposure limit*: None	VP15-00
Wave soldering	Solder temperature: 260 °C or below, Flow time: 10 seconds or below, Number of flow process: 1, Exposure limit*: None	WS60-00
Partial heating method	Terminal temperature: 300 °C or below, Flow time: 10 seconds or below, Exposure limit*: None	

*: Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65% or less.

Note: Do not apply more than a single process at once, except for "Partial heating method".

SINGLE CHIP MICROCONTROLLER FOR DIGITAL TUNING SYSTEM

The μPD17005 is a 4 bit single chip CMOS microcontroller equipped with the hardware exclusively for digital tuning systems.

Adoption of the μPD17000 architecture enables its CPU to directly operate the data memory, perform various calculations, or control the peripheral hardware with just one instruction. All instructions are single 16-bit words.

The μPD17005 integrates input/output ports, LCD drivers, A/D converters, D/A converters (PWM output), clock generator ports, digital tuning 150 MHz prescalars, PLL frequency synthesizers, low pass filter (LPF) amplifiers, and frequency counters into one chip.

With all these in one chip, the μPD17005 provides a high performance and multi-functional digital tuning system.

The one-time PROM (OTP) μPD17P005 is available for evaluating the μPD17005 program and low quantity production.

The μPD17003, which contains the compressed program memory (ROM), is compatible with this microcontroller.

FEATURES

- Employment of the μPD17000 architecture
- 16K byte (16 bits x 7932 steps) program memory (ROM)
- 432 nibble (4 bits x 432 nibbles) general purpose data memory (RAM)
- 4.44 μs (4.5 MHz crystal oscillator) instruction execution time
- Decimal calculation available
- Table referencing available
- Equipped with the PLL frequency synthesizer hardware
  Dual modular prescalars (up to 150 MHz), programmable dividers, phase comparators, charge pumps, and LPF amplifiers
- Abundant peripheral hardware
  General purpose input/output ports, LCD drivers, serial interfaces, A/D converters, D/A converters (PWM output), clock generator ports, frequency counters
- Enriched interrupt function
  External interrupt 2 channels
  Internal interrupt 3 channels
- Equipped with power on reset/CE pin reset/electrical blackout detection circuit
- CMOS low energy requirement
- Voltage: 5 V ±10 %

ORDERING INFORMATION

Order Code	Package
μPD17005GF-xxx-3B9	80-pin plastic QFP (bent lead)

Notes on Serial interface:

The 2-wire mode corresponds to the I2C-Bus specification from Philips.

In case of using this interface mode note the following:

Duties when using I2C bus system

Purchase of NEC's I2C bus system hardware components conveys a license under the Philips I2C patents rights to use this components in an I2C system, provided that the system conforms the I2C standard specifications as defined by Philips.

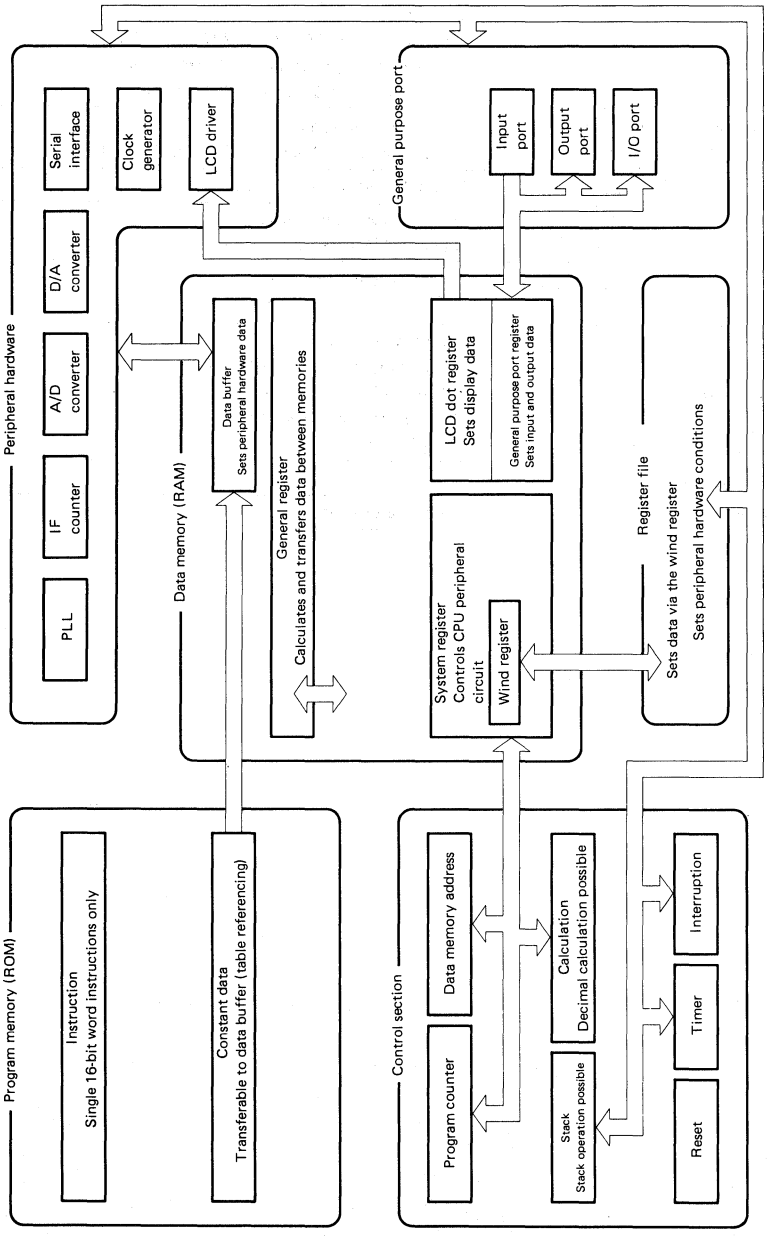
Consequently for all ROM based components with I2C hardware circuits the user is kindly requested to notify the use of the I2C bus interface at the ROM code verification stage.

TABLE OF μPD17005 FUNCTIONS

NAME	FUNCTION
Program memory (ROM)	16K bytes (16 bits x 7932 steps) Table reference area: up to 16 bits x 7932 steps
General purpose data memory (RAM)	432 nibbles (4 bits x 432 nibbles) Data buffer : 4 nibbles General register: 16 nibbles
System register	12 nibbles
Register file	33 nibbles
Port register (including LCD register)	24 nibbles
Instruction execution time	4.44 μs (with 4.5 MHz crystal oscillator)
Stack level	7 levels (stack operation possible)
General purpose port	16 input/output ports 8 input ports 9 output ports (+30: LCD segment pins)
Clock generator port (CGP)	One port Variable duty pulse (VDP) and signal generator (SG) functions
LCD driver	30 segment pins, 2 common pins, 1/2 duty, 1/2 bias, 250 Hz frame frequency, driving voltage V_{DD}, 16 segment pins shared with key source All 30 segments can be used as an output port. (separatable into 4, 4, 6, and 16 segment settings)
Serial interface	2 systems (3 channels) 8 bit 3 lines: 2 channels 8 bit 2 lines: 1 channel
D/A converter	8 bits x 3 lines (PWM output, up to 12 V)
A/D converter	6 bits x 6 lines (consecutive comparison by the software)
Interrupt	5 channels (maskable interrupt) External interrupt: 2 channels (INT_0 pin, INT_1 pin) Internal interrupt: 3 channels (timer, serial interface 1, frequency counter)
Timer	2 systems Timer carry F/F (1, 5, 100, 250 ms) Timer interrupt (1, 5, 100, 250 ms)
Reset	Power on reset (by turning on the power) CE pin reset (CE pin low → high) Electrical blackout detection

NAME		FUNCTION
PLL frequency synthesizer	Division	Two types Direct division (VCOL pin 20 MHz MAX.) Pulse swallow (VCOL pin 40 MHz MAX.) (VCOH pin 250 MHz MAX.)
	Reference frequency	12 choices by program 1, 1.25, 2.5, 3, 5, 6.25, 9, 10, 12.5, 25, 50, 100 kHz
	Charge pump	Two independent error outputs
	Phase comparator	Unlock detection by program Unlock F/F delay time selection
	LPF amplifier	CMOS operation amplifier Output voltage up to 12 V
Frequency counter		Frequency measuring $P1D_3$/FMIFC pin 0.1 to 1 MHz $P1D_2$/AMIFC pin 5 to 15 MHz External gate width measuring POA_1/FCG pin
Power voltage		5 V ±10 %
Package		80-pin plastic QFP

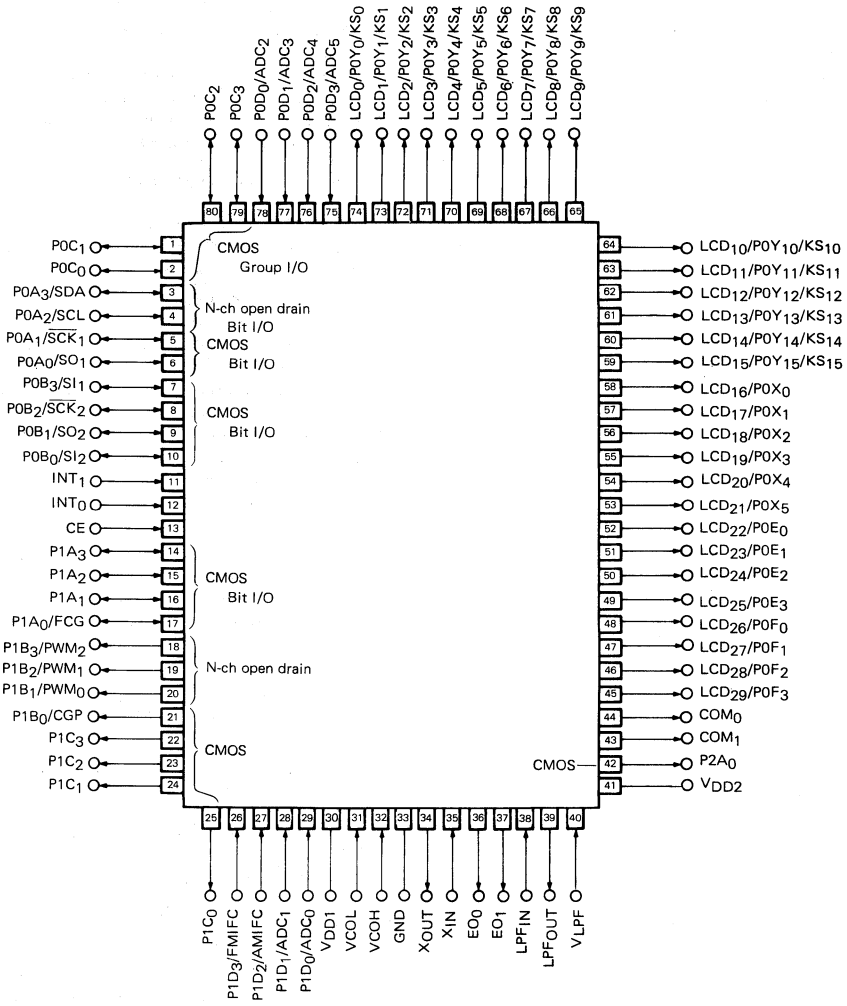
μPD17005 CONCEPT DIAGRAM



2

1. PINS

1.1 PIN CONFIGURATION (Top View)



1.2 PIN DESCRIPTION

<table>
<tr><th>PIN No.</th><th>SYMBOL</th><th>INPUT/ OUTPUT</th><th>OUTPUT FORMAT</th><th>PIN NAME</th><th>DESCRIPTION</th></tr>
<tr><td>79
80
1
2</td><td>P0C3
P0C2
P0C1
P0C0</td><td>Input/ output</td><td>CMOS push/pull</td><td>Port 0C</td><td>4 bit general purpose input/output port pins.
Specify input or output in 4-bit units. (Group I/O)
Specify input/output by the register file's P0CGPIO register (address 27H).
To read the input data or to set the output data, use the port register's P0C register (BANK0 address 27H).
These pins are set as an input port during power resetting, clock stop instruction execution, and CE resetting.</td></tr>
<tr><td>3
4

5
6</td><td>P0A3/SDA
P0A2/SCL

P0A1/$\overline{SCK_1}$
P0A0/SO1</td><td>Input/ output</td><td>N-ch open drain

CMOS push/pull</td><td>Port 0A</td><td>Pins function both as a 4-bit general purpose input/output port and serial interface.
To switch from an input/output port to serial interface, use the register file's SIO1MODE register (address 08H) and the SIO2MODE register (address 02H).
(1) When used as an 4-bit input/output port:
Specify input or output in 1-bit units (bit I/O).
To specify input/output, use the register file's P0ABIO register (address 35H).
To read the input data or set the output data, use the port register's P0A register (BANK0 address 70H). The P0A3/SDA and P0A2/SCL pins require external pull up resistance because they are N-ch open drain. These pins are set to an input port during power resetting, clock stop instruction execution, and CE resetting.
(2) When used as a serial interface:
There are two serial interface lines: serial interface 1 and serial interface 2 including the Port 0B (7 to 10 pins).
The serial interfaces 1 and 2 can be used together at the same time. The serial interface 1 has 2 channels of 2 line and 3 line, and the serial interface 2 has 1 channel of 3 line.
To specify the serial interface 1, use the register file SIO1 MODE register; to specify the serial interface 2, use the register file SIO2MODE register. The following are the pin functions.
<table>
<tr><th>PIN NAME</th><th>FUNCTION</th><th colspan="2">OPERATING MODE</th></tr>
<tr><td>P0A3/SDA</td><td>Data input/output</td><td rowspan="2">2 lines</td><td rowspan="5">Serial inter-face 1</td></tr>
<tr><td>P0A2/SCL</td><td>Clock input/output</td></tr>
<tr><td>P0A1/$\overline{SCK_1}$</td><td>Clock input/output</td><td rowspan="3">3 lines</td></tr>
<tr><td>P0A0/SO1</td><td>Data output</td></tr>
<tr><td>P0B3/SI1</td><td>Data input</td></tr>
<tr><td>P0B2/$\overline{SCK_2}$</td><td>Clock input/output</td><td rowspan="3">3 lines</td><td rowspan="3">Serial inter-face 2</td></tr>
<tr><td>P0B1/SO2</td><td>Data output</td></tr>
<tr><td>P0B0/SI2</td><td>Data input</td></tr>
</table>
</td></tr>
</table>

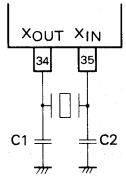
PIN. No.	SYMBOL	INPUT/ OUTPUT	OUTPUT FORMAT	PIN NAME	DESCRIPTION
3 4 5 6	$P0A_3$/SDA $P0A_2$/SCL $P0A_1/\overline{SCK_1}$ $P0A_0/SO_1$				The $P0A_3$/SDA and $P0A_2$/SLC pins require external pull up resistance because they are N-ch open drain. These pins are set as an input port of the general purpose input/output port during power on resetting, clock stop instruction execution, and CE resetting.
7 8 9 10	$P0B_3/SI_1$ $P0B_2/\overline{SCK_2}$ $P0B_1/SO_2$ $P0B_0/SI_2$	Input/ output	CMOS push-pull	Port 0B	Pins function both as a 4 bit general purpose input/output port and serial interface. To switch from input/output port to serial interface, use the register file's SIO1MODE register (address 08H) and the SIO2MODE register (address 02H). (1) When used as an 4-bit input/output port: Specify input or output in 1-bit units (bit I/O). To specify input/output, use the register file's P0BBIO register (address 35H). To read the input data or set the output data, use the port register's P0A register (BANK0 address 71H). These pins are set as an input port during power resetting, clock stop instruction execution, and CE resetting. (2) When used as an serial interface: There are two serial interface lines: serial interface 1 and serial interface 2 including the Port 0A (3 to 6 pins). These pins are set as an input port of the general purpose input/output port during power resetting, clock stop instruction execution, and CE resetting.
11 12	INT_1 INT_0	Input	–	Interrupt	Input pins for external interrupt request signal Interrupt requests are issued at the rising or falling edge of the signal input through these pins. To specify the rising or falling edge, use the register file's INTEDGE register (address 1FH), INT_0 pin, or INT_1 pin. Interrupt requests are not accepted unless permitted (maskable interrupt). The EI instruction permits all interrupts, and the INT_0 pin or INT_1 pin separately also gives permission. To give interrupt permissions, use the register file's INTPM2 register (address 2FH). Interrupt requests are accepted if permitted. Interrupts accepted by the INT_0 pin shift the flow of the program to address 05H, and interrupts accepted by the INT_1 pin shift the flow of the program to address 04H. Interrupts accepted by the INT_0 pin are executed before interrupts accepted by the INT_1 pin, if issued simultaneously. The issuer of the interrupt request can be checked by the register file's INTREQ2 register (address 3) even when the interrupt is not accepted. The register file's INTJDG register (address 0FH) checks the status of these pins and assigns them as a general purpose input port while the interrupt function is not being used. These pins are set as an input port during power resetting, clock stop instruction execution, and CE resetting.

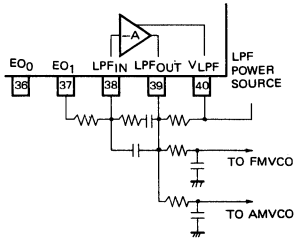
PIN No.	SYMBOL	INPUT/ OUTPUT	OUTPUT FORMAT	PIN NAME	DESCRIPTION
13	CE	Input	–	Chip enables	Input pin for device selection signal or reset signal Device selection is selecting PLL actions or standby status as described below. The PPL frequency synthesizer is enabled when the CE pin is set to high. The PPL frequency synthesizer is disabled when the CE pin is set to low. When the CE pin is set to low, the CPU and the internal crystal oscillation circuit are disabled by the clock stop instruction execution and the data memory is retained by the low energy requirement current (up to 15 μA). (when the CE pin is set to high, the clock stop instruction is executed as the NOP instruction.) During the clock stop instruction execution, the LCD driver display mode is turned off (LCD_0 to LCD_{27}, COM_0, COM_1 pins set to low) and the input/output ports (Port 0A, Port 0B, Port 0C, Port 1A) are set as input ports. The CE pin functioning as a reset signal input pin is described below. When the CE pin is reset to high from low, the internal timer carrier F/F synchronizes and resets the device. When the device is reset, the flow of the program shifts to address 0 and the input/output ports become input ports. The time required from pin resetting to device resetting can be selected from 1, 5, 100, 250 ms, which are offered by the carrier F/F. However, when the clock stop instruction is executed, the device will be reset 100 ms after the CE is reset to high. This pin does not accept anything lower than 110 μs or anything higher than 165 μs in order to prevent mis-operation caused by noise. For this reason, the content of the register is not updated. Also, to detect the pin status, use the register file's CEJDG register (address 07). This pin features Schmidt trigger input with the hysteresis characteristics. Do not apply voltage higher than the V_{DD} pin when turning on the power.
14 15 16 17	$P1A_3$ $P1A_2$ $P1A_1$ $P1A_0$/FCG	Input/ output	CMOS push-pull	Port 1A	Pins functioning both as a 4-bit general purpose input/output port or external gate counter ($P1A_0$/FCG pin). To switch from an input/output port to external gate counter, use the register file's IFCMODE register (address 12H) and the SIO2MODE register (address 02H). (1) When used as a 4-bit input/output port: Specify input or output in 1-bit units (bit I/O). To specify input/output, use the register file's P1A register (address 35H). To read the input data or set the output data, use the port register's P1ABIO register (BANK1 address 70H). These pins are set as input ports during power resetting, clock stop instruction execution, and CE resetting.

PIN No.	SYMBOL	INPUT/ OUTPUT	OUTPUT FORMAT	PIN NAME	DESCRIPTION
14 15 16 17	$P1A_3$ $P1A_2$ $P1A_1$ $P1A_0$/FCG	Input/ output	CMOS push-pull	Port 1A	(2) When using as an external gate counter (FCG) ($P1A_0$/FCG pin): These pins measure the time interval between two rising edges of the $P1A_0$/FCG pin. To measure the internal reference frequencies (1 kHz, 100 kHz, 900 kHz), use the 16-bit counter. To specify the external gate counter, use the register file's IFCMODE register (address 12H) and IFCCONT register (address 23H). To set the $P1A_0$/FCG pin as an input port, use the P1ABIO register (BANK0 address 35H). Use the external gate counter, frequency counter and clock generator port separately, because the IFCMODE register and IFCCONT register also control the frequency counter ($P1D_3$/FMIFC and $P1D_2$/AMIFC pins) and the clock generator port ($P1B_0$/CGP pin). These pins are set as input ports during power on resetting, clock stop instruction execution, and CE resetting.
18 19 20 21	$P1B_3/PWM_2$ $P1B_2/PWM_1$ $P1B_1/PWM_0$ $P1B_0$/CGP	Output	N-ch open drain CMOS push-pull	Port 1B	Pins functioning as a 4-bit general purpose input/output port, D/A converter ($P1B_2/PWM_2$, $P1B_2/PWM_1$, and $P1B_1/PWM_0$ pins), and clock generator port ($P1B_0$/CGP pin). To switch from an input/output port to D/A converter or to clock generator port, use the register file's PWMMODE register (address 13H). (1) When used as a 4-bit input/output port: To set the output data, use the port register's P1B register (BANK1 address 71H). The $P1B_3/PWM_2$, $P1B_2/PWM_1$, and $P1B_1/PWM_0$ pins require pull up resistance because they are for open drain output (up to 16 V). The data output during power resetting is unstable. The previous values are retained during clock stop instruction execution or CE resetting. (2) When used as a D/A converter (PWM output) ($P1B_3/PWM_2$, $P1B_2/PWM_1$, and $P1B_1/PWM_0$ pins): The $P1B_3/PWM_2$, $P1B_2/PWM_1$, and $P1B_1/PWM_0$ pins separately output signals. The output format has a pulse width modulation (PWM) to 878.9 Hz (225/256 kHz) frequency and 0.25/0.26 to 255.25/256 duty (256 gradations). To set the duty, use the PWMR0 to PWMR2 register (address 05 to 07) via the data buffer. $(\text{Duty} = \frac{0.25 + X}{256} \quad X = 0 \text{ to } 255)$ These three pins are for N-ch open drain output and withstands up to 16 volts. These pins are set as a general purpose output port during clock stop instruction execution. The status of these pins functioning as a D/A converter output is retained during CE resetting.

PIN No.	SYMBOL	INPUT/ OUTPUT	OUTPUT FORMAT	PIN NAME	DESCRIPTION
18 19 20 21	$P1B_3/PWM_2$ $P1B_2/PWM_1$ $P1B_1/PWM_0$ $P1B_0/CGP$	Output	N-ch open drain CMOS push-pull	Port 1B	(3) When used as a clock generator port (CGP) ($P1B_0$/CGP pin): To set the $P1B_0$/CGP pin to CGP mode, use the register file's PWMMODE register (address 13H) and IFGMODE register (address 12H). The CGP mode has VDP (variable duty pulse) and SG (signal generator) functions. The VDP function outputs 269 Hz frequency duties at 64 gradations from 2/67 to 65/67. The SG function divides and outputs the standard 18 kHz frequency by 4 to 130 (64 gradations). To set the data for VDP and SG functions, use the CGPR register (address 20H) via the data buffer. VDP duty = $\frac{2+X}{67}$ X = 0 to 63 SG divider = $\frac{18\text{ kHz}}{2(2+X)}$ The $P1B_0$/CGP pin is set as a general purpose output port during clock stop instruction execution and power resetting. The status of these pins functioning as a clock generator port output is retained during CE resetting.
22 23 24 25	$P1C_3$ $P1C_2$ $P1C_1$ $P1C_0$	Output	CMOS push-pull	Port 1C	4-bit general purpose output ports. To set the output data, use the port register's P1C register (BANK1 address 72). The data output during power resetting is unstable. The previous values are retained during clock stop instruction execution or CE resetting.
26 27 28 29	$P1D_3$/FMIFC $P1D_2$/AMIFC $P1D_1/ADC_1$ $P1D_0/ADC_0$	Input	—	Port 1D	Pins functioning as a 4-bit general purpose input port, frequency counter ($P1D_3$/FMIFC, $P1D_2$/AMIFC pins) and A/D converter ($P1D_1/ADC_1$, PAD_0/ADC_0 pins). To switch from input port to frequency counter, use the register file's IFCMODE register (address 12H). To switch from input port to A/D converter, use the register file's ADCCH register (address 14H). (1) When used as a 4 bit input/output port: To read the input data, use the port register's P1D register (BANK1 address 73H). (2) When used as a frequency counter: To use the $P1D_3$/FMIFC and $P1D_2$/AMIFC pins as a frequency measuring pin, use the register file IFCMODE register. The measurable frequency bands for the $P1D_3$/FMIFC pins are 5 to 15 MHz (0.3 Vp-p input) and 0.1 to 1 MHz (0.3 Vp-p input) for the $P1D_2$/AMIFC pin. To measure, count the frequencies input in the gate time (1 ms, 4 ms, 8 ms, open) by the 16 bit counter. The $P1D_3$/FMIFC pin counts the values divided by 1/2. Interrupt requests can be issued after the measuring is completed (when the gate closes). These functions can be utilized for detecting broadcasting stations by counting the intermediate frequencies. When used as a frequency counter, cut DC input signals by the condenser because the AC amplifier accepts inputs only.

PIN No.	SYMBOL	INPUT/ OUTPUT	OUTPUT FORMAT	PIN NAME	DESCRIPTION
26 27 28 29	$P1D_3$/FMIFC $P1D_2$/AMIFC $P1D_1/ADC_1$ $P1D_0/ADC_0$	Input	–	Port 1D	The intermediate voltage of the selected pins are set to approx. 1/2 V_{DD}. Non-selected pins are used as a general purpose input port. Initialize the AC amplifier by programming as necessary, because it is not disabled by resetting the CE pin (No. 13) to low. (Noise from the active amplifier may increase the current consumption.) Use the frequency counter, external gate counter, and clock generator port separately because the IFCMODE register specifies the external gate counter ($P1A_0$/FCG pin) as well as the clock generator port ($P1B_0$/CGP pin). These pins are set as a general purpose input port during power resetting and clock stop instruction execution. These pins continue acting as a frequency counter during CE resetting. (3) Used as an A/D converter ($P1D_1/ADC_1$, $P1D_0/ADC_0$ pin): To use these pins as a 6-bit A/D converter, use the register file's ADCCH register (address 14H). Up to six channels can be switched for the $P1D_1/ADC_1$, $P1D_0/ADC_0$ pins as well as the $P0D_3/ADC_5$ to $P0D_0/ADC_2$ pins (75 to 78 pins). Use the consecutive comparison by programming to convert from A to D and reference voltage is created by R string method, in which the power voltage is divided up. These pins are set as a general purpose input port during power resetting and clock stop instruction execution. These pins continue acting as an A/D converter during CE resetting.
30 41	V_{DD1} V_{DD2}	–	–	Power	Device power pin. These pins supply 5 V ±10 % voltage to the CPU and peripheral functions under operation. These pins lower the voltage to 3.5 V if the CPU alone is being operated. When the CE pin (No. 13) executes the clock stop instruction at low, the crystal oscillator stops oscillation and enters the data memory backup state. During this time, the power voltage is lowered to 2.2 V. When the power voltage rises from 0 to 4.5 V or when the power voltage falls below 3.5 V (2.2 V for clock stop instruction) and rises to 4.5 V, the device enters the power resetting state. After power resetting, the peripheral circuit, system register, and register files are initialized, and the program starts from address 0. The power voltage rising time from 0 to 4.5 V should be up to 500 ms. In addition to power on resetting, just explained, the CE pin also resets the device (CE pin low → high). Electric blackouts can be detected by detecting the timer carrier F/F values of the register file, which are different during power resetting and CE resetting.

<table>
<tr><th>PIN No.</th><th>SYMBOL</th><th>INPUT/ OUTPUT</th><th>OUTPUT FORMAT</th><th>PIN NAME</th><th>DESCRIPTION</th></tr>
<tr><td>30
41</td><td>V_{DD1}
V_{DD2}</td><td>–</td><td>–</td><td>Power</td><td>Do not apply a voltage higher than the V_{DD} pin to the rest of the pins. Pay special attention to both V_{DD} pin and CE pin rising simultaneously, otherwise resulting in latch up. Always connect the V_{DD1} and V_{DD2} pins to the same potential. The V_{DD2} pin supplies power to the crystal oscillation circuit (X_{IN} and X_{OUT} pins), error out circuit (EO_0 and EO_1 pins), and low pass filter circuit (LPF_{IN} and LPF_{OUT} pins); the V_{DD1} pin supplies power to all other parts.</td></tr>
<tr><td>31
32</td><td>VCOL
VCOH</td><td>Input</td><td>–</td><td>Oscillation low input
Oscillation high input</td><td>Pin for entering PLL oscillation frequency (VCO).
To specify one of the two division methods, direct division (MF mode) and pulse swallow (HF mode and VHF mode), use the register file's PLLMODE register (address 21H).
The following shows the input pins, input frequencies, and division ratios for each division methods.
<table>
<tr><th>Division method</th><th>Input pin</th><th>Input frequency</th><th>Input voltage</th><th>Division ratio</th></tr>
<tr><td>Direct division MF mode</td><td>VCOL</td><td>0.5–30 MHz</td><td>0.3 Vp-p</td><td>16 to $2^{16}-1$</td></tr>
<tr><td>Pulse swallow HF mode</td><td>VCOL</td><td>5–40 MHz</td><td>0.3 Vp-p</td><td>256 to $2^{16}-1$</td></tr>
<tr><td rowspan="2">Pulse swallow VHF mode</td><td rowspan="2">VCOH</td><td>9–150 MHz</td><td>0.3 Vp-p</td><td rowspan="2">256 to $2^{16}-1$</td></tr>
<tr><td>9–250 MHz</td><td>0.5 Vp-p</td></tr>
</table>
Cut DC input signals by the condenser because these pins accept AC amplifier inputs only. The pin specified by the PLLMODE register is set to intermediate voltage (approx. 1/2 V_{DD}). The pins that are not specified are internally pulled down. These pins are internally pulled down during PLL disabled and low CE pin states.
These pins disable the PLL during power on resetting and clock stop instruction execution.
These pins enter the PLLMODE register specified state during CE resetting.</td></tr>
<tr><td>33</td><td>GND</td><td>–</td><td>–</td><td>Ground</td><td>Device ground pin</td></tr>
<tr><td>34
35</td><td>X_{OUT}
X_{IN}</td><td>Output
Input</td><td>CMOS</td><td>Crystal oscillator</td><td>Crystal oscillator
The following shows the method for connecting the 4.5 MHz crystal oscillator.
 
</td></tr>
</table>

PIN No.	SYMBOL	INPUT/ OUTPUT	OUTPUT FORMAT	PIN NAME	DESCRIPTION
34 35	X_{OUT} X_{IN}	Output Input	CMOS	Crystal oscillator	The crystal oscillator in use determines the values of C1 and C2. Large C1 and C2 values degrade the oscillation start characteristic and increase the consumption current. Although the trimmer condenser connected to the X_{IN} pin is generally considered to adjust wider range of oscillation frequencies, it is recommended that it be connected to the crystal oscillator in use for a better oscillation stability. If probes are connected to the X_{OUT} pin or X_{IN} pin, the oscillation frequencies cannot be adjusted correctly owing to probe capacitance. Thus, adjust while measuring the LCD driving waveform (125 MHz) of the number of VCO oscillation frequencies. When the oscillation frequency is off the 4.5 MHz setting the oscillation frequencies of the internal timer and LL reference frequency are also off in the same proportion because they employ a divided 4.5 MHz.
36 37	EO_1 EO_0	Output	CMOS 3 state	Error out	Output pin for PLL frequency synthesizer charge pump. These pins output high level when the divided VCO frequency input through the VCOL pin (No. 31) and VCOH pin (No. 32) is higher than the reference frequency; these pins output low level when the divided VCO frequency input through the VCOL pin (No. 31) and VCOH pin (No. 32) is lower than the reference frequency. These pins are set to floating when the divided VCO frequency matches the reference frequency. To construct the PLL frequency synthesizer, use the external low pass filter (LPF) and apply these pin outputs to the voltage control oscillator (VCO). The EO_1 pin and EO_2 pin output the same signals, so use either pin. These pins are set to floating during PLL disabled state, i.e., during low CE pin (No. 13) or power resetting. To detect the PLL unlock state, use the register file's PLLULJDG register (05H). To select one of the four delay times (0.5 μs, 1 μs, 2 μs, disable) for PLL unlock state detection, use the register file's PLULDLY register (address 15H).
38 39 40	LPF_{IN} LPF_{OUT} V_{LPF}	Input Output –	N-ch open drain	LPF amplifier	Low pass filter (LPF) CMOS operation amplifier built-in pin. The following is the example of a pin internal equivalent circuit and application circuit. μPD17005 

PIN No.	SYMBOL	INPUT/ OUTPUT	OUTPUT FORMAT	PIN NAME	DESCRIPTION
38 39 40	LPF_{IN} LPF_{OUT} V_{LPF}	Input Output –	N-ch open drain	LPF amplifier	The LPF_{OUT} pin requires pull up resistance because it is for N-ch open drain output. It withstands voltage up to 16 V. Apply a voltage, which is higher than that applied to the LPF_{OUT} pin, but not exceeding 16 V, to the V_{LPF} pin. The LPF_{OUT} pin is internally pulled up during PLL disabled state.
42	$P2A_0$	Output	CMOS push-pull	Port 2A	1 bit output port pin. To set the data, use the port register's P2A register (BANK2 address 70H). The data output during power on resetting is unstable. The previous output values are retained during clock stop instruction execution and CE resetting.
43 44	COM_1 COM_0	Output	CMOS	Common signal	Output pin for LCD driver common signal. The LCD driver has 1/2 duty, 1/2 bias, a 250 Hz frame frequency, and V_{DD} driving voltage. Up to 60-dot display can be done by matrix with the LCD_0/$P0Y_0$/KS_0 to LCD_{29}/$P0F_3$ pins. These pins output three voltages: ground, 1/2 V_{DD}, and V_{DD}. Dots light up when $\pm V_{DD}$ potential difference is generated between these pins and LCD_0/$P0Y_0$/KS_0 to LCD_{29}/$P0F_3$ pins. These pins output low during power resetting and clock stop instruction execution, provided that the display mode was turned off by the register file's LCDMODE register (address 10H). The output status of these pins is retained during CE resetting, provided that the display mode is turned on.
45 to 48 49 to 52 53 to 58 59 to 74	LCD_{29}/$P0F_3$ to LCD_{26}/$P0F_0$ LCD_{25}/$P0E_3$ to LCD_{22}/$P0E_0$ LCD_{21}/$P0X_5$ to LCD_{16}/$P0X_0$ LCD_{15}/ $P0Y_{15}$/KS_{15} to LCD_0/ $P0Y_0$/KS_0	Output	CMOS push-pull	LCD segment signal	Pins functioning as LCD driver segment signal output pins (LCD_{29}/$P0F_3$ to LCD_0/$P0Y_0$/KS_0 pins), key matrix source signal output pins (LCD_{15}/$P0Y_{15}$/KS_0 to LCD_0/$P0Y_0$/KS_0 pins), and general purpose output port (LCD_{29}/$P0F_3$ to LCD_0/$P0Y_0$/KS_0 pins). To switch from segment signal to key source signal or to general purpose output port, use the register file LCDMODE register (address 10H) or the LCDPORT register (address 11H). (1) When using as an LCD driver segment signal output pin (LCD_{29}/$P0F_3$ to LCD_0/$P0Y_0$/KS_0 pins): The LCD driver has a 1/2 duty, 1/2 bias, and 250 Hz frame frequency (125 Hz segment signal output). Up to 60 dot display can be done by matrix with these segment signal output pins and COM_0 pin and COM_1 pin (No. 44 and 43). Dots light up when $\pm V_{DD}$ potential difference is generated between these pins and LCD_0/$P0Y_0$/KS_0 to LCD_{29}/$P0F_3$ pins. To set the LCD driver display data, use the LCD dot register (BANK0 address 60H to 6EH), or the LCD group register (address 08H to 0FH) via the data buffer. To turn the LCD driver display on or off, use the register file's LCDMODE register. When the display mode is turned off, these segment signal output pins are set to low. But the pins, which are specified as a general purpose output port

PIN No.	SYMBOL	INPUT/ OUTPUT	OUTPUT FORMAT	PIN NAME	DESCRIPTION
45 to 48	$LCD_{29}/P0F_3$ to $LCD_{26}/P0F_0$	Output	CMOS push-pull	LCD segment signal	by the register file's LCDPORT register, output the output port data regardless of the display mode. These pins output low during power resetting and clock stop instruction execution. The output status of these pins are retained during CE resetting, provided that the display mode is turned on. The $LCD_{15}/P0Y_{15}/KS_{15}$ to $LCD_0/P0Y_0/KS_0$ pins can output both the segment signal and key source signal of the 16 key matrix at the same time. (2) When using as a key matrix source signal: To set these 16 $LCD_{15}/P0Y_{15}/KS_{15}$ to $LCD_0/P0Y_0/KS_0$ pins as a key source signal output pin, use the register file's LCDMODE register. The key source signals are output with the LCD segment signals by time division. (Key source signal output time: 220 μs). To use the key source signal, set the $P0D_3/ADC_5$ to $P0D_0/ADC_2$ pins as a key return signal input pin (No. 75 to 78). Therefore, the key matrix with 16 key sources and four input keys is configured. Key source signals are output every 4 ms. To set the output data of the key source signal, use the key source register (address 42H) via the data buffer. The key source signal is not output when the LCD driver display mode is turned off (the segment signal output is low) or when these pins are set as a general purpose output port. The key source signal is not output during power on resetting and clock stop instruction execution. The output status of these pins are retained during CE resetting. (3) When used as an output port: The following table shows how to set these pins as an output port using the register file's LCDPORT register (address 11H).
49 to 52	$LCD_{25}/P0E_3$ to $LCD_{22}/P0E_0$				
53 to 58	$LCD_{21}/P0X_5$ to $LCD_{16}/P0X_0$				
59 to 74	$LCD_{15}/P0Y_{15}/KS_{15}$ to $LCD_0/P0Y_0/KS_0$				

PIN No.	PIN Name	Port name	Number of bits
45 to 48	$LCD_{29}/P0F_3$ to $LCD_{26}/P0F_0$	Port 0F	4 bits
49 to 52	$LCD_{25}/P0E_3$ to $LCD_{22}/P0E_0$	Port 0E	4 bits
53 to 58	$LCD_{21}/P0X_5$ to $LCD_{16}/P0X_0$	Port 0X	6 bits
59 to 74	$LCD_{15}/P0Y_{15}/KS_{15}$ to $LCD_0/P0Y_0/KS_0$	Port 0Y	16 bits

<table>
<tr><th>PIN No.</th><th>SYMBOL</th><th>INPUT/ OUTPUT</th><th>OUTPUT FORMAT</th><th>PIN NAME</th><th>DESCRIPTION</th></tr>
<tr><td>45
to
48

49
to
52

53
to
58

59
to
74</td><td>$LCD_{29}/P0F_3$
to
$LCD_{26}/P0F_0$

$LCD_{25}/P0E_3$
to
$LCD_{22}/P0E_0$

$LCD_{21}/P0X_5$
to
$LCD_{16}/P0X_0$

$LCD_{15}/$
$P0Y_{15}/KS_{15}$
to
$LCD_0/$
$P0Y_0/KS_0$</td><td>Output</td><td>CMOS push-pull</td><td>LCD segment signal</td><td>The Port 0F, Port 0E, Port 0X, and Port 0Y can be specified separately as an output port, otherwise they function as an LCD segment signal output pin. The following table shows how to set output data in each port.

<table><tr><th>Port name</th><th>Output data setting</th></tr><tr><td>Port 0F</td><td>P0F register (BANK0 address 6DH) also functions as the LCD dot register's LCDD 13 register.</td></tr><tr><td>Port 0E</td><td>P0E register (BANK0 address 6BH) also functions as the LCD dot register's LCDD 11 register.</td></tr><tr><td>Port 0X</td><td>P0XH, and P0XL registers (BANK0 address 69H and 68H) also function as the LCD dot register's LCDD 9 register and LCDD 8 register, respectively. To set the output data, use the P0X group register (0CH) via the data buffer.</td></tr><tr><td>Port 0Y</td><td>To set the output data, use the P0Y group register (42CH) via the data buffer.</td></tr></table>
These pins are set as a segment signal output pin and thus output low level during power resetting and clock stop instruction execution.
The previous output status is retained during CE resetting.</td></tr>
<tr><td>75
76
77
78</td><td>$P0C_3/ADC_5$
$P0C_2/ADC_4$
$P0C_1/ADC_3$
$P0C_0/ADC_2$</td><td>Input</td><td>Input with pull down</td><td>Port 0C</td><td>Pins functioning as a 4-bit general purpose input port and A/D converter input pin.
To switch from the input port to A/D converter, use the register file's ADCCH register (address 14H).

(1) When used as an input port:
To read the input data, use the port register's POC register (BANK0 address 72H).
The $P0C_3/ADC_5$ to $P0C_0/ADC_2$ pins have a built-in pull-down resistance enabling them to be used as a key return signal input pin of the key matrix. To use the LCD segment pin as the key source, turn off the pull-down resistance during key source signal output (220 μs), and turn on the pull-down resistance during segment signal output (220 μs). Always keep the pull-down resistance on when the LCD segment pin is not used as the key source.
Turn off the pull-down resistance of the pin set as an A/D converter by the register file's ADCCH register.

(2) When used as an A/D converter:
To set these pins as a 6 bit A/D converter, use the register file's ADCCH register (address 14H).
Use the consecutive comparsion by programming to convert from A to D. The reference voltage is created by the R string method, in which the power voltage is divided up.
Up to six channels can be switched for the $P0C_3/ADC_5$ to $P0C_0/ADC_2$ pins as well as the $P1D_1/ADC_1$, $P1D_0/ADC_0$</td></tr>
</table>

PIN No.	SYMBOL	INPUT/ OUTPUT	OUTPUT FORMAT	PIN NAME	DESCRIPTION
75 76 77 78	$P0C_3/ADC_5$ $P0C_2/ADC_4$ $P0C_1/ADC_3$ $P0C_0/ADC_2$	Input	Input with pull down	Port 0C	pins (No. 28 and 29). To specify the desired channel, use the register file's ADCCH register. The other five channels function as general purpose input ports. The pull-down resistance built-in $P0C_3/ADC_5$ to $P0C_0/ADC_2$ pins are equipped with a pull-down resistance. When these pins are set as an A/D converter input pin by the ADCCH register, the pull-down resistance is turned off. The A/D converter pins are re-specified to the general purpose input port during power resetting and clock stop instruction execution. These pins function as an A/D converter during CE resetting.

1.3 NOTES ON USING GENERAL PURPOSE PORT

1.3.1 Port register data bit

To read the input data or set the output data in the Port 0A, Port 0B, Port 0C, Port 0D, Port 1A, Port 1B, Port 1C, Port 1D, and Port 2A, use port registers (P0A to P2A register) in the data memory.

The $P0A_3$ pin and the $P0A_0$ pin of the Port 0A correspond to the most significant bit and the least significant bit of the port register P0A, respectively.

The same rule applies to the Port 0B, Port 0C, Port 0D, Port 1A, Port 1B, Port 1C, Port 1D, and Port 2A.

To set the output data in the Port 0E, Port 0F, Port 0X, and Port 0Y, use the LCD group register via the LCD dot register or the data buffer in the data memory.

1.3.2 Input/output ports (Port 0A, Port 0B, Port 0C, Port 1A)

(1) When a port is specified as an input port:

Execute the instruction to read the contents of the port register in the data memory (provided that the port register address is defined as m of the SKT m, #i instruction or ADD r, m instruction). The port pin status is stored as the port register value. Execute the instruction to write in the port register (provided that the port register address is defined as m of the MOV m, #i instruction or r of the ADD r, m instruction), and the values are written in the output data latch circuit.

(2) When a port is specified as an output port:

Executes the instruction to write in the port register. The values are written in the output data latch circuit and output through each pin. Execute the instruction to read the contents of the port register. The output data latch content is stored as the port register value. However, when the read instruction is executed through the $P0A_3$/SDA and $P0A_2$/SCL pins, the pin status is read and different data may be output.

These pins are set as an input port during power resetting, CE resetting or clock stop instruction execution. Write the output latch content, which becomes unstable during power resetting, in the port register before setting it in the output port, otherwise the output data will be unstable. The output data latch content is not updated during clock stop instruction execution or CE resetting.

1.3.3 Output ports (Port 1B, Port 1C, Port 0F, Port 0E, Port 0X, and Port 0Y)

Output ports write port register values in the output latch and outputs them through the pins.

Execute the instruction to read the port register value. The latch status is stored as the port register value.

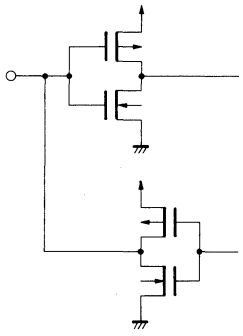
The data output during power on resetting is unstable.

The previous output data is retained during CE resetting or clock stop instruction execution.

The Port 0E, Port 0F, Port 0X, and Port 0Y automatically output low level during power on resetting or clock stop instruction execution.

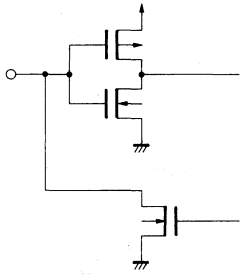
1.4 PIN EQUIVALENT CIRCUITS

1.4.1 P0A ($P0A_1/\overline{SCK}_1$, $P0A_0/SO_1$)
P0B ($P0B_3/SI_1$, $P0B_2/\overline{SCK}_2$, $P0B_1/SO_2$, $P0B_0/SI_1$)
P1A ($P1A_3$, $P1A_2$, $P1A_1$, $P1A_0$)



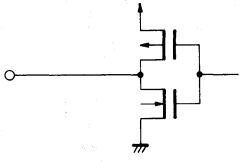
(Input/output)

1.4.2 P0A ($P0A_3$/SDA, $P0A_2$/SCL)



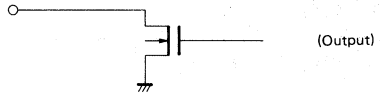
(Input/output)

1.4.3 P0C ($P0C_3/P0C_2$, $P0C_1$, $P0C_0$)
P1B ($P1B_0$/CGP)
P1C ($P1C_3$, $P1C_2$, $P1C_1$, $P1C_0$)
P2A ($P2A_0$)
$LCD_0/P0Y_0/KS_0$ to $LCD_{29}/P0F_3$

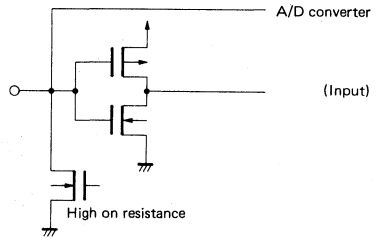


(Output)

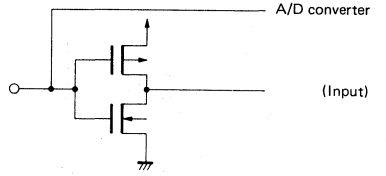
1.4.4 P1B ($P1B_3/PWM_2$, $P1B_2/PWM_1$, $P1B_0/PWM_0$)



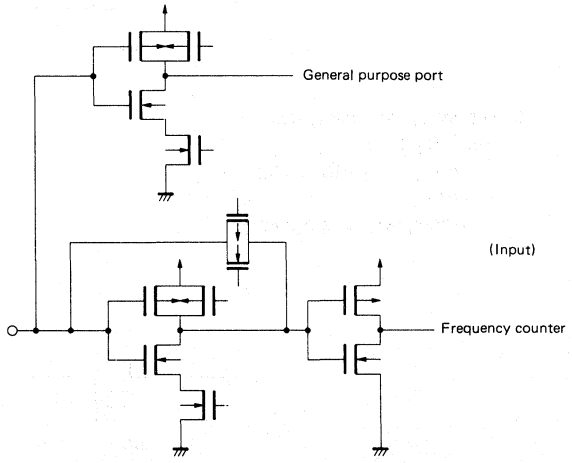
1.4.5 P0D ($P0D_3/ADC_5$, $P0D_2/ADC_4$, $P0D_1/ADC_3$, $P0D_0/ADC_2$)



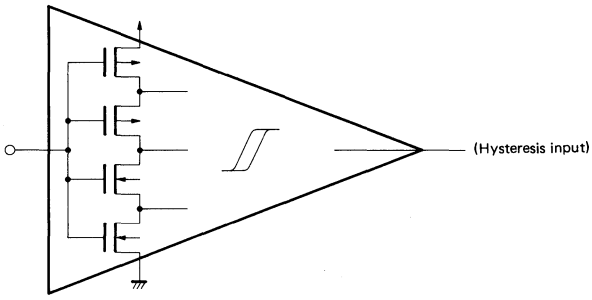
1.4.6 P1D ($P1D_1/ADC_1$, $P1D_0/ADC_0$)



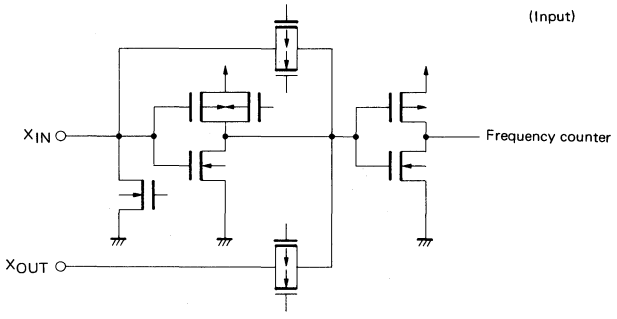
1.4.7 P1D ($P1D_3$/FMIFC, $P1D_2$/AMIFC)



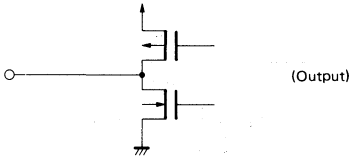
1.4.8 CE
INT_1
INT_0



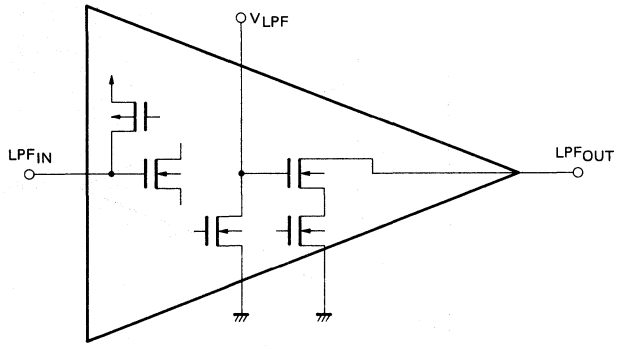
1.4.9 X_{OUT}, X_{IN}



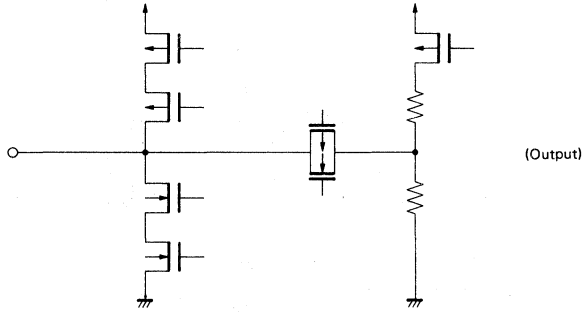
1.4.10 EO_1, EO_0



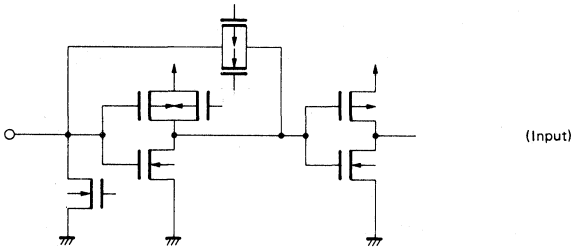
1.4.11 LPF_{IN}, LPF_{OUT}, V_{LPF}



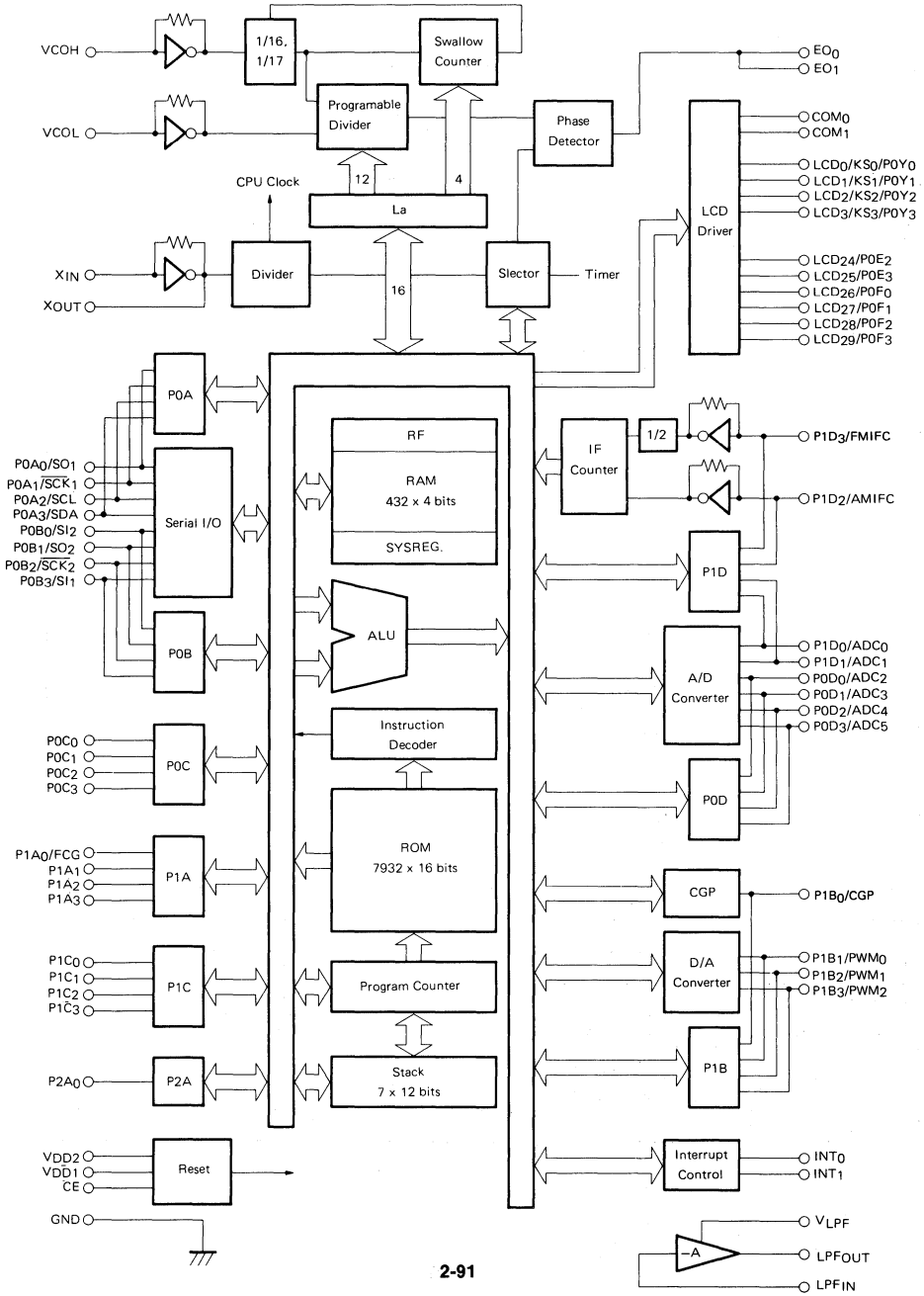
1.4.12 COM_1, COM_0



1.4.13 VCOH
VCOL



2. BLOCK DIAGRAM



3. μPD17005 INSTRUCTIONS

3.1 TABLE OF INSTRUCTION SETS

b_{14} b_{13} b_{12} b_{11} \ b_{16}		0		1	
0 0 0 0	0	ADD	r, m	ADD	m, #i
0 0 0 1	1	SUB	r, m	SUB	m, #i
0 0 1 0	2	ADDC	r, m	ADDC	m, #i
0 0 1 1	3	SUBC	r, m	SUBC	m, #i
0 1 0 0	4	AND	r, m	AND	m, #i
0 1 0 1	5	XOR	r, m	XOR	m, #i
0 1 1 0	6	OR	r, m	OR	m, #i
0 1 1 1	7	INC INC MOVT BR CALL RET RETSK EI DI RETI PUSH POP GET PUT PEEK POKE RORC STOP HALT NOP	AR IX DBF, @AR @AR @AR AR AR DBF, p p, DBF WR, rf rf, WR r 0 h		
1 0 0 0	8	LD	r, m	ST	m, r
1 0 0 1	9	SKE	m, #i	SKGE	m, #i
1 0 1 0	A	MOV	@r, m	MOV	m, @r
1 0 1 1	B	SKNE	m, #i	SKLT	m, #i
1 1 0 0	C	BR	addr (page0)	CALL	addr (page0)
1 1 0 1	D	BR	addr (page1)	MOV	m, #i
1 1 1 0	E	BR	addr (page2)	SKT	m, #n
1 1 1 1	F	BR	addr (page3)	SKF	m, #n

3.2 TABLE OF INSTRUCTIONS

NOTE

M : One of Data memory specified by [(BANK), m]
m : Data memory address specified by (m_H, m_L) of each bank
m_H : Data memory address high (Row address) ; 3bits
m_L : Data memory address Low (Column address) ; 4 bits
R : One of General register specified by [(RD), r]
r : General register address low ; 4bits
RP : General register pointer
RF : One of register file specified by rf
rf : Register file address specified by (rf_H, rf_L)
rf_H : Register file address high
rf_L : Register file address low
AR : Address register
IX : Index register
IXE : Index enable flag
DBF : Data buffer
WR : Window register
MP : Memory pointer
MPE : Memory pointer enable flag
PE : Peripheral
p : Peripheral address
p_H : Peripheral address high
p_L : Peripheral address low

PC : Program memory counter
SP : Stack pointer
STACK : Stack of (PC), (BANK), (IXE)
$STACK_{PC}$: Stack of (PC)
BANK : Bank register
$(ROM)_{PC}$: One of Program memory data specified by (PC)
INTEF : Interrupt enable flag
SGR : Program memory segment register
i : Immediate data ; 4bits
n : Bit position ; 4bits
addr : One of program memory address ; 11bits
CY : Carry flag
c : Carry
b : Borrow
h : Halt release conditions
[ ] : Address of M, R, RF
( ) : Contents of M, R, RF, AR, IX, DBF, WR, PE

	Mnemonic	Operand	Function	Operation	Machine code			
					Op. code			
Addition instruction	ADD	r, m	Add Data memory to General register	(R) ← (R) + (M)	00000	m_H	m_L	r
		m, ≠i	Add immediate data to Data memory	(M) ← (M) + i	10000	m_H	m_L	i
	ADDC	r, m	Add Data memory to General register with carry	(R) ← (R) + (M) + (CY)	00010	m_H	m_L	r
		m, ≠i	Add immediate data to Data memory with carry	(M) ← (M) + i + (CY)	10010	m_H	m_L	i
	INC	AR	Increment Address register	(AR) ← (AR) + 1	00111	000	1001	0000
		IX	Increment Index register	(IX) ← (IX) + 1	00111	000	1000	0000
Subtraction instruction	SUB	r, m	Subtract Data memory from General register	(R) ← (R) − (M)	00001	m_H	m_L	r
		m, ≠i	Subtract immediate data from Data memory	(M) ← (M) − i	10001	m_H	m_L	i
	SUBC	r, m	Subtract Data memory from General register with borrow	(R) ← (R) − (M) − (CY)	00011	m_H	m_L	r
		m, ≠i	Subtract immediate data from Data memory with borrow	(M) ← (M) − i − (CY)	10011	m_H	m_L	i
Logical operation instruction	SKE	m, ≠i	Skip if Data memory equals immediate data	(M) − i & skip if zero	01001	m_H	m_L	i
	SKGE	m, ≠i	Skip if Data memory is greater than or equal to immediate data	(M) − i & skip if not borrow	11001	m_H	m_L	i
	SKLT	m, ≠i	Skip if Data memory is less than immediate data	(M) − i & skip if borrow	11011	m_H	m_L	i
	SKNE	m, ≠i	Skip if Data memory not equal immediate data	(M) − i & skip if not zero	01011	m_H	m_L	i

	Mnemonic	Operand	Function	Operation	Machine code			
					Op. code			
Comparison instruction	AND	m, #i	Logic AND of Data memory and immediate data	(M) ← (M) AND i	10100	m_H	m_L	i
		r, m	Logic AND of General register and Data memory	(R) ← (R) AND (M)	00100	m_H	m_L	r
	OR	m, #i	Logic OR of Data memory and immediate data	(M) ← (M) OR i	10110	m_H	m_L	i
		r, m	Logic OR of General register and Data memory	(R) ← (R) OR (M)	00110	m_H	m_L	r
	XOR	m, #i	Exclusive Logic OR of Data memory and immediate data	(M) ←(M) XOR i	10101	m_H	m_L	i
		r, m	Exclusive Logic OR of General register and Data memory	(R) ←(R) XOR (M)	00101	m_H	m_L	r
Transfer instruction	LD	r, m	Load Data memory to General register	(R) ←(M)	01000	m_H	m_L	r
	ST	m, r	Store General register to Data memory	(M) ←(R)	11000	m_H	m_L	r
	MOU	@r, m	Move Data memory to Destination data memory referring to General register	if MPE = 1 : [(MP), (R)] ←(M) if MPE = 0 : [(m_H), (R)] ←(M)	01010	m_H	m_L	r
		m, @r	Move Source data memory referring to General register to Data memory	if MPE = 1 : (M) ←[(MP), (R)] if MPE = 0 : (M) ←[(m_H), (R)]	11010	m_H	m_L	r
		m, #i	Move immediate data to Data memory	(M) ←i	11101	m_H	m_L	i
	MOUT	DBF, @AR	Move Program memory data specified by Address register to Data buffer	($STACK_{pr}$) ←(PC) & (PC) ←(AR) & (DBF) ←$(ROM)_{pr}$ & (PC) ←($STACK_{pr}$)	00111	000	0001	0000
	PUSH	AR	Decrement Stack pointer, then move Address register to Stack	(SP) ← (SP) − 1 & ($STACK_{pc}$) ←(AR)	00111	000	1101	0000
	POP	AR	Move Stack to Address register, then increment Stack pointer	(AR) ←($STACK_{pc}$) & (SP) ←(SP) + 1	00111	000	1100	0000
	PEEK	WR, rf	Get data of Register file to Window register	(WR) ←(RF)	00111	rf_H	0011	rf_L
	POKE	rf, WR	Put data of Window register into Register file	(RF) ←(WR)	00111	rf_H	0010	rf_L
	GET	DBF, p	Get peripheral data to Data buffer	(DBF) ←(PE)	00111	p_H	1011	p_L
	PUT	p, DBF	Put data of Data buffer to peripheral	(PE) ←(DBF)	00111	p_H	1010	p_L
Judge instruction	SKT	m, #n	Test Data memory bits, then skip if all bits specified are true	if $(M)_n$ = all "1", then skip	11110	m_H	m_L	n
	SKF	m, #n	Test Data memory bits, then skip if all bits specified are false	if $(M)_n$ = all "0", then skip	11111	m_H	m_L	n
Branch instruction	BR	addr	Jump to the address in page 0	(PC) ←addr & $(PC)_{\neq 12, \neq 11}$ ←00	01100	addr (11bits)		
			Jump to the address in page 1	(PC) ←addr & $(PC)_{\neq 12, \neq 11}$ ←01	01101			
			Jump to the address in page 2	(PC) ←addr & $(PC)_{\neq 12, \neq 11}$ ←10	01110			
			Jump to the address in page 3	(PC) ←addr & $(PC)_{\neq 12, \neq 11}$ ←11	01111			
		@AR	Jump to the address specified by Address register	(PC) ←(AR)	00111	000	0100	0000
Shift	RORC	r	Rotate General register right with carry	(CY) ← $(R)_{b3}$ → $(R)_{b2}$ → $(R)_{b1}$ → $(R)_{b0}$ → (CY)	00111	000	0111	r

	Mnemonic	Operand	Function	Operation	Machine code			
					Op. code			
Subroutine instruction	CALL	addr	Call subroutine in page 0	(SP)←(SP) − 1 & ($STACK_{pc}$)←((PC) + 1) & (PC)$_{11}$←0 & (PC)←addr	11100	addr (11bits)		
		@AR	Call subroutine	(SP)←(SP) − 1 & ($STACK_{pc}$)←((PC) + 1) & (PC)←(AR)	00111	000	0101	0000
	RET		Return to main routine from subroutine	(PC)←($STACK_{pc}$) & (SP)←(SP) + 1	00111	000	1110	0000
	RETSK		Return to main routine from subroutine, then skip unconditionally	(PC)←($STACK_{pc}$) & (SP)←(SP) + 1 & and skip	00111	001	1110	0000
	RETI		Return to main routine from interrupt service routine	(PC), (BANK), (IXE)←(STACK) & (SP)←(SP) + 1	00111	100	1110	0000
Inter-rupt	EI		Enable interrupt	INTEF←1	00111	000	1111	0000
	DI		Disable interrupt	INTEF←0	00111	001	1111	0000
Other	STOP	0	Stop clock if CE=low	stop clock if CE=low	00111	010	1111	0000
	HALT	h	Halt the CPU, Restart by condition h	halt	00111	011	1111	h
	NOP		No operation		00111	100	1111	0000

3.3 ASSEMBLER (AS17K) INCORPORATED MACRO

NOTE

flag : One of flag1 to flagn

flag1 to flagn : Flag mane specified by RESERVED TABLE

n : Number

< > : Description can be omitted

Mnemonic	Operand	n	Function	Operation
SKTn	flag1, ···flagn	1 ≦n≦ 4	Test flag1 to flagn, then skip all flags specified are true	if (flag1) to (flagn) = all "1", then skip
SKFn	flag1, ···flagn	1 ≦n≦ 4	Test flag1 to flagn, then skip all flags specified are false	if (flag1) to (flagn) = all "0", then skip
SETn	flag1, ···flagn	1 ≦n≦ 4	Set all flags in flag1 to flagn,	(flag1) to (flagn) ← 1
CLRn	flag1, ···flagn	1 ≦n≦ 4	Clear all flags in flag1 to flagn	(flag1) to (flagn) ← 0
NOTn	flag1, ···flagn	1 ≦n≦ 4	Complement all flags in flag1 to flagn	if (flag) = "0", then (flag) ← 1 & if (flag) = "1", then (flag) ← 0
INITFLG	<NOT>flag1, ···<NOT>flagn	1 ≦n≦ 4	Initialize all flags in flag1 to flagn	if description = NOT flag, (flag) ← 0 if description = flag, (flag) ← 1
BANKn		0 ≦n≦ 3	Set n into Bank register	(BANK) ← n, 0 ≦n≦ 3

4. μPD17005 RESERVED WORDS (ASI7K)

4.1 TABLE OF RESERVED WORDS

4.1.1 System register (SYSREG)

Reserved word	Model	Address	Read/ Write	Function outline
AR3	MEM	0.74H	R	BIT b15-12 of Address Register
AR2	MEM	0.75H	R	BIT b11-8 of Address Register
AR1	MEM	0.76H	R/W	BIT b7-4 of Address Register
AR0	MEM	0.77H	R/W	BIT b3-0 of Address Register
WR	MEM	0.78H	R/W	Window Register
BANK	MEM	0.79H	R/W	Bank Register
IXH	MEM	0.7AH	R/W	Index register high
MPH	MEM	0.7AH	R/W	Memory pointer high
MPE	FLG	0.7AH.3	R/W	Memory pointer enable flag
IXM	MEM	0.7BH	R/W	Index register middle
MPL	MEM	0.7BH	R/W	Memory pointer low
IXL	MEM	0.7CH	R/W	Index register low
RPH	MEM	0.7DH	R/W	General Register pointer high
RPL	MEM	0.7EH	R/W	General Register pointer low
PSW	MEM	0.7FH	R/W	Program status word
BCD	FLG	0.7EH.0	R/W	Binary Coded Decimal flag
CMP	FLG	0.7FH.3	R/W	Compare flag
CY	FLG	0.7FH.2	R/W	Carry flag
Z	FLG	0.7FH.1	R/W	Zero flag
IXE	FLG	0.7FH.0	R/W	Index register enable flag

4.1.2 Data buffer (DBF)

Reserved word	Model	Address	Read/ Write	Function outline
DBF3	MEM	0.0CH	R/W	BIT b15-12 OF DBF
DBF2	MEM	0.0DH	R/W	BIT b11-8 OF DBF
DBF1	MEM	0.0EH	R/W	BIT b7-4 OF DBF
DBF0	MEM	0.0FH	R/W	BIT b3-0 OF DBF

4.1.3 LCD dot data register

Reserved word	Model	Address	Read/ Write	Function outline
LCDD0	MEM	0.60H	R/W	LCD data register
LCDD1	MEM	0.61H	R/W	LCD data register
LCDD2	MEM	0.62H	R/W	LCD data register
LCDD3	MEM	0.63H	R/W	LCD data register
LCDD4	MEM	0.64H	R/W	LCD data register
LCDD5	MEM	0.65H	R/W	LCD data register
LCDD6	MEM	0.66H	R/W	LCD data register
LCDD7	MEM	0.67H	R/W	LCD data register
LCDD8	MEM	0.68H	R/W	LCD data register
LCDD9	MEM	0.69H	R/W	LCD data register
LCDD10	MEM	0.6AH	R/W	LCD data register
LCDD11	MEM	0.6BH	R/W	LCD data register
LCDD12	MEM	0.6CH	R/W	LCD data register
LCDD13	MEM	0.6DH	R/W	LCD data register
LCDD14	MEM	0.6EH	R/W	LCD data register

4.1.4 General Purpose Port Register

Reserved word	Model	Address	Read/ Write	Function outline
P0A3	FLG	0.70H.3	R/W	Port 0A bit b3
P0A2	FLG	0.70H.2	R/W	Port 0A bit b2
P0A1	FLG	0.70H.1	R/W	Port 0A bit b1
P0A0	FLG	0.70H.0	R/W	Port 0A bit b0
P0B3	FLG	0.71H.3	R/W	Port 0B bit b3
P0B2	FLG	0.71H.2	R/W	Port 0B bit b2
P0B1	FLG	0.71H.1	R/W	Port 0B bit b1
P0B0	FLG	0.71H.0	R/W	Port 0B bit b0
P0C3	FLG	0.72H.3	R/W	Port 0C bit b3
P0C2	FLG	0.72H.2	R/W	Port 0C bit b2
P0C1	FLG	0.72H.1	R/W	Port 0C bit b1
P0C0	FLG	0.72H.0	R/W	Port 0C bit b0
P0D3	FLG	0.73H.3	R	Port 0D bit b3
P0D2	FLG	0.73H.2	R	Port 0D bit b2
P0D1	FLG	0.73H.1	R	Port 0D bit b1
P0D0	FLG	0.73H.0	R	Port 0D bit b0

Reserved word	Model	Address	Read/ Write	Function outline
P0XL3	FLG	0.68H.3	R/W	Port 0X bit b1
P0XL2	FLG	0.68H.2	R/W	Port 0X bit b0
P0XL1	FLG	0.68H.1	R/W	DUMMY
P0XL0	FLG	0.68H.0	R/W	DUMMY
P0XH3	FLG	0.69H.3	R/W	Port 0X bit b5
P0XH2	FLG	0.69H.2	R/W	Port 0X bit b4
P0XH1	FLG	0.69H.1	R/W	Port 0X bit b3
P0XH0	FLG	0.69H.0	R/W	Port 0X bit b2
P0E3	FLG	0.6BH.3	R/W	Port 0E bit b3
P0E2	FLG	0.6BH.2	R/W	Port 0E bit b2
P0E1	FLG	0.6BH.1	R/W	Port 0E bit b1
P0E0	FLG	0.6BH.0	R/W	Port 0E bit b0
P0F3	FLG	0.6DH.3	R/W	Port 0F bit b3
P0F2	FLG	0.6DH.2	R/W	Port 0F bit b2
P0F1	FLG	0.6DH.1	R/W	Port 0F bit b1
P0F0	FLG	0.6DH.0	R/W	Port 0F bit b0
P1A3	FLG	1.70H.3	R/W	Port 1A bit b3
P1A2	FLG	1.70H.2	R/W	Port 1A bit b2
P1A1	FLG	1.70H.1	R/W	Port 1A bit b1
P1A0	FLG	1.70H.0	R/W	Port 1A bit b0
P1B3	FLG	1.71H.3	R/W	Port 1B bit b3
P1B2	FLG	1.71H.2	R/W	Port 1B bit b2
P1B1	FLG	1.71H.1	R/W	Port 1B bit b1
P1B0	FLG	1.71H.0	R/W	Port 1B bit b0
P1C3	FLG	1.72H.3	R/W	Port 1C bit b3
P1C2	FLG	1.72H.2	R/W	Port 1C bit b2
P1C1	FLG	1.72H.1	R/W	Port 1C bit b1
P1C0	FLG	1.72H.0	R/W	Port 1C bit b0
P1D3	FLG	1.73H.3	R/W	Port 1D bit b3
P1D2	FLG	1.73H.2	R/W	Port 1D bit b2
P1D1	FLG	1.73H.1	R/W	Port 1D bit b1
P1D0	FLG	1.73H.0	R/W	Port 1D bit b0
P2A3	FLG	2.70H.3	R/W	Port 2A bit b3
P2A2	FLG	2.70H.2	R/W	Port 2A bit b2
P2A1	FLG	2.70H.1	R/W	Port 2A bit b1
P2A0	FLG	2.70H.0	R/W	Port 2A bit b0

4.1.5 Register File (Control Register)

Reserved word	Model	Address	Read/ Write	Function outline
SP	MEM	0.81H	R/W	Stack pointer
SIO2TS	FLG	0.82H.3	R/W	SIO2 start flag
SIO2HIZ	FLG	0.82H.2	R/W	SO2/P0B1 select flag
SIO2CK1	FLG	0.82H.1	R/W	SIO2 clock select bit b1
SIO2CK0	FLG	0.82H.0	R/W	SIO2 clock select bit b0
IFCG	FLG	0.84H.0	R	IF counter gate status flag
PLLUL	FLG	0.85H.0	R	PLL unlock F/F flag
ADCCMP	FLG	0.86H.0	R	ADC judge flag
CE	FLG	0.87H.0	R	CE terminal status flag
SIO1CH	FLG	0.88H.3	R/W	SIO1 mode select flag
SB	FLG	0.88H.2	R/W	SB/SBI select flag
SIO1MS	FLG	0.88H.1	R/W	SIO1 clock mode select flag
SIO1TX	FLG	0.88H.0	R/W	SIO1 TX/RX select flag
TMMD3	FLG	0.89H.3	R/W	Timer interrupt mode select flag
TMMD2	FLG	0.89H.2	R/W	Timer interrupt mode select flag
TMMD1	FLG	0.89H.1	R/W	Timer carry F/F mode select flag
TMMD0	FLG	0.89H.0	R/W	Timer carry F/F mode select flag
INT1	FLG	0.8FH.1	R	INT1 terminal status flag
INT0	FLG	0.8FH.0	R	INT0 terminal status flag
KSEN	FLG	0.90H.1	R/W	Key souce decorder enable flag
LCDEN	FLG	0.90H.0	R/W	LCD driver enable flag
P0YON	FLG	0.91H.3	R/W	Port 0Y enable flag
P0XON	FLG	0.91H.2	R/W	Port 0X enable flag
P0EON	FLG	0.91H.1	R/W	Port 0E enable flag
P0FON	FLG	0.91H.0	R/W	Port 0F enable flag
IFCMD1	FLG	0.92H.3	R/W	IF counter mode select flag
IFCMD0	FLG	0.92H.2	R/W	IF counter mode select flag
IFCCK1	FLG	0.92H.1	R/W	IF counter clock select flag
IFCCK0	FLG	0.92H.0	R/W	IF counter clock select flag
PWM2ON	FLG	0.93H.3	R/W	PWM2 enable flag
PWM1ON	FLG	0.93H.2	R/W	PWM1 enable flag
PWM0ON	FLG	0.93H.1	R/W	PWM0 enable flag
CGPON	FLG	0.93H.0	R/W	CGP enable flag
ADCCH3	FLG	0.94H.3	R	AD mode select flag (DUMMY : 0)
ADCCH2	FLG	0.94H.2	R/W	AD mode select flag
ADCCH1	FLG	0.94H.1	R/W	AD mode select flag
ADCCH0	FLG	0.94H.0	R/W	AD mode select flag

Reserved word	Model	Address	Read/ Write	Function outline
PLULDLY3	FLG	0.95H.3	R	PLL unlock time select flag (DUMMY : 0)
PLULDLY2	FLG	0.95H.2	R	PLL unlock time select flag (DUMMY : 0)
PLULDLY1	FLG	0.95H.1	R/W	PLL unlock time select flag (DUMMY : 0)
PLULDLY0	FLG	0.95H.0	R/W	PLL unlock time select flag
KEYJ	FLG	0.96H.0	R	KEY imput judge flag
TMCY	FLG	0.97H.0	R	Timer carry F/F status flag
SBACK	FLG	0.98H.3	R/W	SB acknowledge flag
SIO1NWT	FLG	0.98H.2	R/W	SIO1 Not wait flag
SIO1WRQ1	FLG	0.98H.1	R/W	SIO1 wait mode flag
SIO1WRQ0	FLG	0.98H.0	R/W	SIO1 wait mode flag
IEG1	FLG	0.9FH.1	R/W	INT1 interrupt edge select flag
IEG0	FLG	0.9FH.0	R/W	INT0 interrupt edge select flag
PLLMD3	FLG	0.0A1H.3	R	PLL mode select flag (DUMMY : 0)
PLLMD2	FLG	0.0A1H.2	R	PLL mode select flag (DUMMY : 0)
PLLMD1	FLG	0.0A1H.1	R/W	PLL mode select flag
PLLMD0	FLG	0.0A1H.0	R/W	PLL mode select flag
IFCSTRT	FLG	0.0A3H.1	W	IF counter start flag
IFCRES	FLG	0.0A3H.0	W	IF counter reset flag
P0CGIO	FLG	0.0A7H.0	R/W	Port 0C I/O select flag
SIO1SF8	FLG	0.0A8H.3	R/W	SIO1 clock counter status flag
SIO1SF9	FLG	0.0A8H.2	R/W	SIO1 clock counter status flag
SBSTT	FLG	0.0A8H.1	R/W	SB start condition status flag
SBBSY	FLG	0.0A8H.0	R/W	SB start & stop condition status flag
IP1FC	FLG	0.0AEH.0	R/W	IF counter interrupt permission flag
IPSIO1	FLG	0.0AFH.3	R/W	SIO1 interrupt permission flag
IPTM	FLG	0.0AFH.2	R/W	Timer interrupt permission flag
IP1	FLG	0.0AFH.1	R/W	INT1 interrupt permission flag
IP0	FLG	0.0AFH.0	R/W	INT0 interrupt permission flag
PLLRFMD3	FLG	0.0B1H.3	R/W	PLL reference clock select flag
PLLRFMD2	FLG	0.0B1H.2	R/W	PLL reference clock select flag
PLLRFMD1	FLG	0.0B1H.1	R/W	PLL reference clock select flag
PLLRFMD0	FLG	0.0B1H.0	R/W	PLL reference clock select flag
P1ABIO3	FLG	0.0B5H.3	R/W	P1A3 I/O select flag
P1ABIO2	FLG	0.0B5H.2	R/W	P1A2 I/O select flag
P1ABIO1	FLG	0.0B5H.1	R/W	P1A1 I/O select flag
P1ABIO0	FLG	0.0B5H.0	R/W	P1A0 I/O select flag
P0BBIO3	FLG	0.0B6H.3	R/W	P0B3 I/O select flag
P0BBIO2	FLG	0.0B6H.2	R/W	P0B2 I/O select flag
P0BBIO1	FLG	0.0B6H.1	R/W	P0B1 I/O select flag
P0BBIO0	FLG	0.0B6H.0	R/W	P0B0 I/O select flag

Reserved word	Model	Address	Read/ Write	Function outline
P0ABIO3	FLG	0.0B7H.3	R/W	P0A3 I/O select flag
P0ABIO2	FLG	0.0B7H.2	R/W	P0A2 I/O select flag
P0ABIO1	FLG	0.0B7H.1	R/W	P0A1 I/O select flag
P0ABIO0	FLG	0.0B7H.0	R/W	P0A0 I/O select flag
SIO1IMD3	FLG	0.0B8H.3	R	SIO1 interrupt mode select flag (DUMMY : 0)
SIO1IMD2	FLG	0.0B8H.2	R	SIO1 interrupt mode select flag (DUMMY : 0)
SIO1IMD1	FLG	0.0B8H.1	R/W	SIO1 interrupt mode select flag
SIO1IMD0	FLG	0.0B8H.0	R/W	SIO1 interrupt mode select flag
SIO1CK3	FLG	0.0B9H.3	R	SIO1 Shift clock select flag (DUMMY : 0)
SIO1CK2	FLG	0.0B9H.2	R	SIO1 Shift clock select flag (DUMMY : 0)
SIO1CK1	FLG	0.0B9H.1	R/W	SIO1 Shift clock select flag
SIO1CK0	FLG	0.0B9H.0	R/W	SIO1 Shift clock select flag
IRQIFC	FLG	0.0BEH.0	R/W	IF counter Interrupt request flag
IRQSIO1	FLG	0.0BFH.3	R/W	SIO1 Interrupt request flag
IRQTM	FLG	0.0BFH.2	R/W	Timer Interrupt request flag
IRQ1	FLG	0.0BFH.1	R/W	INT1 Interrupt request flag
IRQ0	FLG	0.0BFH.0	R/W	INT0 Interrupt request flag

4.1.6 Peripheral hardware address

Reserved word	Model	Address	Read/ Write	Function outline
DBF	DAT	0FH	R/W	Data Buffer address for GET/PUT instructions
IX	DAT	01H	R/W	Index register address for INC instructions
ADCR	DAT	02H	R/W	A/D converter Vref data register
SIO2SFR	DAT	03H	R/W	SIO2 Presettable shift register
SIO1SFR	DAT	04H	R/W	SIO1 Presettable shift register
PWMR0	DAT	05H	R/W	PWM0 Data register
PWMR1	DAT	06H	R/W	PWM1 Data register
PWMR2	DAT	07H	R/W	PWM2 Data register
LCDR0	DAT	08H	W	LCD group data register 0
LCDR1	DAT	09H	W	LCD group data register 1
LCDR2	DAT	0AH	W	LCD group data register 2
LCDR3	DAT	0BH	W	LCD group data register 3
LCDR4	DAT	0CH	W	LCD group data register 4
P0X	DAT	0CH	W	Port 0X data register
LCDR5	DAT	0DH	W	LCD group data register 5
LCDR6	DAT	0EH	W	LCD group data register 6
LCDR7	DAT	0FH	W	LCD group data register 7
CGPR	DAT	20H	R/W	CGP data register
AR	DAT	40H	R/W	Address Register address for GET/PUT/PUSH/CALL/BR/MOUT/INC instructions
PLLR	DAT	41H	R/W	PLL data register
KSR	DAT	42H	R/W	Key souce data register
P0Y	DAT	42H	R/W	Port 0Y data register
IFC	DAT	43H	R	IF counter data register

5. ELECTRIC CHARACTERISTICS (TENTATIVE)

5.1 ABSOLUTE MAXIMUM RATINGS (T_a = 25 ±2 °C, unless otherwise)

Power Voltage	V_{DD}	−0.3 to +6.0	V
Input Voltage	V_I	−0.3 to V_{DD} + 0.3	V
Output Voltage	V_O	−0.3 to V_{DD} + 0.3 (excluding $P1B_1$ to $P1B_3$, $P0A_2$, $P0A_3$, LPF_{OUT})	V
Maximum Output Voltage	V_{BDS1}	18.0 ($P1B_1$ to $P1B_3$, LPF_{OUT})	V
Maximum Output Voltage	V_{BDS2}	V_{DD} + 0.3 ($P0A_2$, $P0A_3$)	V
Output Absorption Current	I_O	10.0	mA
Operating Temperature	T_a	−40 to +85	°C
Storage Temperature	T_{stg}	−55 to +125	°C

5.2 RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Power Voltage	V_{DD1}	4.5	5.0	5.5	V	With PLL and CPU active
Power Voltage	V_{DD2}	3.5	5.0	5.5	V	With CPU active and PLL not active
Data Retention Voltage	V_{DDR}	2.2		5.5	V	No crystal oscillation
Power Voltage Rising Time	T_{rise}			500	ms	V_{DD} = 0 → 4.5 V
Input Magnitude	Vin1	0.5		V_{DD}	V_{P-P}	VCOL, VCOH
Input Magnitude	Vin2	0.5		V_{DD}	V_{P-P}	AMIFC, FMIFC
Maximum Output Voltage	V_{BDS}	0.0		16.0	V	$P1B_1$ to $P1B_3$, LPF_{OUT}
Operating Temperature	T_a	−40		85	°C	

5.3 ELECTRIC CHARACTERISTICS

(T_a = −40 to +85 °C and V_{DD} = 4.5 to 5.5 V, RH ≦ 70 %, unless otherwise specified)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Power Voltage	V_{DD1}	4.5	5.0	5.5	V	With CPU and PLL active
Power Voltage	V_{DD2}	3.5	5.0	5.5	V	With CPU active and PLL not active
Power Current	I_{DD1}		1.2	2.4	mA	With CPU active and PLL not active Positive wave input (fin = 4.5 MHz, V_{IN} = V_{DD}), T_a = 25 °C X_{IN} pin
Power Current	I_{DD2}		0.45	0.90	mA	With CPU active and PLL not active HALT instruction in use (execute 20 instructions per 1 ms) Positive wave input (fin = 4.5 MHz, V_{IN} = V_{DD}), T_a = 25 °C X_{IN} pin
Data Retention Voltage	V_{DDR1}	3.5	5.0	5.5	V	Use electrical blackout detection by timer F/F Crystal oscillation
Data Retention Voltage	V_{DDR2}	2.2	5.0	5.5	V	Use electrical balckout detection by timer F/F No crystal oscillation
Data Retention Voltage	V_{DDR3}	2.0	5.0	5.5	V	Data memory (RAM) retention
Data Retention Current	I_{DDR1}		5	15	μA	No crystal oscillation T_a=25 °C
Data Retention Current	I_{DDR2}		5	10	μA	No crystal oscillation V_{DD}=5.0 V, T_a=25 °C
Intermediate Level Output Voltage	V_{CM1}	2.3	2.5	2.7	V	COM_0, COM_1 V_{DD}=5 V
High Level Output Voltage	V_{IH1}	0.8 V_{DD}	0.6 V_{DD}		V	$P0A_0$ to $P0A_3$, $P0B_0$ to $P0B_3$, $P0C_0$ to $P0C_3$, $P1A_0$ to $P1A_3$, $P1D_0$ to $P1D_3$, CE, INT_0, INT_1
High Level Output Voltage	V_{IH2}	0.6 V_{DD}	0.5 V_{DD}		V	$P0D_0$ to $P0D_3$
Low Level Output Voltage	V_{IL1}		0.4 V_{DD}	0.2 V_{DD}	V	$P0A_0$ to $P0A_3$, $P0B_0$ to $P0B_3$, $P0C_0$ to $P0C_3$, $P0D_0$ to $P0D_3$, $P1A_0$ to $P1A_3$, $P1D_0$ to $P1D_3$, CE, INT_0, INT_1
High Level Output Current	I_{OH1}	−1.0	−5.0		mA	$P0A_0$ to $P0A_1$, $P0B_0$ to $P0B_3$, $P0C_0$ to $P0C_3$, $P0D_0$ to $P0D_3$, $P1A_0$ to $P1A_3$, $P1C_0$ to $P1C_3$, $P1B_0$ V_{OH}=V_{DD}−1 V
High Level Output Current	I_{OH2}	−1.0	−4.0		mA	LCD_0 to LCD_{29}, EO_0, EO_1 V_{OH}=V_{DD}−1 V

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Low Level Output Current	I_{OL1}	1.0	7.0		mA	$P0A_0$, $P0A_1$, $P0B_0$ to $P0B_3$, $P0C_0$ to $P0C_3$, $P0D_0$ to $P0D_3$, $P1A_0$ to $P1A_3$, $P1C_0$ to $P1C_3$, $P1B_0$ $V_{OH}=V_{DD}-1$ V
Low Level Output Current	I_{OL2}	1.0	3.5		mA	LCD_0 to LCD_{29}, EO_0, EO_1 $V_{OH}=V_{DD}-1$ V
Low Level Output Current	I_{OL3}	1.0	2.0		mA	$P1B_1$ to $P1B_3$ $V_{OL}=1$ V
Low Level Output Current	I_{OL4}	1.0	10.0		mA	$P0A_2$, $P0A_3$ $V_{OL}=1$ V
High Level Input Current	I_{IH1}	0.1	0.8		mA	VCOH at pull-down $V_{IH}=V_{DD}$
High Level Input Current	I_{IH2}	0.1	0.8		mA	VCOL at pull-down $V_{IH}=V_{DD}$
High Level Input Current	I_{IH3}	0.1	1.3		mA	X_{IN} at pull-down $V_{IH}=V_{DD}$
High Level Input Current	I_{IH4}	0.05	0.13	0.30	mA	$P0D_0$ to $P0D_3$ at pull-down $V_{IH}=V_{DD}$
Maximum Output Voltage	V_{BDS}	0		16	V	$P1B_1$ to $P1B_3$, LPF_{OUT}
Output Off-Leak Current	I_{L1}			500	nA	$P0A_2$, $P0A_3$ $V_{OH}=V_{DD}$
Output Off-Leak Current	I_{L2}			500	nA	$P1B_1$ to $P1B_3$ $V_{OH}=16$ V
Output Off-Leak Current	I_{L3}			100	nA	EO_0, EO_1 $V_{OH}=V_{DD}$, $V_{OL}=0$ V
AD Conversion Resolution				6	bit	
AD Conversion Absolute Accuracy			1	1.5	LSB	$T_a=-10$ to 50 °C
Operating Frequency	f_{in1}	0.5		30	MHz	VCOL MF mode Positive wave input $V_{IN}=0.3$ V_{P-P}
Operating Frequency	f_{in2}	5		40	MHz	VCOL HF mode Positive wave input $V_{IN}=0.3$ V_{P-P}
Operating Frequency	f_{in3}	9		150	MHz	VCOH Positive wave input $V_{IN}=0.3$ V_{P-P}
Operating Frequency	f_{in4}	9		250	MHz	VCOH Positive wave input $V_{IN}=0.5$ V_{P-P}
Operating Frequency	f_{in5}	0.1		1	MHz	AMIFC Positive wave input $V_{IN}=0.3$ V_{P-P}
Operating Frequency	f_{in6}	5		15	MHz	FMIFC Positive wave input $V_{IN}=0.3$ V_{P-P}

(Reference characteristics)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Power Current	I_{DD3}		15		mA	With CPU and PLL active VCOH Positive wave input fin = 150 MHz, Vin = 0.5 V_{P-P}, V_{DD} = 5 V, T_a = 25 °C
High Level Output Current	I_{OH4}		−0.2		mA	COM_0, COM_1 $V_{OH}=V_{DD}-1$ V
Intermediate Level Output Current	I_{OM1}		20		μA	COM_0, COM_1 $V_{OM}=V_{DD}$
Intermediate Level Output Current	I_{OM2}		−20		μA	COM_0, COM_1 $V_{OM}=0$ V
Low Level Output Current	I_{OL6}		0.2		mA	COM_0, COM_1 $V_{OL}=1$ V

ONE-TIME PROM 4-BIT SINGLE-CHIP MICROCONTROLLER WITH BUILT-IN HARDWARE FOR DIGITAL TUNING SYSTEM

The μPD17P005 is a product with the built-in mask ROM of μPD17005 replaced with the one-time PROM.

μPD17P005 allows the user to write any program and is suitable for prototyping or small volume production in the system development of the μPD17005 or μPD17003A (ROM, RAM scale-down version of μPD17005).

The analog characteristics (PLL) of μPD17P005 are different from the μPD17005 or the μPD17003A cases. Using device really should be evaluated about time constance.

See also μPD17005 or μPD17003A data when reading this data sheet.

FEATURES

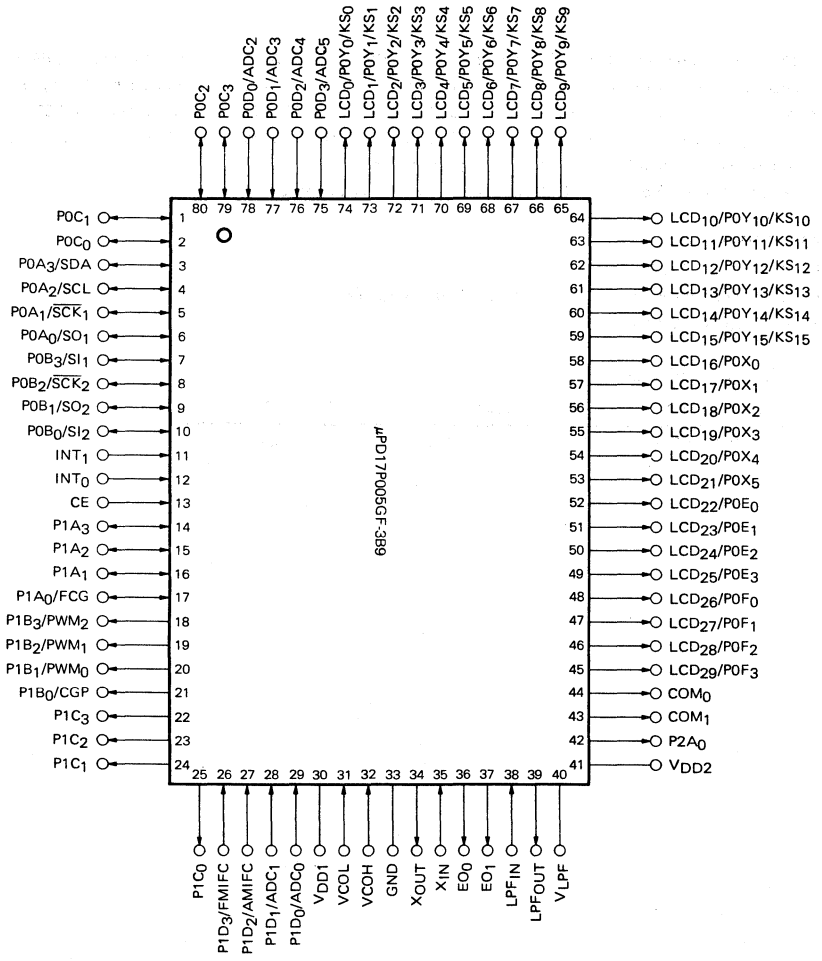
- μPD17005, μPD17003A compatible.
- Built-in one time PROM ROM: 16 KB (7932 steps x 16 bits)
- Single supply 5 V ±10 %

ORDERING INFORMATION

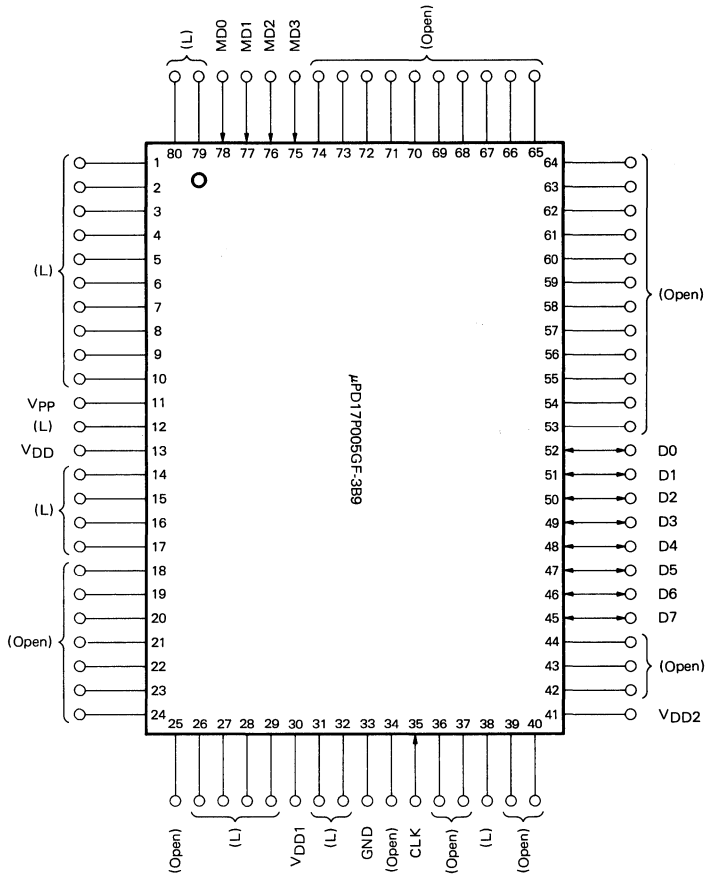
Order Code	Package	Quality Grade
μPD17P005GF-3B9	80-pin plastic QFP (14 x 20)	Standard

PIN CONFIGURATION (Top View)

(1) Normal operation mode



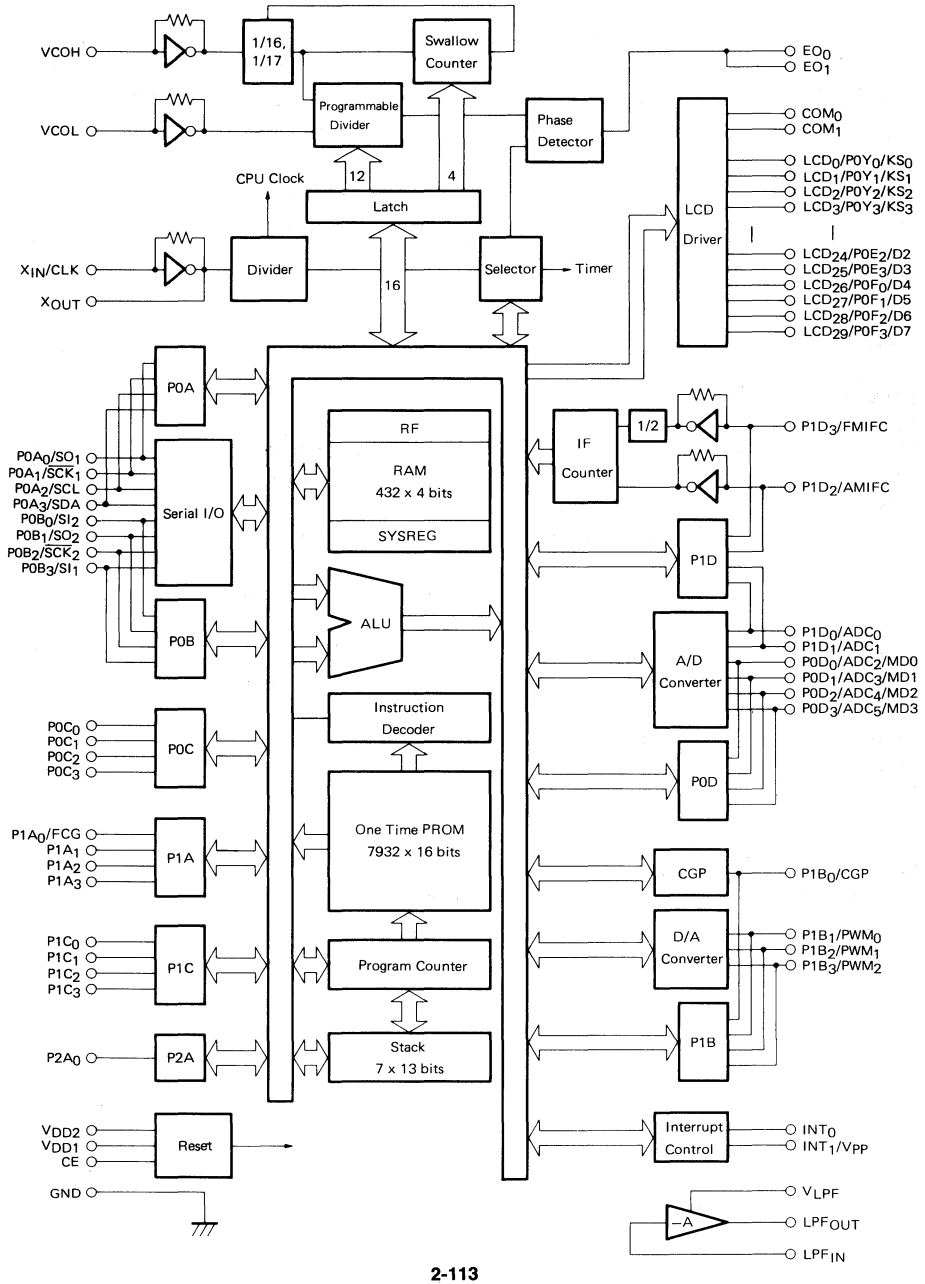
(2) PROM programming mode



Note: ( ): Treatment of pins that are not used in PROM programming mode.
L: Separately connect to respective ground via a resistor (470 Ω)
Open: Do not connect.

$P0A_0$-$P0A_3$	:	Port 0A
$P0B_0$-$P0B_3$	:	Port 0B
$P0C_0$-$P0C_3$	:	Port 0C
$P0D_0$-$P0D_3$	:	Port 0D
$P0E_0$-$P0E_3$	:	Port 0E
$P0F_0$-$P0F_3$	:	Port 0F
$P0X_0$-$P0X_5$	:	Port 0X
$P0Y_0$-$P0Y_{15}$	:	Port 0Y
$P1A_0$-$P1A_3$	:	Port 1A
$P1B_0$-$P1B_3$	:	Port 1B
$P1C_0$-$P1C_3$	:	Port 1C
$P1D_0$-$P1D_3$	:	Port 1D
$P2A_0$	:	Port 2A
SDA	:	Serial data input/output
SCL	:	Serial clock input/output
$\overline{SCK_1}$, $\overline{SCK_2}$	:	Serial clock input/output
SO_1, SO_2	:	Serial data output
SI_1, SI_2	:	Serial data input
INT_0, INT_1	:	External interrupt input
CE	:	Chip enable input
FCG	:	External gate counter input
PWM_0-PWM_2	:	D/A converter output
CGP	:	Clock generator port
FMIFC	:	Frequency counter input
AMIFC	:	Frequency counter input
ADC_0-ADC_5	:	A/D converter input
VCOL	:	Local oscillation low input
VCOH	:	Local oscillation high input
X_{IN}, X_{OUT}	:	Crystal resonator connecting pin
EO_0, EO_1	:	Error-out output
LPF_{IN}	:	LPF amplifier input
LPF_{OUT}	:	LPF amplifier output
COM_0, COM_1	:	LCD common signal output
LCD_0-LCD_{29}	:	LCD segment signal output
KS_0-KS_{15}	:	Key source signal output
CLK	:	Clock input for PROM
MD0-MD3	:	Mode selection for PROM
D0-D7	:	Data input/output for PROM
V_{PP}	:	Power Supply for PROM
V_{LPF}	:	LPF amplifier source
V_{DD1}, V_{DD2}	:	Power source
GND	:	Ground

BLOCK DIAGRAM



1. PIN FUNCTIONS

1.1 Port Pin

Pin Name	Input/ output	Dual function pin (*)	Function	Reset
$P0A_0$	Input/ output	SO_1	4-bit input/output port (Port 0A) Input/output settable in 1-bit.	Input
$P0A_1$		$\overline{SCK}_1$		
$P0A_2$		SCL	N-ch open-drain. 5 V withstand voltage	
$P0A_3$		SDA		
$P0B_0$	Input/ output	SI_2	4-bit input/output port (Port 0B) Input/output settable in 1-bit.	Input
$P0B_1$		SO_2		
$P0B_2$		$\overline{SCK}_2$		
$P0B_3$		SI_1		
$P0C_0$–$P0C_3$	Input/output	–	4-bit input/output port (Port 0C) Input/output settable in 1-bit.	Input
$P0D_0$–$P0D_3$	Input	ADC_2–ADC_5 (MD0–MD3)	4-bit input port (Port 0D) Pull-down resistor built-in.	–
$P0E_0$–$P0E_3$	Output	LCD_{22}–LCD_{25} (D0–D3)	4-bit output port (Port 0E)	–
$P0F_0$–$P0F_3$	Output	LCD_{26}–LCD_{29} (D4–D7)	4-bit output port (Port 0F)	–
$P0X_0$–$P0X_5$	Output	LCD_{16}–LCD_{21}	6-bit output port (Port 0X)	–
$P0Y_0$–$P0Y_{15}$	Output	LCD_0/KS_0–LCD_{15}/KS_{15}	16-bit output port (Port 0Y)	–
$P1A_0$	Input/output	FCG	4-bit input/output port (Port 0A) Input/output settable in 1-bit.	Input
$P1A_1$–$P1A_3$		–		
$P1B_0$	Output	CGP	4-bit output port (Port 1B)	–
$P1B_1$–$P1B_3$		PWM_0–PWM_2	N-ch open-drain. 16 V withstand voltage	
$P1C_0$–$P1C_3$	Output	–	4-bit output port (Port 1C)	–
$P1D_0$	Input	ADC_0	4-bit input port (Port 1D)	–
$P1D_1$		ADC_1		
$P1D_2$		AMIFC		
$P1D_3$		FMIFC		
$P2A_0$	Output	–	1-bit output port (Port 2A)	–

*: Pins in parentheses are dual function pins in PROM programming mode.

1.2 Pin for Other Than Port (In Normal Operation Mode)

Pin Name	Input/output	Dual function pin (*)	Function	Reset
SO_1	Output	$P0A_0$	Serial data output pin	Input
$\overline{SCK}_1$	Input/output	$P0A_1$	Serial clock input/output pin	
SCL	Input/output	$P0A_2$	Serial clock input/output pin	
SDA	Input/output	$P0A_3$	Serial data input/output pin	
SI_2	Input	$P0B_0$	Serial data input pin	Input
SO_2	Output	$P0B_1$	Serial data output pin	
$\overline{SCK}_2$	Input/output	$P0B_2$	Serial clock input/output pin	
SI_1	Input	$P0B_3$	Serial data input pin	
INT_0	Input	–	Edge-sensitive vector interrupt input pin (detection edge selectable)	–
INT_1		(V_{PP})		
CE	Input	–	Operation select pin and reset signal input pin	–
FCG	Input	$P1A_0$	External gate counter input pin	–
CGP	Output	$P1B_0$	Clock generator port output pin	–
PWM_0–PWM_2	Output	$P1B_1$–$P1B_3$	D/A converter output pin. N-ch open-drain. 16 V withstand voltage	–
ADC_0–ADC_1	Input	$P1D_0$–$P1D_1$	Analog input pin to D/A converter	–
ADC_2–ADC_5		$P0D_0$–$P0D_3$ (MD0–MD3)	Key source signal return output pin	
COM_0, COM_1	Output	–	Common signal output pin of LCD controller/ Driver	–
LCD_0–LCD_{15}	Output	$P0Y_0/KS_0$–$P0Y_{15}/KS_{15}$	Segment signal output pin of LCD controller/ Driver	–
LCD_{16}–LCD_{21}		$P0X_0$–$P0X_5$		
LCD_{22}–LCD_{25}		$P0E_0$–$P0E_3$ (D0–D3)		
LCD_{26}–LCD_{29}		$P0F_0$–$P0F_3$ (D4–D7)		
KS_0–KS_{15}	Output	$LCD_0/P0Y_0$–$LCD_{15}/P0Y_{15}$	Key source signal output pin of key matrix	–
AMIFC	Input	$P1D_2$	Frequency counter input pin	–
FMIFC		$P1D_3$		
VCOL	Input	–	Local oscillation frequency input pin	–
VCOH		–		
X_{IN}	Input	(CLK)	Crystal resonator	–
X_{OUT}	Output	–		
EO_0	Output	–	Charge pump output pin of PLL frequency synthesizer	–
EO_1				
LPF_{IN}	Input	–	Amplifier input pin for low-pass filter	–
LPF_{OUT}	Output	–	Amplifier output pin for low-pass filter N-ch open-drain. 16 V withstand voltage	–

Pin Name	Input/ output	Dual function pin (*)	Function	Reset
V_{LPF}	–	–	Amplifier supply pin for low-pass filter	–
V_{DD1}	–	–	Device supply pin. 6 V applied in program memory write/read/verify mode.	–
V_{DD2}				
GND	–	–	Ground pin	–

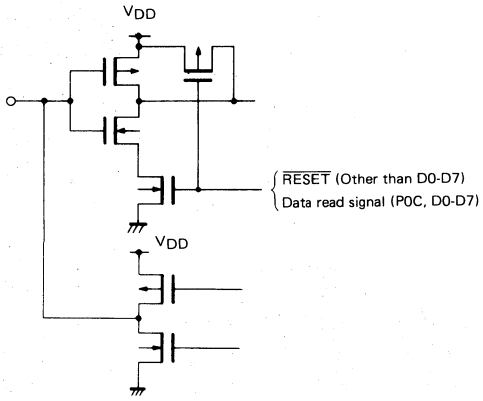
*: Pins in parentheses are dual function pins in PROM programming mode.

1.3 Pin for Other Than Port (In PROM Programming Mode)

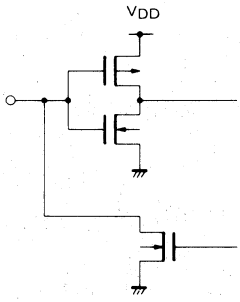
Pin Name	Input/output	Dual function pin	Function	Reset
CLK	Input	X_{IN}	Clock input pin at program memory write/ read/verify.	–
D_0–D_7	Input/output	$LCD_{22}/P0E_0$–$LCD_{29}/P0F_3$	Data input/output pin at program memory write/read/verify.	–
MD0–MD3	Input	$P0D_0/ADC_2$–$P0D_3/ADC_5$	Operation mode select pin at program memory write/read/verify.	–
V_{PP}	–	INT_1	Program voltage application pin at program memory write/read/verify. 12.5 V applied at program memory write/read/ verify. Used as INT_1 pin in normal operation mode.	–

1.4 Equivalent Circuit for Pin

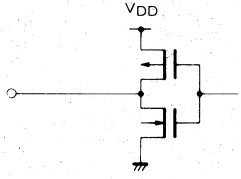
1.4.1 P0A (P0A$_1$ /$\overline{SCK}_1$, P0A$_0$/SO$_1$)
P0B (P0B$_3$/SI$_1$, P0B$_2$ /$\overline{SCK}_2$, P0B$_1$/SO$_2$, P0B$_0$/SI$_2$)
P0C (P0C$_3$, P0C$_2$, P0C$_1$, P0C$_0$) (Note)
P1A (P1A$_3$, P1A$_2$, P1A$_1$, P1A$_0$)
D0-D7
} (Input/Output)



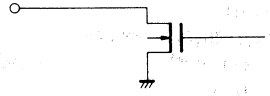
1.4.2 P0A (P0A$_3$/SDA, P0A$_2$/SCL) (Input/output)



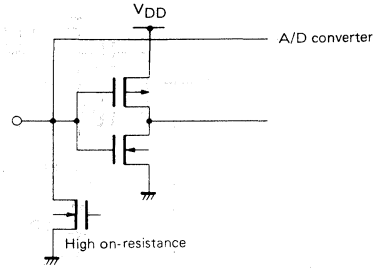
1.4.3 P1B (P1B$_0$/CGP)
P1C (P1C$_3$, P1C$_2$, P1C$_1$, P1C$_0$)
P2A (P2A$_0$)
LCD$_0$/P0Y$_0$/KS$_0$-LCD$_{29}$/P0F$_3$
} (Output)



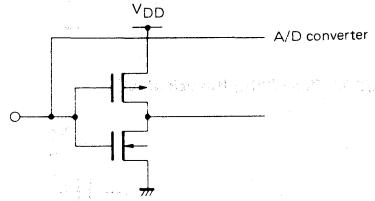
1.4.4 P1B (P1B$_3$/PWM$_2$, P1B$_2$/PWM$_1$, P1B$_1$/PWM$_0$) (Output)



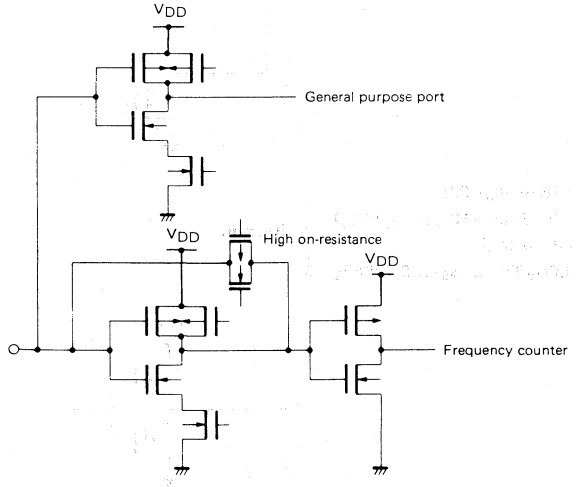
1.4.5 P0D (P0D$_3$/ADC$_5$/MD3, P0D$_2$/ADC$_4$/MD2, P0D$_1$/ADC$_3$/MD1, P0D$_0$/ADC$_2$/MD0) (Input)



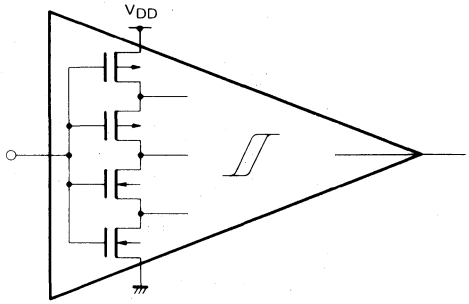
1.4.6 P1D (P1D$_1$/ADC$_1$, P1D$_0$/ADC$_0$) (Input)



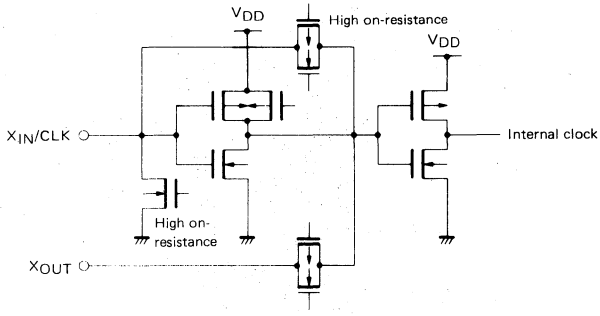
1.4.7 P1D (P1D$_3$/FMIFC, P1D$_2$/AMIFC) (Input)



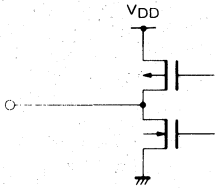
1.4.8 CE, INT_1/V_{PP}, INT_0 (Schmitt triggered input)



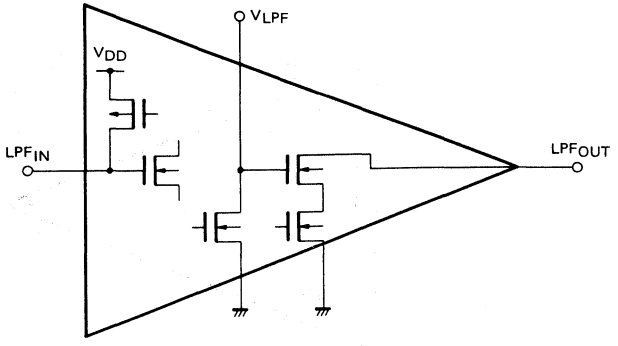
1.4.9 X_{OUT} (Output), X_{IN}/CLK (Input)



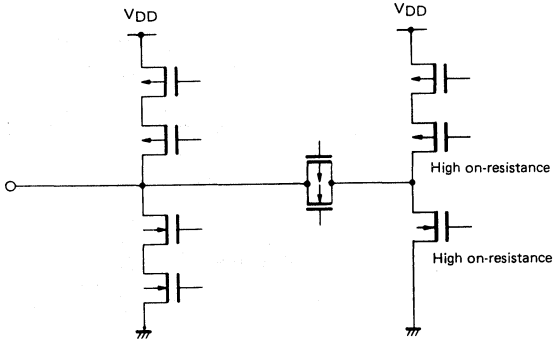
1.4.10 EO_1, EO_0 (Output)



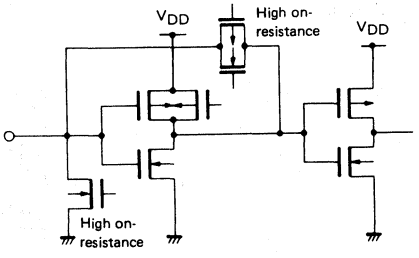
1.4.11 LPF_{IN} (Input), LPF_{OUT} (Output), V_{LPF}



1.4.12 COM_1, COM_0 (Output)



1.4.13 VCOH, VCOL (Input)



2. FUNCTION LIST

Item \ Model		μPD17003A	μPD17005	μPD17P005
ROM (x 16 bits)		3836	7932	7932 (PROM)
Table reference area		256	7932	
RAM (x 4 bits)		320	432	
Data buffer		4		
General register		16		
System register		12 nibbles		
Register file		33 nibbles (control register)		
General-purpose port register		24 nibbles		
Insturction execution time		4.44 μs (4.5 MHz crystal resonator used)		
Stack level		7-level (stack operation available)		
General-purpose port	Input/output port	16 units		
	Input port	8 units		
	Output port	9 units (+30: LCD segment pin)		
Clock generator port		1 unit		
LCD controller/driver		• 30 segments, 2 commons 1/2 duty, 1/2 bias, frame frequency 250 Hz, drive voltage V_{DD} 16 segment pins, also working as key source All of 30 segments can be used as output ports. (4, 4, 6, 16 segments: independently settable.)		
Serial interface		• 2 systems 8-bit 3-wire: 2-channel 8-bit 2-wire: 1-channel		
D/A converter		• 8-bits x 3 (PWM output, output withstand voltage 16 V max.)		
A/D converter		• 6 bits x 6 (successive approximation by software)		
Interrupt		• 5 channels (Maskable interrupt) External interrupt: 2 channels (INT_0 pin, INT_1 pin) Internal interrupt: 3 channels (timer, serial interface 1, frequency counter)		
Timer		• 2 systems Timer carry FF (1, 5, 100, 250 ms) Timer interrupt (1, 5, 100, 250 ms)		
Reset function		• Power-ON reset (at power on) • Reset by CE pin (CE pin goes from low to high.) • Power failure detection function		

Item \ Model		μPD17003A	μPD17005	μPD17P005
PLL frequency synthesizer	Dividing method	• 2 types: Direct dividing method: (VCOL pin 20 MHz max.) Pulse swallowing: (VCOL pin 40 MHz max.) (VCOH pin 250 MHz max.)		
	Reference frequency	• 12 types selectable by program. 1, 1.25, 2.5, 3, 5, 6.25, 9, 10, 12.5, 25, 50, 100 kHz		
	Charge pump	• Two independent error-out output		
	Phase comparator	• Unlock detection available by program. Unlock FF delay time selectable.		
	Amplifier for LPF	• CMOS operational amplifier, output withsatnd voltage 16 V max.		
Frequency counter		• Frequency measurement $P1D_3$/FMIFC pin: 5 to 15 MHz $P1D_2$/AMIFC pin: 0.1 to 1 MHz • External gate width measurement $P0A_1$/FCG pin		
Supply voltage		• V_{DD} = 4.5 to 5.5 V (PLL and CPU operations) • V_{DD} = 3.5 to 5.5 V (PLL stop, CPU operation) • V_{DD} = 2.2 to 5.5 V (Crystal resonator stop)		
Package		80-pin plastic QFP		

3. WRITE/READ/VERIFY THE ONE-TIME PROM (PROGRAM MEMORY)

The program memory built in μPD17P005 is a 15864 x 8-bit electrically writable one-time PROM. This PROM is accessed in 1-word, 16-bit in normal operation mode and in 1-word, 8-bit in program memory write/read/verify mode. In this case, the upper 8 bits of 1-word, 16 bits are allocated to even address and the lower 8 bits to odd address, respectively.

At PROM write/read/verify, set to PROM mode and use those pins shown in Table 3-1.

Addresses are updated by the clock input from the CLK pin instead of the address input.

Table 3-1 Pins to be used at program memory write/read/verify

Pin Name	Function
V_{PP}	Program voltage application pin. 12.5 V applied. Used as INT1 pin in normal operation mode.
CLK	Address update clock input pin
MD0–MD3	Operation mode select pin
D0–D7	8-bit data input/output pin
V_{DD1}, V_{DD2}	Supply voltage application pin. 6 V applied 5 V ±10 % applied in normal operation mode.

The built-in PROM is written using the specified PROM programmer and dedicated program adapter. Use the following PROM programmer and program adapter.

PROM programmer: AF-9703 (Ando Electric Co.)
AF-9704 (Ando Electric Co.)

Program adapter: AF-9803 (Ando Electric Co.)

3.1 Operation Mode at Program Memory Write/Read/Verify

The μPD17P005 changes to the program memory write/read/verify mode when +6 V is applied to the V_{DD} pin and +12.5 V to the V_{PP} pin.

According to the setting of the MD0–MD3, this mode is set to the operation mode as shown in Table 3-2.

All input pins not used in program memory write/read/verify mode are connected to the ground via the pull-down resistance (470 Ω).

Table 3-2 Operation mode at program memory write/read/verify

Designation of operation mode						Operation mode
V_{PP}	V_{DD}	MD0	MD1	MD2	MD3	
+12.5 V	+6 V	H	L	H	L	0 clear of program memory address
		L	H	H	H	Write mode
		L	L	H	H	Read/verify mode
		H	X	H	H	Program inhibit mode

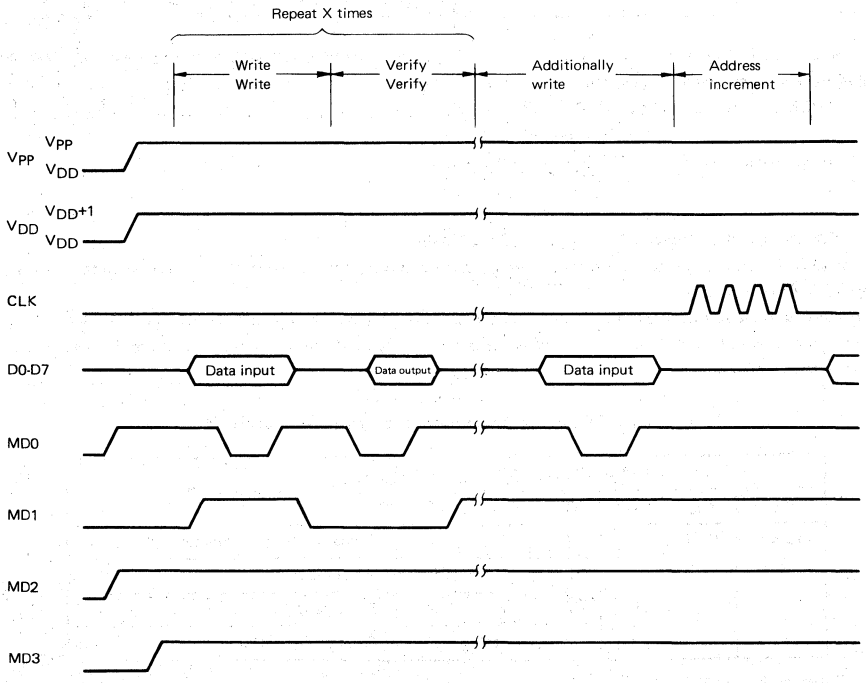
Remark X: L or H

3.2 Program Memory Write Procedure

The program memory write procedure is as follows and High-speed write is avilable.

(1) Pull down the input pins not in use to the ground via the resistance. Set the CLK pin low.
(2) Supply 5 V to the V_{DD} and V_{PP} pins.
(3) Wait for 10 μs.
(4) 0 clear mode of program memory address.
(5) Supply 6 V to the V_{DD} pin and 12.5 V to the V_{PP} pin.
(6) Program inhibit mode
(7) Write data in 1 ms write mode.
(8) Program inhibit mode
(9) Verify mode. Proceed to (1) if written. If not, repeat steps (7) to (9).
(10) Times written in (7) to (9): X) x 1 ms additional writing
(11) Program inhibit mode
(12) The program memory address is updated (+1) by inputting 4 pulse signals to the CLK pin.
(13) Repeat (7) to (12) up to the final address.
(14) 0 clear mode of program memory address
(15) Change the V_{DD}/V_{PP} pin voltage to 5 V.
(16) Power OFF

Steps (2) to (12) are schematically shown below.

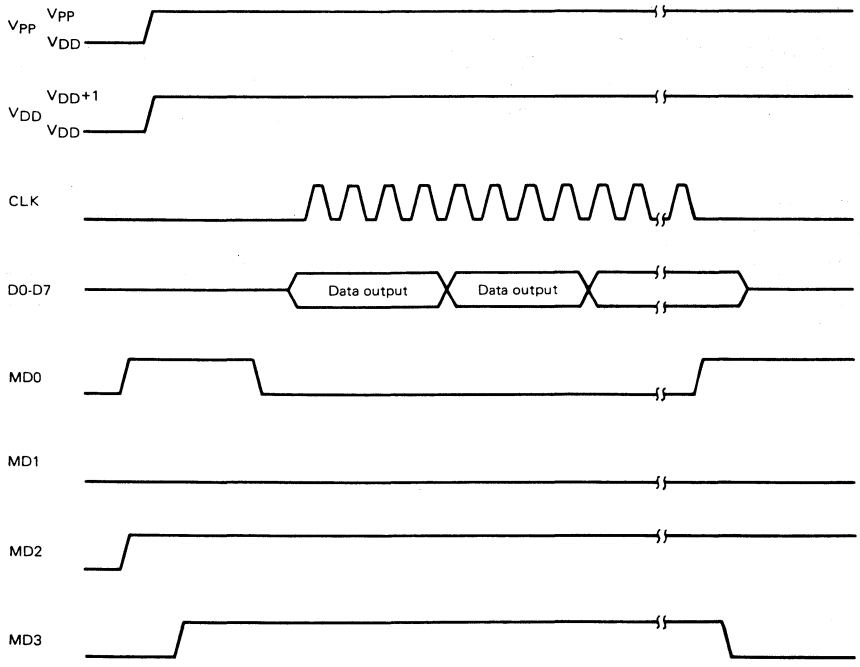


3.3 Program Memory Read Procedure

The μPD17P005 can read the contents of program memory by the following procedures.

(1) Pull down the input pins not in use to the ground via the resistance. Set the CLK pin low.
(2) Supply 5 V to the V_{DD} and V_{PP} pins.
(3) Wait for 10 μs.
(4) 0 clear mode of program memory address.
(5) Supply 6 V to the V_{DD} pin and 12.5 V to the V_{PP} pin.
(6) Program inhibit mode
(7) Verify mode. Sequentially output the data of one address each time 4 clock pulse signals are input to the CLK pin.
(8) Program inhibit mode
(9) 0 clear mode of program memory address
(10) Change the V_{DD}, V_{PP} pin voltage to 5 V.
(11) Power OFF

Steps (2) to (9) are shown below.



4. ELECTRIC CHARACTERISTICS

ABSOLUTE MAXIMUM RATING (T_a = 25 ±2 °C)

Supply Voltage	V_{DD}		−0.3 to +6.0	V
Input Voltage	V_I		−0.3 to V_{DD} + 0.3	V
Output Voltage	V_O	Except $P1B_1$–$P1B_3$, $P0A_2$, $P0A_3$, LPF_{OUT}	−0.3 to V_{DD} + 0.3	V
Ouput Withstand Voltage	V_{BDS1}	$P1B_1$–$P1B_3$, LPF_{OUT}	18.0	V
Output Withstand Voltage	V_{BDS2}	$P0A_2$, $P0A_3$	V_{DD} + 0.3	V
High level Output Current	I_{OH}	1 pin	−12	mA
		All pins	−20	mA
Low Level Output Current	I_{OL}	1 pin	12	mA
		All pins	20	mA
Operating temperature	T_{opt}		−40 to +85	°C
Storage temperature	T_{stg}		−55 to +125	°C

RECOMMENDED OPERATION CONDITIONS

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Supply Voltage	V_{DD1}	4.5	5.0	5.5	V	PLL and CPU operations
Supply Voltage	V_{DD2}	3.5	5.0	5.5	V	PLL stop, CPU operation
Data Retention Voltage	V_{DDR}	2.2		5.5	V	Crystal resonator stop
Supply Voltage Rise Time	t_{rise}			500	ms	V_{DD} = 0 → 4.5 V
Input Amplitude	V_{in1}	0.5		V_{DD}	V_{P-P}	VCOL,VCOH
Input Amplitude	V_{in2}	0.5		V_{DD}	V_{P-P}	AMIFC, FMIFC
Output Withstand Voltage	V_{BDS}			16.0	V	$P1B_1$–$P1B_3$, LPF_{OUT}
Operating Temperature	T_{opt}	−40		+85	°C	

DC CHARACTERISTICS (T_a = −40 to +85 °C, V_{DD} = 4.5 to 5.5 V)

CHARACTERISTIC	SYMBOL	STANDARD VALUE				CONDITION
		MIN.	TYP.	MAX.	UNIT	
Supply Voltage	V_{DD1}	4.5	5.0	5.5	V	CPU and PLL operations
Supply Voltage	V_{DD2}	3.5	5.0	5.5	V	CPU operation, PLL stop
Data Retention Voltage	V_{DDR1}	3.5		5.5	V	At power failure detection by timer F/F. At crystal oscillation.
Data Retention Voltage	V_{DDR2}	2.2		5.5	V	At power failure detection by timer F/F. When crystal oscillation is stopped.
Data Retention Voltage	V_{DDR3}	2.0		5.5	V	Data memory (RAM) Retention
Data Retention Current	I_{DDR1}		2	15	μA	When crystal oscillation is stopped. T_a=25 °C
Data Retention Current	I_{DDR2}		2	10	μA	When crystal oscillation is stopped. V_{DD}=5.0 V, T_a=25 °C
Intermediate Level Output Voltage	V_{OM1}	2.3	2.5	2.7	V	COM_0, COM_1, V_{DD}=5 V
High Level Input Voltage	V_{IH1}	0.8 V_{DD}		V_{DD}	V	$P0A_0$–$P0A_3$, $P0B_0$–$P0B_3$, $P0C_0$–$P0C_3$, $P1A_0$–$P1A_3$, $P1D_0$–$P1D_3$, CE, INT_0, INT_1
High Level Input Voltage	V_{IH2}	0.6 V_{DD}		V_{DD}	V	$P0D_0$–$P0D_3$
Low Level Input Voltage	V_{IL}	0		0.2 V_{DD}	V	$P0A_0$–$P0A_3$, $P0B_0$–$P0B_3$, $P0C_0$–$P0C_3$, $P0D_0$–$P0D_3$, $P1A_0$–$P1A_3$, $P1D_0$–$P1D_3$, CE, INT_0, INT_1
High Level Output Current	I_{OH1}	−1.0	−5.0		mA	$P0A_0$, $P0A_1$, $P0B_0$–$P0B_3$, $P0C_0$–$P0C_3$, $P1A_0$–$P1A_3$, $P1C_0$–$P1C_3$, $P1B_0$, $P2A_0$ V_{OH}=V_{DD}−1 V
High Level Output Current	I_{OH2}	−1.0	−4.0		mA	LCD_0–LCD_{29}, EO_0, EO_1 V_{OH}=V_{DD}−1 V
Low Level Output Current	I_{OL1}	1.0	7.0		mA	$P0A_0$–$P0A_3$, $P0B_0$–$P0B_3$, $P0C_0$–$P0C_3$, $P1A_0$–$P1A_3$, $P1C_0$–$P1C_3$, $P1B_0$, $P2A_0$ V_{OL}=1 V
Low Level Output Current	I_{OL2}	1.0	3.5		mA	LCD_0–LCD_{29}, EO_0, EO_1 V_{OL}=1 V
Low level Output current	I_{OL3}	1.0	2.0		mA	$P1B_1$–$P1B_3$ V_{OL}=1 V
Low Level Output Current	I_{OL4}	1.0	10.0		mA	$P0A_2$, $P0A_3$ V_{OL}=1 V
High Level Input Current	I_{IH1}	0.1	0.8		mA	At VCOH pull-down. V_{IH}=V_{DD}
High Level Input Current	I_{IH2}	0.1	0.8		mA	At VCOL pull-down. V_{IH}=V_{DD}
High Level Input Current	I_{IH3}	0.1	1.3		mA	At X_{IN} pull-down. V_{IH}=V_{DD}
High Level Input Current	I_{IH4}	0.05	0.13	0.30	mA	At $P0D_0$–$P0D_3$ pull-down. V_{IH}=V_{DD}
Output Leakage Current	I_{L1}			500	nA	$P0A_2$, $P0A_3$ V_{OH}=V_{DD}
Output Leakage Current	I_{L2}			500	nA	$P1B_1$–$P1B_3$, LPF_{OUT} V_{OH}=16 V
Output Leakage Current	I_{L3}			±100	nA	EO_0, EO_1 V_{OH}=V_{DD}, V_{OL}=0 V

AC CHARACTERISTICS (T_a = −40 to +85 °C, V_{DD} = 4.5 to 5.5 V)

CHARACTERISTIC	SYMBOL	STANDARD VALUE				CONDITION
		MIN.	TYP.	MAX.	UNIT	
Operating Frequency	f_{in1}	0.5		30	MHz	VCOL MF mode Sine wave input V_{in} = 0.3 V_{P-P}
Operating Frequency	f_{in2}	5		40	MHz	VCOL HF mode Sine wave input V_{in} = 0.3 V_{P-P}
Operating Frequency	f_{in3}	9		150	MHz	VCOH Sine wave input V_{in} = 0.3 V_{P-P}
Operating Frequency	f_{in4}	0.1		1	MHz	AMIFC Sine wave input V_{in} = 0.3 V_{P-P}
Operating Frequency	f_{in5}	0.44		0.46	MHz	AMIFC Sine wave input V_{in} = 0.05 V_{P-P}
Operating Frequency	f_{in6}	5		15	MHz	FMIFC Sine wave input V_{in} = 0.3 V_{P-P}
Operating Frequency	f_{in7}	10.5		10.9	MHz	FMIFC Sine wave input V_{in} = 0.06 V_{P-P}
Analog-to Digital Conversion Resolution				6	bit	
Analog-to-Digital Conversion Total Error			±1	±1.5	LSB	T_a = −10 to +50 °C

REFERENCE CHARACTERISTICS

CHARACTERISTIC	SYMBOL	STANDARD VALUE				CONDITION
		MIN.	TYP.	MAX.	UNIT	
Supply Current	I_{DD3}		15		mA	CPU and PLL operations VCOH sine wave input f_{in} = 150 MHz, V_{in} = 0.5 V_{P-P} V_{DD} = 5 V, T_a = 25 °C
High Level Output Current	I_{OH4}		−0.2		mA	COM_0, COM_1 V_{OH} = V_{DD}−1 V
Intermediate Level Output Current	I_{OM1}		−20		μA	COM_0, COM_1 V_{OM} = V_{DD}−1 V
Intermediate Level Output Current	I_{OM2}		20		μA	COM_0, COM_1 V_{OM} = 1 V
Low Level Output Current	I_{OL5}		0.2		mA	COM_0, COM_1 V_{OL} = 1 V

DC PROGRAMMING CHARACTERISTICS (T_a = 25 °C, V_{DD} = 6.0 ±0.25 V, V_{PP} = 12.5 ±0.5 V)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
High Level Input Voltage	V_{IH1}	0.7 V_{DD}		V_{DD}	V	Other than CLK
	V_{IH2}	V_{DD}-0.5		V_{DD}	V	CLK
Low Level Input Voltage	V_{IL1}	0		0.3 V_{DD}	V	Other than CLK
	V_{IL2}	0		0.4	V	CLK
Input Leakage Current	I_{L1}			±10	μA	V_{IN} = V_{IL} or V_{IH}
High Level Output Voltage	V_{OH}	V_{DD}-1.0			V	I_{OH} = −1 mA
Low Level Output Voltage	V_{OL}			1.0	V	I_{OL} = 1 mA
V_{DD} Supply Current	I_{DD}			30	mA	
V_{PP} Supply Current	I_{PP}			30	mA	MD0 = V_{IL}, MD1 = V_{IH}

Note 1: Be sure to keep V_{PP} below +13.5 V including overshoot.

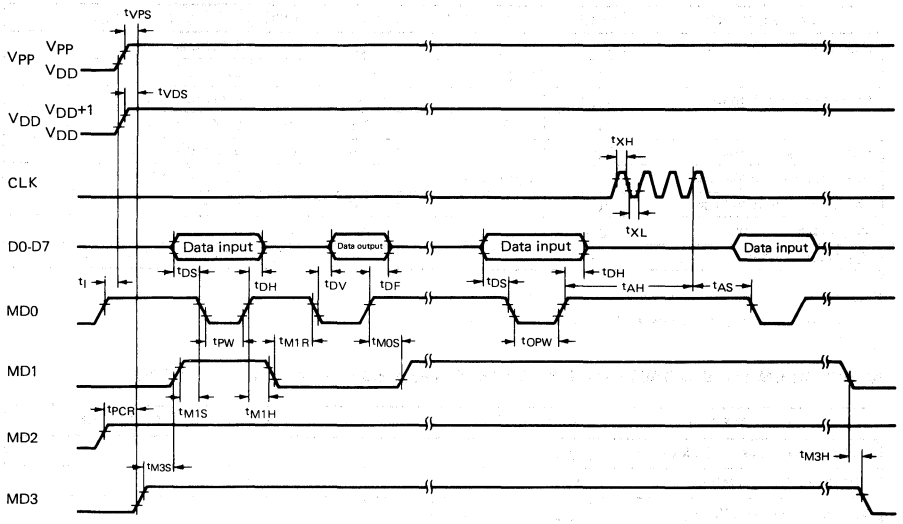
2: Be sure to apply V_{DD} before V_{PP} and cut it after V_{PP}.

AC PROGRAMMING CHARACTERISTICS (T_a = 25 °C, V_{DD} = 6.0 ±0.25 V, V_{PP} = 12.5 ±0.5 V)

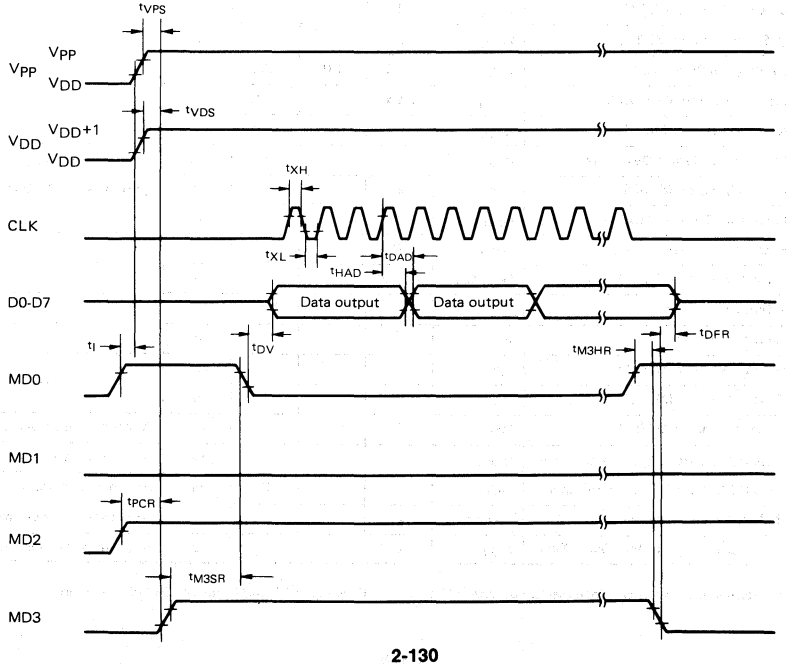
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Address Setup Time (*) (vs MD0 ↓)	t_{AS}	2			μs	
MD1 Setup Time (vs MD0 ↓)	t_{M1S}	2			μs	
Data Setup Time (vs MD0 ↓)	t_{DS}	2			μs	
Address Hold Time (*) (vs MD0 ↑)	t_{AH}	2			μs	
Data Hold Time (vs MD0 ↑)	t_{DH}	2			μs	
MD0 ↑ to Data Output Float Delay Time	t_{DF}	0		130	ns	
V_{PP} Setup Time (vs MD3 ↑)	t_{VPS}	2			μs	
V_{DD} Setup Time (vs MD3 ↑)	t_{VDS}	2			μs	
Initial Program Pulse Width	t_{PW}	0.95	1.0	1.05	ms	
Additional Program Pulse Width	t_{OPW}	0.95		21.0	ms	
MD0 Setup Time (vs MD1 ↑)	t_{MOS}	2			μs	
MD0 ↓ to Data Output Delay Time	t_{DV}			1	μs	MD0 = MD1 = V_{IL}
MD1 Hold Time (vs MD0 ↑)	t_{M1H}	2			μs	$t_{M1H} + t_{M1R} \geq 50$ μs
MD1 Recover Time (vs MD0 ↓)	t_{M1R}	2			μs	
Program Counter Reset Time	t_{PCR}	10			μs	
CLK Input High/Low Level Width	t_{XH}, t_{XL}	0.125			μs	
CLK Input Frequency	f_X			4.19	MHz	
Initial Mode Set Time	t_I	2			μs	
MD3 Setup Time (vs MD1 ↑)	t_{M3S}	2			μs	
MD3 Hold Time (vs MD1 ↓)	t_{M3H}	2			μs	
MD3 Setup Time (vs MD0 ↓)	t_{M3SR}	2			μs	At program memory read.
Address (*) to Data Output Delay Time	t_{DAD}	2			μs	At program memory read.
Address (*) to Data Output Hold Time	t_{HAD}	0		130	ns	At program memory read.
MD3 Hold Time (vs MD0 ↑)	t_{M3HR}	2			μs	At program memory read.
MD3 ↓ to Data Output Float Delay Time	t_{DFR}	2			μs	At program memory read.

*: The internal address signal is incremented by one (+1) at the 3rd CLK input fall and is not connected to the pin.

PROGRAM MEMORY WRITE TIMING



PROGRAM MEMORY READ TIMING



4-BIT SINGLE-CHIP MICROCONTROLLER

The μPD17006 is a 4-bit single-chip CMOS microcontroller for use with a digital tuning system.

The CPU employs 17K architecture which enables to directly operate a data memory by one instruction and to control various operations and peripheral hardware. Each instruction is comprised to one 16-bit word.

The peripheral hardware incorporates a variety of input/output ports, a serial interface, a clock generator port, a prescalar for digital tuning, a PLL frequency synthesizer, a timer for remote controlled decoding, etc.

To cope with the RDS (Radio Data System) various timer functions, interrupt functions and external SRAM interface functions are incorporated.

Thus, a high-performance, multi-functional digital tuning sytem can be constructed.

The μPD17P006* having an on-chip one-time PROM is also available for mask ROM product, μPD17006 program evaluation and small production.

An easy-to-use incircuit emulator (IE-17K) and an assembler (AS17K) are available as μPD17006 system development tools.

*: Under development

FEATURES

- 4-bit microcontroller for digital tuning
- Program memory (ROM):
  24K bytes (12288 x 16 bits)
- General-purpose data memory (RAM):
  896 nibbles (896 x 4 bits)
- Instruction execution time:
  1.78 μs (when a 4.5 MHz crystal oscillator is used.)
- Stack level: 7
- A set of 46 easy-to-understand instructions
- Decimal operation enable
- 12K-step table reference enable
- On-chip PLL frequency synthesizer and 150 MHz prescalar
- 12 kinds of reference frequencies can be selected using appropriate programs
- 2-system error output (EO_{00}, EO_{01} and EO_{10} systems)
- On-chip IF counter (AMIFC, FMIFC)
- On-chip 8-bit serial interface
  2 systems with 3 channels:
  2-wire and 3-wire interfaces
- On-chip D/A converter:
  9 bits x 3 channels (PWM output)
  Usable as a modulo timer
- On-chip A/D converter: 8 bits x 6 channels
  Hardware (32 μs) and software conversion
  Also serves as an external event counter.
- Various timer functions
  12-bit modulo timer (remote controlled: 10, 50 μs)
  8-bit module timer (RDS clock synchronization: 10, 100 μs)
  8-bit modulo timer (general-purpose: 10, 100, 500, 1000 μs)
  Timer carry (general-purpose: 100 ms)
- Various interrupts
  External interrupt: 2 channels (INT_1, INT_2 pins)
  Internal interrupt: 4 channels (timer: 3 channels, serial interface: 1 channel)
  Dual-function interrupt:
  2 channels (serial interface: 2 channels, A/d converter, IF counter and timer overflow)
- General-purpose input/output ports
  Input/output port: 48
  Input port: 8 (with 4 on-chip pull-down resistors)
  Output port: 11
- On-chip function of parallel interface with the external SRAM
- On-chip power-ON reset, CE reset and power failure detection circuit
- CMOS Low power consumption
- Supply voltage: 5 V ±10 %
- 80-pin plastic QFP

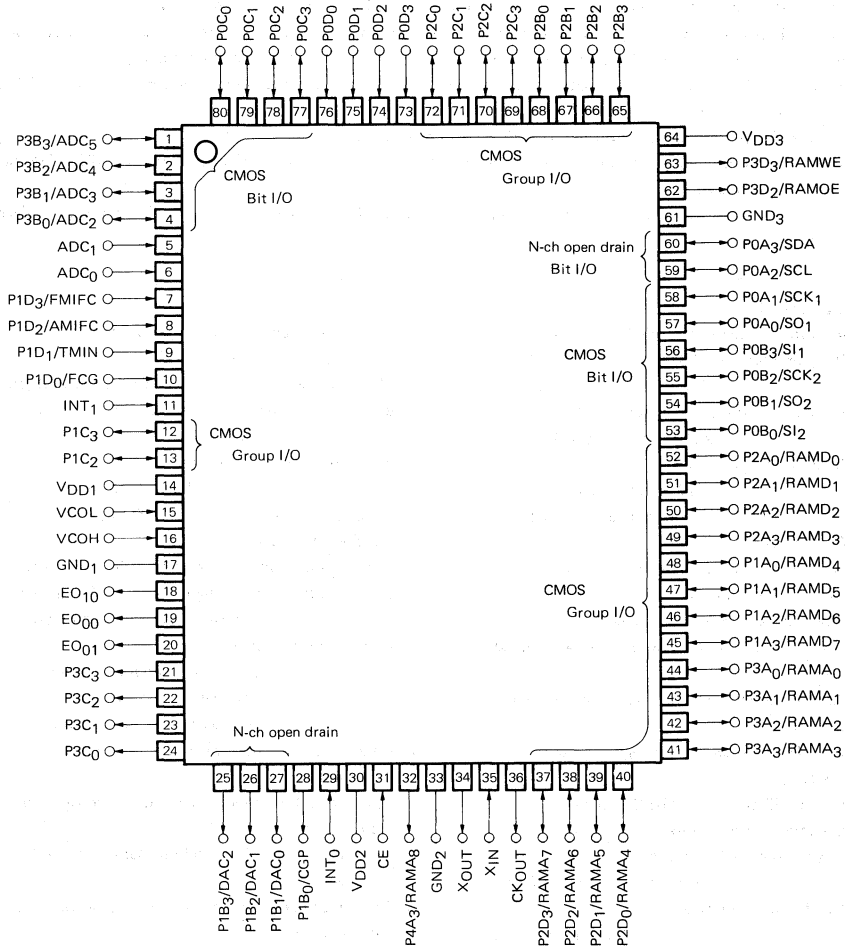
Notes on Serial interface: **The 2-wire mode corresponds to the I2C-Bus specification from Philips. In case of using this interface mode note the following:**

Duties when using I2C bus system

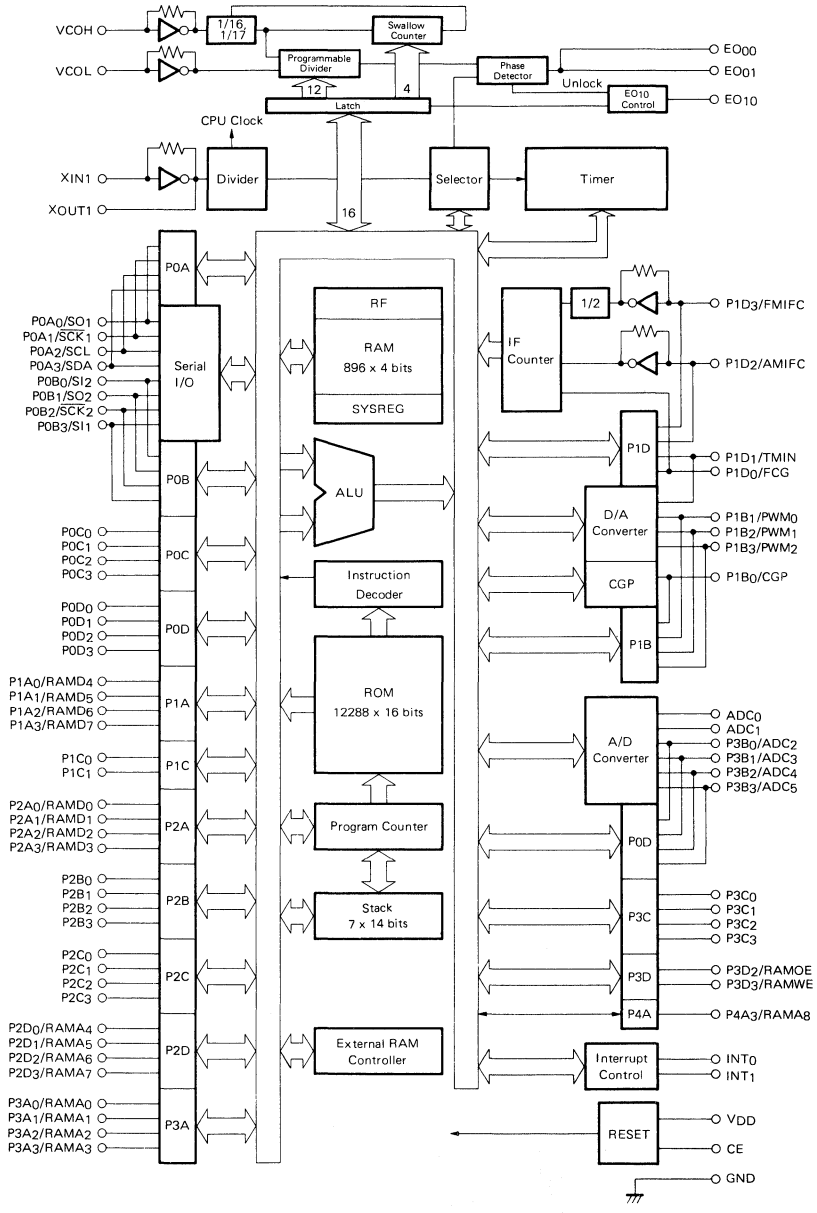
Purchase of NEC's I2C bus system hardware components conveys a license under the Philips I2C patents rights to use this components in an I2C system, provided that the system conforms the I2C standard specifications as defined by Philips.

Consequently for all ROM based components with I2C hardware circuits the user is kindly requested to notify the use of the I2C bus interface at the ROM code verification stage.

PIN CONFIGURATION (Top View)



BLOCK DIRAGRAM



SINGLE-CHIP MICROCONTROLLER

The μPD17P006 is a 4-bit single-chip CMOS microcontroller for use with a digital tuning system.

The CPU employs 17K architecture which enables to directly operate a data memory by one instruction and to control various operations and peripheral hardware. Each instruction is comprised of one 16-bit word.

The peripheral hardware incorporates a variety of input/output ports, a serial interface, a clock generator port, a prescalar for digital tuning, a PLL frequency synthesizer, a timer for remote controlled decoding, etc.

To cope with the RDS (Radio Data System) various timer functions, interrupt functions and external SRAM interface functions are incorporated.

Thus, a high-performance, multi-functional digital tuning system can be constructed.

The μPD17P006 has an on-chip one-time PROM, making it useful for mask ROM product μPD17006* program evaluation and small production.

An easy-to-use incircuit emulator (IE-17K) and an assembler (AS17K) are available as μPD17P006 system development tools.

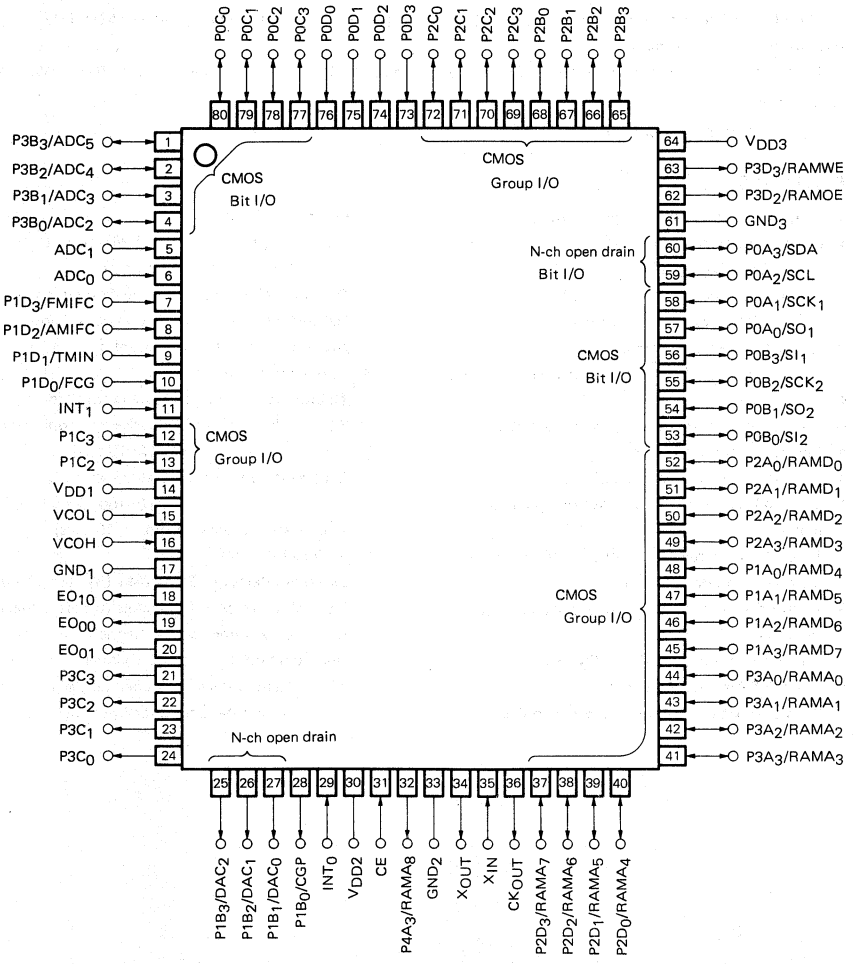
*: Under development

FEATURES

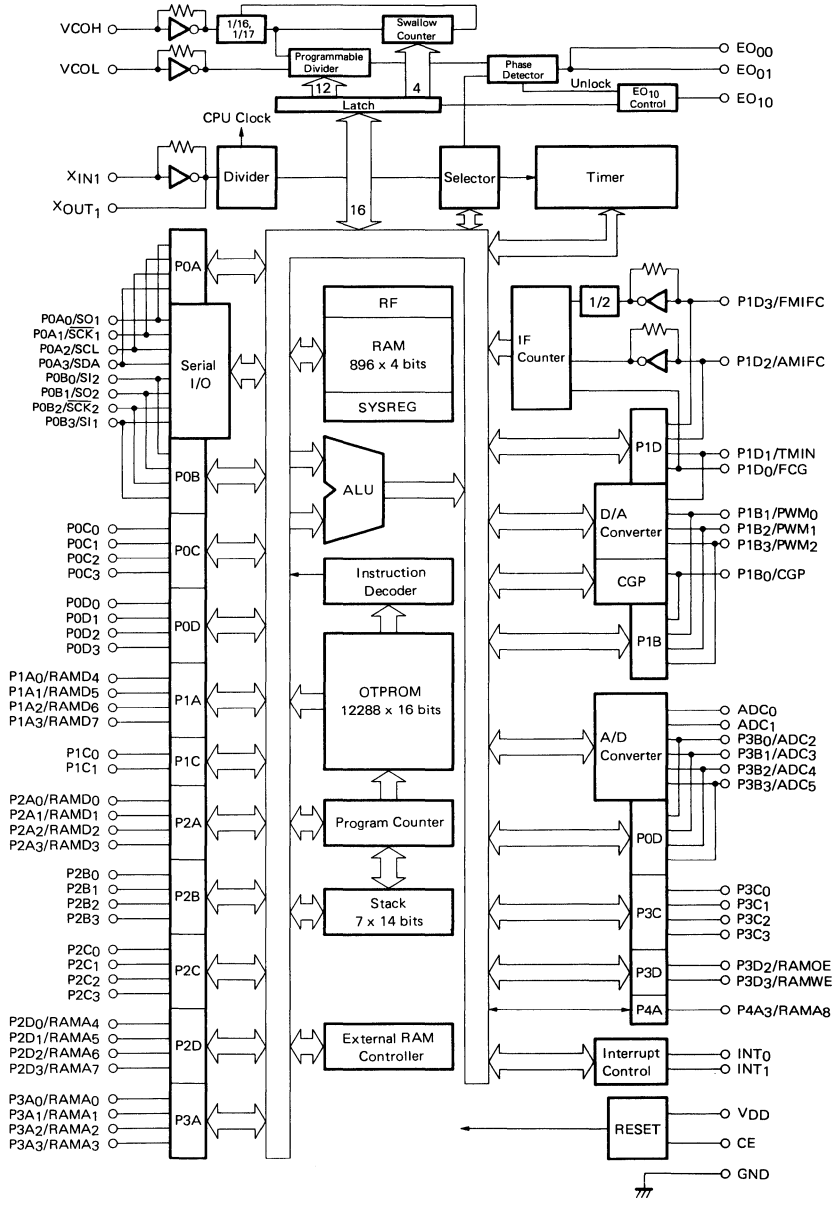
- 4-bit microcontroller for digital tuning
- Program memory (OTPROM):
  24K bytes (12288 x 16 bits)
- General-purpose data memory (RAM):
  896 nibbles (896 x 4 bits)
- Instruction execution time: 1.78 μs
  (when a 4.5 MHz crystal oscillator is used.)
- Stack level: 7
- A set of 46 easy-to-understand instructions
- Decimal operation enable
- 12K-step table reference enable
- On-chip PLL frequency synthesizer and 150 MHz prescalar
- 12 kinds of reference frequencies can be selected using appropriate programs
- 2-system error output (EO_{00}, EO_{01} and EO_{10} systems)
- On-chip IF counter (AMIFC, FMIFC)
- On-chip 8-bit serial interface
  2 systems with 3 channels: 2-wire and 3-wire
- On-chip D/A converter:
  9 bits x 3 channels (PWM output)
  Usable as a modulo timer
- On-chip A/D converter: 8 bits x 6 channels
  Hardware (32 μs) and software conversion
  Also serves as an external event counter.
- Various timer functions
  12-bit modulo timer (remote controlled: 10, 50 μs)
  8-bit modulo timer (RDS clock syncronization:
  10, 100 μs)
  8-bit modulo timer (general-purpose:
  10, 100, 500, 1000 μs)
  Timer carry (general-purpose: 100 ms)
- Various interrupts
  External interrupt: 2 channels (INT_1, INT_2 pins)
  Internal interrupt: 4 channels (timer: 3 channels,
  serial interface: 1 channel)
  Dual-function interrupt: 2 channels
  (serial interface: 2 channels, A/D converter,
  IF counter and timer overflow)

- General-purpose input/output ports
  Input/output port: 42
  Input port: 8 (with 4 on-chip pull-down resistors)
  Output port: 11
- On-chip function of parallel interface with the external SRAM
- On-chip power-ON reset, CE reset and power failure detection circuit
- CMOS low power consumption
- Supply voltage: 5 V ±10 %
- 80-pin plastic QFP

PIN CONFIGURATION (Top View)



BLOCK DIAGRAM



4-BIT SINGLE-CHIP MICROCONTROLLER

The μPD17010 is a 4-bit single-chip microcontroller for digital tunign system which incorporates the sprecaler operational up to 150 MHz, PLL frequency synthesizer, LCD driver, and IF counter.

Since the CPU has no accumulator and adopts 17K architecture which may control the data memory directly, you can perform very effecient programming. It is necessary to be noted that any instruction is 16-bit length 1 word.

PLL frequency synthesizer can operate in pulse swallow system and select such high frequency as 50 or 100 kHz, which makes it much easier to configure a high-performance tuner. Since it also incorporates 16-bit frequency counter, you can use it for the detection of broadcast by counting the intermediate frequency of a tuner.

IE-17K (incircuit emulator) and AS17K (assembler) are available as well, which are easy-to-use as the tools of μPD17010 system development.

Since One-Time PROM version, μPD17P010: is available as well, it is recommendable for the system evaluation when developing the system of μPD17010 and for its small production.

*: Under development

FEATURES

- 4-bit single-chip microcontroller for digital tuning system
- Program memory (ROM)
  - μPD17010: 7932 x 16 bits
- Data memory (RAM)
  - μPD17010: 432 x 4 bits
- Stack level: 9
- Perceptible 35 types of instruction set
- Decimal operational
- Instruction execution time: 4.44 μs (when connecting a 4.5 MHz crystal resonator)
- On-chip PLL frequency synthesizer and 150 MHz prescaler
- 12 types of reference frequency selectable by program
- On-chip LCD driver (1/2 bias, 1/2 duty, frame frequency: 250 Hz)
- On-chip IF counter (AMIFC, FMIFC)
- On-chip 8-bit serial interface (2 systems 3 channels: 3-wire and 2-wire)
- On-chip 12-bit timer modulo counter
- On-chip 8-bit D/A converter: 3 outputs (PWM)
- On-chip 6-bit A/D converter: 6 inputs
- On-chip service interruption detector and power-on reset circuit
- Interrupt (external: 2 systems, internal: 4 systems)
- Various I/O ports available (33 ports (+ 30 ports: segment pins))
- On-chip CGP (Clock Generator Port)
- 5 V ±10 %
- CMOS low power consumption
- 80-pin plastic QFP

Notes on Serial interface:

The 2-wire mode corresponds to the I2C-Bus specification from Philips.

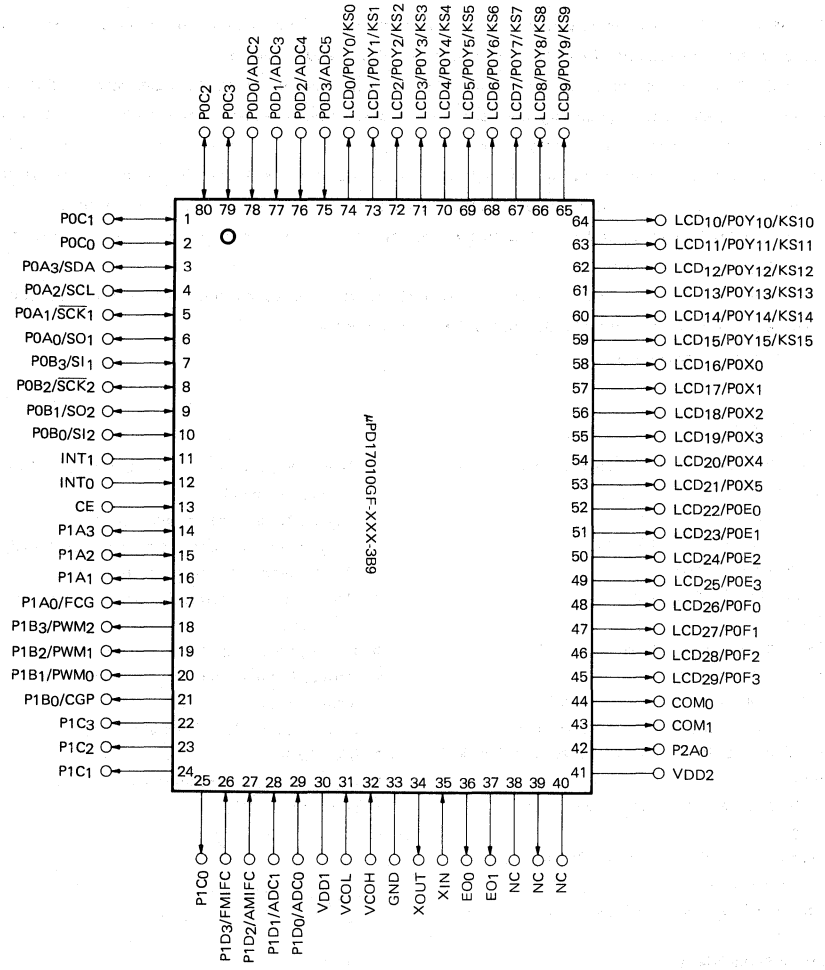
In case of using this interface mode note the following:

Duties when using I2C bus system

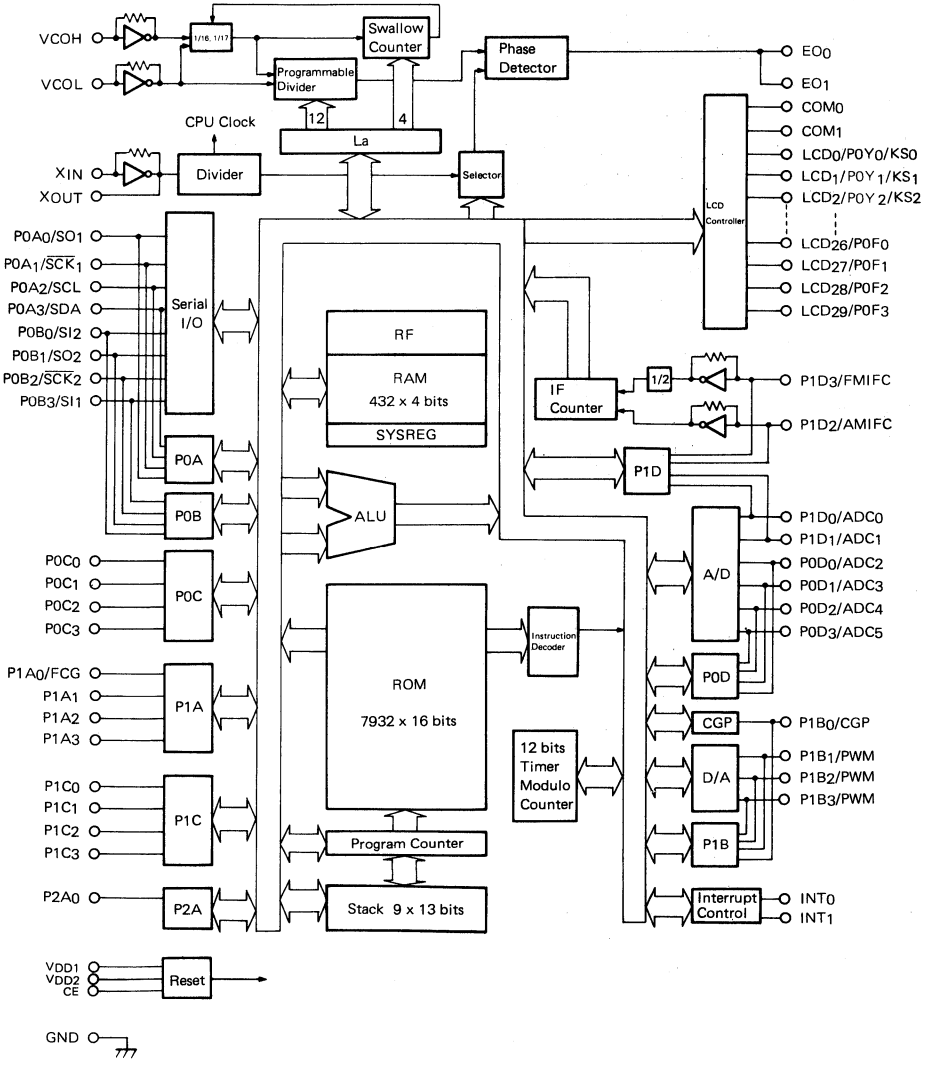
Purchase of NEC's I2C bus system hardware components conveys a license under the Philips I2C patents rights to use this components in an I2C system, provided that the system conforms the I2C standard specifications as defined by Philips.

Consequently for all ROM based components with I2C hardware circuits the user is kindly requested to notify the use of the I2C bus interface at the ROM code verification stage.

PIN CONFIGURATION (Top View)



BLOCK DIAGRAM



FUNCTION LIST

Product Name	μPD17010	μPD17P010
ROM	7932 x 16 bits	
RAM	432 x 4 bits	
System register	12 x 4 bits	
Register file	41 x 4 bits	
Port register	7 x 4 bits	
Port	Input/output port : 16 ports Input port : 8 ports Output port : 9 ports (+30 ports: Segment pins)	
Serial interface	• 2 systems, 3 channels 8 bits, 3-wire and 2-wire	
Interrupt	• 6 channels External interrupt : 2 channels Internal interrupt : 4 channels	
Timer	Timer carry (1 ms, 5 ms, 100 ms, 250 ms) Timer interrupt (1 ms, 5 ms, 100 ms, 250 ms) 12-bit timer modulo counter (10 μs, 11.1 μs, 333.3 μs, 1 ms)	
Standby function	• STOP, HALT	
Power supply voltage	V_{DD} = 5 V ±10 %	
Package	80-pin plastic QFP	

4-BIT SINGLE-CHIP MICROCONTROLLER

μPD17P010 is the 4-bit single-chip microcontroller for digital tuning system which incorporates the prescaler operational up to 150 MHz, PLL frequency synthesizer, LCD driver, and IF counter.

Since the CPU has no any accumulator and adopts 17K architecture which can control the data memory directly, you can perform very efficient programming. It is necessary to be noted that any instruction is 16-bit length 1 word.

PLL frequency synthesizer can operate in pulse swallow system and select such high frequency as 50 or 100 kHz, which makes it much easier to configure a high performance tuner. Since it also incorporates 16-bit frequency counter, you can use it for the detection of broadcast by counting the intermediate frequency of a tuner.

IE-17K (incircuit emulator) and AS17K (assembler) are available, which are easy-to-use as the tools of μPD17P010 system development.

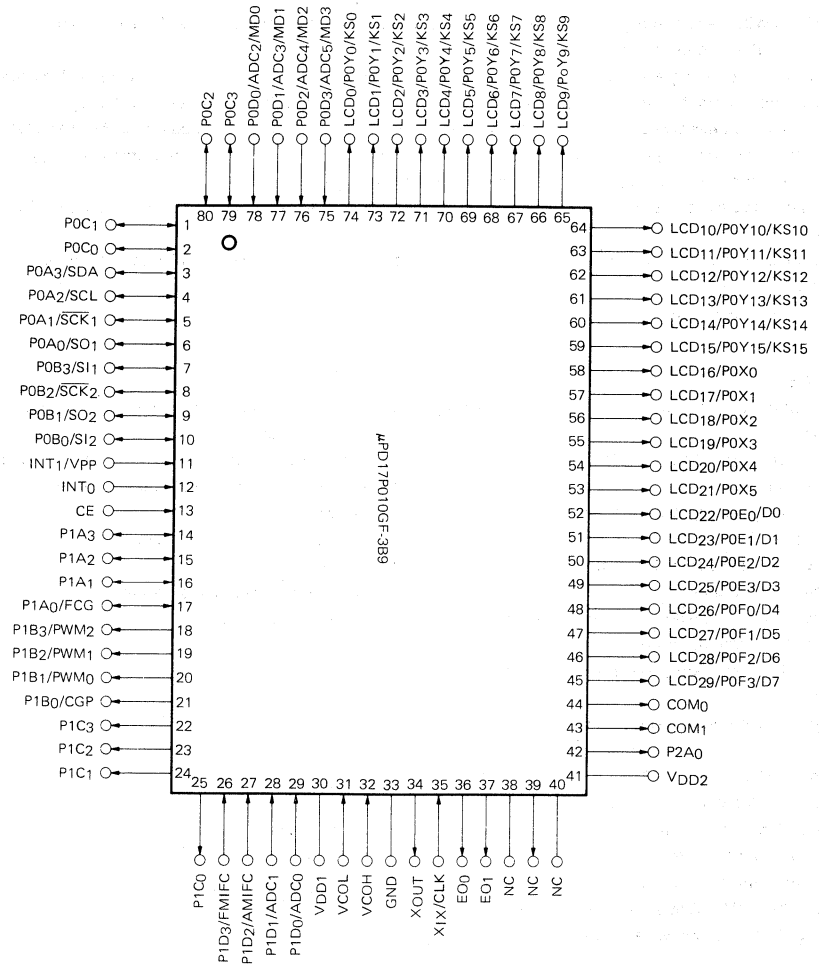
Since it incorporates One-Time PROM, it is useful for the system evaluation when developing the system of μPD17010*, and for small production.

*: Under development.

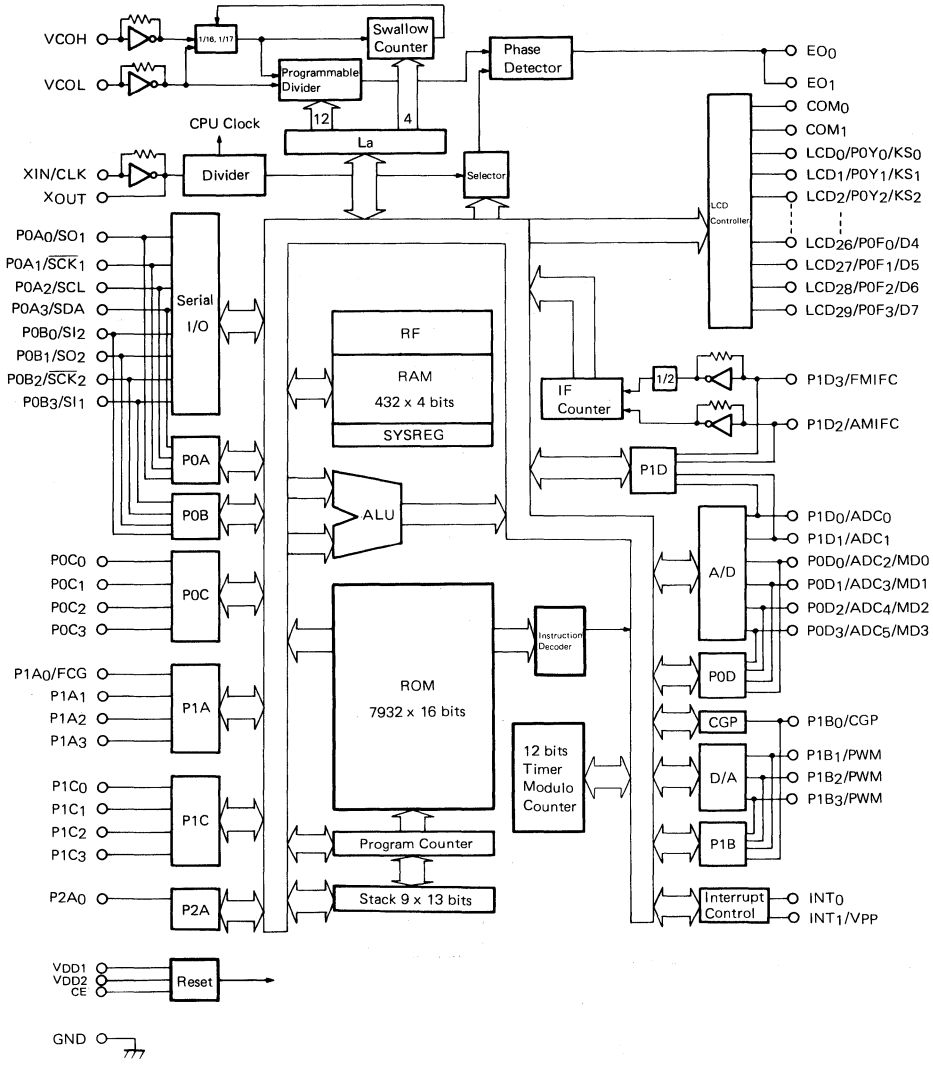
FEATURES

- 4-bit single chip microcontroller for digital tuning system
- Program memory (One-Time PROM): 7932 x 16 bits
- Data memory (RAM): 432 x 16 bits
- Stack level: 9
- Perceptible 35 types of instruction set
- Decimal operational
- Instruction execution time: 4.44 μs (when connecting a 4.5 MHz crystal resonator)
- On-chip PLL frequency synthesizer and 150 MHz prescaler
- 12 types of reference frequency selectable by program
- On-chip LCD driver (1/2 bias, 1/2 duty, frame frequency: 250 MHz)
- On-chip 8-bit serial interface (2 systems 3 channels: 3-wire and 2-wire)
- 12-bit timer modulo counter
- On-chip 8-bit D/A converter: 3 outputs (PWM)
- On-chip 6-bit A/D converter: 6 inputs
- On-chip service interruption detector and power-on reset circuit
- Interrupt (external: 2 systems, internal: 4 systems)
- Various I/O ports available (33 ports (+30 ports: Segment pins))
- On-chip CGP (Clock Generator Port)
- 5 V ±10 %
- CMOS low power consumption
- 80-pin plastic QFP

PIN CONFIGURATION (TOP VIEW)



BLOCK DIAGRAM



FUNCTION LIST

Product Name	μPD17010	μPD17P010
ROM	7932 x 16 bits	
RAM	432 x 4 bits	
System register	12 x 4 bits	
Register file	41 x 4 bits	
Port register	7 x 4 bits	
Port	Input/output port : 16 ports Input port : 8 ports Output port : 9 ports (+30 ports: Segment pins)	
Serial interface	• 2 systems, 3 channels 8 bits, 3-wire and 2-wire	
Interrupt	• 6 channels External interrupt : 2 channels Internal interrupt : 4 channels	
Timer	Timer carry (1 ms, 5 ms, 100 ms, 250 ms) Timer interrupt (1 ms, 5 ms, 100 ms, 250 ms) 12-bit timer modulo counter (10 μs, 11.1 μs, 333.3 μs, 1 ms)	
Standby function	• STOP, HALT	
Power supply voltage	V_{DD} = 5 V ±10 %	
Package	80-pin plastic QFP	

SINGLE CHIP MICROCOMPUTER FOR PLL FREQUENCY SYNTHESIZER BUILT-IN IMAGE DISPLAY CONTROLLER

μPD17002 is a 4 bits CMOS microcomputer for digital tuning system in single chip incorporating an Image Display Controller with various kinds of display capability and a PLL frequency synthesizer.

CPU has 4-bit parallel addition and substruction instructions, logical operation instructions, bit test instructions, carry F/F set and reset instructions, interrupt function, and timer function. Built-in user programable IDC (Image Display Controller) controls various kinds of display with easy program. This IC is made of 48 pin plastic shrink DIP (Dual In-Line Package) provided with plentiful I/O (Input/Output) ports controlled by effective input/output instructions, serial interface function, 4 bits A/D converter and 6 bits PWM output.

FEATURES

- 4 bits microcomputer for digital tuning system
- built-in PLL frequency synthesizer using prescaler: μPB568
- single power supply (5 V ±10 %)
- CMOS with low power consumption
- program memory (ROM): 8 K byte (16 bits x 3 968 steps)
- data memory (RAM): 4 bits x 336 words
- stack level: 6
- 35 types of understandable instruction
- capable of decimal arithmetic
- instruction execution time: 2 μs (with 8 MHz crystal connected)
- IDC (Image Display controller) built-in (user programable)
  - number of display character : 97 characters (max. in one screen)
  - display location : 12 lines x 16 columns
  - number of character types : 120 types
  - character format : 10 x 15 dots (capable of fringe function)
  - character color : 8 colors
  - character size : 4 types of setting is available independently both for line and column (14, 28, 42, 56H)
- built-in 8 bits serial interface (1 system 2 channel: 3 wire and 2 wire system)
- built-in D/A converter: 6 bits x 4 (PWM output)
- built-in A/D converter: 4 bits x 6
- built-in H. Sync. signal counter
- built-in commercial power supply frequency counter
- built-in power-up detection circuit and power-on-reset circuit
- interrupt input for remote control signal (with noise canceller)
- plentiful I/O ports
  - input output port : 15
  - input port : 4
  - output port : 8

ORDERING INFORMATION

Order Code	Package
μPD17002CU-XXX	48-pin plastic shrink DIP (600 mil)

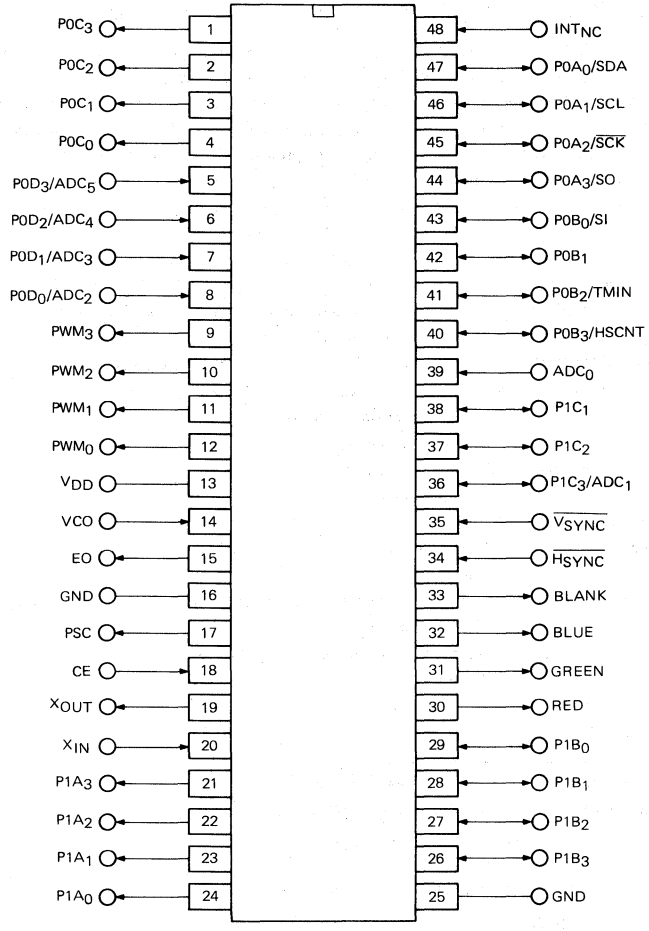
Notes on Serial interface: The 2-wire mode corresponds to the I2C-Bus specification from Philips. In case of using this interface mode note the following:

Duties when using I2C bus system

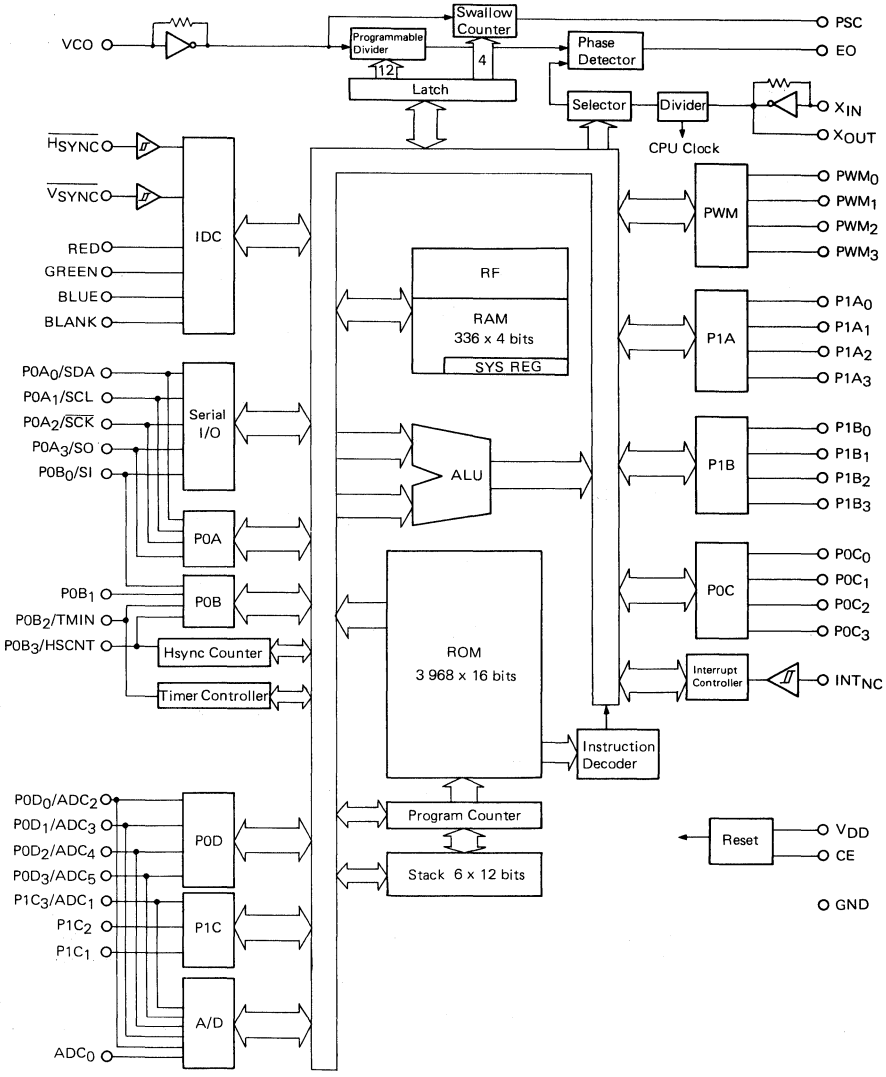
Purchase of NEC's I2C bus system hardware components conveys a license under the Philips I2C patents rights to use this components in an I2C system, provided that the system conforms the I2C standard specifications as defined by Philips.

Consequently for all ROM based components with I2C hardware circuits the user is kindly requested to notify the use of the I2C bus interface at the ROM code verification stage.

PIN CONNECTION (Top View)



BLOCK DIAGRAM



PIN DESCRIPTION

PIN No.	SYMBOL	PIN NAME	FUNCTION	OUTPUT TYPE
1 to 4	$P0C_3$ to $P0C_0$	PORT 0C	4 bit output port. Latch for Port 0C is located at 72H address of BANK 0 or BANK 2 of data memory (RAM). Output status is unconstant at the initial power-on (V_{DD}).	CMOS push-pull
5 6 7 8	$P0D_3/ADC_5$ $P0D_2/ADC_4$ $P0D_1/ADC_3$ $P0D_0/ADC_2$	Port 0D	4 bit input port. These ports can be used also as A/D converter. When used as port, pull-down resistor (100 kΩ TYP.) is connected. The built-in 4-bit A/D converters employ the successive approximation method. The A/D converter reference voltage is V_{DD}. Latch for Port 0D is located at 73H address of BANK 0 or BANK 2 of data memory (RAM).	Input with pull-down resister
9 to 12	PWM_3 to PWM_0	D/A converter	VDP (Variable Duty Port) or output port. VDP function is to output the pulse of 15.625 kHz frequency sequently. The pulse duty is variable by 66-step program.	N-ch open-drain
13	V_{DD}	Power Supply	Device power supply pin. This pin supplies 5 V ±10 % while the device is operating with full functions. When only CPU operates (PLL and IDC stop), 4.0 to 5.5 V is supplied. This voltage can be dropped to 2.5 V to hold the internal data memory (RAM) with a STOP instruction. When the voltage applied to this pin changes from 0 to 4.0 V, the device is reset and the program starts from address 0 because the μPD17002 has a power-on reset circuit. To operate power-on reset circuit normally, the rising time (0→4.0 V) should be within 500 ms.	–
14	VCO	Local Oscillator Signal Input	Input the output of VCO (Voltage Controlled Oscillator) after frequency division by the μPB568 prescaler, that is the output of the prescaler. μPB568 is a Two-Modulus prescaler with division ratio (1 GHz MAX.).	Input (self-bias)

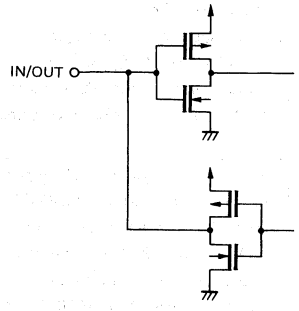
PIN No.	SYMBOL	PIN NAME	FUNCTION	OUTPUT TYPE
15	EO	Error Output	PLL error output pin. If the frequency obtained by dividing the oscillation output of VCO is higher than the reference frequency, high level is output from this pin. Otherwise, low level is output. A floating condition results if the two frequencies are identical. The output is supplied through the LPF (Low Pass Filter) to the varacter diodes that form the VCO (Voltage Controlled Oscillator) as a tuning voltage.	CMOS 3-state
16 25	GND	Ground	Device ground pin. Both pins should be connected to the ground.	–
17	PSC	Pulse Swallowing Control Output	Pin used to output a frequency division ratio switching signal to the μPD568. Connected directly to the PSC pin of the μPB568. The ratios are 1/128 and 1/136 (or 1/64 and 1/68).	CMOS push-pull
18	CE	Chip Enable	Device selection signal input pin. This pin must be high level to enable the device and low level to disable the device. When a STOP instruction in the program is executed while the CE pin is low level, the internal clock generator and CPU stop, and the memory can enter the hold state requiring low power consumption. STOP instruction is effective only when CE pin is low level, and when high level, works as same as NOP instruction. When CE pin goes to the high level from the low level, the device is reset and the program starts from 0 address. When the device is reset, BANK turns 0 and I/O port enters the input mode.	Input
19 20	X_{OUT} X_{IN}	X'tal	Crystal oscillator connector pin. Connect a 8 MHz crystal resonator to this pin.	CMOS push-pull (X_{OUT}) Input (X_{IN})
21 to 24	$P1A_3$ to $P1A_0$	Port 1A	4-bit output port. Latch for this port is located at 70H address of e BANK 1 in the data memory (RAM). This pin is N-channel open drain type. (Breakdown Voltage: 12.5 V) (Sink Current: 20 mA TYP.)	N-ch open-drain

PIN No.	SYMBOL	PIN NAME	FUNCTION	OUTPUT TYPE
26 to 29	$P1B_3$ to $P1B_0$	Port 1B	4-bit input output port. The input or output state of each bit can be specified in these ports. The input and output are set by the P1BBIO word (35H) in the resistor file. Latch for these ports are located at 71H address of BANK 1 in the data memory (RAM).	CMOS push-pull (I/O)
30 31 32	RED GREEN BLUE	Character Signal Output	Character data output pins for R. G. B. Active high output	CMOS push-pull
33	BLANK	Blanking Signal Output	Blanking signal output pin to cut video signal. (Active high output)	CMOS push-pull
34	$\overline{H_{SYNC}}$	H. Sync Signal Input	H. Sync. signal input pin for IDC (Active low input)	Input
35	$\overline{V_{SYNC}}$	V. Sync. Signal Input	V. Sync. signal input pin for IDC (Active low input). This signal can be used for interruption.	Input
36 37 38	$P1C_3/ADC_1$ $P1C_2$ $P1C_1$	Port IC	3-bit input output port or A/D converter pin. The input or output state of each 3-bit can be set in these ports. The input and output are specified by the P1CGIO bit (#0 bit of 27H) in the resistor file. When used as A/D converter, input should be specified. Latch for this port is allocated at 72H address of BANK 1 in the data memory (RAM). Port 1C enters into input at initial power-on (V_{DD}), or at clock stop time or at reset time. (CE pin: Low→High)	CMOS push-pull (I/O)
39	ADC_0	AD Conversion	The A/D converter input pin. The built-in 4-bit A/D converters employ the successive approximation method. The A/D converter reference voltage is V_{DD}.	Input
40 41 42 43	$P0B_3$/HSCNT $P0B_2$/TMIN $P0B_1$ $P0B_0$/SI	Port 0B	4-bit input output ports. The input or output state of each bit can be specified in these ports. The input and output are set by the P0BBIO word (36H) in the resistor file. Latch for these ports are located at 71H address of BANK 0 or BANK 2 in the data memory (RAM). $P0B_2$/TMIN can be used also as an external timer input. Interruption starts by the 1/5 or 1/6 of the frequency input to this pin.	CMOS push-pull (I/O) However $P0B_3$/HSCNT is self biased at input.

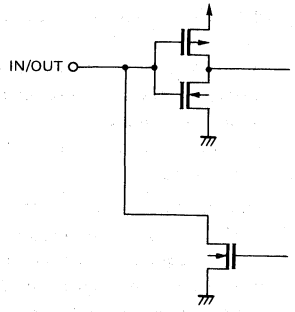
PIN No.	SYMBOL	PIN NAME	FUNCTION	OUTPUT TYPE
40 41 42 43	$P0B_3$/HSCNT $P0B_2$/TMIN $P0B_1$ $P0B_0$/SI	Port 0B	Usually commercial power supply frequency is input to this pin, and used as reference clock for timer. $P0B_0$/SI pin can be used also as a serial interface (μCOM standard mode) data input pin. $P0B_3$/HSCNT pin can be used also as a H. sync. signal counter input pin. Therefore this pin is self biased ($V_{DD}/2$) at any time. Port 0B turns input at the initial power-on (V_{DD}) or at clock stop time or at reset time (CE pin: Low→High).	CMOS push-pull (I/O) However $P0B_3$/HSCNT is self biased at input.
44 45 46 47	$P0A_3$/SO $P0A_2/\overline{SCK}$ $P0A_1$/SCL $P0A_0$/SDA	Port 0A	4-bit input output port. The input or output state of each bit can be specified in these ports. The input and output are set by the P0ABIO word (37H) in the resistor file. Latch for these ports are located at 70H address of BANK 0 or BANK 2 in the data-memory (RAM). $P0A_3$/SO pin can be used also as a serial interface (μCOM standard mode) data output pin. $P0A_2/\overline{SCK}$ pin can be used also as a shift clock input output pin. $P0A_0$/SDA pin can be used as a serial interface (two wire mode and μCOM standard mode) data input output pin. $P0A_1$/SCL pin can be used as a shift clock input output pin.	$P0A_3$/SO $P0A_2/\overline{SCK}$ CMOS push-pull (I/O) P0A1/SCL $P0A_0$/SDA N-ch open-drain (I/O)
48	INT_{NC}	Interrupt Request Signal Input	Interrupt request signal input pin with noise canceller. This pin makes programming easy for a noisy signal such as a remote control signal. Program decides if interruption starts at rising time or at falling time of input signal into this pin. IEDG1 flag reset enters into interruption at rising time. IEDG1 flag set enters into interruption at falling time. At reset time (CE pin: Low→High), IEDG1 flag is reset and interruption starts at the rising edge.	Input

INPUT/OUTPUT CIRCUITS

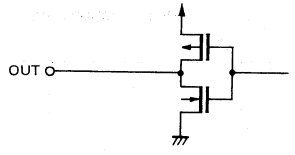
P0A ($P0A_3$/SO, $P0A_2$/$\overline{SCK}$)
P0B ($P0B_1$, $P0B_0$/SI)
P1B ($P1B_3$, $P1B_2$, $P1B_1$, $P1B_0$)
P1C ($P1C_3$/ADC_1, $P1C_2$, $P1C_1$)



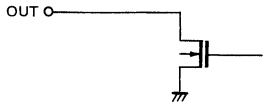
P0A ($P0A_1$/SCL, $P0A_0$/SDA)



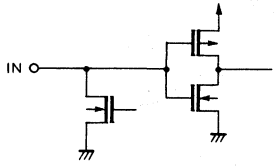
P0C ($P0C_3$, $P0C_2$, $P0C_1$, $P0C_0$)
RED, GREEN, BLUE, BLANK, PSC



PWM (PWM_3, PWM_2, PWM_1, PWM_0)
P1A ($P1A_3$, $P1A_2$, $P1A_1$, $P1A_0$)

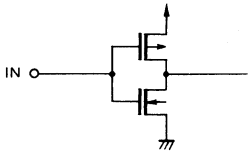


P0D ($P0D_3/ADC_5$, $P0D_2/ADC_4$, $P0D_1/ADC_3$, $P0D_0/ADC_2$)

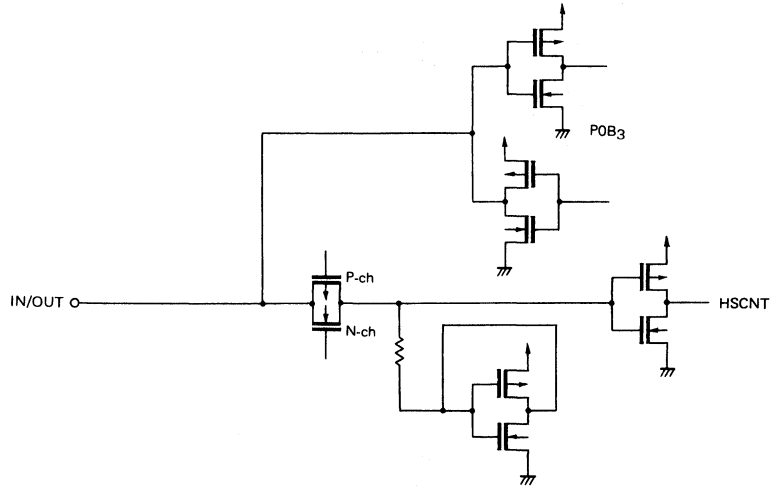


(High ON Register)

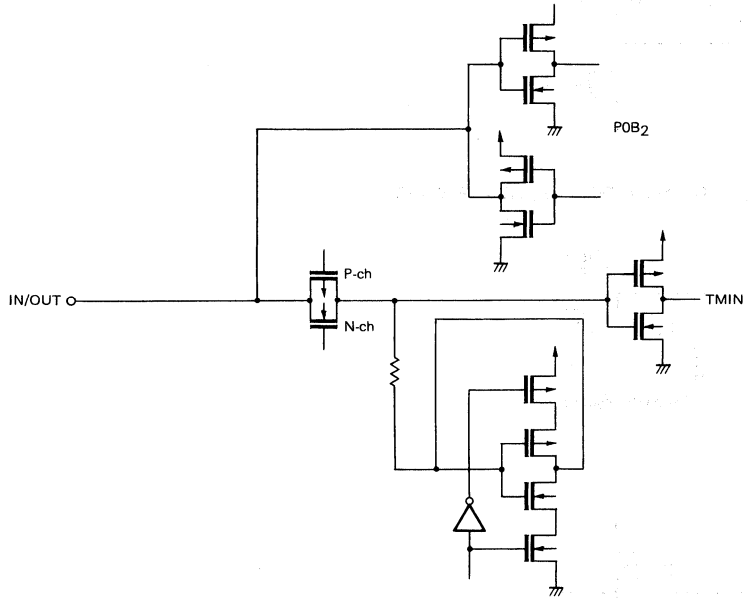
AD_0



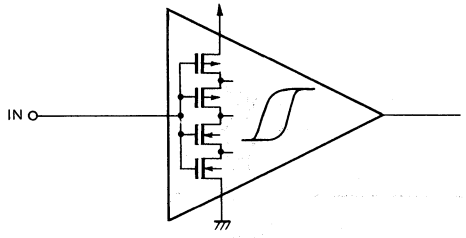
$P0B_3$/HSCNT



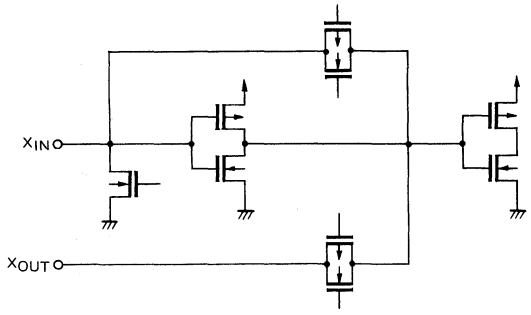
POB_2/TMIN



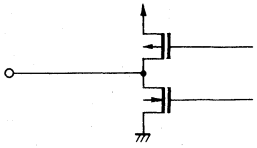
$\overline{H_{SYNC}}$, $\overline{V_{SYNC}}$, INT_{NC}, CE



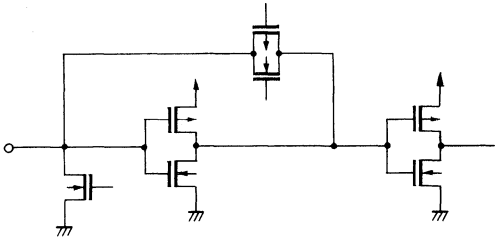
X_{OUT}, X_{IN}



EO



VCO



ELECTRICAL CHARACTERISTICS (TARGET SPEC)

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	−0.3 to +6.0	V
Input Voltage	V_I	−0.3 to V_{DD}	V
Output Voltage	V_O	−0.3 to V_{DD}	V
Output Sink Current	I_O	10 (except P1A)	mA
Output Breakdown Voltage	V_{BDS}	13 (P1A, PWM)	V
Operating Temperature	T_a	−20 to +70	°C
Storage Temperature	V_{stg}	−55 to +125	°C

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Supply Voltage	V_{DD1}	4.5	5.0	5.5	V	All functions operate (CPU, PLL, IDC)
Supply Voltage	V_{DD2}	4.0	5.0	5.5	V	Only CPU operates
Data Retention Voltage	V_{DR}	3.0		5.5	V	Crystal oscillation stopped
Output Breakdown Voltage	V_{BDS}			12.5	V	P1A, PWM
Supply Voltage Rising Time	t_{rise}			500	ms	V_{DD}: 0 → 4.0 V

DC CHARACTERISTICS (T_a = −20 to +70 °C, V_{DD} = 4.5 to 5.5 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Supply Current	I_{DD1}		8		mA	(T_a=25 °C)
Supply Current	I_{DD2}		1		mA	Only CPU operates (T_a=25 °C)
High Level Input Voltage	V_{IH1}	0.7 V_{DD}			V	P0A, P0B, P0D, P1B, P1C
High Level Input Voltage	V_{IH2}	0.8 V_{DD}			V	CE, INT_{NC}, $\overline{V_{SYNC}}$, $\overline{H_{SYNC}}$
Low Level Input Voltage	V_{IL1}			0.3 V_{DD}	V	P0A, P0B, P0D, P1B, P1C
Low Level Input Voltage	V_{IL2}			0.2 V_{DD}	V	CE, INT_{NC}, $\overline{V_{SYNC}}$, $\overline{H_{SYNC}}$
High Level Output Current	I_{OH}		−2	−1	mA	$P0A_2$, $P0A_3$, P0B, P0C, P1B, P1C, RED, GREEN, BLUE, BLANK $V_{OH}=V_{DD}-1$ V
Low Level Output Current	I_{OL1}	1	2		mA	P0A, P0B, P0C, P1B, P1C, RED, GREEN, BLUE, BLANK, PWM V_{OL}=1 V
Low Level Output Current	I_{OL2}	15	20		mA	P1A, V_{OL}=1 V
High Level Input Current	I_{IH}	100			μA	VCO, X_{IN}, $V_I=V_{DD}$=4.5 V
Data Retention Current	I_{DR}			10	μA	Crystal oscillation stopped (T_a=25 °C)
Output Leakage Current	I_L			1	μA	$P0A_0$, $P0A_1$, P1A, PWM, EO, V_{IH}=5 V

AC CHARACTERISTICS (T_a = −20 to +70 °C, V_{DD} = 4.5 to 5.5 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Input Frequency	f_{TMR}	50		60	Hz	POB_2/TMIN
Input Frequency	f_{HS}	10		20	kHz	POB_3/HSCNT
IDC Jitter	IDC_G		4	6	ns	
IDC H. SYNC Start Position	IDC_{HP}		16.25		μs	from last edge of H. SYNC
IDC I. SYNC Start Position	IDC_{VP}		17		H	from last edge of V. SYNC
Operating Frequency	f_{in}			15	MHz	VCO (V_I=0.6 V_{P-P}, SIN WAVE)

A/D CONVERTER CHARACTERISTICS (T_a = −20 to +70 °C, V_{DD} = 4.5 to 5.5 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
A/D Conversion Absolute Accuracy		±1/2		±1	LSB	T_a=−10 to +50 °C
Input Impedance		1			MΩ	

μPD17002 INSTRUCTION SET

Instruction Table

b_{14}	b_{13}	b_{12}	b_{11}	b_{15}	0		1	
0	0	0	0	0	ADD	r, m	ADD	m, #i
0	0	0	1	1	SUB	r, m	SUB	m, #i
0	0	1	0	2	ADDC	r, m	ADDC	m, #i
0	0	1	1	3	SUBC	r, m	SUBC	m, #i
0	1	0	0	4	AND	r, m	AND	m, #i
0	1	0	1	5	XOR	r, m	XOR	m, #i
0	1	1	0	6	OR	r, m	OR	m, #i
0	1	1	1	7	INC INC MOVT BR CALL RET RETSK EI DI RETI PUSH POP GET PUT PEEK POKE RORC STOP HALT NOP	AR IX DBF, @AR @AR @AR AR AR DBF, p p, DBF WR, rf rf, WR r 0 h		
1	0	0	0	8	LD	r, m	ST	m, r
1	0	0	1	9	SKE	m, #i	SKGE	m, #i
1	0	1	0	A	MOV	@r, m	MOV	m, @r
1	0	1	1	B	SKNE	m, #i	SKLT	m, #i
1	1	0	0	C	BR	addr (page 0)	CALL	addr (page 0)
1	1	0	1	D	BR	addr (page 1)	MOV	m, #i
1	1	1	0	E			SKT	m, #n
1	1	1	1	F			SKF	m, #n

Instructions

NOTE

M : One of Data memory specified by [(BANK), m]
m : Data memory address specified by [m_H, m_L] of each bank
m_H : Data memory address high (Row address); 3 bits
m_L : Data memory address low (Column address); 4 bits
R : One of General register specified by [(RP), r]
r : General register address low; 4 bits
RP : General register pointer
RF : One of register file specified by rf
rf : Register file address specified by [rf_H, rf_L]
rf_H : Register file address high
rf_L : Register file address low
AR : Address register
IX : Index register
IXE : Index enable flag
DBF : Data buffer
WR : Window register
MP : Memory pointer
MPE : Memory pointer enable flag
PE : Peripheral
P : Peripheral address
P_H : Peripheral address high
P_L : Peripheral address low
PC : Program memory counter
SP : Stack pointer
STACK : Stack of (PC), (BANK), (IXE)
$STACK_{pc}$: Stack of (PC)
BANK : Bank register
$(ROM)_{pc}$: One of Program memory data specified by (PC)
INTEF : Interrupt enable flag
SGR : Program memory segment register
i : Immediate data; 4 bits
n : Bit position; 4 bits
addr : One of program memory address; 11 bits
CY : Carry flag
c : Carry
b : Borrow
h : Halt release conditions
[ ] : Address of M, R, RF
( ) : Contents of M, R, RF, AR, IX, DBF, WR, PE

	Mnemonic	Operand	Function	Operation	Machine code			
					Op. code			
Addition	ADD	r, m	Add Data memory to General register	(R), (CY) ← (R) + (M)	00000	m_H	m_L	r
		m, #i	Add immediate data to Data memory	(M), (CY) ← (M) + i	10000	m_H	m_L	i
	ADDC	r, m	Add Data memory to General register with carry	(R), (CY) ← (R) + (M) + (CY)	00010	m_H	m_L	r
		m, #i	Add immediate data to Data memory with carry	(M), (CY) ← (M) + i + (CY)	10010	m_H	m_L	i
	INC	AR	Increment Address register	(AR) ← (AR) + 1	00111	000	1001	0000
		IX	Increment Index register	(IX) ← (IX) + 1	00111	000	1000	0000
Subtraction	SUB	r, m	Subtract Data memory from General register	(R), (CY) ← (R) − (M)	00001	m_H	m_L	r
		m, #i	Subtract immediate data from Data memory	(M), (CY) ← (M) − i	10001	m_H	m_L	i
	SUBC	r, m	Subtract Data memory from General register with borrow	(R), (CY) ← (R) − (M) − (CY)	10011	m_H	m_L	r
		m, #i	Subtract immediate data from Data memory	(M), (CY) ← (M) − i − (CY)	10011	m_H	m_L	i
Comparison	SKE	m, #i	Skip if Data memory equals immediate data	(M) − i & skip if zero	01001	m_H	m_L	i
	SKGE	m, #i	Skip if Data memory is greater than or equal to immediate data	(M) − i & skip if not borrow	11001	m_H	m_L	i
	SKLT	m, #i	Skip if Data memory is less than immediate data	(M) − i & skip if borrow	11011	m_H	m_L	i
	SKNE	m, #i	Skip if Data memory not equal immediate data	(M) − i & skip if not zero	01011	m_H	m_L	i

	Mnemonic	Operand	Function	Operation	Machine code			
					Op. code			
Logical operation	AND	m, #i	Logic AND of Data memory and immediate data	(M) ← (M) AND i	10100	m_H	m_L	i
		r, m	Logic AND of General register and Data memory	(R) ← (R) AND (M)	00100	m_H	m_L	r
	OR	m, #i	Logic OR of Data memory and immediate data	(M) ← (M) OR i	10110	m_H	m_L	i
		r, m	Logic OR of General register and Data memory	(R) ← (R) OR (M)	00110	m_H	m_L	r
	XOR	m, #i	Exclusive Logic OR of Data memory and immediate data	(M) ← (M) XOR i	10101	m_H	m_L	i
		r, m	Exclusive Logic OR of General register and Data memory	(R) ← (R) XOR (M)	00101	m_H	m_L	r
Transfer	LD	r, m	Load Data memory to General register	(R) ← (M)	01000	m_H	m_L	r
	ST	m, r	Store General register to Data memory	(M) ← (R)	11000	m_H	m_L	r
	MOV	@r, m	Move Data memory to Destination data memory referring to General register	if MPE=1 : [(MP), (R)] ← (M) if MPE=0 : [(m_H), (R)] ← (M)	01010	m_H	m_L	r
		m, @r	Move Source data memory referring to General register to Data memory	if MPE=1 : (M) ← [(MP), (R)] if MPE=0 : (M) ← [(m_H), (R)]	11010	m_H	m_L	r
		m, #i	Move immediate data to Data memory	(M) ← i	11101	m_H	m_L	i
	MOVT	DBF, @AR	Move Program memory data specified by Address register to Data buffer	($STACK_{pc}$) ← (PC) & (PC) ← (AR) & (DBF) ← $(ROM)_{pc}$ & (PC) ← ($STACK_{pc}$)	00111	000	0001	0000
	PUSH	AR	Decrement Stack pointer, then move Address register to Stack	(SP) ← (SP) − 1 & ($STACK_{pc}$) ← (AR)	00111	000	1101	0000
	POP	AR	Move Stack to Address register, then increment Stack pointer	(AR) ← ($STACK_{pc}$) & (SP) ← (SP) + 1	00111	000	1100	0000
	PEEK	WR, rf	Get data of Register file to Window register	(WR) ← (RF)	00111	rf_H	0011	rf_L
	PCKE	rf, WR	Put data of Window register into Register file	(RF) ← (WR)	00111	rf_H	0010	rf_L
	GET	DBF, p	Get peripheral data to Data buffer	(DBF) ← (PE)	00111	p_H	1011	p_L
	PUT	p, DBF	Put data of Data buffer to peripheral	(PE) ← (DBF)	00111	p_H	1010	p_L
Bit test	SKT	m, #n	Test Data memory bits, then skip if all bits specified are true	if $(M)_n$ = all "1", then skip	11110	m_H	m_L	n
	SKF	m, #n	Test Data memory bits, then skip if all bits specified are false	if $(M)_n$ = all "0", then skip	11111	m_H	m_L	n

	Mnemonic	Operand	Function	Operation	Machine code			
					Op. code			
Jump	BR	addr	Jump to the address in page 0	(PC) ← addr & (PC)*11 ← 0	01100	addr (11 bits)		
			Jump to the address in page 1	(PC) ← addr & (PC)*11 ← 1	01101			
		@AR	Jump to the address specified by Address register	(PC) ← (AR)	00111	000	0100	0000
Shift	RORC	r	Rotate General register right with carry	C ← (R)#3 → (R)#2 → (R)#1 → (R)#0 → C	00111	000	0111	r
Subroutine	CALL	addr	Call subroutine in page 0	(SP) ← (SP) − 1 & (STACK$_{pc}$) ← ((PC) + 1) & (PC)#11 ← 0 & (PC) ← addr	11100	addr (11 bits)		
		@AR	Call subroutine	(SP) ← (SP) − 1 & (STACK$_{pc}$) ← ((PC) + 1) & (PC) ← (AR)	00111	000	0101	0000
	RET		Return to main routine from subroutine	(PC) ← (STACK$_{pc}$) & (SP) ← (SP) + 1	00111	000	1110	0000
	RETSK		Return to main routine from subroutine, then skip unconditionally	(PC) ← (STACK$_{pc}$) & (SP) ← (SP) + 1 & skip	00111	001	1110	0000
	RETI		Return to main routine from interrupt service routine	(PC), (BANK), (IXE) ← (STACK) & (SP) ← (SP) + 1	00111	100	1110	0000
Interrupt	EI		Enable interrupt	INTEF ← 1	00111	000	1111	0000
	DI		Disable interrupt	INTEF ← 0	00111	001	1111	0000
Others	STOP	0	Stop clock if CE = low	stop clock if CE = low	00111	010	1111	0000
	HALT	h	Halt the CPU, Restart by condition h	halt	00111	011	1111	h
	NOP		No operation		00111	100	1111	0000

BUILT-IN IMAGE DISPLAY CONTROLLER

The μPD17P008 is a 4 bits CMOS microcontroller incorporating One Time PROM, 2K bits EEPROM, Image Display Controller (IDC) and PLL frequency synthesizer into one chip for digital tuning of PLL frequency synthesizer system of TV.

Image Display Controller has various display function showing not only letters but also drawings.

Fonts of IDC are selected by user's program and effective debugging can be realized by actual indications from the beginning of software development.

In addition, Hsync. counter for station detection and serial interface for communication with other peripheral devices are incorporated, also 4 bits A/D converter 8 bits D/A converter (PWM output) and 6 bits D/A converter (PWM output) are incorporated.

CPU applies μPD17000 architecture which operates data memory directly without accumulater, and it realizes effective programming.

All instructions consist of 16 bits one word.

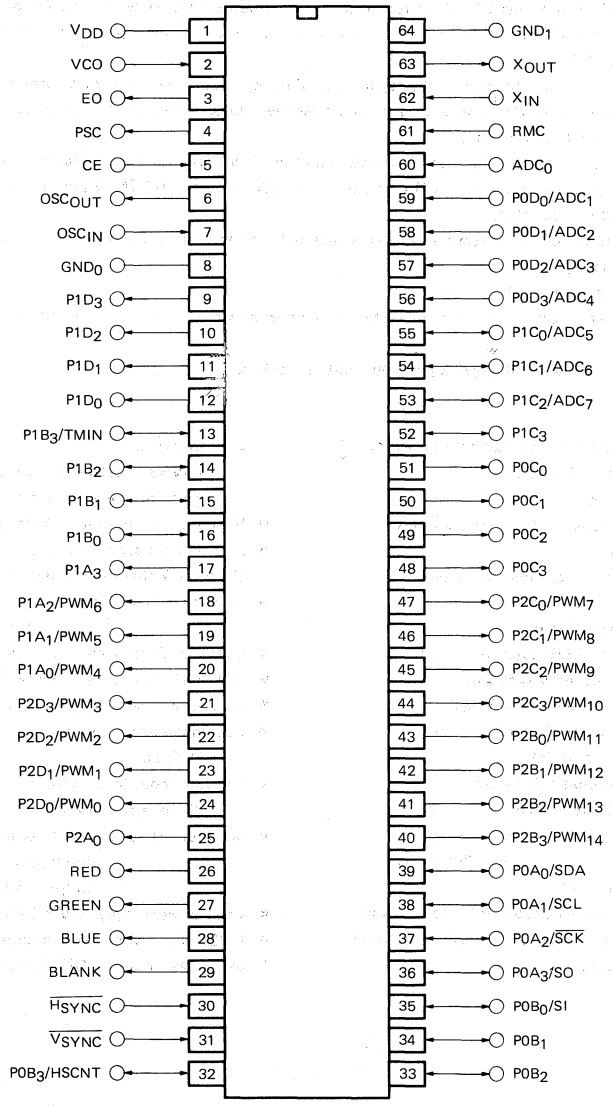
One Time PROM makes it perfect for system evaluation or small lot production of the mask ROM products μPD17008.

Package type is 64-pin plastic shrink DIP (Dual In-Line Package).

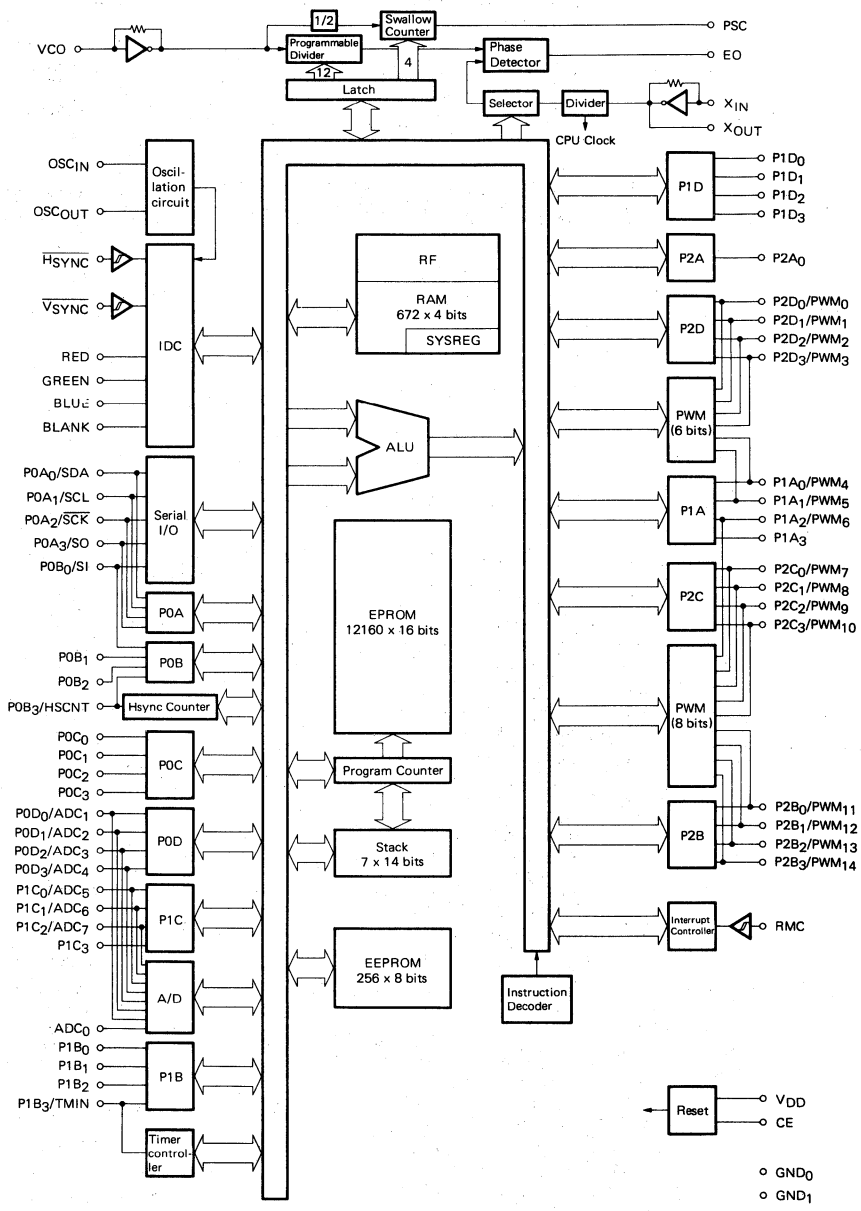
FEATURES

- 4 bits microcontroller for digital tuning system
- program memory (ROM):
  32K byte (16,256 steps x 16 bits)
- data memory (RAM): 672 words x 4 bits
- stack level: 7
- 36 types of understandable instruction
- capable of decimal arithmetic
- instruction execution time:
  2 μs (with 8 MHz crystal connected)
- built-in PLL frequency synthesizer
  using 1 GHz prescaler: μPB568
- IDC (Image Display Controller) built-in
  (user programmable)
  - number of display character:
    200 characters (max. in one screen)
  - display location: 14 lines x 19 columns
  - number of character types: 248 types
  - character format:
    10 x 15 dots (capable of fringe function)
    2-dot space between characters can be set.
  - character color: 8 colors
  - character size:
    4 types of setting is available independently
    both for line and column (14, 28, 42, 56H)
- built-in circuit to prevent 1-dot vertical flicker.
- built-in 8 bits serial interface:
  (1 system 2 channels: 3 wire and 2 wire systems)
- built-in D/A converter: 6 bits x 6 ch (PWM output)
  : 8 bits x 9 ch (PWM output)
- built-in A/D converter: 4 bits x 8 ch
- built-in H. Sync. signal counter
- built-in commercial power supply freq. counter
- built-in power-up detection circuit and power-on reset circuit.
- interrupt input for remote control signal
  (with noise canceller)
- plentiful I/O ports: input output port: 16
  input port : 4
  output port : 25
- single power supply (5 V ± 10 %)
- CMOS with low power consumption
- 64-pin plastic shrink DIP (600 mil)

PIN CONFIGURATION (Top View)



BLOCK DIAGRAM



SINGLE-CHIP MICROCONTROLLER FOR VOLTAGE SYNTHESIZER WITH ON-CHIP IMAGE DISPLAY CONTROLLER

The μPD17051 is a 4-bit CMOS microcontroller for digital tuning systems with an on-chip image display controller (IDC) allowing various kinds of display and 14-bit D/A converter for voltage synthesizer use.

The CPU features include 4-bit parallel addition, logical operations, multiple bit testing, carry flag setting/resetting, powerful interrupt functions and timer functions.

The on-chip user-programmable image display controller for on-screen enables easy program control of various kinds of display.

The μPD17051 comes in 48-pin plastic shrink DIP form, and has a wide range of I/O port and serial interface functions controlled by powerful input/output instructions, plus a 4-bit A/D converter and 6-bit PWM output.

FEATURES

- 4-bit microcontroller for digital tuning systems
- On-chip 14-bit D/A converter for voltage synthesizer
- Programmable memory (ROM) : 16K bytes (8192 steps × 16 bits)
- Data memory (RAM) : 448 words × 4 bits
- Stack levels : 6
- 35 easy-to-understand instruction sets
- Decimal operation capability
- Instruction execution time : 2 μs (with 8 MHz oscillator connected)
- On-chip IDC (user-programmable)
  - Display capacity : Max. 97 characters per screen
  - Display positions : 14 rows × 19 columns
  - Character set : 128 characters (64 simultaneously usable per screen)
  - Character format : 10 × 15 dots (bordering capability)
  - Colors : 8
  - Character size : 4 independent vertical/horizontal settings (15, 30, 45, 60 H) (2.5, 5.0, 7.5 10 μs)
- On-chip 8-bit serial interface (1 system: 3-wire or 2-wire)
- On-chip D/A converter : 6 bits × 3 (PWM output)
- On-chip A/D converter : 4 bits × 8
- On-chip horizontal synchronization signal counter
- On-chip commercial power supply frequency counter
- On-chip power outage detection circuit and power-on reset circuit
- Remote control signal interrupt input (with noise canceler)
- Many I/O ports
  - Input/output ports : 16
  - Input ports : 5
  - Output ports : 10
- 5 V ±10 %
- Low power consumption CMOS

ORDERING INFORMATION

Order Code	Package
μPD17051CU-xxx	48-Pin Plastic Shrink DIP (600 mil)

Notes on Serial interface: The 2-wire mode corresponds to the I2C-Bus specification from Philips. In case of using this interface mode note the following:

Duties when using I2C bus system

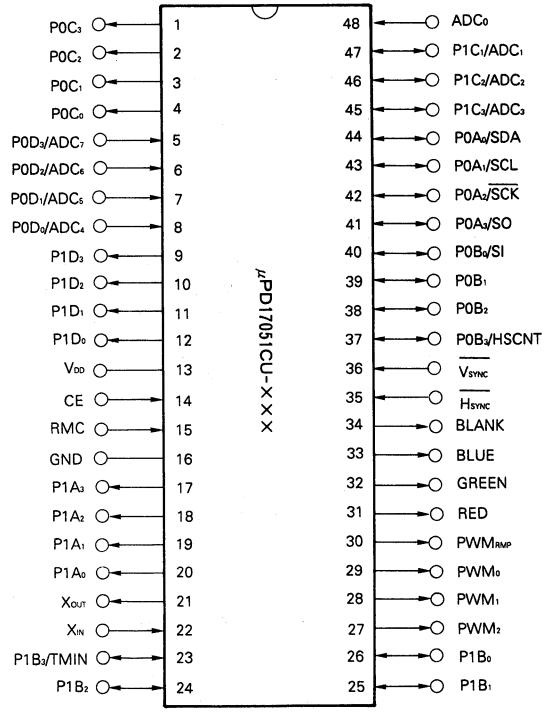
Purchase of NEC's I2C bus system hardware components conveys a license under the Philips I2C patents rights to use this components in an I2C system, provided that the system conforms the I2C standard specifications as defined by Philips.

Consequently for all ROM based components with I2C hardware circuits the user is kindly requested to notify the use of the I2C bus interface at the ROM code verification stage.

FUNCTIONAL OUTLINE

Item	Function
Program memory	• 16K bytes (8192 steps × 16 bits) Table reference area : 256 steps CROM dual-function area : 2048 steps
Data memory	• 448 words (448 words × 4 bits) Data buffer : 4 words General-purpose registers : 16 words VRAM dual-function area : 224 words
System registers	• 12 words
Register file	• 24 words (control registers)
Port registers	• 8 words
Instruction execution time	• 2 μs (using 8 MHz ceramic oscillator)
Stack levels	• 6 levels (stack manipulation capability)
General-purpose ports	• Input/output ports : 16 • Input ports : 5 • Output ports : 10
IDC (Image Display Controller)	• Display capacity : 97 characters per screen • Display positions : 14 rows × 19 columns • Character set : 128 characters (user-programmable) (64 different characters simultaneously displayable per screen) • Character format : 10 × 15 dots • Colors : 8 • Character size : 4 vertical (15, 30, 45, 60 H) 4 horizontal (2.5, 5.0, 7.5 10 μs) Independent vertical/horizontal setting capability
Serial interface	• 1 system (2 channels) 8-bit 3-wire: 1 channel 8-bit 2-wire: 1 channel
D/A converter	• 14-bit × 1 (PWM output, Max. 12.5 V withstand voltage) • 6-bit × 3 (PWM output, Max. 12.5 V withstand voltage)
A/D converter	• 4-bit × 8 (software-driven successive approximation method)
Interrupts	• 4 channels (maskable interrupts) External interrupts: 2 channels (RMC pin, $\overline{V_{SYNC}}$ pin) Internal interrupts: 2 channels (timer, serial interface)
Timer	• 2 systems Internal timer : 5, 20, 100 ms External timer : 1/5, 1/6 frequency input to $P1B_3$/TMIN pin
Reset	• Power-on reset (on powering-on) • Reset by CE pin (CE pin: Low → high) • Power outage detection function
Supply voltage	5 V ± 10 %
Package	48-pin plastic shrink DIP (600 mil)

PIN CONFIGURATION (Top View)



ADC0 to ADC7	:	A/D converter inputs
CE	:	Chip enable
RMC	:	Interrupt signal input
XIN, XOUT	:	Oscillator
TMIN	:	External timer input
PWM0 to PWM2	:	D/A converter outputs
PWMRMP	:	Station selection D/A converter output
RED	:	Character signal output
GREEN	:	Character signal output
BLUE	:	Character signal output
BLANK	:	Blanking signal output
$\overline{\text{HSYNC}}$	:	Horizontal synchronization signal input
$\overline{\text{VSYNC}}$	:	Vertical synchronization signal input
HSCNT	:	Horizontal synchronization signal counter input
SI	:	Data input
SO	:	Data output
$\overline{\text{SCK}}$	:	Shift clock input/output
SCL	:	Shift clock input/output
SDA	:	Data input/output
P0A0 to P0A3	:	Port 0A
P0B0 to P0B3	:	Port 0B
P0C0 to P0C3	:	Port 0C
P0D0 to P0D3	:	Port 0D
P1A0 to P1A3	:	Port 1A
P1B0 to P1B3	:	Port 1B
P1C0 to P1C3	:	Port 1C
P1D0 to P1D3	:	Port 1D
VDD	:	Power supply
GND	:	Ground

1. PIN FUNCTIONS

1.1 SUMMARY OF PIN FUNCTIONS

PIN No.	SIGNAL	PIN NAME	DESCRIPTION	OUTPUT TYPE
1 to 4	$P0C_3$ to $P0C_0$	Port 0C	4-bit output port. Port 0C latch is located in address 72H of data memory (RAM) BANK0 or BANK2. Output status is undefined after power-on reset.	CMOS push-pull
5 6 7 8	$P0D_3/ADC_7$ $P0D_2/ADC_6$ $P0D_1/ADC_5$ $P0D_0/ADC_4$	Port 0D	4-bit input port or A/D converter input pins. When used as a port, a pull-down resistor (100 kΩ TYP.) is attached. Port 0D latch is located in address 73H of data memory (RAM) BANK0 or BANK2.	Input (with pull-down resistor)
9 to 12	$P1D_3$ to $P1D_0$	Port 1D	4-bit output port. Port 1D latch is located in address 73H of data memory (RAM) BANK1 or BANK3. Output status is undefined after power-on reset.	CMOS push-pull
13	V_{DD}	Power supply	Device power supply pin. Supplies 5 V ±10 % voltage when all functions are operated. When IDC is not used, device operations on 4 to 5.5 V. When RAM data is retained (when clock oscillation is stopped) voltage can be reduced to approx. 2.2 V. As the μPD17051 incorporates a power-on reset circuit, a 0 → 4.0 V transition effects a system reset and the program starts at address 0. To ensure proper operation of the power-on reset circuit, the rise time from 0 to 4.0 V should be within 500 ms.	———
14	CE	Chip enable	Device selection signal input pin. Driven high when the device is operated normally, and low when the device is not used. When this pin is low, execution of the STOP instruction stops clock oscillation, allowing low-current-consumption backup. The STOP instruction is only effective when the CE pin is low; when high, this instruction operates identically to an NOP instruction. This pin has a dual function as a reset pin; A low-to high transition of the CE pin resets the device and	Input

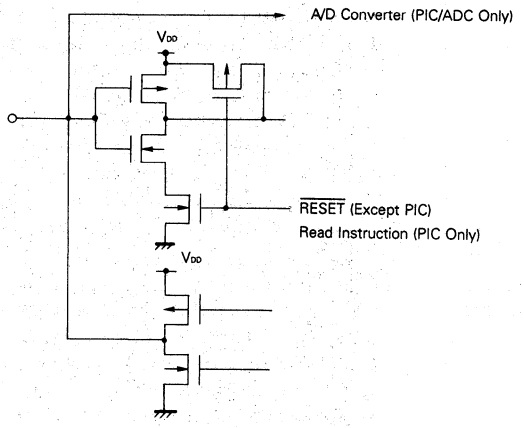
PIN No.	SIGNAL	PIN NAME	DESCRIPTION	OUTPUT TYPE
14	CE	Chip enable	the program starts from address 0. When the device is reset, bank 0 is selected and I/O ports are placed in input mode. Note however that a low-level signal of 188 us or less is not acknowledged.	
15	RMC	Interrupt signal input	Interrupt input pin with noise canceler. Using this pin for noisy signals such as remote control signals facilitates programming. Whether an interrupt is generated on the rise or the fall of the input signal to this pin can be specified by the program. An interrupt is generated on a rise when the IEDG1 flag is reset, and on a fall when this flag is set. In a CE reset the IEDG1 flag is rest, and an interrupt is thus generated on a rise of the signal	Input
16	GND	Ground	Device ground pin.	———
17 to 20	$P1A_3$ to $P1A_0$	Port 1A	4-bit output port. Port 1A latch is located in address 70H of data memory (RAM) BANK1 or BANK3. N-ch open-drain type (medium voltage, high current).	N-ch open-drain
21 22	X_{OUT} X_{IN}	Oscillator	Ceramic oscillator or crystal resonator connection pins. An 8 MHz oscillator/resonator should be used.	CMOS push-pull (X_{OUT}) Input (X_{IN})
23 24 25 26	$P1B_3$/TMIN $P1B_2$ $P1B_1$ $P1B_0$	Port 1B	4-bit input/output port. These port pins can be specified as input/output bit by bit. Input/output setting is performed by the P1BBIO word (35H) in the register file. The latch for this port is located in address 71H of data memory BANK1 or BANK3. $P1B_3$/TMIN can also be used as the external timer input. Interrupts can be generated at 1/5 or 1/6 the frequency input to this pin. Normally the commercial power supply frequency is input to this pin and used as the basic clock for the clock.	CMOS push-pull (I/O)

PIN No.	SIGNAL	PIN NAME	DESCRIPTION	OUTPUT TYPE
27 28 29	PWM_2 PWM_1 PWM_0	D/A converter	VDP (Variable Duty Port) or 1-bit output ports. The VDP function outputs consecutive 15.625 kHz pulses, and the duty of these pulses can be varied by the program in 64 steps.	N-ch open-drain
30	PWM_{RMP}	Station selection D/A converter output	Voltage synthesizer 14-bit D/A converter output or 1-bit output port. The D/A converter outputs pulses combining 9-bit PWM and 5-bit RMP (Rate Multiplier). Therefore, D/A conversion can be performed by external connection of a simple CR filter. Outputs a low-level signal after power-on reset or when clock is stopped.	N-ch open-drain
31 32 33	RED GREEN BLUE	Character signal outputs	Output pins for character data corresponding to R, G, B. Active-high output.	CMOS push-pull
34	BLANK	Blanking signal output	Output pin for blanking signal cutting video signals. Active-high output.	CMOS push-pull
35	$\overline{H_{SYNC}}$	Horizontal synchronization signal input	Input pin for horizontal synchronization signal for IDC. Use active-low input.	Input
36	$\overline{V_{SYNC}}$	Vertical synchronization signal input	Input pin for vertical synchronization signal for IDC. Use active-low input. This pin can be used to effect interrupts.	Input
37 38 39 40	$P0B_3$/ HSCNT $P0B_2$ $P0B_1$ $P0B_0$/SI	Port 0B	4-bit input/output port. These port pins can be specified as input/output bit by bit. Input/output setting is performed by the POBBIO word (36H) in the register file. The latch for this port is located in address 71H of data memory BANK0 or BANK2. The $P0B_0$/SI pin can also be used as the serial interface (serial I/O mode) data input pin. The $P0B_3$/HSCNT pin can also be used as the horizontal synchronization signal counter input pin, in which case self-bias ($V_{DD}/2$) is applied to the HSCNT pin. Port 0B is set to input mode after a power-on reset, when the clock is stopped, or after a CE reset.	CMOS push-pull (I/O) But note that HSCNT is self-bias in input mode.

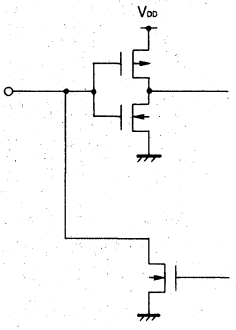
PIN No.	SIGNAL	PIN NAME	DESCRIPTION	OUTPUT TYPE
41 42 43 44	$P0A_3$/SP $P0A_2$/SCK $P0A_1$/SCL $P0A_0$/SDA	Port 0A	4-bit input/output port. These port pins can be specified as input/output bit by bit. Input/output setting is performed by the P0ABIO word (37H) in the register file. The latch for this port is located in address 70H of data memory BANK0 or BANK2. The $P0A_3$/S0 pin can also be used as the serial interface (serial I/O mode) data output pin, and the $P0A_2$/SCK pin can be used as a shift clock input/output pin. The $P0A_0$/SDA pin can be used as a serial interface (2-wire mode and serial I/O mode) data input/output pin, and the $P0A_1$/SCL pin can be used as a shift clock input/output pin.	$P0A_3$/S0 $P0A_2$/SCK CMOS push-pull (I/O) $P0A_1$/SCL $P0A_0$/SDA N-ch open-drain (I/O)
45 46 47	$P1C_3$/ADC_3 $P1C_2$/ADC_2 $P1C_1$/ADC_1	Port 1C	3-bit input/output port or A/D converter input pins. Input/output setting is performed as a 3-bit unit, and is specified by the P1CGI0 bit (bit #0 or 27H) in the register file. When used as A/D converter pins, input must always be specified. The latch for this port is located in address 72H of data memory BANK1 or BANK3. Port 1C is set to input mode after a power-on reset, when the clock stopped, or after a CE reset.	CMOS push-pull (I/O)
48	ADC_0	A/D converter input	A program-driven successive approximation 4-bit A/D converter is incorporated. The A/D converter reference voltage is V_{DD}.	Input

1.2 PIN EQUIVALENCE CIRCUITS

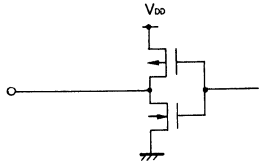
P0A (P0A3/SO, P0A2/$\overline{SCK}$)
P0B (P0B2, P0B1, P0B0/SI)
P1B (P1B2, P1B1, P1B0)
P1C (P1C3/ADC3, P1C2/ADC2, P1C1/ADC1)
} (Input/output)



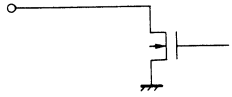
P0A (P0A1/SCL, P0A0/SDA): (Input/output)



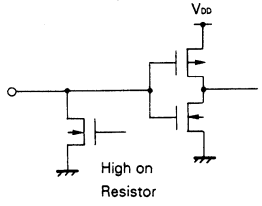
P0C ($P0C_3$, $P0C_2$, $P0C_1$, $P0C_0$)
P1D ($P1D_3$, $P1D_2$, $P1D_1$, $P1D_0$)
RED, GREEN, BLUE, BLANK
} (output)



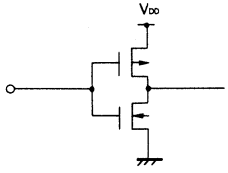
PWM (PWM_2, PWM_1, PWM_0, PWM_{RMP})
P1A ($P1A_3$, $P1A_2$, $P1A_1$, $P1A_0$)
} (output)



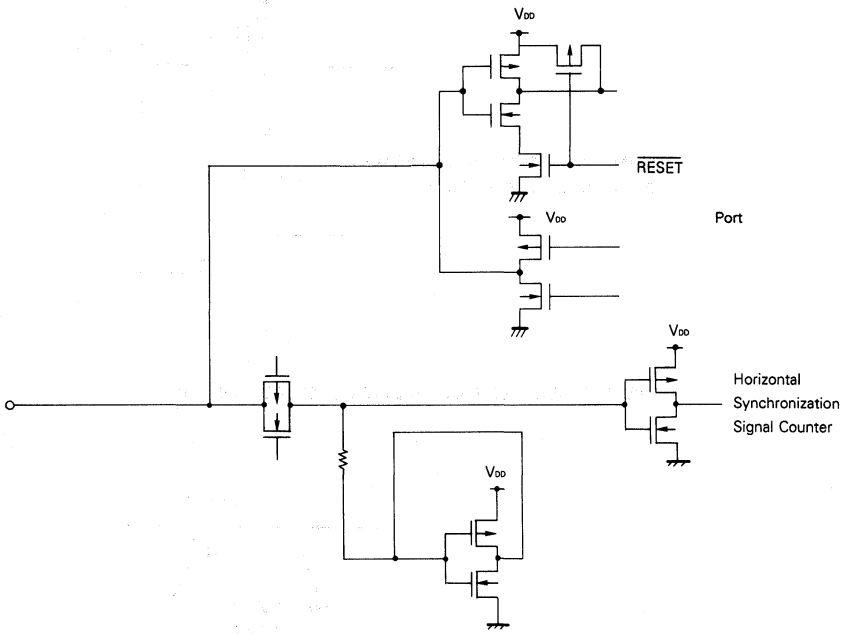
P0D ($P0D_3$/ADC_7, $P0D_2$/ADC_6, $P0D_1$/ADC_5, $P0D_0$/ADC_4): (Input)



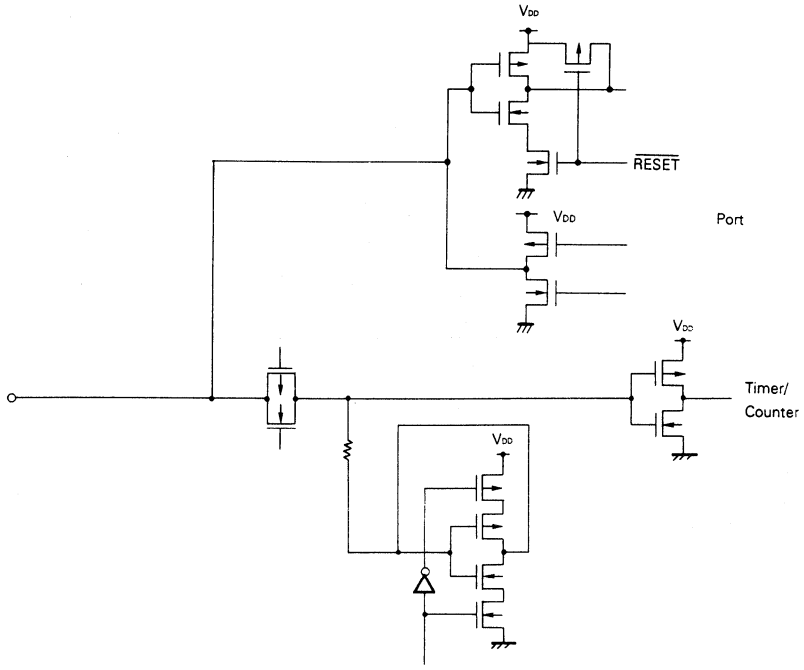
ADC_0: (Input)



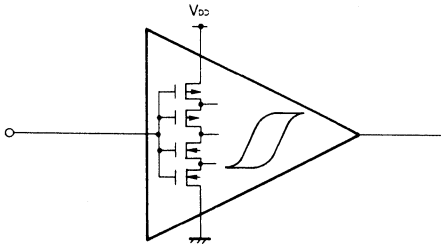
P0B3/HSCNT: (Input/output)



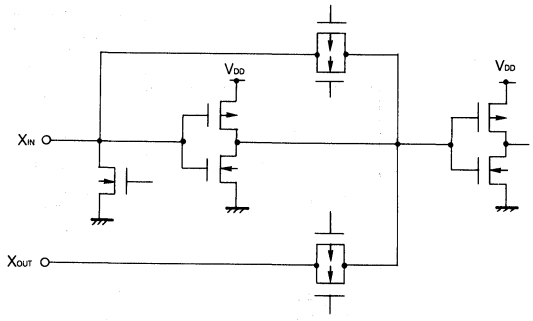
P1B3/TMIN: (Input/output)



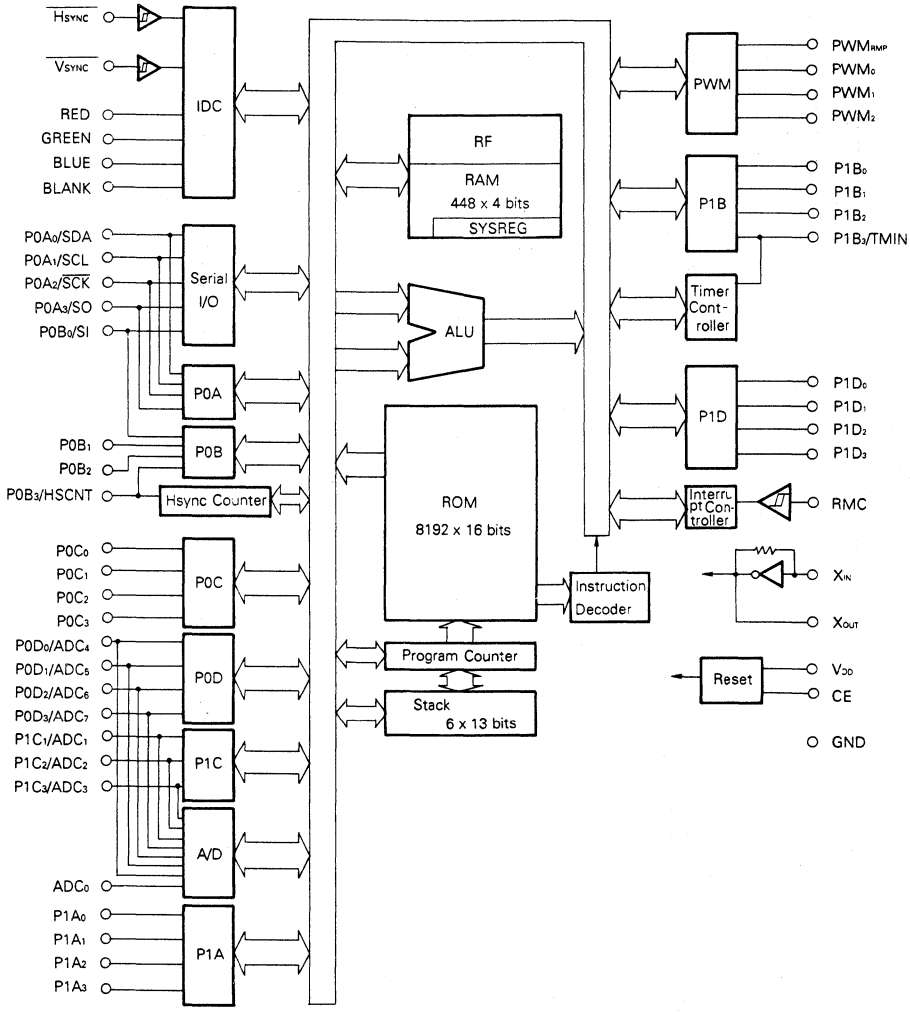
$\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, RMC, CE: (Schmitt triggered inputs)



X_{IN}: (Input)
X_{OUT}: (Output)



2. BLOCK DIAGRAM



22. μPD17051 INSTRUCTIONS

22.1 INSTRUCTION SET LIST

		0		1	
0 0 0 0	0	ADD	r, m	ADD	m, #i
0 0 0 1	1	SUB	r, m	SUB	m, #i
0 0 1 0	2	ADDC	r, m	ADDC	m, #i
0 0 1 1	3	SUBC	r, m	SUBC	m, #i
0 1 0 0	4	AND	r, m	AND	m, #i
0 1 0 1	5	XOR	r, m	XOR	m, #i
0 1 1 0	6	OR	r, m	OR	m, #i
0 1 1 1	7	INC INC MOVT BR CALL RET RETSK EI DI RETI PUSH POP GET PUT PEEK POKE RORC STOP HALT NOP	AR IX DBF, @AR @AR @AR AR AR DBF, p p, DBF WR, rf rf, WR r 0 h		
1 0 0 0	8	LD	r, m	ST	m, r
1 0 0 1	9	SKE	m, #i	SKGE	m, #i
1 0 1 0	A	MOV	@r, m	MOV	m, @r
1 0 1 1	B	SKNE	m, #i	SKLT	m, #i
1 1 0 0	C	BR	addr (page 0)	CALL	addr (page 0)
1 1 0 1	D	BR	addr (page 1)	MOV	m, #i
1 1 1 0	E	BR	addr (page 2)	SKT	m, #n
1 1 1 1	F	BR	addr (page 3)	SKF	m, #n

22.2 INSTRUCTION LIST

Legend

M	:	Data memory indicated by [(BANK), m]
m	:	Data memory address indicated by [m_H, m_L]
m_H	:	Data memory row address (3 bits)
m_L	:	Data memory column address (4 bits)
R	:	General register indicated by [(RP), r]
r	:	General register column address (4 bits)
RP	:	General register pointer
RF	:	Register file indicated by rf
rf	:	Register file address indicated by [rf_H, rf_L]
rf_H	:	Register file address (most significant 3 bits)
rf_L	:	Register file address (least significant 3 bits)
AR	:	Address register
IX	:	Index register
IXE	:	Index enable flag
DBF	:	Data buffer
WR	:	Window register
MP	:	Data memory row address pointer
MPE	:	Memory pointer enable flag
PE	:	Peripheral register
P	:	Peripheral address
P_H	:	Peripheral address (most significant 3 bits)
P_L	:	Peripheral address (least significant 4 bits)
PC	:	Program counter
SP	:	Stack pointer
STACK	:	Stack value indicated by stack pointer
$STACK_{PC}$	:	Program counter value indicated by stack pointer
BANK	:	Bank register
$(ROM)_{PC}$	:	Program memory data indicated by (PC)
INTEF	:	Interrupt enable flag
SGR	:	Program memory segment register
i	:	Immediate data (4 bits)
n	:	Bit position (4 bits)
addr	:	Program memory address (11 bits)
c	:	Carry
b	:	Borrow
h	:	Halt release condition
[ ]	:	Data memory or register address
( )	:	Data memory or register value

Instruction	Mnemonic	Operand	Operation	Machine Code			
				Operation Code			
Add	ADD	r, m	(R)←(R) + (M)	00000	m_H	m_L	r
		m, #i	(M)←(M) + i	10000	m_H	m_L	i
	ADDC	r, m	(R)←(R) + (M) + c	00010	m_H	m_L	r
		m, #i	(M)←(M) + i + c	10010	m_H	m_L	i
	INC	AR	(AR)←(AR) + 1	00111	000	1001	0000
		IX	(IX)←(IX) + 1	00111	000	1000	0000
Suptract	SUB	r, m	(R)←(R) − (M)	00001	m_H	m_L	r
		m, #i	(M)←(M) − i	10001	m_H	m_L	i
	SUBC	r, m	(R)←(R) − (M) − b	00011	m_H	m_L	r
		m, #i	(M)←(M) − i − b	10011	m_H	m_L	i
Compare	SKE	m, #i	(M) − i, skip if zero	01001	m_H	m_L	i
	SKGE	m, #i	(M) − i, skip if not borrow	11001	m_H	m_L	i
	SKLT	m, #i	(M) − i, skip if borrow	11011	m_H	m_L	i
	SKNE	m, #i	(M) − i, skip if not zero	01011	m_H	m_L	i
Logical operation	AND	m, #i	(M)←(M) AND i	10100	m_H	m_L	i
		r, m	(R)←(R) AND (M)	00100	m_H	m_L	r
	OR	m, #i	(M)←(M) OR i	10110	m_H	m_L	i
		r, m	(R)←(R) OR (M)	00110	m_H	m_L	r
	XOR	m, #i	(M)←(M) XOR i	10101	m_H	m_L	i
		r, m	(R)←(R) XOR (M)	00101	m_H	m_L	r
Transfer	LD	r, m	(R)←(M)	01000	m_H	m_L	r
	ST	m, r	(M)←(R)	11000	m_H	m_L	r
	MOV	@r, m	if MPE=1 : [(MP), (R)]←(M) if MPE=0 : [(m_H), (R)]←(M)	01010	m_H	m_L	r
		m, @r	if MPE=1 : (M)←[(MP), (R)] if MPE=0 : (M)←[(m_H), (R)]	11010	m_H	m_L	r
		m, #i	(M)← i	11101	m_H	m_L	i
	MOVT注	DBF, @AR	($STACK_{PC}$)←(PC), (PC)←(AR), (DBF)←(ROM_{PC}), (PC)←($STACK_{PC}$)	00111	000	0001	0000
	PUSH	AR	(SP)←(SP) − 1, ($STACK_{PC}$)←(AR)	00111	000	1101	0000
	POP	AR	(AR)←($STACK_{PC}$), (SP)←(SP) + 1	00111	000	1100	0000
	PEEK	WR, rf	(WR)←(RF)	00111	rf_H	0011	rf_L
	POKE	rf, WR	(RF)←(WR)	00111	rf_H	0010	rf_L
	GET	DBF, p	(DBF)←(PE)	00111	p_H	1011	p_L
	PUT	p, DBF	(PE)←(DBF)	00111	p_H	1010	p_L

*: **2 machine cycles (equivalent to 2 instructions) are necessary for the execution of MOVT instruction. The stack is temporarily used for instruction execution.**

Instruction	Mnemonic	Operand	Operation	Machine Code			
				Operation Code			
Judge	SKT	m, #n	if(M)$_n$=all "1", then skip	11110	m_H	m_L	n
	SKF	m, #n	if(M)$_n$=all "0", then skip	11111	m_H	m_L	n
Branch	BR	addr	(PC)← addr, (PC)$_{12}$, $_{11}$← 00	01100	addr (least significant 11 bits)		
			(PC)← addr, (PC)$_{12}$, $_{11}$← 01	01101			
			(PC)← addr, (PC)$_{12}$, $_{11}$← 10	01110			
			(PC)← addr, (PC)$_{12}$, $_{11}$← 11	01111			
		@AR	(PC)← (AR)	00111	000	0100	0000
Shift	RORC	r	C ← (R)$_3$ → (R)$_2$ → (R)$_1$ → (R)$_0$ → C	00111	000	0111	r
Subroutine	CALL	addr	(SP)← (SP) − 1, (STACK$_{PC}$)← ((PC) + 1) (PC)$_{11}$← 0, (PC)← addr	11100	addr (11 bits)		
		@AR	(SP)← (SP) − 1, (STACK$_{PC}$)← ((PC) + 1) (PC)← (AR)	00111	000	0101	0000
	RET		(PC)← (STACK$_{PC}$), (SP)← (SP) + 1	00111	000	1110	0000
	RETSK		(PC)← (STACK$_{PC}$), (SP)← (SP) + 1, and skip	00111	001	1110	0000
	RETI		(PC), (BANK), (IXE)← (STACK), (SP)← (SP) + 1	00111	100	1110	0000
Interrupt	EI		INTEF ← 1	00111	000	1111	0000
	DI		INTEF ← 0	00111	001	1111	0000
Others	STOP	0	stop clock if CE = low	00111	010	1111	0000
	HALT	h	halt	00111	011	1111	h
	NOP		No operation	00111	100	1111	0000

22.3 INTRINSIC MACRO INSTRUCTIONS

The following macro instructions are available as intrinsic macro instructions for the 17K series assembler (AS17K). For details, refer to the Assembler User's Manual.

Legend

flag : One of flag1 to flagn
flag1 to flagn : Flag name indicated by the reserved word
n : Number
< > : Omissible

	Mnemonic	Operand	n	Operation
Intrinsic Macro Instructions	SKTn	flag1, ··· flagn	1 ≦n≦ 4	if (flag1) − (flagn) = all "1", then skip
	SKFn	flag1, ··· flagn	1 ≦n≦ 4	if (flag1) − (flagn) = all "0", then skip
	SETn	flag1, ··· flagn	1 ≦n≦ 4	(flag1) − (flagn) ← 1
	CLRn	flag1, ··· flagn	1 ≦n≦ 4	(flag1) − (flagn) ← 0
	NOTn	flag1, ··· flagn	1 ≦n≦ 4	if (flag) = "0", then (flag) ← 1, if (flag) = "1", then (flag) ← 0
	INITFLG	<NOT>flag1, ··· <NOT>flagn	1 ≦n≦ 4	if description = NOT flag, (flag) ← 0 if description = flag, (flag) ← 1
	BANKn		0 ≦n≦ 3	(BANK) ← n

23. RESERVATION SYMBOLS FOR ASSEMBLER

μPD17051 reservation symbols for use of an assembler are shown below.

23.1 SYSTEM REGISTER (SYSREG)

Reserved Word	Type	Address	Read Write	Overview of Function
AR3	MEM	0.74H	R	Address register bits b15 to b12
AR2	MEM	0.75H	R	Address register bits b11 to b8
AR1	MEM	0.76H	R W	Address register bits b9 to b4
AR0	MEM	0.77H	R W	Address register bits b3 to b0
WR	MEM	0.78H	R W	Window register
BANK	MEM	0.79H	R W	Bank register
IXH	MEM	0.7AH	R W	Index register high
MPH	MEM	0.7AH	R W	Data memory row address pointer high
MPE	FLG	0.7AH.3	R W	Memory pointer enable flag
IXM	MEM	0.7BH	R W	Index register middle
MPL	MEM	0.7BH	R W	Data memory row address pointer low
IXL	MEM	0.7CH	R W	Index register low
RPH	MEM	0.7DH	R W	General register pointer high
RPL	MEM	0.7EH	R W	General register pointer low
PSW	MEM	0.7FH	R W	Program status word
BCD	FLG	0.7EH.0	R W	BCD flag
CMP	FLG	0.7FH.3	R W	Compare flag
CY	FLG	0.7FH.2	R W	Carry flag
Z	FLG	0.7FH.1	R W	Zero flag
IXE	FLG	0.7FH.0	R W	Index enable flag

23.2 DATA BUFFER (DBF)

Reserved Word	Type	Address	Read Write	Overview of Function
DBF3	MEM	0.0CH	R W	Data buffer bits b15 to b12
DBF2	MEM	0.0DH	R W	Data buffer bits b11 to b8
DBF1	MEM	0.0EH	R W	Data buffer bits b7 to b4
DBF0	MEM	0.0FH	R W	Data buffer bits b3 to b0

23.3 GENERAL-PURPOSE PORT REGISTER

Reserved Word	Type	Address	Read/ Write	Overview of Function
P0A3	FLG	0.70H.3	R/W	Bit b3 of Port 0A
P0A2	FLG	0.70H.2	R/W	Bit b2 of Port 0A
P0A1	FLG	0.70H.1	R/W	Bit b1 of Port 0A
P0A0	FLG	0.70H.0	R/W	Bit b0 of Port 0A
P0B3	FLG	0.71H.3	R/W	Bit b3 of Port 0B
P0B2	FLG	0.71H.2	R/W	Bit b2 of Port 0B
P0B1	FLG	0.71H.1	R/W	Bit b1 of Port 0B
P0B0	FLG	0.71H.0	R/W	Bit b0 of Port 0B
P0C3	FLG	0.72H.3	R/W	Bit b3 of Port 0C
P0C2	FLG	0.72H.2	R/W	Bit b2 of Port 0C
P0C1	FLG	0.72H.1	R/W	Bit b1 of Port 0C
P0C0	FLG	0.72H.0	R/W	Bit b0 of Port 0C
P0D3	FLG	0.73H.3	R	Bit b3 of Port 0D
P0D2	FLG	0.73H.2	R	Bit b2 of Port 0D
P0D1	FLG	0.73H.1	R	Bit b1 of Port 0D
P0D0	FLG	0.73H.0	R	Bit b0 of Port 0D
P1A3	FLG	1.70H.3	R/W	Bit b3 of Port 1A
P1A2	FLG	1.70H.2	R/W	Bit b2 of Port 1A
P1A1	FLG	1.70H.1	R/W	Bit b1 of Port 1A
P1A0	FLG	1.70H.0	R/W	Bit b0 of Port 1A
P1B3	FLG	1.71H.3	R/W	Bit b3 of Port 1B
P1B2	FLG	1.71H.2	R/W	Bit b2 of Port 1B
P1B1	FLG	1.71H.1	R/W	Bit b1 of Port 1B
P1B0	FLG	1.71H.0	R/W	Bit b0 of Port 1B
P1C3	FLG	1.72H.3	R/W	Bit b3 of Port 1C
P1C2	FLG	1.72H.2	R/W	Bit b2 of Port 1C
P1C1	FLG	1.72H.1	R/W	Bit b1 of Port 1C
P1D3	FLG	1.73H.3	R/W	Bit b3 of Port 1D
P1D2	FLG	1.73H.2	R/W	Bit b2 of Port 1D
P1D1	FLG	1.73H.1	R/W	Bit b1 of Port 1D
P1D0	FLG	1.73H.0	R/W	Bit b0 of Port 1D

23.4 REGISTER FILE (CONTROL REGISTER)

Reserved Word	Type	Address	Read Write	Overview of Function
IDCDMAEN	FLG	0.80H.1	R W	DMA enable flag
SP	MEM	0.81H	R W	Stack pointer
CE	FLG	0.87H.0	R	CE pin status flag
SIOCH	FLG	0.88H.3	R W	SIO channel select flag
SB	FLG	0.88H.2	R W	SIO mode select flag
SIOMS	FLG	0.88H.1	R W	SIO clock mode select flag
SIOTX	FLG	0.88H.0	R W	SIO TX RX select flag
ZCROSS	FLG	0.89H.3	R W	Timer interrupt mode select flag
TMMD2	FLG	0.89H.2	R W	Timer carry FF mode select flag
TMMD1	FLG	0.89H.1	R W	Timer carry FF mode select flag
TMMD0	FLG	0.89H.0	R W	Timer carry FF mode select flag
INTVSYN	FLG	0.8FH.2	R	Vsync pin status flag
INT	FLG	0.8FH.0	R	RMC pin status flag
HSCGT3	FLG	0.91H.3	R	Hsync counter mode select flag (dummy : 0)
HSCGT2	FLG	0.91H.2	R	Hsync counter mode select flag (dummy : 0)
HSCGT1	FLG	0.91H.1	R W	Hsync counter mode select flag
HSCGT0	FLG	0.91H.0	R W	Hsync counter mode select flag
HSCGOPN	FLG	0.92H.3	R W	Hsync counter gate open flag
RMCSTAT3	FLG	0.95H.3	R	RMC pin status flag (dummy : 0)
RMCSTAT2	FLG	0.95H.2	R W	RMC pin status flag
RMCSTAT1	FLG	0.95H.1	R W	RMC pin status flag
RMCSTAT0	FLG	0.95H.0	R W	RMC pin status flag
TMCY	FLG	0.97H.0	R	Timer carry FF status flag
SBACK	FLG	0.98H.3	R W	Serial bus acknowledge flag
SIONWT	FLG	0.98H.2	R W	SIO no wait flag
SIOWRQ1	FLG	0.98H.1	R W	SIO wait request flag
SIOWRQ0	FLG	0.98H.0	R W	SIO wait request flag
IEGVSYN	FLG	0.9FH.2	R W	Vsync interrupt edge select flag
IEG	FLG	0.9FH.0	R W	RMC interrupt edge select flag
ADCCH2	FLG	0.0A1H.3	R W	A/D converter channel select flag
ADCCH1	FLG	0.0A1H.2	R W	A/D converter channel select flag
ADCCH0	FLG	0.0A1H.1	R W	A/D converter channel select flag
ADCCMP	FLG	0.0A1H.0	R	A/D converter judge flag
P0CGIO	FLG	0.0A7H.0	R W	Port OC I/O select flag
SIOSF8	FLG	0.0A8H.3	R W	SIO shift 8 clock flag
SIOSF9	FLG	0.0A8H.2	R W	SIO shift 9 clock flag
SBSTT	FLG	0.0A8H.1	R W	Serial bus start test flag
SBBSY	FLG	0.0A8H.0	R W	Serial bus busy flag

Remarks: Dummy is "0".

Reserved Word	Type	Address	Read/ Write	Overview of Function
IPSIO	FLG	0.0AFH.3	R/W	SIO interrupt permission flag
IPVSYN	FLG	0.0AFH.2	R/W	Vsync interrupt permission flag
IPTM	FLG	0.0AFH.1	R/W	Timer interrupt permission flag
IP	FLG	0.0AFH.0	R/W	RMC interrupt permission flag
CROMBNK	FLG	0.0B0H.0	R/W	CROM bank select flag
IDCEN	FLG	0.0B1H.0	R/W	IDC enable flag
P1BBIO3	FLG	0.0B5H.3	R/W	P1B3I/O select flag
P1BBIO2	FLG	0.0B5H.2	R/W	P1B2I/O select flag
P1BBIO1	FLG	0.0B5H.1	R/W	P1B1I/O select flag
P1BBIO0	FLG	0.0B5H.0	R/W	P1B0I/O select flag
P0BBIO3	FLG	0.0B6H.3	R/W	P0B3I/O select flag
P0BBIO2	FLG	0.0B6H.2	R/W	P0B2I/O select flag
P0BBIO1	FLG	0.0B6H.1	R/W	P0B1I/O select flag
P0BBIO0	FLG	0.0B6H.0	R/W	P0B0I/O select flag
P0ABIO3	FLG	0.0B7H.3	R/W	P0A3I/O select flag
P0ABIO2	FLG	0.0B7H.2	R/W	P0A2I/O select flag
P0ABIO1	FLB	0.0B7H.1	R/W	P0A1I/O select flag
P0ABIO0	FLG	0.0B7H.0	R/W	P0A0I/O select flag
SIOIMD3	FLG	0.0B8H.3	R	SIO interrupt mode select flag (dummy: 0)
SIOIMD2	FLG	0.0B8H.2	R	SIO interrupt mode select flag (dummy: 0)
SIOIMD1	FLG	0.0B8H.1	R/W	SIO interrupt mode select flag
SIOIMD0	FLG	0.0B8H.0	R/W	SIO interrupt mode select flag
SIOCK3	FLG	0.0B9H.3	R	SIO shift clock select flag (dummy: 0)
SIOCK2	FLG	0.0B9H.2	R	SIO shift clock select flag (dummy: 0)
SIOCK1	FLG	0.0B9H.1	R/W	SIO shift clock select flag
SIOCK0	FLG	0.0B9H.0	R/W	SIO shift clock select flag
IRQSIO	FLG	0.0BFH.3	R/W	SIO interrupt request flag
IRQVSYN	FLG	0.0BFH.2	R/W	Vsync interrupt request flag
IRQTM	FLG	0.0BFH.1	R/W	Timer interrupt request flag
IRQ	FLG	0.0BFH.0	R/W	RMC interrupt request flag

Remarks: Dummy is "0".

23.5 PERIPHERAL HARDWARE ADDRESS

Reserved Word	Type	Address	Read Write	Overview of Function
DBF	DAT	0FH	R/W	GET/PUT instruction data buffer address
IX	DAT	01H	R/W	INC instruction index register address
IDCORG	DAT	01H	R W	IDC start position set register
ADCR	DAT	02H	R/W	A/D converter V_{REF} data register
SIOSFR	DAT	03H	R W	SIO presettable shift register
HSC	DAT	04H	R W	Hsync counter data register
PWMR0	DAT	05H	R W	PWM data register 0
PWMR1	DAT	06H	R W	PWM data register 1
PWMR2	DAT	07H	R W	PWM data register 2
AR	DAT	40H	R W	GET PUT PUSH CALL BR MOVT INC instruction address register address
PWMRMP	DAT	41H	R W	PWMRMP data register

24. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	V_{DD}		–0.3 to +6.0	V
Input Voltage	V_I		–0.3 to V_{DD}	V
Output Voltage	V_O	Except P1A and PWM	–0.3 to V_{DD}	V
Output Current High	I_{OH}	1 pin	–12	mA
		All pins	–20	mA
Output Current Low	I_{OL1}	1 pin (except P1A)	12	mA
		All pins (except P1A)	20	mA
Output Current Low	I_{OL2}	1 pin (P1A only)	17	mA
		All pins (P1A only)	60	mA
Output Withstand Voltage	V_{BDS}	P1A, PWM	13	V
Operating Temperature	T_{opt}		-20 to +70	°C
Storage Temperature	T_{stg}		-55 to +125	°C

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Power Supply Voltage	V_{DD1}	4.5	5.0	5.5	V	All functions in operation
Power Supply Voltage	V_{DD2}	4.0	5.0	5.5	V	Only IDC stop
Data Hold Voltage	V_{DR}	2.2		5.5	V	Clock oscillation stop
Output Withstand Voltage	V_{BDS}			12.5	V	P1A, PWM
Power Supply Voltage Rising Time	t_{rise}			500	ms	V_{DD}: 0 → 4.0 V

DC CHARACTERISTICS (T_a = −20 to +70 °C, V_{DD} = 4.0 to 5.5 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Power Supply Current	I_{DD1}		7	15	mA	CPU operation, IDC operation V_{DD} = 5.5 V
Power Supply Current	I_{DD2}		3.5	15	mA	CPU operation, IDC stop V_{DD} = 5.5 V
Input Voltage High	V_{IH1}	0.7 V_{DD}		V_{DD}	V	P0A, P0B, P0D, P1B, P1C
Input Voltage High	V_{IH2}	0.8 V_{DD}		V_{DD}	V	CE, RMC, $\overline{V_{SYNC}}$, $\overline{H_{SYNC}}$
Input Voltage Low	V_{IL1}	0		0.3 V_{DD}	V	P0A, P0B, P0D, P1B, P1C
Input Voltage Low	V_{IL2}	0		0.2 V_{DD}	V	CE, RMC, $\overline{V_{SYNC}}$, $\overline{H_{SYNC}}$
Output Current High	I_{OH}	-1	-2		mA	$P0A_2$, $P0A_3$, P0B, P0C, P1B, P1C, P1D, RED, GREEN, BLUE, BLANK V_{OH} = V_{DD} −1 V
Output Current Low	I_{OL1}	2	3		mA	P0A, P0B, P0C, P1B, P1C, P1D, RED, GREEN, BLUE, BLANK V_{OL} = 1 V
Output Current Low	I_{OL2}	15	20		mA	P1A V_{OL} = 1 V
Output Current Low	I_{OL3}	1	2		mA	PWM V_{OL} = 1 V
Input Current High	I_{IH}		50		μA	P0D, when pulled down V_{IH} = V_{DD}
Data Hold Current	I_{DR}			10	μA	Clock oscillation stop T_a = 25 °C, V_{DD} = 5.5 V
Output Leakage	I_L			1	μA	$P0A_0$, $P0A_1$, P1A, PWM V_{OH} = 5 V

AC CHARACTERISTICS (T_a = –20 to +70 °C, V_{DD} = 4.0 to 5.5 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Input Frequency	f_{TMIN}	50		60	Hz	P1B3/TMIN
Input Frequency	f_{HS}	10		20	kHz	P0B3/HSCNT
IDC Jitter	IDCG		3	4	ns	V_{DD} = 4.5 to 5.5 V

A/D CONVERTER CHARACTERISTICS (T_a = –20 to +70 °C, V_{DD} = 4.0 to 5.5 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
A/D conversion absolute accuracy		±1/2		±1	LSB	
A/D input impedance		1			MΩ	

SINGLE-CHIP MICROCOMPUTER
BUILT-IN IMAGE DISPLAY CONTROLLER FOR VOLTAGE SYNTHESIZER

The μPD17052 is a 4-bit single-chip microcomputer with a built-in display controller and 14-bit D/A converter for a digital tuning system designed for use in a voltage synthesizer TV set.

The image display controller (IDC) has a variety of image display functions. It is capable of displaying figures as well as characters. All fonts are user-programmable and can be specified as desired. Debugging can be done by actually outputting this data from the start of program development.

The microcomputer is also provided with a horizontal synchronization signal counter for detecting broadcasting stations, and a serial interface for communication with peripheral devices. Also, a 4-bit A/D converter and a 6-bit D/A converter (PWM output) are provided.

The CPU employs the μPD17000 architecture capable of handling the data memory directly without using an accumulator. This ensures highly efficient programming. All instructions comprise a single word with a length of 16 bits.

We also provide an IE-17K (In-Circuit Emulator) and an assembler as easy-to-use μPD17052 system development tools.

FEATURES

- 4-bit microcomputer for digital tuning system
- Built-in 14-bit D/A voltage synthesizer
- Program memory (ROM) : 16K bytes (16 bits x 8,192 steps)
- Data memory (RAM) : 4 bits x 448 words
- Stack levels : 6
- Easy-to-understand instructions (35)
- Decimal operations available
- Instruction execution time : 2 μs (8 MHz oscillator connected)
- Built-in IDC (Image Display Controller) (User programmable)
  - Number of display characters : Max. 99 characters per screen
  - Display position : 14 lines x 19 columns
  - Character set : 128 characters (64 different characters can be displayed in one screen simultaneously.)
  - Colors : 8 colors
  - Character size : 4 sizes can be set in vertical and/or horizontal directions (14, 28, 42, 56H)
- Built-in 8-bit serial interface (One system with two channels: three-wire and two-wire types)
- Built-in D/A converter : 6 bits x 4 (PWM output)
- Built-in A/D converter : 4 bits x 8
- Built-in horizontal synchronization signal counter
- Built-in commercial power frequency counter
- Built-in power failure detection circuit and Power On reset circuit
- Interrupt input for remote control signals (with noise canceller)
- Wealth of I/O ports
  - Input/output ports : 20
  - Input ports : 4
  - Output ports : 20
- 5 V ±10 %
- Use of low power-consumption CMOS
- 64-pin plastic shrink DIP (750 mil)

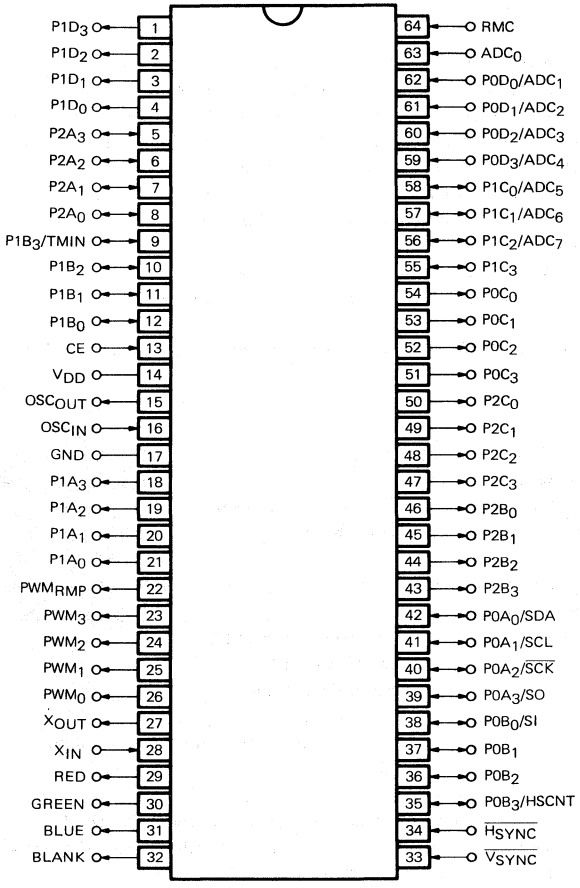
Notes on Serial interface: The 2-wire mode corresponds to the I2C-Bus specification from Philips. In case of using this interface mode note the following:

Duties when using I2C bus system

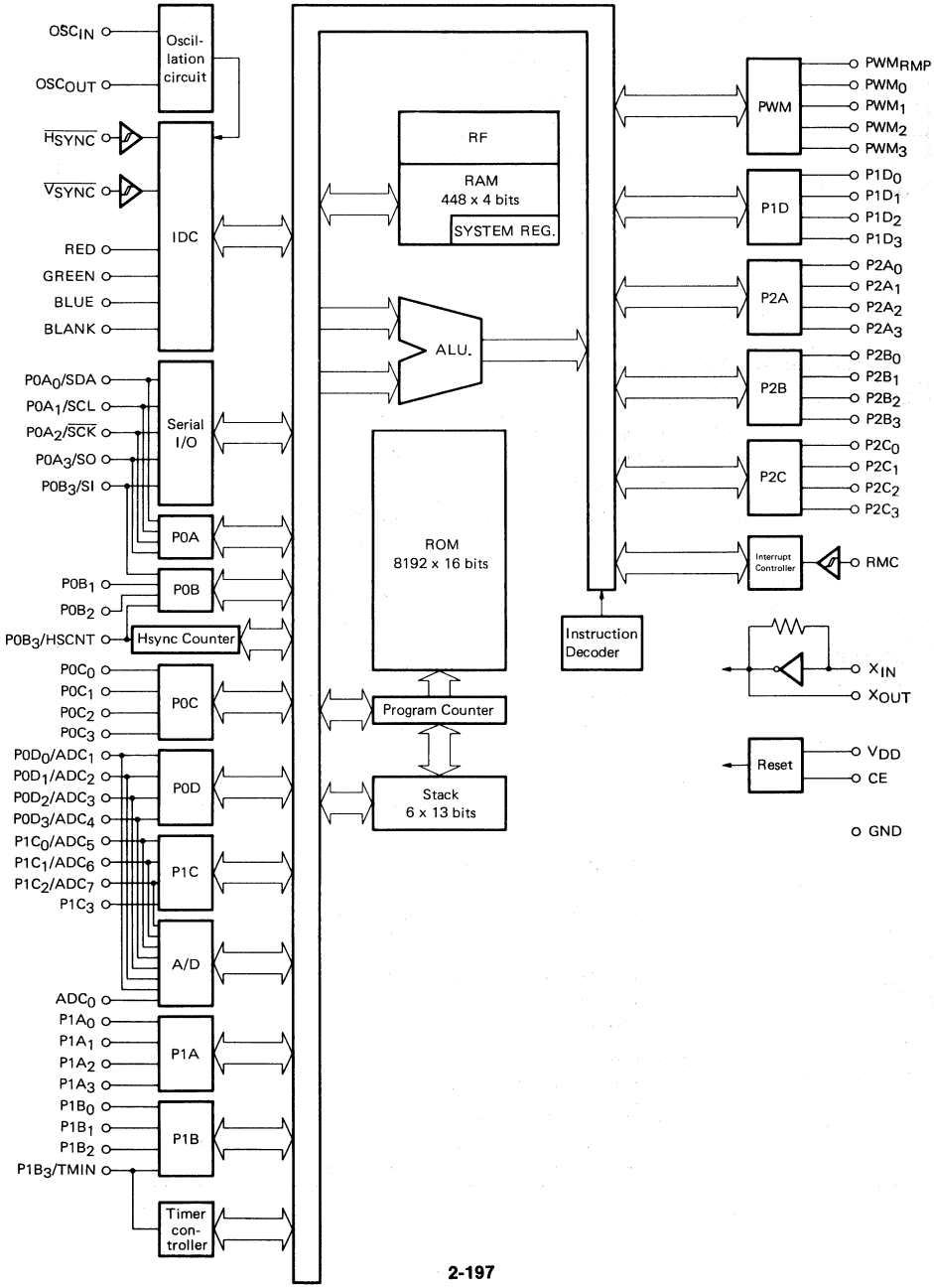
Purchase of NEC's I2C bus system hardware components conveys a license under the Philips I2C patents rights to use this components in an I2C system, provided that the system conforms the I2C standard specifications as defined by Philips.

Consequently for all ROM based components with I2C hardware circuits the user is kindly requested to notify the use of the I2C bus interface at the ROM code verification stage.

PIN CONFIGURATION (Top View)



BLOCK DIAGRAM



List of μPD17052 functions

CHARACTERISTIC	FUNCTION
Program Memory	• 16K bytes (8,192 steps x 16 bits) Table reference area : 256 steps x 16 bits Area serving also as CROM : 2,048 steps x 16bits
Data Memory	• 448 words (448 words x 4 bits) Data buffer : 4 words, General-purpose register : 16 words Area also serving as VRAM : 224 words x 4 bits
System Register	• 12 words
Register File	• 24 words
Port Register	• 11 words
Instruction Execution Time	• 2 μs, using an 8 MHz ceramic oscillator
Stack Levels	• 6 levels (stack operation available)
General-Purpose-Ports	• Input/output ports : 20 • Input ports : 4 • Output ports : 20
IDC (Image Display Controller)	• Number of display character: Max. 99 characters per screen • Display position : 14 lines x 19 columns • Character set : 128 characters (user programmable) (64 different characters can be displayed in one screen simultaneously.) • Character type : 10 x 15 dots • Colors : 8 colors • Character size : 4 sizes in vertical direction (14, 28, 42, 56H) 4 sizes in horizontal direction (2.5, 5.0, 7.5, 10.0 μs) Can be specified in vertical and horizontal directions independently.
Serial Interface	• One system (two channels) 8-bit 3-wire type : one channel 8-bit 2-wire type : one channel
D/A Converter	• 14 bits x 1 (PWM output, withstanding voltage : Max. 12.5 V) • 6 bits x 4 (PWM output, withstanding voltage : Max. 12.5 V)
A/D Converter	• 4 bits x 8 (sequential comparison by means of software)
Interruption	• 4 channels (maskable interrupt) External interrupt : 3 channels (RMC pin, $\overline{V_{SYNC}}$ pin, serial interface) Internal interrupt : One channel (timer)

CHARACTERISTIC	FUNCTION
Timer	• Two system Internal timer : 5, 20, 100 ms External timer : 1/5 and 1/6 of frequency input to PIB_3/TMIN pin
Reset	• Power ON reset (When the power is input) • Resetting by CE pin (CE pin Low → High) • Power failure detection
Power Supply Voltage	• 5 V ±10 %
Package	• 64-pin plastic shrink DIP (750 mil)

PIN DESCRIPTION

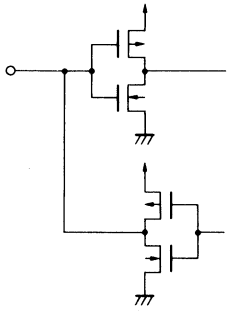
PIN No.	SYMBOL	PIN NAME	DESCRIPTION	OUTPUT TYPE
1 to 4	$P1D_3$ to $P1D_0$	Port 1D	4-bit output ports. The latch of port 1D is assigned to address 73H of Bank 1 of the data memory (RAM). The output state is undefined at the time when the power (V_{DD}) is applied initially.	CMOS push-pull
5 to 8	$P2A_3$ to $P2A_0$	Port 2A	4-bit input/output ports. These ports can be specified for input/output on a bit-by-bit basis. The setting of input/output is performed by using the P1BBIO word (35H) on the register file. The latch of the port is assigned to address 70H of Bank 2 of the data memory (RAM).	CMOS push-pull (I/O)
9 10 11 12	$P1B_3$/TMIN $P1B_2$ $P1B_1$ $P1B_0$	Port 1B	4-bit input/output ports. These ports can be specified for input/output on a bit-by-bit basis. The setting of input/output is performed by using the P1BBIO word (35H) on the register file. The latch of the port is assigned to address 71H of Bank 1 of the data memory (RAM). $P1B_3$/TMIN can also be used as input to an external timer. It is possible to make an interrupt with a frequency equivalent to one-fifth or one-sixth the frequency input to this pin. Normally, the commercial power supply frequency is input to this pin for use as the reference clock.	CMOS push-pull (I/O)
13	CE	Chip enable	Device selection signal input pin. Set the pin at the high level to put the device in normal operation. Set the pin at the low level if the device is not used. When the pin is at the low level, executing the STOP instruction causes the clock oscillation to stop, making backup with a low current possible. The STOP instruction is effective only when the CE pin is at the low level. The instruction is in effect the same as the NOP instruction when the CE pin is at the high level. The pin also serves as a reset pin. Changing the CE pin from the low level to the high level causes the device to be reset and the program to start from address 0. If the device is reset, the bank is made 0 and the I/O ports are put in the input mode.	Input
14	V_{DD}	Power	Device power pin. Supply a voltage of 5 V ±10 % to when activating all functions. If the IDC is not used, apply a voltage of 4 to 5.5 V. To retain the data of RAM (when the clock oscillation is stopped), the voltage may be dropped to 2.5 V. Since the μPD17052 has a built-in power On reset circuit, if the voltage changes from 0 to 4.0 V, the system is reset and the program starts from address 0. To operate the Power On reset circuit properly, it is necessary to limit the rise time from 0 to 4.0 V to 550 ms or less.	–
15 16	OSC_{OUT} OSC_{IN}	LC oscillation	LC oscillation circuit pin for the IDC. Oscillation is made at 4 MHz.	CMOS push-pull (OSC_{OUT}) INPUT (OSC_{IN})
17	GND	Ground	Device grounding pin.	–

PIN No.	SYMBOL	PIN NAME	DESCRIPTION	OUTPUT TYPE
18 to 21	$P1A_3$ to $P1A_0$	Port 1A	4-bit output port. The latch of the port is assigned to address 70H of Bank 1 of the data memory (RAM). N-ch open drain type. (medium withstanding voltage, large current)	N-ch open drain
22	PWM_{RMP}	Tuning D/A converter output	Port for the output of the 14-bit D/A (Digital-to-Analog) converter for a voltage synthesizer, or port for the output of one bit. The D/A converter outputs pulses made up of a combination of 9-bit PWM (Pulse Width Modulation) and 5-bit RMP (Rate Multiplier). D/A conversion is therefore possible by connecting a simple external CR filter. The output is at the low level when Power On is reset or when the clock is stopped.	N-ch open drain
23 to 26	PWM_3 to PWM_0	D/A converter	VDP (Variable Duty Port), or port for the output one bit. The VDP function is to output pulses of a frequency of 15,625 kHz continuously. The duty of the pulse can be made variable in 64 steps by means of a program.	N-ch open drain
27 28	X_{OUT} X_{IN}	Oscillator	CPU oscillation circuit pin. Used to connect a ceramic oscillator or a crystal oscillator. Use an 8 MHz oscillator.	CMOS push-pull (XO) Input (XI)
29 30 31	RED GREEN BLUE	Character signal output	Pins to output character data corresponding to R, G and B. Output is in active High.	CMOS push-pull
32	BLANK	Blanking signal output	Pin to output blanking signals to cut image signals. Output is in active High.	CMOS push-pull
33	$\overline{V_{SYNC}}$	Vertical synchronization signal input	Pin to input vertical synchronization signals for the IDC. Input in active Low. It is possible to make an interrupt with this signal.	Input
34	$\overline{H_{SYNC}}$	Horizontal synchronization signal input	Pin to input horizontal synchronization signals for the IDC. Input in active Low.	Input
35 36 37 38	$P0B_3$/HSCNT $P0B_2$ $P0B_1$ $P0B_0$/SI	Port 0B	4-bit input/output ports. For these ports, it is possible to specify input/output on a bit by bit basis. The setting is made with the P0BBIO word (36H) on the register file. The latch of the port is assigned to address 71H of Bank 0 of the data memory (RAM). The $P0B_0$/SI pin can also serve as a data input pin of a serial interface (μCOM standard mode). The $P0B_3$/HSCNT pin can also serve as an input pin of the horizontal synchronization signal counter. This pin is always self-biased ($V_{DD}/2$). Port 0B is for input when the power (V_{DD}) is input initially, the clock stops, or resetting is done by the CE pin (Low → High).	CMOS push-pull (I/O), provided $P0B_3$/HSCNT is self-biased at the time of input.
39 40 41 42	$P0A_3$/SO $P0A_2/\overline{SCK}$ $P0A_1$/SCL $P0A_0$/SDA	Port 0A	4-bit input/output ports. These ports can be specified for input/output on a bit-by-bit basis. The setting is made with the P0ABIO word (37H) on the register file. The latch of the port is assigned to address 70H of Bank 0 of the data memory. The $P0A_3$ pin can be used as a data output pin of a serial interface (μCMOS standard mode) and the $P0A_2$/SCK pin as a shift clock input/output pin. The $P0A_0$/SDA pin can be used as a data input/output pin of a serial interface (two-wire mode and μCOM standard mode), and the $P0A_1$/SCL pin as a shift clock input/output pin.	CMOS push-pull

PIN No.	SYMBOL	PIN NAME	DESCRIPTION	OUTPUT TYPE
43 to 46	$P2B_3$ to $P2B_0$	Port 2B	4-bit output port. The latch of the port is assigned to address 71H of Bank 2 of the data memory (RAM). N-ch open drain (medium withstanding voltage).	N-ch open drain
47 to 50	$P2C_3$ to $P2C_0$	Port 2C	4-bit output port. The latch of the port is assigned to address 72 of Bank 2 of the data memory (RAM). N-ch open drain. (medium withstanding voltage)	N-ch open drain
51 to 54	$P0C_3$ to $P0C_0$	Port 0C	4-bit output port. The latch of Port 0C is assigned to address 72H of Bank 0 of the data memory (RAM). The output state is indefinite when the power (V_{DD}) is input initially.	CMOS push-pull
55 56 57 58	$P1C_3$ $P1C_2/ADC_7$ $P1C_1/ADC_6$ $P1C_0/ADC_5$	Port 1C	4-bit input/output port or A/D converter pin. The setting of input/output is made every 4 bits. The P1CGIO bit (bit #0 of address 27H) on the register file is used for input/output specification. It is necessary to specify input without fail when used as an A/D converter. The latch of the port is assigned to address 72 of Bank 1 of the data memory (RAM). Port 1C is for input when the power (V_{DD}) is applied for the first time, the clock is stopped or resetting is made with the CE pin (Low → High).	CMOS push-pull (I/O)
59 60 61 62	$P0D_3/ADC_4$ $P0D_2/ADC_3$ $P0D_1/ADC_2$ $P0D_0/ADC_1$	Port 0D	4-bit input port. This port can also be used as an A/D converter. When used as a port, a pull-down resistance (100 kΩ TYP.) is attached. The latch of Port 0D is assigned to address 73H of the data memory (RAM).	Input (with pull-down resistance)
63	ADC_0	A/D converter input	A/D (Analog to Digital) converter input pin. The converter is a 4-bit built-in A/D converter employing programmed sequential comparison. The reference voltage of the A/D converter is V_{DD}.	Input
64	RMC	Interrupt signal input	Interrupt input pin with a noise canceller. Signals with a high level of noise, such as remote control signals, can be programmed easily by using this pin. It is possible to specify by means of a program whether an interrupt is made at the rise or at the fall of an input signal to this pin. Specifically, an interrupt is made at the rise or at the fall of the signal depending on whether the IEDG1 flag is reset or set, respectively. At the time of resetting (CE pin: Low → High), the IEDG1 flag is reset and an interrupt is made at the edge of the rise.	Input

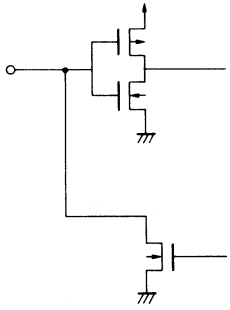
PIN EQUIVALENT CIRCUITS

P0A ($P0A_3$/SO, $P0A_2$/$\overline{SCK}$)
P0B ($P0B_2$, $P0B_1$, $P0B_0$/SI)
P1B ($P1B_2$, $P1B_1$, $P1B_0$)
P1C ($P1C_3$, $P1C_2$/ADC_7, $P1C_1$/ADC_6, $P1C_0$/ADC_5)
P2A ($P2A_3$, $P2A_2$, $P2A_1$, $P2A_0$)



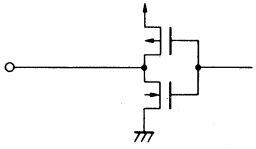
(IN/OUT)

P0A ($P0A_1$/SCL, $P0A_0$/SDA)



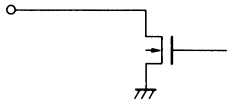
(IN/OUT)

P0C ($P0C_3$, $P0C_2$, $P0C_1$, $P0C_0$)
P1D ($P1D_3$, $P1D_2$, $P1D_1$, $P1D_0$)
RED, GREEN, BLUE, BLANK



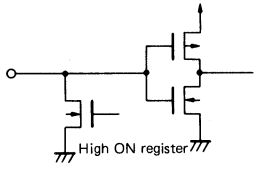
(OUT)

PWM (PWM_3, PWM_2, PWM_1, PWM_0, PWM_{RMP})
P1A ($P1A_3$, $P1A_2$, $P1A_1$, $P1A_0$)
P2B ($P2B_3$, $P2B_2$, $P2B_1$, $P2B_0$)
P2C ($P2C_3$, $P2C_2$, $P2C_1$, $P2C_0$)



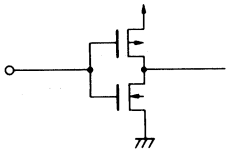
(OUT)

P0D ($P0D_3/ADC_4$, $P0D_2/ADC_3$, $P0D_1/ADC_2$, $P0D_0/ADC_1$)



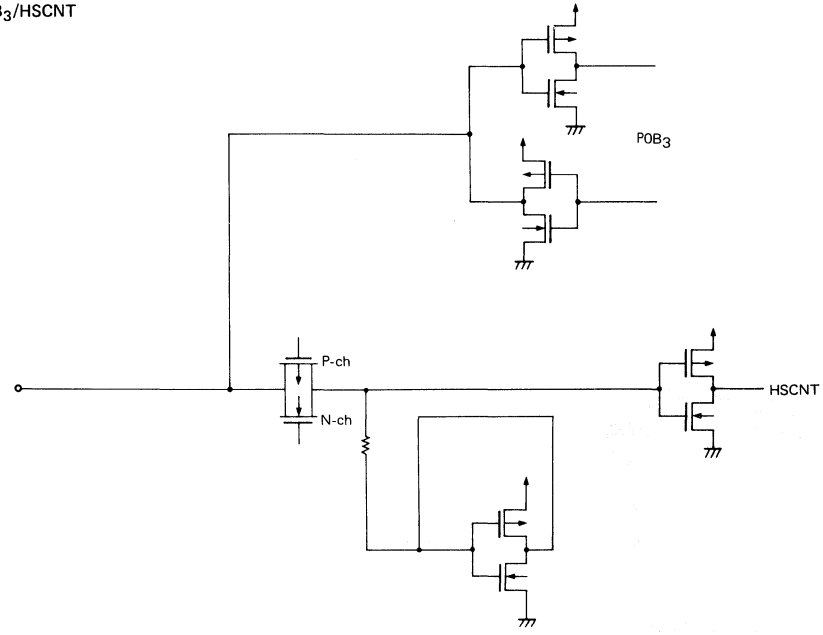
(IN)

ADC_0

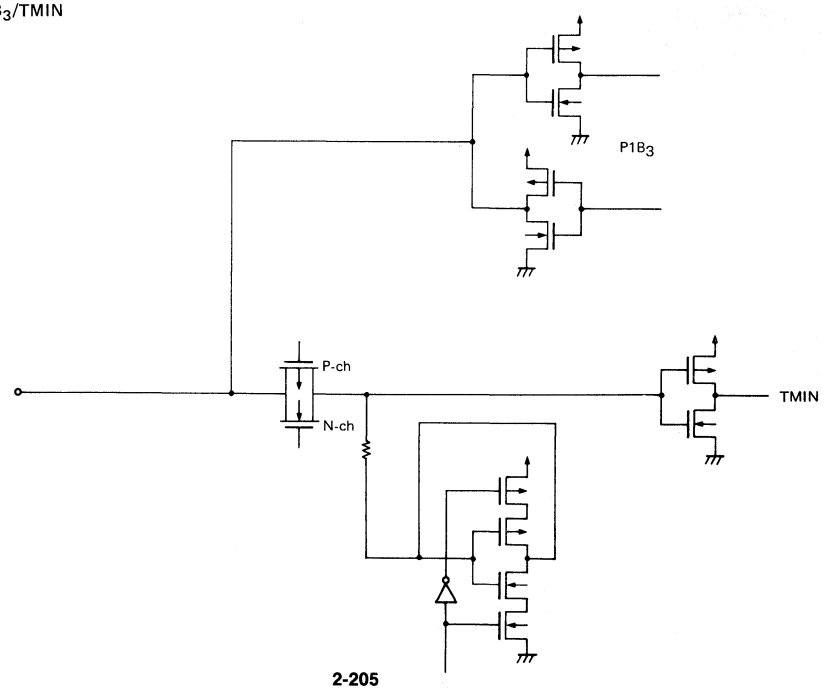


(IN)

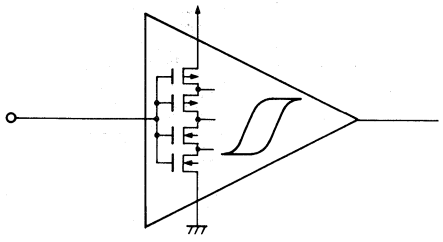
P0B$_3$/HSCNT



P1B$_3$/TMIN

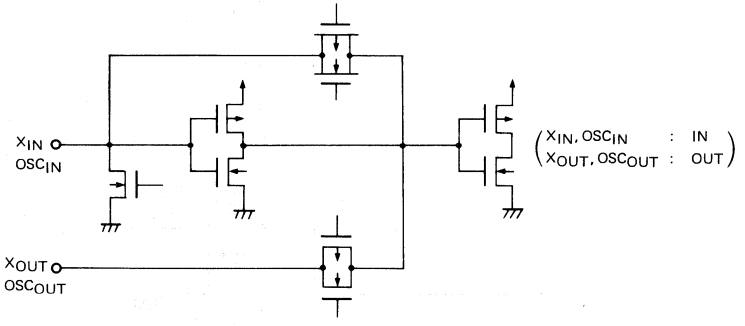


$\overline{H_{SYNC}}$, $\overline{V_{SYNC}}$, RMC, CE



(IN)

X_{OUT}, X_{IN}, OSC_{OUT}, OSC_{IN}



μPD17052 instructions

Instruction set

		0		1	
0000	0	ADD	r, m	ADD	m, #i
0001	1	SUB	r, m	SUB	m, #i
0010	2	ADDC	r, m	ADDC	m, #i
0011	3	SUBC	r, m	SUBC	m, #i
0100	4	AND	r, m	AND	m, #i
0101	5	XOR	r, m	XOR	m, #i
0110	6	OR	r, m	OR	m, #i
0111	7	INC INC MOVT BR CALL RET RETSK EI DI RETI PUSH POP GET PUT PEEK POKE RORC STOP HALT NOP	AR IX DBF, @AR @AR @AR AR AR DBF, p p, DBF WR, rf rf, WR r 0 h		
1000	8	LD	r, m	ST	m, r
1001	9	SKE	m, #i	SKGE	m, #i
1010	A	MOV	@r, m	MOV	m, @r
1011	B	SKNE	m, #i	SKLT	m, #i
1100	C	BR	addr (page 0)	CALL	addr (page 0)
1101	D	BR	addr (page 1)	MOV	m, #i
1110	E	BR	addr (page 2)	SKT	m, #n
1111	F	BR	addr (page 3)	SKF	m, #n

INSTRUCTION

NOTE

M : One of Data memory specified by [(BANK), m]
m : Data memory address specified by [m_H, m_L] of each bank
m_H : Data memory address high (Row address) ; [3bits]
m_L : Data memory address low (Column address) ; [4bits]
R : One of General register specified by [(RP), r]
r : General register address low ; [4bits]
RP : General register pointer
RF : One of register file specified by rf
rf : Register file address specified by [rf_H, rf_L]
rf_H : Register file address high
rf_L : Register file address low
AR : Address register
IX : Index register
IXE : Index enable flag
DBF : Data buffer
WR : Window register
MP : Memory pointer
MPE : Memory pointer enable flag
PE : Peripheral
p : Peripheral address
p_H : Peripheral address high
p_L : Peripheral address low
PC : Program memory counter
SP : Stack pointer
STACK : Stack of (PC), (BANK), (IXE)
$STACK_{PC}$: Stack of (PC)
BANK : Bank register
$(ROM)_{PC}$: One of Program memory data specified by (PC)
INTEF : Interrupt enable flag
SGR : Program memory segment register
i : Immediate data ; [4bits]
n : Bit position ; [4bits]
addr : One of program memory address ; [11bits]
CY : Carry flag
h : Halt release conditions
[ ] : Address of M, R, RF
( ) : Contents of M, R, RF, AR, IX, DBF, WR, PE

	Mnemonic	Operand	Function	Operation	Machine code			
					Operation code			
Addition	ADD	r, m	Add Data memory to General register	(R), (CY)←(R)+(M)	00000	m_H	m_L	r
		m, #i	Add immediate data to Data memory	(M), (CY)←(M)+i	10000	m_H	m_L	i
	ADDC	r, m	Add Data memory to General register with carry	(R), (CY)←(R)+(M)+(CY)	00010	m_H	m_L	r
		m, #i	Add immediate data to Data memory with carry	(M), (CY)←(M)+i+(CY)	10010	m_H	m_L	i
	INC	AR	Increment Address register	(AR)←(AR)+1	00111	000	1001	0000
		IX	Increment Index register	(IX)←(IX)+1	00111	000	1000	0000
Subtraction	SUB	r, m	Subtract Data memory from General register	(R), (CY)←(R)−(M)	00001	m_H	m_L	r
		m, #i	Subtract immediate data from Data memory	(M), (CY)←(M)−i	10001	m_H	m_L	i
	SUBC	r, m	Subtract Data memory from General register with borrow	(R), (CY)←(R)−(M)−(CY)	00011	m_H	m_L	r
		m, #i	Subtract immediate data from Data memory with borrow	(M), (CY)←(M)−i−(CY)	10011	m_H	m_L	i
Comparison	SKE	m, #i	Skip if Data memory equals immediate data	(M)−i & skip if zero	01001	m_H	m_L	i
	SKGE	m, #i	Skip if Data memory is greater than or equal to immediate data	(M)−i & skip if not borrow	11001	m_H	m_L	i
	SKLT	m, #i	Skip if Data memory is less than immediate data	(M)−i & skip if borrow	11011	m_H	m_L	i
	SKNE	m, #i	Skip if Data memory not equal immediate data	(M)−i & skip if not zero	01011	m_H	m_L	i
Logical operation	AND	m, #i	Logic AND of Data memory and immediate data	(M)←(M) AND i	10100	m_H	m_L	i
		r, m	Logic AND of General register and Data memory	(R)←(R) AND (M)	00100	m_H	m_L	r
	OR	m, #i	Logic OR of Data memory and immediate data	(M)←(M) OR i	10110	m_H	m_L	i
		r, m	Logic OR of General register and Data memory	(R)←(R) OR (M)	00110	m_H	m_L	r
	XOR	m, #i	Exclusive Logic OR of Data memory and immediate data	(M)←(M) XOR i	10101	m_H	m_L	i
		r, m	Exclusive Logic OR of General register and Data memory	(R)←(R) XOR (M)	00101	m_H	m_L	r

	Mnemonic	Operand	Function	Operation	Machine code			
					Operation code			
Transfer	LD	r, m	Load Data memory to General register	(R)←(M)	01000	m_H	m_L	r
	ST	m, r	Store General register to Data memory	(M)←(R)	11000	m_H	m_L	r
	MOV	@r, m	Move Data memory to Destination data memory referring to General register	if MPE=1: [(MP), (R)]←(M) if MPE=0: [(m_H), (R)]←(M)	01010	m_H	m_L	r
		m, @r	Move Source data memory referring to General register to Data memory	if MPE=1: (M)←[(MP), (R)] if MPE=0: (M)←[(m_H), (R)]	11010	m_H	m_L	r
		m, #i	Move immediate data to Data memory	(M)←i	11101	m_H	m_L	i
	MOVT	DBF, @AR	Move Program memory data specified by Address register to Data buffer	($STACK_{PC}$)←(PC) & (PC)←(AR) & (DBF)←$(ROM)_{PC}$ & (PC)←($STACK_{PC}$)	00111	000	0001	0000
	PUSH	AR	Decrement Stack pointer, then move Address register to Stack	(SP)←(SP)−1 & ($STACK_{PC}$)←(AR)	00111	000	1101	0000
	POP	AR	Move Stack to Address register, then increment Stack pointer	(AR)←($STACK_{PC}$) & (SP)←(SP)+1	00111	000	1100	0000
	PEEK	WR, rf	Get data of Register file to Window register	(WR)←(RF)	00111	rf_H	0011	rf_L
	POKE	rf, WR	Put data of Window register into Register file	(RF)←(WR)	00111	rf_H	0010	rf_L
	GET	DBF, p	Get peripheral data to Data buffer	(DBF)←(PE)	00111	p_H	1011	p_L
	PUT	p, DBF	Put data of Data buffer to peripheral	(PE)←(DBF)	00111	p_H	1010	p_L
Judgment	SKT	m, #n	Test Data memory bits, then skip if all bits specified are true	if $(M)_n$=all "1", then skip	11110	m_H	m_L	n
	SKF	m, #n	Test Data memory bits, then skip if all bits specified are false	if $(M)_n$=all "0", then skip	11111	m_H	m_L	n
Branch	BR	addr	Jump to the address in page 0	(PC)←addr & $(PC)_{\#12}$←0, $(PC)_{\#11}$←0	01100	addr (11 bits)		
			Jump to the address in page 1	(PC)←addr & $(PC)_{\#12}$←0, $(PC)_{\#11}$←1	01101			
			Jump to the address in page 2	(PC)←addr & $(PC)_{\#12}$←1, $(PC)_{\#11}$←0	01110			
			Jump to the address in page 3	(PC)←addr & $(PC)_{\#12}$←1, $(PC)_{\#11}$←1	01111			
		@AR	Jump to the address specified by Address register	(PC)←(AR)	00111	000	0100	0000
Shift	RORC	r	Rotate General register right with carry	C←→$(R)_{\#3}$→$(R)_{\#2}$→$(R)_{\#1}$→$(R)_{\#0}$	00111	000	0111	r
Subroutine	CALL	addr	Call subroutine in page 0	(SP)←(SP)−1 & ($STACK_{PC}$)←((PC)+1) & $(PC)_{\#11}$←0 & (PC)←addr	11100	addr (11 bits)		
		@AR	Call subroutine	(SP)←(SP)−1 & ($STACK_{PC}$)←((PC)+1) & (PC)←(AR)	00111	000	1110	0000
	RET		Return to main routine from subroutine	(PC)←($STACK_{PC}$) & (SP)←(SP)+1	00111	001	1110	0000
	RETSK		Return to main routine from subroutine, then skip unconditionary	(PC)←($STACK_{PC}$) & (SP)←(SP)+1 & and skip	00111	100	1110	0000
	RETI		Return to main routine from interrupt service routine	(PC), (BANK), (IXE)←(STACK) & (SP)←(SP)+1	00111	000	0101	0000
Interrupt	EI		Enable interrupt	INTEF←1	00111	000	1111	0000
	DI		Disable interrupt	INTEF←0	00111	001	1111	0000
Others	STOP	0	Stop clock if CE=low	stop clock if CE=low	00111	010	1111	0000
	HALT	h	Halt the CPU, Restart by condition h	halt	00111	011	1111	h
	NOP		No operation		00111	100	1111	0000

ELECTRIC CHARACTERISTICS (PROVISIONAL)

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	V_{DD}	−0.3 to +6.0	V
Input Voltage	V_I	−0.3 to V_{DD}	V
Output Voltage	V_O	−0.3 to V_{DD}	V
Output Absorption Current	I_O	10	mA
Withstanding Output Voltage	V_{BDS}	13 (P1A, P2B, P2C, PWM)	V
Operating Temperature	T_a	−20 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Power Supply Voltage	V_{DD1}	4.5	5.0	5.5	V	All function activated
Power Supply Voltage	V_{DD2}	4.0	5.0	5.5	V	Only IDC stopped
Data Storing Voltage	V_{DR}	2.5		5.5	V	Clock oscillation stopped
Withstanding Output Voltage	V_{BDS}			12.5	V	P1A, P2B, P2C, PWM
Power Supply Voltage Rise Time	t_{rise}			500	ms	V_{DD}: 0 → 4.0 V

DC CHARACTERISTICS (T_a = –20 to +70 °C, V_{DD} = 4.0 to 5.5 V)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Power Supply Current	I_{DD1}		7	15	mA	CPU in operation, IDC in operation V_{DD}=5.5 V
Power Supply Current	I_{DD2}		3.5	15	mA	CPU in operation, IDC stopped V_{DD}=5.5 V
High Level Input Voltage	V_{IH1}	0.7 V_{DD}			V	P0A, P0B, P0D, P1B, P1C, P2A
High Level Input Voltage	V_{IH2}	0.8 V_{DD}			V	CE, RMC, $\overline{V_{SYNC}}$, $\overline{H_{SYNC}}$
Low Level Input Voltage	V_{IL1}			0.3 V_{DD}	V	P0A, P0B, P0D, P1B, P1C, P2A
Low Level Input Voltage	V_{IL2}			0.2 V_{DD}	V	CE, RMC, $\overline{V_{SYNC}}$, $\overline{H_{SYNC}}$
High Level Output Current	I_{OH}		–2	–1	mA	$P0A_2$, $P0A_3$, P0B, P0C, P1B, P1C, P1D, RED, GREEN, BLUE, BLANK $V_{OH}=V_{DD}-1$ V
Low Level Output Current	I_{OL1}	2	3		mA	P0A, P0B, P0C, P1B, P1C, P1D, RED, GREEN, BLUE, BLANK V_{OL}=1 V
Low Level Output Current	I_{OL2}	15	20		mA	P1A V_{OL}=1 V
Low Level Output Current	I_{OL3}	1	2		mA	PWM, P2B, P2C V_{OL}=1 V
High Level Input Current	I_{IH}		50		μA	P0D, pull-down time
Data Storing Current	I_{DR}			10	μA	Clock oscillation stopped T_a=25 °C, V_{DD}=5.5 V
Output Leak	I_L			1	μA	$P0A_0$, $P0A_1$, P1A, P2B, P2C, PWM V_{OH}=5 V

AC CHARACTERISTICS

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Input Frequency	f_{TMR}	50		60	Hz	$P1B_3$/TMIN
Input Frequency	f_{HS}	10		20	kHz	$P0B_3$/HSCNT

BUILT-IN IMAGE DISPLAY CONTROLLER

The μPD17053 is a 4 bits CMOS microcontroller incorporating Image Display Controller (IDC) and 14 bits D/A converter into one chip for digital tuning of voltage synthesizer system of TV.

Image Display Controller has various display function showing not only letters but also drawings.

Fonts of IDC are selected by user's program and effective debugging can be realized by actual indications from the beginning of software development.

In addition, Hsync. counter for station detection and serial interface for communication with other peripheral devices are incorporated, also 4 bits A/D converter and 6 bits D/A converter (PWM output) are incorporated.

CPU applies μPD17000 architecture which operates data memory directly without accumulater, and it realizes effective programming.

All instruction consist of 16 bits one word.

As system development support tool of μPD17053, IE-17K (In Circuit Emulator) and assembler are prepared.

FEATURES

- 4 bits microcontroller for digital tuning system
- built-in 14 bits D/A converter
- single power supply (5 V ±10 %)
- CMOS with low power consumption
- program memory (ROM):
  24K byte (16 bits x 12,288 steps)
- data memory (RAM): 4 bits x 672 words
- stack level: 7 levels
- easy to understand instruction set with 36 types
- capable of decimal arithmetic
- instruction execution time:
  2 μs (with 8 MHz ceramic resonator connected)
- IDC (Image Display Controller) built-in
  (user programmable)
  - number of display character:
    199 characters (max. in one screen)
  - display location: 14 lines x 19 columns
  - number of character types: 256 types
  - character format:
    10 x 15 dots (capable of fringe function)
  - character color: 8 colors
  - character size:
    4 types of setting is available independently both for line and column, (14, 28, 42, 56H)
- built-in 8 bits serial interface:
  (1 system 2 channel: 3 wire and 2 wire system)
- built-in D/A converter: 6 bits x 4 (PWM output)
- built-in A/D converter: 4 bits x 8
- built-in H.sync. signal counter
- built-in commercial power supply freq. counter
- built-in blackout detection circuit and power-on-reset circuit.
- interrupt input for remote control signal (with noise canceler)
- plentiful I/O ports: input output port : 20
  input port : 4
  output port : 20
- 64 pin plastic shrink DIP (750 mil)

Notes on Serial interface:

The 2-wire mode corresponds to the I2C-Bus specification from Philips.

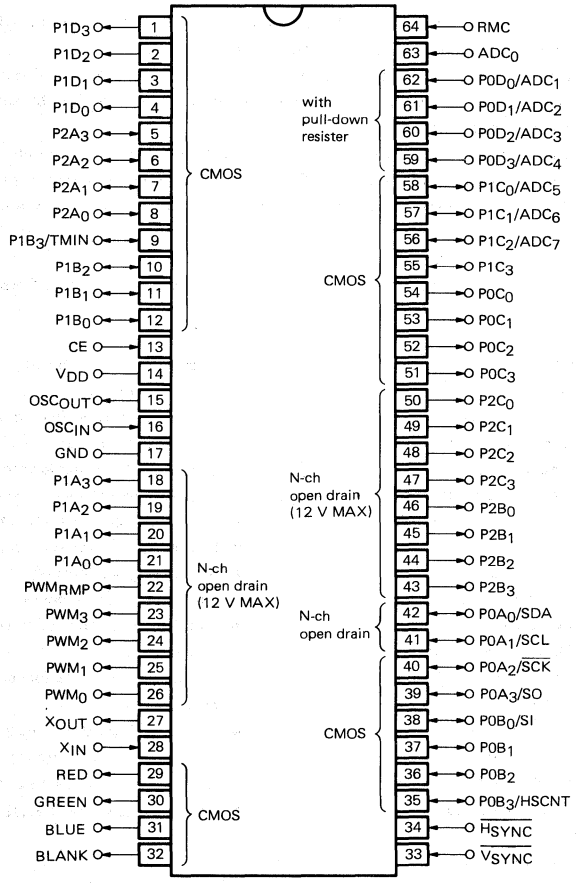
In case of using this interface mode note the following:

Duties when using I2C bus system

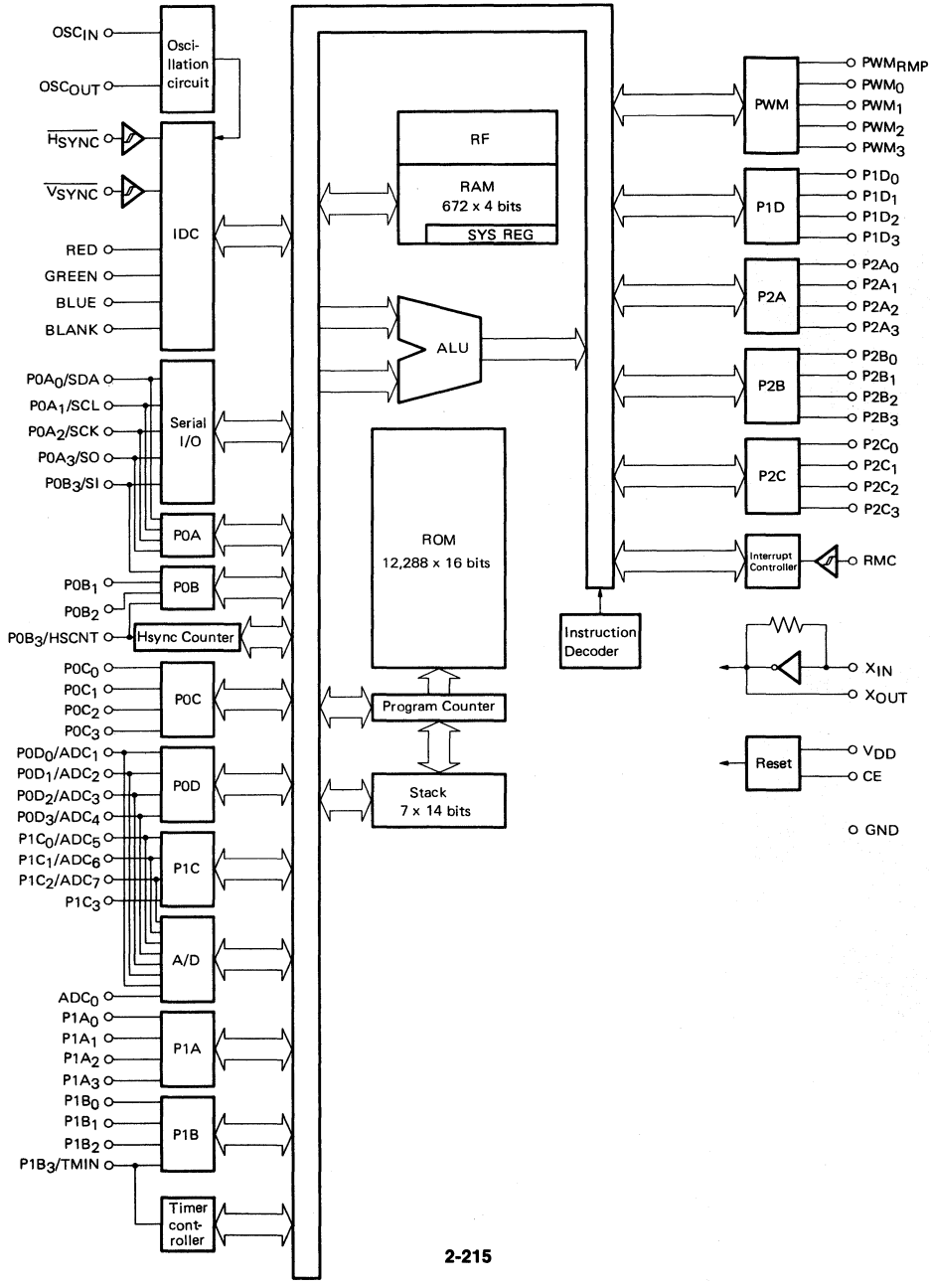
Purchase of NEC's I2C bus system hardware components conveys a license under the Philips I2C patents rights to use this components in an I2C system, provided that the system conforms the I2C standard specifications as defined by Philips.

Consequently for all ROM based components with I2C hardware circuits the user is kindly requested to notify the use of the I2C bus interface at the ROM code verification stage.

PIN CONFIGURATION (Top View)



BLOCK DIAGRAM



SINGLE-CHIP MICROCONTROLLER

The μPD17102 is a four-bit single chip microcontroller which has a built-in LCD controller, D/A converter, and operational amplifier. This CPU uses the μPD17000 architecture, allowing data transfer and operation between data memory areas or between data memory areas and peripheral circuits with only one instruction. It also supports 16-bit (1-word) instructions.

FEATURES

- μPD17000 architecture
- Program memory (ROM) : 4K bytes (2048 x 16 bits)
- Data memory (RAM) : 208 words (208 x 4 bits)
- Command execution time : 2.0 μs (8 MHz, ceramic/crystal oscillator)
- Interrupting function (Internal: 3, and external: 2)
- 8-bit timer/counter : 2 channels (built-in modulo)
- 8-bit serial interface
- 2-channel complete CMOS operational amplifier
  (Two operation modes available: NORMAL and SAMPLE/HOLD)
- 4-channel multiplexer input comparator
- 6-bit D/A converter
- Feasible to realize the 4-channel 6-bit A/D conversion function using the above-mentioned comparator and D/A converter
- LCD controller/driver
  (14SEGMENT x 2COMMON, 13SEGMENT x 3COMMON, and 12SEGMENT x 4COMMON)
- Zero-cross detection selectable
- Standby function (Stop/Halt)

USE:

Electronic rice cooker and blood pressure meter, etc.

ORDERING INFORMATION

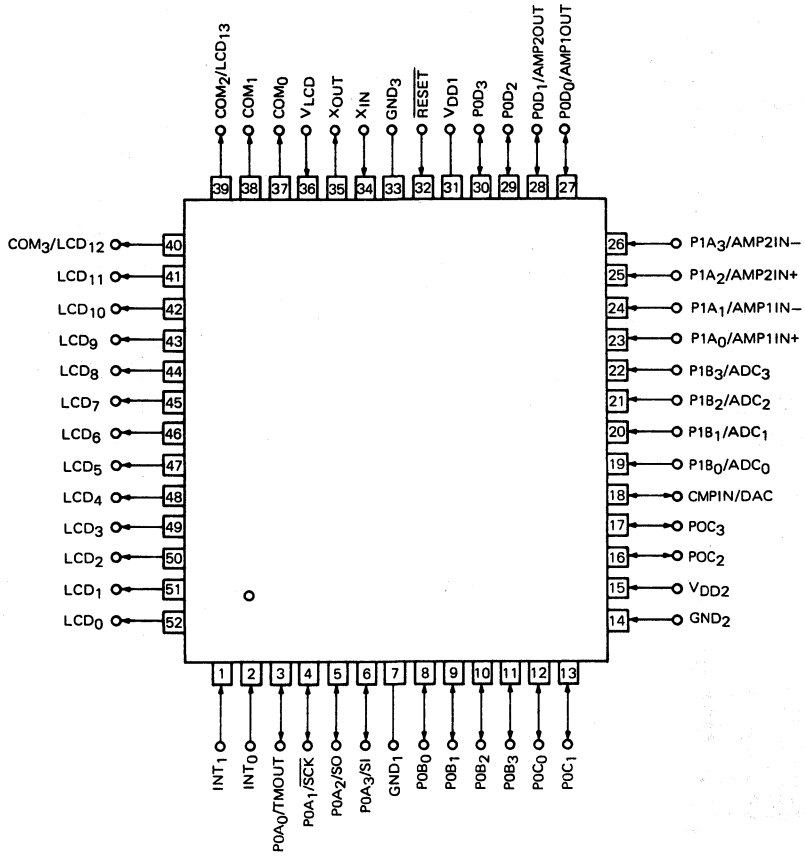
Order Code	Package
μPD17102G-XXX-00	52-pin plastic QFP (bent lead)
μPD17102G-XXX-03	52-pin plastic QFP (straight lead)

OUTLINE OF FUNCTIONS

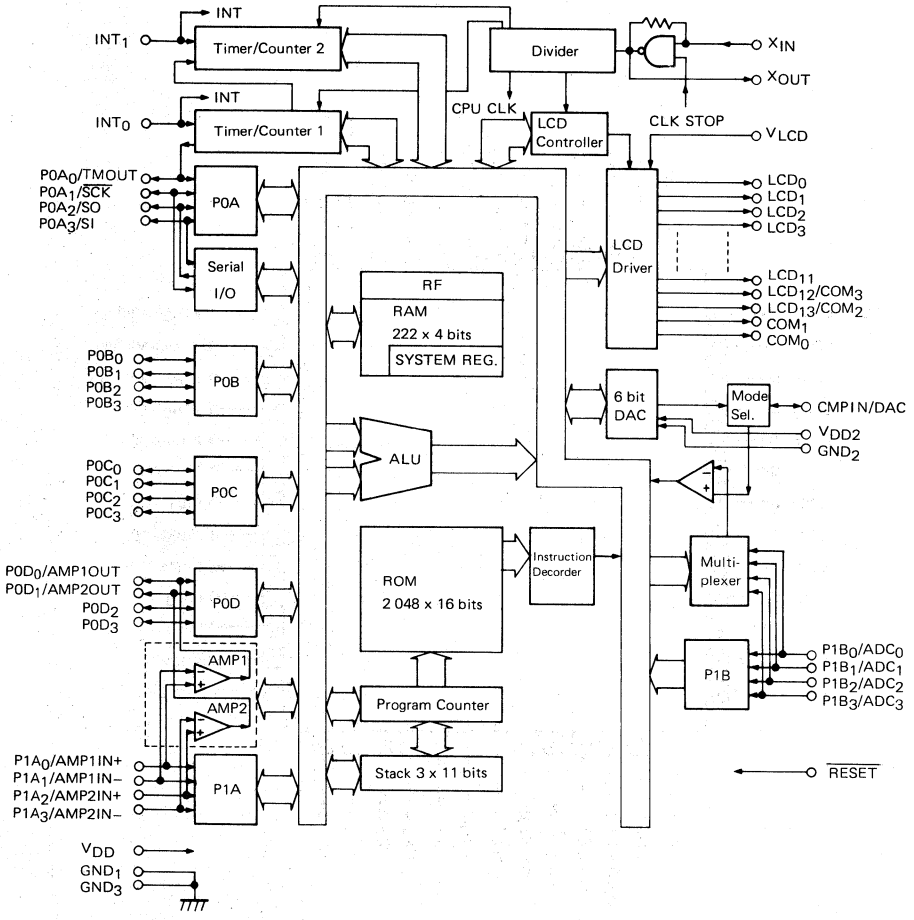
- μPD17000 architecture
- Program memory (ROM) : 4K bytes (2048 x 16 bits)
- Data memory (RAM) : 222 words (222 x 4 bits)
- Stack level : 3 levels
- Instruction cycle : 2 μs (when operated at 5.0 V and 8 MHz)
- Interrupting function : (Internal: 3, and external: 2)
- 8-bit timer/counter : 2 CH (with modulo integrated)
- 8-bit serial interface
- 2-channel complete CMOS operational amplifier
  (Two operation modes available: NORMAL and SAMPLE/HOLD)
- 4-channel input comparator with multiplexer
- 6-bit D/A converter
- Feasible to realize 4-channel, 6-bit A/D conversion function using the above-mentioned comparator and D/A converter
- LCD controller (14SEGMENT x 2COMMON, 13SEGMENT x 3COMMON, and 12SEGMENT x 4COMMON)
- Zero-cross detecting function
- Standby function (STOP/HALT)
- Data/memory low supply voltage holding function
- Oscillator circuit for system clock (ceramic and crystal)
- Single power unit (3.0 to 6.0 V, but 4.5 to 6.0 V when the operational amplifier is used)

2

PIN CONFIGURATION (Top View)



BLOCK DIAGRAM



1. OUTLINE

The μPD17102 is a 4-bit single chip microcontroller which integrates all the following circuits on one chip: 4-bit ALU, program memory (ROM), data memory (RAM), I/O ports, timer/event counter, serial interface, vector interrupt circuit.

This chip using the μPD17000 Series architecture has various built-in peripheral circuits including analog circuits, allowing the user to incorporate it into electrical appliances and intelligent units in a distributed system for home automation.

For program development, NEC supports the in-circuit emulator (IE-17K), so that the user can debug programs easily by using the emulator together with the SE board for each product.

2. PIN FUNCTIONS

2.1 Input/Output Ports

2.1.1 $P0A_0$ to $P0A_3$ (Port 0A): Bi-directional input/output ports

Port 0A is a 4-bit input port (pins from $P0A_0$ to $P0A_3$) with output latch circuits.

This port is mapped to 70H at bank 0 in the data memory space and accessed with normal data memory operation instructions. The direction of input/output is switched for all four bits by the P0AGIO value. Setting P0AGIO to "1" outputs the value stored at 70H of bank 0 to the pin and setting to "0" disables output and sets input mode.

Regardless of the P0AGIO value, the pin status can be read with a data memory reference instruction. The contents of the output latch remain unchanged unless the data at 70H of bank 0 is rewritten.

$P0A_0$ is shared by the timer 1 output pin TMOUT. It operates as TMOUT when PTOUTON in the register file is "0" and in normal input/output mode.

When TMOUT is selected, this pin outputs "1" at time 1 reset and reverses the output each time the timer 1 value matches the contents of the modulo register. At this time, this pin is set in output mode regardless of the P0AGIO value. The pin status at this time can also be read with a data memory reference instruction. The output latch as $P0A_0$ is independent of TMOUT, and therefore data can be written to 70H of bank 0 even if the pin operates as TMOUT and the data is output when PTOUTON is set to "0" while P0AGIO is "1."

$P0A_1$ to $P0A_3$ are shared by $\overline{SCK}$, SO, and SI of the serial interface. The PA0 pin is set in normal input/output mode when the SIOON value in the register file is "0" and used as the SIO pin when it is "1."

In the port 0A input/output format, either of the Nch open/drain input/output or Nch open/drain input/output with a built-in pull-up resistor is selectable by the mask option. In Nch open/drain input/output mode, the port has a 9 V withstanding voltage and is suitable for an interface with a circuit using a different supply voltage. By using the Nch open/drain input/output structure, a 2-wire serial interface can also be used.

When SIOON is "1," data cannot be output to the $\overline{SCK}$ and SO pins as a port. Even if data is transferred to address 70H of bank 0, this data cannot be input to $P0A_1$ to $P0A_3$. At this time, only $P0A_3$ is available.

When the $\overline{SCK}$ pin is in input mode, however, data can be written to the $P0A_1$ output latch.

Table 2-1 Port 0A functions

PTOUTON	SIOON	P0AGIO	Write to bank 0, 70H	Read from bank 0, 70H	Pin function			
					$P0A_0$	$P0A_1$	$P0A_2$	$P0A_3$
0	0	0	All four bits are valid.	Enable. (Pin status)	$P0A_0$ IN	$P0A_1$ IN	$P0A_2$ IN	$P0A_3$ IN
		1	All four bits are valid.		$P0A_0$ OUT	$P0A_1$ OUT	$P0A_2$ OUT	$P0A_3$ OUT
	1	0	Only $P0A_0$ is valid.		$P0A_0$ IN	$\overline{SCK}$	SO	SI
		1	Only $P0A_0$ is valid.		$P0A_0$ OUT			
1	0	0	All four bits are valid		TMOUT	$P0A_1$ IN	$P0A_2$ IN	$P0A_3$ IN
		1	All four bits are valid.			$P0A_1$ OUT	$P0A_2$ OUT	$P0A_3$ OUT
	1	0	Only $P0A_0$ is valid.			$\overline{SCK}$	SO	SI
		1	Only $P0A_0$ is valid.					

Note: If data is written to 70H of bank 0 when SIOON is "1," this data can be written to $P0A_1$ only when the $\overline{SCK}$ pin is in input mode.

2.1.2 $P0B_0$ to $P0B_3$ (port 0B), $P0C_0$ to $P0C_3$ (port 0C): Bi-directional input/output

Ports 0B and 0C are 4-bit input/output pins with output latch circuits: From $P0B_0$ to $P0B_3$ and from $P0C_0$ to $P0C_3$. These ports are mapped to 71H and 72H of bank 0 in the data memory space, respectively and are accessed with normal data memory operation instructions like port 0A. The direction of input/output is switched for all 4-bits by the P0BGIO or P0CGIO value in the register file. Setting the value to "1" outputs the data at 71H or 72H of bank 0 to the corresponding pin and "0" disables the output and sets the input mode. Regardless of the P0BGIO and P0CGIO values, the pin status is read when a data memory reference instruction is executed. At this time, the contents of the output latch remain unchanged.

The input/output format of ports 0B and 0C is the CMOS (push/pull) type.

Table 2-2 Functions of ports 0B and 0C

P0BGIO P0CGIO	Input/output direction of pin	Write to bank 0, 71H or 72H	Read from bank 0, 71H or 72H
0	Input (output disable)	Available	Available (pin status input)
1	Output		

2.1.3 $P0D_0$ to $P0D_3$ (port D): Bi-directional input/output

Port 0D comprises 4-bit input/output pins with output latch circuits. It is mapped to 73H of bank 0 in the data memory space. The input/output direction is switched by the P0DGIO value in the register file.

$P0D_0$ is shared with the AMP1 output pin AMP1OUT, and $P0D_1$ is shared with the AMP2 output pin AMP2OUT. These bits are used in normal input/output mode when the AMP1EN or AMP2EN values in the register file are "0" and as AMP1OUT and AMP2OUT respectively when the values are "1."

When AMP1OUT and AMP2OUT are selected, the pins are used as the AMP1OUT and AMP2OUT output pins, regardless of the P0DGIO value. A data memory reference instruction reads the pin status regardless of the function selected for the pin. At this time, the pin potential is intermediate, the read value is undefined. The μPD17102 reads only at the moment the instruction is executed and disables other input circuits. Therefore, the through current does not flow through the input circuit.

The $P0D_0$ and $P0D_1$ output latch circuits are independent of AMP1OUT and AMP2OUT. Therefore, data can be written to bank 0, 73H by setting AMP1EN and AMP2EN to "1" even if the pins operate as AMP1OUT and AMP2OUT. When P0DGIO is "1," the pins output data as a port by setting AMP1EN and AMP2EN to "0."

The port 0D input/output format is CMOS (push/pull) input/output.

Table 2-3 Port 0D functions

AP1EN AP2EN	P0DGIO	Write to bank 0, 73H	Read from bank 0, 73H	Pin function			
				$P0D_0$	$P0D_1$	$P0D_2$	$P0D_3$
0	0	All four bits are valid.	Enable. Pin status.	$P0D_0$ IN	$P0D_1$ IN	$P0D_2$ IN	$P0D_3$ IN
	1			$P0D_0$ OUT	$P0D_1$ OUT	$P0D_2$ OUT	$P0D_3$ OUT
1	0			AMP1OUT	AMP2OUT	$P0D_2$ IN	$P0D_3$ IN
	1					$P0D_2$ OUT	$P0D_3$ OUT

Note: The AMP output control is selectable for AMP1/2 separately.

2.1.4 $P1A_0$ to $P1A_3$ (port 1A): Input

Port 1A comprises 4-bit input pins.

It is mapped to 70H of bank 1 in the data memory space.

$P1A_0$ and $P1A_1$ are shared with AMP1 non-reverse input (AMP1IN+) and reverse input (AMP1IN−), PI1A and P1A3 are shared with AMP2 non-reverse input (AMP2IN+) and reverse input (AMP2IN−). These pins are not switched and are always connected to both input circuits of the operator amplifier (analog input) and port (digital input).

When used as analog input pins, apply an intermediate potential or AC voltage. If a data memory reference instruction is executed at this time, an undefined value is read. Similar to port 0D, the through current does not flow through the input circuit.

Port 1A has three mask options: With pull-up resistor, with pull-down resistor, and with no built-in resistor. When the pins are used as analog input pins, select the mask option for no built-in resistor. Otherwise, the pins may not operate normally.

Output instructions to the port (data write to 70H in bank 1) are invalid.

Table 2-4 Port 1A function

Read from bank 1, 70H (logical input)	Write to bank 1, 70H	Analog input
Enable (Pin status input) (Undefined at intermediate potential)	Disable	Always connected to AMP input.

2.1.5 $P1B_0$ to $P1B_3$ (port 1B): Input

Port 1B comprises 4-bit input pins.

It is mapped to 71H of bank 1 in the data memory space.

Only one of these pins can be set as the input pin of the non-reserve input from the comparator by ADCCH0 and ADCCH1. For more information, see Section 3.12. Similar to ports 0D and 1A, the pin status of port 1B is read with the data memory reference instruction, regardless of the selected pin function, and the through current does not flow through the input circuit even if the intermediate potential is applied.

Port 1B also has three mask options: With pull-up resistor, with pull-down resistor, and with no built-in resistor. When the pins are used as analog input pins, select the mask option for no built-in resistor. Otherwise, the pins may not operate normally.

Output instructions to port 1B (data write to 71H in bank 1) are invalid.

Table 2-5 Port 1B function

Read from bank 1, 71H (logical input)	Write to bank 1, 71H	Analog input
Enable (Pin status input) (Undefined at intermediate potential)	Disable	Either pin is connected to the comparator input (by ADCCH0 and ADCCH1).

2.2 INT_0, INT_1

INT_0 and INT_1 are interrupt request input pins for which the active rising or falling edge is selectable by IEG_0 and IEG_1. At the rising or falling edge of the INT_0 or INT_1 signal selected by IEG_0 and IEG_1, the interrupt request flag (IRQ0, IRQ1) is set.

To prevent malfunctions from noise, the pins has a built-in noise remover. The status of the pin for which noise is eliminated by the noise remover is read by referencing INT_0 and INT_1 in the register file with the PEEK instruction, so that the pins are simply used as input pins.

In addition, INT_0/INT_1 are the count clock input pins of timer 1/2, respectively, and are used when external clocks are selected as timer count clock sources. When sharing the timer input and INT_0/INT_1 interrupt request input, note that the INT_0/INT_1 interrupt request flag is also set by the clock.

The INT_1 pin is also used to detect zero-cross when ZCROSS in the register file is set to "1."

2.3 CMPIN/DAC, V_{DD2}, GND_2

V_{DD2} and GND_2 are pins used to apply the reference voltage of the built-in 6-bit D/A converter. Apply the V_{DD} potential to V_{DD2} and the GND potential to GND_2. These two pins are separated from V_{DD} and GND and can have separated digital and analog power sources. The applied voltage between the pins is divided into 2^6 steps (64 steps). The analog value corresponding to digital data stored in four bits of 72H and high-order two bits of 73H of bank 1 in the data memory space is the D/A converter output.

To output the D/A converter data from the CMPIN/DAC pin, set DACEN to "1" and CMPEN to "0" in the register file.

To use a comparator, set DACEN to "0" and CMPEN to "1" in the register file. At this time, the CMPIN/DAC pin operates as the reverse input pin of the comparator (CMPIN). Apply a voltage with the same potential as V_{DD} to the V_{DD2} pin. Also apply the same potential to GND_2 pin to minimize the current flowing through the D/A converter which is not used.

When using the 6-bit D/A converter under program control, set DACEN to "1" and CMPEN to "1" in the register file. At this time, D/A converter data is not output externally, but is directly input to the comparator reverse input pin. Therefore, the CMPIN/DAC pin is not used.

Table 2-6 V_{DD2}, GND_2, and CMPIN/DAC functions

DACEN	CMPEN	V_{DD2}	GND_2	CMPIN/DAC	Function
0	0	V_{DD} potential	V_{DD} potential	V_{DD} potential	D/A converter and comparator are not used.
		V_{DD2}	GND_2	High impedance	Initial state when the D/A converter is used **(Note)**.
0	1	V_{DD} potential	V_{DD} potential	CMPIN	When the comparator is used.
1	0	V_{DD2}	GND_2	DAC	When the D/A converter is used.
1	1	V_{DD2}	GND_2	V_{DD} potential	Used as D/A converter

V_{DD} potential indicates that V_{DD} potential is applied externally.

Note: DACEN and CMPEN are set to "0" at reset.

2.4 V_{LCD}

V_{LCD} is a power supply pin for driving the liquid crystal display panel (LCD panel).

Depending on the bias method used, it generates the 1/2 V_{LCD}, 1/3 V_{LCD}, and 2/3 V_{LCD} voltages. When using LCD_0 to LCD_{13} as the output pins, apply the high voltage under the supply voltage (V_{DD}).

2.5 LCD_0 to LCD_{11}, COM_3/LCD_{12}, COM_2/LCD_{13}, COM_1, COM_0

LCD_0 to LCD_{11}, COM_3, LCD_{12}, COM_2/LCD_{13}, COM_1, and COM_0 are LCD panel segment driver pins used to select drive method, such as 14-segment 2-common, 13-segment 3-common, 12-segment 4-common.

LCD_0 to LCD_{13} are used as output pins when LCDEN in the register file is "0." At this time, COM_1 and COM_0 are not used.

For more information on the LCD panel, see Section 3.10.

Table 2-7 LCD_0 to LCD_{11}, COM_3/LCD_{12}, COM_2/LCD_{13}, COM_1, and COM_0 functions

LCDEN	LCD_0 to LCD_{11}, COM_3/LCD_{12}, COM_2/LCD_{13}	COM_1, COM_0
0	All are output pins.	Not used
1	LCD drivers and common drivers	Common drivers

2.6 X_{IN}, X_{OUT}

X_{IN} and X_{OUT} are pins used to connect the oscillation vibrator in the system clock generator.

2.7 $\overline{RESET}$

$\overline{RESET}$ is a low-level active reset input pin. The reset has priority over all other operations.

In addition to CPU initial start, this pin is also used to release standby mode.

2.8 V_{DD1}

V_{DD1} is a positive power supply pin.

2.9 GND_1, GND_2

GND_1 and GND_2 are GND potential pins. Wire them so that the same potential is used externally.

2.10 Pin Mask Options

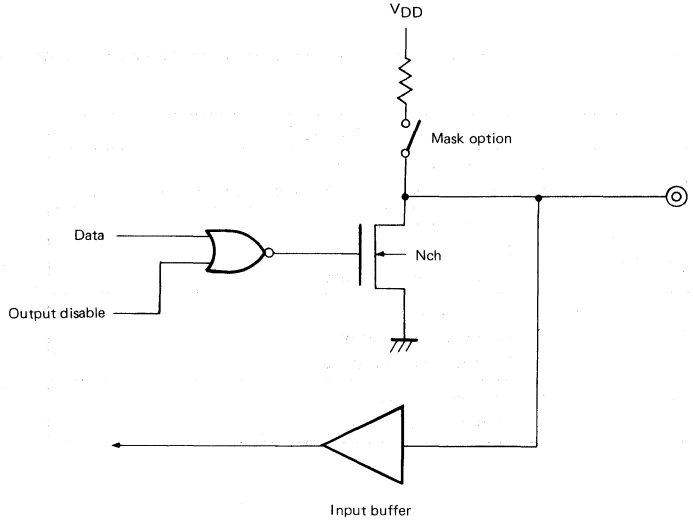
The μPD17102 pins have the mask options listed below. These option can be selected bit according to purpose.

Pin name	Mask option
POA_0 to POA_3	(1) Nch open-drain input/output (2) Nch open-drain plus built-in pull-up resistor input/output
$P1A_0$ to $P1A_3$ $P1B_0$ to $P1B_3$	(1) No built-in resistor (2) Built-in pull-up resistor (3) Built-in pull-down resistor
INT_0 INT_1	(1) No built-in resistor (2) Built-in pull-up resistor (3) Built-in pull-down resistor
$\overline{RESET}$	(1) No built-in resistor (2) Built-in pull-up resistor

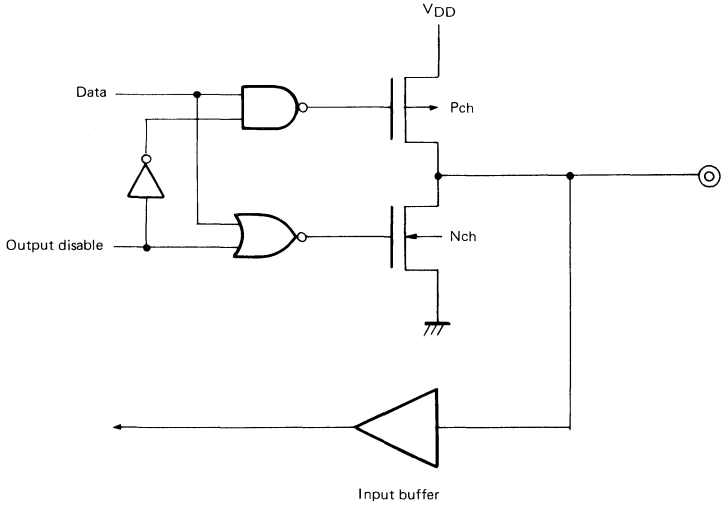
2.11 Pin Input/Output Circuits

The Input/output circuit of each pin of the μPD17102 is shown below in a partly simplified format:

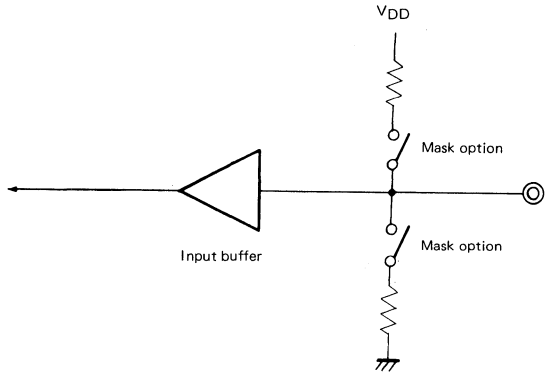
(1) POA_0 to POA_3



(2) POB_0 to POB_3, POC_0 to POC_3, POD_0 to POD_3



(3) $P1A_0$ to $P1A_3$, $P1B_0$ to $P1B_3$, INT_0, INT_1



(4) $\overline{RESET}$

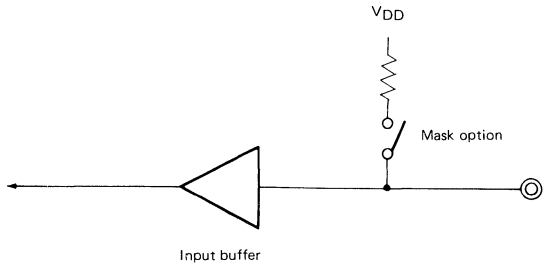


Table 2-8 Digital input/output port pin functions

PIN NAME	I/O	COMBINED USE	FUNCTION	WHEN RESET
$P0A_0$	Input/output	TMOUT	4-bit I/O port (port 0A)	High impedance (P0An input)
$P0A_1$		$\overline{SCK}$		
$P0A_2$		SO		
$P0A_3$		SI		
$P0B_0$ to $P0B_3$	Input/output		4-bit I/O port (port 0B) Large current (15 mA)	High impedance (input)
$P0C_0$ to $P0C_3$	Input/output		4-bit I/O port (port 0C) Large current (15 mA)	High impedance (input)
$P0D_0$	Input/output	AMP1OUT	4-bit I/O port (port 0D) Middle current (10 mA)	High impedance (P0Dn input)
$P0D_1$		AMP2OUT		
$P0D_2$ to $P0D_3$				High impedance (input)
$P1A_0$	Input	AMP1IN+	4-bit input port (port 1A)	Input
$P1A_1$		AMP1IN−		
$P1A_2$		AMP2IN+		
$P1A_3$		AMP2IN−		
$P1B_0$	Input	ADC_0	4-bit input port (port 1B)	Input
$P1B_1$		ADC_1		
$P1B_2$		ADC_2		
$P1B_3$		ADC_3		

Table 2-9 Pins other than port pins

Pin name	Input/output	Shared	Function	At reset
INT_0	Input		Used as both the timer 1 count clock input pin and the external interrupt input pin.	Input
INT_1	Input		Used as the timer 2 count clock input pin and external interrupt input pin. Zero-cross detection function is selectable.	Input
TMOUT	Output	$P0A_0$	Timer 1 output pin	$P0A_0$ input
$\overline{SCK}$	Input/output	$P0A_1$	Serial clock input/output pin	$P0A_1$ input
SO	Output	$P0A_2$	Serial data output pin	$P0A_2$ input
SI	Input	$P0A_3$	Serial data input pin	$P0A_3$ input
AMP1OUT	Output	$P0D_0$	AMP1 output pin	$P0D_0$ input
AMP2OUT		$P0D_1$	AMP2 output pin	$P0D_1$ input
AMP1IN+	Input	$P1A_0$	AMP1 non-reversed input pin	Input
AMP1IN−		$P1A_1$	AMP1 reversed input pin	
AMP2IN+		$P1A_2$	AMP2 non-reversed input pin	
AMP2IN−		$P1A_3$	AMP2 reversed input pin	
ADC_0 to ADC_3	Input	$P1B_0$ to $P1B_3$	Comparator input pin	Input
V_{DD2}	Input		D/A converter reference voltage input pin (high-potential side)	
GND_2	Input		D/A converter reference voltage input pin (low-potential side)	
CMPIN	Input/output	DAC	Used as the D/A converter output pin and comparator input pin.	High impedance
LCD_0 to LCD_{11}	Output		LCD segment driver output pin. Also used as the output port.	Output
COM_3	Output	LCD_{12}	Used as the LCD common driver output and LCD segment driver pin. Also used as an output port.	Output
COM_2		LCD_{13}		
COM_0, COM_1	Output		LCD common driver output pin	Output
V_{LCD}	Input		LCD driver split potential setting pin	Input
$\overline{RESET}$	Input		System reset input pin	Input
V_{DD1}			Positive power supply pin	
GND_1, GND_3			GND potential pin	
X_{IN}, X_{OUT}			System clock oscillator pin	

3. INTERNAL BLOCK

3.1 Program Counter (PC)

The program counter (PC) is an 11-bit binary counter that retains address data of the program memory (ROM).

Fig. 3-1 Program counter configuration

PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0

When the $\overline{\text{RESET}}$ signal goes to low, the PC is set to 0.

Usually, the counter is incremented by one each time an instruction is executed.

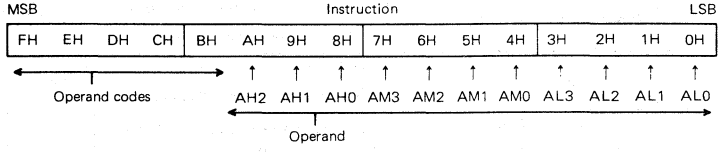
The CALL instruction saves the contents of the counter (return address) to the stack memory then loads the branch destination address to the counter. Return instructions (RET, RETSK, and RETI) load the contents of the stack memory (return address) to the counter. The branch instruction (BR) loads the branch destination address to the counter. The ROM data reference instruction (MOVT) temporarily loads the address at which the data to be referenced is stored to the counter. Take care with the level because the contents of the PC are saved to the stack memory immediately before the address is loaded.

In Fig. 3-2, AHn, AMn, and ALn are addresses indicated by the instruction operand. (See Fig. 3-3.) ARmm is bit n in the address register (ARm) which contains the address to be loaded to the program counter. SP is the stack pointer which points to the contents of the stack memory.

Fig. 3-2 Relationship between instructions and values to be loaded

	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
RET, RETSK, RETI	(SP)	(SP)	(SP)	(SP)	(SP)	(SP)	(SP)	(SP)	(SP)	(SP)	(SP)
BR, CALL	AH2	AH1	AH0	AM3	AM2	AM1	AM0	AL3	AL2	AL1	AL0
BR@AR, CALL@AR, MOVT	1	1	1	AR13	AR12	AR11	AR10	AR03	AR02	AR01	AR00

Fig. 3-3 Instruction word configuration



7. ASSEMBLER RESERVED WORDS

7.1 Mask Option Pseudo Instructions

For coding μPD17102 programs, a mask option must be specified in Assembler source programs with the mask option pseudo instruction.

The following pins require the mask option:

- $P0A_0$, $P0A_1$, $P0A_2$, $P0A_3$
- $P1A_0$, $P1A_1$, $P1A_2$, $P1A_3$
- $P1B_0$, $P1B_1$, $P1B_2$, $P1B_3$
- INT_0, INT_1
- $\overline{RESET}$

7.1.1 OPTION and ENDOP pseudo instructions

From the OPTION pseudo instruction to the ENDOP pseudo instruction is referred to as the mask option definition block. The format of this block is shown below.

Only the six pseudo instructions explained in Section 7.1.2 can be input to the mask option definition block.

Format:

Symbol field	Mnemonic field	Operand field	Comment field
[level:]	OPTION		[comment:]
	⋮		
	ENDPOP		

7.1.2 Mask option definition pseudo instructions

Table 7-1 lists the pseudo instruction that are allowed in the mask option definition block.

An example for defining the mask option is shown below.

Format:

Symbol field	Mnemonic field	Operand field
[level:]	OPTP1A	P1APLUP, P1APLDW, OPEN, OPEN

- OPEN, OPEN → PIA_1 and PIA_0 are open.
- P1APLDW → PIA_2 is pull-down.
- P1APLUP → PIA_3 is pull-up.

Table 7-1 Mask option definition pseudo instructions

Pin name	Mask option pseudo instruction	Number of parameters	Parameter name
$P0A_0$ to $P0A_3$	OPTP0A	4	P0APLUP : Pull up OPEN : Open
$P1A_0$ to $P1A_3$	OPTP1A	4	P1APLUP : Pull up P1APLDW : Pull down OPEN : Open
$P1B_0$ to $P1B_3$	OPTP1B	4	P1BPLUP : Pull up P1BPLDW : Pull down OPEN : Open
INT_0	OPTINT0	1	INT0PLUP : Pull up INT0PLDW : Pull down OPEN : Open
INT_1	OPTINT1	1	INT1PLUP : Pull up INT1PLDW : Pull down OPEN : Open
$\overline{RESET}$	OPTRES	1	RESPLUP : Pull up OPEN : Open

7.2 Reserved Symbols

Table 7-2 lists the symbols defined in the μPD17102 device file. These defined symbols include the control register names, port names, and peripheral device names.

(1) Control registers in register file

The names of the control register assigned to data memory addresses 80H to BFH in bank 0 are defined. These registers are accessible through the window register (WR) with the PEEK and POKE instructions.

(2) Registers and ports in data memory

Registers assigned to data memory addresses 00H to 7FH, and ports and system registers assigned to 70H and after are defined.

(3) Peripheral circuits

Peripheral circuits accessible with the GET and PUT D/A converters are defined.

Table 7-2 List of reserved symbols (1/4)

NAME	ATTRIBUTE	VALUE	R/W	DESCRIPTION
DBF3	MEM	0.0CH	R/W	Bit 15 to bit 12 of data buffer
DBF2	MEM	0.0DH	R/W	Bit 11 to bit 8 of data buffer
DBF1	MEM	0.0EH	R/W	Bit 7 to bit 4 of data buffer
DBF0	MEM	0.0FH	R/W	Bit 3 to bit 0 of data buffer
AR3	MEM	0.74H	R	Bit 15 to bit 12 of address register
AR2	MEM	0.75H	R	Bit 11 to bit 8 of address register
AR1	MEM	0.76H	R/W	Bit 7 to bit 4 of address register
AR0	MEM	0.77H	R/W	Bit 3 to bit 0 of address register
WR	MEM	0.78H	R/W	Window register
BANK	MEM	0.79H	R/W	Bank register
IXH	MEM	0.7AH	R/W	Bit 11 to bit 8 of index register
MPH	MEM	0.7AH	R/W	Bit 7 to bit 4 of memory pointer
MPE	FLG	0.7AH.3	R/W	Memory pointer enable flag
IXM	MEM	0.7BH	R/W	Bit 7 to bit 4 of index register
MPL	MEM	0.7BH	R/W	Bit 3 to bit 0 of memory pointer
IXL	MEM	0.7CH	R/W	Bit 3 to bit 0 of index register
RPH	MEM	0.7DH	R/W	Bit 7 to bit 4 of register pointer
RPL	MEM	0.7EH	R/W	Bit 3 to bit 0 of register pointer
PSW	MEM	0.7FH	R/W	Program status word
BCD	FLG	0.7EH.0	R/W	BCD operation flag
CMP	FLG	0.7FH.3	R/W	Compare flag
CY	FLG	0.7FH.2	R/W	Carry flag
Z	FLG	0.7FH.1	R/W	Zero flag
IXE	FLG	0.7FH.0	R/W	Index register enable flag
LCDD0	MEM	0.60H	R/W	LCD segment 0
LCDD1	MEM	0.61H	R/W	LCD segment 1
LCDD2	MEM	0.62H	R/W	LCD segment 2
LCDD3	MEM	0.63H	R/W	LCD segment 3
LCDD4	MEM	0.64H	R/W	LCD segment 4
LCDD5	MEM	0.65H	R/W	LCD segment 5
LCDD6	MEM	0.66H	R/W	LCD segment 6

Table 7-2 List of reserved symbols (2/4)

NAME	ATTRIBUTE	VALUE	R/W	DESCRIPTION
LCDD7	MEM	0.67H	R/W	LCD segment 7
LCDD8	MEM	0.68H	R/W	LCD segment 8
LCDD9	MEM	0.69H	R/W	LCD segment 9
LCDD10	MEM	0.6AH	R/W	LCD segment 10
LCDD11	MEM	0.6BH	R/W	LCD segment 11
LCDD12	MEM	0.6CH	R/W	LCD segment 12
LCDD13	MEM	0.6DH	R/W	LCD segment 13
P0A0	FLG	0.70H.0	R/W	Port 0A bit 0
P0A1	FLG	0.70H.1	R/W	Port 0A bit 1
P0A2	FLG	0.70H.2	R/W	Port 0A bit 2
P0A3	FLG	0.70H.3	R/W	Port 0A bit 3
P0B0	FLG	0.70H.0	R/W	Port 0B bit 0
P0B1	FLG	0.71H.1	R/W	Port 0B bit 1
P0B2	FLG	0.71H.2	R/W	Port 0B bit 2
P0B3	FLG	0.71H.3	R/W	Port 0B bit 3
P0C0	FLG	0.71H.0	R/W	Port 0C bit 0
P0C1	FLG	0.72H.1	R/W	Port 0C bit 1
P0C2	FLG	0.72H.2	R/W	Port 0C bit 2
P0C3	FLG	0.72H.3	R/W	Port 0C bit 3
P0D0	FLG	0.73H.0	R/W	Port 0D bit 0
P0D1	FLG	0.73H.1	R/W	Port 0D bit 1
P0D2	FLG	0.73H.2	R/W	Port 0D bit 2
P0D3	FLG	0.73H.3	R/W	Port 0D bit 3
P1A0	FLG	1.70H.0	R	Port 1A bit 0
P1A1	FLG	1.70H.1	R	Port 1A bit 1
P1A2	FLG	1.70H.2	R	Port 1A bit 2
P1A3	FLG	1.70H.3	R	Port 1A bit 3
P1B0	FLG	1.71H.0	R	Port 1B bit 0
P1B1	FLG	1.71H.1	R	Port 1B bit 1
P1B2	FLG	1.71H.2	R	Port 1B bit 2
P1B3	FLG	1.71H.3	R	Port 1B bit 3
DARH	MEM	1.72H	R/W	D/A conversion data bit 4 and bit 5

Table 7-2 List of reserved symbols (3/4)

NAME	ATTRIBUTE	VALUE	R/W	DESCRIPTION
DARL	MEM	1.73H	R/W	D/A conversion data bit 3 to bit 0
DACCMP	FLG	1.73H.0	R	Result of comparison
SP	MEM	0.81H	R/W	Stack pointer
SIOTS	FLG	0.82H.3	R/W	SIO operating status
SIOHIZ	FLG	0.82H.2	R/W	Status of SO pin
SIOCK1	FLG	0.82H.1	R/W	Selection of serial clock
SIOCK0	FLG	0.82H.0	R/W	Selection of serial clock
INT1	FLG	0.8FH.2	R	Status of INT_1 pin
INT0	FLG	0.8FH.1	R	Status of INT_0 pin
ZCROSS	FLG	0.8FH.0	R/W	Status of zero-cross detection circuit
TM1EN	FLG	0.91H.3	R/W	Timer 1 permit
TM1RES	FLG	0.91H.2	R/W	Timer 1 reset
TM1CK1	FLG	0.91H.1	R/W	Timer 1 clock selection
TM1CK0	FLG	0.91H.0	R/W	Timer 1 clock selection
TM2EN	FLG	0.92H.3	R/W	Timer 2 permit
TM2RES	FLG	0.92H.2	R/W	Timer 2 reset
TM2CK1	FLG	0.92H.1	R/W	Timer 2 clock selection
TM2CK0	FLG	0.92H.0	R/W	Timer 2 clock selection
IEG1	FLG	0.9FH.2	R/W	INT1 edge selection
IEG0	FLG	0.9FH.1	R/W	INT0 edge selection
AMP1EN	FLG	0.A1H.3	R/W	AMP1 permit
AMP1MD2	FLG	0.A1H.2	R/W	Mode selection
AMP2MD1	FLG	0.A2H.1	R/W	Be sure to write "0"
AMP2MD0	FLG	0.A2H.0	R/W	SAMPLE-HOLD selection
CMPEN	FLG	0.A3H.3	R/W	Comparator permit
DACEN	FLG	0.A3H.2	R/W	D/A converter permit
ADCCH1	FLG	0.A3H.1	R/W	Comparator input selection
ADCCH0	FLG	0.A3H.0	R/W	Comparator input selection
P0DGIO	FLG	0.A7H.3	R/W	Port 0D I/O selection
P0DGIO	FLG	0.A7H.2	R/W	Port 0C I/O selection
P0BGIO	FLG	0.A7H.1	R/W	Port 0B I/O selection
P0AGIO	FLG	0.A7H.0	R/W	Port 0A I/O selection

Table 7-2 List of reserved symbols (4/4)

NAME	ATTRIBUTE	VALUE	R/W	DESCRIPTION
IPTM2	FLG	0.AEH.1	R/W	INTTM2 permit flag
IP1	FLG	0.AEH.0	R/W	INT1 permit flag
IPSIO	FLG	0.AFH.3	R/W	INTSI0 permit flag
IP0	FLG	0.AFH.2	R/W	INT0 permit flag
IPTM1	FLG	0.AFH.1	R/W	INTTM1 permit flag
LCDOFF	FLG	0.B1H.3	R/W	LCD segment/port selection
LCDMD2	FLG	0.B1H.2	R/W	LCD mode selection
LCDMD1	FLG	0.B1H.1	R/W	LCD mode selection
LCDMD0	FLG	0.B1H.0	R/W	LCD mode selection
LCDEN	FLG	0.B2H.3	R/W	ICD segment output permit
PTOUTON	FLG	0.B7H.0	R/W	PTOUT output permit
SIOON	FLG	0.B7H.1	R/W	SIO output permit
IRQTM2	FLG	0.BEH.1	R/W	INTTM2 interrupt request
IRQ1	FLG	0.BEH.0	R/W	INT1 interrupt request
IRQSIO	FLG	0.BFG.3	R/W	INTSIO interrupt request
IRQ0	FLG	0.BFH.2	R/W	INT0 interrupt request
IRQTM1	FLG	0.BFG.1	R/W	INTTM1 interrupt request
DBF	DAT	0FH	R/W	GET/PUT instruction operand
IX	DAT	01H	R/W	Index register
AR	DAT	00H	R/W	Address register
SIOSFR	DAT	01H	R/W	SIO register
TM1M	DAT	02H	W	Timer 1 modulo register
TM2M	DAT	03H	W	Timer 2 modulo register
TMC	DAT	41H	R	Timer count register

Note: "W. XYH. Z" in the value field indicates

W ..... Bank
X ..... Row address
Y ..... Colum address
Z ..... Bit

8. INSTRUCTION SET

Table 8-1 List of instruction sets

b14 to b11 \ b15		0	1
BIN	HEX		
0000	0	ADD r, m	ADD m, #i
0001	1	SUB r, m	SUB m, #i
0010	2	ADDC r, m	ADDC m, #i
0011	3	SUBC r, m	SUBC m, #i
0100	4	AND r, m	AND m, #i
0101	5	XOR r, m	XOR m, #i
0110	6	OR r, m	OR m, #i
01111	7	INC AR INC IX MOVT DBF, @AR BR @AR CALL @AR RET RETSK EI DI RETI PUSH AR POP AR GET DBF PUT p, DBF PEEK WR, RA POKE RA, WR RORC r STOP s HALT h NOP	
1000	8	LD r, m	ST m, r
1001	9	SKE m, #i	SKGE m, #i
1010	A	MOV @r, m	MOV m, @r
1011	B	SKNE m, #i	SKLT m, #i
1100	C	BR addr	CALL addr
1101	D		MOV m, #i
1110	E		SKT m, #n
1111	F		SKF m, #n

Table 8-2 List of INSTRUCTIONS

Legends

M : One of data memory specified by [(BANK), m]
m : Data memory address specified by [mH,mL] of each bank
m_H : Date memory address high (row address) : 3 bits
m_L : Data memory address low (column address) : 4 bits
R : One of general register specified by [(RP) ,r]
r : General register address low (column address) : 4 bits
RP : General register pointer
RF : One of register file specified by rf
rf : Register file address specified by [rfH,rfL]
rf_H : Register file address high (row address) : 3 bits
rf_L : Register file address low (column address) : 4 bits
AR : Address register
IX : Index register
IXE : Index register enable flag
DBF : Data buffer
WR : Window register
MP : Memory pointer
MPE : Memory pointer enable flag
PE : Peripheral
p : Peripheral address
p_H : Peripheral address high (row address) : 3 bits
p_L : Peripheral address low (column address) : 4 bits

PC : Program counter
SP : Stack pointer
STACK : Stack specified by (SP)
BANK : Bank register
(AR) rom : One of program memory data specified by (AR)
INTEF : Interrupt enable flag
i : Immediate data : 4 bits
n : Bit position : 4 bits
addr : One of program memory address : 11 bits
a_H : Program memory address high : 3 bits
a_M : Program memory address middle : 4 bits
a_L : Program memory address low : 4 bits
CY : Carry flag
CMP : Compare flag
s : Stop release condition
h : Halt release condition
[ ] : Address of M,R.RF
( ) : Contents of M,R.RF,AR,IX,DBF,WR,PE

Instruction group	Mnemonic	Operand	Function	Operation	Machine code			
					Opration code	3bits	4bits	4bits
Addition	ADD	r,m	Add memory to register	R, CY← (R) + (M)	00000	m_H	m_L	r
		m, #i	Add immediate data to memory	M, CY← (M) +i	10000	m_H	m_L	i
	ADDC	r,m	Add memory to register with carry	R, CY← (R) + (M) + (CY)	00010	m_H	m_L	r
		m, #i	Add immediate data to memory with carry	R, CY← (M) +i← (CY)	10010	m_H	m_L	i
	INC	AR	Increment address register	AR←AR+1	00111	000	1001	0000
		IX	Increment index register	IX←IX+1	00111	000	1000	0000
Subtraction	SUB	r,m	Subtract memory from register	R, CY← (R) − (M)	00001	m_H	m_L	r
		m, #i	Subtract immediate data from memory	M, CY← (M) −i	10001	m_H	m_L	i
	SUBC	r,m	Subtract memory from register with borrow	R, CY← (R) − (M) − (CY)	00011	m_H	m_L	r
		m, #i	Subtract immediate data from memory with borrow	M, CY← (M) −i− (CY)	10011	m_H	m_L	i
Comparison	SKE	m, #i	Skip if memory equal to immediate data	M−i,skip if zero	01001	m_H	m_L	i
	SKGE	m, #i	Skip if memory greater than or equal to immediate data	M−i,skip if not borrow	11001	m_H	m_L	i
	SKLT	m, #i	Skip if memory less than immediate data	M−i,skip if borrow	11011	m_H	m_L	i
	SKNE	m, #i	Skip if memory not equal to immediate data	M−i,skip if not zero	01011	m_H	m_L	i
Logical operation	AND	m, #i	Logical AND of memory and immediate data	M← (M) AND i	10100	m_H	m_L	i
		r,m	Logical AND of register and memory	R← (R) AND (M)	00100	m_H	m_L	r
	OR	m, #i	Logical OR of memory and immediate data	M← (M) OR i	10110	m_H	m_L	i
		r,m	Logical OR of register and memory	R← (R) OR (M)	00110	m_H	m_L	r
	XOR	m, #i	Logical XOR of memory and immediate data	M← (M) XOR i	10101	m_H	m_L	i
		r,m	Logical XOR of register and memory	R← (R) XOR (M)	00101	m_H	m_L	r
Transfer	LD	r,m	Load memory to register	R← (M)	01000	m_H	m_L	r
	ST	m,r	Store register to memory	(M) ←R	11000	m_H	m_L	r
	MOV	@r,m	Move memory to destination memory referring to register	if MPE=1, [(MP),(R)]←(M) if MPE=0, [(m_H),(R)]←(M)	01010	m_H	m_L	r
		m,@r	Move source memory referring to register to memory	if MPE=1, M←[(MP),(R)] if MPE=0, M←[(m_H),(R)]	11010	m_H	m_L	r
		m, #i	Move immediate data to memory	M←i	11101	m_H	m_L	i
	MOVT	DBF, @AR	Move ROM data from the address specified in AR to DBF	sp←(sp)−1,STACK←PC DBF←(AR) rom, PC←STACK,sp←(sp)+1	00111	000	0001	0000
	PUSH	AR	Decrement SP,then move AR to stack top	SP←(SP)−1,STACK←AR	00111	000	1101	0000
	POP	AR	Move stack top to AR,then increment SP	AR←STACK,SP←SP+1	00111	000	1100	0000
	PEEK	WR,RA	Get RA from RF through WR	WR←(RF)	00111	rf_H	0011	rf_L

Instruction group	Mnemonic	Operand	Function	Operation	Machine code			
					Opration code	3bits	4bits	4bits
Transfer	POKE	RA,WR	Put data on WR into RA of RF	(RF)←WR	00111	rf_H	0010	rf_L
	GET	DBF,p	Get peripheral data to DBF	DBF←p	00111	p_H	1011	p_L
	PUT	p,DBF	Put data in DBF to peripheral	p←DBF	00111	p_H	1010	p_L
Decision	SKT	m, #n	Test memory bits, then skip if all bits specified are true	CMP←0 skip if M(N) = all"1"	11110	m_H	m_L	n
	SKF	m, #n	Test memory bits, then skip if all bits specified are false	CMP←0 skip if M(N) = all"0"	11111	m_H	m_L	n
Branch	BR	addr	Jump to the address	PC←ADDR	01100	a_H	a_M	a_L
		@AR	Jump to the address specified in AR	PC←AR	00111	000	0100	0000
Shift	RORC	r	Rotate register right with carry	(CY)→(R)→CY	00111	000	0111	r
Subroutine	CALL	addr	Call subroutine	SP←(SP) − 1 STACK←((PC) + 1), PC←ADDR	11100	a_H	a_M	a_L
		@AR	Call subroutine specified in AR	SP←(SP) − 1, STACK←((PC) + 1), PC←(AR)	00111	000	0101	0000
	RET		Return to main routine from subroutine	PC←(STACK),SP←(SP) + 1	00111	000	1110	0000
	RETSK		Return to main routine from subroutine,then skip unconditionary	PC←(STACK),SP←(SP) + 1 and skip	00111	001	1110	0000
	RETI		return to main routine from interrupt service routine	PC←(STACK),SP←(SP) + 1 BANK←(interrupt stack)	00111	100	1110	0000
Interrupt	EI		Enable interrupt	INTE flag←1	00111	000	1111	0000
	DI		Disable interrupt	INTE flag←0	00111	001	1111	0000
Others	STOP	s	Stop clock	STOP	00111	010	1111	s
	HALT	h	Halt the CPU,restart by condition H	HALT	00111	011	1111	h
	NOP		No operation	No operation	00111	100	1111	0000

9. ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (T_a = 25 °C)

Supply Voltage	V_{DD}	−0.3 to +7.0	V		
Input Voltage	V_I	−0.3 to V_{DD} +0.3	V	P0A	(1)
		−0.3 to +11	V		(2)
		−0.3 to V_{DD} + 0.3	V	All pins other than P0A	
Output Voltage	V_O	−0.3 to V_{DD} +0.3	V	P0A	(1)
		−0.3 to +11	V		(2)
		−0.3 to V_{LCD} +0.3	V	Segment/common pins	
		−0.3 to V_{DD} +0.3	V	Pins other than above	
High-Level Output Current	I_{OH}	−5	mA	1 pin	
		−20	mA	Total of all pins	
Low-Level Output Current	I_{OL}	15	mA	1 pin	P0A, P0D
		30	mA		P0B, P0C
		100	mA	Total of all pins	
Operating Temperature	T_{opt}	−40 to +85	°C		
Storage Temperature	T_{stg}	−65 to +150	°C		
Power Consumption	P_d	190	mW	T_a = 85 °C	

Remarks: 1. N-ch open/drain output plus built-in pull-up resistor output
2. N-ch open/drain input/output

CAPACITY (T_a = 25 °C, V_{DD} = 0 V)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Input Capacity	C_{IN}			15	pF	f = 1 MHz Pins other than those measured: 0 V
Output Capacity	C_{OUT}			15	pF	
Input/Output Capacity	C_{IO}			15	pF	

DC CHARACTERISTICS (T_a = −40 to +85 °C, V_{DD} = 3.0 to 6.0 V)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION	
High-Level Input Voltage	V_{IH1}	0.8 V_{DD}		9	V	At SI or $\overline{SCK}$ input	
	V_{IH2}	0.7 V_{DD}		9	V	At P0A input	
	V_{IH3}	0.8 V_{DD}		V_{DD}	V	INT_1, INT_1, $\overline{RESET}$	
	V_{IH4}	0.7 V_{DD}		V_{DD}	V	Pins other than above	
Low-Level Input Voltage	V_{IL1}	0		0.2 V_{DD}	V	SI, $\overline{SCK}$, INT_0, INT_1, $\overline{RESET}$	
	V_{IL2}	0		0.3 V_{DD}	V	Pins other than above	
High-Level Output Voltage	V_{OH}	V_{DD}−2.0	V_{DD}−0.4		V		V_{DD} = 4.5 to 6.0 V I_{OH} = −1 mA
		V_{DD}−1.0	V_{DD}−0.04		V		I_{OH} = −100 μA
Low-Level Output Voltage	V_{OL}		0.85	2.0	V	P0B, P0C	V_{DD} = 4.5 to 6.0 V I_{OL} = 15 mA
			0.06	0.5	V		I_{OL} = 600 μA
			0.85	2.0	V	P0A, P0D	V_{DD} = 4.5 to 6.0 V I_{OL} = 10 mA
			0.15	0.4	V		V_{DD} = 4.5 to 6.0 V I_{OL} = 1.6 mA
			0.04	0.5	V		I_{OL} = 400 μA
High-Level Input Leak Current	I_{LIH1}			3	μA	Other than XI and XO	V_{IN} = V_{DD}
	I_{LIH2}			10	μA	XI, XO	V_{IN} = V_{DD}
	I_{LIH3}			10	μA	P0A (3)	V_{IN} = 9 V
Low-Level Input Leak Current	I_{LIL}			−3	μA	Other than XI and XO	V_{IN} = 0 V
				−10	μA	XI, XO	V_{IN} = 0 V
High-Level Output Leak Current	I_{LOH1}			3	μA		V_{OUT} = V_{DD}
	I_{LOH2}			10	μA	P0A (3)	V_{OUT} = 9 V
Low-Level Output Leak Current	I_{LOL}			−3	μA		V_{OUT} = 0 V
Input pin with built-in resistor (pull up/pull down)		35	65	110	kΩ	INT0, INT1, P1A, P1B	
Input pin with built-in resistor (pull up)		35	65	110	kΩ	$\overline{RESET}$	
Input pin with built-in resistor (pull down)		7	15	26.5	kΩ	P0A	
Supply Current (4)	I_{DD1}		1500	4500	μA	Operation mode	V_{DD} = 5 V ± 10 % f_{CC} = 8 MHz
			250	750	μA		V_{DD} = 3 V ± 10 % f_{CC} = 2 MHz
	I_{DD2}		550	1600	μA	Halt mode	V_{DD} = 5 V ± 10 % f_{CC} = 8 MHz
			110	330	μA		V_{DD} = 3 V ± 10 % f_{CC} = 2 MHz
	I_{DD3}		0.1	10	μA	Stop mode	V_{DD} = 5 V ± 10 %
			0.1	5	μA		V_{DD} = 3 V ± 10 %

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION	
V_{LCD} Voltage Range	V_{LCD}	3.0		V_{DD}	V		
Common Output Impedance (5)	R_{COM}		40		kΩ		V_{DD} = 4.5 to 6.0 V
Segment Output Impedance (5)	R_{SEG1}		40		kΩ	At LCD drive	V_{DD} = 4.5 to 6.0 V
	R_{SEG2}		5		kΩ	At port operation	Total output of all segment pins Current 2 mA or less $V_{DD} = V_{LCD}$ = 4.5 to 6.0 V
Resistance Between V_{LCD} and GND	R_{VLC}		100		kΩ	When normal	
			3.0		kΩ	When switching	

Remarks: **3.** When N-ch open/drain input/output is selected

4. The current that flows through the built-in pull-up or pull-down resistor is excluded

5. 3.5 kΩ (typ.) when switching between the common and segment output.

AMPLIFIER CHARACTERISTICS (T_a = −40 = +85 °C, V_{DD} = 4.5 to 6.0 V)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Input Offset Voltage	V_{OS}		±6	±18	mV	Normal amplifier mode
In-phase Input Voltage	V_{ICM}	0.0		3.6	V	V_{DD} = 5.0 V
Output Voltage Range	V_{OUT}	0.12		4.8	V	V_{DD} = 5.0 V, I_{OUT} = 0 μA
Unity Gain Frequency	f_O		1.5		MHz	
Large Amplitude Gain	A_V		85		dB	V_{DD} = 5.0 V
Output Current	I_{OUT}	−50		100	μA	V_{DD} = 5.0 V
CMRR			75		dB	
SVRR			−60		dB	
Through Rate		1.0			V/μs	
Hold Time	t_{SAMP}		0.05		ms	Sample/hold amplifier mode
Input/Output Voltage Error	V_{DIF}		±6	±18	mV	Sample/hold amplifier mode
Input Voltage Range	V_{IN}		0.12	2.5	V	Sample/hold amplifier mode
Supply Current	I_{AMP}		230	500	μA	

COMPARATOR CHARACTERISTICS (T_a = −40 to +85 °C, V_{DD} = 4.5 to 6.0 V)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Input Voltage Range	V_{IN}	V_{SS}		V_{DD}	V	
Response Speed (6)	t_{COMP}	2			IC	
Power Consumption	V_{COMP}		100		μA	V_{DD} = 5.0 V
Absolute Accuracy	V_{IT}		±8.0	±15.0	mV	
Input Resolution	V_{RE}		3.0		mV	

D/A CONVERTER CHARACTERISTICS (T_a = −40 to +85 °C, V_{DD} = 4.5 to 6.0 V, V_{REFH} = V_{DD}, V_{REFL} = 0 V)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Resolution		6	6	6	Bit	
Linearity				±0.5	LSB	
D/A Conversion Time (6)	t_{CONV}	2			IC	At no output load
DAC Current	I_{DAC}		220	390	μA	
A/D Conversion Time (6)		4			IC	

Remarks 6: IC indicates "instruction cycle".

ZERO-CROSS CHARACTERISTICS (T_a = −40 to +85 °C, V_{DD} = 4.5 to 6.0 V)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Detection Input Level	V_{ZX}	0.8	3.0		V_{P-P}	Input AC
Accuracy	A_{ZX}		±120		mV	50/60 Hz
Detection Input Frequency	f_{ZX}	0.04	1		kHz	

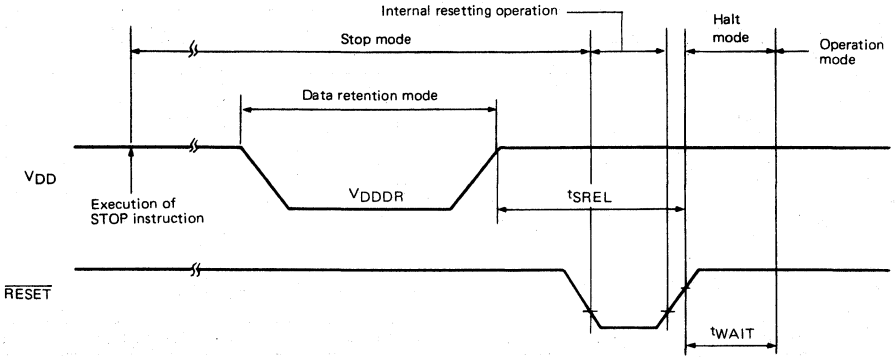
DATA MEMORY DATA RETENTION CHARACTERISTICS AT LOW SUPPLY VOLTAGE IN STOP MODE (T_a = −40 to +85 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Data Retention Supply Voltage	V_{DDDR}	2.0		6.0	V	
Data Retention Supply Current	I_{DDDR}		0.1	5.0	μA	V_{DDDR} = 2.0 V
Release Signal Set Time	t_{SREL}	0			μs	
Wait Time for Stable Oscillation	t_{WAIT}		$2^{19}/fx$		ms	Release by $\overline{\text{RESET}}$ (7)
			(8)		ms	Release by interrupt request

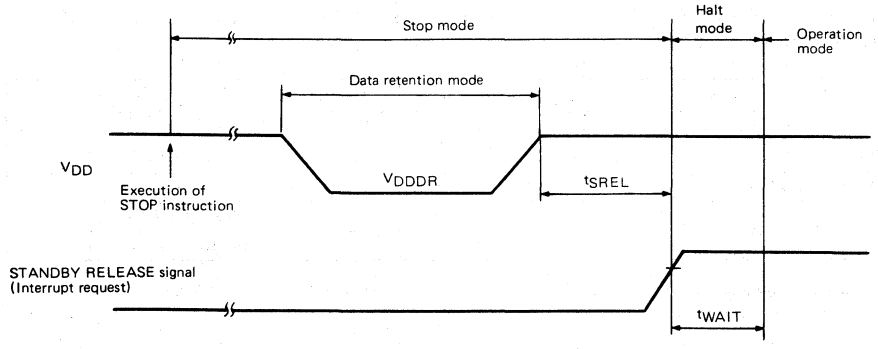
Remarks: 7. fx indicates the oscillator frequency.

8. According to the timer 2 value.

Data Retention Timing (Stop Mode Release by Reset)



Data Retention Timing (Stand-by Release Signal: Stop Mode Release)

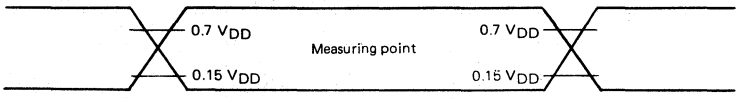


AC CHARACTERISTICS (T_a = −40 to +85 °C, V_{DD} = 3.0 to 6.0 V)

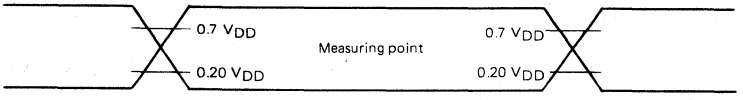
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION	
Internal Clock Cycle Time	t_{CY}	2		30	μs	V_{DD} = 4.5 to 6.0 V	
		8		30	μs		
Event Input Frequency	f_{PO}	0		1000	kHz	duty = 50 %	V_{DD} = 4.5 to 6.0 V
		0		350	kHz		
Event Input Rising/Falling Time	t_{POR} t_{POF}			0.1	μs	Excluding zero-cross mode	
Event Input High/Low Level Width	t_{POH} t_{POL}	0.5			μs	V_{DD} = 4.5 to 6.0 V	
		1.45			μs		
$\overline{SCK}$ Input Cycle Time (9)	t_{KCY}	2.0			μs	At data input	V_{DD} = 4.5 to 6.0 V
		10.0			μs	At data output	
		5.0			μs	At data input	
		13.0			μs	At data output	
$\overline{SCK}$ Input High/Low Level Width (9)	t_{KH} t_{KL}	1.0			μs	At data input	V_{DD} = 4.5 to 6.0 V
		5.0			μs	At data Output	
		2.5			μs	At data input	
		6.5			μs	At data Output	
SI Setup Time (to $\overline{SCK}$↑)	t_{SIK}	100			μs		
SI Hold Time (to $\overline{SCK}$↑)	t_{KSI}	100			μs		
$\overline{SCK}$↓ → SO output delay time (9)	t_{KSO}			4.5	μs	Cp = 100 pF	
INT high/low level width	t_{IOH} t_{IOL}	10			μs		
$\overline{RESET}$ low level width	t_{RSL}	10			μs		

Remarks 9: For SI, SO and $\overline{SCK}$ pins, the N-ch open/drain output plus built-in pull-up resistor input/output.

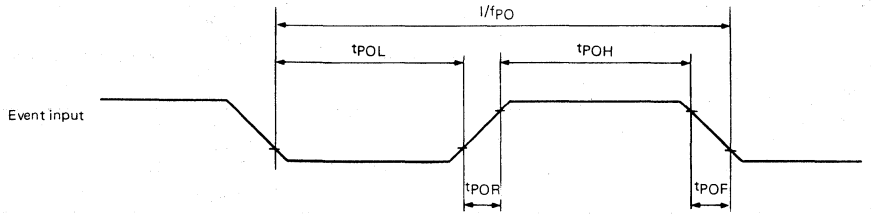
AC Timing Measuring Point (INT_0, INT_1, SI, $\overline{SCK}$ and SO Pins)



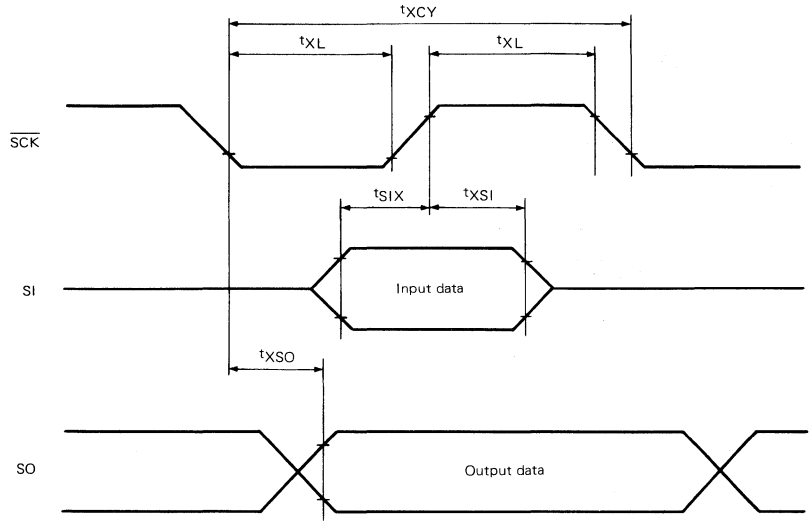
AC Timing Measuring Point (Pins other than INT_0, INT_1, SI, $\overline{SCK}$ SO)



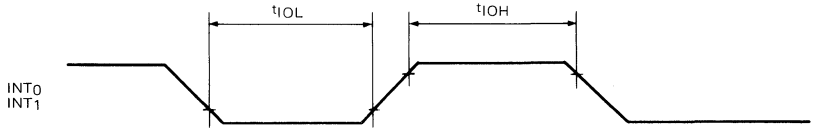
Event Input Timing



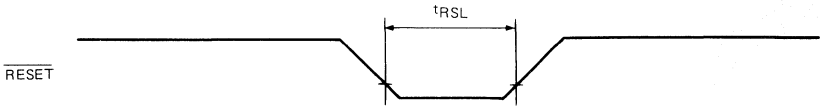
Serial Transfer Timing



INT Input Timing



$\overline{\text{RESET}}$ Input Timing



10. RECOMMENDED SOLDERING CONDITIONS

The following conditions (see table below) must be met when soldering this product.

Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

TYPES OF SURFACE MOUNT DEVICE

For more details, refer to our document "SMT MANUAL" (IEI-1207).

μPD17102G

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak package's surface temperature : 230 °C or below, Reflow time : 30 seconds or below (210 °C or higher), Number of reflow process : 1, Exposure limit* : None	IR30-00
VPS	Peak package's surface temperature : 215 °C or below, Reflow time : 40 seconds or below (200 °C or higher), Number of reflow process : 1, Exposure limit* : None	VP15-00
Wave soldering	Solder temperature : 260 °C or below, Flow time : 10 seconds or below, Number of flow process: 1, Exposure limit* : None	WS60-00
Partial heating method	Terminal temperature : 300 °C or below, Flow time : 10 seconds or below, Exposure limit* : None	

*: Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Note: Do not apply more than a single process at once, except for "Partial heating method".

11. DEVELOPMENT SUPPORT TOOLS

The following tools are supported for developing systems using the μPD17102 chip.

Hard-ware	IE-17K	IE-17K is an in-circuit emulator available for all the μPD17000 Series chips. For the μPD17102 chip, use IE-17K and the optional SE-17102 together. When connected to a personal computer, IE-17K adds and modifies programs in real time. A PC-9801 personal computer runs the support software SIMPLEHOST, providing a more advanced development environment.		
	SE-17102	SE-17102 is an emulation board (SE board) used to evaluate the system by mounting the program developed by IE-17K and loading the board instead of the μPD17102 to the system.		
	EP-17102G	Probe used to connect the target system.		
Soft-ware	μPD17000 Series Assembler AS17K	Host machine	OS	Order name (product name)
		PC-9800 Series (excluding PC-98LT)	MS-DOS™ (Ver 2.11 or later)	μS5A1AS17K (8″ 2D) μS5A10AS17K (5″ 2HD)
	Device file	Used together with the μPD17000 Series Assembler AS17K (for μPD17102 only).		μS5A1AS17102 (8″2D) μS5A10AS17102 (5″ 2HD)
	SIMPLEHOST*	Program to support man-machine interface when connecting PC-9801 to IE-17K. MS-WINDOWS™ is required.		μS5A1IE17K (8″ 2D) μS5A10IE17K (5″ 2HD)

*: Under development

MS-DOS™ and MS-WINDOW™ are the trademark of Microsoft Co., Ltd.

FRONT PANEL CONTROLLER (FPC)

μPD17106

SINGLE-CHIP MICROCONTROLLER

The μPD17106 is a 4-bit single-chip CMOS microcomputer for front panel control.

The CPU uses the μPD17000 architecture, allowing direct operation of data memory, arithmetic operation, and peripheral hardware control by the use of a single instruction. Every instrustion consists of a 16-bit word.

The peripheral hardware includes an abundant series of input/output ports, serial interface, clock generator port,LCD driver for front panel control, key source decoder, and timer for remote control decoding.

The μPD17106 can make up a sophisticated, high performance front panel system.

The OTP (one-time PROM) version of the μPD17106 is also available as the μPD17P106 (*). The μPD17P106 is used for program evaluation or limited production of the μPD17106.

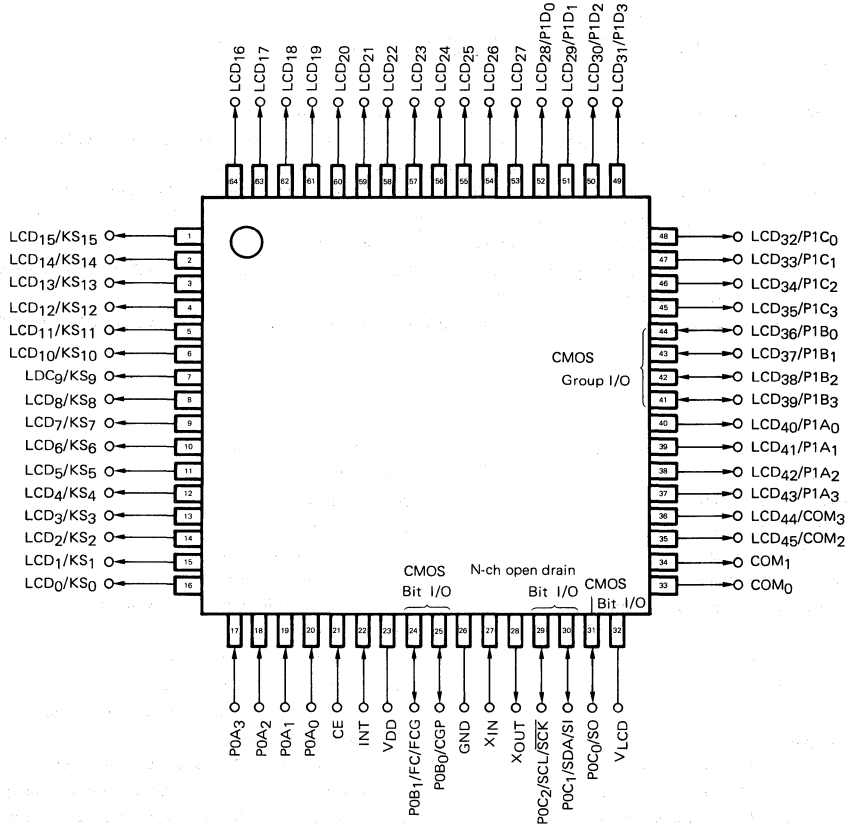
NEC provides easy-to-use tools for μPD17106 system development: in-circuit emulator (IE-17K) and assembler (AS17K).

*:under development

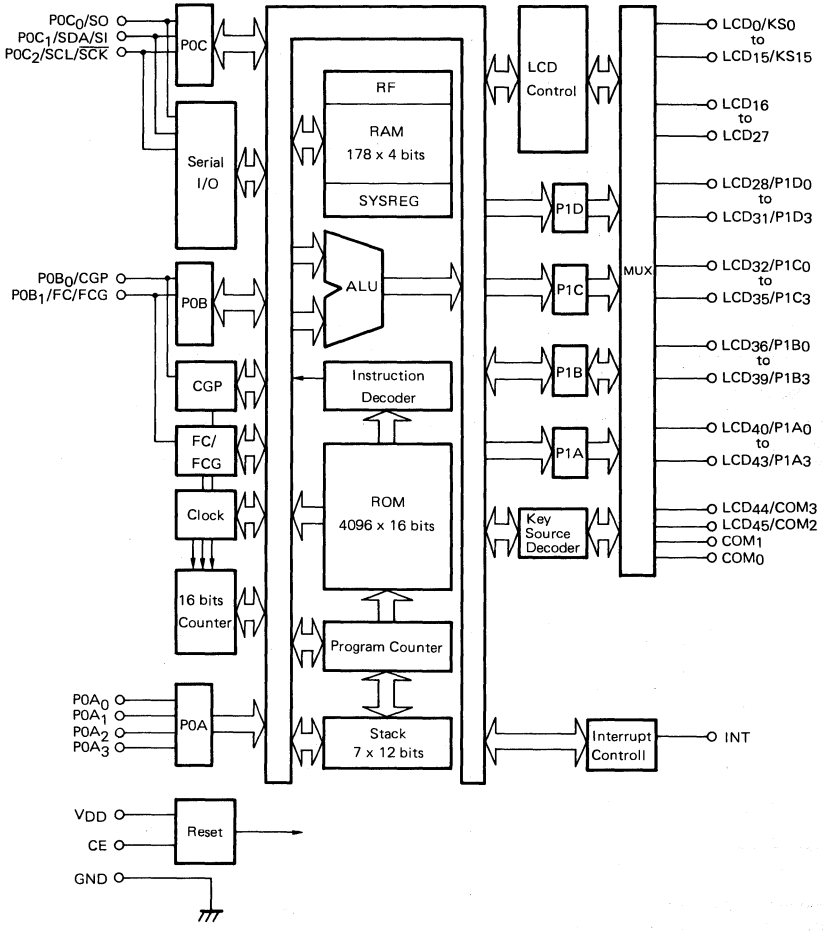
Features

- 4-bit microcontroller for front panel control
- Program memory (ROM):
  8K bytes (4096 steps x 16bits)
- General-purpose data memory (RAM):
  178 nibbles (178 nibbles x 4 bits)
- Instruction executionn time:
  4.44μs (using a 4.5MHz crystal oscillator)
- Stack level: 7
- Easy 46-instruction set
- Decimal operation possible
- Table reference possible
- Built-in LCD driver
  Static : 46 x 1= 46 segments
  1/2 duty, 1/2 bias : 46 x 2= 92 segments
  1/3 duty, 132 bias: 45 x 3= 135 segments
  1/4 duty, 1/4 bias : 44 x 4= 176 segments
- Built-in key source decoder
  16 lines (Output by time division with LCD segment signal)
- Built-in 16-bit counter providing four functions
  Timer modulo
  Frequency counter
  Pulse width counter
  CGP (clock generator port)
- Built-in 8-bit serial interface
  Two 1-system channels (2- or 3-wire type)
- Interrupt
  • External interrupt : 1 channel (INT pin)
  • Internal interrupt : 2 channels
  (timer and serial interface)
- General-purpose I/O ports
  • Input/output ports : 5 lines (+4: segment pin)
  • Input ports : 4 lines (built-in pull-up resistor)
  • Output ports : 0 line (+12: segment pins.8 out of 12 allows LED direct drive.)
- Built-in power-on reset, CE reset, and power failure detection circuit
- Low-power consumption CMOS
- Power-supply voltage: 5 V ±10%
- 64-pin plastic QFP

PIN CONFIGURATION (Top View)



BLOCK DIAGRAM



SUPPORT TOOLS FOR PROGRAM DEVELOPMENT

The following support tools are available to develop the program for the μPD17106:

Hardware		
Name	Description	Order name
In-circuit emulator (IE-17K)	The IE-17K is the in-circuit emulator for evaluation, to be used commonly for the μPD17000 series. The IE-17K serves for program development for the μPD17106 together with the system evaluation board SE-17106. The IE-17K operates based on RAM. A program can be added or modified a console by simply connecting the console to the IE-17K. Running the support software SIMPLEHOST on the personal computer PC-9801 instead of using the console will bring sophistication to the program development environment.	IE-17K
SE board (*) (SE-17106)	The SE-17106 is a system evaluation board for the μPD17106. It is used independently or in combination with the IE-17K.	SE-17106
Probe (*) (EP-17106GC)	The EP-17106GC is a probe to connect the SE-17106 to a target system.	EP-17106GC
Receptacle (*) (EV-9200GC-64)	The EV-9200GC-64 is a socket to connect the EP-17106 to a target system.	EV-9200GC-64
OTP (*) (μPD17P106)	The μPD17P106 is an OTP (One-time PROM) for program evaluation or limited production of the μPD17106.	μPD17P106GC-3BE

Software					
Name		Description	Host machine	OS	Order name
Assembler	Assembler (AS17K)	The AS17K is the assembler main routine to be used commonly for the μPD17000 series. The AS17K is used in combination with the device file (AS17106).	PC-9801 series IBM PC-AT™	MS-DOS™ Ver. 2.11 Ver. 3.1	MS-DOS version μS5A1AS17K (8-inch 2D) μS5A10AS17K (5-inch 2HD) PC-DOS version μS7B11AS17K (5-inch 2D)
	Device file (*) (AS17106)	The AS17106 is used to assemble the program for the μPD17106 in combination with the AS17K.		PC DOS™ Ver. 3.1	MS-DOS version μS5AIAS17106 (8-inch 2D) μS5A10AS17106 (5-inch 2HD) PC-DOS version μS7B11AS17106 (5-inch 2D)
Support software (*) (SIMPLEHOST)		SIMPLEHOST is software to provide a man-machine interface during program development using the IE-17K and a personal computer.		MS-WINDOWS™	–

* Under development

MS-DOS™ and MS-WINDOWS™ are the trademarks of MicroSoft Corp.
IBM PC-AT™ and PC DOS™ are the trademarks of IBM Corp.

FRONT PANEL CONTROLLER (FPC) WITH ON-CHIP ONE TIME PROM

μPD17P106

4-BIT SINGLE-CHIP MICROCONTROLLER

The μPD17P106 is a 4-bit single-chip CMOS microcontroller with on-chip ONE TIME PROM, for use in front panel control.

The CPU uses the μPD17000 architecture, which allows direct data memory manipulation and various operations with a single instructionand peripheral hardware control. Moreover, all instrustions are one 16-bit word in lenght.

In addition to a wide range of input/output ports, serial interface, and clock generator port, on chip peripheral hardware includes, for front panel control, an LCD driver, key source decoder, and remote control decoding timer, enabling high-performance front panel systems of various kinds to be configured.

As the μPD17P106 includes on-chip ONE TIME PROM,it is ideal for system evaluation in program development for the μPD17106* mask ROM version, or for small-volume production.

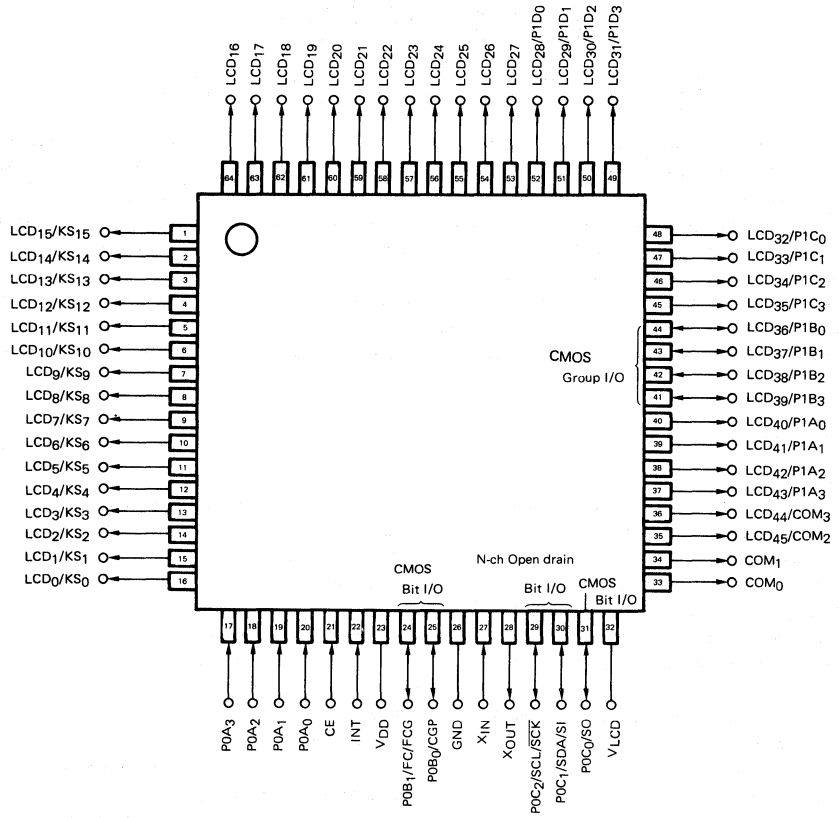
An easy-to-use in-circuit emulator (IE-17K) and assembler (AS17K) are available as μPD17P106 system development tools.

*:under development

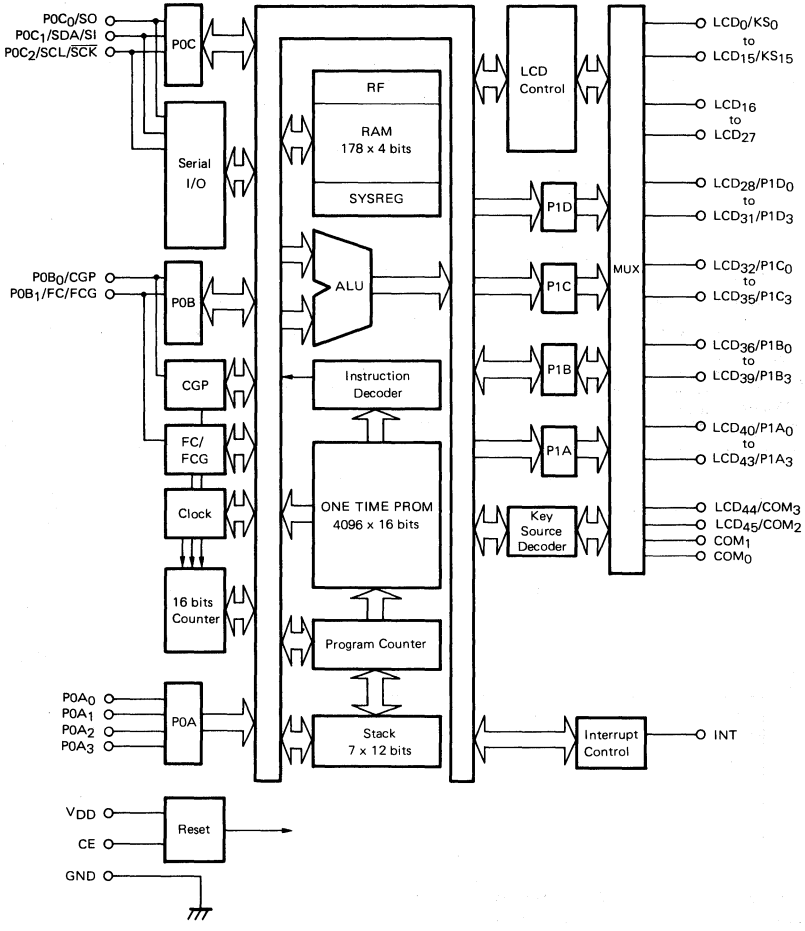
Features

- 4-bit microcontroller for front panel controller use
- Program memory (ONE TIME PROM):
  8K bytes (4096 steps x 16bits)
- General-purpose data memory (RAM):
  178 nibbles (178 nibbles x 4 bits)
- Instruction executionn time:
  4.44μs (using a 4.5MHz crystal oscillator)
- Stack levels: 7
- Easy-to-understand instructiion set (46 instructions)
- Decimal operation capability
- Table reference capability
- On-chip LCD driver
  Static : 46 x 1= 46 segments
  1/2 duty, 1/2 bias : 46 x 2= 92 segments
  1/3 duty, 132 bias: 45 x 3= 135 segments
  1/4 duty, 1/4 bias : 44 x 4= 176 segments
- On-chip key source decoder
- 16 lines (Output by time-division multiplexing with LCD segment signal)
- On-chip 16-bit counter with 4 functions:
  Timer modulo
  Frequency count
  Pulse width count
  CGP (clock generator port)
- On-chip 8-bit serial interface
  1 system 2 channels (2-wire and 3-wire)
- Variety of interrupts
  External interrupts : 1 channel (INT pin)
  Internal interrupts : 2 channels
  (timer, serial interface)
- General input/output ports
  • Input/output ports : 5 lines (+4: Segment pins)
  • Input ports : 4 lines (with internal pull-up resistor)
  • Output ports : 0 (+12: segment pins, 8 with LED direct drive capability.)
- Power-on reset, CE reset, and power failure detection circuit on chip
- Low-power consumption CMOS
- Supply voltage : 5 V ±10%
- 64-pin plastic QFP
- Mask ROM version : μPD17106

PIN CONFIGURATION (Top View)



BLOCK DIAGRAM



DEVELOPMENT SUPPORT TOOLS

The following support tools are available for system development using the μPD17P106.

Hardware		
Name		Description
In-circuit emulator (IE-17K)		The IE-17K is an in-circuit emulator which can be used with all models in the μPD17000 series. For μPD17P106 program development, the IE-17K is used in conjunction with the SE-17106 system evaluation board. As the IE-17K features RAM-based operation, immediate program additions and amendments can be made by connecting a console to the IE-17K. Moreover, use of the "SIMPLEHOST" support software provides a higher-level development environment.
SE board* (SE-17106)		The SE-17106 is a μPD17P106 system evaluation board used either alone or together with the IE-17K.
Probe* (EP-17106GC)		The EP-17106GC is a probe for connection of the target system to the SE-17106.
Receptacle* (EV-9200GC-64)		The EV-9200GC-64 is a socket for connection of the target system to the EP-17106.
EPROM programmer (Manuf. by Ando Electric Co., Ltd.)	AF-9703	EPROM programmer. For the μPD17P106, the programmer is used in conjunction with the special μPD17P106 adapter (Ver. 5 or later should be used).
	Special adapter for μPD17P106*	Adapter used in conjunction with the AF-9703.

Software					
Name		Description	Host Machine	OS	Ordering Code
Assembler	Assembler (AS17K)	AS17K is the assembler for use with the entire μPD17000 series. AS17K is used in conjunction with the device file (AS17106).	PC-9801 series IBM PC-AT™	MS-DOS™ Ver. 2.11 Ver. 3.1 PC DOS™ Ver. 3.1	MS-DOS version μS5A1AS17K (8-inch 2D) μS5A10AS17K (5-inch 2HD) PC DOS version μS7B11AS17K (5-inch 2D)
	Device file* (AS17106)	AS17106 is used together with AS17K to assemble μPD17P106 programs.			MS-DOS version μS5A1AS17106 (8-inch 2D) μS5A10AS17106 (5-inch 2HD) PC DOS version μS7B11AS17106 (5-inch 2D)
Support software* (SIMPLEHOST)		SIMPLEHOST is software which implements the man-machine interface under MS-WINDOWS™ during program development using the IE-17K and a personal computer.		MS-WINDOWS™	——

Remarks: For details of the EPROM programmer, please consult Ando Electric Co., Ltd.

*: Under development

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IBM PC-AT™ and PC DOS™ are trademarks of IBM Corporation.

FOUR-BIT SINGLE-CHIP MICROCOMPUTERS

μPD17103 and μPD17104 are tiny microcontrollers each consisting of a 1K-byte ROM, 16-word RAM, and 11 pins (for μPD17103) or 16 pins (for μPD17104) for I/O ports.

The CPU can be programmed using the μPD17000 architecture based on a general register system that allows direct access to data memory. Every instruction for these microcontrollers consists of a 16-bit single word.

FEATURES

- Program memory (ROM): 1 K bytes (512 words x 16 bits)
- Data memory (RAM): 16 words x 4 bits
- I/O ports:
  μPD17103: 11 pins (including three ports for N-ch open-drain output)
  μPD17104: 16 pins (including four ports for N-ch open-drain output)
- Instruction execution time: 2 μs (in connection with an 8 MHz crystal or ceramic oscillator)
- Instruction types: 31 types (single-word instructions)
- Stack level: 1 level
- Standby functions (using STOP and HALT instructions)
- Retains data in data memory at low voltage (Min. 2.0 V).
- Incorporates an oscillating circuit for a system clock (crystal or ceramic oscillator).
- Operating supply voltage range:
  2.7 to 6.0 V (in 2 MHz operation)
  4.5 to 6.0 V (in 8 MHz operation)

APPLICATIONS

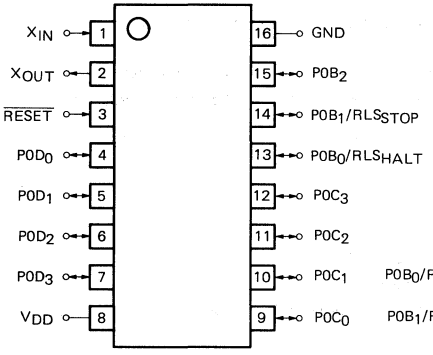
- Electronic control of electric home appliances and toys
- Circuit integration of general-purpose logic ICs on one chip

ORDERING INFORMATION

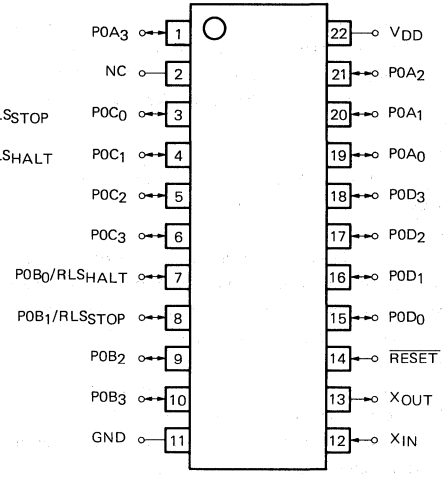
Order Code	Package
μPD17103CX-XXX	16 pin plastic DIP (300 mil)
μPD17103GS-XXX	16 pin plastic SOP (300 mil)
μPD17104CS-XXX	22 pin plastic shrink DIP (300 mil)
μPD17104GS-XXX	24 pin plastic SOP (300 mil)

PIN CONFIGURATION (Top View)

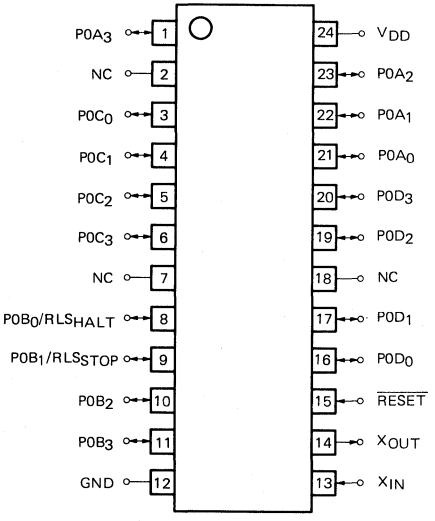
μPD17103CX/μPD17103GS



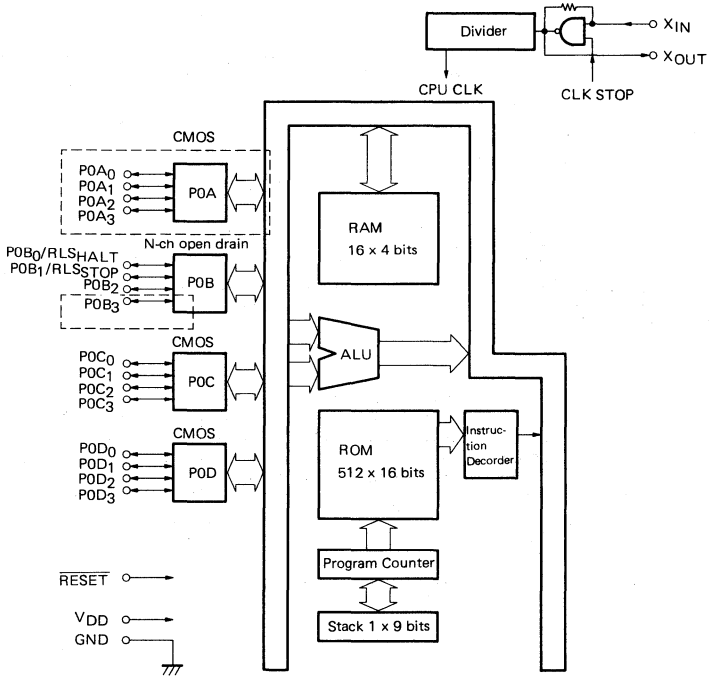
μPD17104CS



μPD17104GS



BLOCK DIAGRAM



Note: The section enclosed in a dotted line is not supported by the μPD17103.

1. PIN FUNCTIONS

1.1 LISTS

- Port pins

PIN NAME	INPUT/ OUTPUT	FUNCTIONS	ON RESETTING
$P0A_0$ to $P0A_3$ (*)	Input/output	• CMOS (push-pull) 4-bit input/output port (Port 0A)	High impedance (input mode)
$P0B_0/RLS_{HALT}$	Input/output	For resetting HALT mode	• High impedance at open-drain (input mode) • High level with built-in pull-up resistor (input mode)
$P0B_1/RLS_{STOP}$		For resetting STOP mode	
$P0B_2$		• N-ch open-drain 4-bit I/O port; (Port 0B) • Can corporate a pull-up resistor for each bit (by mask option) • Dielectric strength of 9 V at open-drain	
$P0B_3$ (*)			
$P0C_0$ to $P0C_3$	Input/output	• CMOS (push-pull) 4-bit input/output port (Port 0C)	High impedance (input mode)
$P0D_0$ to $P0D_3$	Input/output	• CMOS (push-pull) 4-bit input/output port (Port 0D)	High impedance (input mode)

* The pins marked by an asterisk * are not built into μPD17103.

- Pins other than port pins

PIN NAME	INPUT/ OUTPUT	FUNCTIONS	ON RESETTING
$\overline{RESET}$	Input	• System reset input pin • Can incorporate a pull-up resistor (by mask option)	
V_{DD}		• Positive power supply pin	
GND		• GND pin	
X_{IN}, X_{OUT}		• System clock oscillator connecting pin	

1.2 DESCRIPTION

1.2.1 $P0A_0$ to $P0A_3$ (Port 0A), $P0C_0$ to $P0C_3$ (Port 0C), and $P0D_0$ to $P0D_3$ (Port 0D): Input/output pins

$P0A_0$ to $P0A_3$, $P0C_0$ to $P0C_3$, and $P0D_0$ to $P0D_3$ are four-bit input/output pins with output latches for ports 0A, 0C, and 0D, respectively.

The contents of ports 0A, 0C, and 0D are respectively mapped to addresses 70H, 72H, and 73H in data memory space as port registers. Data can be read from and written to the port registers using the normal data memory access instructions.

On being reset, each pin goes into the input mode. When data is written into each port register, each pin for the corresponding port enters into the output mode to output the written data. Once the pin enters into the output mode, the written data and the mode are held until another datum is written into the port register or the mode is reset.

Whenever datum in a port register is read out, the corresponding pin outputs its status whether in input or output mode. The contents of the port register do not change at this time.

Ports 0A, 0C, and 0D use the CMOS (push-pull) output form. Note that μPD17103 does not have $P0A_0$ to $P0A_3$.

1.2.2 $P0B_0/RLS_{HALT}$, $P0B_1/RLS_{STOP}$, $P0B_2$, and $P0B_3$ (Port 0B): Input/Output Pins

$P0B_0$ to $P0B_3$ are four-bit input/output pins each with an output latch for the port 0B.

The port 0B is mapped to 71H in data memory space and can be accessed by the normal data memory access instructions. On being reset, each pin enters into the input mode.

When data is written into the port register, each pin for the port enters into the output mode to output the written data. Once the pin enters into the output mode, the written data and the mode are held until another datum is written into the port register or the mode is reset.

Whenever data in the port register is read out, the pin outputs its status whether in input or output mode. The contents of the port register do not change at this time.

For the output format of the port 0B, N-ch open-drain output or N-ch open-drain plus pull-up built-in resistance output can be selected using the mask option. (See Section 1.3.)

The N-ch open-drain output has a dielectric strength of 9 V, providing efficient interface to a circuit operating at a different supply voltage.

$P0B_0$ and $P0B_1$ are pins for pseudo-interruption to reset the HALT or STOP mode on the leading edge of the input signal. The pin incorporates a hazard preventive circuit to prevent malfunction resulting from noise of 1 μs or less.

Note that μPD17103 has no $P0B_3$. Therefore, whenever an attempt is made to read data from $P0B_3$, only "0" (fixed) is read from μPD17103. Data attempted to be written into $P0B_3$ become invalid.

1.2.3 X_{IN} and X_{OUT}

These pins are connected to the oscillator of a system clock oscillating circuit.

1.2.4 $\overline{RESET}$

This pin is a low-level-active system reset input pin. It is used for resetting the standby mode as well as normal system resetting.

1.2.5 V_{DD}

Positive power supply pin

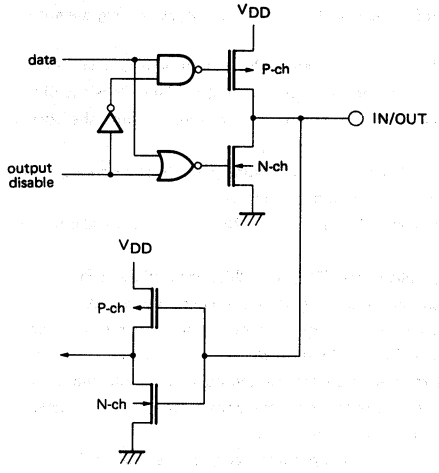
1.2.6 GND

GND pin

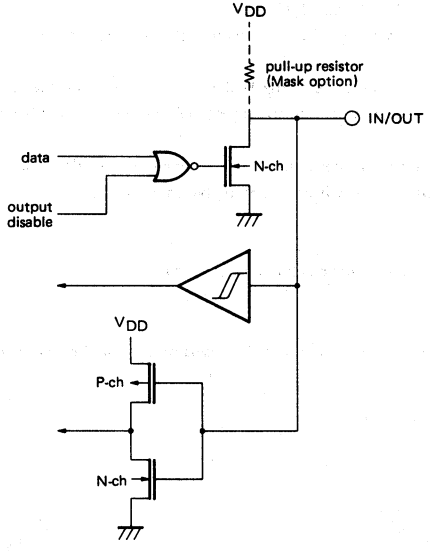
1.3 INPUT/OUTPUT CIRCUITS OF PINS

This section illustrates the input/output circuit of each pin of μPD17103 and μPD17104 in a partly simplified form.

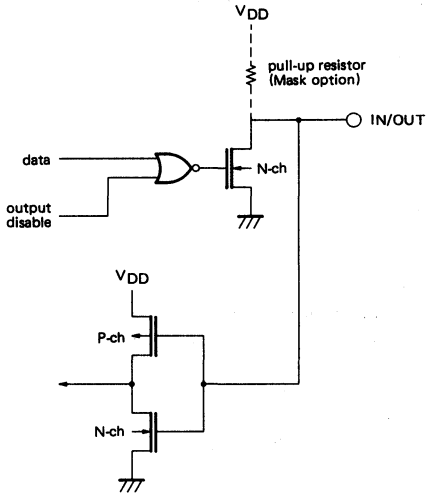
(1) POA, POC and POD



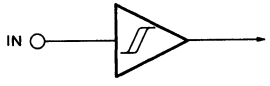
(2) POB_0 and POB_1



(3) $P0B_2$ and $P0B_3$



(4) $\overline{\text{RESET}}$



1.4 PIN MASK OPTIONS

In programming μPD17103 or μPD17104, the mask options for pins must be set using mask option pseudo-instructions in the assembler source program. Before setting the mask options, the file D17103.OPT or D17104.OPT must be stored in the current directory.

The following pins require mask option setting:

- $P0B_0$
- $P0B_1$
- $P0B_2$
- $P0B_3$(*)
- $\overline{RESET}$

* The pin marked by the asterisk * is not built into μPD17103.

1.4.1 Mask option pseudo-instructions

(1) OPTION and ENDOP pseudo-instructions

Assume the mask option definition block ranging from the OPTION pseudo-instruction to the ENDOP pseudo-instruction. Within this block, execute the following mask option pseudo-instruction shown in (2).

Description format:

Label	Instruction	Operand	Comment
[Label:]	OPTION		[;Comment]
	⋮		
	ENDOP		

(2) Mask option defining pseudo-instruction

This pseudo-instruction defines the mask option for each pin.

〈μPD17103〉

① Pins $P0B_0$ to $P0B_2$

Description format:

Label	Instruction	Operand
	OPTP0B	(P0B2), (P0B1), (P0B0)

A series of "P0BX" (X: 0 to 2) indicates the option parameters that can be described as the operand each. Beginning with the first operand, they define mask options for pins $P0B_2$, $P0B_1$ and $P0B_0$, respectively. P0BPLUP (Pull-up) and OPEN (open) are available as option parameters.

〈μPD17104〉

① $P0B_0$ to $P0B_3$

Description format:

Label	Instruction	Operand
	OPTP0B	(P0B3), (P0B2), (P0B1), (P0B0)

A series of "P0BX" (X: 0 to 3) indicates the option parameters that can be described as the operand each. Beginning with the first operand, they define mask options for pins $P0B_3$, $P0B_2$, $P0B_1$, and $P0B_0$, respectively.

P0BPLUP (pull-up) and OPEN (open) are available as option parameters.

② RESET pin

Description format:

Label	Instruction	Operand
	OPTRES	(RESET)

"RESET" indicates the option parameter which can be described as the operand. RESPLUP (pull-up) and OPEN (open) are available as option parameters.

Example 1 Set the following mask option using the source file for assembling of μPD17103:

$P0B_2$: Pull-up $P0B_1$: Open

$P0B_0$: Open $\overline{RESET}$: Pull-up

```
; 17103
 Mask option setting:    OPTION
                             OPTPOB   POBPLUP, OPEN, OPEN
                             OPTRES   RESPLUP
                         ENDOP
```

Example 2 Set the following mask option using the source file for assembling μPD17104:

$P0B_3$: Pull-up $P0B_2$: Open

$P0B_1$: Open $P0B_0$: Open

$\overline{RESET}$: Pull-up

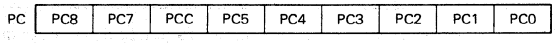
```
; 17104
 Mask option setting:    OPTION
                             OPTPOB   POBPLUP, POBPLUP, OPEN, OPEN
                             OPTRES   RESPLUP
                         ENDOP
```

2. INTERNAL BLOCK FUNCTIONS

2.1 PROGRAM COUNTER (PC) ..... 9 BITS

The program counter is a nine-bit binary counter to retain program memory address information.

Fig. 2-1 Program counter configuration

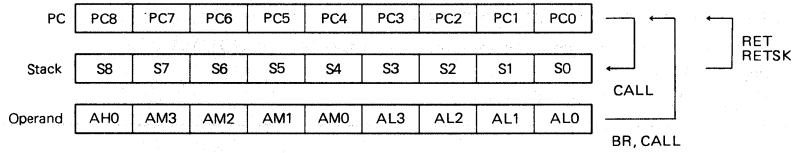


Usually the program counter is incremented by one whenever one instruction is executed.

When the call instruction (CALL) is executed, the call address is loaded onto the PC after the current contents (return address) of the PC are saved on the stack. When the return instruction (RET or RETSK) is executed, the current contents (return address) of the PC are loaded onto the PC. When the jump instruction (BR) is executed, the jump address indicating the destination of the jump is loaded onto the PC.

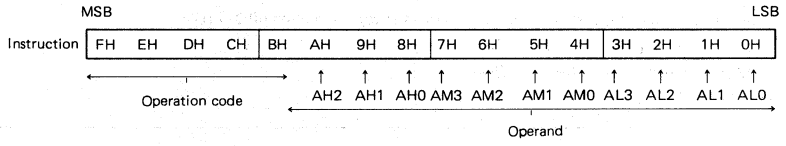
The address stack has only one level.

Fig. 2-2 Relationship among PC, stack, and instruction



In Fig. 2-2, AHn, AMn, and ALn (n: 0 to 3) indicate their respective bits in a 16-bit instruction as shown in Fig. 2-3.

Fig. 2-3 16-bit instruction configuration



When using a BR or CALL instruction, be sure to set AH2 and AH3 both to 0.

Sn (n: 0 to 8) indicates the address stack.

When RESET is input, program counter bits are all cleared to zero.

2.2 ADDRESS STACK

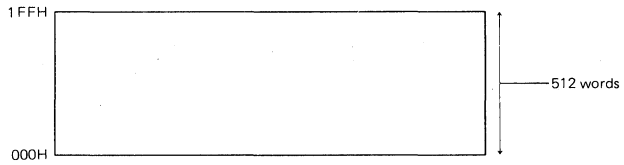
The address stack has a dedicated stack format of only one level. Note that the stack pointer can neither be written nor read by any instruction.

The contents (return address) of the PC for the last-executed CALL instruction are saved on the address stack.

2.3 PROGRAM MEMORY (ROM) ..... 512 WORDS x 16 BITS

This memory is a mask programmable ROM having a capacity of 512 words x 16 bits. It is addressed by the program counter. The programmable memory stores programs. Address 000H is a reset start address.

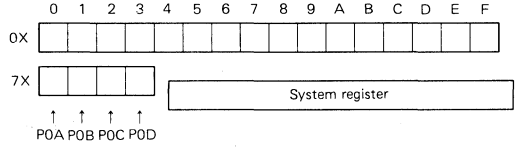
Fig. 2-4 Program memory map



2.4 DATA MEMORY (RAM) ..... 16 WORDS x 4 BITS

The data memory occupies 16 nibbles as memory space.

Fig. 2-5 Data memory map



16 words between 00H and 0FH are available for the data storage area.

Since μPD17103 has neither the four bits of 70H nor the third bit of 71H, 0 is read from the data memory in μPD17103.

2.4.1 Port data mapping

Port data is mapped into addresses 70H to 73H (port register) on the data memory space. The data written in these addresses is output from each port. When port data is read, the read data is not stored in this area until the instruction to write the data into the data memory is executed.

2.4.2 Addressing

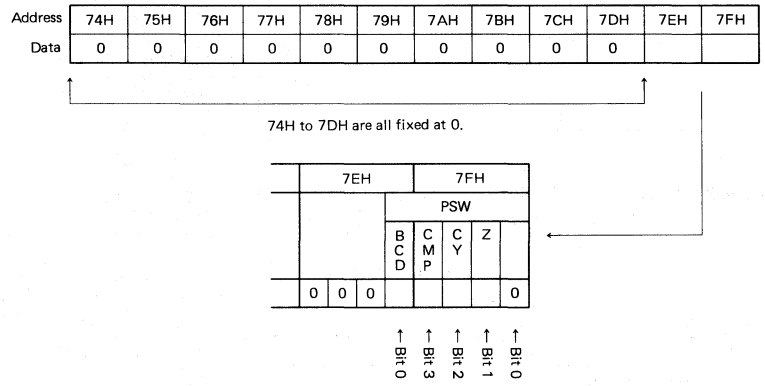
Addresses can be specified by three-bit row addresses and four-bit column addresses.

μPD17000 series allows determining the area to be used for general registers by setting the value of the register pointer (RP). μPD17103 or μPD17104 allows the 16 words of 0H to 0FH to be used as general registers because the register pointer is fixed at 0. Thus 0H to 0FH can be specified either as registers or certain addresses in the data memory. The operands of one instruction carry information specifying one (column) of 16 general registers and information on row and column addresses of the data memory. In data transfer between data memory and a general register, data is transferred between the data memory at the address specified by the corresponding operand of the instruction and the register with the number (column) specified by the corresponding operand of the instruction.

2.5 SYSTEM REGISTERS

System registers are the ones directly concerning the control of the CPU, which are mapped into addresses 74H to 7FH on the data memory address space. μPD17103 and μPD17104 have only one system register, program status word (PSW).

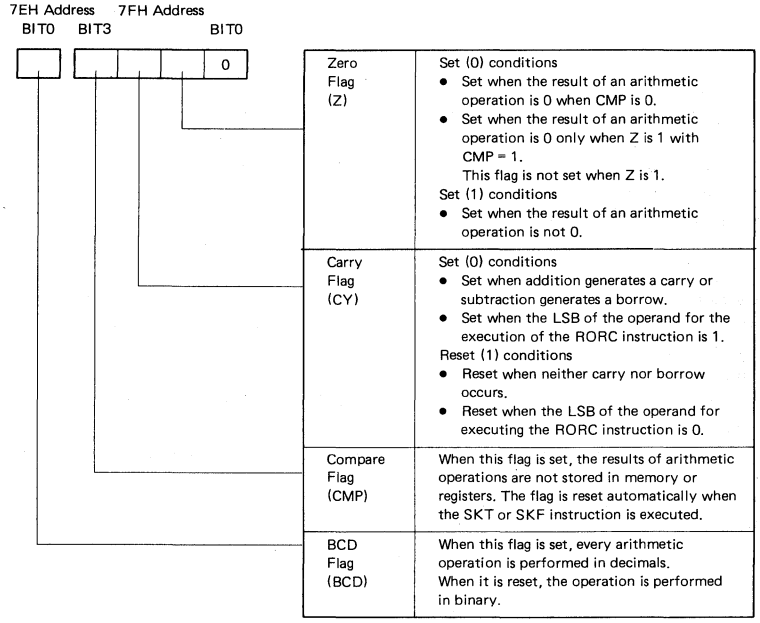
Fig. 2-6 System register map



Bit 0 at address 7EH and the higher three bits at address 7FH are assigned for the program status word. Bit 0 at address 7EH is mapped for a BCD flag. Bits 3, 2, and 1 at address 7FH are mapped respectively for CMP, carry (CY), and zero (Z) flags.

The higher three bits at address 7EH and bit 0 at address 7FH are fixed at 0.

Fig. 2-7 Structure of program status word



The CY flag does not change with the compare instruction (SKE, SKNE, SKGE, or SKLT). However, it changes according to the result of an arithmetic operation even though the CMP flag has been set.

Note that each bit of the program status word is initialized to 0 when the reset signal is input.

The Z flag in the program status word varies with the value of the CMP flag as shown in Table 2-1.

Table 2-1 Variation of Z-flag value

Conditions	Value of Z flag	
	CMP = 0	CMP = 1
On resetting	0	—
Z flag is set to 0 by memory operation.	0	0
Z flag is set to 1 by memory operation.	1	1
Result of arithmetic operation is 0.	0	0
Result of arithmetic operation is 1.	1	Zn-1

Zn-1: Value of Z flag just before execution.

When the CMP is 1, the value of the Z flag is held to be 1 when the value of the Z flag is 1 and the result of an arithmetic operation is 0H. If the result becomes any value other than 0H at this time, the value of the Z flag is reset to 0. In this case, the value of the Z flag is not set to 1 even though the result of the retried arithmetic operation becomes 0H.

That is, if the Z flag remains 1 when being referenced after setting of CMP and Z flags both to 1 and several times of comparison (though subtraction), it means that the result of each comparing operation is identically 0. If the Z flag becomes 0 then, it means that the comparing operations have given different values at least once.

2.6 LOGICAL ARITHMETIC UNIT (ALU) ..... 4 BITS

The logical arithmetic unit (ALU) executes arithmetic and logical operations on four-bit data, bit check, comparison, and data rotation.

2.6.1 Arithmetic operations

The ALU performs two types of arithmetic operations: binary and decimal. It performs a decimal operation when the value of the BCD flag (in the program status word) is 1 and a binary operation when the value is 0.

When addition generates a carry or subtraction generates a borrow, the carry (CY) flag is set to 1. If neither of them occurs, the flag is reset to 0.

If the result of an arithmetic operation is 0, the zero (Z) flag is set to 1. The flag is reset to 0 when the result is not 0.

(1) Binary operation

A carry occurs when the result of a binary arithmetic operation exceeds 15 (1111B). When the result is less than 0, a borrow occurs and the CY flag is set to 1.

(2) Decimal operation

A carry occurs when the result of a decimal arithmetic operation exceeds 9 (1001B). When the result is less than 0, a borrow occurs and the CY flag is set to 1. The decimal arithmetic operation can be executed only when the operation results as follows. If the result of the operation falls out of the following specified ranges, the CY flag is set to 1 and the value of the operation is 10 (1010B) or more:

1. The result of addition must be within 0 to 19.,
2. The result of subtraction must be within 0 to 9 or −10 to −1.

2.6.2 Logical operations

The ALU performs three types of logical operations: conjunction (AND), disjunction (OR), exclusive OR (XOR).

2.6.3 Other operations

The ALU performs bit check, decision though comparison, and data rotation.

3. STANDBY FUNCTIONS

This device provides two types of standby modes: HALT mode and STOP mode.

3.1 HALT MODE

The HALT mode sets the state where the program counter (PC) stops carrying out any further operations until restarted with the system clock left oscillating. This mode is set by the HALT instruction and reset by the reset signal $\overline{\text{RESET}}$ or input to the $P0B_0$ pin. When the mode is reset by the input to the $P0B_0$ pin, the device resets the mode without waiting for the system clock to stabilize its oscillation. In this case, the first instruction to be executed after the resetting of the mode is the one next to the HALT instruction.

The normal system reset (restarting from address 0H) occurs if the mode is forced to be reset by the reset signal $\overline{\text{RESET}}$.

3.2 STOP MODE

The STOP mode stops the oscillation of the system clock and sets the state where data can be retained at a low supply voltage. This mode is set by the STOP instruction and reset by the reset signal $\overline{\text{RESET}}$ or input to the $P0B_1$ pin. When the mode is reset by input to the $P0B_1$ pin, the first instruction to be executed after the reset is the one that follows the STOP instruction.

The normal system reset (restarting from address 0H) occurs if the mode is forced to be reset by the reset signal $\overline{\text{RESET}}$.

3.3 SETTING AND RESETTING STANDBY MODES

(1) Setting and resetting HALT mode

The HALT instruction allows selection of the conditions to set and reset the HALT mode depending on the setting of the low-order bit of the operand as follows. Fix the higher three bits of the operand to 0.

Fig. 3-1 Mode setting/resetting conditions of HALT instruction

HALT 000X B ← Four-bit data of operand

X	Setting and resetting conditions
0	When executed, the HALT instruction sets the HALT mode unconditionally. The mode is reset only by the reset signal $\overline{\text{RESET}}$. After the mode is reset, execution of instructions is started from address 0H.
1	When $P0B_0$ is 0, the HALT instruction sets the HALT mode when executed. If $P0B_0$ is 1, the instruction does not set the mode when executed. The mode set by this instruction is reset by the reset signal $\overline{\text{RESET}}$. After the resetting, execution of instructions are started from address 0H. The mode is also reset at rise of the input signal to the $P0B_0$ pin. In this case, the first instruction to be executed after the reset is the one that follows the HALT instruction.

(2) Setting and resetting STOP mode

The STOP instruction allows selection of the conditions to set and reset the STOP mode depending on the setting of the low-order bit of the operand as follows. Fix the higher three bits of the operand to 0.

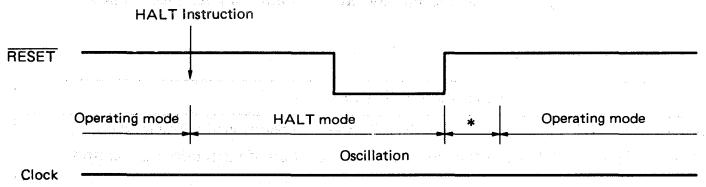
Fig. 3-2 Mode setting/resetting condition of the STOP instruction

STOP 000X̲B←Four-bit data of operand

X	Setting and resetting conditions
0	When executed, the STOP instruction sets the STOP mode unconditionally. All the peripheral circuits stop operations after returning to their initial status as if the system reset occurs. The mode is reset only by the reset signal $\overline{\text{RESET}}$. After the mode is reset, execution of instructions are started from address 0H.
1	When $P0B_1$ is 0, the STOP instruction sets the STOP mode when executed. If $P0B_1$ is 1, the instruction does not set the mode when executed., The mode set by this instruction is reset by reset signal $\overline{\text{RESET}}$. After the resetting, execution of instructions are started from address 0H. The mode is also reset at rise of the input signal to the $P0B_1$ pin. In this case, the first instruction to be executed after the reset is the one that follows the HALT instruction.

3.4 STANDBY MODE RESETTING TIMING

Fig. 3-3 Resetting HALT mode by $\overline{\text{RESET}}$ signal input



When the HALT mode is reset by inputting the $\overline{\text{RESET}}$ signal, the device enters the operating mode after returning the $\overline{\text{RESET}}$ input to a high level.

*: This interval is the time for waiting for stable oscillation in the HALT mode.

Fig. 3-4 Resetting the HALT mode by interruption

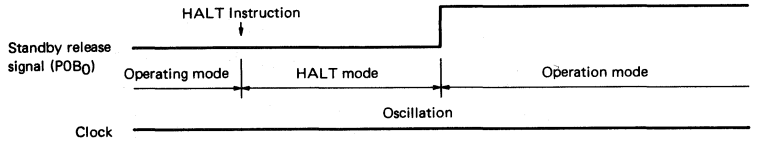
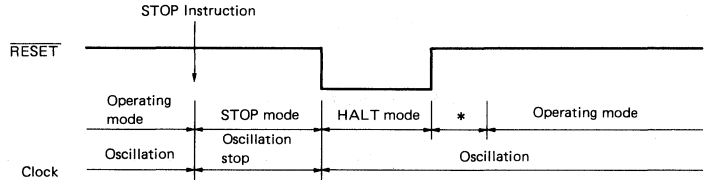


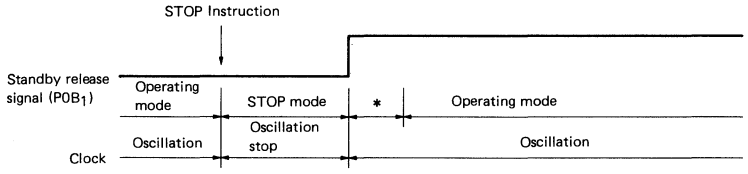
Fig. 3-5 Resetting STOP mode by $\overline{\text{RESET}}$ signal input



The clock starts oscillation the moment the $\overline{\text{RESET}}$ input goes from high to low level in the STOP mode.

*: This interval is the time for waiting for stable oscillation in the HALT mode.

Fig. 3-6 Resetting the STOP mode by interruption



*: This interval is the time for waiting for stable oscillation in the HALT mode.

4. RESETTING

4.1 HARDWARE STATUS ON RESETTING

When the $\overline{\text{RESET}}$ pin inputs a low-level active reset signal, the hardware components are set as follows. They are released from their reset status when the $\overline{\text{RESET}}$ pin returns to the high level.

Table 4-1 Hardware after reset

Component	Memory address	Set value
Program counter		000H
RAM	0H to 0FH	Data before reset is retained.
Program status word (PSW)	7EH BIT0 7FH BIT3-1	All 0
Ports 0A to 0D	70H to 73H	Data is retained. All the pins enter the input mode.

5. RESERVED WORDS

Table 5-1 lists the reserved words defined in the device files of the μPD17103 and μPD17104.

Table 5-1 Reserved words list

Name	Attribute	Value	R/W	Description
*P0A0	FLG	0.70H. 0	R/W	Bit 0 of port 0A
*P0A1	FLG	0.70H. 1	R/W	Bit 1 of port 0A
*P0A2	FLG	0.70H. 2	R/W	Bit 2 of port 0A
*P0A3	FLG	0.70H. 3	R/W	Bit 3 of port 0A
P0B0	FLG	0.71H. 0	R/W	Bit 0 of port 0B
P0B1	FLG	0.71H. 1	R/W	Bit 1 of port 0B
P0B2	FLG	0.71H. 2	R/W	Bit 2 of port 0B
*P0B3	FLG	0.71H. 3	R/W	Bit 3 of port 0B
P0C0	FLG	0.72H. 0	R/W	Bit 0 of port 0C
P0C1	FLG	0.72H. 1	R/W	Bit 1 of port 0C
P0C2	FLG	0.72H. 2	R/W	Bit 2 of port 0C
P0C3	FLG	0.72H. 3	R/W	Bit 3 of port 0C
P0D0	FLG	0.73H. 0	R/W	Bit 0 of port 0D
P0D1	FLG	0.73H. 1	R/W	Bit 1 of port 0D
P0D2	FLG	0.73H. 2	R/W	Bit 2 of port 0D
P0D3	FLG	0.73H. 3	R/W	Bit 3 of port 0D
BCD	FLG	0.7EH. 0	R/W	BCD arithmetic flag
PSW	MEM	0.7FH	R/W	Program status word
Z	FLG	0.7FH. 1	R/W	Zero flag
CY	FLG	0.7FH. 2	R/W	Carry flag
CMP	FLG	0.7FH. 3	R/W	Compare flag

*: $P0A_0$ to $P0A_3$ are not defined in the device file of μPD17103. The $P0B_3$ is not provided for μPD17103 but registered as a read-only flag to be used as a dummy bit in using a built-in macro.

6. INSTRUCTION SET

6.1 INSTRUCTION LIST

MNEMO	OPERND	OPERATION	SKIP	OPCODE	A98	7654	3210
ADD	R, M	R←(R)+(M)		00000	MH	ML	R
ADDC	R, M	R←(R)+(M)+CY		00010	MH	ML	R
ADD	M, #I	M←(M)+I		10000	MH	ML	I
ADDC	M, #I	M←(M)+I+CY		10010	MH	ML	I
SUB	R, M	R←(R)−(M)		00001	MH	ML	R
SUBC	R, M	R←(R)−(M)−BRW		00011	MH	ML	R
SUB	M, #I	M←(M)−I		10001	MH	ML	I
SUBC	M, #I	M←(M)−I−BRW		10011	MH	ML	I
SKE	M, #I	(M)−I	ZERO	01001	MH	ML	I
SKNE	M, #I	(M)−I	NOT ZERO	01011	MH	ML	I
SKGE	M, #I	(M)−I	NOT BRW	11001	MH	ML	I
SKLT	M, #I	(M)−I	BRW	11011	MH	ML	I
AND	M, #I	M←(M) AND I		10100	MH	ML	I
OR	M, #I	M←(M) OR I		10110	MH	ML	I
XOR	M, #I	M←(M) XOR I		10101	MH	ML	I
AND	R, M	R←(R) AND (M)		00100	MH	ML	R
OR	R, M	R←(R) OR (M)		00110	MH	ML	R
XOR	R, M	R←(R) XOR (M)		00101	MH	ML	R
RORC	R	CY→(R)→CY		00111	000	0111	R
LD	R, M	R←(M)		01000	MH	ML	R
ST	M, R	M←(R)		11000	MH	ML	R
MOV	M, #I	M←I		11101	MH	ML	I
SKT	M, #n	TEST (M)n, CMP←0	ALL TRUE	11110	MH	ML	n
SKF	M, #n	TEST (M)n, CMP←0	ALL FALSE	11111	MH	ML	n

MNEMO	OPERND	OPERATION	SKIP	OPCODE	A98	7654	3210
BR		PC(8–0)←A		01100	AH	AM	AL
CALL		SP←(SP)–1, STACK←((PC)+1), PC(8–0)←A		11100	AH	AM	AL
RET		PC←(STACK), SP←(SP)+1		00111	000	1110	0000
RETSK		PC←(STACK), SP←(SP)+1	UNCONDITION	00111	001	1110	0000
STOP	C	STOP CLOCK		00111	010	1111	C
HALT	h	HALT CPU		00111	011	1111	h
NOP		NO OPERATION		00111	100	1111	0000

CY : Carry flag
CMP : Compare flag
(R) : Value of register
(M) : Value of data memory
R : Register number
I : Numerical data
#n : Bit number
PC : Program counter
R : Register
M : Data memory MH, ML
A : Address AH, AM, AL

7. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage	V_{DD}			−0.3 to +7.0	V
Input Voltage	V_I	P0A, C, D		−0.3 to V_{DD} +0.3	V
		P0B	(1)	−0.3 to V_{DD} +0.3	V
			(2)	−0.3 to +11	V
Output Voltage	V_O	P0A, C, D		−0.3 to V_{DD} +0.3	V
		P0B	(1)	−0.3 to V_{DD} +0.3	V
			(2)	−0.3 to +11	V
High Output Current	I_{OH}	One pin of P0A, P0B, P0C and P0D each		−5	mA
		Total of all pins		−15	mA
Low Level Output Current	I_{OL}	One pin of P0A, P0B, P0C and P0D		30	mA
		Total of all pins		100	mA
Operating Temperature	T_{opt}			−40 to −85	C
Storage Temperature	T_{stg}			−65 to +150	C
Power Consumption	P_d	T_a = 85 °C	16 pin DIP	400	mW
			16 pin SOP	190	mW
			22 pin DIP	400	mW
			24 pin SOP	250	mW

Remarks: **(1)** N-ch open-drain input/output + pull-up resistor built-in input/output
(2) N-ch open-drain input/output

CAPACITY (T_a = 25 °C, V_{DD} = 0 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Input Capacity	C_{IN}			15	pF	f = 1 MHz, Pins except the one under measurement: 0 V
Input/Output Capacity	C_{IO}			15	pF	

DC CHARACTERISTICS (T_a = 40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS	
High Level Input Voltage	V_{IH1}	0.7V_{DD}		V_{DD}	V	Other than below	
	V_{IH2}	0.8V_{DD}		V_{DD}	V	P0B, $\overline{RESET}$	
	V_{IH3}	0.8V_{DD}		9	V	P0B	(3)
	V_{IH4}	V_{DD}–0.5		V_{DD}	V	X_{IN}	
Low Level Input Voltage	V_{IL1}	0		0.3V_{DD}	V	Other than below	
	V_{IL2}	0		0.2V_{DD}	V	P0B, $\overline{RESET}$	
	V_{IL3}	0		0.5	V	X_{IN}	
P0A, C, D High Level Output Voltage	V_{OH}	V_{DD}–2.0			V	V_{DD} = 4.5 to 6.0 V, I_{OH} = –2 mA	
		V_{DD}–1.0				I_{OH} = –200 A	
P0A, B, C, D Low Level Output Voltage	V_{OL}			2.0	V	V_{DD} = 4.5 to 6.0 V, I_{OL} = 15 mA	
				0.5	V	I_{OL} = 600 μA	
P0A, B, C, D High Level Input Leak Current	I_{LIH1}			5	μA	V_{IN} = V_{DD}	
	I_{LIH2}			10	μA	V_{IN} = 9 V	(3)
P0A, B, C, D Low Level Input Leak Current	I_{LIL}			–5	μA	V_{IN} = 0 V	
P0A, B, C, D High Level Output Leak Current	I_{LOH1}			5	μA	V_{OUT} = V_{DD}	
	I_{LOH2}			10	μA	V_{OUT} = 9 V	(3)
P0A, B, C, D Low Level Output Leak Current	I_{LOL}			–5	μA	V_{OUT} = 0 V	
Input Pin Built in Resistor		20	47	95	kΩ	$\overline{RESET}$ (Pull-up)	
I/O Pin Built-in Resistor		5	15	30	kΩ	$P0B_0$, $P0B_1$, $P0B_2$, $P0B_3$ (Pull-up)	
Power Supply Current (4)	I_{DD1}		1.5	4.5	mA	Operating mode	V_{DD} = 5 V ± 10 %, f_{CC} = 8.0 MHz
			250	750	μA		V_{DD} = 3 V ± 10 %, f_{CC} = 2.0 MHz
	I_{DD2}		1.0	3.0	mA	HALT mode	V_{DD} = 5 V ± 10 %, f_{CC} = 8.0 MHz
			200	600	μA		V_{DD} = 3 V ± 10 %, f_{CC} = 2.0 MHz
	I_{DD3}		0.1	10	μA	STOP mode	V_{DD} = 5 V ± 10 %
			0.1	5	μA		V_{DD} = 3 V ± 10 %

Remark (3): For N-ch open-drain input/output selection.

Remark (4): The current flowing to the built-in pull-up resistor is excluded.

CHARACTERISTICS OF DATA RETENTION IN DATA MEMORY AT LOW SUPPLY VOLTAGE (T_a = –40 to +85 °C)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Data Retention Supply Voltage	V_{DDDR}	2.0		6.0	V	
Data Retention Supply Current	I_{DDDR}		0.1	5.0	μA	V_{DDDR} = 2.0 V
Release Signal Setting Time	t_{SREL}	0			μs	
Stable Oscillation Wait Time	t_{WAIT} request		8/fx (5)		mS	Reset by $\overline{RESET}$
			8/fx (5)		mS	Reset by interrupt (POB_0)
		0			mS	Reset by interrupt (POB_1)

Remark (5): fx indicates an oscillator frequency.

AC CHARACTERISTICS (T_a = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Internal Clock Cycle Time	T_{cy}	1.9		30	μs	V_{DD} = 4.5 to 6.0 V
		7.6		30	μs	
POB_0, High/Low Level Width	T_{PBH} T_{PBL}	10			μs	
$\overline{RESET}$ High/Low Level Width	T_{RSH} T_{RSLK}	10			μs	

4-BIT SINGLE-CHIP MICROCONTROLLER

The μPD17P103 is a tiny microcontrollers consisting of a 1K-byte ROM, 16-word RAM, and 11 input/output ports. It is a one-time PROM version of the μPD17103, whose internal mask ROM is replaced with a one-time PROM.

Two μPD17P103 models are available: μPD17P103CX, which allows a program to be written only once, and μPD17P103GS. They are suitable for evaluation of μPD17103 and for small-scale production.

The μPD17000 architecture of the CPU uses general registers so that data memory can be manipulated directly for effective programming. Every instruction is 1 word long, consisting of 16 bits.

FEATURES

- Compatible with the μPD17103
- Program memory (one-time PROM): 1K bytes (512 words x 16 bits)
- Data memory (RAM): 16 words x 4 bits
- Input/output ports: 11 ports (including three N-ch open-drain outputs)
- Instruction execution time: 2 μs (with 8-MHz crystal or ceramic resonator connected)
- Number of instructions: 24 (Each instruction is 1 word long.)
- Stack level: 1
- A standby function is supported (with the STOP and HALT instructions).
- Data memory can retain data on low voltage (2.0 V at minimum).
- An oscillator is included for the system clock (for crystal or ceramic resonator).
- Operating supply voltage: 2.7 to 6.0 V (at 2 MHz)
  4.5 to 6.0 V (at 8 MHz)

APPLICATIONS

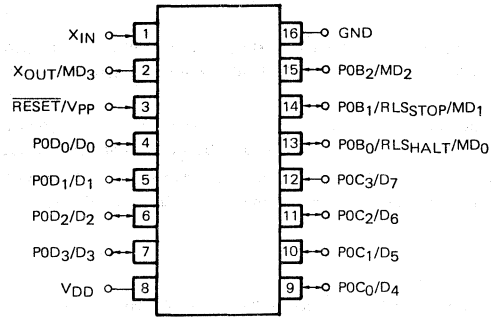
- Controlling electric appliances or toys
- Providing general-purpose logic ICs in one chip

ORDERING INFORMATION

Order Code	Package
μPD17P103CX	16-pin plastic DIP (300 mil)
μPD17P103GS	16-pin plastic SOP (300 mil)

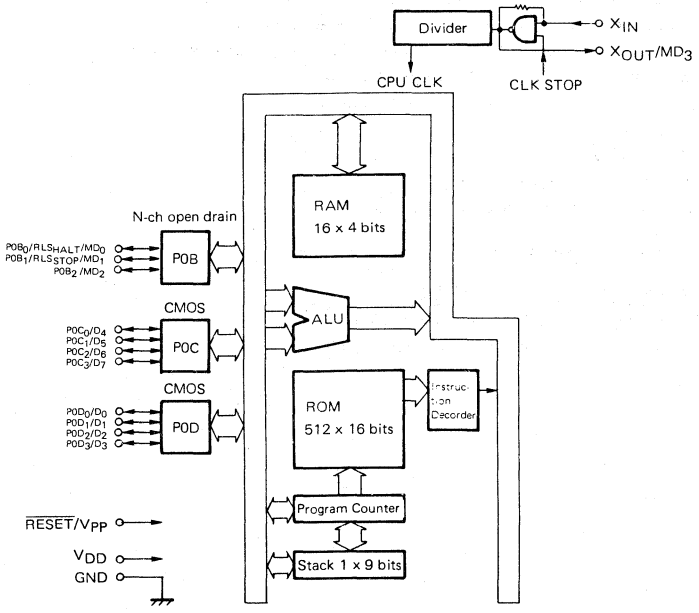
PIN CONFIGURATION (Top View)

μPD17P103CX/μPD17P103GS



16-pin plastic DIP
16-pin plastic SOP

BLOCK DIAGRAM



PIN FUNCTIONS

PIN FUNCTIONS

- Port pins

PIN NAME	INPUT/ OUTPUT	DUAL FUNCTION PIN		FUNCTION		When writing to program memory or verifying its contents	WHEN RESET
$P0B_0$	Input/ output	RLS_{HALT}	MD_0	• N-ch open-drain 4-bit input/ output port (port 0B)	For the HALT mode releasing	Mode selection pin	High impedance (input mode)
$P0B_1$		RLS_{STOP}	MD_1		For the STOP mode releasing		
$P0B_2$		MD_2					
$P0C_0$	Input/ output	D_4		• CMOS (push-pull) 4-bit input/output port (port 0C)		8-bit data input/ output pin (high-order 4 bits)	High impedance (input mode)
$P0C_1$		D_5					
$P0C_2$		D_6					
$P0C_3$		D_7					
$P0D_0$	Input/ output	D_0		• CMOS (push-pull) 4-bit input/output port (port 0D)		8-bit data input/ output pin (low-order 4-bits)	High impedance (input mode)
$P0D_1$		D_1					
$P0D_2$		D_2					
$P0D_3$		D_3					

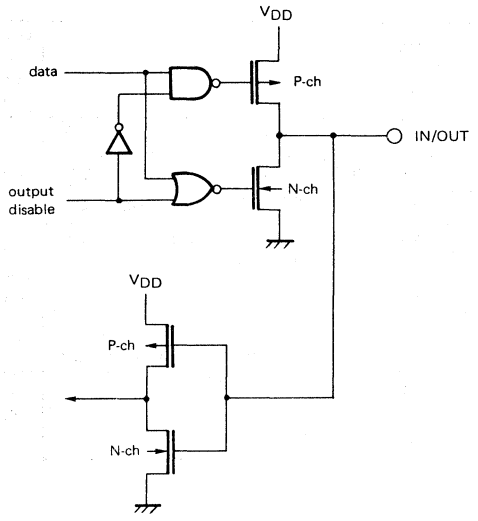
- Non-port pins

PIN NAME	INPUT/ OUTPUT	DUAL FUNCTION PIN	FUNCTION	When writing to program memory or verifying its contents
$\overline{RESET}$	Input	V_{PP}	System reset input pin	Voltage is applied to this pin (+12.5 V)
V_{DD}			Positive power supply pin	Positive power supply pin (+6.0 V)
GND			GND pin	GND pin
X_{IN}			Pins to be connected to the system clock resonator	Program memory address update
X_{OUT}		MD_3	Pins to be connected to the system clock resonator	Mode selection pin

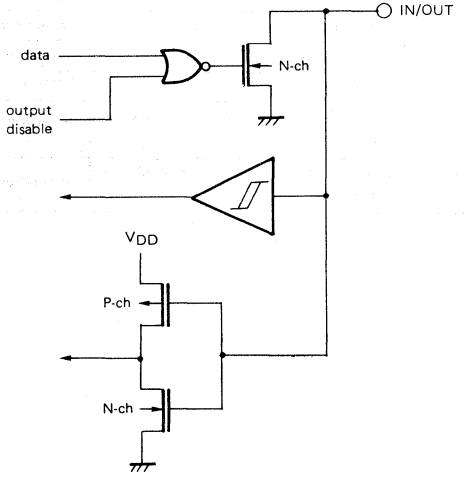
PIN INPUT/OUTPUT CIRCUITS

Following are schematics of the input/output circuits of the pins of the μPD17P103.

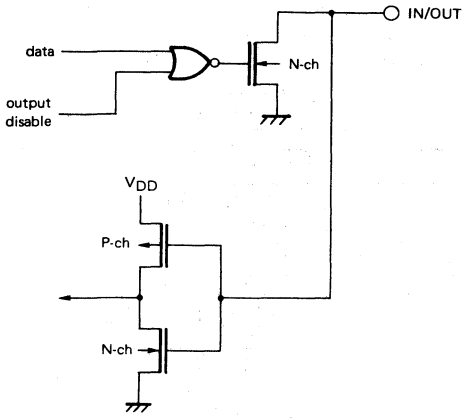
(1) P0C and P0D



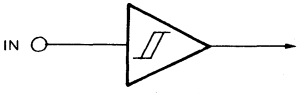
(2) $P0B_0$ and $P0B_1$



(3) $P0B_2$



(4) $\overline{RESET}$



9. DIFFERENCES BETWEEN THE μPD17P103 AND μPD17103

The μPD17P103 is a one-time PROM version of the μPD17103, in which the internal mask ROM is replaced with a one-time PROM. The μPD17P103 has the same CPU functions and internal hardwares as those of μPD17103 except for its program memory and mask option. Table 9-1 lists the differences between them.

Table 9-1 Differences between μPD17P103 and μPD17103

ITEM	μPD17P103	μPD17103
ROM	One-time PROM 512 x 16 bits	Mask ROM 512 x 16 bits
Pull-up resistors of pins $P0B_0$ to $P0B_2$	None	Mask option
Pull-up resistors of $\overline{RESET}$ pin	None	Mask option
Connection pin	V_{PP} pin and operation mode selection pins are provided.	V_{PP} pin and operation mode selection pins are not provided.
Power supply	2.7 to 6.0 V (at 2 MHz) 4.5 to 6.0 V (at 8 MHz)	
Package	16-pin DIP 16-pin SOP	

10. WRITING TO AND VERIFYING ONE-TIME PROM (PROGRAM MEMORY)

The μPD17P103's internal program memory consists of a 512 x 16 bit one-time PROM.

Writing to the one-time PROM or verifying the contents of the PROM is accomplished using the pins shown in the table below. Note that address inputs are not used; instead, the address is updated using the clock input from the X_{IN} pin.

PIN NAME	FUNCTION
V_{PP}	Voltage is applied to this pin when writing to program memory or verifying its contents.
X_{IN}	Input pin for address update clock used when writing to program memory or verifying its contents.
MD_0 to MD_3	Pins that turn to input pins and are used as operation mode selection pins when writing to program memory or verifying its contents
D_0 to D_7	Input/output pins for 8-bit data used when writing to program memory or verifying its contents

10.1 Program Memory Write/Verify Modes

If +6 V is applied to the V_{DD} pin and +12.5 V is applied to the V_{PP} pin after a certain duration of reset status (V_{DD} = 5 V, $\overline{RESET}$ = 0 V), the μPD17P103 enters program memory write/verify mode. A specific operating mode is then selected by setting the MD_0 through MD_3 pins as follows. Set the other unused pins to GND level by means of pull-down resistors.

Operating mode specification						Operating mode
V_{PP}	V_{DD}	MD_0	MD_1	MD_2	MD_3	
+12.5 V	+6 V	H	L	H	L	Program memory address clear mode
		L	H	H	H	Write mode
		L	L	H	H	Verify mode
		H	X	H	H	Program inhibit mode

X: L (low) or H (high)

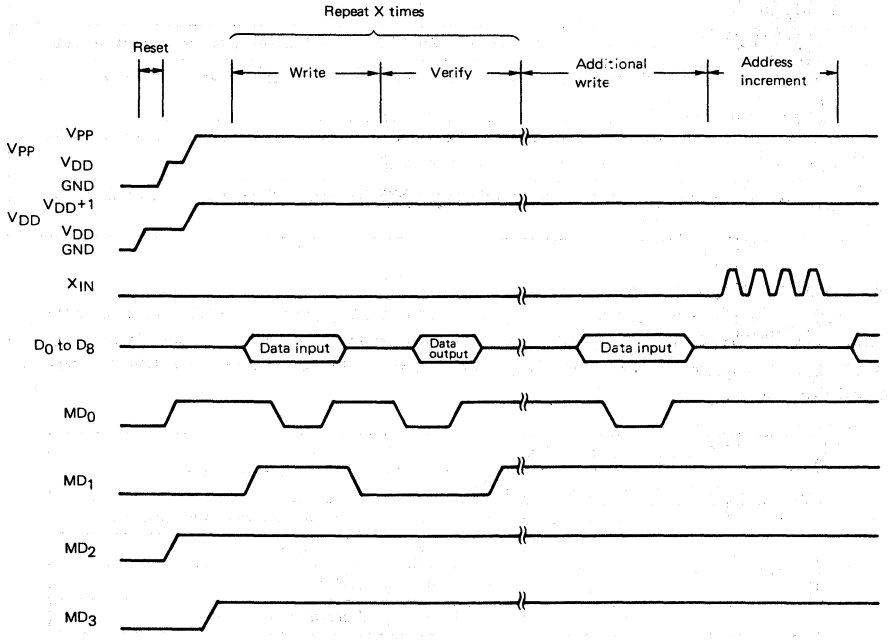
10.2 Writing to Program Memory

The procedure for writing to program memory is described below: high-speed write is possible.

(1) Pull low the levels on all unused pins to GND by means of resistors. Bring X_{IN} to low level.
(2) Apply 5 V to V_{DD} and bring V_{PP} to low level.
(3) Wait 10 μs. Then apply 5 V to V_{PP}.
(4) Set the mode selection pins to program memory address clear mode.
(5) Apply 6 V to V_{DD} and 12.5 V to V_{PP}.
(6) Select program inhibit mode.
(7) Write data in 1 ms write mode.
(8) Select program inhibit mode.
(9) Select verify mode. If the write operation is found successful, proceed to step (10). If the operation is found unsuccessful, repeat steps (7) to (9).
(10) Perform additional write for (number of repetitions of steps (7) to (9)) x 1 ms.
(11) Select program inhibit mode.
(12) Increment the program memory address by one on reception of four pulses on the X_{IN} pin.

(13) Repeat steps (7) to (12) until the last address is reached.
(14) Select program memory address clear mode.
(15) Apply 5 V to the V_{DD} and V_{PP} pins.
(16) Turn power off.

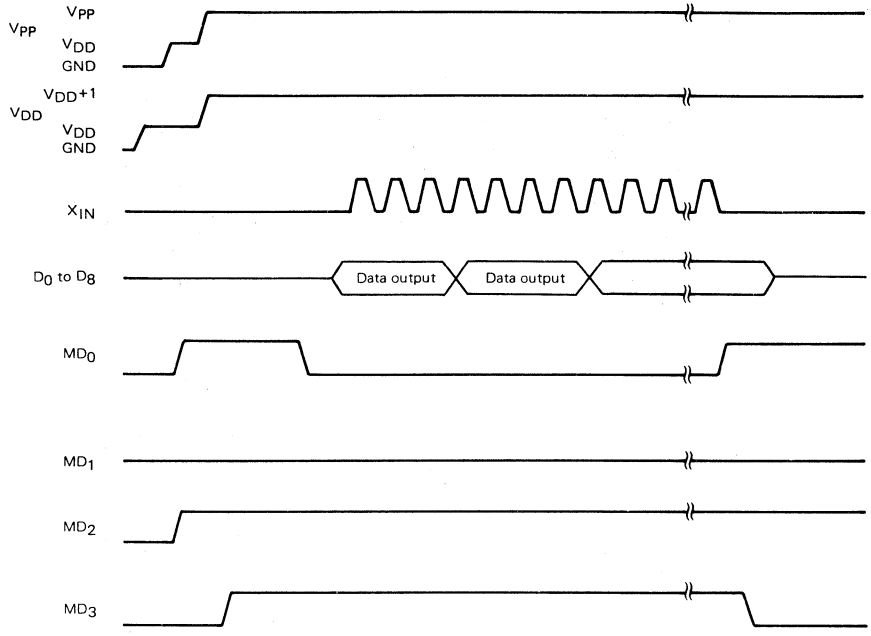
The timing for steps (2) to (12) is shown below.



10.3 Reading Program Memory

(1) Pull low the levels of all unused pins to GND by means of resistors. Bring X_{IN} to low level.
(2) Apply 5 V to V_{DD} and bring V_{PP} to low level.
(3) Wait 10 μs. Then apply 5 V to V_{PP}.
(4) Set the mode selection pins to program memory address clear mode.
(5) Apply 6 V to V_{DD} and 12.5 V to V_{PP}.
(6) Select program inhibit mode.
(7) Select verify mode. Data is output sequentially one address at a time for each cycle of four clock pulses on the X_{IN} pin.
(8) Select program inhibit mode.
(9) Select program memory address clear mode.
(10) Apply 5 V to the V_{DD} and V_{PP} pins.
(11) Turn power off.

The timing for steps (2) to (9) is shown below.



11. RESERVED WORDS

Table 11-1 lists the reserved words defined in the μPD17P103 device file (AS17103).

Table 11-1 Reserved Words

Name	Attribute	Value	Read/write	Description
P0B0	FLG	0.71H.0	Read/write	Bit 0 of port 0B
P0B1	FLG	0.71H.1	Read/write	Bit 1 of port 0B
P0B2	FLG	0.71H.2	Read/write	Bit 2 of port 0B
*P0B3	FLG	0.71H.3	Read	Always set to 0
P0C0	FLG	0.72H.0	Read/write	Bit 0 of port 0C
P0C1	FLG	0.72H.1	Read/write	Bit 1 of port 0C
P0C2	FLG	0.72H.2	Read/write	Bit 2 of port 0C
P0C3	FLG	0.72H.3	Read/write	Bit 3 of port 0C
P0D0	FLG	0.73H.0	Read/write	Bit 0 of port 0D
P0D1	FLG	0.73H.1	Read/write	Bit 1 of port 0D
P0D2	FLG	0.73H.2	Read/write	Bit 2 of port 0D
P0D3	FLG	0.73H.3	Read/write	Bit 3 of port 0D
BCD	FLG	0.7EH.0	Read/write	BCD arithmetic flag
PSW	MEM	0.7FH	Read/write	Program status word
Z	FLG	0.7FH.1	Read/write	Zero flag
CY	FLG	0.7FH.2	Read/write	Carry flag
CMP	FLG	0.7FH.3	Read/write	Compare flag

* Although P0B3 does not exist in the μPD17P103, it is defined as a ready-only flag so that it is treated as a dummy bit when a built-in macro is used.

12. INSTRUCTION SET

12.1 Instruction Set List

$b_{14}-b_{11}$ \ b_{15}		0		1	
BIN	HEX				
0 0 0 0	0	ADD	r, m	ADD	m, #i
0 0 0 1	1	SUB	r, m	SUB	m, #i
0 0 1 0	2	ADDC	r, m	ADDC	m, #i
0 0 1 1	3	SUBC	r, m	SUBC	m, #i
0 1 0 0	4	AND	r, m	AND	m, #i
0 1 0 1	5	XOR	r, m	XOR	m, #i
0 1 1 0	6	OR	r, m	OR	m, #i
0 1 1 1	7	RET RETSK RORC STOP HALT NOP	 r s h 		
1 0 0 0	8	LD	r, m	ST	m, r
1 0 0 1	9	SKE	m, #i	SKGE	m, #i
1 0 1 0	A				
1 0 1 1	B	SKNE	m, #i	SKLT	m, #i
1 1 0 0	C	BR	addr	CALL	addr
1 1 0 1	D			MOV	m, #i
1 1 1 0	E			SKT	m, #n
1 1 1 1	F			SKF	m, #n

12.2 INSTRUCTIONS LIST

Legend:

M	: One of data memory	n	: Bit position : 4 bits
m	: Data memory address specified by [m_H, m_L] of each bank	addr	: One of program memory address ; 11 bits
m_H	: Data memory address high (row address) ; 3 bits	a_H	: Program memory address high ; 3 bits
m_L	: Data memory address low (column address) ; 4 bits	a_M	: Program memory address middle ; 4 bits
R	: One of general register specified by [(RP), r]	a_L	: Program memory address low ; 4 bits
r	: General register address low (column address) ; 4 bits	CY	: Carry flag
RP	: General register pointer	CMP	: Compare flag
PC	: Program counter	s	: Stop release condition
SP	: Stack pointer	h	: Halt release condition
STACK	: Stack specified by (SP)	[ ]	: Address of M,R
i	: Immediate data ; 4 bits	( )	: Contents of M,R

Type	Mnemonic	Operand	Function	Operation	Machine code			
					Op code	3 bits	4 bits	4 bits
Add	ADD	r,m	Add memory to register	R← (R) + (M)	00000	m_H	m_L	r
		m,#i	Add immediate data to memory	M← (M) + i	10000	m_H	m_L	i
	ADDC	r,m	Add memory to register with carry	R← (R) + (M) + (CY)	00010	m_H	m_L	r
		m,#i	Add immediate data to memory with carry	R← (M) + i+ (CY)	10010	m_H	m_L	i
Subtract	SUB	r,m	Subtract memory from register	R← (R) − (M)	00001	m_H	m_L	r
		m,#i	Subtract immediate data from memory	M← (M) − i	10001	m_H	m_L	i
	SUBC	r,m	Subtract memory from register with borrow	R← (R) − (M) − (CY)	00011	m_H	m_L	r
		m,#i	Subtract immediate data from memory with borrow	M← (M) − i − (CY)	10011	m_H	m_L	i
Compare	SKE	m,#i	Skip if memory equal to immediate data	M−i, skip if zero	01001	m_H	m_L	i
	SKGE	m,#i	Skip if memory greater than or equal to immediate data	M−i, skip if not borrow	11001	m_H	m_L	i
	SKLT	m,#i	Skip if memory less than immediate data	M−i, skip if borrow	11011	m_H	m_L	i
	SKNE	m,#i	Skip if memory not equal to immediate data	M−i, skip if not zero	01011	m_H	m_L	i
Logical operation	AND	m,#i	Logical AND of memory and immediate data	M← (M) AND i	10100	m_H	m_L	i
		r,m	Logical AND of register and memory	R← (R) AND (M)	00100	m_H	m_L	r
	OR	m,#i	Logical OR of memory and immediate data	M← (M) OR i	10110	m_H	m_L	i
		r,m	Logical OR of register and memory	R← (R) OR (M)	00110	m_H	m_L	r
	XOR	m,#i	Logical XOR of memory and immediate data	M← (M) XOR i	10101	m_H	m_L	i
		r,m	Logical XOR of register and memory	R← (R) XOR (M)	00101	m_H	m_L	r
Transfer	LD	r,m	Load memory to register	R← (M)	01000	m_H	m_L	r
	ST	m,r	Store register to memory	(M)←R	11000	m_H	m_L	r
	MOV	m,#i	Move immediate data to memory	M←i	11101	m_H	m_L	i
Test	SKT	m,#n	Test memory bits, then skip if all bits specified are true	CMP←0 skip if M_n=all "1"	11110	m_H	m_L	n
	SKF	m,#n	Test memory bits, then skip if all bits specified are false	CMP←0 skip if M_n=all "0"	11111	m_H	m_L	n

Type	Mnemonic	Operand	Function	Operation	Machine code			
					Op code	3 bits	4 bits	4 bits
Branch	BR	addr	Jump to the address	PC←ADDR	01100	a_H	a_M	a_L
Shift	RORC	r	Rotate register right with carry	(CY)→(R)→CY	00111	000	0111	r
Subroutine	CALL	addr	Call subroutine	SP←(SP) − 1 STACK←((PC) + 1), PC←ADDR	11100	a_H	a_M	a_L
	RET		Return to main routine from subroutine	PC←(STACK), SP←(SP) + 1	00111	000	1110	0000
	RETSK		Return to main routine from subroutine, then skip unconditionally	PC←(STACK), SP←(SP) + 1 and skip	00111	001	1110	0000
Miscellaneous	STOP	s	Stop clock	STOP	00111	010	1111	s
	HALT	h	Halt the CPU, restart by condition h	HALT	00111	011	1111	h
	NOP		No operation	No Operation	00111	100	1111	0000

13. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage	V_{DD}			−0.3 to +7.0	V
Supply Voltage	V_{PP}			−0.3 to +13.5	V
Input Voltage	V_I	P0C, P0D		−0.3 to V_{DD} +0.3	V
		P0B		−0.3 to +11	V
Output Voltage	V_O	P0C, P0D		−0.3 to V_{DD} +0.3	V
		P0B		−0.3 to +11	V
High-Level Output Current	I_{OH}	Each of P0B, P0C, P0D		−5	mA
		Total of all pins		−15	mA
Low-Level Output Current	I_{OL}	Each of P0B, P0C, P0D		30	mA
		Total of all pins		100	mA
Operating Temperature	T_{opt}			−40 to +85	°C
Storage Temperature	T_stg			−65 to +150	°C
Power Consumption	P_d	T_a = 85 °C	16-pin DIP	400	mW
			16-pin SOP	190	

CAPACITANCE (T_a = 25 °C, V_{DD} = 0 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Input Capacitance	C_{IN}			15	pF	f=1 MHz
I/O(*) Capacitance	C_{IO}			15	pF	0 V for pins other than pins to be measured

*: Input/Output

DC CHARACTERISTICS (T_a = −40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION	
High-Level Input Voltage	V_{IH1}	0.7 V_{DD}		V_{DD}	V	Other than the following pins and port	
	V_{IH2}	0.8 V_{DD}		V_{DD}	V	P0B and $\overline{RESET}$	
	V_{IH3}	0.8 V_{DD}		9	V	P0B	(*)
	V_{IH4}	V_{DD}-0.5		V_{DD}	V	X_{IN}	
Low-Level Input Voltage	V_{IL1}	0		0.3 V_{DD}	V	Other than the following pins and port	
	V_{IL2}	0		0.2 V_{DD}	V	P0B and $\overline{RESET}$	
	V_{IL3}	0		0.5	V	X_{IN}	
High-Level Output Voltage on P0C and P0D	V_{OH}	V_{DD}-2.0			V	V_{DD}=4.5 to 6.0 V, I_{OH}=−2 mA	
		V_{DD}-1.0			V	I_{OH}=−200 μA	
Low-Level Output Voltage on P0B, P0C, and P0D	V_{OL}			2.0	V	V_{DD}=4.5 to 6.0 V, I_{OL}=15 mA	
				0.5	V	I_{OL}=600 μA	
High-Level Input Leakage Current on P0B, P0C, and P0D	I_{LIH1}			5	μA	V_{IN}=V_{DD}	
	I_{LIH2}			10	μA	V_{IN}=9 V	(*)
Low-Level Input Leakage Current on P0B, P0C, and P0D	I_{LIL}			−5	μA	V_{IN}=0 V	
High-Level Output Leakage Current on P0B, P0C, and P0D	I_{LOH1}			5	μA	V_{OUT}=V_{DD}	
	I_{LOH2}			10	μA	V_{OUT}=9 V	(*)
Low-Level Output Leakage Current on P0B, P0C, and P0D	I_{LOL}			−5	μA	V_{OUT}=0 V	
Power Supply Current	I_{DD1}		1.5	4.5	mA	Operation mode	V_{DD}=5.0 V ±10 %, f_{CC}=8.0 MHz
			250	750	μA		V_{DD}=3.0 V ±10 %, f_{CC}=2.0 MHz
	I_{DD2}		1.0	3.0	mA	HALT mode	V_{DD}=5.0 V ±10 %, f_{CC}=8.0 MHz
			200	600	μA		V_{DD}=3.0 V ±10 %, f_{CC}=2.0 MHz
	I_{DD3}		0.1	10	μA	STOP mode	V_{DD}=5.0 V ±10 %,
			0.1	5	μA		V_{DD}=3.0 V ±10 %

*: When N-ch open-drain input/output is selected.

CHARACTERISTICS OF DATA MEMORY FOR HOLDING DATA ON LOW SUPPLY VOLTAGE IN THE STOP MODE (T_a = −40 to +85 °C)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Data Hold Supply Voltage	V_{DDDR}	2.0		6.0	V	
Data Hold Supply Current	I_{DDDR}		0.1	5.0	μA	V_{DDDR} = 2.0 V
Release Signal Set Time	t_{SREL}	0			μs	

AC CHARACTERISTICS (T_a = −40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Internal Clock Cycle Time	T_{CY}	1.9		33	μs	V_{DD} = 4.5 to 6.0 V
		7.6		33	μs	
High/Low Level Width on $P0B_0$ and $P0B_1$	T_{PBH} T_{PBL}	10			μs	
High/Low Level Width on $\overline{RESET}$	T_{RSH} T_{RSL}	10			μs	

DC PROGRAMING CHARACTERISTICS (T_a = 25 °C, V_{DD} = 6.0 ±0.25 V, V_{PP} = 12.5 ±0.5 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Input Voltage High	V_{IH1}	0.7-V_{DD}		V_{DD}	V	Except X_{IN}
	V_{IH2}	V_{DD}-0.5		V_{DD}	V	X_{IN}
Input Voltage Low	V_{IL1}	0		0.3 V_{DD}	V	Except X_{IN}
	V_{IL2}	0		0.4	V	X_{IN}
Input Leakage Current	I_{LI}			10	μA	V_{IN} = V_{IL} or V_{IH}
Output Voltage High	V_{OH}	V_{DD}-1.0			V	I_{OH} = −1 mA
Output Voltage Low	V_{OL}			0.4	V	I_{OL} = 1.6 mA
V_{DD} Power Supply Current	I_{DD}			30	mA	
V_{PP} Power Supply Current	I_{PP}			30	mA	MD0 = V_{IL}, MD1 = V_{IH}

Notes 1: V_{PP} must be under +13.5 V including overshoot.

2: V_{DD} must be applied before V_{PP} on and must be off after V_{PP} off.

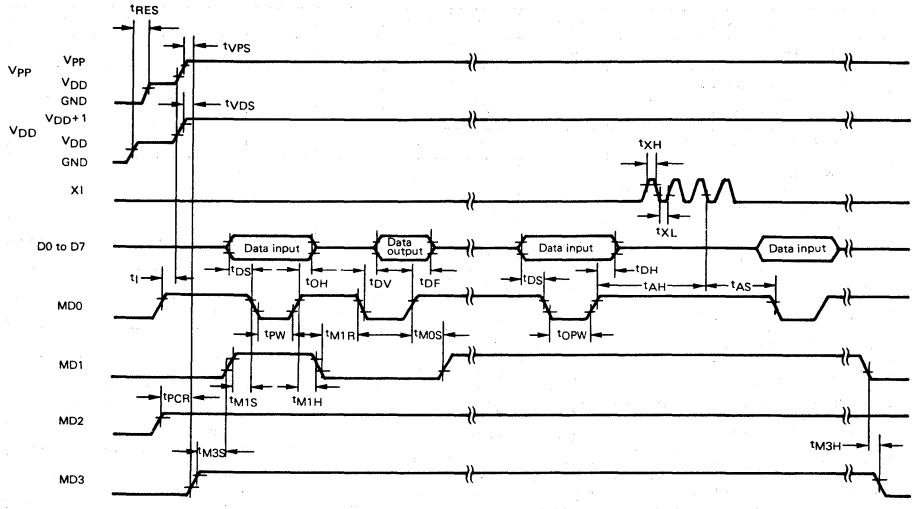
AC PROGRAMMING CHARACTERISTICS
(T_a = 25 °C, V_{DD} = 6.0 ±0.25 V, V_{PP} = 12.5 ±0.5 V)

CHARACTERISTICS	SYMBOL	*1	MIN.	TYP.	MAX.	UNIT	CONDITION
Address Set Up Time(*2) to MD0 ↓	t_{AS}	t_{AS}	2			μs	
MD1 Setup Time to MD0 ↓	t_{M1S}	t_{OES}	2			μs	
Data Setup Time to MD0 ↓	t_{DS}	t_{DS}	2			μs	
Address Hold Time(*2) to MD0 ↑	t_{AH}	t_{AH}	2			μs	
Data Hold Time to MD0 ↑	t_{DH}	t_{DH}	2			μs	
Data Output Float Delay Time From MD0 ↑→	t_{DF}	t_{DF}	0		130	ns	
V_{PP} Setup Time to MD3 ↑	t_{VPS}	t_{VPS}	2			μs	
V_{DD} Setup Time to MD3 ↑	t_{VDS}	t_{VCS}	2			μs	
Initial Program Pulse Width	t_{PW}	t_{PW}	0.95	1.0	1.05	ms	
Additional Program Pulse Width	t_{OPW}	t_{OPW}	0.95		21.0	ms	
MD0 Setup Time to MD1 ↑	t_{MOS}	t_{CES}	2			μs	
Data Output Delay Time From MD0 ↓→	t_{DV}	t_{DV}			1	μs	MD0 = MD1 = V_{IL}
MD1 Hold Time to MD0 ↑	t_{M1H}	t_{OEH}	2			μs	$t_{M1H} + t_{M1R} \geqq 50$ μs
MD1 Recovery Time to MD0 ↓	t_{M1R}	t_{OR}	2			μs	
Program Counter Reset Time	t_{PCR}	–	10			μs	
X_{IN} Input High, Low Level Range	t_{XH}, t_{XL}	–	0.125			μs	
X_{IN} Input Frequency	f_X	–			4.19	MHz	
Initial Mode Set Time	t_I	–	2			μs	
MD3 Setup Time to MD1 ↑	t_{M3S}	–	2			μs	
MD3 Hold Time to MD1 ↓	t_{M3H}	–	2			μs	
MD3 Setup Time to MD0 ↓	t_{M3SR}	–	2			μs	Read program memory
Data Output Delay Time From Address(*2)	t_{DAD}	t_{ACC}	2			μs	Read program memory
Data Output Hold Time From Address(*2)	t_{HAD}	t_{OH}	0		130	ns	Read program memory
MD3 Hold Time to MD0 ↑	t_{M3HR}	–	2			μs	Read program memory
Data Output Float Delay Time From MD3 ↓→	t_{DFR}	–	2			μs	Read program memory
Reset Setup Time	t_{RES}		10			μs	

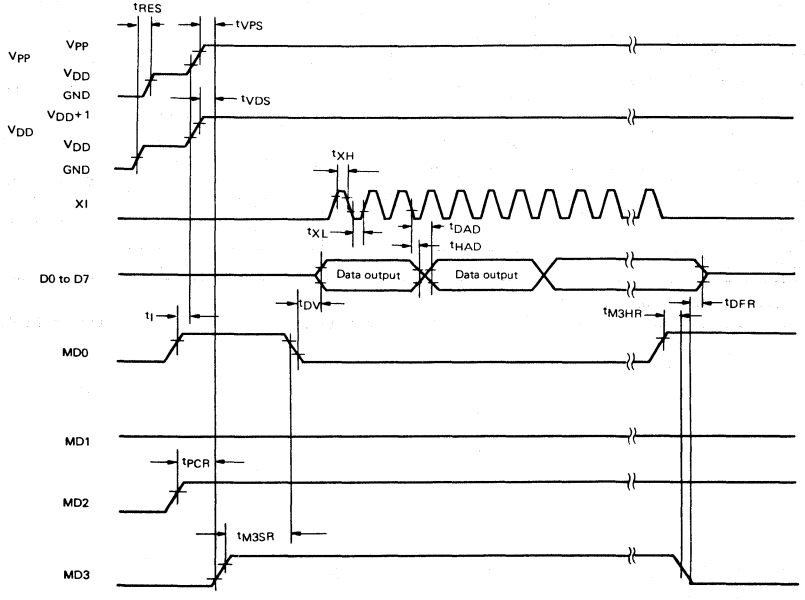
*1: Symbols for corresponding μPD27C256.

*2: Internal address signal is incremented by one at the falling edge of the third X_{IN} input, and it is not connected to the pin.

Write program memory timing



Read program memory timing



4-BIT SINGLE-CHIP MICROCONTROLLER

The μPD17P104 is a tiny microcontroller consisting of a 1K-byte ROM, 16-word RAM, and 16 input/output ports. It is a one-time PROM version of the μPD17104, whose internal mask ROM is replaced with a one-time PROM.

Two μPD17P104 models are available: μPD17P104CS and μPD17P104GS, which allow a program to be written only once. They are suitable for evaluation of μPD17104 and for small-scale production.

The μPD17000 architecture of the CPU uses general registers so that data memory can be manipulated directly for effective programming. Every instruction is 1 word long, consisting of 16 bits.

FEATURES

- Compatible with the μPD17104
- Program memory (one-time PROM): 1K bytes (512 words x 16 bits)
- Data memory (RAM): 16 words x 4 bits
- Input/output ports: 16 ports (including four N-ch open-drain outputs)
- Instruction execution time: 2 μs (with 8 MHz crystal or ceramic resonator connected)
- Number of instructions: 24 (Each instruction is 1 word long.)
- Stack level: 1
- A standby function is supported (with the STOP and HALT instructions).
- Data memory can retain data on low voltage (2.0 V at minimum).
- An oscillator is included for the system clock (for crystal or ceramic resonator).
- Operating supply voltage: 2.7 to 6.0 V (at 2 MHz)
  4.5 to 6.0 V (at 8 MHz)

APPLICATIONS

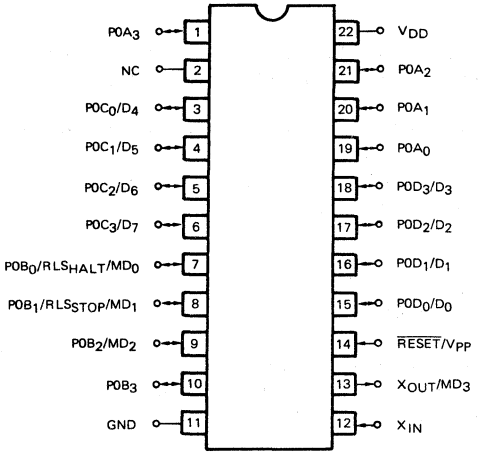
- Controlling electric appliances or toys
- Providing general-purpose logic ICs in one chip

ORDERING INFORMATION

Order Code	Package
μPD17P104CS	22-pin plastic shrink DIP (300 mil)
μPD17P104GS	24-pin plastic SOP (300 mil)

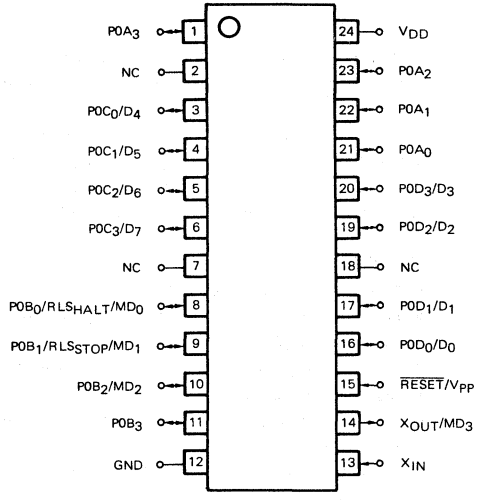
PIN CONFIGURATION (Top View)

μPD17P104CS



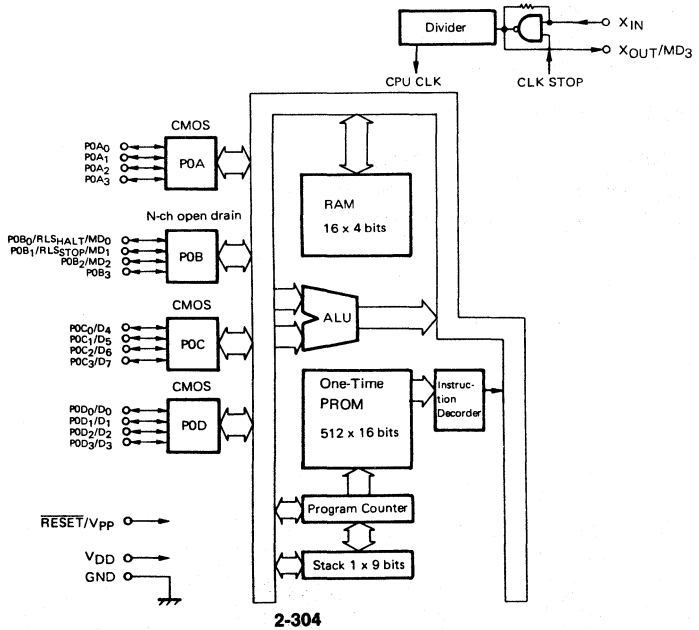
22-pin plastic shrink DIP

μPD17P104GS



24-pin plastic SOP

BLOCK DIAGRAM



PIN FUNCTIONS

- Port pins

PIN NAME	INPUT/ OUTPUT	DUAL FUNCTION PIN		FUNCTION		When writing to program memory or verifying its contents	WHEN RESET
$P0A_0$	Input/output			• CMOS (push-pull) 4-bit input/ output port (port 0A)		Pull down	High impedance (input mode)
$P0A_1$							
$P0A_2$							
$P0A_3$							
$P0B_0$	Input/output	RLS_{HALT}	MD_0	• N-ch open-drain 4-bit input/ output port (port 0B)	For the HALT mode releasing	Mode selection pin	High impedance (input mode)
$P0B_1$		RLS_{STOP}	MD_1		For the STOP mode releasing		
$P0B_2$		MD_2					
$P0B_3$						Pull down	
$P0C_0$	Input/output	D_4		• CMOS (push-pull) 4-bit input/ output port (port 0C)		8-bit data input/output pin (high-order 4 bits)	High impedance (input mode)
$P0C_1$		D_5					
$P0C_2$		D_6					
$P0C_3$		D_7					
$P0D_0$	Input/output	D_0		• CMOS (push-pull) 4-bit input/ output port (port 0D)		8-bit data input/output pin (low-order 4-bits)	High impedance (input mode)
$P0D_1$		D_1					
$P0D_2$		D_2					
$P0D_3$		D_3					

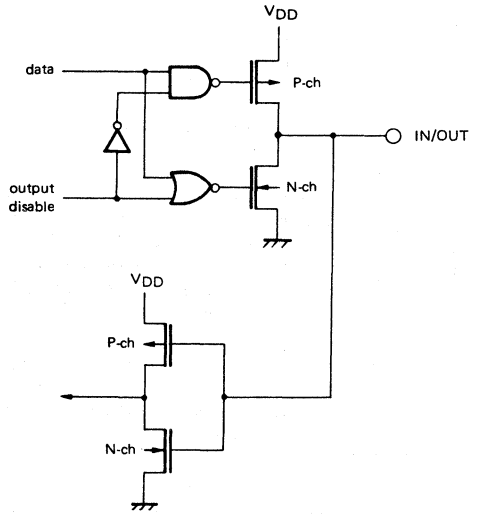
- Non-port pins

PIN NAME	INPUT/ OUTPUT	DUAL FUNCTION PIN	FUNCTION	When writing to program memory or verifying its contents
$\overline{RESET}$	Input	V_{PP}	System reset input pin	Voltage is applied to this pin (+12.5 V)
V_{DD}			Positive power supply pin	Positive power supply pin (+6.0 V)
GND			GND pin	GND pin
X_{IN}			Pins to be connected to the system clock resonator	Program memory address update
X_{OUT}		MD_3	Pins to be connected to the system clock resonator	Mode selection pin
NC			NC pin is not connected internally.	

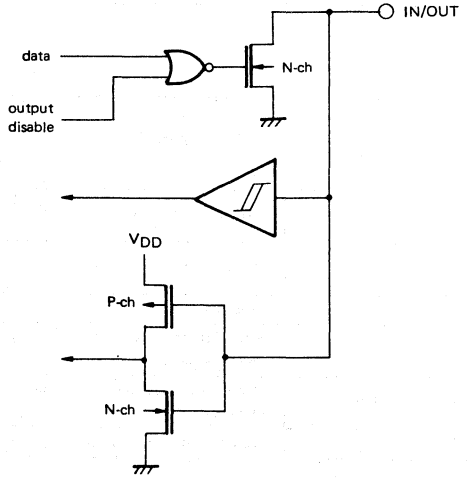
PIN INPUT/OUTPUT CIRCUITS

Following are schematics of the input/output circuits of the pins of the μPD17P104.

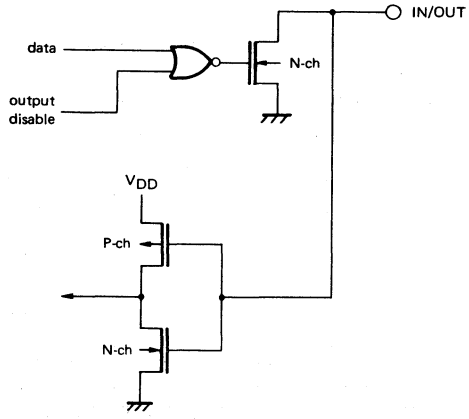
(1) POC and POD



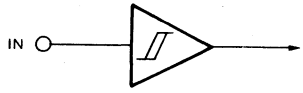
(2) POB_0 and POB_1



(3) POB_2 and POB_3



(4) $\overline{RESET}$



9. DIFFERENCES BETWEEN THE μPD17P104 AND μPD17104

The μPD17P104 is a one-time PROM version of the μPD17104, in which the internal mask ROM is replaced with a one-time PROM. The μPD17P104 has the same CPU functions and internal hardwares as those of μPD17104 except for its program memory and mask option. Table 9-1 lists the differences between them.

Table 9-1 Differences between μPD17P104 and μPD17104

ITEM	μPD17P104	μPD17104
ROM	One-time PROM 512 x 16 bits	Mask ROM 512 x 16 bits
Pull-up resistors of pins $P0B_0$ to $P0B_3$	None	Mask option
Pull-up resistors of $\overline{RESET}$ pin	None	Mask option
Connection pin	V_{PP} pin and operation mode selection pins are provided.	V_{PP} pin and operation mode selection pins are not provided.
Power supply	2.7 to 6.0 V (at 2 MHz) 4.5 to 6.0 V (at 8 MHz)	
Package	22-pin plastic shrink DIP 24-pin plastic SOP	
Waiting time for the operation mode	16 clock pulses	8 clock pulses

10. WRITING TO AND VERIFYING ONE-TIME PROM (PROGRAM MEMORY)

The μPD17P104's internal program memory consists of a 512 x 16 bit one-time PROM.

Writing to the one-time PROM or verifying the contents of the PROM is accomplished using the pins shown in the table below. Note that address inputs are not used; instead, the address is updated using the clock input from the X_{IN} pin.

PIN NAME	FUNCTION
V_{PP}	Voltage is applied to this pin when writing to program memory or verifying its contents.
X_{IN}	Input pin for address update clock used when writing to program memory or verifying its contents
MD_0 to MD_3	Pins that turn to input pins and are used as operation mode selection pins when writing to program memory or verifying its contents
D_0 to D_7	Input/output pins for 8-bit data used when writing to program memory or verifying its contents

10.1 PROGRAM MEMORY WRITE/VERIFY MODES

If +6 V is applied to the V_{DD} pin and +12.5 V is applied to the V_{PP} pin after a certain duration of reset status (V_{DD} = 5 V, $\overline{RESET}$ = 0 V), the μPD17P104 enters program memory write/verify mode. A specific operating mode is then selected by setting the MD_0 through MD_3 pins as follows. Set the other unused pins to GND level by means of pull-down resistors.

OPERATING MODE SPECIFICATION						OPERATING MODE
V_{PP}	V_{DD}	MD_0	MD_1	MD_2	MD_3	
+12.5 V	+6 V	H	L	H	L	Program memory address clear mode
		L	H	H	H	Write mode
		L	L	H	H	Verify mode
		H	X	H	H	Program inhibit mode

X: L (low) or H (high)

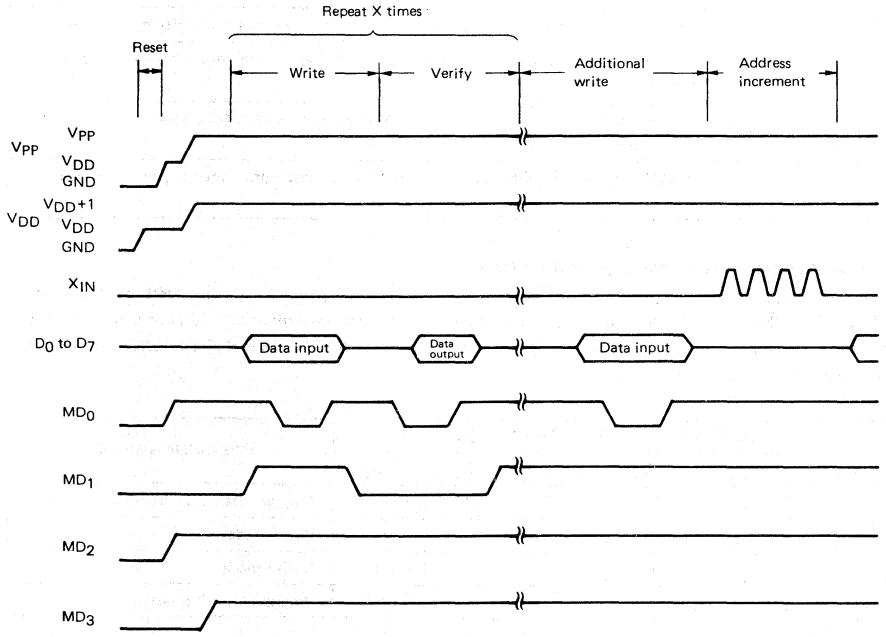
10.2 WRITING TO PROGRAM MEMORY

The procedure for writing to program memory is described below; high-speed write is possible.

(1) Pull low the levels on all unused pins to GND by means of resistors. Bring X_{IN} to low level.
(2) Apply 5 V to V_{DD} and bring V_{PP} to low level.
(3) Wait 10 μs. Then apply 5 V to V_{PP}.
(4) Set the mode selection pins to program memory address clear mode.
(5) Apply 6 V to V_{DD} and 12.5 V to V_{PP}.
(6) Select program inhibit mode.
(7) Write data in 1 ms write mode.
(8) Select program inhibit mode.
(9) Select verify mode. If the write operation is found successful, proceed to step (10). If the operation is found unsuccessful, repeat steps (7) to (9).
(10) Perform additional write for (number of repetitions of steps (7) to (9)) x 1 ms.
(11) Select program inhibit mode.

(12) Increment the program memory address by one on reception of four pulses on the X_{IN} pin.
(13) Repeat steps (7) to (12) until the last address is reached.
(14) Select program memory address clear mode.
(15) Apply 5 V to the V_{DD} and V_{PP} pins.
(16) Turn power off.

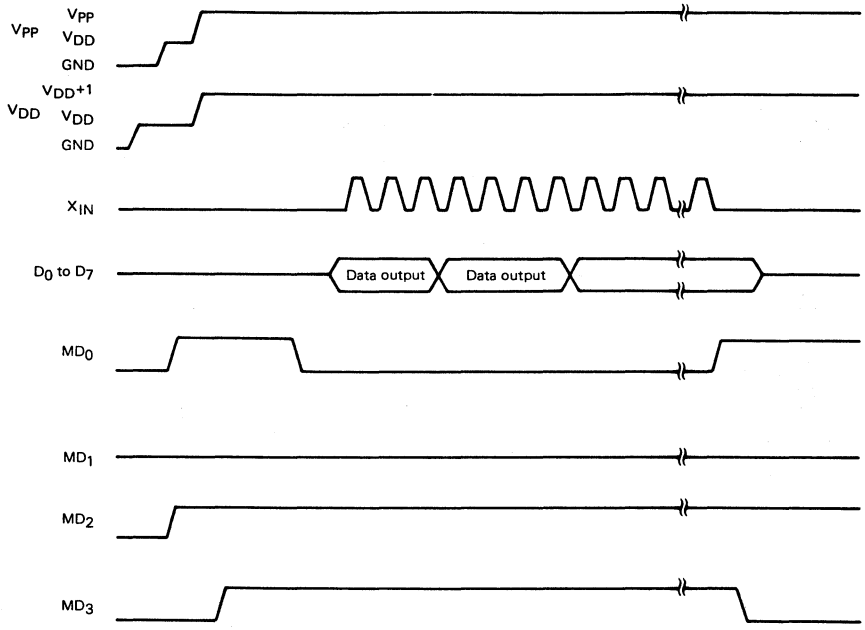
The timing for steps (2) to (12) is shown below.



10.3 READING PROGRAM MEMORY

(1) Pull low the levels of all unused pins to GND by means of resistors. Bring X_{IN} to low level.
(2) Apply 5 V to V_{DD} and bring V_{PP} to low level.
(3) Wait 10 μs. Then apply 5 V to V_{PP}.
(4) Set the mode selection pins to program memory address clear mode.
(5) Apply 6 V to V_{DD} and 12.5 V to V_{PP}.
(6) Select program inhibit mode.
(7) Select verify mode. Data is output sequentially one address at a time for each cycle of four clock pulses on the X_{IN} pin.
(8) Select program inhibit mode.
(9) Select program memory address clear mode.
(10) Apply 5 V to the V_{DD} and V_{PP} pins.
(11) Turn power off.

The timing for steps (2) to (9) is shown below.



11. ASSEMBLER RESERVED WORDS

Table 11-1 lists the reserved words defined in the μPD17P104 device file (AS17104).

Table 11-1 Reserved Words

Name	Attribute	Value	Read/write	Description
P0A0	FLG	0.70H.0	Read/write	Bit 0 of port 0A
P0A1	FLG	0.70H.1	Read/write	Bit 1 of port 0A
P0A2	FLG	0.70H.2	Read/write	Bit 2 of port 0A
P0A3	FLG	0.70H.3	Read/write	Bit 3 of port 0A
P0B0	FLG	0.71H.0	Read/write	Bit 0 of port 0B
P0B1	FLG	0.71H.1	Read/write	Bit 1 of port 0B
P0B2	FLG	0.71H.2	Read/write	Bit 2 of port 0B
P0B3	FLG	0.71H.3	Read/write	Bit 3 of port 0B
P0C0	FLG	0.72H.0	Read/write	Bit 0 of port 0C
P0C1	FLG	0.72H.1	Read/write	Bit 1 of port 0C
P0C2	FLG	0.72H.2	Read/write	Bit 2 of port 0C
P0C3	FLG	0.72H.3	Read/write	Bit 3 of port 0C
P0D0	FLG	0.73H.0	Read/write	Bit 0 of port 0D
P0D1	FLG	0.73H.1	Read/write	Bit 1 of port 0D
P0D2	FLG	0.73H.2	Read/write	Bit 2 of port 0D
P0D3	FLG	0.73H.3	Read/write	Bit 3 of port 0D
BCD	FLG	0.7EH.0	Read/write	BCD arithmetic flag
PSW	MEM	0.7FH	Read/write	Program status word
Z	FLG	0.7FH.1	Read/write	Zero flag
CY	FLG	0.7FH.2	Read/write	Carry flag
CMP	FLG	0.7FH.3	Read/write	Compare flag

12. INSTRUCTION SET

12.1 INSTRUCTION SET LIST

b_{14} to b_{11} \ b_{15}		0		1	
BIN	HEX				
0 0 0 0	0	ADD	r, m	ADD	m, #i
0 0 0 1	1	SUB	r, m	SUB	m, #i
0 0 1 0	2	ADDC	r, m	ADDC	m, #i
0 0 1 1	3	SUBC	r, m	SUBC	m, #i
0 1 0 0	4	AND	r, m	AND	m, #i
0 1 0 1	5	XOR	r, m	XOR	m, #i
0 1 1 0	6	OR	r, m	OR	m, #i
0 1 1 1	7	RET RETSK RORC STOP HALT NOP	 r s h 		
1 0 0 0	8	LD	r, m	ST	m, r
1 0 0 1	9	SKE	m, #i	SKGE	m, #i
1 0 1 0	A				
1 0 1 1	B	SKNE	m, #i	SKLT	m, #i
1 1 0 0	C	BR	addr	CALL	addr
1 1 0 1	D			MOV	m, #i
1 1 1 0	E			SKT	m, #n
1 1 1 1	F			SKF	m, #n

12.2 INSTRUCTIONS

Legend:

M	: One of data memory	n	: Bit position : 4 bits
m	: Data memory address specified by [m_H, m_L] of each bank	addr	: One of program memory address : 11 bits
m_H	: Data memory address high (row address) : 3 bits	a_H	: Program memory address high : 3 bits
m_L	: Data memory address low (column address) : 4 bits	a_M	: Program memory address middle : 4 bits
R	: One of general register specified by [(RP), r]	a_L	: Program memory address low : 4 bits
r	: General register address low (column address) : 4 bits	CY	: Carry flag
RP	: General register pointer	CMP	: Compare flag
PC	: Program counter	s	: Stop release condition
SP	: Stack pointer	h	: Halt release condition
STACK	: Stack specified by (SP)	[ ]	: Address of M,R
i	: Immediate data : 4 bits	( )	: Contents of M,R

Type	Mnemonic	Operand	Function	Operation	Machine code			
					Op code	3 bits	4 bits	4 bits
Add	ADD	r,m	Add memory to register	R← (R) + (M)	00000	m_H	m_L	r
		m, #i	Add immediate data to memory	M← (M) + i	10000	m_H	m_L	i
	ADDC	r,m	Add memory to register with carry	R← (R) + (M) + (CY)	00010	m_H	m_L	r
		m, #i	Add immediate data to memory with carry	R← (M) + i+ (CY)	10010	m_H	m_L	i
Subtract	SUB	r,m	Subtract memory from register	R← (R) − (M)	00001	m_H	m_L	r
		m, #i	Subtract immediate data from memory	M← (M) − i	10001	m_H	m_L	i
	SUBC	r,m	Subtract memory from register with borrow	R← (R) − (M) − (CY)	00011	m_H	m_L	r
		m, #i	Subtract immediate data from memory with borrow	M← (M) − i − (CY)	10011	m_H	m_L	i
Compare	SKE	m, #i	Skip if memory equal to immediate data	M−i, skip if zero	01001	m_H	m_L	i
	SKGE	m, #i	Skip if memory greater than or equal to immediate data	M−i, skip if not borrow	11001	m_H	m_L	i
	SKLT	m, #i	Skip if memory less than immediate data	M−i, skip if borrow	11011	m_H	m_L	i
	SKNE	m, #i	Skip if memory not equal to immediate data	M−i, skip if not zero	01011	m_H	m_L	i
Logical operation	AND	m, #i	Logical AND of memory and immediate data	M← (M) AND i	10100	m_H	m_L	i
		r,m	Logical AND of register and memory	R← (R) AND (M)	00100	m_H	m_L	r
	OR	m, #i	Logical OR of memory and immediate data	M← (M) OR i	10110	m_H	m_L	i
		r,m	Logical OR of register and memory	R← (R) OR (M)	00110	m_H	m_L	r
	XOR	m, #i	Logical XOR of memory and immediate data	M← (M) XOR i	10101	m_H	m_L	i
		r,m	Logical XOR of register and memory	R← (R) XOR (M)	00101	m_H	m_L	r
Transfer	LD	r,m	Load memory of register	R← (M)	01000	m_H	m_L	r
	ST	m,r	Store register to memory	(M)←R	11000	m_H	m_L	r
	MOV	m, #i	Move immediate data to memory	M←i	11101	m_H	m_L	i
Test	SKT	m, #n	Test memory bits, then skip if all bits specified are true	CMP ← 0 skip if M_n = all "1"	11110	m_H	m_L	n
	SKF	m, #n	Test memory bits, then skip if all bits specified are false	CMP ← 0 skip if M_n = all "0"	11111	m_H	m_L	n

Type	Mnemonic	Operand	Function	Operation	Machine code			
					Op code	3 bits	4 bits	4 bits
Branch	BR	addr	Jump to the address	PC←ADDR	01100	a_H	a_M	a_L
Shift	RORC	r	Rotate register right with carry	(CY)→(R)→CY	00111	000	0111	r
Subroutine	CALL	addr	Call subroutine	SP←(SP) − 1 STACK←((PC) + 1), PC←ADDR	11100	a_H	a_M	a_L
	RET		Return to main routine from subroutine	PC←(STACK), SP←(SP) + 1	00111	000	1110	0000
	RETSK		Return to main routine from subroutine, then skip unconditionary	PC←(STACK), SP←(SP) + 1 and skip	00111	001	1110	0000
Miscellaneous	STOP	s	Stop clock	STOP	00111	010	1111	s
	HALT	h	Halt the CPU, restart by condition h	HALT	00111	011	1111	h
	NOP		No operation	No Operation	00111	100	1111	0000

13. ELECTRICAL CHARACTERISTICS (PRELIMINARY)

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voitage	V_{DD}			−0.3 to +7.0	V
Supply Voltage	V_{PP}			−0.3 to +13.5	V
Input Voltage	V_I	P0A, P0C, P0D		−0.3 to V_{DD} +0.3	V
		P0B		−0.3 to +11	V
Output Voltage	V_O	P0A, P0C, P0D		−0.3 to V_{DD} +0.3	V
		P0B		−0.3 to +11	V
High-Level Output Current	I_{OH}	Each of P0A, P0B, P0C, P0D		−5	mA
		Total of all pins		−15	mA
Low-Level Output Current	I_{OL}	Each of P0A, P0B, P0C, P0D		30	mA
		Total of all pins		100	mA
Operating Temperature	T_{opt}			−40 to +85	°C
Storage Temperature	T_{stg}			−65 to +150	°C
Power Consumption	P_d	T_a = 85 °C	22-pin shrink DIP	400	mW
			24-pin SOP	250	

CAPACITANCE (T_a = 25 °C, V_{DD} = 0 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Input Capacitance	C_{IN}			15	pF	f = 1 MHz 0 V for pins other than pins to be measured
I/O(*) Capacitance	C_{IO}			15	pF	

* Input/output

DC CHARACTERISTICS (T_a = −40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS	
High-Level Input Voltage	V_{IH1}	0.7 V_{DD}		V_{DD}	V	Other than the following pins and port	
	V_{IH2}	0.8 V_{DD}		V_{DD}	V	P0B and $\overline{RESET}$	
	V_{IH3}	0.8 V_{DD}		9	V	P0B	(*)
	V_{IH4}	V_{DD}-0.5		V_{DD}	V	X_{IN}	
Low-Level Input Voltage	V_{IL1}	0		0.3 V_{DD}	V	Other than the following pins and port	
	V_{IL2}	0		0.2 V_{DD}	V	P0B and $\overline{RESET}$	
	V_{IL3}	0		0.5	V	X_{IN}	
High-Level Output Voltage on P0A, P0C, and P0D	V_{OH}	V_{DD}-2.0			V	V_{DD} = 4.5 to 6.0 V, I_{OH} = −2 mA	
		V_{DD}-1.0			V	I_{OH} = −200 μA	
Low-Level Output Voltage on P0A, P0B, P0C, and P0D	V_{OL}			2.0	V	V_{DD} = 4.5 to 6.0 V, I_{OL} = 15 mA	
				0.5	V	I_{OL} = 600 μA	
High-Level Input Leakage Current on P0A to P0D	I_{LIH1}			5	μA	V_{IN} = V_{DD}	
	I_{LIH2}			10	μA	V_{IN} = 9 V	(*)
Low-Level Input Leakage Current on P0A to P0D	I_{LIL}			−5	μA	V_{IN} = 0 V	
High-Level Output Leakage Current on P0A to P0D	I_{LOH1}			5	μA	V_{OUT} = V_{DD}	
	I_{LOH2}			10	μA	V_{OUT} = 9 V	(*)
Low-Level Output Leakage Current on P0A to P0D	I_{LOL}			−5	μA	V_{OUT} = 0 V	
Power Supply Current	I_{DD1}		1.5	4.5	mA	Operation mode	V_{DD} = 5 V ±10 %, f_{CC} = 8.0 MHz
			250	750	μA		V_{DD} = 3 V ±10 %, f_{CC} = 2.0 MHz
	I_{DD2}		1.0	3.0	mA	HALT mode	V_{DD} = 5 V ±10 %, f_{CC} = 8.0 MHz
			200	600	μA		V_{DD} = 3 V ±10 %, f_{CC} = 2.0 MHz
	I_{DD3}		0.1	10	μA	STOP mode	V_{DD} = 5 V ±10 %
			0.1	5	μA		V_{DD} = 3 V ±10 %

* When N-ch open-drain input/output is selected

CHARACTERISTICS OF DATA MEMORY FOR HOLDING DATA ON LOW SUPPLY VOLTAGE IN THE STOP MODE (T_a = −40 to +85 °C)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Data Hold Supply Voltage	V_{DDDR}	2.0		6.0	V	
Data Hold Supply Current	I_{DDDR}		0.1	5.0	μA	V_{DDDR} = 2.0 V
Release Signal Set Time	t_{SREL}	0			μs	

AC CHARACTERISTICS (T_a = −40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Internal Clock Cycle Time	T_{CY}	1.9		33	μs	V_{DD} = 4.5 to 6.0 V
		7.6		33	μs	
High/Low Level Width on $P0B_0$ and $P0B_1$	T_{PBH} T_{PBL}	10			μs	
High/Low Level Width on $\overline{RESET}$	T_{RSH} T_{RSL}	10			μs	

DC PROGRAMING CHARACTERISTICS (T_a = 25 °C, V_{DD} = 6.0 ± 0.25 V, V_{PP} = 12.5 ± 0.5 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Input Voltage High	V_{IH1}	0.7 V_{DD}		V_{DD}	V	Except X_{IN}
	V_{IH2}	V_{DD}-0.5		V_{DD}	V	X_{IN}
Input Voltage Low	V_{IL1}	0		0.3 V_{DD}	V	Except X_{IN}
	V_{IL2}	0		0.4	V	X_{IN}
Input Leakage Current	I_{LI}			10	μA	V_{IN} = V_{IL} or V_{IH}
Output Voltage High	V_{OH}	V_{DD}-1.0			V	I_{OH} = −1 mA
Output Voltage Low	V_{OL}			0.4	V	I_{OL} = 1.6 mA
V_{DD} Power Supply Current	I_{DD}			30	mA	
V_{PP} Power Supply Current	I_{PP}			30	mA	MD0 = V_{IL}, MD1 = V_{IH}

Notes 1. V_{PP} must be under +13.5 V including overshoot.

2. V_{DD} must be applied before V_{PP} on and must be off after V_{PP} off.

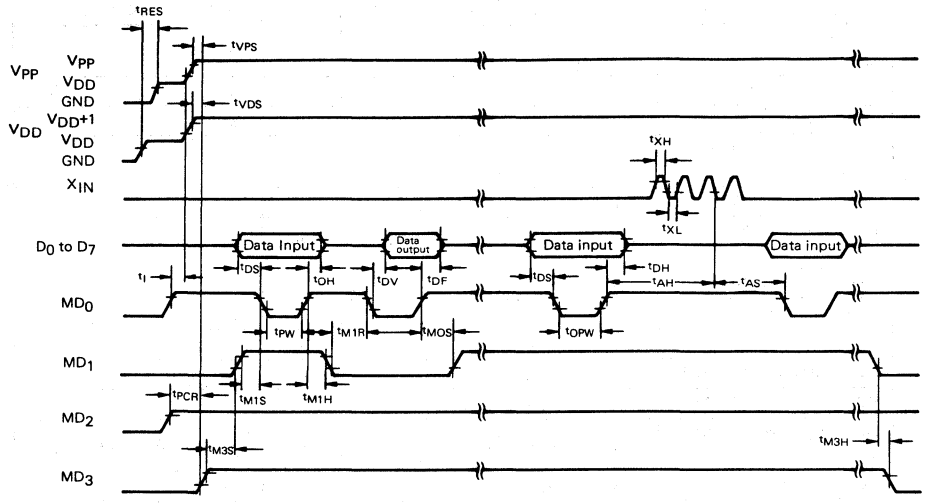
AC CHARACTERISTICS (T_a = 25 °C, V_{DD} = 6.0 ± 0.25 V, V_{PP} = 12.5 ± 0.5 V)

CHARACTERISTICS	SYMBOL	(*1)	MIN.	TYP.	MAX.	UNIT	CONDITION
Address Set Up Time(*2) to MD0↓	t_{AS}	t_{AS}	2			μs	
MD1 Setup Time to MD0↓	t_{M1S}	t_{OES}	2			μs	
Data Setup Time to MD0↓	t_{DS}	t_{DS}	2			μs	
Address Hold Time(*2) to MD0↑	t_{AH}	t_{AH}	2			μs	
Data Hold Time to MD0↑	t_{DH}	t_{DH}	2			μs	
Data Output Float Delay Time from MD0↑→	t_{DF}	t_{DF}	0		130	ns	
V_{PP} Setup Time to MD3↑	t_{VPS}	t_{VPS}	2			μs	
V_{DD} Setup Time to MD3↑	t_{VDS}	t_{VCS}	2			μs	
Initial Program Pulse Width	t_{PW}	t_{PW}	0.95	1.0	1.05	ms	
Additional Program Pulse Width	t_{OPW}	t_{OPW}	0.95		21.0	ms	
MD0 Setup Time to MD1↑	t_{MOS}	t_{CES}	2			μs	
Data Output Delay Time from MD0↓→	t_{DV}	t_{DV}			1	μs	MD0 = MD1 = V_{IL}
MD1 Hold Time to MD0↑	t_{M1H}	t_{OEH}	2			μs	$t_{M1H} + t_{M1R} \geq 50$ μs
MD1 Recovery Time to MD0↓	t_{M1R}	t_{OR}	2			μs	
Program Counter Reset Time	t_{PCR}	–	10			μs	
X_{IN} Input High, Low Level Range	t_{XH}, t_{XL}	–	0.063			μs	
X_{IN} Input Frequency	f_X	–			8	MHz	
Initial Mode Set Time	t_I	–	2			μs	
MD3 Setup Time to MD1↑	t_{M3S}	–	2			μs	
MD3 Hold Time to MD1↓	t_{M3H}	–	2			μs	
MD3 Setup Time to MD0↓	t_{M3SR}	–	2			μs	Read program memory
Data Output Delay Time from Address(*2)	t_{DAD}	t_{ACC}	2			μs	Read program memory
Data Output Hold Time from Address(*2)	t_{HAD}	t_{OH}	0		130	ns	Read program memory
MD3 Hold Time to MD0↑	t_{M3HR}	–	2			μs	Read program memory
Data Output Float Delay Time from MD3↓→	t_{DFR}	–	2			μs	Read program memory
Reset Setup Time	t_{RES}		10			μs	

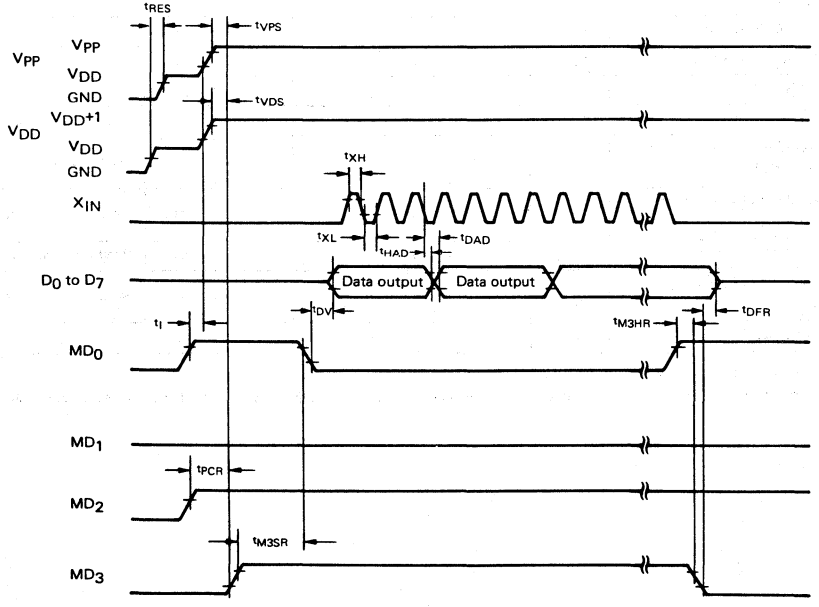
*1 Symbols for corresponding μPD27C256.

*2 Internal address signal is incremented by one at the falling edge of the third X_{IN} input, and it is not connected to the pin.

WRITE PROGRAM MEMORY TIMING



READ PROGRAM MEMORY TIMING



4-BIT SINGLE-CHIP MICROCONTROLLER

The μPD17107 is a tiny microcontroller consisting of a 1K-byte ROM, 16-word RAM, and 11 input/output ports.

The 17K architecture of the CPU uses general registers so that data memory can be manipulated directly for effective programming. Every instruction is 1 word long, consisting of 16 bits.

FEATURES

- Program memory (ROM): 1K bytes (512 words x 16 bits)
- Data memory (RAM): 16 words x 4 bits
- Input/output ports: 11 ports (including three N-ch open-drain outputs)
- Instruction execution time: 128 μs (for 62.5 kHz) to 8 μs (for 1 MHz)
- Number of instructions: 24 (Each instruction is 1 word long.)
- Stack level: 1
- A standby function is supported (with the STOP and HALT instructions).
- Data memory can retain data on low voltage (2.0 V at minimum).
- An oscillator is included for the system clock (only resistor for external circuit).
- Operating supply voltage: 2.5 to 6.0 V (at 250 kHz)
  4.5 to 6.0 V (at 1 MHz)

APPLICATIONS

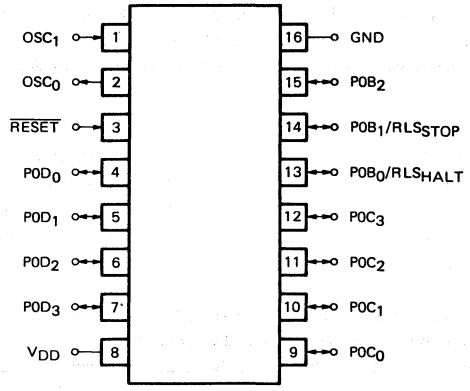
- Controlling electric appliances or toys

ORDERING INFORMATION

Ordering Code	Package
μPD17107CX-xxx	16-pin plastic DIP (300 mil)
μPD17107GS-xxx	16-pin plastic SOP (300 mil)

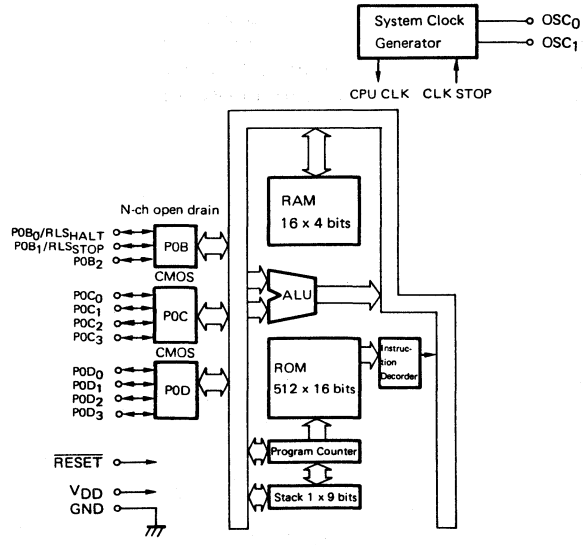
PIN CONFIGURATIONS (Top View)

μPD17107CX / μPD17107GS



16-pin plastic DIP
16-pin plastic SOP

BLOCK DIAGRAM



PIN FUNCTIONS

- Port pins

Pin name	I/O	Function	Reset
$P0B_0$/RLS_{HALT}	I/O	For releasing the HALT mode	• Open-drain: High impedance (input mode) • With pull-up resistor provided: High level (input mode)
$P0B_1$/RLS_{STOP}		For releasing the STOP mode	
$P0B_2$		• N-ch open-drain 4-bit I/O port (port 0B) • A pull-up resistor can be provided bit by bit (mask-selected). • 9 V in open-drain mode	
$P0B_3$			
$P0C_0$ to $P0C_3$	I/O	CMOS (push-pull) 4-bit I/O port (port 0C)	High impedance (input mode)
$P0D_0$ to $P0D_3$	I/O	CMOS (push-pull) 4-bit I/O (port 0D)	High impedance (input mode)

- Non-port pins

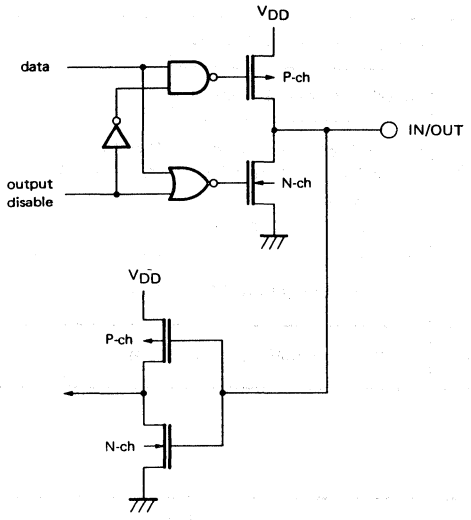
Pin name	I/O	Function	Reset
$\overline{RESET}$	Input	• System reset input pin • A built-in pull-up resistor can be provided bit by bit (mask-selected).	
V_{DD}		• Positive power supply pin	
GND		• GND pin	
OSC_0, OSC_1		• Pins to be connected to the system clock resonator	

I/O: Input/output

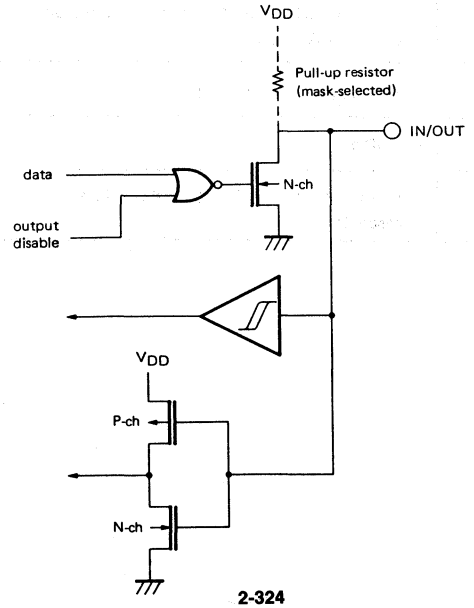
PIN INPUT/OUTPUT CIRCUITS

Following are schematics of the input/output circuits of the pins of the μPD17107.

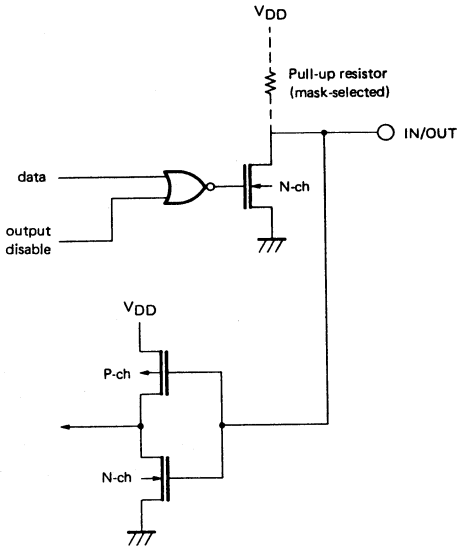
(1) P0C, and P0D



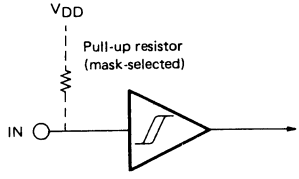
(2) $P0B_0$ and $P0B_1$



(3) $P0B_2$



(4) $\overline{\text{RESET}}$

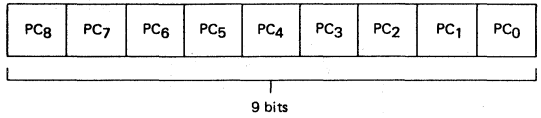


1. PROGRAM COUNTER (PC)

1.1 FORMAT OF THE PROGRAM COUNTER (PC)

The program counter is a 9-bit binary counter formatted as shown in Fig. 1-1.

Fig. 1-1 Format of the Program Counter



1.2 FUNCTIONS OF THE PROGRAM COUNTER (PC)

The program counter specifies the address of a program memory (ROM) or a program.

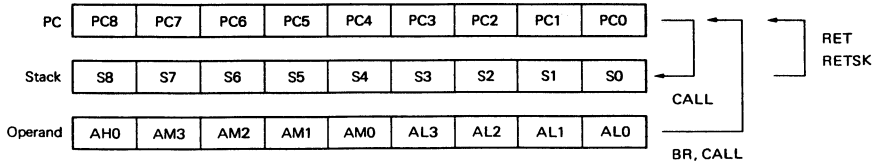
Usually, every time an instruction is executed, the program counter is incremented by one. When a branch instruction (BR), a subroutine call instruction (CALL), or a return instruction (RET) is executed, the address specified in the operand is loaded in the PC. Then the instruction in the address is executed. When a skip instruction is executed, the address of the instruction next to the skip instruction is specified irrespective of the contents of the skip instruction. If the skip conditions are satisfied, the instruction next to the skip instruction is regarded as a No Operation (NOP) instruction. So, the NOP instruction is executed and the address of the next instruction is specified.

2. STACK

Stack of the μPD17107 is a register in which the return address of a program is saved when a subroutine call instruction is executed. One level of address stack is provided.

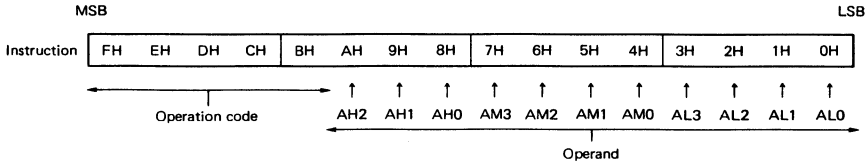
Fig. 2-1 shows the relationship between PC, stack, and instructions.

Fig. 2-1 Relationship between PC, Stack, and Instructions



In Fig. 2-1, AHn, AMn, and ALn (n = 0 to 3) indicate bit positions in a 16-bit instruction as follows:

Fig. 2-2 Format of a 16-Bit Instruction



When the assembler (AS17K) is not used and a BR or CALL instruction is used, AH2 and AH1 must be set to 0.

Sn (n = 0 to 8) denotes a stack.

$\overline{\text{RESET}}$ signal input clears all bits of the program counter to 0.

3. PROGRAM MEMORY (ROM)

Fig. 3-1 shows the configuration of program memory (ROM).

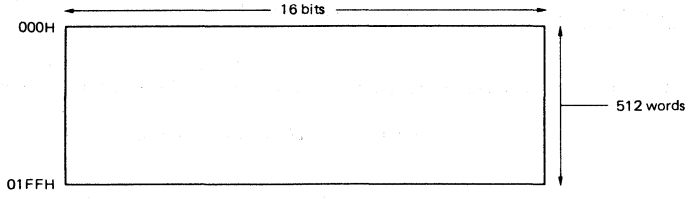
The program memory consists of 512 words by 16 bits.

The program memory is addressed in units of 16 bits and it ranges from addresses 000H to 01FFH. Each address is specified by the program counter (PC).

Since an instruction consists of 16 bits (one word), the instruction is stored at one address of the program memory.

Address 000H is assigned to a reset start address.

Fig. 3-1 Program Memory Map



4. DATA MEMORY (RAM)

The data memory stores data of arithmetic/logic and control operations. Data can be always written to or read from it by means of instructions.

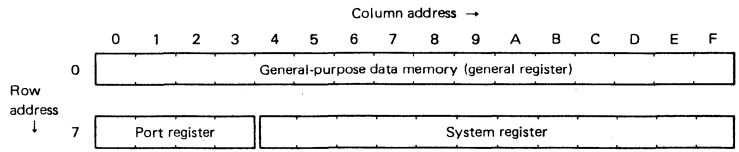
4.1 FORMAT OF THE DATA MEMORY (RAM)

Fig. 4-1 shows the format of the data memory (RAM).

The data memory is configured in units of four bits, or "one nibble," and an address is assigned to each four bits of data. The three high-order bits are called the "row address," and the four low-order bits are called the "column address."

According to its functions, the data memory is divided into three blocks as shown below: general-purpose data memory, port register, and system register.

Fig. 4-1 Data Memory Map



4.1.1 Functions of the general-purpose data memory

The general-purpose data memory is a part of the data memory from which the system register (SYSREG) and port register are excluded. By executing a data memory manipulation instruction, a four-bit arithmetic operation and comparison, evaluation, and transfer between data on data memory and any immediate data can be executed with a single operation.

4.1.2 Functions of the general register

The general register indicates any identical row address (16 nibbles) in the data memory specified in the register pointer (RP) in the system register. Since the μPD17107 register pointer is always set to 0, the general-purpose data memory is also used as a general register. The general register can operate or transfer data to and from the data memory.

4.1.3 Functions of the port register

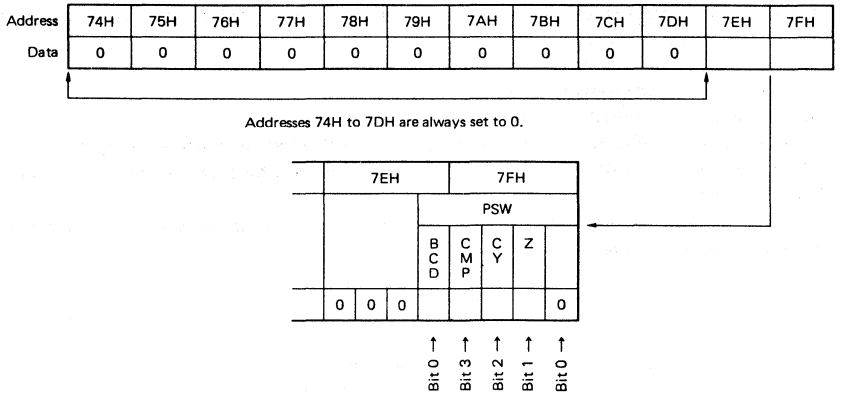
The port register is used to set output data or to read the input data of input/output ports.

Once data are written to the port register corresponding to a port, the port is set as an output port and continues to output the value unless the value is rewritten. Whenever a read instruction is executed for a port register, the read data indicate the states of the pins, not the value of the port register, regardless of whether the pins are in the input or output mode.

4.1.4 Functions of the system register

The system register controls the CPU. The program status word (PSW) is the only system register existing in the μPD17107.

Fig. 4-2 System Register Map

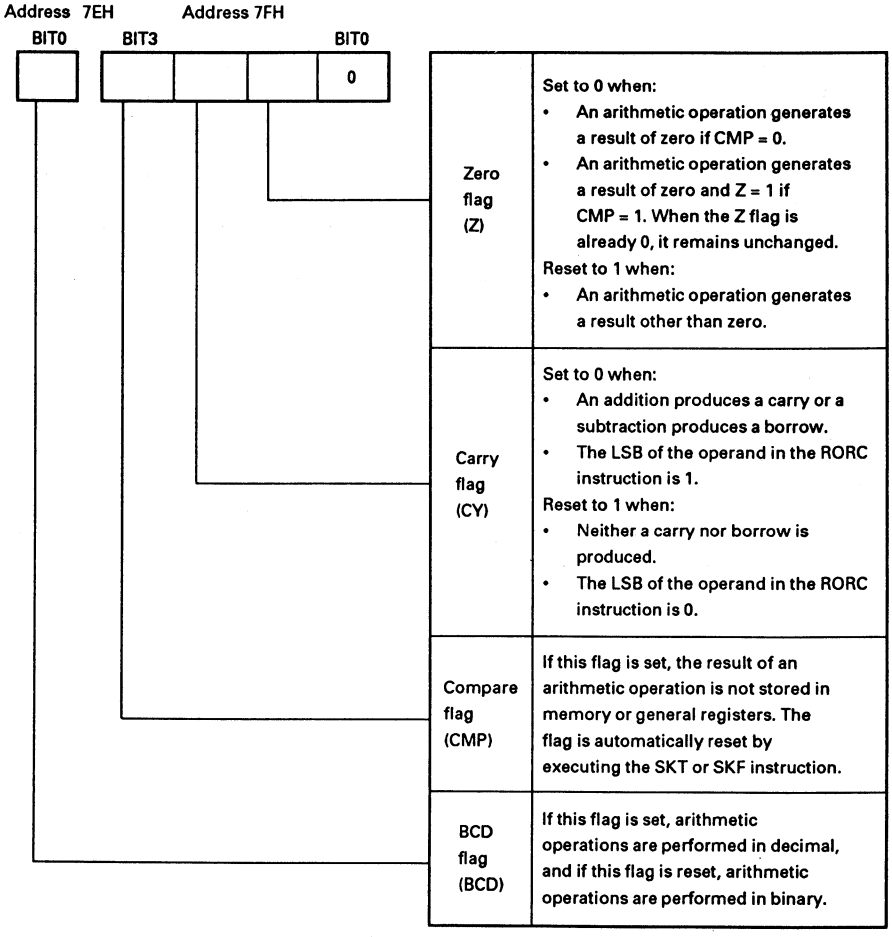


Bit 0 at address 7EH and the high-order three bits at address 7FH are assigned to the program status word.

The BCD flag is mapped in bit 0 at address 7EH, the CMP flag is mapped in bit 3 at address 7FH, the carry (CY) flag is mapped in bit 2 at address 7FH, and the zero (Z) flag is mapped in bit 1 at address 7FH.

The high-order three bits at address 7EH and bit 0 at address 7FH are always set to 0.

Fig. 4-3 Format of the Program Status Word



Comparison instructions (SKE, SKNE, SKGE, or SKLT) do not change the state of the CY flag, but an arithmetic operation may affect the CY flag according to the result even if the CMP flag is set.

Each bit of the program status word is initialized to 0 when a reset signal is applied.

The Z flag in the program status word changes according to the set value of the CMP flag as listed in Table 4-1.

Table 4-1 Change in Z Flag

Condition	Z flag value	
	CMP = 0	CMP = 1
Reset	0	–
Memory manipulation sets the Z flag to 0.	0	0
Memory manipulation sets the Z flag to 1.	1	1
Arithmetic operation results in a non-zero value.	0	0
Arithmetic operation results in 0.	1	Z_{n-1}

Zn-1: The Z flag value present immediately before arithmetic operation

While CMP is 1, if an arithmetic operation results in 0H when the value of the Z flag is 1, the Z flag does not change. If an arithmetic operation results in other than 0H, the Z flag is reset to 0 and remains intact even when a second arithmetic operation results in 0H.

After the CMP and Z flags are set to 1, subtraction and comparison are performed several times. Then, if the Z flag still indicates 1, all of the comparison operations showed a match, resulting in 0. If the Z flag is 0 after the comparison operations, a mismatch occurred in at least one comparison operation.

5. ARITHMETIC AND LOGIC UNIT (ALU)

The arithmetic and logic unit (ALU) performs arithmetic operations, logical operations, bit tests, comparisons, and rotations on 4-bit data.

5.1 ARITHMETIC OPERATIONS

Arithmetic operations are performed on binary or decimal data. If the BCD flag in the program status word is 1, the ALU operates on decimal data, and if the flag is 0, it operates on binary data.

If an addition produces a carry or if a subtraction produces a borrow, the carry (CY) flag is set to 1. If neither a carry nor borrow is produced, the flag is reset to 0.

If an arithmetic operation results in zero, the zero (Z) flag is set to 1. Otherwise, the flag is reset to 0.

(1) Binary operation

If the result of a binary arithmetic operation is greater than 15 (1111B), a carry is made. If it is less than zero, a borrow is made. In either case, the CY flag is set to 1.

(2) Decimal operation

If the result of a decimal arithmetic operation is greater than 9 (1001B), a carry is made. If it is less than 0, a borrow is made. In either case, the CY flag is set to 1.

Decimal operations are allowed if one of the following results is generated. If the result of a decimal operation does not fall into these ranges, the CY flag is set to 1, and a result greater than or equal to 10 (1010B) is produced.

1. Addition must generate a result from 0 to 19.
2. Subtraction must generate a result from 0 to 9 or −10 to −1.

5.2 LOGICAL OPERATIONS

Logical operations include ANDing, ORing, and XORing.

5.3 OTHER OPERATIONS

The ALU enables bit testing, comparison, and data rotation.

6. PORTS

6.1 PORT 0B ($P0B_0$/RLS_{HALT}, $P0B_1$/RLS_{STOP}, $P0B_2$)

Port 0B is a three-bit input/output port. Only N-ch open-drain outputs appear on the pins of port 0B. The N-ch open-drain output mode allows application of 9 V, so it can be used for interfacing with a circuit operating on a different power supply voltage.

Input and output are set in units of nibbles. The input mode is set at reset, and the output mode is set by writing data to the port register in address 71H of the data memory. The output mode is maintained until the system is reset.

Output to the port is executed via the port register. Once data are written to the port register, all pins of port P0B are placed in the output mode to continue to output written data. The data are retained unless new data are written to the register.

Whenever the port register is read, the read data indicate the states of the pins, not the contents of the port register, regardless of whether the pins are in the input or output mode. In this case, the contents of the port register remain unchanged.

The port register for port B consists of four bits but its highest bit is always set to 0. This means that if an attempt is made to write data to the highest bit of 71H, the data is invalidated and if an attempt is made to read it, 0 is always returned.

When the μPD17107 is in the HALT or STOP mode, $P0B_0$ and $P0B_1$ function as pseudo interrupt pins to release the HALT and STOP modes. (Refer to Section 8).

6.2 PORT 0C ($P0B_0$ to $P0C_3$)

Port 0C is a four-bit input/output port. CMOS (push-pull) outputs appear on those pins.

Input and output are set in units of nibbles. The input mode is set at reset, and the output mode is set by writing data to the port register in address 72H of the data memory. The output mode is maintained until the system is reset.

Output to the port is executed via the port register. Once data are written to the port register, all pins of the port P0C are placed in the output mode to continue to output written data. The data are retained unless new data are written to the register.

Whenever the port register is read, the read data indicate the states of the pins, not the contents of the port register, regardless of whether the pins are in the input or output mode. In this case, the contents of the port register remain unchanged.

6.3 PORT 0D ($P0D_0$ to $P0D_3$)

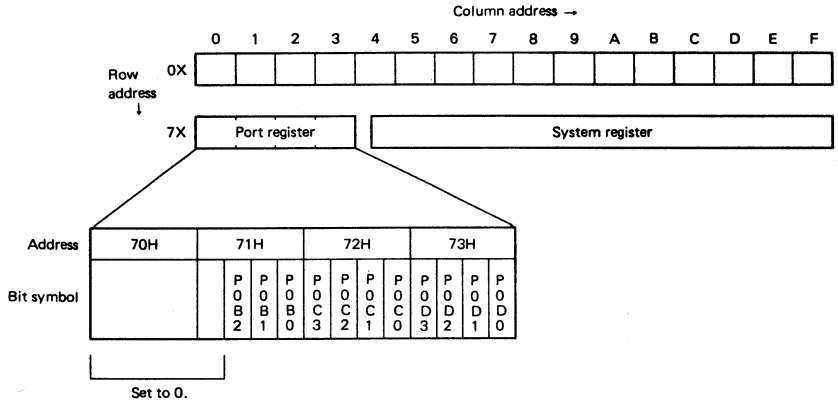
Port 0D is a four-bit input/output port. CMOS (push-pull) outputs appear on these pins.

Input and output are set in units of nibbles. The input mode is set at reset, and the output mode is set by writing data to the port register in address 73H of the data memory. The output mode is maintained until the system is reset.

Output to the port is executed via the port register. Once data are written to the port register, all pins of the port P0D are placed in the output mode to continue to output written data. The data are retained until new data are written to the register.

Whenever the port register is read, the read data indicate the states of the pins, not the contents of the port register, regardless of whether the pins are in the input or output mode. In this case, the contents of the port register remain unchanged.

Fig. 6-1 Port Register Map



6.4 RECOMMENDED CONDITIONS FOR UNUSED μPD17107 PINS

To prevent malfunction, process unused input/output pins as shown below.

Table 6-1 Recommended Conditions for Unused Pins

Input/ output mode	Port	Recommended connection
Input mode	Ports B, C, and D	Connect to V_{DD} or GND.
Output mode	CMOS ports (ports C and D)	Open
	N-ch open-drain port (port B)	

7. STANDBY FUNCTIONS

The μPD17107 provides two standby modes, the HALT mode and the STOP mode.

7.1 HALT MODE

The HALT mode stops the program counter (PC) while allowing the system clock to continue operating. The HALT mode can be entered with the HALT instruction, and can be released by a reset signal ($\overline{\text{RESET}}$) or input to the $P0B_0$ pin. When the HALT mode is released by input to the $P0B_0$ pin, the next instruction after the HALT instruction is executed without waiting for stable oscillation of the system clock.

When the HALT mode is released forcibly by the reset signal ($\overline{\text{RESET}}$), normal system reset occurs, and execution starts at address 0H.

7.2 STOP MODE

The STOP mode stops oscillation of the system clock so that data can be retained at low voltage. The STOP mode can be entered with the STOP instruction, and can be released by a reset signal ($\overline{\text{RESET}}$) or input to the $P0B_1$ pin. When the mode is released by input to the $P0B_1$ pin, execution starts with the next instruction after the STOP instruction.

When the STOP mode is released forcibly by the reset signal ($\overline{\text{RESET}}$), normal system reset occurs, and execution starts at address 0H.

7.3 SETTING AND RELEASING THE STANDBY MODES

(1) Setting and releasing the HALT mode

The conditions for releasing the HALT mode can be selected with the least significant bit of the operand in the HALT instruction. The high-order three bits of the operand must be set to 0.

Table 7-1 Setting and Releasing Conditions Specified in the HALT Instruction

HALT 000X̲B ← 4-bit data in the operand

X	Conditions for setting/releasing the HALT mode
0	Executing the HALT instruction enters the HALT mode unconditionally. The mode can be released only by the reset signal ($\overline{\text{RESET}}$). After the mode is released, instructions are executed starting at address 0H.
1	If P0B0 is 0, executing the HALT instruction enters the HALT mode. If P0B0 is 1, executing the HALT instruction does not enter the HALT mode. Application of the reset signal ($\overline{\text{RESET}}$) releases the HALT mode. After the mode is released, instructions are executed starting at address 0H. The rising edge of an input signal on the $P0B_0$ pin also releases the HALT mode. In this case, execution starts with the next instruction after the HALT instruction.

(2) Setting and releasing the STOP mode

Conditions to release the STOP mode can be selected with the least significant bit of the operand in the STOP instruction. The high-order three bits of the operand must be set to 0.

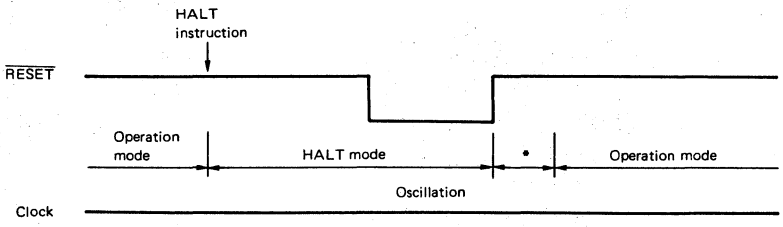
Table 7-2 Setting/Releasing Conditions Specified in the STOP Instruction

STOP 000X8 ← 4-bit data in the operand

X	Conditions for setting/releasing the STOP mode
0	Executing the STOP instruction enters the STOP mode unconditionally. All peripheral circuits are placed in the same initial state as when the system is reset, then they stop operating. Only the reset signal ($\overline{RESET}$) can release the STOP mode. After the mode is released, instructions are executed starting at address 0H.
1	If P0B1 is 0, executing the STOP instruction enters the STOP mode. If P0B1 is 1, executing the STOP instruction does not enter the STOP mode. Application of the reset signal ($\overline{RESET}$) can release the STOP mode. After the mode is released, instructions are executed starting at address 0H. The rising edge of the signal applied to the $P0B_1$ pin can also release the mode. In this case, execution starts with the next instruction after the STOP instruction.

7.4 TIMING FOR RELEASING THE STANDBY MODES

Fig. 7-1 Releasing the HALT Mode by $\overline{RESET}$ Input



When the $\overline{RESET}$ signal is applied to release the HALT mode, the $\overline{RESET}$ input makes a transition from low to high, then an operation mode is entered.

* The HALT mode remains effective in this period, waiting for the operation mode.
  At least eight clock pulses on the OSC_1 pin cause operation to start.

Fig. 7-2 Releasing the HALT Mode by Interrupt

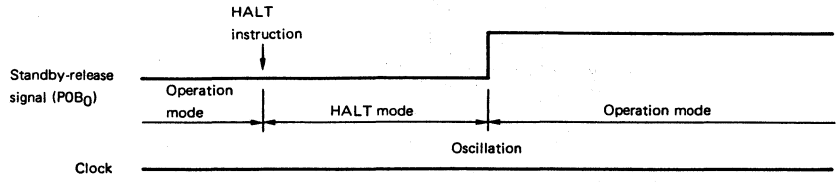
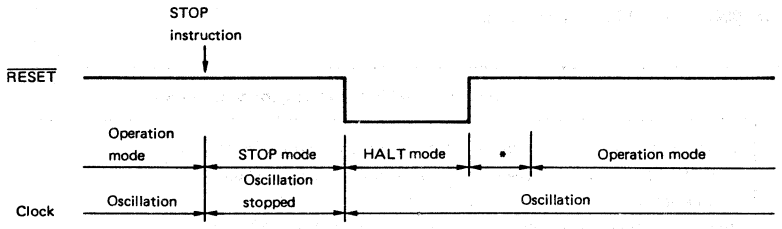


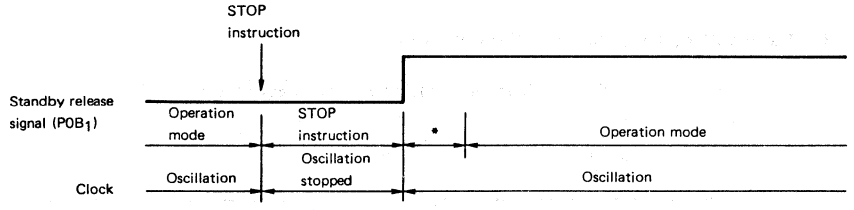
Fig. 7-3 Releasing the STOP Mode by RESET Input



As soon as the $\overline{\text{RESET}}$ input makes a transition from high to low in the STOP mode, the system clock starts generating clock pulses.

* The HALT mode remains effective in this period, waiting for the generation of clock pulses to stabilize. At least eight clock pulses on the OSC_1 pin cause operation to start.

Fig. 7-4 Releasing the STOP Mode by Interrupt



* The HALT mode remains effective in this period, waiting for the generation of clock pulses to stabilize. At least eight clock pulses on the OSC_1 pin cause operation to start.

8. RESET FUNCTION

8.1 HARDWARE STATE AT RESET

A low-active reset signal applied to the $\overline{\text{RESET}}$ pin sets the hardware states as listed below. A transition from low to high on the $\overline{\text{RESET}}$ pin releases the reset state.

Table 8-1 Hardware after Reset

Name	Location in memory space	Set value
Program counter		000H
RAM	0H to 0FH	Data present before reset is retained.
Program status word (PSW)	Bit 0 at 7EH Bits 3 to 1 at 7FH	All 0s
Ports 0B to 0D	71H to 73H	Data present before reset is retained. All pins are placed in the input mode.

9. ASSEMBLER RESERVED WORDS

9.1 MASK OPTION PSEUDO INSTRUCTIONS

Source programs in the assembly language for the μPD17107 must include mask option pseudo instructions to select pin options.

To do this, be sure to catalog the D17107. OPT file in AS17107 (device file for μPD17107) into the current directory beforehand.

Options must be mask-selected for the following pins:

- $P0B_0$
- $P0B_1$
- $P0B_2$
- $\overline{RESET}$

9.1.1 OPTION and ENDOP pseudo instructions

The part starting with the OPTION pseudo instruction and ending with the ENDOP pseudo instruction is referred to as a mask option definition block. The coding format of the mask option definition block is shown on the next page.

Within this block, the mask option definition pseudo instructions listed in Table 9-1 can be coded.

Format Symbol	Mnemonic	Operand	Comment
[label:]	OPTION		[;comment]
	.		
	.		
	.		
	ENDOP		

9.1.2 Mask option definition pseudo instructions

Table 9-1 lists the mask option definition pseudo instructions corresponding to each pin.

Table 9-1 Mask Option Definition Pseudo Instructions

Pin	Mask option pseudo instruction	Number of operands	Operand name
$P0B_2$ to $P0B_0$	OPTP0B	3	P0BPLUP (with pull-up resistor) OPEN (without pull-up resistor)
$\overline{RESET}$	OPTRES	1	RESPLUP (with pull-up resistor) OPEN (without pull-up resistor)

The coding format of OPTP0B is shown below. The operands $P0B_2$, $P0B_1$, and $P0B_0$ are defined in this order.

Format Symbol	Mnemonic	Operand	Comment
[label:]	OPTP0B	($P0B_2$), ($P0B_1$), ($P0B_0$)	[;comment]

The coding format of OPTRES is shown below.

Format Symbol	Mnemonic	Operand	Comment
[label:]	OPTRES	(RESET)	[;comment]

Example:

To set the following mask options in a μPD17107 source file to be assembled:
$P0B_2$: Pull-up $P0B_1$: Open $P0B_0$: Open
$\overline{\text{RESET}}$: Pull-up

```
                    ⋮
; 17107
Setting mask options: OPTION
                      OPTP0B  P0BPLUP, OPEN, OPEN
                      OPTRES  RESPLUP
                      ENDOP
                    ⋮
```

9.2 RESERVED WORDS

Table 9-2 lists the reserved words defined in the μPD17107 device file (AS17107).

Table 9-2 Reserved Words

Name	Attribute	Value	Read/write	Description
P0B0	FLG	0.71H.0	Read/write	Bit 0 of port 0B
P0B1	FLG	0.71H.1	Read/write	Bit 1 of port 0B
P0B2	FLG	0.71H.2	Read/write	Bit 2 of port 0B
*P0B3	FLG	0.71H.3	Read	Set to 0.
P0C0	FLG	0.72H.0	Read/write	Bit 0 of port 0C
P0C1	FLG	0.72H.1	Read/write	Bit 1 of port 0C
P0C2	FLG	0.72H.2	Read/write	Bit 2 of port 0C
P0C3	FLG	0.72H.3	Read/write	Bit 3 of port 0C
P0D0	FLG	0.73H.0	Read/write	Bit 0 of port 0D
P0D1	FLG	0.73H.1	Read/write	Bit 1 of port 0D
P0D2	FLG	0.73H.2	Read/write	Bit 2 of port 0D
P0D3	FLG	0.73H.3	Read/write	Bit 3 of port 0D
BCD	FLG	0.7EH.0	Read/write	BCD arithmetic flag
PSW	MEM	0.7FH	Read/write	Program status word
Z	FLG	0.7FH.1	Read/write	Zero flag
CY	FLG	0.7FH.2	Read/write	Carry flag
CMP	FLG	0.7FH.3	Read/write	Compare flag

- Although P0B3 does not exist in the μPD17107, it is defined as a read-only flag so that it is treated as a dummy bit when a built-in macro is used.

10. INSTRUCTION SET

10.1 INSTRUCTION SET LIST

$b_{14}-b_{11}$ \ b_{15}		0		1	
BIN	HEX				
0 0 0 0	0	ADD	r, m	ADD	m, #i
0 0 0 1	1	SUB	r, m	SUB	m, #i
0 0 1 0	2	ADDC	r, m	ADDC	m, #i
0 0 1 1	3	SUBC	r, m	SUBC	m, #i
0 1 0 0	4	AND	r, m	AND	m, #i
0 1 0 1	5	XOR	r, m	XOR	m, #i
0 1 1 0	6	OR	r, m	OR	m, #i
0 1 1 1	7	RET RETSK RORC STOP HALT NOP	 r s h 		
1 0 0 0	8	LD	r, m	ST	m, r
1 0 0 1	9	SKE	m, #i	SKGE	m, #i
1 0 1 0	A				
1 0 1 1	B	SKNE	m, #i	SKLT	m, #i
1 1 0 0	C	BR	addr	CALL	addr
1 1 0 1	D			MOV	m, #i
1 1 1 0	E			SKT	m, #n
1 1 1 1	F			SKF	m, #n

10.2 INSTRUCTIONS

Legend:

M	: One of data memory	n	: Bit position : 4 bits
m	: Data memory address specified by [m_H, m_L] of each bank	addr	: One of program memory address : 11 bits
m_H	: Data memory address high (row address) : 3 bits	a_H	: Program memory address high : 3 bits
m_L	: Data memory address low (column address) : 4 bits	a_M	: Program memory address middle : 4 bits
R	: One of general register specified by [(RP), r]	a_L	: Program memory address low : 4 bits
r	: General register address low (column address) : 4 bits	CY	: Carry flag
RP	: General register pointer	CMP	: Compare flag
PC	: Program counter	s	: Stop release condition
SP	: Stack pointer	h	: Halt release condition
STACK	: Stack specified by (SP)	[ ]	: Address of M,R
i	: Immediate data : 4 bits	( )	: Contents of M,R

Type	Mnemonic	Operand	Function	Operation	Machine code			
					Op code	3bits	4bits	4bits
Add	ADD	r,m	Add memory to register	R← (R) + (M)	00000	m_H	m_L	r
		m, #i	Add immediate data to memory	M← (M) + i	10000	m_H	m_L	i
	ADDC	r,m	Add memory to register with carry	R← (R) + (M) + (CY)	00010	m_H	m_L	r
		m, #i	Add immediate data to memory with carry	R← (M) + i + (CY)	10010	m_H	m_L	i
Subtract	SUB	r,m	Subtract memory from register	R← (R) − (M)	00001	m_H	m_L	r
		m, #i	Subtract immediate data from memory	M← (M) − i	10001	m_H	m_L	i
	SUBC	r,m	Subtract memory from register with borrow	R← (R) − (M) − (CY)	00011	m_H	m_L	r
		m, #i	Subtract immediate data from memory with borrow	M← (M) − i − (CY)	10011	m_H	m_L	i
Compare	SKE	m, #i	Skip if memory equal to immediate data	M−i, skip if zero	01001	m_H	m_L	i
	SKGE	m, #i	Skip if memory greater than or equal to immediate data	M−i, skip if not borrow	11001	m_H	m_L	i
	SKLT	m, #i	Skip if memory less than immediate data	M−i, skip if borrow	11011	m_H	m_L	i
	SKNE	m, #i	Skip if memory not equal to immediate data	M−i, skip if not zero	01011	m_H	m_L	i
Logical operation	AND	m, #i	Logical AND of memory and immediate data	M← (M) AND i	10100	m_H	m_L	i
		r,m	Logical AND of register and memory	R← (R) AND (M)	00100	m_H	m_L	r
	OR	m, #i	Logical OR of memory and immediate data	M← (M) OR i	10110	m_H	m_L	i
		r,m	Logical OR of register and memory	R← (R) OR (M)	00110	m_H	m_L	r
	XOR	m, #i	Logical XOR of memory and immediate data	M← (M) XOR i	10101	m_H	m_L	i
		r,m	Logical XOR of register and memory	R← (R) XOR (M)	00101	m_H	m_L	r
Transfer	LD	r,m	Load memory of register	R← (M)	01000	m_H	m_L	r
	ST	m,r	Store register to memory	(M)←R	11000	m_H	m_L	r
	MOV	m, #i	Move immediate data to memory	M← i	11101	m_H	m_L	i
Test	SKT	m, #n	Test memory bits, then skip if all bits specified are true	CMP ← 0 skip if M_n = all "1"	11110	m_H	m_L	n
	SKF	m, #n	Test memory bits, then skip if all bits specified are false	CMP ← 0 skip if M_n = all "0"	11111	m_H	m_L	n

Type	Mnemonic	Operand	Function	Operation	Machine code			
					Op code	3bits	4bits	4bits
Branch	BR	addr	Jump to the address	PC←ADDR	01100	a_H	a_M	a_L
Shift	RORC	r	Rotate register right with carry	(CY)→(R)→CY	00111	000	0111	r
Subroutine	CALL	addr	Call subroutine	SP←(SP)−1 STACK←((PC)+1), PC←ADDR	11100	a_H	a_M	a_L
	RET		Return to main routine from subroutine	PC←(STACK), SP←(SP)+1	00111	000	1110	0000
	RETSK		Return to main routine from subroutine, then skip unconditionary	PC←(STACK), SP←(SP)+1 and skip	00111	001	1110	0000
Miscellaneous	STOP	s	Stop clock	STOP	00111	010	1111	s
	HALT	h	Halt the CPU, restart by condition h	HALT	00111	011	1111	h
	NOP		No operation	No Operation	00111	100	1111	0000

11. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage	V_{DD}			-0.3 to +7.0	V
Input Voltage	V_I	P0C, P0D,		-0.3 to V_{DD}+0.3	V
		P0B	(*1)	-0.3 to V_{DD}+0.3	V
			(*2)	-0.3 to +11	V
		P0C, P0D, $\overline{RESET}$		-0.3 to V_{DD}+0.3	V
Output Voltage	V_O	P0B	(*1)	-0.3 to V_{DD}+0.3	V
			(*2)	-0.3 to +11	V
High-Level Output Current	I_{OH}	Each of P0B, P0C, P0D		-5	mA
		Total of all pins		-15	mA
Low-Level Output Current	I_{OL}	Each of P0B, P0C, P0D		30	mA
		Total of all pins		100	mA
Operating Temperature	T_{opt}			-40 to +85	°C
Storage Temperature	T_{stg}			-65 to +150	°C
Power Consumption	P_d	T_a = 85 °C	16-pin DIP	400	mW
			16-pin SOP	250	

* 1 N-ch open-drain input/output and input/output with a pull-up resistor provided

* 2 N-ch open-drain input/output

CAPACITANCE (T_a = 25 °C, V_{DD} = 0V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Input capacitance	C_{IN}			15	pF	f = 1 MHz
Input/output capacitance	C_{IO}			15	pF	0 V for pins other than pins to be measured

DC CHARACTERISTICS (T_a = -40 to +85 °C, V_{DD} = 2.5 to 6.0 V)

CHARACTERISTICS	SYMBOL	MIN.	TYPE	MAX.	UNIT	CONDITION
High-Level Input Voltage	V_{IH1}	0.7 V_{DD}		V_{DD}	V	Other than the following pins and port
	V_{IH2}	0.8 V_{DD}		V_{DD}	V	P0B and $\overline{RESET}$
	V_{IH3}	0.8 V_{DD}		9	V	P0B *3
	V_{IH4}	V_{DD} - 0.5		V_{DD}	V	OSC_1
Low-Level Input Voltage	V_{IL1}	0		0.3 V_{DD}	V	Other than the following pins and port
	V_{IL2}	0		0.2 V_{DD}	V	P0B and $\overline{RESET}$
	V_{IL3}	0		0.5	V	OSC_1
High-Level Output Voltage on P0C and P0D	V_{OH}	V_{DD} - 2.0			V	V_{DD} = 4.5 to 6.0 V, I_{OH} = -2 mA
		V_{DD} - 1.0			V	I_{OH} = -200 μA
Low-Level Output Voltage on P0B, P0C and P0D	V_{OL}			2.0	V	V_{DD} = 4.5 to 6.0 V, I_{OL} = 15 mA
				0.5	V	I_{OL} = 600 μA
High-Level Input Leakage Current on P0B to P0D	I_{LIH1}			5	μA	V_{IN} = V_{DD}
	I_{LIH2}			10	μA	V_{IN} = 9 V *3
Low-Level Input Leakage Current on P0B to P0D	I_{LIL}			-5	μA	V_{IN} = 0 V
High-Level Output Leakage Current on P0B to P0D	I_{LOH1}			5	μA	V_{OUT} = V_{DD}
	I_{LOH2}			10	μA	V_{OUT} = 9 V *3
Low-Level Output Leakage Current on P0B to P0D	I_{LOL}			-5	μA	V_{OUT} = 0 V
Resistor Provided for Input Pin		20	47	95	kΩ	$\overline{RESET}$ (pull-up)
Resistor Provided for Input/Output Pin		5	15	30	kΩ	$P0B_0$, $P0B_1$, and $P0B_2$ (pull-up)

* 3 When N-ch open-drain input/output is selected

CHARACTERISTICS	SYMBOL		MIN.	TYP.	MAX.	UNIT	CONDITION
Power Supply Current (*4)	I_{DD1}	Operation mode		0.4	1.2	mA	V_{DD} = 5 V ± 10 % f_{CC} = 1.0 MHz ± 20 %
				50	150	μA	V_{DD} = 3 V ± 10 %, f_{CC} = 250 KHz ± 20 %
	I_{DD2}	HALT mode		0.3	0.9	mA	V_{DD} = 5 V ± 10 %, f_{CC} = 1.0 MHz ± 20 %
				40	120	μA	V_{DD} = 3 V ± 10 %, f_{CC} = 250 kHz ± 20 %
	I_{DD3}	STOP mode		0.1	10	μA	V_{DD} = 5 V ± 10 %
				0.1	5	μA	V_{DD} = 3 V ± 10 %

*4 This current excludes the current which flows through the built-in pull-up resistors.

CHARACTERISTICS OF DATA MEMORY FOR HOLDING DATA ON LOW SUPPLY VOLTAGE IN THE STOP MODE (T_a = -40 to +85 °C)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Data Hold Supply Voltage	V_{DDDR}	2.0		6.0	V	
Data Hold Supply Current	I_{DDDR}		0.1	5.0	μA	V_{DDDR} = 2.0 V
Release Signal Set Time	t_{SREL}	0			μs	

AC CHARACTERISTICS (T_a = -40 to +85 °C, V_{DD} = 2.5 to 6.0 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Internal Clock Cycle Time	T_{CY}	6.6		160	μs	V_{DD} = 4.5 to 6.0 V
		26.6		160	μs	
High/Low Level Width on $P0B_0$ and $P0B_1$	T_{PBH} T_{PBL}	10			μs	
High/Low Level Width on $\overline{RESET}$	T_{ASH} T_{RSL}	10			μs	

4-BIT SINGLE-CHIP MICROCONTROLLER

The μPD17108 is a tiny microcontroller consisting of a 1K-byte ROM, 16-word RAM, and 16 input/output ports.

The 17K architecture of the CPU uses general registers so that data memory can be manipulated directly for effective programming. Every instruction is 1 word long, consisting of 16 bits.

FEATURES

- Program memory (ROM): 1K bytes (512 words x 16 bits)
- Data memory (RAM): 16 words x 4 bits
- Input/output ports: 16 ports (including four N-ch open-drain outputs)
- Instruction execution time: 128 μs (for 62.5 kHz) to 8 μs (for 1 MHz)
- Number of instructions: 24 (Each instruction is 1 word long.)
- Stack level: 1
- A standby function is supported (with the STOP and HALT instructions).
- Data memory can retain data on low voltage (2.0 V at minimum).
- An oscillator is included for the system clock (only resistor for external circuit).
- Operating supply voltage: 2.5 to 6.0 V (at 250 kHz)
  4.5 to 6.0 V (at 1 MHz)

APPLICATIONS

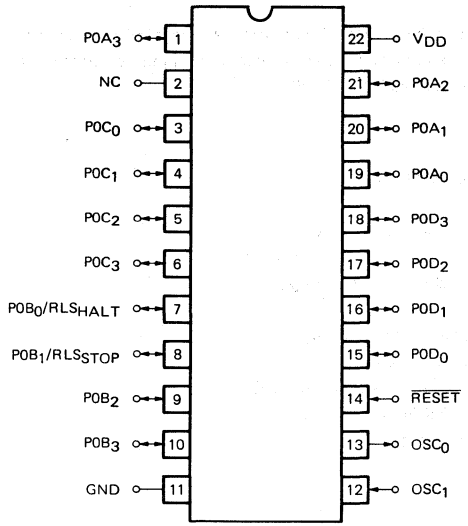
- Controlling electric appliances or toys

ORDERING INFORMATION

Order Code	Package
μPD17108CS-xxx	22-pin plastic shrink DIP (300 mil)
μPD17108GS-xxx	24-pin plastic SOP (300 mil)

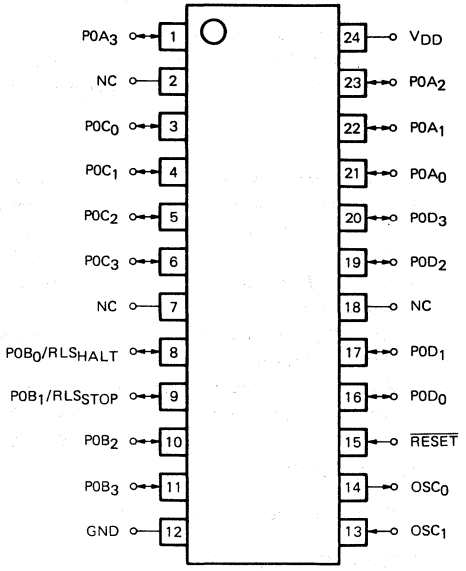
PIN CONFIGURATION (Top View)

μPD17108CS



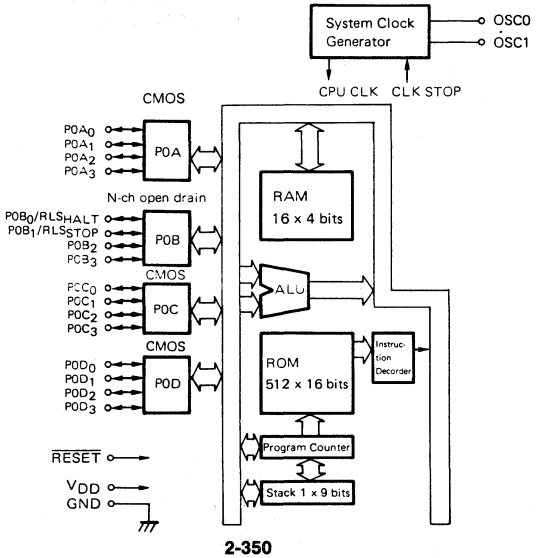
22-pin plastic shrink DIP

μPD17108GS



24-pin plastic SOP

BLOCK DIAGRAM



PIN FUNCTIONS

- Port pins

Pin name	I/O	Function	Reset
$P0A_0$ to $P0A_3$	I/O	• CMOS (push-pull) 4-bit I/O port (port 0A)	High impedance (input mode)
$P0B_0$/RLS_{HALT}	I/O	For releasing the HALT mode	• Open-drain: High impedance (input mode) • With pull-up resistor provided: High level (input mode)
$P0B_1$/RLS_{STOP}		For releasing the STOP mode	
$P0B_2$		• N-ch open-drain 4-bit I/O port (port 0B) • A pull-up resistor can be provided bit by bit (mask-selected). • 9 V in open-drain mode	
$P0B_3$			
$P0C_0$ to $P0C_3$	I/O	CMOS (push-pull) 4-bit I/O port (port 0C)	High impedance (input mode)
$P0D_0$ to $P0D_3$	I/O	CMOS (push-pull) 4-bit I/O port (port 0D)	High impedance (input mode)

- Non-port pins

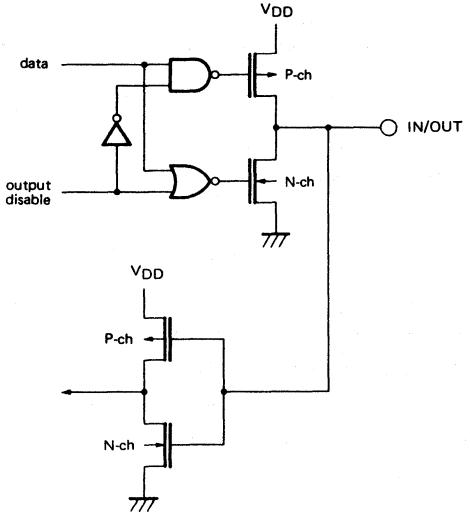
Pin name	I/O	Function	Reset
$\overline{RESET}$	Input	• System reset input pin • A built-in pull-up resistor can be provided (mask-selected).	
V_{DD}		• Positive power supply pin	
GND		• GND pin	
OSC_0, OSC_1		• Pins to be connected to the system clock resonator	

I/O: Input/output

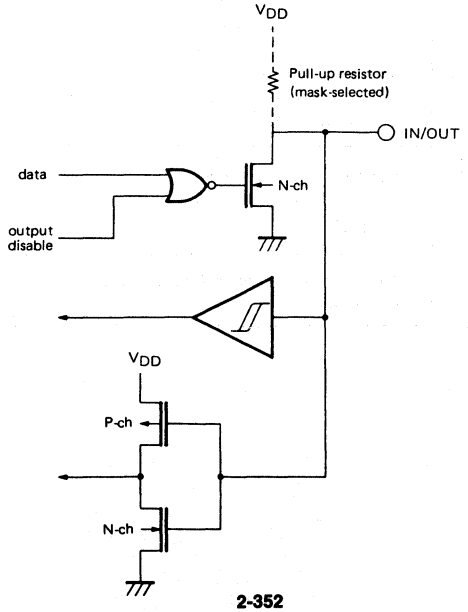
PIN INPUT/OUTPUT CIRCUITS

Following are schematics of the input/output circuits of the pins of the μPD17108.

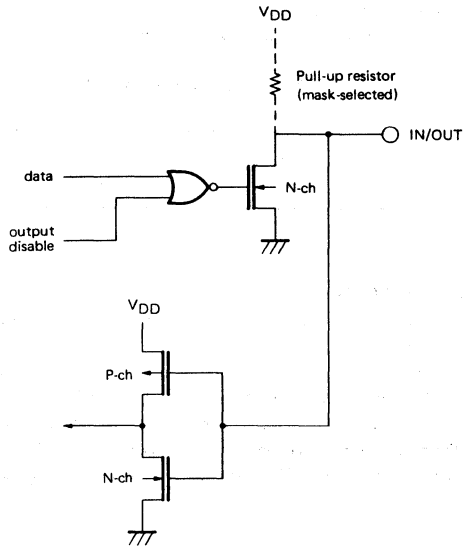
(1) P0A, P0C, and P0D



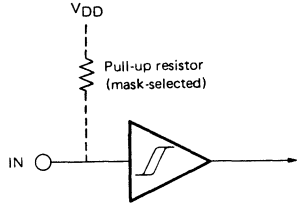
(2) $P0B_0$ and $P0B_1$



(3) $P0B_2$ and $P0B_3$



(4) $\overline{RESET}$

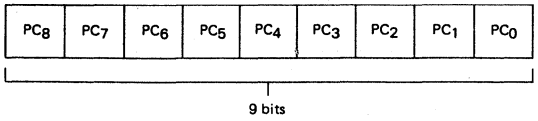


1. PROGRAM COUNTER (PC)

1.1 FORMAT OF THE PROGRAM COUNTER (PC)

The program counter is a 9-bit binary counter formatted as shown in Fig. 1-1.

Fig. 1-1 Format of the Program Counter



1.2 FUNCTIONS OF THE PROGRAM COUNTER (PC)

The program counter specifies the address of a program memory (ROM) or a program.

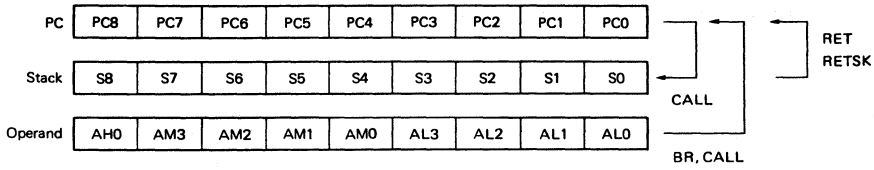
Usually, every time an instruction is executed, the program counter is incremented by one. When a branch instruction (BR), a subroutine call instruction (CALL), or a return instruction (RET) is executed, the address specified in the operand is loaded in the PC. Then the instruction in the address is executed. When a skip instruction is executed, the address of the instruction next to the skip instruction is specified irrespective of the contents of the skip instruction. If the skip conditions are satisfied, the instruction next to the skip instruction is regarded as a No Operation (NOP) instruction. So, the NOP instruction is executed and the address of the next instruction is specified.

2. STACK

Stack of the μPD17108 is a register in which the return address of a program is saved when a subroutine call instruction is executed. One level of address stack is provided.

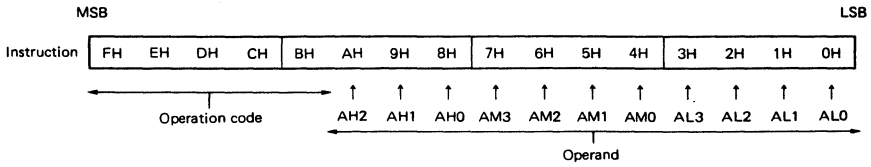
Fig. 2-1 shows the relationship between PC, stack, and instructions.

Fig. 2-1 Relationship between PC, Stack, and Instructions



In Fig. 2-1, AHn, AMn, and ALn (n = 0 to 3) indicate bit positions in a 16-bit instruction as follows:

Fig. 2-2 Format of a 16-Bit Instruction



When the assembler (AS17K) is not used and a BR or CALL instruction is used, AH2 and AH1 must be set to 0.

Sn (n = 0 to 8) denotes a stack.

RESET signal input clears all bits of the program counter to 0.

3. PROGRAM MEMORY (ROM)

Fig. 3-1 shows the configuration of program memory (ROM).

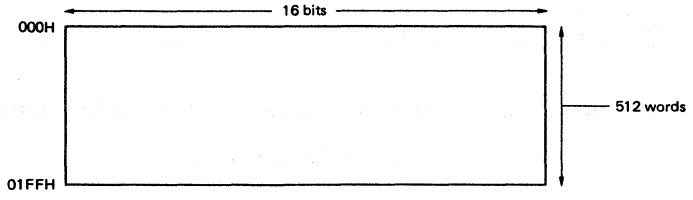
The program memory consists of 512 words by 16 bits.

The program memory is addressed in units of 16 bits and it ranges from addresses 000H to 01FFH. Each address is specified by the program counter (PC).

Since an instruction consists of 16 bits (one word), the instruction is stored at one address of the program memory.

Address 000H is assigned to a reset start address.

Fig. 3-1 Program Memory Map



4. DATA MEMORY (RAM)

The data memory stores data of arithmetic/logic and control operations. Data can be always written to or read from it by means of instructions.

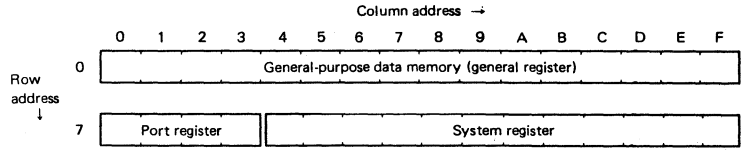
4.1 FORMAT OF THE DATA MEMORY (RAM)

Fig. 4-1 shows the format of the data memory (RAM).

The data memory is configured in units of 4 bits, or "1 nibble," and an address is assigned to each 4-bits of data. The 3 high-order bits are called the "row address," and the 4 low-order bits are called the "column address."

According to its functions, the data memory is divided into 3 blocks as shown below: general-purpose data memory, port register, and system register.

Fig. 4-1 Data Memory Map



4.1.1 Functions of the general-purpose data memory

The general-purpose data memory is a part of the data memory from which the system register (SYSREG) and port register are excluded. By executing a data memory manipulation instruction, a 4-bit arithmetic operation and comparison, evaluation, and transfer between data on data memory and any immediate data can be executed with a single operation.

4.1.2 Functions of the general register

The general register indicates any identical row address (16 nibbles) in the data memory specified in the register pointer (RP) in the system register. Since the μPD17108 register pointer is always set to 0, the general-purpose data memory is also used as a general register. The general register can operate or transfer data to and from the data memory.

4.1.3 Functions of the port register

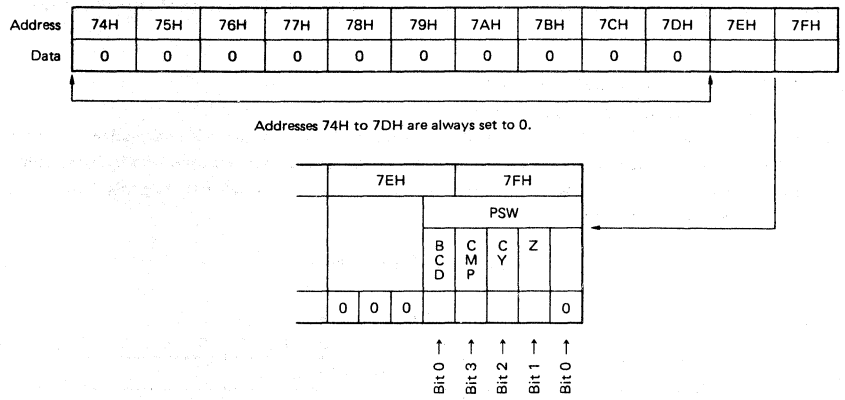
The port register is used to set output data or to read the input data of input/output ports.

Once data is written to the port register corresponding to a port, the port is set as an output port and continues to output the value unless the value is rewritten. Whenever a read instruction is executed for a port register, the read data indicates the states of the pins, not the value of the port register, regardless of whether the pins are in the input or output mode.

4.1.4 Functions of the system register

The system register controls the CPU. The program status word (PSW) is the only system register existing in the μPD17108.

Fig. 4-2 System Register Map

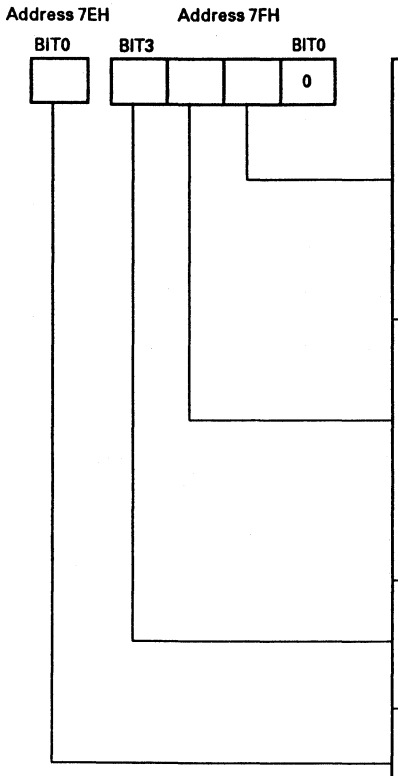


Bit 0 at address 7EH and the high-order three bits at address 7FH are assigned to the program status word.

The BCD flag is mapped in bit 0 at address 7EH, the CMP flag is mapped in bit 3 at address 7FH, the carry (CY) flag is mapped in bit 2 at address 7FH, and the zero (Z) flag is mapped in bit 1 at address 7FH.

The high-order three bits at address 7EH and bit 0 at address 7FH are always set to 0.

Fig. 4-3 Format of the Program Status Word



Zero flag (Z)	Set to 0 when: • An arithmetic operation generates a result of zero if CMP = 0. • An arithmetic operation generates a result of zero and Z = 1 if CMP = 1. When the Z flag is already 0, it remains unchanged. Reset to 1 when: • An arithmetic operation generates a result other than zero.
Carry flag (CY)	Set to 0 when: • An addition produces a carry or a subtraction produces a borrow. • The LSB of the operand in the RORC instruction is 1. Reset to 1 when: • Neither a carry nor borrow is produced. • The LSB of the operand in the RORC instruction is 0.
Compare flag (CMP)	If this flag is set, the result of an arithmetic operation is not stored in memory or general registers. The flag is automatically reset by executing the SKT or SKF instruction.
BCD flag (BCD)	If this flag is set, arithmetic operations are performed in decimal, and if this flag is reset, arithmetic operations are performed in binary.

Comparison instructions (SKE, SKNE, SKGE, or SKLT) do not change the state of the CY flag, but an arithmetic operation may affect the CY flag according to the result even if the CMP flag is set.

Each bit of the program status word is initialized to 0 when a reset signal is applied.

The Z flag in the program status word changes according to the set value of the CMP flag as listed in Table 4-1.

Table 4-1 Change in Z Flag

Condition	Z flag value	
	CMP = 0	CMP = 1
Reset	0	–
Memory manipulation sets the Z flag to 0.	0	0
Memory manipulation sets the Z flag to 1.	1	1
Arithmetic operation results in a non-zero value.	0	0
Arithmetic operation results in 0.	1	Z_{n-1}

Z_{n-1}: The Z flag value presents immediately before arithmetic operation

While CMP is 1, if an arithmetic operation results in 0H when the value of the Z flag is 1, the Z flag does not change. If an arithmetic operation results in other than 0H, the Z flag is reset to 0 and remains intact even when a second arithmetic operation results in 0H.

After the CMP and Z flags are set to 1, subtraction and comparison are performed several times. Then, if the Z flag still indicates 1, all of the comparison operations showed a match, resulting in 0. If the Z flag is 0 after the comparison operations, a mismatch occurred in at least one comparison operation.

5. ARITHMETIC AND LOGIC UNIT (ALU)

The arithmetic and logic unit (ALU) performs arithmetic operations, logical operations, bit tests, comparisons, and rotations on 4-bit data.

5.1 ARITHMETIC OPERATIONS

Arithmetic operations are performed on binary or decimal data. If the BCD flag in the program status word is 1, the ALU operates on decimal data, and if the flag is 0, it operates on binary data.

If an addition produces a carry or if a subtraction produces a borrow, the carry (CY) flag is set to 1. If neither a carry nor borrow is produced, the flag is reset to 0.

If an arithmetic operation results in zero, the zero (Z) flag is set to 1. Otherwise, the flag is reset to 0.

(1) Binary operation

If the result of a binary arithmetic operation is greater than 15 (1111B), a carry is made. If it is less than zero, a borrow is made. In either case, the CY flag is set to 1.

(2) Decimal operation

If the result of a decimal arithmetic operation is greater than 9 (1001B), a carry is made. If it is less than 0, a borrow is made. In either case, the CY flag is set to 1.

Decimal operations are allowed if one of the following results is generated. If the result of a decimal operation does not fall into these ranges, the CY flag is set to 1, and a result greater than or equal to 10 (1010B) is produced.

1. Addition must generate a result from 0 to 19.
2. Subtraction must generate a result from 0 to 9 or -10 to -1.

5.2 LOGICAL OPERATIONS

Logical operations include ANDing, ORing, and XORing.

5.3 OTHER OPERATIONS

The ALU enables bit testing, comparison, and data rotation.

6. PORTS

6.1 PORT 0A ($P0A_0$ to $P0A_3$)

Port 0A is a 4-bit input/output port. CMOS (push-pull) outputs appear on these pins.

Input and output are set in units of nibbles. The input mode is set at reset, and the output mode is set by writing data to the port register in address 70H of the data memory. The output mode is maintained until the system is reset.

Output to the port is executed via the port register. Once data is written to the port register, all pins of the port P0A are placed in the output mode to continue to output written data. The data is retained unless new data is written to the register.

Whenever the port register is read, the read data indicates the states of the pins, not the contents of the port register, regardless of whether the pins are in the input or output mode. In this case, the contents of the port register remain unchanged.

6.2 PORT 0B ($P0B_0$/RLS_{HALT}, $P0B_1$/RLS_{STOP}, $P0B_2$, $P0B_3$)

Port 0B is a 4-bit input/output port. Only N-ch open-drain outputs appear on the pins of port 0B. The N-ch open-drain output mode allows application of 9 V, so it can be used for interfacing with a circuit operating on a different power supply voltage.

Input and output are set in units of nibbles. The input mode is set at reset, and the output mode is set by writing data to the port register in address 71H of the data memory. The output mode is maintained until the system is reset.

Output to the port is executed via the port register. Once data is written to the port register, all pins of port P0B are placed in the output mode to continue to output written data. The data are retained unless new data is written to the register.

Whenever the port register is read, the read data indicates the states of the pins, not the contents of the port register, regardless of whether the pins are in the input or output mode. In this case, the contents of the port register remain unchanged.

The port register for port B consists of four bits but its highest bit is always set to 0. This means that if an attempt is made to write data to the highest bit of 71H, the data is invalidated and if an attempt is made to read it, 0 is always returned.

When the μPD17108 is in the HALT or STOP mode, $P0B_0$ and $P0B_1$ function as pseudo interrupt pins to release the HALT and STOP modes. (Refer to Section 8).

6.3 PORT 0C ($P0C_0$ to $P0C_3$)

Port 0C is a 4-bit input/output port. CMOS (push-pull) outputs appear on these pins.

Input and output are set in units of nibbles. The input mode is set at reset, and the output mode is set by writing data to the port register in address 72H of the data memory. The output mode is maintained until the system is reset.

Output to the port is executed via the port register. Once data is written to the port register, all pins of the port P0C are placed in the output mode to continue to output written data. The data is retained unless new data is written to the register.

Whenever the port register is read, the read data indicates the states of the pins, not the contents of the port register, regardless of whether the pins are in the input or output mode. In this case, the contents of the port register remain unchanged.

6.4 PORT 0D ($P0D_0$ to $P0D_3$)

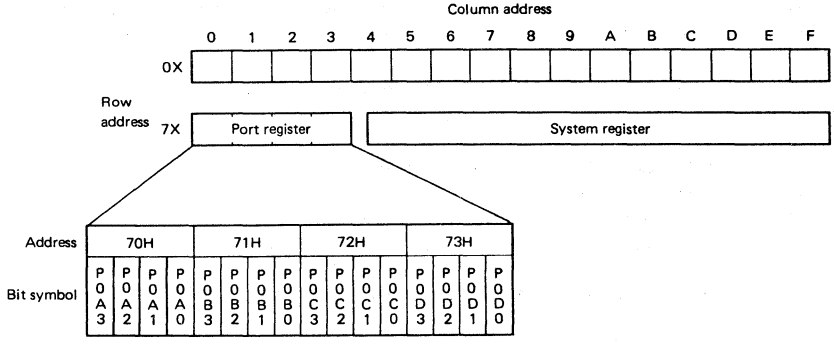
Port 0D is a 4-bit input/output port. CMOS (push-pull) outputs appear on these pins.

Input and output are set in units of nibbles. The input mode is set at reset, and the output mode is set by writing data to the port register in address 73H of the data memory. The output mode is maintained until the system is reset.

Output to the port is executed via the port register. Once data is written to the port register, all pins of the port P0D are placed in the output mode to continue to output written data. The data is retained until new data is written to the register.

Whenever the port register is read, the read data indicates the states of the pins, not the contents of the port register, regardless of whether the pins are in the input or output mode. In this case, the contents of the port register remain unchanged.

Fig. 6-1 Port Register Map



6.5 RECOMMENDED CONDITIONS FOR UNUSED μPD17108 PINS

To prevent malfunction, process unused input/output pins as shown below.

Table 6-1 Recommended Conditions for Unused Pins

Input/ output mode	Port	Recommended connection
Input mode	Ports A, B, C, and D	Connect to V_{DD} or GND.
Output mode	CMOS ports (ports A, C, D)	Open
	N-ch open-drain port (port B)	

7. STANDBY FUNCTIONS

The μPD17108 provides two standby modes, the HALT mode and the STOP mode.

7.1 HALT MODE

The HALT mode stops the program counter (PC) while allowing the system clock to continue operating. The HALT mode can be entered with the HALT instruction, and can be released by a reset signal ($\overline{RESET}$) or input to the $P0B_0$ pin. When the HALT mode is released by input to the $P0B_0$ pin, the next instruction after the HALT instruction is executed without waiting for stable oscillation of the system clock.

When the HALT mode is released forcibly by the reset signal ($\overline{RESET}$), normal system reset occurs, and execution starts at address 0H.

7.2 STOP MODE

The STOP mode stops oscillation of the system clock so that data can be retained at low voltage. The STOP mode can be entered with the STOP instruction, and can be released by a reset signal ($\overline{RESET}$) or input to the $P0B_1$ pin. When the mode is released by input to the $P0B_1$ pin, execution starts with the next instruction after the STOP instruction.

When the STOP mode is released forcibly by the reset signal ($\overline{RESET}$), normal system reset occurs, and execution starts at address 0H.

7.3 SETTING AND RELEASING THE STANDBY MODES

(1) Setting and releasing the HALT mode

The conditions for releasing the HALT mode can be selected with the least significant bit of the operand in the HALT instruction. The high-order three bits of the operand must be set to 0.

Table 7-1 Setting and Releasing Conditions Specified in the HALT Instruction

HALT 000XB ← 4-bit data in the operand

X	Conditions for setting/releasing the HALT mode
0	Executing the HALT instruction enters the HALT mode unconditionally. The mode can be released only by the reset signal ($\overline{RESET}$). After the mode is released, instructions are executed starting at address 0H.
1	If P0B0 is 0, executing the HALT instruction enters the HALT mode. If P0B0 is 1, executing the HALT instruction does not enter the HALT mode. Application of the reset signal ($\overline{RESET}$) releases the HALT mode. After the mode is released, instructions are executed starting at address 0H. The rising edge of an input signal on the $P0B_0$ pin also releases the HALT mode. In this case, execution starts with the next instruction after the HALT instruction.

(2) Setting and releasing the STOP mode

Conditions to release the STOP mode can be selected with the least significant bit of the operand in the STOP instruction. The high-order three bits of the operand must be set to 0.

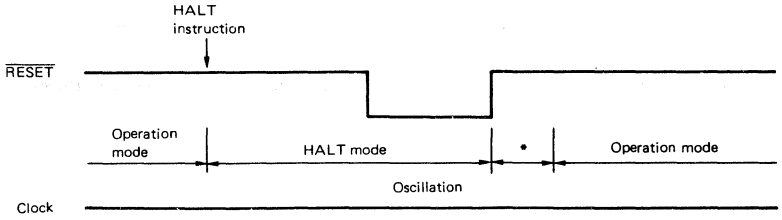
Table 7-2 Setting/Releasing Conditions Specified in the STOP Instruction

STOP 000XB ← 4-bit data in the operand

X	Conditions for setting/releasing the STOP mode
0	Executing the STOP instruction enters the STOP mode unconditionally. All peripheral circuits are placed in the same initial state as when the system is reset, then they stop operating. Only the reset signal ($\overline{RESET}$) can release the STOP mode. After the mode is released, instructions are executed starting at address 0H.
1	If P0B1 is 0, executing the STOP instruction enters the STOP mode. If P0B1 is 1, executing the STOP instruction does not enter the STOP mode. Application of the reset signal ($\overline{RESET}$) can release the STOP mode. After the mode is released, instructions are executed starting at address 0H. The rising edge of the signal applied to the $P0B_1$ pin can also release the mode. In this case, execution starts with the next instruction after the STOP instruction.

7.4 TIMING FOR RELEASING THE STANDBY MODES

Fig. 7-1 Releasing the HALT Mode by $\overline{RESET}$ Input



When the $\overline{RESET}$ signal is applied to release the HALT mode, the $\overline{RESET}$ input makes a transition from low to high, then an operation mode is entered.

* The HALT mode remains effective in this period, waiting for the operation mode.
At least eight clock pulses on the OSC_1 pin cause operation to start.

Fig. 7-2 Releasing the HALT Mode by Interrupt

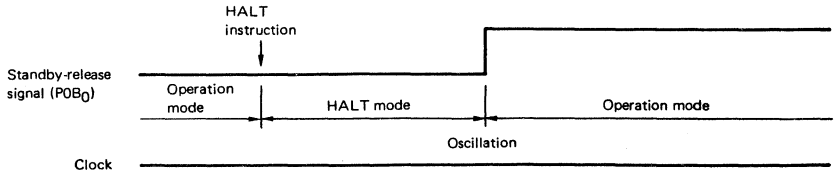
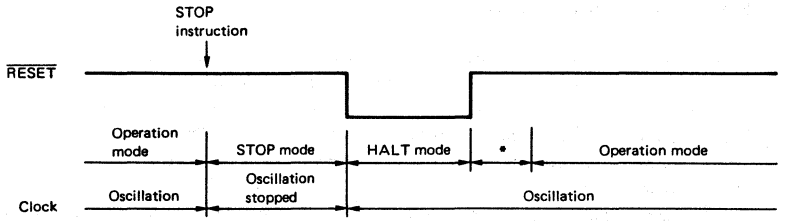


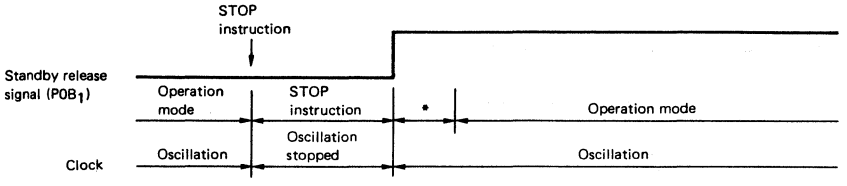
Fig. 7-3 Releasing the STOP Mode by $\overline{\text{RESET}}$ Input



As soon as the $\overline{\text{RESET}}$ input makes a transition from high to low in the STOP mode, the system clock starts generating clock pulses.

* The HALT mode remains effective in this period, waiting for the generation of clock pulses to stabilize. At least eight clock pulses on the OSC_1 pin cause operation to start.

Fig. 7-4 Releasing the STOP Mode by Interrupt



* The HALT mode remains effective in this period, waiting for the generation of clock pulses to stabilize. At least eight clock pulses on the OSC_1 pin cause operation to start.

8. RESET FUNCTION

8.1 HARDWARE STATE AT RESET

A low-active reset signal applied to the $\overline{\text{RESET}}$ pin sets the hardware states as listed below. A transition from low to high on the $\overline{\text{RESET}}$ pin releases the reset state.

Table 8-1 Hardware after Reset

Name	Location in memory space	Set value
Program counter		000H
RAM	0H to 0FH	Data present before reset is retained.
Program status word (PSW)	Bit 0 at 7EH Bits 3 to 1 at 7FH	All 0s
Ports 0A to 0D	70H to 73H	Data present before reset is retained. All pins are placed in the input mode.

9. ASSEMBLER RESERVED WORDS

9.1 MASK OPTION PSEUDO INSTRUCTIONS

Source programs in the assembly language for the μPD17108 must include mask option pseudo instructions to select mask options. To do this, be sure to catalog the D17108. OPT file in AS17108 (device file for μPD17108) into the current directory beforehand.

Options must be mask-selected for the following pins:

- $P0B_0$
- $P0B_1$
- $P0B_2$
- $P0B_3$
- $\overline{RESET}$

9.1.1 OPTION and ENDOP pseudo instructions

The part starting with the OPTION pseudo instruction and ending with the ENDOP pseudo instruction is referred to as a mask option definition block.

The coding format of the mask option definition block is shown on the next page.

Within this block, the mask option definition pseudo instructions listed in Table 9-1 can be coded.

Format

Symbol	Mnemonic	Operand	Comment
[label :]	OPTION		[; comment]
	.		
	.		
	.		
	ENDOP		

9.1.2 Mask option definition pseudo instructions

Table 9-1 lists the mask option definition pseudo instructions corresponding to each pin.

Table 9-1 Mask Option Definition Pseudo Instructions

Pin	Mask option pseudo instruction	Number of operands	Operand name
$P0B_3$ to $P0B_0$	OPTP0B	4	P0BPLUP (with pull-up resistor) OPEN (without pull-up resistor)
RESET	OPTRES	1	RESPLUP (with pull-up resistor) OPEN (without pull-up resistor)

The coding format of OPTP0B is shown on the next page. The operands $P0B_3$, $P0B_2$, $P0B_1$ and $P0B_0$ are defined in this order.

Format

Symbol	Mnemonic	Operand	Comment
[label :]	OPTP0B	($P0B_3$), ($P0B_2$), ($P0B_1$), ($P0B_0$)	[; comment]

The coding format of OPTRES is shown below.

Format

Symbol	Mnemonic	Operand	Comment
[label :]	OPTRES	(RESET)	[; comment]

Example:

To set the following mask options in a μPD17108 source file to be assembled:

$P0B_3$:	Pull-up	$P0B_2$:	Pull-up	$P0B_1$:	Open	$P0B_0$:	Open
RESET:	Pull-up						

```
                                .
                                .
                                .
;17108
Setting mask options:           OPTION
                                OPTP0B P0BPLUP, P0BPLUP, OPEN, OPEN
                                OPTRES RESPLUP
                                ENDOP
                                .
                                .
                                .
```

9.2 RESERVED WORDS

Table 9-2 lists the reserved words defined in the μPD17108 device file (AS17108).

Table 9-2 Reserved Words

Name	Attribute	Value	Read/write	Description
P0A0	FLG	0.70H.0	Read/write	Bit 0 of port 0A
P0A1	FLG	0.70H.1	Read/write	Bit 1 of port 0A
P0A2	FLG	0.70H.2	Read/write	Bit 2 of port 0A
P0A3	FLG	0.70H.3	Read/write	Bit 3 of port 0A
P0B0	FLG	0.71H.0	Read/write	Bit 0 of port 0B
P0B1	FLG	0.71H.1	Read/write	Bit 1 of port 0B
P0B2	FLG	0.71H.2	Read/write	Bit 2 of port 0B
P0B3	FLG	0.71H.3	Read/write	Bit 3 of port 0B
P0C0	FLG	0.72H.0	Read/write	Bit 0 of port 0C
P0C1	FLG	0.72H.1	Read/write	Bit 1 of port 0C
P0C2	FLG	0.72H.2	Read/write	Bit 2 of port 0C
P0C3	FLG	0.72H.3	Read/write	Bit 3 of port 0C
P0D0	FLG	0.73H.0	Read/write	Bit 0 of port 0D
P0D1	FLG	0.73H.1	Read/write	Bit 1 of port 0D
P0D2	FLG	0.73H.2	Read/write	Bit 2 of port 0D
P0D3	FLG	0.73H.3	Read/write	Bit 3 of port 0D
BCD	FLG	0.7EH.0	Read/write	BCD arithmetic flag
PSW	MEM	0.7FH	Read/write	Program status word
Z	FLG	0.7FH.1	Read/write	Zero flag
CY	FLG	0.7FH.2	Read/write	Carry flag
CMP	FLG	0.7FH.3	Read/write	Compare flag

10. INSTRUCTION SET

10.1 INSTRUCTION SET LIST

$b_{14}-b_{11}$ \ b_{15}		0	1
BIN	HEX		
0 0 0 0	0	ADD r, m	ADD m, #i
0 0 0 1	1	SUB r, m	SUB m, #i
0 0 1 0	2	ADDC r, m	ADDC m, #i
0 0 1 1	3	SUBC r, m	SUBC m, #i
0 1 0 0	4	AND r, m	AND m, #i
0 1 0 1	5	XOR r, m	XOR m, #i
0 1 1 0	6	OR r, m	OR m, #i
0 1 1 1	7	RET RETSK RORC r STOP s HALT h NOP	
1 0 0 0	8	LD r, m	ST m, r
1 0 0 1	9	SKE m, #i	SKGE m, #i
1 0 1 0	A		
1 0 1 1	B	SKNE m, #i	SKLT m, #i
1 1 0 0	C	BR addr	CALL addr
1 1 0 1	D		MOV m, #i
1 1 1 0	E		SKT m, #n
1 1 1 1	F		SKF m, #n

10.2 INSTRUCTIONS

Legend:

M		: One of data memory	n		: Bit position : 4 bits
	m	: Data memory address specified by [m_H, m_L] of each bank	addr		: One of program memory address ; 11 bits
	m_H	: Data memory address high (row address) ; 3 bits		a_H	: Program memory address high ; 3 bits
	m_L	: Data memory address low (column address) ; 4 bits		a_M	: Program memory address middle ; 4 bits
R		: One of general register specified by [(RP), r]		a_L	: Program memory address low ; 4 bits
r		: General register address low (column address) ; 4 bits	CY		: Carry flag
	RP	: General register pointer	CMP		: Compare flag
PC		: Program counter	s		: Stop release condition
SP		: Stack pointer	h		: Halt release condition
STACK		: Stack specified by (SP)	[ ]		: Address of M, R
i		: Immediate data ; 4 bits	( )		: Contents of M, R

Type	Mnemonic	Operand	Function	Operation	Machine code			
					Op code	3 bits	4 bits	4 bits
Add	ADD	r, m	Add memory to register	R← (R) + (M)	00000	m_H	m_L	r
		m, #i	Add immediate data to memory	M← (M) + i	10000	m_H	m_L	i
	ADDC	r, m	Add memory to register with carry	R← (R) + (M) + (CY)	00010	m_H	m_L	r
		m, #i	Add immediate data to memory with carry	R← (M) + i + (CY)	10010	m_H	m_L	i
Subtract	SUB	r, m	Subtract memory from register	R← (R) − (M)	00001	m_H	m_L	r
		m, #i	Subtract immediate data from memory	M← (M) − i	10001	m_H	m_L	i
	SUBC	r, m	Subtract memory from register with borrow	R← (R) − (M) − (CY)	00011	m_H	m_L	r
		m, #i	Subtract immediate data from memory with borrow	M← (M) − i − (CY)	10011	m_H	m_L	i
Compare	SKE	m, #i	Skip if memory equal to immediate data	M−i, skip if zero	01001	m_H	m_L	i
	SKGE	m, #i	Skip if memory greater than or equal to immediate data	M−i, skip if not borrow	11001	m_H	m_L	i
	SKLT	m, #i	Skip if memory less than immediate data	M−i, skip if borrow	11011	m_H	m_L	i
	SKNE	m, #i	Skip if memory not equal to immediate data	M−i, skip if not zero	01011	m_H	m_L	i
Logical operation	AND	m, #i	Logical AND of memory and immediate data	M← (M) AND i	10100	m_H	m_L	i
		r, m	Logical AND of register and memory	R← (R) AND (M)	00100	m_H	m_L	r
	OR	m, #i	Logical OR of memory and immediate data	M← (M) OR i	10110	m_H	m_L	i
		r, m	Logical OR of register and memory	R← (R) OR (M)	00110	m_H	m_L	r
	XOR	m, #i	Logical XOR of memory and immediate data	M← (M) XOR i	10101	m_H	m_L	i
		r, m	Logical XOR of register and memory	R← (R) XOR (M)	00101	m_H	m_L	r
Transfer	LD	r, m	Load memory of register	R← (M)	01000	m_H	m_L	r
	ST	m, r	Store register to memory	(M)←R	11000	m_H	m_L	r
	MOV	m, #i	Move immediate data to memory	M←i	11101	m_H	m_L	i
Test	SKT	m, #n	Test memory bits, then skip if all bits specified are true	CMP ←0 skip if M_n=all "1"	11110	m_H	m_L	n
	SKF	m, #n	Test memory bits, then skip if all bits specified are false	CMP ←0 skip if M_n=all "0"	11111	m_H	m_L	n

Type	Mnemonic	Operand	Function	Operation	Machine code			
					Op code	3 bits	4 bits	4 bits
Branch	BR	addr	Jump to the address	PC←ADDR	01100	a_H	a_M	a_L
Shift	RORC	r	Rotate register right with carry	(CY)→(R)→CY	00111	000	0111	r
Subroutine	CALL	addr	Call subroutine	SP←(SP)−1 STACK←((PC)+1), PC←ADDR	11100	a_H	a_M	a_L
	RET		Return to main routine from subroutine	PC←(STACK), SP←(SP)+1	00111	000	1110	0000
	RETSK		Return to main routine from subroutine, then skip unconditionary	PC←(STACK), SP←(SP)+1 and skip	00111	001	1110	0000
Miscellaneous	STOP	s	Stop clock	STOP	00111	010	1111	s
	HALT	h	Halt the CPU, restart by condition h	HALT	00111	011	1111	h
	NOP		No operation	No Operation	00111	100	1111	0000

11. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage	V_{DD}			-0.3 to +7.0	V
Input Voltage	V_I	P0A, P0C, P0D		-0.3 to V_{DD}+0.3	V
		P0B	(*1)	-0.3 to V_{DD}+0.3	V
Output Voltage	V_O		(*2)	-0.3 to +11	V
		P0A, P0C, P0D, $\overline{RESET}$		-0.3 to V_{DD}+0.3	V
High-Level Output Current	I_{OH}		(*1)	-0.3 to V_{DD}+0.3	V
		P0B	(*2)	-0.3 to +11	V
Low Level Output Current	I_{OL}	Each of P0A, P0B, P0C, P0D		-5	mA
		Total of all pins		-15	mA
				30	mA
Operating Temperature	T_{OPT}	Each of P0A, P0B, P0C, P0D		100	mA
		Total of all pins		-40 to +85	°C
Storage Temperature	T_{stg}			-65 to +150	°C
Power Consumption	P_d	T_a = 85° C	22-pin shrink DIP	400	mW
			24-pin SOP	250	

*1 N-ch open-drain input/output and input/output with a pull-up resistor provided

*2 N-ch open-drain input/output

CAPACITANCE (T_a = 25 °C, V_{DD} = 0 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	Unit	CONDITION
Input Capacitance	C_{IN}			15	pF	f = 1 MHz
Input/Output Capacitance	C_{IO}			15	pF	0V for pins other than pins to be measured

DC CHARACTERISTICS (T_a = -40 to + 85 °C, V_{DD} = 2.5 to 60 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
High-Level Input Voltage	V_{IH1}	0.7 V_{DD}		V_{DD}	V	Other than the following pins and port
	V_{IH2}	0.8 V_{DD}		V_{DD}	V	P0B and $\overline{RESET}$
	V_{IH3}	0.8 V_{DD}		9	V	P0B *3
	V_{IH4}	V_{DD} - 0.5		V_{DD}	V	OSC_1
Low-Level Input Voltage	V_{IL1}	0		0.3 V_{DD}	V	Other than the following pins and port
	V_{IL2}	0		0.2 V_{DD}	V	P0B and $\overline{RESET}$
	V_{IL3}	0		0.5	V	OSC_1
High-Level Output Voltage on P0A, P0C, and P0D	V_{OH}	V_{DD} - 2.0			V	V_{DD} = 4.5 to 6.0 V, I_{OH} = -2 mA
		V_{DD}- 1.0			V	I_{OH} = -200 μA
Low-Level Output Voltage on P0A, P0B, P0C, and P0D	V_{OL}			2.0	V	V_{DD} = 4.5 to 6.0 V, I_{OL} = 15 mA
				0.5	V	I_{OL} = 600 μA
High-Level Input Leakage Current on P0A to P0D	I_{LIH1}			5	μA	V_{IN} = V_{DD}
	I_{LIH2}			10	μA	V_{IN} = 9 V *3
Low-Level Input Leakage Current on P0A to P0D	I_{LIL}			-5	μA	V_{IN} = 0 V
High-Level Output Leakage Current on P0A to P0D	I_{LOH1}			5	μA	V_{OUT} = V_{DD}
	I_{LOH2}			10	μA	V_{OUT} = 9 V *3
Low-Level Output Leakage Current on P0A to P0D	I_{LOL}			-5	μA	V_{OUT} = 0 V
Resistor Provided for Input Pin		20	47	95	KΩ	$\overline{RESET}$ (pull-up)
Resistor Provided for Input/Output Pin		5	15	30	KΩ	P0B0, P0B1, P0B2 and P0B3 (pull-up)

*3 When N-ch open-drain input/output is selected

CHARACTERISTICS	SYMBOL	TYP.	MAX.	UNIT	MIN.	CONDITION
Power Supply Current *4	I_{DD1}	0.4	1.2	mA	Operation mode	V_{DD} = 5 V ± 10 % f_{CC} = 1.0 MHz ± 20 %
		50	150	μA		V_{DD} = 3 V ± 10 %, f_{CC} = 250 KHz ± 20 %
	I_{DD2}	0.3	0.9	mA	HALT mode	V_{DD} = 5 V ± 10 %, f_{CC} = 1.0 MHz ± 20 %
		40	120	μA		V_{DD} = 3 V ± 10 %, f_{CC} = 250 kHz ± 20 %
	I_{DD3}	0.1	10	μA	STOP mode	V_{DD} = 5 V ± 10 %
		0.1	5	μA		V_{DD} = 3 V ± 10 %

*4 This current excludes the current which flows through the built-in pull-up resistors.

CHARACTERISTICS OF DATA MEMORY FOR HOLDING DATA ON LOW SUPPLY VOLTAGE IN THE STOP MODE (T_a = − 40 to +85 °C)

CHARACTERISTICS	SYMBOL	MIN.	TYPE	MAX.	UNIT	CONDITION
Data Hold Supply Voltage	V_{DDDR}	2.0		6.0	V	
Data Hold Supply Current	I_{DDDR}		0.1	5.0	μA	V_{DDDR} = 2.0 V
Release Signal Set Time	t_{SREL}	0			μs	

AC CHARACTERISTICS (T_a = -40 to +85 °C, V_{DD} = 2.5 to 6.0 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Internal Clock Cycle Time	T_{CY}	6.6		160	μs	V_{DDD} = 4.5 to 6.0 V
		26.6		160	μs	
High/Low Level Width on $P0B_0$ and $P0B_1$	T_{PBH} T_{PBL}	10			μs	
High/Low Level Width on $\overline{RESET}$	T_{RSH} T_{RSL}	10			μs	

4-BIT SINGLE-CHIP MICROCONTROLLER

The μPD17P107 is a tiny microcontroller composed of a ROM with 1K-byte capacity, a RAM with 16-word capacity and 11 I/O ports. It is a product developed by replacing the on-chip mask ROM of the μPD17107 with the one-time PROM.

The μPD17P107CX, which is writable only once, and the μPD17P107GS are available. They are convenient for evaluating or producing in small quantities the μPD17107.

Very efficient programming is possible due to the μPD17000 architecture incorporating the general-purpose register system, which allows the data memory to be manipulated directly, being adopted in the CPU. Every instruction is composed of 1 word of 16-bit length.

FEATURES

- μPD17107 compatible
- Program memory (one-time PROM): 1K byte (512 words × 16 bits)
- Data memory (RAM): 16 words × 4 bits
- I/O ports: 11 ports (N-ch open-drain output 3 ports)
- Instruction execution time: 128 μs (62.5 kHz) to 8 μs (1 MHz)
- Instruction types: 24 types (all 1-word instructions)
- Stack levels: 1 level
- Standby function available (by STOP, HALT instruction)
- Data memory data retainable at low voltage (MIN. 2.0 V)
- With on-chip system clock oscillator (only resistor externally provided)
- Operating supply voltage: 2.5 to 6.0 V (at 250 kHz)
  4.5 to 6.0 V (at 1 MHz)

APPLICATIONS

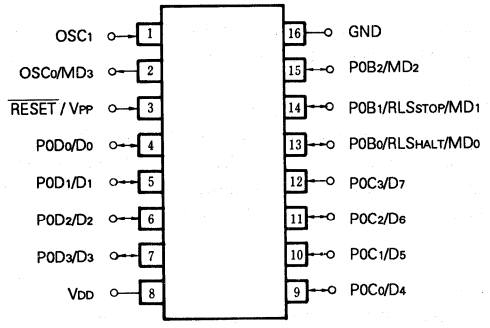
- Electronic control of home electric appliances, TOY, etc.

ORDERING INFORMATION

Order Code	Package
μPD17P107CX	16-pin plastic DIP (300 mil)
μPD17P107GS	16-pin plastic SOP (300 mil)

PIN CONFIGURATION (Top View)

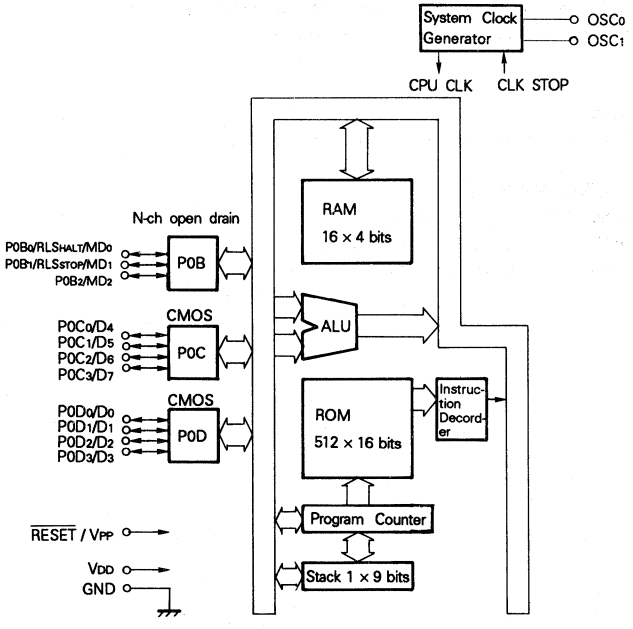
μPD17P107CX/μPD17P107GS



16 Pin Plastic DIP

16 Pin Plastic SOP

BLOCK DIAGRAM



PIN FUNCTIONS

PIN FUNCTION LIST

- Port pins

Pin Name	Input/ Output	Dual-Function Pin		Function		Program Memory Write/Verify Mode	Reset
P0B0	Input/ Output	RLSHALT	MD0	• N-ch open-drain 4-bit input/ output port (Port 0B)	HALT mode releasing	Mode setting pin	High impedance (input mode)
P0B1		RLSSTOP	MD1		STOP mode releasing		
P0B2		MD2					
P0C0	Input/ Output	D4		• CMOS (push-pull) 4-bit input/output port (Port 0C)		8-bit data input/ output pin (high-order 4 bits)	High impedance (input mode)
P0C1		D5					
P0C2		D6					
P0C3		D7					
P0D0	Input/ output	D0		• CMOS (push-pull) 4-bit input/output port (Port 0D)		8-bit data input/ output pin (low-order 4 bits)	High impedance (input mode)
P0D1		D1					
P0D2		D2					
P0D3		D3					

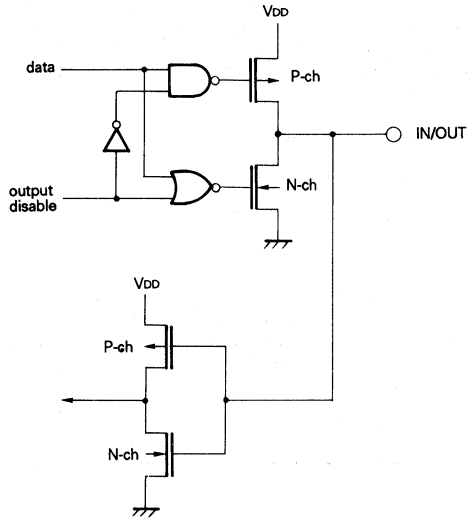
- Other than port pins

Pin Name	Input Output	Dual-Function Pin	Function	Program Memory Write/Verify Mode
$\overline{\text{RESET}}$	Input	VPP	System reset input pin	Voltage impression pin (+12.5 V)
VDD			Positive power pin	Positive power pin (+6.0 V)
GND			GND pin	GND pin
OSC1			System clock oscillation resonator connection pin	Program memory address update
OSC0		MD3	System clock oscillation resonator connection pin	Mode setting pin

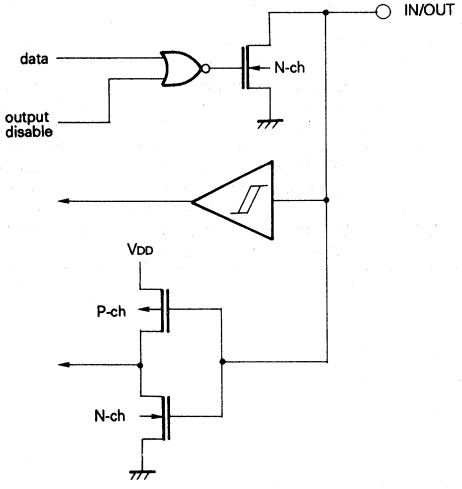
PIN INPUT/OUTPUT CIRCUITS

The μPD17P107 pin input/output circuit diagrams are shown below.

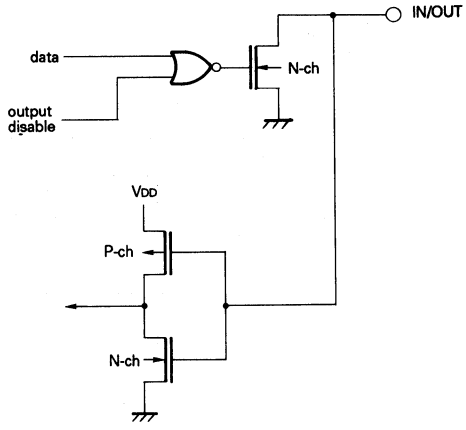
(1) P0C, P0D



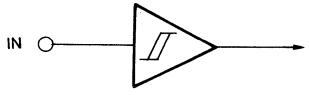
(2) P0B0, P0B1



(3) $P0B_2$



(4) $\overline{\text{RESET}}$



9. DIFFERENCES BETWEEN μPD17P107 AND μPD17107

The μPD17P107 is a product developed by replacing the program memory of the μPD17107 with the on-chip mask ROM with the one-time PROM. These 2 models have the same CPU functions and on-chip hardware with the only difference being the program memory and the mask option. Table 9-1 shows the differences between the μPD17P107 and μPD17107.

Table 9-1 Differences between μPD17P107 and μPD17107

Item	μPD17P107	μPD17107
ROM	One-time PROM 512 × 16 bits	Mask ROM 512 × 16 bits
$P0B_0$ to $P0B_2$ pin pull-up resistor	Not available	Mask option
$\overline{RESET}$ pin pull-up resistor	Not available	Mask option
Connection pin	V_{PP} pin, run mode selection pin available	V_{PP} pin, run mode selection pin not available
Input power	2.5 to 6.0 V (at 250 kHz) 4.5 to 6.0 V (at 1 MHz)	
Package	16-pin DIP 16-pin SOP	

10. ONE-TIME PROM (PROGRAM MEMORY) WRITE AND VERIFY

The μPD17P107's on-chip program memory is a 512 × 16-bit one-time PROM.

To write/verify this one-time PROM, the pins shown in the table below are used. No address input is available. Instead, a system to update the address by the clock input via the OSC_1 pin is adopted.

Pin Name	Function
V_{PP}	Voltage impression pin at program memory write/verify
OSC_1	Address updating clock input pin at program memory write/verify
MD_0 to MD_3	Input pin at program memory write/verify. Used as run mode selection pin.
D_0 to D_7	8-bit data input/output pin at program memory write/verify

10.1 RUN MODE AT PROGRAM MEMORY WRITE/VERIFY

The μPD17P107 assumes the program memory write/verify mode if +6 V is impressed to the V_{DD} pin and +12.5 V is impressed to the V_{PP} pin after the reset status (V_{DD} = 5 V, $\overline{RESET}$ = 0 V) assumed for a certain period of time. In that mode, the following run mode is entered according to the MD_0 to MD_3 pin setting. All the remaining pins are at the GND potential by the pull-down resistor.

Run Mode Setting						Run Mode
V_{PP}	V_{DD}	MD_0	MD_1	MD_2	MD_3	
+12.5 V	+6 V	H	L	H	L	Program memory address 0 clear
		L	H	H	H	Write mode
		L	L	H	H	Verify mode
		H	x	H	H	Program inhibit mode

x: L or H

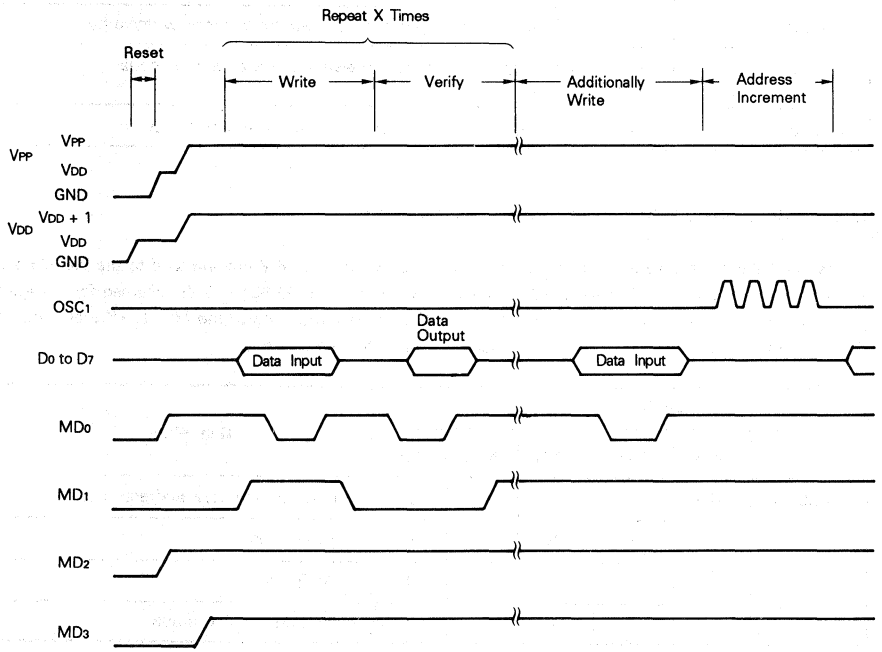
10.2 PROGRAM MEMORY WRITING PROCEDURE

The program memory writing procedure is shown below. High-speed write is possible.

(1) Pull down the pins not to be used to GND via the resistor. The OSC_1 pin at the low level.
(2) Supply 5 V to the V_{DD} pin. The V_{PP} pin at the low level.
(3) Wait 10 μs and then supply 5 V to the V_{PP} pin.
(4) Set the mode setting pin to the program memory address 0 clear mode.
(5) Supply 6 V to V_{DD} and 12.5 V to V_{PP}.
(6) Assume the program inhibit mode.
(7) Write data in the 1-ms write mode.
(8) Assume the program inhibit mode.
(9) Assume the verify mode. If written, go to (10). If not, repeat (7) to (9).

(10) Additionally write (number of times written in (7) to (9): X) × 1 ms.
(11) Assume the program inhibit mode.
(12) Update (+1) the program memory address by inputting a pulse to the OSC_1 pin 4 times.
(13) Repeat (7) to (12) up to the last address.
(14) Assume the program memory address 0 clear mode.
(15) Change the V_{DD}, V_{PP} pin voltage to 5 V.
(16) Power off.

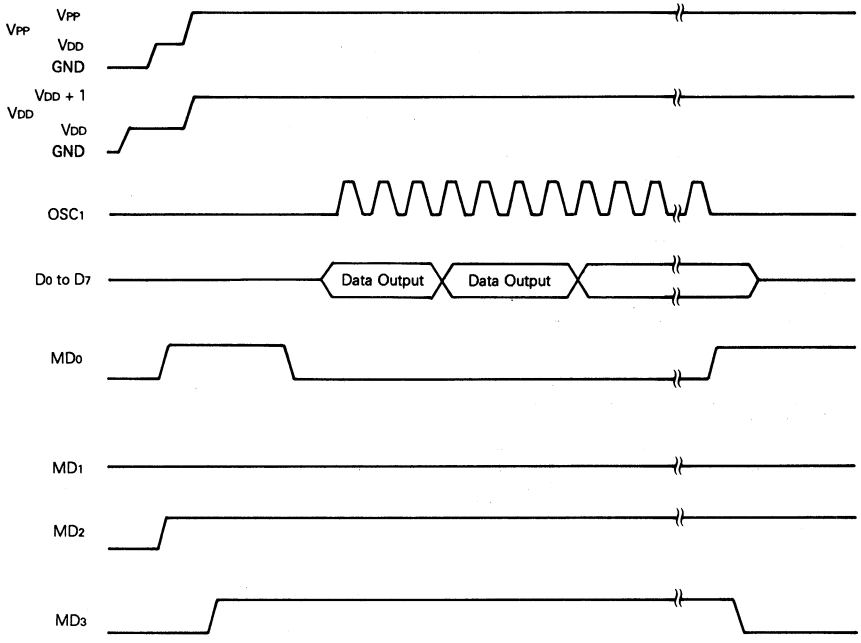
The above procedure of (2) to (12) is shown in the diagram below.



10.3 PROGRAM MEMORY READING PROCEDURE

(1) Pull down the pins not to be used to GND via the resistor. The OSC_1 pin at the low level.
(2) Supply 5 V to the V_{DD} pin. The V_{PP} pin at the low level.
(3) Wait 10 μs and then supply 5 V to the V_{PP} pin.
(4) Set the mode setting pin to the program memory address 0 clear mode.
(5) Supply 6 V to V_{DD} and 12.5 V to V_{PP}.
(6) Assume the program inhibit mode.
(7) Assume the verify mode. Output data sequentially 1 address at a time at intervals of 4 inputs when a clock pulse is input to the OSC_1 pin.
(8) Assume the program inhibit mode.
(9) Assume the program memory address 0 clear mode.
(10) Change the V_{DD}, V_{PP} pin voltage to 5 V.
(11) Power off.

The above procedure of (2) to (9) is shown in the diagram below.



11. ASSEMBLER RESERVED WORDS

Table 11-1 lists the reserved symbols defined in the μPD17P107's device file (AS17107).

Table 11-1 Reserved Symbol List

Name	Attribute	Value	R/W	Description
P0B0	FLG	0.71H.0	R/W	Port 0B, bit 0
P0B1	FLG	0.71H.1	R/W	Port 0B, bit 1
P0B2	FLG	0.71H.2	R/W	Port 0B, bit 2
P0B3*	FLG	0.71H.3	R	Value "0" fixed
P0C0	FLG	0.72H.0	R/W	Port 0C, bit 0
P0C1	FLG	0.72H.1	R/W	Port 0C, bit 1
P0C2	FLG	0.72H.2	R/W	Port 0C, bit 2
P0C3	FLG	0.72H.3	R/W	Port 0C, bit 3
P0D0	FLG	0.73H.0	R/W	Port 0D, bit 0
P0D1	FLG	0.73H.1	R/W	Port 0D, bit 1
P0D2	FLG	0.73H.2	R/W	Port 0D, bit 2
P0D3	FLG	0.73H.3	R/W	Port 0D, bit 3
BCD	FLG	0.7EH.0	R/W	BCD operation flag
PSW	MEM	0.7FH	R/W	Program status word
Z	FLG	0.7FH.1	R/W	Zero flag
CY	FLG	0.7FH.2	R/W	Carry flag
CMP	FLG	0.7FH.3	R/W	Compare flag

*: P0B3, which is not available in the μPD17P107, has been registered as a read only flag to be used as a dummy bit when using a built-in macro.

12. INSTRUCTION SETS

12.1 INSTRUCTION SET LIST

$b_{14}-b_{11}$ \ b_{15}		0		1	
BIN	HEX				
0 0 0 0	0	ADD	r, m	ADD	m, #i
0 0 0 1	1	SUB	r, m	SUB	m, #i
0 0 1 0	2	ADDC	r, m	ADDC	m, #i
0 0 1 1	3	SUBC	r, m	SUBC	m, #i
0 1 0 0	4	AND	r, m	AND	m, #i
0 1 0 1	5	XOR	r, m	XOR	m, #i
0 1 1 0	6	OR	r, m	OR	m, #i
0 1 1 1	7	RET RETSK RORC STOP HALT NOP	 r s h 		
1 0 0 0	8	LD	r, m	ST	m, r
1 0 0 1	9	SKE	m, #i	SKGE	m, #i
1 0 1 0	A				
1 0 1 1	B	SKNE	m, #i	SKLT	m, #i
1 1 0 0	C	BR	addr	CALL	addr
1 1 0 1	D			MOV	m, #i
1 1 1 0	E			SKT	m, #n
1 1 1 1	F			SKF	m, #n

12.2 INSTRUCTION LIST

Legend

M	: One of data memory	n	: Bit position ; 4 bits
m	: Data memory address specified by [m_H, m_L] of each bank	addr	: One of program memory address ; 11 bits
m_H	: Data memory address high (row address) ; 3 bits	a_H	: Program memory address high ; 3 bits
m_L	: Data memory address low (column address) ; 4 bits	a_M	: Program memory address middle ; 4 bits
R	: One of general register specified by [(RP), r]	a_L	: Program memory address low ; 4 bits
r	: General register address low (column address) ; 4 bits	CY	: Carry flag
RP	: General register pointer	CMP	: Compare flag
PC	: Program counter	s	: Stop release condition
SP	: Stack pointer	h	: Halt release condition
STACK	: Stack specified by (SP)	[ ]	: Address of M,R
i	: Immediate data ; 4 bits	( )	: Contents of M,R

Instruction	Mnemonic	Operand	Function	Operation	Machine Code			
					Op. Code	3-Bit	4-Bit	4-Bit
Add	ADD	r,m	Add memory to register	R← (R) + (M)	00000	m_H	m_L	r
		m, #i	Add immediate data to memory	M← (M) + i	10000	m_H	m_L	i
	ADDC	r,m	Add memory to register with carry	R← (R) + (M) + (CY)	00010	m_H	m_L	r
		m, #i	Add immediate data to memory with carry	R← (M) + i+ (CY)	10010	m_H	m_L	i
Subtraction	SUB	r,m	Subtract memory from register	R← (R) − (M)	00001	m_H	m_L	r
		m, #i	Subtract immediate data from memory	M← (M) − i	10001	m_H	m_L	i
	SUBC	r,m	Subtract memory from register with borrow	R← (R) − (M) − (CY)	00011	m_H	m_L	r
		m, #i	Subtract immediate data from memory with borrow	M← (M) − i − (CY)	10011	m_H	m_L	i
Compare	SKE	m, #i	Skip if memory equal to immediate data	M−i, skip if zero	01001	m_H	m_L	i
	SKGE	m, #i	Skip if memory greater than or equal to immediate data	M−i, skip if not borrow	11001	m_H	m_L	i
	SKLT	m, #i	Skip if memory less than immediate data	M−i, skip if borrow	11011	m_H	m_L	i
	SKNE	m, #i	Skip if memory not equal to immediate data	M−i, skip if not zero	01011	m_H	m_L	i
Logic operation	AND	m, #i	Logical AND of memory and immediate data	M← (M) AND i	10100	m_H	m_L	i
		r,m	Logical AND of register and memory	R← (R) AND (M)	00100	m_H	m_L	r
	OR	m, #i	Logical OR of memory and immediate data	M← (M) OR i	10110	m_H	m_L	i
		r,m	Logical OR of register and memory	R← (R) OR (M)	00110	m_H	m_L	r
	XOR	m, #i	Logical XOR of memory and immediate data	M← (M) XOR i	10101	m_H	m_L	i
		r,m	Logical XOR of register and memory	R← (R) XOR (M)	00101	m_H	m_L	r
Transfer	LD	r,m	Load memory of register	R← (M)	01000	m_H	m_L	r
	ST	m,r	Store register to memory	(M)←R	11000	m_H	m_L	r
	MOV	m, #i	Move immediate data to memory	M← i	11101	m_H	m_L	i
Judge	SKT	m, #n	Test memory bits, then skip if all bits specified are true	CMP ← 0 skip if M_n = all "1"	11110	m_H	m_L	n
	SKF	m, #n	Test memory bits, then skip if all bits specified are false	CMP ← 0 skip if M_n = all "0"	11111	m_H	m_L	n

Instruction	Mnemonic	Operand	Function	Operation	Machine Code			
					Op. Code	3-Bit	4-Bit	4-Bit
Branch	BR	addr	Jump to the address	PC←ADDR	01100	a_H	a_M	a_L
Shift	RORC	r	Rotate register right with carry	(CY)→(R)→CY	00111	000	0111	r
Subroutine	CALL	addr	Call subroutine	SP←(SP) − 1 STACK←((PC) + 1), PC←ADDR	11100	a_H	a_M	a_L
	RET		Return to main routine from subroutine	PC←(STACK), SP←(SP) + 1	00111	000	1110	0000
	RETSK		Return to main routine from subroutine, then skip unconditionary	PC←(STACK), SP←(SP) + 1 and skip	00111	001	1110	0000
Other	STOP	s	Stop clock	STOP	00111	010	1111	s
	HALT	h	Halt the CPU, restart by condition h	HALT	00111	011	1111	h
	NOP		No operation	No Operation	00111	100	1111	0000

13. ELECTRIC CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage	V_{DD}			−0.3 to +7.0	V
Supply Voltage	V_{PP}			−0.3 to +13.5	V
Input Voltage	V_I	P0C, P0D, $\overline{\text{RESET}}$		0.3 to V_{DD} +0.3	V
		P0B		−0.3 to +11	V
Output Voltage	V_O	P0C, P0D		0.3 to V_{DD} +0.3	V
		P0B		−0.3 to +11	V
High-level Output Amperage	I_{OH}	P0B, P0C, P0D per pin		−5	mA
		Total for all pins		−15	mA
Low-level Output Amperage	I_{OL}	P0B, P0C, P0D per pin		30	mA
		Total for all pins		100	mA
Operating Temperature	T_{opt}			−40 to +85	°C
Storage temperature	T_{stg}			−65 to +150	°C
Power Dissipation	P_d	T_a = 85 °C	16 pin DIP	400	mW
			16 pin SOP	190	mW

CAPACITY (T_a = 25 °C, V_{DD} = 0 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Input Capacity	C_{IN}			15	pF	f = 1 MHz, 0 V at other than measured pins
Input/Output Capacity	C_{IO}			15	pF	

DC CHARACTERISTICS (T_a = −40 to +85 °C, V_{DD} = 2.5 to 6.0 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION	
High-level Input Voltage	V_{IH1}	0.7 V_{DD}		V_{DD}	V	Other than specified below.	
	V_{IH2}	0.8 V_{DD}		V_{DD}	V	P0B, $\overline{RESET}$	
	V_{IH3}	0.8 V_{DD}		9	V	P0B*	
	V_{IH4}	V_{DD} - 0.5		V_{DD}	V	OSC_1	
Low-level Input Voltage	V_{IL1}	0		0.3 V_{DD}	V	Other than specified below.	
	V_{IL2}	0		0.2 V_{DD}	V	P0B, $\overline{RESET}$	
	V_{IL3}	0		0.5	V	OSC_1	
P0C, D High-level Output Voltage	V_{OH}	V_{DD} - 2.0			V	V_{DD} = 4.5 to 6.0 V I_{OH} = −2 mA	
		V_{DD} - 1.0			V	I_{OH} = −200 μA	
P0B, C, D Low-level Input Voltage	V_{OL}			2.0	V	V_{DD} = 4.5 to 6.0 V I_{OL} = 15 mA	
				0.5	V	I_{OL} = 600 μA	
P0B, C, D High-level Input Leak Current	I_{LIH1}			5	μA	V_{IN} = V_{DD}	
	I_{LIH2}			10	μA	V_{IN} = 9 V*	
P0B, C, D Low-level Input Leak Current	I_{LIL}			−5	μA	V_{IN} = 0 V	
P0B, C, D High-level Output Leak Current	I_{LOH1}			5	μA	V_{OUT} = V_{DD}	
	I_{LOH2}			10	μA	V_{OUT} = 9 V*	
P0B, C, D Low-level Output Leak Current	I_{LOL}			−5	μA	V_{OUT} = 0 V	
Supply Amperage	I_{DD1}		0.4	1.2	mA	Run mode	V_{DD} = 5 V ±10 % f_{CC} = 1.0 MHz ±20 %
			50	150	μA		V_{DD} = 3 V ±10 % f_{CC} = 250 kHz ±20 %
	I_{DD2}		0.3	0.9	mA	HALT mode	V_{DD} = 5 V ±10 % f_{CC} = 1.0 MHz ±20 %
			40	120	μA		V_{DD} = 3 V ±10 % f_{CC} = 250 kHz ±20 %
	I_{DD3}		0.1	10	μA	STOP mode	V_{DD} = 5 V ±10 %
			0.1	5	μA		V_{DD} = 3 V ±10 %

*: If N-ch open-drain input/output selected.

LOW-SUPPLY VOLTAGE DATA HOLDING CHARACTERISTICS IN DATA MEMORY STOP MODE (T_a = −40 to +85 °C)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Data Holding Supply Voltage	V_{DDDR}	2.0		6.0	V	
Data Holding Supply Amperage	I_{DDDR}		0.1	5.0	μA	V_{DDDR} = 2.0 V
Release Signal Set Time	t_{SREL}	0			μs	

AC CHARACTERISTICS (T_a = −40 to +85 °C, V_{DD} = 2.5 to 6.0 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Internal Clock Cycle Time	T_{CY}	6.6		160	μs	V_{DD} = 4.5 to 6.0 V
		26.6		160	μs	
$P0B_0$, $P0B_1$, High/Low Level Width	T_{PBH} T_{PBL}	10			μs	
$\overline{RESET}$, High/Low Level Width	T_{RSH} T_{RSL}	10			μs	

DC PROGRAMMING CHARACTERISTICS (T_a = 25 °C, V_{DD} = 6.0 ±0.25 V, V_{PP} = 12.5 ±0.5 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
High-Level Input Voltage	V_{IH1}	0.7 V_{DD}		V_{DD}	V	Other than OSC_1
	V_{IH2}	V_{DD} - 0.5		V_{DD}	V	OSC_1
Low-Level Input Voltage	V_{IL1}	0		0.3 V_{DD}	V	Other than OSC_1
	V_{IL2}	0		0.4	V	OSC_1
Input Leak Current	I_{LI}			10	μA	V_{IN} = V_{IL} or V_{IH}
High-Level Output Voltage	V_{OH}	V_{DD} - 1.0			V	I_{OH} = −1 mA
Low-Level Output Voltage	V_{OL}			0.4	V	I_{OL} = 1.6 mA
V_{DD} Supply Current	I_{DD}			30	mA	
V_{PP} Supply Current	I_{PP}			30	mA	MD0 = V_{IL}, MD1 = V_{IH}

NOTE 1: V_{PP} must not be a minimum of +13.5 V including overshoot.
2: Impress V_{DD} before V_{PP} and break it after V_{PP}.

AC PROGRAMMING CHARACTERISTICS (T_a = 25 °C, V_{DD} = 6.0 ±0.25 V, V_{PP} = 12.5 ±0.5 V)

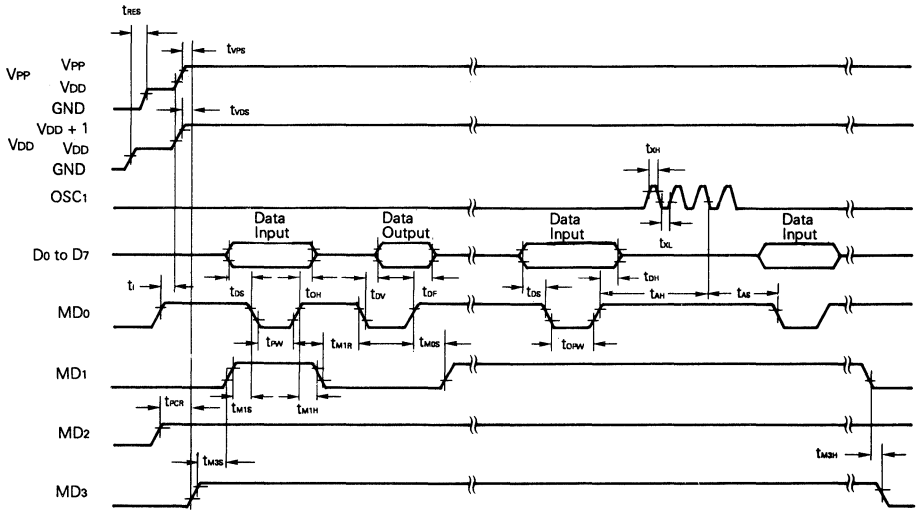
CHARACTERISTICS	SYMBOL	*1	MIN.	TYP.	MAX.	UNIT	CONDITION
Address Set-Up Time *2 (for MD0 ↓)	t_{AS}	t_{AS}	2			μs	
MD1 Set-Up Time (for MD0 ↓)	t_{M1S}	t_{OES}	2			μs	
Data Set-Up Time (for MD0 ↓)	t_{DS}	t_{DS}	2			μs	
Address Hold Time *2 (for MD0 ↑)	t_{AH}	t_{AH}	2			μs	
Data Hold Time (for MD0 ↑)	t_{DH}	t_{DH}	2			μs	
MD0 ↑ → Data Output Float Delay Time	t_{DF}	t_{DF}	0		130	ns	
V_{PP} Set-Up Time (for MD3 ↑)	t_{VPS}	t_{VPS}	2			μs	
V_{DD} Set-Up Time (for MD3 ↑)	t_{VDS}	t_{VCS}	2			μs	
Initial Program Pulse Width	t_{PW}	t_{PW}	0.95	1.0	1.05	ms	

CHARACTERISTICS	SYMBOL	*1	MIN.	TYP.	MAX.	UNIT	CONDITION
Additional Program Pulse Width	t_{OPW}	t_{OPW}	0.95		21.0	ms	
MD0 Set-Up Time (for MD1 ↑)	t_{MOS}	t_{CES}	2			μs	
MD0 ↓→ Data Output Delay Time	t_{DV}	t_{DV}			1	μs	MD0 = MD1 = V_{IL}
MD1 Hold Time (for MD0 ↑)	t_{M1H}	t_{OEH}	2			μs	$t_{M1H} + t_{M1R} \geq 50$ μs
MD1 Recover Time (for MD0 ↓)	t_{M1R}	t_{OR}	2			μs	
Program Counter Reset Time	t_{PCR}	-	10			μs	
OSC_1 Input High/Low Level Width	t_{XH}, t_{XL}	-	0.42			μs	
OSC_1 Input Frequency	f_{OSC}	-			1.2	MHz	
Initial Mode Set Time	t_I	-	2			μs	
MD3 Set-Up Time (for MD1 ↑)	t_{M3S}	-	2			μs	
MD3 Hold Time (for MD1 ↓)	t_{M3H}	-	2			μs	
MD3 Set-Up Time (for MD0 ↓)	t_{M3SR}	-	2			μs	At program memory read
Address *2 → Data Output Delay Time	t_{DAD}	t_{ACC}	2			μs	At program memory read
Address *2 → Data Output Hold Time	t_{HAD}	t_{OH}	0		130	ns	At program memory read
MD3 Hold Time (for MD0 ↑)	t_{M3HR}	-	2			μs	At program memory read
MD3 ↓→ Data Output Float Delay Time	t_{DFR}	-	2			μs	At program memory read
Reset Set-Up Time	t_{RES}		10			μs	

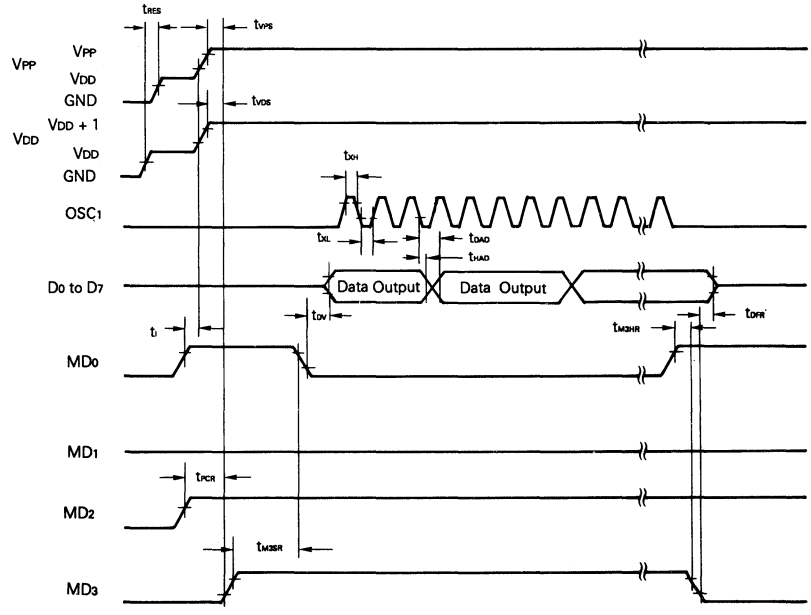
*1: A symbol of the corresponding μPD27C256.

*2: The internal address signal is incremented (+1) at the 3rd OSC_1 input falling and is not connected to a pin.

PROGRAM MEMORY WRITING TIMING



PROGRAM MEMORY READING TIMING



4-BIT SINGLE CHIP MICROCONTROLLER

The μPD17P108 is a tiny microcontroller consisting of a 1K-byte ROM, 16-word RAM, and 16 input/output ports. It is a one-time PROM version of the μPD17108, whose internal mask ROM is replaced with a one-time PROM.

Two μPD17P108 models are available: μPD17P108CS and μPD17P108GS, which allow a program to be written only once. They are suitable for evaluation of μPD17108 and for small-scale production.

The 17K architecture of the CPU uses general registers so that data memory can be manipulated directly for effective programming. Every instruction is 1 word long, consisting of 16 bits.

FEATURES

- Compatible with the μPD17108
- Program memory (one-time PROM) : 1K bytes (512 words x 16 bits)
- Data memory (RAM) : 16 words x 4 bits
- Input/output ports : 16 ports (including four N-ch open-drain outputs)
- Instruction execution time : 128 μs (62.5 kHz) to 8 μs (1 MHz)
- Number of instructions : 24 (Each instruction is 1 word long.)
- Stack level : 1
- A standby function is supported (with the STOP and HALT instructions).
- Data memory can retain data on low voltage (2.0 V at minimum).
- An oscillator is included for the system clock. (Only resistors are mounted externally.)
- Operating supply voltage : 2.5 to 6.0 V (at 250 kHz)
  4.5 to 6.0 V (at 1 MHz)

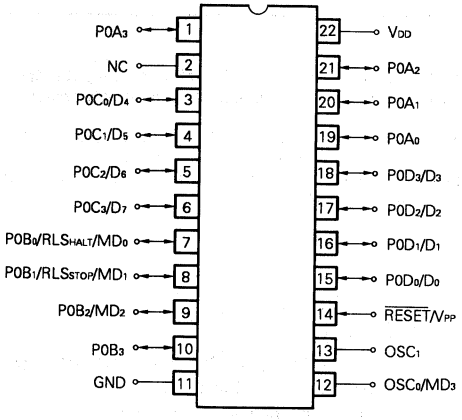
APPLICATIONS

- Controlling electric appliances or toys

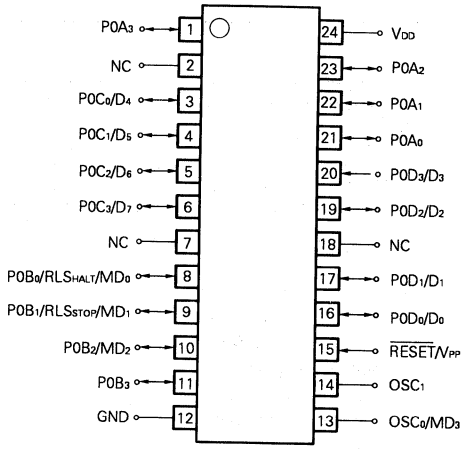
ORDERING INFORMATION

Order Code	Package
μPD17P108CS	22-pin plastic shrink DIP (300 mil)
μPD17P108GS	24-pin plastic SOP (300 mil)

PIN CONFIGURATION (Top View)

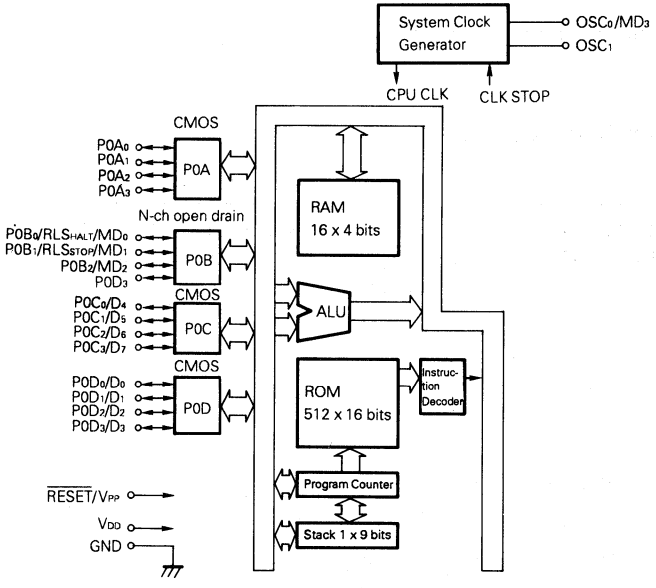


22-pin plastic shrink DIP



24-pin plastic SOP

BLOCK DIAGRAM



PIN FUNCTIONS

Pin Functions

- Port pins

Pin name	Input/ output	Dual function pin		Function		When writing to program memory or verifying its contents	When reset
$P0A_0$	Input/ output			CMOS (push-pull) 4-bit input/output port (port 0A)		Pull down	High impedance (input mode)
$P0A_1$							
$P0A_2$							
$P0A_3$							
$P0B_0$	Input/ output	RLS_{HALT}	MD_0	N-ch open-drain 4-bit input/output port (port 0B)	For the HALT mode releasing	Mode selection pin	High impedance (input mode)
$P0B_1$		RLS_{STOP}	MD_1		For the STOP mode releasing		
$P0B_2$		MD_2					
$P0B_3$						Pull down	
$P0C_0$	Input/ output	D_4		CMOS (push-pull) 4-bit input/output port (port 0C)		8-bit data input/ output pin (high-order 4 bits)	High impedance (input mode)
$P0C_1$		D_5					
$P0C_2$		D_6					
$P0C_3$		D_7					
$P0D_0$	Input/ output	D_0		CMOS (push-pull) 4-bit input/output port (port 0D)		8-bit data input/ output pin (low-order 4 bits)	High impedance (input mode)
$P0D_1$		D_1					
$P0D_2$		D_2					
$P0D_3$		D_3					

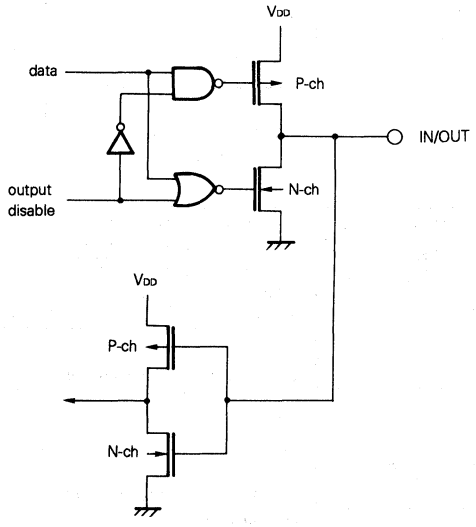
- Non-port pins

Pin name	Input/ output	Dual Function pin	Function	When writing to program memory or verifying its contents
$\overline{RESET}$	Input	V_{PP}	System reset input pin	Voltage is applied to this pin (+12.5 V)
V_{DD}			Positive power supply pin	Positive power supply pin (+6.0 V)
GND			GND pin	GND pin
OSC_1			Pins to be connected to the system clock resonator	Program memory address update
OSC_0		MD_3	Pins to be connected to the system clock resonator	
NC			NC pin is not connected internally.	Mode selection pin

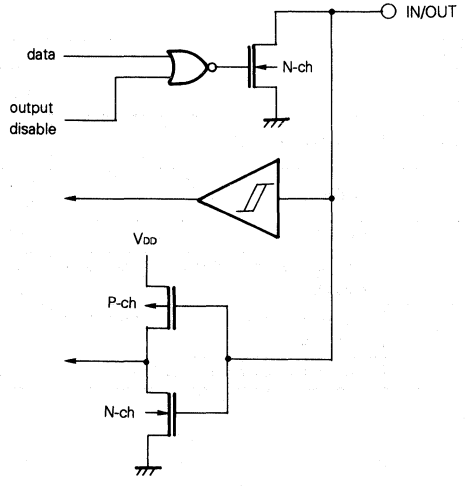
PIN INPUT/OUTPUT CIRCUITS

Following are schematics of the input/ouput circuits of the pins of the μPD17P108.

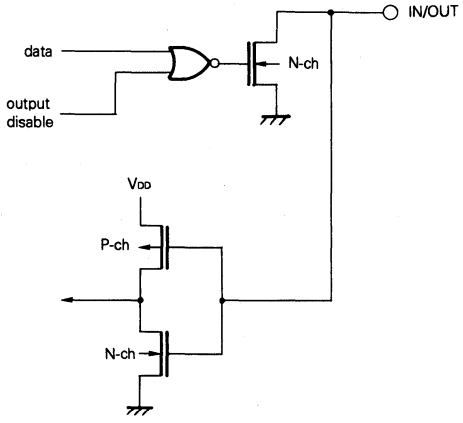
(1) P0A, P0C, and P0D



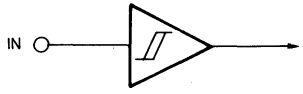
(2) P0B0 and P0B1



(3) POB_2 and POB_3



(4) $\overline{RESET}$



10. WRITING TO AND VERIFYING ONE-TIME PROM (PROGRAM MEMORY)

The μPD17P108's internal program memory consists of a 512 x 16 bit one-time PROM.

Writing to the one-time PROM or verifying the contents of the PROM is accomplished using the pins shown in the table below. Note that address inputs are not used; instead, the address is updated using the clock input from the OSC_1 pin.

Pin name	Function
V_{PP}	Voltage is applied to this pin when writing to program memory or verifying its contents.
OSC_1	Input pin for address update clock used when writing to program memory or verifying its contents
MD_0 to MD_3	Pins that turn to input pins and are used as operation mode selection pins when writing to program memory or verifying its contents
D_0 to D_7	Input/output pins for 8-bit data used when writing to program memory or verifying its contents

10.1 PROGRAM MEMORY WRITE/VERIFY MODES

If +6 V is applied to the V_{DD} pin and +12.5 V is applied to the V_{PP} pin after a certain duration of reset status (V_{DD} = 5 V, $\overline{RESET}$ = 0 V), the μPD17P108 enters program memory write/verify mode. A specific operating mode is then selected by setting the MD_0 through MD_3 pins as follows. Set the other unused pins to GND level by means of pull-down resistors.

Operating mode specification						Operating mode
V_{PP}	V_{DD}	MD_0	MD_1	MD_2	MD_3	
+12.5 V	+6 V	H	L	H	L	Program memory address clear mode
		L	H	H	H	Write mode
		L	L	H	H	Verify mode
		H	x	H	H	Program inhibit mode

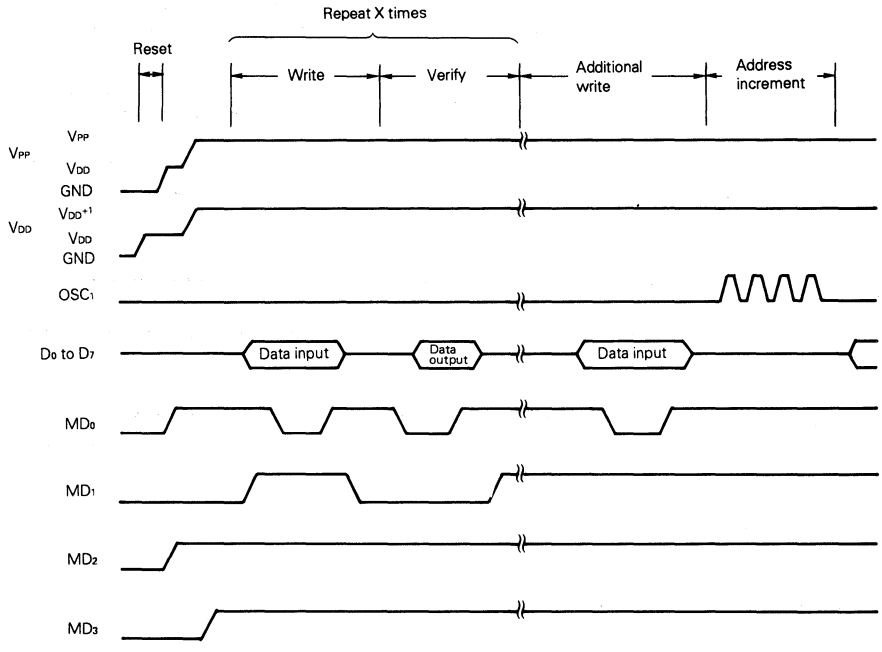
x : L (low) or H (high)

10.2 WRITING TO PROGRAM MEMORY

The procedure for writing to program memory is described below; high-speed write is possible.

(1) Pull low the levels on all unused pins to GND by means of resistors. Bring OSC_1 to low level.
(2) Apply 5 V to V_{DD} and bring V_{PP} to low level.
(3) Wait 10 μs. Then apply 5 V to V_{PP}
(4) Set the mode selection pins to program memory address clear mode.
(5) Apply 6 V to V_{DD} and 12.5 V to V_{PP}.
(6) Select program inhibit mode.
(7) Write data in 1 ms write mode.
(8) Select program inhibit mode.
(9) Select verify mode. If the write operation is found successful, proceed to step (10). If the operation is found unsuccessful, repeat steps (7) to (9).
(10) Perform additional write for (number of repetitions of steps (7) to (9) x 1 ms.
(11) Select program inhibit mode.
(12) Increment the program memory address by one on reception of four pulses on the OSC_1 pin.
(13) Repeat steps (7) to (12) until the last address is reached.
(14) Select program memory address clear mode.
(15) Apply 5 V to the V_{DD} and V_{PP} pins.
(16) Turn power off.

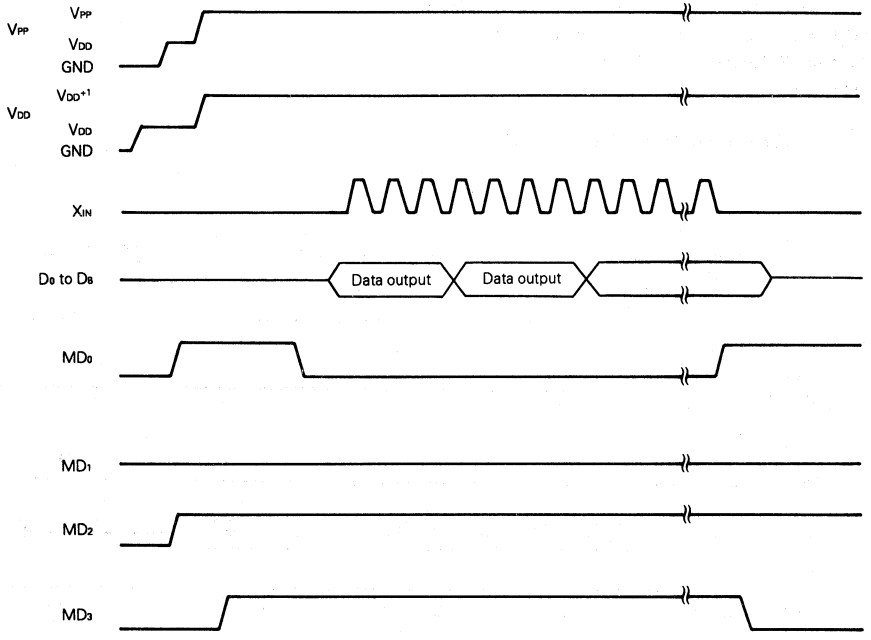
The timing for steps (2) to (12) is shown below.



10.3 READING PROGRAM MEMORY

(1) Pull low the levels of all unused pins to GND by means of resistors. Bring OSC_1 to low level.
(2) Apply 5 V to V_{DD} and bring V_{PP} to low level.
(3) Wait 10 μs. Then apply 5 V to V_{PP}
(4) Set the mode selection pins to program memory address clear mode.
(5) Apply 6 V to V_{DD} and 12.5 V to V_{PP}
(6) Select program inhibit mode.
(7) Select verify mode. Data is output sequentially one address at a time for each cycle of four clock pulses on the OSC_1 pin.
(8) Select program inhibit mode.
(9) Select program memory address clear mode.
(10) Apply 5 V to the V_{DD} and V_{PP} pins.
(11) Turn power off.

The timing for steps (2) to (9) is shown below.



11. ASSEMBLER RESERVED WORDS

Table 11-1 lists the reserved words defined in the μPD17P108 device file (AS17108).

Table 11-1 Reserved Words

Name	Attribute	Value	Read/write	Description
P0A0	FLG	0.70H.0	Read/write	Bit 0 of port 0A
P0A1	FLG	0.70H.1	Read/write	Bit 1 of port 0A
P0A2	FLG	0.70H.2	Read/write	Bit 2 of port 0A
P0A3	FLG	0.70H.3	Read/write	Bit 3 of port 0A
P0B0	FLG	0.71H.0	Read/write	Bit 0 of port 0B
P0B1	FLG	0.71H.1	Read/write	Bit 1 of port 0B
P0B2	FLG	0.71H.2	Read/write	Bit 2 of port 0B
P0B3	FLG	0.71H.3	Read/write	Bit 3 of port 0B
P0C0	FLG	0.72H.0	Read/write	Bit 0 of port 0C
P0C1	FLG	0.72H.1	Read/write	Bit 1 of port 0C
P0C2	FLG	0.72H.2	Read/write	Bit 2 of port 0C
P0C3	FLG	0.72H.3	Read/write	Bit 3 of port 0C
P0D0	FLG	0.73H.0	Read/write	Bit 0 of port 0D
P0D1	FLG	0.73H.1	Read/write	Bit 1 of port 0D
P0D2	FLG	0.73H.2	Read/write	Bit 2 of port 0D
P0D3	FLG	0.73H.3	Read/write	Bit 3 of port 0D
BCD	FLG	0.7EH.0	Read/write	BCD arithmetic flag
PSW	MEM	0.7FH	Read/write	Program status word
Z	FLG	0.7FH.1	Read/write	Zero flag
CY	FLG	0.7FH.2	Read/write	Carry flag
CMP	FLG	0.7FH.3	Read/write	Compare flag

12. INSTRUCTION SET

12.1 INSTRUCTION SET LIST

$b_{14}-b_{11}$ \ b_{15}		0		1	
BIN	HEX				
0 0 0 0	0	ADD	r, m	ADD	m, #i
0 0 0 1	1	SUB	r, m	SUB	m, #i
0 0 1 0	2	ADDC	r, m	ADDC	m, #i
0 0 1 1	3	SUBC	r, m	SUBC	m, #i
0 1 0 0	4	AND	r, m	AND	m, #i
0 1 0 1	5	XOR	r, m	XOR	m, #i
0 1 1 0	6	OR	r, m	OR	m, #i
0 1 1 1	7	RET RETSK RORC STOP HALT NOP	 r s h 		
1 0 0 0	8	LD	r, m	ST	m, r
1 0 0 1	9	SKE	m, #i	SKGE	m, #i
1 0 1 0	A				
1 0 1 1	B	SKNE	m, #i	SKLT	m, #i
1 1 0 0	C	BR	addr	CALL	addr
1 1 0 1	D			MOV	m, #i
1 1 1 0	E			SKT	m, #n
1 1 1 1	F			SKF	m, #n

12.2 INSTRUCTIONS

Legend:

M	: One of data memory	n	: Bit position : 4 bits
m	: Data memory address specified by [m_H, m_L] of each bank	addr	: One of program memory address ; 11 bits
m_H	: Data memory address high (row address) ; 3 bits	a_H	: Program memory address high ; 3 bits
m_L	: Data memory address low (column address) ; 4 bits	a_M	: Program memory address middle ; 4 bits
R	: One of general register specified by [(RP), r]	a_L	: Program memory address low ; 4 bits
r	: General register address low (column address) ; 4 bits	CY	: Carry flag
RP	: General register pointer	CMP	: Compare flag
PC	: Program counter	s	: Stop release condition
SP	: Stack pointer	h	: Halt release condition
STACK	: Stack specified by (SP)	[ ]	: Address of M, R
i	: Immediate data ; 4 bits	( )	: Contents of M, R

Type	Mnemonic	Operand	Function	Operation	Machine code			
					Op code	3 bits	4 bits	4 bits
Add	ADD	r, m	Add memory to register	R← (R) + (M)	00000	m_H	m_L	r
		m, #i	Add immediate data to memory	M← (M) + i	10000	m_H	m_L	i
	ADDC	r, m	Add memory to register with carry	R← (R) + (M) + (CY)	00010	m_H	m_L	r
		m, #i	Add immediate data to memory with carry	R← (M) + i + (CY)	10010	m_H	m_L	i
Subtract	SUB	r, m	Subtract memory from register	R← (R) − (M)	00001	m_H	m_L	r
		m, #i	Subtract immediate data from memory	M← (M) − i	10001	m_H	m_L	i
	SUBC	r, m	Subtract memory from register with borrow	R← (R) − (M) − (CY)	00011	m_H	m_L	r
		m, #i	Subtract immediate data from memory with borrow	M← (M) − i − (CY)	10011	m_H	m_L	i
Compare	SKE	m, #i	Skip if memory equal to immediate data	M−i, skip if zero	01001	m_H	m_L	i
	SKGE	m, #i	Skip if memory greater than or equal to immediate data	M−i, skip if not borrow	11001	m_H	m_L	i
	SKLT	m, #i	Skip if memory less than immediate data	M−i, skip if borrow	11011	m_H	m_L	i
	SKNE	m, #i	Skip if memory not equal to immediate data	M−i, skip if not zero	01011	m_H	m_L	i
Logical operation	AND	m, #i	Logical AND of memory and immediate data	M← (M) AND i	10100	m_H	m_L	i
		r, m	Logical AND of register and memory	R← (R) AND (M)	00100	m_H	m_L	r
	OR	m, #i	Logical OR of memory and immediate data	M← (M) OR i	10110	m_H	m_L	i
		r, m	Logical OR of register and memory	R← (R) OR (M)	00110	m_H	m_L	r
	XOR	m, #i	Logical XOR of memory and immediate data	M← (M) XOR i	10101	m_H	m_L	i
		r, m	Logical XOR of register and memory	R← (R) XOR (M)	00101	m_H	m_L	r
Transfer	LD	r, m	Load memory of register	R← (M)	01000	m_H	m_L	r
	ST	m, r	Store register to memory	(M)←R	11000	m_H	m_L	r
	MOV	m, #i	Move immediate data to memory	M← i	11101	m_H	m_L	i
Test	SKT	m, #n	Test memory bits, then skip if all bits specified are true	CMP ← 0 skip if M_n = all "1"	11110	m_H	m_L	n
	SKF	m, #n	Test memory bits, then skip if all bits specified are false	CMP ← 0 skip if M_n = all "0"	11111	m_H	m_L	n

Type	Mne-monie	Operahd	Function	Operation	Machine code			
					Op code	3 bits	4 bits	4 bits
Branch	BR	addr	Jump to the address	PC←ADDR	01100	a_H	a_M	a_L
Shift	RORC	r	Rotate register right with carry	(CY)→(R)→CY	00111	000	0111	r
Subroutine	CALL	addr	Call subroutine	SP←(SP)−1 STACK←((PC)+1), PC←ADDR	11100	a_H	a_M	a_L
	RET		Return to main routine from subroutine	PC←(STACK), SP←(SP)+1	00111	000	1110	0000
	RETSK		Return to main routine from subroutine, then skip unconditionary	PC←(STACK), SP←(SP)+1 and skip	00111	001	1110	0000
Miscell-aneous	STOP	s	Stop clock	STOP	00111	010	1111	s
	HALT	h	Halt the CPU, restart by condition h	HALT	00111	011	1111	h
	NOP		No operation	No Operation	00111	100	1111	0000

13. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage	V_{DD}			−0.3 to +7.0	V
Supply Voltage	V_{PP}			−0.3 to +13.5	V
Input Voltage	V_I	P0A, P0C, P0D		−0.3 to V_{DD}+0.3	V
		P0B		−0.3 to +11	V
Output Voltage	V_O	P0A, P0C, P0D		−0.3 to V_{DD}+0.3	V
		P0B		−0.3 to +11	V
High-Level output Current	I_{OH}	Each of P0A, P0B, P0C, P0D		−5	mA
		Total of all pins		−15	mA
Low-Level output Current	I_{OL}	Each of P0A, P0B, P0C, P0D		30	mA
		Total of all pins		100	mA
Operating Temperature	T_{opt}			−40 to +85	°C
Storage Temperature	T_{stg}			−65 to +150	°C
Power Consumption	P_d	T_a = 85 °C	22-pin shrink DIP	400	mW
			24-pin SOP	250	mW

CAPACITY (T_a = 25 °C, V_{DD} = 0 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Input Capacitance	C_{IN}			15	pF	f = 1 MHz
Input/Output Capacitance	C_{IO}			15	pF	0 V for pins other than pins to be measured

DC CHARACTERISTICS (T_a = –40 to +85 °C, V_{DD} = 2.5 to 6.0 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION	
High-Level Input Voltage	V_{IH1}	0.7 V_{DD}		V_{DD}	V	Other than the following pins and port	
	V_{IH2}	0.8 V_{DD}		V_{DD}	V	P0B and $\overline{RESET}$	
	V_{IH3}	0.8 V_{DD}		9	V	P0B (*)	
	V_{IH4}	V_{DD} – 0.5		V_{DD}	V	OSC_1	
Low-Level Input Voltage	V_{IL1}	0		0.3 V_{DD}	V	Other than the following pins and port	
	V_{IL2}	0		0.2 V_{DD}	V	P0B and $\overline{RESET}$	
	V_{IL3}	0		0.5	V	OSC_1	
High-Level Output Voltage on P0A, P0C, and P0D	V_{OH}	V_{DD} – 2.0			V	V_{DD} = 4.5 to 6.0 V, I_{OH} = –2 mA	
		V_{DD} – 1.0			V	I_{OH} = –200 μA	
Low-Level Output Voltage on P0A, P0B, P0C, and P0D	V_{OL}			2.0	V	V_{DD} = 4.5 to 6.0 V, I_{OL} = 15 mA	
				0.5	V	I_{OL} = 600 μA	
High-Level Input Leakage Current on P0A to P0D	I_{LIH1}			5	μA	V_{IN} = V_{DD}	
	I_{LIH2}			10	μA	V_{IN} = 9 V (*)	
Low-Level Input Leakage Current on P0A to P0D	I_{LIL}			–5	μA	V_{IN} = 0 V	
High-Level Output Leakage Current on P0A to P0D	I_{LOH1}			5	μA	V_{OUT} = V_{DD}	
	I_{LOH2}			10	μA	V_{OUT} = 9 V (*)	
Low-Level Output Leakage Current on P0A to P0D	I_{LOL}			–5	μA	V_{OUT} = 0 V	
Power Supply Current	I_{DD1}		0.4	1.2	mA	Operation mode	V_{DD} = 5 V ±10%, f_{CC} = 1.0 MHz ±20%
			50	150	μA		V_{DD} = 3 V ±10% f_{CC} = 250 kHz ±20%
	I_{DD2}		0.3	0.9	mA	HALT mode	V_{DD} = 5 V ±10%, f_{CC} = 1.0 MHz ±20%
			40	120	μA		V_{DD} = 3 V ±10% f_{CC} = 250 kHz ±20%
	I_{DD3}		0.1	10	μA	STOP mode	V_{DD} = 5 V ±10%
			0.1	5	μA		V_{DD} = 3 V ±10%

* When N-ch open-drain input/output is selected

CHARACTERISTICS OF DATA MEMORY FOR HOLDING DATA ON LOW SUPPLY VOLTAGE IN THE STOP MODE (T_a = −40 to +85 °C)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Data Hold Supply Voltage	V_{DDDR}	2.0		6.0	V	
Data Hold Supply Current	I_{DDDR}		0.1	5.0	μA	V_{DDDR} = 2.0 V
Release Signal Set Time	t_{SREL}	0			μs	

AC CHARACTERISTICS (T_a = -40 to +85 °C, V_{DD} = 2.5 to 6.0 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Internal Clock Cycle Time	T_{CY}	6.6		160	μs	V_{DD} = 4.5 to 6.0 V
		26.6		160	μs	
High/Low Level Width on $P0B_0$ and $P0B_1$	T_{PBH} T_{PBL}	10			μs	
High/Low Level Width on $\overline{RESET}$	T_{RSH} T_{RSL}	10			μs	

DC PROGRAMMING CHARACTERISTICS (T_a = 25 °C, V_{DD} = 6.0 ±0.25 V, V_{PP} = 12.5 ±0.5 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Input Voltage High	V_{IH1}	0.7 V_{DD}		V_{DD}	V	Except OSC_1
	V_{IH2}	V_{DD} −0.5		V_{DD}	V	OSC_1
Input Voltage Low	V_{IL1}	0		0.3 V_{DD}	V	Except OSC_1
	V_{IL2}	0		0.4	V	OSC_1
Input Leakage Current	I_{LI}			10	μA	V_{IN} = V_{IL} or V_{IH}
Output Voltage High	V_{OH}	V_{DD} −1.0			V	I_{OH} = −1 mA
Output Voltage Low	V_{OL}			0.4	V	I_{OL} = 1.6 mA
V_{DD} Power Supply Current	I_{DD}			30	mA	
V_{PP} Power Supply Current	I_{PP}			30	mA	MD0 = V_{IL}, MD1 = V_{IH}

Notes 1. V_{PP} must be under +13.5 V including overshoot.
2. V_{DD} must be applied before V_{PP} on and must be off after V_{PP} off.

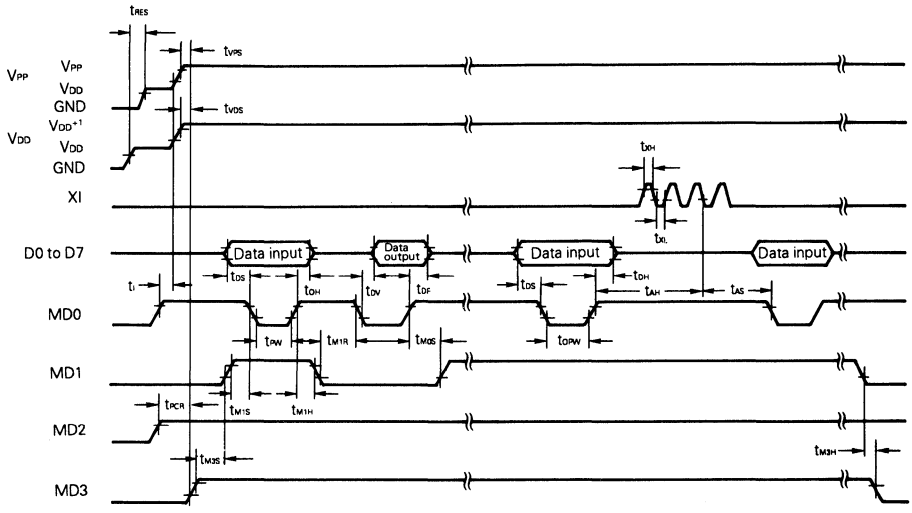
AC PROGRAMMING CHARACTERISTICS (T_a = 25 °C, V_{DD} = 6.0 ±0.25 V, V_{PP} = 12.5 ±0.5 V)

CHARACTERISTICS	SYMBOL	(*1)	MIN.	TYP.	MAX.	UNIT	CONDITION
Address Set Up Time to MD0↓ (*2)	t_{AS}	t_{AS}	2			μs	
MD1 Setup Time to MD0↓	t_{M1S}	t_{OES}	2			μs	
Data Setup Time to MD0↓	t_{DS}	t_{DS}	2			μs	
Address Hold Time to MD0↑ (*2)	t_{AH}	t_{AH}	2			μs	
Data Hold Time to MD0↑	t_{DH}	t_{DH}	2			μs	
Data Output Float Delay Time from MD0↑→	t_{DF}	t_{DF}	0		130	ns	
V_{PP} Setup Time to MD3↑	t_{VPS}	t_{VPS}	2			μs	
V_{DD} Setup Time to MD3↑	t_{VDS}	t_{VCS}	2			μs	
Initial Program Pulse Width	t_{PW}	t_{PW}	0.95	1.0	1.05	ms	
Additional Program Pulse Width	t_{OPW}	t_{OPW}	0.95		21.0	ms	
MD0 Setup Time to MD1↑	t_{MOS}	t_{CES}	2			μs	
Data Output Delay Time from MD0↓→	t_{DV}	t_{DV}			1	μs	
MD1 Hold Time to MD0↑	t_{M1H}	t_{OEH}	2			μs	MD0 = MD1 = V_{IL}
MD1 Recovery Time to MD0↓	t_{M1R}	t_{OR}	2			μs	
Program Counter Reset Time	t_{PCR}	–	10			μs	$t_{M1H} = t_{M1R} \geqq 50$ μs
OSC_1 Input High, Low Level Range	t_{XH}, t_{XL}	–	0.42			μs	
OSC_1 Input Frequency	f_{OSC}				1.2	MHz	
Initial Mode Set Time	t_I	–	2			μs	
MD3 Setup Time to MD1↑	t_{M3S}	–	2			μs	
MD3 Hold Time to MD1↓	t_{M3H}	–	2			μs	
MD3 Setup Time to MD0↓	t_{M3SR}	–	2			μs	Read program memory
Data Output Delay Time From Address (*2)	t_{DAD}	–	2			μs	Read program memory
Data Output Hold Time From Address (*2)	t_{HAD}	t_{ACC}	0		130	ns	Read program memory
MD3 Hold Time to MD0↑	t_{M3HR}	t_{OH}	2			μs	Read program memory
Data Output float Delay Time From MD3↓→	t_{DFR}	–	2			μs	Read program memory
Reset Setup Time	t_{RES}	–	10			μs	

*1 Symbols for corresponding μPD27C256.

*2 Internal address signal is incremented by one at the falling edge of the third OSC_1 input, and it is not connected to the pin.

Write program memory timing



The μPD17134A and μPD17136A are 4-bit single-chip microcontrollers containing four channels of 8-bit A/D converters, two channels of 8-bit timers, an AC zerocross detector, a power-on reset circuit, and a serial interface in one chip.

For the CPU, the 17K architecture is used. This enables accumulator direct data memory manipulation, facilitating effective programming. Every instruction is one word long, consisting of 16 bits.

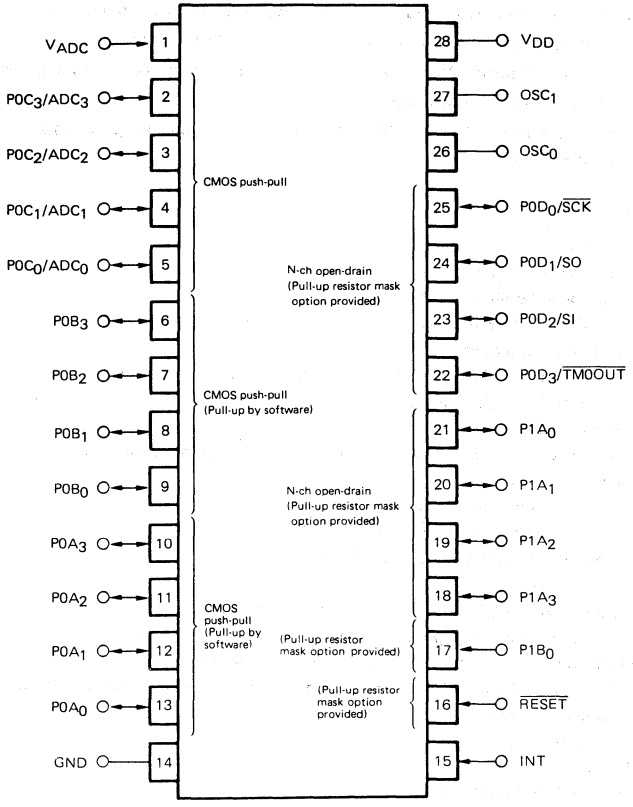
Since the μPD17134A and μPD17136A have the on-chip A/D converters and AC zerocross detector, they can provide economical electronic control in appliances.

For the evaluation of the μPD 17134A and μPD17136A or small production, the μPD17P136A, in which a program can be written once, is provided.

FEATURES

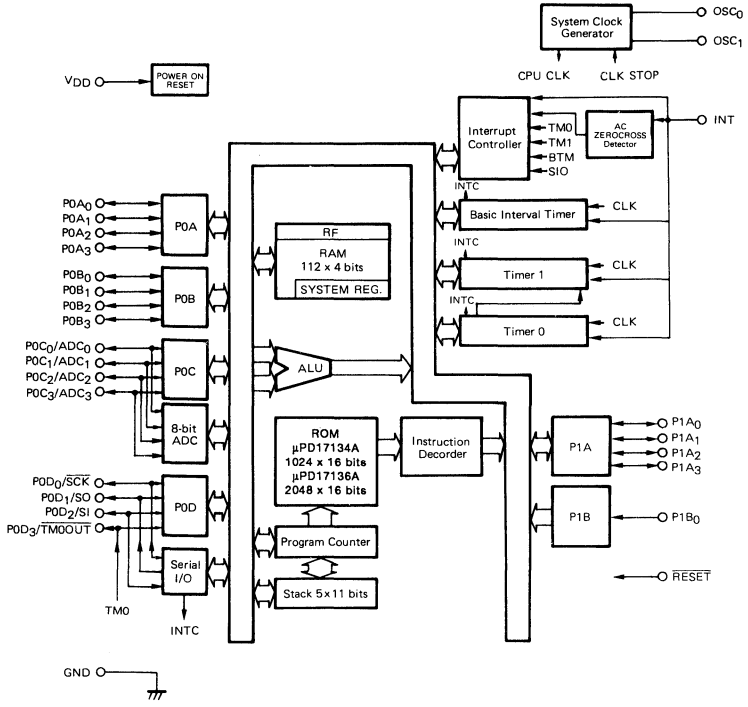
- Program memory (ROM)
  μPD17134A: 2 K bytes (1024 x 16 bits)
  μPD17136A: 4 K bytes (2048 x 16 bits)
- Data memory (RAM): 112 words (112 x 4 bits)
- 35 easy-to-understand instructions
- Instruction execution time: 8 μs (at 2 MHz) with Resistance, when V_{DD} = 5 V
- Stack level: 5 levels (interrupt: 3 levels)
- Vectored interrupt function:
  5 interrupt sources (INT pin, timer 1, timer 0, basic interval timer, and serial interface)
- 8-bit A/D converter: 4 channels
  Absolute accuracy
  ±1.5 LSB or higher (on 5 V ±10 %)
- AC zerocross detector: 1 input (also used as INT pin)
- 8-bit timer: 2 channels
  Timer 0 count clock (f_{OSC}/16, f_{OSC}/64, f_{OSC}/256, INT pin input)
  Timer 1 count clock (f_{OSC}/256, f_{OSC}/512, f_{OSC}/2048, incrementing timer 0)
- 8-bit basic interval timer: 1 channel. Can be used as watchdog timer
  Basic interval timer count clock (INT pin input, incrementing timer 0, f_{OSC}/4096, f_{OSC}/8192)
- 3-wire serial interface: 1 channel
- On-chip power-on reset circuit
- I/O pin: 21 pins
- Standby function (HALT/STOP) provided
- Operating temperature: −40 to +85°C
- Operating voltage: 2.7 to 6.0 V
- CMOS low power consumption

PIN CONNECTION FOR THE μPD17134A AND μPD17136A (Top View)



28-pin shrink DIP
28-pin SOP

BLOCK DIAGRAM OF THE μPD17134A AND μPD17136A



MICROCONTROLLER FAMILY FOR SMALL WHITE GOODS APPLIANCES

Item	μPD17134A	μPD17136A	μPD17135A	μPD17137A	Remarks
ROM size	1024 x 16 bits	2048 x 16 bits	1024 x 16 bits	2048 x 16 bits	
RAM size	112 x 4 bits	112 x 4 bits	112 x 4 bits	112 x 4 bits	
Number of I/O port lines	21 lines				Including 8 N-ch open-drain lines
Analog input	4 channels				Also used as port pins
Timer	3 timers				
Serial interface	1 channel				Also used as port pin
Stack	5 levels				
Power-on reset	Provided				
System clock	RC source		Ceramic/crystal source		
Standby function	Provided				STOP/HALT
Power supply	2.7 to 6.0 V				5 V ±10 % for A/D
Package	28-pin shrink DIP 28-pin SOP				
PROM version	μPD17P136A		μPD17P137A		

4-BIT SINGLE-CHIP MICROCONTROLLER

The μPD17P136A has been developed by replacing the on-chip ROM of μPD17136A, which is a mask ROM, with a one-time PROM, which is writable only once. It is convenient for evaluating or producing in small quantities the μPD17134A, μPD17136A.

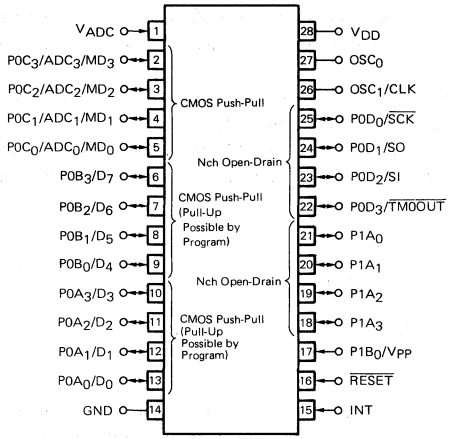
The μPD17P136A is a 4-bit single-chip microcontroller with on-chip 8-bit A/D converter (4-channel), 8-bit timer (2-channel), AC zero cross detector, power on resetter and serial interface.

Very efficient programming is possible through the use of the 17K architecture, which allows the accumulator direct data memory to be operated, being adopted in the CPU. Every instruction is composed of 1 word of 16-bit lenght.

FEATURES

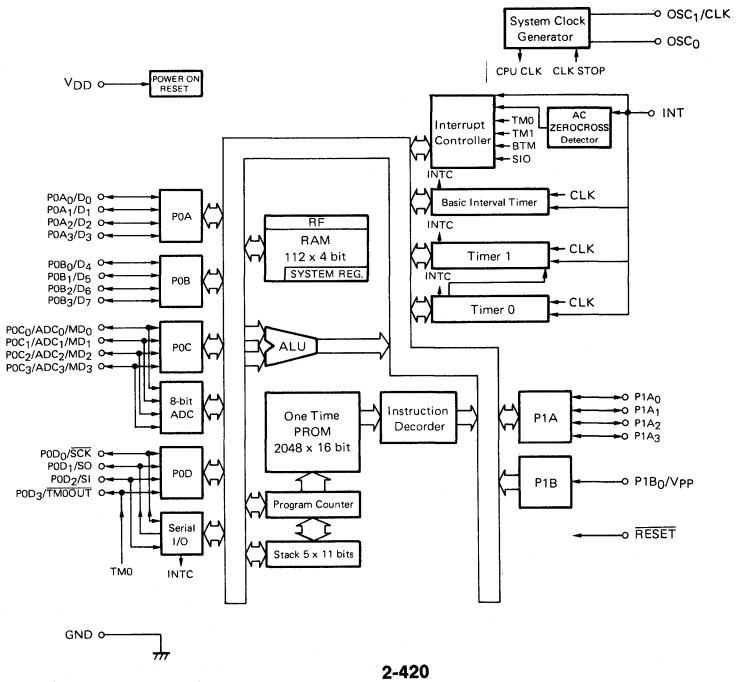
- Program memory (OTP): 4K bytes (2048 x 16 bits)
- Data memory (RAM): 112 words (112 x 4 bits)
- Instruction execution time: 8 μs (2 MHz) R resonator, if V_{DD} = 5 V used
- Stack level: 5 levels (interrupt: 3 levels)
- Vectored interrupt function:
  5 types of causes of interrupt (INT pin, timer 1, timer 0, basic interval timer, and serial interface)
- 8-bit A/D converter: 4 channels, absolute precision ± 1.5 LSB max. (5 V ±10 %)
- AC zero cross detector: 1 input (dual function with INT pin)
- 8-bit timer: 2 channels
- 8-bit basic interval timer: 1 channel, available as watchdog timer
- 3-wire serial interface: 1 channel
- On-chip power on resetter
- Input/output pin: 21 pins
- Standby function available (HALT/STOP)
- Operating supply voltage: 2.7 to 5.5 V

μPD17P136A PIN CONFIGURATION (Top View)



28-pin plastic shrink DIP
28-pin plastic SOP

μPD17P136A BLOCK DIAGRAM



MICROCONTROLLER FAMILY FOR SMALL WHITE GOOD'S APPLIANCES

Item	μPD17134A	μPD17136A	μPD17135A	μPD17137A	Remarks
ROM capacity	1024 x 16 bits	2048 x 16 bits	1024 x 16 bits	2048 x 16 bits	
RAM capacity	112 x 4 bits	112 x 4 bits	112 x 4 bits	112 x 4 bits	
Number of input/ output ports	21 pins				Including 8 Nch open-drain input/output ports
Analog input	4 channels				Dual function with port pin
Timer	3 systems				
Serial interface	1 channel				Dual function with port pin
Stack	5 levels				
Power on reset	Available				
System clock	RC resonator		Ceramic/crystal resonator		
Standby function	Available				STOP/HALT
Input power	2.7 to 5.5 V				5 V ±10 % if A/D used
Package	28-pin shrink DIP 28-pin SOP				
PROM product	μPD17P136A		μPD17P137A		

4-BIT SINGLE-CHIP MICROCONTROLLER

The μPD17135A and μPD17137A are 4-bit single-chip microcontrollers containing four channels of 8-bit A/D converters, two channels of 8-bit timers, an AC zerocross detector, a power-on reset circuit, and a serial interface in one chip.

For the CPU, the 17K architecture is used. This enables accumulator direct data memory manipulation, facilitating effective programming. Every instruction is one word long, consisting of 16 bits.

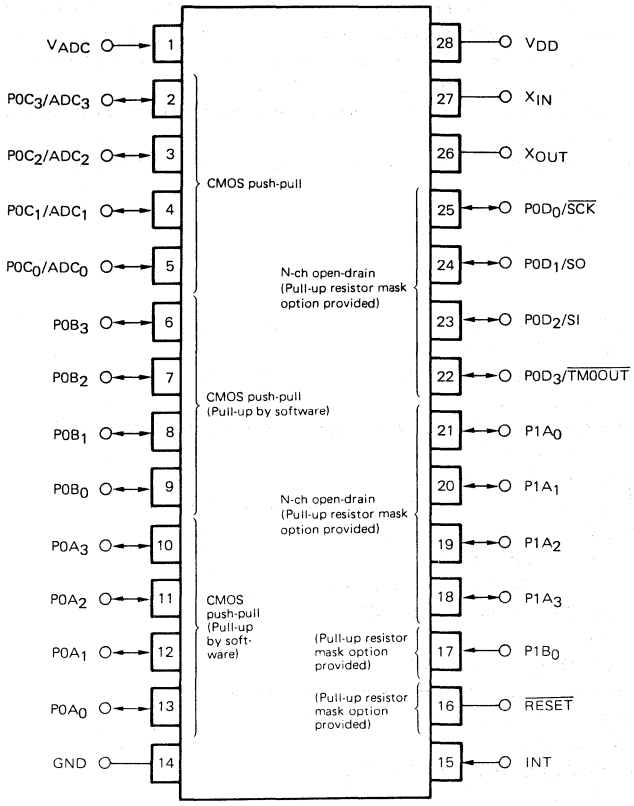
Since the μPD17135A and μPD17137A have the on-chip A/D converters and AC zerocross detector, they can provide economical electronic control in appliances.

For the evaluation of the μPD17135A and μPD17137A or small production, the μPD17P137A, in which a program can be written once, is provided.

FEATURES

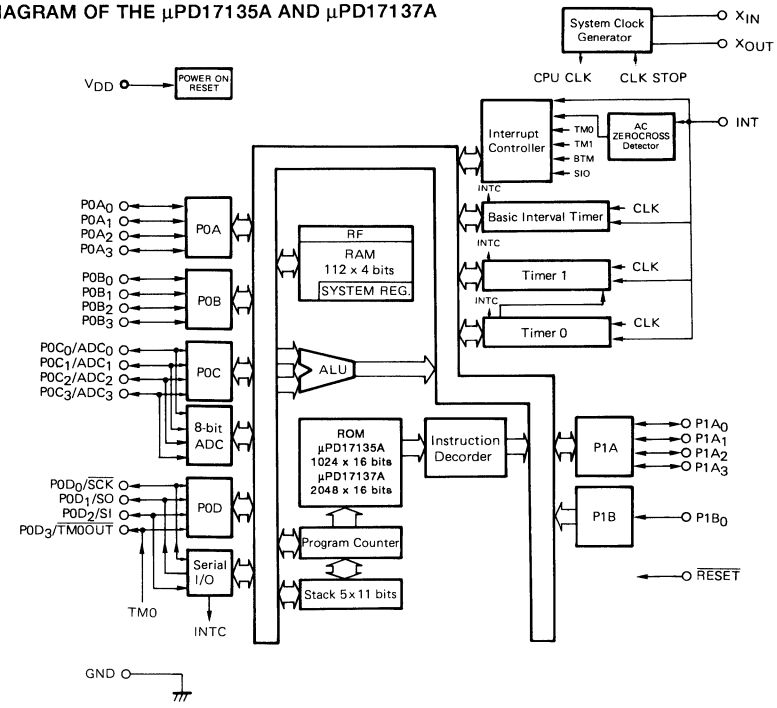
- Program memory (ROM)
  μPD17135A: 2 K bytes (1024 x 16 bits)
  μPD17137A: 4 K bytes (2048 x 16 bits)
- Data memory (RAM): 112 words (112 x 4 bits)
- 35 easy-to-understand instructions
- Instruction execution time: 2 μs (at 8 MHz) with ceramic/crystal source when V_{DD} = 5 V)
- Stack level: 5 levels (interrupt: 3 levels)
- Vectored interrupt function:
  5 interrupt sources (INT pin, timer 1, timer 0, basic interval timer, and serial interface)
- 8-bit A/D converter: 4 channels
  Absolute accuracy
  ± 1.5 LSB or higher (on 5 V ±10 %)
- AC zerocross detector: 1 input (also used as INT pin)
- 8-bit timer: 2 channels
  Timer 0 count clock (f_x/16, f_x/64, f_x/256, INT pin input)
  Timer 1 count clock (f_x/256, f_x/512, f_x/2048, incrementing timer 0)
- 8-bit basic interval timer: 1 channel. Can be used as wathcdog timer.
  Basic interval timer count clock
  (INT pin input, incrementing timer 0, f_x/4096, f_x/8192)
- 3-wire serial interface: 1 channel
- On-chip power-on reset circuit
- I/O pin: 21 pins
- Standby function (HALT/STOP) provided
- Operating temperature: −40 to +85 °C
- Operating voltage: 2.7 to 6.0 V
- CMOS low power consumption

PIN CONFIGURATION FOR THE μPD17135A AND μPD17137A (Top View)



28-pin shrink DIP
28-pin SOP

BLOCK DIAGRAM OF THE μPD17135A AND μPD17137A



MICROCONTROLLER FAMILY FOR SMALL WHITE GOODS APPLIANCES

Item	μPD17134A	μPD17136A	μPD17135A	μPD17137A	Remarks
ROM size	1024 x 16 bits	2048 x 16 bits	1024 x 16 bits	2048 x 16 bits	
RAM size	112 x 4 bits	112 x 4 bits	112 x 4 bits	112 x 4 bits	
Number of I/O port lines	21 lines				Including 8 N-ch open-drain lines
Analog input	4 channels				Also used as port pins
Timer	3 timers				
Serial interface	1 channel				Also used as port pin
Stack	5 levels				
Power-on reset	Provided				
System clock	RC source		Ceramic/crystal source		
Standby function	Provided				STOP/HALT
Power supply	2.7 to 6.0 V				5 V ±10 % for A/D
Package	28-pin shrink DIP 28-pin SOP				
PROM version	μPD17P136A		μPD17P137A		

4-BIT SINGLE-CHIP MICROCONTROLLER

The μPD17P137A is a one-time PROM version of the μPD17137A, whose internal mask ROM is replaced with a one-time PROM, and is therefore suitable for evaluation of the μPD17135A, and μPD17137A or for small-scale production.

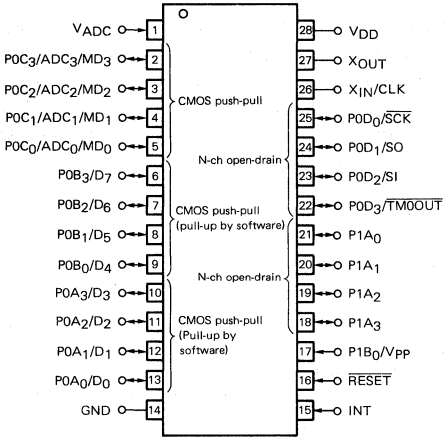
The μPD17P137A is a 4-bit single-chip microcontroller containing four channels of 8-bit A/D converters, two channels of 8-bit timers, an AC zerocross detector, a power-on reset circuit and a serial interface in one chip.

For the CPU, the 17K architecture is used.This enables accumulator direct data memory manipulation, facilitating effective programming. Every instruction is one word long, consisting of 16 bits.

FEATURES

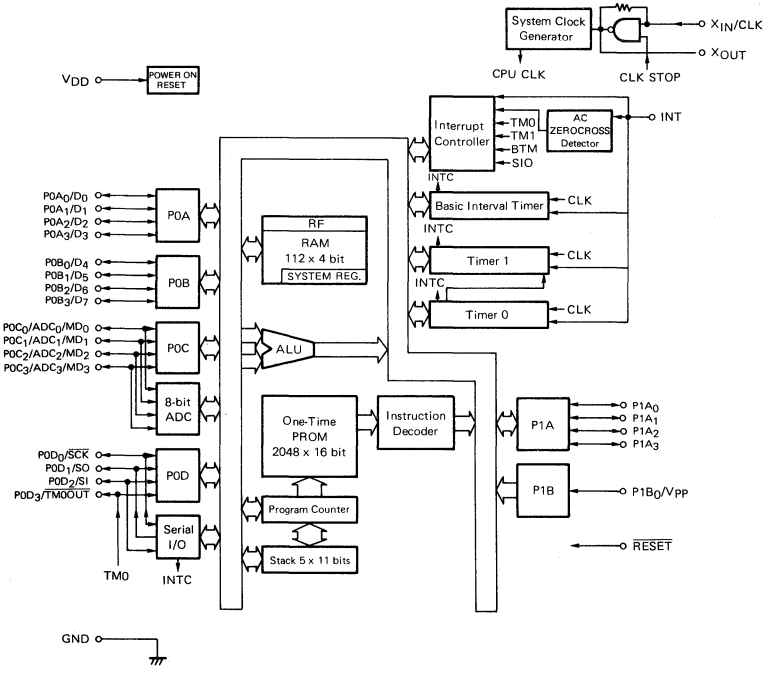
- Program memory (OTP): 4K bytes (2048 x 16 bits)
- Data memory (RAM): 112 words (112 x 4 bits)
- Instruction execution time: 2 μs (at 8 MHz) with ceramic or crystal source, when V_{DD} = 5 V used
- Stack level: 5 levels (interrupt: 3 levels)
- Vectored interrupt function: 5 interrupt sources
- 8-bit A/D converter: 4 channels absolute accuracy ± 1.5 LSB or higher (on 5 V ±10 %)
- AC zerocross detector: 1 input (also used as INT pin)
- 8-bit timer: 2 channels
- 8-bit basic interval timer: 1 channel. Can be used as watchdog timer.
- 3-wire serial interface: 1 channel
- On-chip power-on reset circuit
- Input/output pin: 21 pins
- Standby function (HALT/STOP) provided
- Operating voltage: 2.7 to 5.5 V

PIN CONNECTION μPD17P137A (Top View)



28-pin plastic shrink DIP
28-pin plastic SOP

μPD17P137A BLOCK DIAGRAM



MICROCONTROLLER FAMILY FOR SMALL WHITE GOODS APPLIANCES

Item	μPD17134A	μPD17136A	μPD17135A	μPD17137A	Remarks
ROM size	1024 x 16 bits	2048 x 16 bits	1024 x 16 bits	2048 x 16 bits	
RAM size	112 x 4 bits	112 x 4 bits	112 x 4 bits	112 x 4 bits	
Number of input/ output port lines	21 lines				Including 8 N-ch open-drain lines
Analog input	4 channels				Also used as port pins
Timer	3 timers				
Serial interface	1 channel				Also used as port pin
Stack	5 levels				
Power-on reset	Provided				
System clock	RC source		Ceramic/crystal source		
Standby function	Provided				STOP/HALT
Power supply	2.7 to 5.5 V				5 V ±10 % for A/D
Package	28-pin shrink DIP 28-pin SOP				
PROM version	μPD17P136A		μPD17P137A		

4-BIT SINGLE-CHIP MICROCONTROLLER WITH A/D CONVERTER AND LCD CONTROLLER/DRIVER FOR INFRARED REMOTE CONTROLLER

The μPD17201A is a 4-bit single-chip microcontroller integrating an LCD controller/driver, A/D converter, and an infrared remote controller carrier generator circuit on a single chip.

This microcontroller employs the 17K architecture and can execute transfer and arithmetic operations with a single 16-bit instruction between data memory addresses, and between the data memory and a peripheral circuit.

μPD17201A is housed in an 80-pin plastic QFP.

FEATURES

- 17K architecture
- Program memory (ROM): 6K bytes (3072 x 16 bits)
- Data memory (RAM): 336 words (336 x 4 bits)
- Internal infrared remote controller carrier generator
- 4 channel 8-bit A/D converter
- Internal LCD controller/driver (can display up to 136 segments)
  Common pins: 4, segment pins: 34 (two of the common pins can also be used a segment pins)
  Internal LCD drive constant rising-voltage circuit: LCD drive voltage can be arbitrarily set at 2.4 to 5.4 V by external resistor
- I/O ports: 19
- Three-line serial interface
- Stack levels: 5 (3 interrupt levels)
- 8-bit timer: 1 channel
- Watch timer: 1 channel
- Instruction execution time: 4 μs (with 4 MHz ceramic/crystal oscillator)
- Standby function (STOP, HALT): Watch display with 32,768 kHz crystal oscillator inSTOP mode
- Operating voltage range: 2.2 to 5.5 V

APPLICATIONS

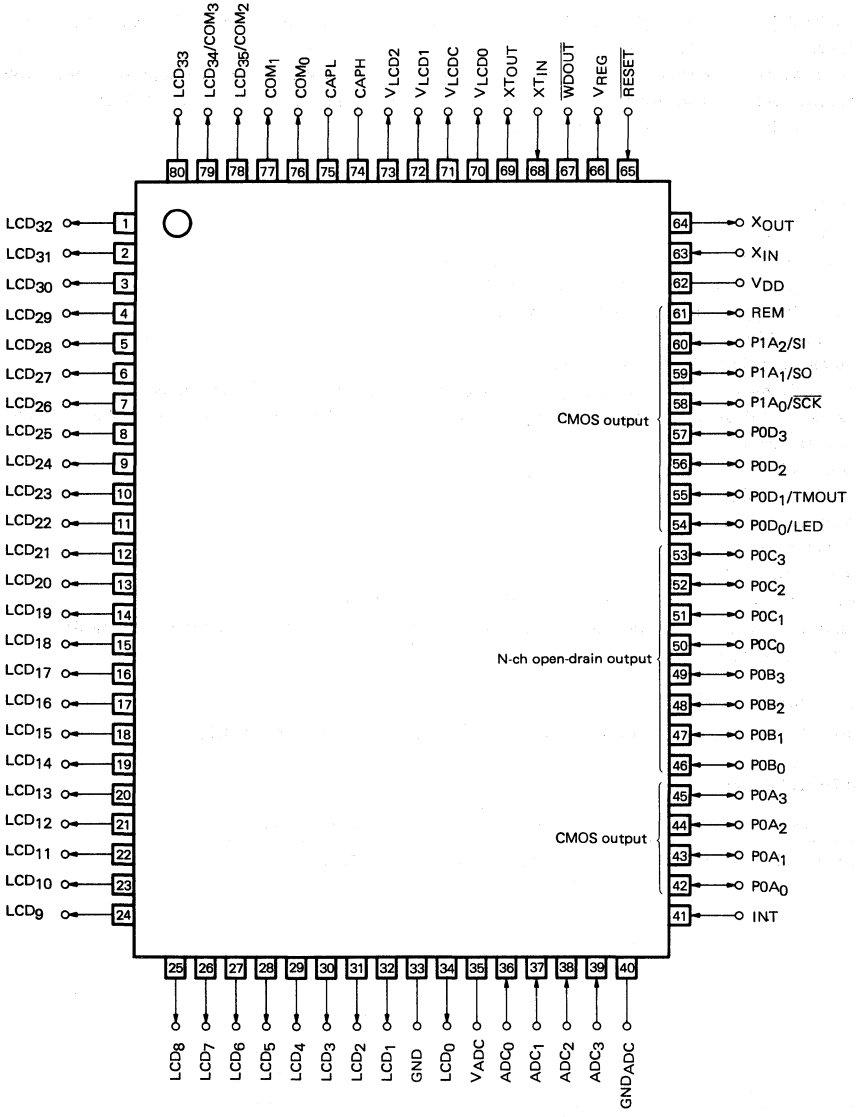
Infrared remote controllers for air conditioners, and remote controllers with LCD

ORDERING INFORMATION

Order Code	Package	Quality Grade
μPD17201AGF-xxx-3B9	80-pin plastic QFP	Standard

1. PIN CONFIGURATION (Top View)

1.1 PIN CONFIGURATION (Top View



1.2 PIN FUNCTION LIST

PIN No.	SYMBOL	I/O	OUTPUT TYPE	PIN NAME	FUNCTION
78 79 80 81 32 34	LCD_{35}/COM_2 LCD_{34}/COM_3 LCD_{33} LCD_{32} LCD_1 LCD_0	Output		LCD segment signal	Segment signal output pins for the LCD driver. LCD_{35}/CM_2 and LCD_{34}/COM_3 serve as segment signal output and common signal output pins. The function for these pins. The function for these pins is selected by LCDMD3 through LCDMD0 (address 32H, bit 3-0) in the register file. Display dots can number 72, 105, or 136, depending on the matrix for the segment signal output and common signal output pins. The bias is fixed to 1/3, and the duty factor is 1/2, 1/3, or 1/4, depending on the selected number of common pins. The frame frequency can be selected by LCDCK2 through LCDCK0 registers (address 31H) in the register file. The dot with a segment signal output pin and common signal output, between which a ± V_{DD} potential difference is generated, lights. The display data for the LCD driver is set through the LCD display register (addresses 40H through 63H in BANK0). The display ON and OFF modes for the LCD driver are set by the LCDEN register (address 31H, bit 3) in the register file. In the display OFF mode, the segment signal output pin outputs a signal waveform, because the display goes off. When μPD17201A is reset by the $\overline{RESET}$ signal, low voltage detection by the voltage detector, or watch-dog timer, the LCDEN register is set in the display OFF mode.
33	GND	–	–	Ground	Device ground pin
35	V_{ADC}	–	–	Analog power	A/D converter power pin. Connect this pin to the V_{DD} pin.
36 37 38 39	ADC_0 ADC_1 ADC_2 ADC_3	Input Input Input Input		A/D converter input 0 A/D converter input 1 A/D converter input 2 A/D converter input 3	Input pins for the 8-bit A/D converter. The A/D converter can also be used as a comparator, when so specified by VREFEN, ADCEN, ADCCH1 and ADCCHO (address 21H) in the register file. The A/D converter has a successive approximate type and its reference voltage is generated by dividing the voltage on the analog power pin (V_{ADC}) with a resistor string. A total of six A/D converter channels, ADC_0 through ADC_3 pins, are available. Two comparator channels, with one consisting of ADC_0 and ADC_2 pins and the other consisting of ADC_1 and ADC_3, are available. The A/D converter or comparator function and the channel to be used are selected by VREFEN, ADCEN, ADCCH1, and ADCCH0 (address 21H) in the register file.
40	GND_{ADC}	–	–	Analog ground	A/D converter ground pin

PIN. NO.	SYMBOL	I/O	OUTPUT TYPE	PIN NAME	FUNCTION
41	INT	Input	–	Interrupt	External interrupt request signal input pin. The interrupt request is issued at the rising edge of the signal input to this pin. The interrupt is not accepted, even when the interrupt request is issued, unless the interrupt is enabled (maskable interrupt). All the interrupts can be enabled by the EI instruction, or only the INT pin can be enabled by IP (address 2FH) in the register file. When the interrupt request is issued, while the interrupt is enabled, the interrupt is accepted, and the program execution branches to address 03H. The interrupt request issuance can be checked by IRQ (address 3FH) in the register file, even when the interrupt is not enabled. All the interrupts are disabled and interrupt requests are cleared, when μPD17201A is reset by the $\overline{\text{RESET}}$ pin or watchdog timer.
42 43 44 45	$P0A_0$ $P0A_1$ $P0A_2$ $P0A_3$	I/O	CMOS push-pull	Port 0A	These pins constitute a 4-bit I/O port, which can be set in input or output mode in 4 bits units (group I/O). The input mode is specified by P0AGIO (address 37H, bit 0) in the register file. The input data is read and output data is set through port register P0A (address 70H in BANK0). $P0A_0$ through $P0A_3$ are internally connected with a pull-up resistor. When μPD17201A is reset by the $\overline{\text{RESET}}$ signal or watchdog timer, these pins are set in the input mode.
46 47 48 49	$P0B_0$ $P0B_1$ $P0B_2$ $P0B_3$	I/O	N-ch open-drain	Port 0B	These pins constitute a 4-bit I/O port, which can be set in input or output mode in 4 bits units (group I/O). The input mode is specified by P0BGIO (address 37H, bit 1) in the register file. The input data is read and output data is set through port register P0B (address 71H in BANK0). Since these pins are N-ch opendrain, they must be connected to an external pull-up resistor. When μPD17201A is reset by the $\overline{\text{RESET}}$ signal or watchdog timer, these pins are set in the input mode.
50 51 52 53	$P0C_0$ $P0C_1$ $P0C_2$ $P0C_3$	I/O	N-ch open-drain	Port 0C	These pins constitute a 4-bit I/O port, which can be set in input or output mode in 4 bit units (group I/O). The input mode is specified by P0CGIO (address 37H, bit 2) in the register file. The input data is read and output data is set through port register P0C (address 72H in BANK0). Since these pins are N-ch opendrain, they must be connected to an external pull-up resistor. When μPD17201A is reset by the $\overline{\text{RESET}}$ signal or watchdog timer, these pins are set in the input mode.

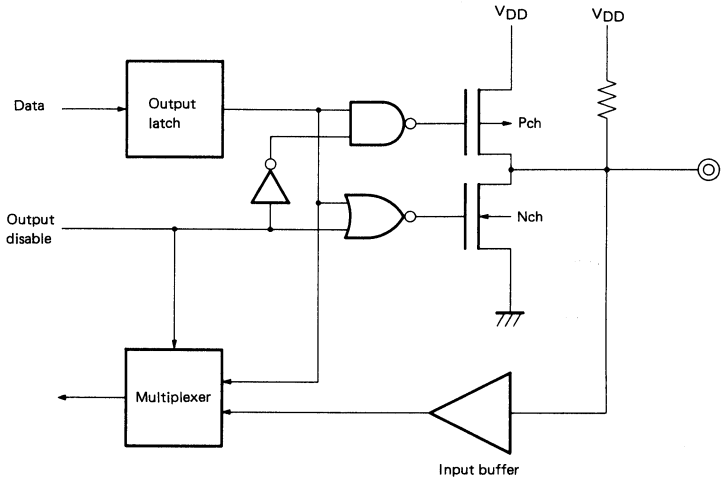
PIN NO.	SYMBOL	I/O	OUTPUT TYPE	PIN NAME	FUNCTION
54 55 56	POD_0/LED POD_1/TMOUT POD_2	I/O	CMOS11 push-pull	Port 0D	POD_0/LED is a 4-bit I/O port pin and LED output pin. POD_1/TMOUT is a 4-bit I/O port pin and an external signal output pin for the timer. Whether these pins function as port pins or LED output and timer output pins is specified by NRZEN (bit 2 in address 23H) and TMOE (bit 1 in address 23H). When μPD17201A is reset by the $\overline{RESET}$ signal or watchdog timer, these pins are set in the input mode. (1) As I/O port pin These pins can be set in input or output mode bitwise (bit I/O) by P0DBIO3 through P0DBIO0 (address 27H, bits 3 through 0). The input data is read and output data is set through port register P0D (address 73H in BANK0). (2) POD_0 as LED output pin Whether POD_0 pin functions as LED output pin or I/O port pin is specified by NRZEN. As an LED output pin, this pin outputs an NRZ signal in synchronization with REM output. (3) POD_1 as timer output pin Whether this pin functions as the external signal output pin for the 8-bit timer or I/O port pin is specified by TMOE).
58 59 60	$P1A_0/\overline{SCK}$ $P1A_1$/SO $P1A_2$/SI	I/O	CMOS push-pull	Port 1A	These pins constitute a 3-bit general-purpose I/O port, which also functions as a serial interface. Whether these pins function as an I/O port or serial interface is specified by SIOEN (address 23H, bit 0) in the register file. When μPD17201A is reset by the $\overline{RESET}$ signal or watchdog timer, these pins are set in the input mode. (1) As 3-bit I/O port The I/O port can be set in the input or output mode in 3 bit units (group I/O) by P1AGIO (address 37H, bit 3) in the register file. The input data is read or output data is set through port register P1A (address 70H in BANK1). (2) As serial interface The serial interface function (μCOM standard mode) is selected by SIOEN.
61	REM	Output	CMOS push-pull	Remote controller transfer output	Infrared remote controller signal output pin. The carrier frequency can be set for from to 16 to 1024 kHz.
62	V_{DD}			Power supply	Device power supply pin
63 64	X_{IN} X_{OUT}	Input Output		Main clock oscillator	Connect a 4 MHz ceramic/crystal oscillator between these pins.
65	$\overline{RESET}$	Input		Reset	Inputs the system reset signal. μPD17021A is reset, when a low-level signal is input to this pin for 50 μs or longer.
66	V_{REG}	Output		Voltage regulator output	Voltage regulator output pin. Connect an external 0.1 μF capacitor to this pin.
67	$\overline{WDOUT}$	Output		Watchdog output	Detects program overrunning, such as for watchdog timer and stack overflow

PIN NO.	SYMBOL	I/O	OUTPUT TYPE	PIN NAME	FUNCTION
68 74	XT_{IN} XT_{OUT}	Input Output		Subclock oscillator	Connect a 32 kHz crystal oscillator between these pins.
71	V_{LCDC}	Output		LCD drive reference voltage adjuster	This pin adjusts the LCD drive reference voltage. Connect a resistor between V_{LCD0} and V_{LCDC}, and between V_{LCDC} and GND to adjust the reference voltage.
70 72 73	V_{LCD0} V_{LCD1} V_{LCD2}	Output		LCD drive reference voltage output	LCD drive reference voltage output pins. V_{LCD0} outputs the reference voltage. V_{LCDC1} outputs a voltage two times the reference voltage (doubler), while V_{LCDC2} outputs a voltage three times the reference voltage (tripler). Connect a resistor to adjust the reference voltage between V_{LCD0} and V_{LCDC} and between V_{LCDC} and GND. Connect a 0.47 μF capacitor between each pin and GND.
74 75	CAPH CAPL			Voltage-raising capacitor	Connect a voltage-raising capacitor between these pins. Connect a 0.47 μF capacitor between these pins.
76 77	COM_0 COM_1	Output		Common signal	Common signal output pins for the LCD driver. In addition to these pins, LCD_{35}/COM_2 and LCD_{34}/COM_3 pins can also be used as common signal output pins. The function of these pins is selected by LCDMD0 and LCDMD1 registers (address 32H) in the register file. The display dots can number 72, 105, or 136, depending on the matrix of the segment signal output and common signal output pins. The bias is fixed to 1/3, and the duty factor is 1/2, 1/3, or 1/4, depending on the selected number of common pins. The frame frequency can be selected by LCDCK0 and LCDCK1 registers (address 31H) in the register file. The dot with a segment signal output pin and common signal output, between which a $\pm V_{DD}$ potential difference is generated, lights. The display ON and OFF modes for the LCD driver are set by the LCDEN register (address 31H) in the register file. In the display OFF mode, the segment signal output pin outputs a signal waveform, because the display goes off. When μPD17201A is reset by the $\overline{RESET}$ signal, low voltage detection by the voltage detector, or watchdog timer, the LCDEN register is set in the display OFF mode.

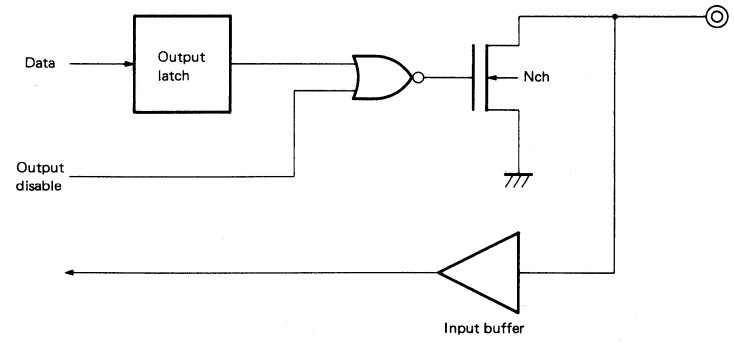
1.3 INPUT/OUTPUT CIRCUITS

The input/output circuits for each μPD17201A pin are shown below.

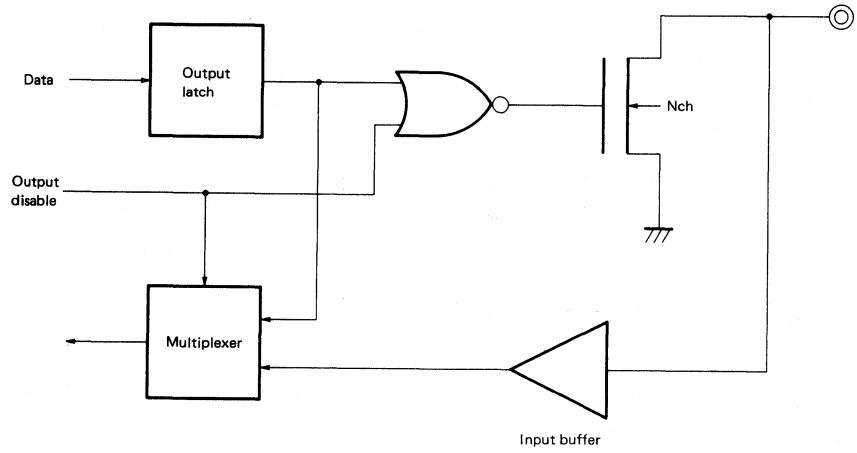
(1) $P0A_0$-$P0A_3$



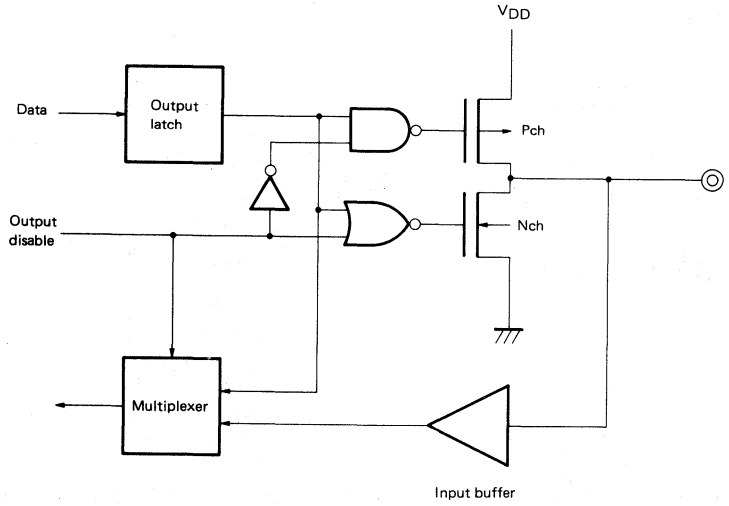
(2) $P0B_0$-$P0B_3$



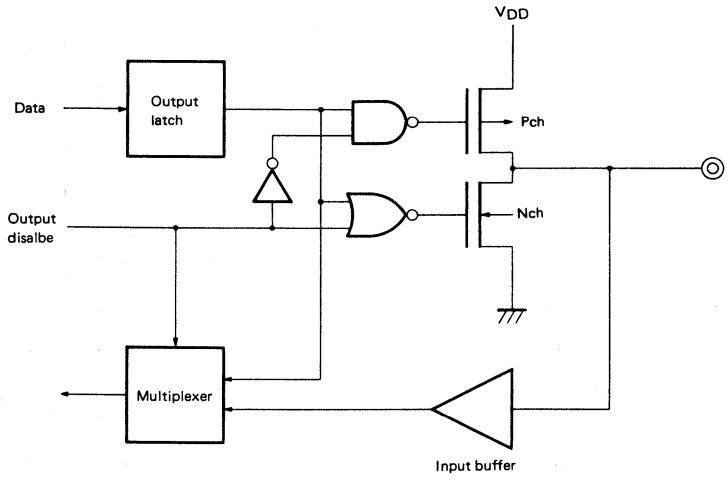
(3) $P0C_0$-$P0C_3$



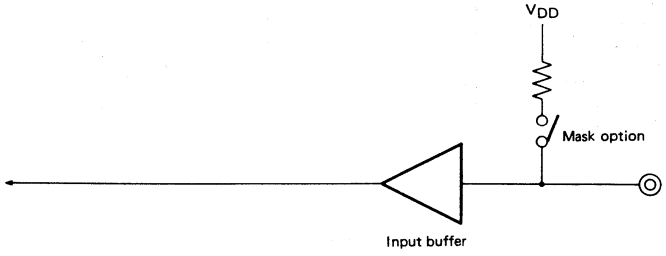
(4) $P0D_0$-$P0D_3$



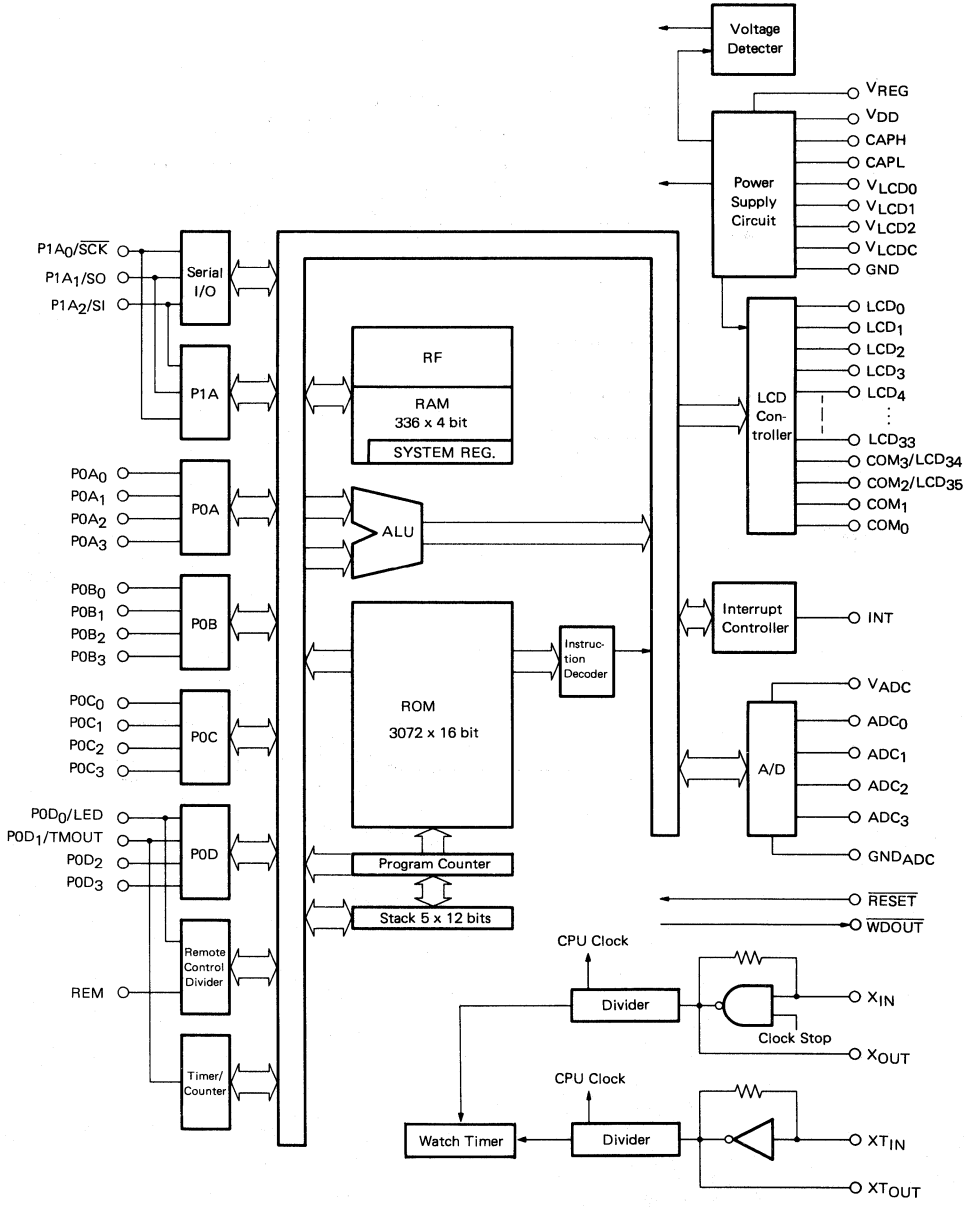
(5) $P1A_0$-$P1A_2$



(6) $\overline{\text{RESET}}$



2. BLOCK DIAGRAM



3.1 MASK OPTION DEFINITION DIRECTIVES

Table 3-1 lists the directives that can be used in the mask option definition block.
Here is an example of mask option definition:

Symbol field	Mnemonic field	Operand field	Comment field
[label:]	OPTION		[; comment]
	OPTRES	RESPLUP	
	OPTCK	USEX,USEXT	
	ENDOP		

Table 3-1 Mask Option Definition Directives

Item	Directive	No. of Operands	First Operand	Second Operand
$\overline{\text{RESET}}$ pin	OPTRES	1	RESET Mask option	
			RESPLUP (w/pull-up resistor) OPEN (w/o pull-up resistor)	
External oscillator	OPTCK	2	Using main clock	Using subclock
			USEX (main clock is used) NOX (main clock is not used)	USEXT (subclock is used) NOXT (subclock is not used)

3.2 KEYWORD SYMBOLS

The symbols defined by the μPD17201A device file, are listed in Table 3-2. The defined symbols are the following register file names, port names, and peripheral device names.

Table 3-2 Keyword Symbols

Symbol	Attribute	Value	R/W	Remarks
DBF3	MEM	0.0CH	R/W	Bits 15-12 for data buffer
DBF2	MEM	0.0DH	R/W	Bits 11-8 for data buffer
DBF1	MEM	0.0EH	R/W	Bits 7-4 for data duffer
DBF0	MEM	0.0FH	R/W	Bits 3-0 for data duffer
AR3	MEM	0.74H	R	Bits 15 12 for address register
AR2	MEM	0.75H	R/W	Bits 11-8 for address register
AR1	MEM	0.76H	R/W	Bits 7-4 for address register
AR0	MEM	0.77H	R/W	Bits 3-0 for address register
WR	MEM	0.78H	R/W	Window register
BANK	MEM	0.79H	R/W	Bank register
IXH	MEM	0.7AH	R/W	Bits 11-8 for index register
MPH	MEM	0.7AH	R/W	Bits 7-4 for memory pointer
MPE	FLG	0.7AH.3	R/W	Memory pointer enable flag
IXM	MEM	0.7BH	R/W	Bits 7-4 for index register
MPL	MEM	0.7BH	R/W	Bits 3-0 for memory pointer
IXL	MEM	0.7CH	R/W	Bits 3-0 for index register
RPH	MEM	0.7DH	R/W	Bits 7-4 for register pointer
RPL	MEM	0.7EH	R/W	Bits 3-0 for register pointer
PSW	MEM	0.7FH	R/W	Program status word
BCD	FLG	0.7EH.0	R/W	BCD arithmetic flag
CMP	FLG	0.7FH.3	R/W	Compare flag
CY	FLG	0.7FH.2	R/W	Carry flag
Z	FLG	0.7FH.1	R/W	Zero flag
IXE	FLG	0.7FH.0	R/W	Index register enable flag
LCDD0	MEM	0.40H	R/W	LCD segment 0
LCDD1	MEM	0.41H	R/W	LCD segment 1
LCDD2	MEM	0.42H	R/W	LCD segment 2
LCDD3	MEM	0.43H	R/W	LCD segment 3
LCDD4	MEM	0.44H	R/W	LCD segment 4
LCDD5	MEM	0.45H	R/W	LCD segment 5
LCDD6	MEM	0.46H	R/W	LCD segment 6
LCDD7	MEM	0.47H	R/W	LCD segment 7
LCDD8	MEM	0.48H	R/W	LCD segment 8
LCDD9	MEM	0.49H	R/W	LCD segment 9
LCDD10	MEM	0.4AH	R/W	LCD segment 10
LCDD11	MEM	0.4BH	R/W	LCD segment 11

Symbol	Attribute	Value	R/W	Remarks
LCDD12	MEM	0.4CH	R/W	LCD segment 12
LCDD13	MEM	0.4DH	R/W	LCD segment 13
LCDD14	MEM	0.4EH	R/W	LCD segment 14
LCDD15	MEM	0.4FH	R/W	LCD segment 15
LCDD16	MEM	0.50H	R/W	LCD segment 16
LCDD17	MEM	0.51H	R/W	LCD segment 17
LCDD18	MEM	0.52H	R/W	LCD segment 18
LCDD19	MEM	0.53H	R/W	LCD segment 19
LCDD20	MEM	0.54H	R/W	LCD segment 20
LCDD21	MEM	0.55H	R/W	LCD segment 21
LCDD22	MEM	0.56H	R/W	LCD segment 22
LCDD23	MEM	0.57H	R/W	LCD segment 23
LCDD24	MEM	0.58H	R/W	LCD segment 24
LCDD25	MEM	0.59H	R/W	LCD segment 25
LCDD26	MEM	0.5AH	R/W	LCD segment 26
LCDD27	MEM	0.5BH	R/W	LCD segment 27
LCDD28	MEM	0.5CH	R/W	LCD segment 28
LCDD29	MEM	0.5DH	R/W	LCD segment 29
LCDD30	MEM	0.5EH	R/W	LCD segment 30
LCDD31	MEM	0.5FH	R/W	LCD segment 31
LCDD32	MEM	0.60H	R/W	LCD segment 32
LCDD33	MEM	0.61H	R/W	LCD segment 33
LCDD34	MEM	0.62H	R/W	LCD segment 34
LCDD35	MEM	0.63H	R/W	LCD segment 35
P0A0	FLG	0.70H.0	R/W	Bit 0 for port 0A
P0A1	FLG	0.70H.1	R/W	Bit 1 for port 0A
P0A2	FLG	0.70H.2	R/W	Bit 2 for port 0A
P0A3	FLG	0.70H.3	R/W	Bit 3 for port 0A
P0B0	FLG	0.71H.0	R/W	Bit 0 for port 0B
P0B1	FLG	0.71H.1	R/W	Bit 1 for port 0B
P0B2	FLG	0.71H.2	R/W	Bit 2 for port 0B
P0B3	FLG	0.71H.3	R/W	Bit 3 for port 0B
P0C0	FLG	0.72H.0	R/W	Bit 0 for port 0C
P0C1	FLG	0.72H.1	R/W	Bit 1 for port 0C
P0C2	FLG	0.72H.2	R/W	Bit 2 for port 0C
P0C3	FLG	0.72H.3	R/W	Bit 3 for port 0C
P0D0	FLG	0.73H.0	R/W	Bit 0 for port 0D
P0D1	FLG	0.73H.1	R/W	Bit 1 for port 0D
P0D2	FLG	0.73H.2	R/W	Bit 2 for port 0D
P0D3	FLG	0.73H.3	R/W	Bit 3 for port 0D
P1A0	FLG	1.70H.0	R/W	Bit 0 for port 1A

Symbol	Attribute	Value	R/W	Remarks
P1A1	FLG	1.70H.1	R/W	Bit 1 for port 1A
P1A2	FLG	1.70H.2	R/W	Bit 2 for port 1A
SP	MEM	0.81H	R/W	Stack pointer
SYSCK	FLG	0.82H.1	R/W	Selects system clock
XEN	FLG	0.82H.0	R/W	Enables main clock
WDTRES	FLG	0.83H.3	R/W	Resets watchdog timer
WTMMD	FLG	0.83H.2	R/W	Selects watch timer mode
WTMRES	FLG	0.83H.1	R/W	Resets watch timer mode
VDDDET1	FLG	0.87H.3	R/W	VDD detection flag 1
VDDDET0	FLG	0.87H.2	R/W	VDD detection flag 0
INT	FLG	0.8FH.0	R	Interrupt pin status
NRZBF	FLG	0.91H.0	R/W	NRZ buffer data
NRZ	FLG	0.92H.0	R/W	NRZ data
ADCCMP	FLG	0.A0H.0	R/W	Comparator result
VREFEN	FLG	0.A1H.3	R/W	Enables VDD reference terminal
ADCEN	FLG	0.A1H.2	R/W	ADC enable flag
ADCCH0	FLG	0.A1H.1	R/W	ADC channel selection #1
ADCCH0	FLG	0.A1H.0	R/W	ADC channel selection #0
SIOTS	FLG	0.A2H.3	R/W	Serial interface
SIOHIZ	FLG	0.A2H.2	R/W	SO/port selection
SIOCK1	FLG	0.A2H.1	R/W	Serial interface clock #1
SIOCK0	FLG	0.A2H.0	R/W	Serial interface clock #0
NRZEN	FLG	0.A3H.2	R/W	NRZ enable flag
TMOE	FLG	0.A3H.1	R/W	Timer output enable flag
SIOEN	FLG	0.A3H.0	R/W	SIO enable flag
P0DBI03	FLG	0.A7H.3	R/W	I/O setting flag for bit 3 in P0D port
P0DBI02	FLG	0.A7H.2	R/W	I/O setting flag for bit 2 in P0D port
P0DBI01	FLG	0.A7H.1	R/W	I/O setting flag for bit 1 in P0D port
P0DBI00	FLG	0.A7H.0	R/W	I/O setting flag for bit 0 in P0D port
IPSIO	FLG	0.AFH.3	R/W	Interrupt enable flag for INTSIO
IPWTM	FLG	0.AFH.2	R/W	Watch timer interrupt enable flag
IP	FLG	0.AFH.1	R/W	INT interrupt enable flag
IPTM	FLG	0.AFH.0	R/W	8-bit timer interrupt enable flag
LCDEN	FLG	0.B1H.3	R/W	LCD display enable flag
LCDCK2	FLG	0.B1H.2	R/W	LCD display setting #2
LCDCK1	FLG	0.B1H.1	R/W	LCD display setting #1
LCDCK0	FLG	0.B1H.0	R/W	LCD display setting #0
LCDMD3	FLG	0.B2H.3	R/W	LCD display setting #3
LCDMD2	FLG	0.B2H.2	R/W	LCD display setting #2
LCDMD1	FLG	0.B2H.1	R/W	LCD display setting #1
LCDMD0	FLG	0.B2H.0	R/W	LCD display setting #0

Symbol	Attribute	Value	R/W	Remarks
TMEN	FLG	0.B3H.3	R/W	8-bit timer counter enable flag
TMRES	FLG	0.B3H.2	R/W	8-bit timer reset flag
TMCK1	FLG	0.B3H.1	R/W	Selects 8-bit timer clock source
TMCK0	FLG	0.B3H.0	R/W	Selects 8-bit timer clock source
P1AGI0	FLG	0.B7H.3	R/W	P1A port I/O setting flag
P0CGI0	FLG	0.B7H.2	R/W	P0C port I/O setting flag
P0BGI0	FLG	0.B7H.1	R/W	P0B port I/O setting flag
P0AGI0	FLG	0.B7H.0	R/W	P0A port I/O setting flag
IRQSIO	FLG	0.BBH.3	R/W	SIO interrupt request flag
IRQWTM	FLG	0.BCH.2	R/W	Watch timer interrupt request flag
IRQ	FLG	0.BDH.1	R/W	INT interrupt request flag
IRQTM	FLG	0.BEH.0	R/W	8-bit timer interrupt request flag
SIOSFR	DAT	01H	R/W	Serial I/O register
TMM	DAT	02H	W	8-bit timer modulo register
TMC	DAT	02H	R	8-bit timer count register
NRZLTMM	DAT	03H	R/W	NRZ modulo register, low
NRZHTMM	DAT	04H	R/W	NRZ modulo register, high
ADCR	DAT	05H	R/W	ADC reference voltage setting register
DBF	DAT	0FH	R/W	Data buffer
IX	DAT	01H	R/W	Index register
AR	DAT	40H	R/W	Address register

4. μPD17201A INSTRUCTION SET

4.1 INSTRUCTION SET OUTLINE

$b_{14}-b_{11}$ \ b_{15}		0	1
BIN	HEX		
0 0 0 0	0	ADD r, m	ADD m, #i
0 0 0 1	1	SUB r, m	SUB m, #i
0 0 1 0	2	ADDC r, m	ADDC m, #i
0 0 1 1	3	SUBC r, m	SUBC m, #i
0 1 0 0	4	AND r, m	AND m, #i
0 1 0 1	5	XOR r, m	XOR m, #i
0 1 1 0	6	OR r, m	OR m, #i
0 1 1 1	7	INC AR INC IX MOVT DBF, @AR BR @AR CALL @AR RET RETSK EI DI RETI PUSH AR POP AR GET DBF, p PUT p, DBF PEEK WR, RA POKE RA, WR RORC r HALT h NOP	
1 0 0 0	8	LD r, m	ST m, r
1 0 0 1	9	SKE m, #i	SKGE m, #i
1 0 1 0	A	MOV @r, m	MOV m, @r
1 0 1 1	B	SKNE m, #i	SKLT m, #i
1 1 0 0	C	BR addr (page 0)	CALL addr (page 0)
1 1 0 1	D	BR addr (page 1)	MOV m, #i
1 1 1 0	E		SKT m, #n
1 1 1 1	F		SKF m, #n

4.2 INSTRUCTION LIST

Legend

M : One of data memory specified by [(BANK), m]
m : Data memory address specified by [m_H, m_L] of each bank
m_H : Data memory address high (row address) ; 3 bits
m_L : Data memory address low (column address) ; 4 bits
R : One of general register specified by [(RP), r]
r : General register address low (column address) ; 4 bits
RP : General register pointer
RF : One of register file specified by rf
rf : Register file address specified by [rf_H, rf_L]
rf_H : Register file address high (row address) ; 3 bits
rf_L : Register file address low (column address) ; 4 bits
AR : Address register
IX : Index register
IXE : Index register enable flag
DBF : Data buffer
WR : Window register
MP : Memory pointer
MPE : Memory pointer enable flag
PE : Peripheral
p : Peripheral address
p_H : Peripheral address high (row address) ; 3 bits
p_L : Peripheral address low (column address) ; 4 bits

PC : Program counter
SP : Stack pointer
STACK : Stack specified by (SP)
BANK : Bank register
(AR)rom : One of program memory data specified by (AR)
INTEF : Interrupt enable flag
i : Immediate data ; 4 bits
n : Bit position ; 4 bits
addr : One of program memory address ; 11 bits
a_H : Program memory address high ; 3 bits
a_M : Program memory address middle ; 4 bits
a_L : Program memory address low ; 4 bits
CY : Carry
s : Stop releasing condition
h : Halt releasing condition
[ ] : Address of M, R, RF
( ) : Contents of M, R, RF, AR, IX, DBF, WR, PE

Group	Mnemonic	Operand	Function	Operation	Machine code			
					OP code			
Addition	ADD	r, m	Add memory to register	R ← (R) + (M)	00000	m_H	m_L	r
		m, #i	Add immediate data to memory	M ← (M) + i	10000	m_H	m_L	i
	ADDC	r, m	Add memory to register with carry	R ← (R) + (M) + (CY)	00010	m_H	m_L	r
		m, #i	Add immediate data to memory with carry	R ← (M) + i + (CY)	10010	m_H	m_L	i
	INC	AR	Increment address register	AR ← AR + i	00111	000	1001	0000
		IX	Increment index register	IX ← IX + i	00111	000	1000	0000
Subtraction	SUB	r, m	Subtract memory from register	R ← (R) − (M)	00001	m_H	m_L	r
		m, #i	Subtract immediate data from memory	M ← (M) − i	10001	m_H	m_L	i
	SUBC	r, m	Subtract memory from register with borrow	R ← (R) − (M) − (CY)	00011	m_H	m_L	r
		m, #i	Subtract immediate data from memory with borrow	M ← (M) − i − (CY)	10011	m_H	m_L	i
Compare	SKE	m, #i	Skip if memory equal to immediate data	M − i, skip if zero	01001	m_H	m_L	i
	SKGE	m, #i	Skip if memory greater than or equal to immediate data	M − i, skip if not borrow	11001	m_H	m_L	i
	SKLT	m, #i	Skip if memory less than immediate data	M − i, skip if borrow	11011	m_H	m_L	i
	SKNE	m, #i	Skip if memory not equal to immediate data	M − i, skip if not zero	01011	m_H	m_L	i
Logical	AND	m, #i	Logical AND of memory and immediate data	M ← (M) AND i	10100	m_H	m_L	i
		r, m	Logical AND of register and memory	R ← (R) AND (M)	00100	m_H	m_L	r
	OR	m, #i	Logical OR of memory and immediate data	M ← (M) OR i	10110	m_H	m_L	i
		r, m	Logical OR of register and memory	R ← (R) OR (M)	00110	m_H	m_L	r
	XOR	m, #i	Logical XOR of memory and immediate data	M ← (M) XOR i	10101	m_H	m_L	i
		r, m	Logical XOR of register and memory	R ← (R) XOR (M)	00101	m_H	m_L	r

Group	Mnemonic	Operand	Function	Operation	Machine code			
					OP code			
Transfer	LD	r, m	Load memory to register	R ← (M)	01000	m_H	m_L	r
	ST	m, r	Store register to memory	(M) ← R	11000	m_H	m_L	r
	MOV	@r, m	Move memory to destination memory referring to register	if MPE ≠ 1, [(MP), (R)] ← (M) if MPE = 0, [(m_H), (R)] ← (M)	01010	m_H	m_L	r
		m, @r	Move source memory referring to register to memory	if MPE = 1, M ← [(MP), (R)] if MPE = 0, M ← [(m_H), (R)]	11010	m_H	m_L	r
		m, #i	Move immediate data to memory	M ← i	11101	m_H	m_L	i
	MOVT	DBF, @AR	Move ROM data from the address specified in AR to DBF	sp ← (sp) − 1, STACK ← PC DBF ← (AR) rom, PC ← STACK, sp ← (sp) + 1	00111	000	0001	0000
	PUSH	AR	Decrement SP, then move AR to stack top	SP ← (SP) − 1, STACK ← AR	00111	000	1101	0000
	POP	AR	Move stack top to AR, then increment SP	AR ← STACK, SP ← SP + 1	00111	000	1100	0000
	PEEK	WR, RA	Get from RF through WR	WR ← (RF)	00111	rf_H	0011	rf_L
	POKE	RA, WR	Put data on WR into RF	(RF) ← WR	00111	rf_H	0010	rf_L
	GET	DBF, p	Get peripheral data to DBF	DBF ← P	00111	p_H	1011	p_L
	PUT	p, DBF	Put data in DBF to peripheral	P ← DBF	00111	p_H	1010	p_L
Judge	SKT	m, #n	Test memory bits, then skip if all bits specified are true	CMP ← 0, skip if M_n = all "1"	11110	m_H	m_L	n
	SKF	m, #n	Test memory bits, then skip if all bits specified are false	CMP ← 0, skip if M_n = all "0"	11111	m_H	m_L	n
Branch	BR	addr	Jump to the address specified in page 0	PC ← ADDR, PAGE ← 00	01100	a_H	a_M	a_L
			Jump to the address specified in page 1	PC ← ADDR, PAGE ← 01	01101	a_H	a_M	a_L
		@AR	Jump to the address specified in AR	PC ← AR	00111	000	0100	0000
Shift	RORC	r	Rotate register right with carry	(CY) → (R) → CY	00111	000	0111	r
Subroutine	CALL	addr	Call subroutine in page 0	SP ← (SP) − 1, STACK ← ((PC) + 1), PC ← ADDR, PAGE ← 00	11100	a_H	a_M	a_L
		@AR	Call subroutine specified in AR	SP ← (SP) − 1, STACK ← ((PC) + 1), PC ← (AR)	00111	000	0101	0000
	RET		Return to main routine from subroutine	PC ← (STACK), SP ← (SP) + 1	00111	000	1110	0000
	RETSK		Return to main routine from subroutine, then skip unconditionary	PC ← (STACK), SP ← (SP) + 1 and skip	00111	001	1110	0000
	RETI		Return to main routine from interrupt service routine	PC ← (STACK), SP ← (SP) + 1 BANK ← (Interruptstack)	00111	100	1110	0000
Interrupt	EI		Enable interrupt	INTE flag ← 1	00111	000	1111	0000
	DI		Disable interrupt	INTE flag ← 0	00111	001	1111	0000
Other	HALT	h	Halt the CPU, restart by condition H	HALT	00111	011	1111	h
	NOP		No operation	No operation	00111	100	1111	0000

5. ELECTRICAL CHARACTERISTICS (Preliminary)

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage	V_{DD}		-0.3 to +7.0	V
Input Voltage	V_I	P0B0-P0B3	-0.3 to V_{DD}+0.3	V
		All pins, except above	-0.3 to V_{DD}+0.3	V
Operating Temperature	T_{opt}		-20 to +75	°C
Storage Temperature	T_{stg}		-40 to +125	°C

CAPACITANCE (T_a = 25 °C, V_{DD} = 0 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Input Capacitance	C_{IN}			10	pF	INT, SI, $\overline{RESET}$ pins
	C_{PIN}			10	pF	Other than INT, SI, $\overline{RESET}$

RECOMMENDED OPERATING RANGE

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Supply Voltage	V_{DD1}	2.2	3.0	5.5	V	f_X = 4 MHz
	V_{DD2}	3.5	5.0	5.5	V	f_X = 8 MHz
Main Clock Oscillation Frequency	f_X	2.0	4.0	8.0	MHz	
Subclock Oscillation Frequency	f_{XT}		32.768		kHz	

DC CHARACTERISTICS (V_{DD} = 2.2 to 5.5 V, T_a = −20 to +75 °C, f_X = 4 MHz, f_{XT} = 32 kHz)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS	
Operating Supply Voltage	V_{DD}	2.2	3.0	5.5	V		
High-level Input Voltage	V_{IH1}	2.4			V	$\overline{RESET}$ pin	
	V_{IH2}	2.			V	Other than $\overline{RESET}$	
Low-level Input Voltage	V_{IL1}			0.6	V	$\overline{RESET}$ pin	
	V_{IL2}			0.9	V	Other than $\overline{RESET}$ pin	
High-Level Input Current	I_{IH1}			0.2	μA	INT pin	V_{IH} = 3.0 V
	I_{IH2}			0.2	μA	$\overline{RESET}$ pin	V_{IH} = 3.0 V
	I_{IH3}			0.2	μA	P0A-P1A pin	V_{IH} = 3.0 V
Low-Level Input Current	I_{IL1}			0.2	μA	INT pin	V_{IL} = 0 V
	I_{IL2}			0.2	μA		VIL = 0 V w/o pull-up resistor
	I_{IL3}	20	50	100	μA	$\overline{RESET}$ pin	V_{IL} = 0 V w/pull-up resistor
	IIL4			0.2	μA	P0A pin	V_{IL} = 0 V w/o pull-up resistor
	I_{IL5}	6	12	20	μA		V_{IL} = 0 V w/pull-up resistor
	I_{IL6}			0.2	μA	P0B, P0C, P0D, P1A, pin	V_{IL} = 0 V
High-Level Output Current	I_{OH1}	0.6	2.0	4.0	mA	P0A, P0D, P1A pin	V_{OH} = 2.7 V
	I_{OH2}	7.0	15.0	25.0	mA	REM pin	V_{OH} = 1.0 V
Low-Level Output Current	I_{OL1}	0.5	1.5	2.5	mA	P0A, P0D, P1A pin	V_{OL} = 0.3 V
	I_{OL2}	0.5	1.5	2.5	mA	P0B, P0C pin	V_{OL} = 0.3 V
	I_{OL3}	0.5	1.5	2.5	mA	REM pin	V_{OL} = 0.3 V
Supply Current	I_{DD1}	0.2	0.5	1.5	mA	Operation mode	XT and X
	I_{DD2}		15	30	μA		Only XT
	I_{DD3}		0.5	1.5	mA	HALT mode	XT and X
	I_{DD4}		10	15	μA		Only XT
LCD Output Voltage Adjustable Range	V_{LCD0}	0.6		1.8	V		
Doubler Output Voltage	V_{LCD1}	1.9 V_{LCD0}	2 V_{LCD0}		V		
Tripler Output Voltage	V_{LCD2}	2.85 V_{LCD0}	3 V_{LCD0}		V		
Common Output Current	I_{COM}	30			μA	V_{DS} = 0.2 V	
Segment Output Current	I_{LCD}	5			μA	V_{DS} = 0.2 V	
Low Voltage Detection Voltage 1	V_{DET1}	1.6	2.0	2.9	V		
Low Voltage Detection Voltage 2	V_{DET2}	1.9	2.2	2.9	V		
A/D Converter Current Dissipation	I_{DD5}		60	120	μA	V_{ADC} = 3 V	
Absolute A/D Conversion Accuracy			±1	±2	LSB	V_{ADC} = 3 V	

AC CHARACTERISTICS (T_a = −20 to +75 °C, V_{DD} = 2.2 to 5.5 V)

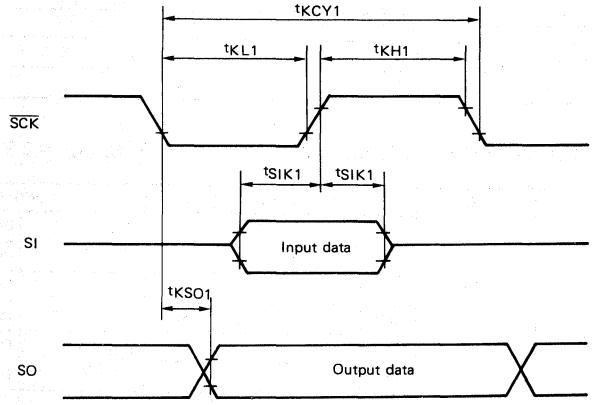
CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Main Clock Oscillation Frequency	fX	2.0		4.0	MHz	V_{DD} = 2.2 to 5.5 V
		2.0		8.0	MHz	V_{DD} = 3.5 to 5.5 V
Subclock Oscillation Frequency	f_{XT}		32.768		kHz	
INT Input High-Level Width	t_{INTH}	50			μs	
$\overline{\text{RESET}}$ Low-Level Width	t_{RSL}	50			μs	

SERIAL INTERFACE AC CHARACTERISTICS (T_a = −20 to +75 °C, V_{DD} = 2.2 to 5.5 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS	
$\overline{\text{SCK}}$ Cycle Time	t_{KCY}	2.0			μs	V_{DD} = 4.5 to 5.5 V	Data input
		10.0			μs		Data output
		5.0			μs		Data input
		13.0			μs		Data output
$\overline{\text{SCK}}$ Low-Level Width	t_{KH}, t_{KL}	1.0			μs	V_{DD} = 4.5 to 5.5 V	Data-input
		5.0			μs		Data output
		2.5			μs		Data input
		6.5			μs		Data output
SI Setup Time (vs. $\overline{\text{SCK}}$ ↑)	t_{SIK}	100			ns		
SI Hold Time (vs. $\overline{\text{SCK}}$ ↑)	t_{KS}	100			ns		
$\overline{\text{SCK}}$ ↓ → SO Output Delay Time	t_{KSO}			4.5	μs	C_L = 100 pF	

SERIAL TRANSFER TIMING

Three-line Serial I/O Mode:



RECOMMENDED OSCILLATORS

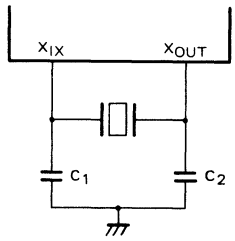
Main System Clock: Ceramic Oscillator

Manufacturer	Product name	External capacitor (pf)		Oscillation voltage (V)		Remarks
		C1	C2	MIN.	MAX.	
Murata Mfg	CSA3.58MG	30	30	2.0	6.0	
	CSA4.00MG	30	30	2.0	6.0	
	CSA4.19MG	30	30	2.0	6.0	
	CST3.58MGW	none	none	2.0	6.0	C contained type
	CST4.00MGW	none	none	2.0	6.0	
	CST4.19MGW	none	none	2.0	6.0	
Kyocera	KBR3.58MS	33	33	2.0	6.0	
	KBR4.0MS	33	33	2.0	6.0	
	KBR4.19MS	33	33	2.0	6.0	
Toko	CRHF4.00	18	18	2.0	6.0	
Dai-Shinku	PRS0400BCSAN	39	33	2.0	6.0	

Main System Clock: Crystal Oscillator

Manufacturer	Frequency (MHz)	Retainer	External Capacitor (pf)		Oscillation voltage (V)		Remarks
			C1	C2	MIN.	MAX.	
Kinseki	4.0	HC-49U-S	22	22	2.0	6.0	

OSCILLATOR CIRCUIT



4-BIT SINGLE-CHIP MICROCONTROLLER

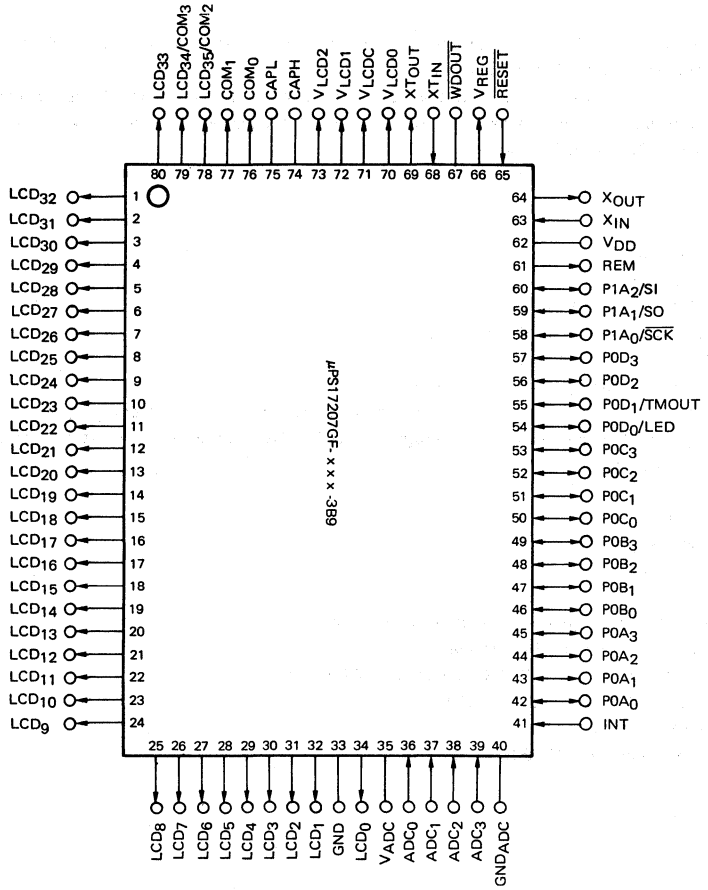
The μP17207 is a 4-bit single-chip microcontroller for infrared remote controller containing the LCD controller/driver, A/D converter, and the remote control carrier generator.

The μPD17207 employs the 17K architecture. Therefore, data transfer or operation within the data memory or between the data memory and peripheral circuit is possible by single instruction. All instructions are 16-bit one word instructions. The μPD17207 is packaged in 80-pin plastic QFP.

FEATURES

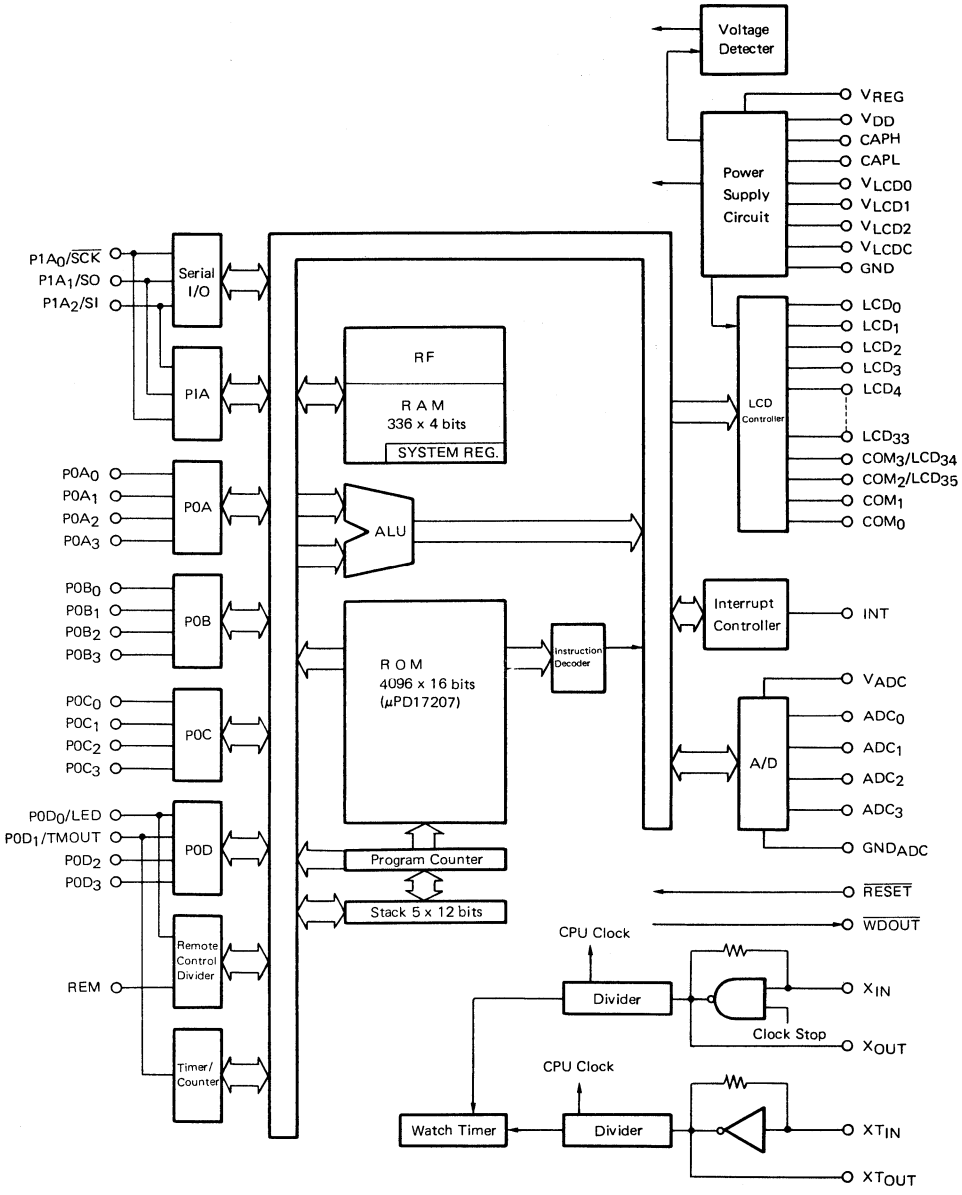
- Program memory (ROM)
  μPD17207: 4096 x 16 bits
- Data memory (RAM): 336 x 4 bits)
- Built-in infrared remote control carrier generator
- Built-in 8-bit A/D converter: 4 inputs
- Built-in LCD controller/driver (136 segments max.)
  Common pins: 4, Segments pins: 34 (2 of the common pins can be used as segment pins)
- LCD drive voltage boosting circuit with voltage regulator: LCD drive voltage can be boosted up to 2.4 to 5.4 V, using the external resistor
- Abundant I/O ports pins: 19
- Built-in 3-line serial interface
- Stack levels: 5 levels
- 8-bit timer: 1 channel
- Clock timer: 1 channel
- Instruction execution time: 4 μs (with 4 MHz resonator connected)
- Standby functions: STOP mode, HALT mode
  Clock display is possible with 32.768 kHz crystal in STOP mode
- Can operate at low voltage: V_{DD} = 2.2 to 5.5 V
- 80-pin plastic QFP (14 x 20 mm)
- One-time PROM versions: μPD17P207GF-3B9

PIN CONFIGURATION (Top View)



$P0A_0$-$P0A_3$	:	Input/output port
$P0B_0$-$P0B_3$	:	Input/output port
$P0C_0$-$P0C_3$	:	Input/output port
$P0D_0$-$P0D_3$	:	Input/output port
$P1A_0$-$P1A_2$	:	Input/output port
LED	:	Remote control transmission output indication
REM	:	Remote control transmission output
LCD_0-LCD_{35}	:	LCD segment signal output
COM_0-COM_3	:	LCD common signal output
TMOUT	:	Timer output
$\overline{WDOUT}$	:	Watchdog timer output
$\overline{INT}$	:	External interrupt input
$\overline{RESET}$	:	Reset signal input
ADC_0-ADC_3	:	A/D converter input
X_{IN}, X_{OUT}	:	Main clock oscillator circuit
XT_{IN}, XT_{OUT}	:	Subclock oscillator circuit
SI	:	Serial data input
SO	:	Serial data output
$\overline{SCK}$	:	Serial clock input/output
V_{LCDC}	:	LCD drive reference voltage adjustment
V_{LCD0}-V_{LCD2}	:	LCD drive reference voltage output
CAPH, CAPL	:	Booster capacitor connection pins
V_{REG}	:	Subclock voltage regulator output
V_{ADC}	:	A/D converter reference voltage input
V_{DD}	:	Power supply pin
GND, GND_{ADC}	:	Ground

BLOCK DIAGRAM



FUNCTION LIST

Product	μPD17201A	μPD17207	μPD17P207
ROM	3072 x 16 bits	4096 x 16 bits	
	Mask ROM	Mask ROM	One-time PROM
RAM	336 x 4 bits		
Instruction execution time	4 μs (with 4 MHz resonator connected)		
Stack level	5 levels (Multiple interrupt: up to 2 levels)		
Input/output ports	19		
Serial interface	• 8-bit, 3-line: 1 channel		
Interrupts	• 4 channels External interrupts: 1 channel Internal interrupts: 3 channels		
Timers	• 2 systems 8-bit timer Clock timer (also serves as watchdog timer)		
Standby functions	• STOP mode, HALT mode		
Operating voltage	V_{DD}=2.2 to 5.5 V		
Package	80-pin plastic QFP (14 x 20 mm)		

μPD17P207 is a model of μPD17207 which is equipped with a one-time PROM in place of the μPD17207 internal mask ROM.

Sice the user can write the program to μPD17P207, the microcontroller is suitable for experimental or small-scale production of μPD17207 systems.

It is recommended that you also read the documents related to μPD17207, in addition to this data sheet.

FEATURES

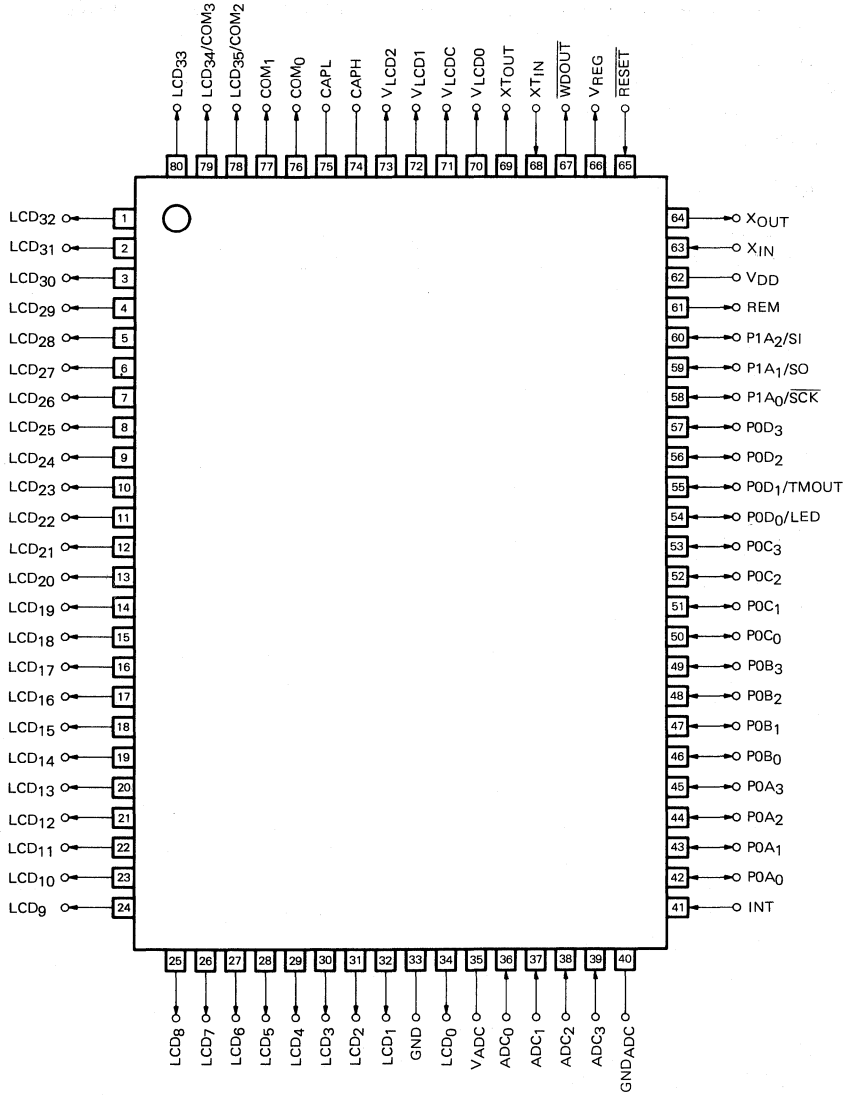
- Compatible with μPD17207
- Internal one-time PROM: 4096 x 16 bits
- Operating voltage range: 2.2 to 5.5 V

ORDERING INFORMATION

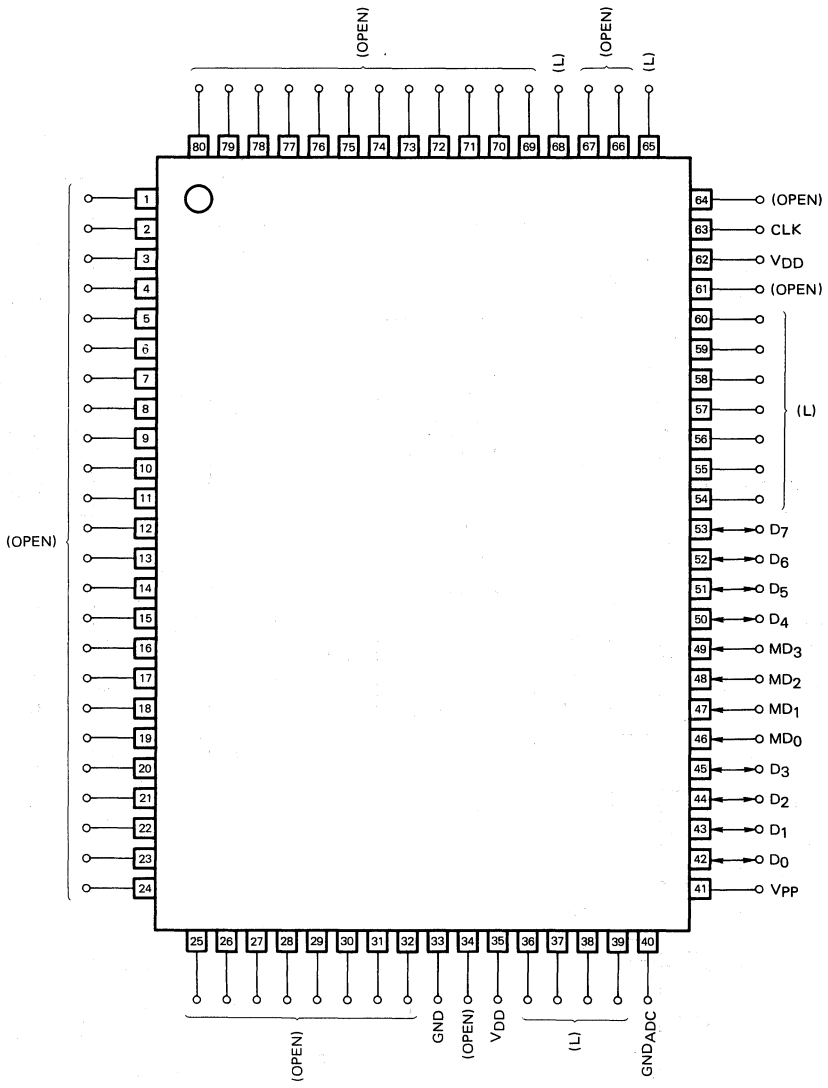
Order Code	Package	Quality Grade
μPD17P207GF-3B9	80-pin-plastic QFP (14 x 20)	Standard

PIN CONFIGURATION (Top View)

(1) Ordinary operation

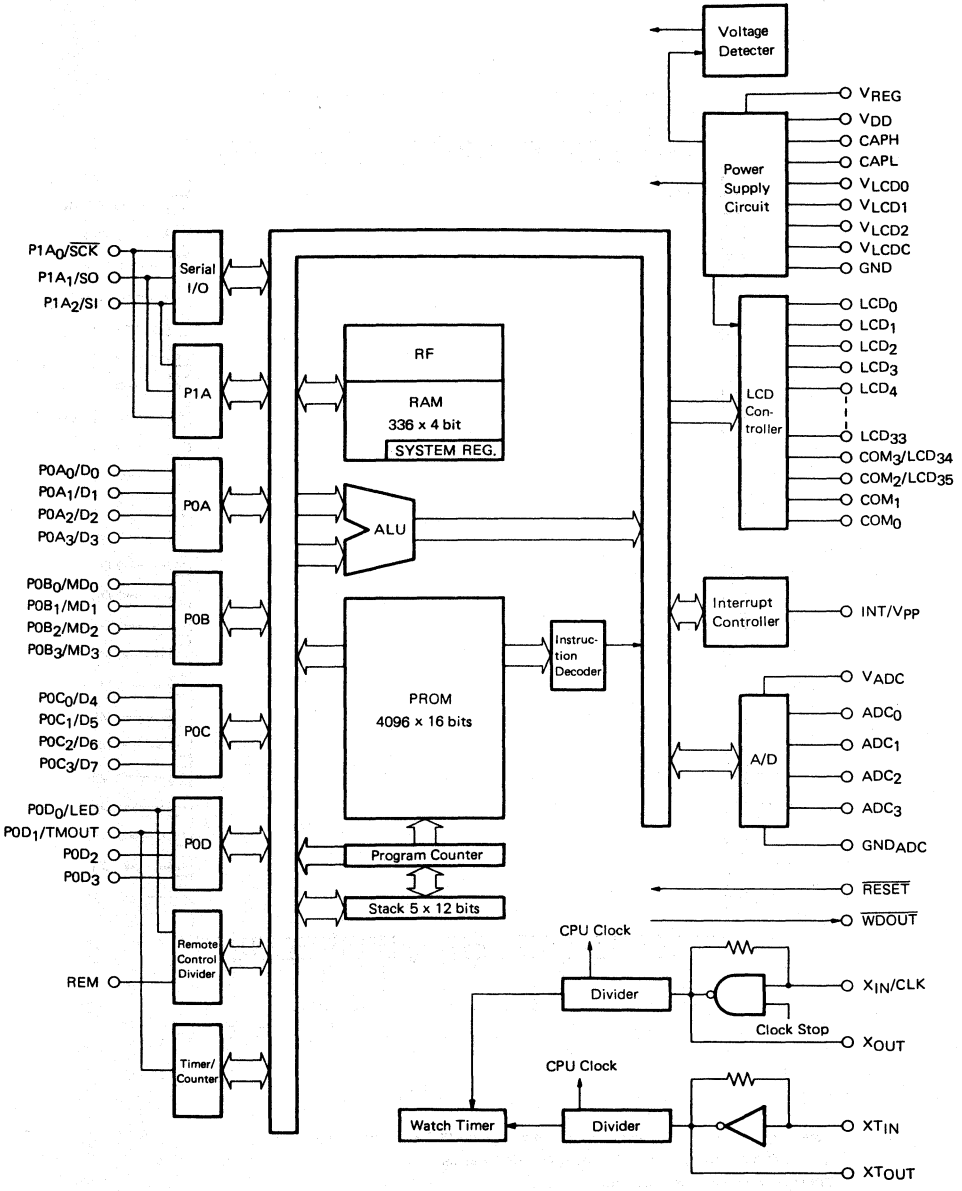


(2) In PROM programming mode



Note : ( ) indicates processing for pins not used in the PROM programming mode.
L : Ground each of these pins through a 470 Ω resistor.
OPEN : Do not connect these pins.

BLOCK DIAGRAM



1. PIN FUNCTIONS

1.1 IN ORDINARY OPERATION MODE

Pin No.	Symbol	I/O	Output format	Pin name	Function
78 79 80 1 32 34	LCD_{35}/COM_2 LCD_{34}/COM_3 LCD_{33} LCD_{32} LCD_1 LCD_0	Output		LCD segment signal	These are the segment signal output pins for the LCD driver. LCD_{35}/COM_2 and LCD_{34}/COM_3 pins are multiplexed pins equipped with segment signal output and common signal output functions. Whether the segment signal output function or common signal output function is selected is specified by LCDMD3 through LCDMD0 (address 32H, bits 3-0) of the register file. The number of display dots can be selected by the matrix of segment signal output pins and common signal output pins from 72, 105, or 136 dots. The bias is fixed to 1/3. Duty factors of 1/2, 1/3, and 1/4 can be selected, depending on the selected number of common signal output pins. The frame frequency can be selected by LCDCK2-LCDCK0 registers (address 31H) for the register file. The dot corresponding to a segment signal output pin and a common signal output pin, between which a potential difference of $+V_{DD}$ is generated illuminates. Display data are set in the LCD driver through LCD display register (address 40H-63H of BANK0). The display ON mode and display OFF mode for the LCD driver are selected by the LCDEN register (address 31H, bit 3) for the register file. In the display OFF mode, the segment signal output pin outputs a signal waveform that extinguishes the display. When reset is effected by the $\overline{RESET}$ pin, the voltage detector detecting a voltage drop, or the watchdog timer, the LCDEN register is set in the display OFF mode.
33	GND	–	–	Ground	Device ground pin
35	V_{ADC}	–	–	Analog power	This pin supplies power to the A/D converter. Connect this pin to the V_{DD} pin.

Pin No.	Symbol	I/O	Output format	Pin name	Function
36	ADC_0	Input		A/D converter input 0	These pins are input pins for the 8-bit A/D converter, which can function as either an 8-bit A/D converter or a comparator, depending on the settings used in VREFEN, ADCEN, ADCCH1, and ADCCH0 (address 21H), for the register file. The A/D converter is of successive approximation type. The reference voltage for the converter is created by dividing the voltage of an analog power supply (V_{ADC} pin) with a registor string. The A/D converter can use a total of six channels, formed by pins ADC_0 through ADC_3. The comparator is provided with a total of two channels with one channel consisting of pins ADC_0 and ACD_2 and the other of pin ADC_1 and pin ADC_3. Whether the A/D converter or comparator is used, and which channel is selected, are specified by VREFEN, ADCEN, ADCCH1, and ADCCH0 (address 21H), for the register file.
37	ADC_1	Input		A/D converter input 1	
38	ADC_2	Input		A/D converter input 2	
39	ADC_3	Input		A/D converter input 3	
40	GND_{ADC}	–	–	Analog ground	This is the ground pin for the A/D converter.
41	INT	Input	–	Interrupt	This pin inputs an external interrupt request signal. The interrupt request is issued at the rising edge of the signal input to this pin. Even when an interrupt request has been issued, the interrupt is not accepted unless it is enabled (maskable interrupt). All interrupts can be enabled by the EI instruction, or only a selected interrupt can be enabled by the INT pin. Enabling an interrupt by the INT pin is specified by IP (address 2FH) for the register file. If an interrupt is enabled, and when an interrupt request is issued, the interrupt is accepted. When an interrupt has been accepted, the program is executed, starting from address 03H. Whether an interrupt request has been issued can be checked by IRQ (address 3FH) for the register file, even when the interrupt is not enabled. When reset is effected by the $\overline{RESET}$ pin or watchdog timer, all interrupts are disabled and all interrupt requests are cleared.
42	POA_0	I/O	CMOS push-pull	Port 0A	These pins constitute a 4-bit general-purpose I/O port, which can be set in the input or output mode in 4 bit units (group I/O) by P0AGIO (address 37H, bit 0) for the register file. The input data is read and output data is set by port register P0A (address 70H for BANK0). These port pins are internally connected with pull-up resistors. When reset is effected by the $\overline{RESET}$ pin or watchdog timer, these pins are set in the input mode.
43	POA_1				
44	POA_2				
45	POA_3				

Pin No.	Symbol	I/O	Output format	Pin name	Function
46 47 48 49	$P0B_0$ $P0B_1$ $P0B_2$ $P0B_3$	I/O	N-ch open drain	Port 0B	These pins constitute a 4-bit general-purpose I/O port, which can be set in the input or output mode in 4 bit units (group I/O) by P0BGIO (address 37H, bit 1). The input data is read or output data is set by port register P0B (address 71H for BANK0). Since these pins are N-ch open-drain, they must be connected to external pull-up resistors. When reset is effected by the $\overline{RESET}$ pin or watch-dog timer, these pins are set in the input mode.
50 51 52 53	$P0C_0$ $P0C_1$ $P0C_2$ $P0C_3$	I/O	N-ch open drain	Port0C	These pins constitute a 4-bit general-purpose I/O port, which can be set in the input or output mode in 4-bit units (group I/O) by P0CGIO (address 37H, bit 2). The input data is read and output data is set by port register P0C (address 72H for BANK0). Since these pins are N-ch open-drain, they must be connected with pull-up registors. When reset is effected by the $\overline{RESET}$ pin or watch-dog timer, these pins are set in the input mode.
54 55 56 57	$P0D_0$/LED $P0D_1$/TMOUT $P0D_2$ $P0D_3$	I/O	CMOS push-pull	Port 0D	These pins constitute a 4-bit general-purpose I/O port. Of these four pin, P0D0 also function as an LED output pin (LED), and P0D1 serves as the external signal output pin for the timer (TMOUT). Whether the port pin, LED output, or timer output function is used is specified by NRZEN (address 23H,bit 2) and TMOE (address 23H,bit 1) for the register file. When reset is effected by the $\overline{RESET}$ pin or watch-dog timer, these pins are set in the input mode. (1) When 4-bit I/O port function is used The port can be set in the input or output mode bitwise (bit I/O) by P0DBIO3 through P0DBIO0 (address 27H, bits 3 through 0) for the register file. The input data is read or output data is set by port register P0D (address 73H for BANK0). (2) When $P0D_0$ pin is used as LED output pin Whether this pin functions as an I/O port pin ($P0D_0$) or LED output pin is specified by NRZEN. As an LED output pin, NRZ signal is output in synchronization with REM output. (3) When $P0D_1$ pin is used as external signal output pin for 8-bit timer Whether this pin functions as an I/O port pin ($P0D_1$) or timer output pin is specified by TMOE.

Pin No.	Symbol	I/O	Output format	Pin name	Function
58 59 60	P1A$_0$/$\overline{SCK}$ P1A$_1$/SO P1A$_2$/SI	I/O	CMOS push-pull	Port1A	These pins constitute a 3-bit general-purpose I/O port. They also form a serial interface. Whether these pins function as port pins or serial interface pins can be specified by SIOEN (address 23H, bit 0) for the register file. When RESET is effected by the $\overline{RESET}$ pin or watchdog timer, these pins are set in the input mode. (1) When used as 3-bit I/O port The port can be set in the input or output mode in 3 bit units (group I/O) by P1AGIO (address 37H, bit 3) for the register file. The input data can be read or output data can be set by port register P1A (address 70H of BANK1). (2) When used as serial interface The serial interface (μCOM standard mode) function for these pins is selected by SIOEN.
61	REM	Output	CMOS push-pull	Remote controller transmission output	This pin outputs an infrared remote controller signal. The carrier frequency can be set from 16 to 1,024 kHz.
62	V_{DD}			Power	Device power supply
63 64	X_{IN} X_{OUT}	Input Output		Main clock oscillation	Connect a 4 MHz ceramic/crystal oscillator across these pins.
65	$\overline{RESET}$	Input		Reset	This pin inputs a system reset signal. The system is reset, when a lower-level signal is input to this pin for 50 μs or longer.
66	V_{REG}	Output		Voltage regulator output	This is the output pin for the voltage regulator. Connect an external 0.1 μF capacitor to this pin.
67	$\overline{WDOUT}$	Output	CMOS push-pull	Watchdog output	This pin goes low, when overrunning, such as watchdog timer operation and stack overflow, is detected.
68 74	XT_{IN} XT_{OUT}	Input Output		Subclock oscillation	Connect a 32 kHz crystal oscillator across these pins.
71	V_{LCDC}	Output		LCD drive reference voltage adjustment	This pin adjusts the reference voltage for the LCD driver. Connect variable resistors for reference voltage adjustment between V_{LCD0} and V_{LCDC}, and between V_{LCDC} and GND.
70 72 73	V_{LCD0} V_{LCD1} V_{LCD2}	Output		LCD drive reference voltage output	These pins output the reference voltages for the LCD driver. V_{LCD0} outputs the reference voltage, V_{LCD1} outputs a voltage two times the reference voltage (doubler output), and V_{LCD2} outputs a voltage three times the reference voltage (tripler output). Connect variable resitors for reference voltage adjustment between V_{LCD0} and V_{LCDC}, and between V_{LCDC} and GND. In addition, connect a 0.47 μF capacitors between V_{LCD0} and V_{LCD1}, and V_{LCD2} and GND.
74 75	CAPH CAPL			Voltage raising capacitor	Connect a 0.47 μF capacitor, to raise the voltage across these pins.

Pin No.	Symbol	I/O	Output format	Pin name	Function
76 77	COM_0 COM_1	Output	CMOS	Common signal	These pins output the common signals from the LCD driver. In addition, LCD_{35}/COM_2 and LCD_{34}/COM_3 pins can also be used as common signal output pins. Whether the segment signal output function or common signal output function is selected is specified by LCDMD0 and LCDMD1 registers (address 32H) for the register file. The number of display dots can be selected by the matrix of segment signal output pins and common signal output pins, from 72, 105, or 136 dots. The bias is fixed to 1/3. Duty factors of 1/2, 1/3, and 1/4 can be selected, depending on the selected number of common signal output pins. The frame frequency can be selected by LCDCK0 and LCDCK1 registers (address 31H) for the register file. The dot corresponding to a segment signal output pin and a common signal output pin, between which a potential difference of $+V_{DD}$ is generated, illuminates. The display ON mode and display OFF mode for the LCD driver are selected by the LCDEN register (address 31H) for the register file. In the display OFF mode, the common signal output pin outputs a signal waveform that extinguishes the display. When reset is effected by the $\overline{RESET}$ pin, the voltage detector, upon detecting a voltage drop, for the watchdog timer, the LCDEN register is set in the display OFF mode.

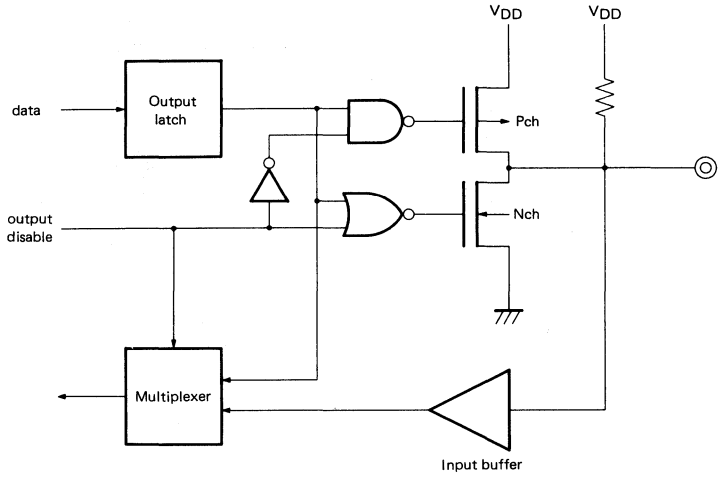
1.2 IN PROM PROGRAMMING MODE

Pin name	I/O	Shared by:	Function	At reset
CLK	Input	X_{IN}	Address updating clock input pin	–
D0 to D3	I/O	$P0A_0$ to $P0A_3$	8-bit data I/O pin	Input
D4 to D7		$P0C_0$ to $P0C_3$		
MD0 to MD3	Input	$P0B_0$ to $P0B_3$	Operation mode selector pins	Input
V_{PP}	–	INT	Apply the program voltage (12.5 V) to this pin. In the ordinary operation mode, this pin is used as the INT pin.	–

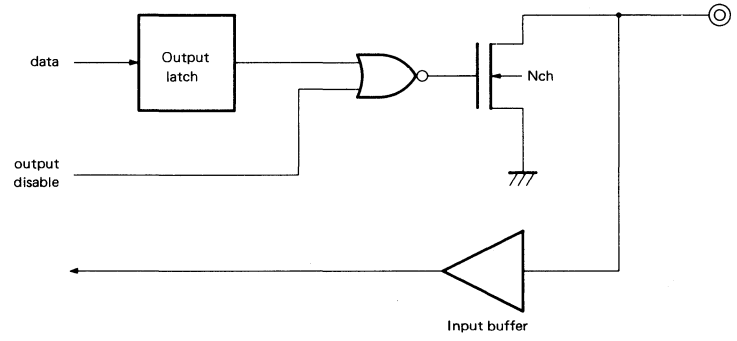
1.3 I/O CIRCUITS

The simplified I/O circuits schematic views for μPD17P207 pins are presented below.

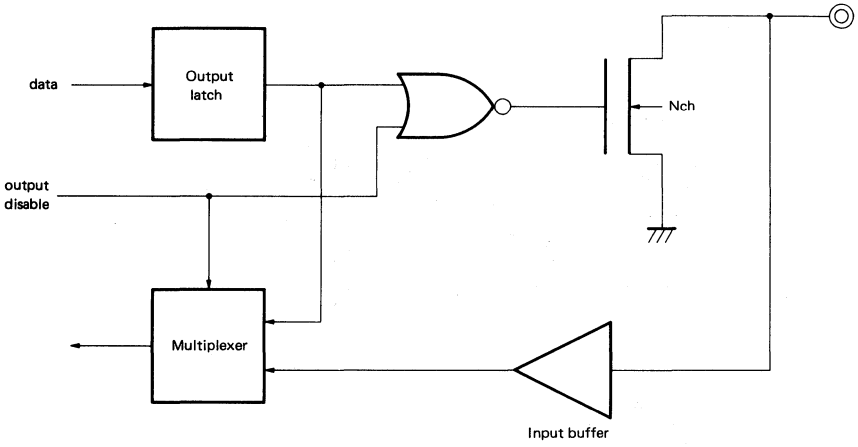
(1) POA_0 to POA_3



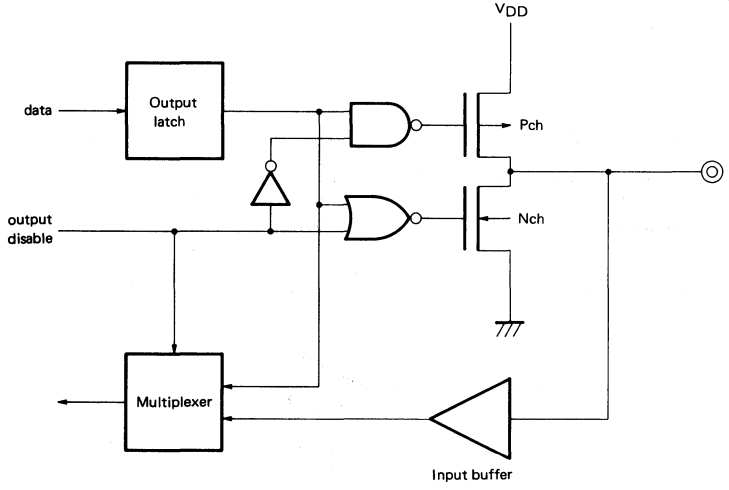
(2) POB_0 to POB_3



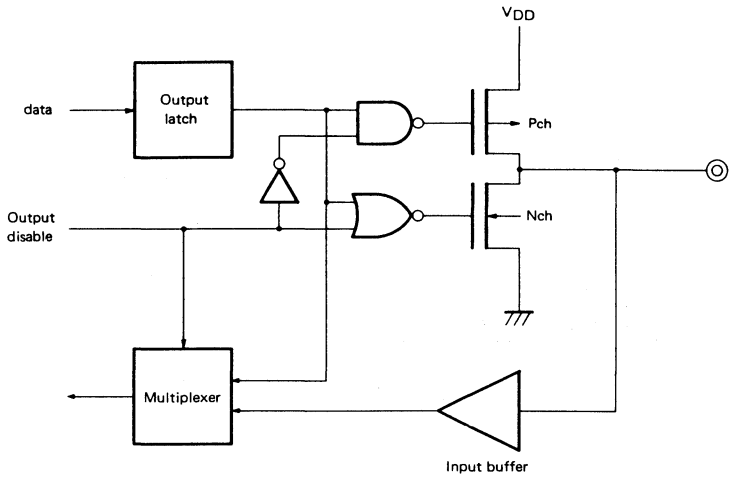
(3) POC_0 to POC_3



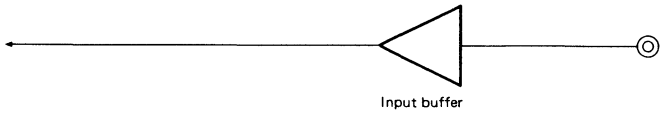
(4) POD_0 to POD_3



(5) $P1A_0$ to $P1A_2$



(6) $\overline{RESET}$



2. WRITING, READING, AND VERIFYING ONE-TIME PROM (PROGRAM MEMORY)

When the PROM is to be written, read, or verified, μPD17P207 is set in the PROM mode, and the pins shown in Table 2-1 are used.

No address has to be input. Instead, the address is incremented by the clock input from the CLK pin.

Table 2-1 Pins Used to Write/Read/Verify Program Memory

Pin name	Function
V_{PP}	Apply program voltage (12.5 V) to this pin. This pin is used as INT pin in ordinary operation mode.
CLK	Address incrementing clock input pin.
MD_0 to MD_3	Operation mode selector pins.
D_0 to D_7	8-bit I/O pins.
V_{DD}	Apply operating voltage (6 V) to this pin. Apply 2.2 to 5.5 V in ordinary operation mode.

2.1 OPERATION MODES FOR PROGRAM MEMORY WRITE, READ, AND VERIFY

μPD17P207 is set in the program memory write, read, or verify mode, when +6 V is applied to pin V_{DD}, and +12.5 V is applied to pin V_{PP}, after being placed in the reset status (V_{DD} = 5 V, $\overline{RESET}$ = low level) for a certain period of time.

The operation modes, selected by pins MD0 through MD3, are listed in Table 2-2.

Any pins not used to write, read, or verify the program memory must be grounded through pull-down resistors (470 Ω).

Table 2-2 Operation Modes for Program Memory Write, Read, and Verify

Operation mode selection						Operation mode
V_{PP}	V_{DD}	MD0	MD1	MD2	MD3	
+12.5 V	+6 V	H	L	H	L	Program memory address 0 clear
		L	H	H	H	Write mode
		L	L	H	H	Read, verify mode
		H	x	H	H	Program inhibit mode

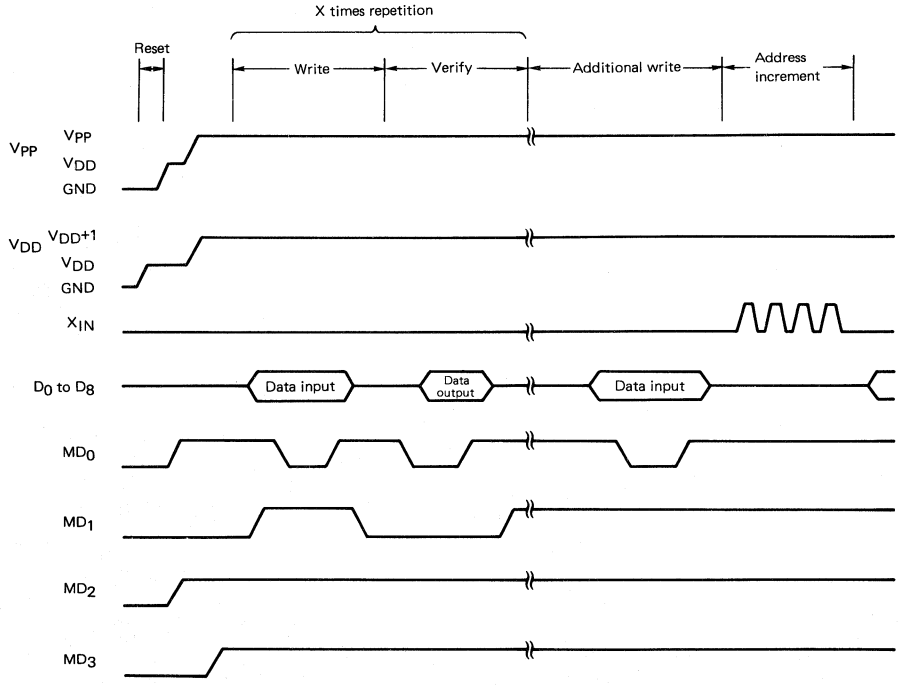
Remarks: x: L or H

2.2 PROGRAM MEMORY WRITING PROCEDURE

Write the program memory by following these steps. The program memory can be written at high speeds.

(1) Pull down the unused pins to the ground potential through resistors. Make the pin CLK low.
(2) Apply 5 V to pin V_{DD}. Make pin V_{PP} low.
(3) Wait for 10 μs. Then, apply 5 V to pin V_{PP}.
(4) Set the program memory address 0 clear mode by the mode selector pins.
(5) Apply 6 V to pin V_{DD}, and 12.5 V to pin V_{PP}.
(6) Program inhibit mode
(7) Write data in the 1 ms write mode.
(8) Program inhibit mode
(9) Verify mode. Proceed to (10), if the memory has been written. If it has not been written, repeat (7) through (9).
(10) Additional writing for (the number of times (7) through (9) are repeated: X) x 1 ms
(11) Program inhibit mode
(12) Input a pulse four times to pin CLK, in order to increment the program memory address (by one).
(13) Repeat (7) through (12), until the last address is programmed.
(14) Program memory address 0 clear mode
(15) Decrease the voltages on pin V_{DD} and V_{PP} to 5 V.
(16) Turn power off.

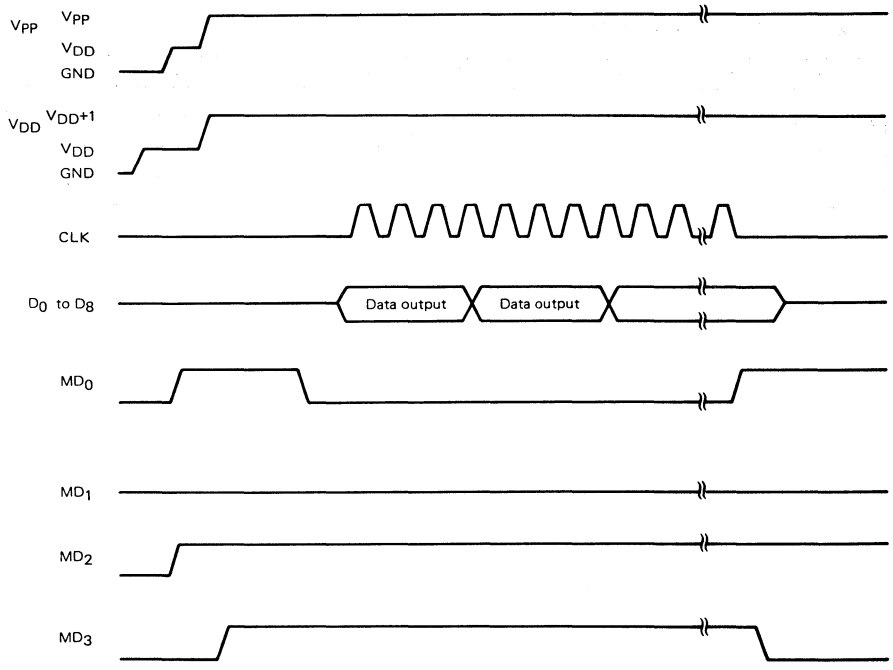
The following figure illustrates steps (2) through (12) above.



2.3 PROGRAM MEMORY READING PROCEDURE

(1) Pull down the unused pins to the ground potential through resistors. Make the pin CLK low.
(2) Apply 5 V to pin V_{DD}. Make pin V_{PP} low.
(3) Wait for 10 μs. Then, apply 5 V to pin V_{PP}.
(4) Set the program memory address 0 clear mode by the mode selector pins.
(5) Apply 6 V to pin V_{DD}, and 12.5 V to pin V_{PP}.
(6) Program inhibit mode
(7) Verify mode. The data for each address is output on a one-by-one basis in a cycle during which the clock pulse is input to pin CLK four times.
(8) Program inhibit mode
(9) Program memory address 0 clear mode
(10) Decrease the voltages on pin V_{DD} and V_{PP} to 5 V.
(11) Turn power off.

The following figure illustrates steps (2) through (9) above.



3. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage	V_{DD}		−0.3 to +7.0	V
Input Voltage	V_I	P0B0-P0P3	−0.3 to V_{DD}+0.3	V
		All pins, except P0B0-P0P3	−0.3 to V_{DD}+0.3	V
Operating Temperature	T_{opt}		−20 to +75	°C
Storage Temperature	T_{stg}		−40 to +125	°C

CAPACITANCE (T_a = 25 °C, V_{DD} = 0 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Input Capacitance	C_{IN}			10	pF	Pins INT, SI, $\overline{RESET}$
	C_{PIN}			10	pF	Other than pins INT, SI, $\overline{RESET}$

RECOMMENDED OPERATING RANGE

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Supply Voltage	V_{DD1}	2.2	3.0	5.5	V	f_X = 4 MHz
	V_{DD2}	3.5	5.0	5.5	V	f_X = 8 MHz
Main Clock Oscillation Frequency	f_X	2.0	4.0	8.0	MHz	
Subclock Oscillation Frequency	f_{XT}		32.768		kHz	

DC CHARACTERISTICS (V_{DD}=2.2 to 5.5 V, T_a=−20 to +75 °C, f_X=4 MHz, f_{XT}=32 kHz)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS	
Operating Supply Voltage	V_{DD}	2.2	3.0	5.5	V		
High-Level Input Voltage	V_{IH1}	2.4			V	$\overline{RESET}$ pin	
	V_{IH2}	2.1			V	Other than $\overline{RESET}$ pin	
Low-Level Input Voltage	V_{IL1}			0.6	V	$\overline{RESET}$ pin	
	V_{IL2}			0.9	V	Other than $\overline{RESET}$ pin	
High-Level Input Current	I_{IH1}			0.2	μA	INT pin	V_{IH} = 3.0 V
	I_{IH2}			0.2	μA	$\overline{RESET}$ pin	V_{IH} = 3.0 V
	I_{IH3}			0.2	μA	P0A-P1A pin	V_{IH} = 3.0 V
Low-Level Input Current	I_{IL1}			0.2	μA	INT pin	V_{IL} = 0 V
	I_{IL2}			0.2	μA	$\overline{RESET}$ pin	V_{IL} = 0 V w/o pull-up resistor
	I_{IL3}	20	50	100	μA		V_{IL} = 0 V w/pull-up resistor
	I_{IL4}			0.2	μA	P0A pin	V_{IL} = 0 V w/o pull-up resistor
	I_{IL5}	6	12	20	μA		V_{IL} = 0 V w/pull-up resistor
	I_{IL6}			0.2	μA	P0B, P0C, P0D, P1A pin	V_{IL} = 0 V
High-Level Output Current	I_{OH1}	0.6	2.0	4.0	mA	P0A, P0D, P1A pin	V_{OH} = 2.7 V
	I_{OH2}	7.0	15.0	25.0	mA	REM pin	V_{OH} = 1.0 V
Low-Level Output Current	I_{OL1}	0.5	1.5	2.5	mA	P0A, P0D, P1A pin	V_{OL} = 0.3 V
	I_{OL2}	0.5	1.5	2.5	mA	P0B, P0C pin	V_{OL} = 0.3 V
	I_{OL3}	0.5	1.5	2.5	mA	REM pin	V_{OL} = 0.3 V
Supply Current	I_{DD1}	0.2	0.5	1.5	mA	Operation mode	Both XT and X oscillate
	I_{DD2}		15	30	μA		Only XT oscillates
	I_{DD3}		0.5	1.5	mA	HALT mode	Both XT and X oscillate
	I_{DD4}		10	15	μA		Only XT oscillates
LCD Output Voltage Variable Range	V_{LCD0}	0.6		1.8	V		
Doubler Output Voltage	V_{LCD1}	1.9 V_{LCD0}	2 V_{LCD0}		V		
Tripler Output Voltage	V_{LCD2}	2.85 V_{LCD0}	3 V_{LCD0}		V		
Common Output Current	I_{COM}	30			μA	V_{DS} = 0.2 V	
Segment Output Current	I_{LCD}	5			μA	V_{DS} = 0.2 V	
Low-Voltage Detection Voltage 1	V_{DET1}	1.6	2.0	2.5	V		
Low-Voltage Detection Voltage 2	V_{DET2}	1.9	2.2	2.9	V		

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
A/D Converter Current Dissipation	I_{DD5}		60	120	μA	V_{ADC} = 3 V
A/D Converter Absolute Accuracy			±1	±2	LSB	V_{ADC} = 3 V

AC CHARACTERISTICS (T_a = −20 to +75 °C, V_{DD} = 2.2 to 5.5 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Main Clock Oscillation Frequency	f_X	2.0		4.0	MHz	V_{DD} = 2.2 to 5.5 V
		2.0		8.0	MHz	V_{DD} = 3.5 to 5.5 V
Subclock Oscillation Frequency	f_{XT}		32.768		kHz	
INT Input High-Level Width	t_{INTH}	50			μs	
$\overline{RESET}$ Low-Level Width	t_{RSL}	50			μs	

RECOMMENDED OSCILLATOR

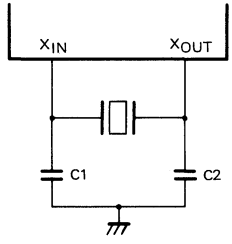
MAIN SYSTEM CLOCK: CERAMIC OSCILLATORS

Manufacturer	Product name	External capacitance (pF)		Oscillation voltage range (V)		Remarks
		C1	C2	MIN.	MAX.	
Murata Mfg	CSA3.58MG	30	30	2.0	6.0	
	CSA4.00MG	30	30	2.0	6.0	
	CSA4.19MG	30	30	2.0	6.0	
	CST3.58MGW	unnecessary	unnecessary	2.0	6.0	C-contained type
	CST4.00MGW	unnecessary	unnecessary	2.0	6.0	
	CST4.19MGW	unnecessary	unnecessary	2.0	6.0	
Kyocera	KBR3.58MS	33	33	2.0	6.0	
	KBR4.00MS	33	33	2.0	6.0	
	KBR4.19MS	33	33	2.0	6.0	
Toko	CRHF4.00	18	18	2.0	6.0	
Dai-Shinku	PRS0400BCSAN	39	33	2.0	6.0	

MAIN SYSTEM CLOCK: CRYSTAL OSCILLATOR

Manufacturer	Frequency (MHz)	Retainer	External capacitance (pF)		Oscillation voltage range (V)		Remarks
			C1	C2	MIN.	MAX.	
Kinseki	4.0	HC-49U-S	22	22	2.0	6.0	

Oscillator

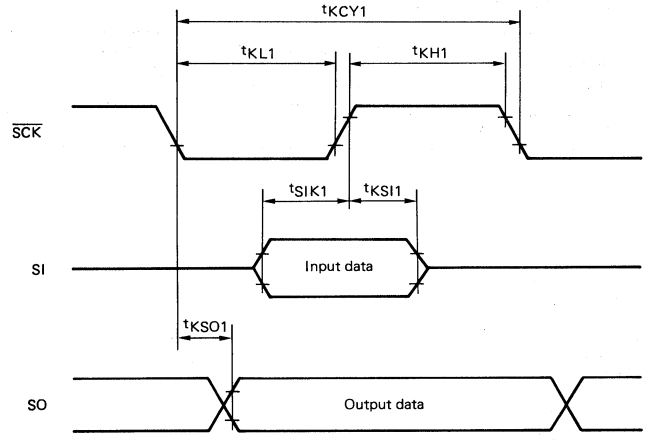


SERIAL INTERFACE AC CHARACTERISTICS (T_a = −20 to +75 °C, V_{DD} = 2.2 to 5.5 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS	
$\overline{SCK}$ Cycle Time	t_{KCY}	2.0			μs	V_{DD} = 4.5 to 5.5 V	Data input
		10.0			μs		Data output
		5.0			μs		Data input
		13.0			μs		Data output
$\overline{SCK}$ Low-Level Width	t_{KH}, t_{KL}	1.0			μs	V_{DD} = 4.5 to 5.5 V	Data input
		5.0			μs		Data output
		2.5			μs		Data input
		6.5			μs		Data output
SI Setup Time (vs. $\overline{SCK}$ ↑)	t_{SIK}	100			ns		
SI Hold Time (vs. $\overline{SCK}$ ↑)	t_{KS}	100			ns		
$\overline{SCK}$ ↓ → SO Output Delay Time	t_{KSO}			4.5	μs	C_L = 100 pF	

SERIAL TRANSFER TIMING

3-line serial I/O mode:



DC PROGRAMMING CHARACTERISTICS (T_a = 25 °C, V_{DD} = 6.0±0.25 V, V_{PP} = 12.5±0.5 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
High-Level Input Voltage	V_{IH1}	0.7 V_{DD}		V_{DD}	V	Other than CLK
	V_{IH2}	V_{DD}-0.5		V_{DD}	V	CLK
Low-Level Input Voltage	V_{IL1}	0		0.3 V_{DD}	V	Other than CLK
	V_{IL2}	0		0.4	V	CLK
Input Leakage Current	I_{L1}			10	μA	V_{IN} = V_{IL} or V_{IH}
High-Level Output Voltage	V_{OH}	V_{DD}-1.0			V	I_{OH} = −1 mA
Low-Level Output Voltage	V_{OL}			0.4	V	I_{OL} = 1.6 mA
V_{DD} Supply Current	I_{DD}			30	mA	
V_{PP} Supply Current	I_{PP}			30	mA	MD0 = V_{IL}, MD1 = V_{IH}

Note 1: Keep V_{PP} to below +13.5 V, including the overshoot.

2: Apply V_{DD} before V_{PP}, and remove V_{DD} after V_{PP}.

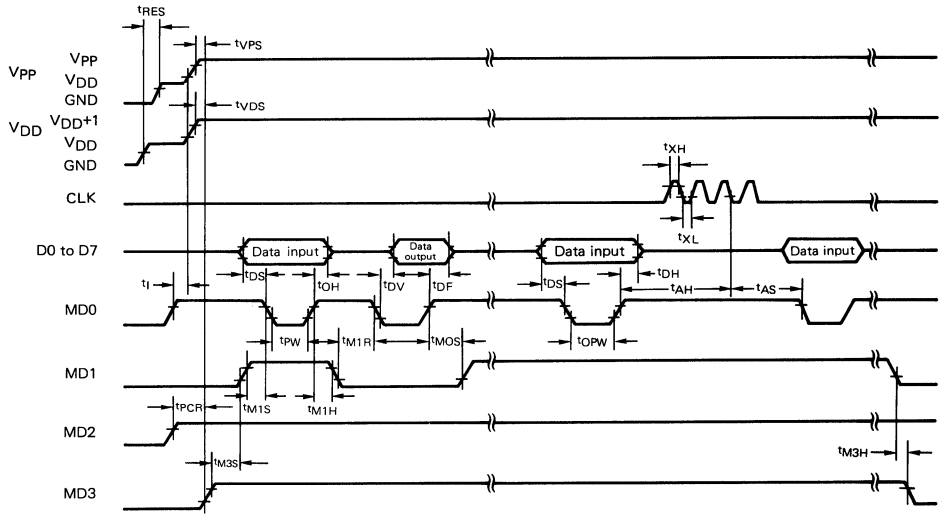
AC PROGRAMMING CHARACTERISTICS (T_a = 25 °C, V_{DD} = 6.0±0.25 V, V_{PP} = 12.5±0.5 V)

CHARACTERISTICS	SYMBOL	*1	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Address Setup Time*2 (vs. MD0 ↓)	t_{AS}	t_{AS}	2			μs	
MD1 Setup Time (vs. MD0 ↓)	t_{M1S}	t_{OES}	2			μs	
Data Setup Time (vs. MD0 ↓)	t_{DS}	t_{DS}	2			μs	
Address Hold Time*2 (vs. MD0 ↑)	t_{AH}	t_{AH}	2			μs	
Data Hold Time (vs. MD0 ↑)	t_{DH}	t_{DH}	2			μs	
MD0 ↑→ Data Output Float Delay Time	t_{DF}	t_{DF}	0		130	μs	
V_{PP} Setup Time (vs. MD3 ↑)	t_{VPS}	t_{VPS}	2			μs	
V_{DD} Setup Time (vs. MD3 ↑)	t_{VDS}	t_{VCS}	2			μs	
Initial Program Pulse Width	t_{PW}	t_{PW}	0.95	1.0	1.05	ms	
Additional Program Pulse Width	t_{OPW}	t_{OPW}	0.95		21.0	ms	
MD0 Setup Time (vs. MD1 ↑)	t_{MOS}	t_{CES}	2			μs	
MD0 ↓→ Data Output Delay Time	t_{DV}	t_{DV}			1	μs	MD0 = MD1 = V_{IL}
MD1 Hold Time (vs. MD0 ↓)	t_{M1H}	t_{OEH}	2			μs	$t_{M1H} + t_{M1R} \geqq 50$ μs
MD1 Recovery Time (vs. MD0 ↓)	t_{M1R}	t_{OR}	2			μs	
Program Counter Reset Time	t_{PCR}	–	10			μs	
CLK Input High-Low-Level Width	t_{XH}, t_{XL}	–	0.125			μs	
CLK Input Frequency	f_X	–			4	MHz	
Initial Mode Set Time	t_I	–	2			μs	
MD3 Setup Time (vs. MD1 ↑)	t_{M3S}	–	2			μs	
MD3 Hold Time (vs. MD1 ↓)	t_{M3H}	–	2			μs	
MD3 Setup Time (vs. MD0 ↓)	t_{M3SR}	–	2			μs	When program memory is read
Address*2 → Data Output Delay Time	t_{DAD}	t_{ACC}			2	μs	When program memory is read
Address*2 → Data Output Hold Time	t_{HAD}	t_{OH}	0		130	μs	When program memory is read
MD3 Hold Time (vs. MD0 ↑)	t_{M3HR}	–	2			μs	When program memory is read
MD3 ↓→ Data Output Float Delay Time	t_{DFR}	–	2			μs	When program memory is read
Reset Setup Time	t_{RES}		10			μs	

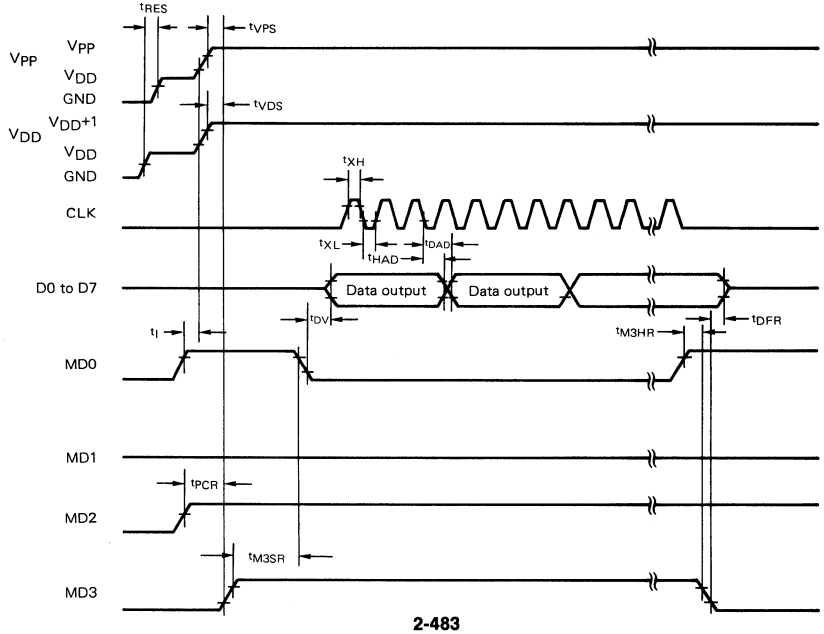
*1: Symbols for corresponding μPD27C256

*2: The internal address signal is incremented by one at the falling edge of the third CLK input and is not connected to a pin.

PROGRAM MEMORY WRITE TIMING



PROGRAM MEMORY READ TIMING



4-BIT SINGLE-CHIP MICROCONTROLLER WITH LCD CONTROLLER/DRIVER FOR INFRARED REMOTE CONTROLLER

μPD17202A is a 4-bit single-chip microcontroller containing an LCD controller/driver and an infrared remote controller carrier generator circuit.

This microcontroller employs the 17K architecture and can execute transfer and arithmetic operations with a single 16-bit instruction between data memory addresses and between the data memory and a peripheral circuit.

μPD17202A is housed in a 64-pin plastic QFP.

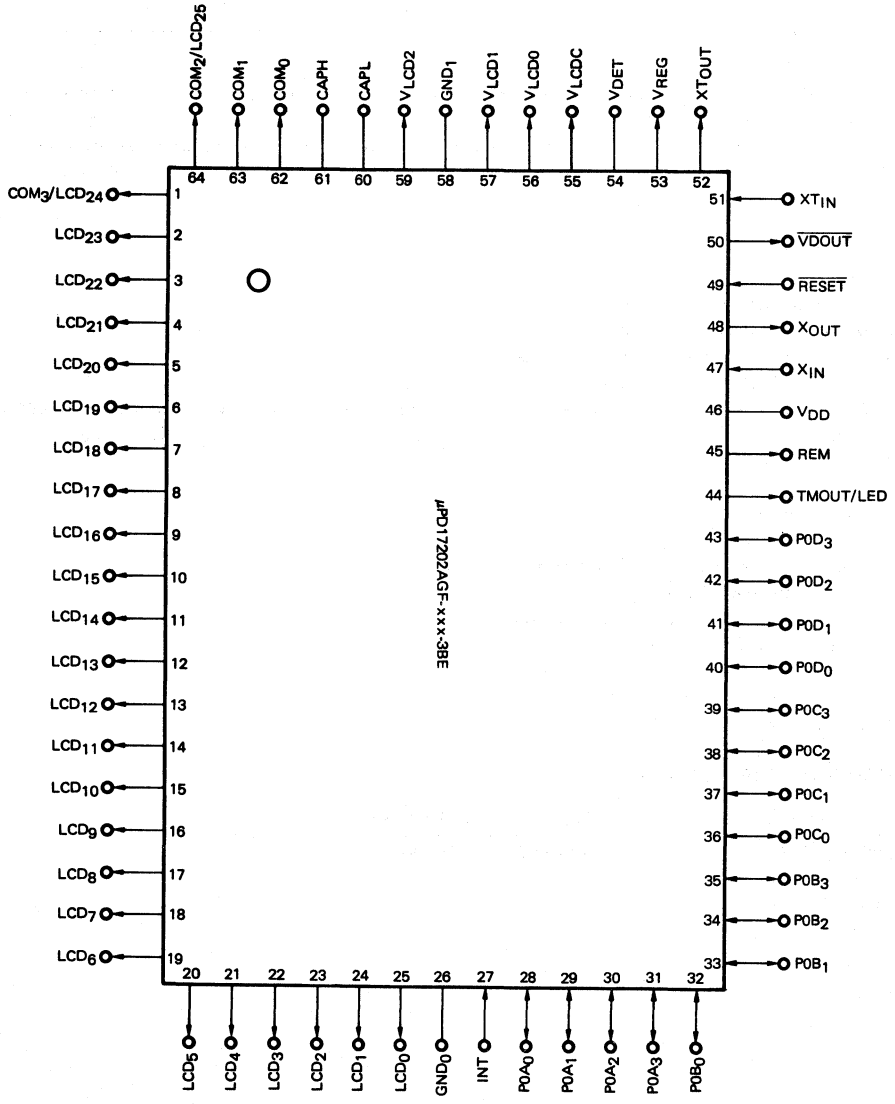
FEATURES

- 17K architecture
- Program memory (ROM): 2048 x 16 bits
- Data memory (RAM): 112 x 4 bits
- Internal infrared remote controller carrier generator
- Internal LCD controller/driver (can display up to 96 segments)
  Common pins: 4, segment pins: 24 (two of the common pins can also be used as segment pins), internal LCD constant voltage supply circuit: LCD drive voltage can be arbitrarily set at 2.4 to 5.4 V by external resistor
- I/O ports: 16
- External interrupt pin: 1
- Stack levels: 5 (two interrupt levels)
- 8-bit timer: 1 channel
- Watch timer: 1 channel (used as watchdog timer or watch timer)
- Standby function: STOP and HALT
  (to reduce current dissipation)
- Instruction execution time: 4 μs
  (with 4 MHz ceramic oscillator)
- Operation clock: 4 MHz or 32 kHz
- Operating voltage range: 2.2 to 5.5 V

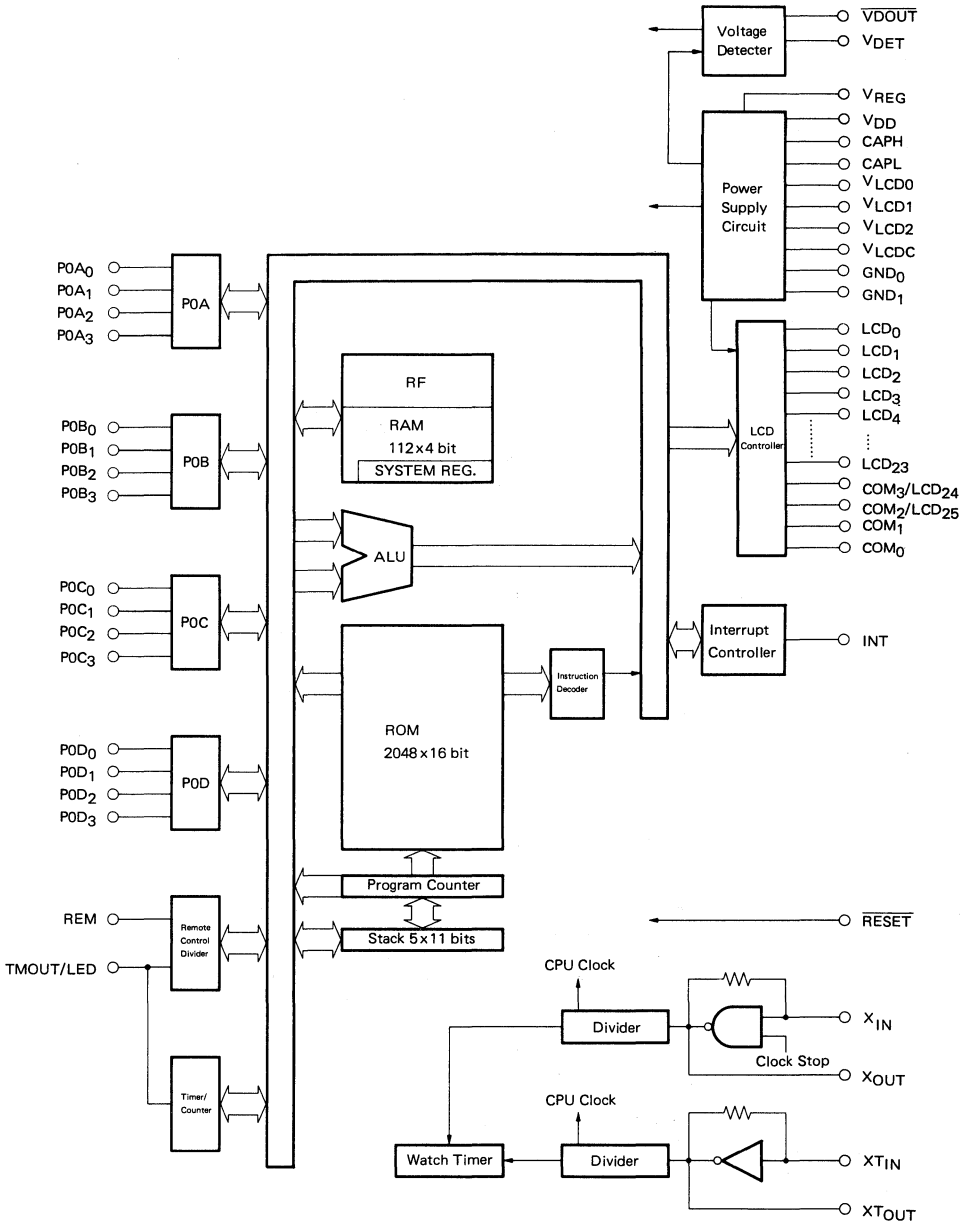
ORDERING INFORMATION

Order Code	Package	Quality Grade
μPD17202AGF-xxx-3BE	64-pin plastic QFP	Standard

PIN CONFIGURATION (Top View)



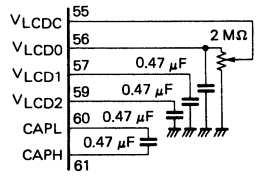
BLOCK DIAGRAM



1. PIN FUNCTIONS

1.1 PIN FUNCTION LIST

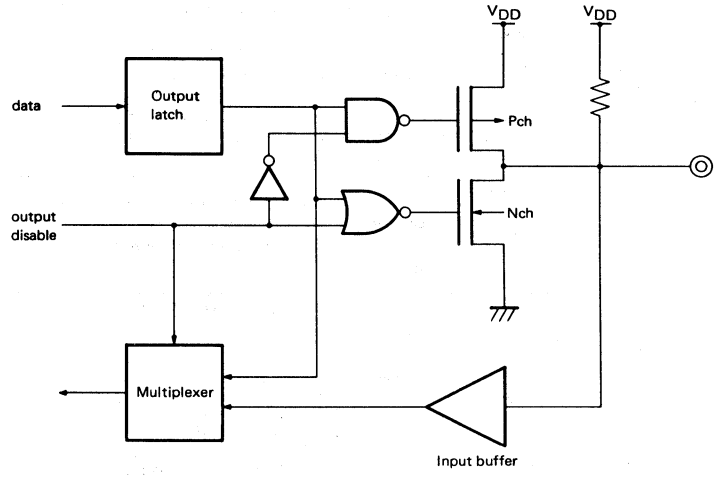
PIN NO.	SYMBOL	PIN NAME	FUNCTION	OUTPUT TYPE
28 29 30 31	$P0A_0$ $P0A_1$ $P0A_2$ $P0A_3$	Port 0A	These pins constitute a 4-bit I/O port which can be set in input or output mode in 4 bit units. In output mode, the port serves as a CMOS output port. In input mode, the port serves as a CMOS input port with pull-up resistor and can be used for key return input for a key matrix. If any one of these pins is made low in standby mode, the standby mode is released.	CMOS
32 33 34 35	$P0B_0$ $P0B_1$ $P0B_2$ $P0B_3$	Port 0B	These pins constitute a 4-bit I/O port which can be set in input or output mode in 4 bit units. In output mode, the port serves as a CMOS output port. In input mode, the port serves as a CMOS input port with pull-up resistor and can be used for key return input for a key matrix. If any one of these pins is made low in standby mode, the standby mode is released.	CMOS
36 37 38 39	$P0C_0$ $P0C_1$ $P0C_2$ $P0C_3$	Port 0C	These pins constitute a 4-bit I/O port which can be set in input or output mode in 4 bit units. In output mode, the port serves as an N-ch open-drain port and can be used for key source output for a key matrix. In input mode, the port serves as a CMOS input port. The standby mode cannot be set, when any one of these pins outputs a high level.	N-ch open drain
40 41 42 43	$P0D_0$ $P0D_1$ $P0D_2$ $P0D_3$	Port 0D	These pins constitute a 4-bit I/O port which can be set in input or output mode in 4 bit units. In output mode, the port serves as an N-ch open-drain port and can be used for key source output for a key matrix. In input mode, the port serves as a CMOS input port. The standby mode cannot be set, when any one of these pins outputs a high level.	N-ch open drain
27	INT	External interrupt input	This CMOS input pin inputs an external interrupt signal.	–
44	TMOUT/LED	Remote controller transfer/ display output	This pin outputs an NRZ (LED) signal in synchronization with an infrared remote controller signal, or 8-bit timer's output signal (TMOUT). When the NRZ signal is selected and while the remote controller carrier is output, this pin remains low.	CMOS
45	REM	Remote controller transfer output	This pin outputs an active-high infrared remote controller signal.	CMOS
47 48	X_{IN} X_{OUT}	Main clock oscillator	Connect a 4 MHz ceramic/crystal oscillator across these pins.	–

PIN NO.	SYMBOL	PIN NAME	FUNCTION	OUTPUT TYPE
49	$\overline{RESET}$	Reset input	This pin inputs the system reset signal. While a low level is input to this pin, main clock oscillation stops.	–
50	$\overline{VDOUT}$	Low voltage detector circuit output	This is the output pin for the internal low-voltage detector circuit. It outputs a low level, if the supply voltage drops below the specified value.	CMOS
51 52	XT_{IN} XT_{OUT}	Subclock oscillator	Connect a 32 kHz crystal oscillator across these pins.	–
53	V_{REG}	Voltage regulator output	This is the output pin for the voltage regulator for the XT oscillator. Connect an external 0.1 μF capacitor to this pin.	–
54	V_{DET}	Voltage detector voltage adjuster circuit	Connect a resistor, that adjusts the voltage level detected by the voltage regulator, between this pin and GND. The resistor is a variable resistor with several megohms resistance.	–
55	V_{LCDC}	LCD driver reference voltage adjuster circuit input	This pin adjusts the reference voltage for the LCD driver. **Example:**  	–
56 57 59	V_{LCD0} V_{LCD1} V_{LCD2}	LCD driver reference voltage output	These pins output the voltage obtained by raising the reference voltage for the LCD driver. The reference voltage is the voltage on V_{LCD0}. Connect a 0.47 μF capacitor between V_{LCD1} and V_{LCD2} and GND.	–
60 61	CAPL CAPH	Voltage raising capacitor	Connect a 0.47 μF capacitor across these pins to raise the voltage.	–
62 63	COM_0 COM_1	Common output	LCD drive common output pins.	CMOS
64 1	LCD_{25}/COM_2 LCD_{24}/COM_3	Common/ segment output	These pins can be used to output either LCD drive common or segment signals.	CMOS
2-25	LCD_{23}-LCD_0	Segment output	These are LCD drive segment output pins.	CMOS
46	V_{DD}	Power	Power supply pin. The operating voltage range is from 2.2 to 5.5 V.	–
26 58	GND_0 GND_1	Ground	Ground pin	–

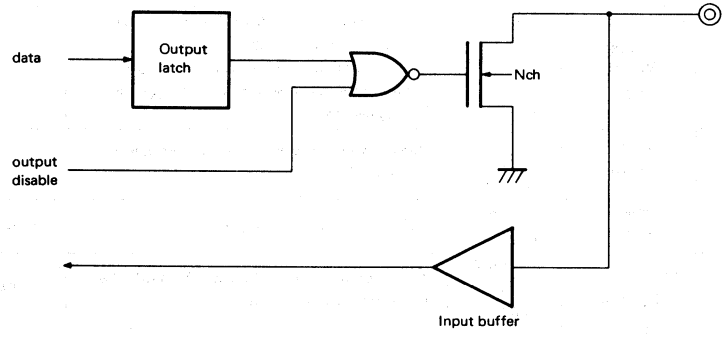
1.2 INPUT/OUTPUT CIRCUITS

The input/output circuit for each μPD17202A's pin is shown below.

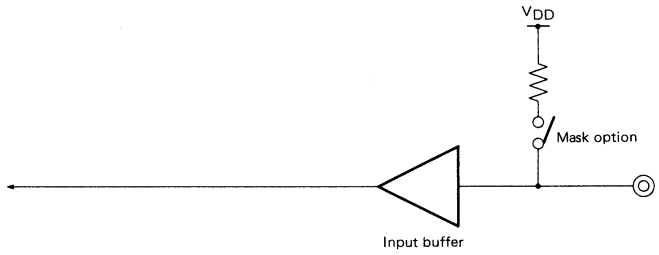
(1) $P0A_0$-$P0A_3$, $P0B_0$-$P0B_3$



(2) $P0C_0$-$P0C_3$, $P0D_0$-$P0D_3$



(3) $\overline{\text{RESET}}$



2. ASSEMBLER KEYWORDS

2.1 MASK OPTION DIRECTIVES

When developing the μPD17202A program, mask options must be specified by using mask option directives in the program.

The mask options must be specified for the following items:

- $P0A_0$, $P0A_1$, $P0A_2$, $P0A_3$
- $P0B_0$, $P0B_1$, $P0B_2$, $P0B_3$
- $\overline{RESET}$
- SYSTEM CLOCK

2.1.1 OPTION and ENDOP Directives

That portion of the program enclosed by the OPTION and ENDOP directives is called a mask option definition block. This block is described in the following format:

Description:

Symbol field	Mnemonic field	Operand field	Comment field
[label:]	OPTION		[; comment]
	⋮		
	ENDOP		

2.1.2 Mask Option Definition Directives

Table 2-1 lists the directives that can be used in the mask option definition block.

Here is an example of mask option definition:

Description:

Symbol field	Mnemonic field	Operand field
[label:]	OPTP0A	P0APLUP, P0APLUP, OPEN, OPEN

P0APLUP, P0APLUP, OPEN, OPEN
- OPEN, OPEN → $P0A_1$ and $P0A_0$ are open
- P0APLUP → $P0A_2$ is pulled up
- P0APLUP → $P0A_3$ is pulled up

Table 2-1 Mask Option Definition Directives

Name	Directive	Operands	1st operand	2nd operand	3rd operand	4th operand
RESET	OPTRES	1	Maks option of RESET			
			RESPLUP (w/pull-up resistor) OPEN (w/o pull-up resistor)			
P0A3-P0A0	OPTP0A	4	P0A3 Mask option	P0A2 Mask option	P0A1 Mask option	P0A0 Mask option
			P0APLUP (w/pull-up resistor) OPEN (w/o pull-up resistor)	P0APLUP (w/pull-up resistor) OPEN (w/o pull-up resistor)	P0APLUP (w/pull-up resistor) OPEN (w/o pull-up resistor)	P0APLUP (w/pull-up resistor) OPEN (w/o pull-up resistor)
P0B3-P0B0	OPTP0B	4	P0B3 Mask option	P0B2 Mask option	P0B1 Mask option	P0B0 Mask option
			P0BPLUP (w/pull-up resistor) OPEN (w/o pull-up resistor)	P0BPLUP (w/pull-up resistor) OPEN (w/o pull-up resistor)	P0BPLUP (w/pull-up resistor) OPEN (w/o pull-up resistor)	P0BPLUP (w/pull-up resistor) OPEN (w/o pull-up resistor)
SYSTEM CLOCK	OPTCK	2	Main clock	Subclock		
			USEX (main clock is used) NOX (main clock is not used)	USEXT (subclock is used) NOXT (subclock is not used)		

2.2 KEYWORD SYMBOLS

The symbols defined by the μPD17202A device file are listed in Table 2-2.

The defined symbols are the following register file names, port names, and peripheral device names.

2.2.1 Register File

The names of the symbols assigned to the register file are defined. These registers are accessed by the PEEK and POKE instructions through the window register (WR).

2.2.2 Registers and Ports on Data Memory

The names of the registers assigned at addresses 00H through 7FH on the data memory and the names of ports assigned to address 70H and those that follow, and system register names are defined.

2.2.3 Peripheral Circuits

The names of peripheral circuits accessed by the GET and PUT instructions are defined.

Table 2-2 Keyword Symbols (1/3)

Symbol	Attribute	Value	R/W	Remarks
DBF3	MEM	0.0CH	R/W	Bits 15-12 of data buffer
DBF2	MEM	0.0DH	R/W	Bits 11-8 of data buffer
DBF1	MEM	0.0EH	R/W	Bits 7-4 of data buffer
DBF0	MEM	0.0FH	R/W	Bits 3-0 of data buffer
AR3	MEM	0.74H	R	Bits 15-12 of address register
AR2	MEM	0.75H	R/W	Bits 11-8 of address register
AR1	MEM	0.76H	R/W	Bits 7-4 of address register
AR0	MEM	0.77H	R/W	Bits 3-0 of address register
WR	MEM	0.78H	R/W	Window register
BANK	MEM	0.79H	R	Bank register
IXH	MEM	0.7AH	R/W	Bits 11-8 of index register
MPH	MEM	0.7AH	R/W	Bits 7-4 of memory pointer
MPE	FLG	0.7AH.3	R/W	Memory pointer enable flag
IXM	MEM	0.7BH	R/W	Bits 7-4 of index register
MPL	MEM	0.7BH	R/W	Bits 3-0 of memory pointer
IXL	MEM	0.7CH	R/W	Bits 3-0 of index register
RPH	MEM	0.7DH	R/W	Bits 7-4 of register pointer
RPL	MEM	0.7EH	R/W	Bits 3-0 of register pointer
PSW	MEM	0.7FH	R/W	Program status word
BCD	FLG	0.7EH.0	R/W	BCD flag
CMP	FLG	0.7FH.3	R/W	Compare flag
CY	FLG	0.7FH.2	R/W	Carry flag
Z	FLG	0.7FH.1	R/W	Zero flag
IXE	FLG	0.7FH.0	R/W	Index register enable flag
LCDD0	MEM	0.40H	R/W	LCD segment 0
LCDD1	MEM	0.41H	R/W	LCD segment 1
LCDD2	MEM	0.42H	R/W	LCD segment 2
LCDD3	MEM	0.43H	R/W	LCD segment 3
LCDD4	MEM	0.44H	R/W	LCD segment 4
LCDD5	MEM	0.45H	R/W	LCD segment 5
LCDD6	MEM	0.46H	R/W	LCD segment 6
LCDD7	MEM	0.47H	R/W	LCD segment 7
LCDD8	MEM	0.48H	R/W	LCD segment 8
LCDD9	MEM	0.49H	R/W	LCD segment 9
LCDD10	MEM	0.4AH	R/W	LCD segment 10
LCDD11	MEM	0.4BH	R/W	LCD segment 11
LCDD12	MEM	0.4CH	R/W	LCD segment 12
LCDD13	MEM	0.4DH	R/W	LCD segment 13
LCDD14	MEM	0.4EH	R/W	LCD segment 14
LCDD15	MEM	0.4FH	R/W	LCD segment 15

Table 2-2 Keyword Symbols (2/3)

Symbol	Attribute	Value	R/W	Remarks
LCDD16	MEM	0.50H	R/W	LCD segment 16
LCDD17	MEM	0.51H	R/W	LCD segment 17
LCDD18	MEM	0.52H	R/W	LCD segment 18
LCDD19	MEM	0.53H	R/W	LCD segment 19
LCDD20	MEM	0.54H	R/W	LCD segment 20
LCDD21	MEM	0.55H	R/W	LCD segment 21
LCDD22	MEM	0.56H	R/W	LCD segment 22
LCDD23	MEM	0.57H	R/W	LCD segment 23
LCDD24	MEM	0.58H	R/W	LCD segment 24
LCDD25	MEM	0.59H	R/W	LCD segment 25
P0A0	FLG	0.70H.0	R/W	Bit 0 of port 0A
P0A1	FLG	0.70H.1	R/W	Bit 1 of port 0A
P0A2	FLG	0.70H.2	R/W	Bit 2 of port 0A
P0A3	FLG	0.70H.3	R/W	Bit 3 of port 0A
P0B0	FLG	0.71H.0	R/W	Bit 0 of port 0B
P0B1	FLG	0.71H.1	R/W	Bit 1 of port 0B
P0B2	FLG	0.71H.2	R/W	Bit 2 of port 0B
P0B3	FLG	0.71H.3	R/W	Bit 3 of port 0B
P0C0	FLG	0.72H.0	R/W	Bit 0 of port 0C
P0C1	FLG	0.72H.1	R/W	Bit 1 of port 0C
P0C2	FLG	0.72H.2	R/W	Bit 2 of port 0C
P0C3	FLG	0.72H.3	R/W	Bit 3 of port 0C
P0D0	FLG	0.73H.0	R/W	Bit 0 of port 0D
P0D1	FLG	0.73H.1	R/W	Bit 1 of port 0D
P0D2	FLG	0.73H.2	R/W	Bit 2 of port 0D
P0D3	FLG	0.73H.3	R/W	Bit 3 of port 0D
SP	MEM	0.81H	R/W	Stack pointer
SYSCK	FLG	0.82H.1	R/W	Selects system clock
XEN	FLG	0.82H.0	R/W	Enables main clock
WDTRES	FLG	0.83H.3	R/W	Resets watchdog timer
WTMMD	FLG	0.83H.2	R/W	Selects watch timer mode
WTMRES	FLG	0.83H.1	R/W	Resets watch timer mode
VDDDET	FLG	0.87H.3	R/W	VDD detection flag
INT	FLG	0.8FH.0	R	INT pin status
NRZBF	FLG	0.91H.0	R/W	NRZ buffer data
NRZ	FLG	0.92H.0	R/W	NRZ data
IEG	FLG	0.9FH.0	R/W	Selects interrupt edge of INT pin
TMOE	FLG	0.A4H.1	R/W	8-bit timer output enable flag
IPWTM	FLG	0.AFH.2	R/W	Watch timer interrupt enable flag
IP	FLG	0.AFH.1	R/W	INT interrupt enable flag

Table 2-2 Keyword Symbols (3/3)

Symbol	Attribute	Value	R/W	Remarks
IPTM	FLG	0.AFH.0	R/W	8-bit timer interrupt enable flag
LCDEN	FLG	0.B1H.3	R/W	LCD display enable flag
LCDCK2	FLG	0.B1H.2	R/W	LCD display setting #2
LCDCK1	FLG	0.B1H.1	R/W	LCD display setting #1
LCDCK0	FLG	0.B1H.0	R/W	LCD display setting #0
LCDMD3	FLG	0.B2H.3	R/W	LCD display setting #3
LCDMD2	FLG	0.B2H.2	R/W	LCD display setting #2
LCDMD1	FLG	0.B2H.1	R/W	LCD display setting #1
LCDMD0	FLG	0.B2H.0	R/W	LCD display setting #0
TMEN	FLG	0.B3H.3	R/W	8-bit timer counter enable flag
TMRES	FLG	0.B3H.2	R/W	8-bit timer reset flag
TMCK1	FLG	0.B3H.1	R/W	Selects clock source of 8-bit timer
TMCK0	FLG	0.B3H.0	R/W	Selects clock source of 8-bit timer
P0DGIO	FLG	0.B7H.3	R/W	P0D port I/O setting flag
P0CGIO	FLG	0.B7H.2	R/W	P0C port I/O setting flag
P0BGIO	FLG	0.B7H.1	R/W	P0B port I/O setting flag
P0AGIO	FLG	0.B7H.0	R/W	P0A port I/O setting flag
IRQWTM	FLG	0.BDH.0	R/W	Watch timer interrupt request flag
IRQ	FLG	0.BEH.0	R/W	INT interrupt request flag
IRQTM	FLG	0.BFH.0	R/W	8-bit timer interrupt request flag
DBF	DAT	0FH	R/W	Operand of GET and PUT instructions
IX	DAT	01H	R/W	Index register
TMC	DAT	02H	R	8-bit timer/counter
TMM	DAT	02H	W	Modulo register of 8-bit timer
NRZLTMM	DAT	03H	R/W	NRZ modulo register, low
NRZHTMM	DAT	04H	R/W	NRZ modulo register, high
AR	DAT	40H	R/W	Address register

3. μPD17202A INSTRUCTION SET

3.1 INSTRUCTION SET OUTLINE

$b_{14}-b_{11}$ \ b_{15}		0	1
Bin.	Hex.		
0 0 0 0	0	ADD r, m	ADD m, #i
0 0 0 1	1	SUB r, m	SUB m, #i
0 0 1 0	2	ADDC r, m	ADDC m, #i
0 0 1 1	3	SUBC r, m	SUBC m, #i
0 1 0 0	4	AND r, m	AND m, #i
0 1 0 1	5	XOR r, m	XOR m, #i
0 1 1 0	6	OR r, m	OR m, #i
0 1 1 1	7	INC AR INC IX MOVT DBF, @AR BR @AR CALL @AR RET RETSK EI DI RETI PUSH AR POP AR GET DBF, p PUT p, DBF PEEK WR, rf POKE rf, WR RORC r STOP s HALT h NOP	
1 0 0 0	8	LD r, m	ST m, r
1 0 0 1	9	SKE m, #i	SKGE m, #i
1 0 1 0	A	MOV @r, m	MOV m, @r
1 0 1 1	B	SKNE m, #i	SKLT m, #i
1 1 0 0	C	BR addr	CALL addr
1 1 0 1	D		MOV m, #i
1 1 1 0	E		SKT m, #n
1 1 1 1	F		SKF m, #n

3.2 LEGEND

M	:	Data memory address
m	:	Data memory address except bank
m_H	:	Data memory row address
m_L	:	Data memory column address
R	:	General register address
r	:	General register column address
RP	:	General register pointer
RF	:	Register file
rf	:	Register file address
rf_H	:	Register file address (higher 3 bits)
rf_L	:	Register file address (lower 3 bits)
AR	:	Address register
IX	:	Index register
IXE	:	Index enable flag
DBF	:	Data buffer
WR	:	Window register
MP	:	Data memory row address pointer
MPE	:	Memory pointer enable flag
PE	:	Peripheral register
p	:	Peripheral address
p_H	:	Peripheral address (higher 3 bits)
p_L	:	Peripheral address (lower 4 bits)
PC	:	Program memory counter
SP	:	Stack pointer
STACK	:	Stack value indicated by stack pointer
BANK	:	Bank register
(AR)rom	:	Data for program memory indicated by address register
INTEF	:	Interrupt enable flag
i	:	Immediate data (4 bits)
n	:	Bit position (4 bits)
addr	:	Program memory address (11 bits)
CY	:	Carry flag
s	:	STOP releasing condition
h	:	HALT releasing condition
[ ]	:	Data memory or register address
( )	:	Data memory or register value

3.3 INSTRUCTION LIST

Group	Mnemonic	Operand	Operation	Machine code			
				OP code	3 bits	4 bits	4 bits
Addition	ADD	r, m	(R) ← (R) + (M)	00000	m_H	m_L	r
		m, #i	(M) ← (M) + i	10000	m_H	m_L	i
	ADDC	r, m	(R) ← (R) + (M) + (CY)	00010	m_H	m_L	r
		m, #i	(M) ← (M) + i + (CY)	10010	m_H	m_L	i
	INC	AR	(AR) ← (AR) + 1	00111	000	1001	0000
		IX	(IX) ← (IX) + 1	00111	000	1000	0000
Subtraction	SUB	r, m	(R) ← (R) − (M)	00001	m_H	m_L	r
		m, #i	(M) ← (M) − i	10001	m_H	m_L	i
	SUBC	r, m	(R) ← (R) − (M) − (CY)	00011	m_H	m_L	r
		m, #i	(M) ← (M) − i − (CY)	10011	m_H	m_L	i
Compare	SKE	m, #i	(M) − i, skip if zero	01001	m_H	m_L	i
	SKGE	m, #i	(M) − i, skip if not borrow	11001	m_H	m_L	i
	SKLT	m, #i	(M) − i, skip if borrow	11011	m_H	m_L	i
	SKNE	m, #i	(M) − i, skip if not zero	01011	m_H	m_L	i
Logical	AND	m, #i	(M) ← (M) AND i	10100	m_H	m_L	i
		r, m	(R) ← (R) AND (M)	00100	m_H	m_L	r
	OR	m, #i	(M) ← (M) OR i	10110	m_H	m_L	i
		r, m	(R) ← (R) OR (M)	00110	m_H	m_L	r
	XOR	m, #i	(M) ← (M) XOR i	10101	m_H	m_L	i
		r, m	(R) ← (R) XOR (M)	00101	m_H	m_L	r
Transfer	LD	r, m	(R) ← (M)	01000	m_H	m_L	r
	ST	m, r	(M) ← (R)	11000	m_H	m_L	r
	MOV	@r, m	if MPE = 1 : [(MP), (R)] ← (M) if MPE = 0 : [(m_H), (R)] ← (M)	01010	m_H	m_L	r
		m, @r	if MPE = 1 : (M) ← [(MP), (R)] if MPE = 0 : (M) ← [(m_H), (R)]	11010	m_H	m_L	r
		m, #i	(M) ← i	11101	m_H	m_L	i
	MOVT	DBF, @AR	SP ← (SP) − 1, STACK ← PC, DBF ← (AR)rom, PC ← STACK, SP ← (SP) + 1	00111	000	0001	0000
	PUSH	AR	(SP) ← (SP) − 1, (STACK) ← (AR)	00111	000	1101	0000
	POP	AR	(AR) ← (STACK), (SP) ← (SP) + 1	00111	000	1100	0000
	PEEK	WR, rf	(WR) ← (RF)	00111	rf_H	0011	rf_L
	POKE	rf, WR	(RF) ← (WR)	00111	rf_H	0010	rf_L
	GET	DBF, p	(DBF) ← (PE)	00111	p_H	1011	p_L
	PUT	p, DBF	(PE) ← (DBF)	00111	p_H	1010	p_L
Judge	SKT	m, #n	CMP ← 0, skip if M_N = all "1"	11110	m_H	m_L	n
	SKF	m, #n	CMP ← 0, skip if M_N = all "0"	11111	m_H	m_L	n

Group	Mnemonic	Operand	Operation	Machine code			
				OP code	3 bits	4 bits	4 bits
Branch	BR	addr	PC ← addr	01100	addr		
		@AR	PC ← AR	00111	000	0100	0000
Shift	RORC	r	(CY) → (R) → CY	00111	000	0111	r
Subroutine	CALL	addr	SP ← (SP) − 1, STACK ← ((PC) + 1), PC ← addr	11100	addr		
		@AR	SP ← (SP) − 1, STACK ← ((PC) + 1), PC ← (AR)	00111	000	0101	0000
	RET		PC ← (STACK), SP ← (SP) + 1	00111	000	1110	0000
	RETSK		PC ← (STACK), SP ← (SP) + 1 and skip	00111	001	1110	0000
	RETI		PC ← (STACK), SP ← (SP) + 1	00111	100	1110	0000
Interrupt	EI		INTEF ← 1	00111	000	1111	0000
	DI		INTEF ← 0	00111	001	1111	0000
Other	STOP	8H	STOP	00111	010	1111	1000
	HALT	h	HALT	00111	011	1111	h
	NOP		No operation	00111	100	1111	0000

3.4 ASSEMBLER (AS17K) MACROINSTRUCTIONS

Legend

flag : One of flag1-flagn
flag1-flagn : Flag name indicated by keyword
n : Number
< > : Can be omitted

Mnemonic	Operand	n	Operation
SKTn	flag1, ···flagn	1 ≦n≦ 4	if (flag1) − (flagn) = all "1", then skip
SKFn	flag1, ···flagn	1 ≦n≦ 4	if (flag1) − (flagn) = all "0", then skip
SETn	flag1, ···flagn	1 ≦n≦ 4	(flag1) − (flagn) ← 1
CLR	flag1, ···flagn	1 ≦n≦ 4	(flag1) − (flagn) ← 0
NOTn	flag1, ···flagn	1 ≦n≦ 4	if (flag) = "0", then (flag) ← 1, if (flag) = "1", then (flag) ← 0
INITFLG	<NOT>flag1, ···<NOT>flagn	n= 4	if description = NOT flag, (flag) ← 0 if description = flag, (flag) ← 1

4. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage	V_{DD}	−0.3 to +7.0	V
Input Voltage	V_I	−0.3 to V_{DD} + 0.3	V
Operating Temperature	T_{opt}	−20 to +75	°C
Storage Temperature	T_{stg}	−40 to +125	°C

RECOMMENDED OPERATING RANGE

CAHRACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Supply Voltage	V_{DD1}	2.2	3.0	5.5	V	f_X = 4 MHz
	V_{DD2}	3.5	5.0	5.5	V	f_X = 8 MHz
Main Clock Oscillation Frequency	f_X	2.0	4.0	5.0	MHz	
Subclock Oscillation Frequency	f_{XT}		32.768		kHz	

CAPACITANCE (T_a = 25 °C, V_{DD} = 0 V)

CAHRACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Input Capacitance	C_{IN}			10	pF	INT, $\overline{\text{RESET}}$ pins
	C_{PIN}			10	PF	Other than INT, $\overline{\text{RESET}}$ pins

DC CHARACTERISTICS (V_{DD} = 3 V, T_a = −20 to +75 °C, f_X = 4 MHz, f_{XT} = 32 kHz)

CAHRACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS	
Low Voltage Detection Voltage	V_{DET}	1.3	2.0	2.9	V		
High-Level Input Voltage	V_{IH1}	0.8V_{DD}		V_{DD}	V	$\overline{RESET}$, INT pins	
	V_{IH2}	0.7V_{DD}		V_{DD}	V	Other than $\overline{RESET}$, INT pins	
Low-Level Input Voltage	V_{IL1}	0		0.2V_{DD}	V	$\overline{RESET}$, INT pins	
	V_{IL2}	0		0.3V_{DD}	V	Other than $\overline{RESET}$, INT pins	
High-Level Input Current	I_{IH1}			0.2	μA	INT pin	$V_{IH} = V_{DD}$
	I_{IH2}			0.2	μA	$\overline{RESET}$ pin	$V_{IH} = V_{DD}$
	I_{IH3}			0.2	μA	P0A-P0D pin	$V_{IH} = V_{DD}$
Low-Level Input Current	I_{IL1}			-0.2	μA	INT pin	V_{IL} = 0 V
	I_{IL2}			-0.2	μA	$\overline{RESET}$ pin	V_{IL} = 0 V w/o pull-up resistor
	I_{IL3}	-20	-50	-100	μA		V_{IL} = 0 V w/pull-up resistor
	I_{IL4}			-0.2	μA	P0A, P0B pins	V_{IL} = 0 V w/o pull-up resistor
	I_{IL5}	-6	-12	-20	μA		V_{IL} = 0 V w/pull-up resistor
	I_{IL6}			-0.2	μA	P0C, P0D pins	V_{IL} = 0 V
High-Level Output Current	I_{OH1}	-0.6	-2.0	-4.0	mA	P0A, P0B pins	$V_{OH} = V_{DD} - 0.3$ V
	I_{OH2}	-7.0	-15.0	-25.0	mA	REM pin	$V_{OH} = V_{DD} - 2.0$ V
	I_{OH3}	-0.3	-1.0	-2.0	mA	LED pin	$V_{OH} = V_{DD} - 0.3$ V
High-Level Output Current	I_{OH4}	-0.3	-1.0	-2.0	mA	$\overline{VDOUT}$ pin	$V_{OH} = V_{DD} - 0.3$ V
Low-Level Output Current	I_{OL1}	0.5	1.5	2.5	mA	P0A, P0B pins	V_{OL} = 0.3 V
	I_{OL2}	0.5	1.5	2.5	mA	P0C, P0D pins	V_{OL} = 0.3 V
	I_{OL3}	0.5	1.5	2.5	mA	REM pin	V_{OL} = 0.3 V
	I_{OL4}	0.5	1.5	2.5	mA	LED pin	V_{OL} = 0.3 V
	I_{OL5}	0.5	1.5	2.5	mA	$\overline{VDOUT}$ pin	V_{OL} = 0.3 V
Supply Current	I_{DD1}	0.2	0.5	1.5	mA	Operation mode	XT and X
	I_{DD2}		15	30	μA		Only XT
	I_{DD3}		0.5	1.5	mA	HALT mode	XT and X
	I_{DD4}		10	15	μA		Only XT
LCD Output Voltage Adjustable Range	V_{LCD0}	0.6		1.8	V		
Doubler Output Voltage	V_{LCD1}	1.9V_{LCD0}	2V_{LCD0}		V		
Tripler Output Voltage	V_{LCD2}	2.85V_{LCD0}	3V_{LCD0}		V		
Common Output Current	I_{COM}	30			μA	V_{DS} = 0.2 V	
Segment Output Current	I_{LCD}	5			μA	V_{DS} = 0.2 V	

RECOMMENDED OSCILLATORS

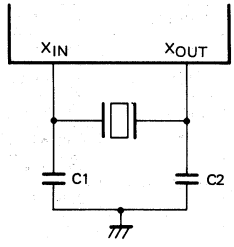
MAIN SYSTEM CLOCK: CERAMIC OSCILLATOR

MANUFACTURER	PRODUCT NAME	EXTERNAL CAPACITOR (pF)		OSCILLATION VOLTAGE (V)		REMARKS
		C1	C2	MIN.	MAX.	
Murata Mfg.	CSA3.58MG	30	30	2.0	6.0	
	CSA4.00MG	30	30	2.0	6.0	
	CSA4.19MG	30	30	2.0	6.0	
	CST3.58MGW	none	none	2.0	6.0	C contained type
	CST4.00MGW	none	none	2.0	6.0	
	CST4.19MGW	none	none	2.0	6.0	
Kyocera	KBR3.58MS	33	33	2.0	6.0	
	KBR4.0MS	33	33	2.0	6.0	
	KBR4.19MS	33	33	2.0	6.0	
Toko	CRHF4.00	18	18	2.0	6.0	
Dai-Shinku	PRS0400BCSAN	39	33	2.0	6.0	

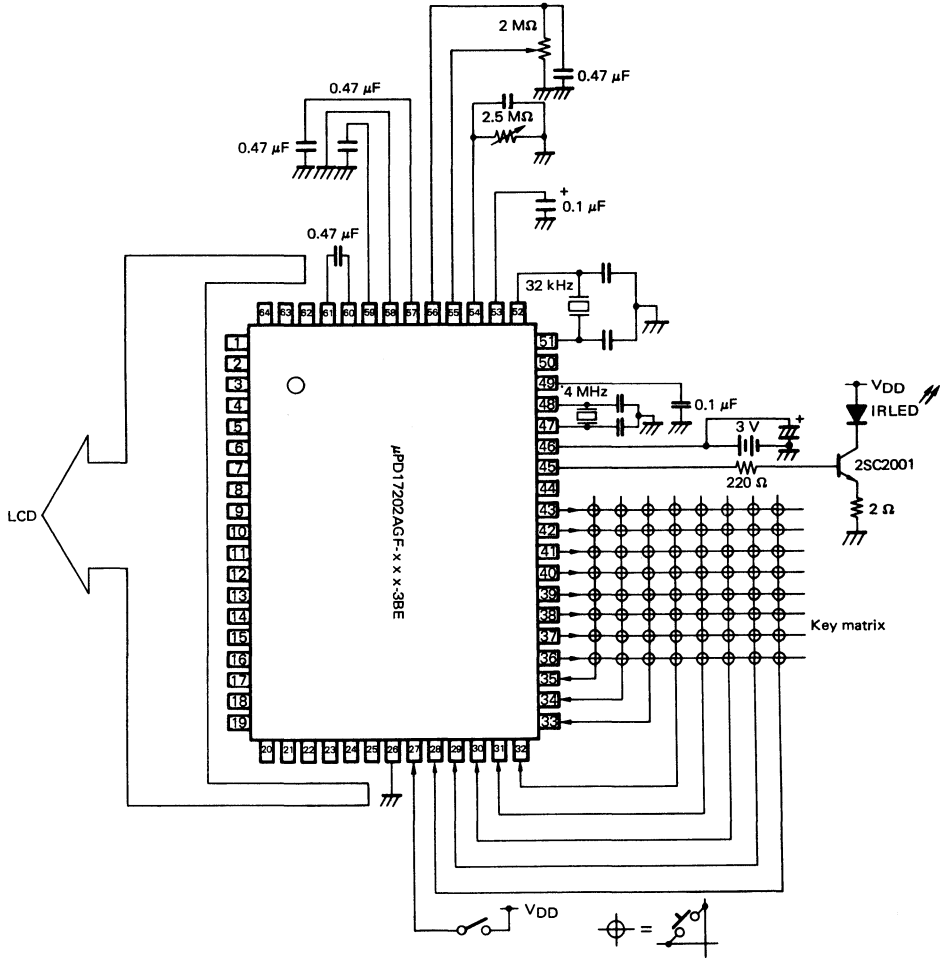
MAIN SYSTEM CLOCK: CRYSTAL OSCILLATOR

MANUFACTURER	FREQUENCY (MHz)	RETAINER	EXTERNAL CAPACITOR (pF)		OSCILLATION VOLTAGE (V)		REMARKS
			C1	C2	MIN.	MAX.	
Kinseki	4.0	HC-49U-S	22	22	2.0	6.0	

Oscillator circuit



5. APPLICATION CIRCUIT EXAMPLE



μPD17P202A is a model of μPD17202A which is equipped with a one-time PROM in place of the μPD17202A internal mask ROM.

Since the user can write the program to μPD17P202A, the microcomputer is suitable for experimental or small-scale production of μPD17202A systems.

It is recommended that you also read the documents related to μPD17202A, in addition to this data sheet.

FEATURES

- Compatible with μPD17202A
- Internal one-time PROM: 2,048 x 16 bits
- Operating voltage range: 2.2 to 5.5 V

ORDERING INFORMATION

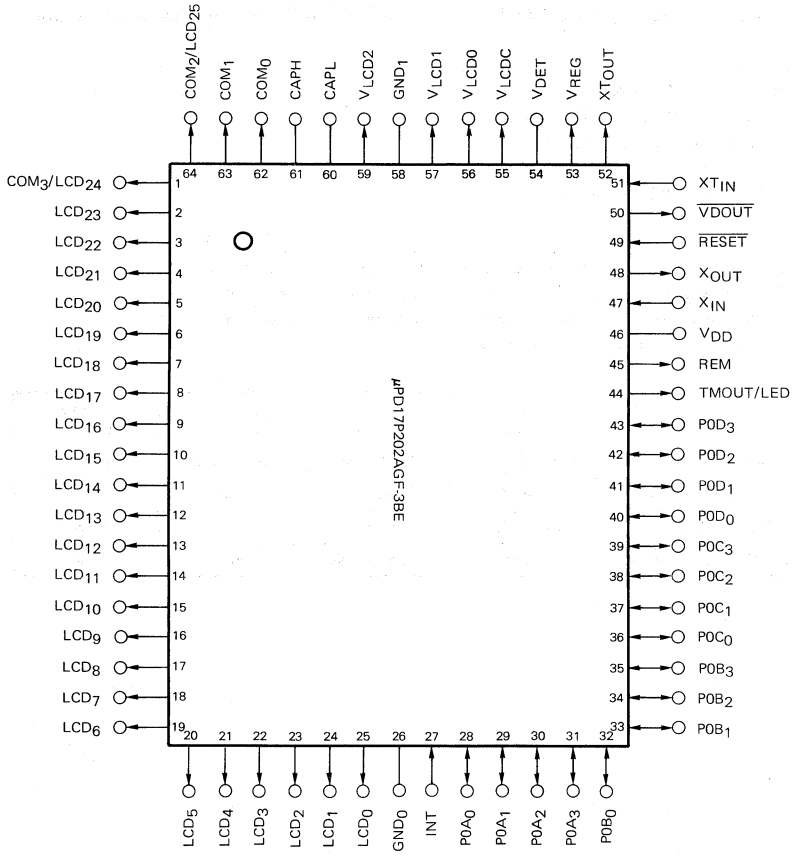
Order Code	Package	Quality Grade
μPD17P202AGF-001-3BE	64-pin plastic QFP (14 x 20 mm)	Standard
μPD17P202AGF-002-3BE	64-pin plastic QFP (14 x 20 mm)	Standard
μPD17P202AGF-003-3BE	64-pin plastic QFP (14 x 20 mm)	Standard

Note: Table below indicates differences in these products:

Item / Part number	Pull-up resistor for $\overline{\text{RESET}}$ pin	Pull-up resistors for P0A, P0B pins	Main clock generator used/unused	Subclock generator used/unused
μPD17P202AGF-001-3BE	Provided	Provided	Used	Used
μPD17P202AGF-002-3BE	Not provided	Provided	Used	Unused
μPD17P202AGF-003-3BE	Not provided	Not provided	Unused	Used

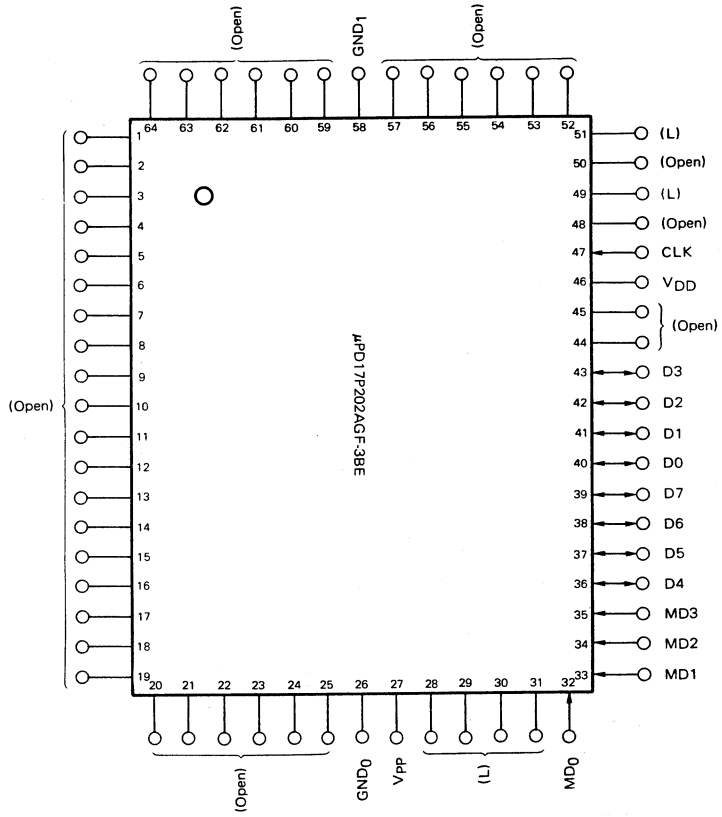
PIN CONFIGURATION (Top View)

(1) Ordinary operation



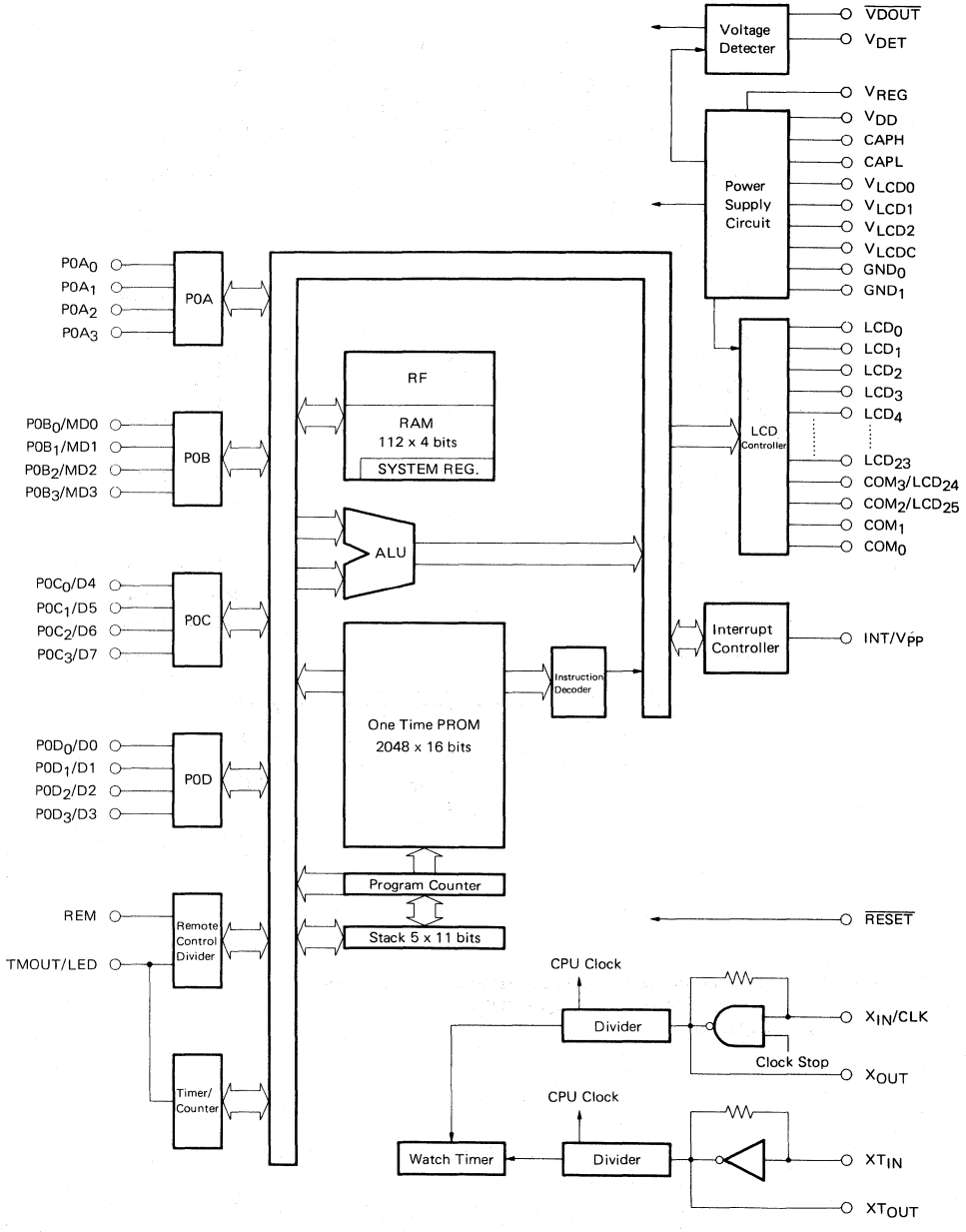
$P0A_0$-$P0A_3$	:	Input/output port
$P0B_0$-$P0B_3$	:	Input/output port
$P0C_0$-$P0C_3$	:	Input/output port
$P0D_0$-$P0D_3$	:	Input/output port
V_{REG}	:	Voltage regulator output
V_{DET}	:	Voltage detector detection voltage adjustment
V_{LCDC}	:	LCD drive reference voltage adjustment
V_{LCD0}-V_{LCD2}	:	LCD drive voltage outputs
LCD_0-LCE_{35}	:	LCD segment signal output
COM_0-COM_3	:	LCD common signal output
TMOUT	:	8-bit timer output
LED	:	Remote control transmission indication output
REM	:	Remote control transmission output
INT	:	External interrupt request signal input
$\overline{RESET}$	:	Reset input
$\overline{VDOUT}$	:	Low voltage detection circuit output
X_{IN}, X_{OUT}	:	Main clock oscillator circuit
XT_{IN}, XT_{OUT}	:	Subclock oscillator circuit
CAPH, CAPL	:	Booster capacitor connection pins
CLK	:	PROM clock input
MD0-MD3	:	PROM mode selection input
D0-D7	:	PROM data input/output
V_{PP}	:	PROM write voltage power supply pin
V_{DD}	:	Power supply pin
GND_0, GND_1	:	GND

(2) PROM programming mode



Note: ( ) indicates processing for pins not used in the PROM programming mode.
L : Ground each of these pins through a 470 Ω resistor.
Open : Do not connect these pins.

BLOCK DIAGRAM



1. PIN FUNCTIONS

1.1 ORDINARY OPERATION MODE

PIN No.	SYMBOL	FUNCTION	OUTPUT TYPE	POWER ON RESET
62 63 64 1 2 ⋮ 25	COM_0 COM_1 LCD_{25}/COM_2 LCD_{24}/COM_3 LCD_{23} ⋮ LCD_0	LCD controller/driver segment signal outputs and LCD controller/driver common signal outputs. ● LCD_{25} to LCD_0 ・ LCD controller/driver segment signal outputs ● COM_0 to COM_3 ・ LCD controller/driver common signal outputs	CMOS	–
26	GND_0	GND	–	–
27	INT	Inputs external interrupt request signal. Either the rising edge or the falling edge can be specified as the interrupt request effective edge.	–	Input
28 ⋮ 31	$P0A_0$ ⋮ $P0A_3$	4-bit CMOS input/output port. This port can be specified for input/output in 4-bit units. In the input mode, these pins become CMOS inputs, and can be used as key return inputs for key matrix. See **Note.**	CMOS push-pull	Input
32 ⋮ 35	$P0B_0$ ⋮ $P0B_3$	4-bit CMOS input/output port. This port can be specified for input/output in 4-bit units. In the input mode, these pins become CMOS inputs, and can be used as key return inputs for key matrix. See **Note.**	CMOS push-pull	Input
36 ⋮ 39	$P0C_0$ ⋮ $P0C_3$	4-bit CMOS input/output port. This port can be specified for input/output in 4-bit units. In the output mode, these pins become N-ch open-drain output, and can be used for key source output for key matrix.	N-ch open-drain	Input
40 ⋮ 43	$P0D_0$ ⋮ $P0D_3$	4-bit CMOS input/output port. This port can be specified for input/output in 4-bit units. In the output mode, these pins become N-ch open-drain output, and can be used for key source output for key matrix.	N-ch open-drain	Input
44	TMOUT/LED	This pin outputs NRZ signal (LED) synchronized with infrared remote control signal and 8-bit timer (TMOUT). ● TMOUT ・ 8-bit timer output ● LED ・ Remote control transmission indication output	CMOS push-pull	High level output

Note: Pull-up resistors are provided only in the μPD17P202A-001 and μPD17P202A-002.

PIN No.	SYMBOL	FUNCTION	OUTPUT TYPE	POWER ON RESET
45	REM	Infrared remote control signal output.	CMOS push-pull	High level output
46	V_{DD}	Positive voltage power supply pin. 2.2 to 5.5 V is applied in the normal operation mode.	–	–
47 48	X_{IN} X_{OUT}	Main clock oscillation circuit is connected across these pins. Connect a 4 MHz ceramic resonator or crystal resonator across these pins.	–	–
49	$\overline{RESET}$	Reset signal input.	–	Input
50	$\overline{VDOUT}$	Internal low voltage detection circuit output.	CMOS push-pull	–
51 52	XT_{IN} XT_{OUT}	Subclock oscillation circuit is connected across these pins. Connect a 32 kHz crystal resonator across these pins.	–	–
53	V_{REG}	Voltage regulator output for subclock generator.	–	–
54	V_{DET}	A resistor for adjusting the voltage detector detection level is connected to this pin.	–	–
55	V_{LCDC}	Adjusts LCD drive reference voltage.	–	–
56 57	V_{LCD0} V_{LCD1}	Outputs a voltage boosted from LCD drive reference voltage.	–	–
58	GND_1	GND	–	–
59	V_{LCD2}	Outputs a voltage boosted from LCD drive reference voltage.	–	–
60 61	CAPL CAPH	Voltage boosting capacitor is connected across these pins.	–	–

1.2 PROM PROGRAMMING MODE

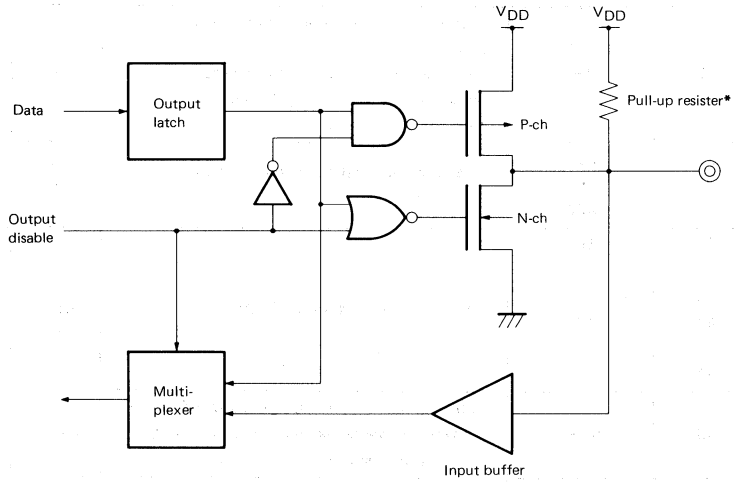
PIN No.	SYMBOL	FUNCTION	OUTPUT TYPE	POWER ON RESET
26	GND_0	GND	–	–
27	V_{PP}	Positive power supply pin for PROM programming. 12.5 V is applied to this pin when programming, reading, or verifying the program memory.	–	–
32 | 35	MD3 | MD0	Operation mode selection inputs for PROM programming.	–	Input
36 | 39 40 | 43	D4 | D7 D0 | D3	8-bit data input/output for PROM programming.	CMOS push-pull	Input
46	V_{DD}	Positive power supply pin. 6 V is applied to this pin when programming, reading, or verifying the program memory.	–	–
47	CLK	Clock input for PROM programming.	–	–
48	GND_1	GND	–	–

Remarks: Pins other then listed above are not used in the PROM programming mode. Refer to **"Pin Connection Diagram (2) PROM Programming Mode"** for recommended conditions for unused pins.

1.3 PIN EQUIVALENT CIRCUITS

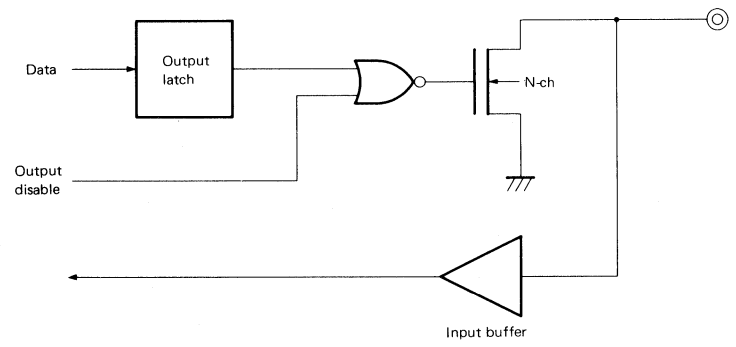
The simplified pin equivalent circuits schematic views for μPD17P202A's pins are presented below.

(1) $P0A_0$ through $P0A_3$, $P0B_0$/MD0 through $P0B_3$/MD3

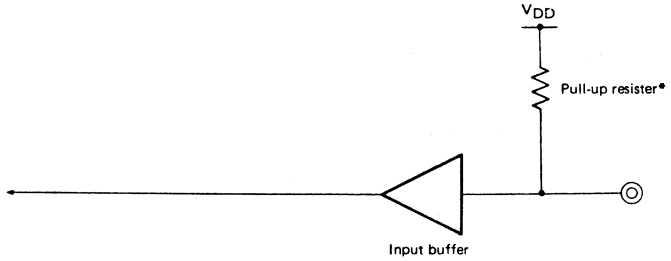


*: Only μPD17P202A-001 and μPD17P202A-002

(2) $P0C_0$/D4 through $P0C_3$/D7, $P0D_0$/D0 through $P0D_3$/D3



(3) $\overline{\text{RESET}}$



*: Only μPD17P202A-001

2. WRITING, READING, AND VERIFYING ONE-TIME PROM (PROGRAM MEMORY)

When the PROM is to be written, read, or verified, μPD17P201A is set in the PROM mode, and the pins shown in Table 2-1 are used. No address has to be input. Instead, the address is incremented by the clock input from the CLK pin.

Table 2-1 Pins Used to Write/Read/Verify Program Memory

Pin name	Function
V_{PP}	Apply program voltage (12.5 V) to this pin.
CLK	Address incrementing clock input
MD0 to MD3	Operation mode selector
D0 to D7	8-bit data input/output
V_{DD}	Apply operating voltage (6 V) to this pin.

2.1 OPERATION MODES FOR PROGRAM MEMORY WRITE, READ, AND VERIFY

μPD17P202A is set in the program memory write, read, or verify mode, when +6 V is applied to pin V_{DD}, and +12.5 V is applied to pin V_{PP}, after being placed in the reset status (V_{DD} = 5 V, $\overline{RESET}$ = low level) for a certain period of time.

The operation modes, selected by pens MD0 through MD3, are listed in Table 2-2.

Pins not used to write, read, or verify the program memory must be open, or grounded through pull-down resistors (470 Ω).

Table 2-2 Operation Modes for Program Memory Write, Read, and Verify

Operation mode selection						Operation mode
V_{PP}	V_{DD}	MD0	MD1	MD2	MD3	
+12.5 V	+6 V	H	L	H	L	Program memory address 0 clear
		L	H	H	H	Write mode
		L	L	H	H	Read, verify mode
		H	x	H	H	Program inhibit mode

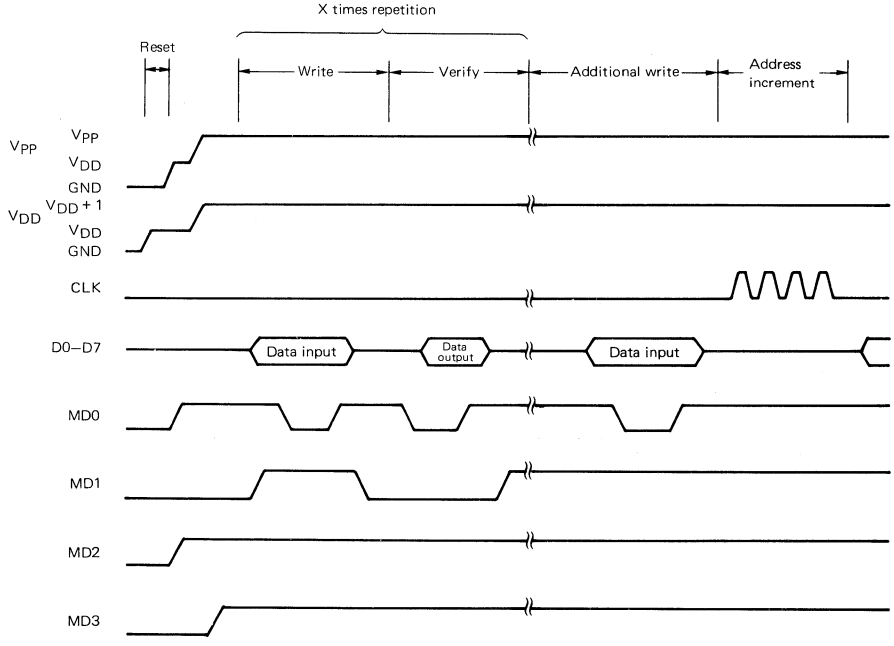
Remarks: x: L or H

2.2 PROGRAM MEMORY WRITING PROCEDURE

Write the program memory by following these steps. The program memory can be written at high speeds.

(1) Pull down the unused pins to the ground potential through resistors. Make the pin CLK low.
(2) Apply 5 V to pin V_{DD}. Make pin V_{PP} low.
(3) Wait for 10 μs. Then, apply 5 V to pin V_{PP}.
(4) Set the program memory address 0 clear mode by the mode selector pins.
(5) Apply 6 V to pin V_{DD}, and 12.5 V to pin V_{PP}.
(6) Program inhibit mode
(7) Write data in the 1 ms write mode.
(8) Program inhibit mode
(9) Verify mode. Proceed to (10), if the memory has been written. If it has not been written, repeat (7) through (9).
(10) Additional writing for (the number of times (7) through (9) are repeated: X) x 1 ms
(11) Program inhibit mode
(12) Input a pulse four times to pin CLK, in order to increment the program memory address (by one).
(13) Repeat (7) through (12), until the last address is programmed.
(14) Program memory address 0 clear mode
(15) Decrease the voltages on pin V_{DD} and V_{PP} to 5 V.
(16) Turn power off.

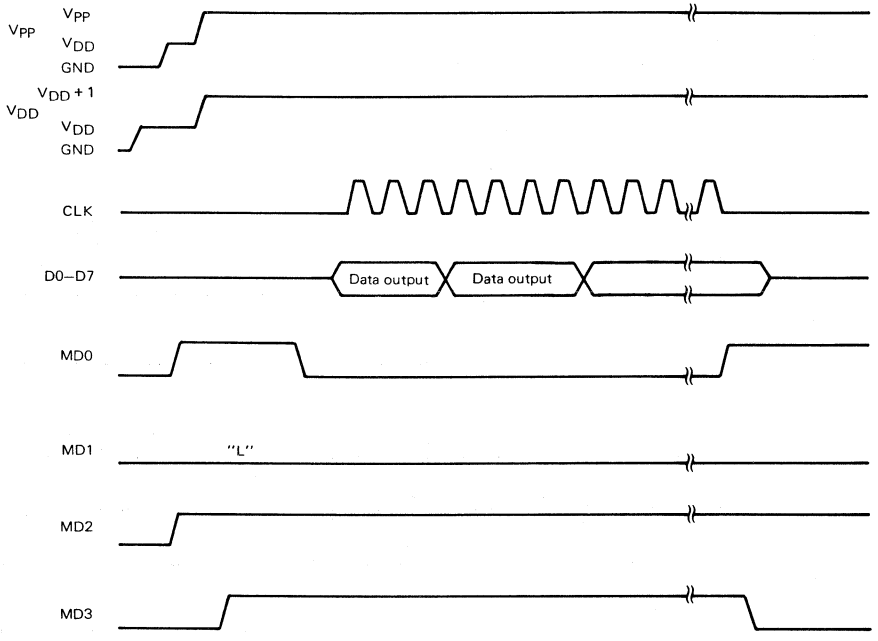
The following figure illustrates steps (2) through (12) above.



2.3 PROGRAM MEMORY READING PROCEDURE

(1) Pull down the unused pins to the ground potential through resistors. Make the pin CLK low.
(2) Apply 5 V to pin V_{DD}. Make pin V_{PP} low.
(3) Wait for 10 μs. Then, apply 5 V to pin V_{PP}.
(4) Set the program memory address 0 clear mode by the mode selector pins.
(5) Apply 6 V to pin V_{DD}, and 12.5 V to pin V_{PP}.
(6) Program inhibit mode
(7) Verify mode. The data for each address is output on a one-by-one basis in a cycle during which the clock pulse is input to pin CLK four times.
(8) Program inhibit mode
(9) Program memory address 0 clear mode
(10) Decrease the voltages on pin V_{DD} and V_{PP} to 5 V.
(11) Turn power off.

The following figure illustrates steps (2) through (9) above.



3. DIFFERENCES BETWEEN μPD17P202A AND μPD17202A

In the μPD17P202A, the internal mask ROM (program memory) for the μPD17202A is replaced by the PROM which can be programmed by the user. Therefore, the program memory and some mask options are the only differences between the μPD17P202A and μPD17202A, so the CPU functions and internal hardware are identical.

The table below summarizes the differences between the μPD17P202A and μPD17202A.

Refer to the μPD17202A data sheet for details on CPU functions and internal hardware.

<table>
<tr><th>Device / Item</th><th>μPD17P202A-001</th><th>μPD17P202A-002</th><th>μPD17P202A-003</th><th>μPD17202A</th></tr>
<tr><td>Program memory</td><td colspan="3">• PROM
• 0000H-07FFH
• 2048 x 16 bits</td><td>• Mask ROM
• 0000H-07FFH
• 2048 x 16 bits</td></tr>
<tr><td>$\overline{\text{RESET}}$ pin pull-up resistor</td><td rowspan="4">Provided</td><td>None</td><td rowspan="3">None</td><td rowspan="4">(Mask option)</td></tr>
<tr><td>P0A, P0B pins pull-up resistors</td><td rowspan="3">Provided</td></tr>
<tr><td>Main clock generator provided/not provided</td></tr>
<tr><td>Subclock generator provided/not provided</td><td>None</td><td>Provided</td></tr>
<tr><td>Pin connections</td><td colspan="3">V_{PP} pin, PROM programming pin are provided.</td><td>V_{PP} pin, PROM programming pin not provided</td></tr>
<tr><td>Operating voltage range</td><td colspan="4">2.2 to 5.5 V</td></tr>
<tr><td>Package</td><td colspan="4">64-pin plastic QFP (14 x 20 mm)</td></tr>
</table>

4. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage	V_{DD}	−0.3 to +7.0	V
Input Voltage	V_I	−0.3 to V_{DD} +0.3	V
Operating Temperature	T_{opt}	−20 to +75	°C
Storage Temperature	T_{stg}	−40 to +125	°C

CAPACITANCE (T_a = 25 °C, V_{DD} = 0 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Input Capacitance	C_{IN}			10	pF	Pins INT, $\overline{RESET}$
	C_{PIN}			10	pF	Other than pins INT, $\overline{RESET}$

RECOMMENDED OPERATING RANGE

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Supply Voltage	V_{DD1}	2.2	3.0	5.5	V	f_X = 4 MHz
	V_{DD2}	3.5	5.0	5.5	V	f_X = 8 MHz
Main Clock Oscillation Frequency	f_X	2.0	4.0	8.0	MHz	
Subclock Oscillation Frequency	f_{XT}		32.768		kHz	

DC CHARACTERISTICS (V_{DD} = 3 V, T_a = −20 to +75 °C, f_X = 4 MHz, f_{XT} = 32 kHz)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS	
LCD Output Voltage Variable Range	V_{LCD0}	0.8		1.8	V		
Doubler Output Voltage	V_{LCD1}	1.9 V_{LCD0}	2 V_{LCD0}		V		
Tripler Output Voltage	V_{LCD2}	2.85 V_{LCD0}	3 V_{LCD0}		V		
Low-voltage Detection Voltage	V_{DET}	1.3	2.0	2.9	V	VDET pin external resistance = 2 MΩ	
High-Level Input Voltage	V_{IH1}	0.8 V_{DD}		V_{DD}	V	$\overline{\text{RESET}}$ pin and INT pin	
	V_{IH2}	0.7 V_{DD}		V_{DD}	V	Other than $\overline{\text{RESET}}$ pin and INT pin	
Low-Level Input Voltage	V_{IL1}	0		0.2 V_{DD}	V	$\overline{\text{RESET}}$ pin and INT pin	
	V_{IL2}	0		0.3 V_{DD}	V	Other than $\overline{\text{RESET}}$ pin and INT pin	
High-Level Input Current	I_{IH1}			0.2	μA	INT	$V_{IH} = V_{DD}$
	I_{IH2}			0.2	μA	RESET	$V_{IH} = V_{DD}$
	I_{IH3}			0.2	μA	P0A-P0D	$V_{IH} = V_{DD}$
Low-Level Input Current	I_{IL1}			0.2	μA	INT	V_{IL} = 0 V
	I_{IL2}			0.2	μA	$\overline{\text{RESET}}$	V_{IL} = 0 V, w/o pull-up resistor
	I_{IL3}	20	50	100	μA		V_{IL} = 0 V w/pull-up resistor
	I_{IL4}			0.2	μA	P0A, P0B	V_{IL} = 0 V w/o pull-up resistor
	I_{IL5}	6	12	20	μA		V_{IL} = 0 V w/pull-up resistor
Low-Level Input Current	I_{IL6}			0.2	μA	P0C, P0D	V_{IL} = 0 V
High-Level Output Current	I_{OH1}	−0.6	−2.0	−4.0	mA	P0A, P0B	$V_{OH} = V_{DD}$-0.3 V
	I_{OH2}	−7.0	−15.0	−25.0	mA	REM	$V_{OH} = V_{DD}$-2 V
	I_{OH3}	−0.3	−1.0	−2.0	mA	LED	$V_{OH} = V_{DD}$-0.3 V
	I_{OH4}	−0.3	−1.0	−2.0	mA	$\overline{\text{VDOUT}}$	$V_{OH} = V_{DD}$-0.3 V

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS	
Low-Level Output Current	I_{OL1}	0.5	1.5	2.5	mA	P0A, P0B	V_{OL} = 0.3 V
	I_{OL2}	0.5	1.5	2.5	mA	P0C, P0D	V_{OL} = 0.3 V
	I_{OL3}	0.5	1.5	2.5	mA	REM	V_{OL} = 0.3 V
	I_{OL4}	0.5	1.5	2.5	mA	LED	V_{OL} = 0.3 V
	I_{OL5}	0.5	1.5	2.5	mA	$\overline{VDOUT}$	V_{OL} = 0.3 V
Common Output Current	I_{COM}	30			μA	Output voltage deviation = 0.2 V	
Segment Output Current	I_{LCD}	5			μA	Output voltage deviation = 0.2 V	
Supply Current	I_{DD1}		0.5	1.5	mA	Oepration mode	Both XT and X oscillate
	I_{DD2}		15	30	μA		Only XT oscillates
	I_{DD3}		0.5	1.5	mA	HALT mode	Both XT and X oscillate
	I_{DD4}		10	15	μA	STOP mode	Only XT oscillates

DC PROGRAMMING CHARACTERISTICS (T_a = 25 ± 5 °C, V_{DD} = 6.0 ± 0.25 V, V_{PP} = 12.5 ± 0.3 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
High-Level Input Voltage	V_{IH1}	0.7 V_{DD}		V_{DD}	V	Other than CLK
	V_{IH2}	V_{DD}-0.5		V_{DD}	V	CLK
Low-Level Input Voltage	V_{IL1}	0		0.3 V_{DD}	V	Other than CLK
	V_{IL2}	0		0.4	V	CLK
Input Leakage Current	I_{L1}			10	μA	V_{IN} = V_{IL} or V_{IH}
High-Level Output Voltage	V_{OH}	V_{DD}-1.0			V	I_{OH} = −1 mA
Low-Level Output Voltage	V_{OL}			0.4	V	I_{OL} = 1.6 mA
V_{DD} Supply Current	I_{DD}			30	mA	
V_{PP} Supply Current	I_{PP}			30	mA	MD0 = V_{IL}, MD1 = V_{IH}

Note 1: Keep V_{PP} to below +13.5 V, including the overshoot.

2: Apply V_{DD} before V_{PP}, and remove V_{DD} after V_{PP}.

AC PROGRAMMING CHARACTERISTICS (T_a = 25 ± 5 °C, V_{DD} = 6.0 ± 0.25 V, V_{PP} = 12.5 ± 0.3 V)

CHARACTERISTICS	SYMBOL	*1	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Address setup time*2 (vs. MD0 ↓)	t_{AS}	t_{AS}	2			μs	
MD1 setup time (vs. MD0 ↓)	t_{M1S}	t_{OES}	2			μs	
Data setup time (vs. MD0 ↓)	t_{DS}	t_{DS}	2			μs	
Address hold time*2 (vs. MD0 ↑)	t_{AH}	t_{AH}	2			μs	
Data hold time (vs. MD0 ↑)	t_{DH}	t_{DH}	2			μs	
MD0 ↑ → data output float delay time	t_{DF}	t_{DF}	0		130	ns	
V_{PP} setup time (vs. MD3 ↑)	t_{VPS}	t_{VPS}	2			μs	
V_{DD} setup time (vs. MD3 ↑)	t_{VDS}	t_{VCS}	2			μs	
Initial program pulse width	t_{PW}	t_{PW}	0.95	1.0	1.05	ms	
Additional program pulse width	t_{OPW}	t_{OPW}	0.95		21.0	ms	
MD0 setup time (vs. MD1 ↑)	t_{MOS}	t_{CES}	2			μs	
MD0 ↓ → data output delay time	t_{DV}	t_{DV}			1	μs	MD0=MD1=V_{IL}
MD1 hold time (vs. MD0 ↑)	t_{M1H}	t_{OEH}	2			μs	$t_{M1H}+t_{M1R}$ ≧ 50 μs
MD1 recovery time (vs. MD0 ↓)	t_{M1R}	t_{OR}	2			μs	
Program counter reset time	t_{PCR}	–	10			μs	
CLK input high-, low-level width	t_{XH}, t_{XL}	–	0.125			μs	
CLK Input Frequency	f_X	–			4.19	MHz	
Initial Mode Set Time	t_I	–	2			μs	
MD3 Setup Time (vs. MD1 ↑)	t_{M3S}	–	2			μs	
MD3 Hold Time (vs. MD1 ↓)	t_{M3H}	–	2			μs	
MD3 Setup Time (vs. MD0 ↓)	t_{M3SR}	–	2			μs	When program memory is read
Address*2 → Data Output Delay Time	t_{DAD}	t_{ACC}			2	μs	When program memory is read
Address*2 → Data Output Hold Time	t_{HAD}	t_{OH}	0		130	μs	When program memory is read
MD3 Hold Time (vs. MD0 ↑)	t_{M3HR}	–	2			μs	When program memory is read
MD3 ↓ → Data Output Float Delay Time	t_{DFR}	–	2			μs	When program memory is read
Reset Setup Time	t_{RES}		10			μs	

*1: Symbols for corresponding μPD27C256

*2: The internal address is incremented (+1) at the falling edge of third clock periods for the four CLK clock periods, which constitute one cycle. The internal address has no external pin connection.

4-BIT SINGLE-CHIP MICROCONTROLLER

The μPD17203A is a 4-bit CMOS microcontroller for infrared remote controllers. It contains 16K-bit static RAM, three channels of timers, a carrier generator for remote control, an amplifier for remote control receive signals, and a waveform shaping circuit in one chip.

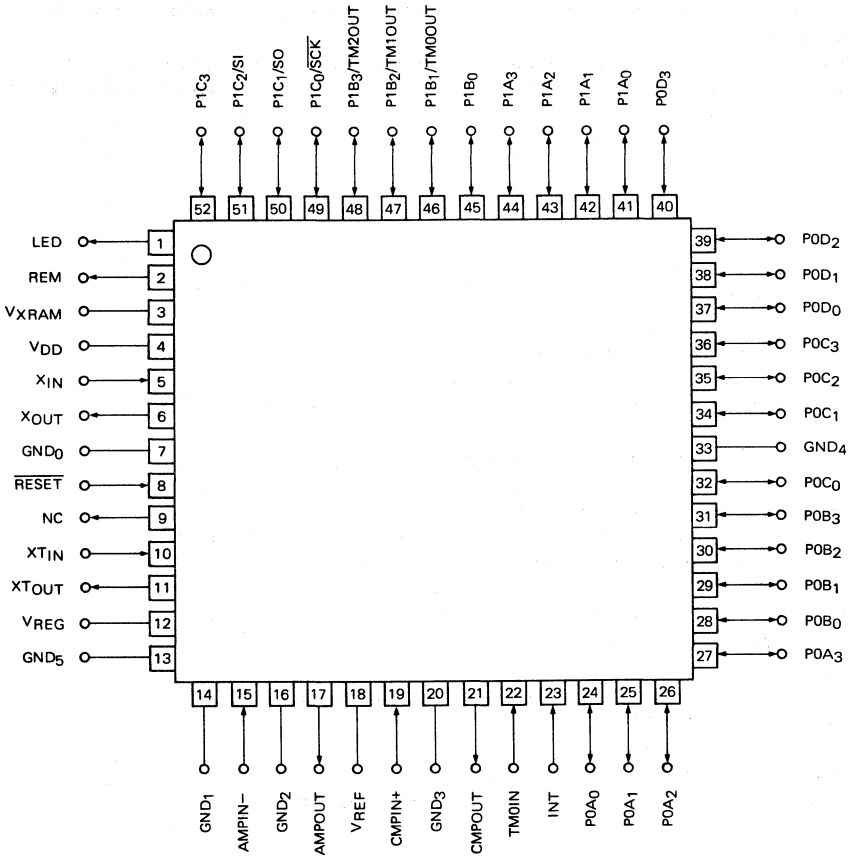
The 17K architecture used in the μPD17203A allows the user to perform an arithmetic/logical operation or data transfer between data memory locations or between data memory and a peripheral circuit with a single instruction. Every instruction is 1 word long, consisting of 16 bits.

The microcontroller is packaged in a 52-pin plastic QFP.

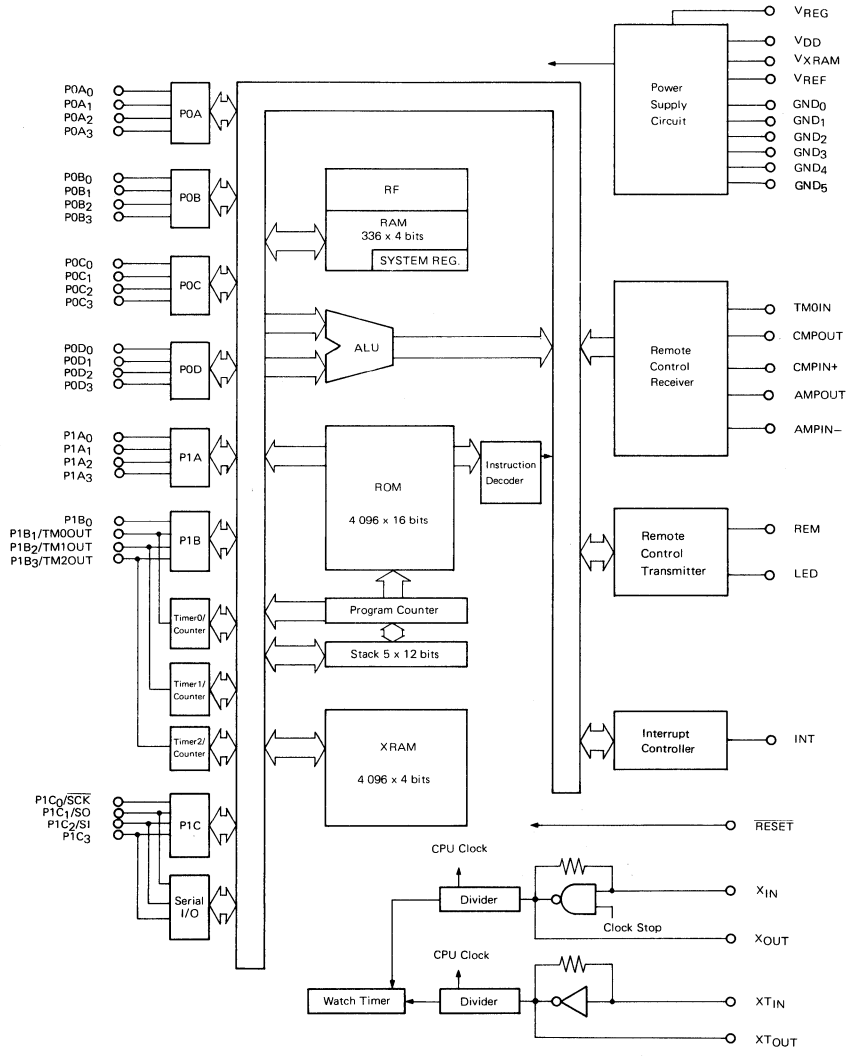
FEATURES

- 17K architecture
- Program memory (ROM): 8K bytes (4096 x 16 bits)
- Data memory (RAM): 336 words (336 x 4 bits)
- Static RAM: 16K bits (4096 x 4 bits)
- On-chip carrier generator for infrared remote control
- On-chip amplifier for infrared remote control receive signals
- On-chip waveform shaping circuit for infrared remote control receive signals
- Many input/output ports provided (28 lines)
- 3-wire serial interface contained (also used as a input/output port)
- 5 stack levels
- 8-bit timer: 1 channel (with a modulo function)
  Clock for the timer (8 μs, 16 μs, 64 μs, remote control carrier input)
- 10-bit timer: 1 channel (with a modulo function)
  Clock for the timer (0.5 μs, 4 μs, INT input)
- 16-bit timer: 1 channel (with a modulo function)
  Clock for the timer (8 μs, 16 μs, 32 μs, 64 μs)
- Clock timer: 1 channel (used as a watchdog timer or a clock)
- Instruction execution time: 4 μs (when a 4 MHz ceramic resonator is used)
- Standby function (STOP, HALT)
- Low-voltage detector contained
- Operating voltage: 2.2 to 5.5 V
- Operating clock: 4 MHz ceramic resonator/32.768 kHz crystal resonator

PIN CONFIGURATION (Top View)



BLOCK DIAGRAM



The μPD17P203A is provided with a one-time PROM in the place of the internal ROM in the μPD17203A.

Since a program can be written into the PROM for this microcomputer, it is suitable for experimental production or small-scale production of systems using μPD17203A.

It is recommended that you also read the separately available reference materials on μPD17203A.

FEATRUES

- Internal one-time PROM: 4,096 x 16 bits
- Single power source: 2.2 to 5.5 V

ORDERING INFORMATION

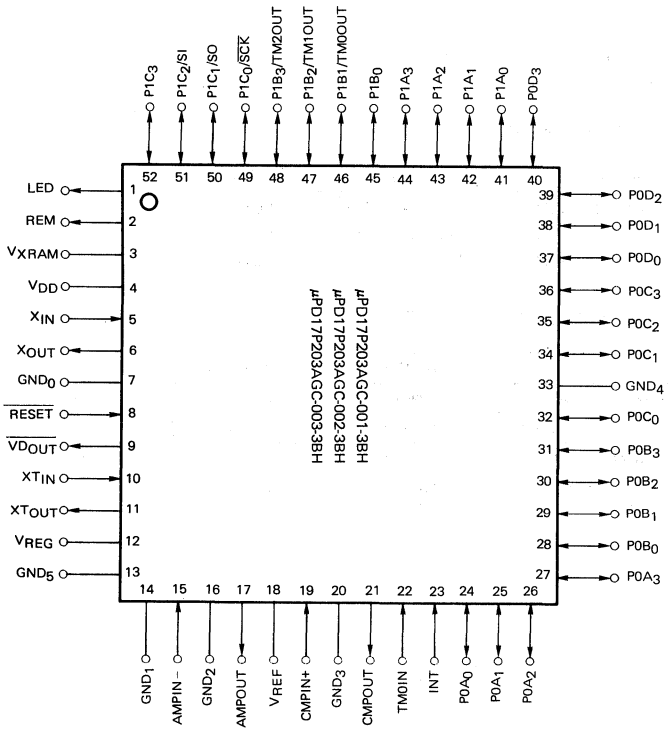
Order Code	Package	Quality Grade
μPD17P203AGC-001-3BH	52-pin plastic QFP	Standard
μPD17P203AGC-002-3BH	52-pin plastic QFP	Standard
μPD17P203AGC-003-3BH	52-pin plastic QFP	Standard

The differences among the above models are as follows:

Item	μPD17P203A-001	μPD17P203A-002	μPD17P203A-003	μPD17203A
$\overline{\text{RESET}}$ pin pull-up resistor	Provided	Not provided	Not provided	Mask option
P0A and P0B pins pull-up resistor	Provided	Provided	Not provided	Mask option
Main clock oscillator circuit	Provided	Provided	Not provided	Mask option
Subclock oscillator circuit	Provided	Not provided	Provided	Mask option

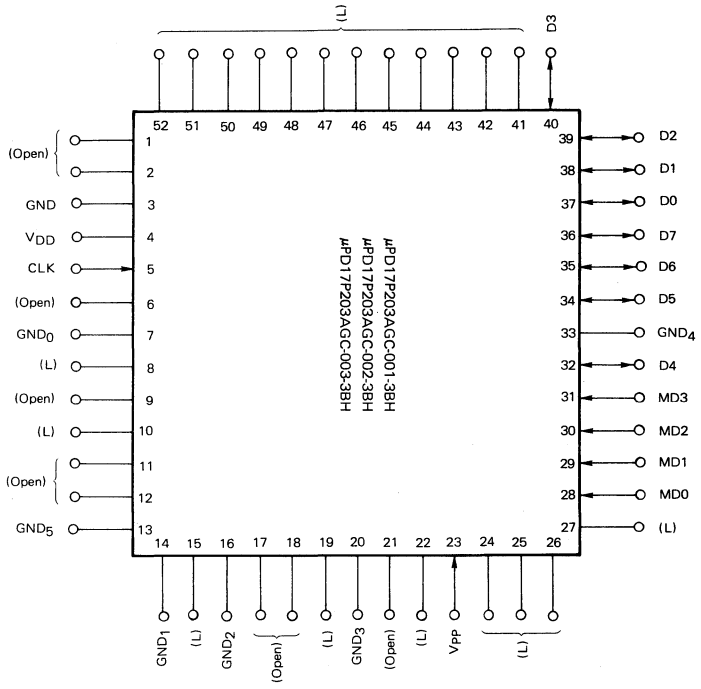
PIN CONFIGURATION (Top View)

(1) For Ordinary Operations



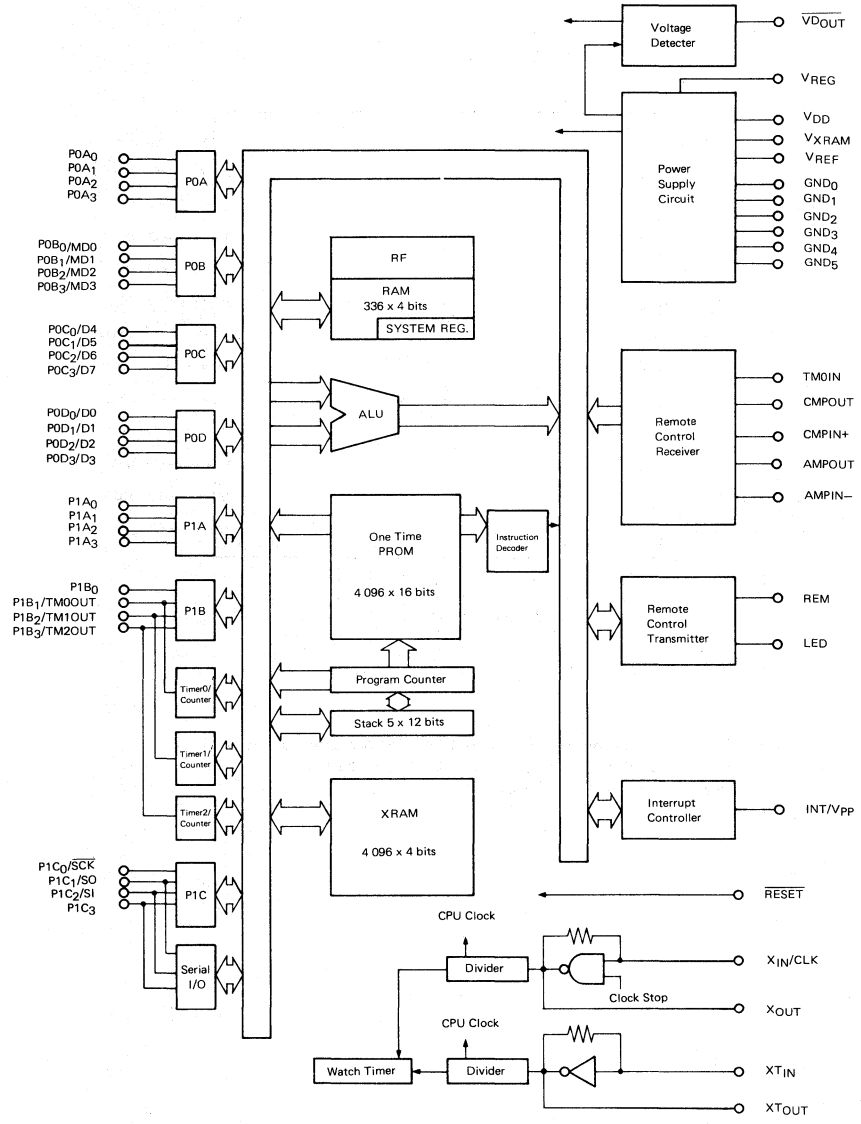
LED	:	Remote controller signal transmission output display
REM	:	Remote controller signal transmission output
X_{IN}, X_{OUT}	:	Main clock oscillator
$\overline{RESET}$	:	Reset input
$\overline{VD_{OUT}}$	:	Low voltage detector output
XT_{IN}, XT_{OUT}	:	Subclock oscillator
V_{REG}	:	Voltage regulator output
AMPIN−	:	Operational amplifier input
AMPOUT	:	Operational amplifier output
V_{REF}	:	Reference voltage output
CMPIN+	:	Comparator input
CMPOUT	:	Comparator output
TM0IN	:	Timer 0 input
INT	:	External interrupt input
TM0OUT	:	Timer 0 output
TM1OUT	:	Timer 1 output
TM2OUT	:	Timer 2 output
$\overline{SCK}$	:	Serial clock input/output
SO	:	Serial data output
SI	:	Serial data input
$P0A_0$–$P0A_3$	:	Port 0A
$P0B_0$–$P0B_3$	:	Port 0B
$P0C_0$–$P0C_3$	:	Port 0C
$P0D_0$–$P0D_3$	:	Port 0D
$P1A_0$–$P1A_3$	:	Port 1A
$P1B_0$–$P1B_3$	:	Port 1B
$P1C_0$–$P1C_3$	:	Port 1C
CLK	:	PROM clock input
MD0–MD3	:	PROM mode selection
D0–D7	:	PROM data input/output
V_{PP}	:	PROM power
V_{DD}	:	Power
V_{XRAM}	:	XRAM power
GND	:	Ground

(2) PROM programming mode



Note: ( ) indicates processing of pins not used in the PROM programming mode.
L : Ground each of these pins through a resistor (470 Ω).
Open : Connect nothing to these pins.

BLOCK DIAGRAM



1. PIN FUNCTIONS

1.1 PORT PINS

Symbol	I/O	Shared by: *	Function	At reset
$P0A_0$–$P0A_3$	I/O	–	4-bit I/O port (Port 0A). Can be set in input or output mode in 4 bit units. Pull-up resistors are connected in I/O mode.	Input
$P0B_0$–$P0B_3$	I/O	(MD0–MD3)	4-bit I/O port (Port 0B). Can be set in input or output mode in 4 bit units. Pull-up resistors are connected in I/O mode.	Input
$P0C_0$–$P0C_3$	I/O	(D4–D7)	4-bit I/O port (Port 0C). Can be set in input or output mode in 4 bit units. N-ch open-drain in output mode.	Input
$P0D_0$–$P0D_3$	I/O	(D0–D3)	4-bit I/O port (Port 0D). Can be set in input or output mode in units of 4 bits. N-ch open-drain in output mode.	Input
$P1A_0$–$P1A_3$	I/O	–	4-bit I/O port (Port 1A). Can be set in input or output mode in bit units. N-ch open-drain in output mode. Pull-up resistor can be connected by program in I/O mode.	Input
$P1B_0$	I/O	–	4-bit I/O port (Port 1B). Can be set in input or output mode in bit units. N-ch open drain in output mode. Pull-up resistor can be connected by program in I/O mode.	Input
$P1B_1$–$P1B_3$		TM0OUT–TM2OUT		
$P1C_0$	I/O	$\overline{SCK}$	4-bit I/O port (Port 1C). Can be set in input or output mode in bit units. Pull-up resistor can be connected by program in I/O mode.	Input
$P1C_1$		SO		
$P1C_2$		SI		
$P1C_3$		–		

*( ): Pins shared in PROM programming mode.

1.2 PINS OTHER THAN PORT PINS (IN ORDINARY OPERATION MODE)

Symbol	I/O	Shared by:	Function	At reset
LED	Output	–	For display of infrared remote controller signal output	Low-level output
REM	Output	–	Infrared remote controller signal output	Low-level output
X_{IN}	Input	–	For main clock oscillator. Connect 4 MHz ceramic oscillator to these pins.	–
X_{OUT}	Output	–		
$\overline{RESET}$	Input	–	RESET signal input	–
$\overline{VDOUT}$	Output	–	Low-voltage detector circuit output	–
XT_{IN}	Input	–	For subclock oscillator	–
XT_{OUT}	Output	–		–
V_{REG}	Output	–	Output from voltage regulator for subclock oscillator	–
AMPIN–	Input	–	Inverted input from internal operational amplifier	–
AMPOUT	Output	–	Internal operational amplifier output	–
V_{REF}	Output	–	Reference voltage output	–
CMPIN+	Input	–	Non-inverted input for comparator	–
CMPOUT	Output	–	Comparator output	–
TM0IN	Input	–	Clock input to timer 0	–
INT	Input	(V_{PP})	External interrupt signal input	–
V_{DD}	–	–	Power	–
V_{XRAM}	–	–	Power to XRAM	–
GND_0–GND_5	–	–	Ground	–

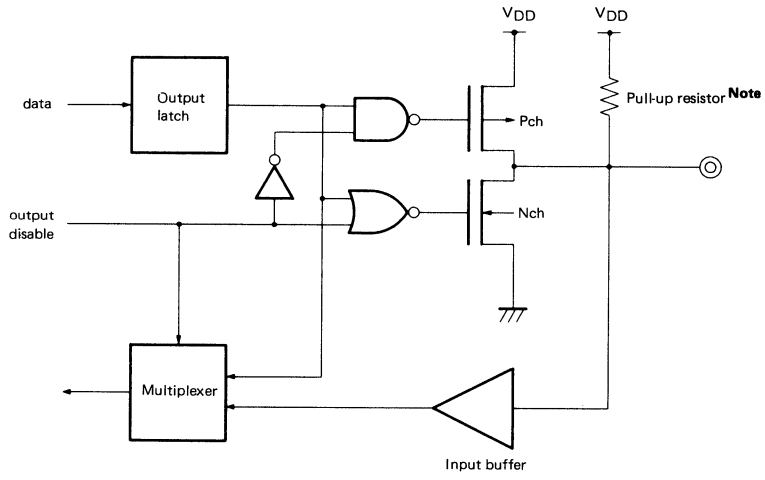
1.3 PINS OTHER THAN PORT PINS (IN PROM PROGRAMMING MODE)

Symbol	I/O	Shared by:	Function	At reset
CLK	Input	X_{IN}	Address updating clock input	–
D0–D3	I/O	$P0D_0$–$P0D_3$	8-bit data input/output	Input
D4–D7		$P0C_0$–$P0C_3$		
MD0–MD3	Input	$P0B_0$–$P0B_3$	Operation mode selection	Input
V_{PP}	–	INT	Applies program voltage (12.5 V). Used as INT pin in ordinary operation mode.	–

1.4 INPUT/OUTPUT CIRCUITS

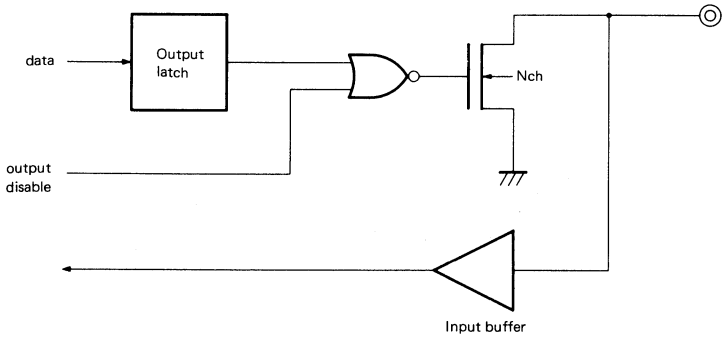
The input/output circuit for each μPD17P203A's pin are shown below.

(1) $P0A_0$–$P0A_3$, $P0B_0$/MD0–$P0B_3$/MD3

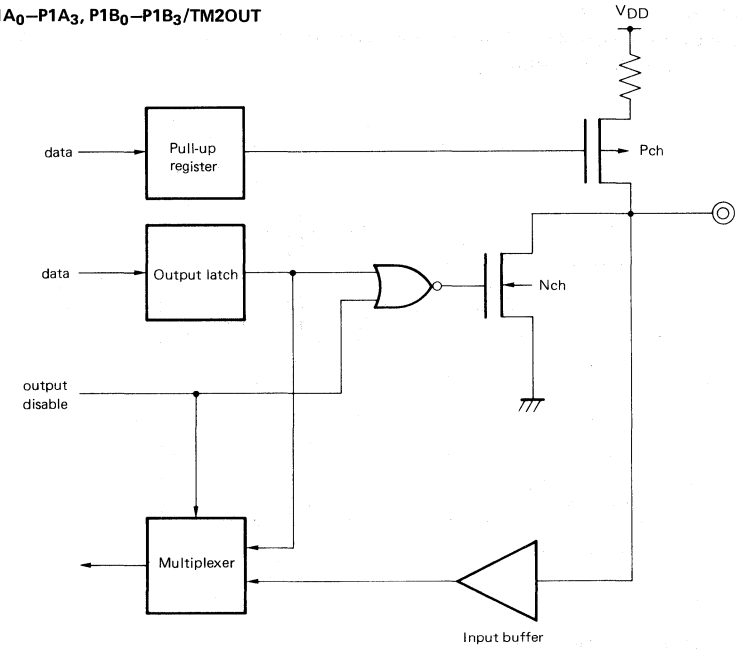


Note: μPD17P203A-001 and -002 only.

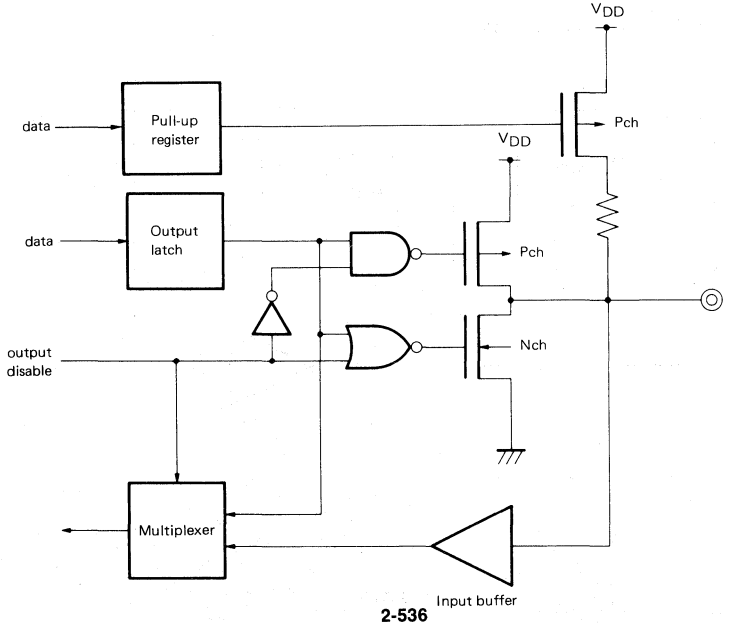
(2) $P0C_0$/D4–$P0C_3$/D7, $P0D_0$/D0–$P0D_3$/D3



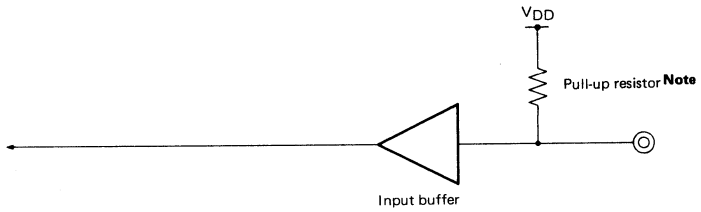
(3) $P1A_0$–$P1A_3$, $P1B_0$–$P1B_3$/TM2OUT



(4) $P1C_0/\overline{SCK}$–$P1C_3$



(3) $\overline{\text{RESET}}$



Note: μPD17P203A-001 only.

2. DIFFERENCES BETWEEN μPD17P203A AND μPD17203A

Since μPD17P203A replaces the internal mask ROM for μPD17203A with a PROM that can be written by the user, the only differences between the two microcomputers are the program memory and mask option. Their CPU functions and internal hardware are essentially the same. The following table lists the differences between μPD17P203A and μPD17203A.

Refer to the μPD17203A Data Sheet for the CPU functions and internal hardware for μPD17P203A.

Item \ Product name	μPD17P203A-001	μPD17P203A-002	μPD17P203A-003	μPD17203A
Program memory	• PROM • 0000H-0FFFH • 4,096 x 16 bits			• Mask ROM • 0000H-0FFFH • 4,096 x 16 bits
Pull-up resistor for $\overline{\text{RESET}}$ pin	Provided	Not provided	Not provided	Mask option
Pull-up resistor for P0A and P0B pins	Provided	Provided	Not provided	Mask option
Main clock oscillator circuit	Provided	Provided	Not provided	Mask option
Subclock oscillator circuit	Provided	Not provided	Provided	Mask option
Pin connection	V_{PP} and PROM programming pins are provided			V_{PP} and PROM programming pins are not provided
Operating voltage range	2.2 to 5.5 V			
Package	52-pin plastic QFP			

3. WRITING, READING, AND VERIFYING ONE-TIME PROM (PROGRAM MEMORY)

The μPD17P203A internal program memory is a one-time 4,096 x 16 bit PROM.

The write, read, and verify this one-time PROM, the pins shown in the following table are used. Note that no address input pin is provided. Instead, the address is updated by the clock signal input from the CLK pin.

Pin	Function
V_{PP}	Program voltage application
CLK	Address updating clock input
MD0–MD3	Operation mode selection
D0–D7	8-bit data input/output

3.1 OPERATION MODES WHEN PROGRAM MEMORY IS WRITTEN, READ, OR VERIFIED

μPD17P203A is set in the program memory write, read, and verify mode, when, +6 V is applied to the V_{DD} pin and +12.5 V is applied to the V_{PP} pin after it has been reset for a certain period of time (V_{DD} = 5 V, $\overline{RESET}$ = 0 V). Once this mode has been set, the following operation modes are available, depending on the setting of the MD0 through MD3 pins. Note that all the unused pins are pulled down with resistors to the ground potential.

Operation mode setting						Operation mode
V_{PP}	V_{DD}	MD0	MD1	MD2	MD3	
+12.5 V	+6 V	H	L	H	L	Program memory address 0 clear
		L	H	H	H	Write mode
		L	L	H	H	Read and verify mode
		H	X	H	H	Program inhibit mode

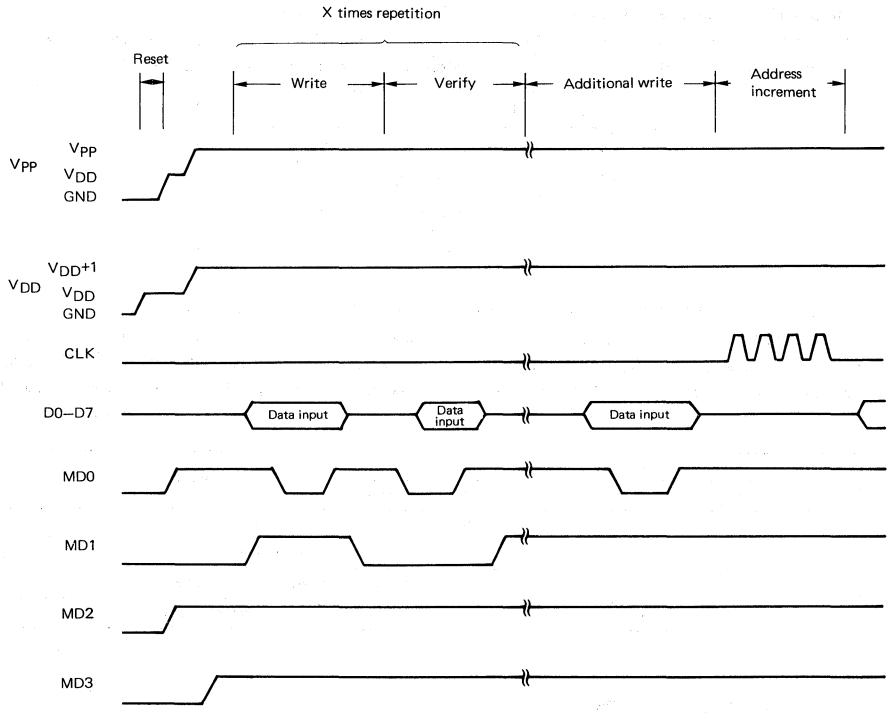
X: L or H

3.2 PROGRAM MEMORY WRITING PROCEDURE

The program memory can be written in the following procedure at high speeds:

(1) Pull down the unused pins with resistors to the ground potential. Make the CLK pin low.
(2) Apply 5 V to the V_{DD} pin. Make the V_{PP} pin low.
(3) Wait for 10 μs. Then apply 5 V to the V_{PP} pin.
(4) Set the program memory address 0 clear mode by using the mode selection pins.
(5) Apply 6 V to V_{DD} and 12.5 V to V_{PP}.
(6) Set the program inhibit mode.
(7) Write data in the 1 ms write mode.
(8) Set the program inhibit mode.
(9) Set the verify mode. If the data has been correctly written, proceed to step (10). If not, repeat (7) through (9).
(10) Additional write for (the number of times (7) through (9) are repeated: X) x 1 ms.
(11) Set the program inhibit mode.
(12) Input a pulse to the CLK pin four times to increment the program memory address by one.
(13) Repeat (7) through (12) until the last address is written.
(14) Set the program memory address 0 clear mode.
(15) Apply 5 V to the V_{DD} and V_{PP} pins.
(16) Turn off power.

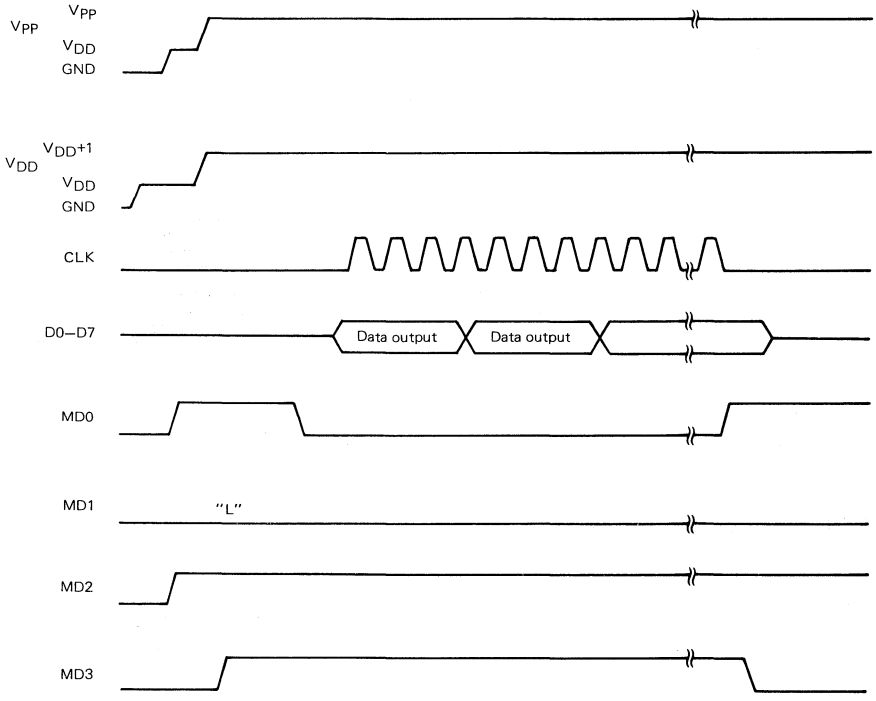
Steps (2) through (12) are illustrated below.



3.3 PROGRAM MEMORY READING PROCEDURE

(1) Pull down the unused pins with resistors to the ground potential. Make the CLK pin low.
(2) Apply 5 V to the V_{DD} pin. Make the V_{PP} pin low.
(3) Wait for 10 μs. Then apply 5 V to the V_{PP} pin.
(4) Set the program memory address 0 clear mode by using the mode selection pins.
(5) Apply 6 V to V_{DD} and 12.5 V to V_{PP}.
(6) Set the program inhibit mode.
(7) Set the verify mode. Input the clock pulse to the CLK pin. Data for one address is output each time the pulse is input four times.
(8) Set the program inhibit mode.
(9) Set the program memory address 0 clear mode.
(10) Apply 5 V to the V_{DD} and V_{PP} pins.
(11) Turn off power.

Steps (2) through (9) are illustrated below.



4. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage	V_{DD}	−0.3 to +7.0	V
Input Voltage	V_I	−0.3 to V_{DD} +0.3	V
Operating Temperature	T_{opt}	−20 to +75	°C
Storage Temperature	T_{stg}	−40 to +125	°C

RECOMMENDED OPERATING RANGE

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Supply Voltage	V_{DD1}	2.2	3.0	5.5	V	f_X = 4 MHz
	V_{DD2}	3.5	5.0	5.5	V	f_X = 8 MHz
XRAM Supply Voltage	V_{XRAM}	1.3		V_{DD}	V	$V_{XRAM} \leqq V_{DD}$
Main Clock Oscillation Frequency	f_X	2.0	4.0	8.0	MHz	
Subclock Oscillation Frequency	f_{XT}		32.768		kHz	

CAPACITANCE (T_a = 25 °C, V_{DD} = 0 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Input Capacitance	C_{IN}			10	pF	INT, $\overline{\text{RESET}}$ pins
	C_{PIN}			10	pF	Other than INT, $\overline{\text{RESET}}$ pin

DC CHARACTERISTICS (V_{DD} = 3 V, T_a = −20 to +75 °C, f_X = 4 MHz, f_{XT} = 32 kHz)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION	
Low Voltage Detection Voltage	V_{DET}	1.3	2.0	2.9	V		
High-Level Input Voltage	V_{IH1}	0.8 V_{DD}		V_{DD}	V	$\overline{RESET}$, INT pins	
	V_{IH2}	0.7 V_{DD}		V_{DD}	V	Other than $\overline{RESET}$, INT pins	
Low-Level Input Voltage	V_{IL1}	0		0.2 V_{DD}	V	$\overline{RESET}$, INT pins	
	V_{IL2}	0		0.3 V_{DD}	V	Other than $\overline{RESET}$, INT pins	
High-Level Input Current	I_{IH1}			0.2	μA	INT	$V_{IH} = V_{DD}$
	I_{IH2}			0.2	μA	TM0IN	$V_{IH} = V_{DD}$
	I_{IH3}			0.2	μA	$\overline{RESET}$	$V_{IH} = V_{DD}$
	I_{IH4}			0.2	μA	P0A–P0D	$V_{IH} = V_{DD}$
	I_{IH5}			0.2	μA	P1A–P1C	$V_{IH} = V_{DD}$
Low-Level Input Current	I_{IL1}			−0.2	μA	INT	V_{IL} = 0 V
	I_{IL2}			−0.2	μA	TM0IN	V_{IL} = 0 V
	I_{IL3}			−0.2	μA	$\overline{RESET}$	V_{IL} = 0 V w/o pull-up resistor
	I_{IL4}	−20	−50	−100	μA		I_{IL} = 0 V w/pull-up resistor
	I_{IL5}	−6	−12	−20	μA	P0A, P0B	V_{IL} = 0 V w/pull-up resistor
	I_{IL6}			−0.2	μA	P0C, P0D	V_{IL} = 0 V
	I_{IL7}			−0.2	μA	P1A–P1C	V_{IL} = 0 V w/o pull-up resistor
	I_{IL8}	−20	−50	−90	μA		I_{IL} = 0 V w/pull-up resistor
High-Level Output Current	I_{OH1}	−0.6	−2.0	−4.0	mA	P0A, P0B	$V_{OH} = V_{DD}-0.3$ V
	I_{OH2}	−0.6	−2.0	−4.0	mA	P1C	$V_{OH} = V_{DD}-0.3$ V
	I_{OH3}	−7.0	−15.0	−25.0	mA	REM	$V_{OH} = V_{DD}-2$ V
	I_{OH4}	−0.3	−1.0	−2.0	mA	LED	$V_{OH} = V_{DD}-0.3$ V
	I_{OH5}	−0.3	−1.0	−2.0	mA	$\overline{VD_{OUT}}$	$V_{OH} = V_{DD}-0.3$ V
	I_{OH6}	−0.3	−1.0	−2.0	mA	CMPOUT	$V_{OH} = V_{DD}-0.3$ V
Low-Level Output Current	I_{OL1}	0.5	1.5	2.5	mA	P0A, P0B	V_{OL} = 0.3 V
	I_{OL2}	0.5	1.5	2.5	mA	P0C, P0D	V_{OL} = 0.3 V
	I_{OL3}	0.5	1.5	2.5	mA	REM	V_{OL} = 0.3 V
	I_{OL4}	0.5	1.5	2.5	mA	LED	V_{OL} = 0.3 V
	I_{OL5}	0.5	1.5	2.5	mA	$\overline{VD_{OUT}}$	V_{OL} = 0.3 V
	I_{OL6}	0.5	1.5	2.5	mA	CMPOUT	V_{OL} = 0.3 V
V_{REF} Output Voltage	V_{REF}	0.8	1.2	1.6	V	External capacitance for V_{REF} pin = 0.1 μF	
Supply Current	I_{DD1}	0.5	1.0	2.0	mA	Operation mode	XT and X
	I_{DD2}		15	30	μA		Only XT
	I_{DD3}			2.0	mA	HALT mode	XT and X
	I_{DD4}		10	15	μA		Only XT
XRAM Hold Voltage	V_{XRAM}	1.3	3.0	5.5	V	Operation mode, V_{XRAM} = 3 V	
XRAM Supply Current	I_{XRAM1}		3.0		μA	HALT mlde, V_{XRAM} = 3 V, T_a = 25 °C	
	I_{XRAM2}		0.2	1.0	μA		

DC PROGRAMMING CHARACTERISTICS (T_a = 25 °C, V_{DD} = 6.0±0.25 V, V_{PP} = 12.5±0.5 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
High-Level Input Voltage	V_{IH1}	0.7 V_{DD}		V_{DD}	V	Other than CLK
	V_{IH2}	V_{DD}–0.5		V_{DD}	V	CLK
Low-Level Input Voltage	V_{IL1}	0		0.3 V_{DD}	V	Other than CLK
	V_{IL2}	0		0.4	V	CLK
Input Leakage Current	I_{L1}			10	μA	$V_{IN} = V_{IL}$ or V_{IH}
High-Level Output Voltage	V_{OH}	V_{DD}–1.0			V	I_{OH} = –1 mA
Low-Level Output Voltage	V_{OL}			0.4	V	I_{OL} = 1.6 mA
V_{DD} Supply Current	I_{DD}			30	mA	
V_{PP} Supply Current	I_{PP}			30	mA	MD0 = V_{IL}, MD1 = V_{IH}

Note: 1. Keep V_{PP} to less than +13.5 V, including the overshoot.

2. Apply V_{DD} before V_{PP}. Remove V_{DD} after V_{PP}.

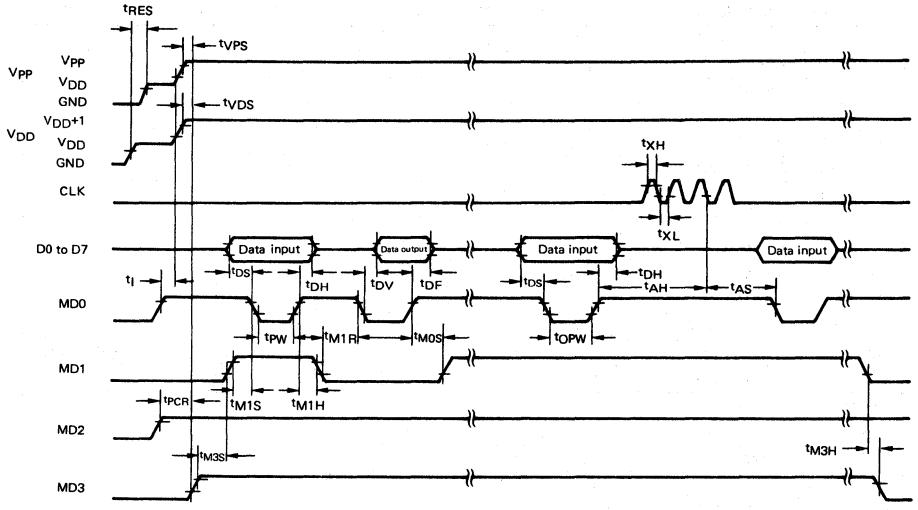
AC PROGRAMMING CHARACTERISTICS (T_a = 25 °C, V_{DD} = 6.0±0.25 V, V_{PP} = 12.5±0.5 V)

CHARACTERISTICS	SYMBOL	*1	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Address Setup Time*2 (vs. MD0 ↓)	t_{AS}	t_{AS}	2			μs	
MD1 Setup Time (vs. MD0 ↓)	t_{MIS}	t_{OES}	2			μs	
Data Setup Time (vs. MD0 ↓)	t_{DS}	t_{DS}	2			μs	
Address Hold Time*2 (vs. MD0 ↑)	t_{AH}	t_{AH}	2			μs	
Data Hold Time (vs. MD0 ↑)	t_{DH}	t_{DH}	2			μs	
MD0 ↑→Data Output Float Delay Time	t_{DF}	t_{DF}	0		130	ns	
Vpp Setup Time (vs. MD3 ↑)	t_{VPS}	t_{VPS}	2			μs	
V_{DD} Setup Time (vs. MD3 ↑)	t_{VDS}	t_{VCS}	2			μs	
Initial Program Pulse Width	t_{PW}	t_{PW}	0.95	1.0	1.05	ms	
Additional Program Pulse Width	t_{OPW}	t_{OPW}	0.95		21.0	ms	
MD0 Setup Time (vs. MD1 ↑)	t_{MOS}	t_{CES}	2			μs	
MD0 ↓→Data Output Delay Time	t_{DV}	t_{DV}			1	μs	MD0 = MD1 = V_{IL}
MD1 Hold Time (vs. MD0 ↑)	t_{M1H}	t_{OEH}	2			μs	$t_{M1H} + t_{M1R} \geqq 50$ μs
MD1 Recovery Time (vs. MD0 ↓)	t_{M1R}	t_{OR}	2			μs	
Program Counter Reset Time	t_{PCR}	–	10			μs	
CLK Input High, Low Level Widths	t_{XH}, t_{XL}	–	0.063			μs	
CLK Input Frequency	f_X	–			8	MHz	
Initial Mode Set Time	t_I	–	2			μs	
MD3 Setup Time (vs. MD1 ↑)	t_{M3S}	–	2			μs	
MD3 Hold Time (vs. MD1 ↓)	t_{M3H}	–	2			μs	
MD3 Setup Time (vs. MD0 ↓)	t_{M3SR}	–	2			μs	When program memory is read
Address*2 → Data Output Delay Time	t_{DAD}	t_{ACC}			2	μs	When program memory is read
Address*2 → Data Output Hold Time	t_{HAD}	t_{OH}	0		130	ns	When program memory is read
MD3 Hold Time (vs. MD0 ↑)	t_{M3HR}	–	2			μs	When program memory is read
MD3 ↓→Data Output Float Delay Time	t_{DFR}	–	2			μs	When program memory is read
Reset Setup Time	t_{RES}		10			μs	

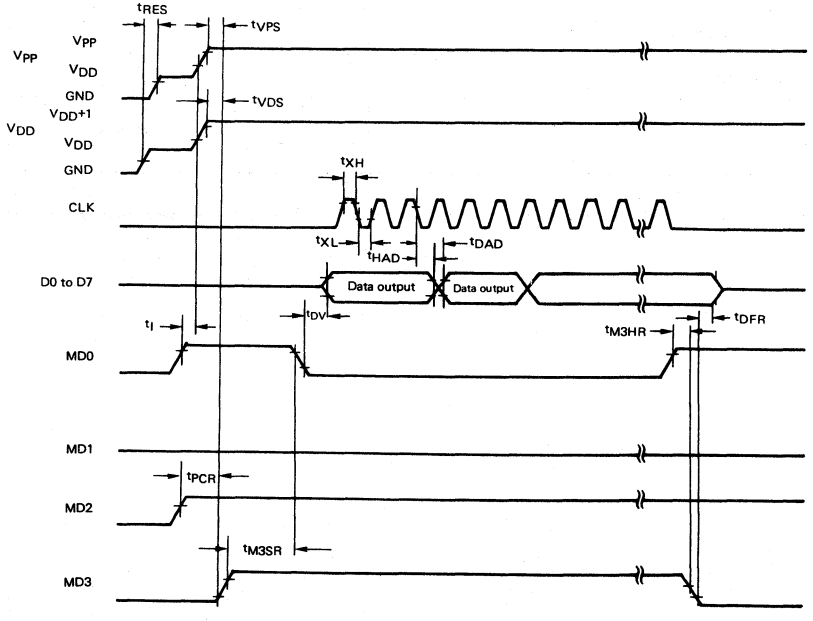
*1. Corresponding symbols of μPD27C256.

*2. The internal address signal is incremented by one at the falling edge of the third CLK input signal and is not connected to a pin.

PROGRAM MEMORY WRITE TIMING



PROGRAM MEMORY READ TIMING



4-BIT SINGLE-CHIP MICROCONTROLLER

The μPD17204 is a 4-bit CMOS microcontroller with an 8K-bit RAM, a 3-channel timer, a remote controlled carrier generator, a remote controlled receive signal amplifier and a waveform rectifier integrated on a single-chip for infrared remote controller.

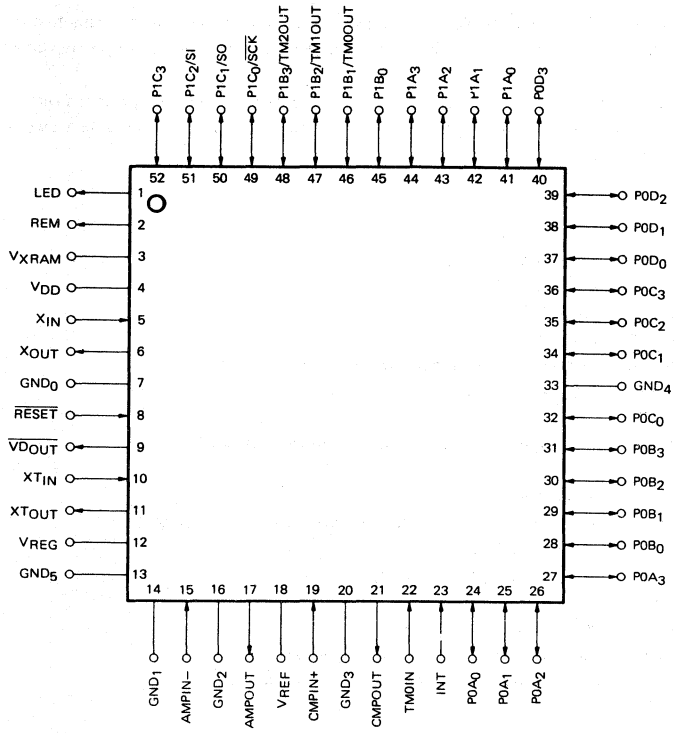
The μPD17204 employs the μPD17000 architecture and can execute data transfer and operations with one instruction between data memories or between a data memory and peripheral circuits. All instructions are a 16-bit word.

52-pin plastic QFP package is used.

FEATURES

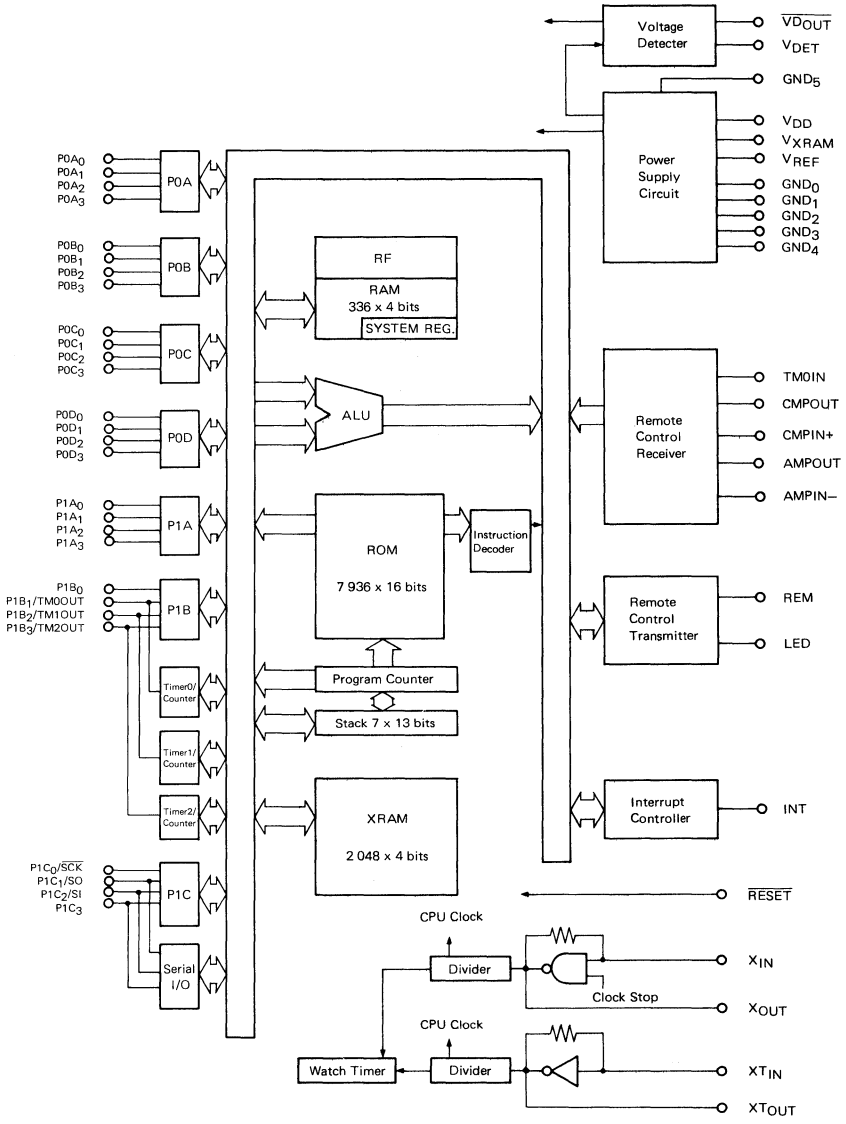
- μPD17000 architecture is employed.
- Program memory (ROM): 16K bytes (7936 x 16 bits)
- Data memory (RAM): 336 words (336 x 4 bits)
- Static RAM: 8K bits (2048 x 4 bits)
- On-chip infrared remote controlled carrier generator
- On-chip infrared remote controlled receive signal amplifier
- Variety of I/O ports (28 ports)
- On-chip 3-wire serial interface (which also serves as an input/output port)
- Stack level: 7 levels
- 8-bit timer: 1 channel (with modulo function)
  Timer clock (8 μs, 16 μs and 64 μs remote controlled carrier inputs)
- 10-bit timer: 1 channel (with modulo function)
  Timer clock (0.5 μs and 4 μs, INT input)
- 16-bit timer: 1 channel
  Timer clock (8 μs, 16 μs, 32 μs, 64 μs)
- Watch timer: 1 channel (which also serves as a watchdog timer)
- Instruction execution time: 4 μs (when 4 MHz ceramic oscillator is used)
- Standby function (STOP, HALT)
- On-chip low-voltage detector
- Operating voltage range: 2.2 to 5.5 V
- Operating clock: 4 MHz ceramic resonator/32.768 kHz crystal resonator
- OTP product: μPD17P204GC is available.

PIN CONFIGURATION (Top View)



LED	: Remote controlled transmit output display pin
REM	: Remote controlled transmit output
X_{IN}, X_{OUT}	: Main clock oscillator connect pin
$\overline{RESET}$	: Reset input pin
$\overline{VD_{OUT}}$	: Low-voltage detector output pin
XT_{IN}, XT_{OUT}	: Subclock oscillator connect pin
V_{REG}	: Subclock voltage regulator output pin
AMPIN−	: Operation amplifier input pin
AMPOUT	: Operation amplifier output pin
V_{REF}	: Reference voltage output pin
CMPIN+	: Comparator input pin
CMPOUT	: Comparator output pin
TM0IN	: Timer 0 input pin
INT	: External interrupt input pin
TM0OUT	: Timer 0 output pin
TM1OUT	: Timer 1 output pin
TM2OUT	: Timer 2 output pin
$\overline{SCK}$	: Serial clock input/output pin
SO	: Serial data output pin
SI	: Serial data input pin
$P0A_0$ to $P0A_3$	: Input/output ports
$P0B_0$ to $P0B_3$	: Input/output ports
$P0C_0$ to $P0C_3$	: Input/output ports
$P0D_0$ to $P0D_3$	: Input/output ports
$P1A_0$ to $P1A_3$	: Input/output ports
$P1B_0$ to $P1B_3$	: Input/output ports
$P1C_0$ to $P1C_3$	: Input/output ports
V_{DD}	: Power supply
V_{XRAM}	: XRAM power supply
GND	: Ground

BLOCK DIAGRAM



FUNCTIONAL COMPARISON BETWEEN μPD17203A AND μPD17204

Product Name	μPD17203A	μPD17204
ROM	4096 x 16 bits	7936 x 16 bits
RAM	336 x 4 bits	
SRAM	4096 x 4 bits	2048 x 4 bits
Instruction execution time	4 μs (when 4 MHz ceramic oscillator is used)	
Stack level	5 levels	7 levels
Input/output port	28 ports	
Serial interface	8-bit 3-wire: 1 channel	
Interrupt	7 channels External interrupt: 1 channel Internal interrupt: 6 channel	
Timer	4 systems 8-bit timer 10-bit timer 16-bit timer Watch timer (which also serves as a watchdog timer)	
Standby function	STOP mode, HALT mode	
Recommended operating voltage range	V_{DD} = 2.2 to 5.5 V	
Package	52-pin plastic QFP	

4-BIT SINGLE-CHIP MICROCONTROLLER

The μPD17301 is a 4-bit single-chip microcontroller with on-chip DTMF generator, DTMF receiver, and abbreviated dial memory.

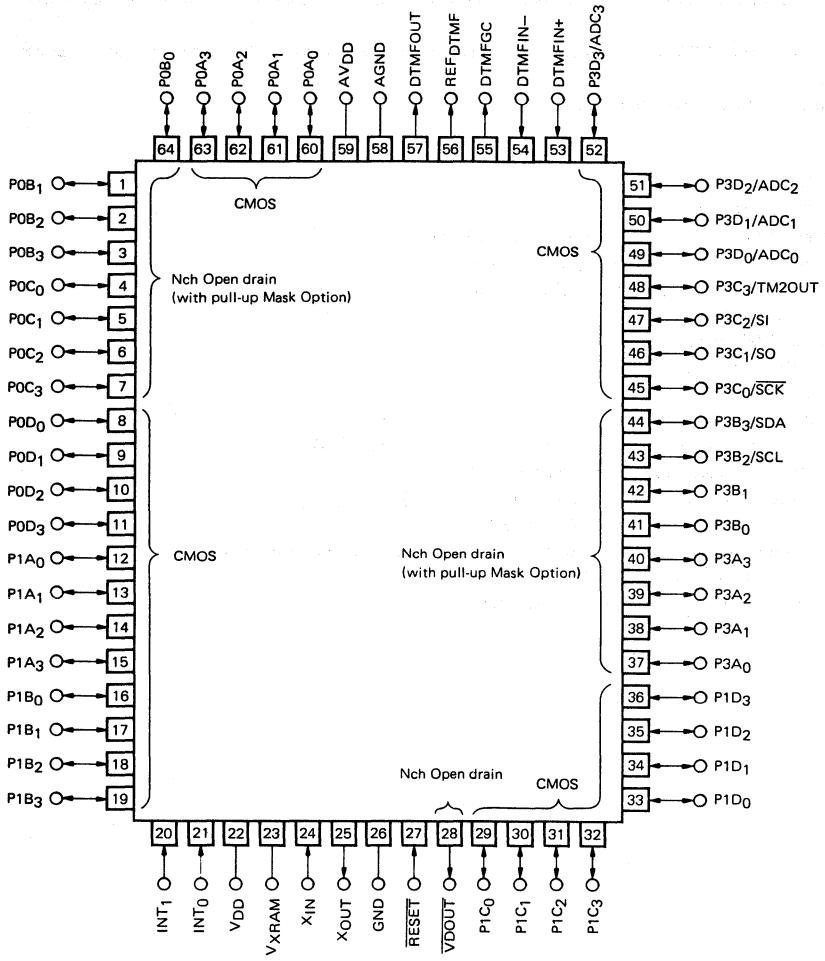
The CPU uses μPD17000 architecture. Since all instructions have a 16-bit word configuration, efficient programming is possible.

The package is a 64-pin plastic QFP.

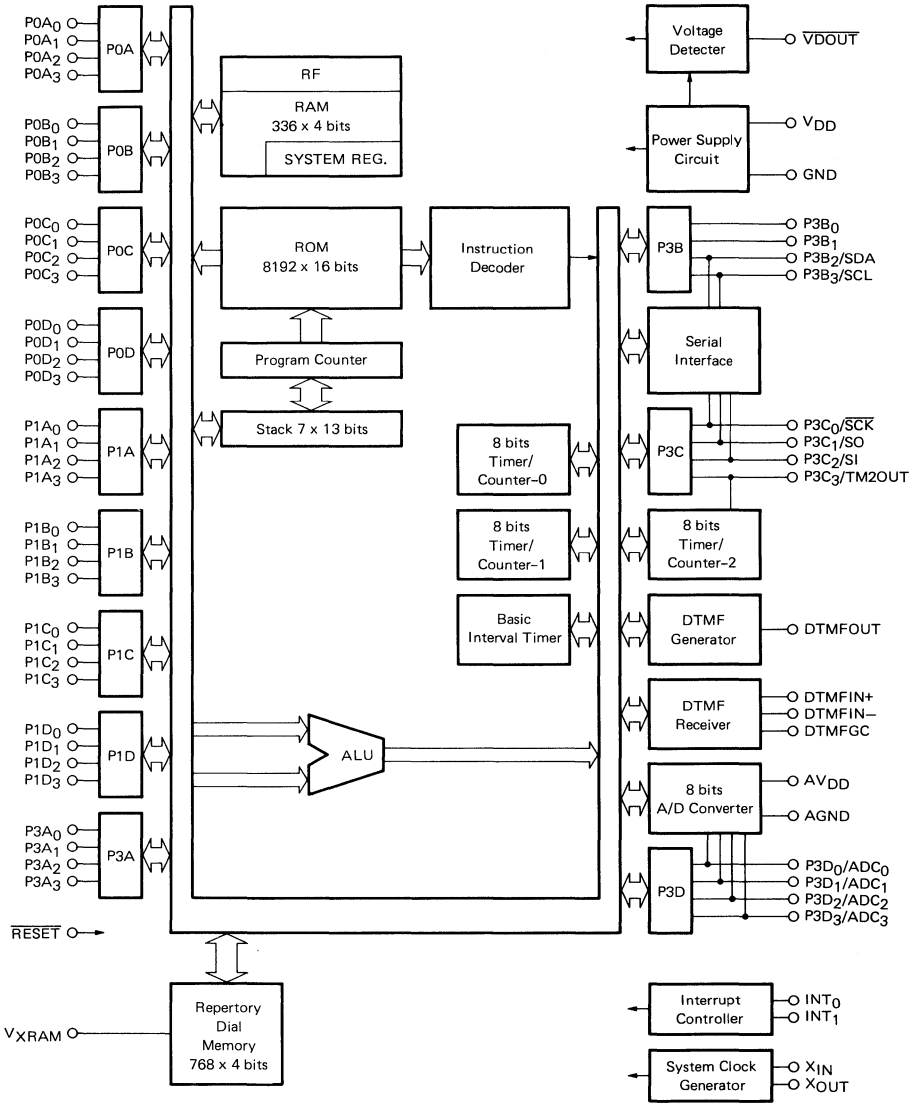
FEATURES

- μPD17000 architecture
- Program memory (ROM): 16K bytes (8192 x 16 bits)
- Data memory (RAM): 336 words (336 x 4 bits)
- Repertory dial memory 768 words (768 x 4 bits)
- On-chip DTMF generator
- On-chip DTMF receiver
- Serial interfaces: 2ch
- Abundant I/O ports: 48
- 8-bit A/D converter: 4ch
- Abundant interupt functions (external cause: 2, internal cause: 7)
- Stack level: 7 levels (multiple interrupt: max. 3 levels)
- Timer: 4 (8-bit modulo timer: 3, basic interval timer: 1)
- Standby function (STOP mode, HALT mode)
- Instruction execution time: 2.23 μs (when 3.58 MHz ceramic oscillator used)
- Operating voltage range: 2.0 to 5.5 V
- Program evaluation OTP product: μPD17P301GF

PIN CONFIGURATION (Top View)



μPD17301 BLOCK DIAGRAM



4-BIT SINGLE-CHIP MICROCONTROLLER FOR VCR CAMERA

μPD17401 is a 4-bit single-chip microcontroller for the home VCR camera with an on-chip image display controller and LCD controller/driver.

The Image Display Controller (IDC) has various screen display functions. It can display graphics as well as characters. All the display fonts are user-programmable and can be specified freely. Debugging is possible while actually outputting these displays from the time of the program development.

It has an on-chip LCD controller/driver for displaying the operating condition of the camera and serial interface circuit for communication with peripheral devices. It also has an on-chip 6-bit A/D converter and 32 kHz clock counter.

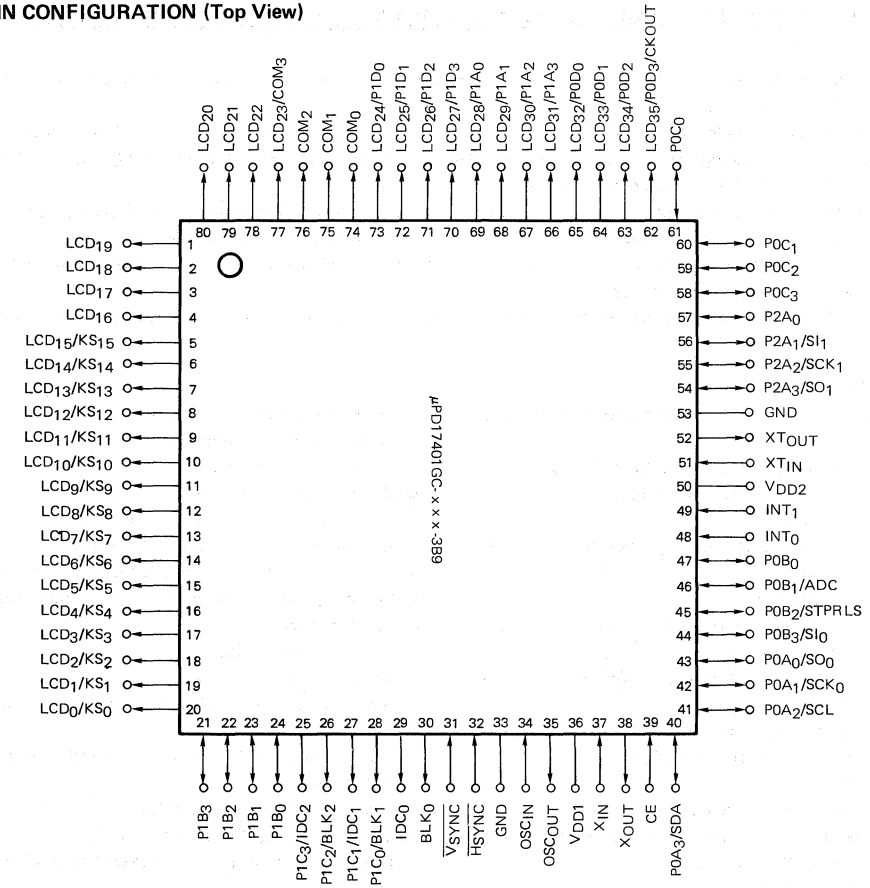
The CPU, which has no accumulator and in which the 17K architecture to allow the data memory to be operated directly is adopted, enables very efficient programming.

As the μPD17401 system development tools, the easy-to-use IE-17K (incircuit emulator) and assembler are available.

FEATURES

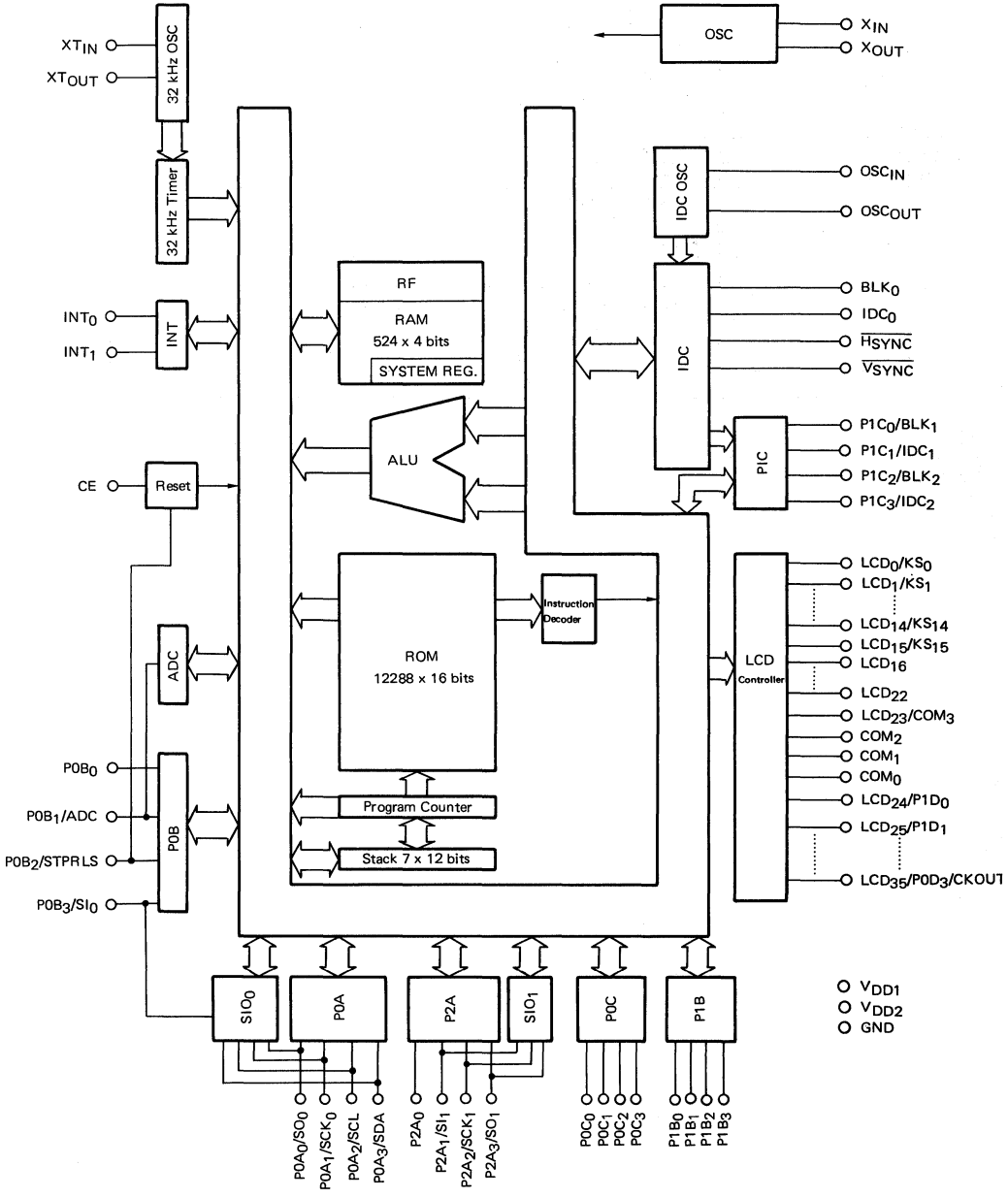
- A 4-bit single-chip microcontroller for the home VCR camera
- Program memory (ROM): 12288 x 16 bits
- Data memory (RAM): 524 x 4 bits
- Stack level: 7
- Instruction set comprising 36 easy-to-understand instructions
- Decimal capability
- Instruction execution time: 1.6 μs (at 10 MHz oscillator connection)
- With IDC on-chip (Image Display Controller9 (user-programmable)
  Number of display characters: Max. 155 per screen
  Display position: 14 lines x 25 columns
  Character types: 256 types
  Character format: 10 x 15 dots (framable)
  Character size: 4 types settable independently between vertical and horizontal (14, 28, 42, 56H) (2.5, 5.0, 7.5, 10 μs)
- On-chip LCD controller/driver
  35-segment, 4-common or
  36-segment, 3-common
- On-chip serial interface
  (2-system, 3-channel: 3-wire and 2-wire)
- On-chip 6-bit A/D converter: 1 input
- On-chip 32 kHz clock counter (V_{DD} = 2.2 to 5.5 V)
- On-chip power failure detection circuit and power-on reset circuit
- Interrupt pins: 2 pins
- Various range of I/O ports
  Input/output ports: 20 (including dual-function pins)
  Output ports: 16 (including dual-function pins)
- 5 V ±10%
- CMOS low power consumption
- 80-pin plastic QFP (14 x 14 mm)
- One-time PROM product: μPD17P401GC-3B9 available

PIN CONFIGURATION (Top View)



$P0A_0$ to $P0A_3$	:	Input/output ports
$P0B_0$ to $P0B_3$	:	Input/output ports
$P0C_0$ to $P0C_3$	:	Input/output ports
$P0D_0$ to $P0D_3$	:	Output ports
$P1A_0$ to $P1A_3$	:	Output ports
$P1B_0$ to $P1B_3$	:	Input/output ports
$P1C_0$ to $P1C_3$	:	Output ports
$P1D_0$ to $P1D_3$	:	Output ports
$P2A_0$ to $P2A_3$	:	Input/output ports
KS_0 to KS_{15}	:	Key source signal output
LCD_0 to LCD_{35}	:	LCD segment signal output
COM_0 to COM_3	:	LCD common signal output
CKOUT	:	Subclock output
STPRLS	:	Stop mode release input
CE	:	Chip enable input
INT_0, INT_1	:	External interrupt input
ADC	:	A/D converter input
SDA	:	Serial data input/output
SCL	:	Serial clock input/output
SI_0, SI_1	:	Serial data input
SO_0, SO_1	:	Serial data output
$\overline{SCK_0}$, $\overline{SCK_1}$	:	Serial clock input/output
X_{IN}, X_{OUT}	:	Main clock oscillation circuits
XT_{IN}, XT_{OUT}	:	Subclock oscillation circuits
OSC_{IN}, OSC_{OUT}	:	IDC oscillation circuits
IDC_0 to IDC_2	:	IDC display signal output
BLK_0 to BLK_2	:	Blanking signal output
$\overline{H_{SYNC}}$	:	Horizontal synchronizing signal input
$\overline{V_{SYNC}}$	:	Vertical synchronizing signal input
V_{DD1}, V_{DD2}	:	Power supply
GND	:	Ground

BLOCK DIAGRAM



LIST OF FUNCTIONS

Product Name	μPD17401	μPD17P401
ROM	12288 x 16 bits (Mask ROM)	12288 x 16 bits (One-time PROM)
RAM	524 x 4 bits	
System register	12 x 4 bits	
Register file	45 x 4 bits (Control register)	
Port register	6 x 4 bits	
Instruction execution time	1.6 μs (at 10 MHz oscillator connection)	
Stack levels	7 levels	
Serial interface	• 2-system, 3-channel 3-wire and 2-wire	
Interrupt	• 2 channels	
Timer	• 2 systems 8-bit timer (10 μs, 100 μs, 500 μs, 1 ms (at 10 MHz oscillator connection)) Clock timer (100 ms (at 10 MHz oscillator connection))	
Standby function	• STOP, HALT	
Supply voltage	V_{DD} = 4.5 to 5.5 V (32 kHz clock counter operated at 2.2 to 5.5 V)	
Package	80-pin plastic QFP (14 x 14 mm)	

4-BIT SINGLE-CHIP MICROCONTROLLER FOR VCR CAMERA

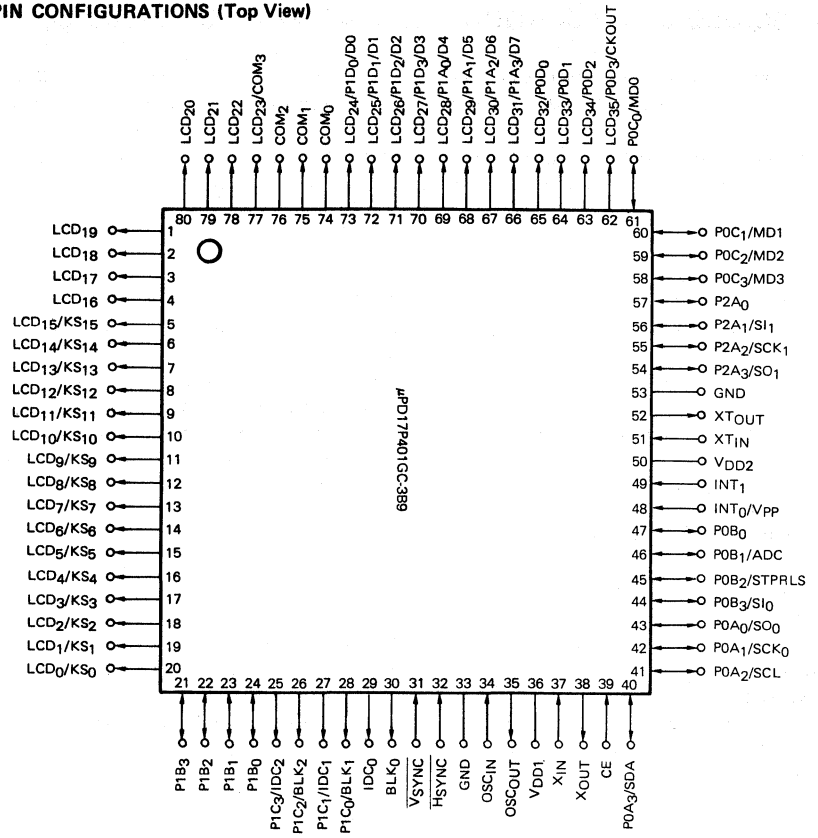
μPD17P401 is a product which has replaced an on-chip mask ROM in 4-bit single-chip microcontroller μPD17401 for a VTR camera with an on-time PROM. μPD17401 allows write operation only once. It is effective for small production of a set, and an earlier start-up.

μPD17P401 incorporates an image display controller (IDC) and an LCD controller/driver. Since it can be operated on the same power-supply voltage as for the mask product, it is the most suitable for preproduction and small production at system development.

FEATURES

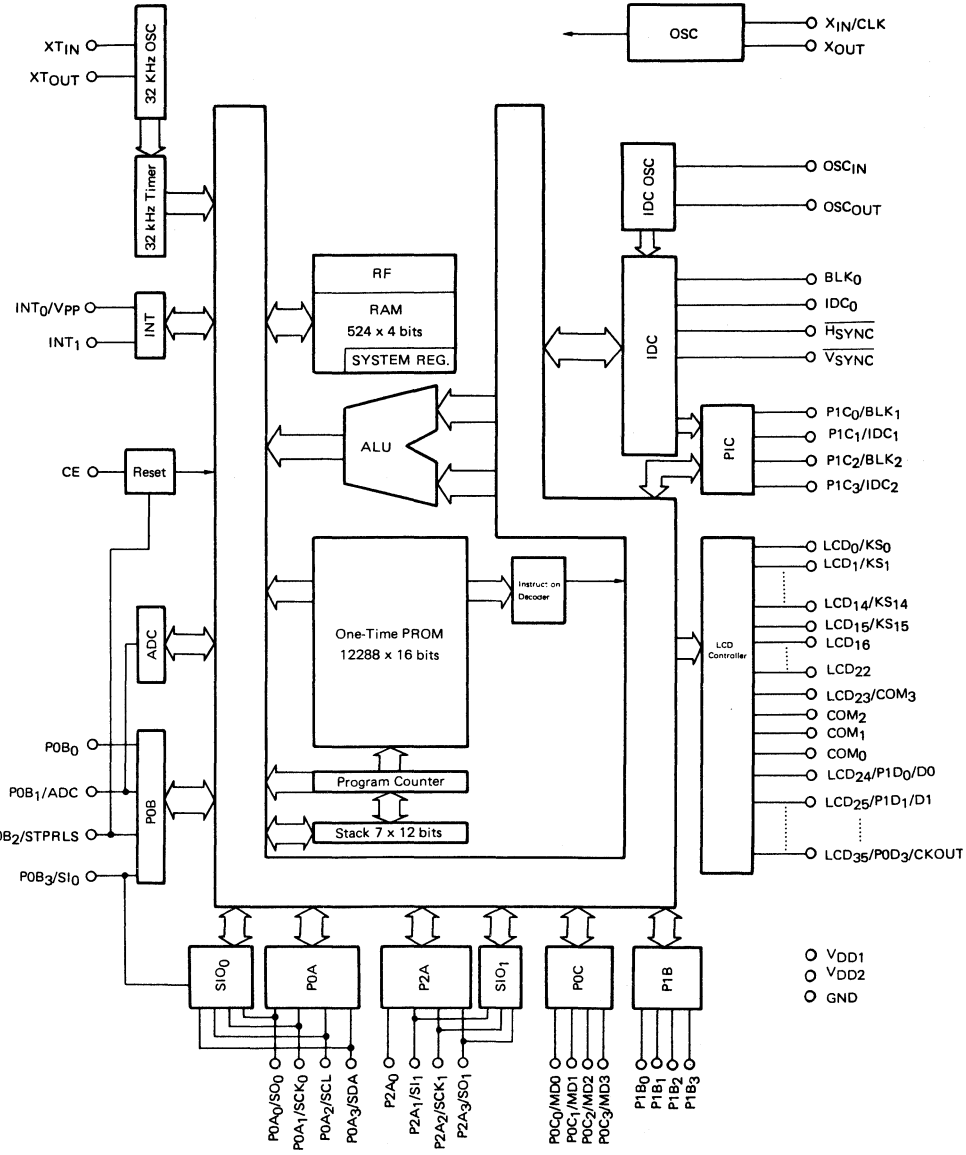
- Fully compatible with μPD17401
- Program memory (one-time PROM): 12288 x 16 bits
- Data memory (RAM): 524 x 4 bits
- Stack level: 7
- Instruction set comprising 36 easy-to-understand instructions
- Decimal operation capability
- Instruction execution time: 1.6 μs (at 10 MHz oscillator connection)
- On-chip Image Display Controller (IDC) (user programmable)
  Number of display characters: Up to 155 characters on one screen
  Display position: 14 lines x 24 digits
  Character types: 256 types
  Character format: 10 x 15 dots (Can be fringed)
  Character size: 4 types can be independently set for each of vertical and horizontal directions. (14, 28, 42, 56H) (2.5, 5.0, 7.5, 10 μs)
- On-chip LCD controller/driver
  35-segment, 4-common or 36-segment, 3-common
- On-chip serial interface
  (2-system, 3-channel: 3-wire and 2-wire)
- On-chip 6-bit A/D converter: 1 input
- On-chip 32 kHz clock counter (V_{DD} = 2.2 to 5.5 V)
- On-chip power failure detection circuit and power-on reset circuit
- Interrupt pins: 2 pins
- Various range of I/O ports
  Input/output ports: 20 (dual-function pin included)
  Output ports: 16 (dual-function pin included)
- 5 V ±10%
- CMOS low power consumption
- 80-pin plastic QFP (14 x 14 mm)
- Mask PROM product:
  μPD17P401GC-xxx-3B9 is available

PIN CONFIGURATIONS (Top View)



$P0A_0$ to $P0A_3$	:	Input/output port
$P0B_0$ to $P0B_3$	:	Input/output port
$P0C_0$ to $P0C_3$	:	Input/output port
$P0D_0$ to $P0D_3$	:	Output port
$P1A_0$ to $P1A_3$	:	Output port
$P1B_0$ to $P1B_3$	:	Input/output port
$P1C_0$ to $P1C_3$	:	Output port
$P1D_0$ to $P1D_3$	:	Output port
$P2A_0$ to $P2A_3$	:	Input/output port
KS_0 to KS_{15}	:	Key source signal output
LCD_0 to LCD_{35}	:	LCD segment signal output
COM_0 to COM_3	:	LCD common signal output
CKOUT	:	Subclock output
STPRLS	:	Stop mode release input
CE	:	Chip enable input
INT_0, INT_1	:	External interrupt input
ADC	:	A/D converter input
SDA	:	Serial data input/output
SCL	:	Serial clock input/output
SI_0, SI_1	:	Serial data input
SO_0, SO_1	:	Serial data output
$\overline{SCK_0}$, $\overline{SCK_1}$	:	Serial clock input/output
X_{IN}, X_{OUT}	:	Oscillation circuit for main clock
XT_{IN}, XT_{OUT}	:	Oscillation circuit for subclock
OSC_{IN}, OSC_{OUT}	:	Oscillation circuit for IDC
IDC_0 to IDC_2	:	IDC Display signal output
BLK_0 to BLK_2	:	Blanking signal output
$\overline{H_{SYNC}}$	:	Horizontal synchronous signal input
$\overline{V_{SYNC}}$	:	Vertical synchronous signal input
CLK	:	Clock input for PROM
MD0 to MD3	:	Mode selection input for PROM
D0 to D7	:	Data input/output for PROM
V_{PP}	:	Power supply for PROM
V_{DD1}, V_{DD2}	:	Power supply
GND	:	Ground

BLOCK DIAGRAM



FUNCTION LIST

Product Name	μPD17401	μPD17P401
ROM	12288 x 16 bits (mask ROM)	12288 x 16 bits (One-time PROM)
RAM	524 x 4 bits	
System register	12 x 4 bits	
Register file	45 x 4 bits (control register)	
Port register	6 x 4 bits	
Instruction execution time	1.6 μs (at 10 MHz oscillation)	
Stack level	7 levels	
Serial interface	• 2-system, 3 channel 3-wire and 2-wire	
Interrupt	• 2 channels	
Timer	• 2-system 8-bit timer (10 μs, 100 μs, 500 μs, 1 ms (at 10 MHz oscillation)) clock timer (100 ms (at 10 MHz oscillation))	
Standby function	• STOP, HALT	
Power supply voltage	V_{DD} = 4.5 to 5.5 V (32 kHz counter for clock is operated at 2.2 to 5.5 V.	
Package	80-pin plastic QFP (14 x 14 mm)	

Instruction Manual of the μPD17K-Family

Section 3 - Instruction Manual of the μPD17K-Family

CHAPTER 1 GENERAL

1.1 GENERAL DESCRIPTION

Each instruction of the μPD17000 series is composed of 16 bits per word. The instruction set contains 47 useful instructions having the following features:

(1) Permitting operation between memories in single step
(2) Permitting both binary and decimal calculation
(3) Permitting table reference on program memory (ROM)
(4) Permitting branching and subroutine call using the register value as address
(5) Well-arranged 47 types of instructions

This manual explains the instructions of the μPD17000 series. However, some instructions are inapplicable or limited in usage for certain products. Careful reference should be taken to the data sheet of the product you want to use before creating a program.

1.2 CONFIGURATION OF INSTRUCTION

The instruction codes of μPD17000 series are classified into the following three types:

(1) 0 operand instruction
Instructions 'INC AR', 'PUSH AR', 'RET', etc. These instructions have a unique or no operand.
(2) 1 operand instruction
Instructions 'RORC r', 'STOP s', etc. The address or immediate data is described in the operand.
(3) 2 operand instruction
Instructions 'ADD r, m', 'ADD m, #i', etc. Two addresses, or an address and immediate data are described in the operand.

CHAPTER 2 DATA MEMORY ADDRESSING

A data memory address is composed of a bank (four bits), row address (3 bits) and column address (four bits).

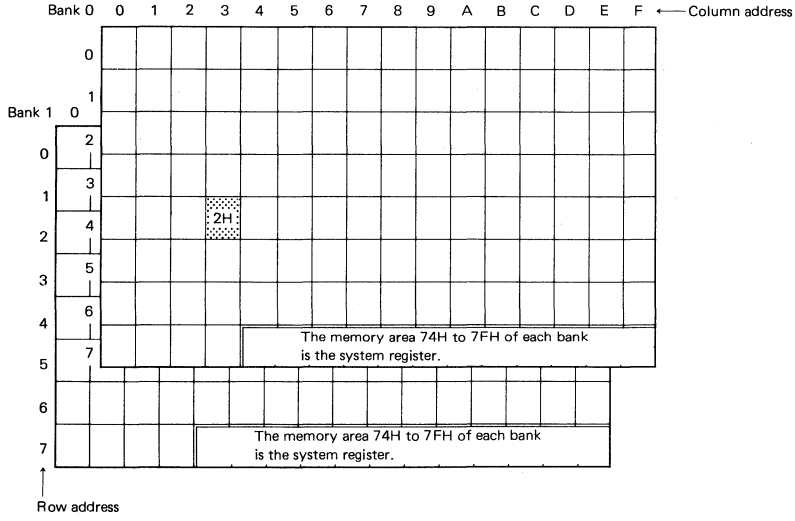
2.1 DIRECT ADDRESSING OF DATA MEMORY

When directly specifying data memory, the bank is specified by the BANK (bank register: 79H) of the system register, and the row address and column address are specified by the instruction operand m (seven bits).

[Example]

If BANK = 0,

```
MOV 43H, #2H
        └── Immediate data
    └── Address (Column address = 3, row address = 4)
```



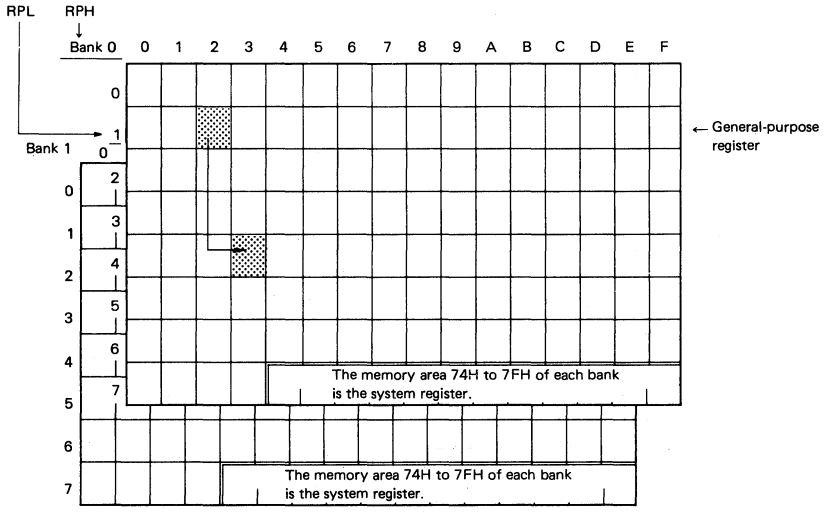
2.2 GENERAL-PURPOSE REGISTER ADDRESSING

When specifying a general-purpose register, the bank and row addresses are specified by RPH and RPL (register pointer: 7DH, 7EH) of the system register, and the column address is specified by the instruction operand r (four bits).

[Example]

When BANK = 0, RPH = 0, and RPL = 1;

```
ST 43H, 2H
   |    |
   |    └──General-purpose register column address
   └───Address
```



2.3 INDEX MODIFICATION ADDRESSING OF DATA MEMORY

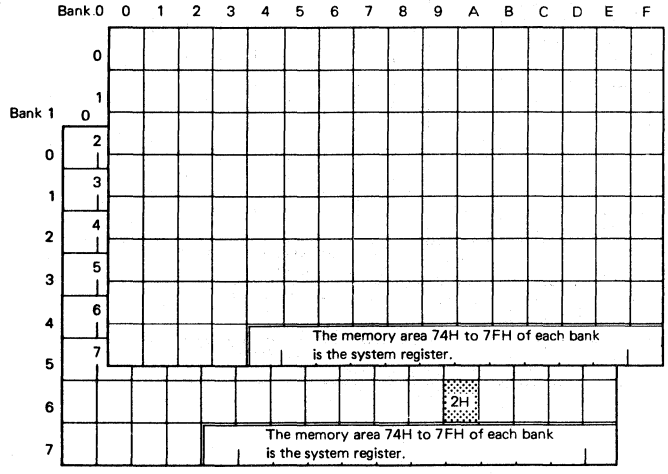
If IXE (index addressing enable flag: 7FH.0) of the system register is set '1', the data memory address is specified as the ORed result of the address specified by the system register BANK (bank register: 79H) and instruction operand m (seven bits) and the contents of system register IXH, IXM, and IXL (index register: 7AH, 7BH, and 7CH).

[Example]

If BANK = 0, IXE = 1, IXH = 0, IXM = 0EH, and IXL = 8;

MOV 43H, #2H
- #2H: Immediate data
- 43H: Address

Data memory address = [BANK, m] OR [IXH, IXM, IXL]
= [0000 1000011B] OR [000 1110 1000B]
= [0001 1101011B]
= 6BH of bank 1



2.4 GENERAL-PURPOSE REGISTER INDIRECT ADDRESSING OF DATA MEMORY

The data memory address specification method for executing the general-purpose register indirect transfer instruction 'MOV @r, m' and 'MOV m, @r' is explained below.

(1) When MPE = 0, IXE = 0

The bank for direct specification by operand m is specified by the system register BANK (bank register: 79H) and the row address and column address are specified by the instruction operand m (seven bits).

The bank for indirect specification by operand @r is specified by the system register BANK (bank register: 79H), and the row address is specified by the upper three bits of operand m. The column address is specified by the value of the general-purpose register. The bank and row address of the general-purpose register are specified by the system register RPH and RPL (register pointer: 7DH, 7EH), and the column address is specified by the instruction operand r (four bits).

Accordingly, indirect transfer with MPE = 0 and IXE = 0 occurs within the same row address of the same bank.

[Example]

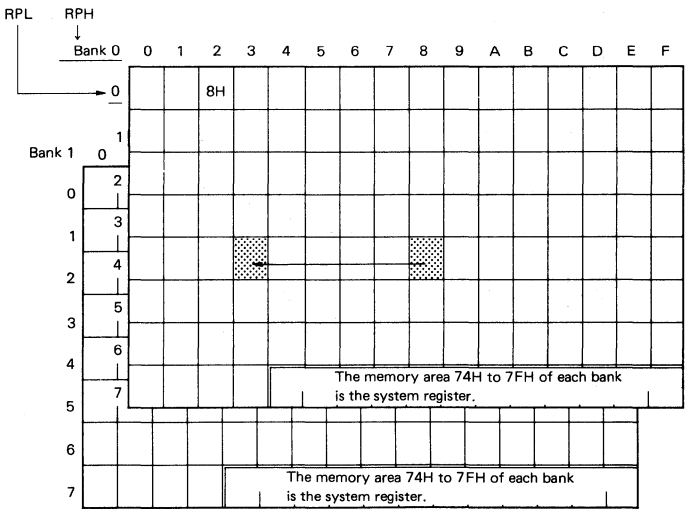
When BANK = 0, RPH = 0, RPL = 0, and the value of address 0.02H is 8H;

MOV 43H, @2H

- 43H: Direct specification address
- @2H: Indirect specification address

Direct specification address = [BANK, m]
= [0000 1000011B]
= 43H of bank 0

Indirect specification address = [BANK, $m_{6\text{-}4}$, (R)]
= [0000 100 1000B]
= 48H of bank 0



(2) When MPE = 1 and IXE = 0

The bank for direct specification by operand m is specified by the system register BANK (bank register: 79H), and the row address and column address are specified by the instruction operand m (seven bits).

The bank for indirect specification by operand @r and the row address are specified by the MPH and MPL (memory pointer: 7AH, 7BH) of the system register, and the column address is specified by the value of the general-purpose register. The bank and row address of the general-purpose register are specified by the RPH and RPL (register pointer: 7DH, 7EH) of the system register, and the column address is specified by the instruction operand r (four bits).

Accordingly, when MPE = 1 and IXE = 0, indirect data transfer is allowed between any data memories.

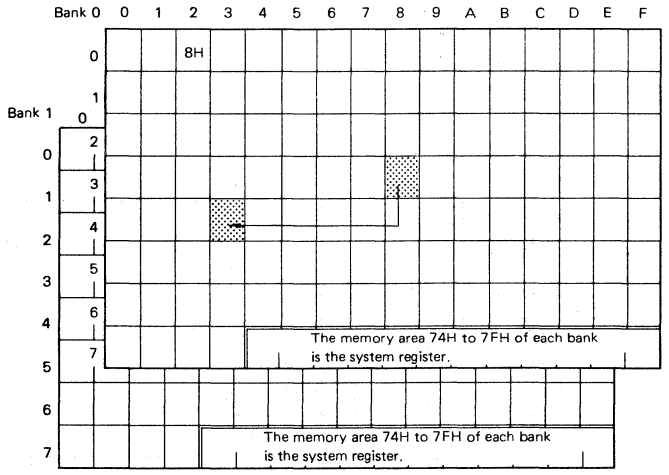
[Example]

When BANK = 0, MPH = 0, MPL = 3, RPH = 0, RPL = 0, and the value of 0.02H address is 8H;

MOV 43H, @2H
- 43H: Direct specification address
- @2H: Indirect specification address

Direct specification address = [BANK, m]
= [0000 1000011B]
= 43H of bank 0

Indirect specification address = [MPH, MPL, (R)]
= [000 0011 1000B]
= 38H of bank 0



(3) When MPE = 0 and IXE = 1

The bank, row address and column address for direct specification by operand m are specified by the ORed result of the address specified by the system register BANK (bank register: 79H) and instruction operand m (seven bits) and the contents of system registers IXH, IXM and IXL (index registers: 7AH, 7BH, 7CH).

The bank and row address of the indirect specification by operand @r are specified by the ORed result of the address specified by the system register BANK (bank register: 79H) and the upper three bits of operand m and the contents of system registers IXH and IXM (index registers: 7AH, 7BH). The column address is specified by the value of the general-purpose register. The bank and row address of the general-purpose register are specified by the system registers RPH and RPL (register pointers: 7DH, 7EH), and the column address is specified by the instruction operand r (four bits).

If MPE = 0 and IXE = 1, indirect transfer of data occurs within the same row address of the same bank.

[Example]

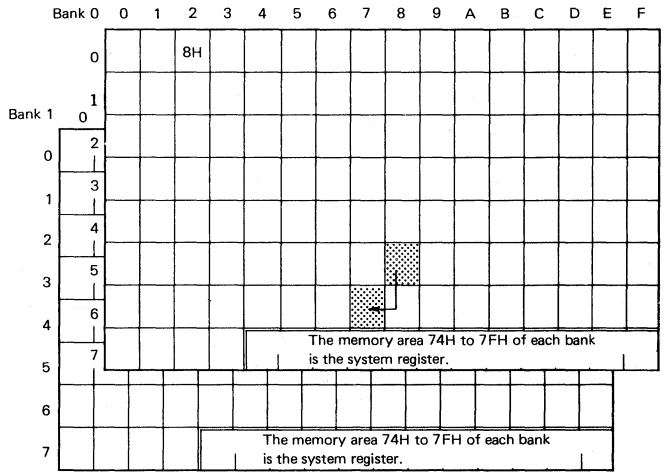
When BANK = 0, IXH = 0, IXM = 2, IXL = 4, RPH = 0, RPL = 0, and the value of address 0.02H is 8H;

MOV 43H, @2H

- 43H: Direct specification address
- @2H: Indirect specification address

Direct specification address = [BANK, m] OR [IXH, IXM, IXL]
= [0000 1000011B] OR [000 0010 0100B]
= [0000 1100111B]
= 67H of bank 0

Indirect specification address = [BANK, $m_{6\text{-}4}$, (R)] OR [IXH, IXM, 0]
= [0000 100 1000B] OR [000 0010 0000B]
= [0000 101 1000B]
= 58H of bank 0



(4) When MPE = 1, IXE = 1

The bank, row address, and column address by direct specification with operand m are specified by the ORed result of the address specified by the system register BANK (bank register: 79H) and instruction operand m (seven bits) and the contents of the system registers IXH, IXM, and IXL (index registers: 7AH, 7BH and 7CH).

The bank and row address by indirect specification with operand @r is specified by the system registers MPH and MPL (memory pointers; 7AH, 7BH), and the column address is specified by the value of the general-purpose register. The bank and row address of the general-purpose register are specified by the system registers RPH and RPL (register pointers: 7DH, 7EH), and the column address is specified by the instruction operand r (four bits).

Accordingly, indirect data transfer with MPE = 1 and IXE = 1 is allowed between any data memories.

[Example]

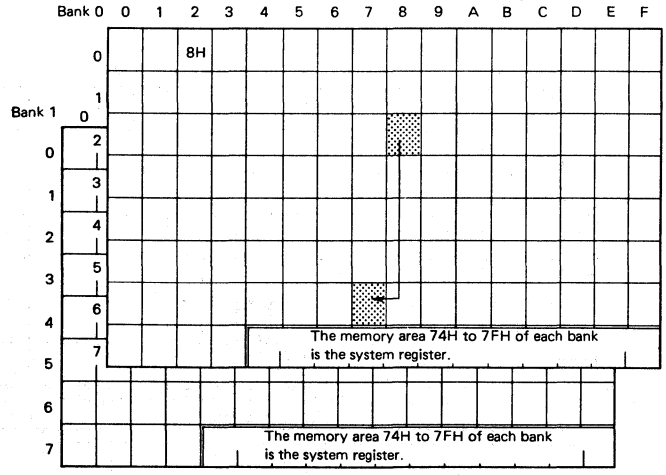
When BANK = 0, IXH (MPH) = 0, IXM (MPL) = 2, IXL = 4, RPH = 0, RPL = 0, and value of address 0.02H is 8H;

MOV 43H, @2H

- 43H: Direct specification address
- @2H: Indirect specification address

Direct specification address = [BANK, m] OR [IXH, IXM, IXL]
= [0000 1000011B] OR [000 0010 0100B]
= [0000 1100111B]
= 67H of bank 0

Indirect specification address = [MPH, MPL, (R)]
= [000 0010 10000B]
= 28H of bank 0



CHAPTER 3 INSTRUCTION SET

This chapter explains the instruction set. The abbreviations used in the explanation of instruction set are shown below:

(X)	:	Value of data memory or register indicated by X (four bits)
[X, Y, Z]	:	Address consisting of upper 4 bits (X), medium 3 bits (Y) and lower 4 bits (Z) (Total 11 bits)
M	:	Data memory address If IXE = 0, then M = [(BANK), m_H, m_L] If IXE = 1, then M = [(BANK), m_H, m_L] OR (IX)
IXE	:	Index enable flag
(BANK)	:	Bank register value (4 bits)
m_H	:	Data memory row address (3 bits)
m_L	:	Data memory column address (4 bits)
(IX)	:	Index register value (11 bits)
R	:	General-purpose register address R = [(RP_H), (RP_L), r]
(RP_H)	:	General-purpose register bank (4 bits)
(RP_L)	:	General-purpose register row address (3 bits)
r	:	General-purpose register column address (4 bits)
i	:	Immediate data (4 bits)
addr	:	Address of branching destination
CY	:	Carry flag
SP	:	Stack pointer
STACK	:	Stack value indicated by stack pointer
AR	:	Address register
DBF	:	Data buffer
WR	:	Window register
rf	:	Register file address
rf_H	:	Upper 3 bits of register file address
rf_L	:	Lower 4 bits of register file address
p	:	Address of peripheral circuit
p_H	:	Upper 3 bits of peripheral circuit address
p_L	:	Lower 4 bits of peripheral circuit address

Note: Unless otherwise specified, the following conditions are used:

BANK = 0
RPH = 0, RPL = 0
IXE = 0

The data memory address is represented by direct address. When actually using an assembler, be sure to use the type MEM symbol. Any description of memory address directly into the operand will cause an error.

3.1 ADD r, m

Add data memory to general register

(1) Instruction code

00000	m_H	m_L	r

(2) Function

If CMP = 0, R ← (R) + (M)

The contents of the data memory addressed by M is added to the contents of the general-purpose register indicated by R, and the results are stored into the general-purpose register indicated by R.

If CMP = 1, then (R) + (M)

No results are stored. The flag only changes.

If a carry is made, set a carry flag (CY). If no carry is made, reset the carry flag (CY).

If the result of addition is other than zero, the zero flag (Z) is reset.

If the result of addition is zero, the zero flag (Z) will be set when the compare flag is in the reset status (CMP = 0). When the compare flag is in the set status (CMP = 1), the zero flag (Z) will not be changed if the result of addition is zero.

There are two types in addition: binary operation and BCD operation. The addition type is selected by the BCD flag (BCD) of PSW.

(3) **Example 1**

When the row address 0 (0.00H to 0.0FH) of bank 0 is specified as general-purpose register (RPH = 0, RPL = 0), the result of addition of the contents of 0.2FH address is stored to the contents of 0.03H address.

```
0.03H ← (0.03H) + (0.2FH)
MOV BANK, #00H ;  Data memory bank 0
MOV RPH, #00H  ;  General-purpose register bank to 0
MOV RPL, #00H  ;  General-purpose register row address to 0
ADD 03H, 2FH
```

Example 2

When row address 2 (1.20H to 1.2FH) of bank 1 is specified as general-purpose register (RPH = 1, RPL = 4), the content of address 1.23H is added to the content of address 0.2FH, and the results are stored into address 1.23H.

```
1.23H ← (1.23H) + (0.2FH)
MOV BANK, #00H ;  Data memory bank 0
MOV RPH, #01H  ;  General-purpose register bank 1
MOV RPL, #04H  ;  General-purpose register row address 2
ADD 03H, 2FH
```

Example 3

The result of addition of the contents of address 0.03H and address 0.6FH is stored into address 0.03H. If IXE = 1, IXH = 0, IXM = 4, and IXL = 0, that is, if IX = 0.40H, then the data memory 0.6FH can be specified by setting the data memory address at 2FH.

0.03H ← (0.03H) + (0.6FH)
└── ORed result of index register content 0.40H and data memory address 0.2FH

```
MOV  RPH, #00H   ;  General-purpose register bank 0
MOV  RPL, #00H   ;  General-purpose register row address 0
MOV  IXH, #00H   ;  IX ← 00001000000B
MOV  IXM, #04H   ;
MOV  IXL, #00H   ;
SET1 IXE         ;  IXE flag ← 1
ADD  03H, 2FH    ;  IX                    00001000000B (0.40H)
                 ;  Bank operand OR    )  00000101111B (0.2FH)
                 ;  Specified address      00001101111B (0.6FH)
```

Example 4

The result of addition of the contents of address 0.03H and address 2.3FH is stored into address 0.03H. If IXE = 1, IXH = 1, IXM = 1, and IXL = 0, that is, if IX = 2.10H, then the data memory 2.3FH can be specified by setting the data memory address at 2FH.

0.03H ← (0.03H) + (2.3FH)
└── ORed result of the content of index register 2.10H and data memory address 0.2FH

```
MOV  BANK, #00H
MOV  RPH, #00H   ;  General-purpose register bank 0
MOV  RPL, #00H   ;  General-purpose register row address 0
MOV  IXH, #01H   ;  IX ← 00100010000B (2.10H)
MOV  IXM, #01H
MOV  IXL, #00H
SET1 IXE         ;  IXE flag ← 1
ADD  03H, 2FH    ;  IX                    00100010000B (2.10H)
                 ;  Bank operand OR    )  00000101111B (0.2FH)
                 ;  Specified address      00100111111B (2.3FH)
```

(4) **Note**

The 1st operand of 'ADD r, m' instruction is the column address of general-purpose register. If it is described as follows, the general-purpose register column address is taken as 03H. This will not cause any error in assembling.

```
ADD 13H, 2FH
    └── General-purpose register column address is meant.
        The lower 4 bits are significant.
```

If CMP flag = 1, no added result is stored.

If BCD flag = 1, the result of decimal operation is stored.

3.2 ADD m, #i

Add immediate data to data memory

(1) Instruction code

10000	m_H	m_L	i

(2) Function

If CMP = 0, then M ← (M) + i

The immediate data i is added to the content of data memory addressed by M, and the result is stored into the data memory addressed by M.

If CMP = 1, then (M) + i

No result is stored. Only the flag changes.

If any carry occurs as a result of addition, the carry flag (CY) is set. If no carry occurs, the carry flag (CY) is reset.

If the result of addition is other than zero, the zero flag (Z) is reset.

If the compare flag is reset (CMP = 0) when the result of addition is zero, the zero flag (Z) is set. If the compare flag is set (CMP = 1), the zero flag (Z) will not change when the result of addition turns zero.

There are two types of addition: binary operation and BCD operation. The addition type is specified by the BCD flag (BCD) of PSW.

(3) **Example 1**

Value 5 is added to the content of address 0.2FH, and the result is stored to address 0.2FH.

```
0.2FH ← (0.2FH) + 5
ADD 2FH, #05H
```

Example 2

Value 5 is added to the content of address 0.6FH, and the result is stored to address 0.6FH. If IXE = 1, IXH = 0, IXM = 4, and IXL = 0, that is, if IX = 0.40H, then the data memory 0.6FH can be specified by setting the data memory address at 2FH.

```
0.6FH ← (0.6FH) + 05H
          └── ORed result of the index register content 0.40H and data
              memory address 0.2FH
MOV BANK, #00H ;  Data memory bank 0
MOV IXH, #00H  ;  IX ← 000010000000B (0.40H)
MOV IXM, #04H
MOV IXL, #00H
SET1 IXE       ;  IXE flag ← 1
ADD 2FH, #05H  ;  IX                    000010000000B
               ;  Bank operand OR )      00000101111B (0.2FH)
               ;  Specified address      00001101111B (0.6FH)
```

Example 3

Value 5 is added to the content of address 2.2FH, and the result is stored to address 2.2FH. If IXE = 1, IXH = 1, IXM = 0 and IXL = 0, that is, if IX = 2.00H, then the data memory 2.2FH can be specified by setting the data memory address at 2FH.

2.2FH ← (2.2FH) + 05H

└── ORed result of index register content 2.00H and data memory address 0.2FH

```
MOV  BANK, #00H ;  Data memory bank 0
MOV  IXH, #01H  ;  iX ← 00100000000B
MOV  IXM, #00H
MOV  IXL, #00H
SET1 IXE        ;  IXE flag ← 1
ADD  2FH, #05H  ;  IX                  00100000000B (2.00H)
                ;  Bank operand OR  ) 00000101111B (0.2FH)
                ;  Specified address  00100101111B (2.2FH)
```

(4) **Note**

If CMP flag = 1, then no addition result is stored.

If BCD flag = 1, the result of decimal operation is indicated.

3.3 ADDC r, m

Add data memory to general register with carry flag

(1) Instruction code

00010	m_H	m_L	r

(2) Function

If CMP = 0, then R ← (R) + (M) + CY

The content of general-purpose register indicated by R, the content of data memory addressed by M and the value of carry flag (CY) are added, and the result is stored into the general-purpose register indicated by R.

If CMP = 1, then (R) + (M) + CY

The result of addition is not stored. Only the flag is changed.

Use of this 'ADDC' instruction permits addition to two words or more can be performed easily.

If a carry occurs as a result of addition, the carry flag (CY) is set; if no carry occurs, the carry flag (CY) is reset.

If the result of addition is other than zero, then zero flag (Z) is reset.

If the compare flag is reset (CMP = 0) when the result of addition is zero, the zero flag (Z) is set. If the compare flag is set (CMP = 1), the zero flag (Z) will not change when the result of addition turns zero.

There are two types of addition: binary operation and BCD operation. The addition type is specified by the BCD flag (BCD) of PSW.

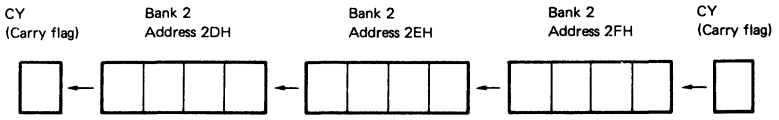
(3) **Example 1**

When row address 0 (0.00H to 0.0FH) of bank 0 is specified as a general-purpose register, the 12-bit content of address 0.2DH-0.2FH is added to the 12-bit content of address 0.0DH-0.0FH, and then the result is stored into the 12-bit area of address 0.0DH-0.0FH.

```
0.0FH ← (0.0FH) + (0.2FH)
0.0EH ← (0.0EH) + (0.2EH) + CY
0.0DH ← (0.0DH) + (0.2DH) + CY
MOV  BANK, #00H  ;  Data memory bank 0
MOV  RPH, #00H   ;  General-purpose register bank 0
MOV  RPL, #00H   ;  General-purpose register row address 0
ADD  0FH, 2FH
ADDC 0EH, 2EH
ADDC 0DH, 2DH
```

Example 2

When row address 2 (1.20H to 1.2FH) of bank 1 is specified as a general-purpose register, the 12-bit content of address 1.2DH to 1.2FH is shifted to the left including a carry flag by one.




```
MOV  RPH, #01H   ;  General-purpose register bank 1
MOV  RPL, #04H   ;  General-purpose register row address 2
MOV  BANK, #01H  ;  Data memory bank 1
ADDC 0FH, 2FH
ADDC 0EH, 2EH
ADDC 0DH, 2DH
```

Example 3

The content of address 0.0FH and the contents of addresses 0.40H to 0.4FH are added, and then store the result into address 0.0FH.

0.0FH ← (0.0FH) + (0.40H) + (0.41H) + ... + (0.4FH)

```
        MOV  BANK, #00H ;  Data memory bank 0
        MOV  RPH, #00H  ;  General-purpose register bank 0
        MOV  RPL, #00H  ;  General-purpose register row address 0
        MOV  IXH, #00H  ;  IX ← 00001000000B (0.40H)
        MOV  IXM, #04H
        MOV  IXL, #00H
LOOP1:
        SET1 IXE        ;  IXE flag ← 1
        ADD  0FH, 00H
        CLR1 IXE        ;  IXE flag ← 0
        INC  IX         ;  IX ← IX + 1
        SKE  IXL, #0
        JMP  LOOP1
```

Example 4

The 12-bit contents of addresses 1.40H to 1.42H are added to the 12-bit contents of addresses 0.0DH to 0.0FH, then the result is stored to the 12-bit area of addresses 0.0DH to 0.0FH.

0.0DH ← (0.0DH) + (1.40H)
0.0EH ← (0.0EH) + (1.41H) + CY
0.0FH ← (0.0FH) + (1.42H) + CY

```
MOV  BANK, #00H ;  Data memory bank 0
MOV  RPH, #00H  ;  General-purpose register bank 0
MOV  RPL, #00H  ;  General-purpose register row address 0
MOV  IXH, #00H  ;  IX ← 00011000000 (1.40H)
MOV  IXM, #0CH
MOV  IXL, #00H
SET1 IXE        ;  IXE flag ← 1
ADD  0DH, 00H   ;  0.0DH ← (0.0DH) + (1.40H)
ADDC 0EH, 01H   ;  0.0EH ← (0.0EH) + (1.41H)
ADDC 0FH, 02H   ;  0.0FH ← (0.0FH) + (1.42H)
```

3.4 ADDC m, #i

Add immediate data to data memory with carry flag

(1) Instruction code

10010	m_H	m_L	i

(2) Function

If CMP = 0: M ← (M) + i + CY

The values of immediate data i and carry flag (CY) are added to the content of data memory addressed by M, and the result is stored to the data memory addressed by M.

If CMP = 1: (M) + i + CY

The result is not stored. Only the flag is changed.

If a carry occurs as a result of addition, the carry flag (CY) is set; if no carry occurs, the carry flag (CY) is reset.

If the result of addition is other than zero, then zero flag (Z) is reset.

If the compare flag is reset (CMP = 0) when the result of addition is zero, the zero flag (Z) is set. If the compare flag is set (CMP = 1), the zero flag (Z) will not change when the result of addition turns zero.

There are two types of addition: binary operation and BCD operation. The addition type is specified by the BCD flag (BCD) of PSW.

(3) **Example 1**

The value 5 is added to the 12-bit contents of addresses 0.0DH to 0.0FH, and then the result is stored to the addresses 0.0DH to 0.0FH.

```
0.0FH ← (0.0FH) + 05H
0.0EH ← (0.0EH) + CY
0.0DH ← (0.0DH) + CY
MOV BANK, #00H ;  Data memory bank 0
ADD 0FH, #05H
ADDC 0EH, #00H
ADDC 0DH, #00H
```

Example 2

The value 5 is added to the 12-bit contents of addresses 0.4DH to 0.4FH, and the result is stored to the addresses 0.4DH to 0.4FH.

```
0.4FH ← (0.4FH) + 05H
0.4EH ← (0.4EH) + CY
0.4DH ← (0.4DH) + CY
MOV  BANK, #00H ;  Data memory bank 0
MOV  IXH, #00H  ;  IX ← 00001000000B (0.40H)
MOV  IXM, #04H
MOV  IXL, #00H
SET1 IXE        ;  IXE flag ← 1
ADD  0FH, #5       0.4FH ← (0.4FH) + 05H
ADDC 0EH, #0       0.4EH ← (0.4EH) + CY
ADDC 0DH, #0       0.4DH ← (0.4DH) + CY
```

3.5 SUB r, m

Subtract data memory from general register

(1) Instruction code

00001	m_H	m_L	r

(2) Function

If CMP = 0: R ← (R) – (M)

The content of data memory addressed by M is subtracted from the content of general-purpose register indicated by R, and the result is stored into the general-purpose register indicated by R.

If CMP = 1: (R) – (M)

The result is not stored. Only the flag is changed.

If a borrow occurs as a result of subtraction, the carry flag (CY) is set; if no borrow occurs, the carry flag (CY) is reset.

If the result of subtraction is other than zero, then zero flag (Z) is reset.

If the compare flag is reset (CMP = 0) when the result of subtraction is zero, the zero flag (Z) is set. If the compare flag is set (CMP = 1), the zero flag (Z) will not change when the result of subtraction turns zero.

There are two types of subtraction: binary operation and BCD operation. The subtraction type is specified by the BCD flag (BCD) of PSW.

(3) **Example 1**

When row address 0 (0.00H to 0.0FH) of bank 0 is specified as general-purpose register (RPH = 0, RPL = 0), the content of address 0.2FH is subtracted from the content of address 0.03H, then the result is stored to the address 0.03H.

```
0.03H ← (0.03H) – (0.2FH)
SUB 03H, 2FH
```

Example 2

When bank 1 row address 2 (1.20H to 1.2FH) is specified as general-purpose register (RPH = 1, RPL = 4), the content of address 0.2FH is subtracted from the content of address 1.23H, and the result is stored to the address 1.23H.

```
1.23H ← (1.23H) – (0.2FH)
MOV BANK, #00H ;  Data memory bank 0
MOV RPH, #01H  ;  General-purpose register bank 1
MOV RPL, #04H  ;  General-purpose register row address 2
SUB 03H, 2FH
```

Example 3

The content of address 0.6FH is subtracted from the content of address 0.03H, and the result is stored to the address 0.03H. If IXE = 1, IXH = 0, IXM = 4, and IXL = 0, that is, if IX = 0.40H, then the data memory 0.6FH can be specified by setting the data memory address at 2FH.

0.03H ← (0.03H) – (0.6FH)

```
MOV  BANK, #00H ;  Data memory bank 0
MOV  RPH, #00H  ;  General-purpose register bank 0
MOV  RPL, #00H  ;  General-purpose register row address 0
MOV  IXH, #00H  ;  IX ← 00001000000B (0.40H)
MOV  IXM, #04H  ;
MOV  IXL, #00H  ;
SET1 IXE        ;  IXE flag ← 1
SUB  03H, 2FH   ;  IX                  00001000000B (0.40H)
                ;  Bank operand OR  )  00000101111B (0.2FH)
                ;  Specified address   00001101111B (0.6FH)
```

Example 4

The content of address 2.3FH is subtracted from the content of address 0.03H, and the result is stored to the address 0.03H. If IXE = 1, IXH = 1, IXM = 1 and IXL = 0, that is, if IX = 2.10H, then the data memory 2.3FH can be specified by setting the data memory address at 2FH.

0.03H ← (0.03H) – (2.3FH)

```
MOV  BANK, #00H ;  Data memory bank 0
MOV  RPH, #00H  ;  General-purpose register bank 0
MOV  RPL, #00H  ;  General-purpose register row address 0
MOV  IXH, #01H  ;  IX ← 00100010000B (2.10H)
MOV  IXM, #01H  ;
MOV  IXL, #00H  ;
SET1 IXE        ;  IXE flag ← 1
SUB  03H, 2FH   ;  IX                  00100010000B (2.10H)
                ;  Bank operand OR  )  00000101111B (0.2FH)
                ;  Specified address   00100111111B (2.3FH)
```

(4) **Note**

The 1st operand of the 'SUB r, m' instruction must be a general-purpose register address. The address 03H is specified as a register if described as follows. This will not cause an error in assembling.

```
SUB 13H, 2FH
      └──The general-purpose register address must fall within the range from 00H to 0FH
          (with register pointer set at other than row address 1).
```

If CMP flag = 1, the subtracted result is not stored.

If BCD flag = 1, the result of decimal operation is stored.

3.6 SUB m, #i

Subtract immediate data from data memory

(1) Instrctuion code

10001	m_H	m_L	i

(2) Function

If CMP = 0: M ← (M) − i

The immediate data i is subtracted from the content of data memory addressed by M, and the result is stored into the data memory addressed by M.

If CMP = 1: (M) − i

The result is not stored. Only the flag is changed.

If a borrow occurs as a result of subtraction, the carry flag (CY) is set; if no borrow occurs, the carry flag (CY) is reset.

If the result of subtraction is other than zero, then zero flag (Z) is reset.

If the compare flag is reset (CMP = 0) when the result of subtraction is zero, the zero flag (Z) is set. If the compare flag is set (CMP = 1), the zero flag (Z) will not change when the result of subtraction turns zero.

There are two types of subtraction: binary operation and BCD operation. The subtraction type is specified by the BCD flag (BCD) of PSW.

(3) **Example 1**

Value 5 is subtracted from the contents of address 0.2FH, and the result is stored to the address 0.2FH.

```
0.2FH ← (0.2FH) − 5
SUB 2FH, #05H
```

Example 2

The value 5 is subtracted from the content of address 0.6FH, and the result is stored to the address 0.6FH. If IXE = 1, IXH = 0, IXM = 4, and IXL = 0, that is, if IX = 0.40H, then the data memory 0.6FH can be specified by setting the data memory address at 2FH.

```
0.6FH ← (0.6FH) − 5
          └── ORed result of the content 0.40H of index register and the data
              memory address 0.2FH
MOV  BANK, #00H ;  Data memory bank 0
MOV  IXH, #00H  ;  IX ← 00001000000B (0.40H)
MOV  IXM, #04H  ;
MOV  IXL, #00H  ;
SET1 IXE        ;  IXE flag ← 1
SUB  2FH, #05H  ;  IX                    00001000000B (0.40H)
                ;  Bank operand OR  )   00000101111B (0.2FH)
                ;  Specified address     00001101111B (0.6FH)
```

Example 3

The value 5 is subtracted from the content of address 2.2FH, and the result is stored to the address 2.2FH. If IXE = 1, IXH = 1, IXM = 0, and IXL = 0, that is, if IX = 2.00H, then the data memory 2.2FH can be specified by setting the data memory address at 2FH.

2.2FH ← (2.2FH) – 5
└—ORed result of the content 2.00H of index register and the data memory address 0.2FH

```
MOV BANK0, #00H;  Data memory bank 0
MOV IXH, #01H     ;  IX ← 00100000000B (2.00H)
MOV IXM, #00H     ;
MOV IXL, #00H     ;
SET1 IXE          ;  IXE flag ← 1
SUB 2FH, #05H     ;  IX                    00100000000B (2.00H)
                  ;  Bank operand OR )     00000101111B (0.2FH)
                  ;  Specified address     00100101111B (2.2FH)
```

(4) **Note**

If CMP flag = 1, no subtract result is stored.

If BCD flag = 1, the result of decimal operation is stored.

3.7 SUBC r, m

Subtract data memory from general register with carry flag

(1) Instruction code

00011	m_H	m_L	r

(2) Function

If CMP = 0: R ← (R) − (M) − CY

The content of data memory indicated by address M and the value of carry flag (CY) are subtracted from the content of general-purpose register indicated by R, and the result is stored into the general-purpose register indicated by R. Use of this SUBC instruction permits subtraction of more than two words to be performed easily.

If CMP = 1: (R) − (M) − CY

The result is not stored. Only the flag is changed.

If a borrow occurs as a result of subtraction, the carry flag (CY) is set; if no borrow occurs, the carry flag (CY) is reset.

If the result of subtraction is other than zero, then zero flag (Z) is reset.

If the compare flag is reset (CMP = 0) when the result of subtraction is zero, the zero flag (Z) is set. If the compare flag is set (CMP = 1), the zero flag (Z) will not change when the result of subtraction turns zero.

There are two types of subtraction: binary operation and BCD operation. The subtraction type is specified by the BCD flag (BCD) of PSW.

(3) **Example 1**

When bank 0 row address 0 (0.00H to 0.0FH) is specified as general-purpose register, the 12-bit contents of addresses 0.2DH to 0.2FH are subtracted from the 12-bit content of addresses 0.0DH to 0.0FH, and then the result is stored into the 12-bit area of addresses 0.0DH to 0.0FH.

0.0FH ← (0.0FH) − (0.2FH)
0.0EH ← (0.0EH) − (0.2EH) − CY
0.0DH ← (0.0DH) − (0.2DH) − CY

```
SUB  0FH, 2FH
SUBC 0EH, 2EH
SUBC 0DH, 2DH
```

Example 2

The contents of 12 bits from addresses 1.40H to 1.42H are subtracted from the contents of 12 bits from addresses 0.0DH to 0.0FH, and then the result is stored to the 12 bits from 0.0DH to 0.0FH.

0.0DH ← (0.0DH) – (1.40H)
0.0EH ← (0.0EH) – (1.41H) – CY
0.0FH ← (0.0FH) – (1.42H) – CY

```
MOV  BANK, #00H ;  Data memory bank 0
MOV  RPH, #00H  ;  General-purpose register bank 0
MOV  RPL, #00H  ;  General-purpose register row address 0
MOV  IXH, #00H  ;  IX ← 00011000000B (1.40H)
MOV  IXM, #0CH  ;
MOV  IXL, #00H  ;
SET1 IXE        ;  IXE flag ← 1
SUB  0DH, 00H   ;  0.0DH ← (0.0DH) – (1.40H)
SUBC 0EH, 01H   ;  0.0EH ← (0.0EH) – (1.41H)
SUBC 0FH, 02H   ;  0.0FH ← (0.0FH) – (1.42H)
```

Example 3

The contents of 12 bits from addresses 0.00H to 0.03H and the contents of 12 bits from addresses 0.0CH to 0.0FH are compared. If identical, jump is made to LAB1; if different, jump is made to LAB2.

```
        SET2 CMP, Z    ;  CMP flag ← 1, Z flag ← 1
        SUB  00H, 0CH  ;  The contents of addresses 0.00H-0.03H
        SUBC 01H, 0DH  ;  are not changed because the CMP flag is
        SUBC 02H, 0EH  ;  set.
        SUBC 03H, 0FH
        SKF1 Z         ;  If proven as identical by comparison, Z
        BR   LAB1      ;  flag = 1; if proven as different, Z
        BR   LAB2      ;  flag = 0.

LAB1:   ⋮
LAB2:   ⋮
```

3.8 SUBC m, #i

Subtract immediate data from data memory with carry flag

(1) Instruction code

10011	m_H	m_L	i

(2) Function

If CMP = 0: M ← (M) – i – CY

The immediate data i and the value of carry flag (CY) are subtracted from the content of data memory addressed by M, and the result is stored into the data memory addressed by M.

If CMP = 1: (M) – i – CY

The result is not stored. Only the flag is changed.

If a borrow occurs as a result of subtraction, the carry flag (CY) is set; if no borrow occurs, the carry flag (CY) is reset.

If the result of subtraction is other than zero, then zero flag (Z) is reset.

If the compare flag is reset (CMP = 0) when the result of subtraction is zero, the zero flag (Z) is set. If the compare flag is set (CMP = 1), the zero flag (Z) will not change when the result of subtraction turns zero.

There are two types of subtraction: binary operation and BCD operation. The subtraction type is specified by the BCD flag (BCD) of PSW.

(3) **Example 1**

Value 5 is subtracted from the contents of 12 bits of addresses 0.0DH to 0.0FH, and the result is stored to addresses 0.0DH to 0.0FH.

```
0.0FH ← (0.0FH) – 05H
0.0EH ← (0.0EH) – CY
0.0DH ← (0.0DH) – CY
SUB  0FH, #05H
SUBC 0EH, #00H
SUBC 0DH, 00H
```

Example 2

Value 5 is subtracted from the contents of 12 bits of addresses 0.4DH to 0.4FH, and the result is stored into addresses 0.4DH to 0.4FH.

```
0.4FH ← (0.4FH) – 05H
0.4EH ← (0.4EH) – CY
0.4DH ← (0.4DH) – CY
MOV  BANK, #00H ;  Data memory bank 0
MOV  IXH, #00H  ;  IX ← 00001000000B (0.40H)
MOV  IXM, #04H  ;
MOV  IXL, #00H  ;
SET1 IXE        ;  IXE flag ← 1
SUB  0FH, #5    ;  (0.4FH) (0.4FH) – 05H
SUBC 0EH, #0    ;  (0.4EH) (0.4EH) – CY
SUBC 0DH, #0    ;  (0.4DH) (0.4DH) – CY
```

Example 3

The contents of 12 bits of addresses 0.00H to 0.03H and 0A3FH of the immediate data are compared. If identical, jump is made to LAB1; if different, jump is made to LAB2.

```
        SET2 CMP, Z     ;  CMP flag ← 1, Z flag ← 1
        SUB 00H, #0H    ;  The contents of addresses 0.00H to 0.03H
        SUBC 01H, #AH   ;  remain unchanged because the CMP flag is
        SUBC 02H, #3H   ;  set.
        SUBC 03H, #FH
        SKF1  Z         ;  If identical in comparison, Z flag = 1;
        BR    LAB1      ;  if different, Z flag = 0
        BR    LAB2
            :
            :
LAB1:
            :
            :
LAB2:
            :
```

3.9 INC AR

Increment address register

(1) Instruction code

00111	000	1001	0000

(2) Function

AR ← (AR) + 1

Address register (AR) is incremented.

(3) **Example 1**

Value 1 is added to the contents of 16 bits of AR3 to AR0 (address register) in the system register, and the result is stored from AR3 to AR0.

```
AR0 ← AR0 + 1
AR1 ← AR1 + CY
AR2 ← AR2 + CY
AR3 ← AR3 + CY
```

INC AR

This instruction can be performed by using addition instruction as follows:

```
ADD  AR0, #01H
ADDC AR1, #00H
ADDC AR2, #00H
ADDC AR3, #00H
```

Example 2

The table data is transferred to DBF (data buffer) in units of 16 bits (one address). (For details, refer to 3.26 "MOVT Instruction".)

```
; Address          Table data
010H   DW          0F3FFH
011H   DW          0A123H
012H   DW          0FFF1H
013H   DW          0FFF5H
014H   DW          0FF11H
       :
       :
       MOV         AR3, #0H  ;  Table data address
       MOV         AR2, #0H  ;  0010H is set into address
       MOV         AR1, #1H  ;  register.
       MOV         AR0, #0H
LOOP:
       MOVT        @AR       ;  Table data is read into DBF.
       :
       :                     ;  Table data referencing
       :
       INC         AR        ;  Address register is incremented
       BR          LOOP         by 1.
```

(4) Note

The number of bits allowed for use with address registers (AR3, AR2, AR1, AR0) vary with the device types. When using, reference should be made to the appropriate manual of the device to be used.

3.10 INC IX

Increment index register

(1) Instruction code

00111	000	1000	0000

(2) Function

IX ← (IX) + 1

The index register (IX) is incremented.

(3) **Example 1**

Value 1 is added to the content of 12 bits of IXH to IXL (index register) in the system register, and the result is stored into the IXH to IXL.

```
IXL ← IXL + 1
IXM ← IXM + CY
IXH ← IXH + CY
INC IX
```

This operation can be performed by using the addition instruction as follows:

```
ADD  IXL, #01H
ADDC IXM, #00H
ADDC IXH, #00H
```

Example 2

The contents of data memory 0.00H to 0.73H are all turned '0' using the index register.

```
    MOV  IXH, #00H   ;  The contents of index register
    MOV  IXM, #00H   ;  are all set at 00H of bank 0.
    MOV  IXL, #00H   ;
RAM clear:
    SET1 IXE         ;  IXE flag ← 1
    MOV  00H, #00H   ;  0 is written into the data memory indicated by the index register.
    CLR1 IXE         ;  IXE flag ← 0
    INC  IX
    SET2 CMP, Z      ;  CMP flag ← 1, Z flag ← 1
    SUB  IXL, #03H   ;  Whether the content of index
    SUBC IXM, #07H   ;  register turned to 73H of bank 0
    SUBC IXH, #00H   ;  is checked.
    SKT1 Z           ;  Loop is repeated until the contents
    BR   RAM clear   ;  of index register turns to 73H of
                     ;  bank 0.
```

3.11 SKE m, #i

Skip if data memory equal to immediate data

(1) Instruction code

01001	m_H	m_L	i

(2) Function

If the content of the data memory addressed by M is equal to the value of immediate data i, then the instruction that follows is skipped.

(3) **Example**

0FH is transferred to address 24H if the content of address 24H is 0. If not 0, control jumps to OPE1.

```
    SKE 24H, #00H
    BR  OPE1
    MOV 24H, #0FH
OPE1 :
```

3.12 SKGE m, #i

Skip if data memory greater than or equal to immediate data

(1) Instruction code

11001	m_H	m_L	i

(2) Function

If the content of the data memory addressed by M is greater than the value of immediate data i, then the instruction that follows is skipped.

(3) **Example**

If the 8-bit data stored in address 1FH (upper) and address 2FH (lower) is greater than the immediate data '17H', then RET occurs; otherwise, RETSK occurs.

```
SKGE   1FH, #1
RETSK
SKNE   1FH, #1
SKLT   2FH, #8  ;  7+1
RET
RETSK
```

3.13 SKLT m, #i

Skip if data memory less than immediate data

(1) Instruction code

11011	m_H	m_L	i

(2) Function

If the content of data memory addressed by M is less than the value of immediate data i, then the instruction that follows is skipped.

(3) **Example**

If the content of address 10H is greater than the immediate data '6', then 01H is stored into address 0FH; if less than the immediate data '6', 02H is stored into address 0FH.

```
MOV   0FH, #02H
SKLT  10H, #06H
MOV   0FH, #01H
```

3.14 SKNE m, #i

Skip if data memory not equal to immediate data

(1) Instruction code

01011	m_H	m_L	i

(2) Function

If the content of data memory addressed by M is different from the value of immediate data i, then the instruction that follows is skipped.

(3) **Example**

If the content of address 1FH is 1 and the content of 1EH is 3, then control jumps to XYZ; if not, control jumps to ABC. Comparison of 8 bits can be performed by combining the instructions as shown below:


```
SKNE 1FH, #1
SKE 1EH, #3
BR  ABC
BR  XYZ
```

The same operation can be performed by using the compare flag and zero flag, as shown below.

```
SET2 CMP, Z        ;  CMP flag ← 1, Z flag ← 1
SUB 1FH, #1
SUBC 1EH, #3
SKT1 Z
BR  ABC
BR  XYZ
```

3.15 AND m, #i

AND between data memory and immediate data

(1) Instruction code

10100	m_H	m_L	i

(2) Function

M ← (M) AND i

The content of data memory addressed by M and the immediate data are ANDed, and the result is stored into the data memory addressed by M.

(3) **Example 1**

Bit 3 (MSB) of address 0.03H is reset.

0.03H ← (0.03H) and 0111B

Address 0.03H

0	x	x	x

x: Don't care

```
AND     03H, #0111B
```

Example 2

All the bits of address 0.03H are reset.

```
AND     03H, #0000B
```

or

```
MOV     03H, #00H
```

3.16 AND r, m

AND between general register and data memory

(1) Instruction code

00100	m_H	m_L	r

(2) Function

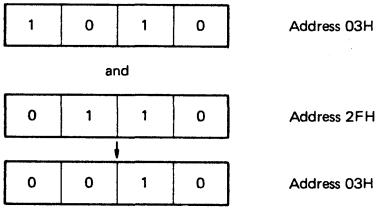
R ← (R) AND (M)

The content of general-purpose register indicated by R and the content of data memory addressed by M are ANDed, and the result is stored into the general-purpose register indicated by R.

(3) **Example 1**

The content (1010B) of address 0.03H and the content (0110B) of address 0.2FH are ANDed, and the result (0010B) is stored into address 0.03H.

0.03H ← (0.03H) and (0.2FH)




```
MOV 03H, #1010B
MOV 2FH, #0110B
AND 03H, 2FH
```

3.17 OR m, #i

OR between data memory and immediate data

(1) Instruction code

10110	m_H	m_L	i

(2) Function

M ← (M) OR i

The content of data memory addressed by M and the immediate data i are ORed, and the result is stored into the data memory addressed by M.

(3) **Example 1**

Bit 3 (MSB) of address 0.03H is set.

0.03H ← (0.03H) or 1000B

Address 0.03H

1	x	x	x

x: Don't care

```
OR      03H, #1000B
```

Example 2

All the bits of address 0.03H are set.

```
OR      03H, #1111B
or
MOV     03H, #0FH
```

3.18 OR r, m

OR between general register and data memory

(1) Instruction code

00110	m_H	m_L	r

(2) Function

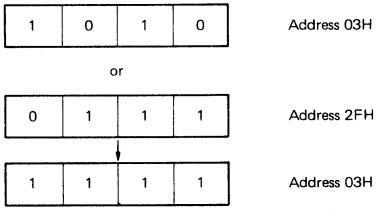
R ← (R) OR (M)

The content of general-purpose register indicated by R and the content of data memory addressed by M are ORed, and the result is stored into the general-purpose register indicated by R.

(3) **Example 1**

The content (1010B) of address 0.03H and the content (0111B) of address 0.2FH are ORed, and the result (1111B) is stored into address 0.03H.

0.03H ← (0.03H) or (0.2FH)




```
MOV   03H, #1010B
MOV   2FH, #0111B
OR    03H, 2FH
```

3.19 XOR m, #i

Exclusive OR between data memory and immediate data

(1) Instruction code

10101	m_H	m_L	i

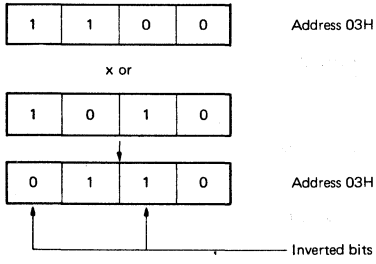
(2) Function

M ← (M) XOR i

The content of data memory addressed by M and the immediate data i are XORed, and the result is stored into the data memory addressed by M.

(3) **Example**

The bit 1 and bit 3 of address 0.03H are inverted, and the result is stored into address 03H.



XOR 03H, #1010B

3.20 XOR r, m

Exclusive OR between general register and data memory

(1) Instruction code

00101	m_H	m_L	r

(2) Function

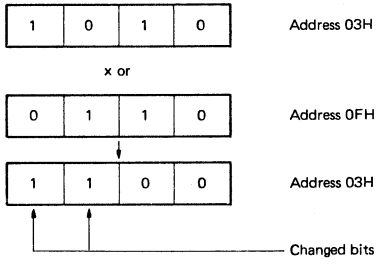
R ← (R) XOR (M)

The content of general-purpose register indicated by R and the content of data memory addressed by M are XORed, and the result is stored into the general-purpose register indicated by R.

(3) **Example 1**

The content of address 0.03H and the content of address 0.0FH are compared, and the different bits are set and stored into address 0.03H. If all bits of 0.03H are reset (that is, the address 0.03H and address 0.0FH have the same content), then control jumps to LBL1; otherwise, jumps to LBL2.

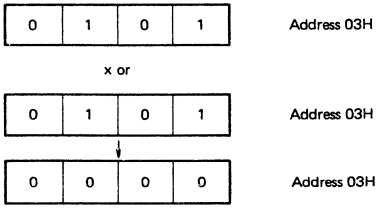
This operation occurs when the status of an alternate switch (content of address 0.03H) and internal status (content of address 0.0FH) are compared and branch is made to the processing of changed switch.




```
XOR   03H, 0FH
SKNE  03H, #00H
BR    LBL1
BR    LBL2
```

Example 2

The content of address 0.03H is cleared.




```
XOR   03H, 03H
```

3.21 LD r, m

Load data memory to general register

(1) Instruction code

01000	m_H	m_L	r

(2) Function

R ← (M)

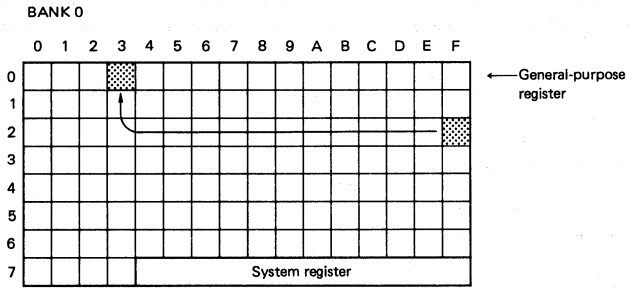
The content of data memory addressed by M is stored into the general-purpose register indicated by R.

(3) **Example 1**

The content of address 0.2FH is stored into address 0.03H.

0.03H ← (0.2FH)

```
LD      03H, 2FH
```

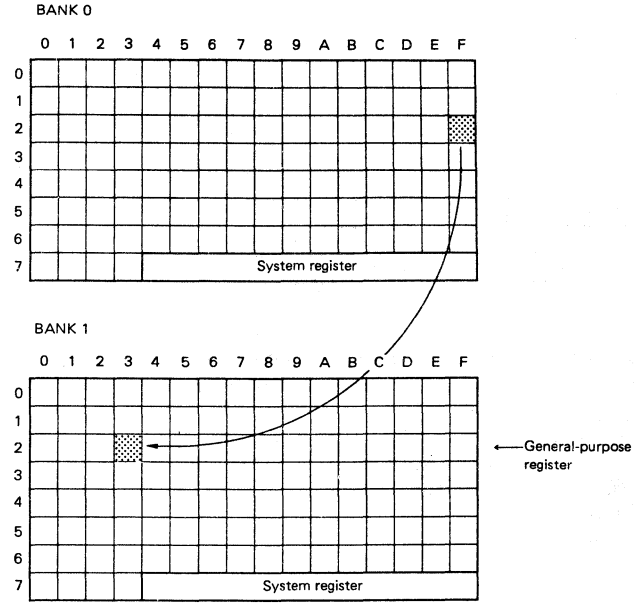


Example 2

When row address 2 of bank 1 (1.20H to 1.2FH) is specified as general-purpose register (RPH = 1, RPL = 4), the content of address 0.2FH is stored into address 1.23H.

1.23H ← (0.2FH)

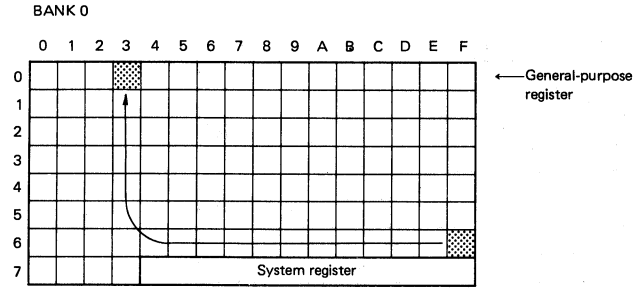
```
MOV  RPH, #01H   ;  Bank 1 is selected for general-purpose register.
MOV  RPL, #04H   ;  Row address 2 is selected for general-purpose register
LD   03H, 2FH
```



Example 3

The content of address 0.6FH is stored into address 0.03H. If IXE = 1, IXH = 0, IXM = 4, and IXL = 0, that is, if IX = 0.40H, then the data memory 0.6FH can be specified by setting the data memory address at 2FH.

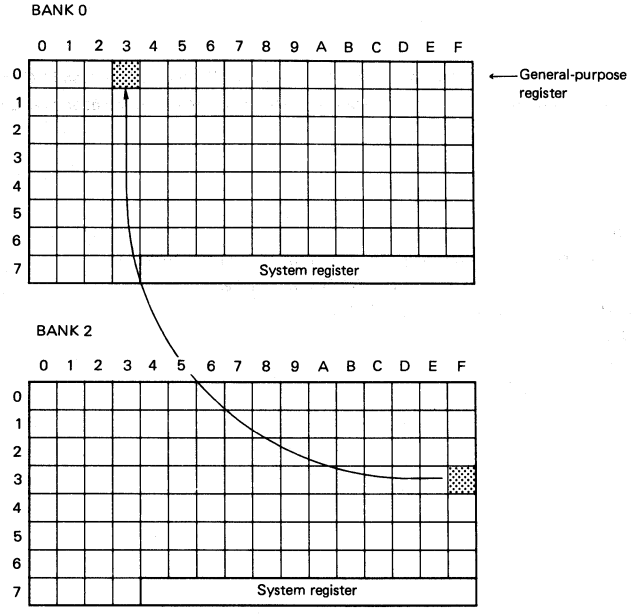
```
IXH ← 00H
IXM ← 04H
IXL ← 00H
IXE flag ← 1
0.03H ← (0.6FH)
          └── Address obtained by computing OR of the content (0.40H) of
              index register and the content (0.2FH) of data memory.
MOV  IXH, #00H    ;  IX ← 00001000000B (0.40H)
MOV  IXM, #04H
MOV  IXL, #00H
SET1 IXE          ;  IXE flag ← 1
LD   03H, 2FH
```



Example 4

The content of address 2.3FH is stored into address 0.03H. If IXE = 1, IXH = 1, IXM = 1, and IXL = 0, that is, if IX = 2.10H, then the data memory 2.3FH can be specified by setting the data memory address at 2FH.

```
0.03H ← (2.3FH)
          └──Address obtained by computing OR of the content (2.10H) of
             index register and the content (0.2FH) of data memory
MOV  IXH, #01H    ;  IX ← 00100010000B (2.10H)
MOV  IXM, #01H
MOV  IXL, #00H
SET1 IXE          ;  IXE flag ← 1
LD   03H, 2FH
```



(4) **Note**

The 1st operand of the 'LD r, m' instruction is the column address of the general-purpose register. If described as shown below, the column address of the general-purpose register is set at 03H. This will cause no error in assembling.

```
LD  13H, 2FH
    └── Column address of general-purpose register is meant, and the lower four bits
        are significant. If row address 0 of bank 0 is specified as general-purpose
        register, the address 03H is specified.
```

3.22 ST m, r

Store general register to data memory

(1) Instruction code

11000	m_H	m_L	r

(2) Function

M ← (R)

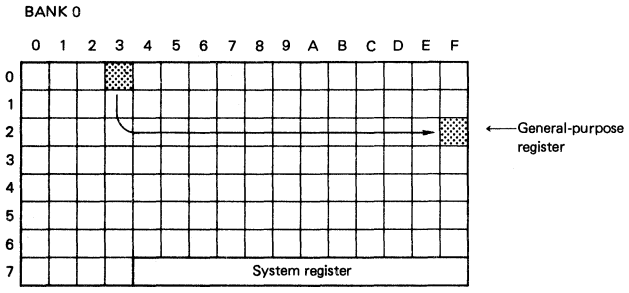
The content of general-purpose register indicated by R is stored into the data memory addressed by M.

(3) **Example 1**

The content of address 0.03H is stored into address 0.2FH.

(0.2FH) ← (0.03H)

```
ST   2FH, 03H      ;  The content of general-purpose register is transferred to data memory.
```

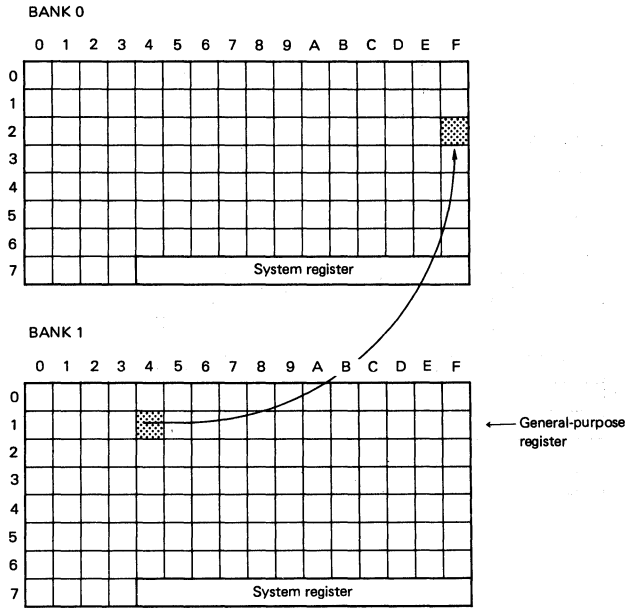


Example 2

The content of address 1.13H is stored into address 0.2FH. The general-purpose register is specified at row address 1 of bank 1 (1.10H to 1.1FH) by using register pointer.

(0.2FH) ← (1.13H)

```
MOV  RPH, #01H     ;  General-purpose register is set in bank 1
MOV  RPL, #02H     ;  General-purpose register is set at row address 1.
ST   2FH, 13H      ;  The content of general-purpose register is transferred to data memory.
```

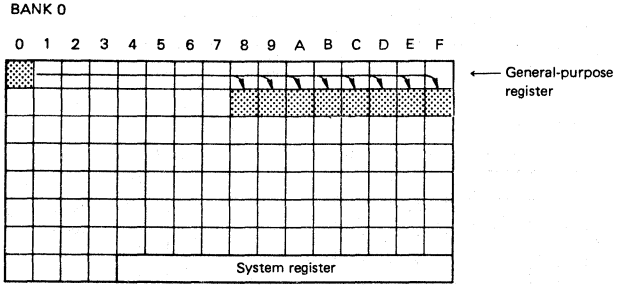


Example 3

The content of address 0.00H is stored into the addresses 0.18H to 0.1FH. The data memory (18H to 1FH) is specified by index register.

```
(0.18H) ← (0.00H)
(0.19H) ← (0.00H)
        :
        :
(0.1FH) ← (0.00H)
    MOV  IXH, #00H ;   IX ← 00000000000B (0.00H)
    MOV  IXM, #00H
    MOV  IXL, #00H ;   Address 0.00H is specified for data memory.
```

```
LOOP1:
    SET1 IXE        ;  IXE flag ← 1
    ST 18H, 00H     ;  (0.1XH) ← (0.00H)
    CLR1 IXE        ;  IXE flag ← 0
    INC IX          ;  Index register + 1
    SKGE IXL, #08H
    BR LOOP1
```



3.23 MOV @r, m

Move data memory to destination indirect

(1) Instruction code

01010	m_H	m_L	r

(2) Function

If MPE = 1:

[(MP), (R)] ← (M)

If MPE = 0:

[m_H, (R)] ← (M)

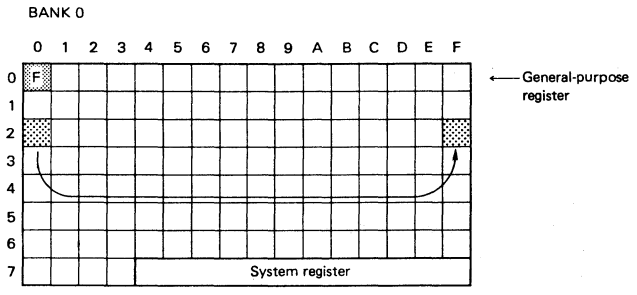
The content of data memory addressed by M is stored into the data memory indicated by general-purpose register R. If MPE = 0, transfer occurs within the same row address of the same bank.

(3) **Example 1**

The content of address 0.20H is stored into address 0.2FH. The destination data memory is specified by the column address indicated by the general-purpose register (00H) and the row address of data memory (20H).

(0.2FH) ← (0.20H)

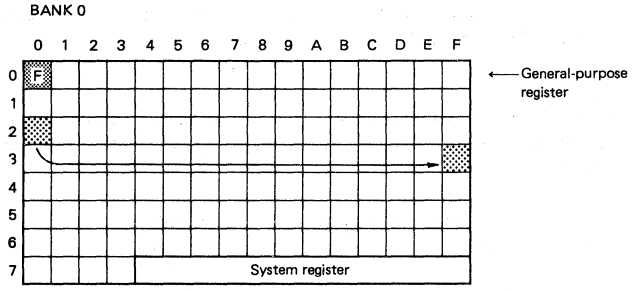
```
CLR1 MPE          ;  MPE flag ← 0
MOV 00H, #0FH     ;  Column address is set at general-purpose register
MOV @00H, 20H     ;  Store.
```



Example 2

The content of address 0.20H is stored into address 0.3FH. The destination data memory is specified by the column address indicated by general-purpose register (00H) and the row address indicated by the memory pointer (MP).

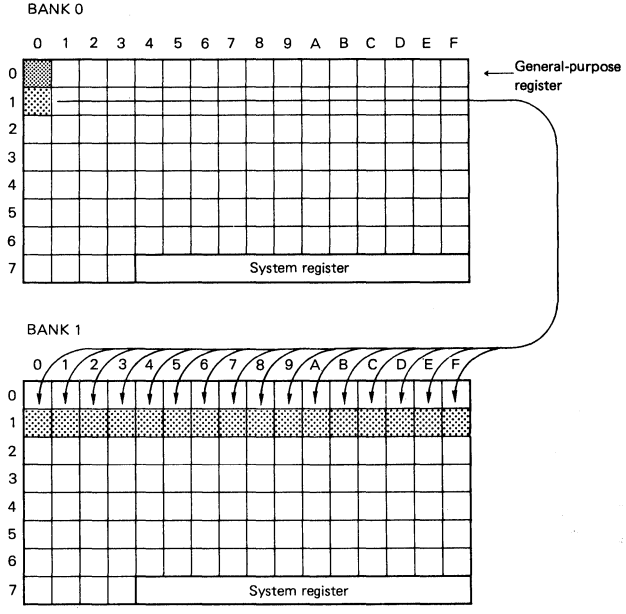
```
(0.3FH) ← (0.20H)
MOV  RPH, #00H   ;  General-purpose register is set on bank 0
MOV  RPL, #00H   ;  General-purpose register is set at row address 0
MOV  00H, #0FH   ;  Column address is set in general-purpose register
MOV  MPH, #00H   ;  Row address is set in memory pointer.
MOV  MPL, #03H
SET1 MPE         ;  MPE flag ← 1
MOV  @00H, 20H   ;  Store.
```



Example 3

The content of address 0.10H is stored into addresses 1.10H to 1.1FH.

```
(1.10H) ← (0.10H)
(1.11H) ← (0.10H)
        :
        :
(1.1FH) ← (0.10H)
MOV  RPH, #00H   ;  General-purpose register is set on bank 0.
MOV  RPL, #00H   ;  General-purpose register is set at row address 0.
MOV  00H, #00H   ;  Column address is set in general-purpose register.
MOV  MPH, #00H   ;  Bank 1 and row address 1 are set for memory pointer.
MOV  MPL, #09H
SET1 MPE         ;  MPE flag ← 1
LOOP 1:
MOV  @00H, 10H   ;  [(MP), (00H)] ← (10H)
ADD  00H, #01H   ;  Column address + 1
SKT1 CY          ;  Operation completed for address 1FH of bank 1?
BR   LOOP1
```


BANK 0
0 1 2 3 4 5 6 7 8 9 A B C D E F
0
1
2
3
4
5
6
7
System register
General-purpose register
BANK 1
0 1 2 3 4 5 6 7 8 9 A B C D E F
0
1
2
3
4
5
6
7
System register

3.24 MOV m, @r

Move data memory to destination indirect

(1) Instruction code

11010	m_H	m_L	r

(2) Function

If MPE = 1: (M) ← [(MP), (R)]

If MPE = 0: (M) ← [m_H, (R)]

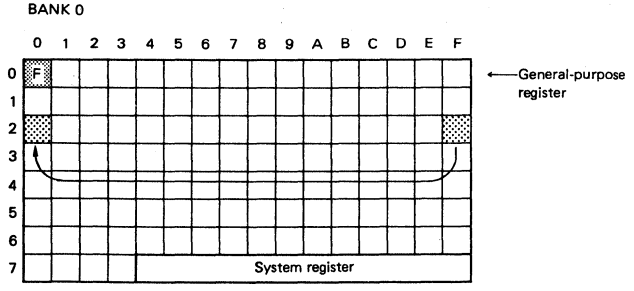
The content of data memory indicated by the general-purpose register R is stored into the data memory addressed by M. When MPE = 0, this movement occurs within the same row address on the same bank.

(3) **Example 1**

The content of address 0.2FH is stored into address 0.20H. The destination data memory is specified by the column address indicated by the general-purpose register (00H) and the row address of the data memory (20H).

(0.20H) ← (0.2FH)

```
CLR1 MPE          ; MPE flag ← 0
MOV 00H, #0FH     ; Column address is set at general-purpose register
MOV 20H, @00H     ; Store
```

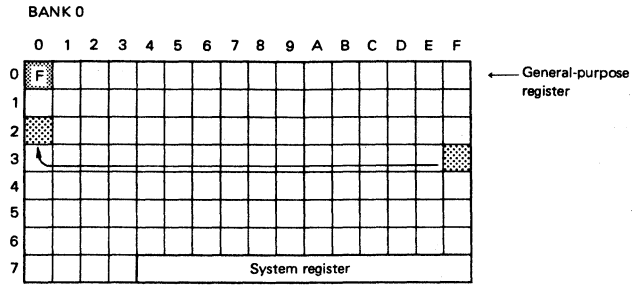


Example 2

The content of address 0.3FH is stored into address 0.20H. The destination data memory is specified by the column address indicated by general-purpose register (00H) and the row address indicated by memory pointer (MP).

(0.20H) ← (0.3FH)

```
MOV 00H, #0FH     ; Column address is set at general-purpose register
MOV MPH, #00H     ; Row address is set at memory pointer.
MOV MPL, #03H     ;
SET1 MPE          ; MPE flag ← 1
MOV 20H, @00H     ; Store
```

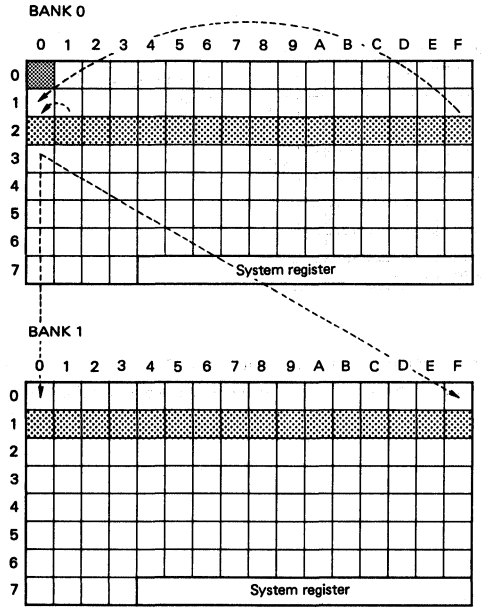


Example 3

The contents of addresses 0.20H to 0.2FH are stored into addresses 1.10H to 1.1FH. The storing data memory is specified by the column address indicated by the general-purpose register (00H) and memory pointer (MP) or row address of data memory (20H).

(1.10H) ← (0.20H)
(1.11H) ← (0.21H)
(1.12H) ← (0.22H)
:
:
(1.1FH) ← (0.2FH)

```
        CLR1  MPE          ;  MPE flag ← 0
        MOV   00H, #00H    ;  Column address is set in the general-purpose register.
        MOV   MPH, #00H    ;  Memory pointer is set.
        MOV   MPL, #09H    ;  Bank 1, row address 1
LOOP1:
        MOV   20H, @00H    ;  (20H) ← [2, (00H)]
        SET1  MPE          ;  MPE flag ← 1
        MOV   @00H, 20H    ;  [(MP), (00H)] ← (20H)
        CLR1  MPE          ;  MPE flag ← 0
        ADD   00H, #01H    ;  Column address +1
        SKT1  CY           ;  Up to 1FH of bank 1 terminated
        BR    LOOP1
```


BANK 0
0 1 2 3 4 5 6 7 8 9 A B C D E F
0
1
2
3
4
5
6
7
System register
General-purpose register
The data is transferred via 20H.
BANK 1
0 1 2 3 4 5 6 7 8 9 A B C D E F
0
1
2
3
4
5
6
7
System register

3.25 MOV m, #i

Move immediate data to data memory

(1) Instruction code

11101	m_H	m_L	i

(2) Function

(M) ← i

The immediate data i is stored in the data memory addressed by M.

(3) **Example 1**

The immediate data 0AH is stored to address 0.50H used as data memory.

```
0.50H ← 0AH
MOV 50H, #0AH
```

Example 2

If IXH = 0, IXM = 3, IXL = 2 and IXE flag = 1 when address 0.00H is specified as data memory, then the immediate data 07H is stored into address 0.32H.

```
0.32H ← 07H
MOV IXH, #00H    ;  IX ← 00000110010B (0.32H)
MOV IXM, #03H
MOV IXL, #02H
SET1 IXE         ;  IXE flag ← 1
MOV 00H, #07H
```

3.26 MOVT DBF, @AR

Move program memory data specified by AR to DBF

(1) Instruction code

00111	000	0001	0000

(2) Function

SP ← SP – 1,
STACK ← PC,
DBF ← $(AR)_{rom}$,
PC ← STACK,
SP ← SP + 1

The content of program memory addressed by address register AR is stored into data buffer DBF.
Attention should be paid to the nesting such as subroutine and interruption, because this instruction temporarily uses one level of stack.

(3) **Example 1**

The 16-bit table data is transferred to the data buffers (DBF3, DBF2, DBF1, DBF0) according to the values of address registers (AR3, AR2, AR1, AR0) in the system register.

```
                ;*
                ;** Table data
                :*
Address         ORG 0010H
0010H           DW 0000000000000000B ; (0000H)
0011H           DW 1010101111001101B ; (0ABCDH)
                                :
                ;*
                ;** Table reference program
                ;*
                MOV AR3, #00H  ;  AR3 ← 00H  0011H is set in address register.
                MOV AR2, #00H  ;  AR2 ← 00H
                MOV AR1, #01H  ;  AR1 ← 01H
                MOV AR0, #01H  ;  AR0 ← 01H
                MOVT DBF, @AR  ;  Data of address 0011H is transferred to DBF.
```

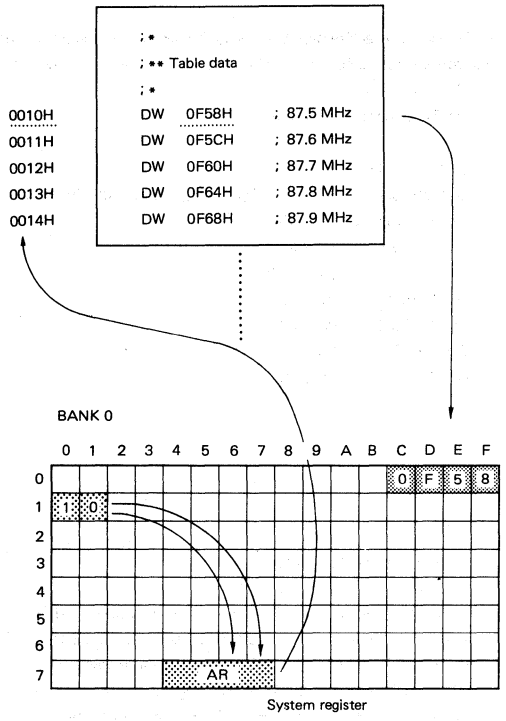
In this case, the data stored in DBF is shown below.

DBF3 = 0AH
DBF2 = 0BH
DBF1 = 0CH
DBF0 = 0DH

Example 2

The channel number is set at addresses 0.10H and 0.11H as data memory, and the divided value (N value) of PLL is obtained according to the content of the memory. The N value is then transferred to the PLL register.

```
                ;*
                ;** Table data for N value
                ;*
Address         ORG 0010H
0010H           DW 0F58H   ;  87.5 MHz (Lowest frequency 00 channel)
0011H           DW 0F5CH   ;  87.6 MHz
0012H           DW 0F60H   ;  87.7 MHz
0013H           DW 0F64H   ;  87.8 MHz
0014H           DW 0F68H   ;  87.9 MHz
0015H           DW 0F6CH   ;  88.0 MHz
0016H           DW 0F70H   ;  88.1 MHz
0017H           DW 0F74H   ;  88.2 MHz
                    :
                    :
                    :
                    :
                    :
                    :
                ;*
                ;** N value setting program
                ;*
                MOV  RPH, #00H   ;  RPH ← 00H  Row address 7 (0.70H
                MOV  RPL, #0EH   ;  RPL ← 0EH to 0.7FH) is set as
                MOV  AR3, #00H   ;  AR3 ← 0  general-purpose
                MOV  AR2, #00H   ;  AR2 ← 0  register.
                LD   AR1, 10H    ;  AR1 ← 10H  Channel data upper
                LD   AR0, 11H    ;  AR0 ← 11H  Channel data lower
                ADD  AR1, #01H   ;  0010H is added to the address
                ADDC AR2, #00H   ;  register since table data start
                ADDC AR3, #00H   ;  address starts at address 0010H.
                MOVT DBF, @AR    ;  Table data is stored to DBF.
                PUT  PLLR, DBF   ;  N value is transferred to PLL register (PLLR).
```



(4) **Notes**

1. The number of bits allowed for use with address registers (AR3, AR2, AR1, AR0) vary with the device types. When using, reference should be made to the appropriate manual of the device to be used.
2. When executing 'MOVT' instruction, one level of stack is used. Accordingly, sufficient care should be exercised to the stack level when using this instruction within a subroutine or interrupt processing routine.

3.27 PUSH AR

Push address register

(1) Instruction code

00111	000	1101	0000

(2) Function

SP ← SP – 1,

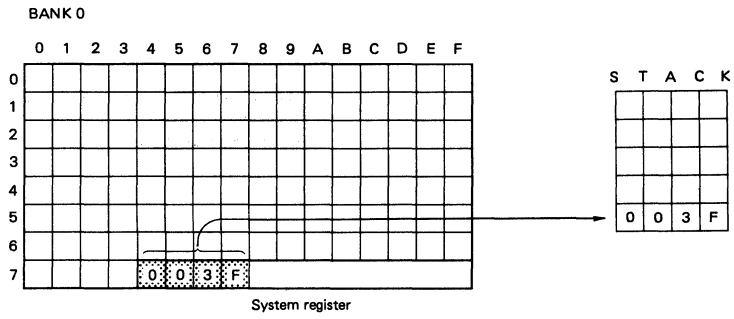
STACK ← AR

The value of address register AR is stored into STACK after decrement of the stack pointer SP.

(3) **Example 1**

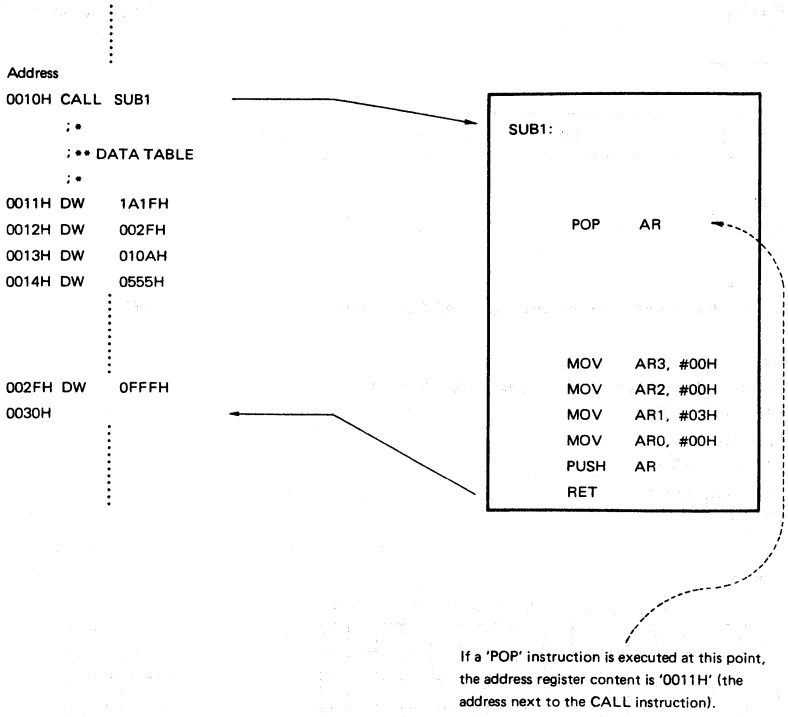
The address register is set at 003FH and stored into the stack.

```
MOV AR3, #00H
MOV AR2, #00H
MOV AR1, #03H
MOV AR0, #0FH
PUSH AR
```



Example 2

When the data table is placed behind a subroutine, the return address of the subroutine is set in the address register for returning.


Address
0010H CALL SUB1
;•
;•• DATA TABLE
;•
0011H DW 1A1FH
0012H DW 002FH
0013H DW 010AH
0014H DW 0555H
002FH DW 0FFFH
0030H
SUB1:
POP AR
MOV AR3, #00H
MOV AR2, #00H
MOV AR1, #03H
MOV AR0, #00H
PUSH AR
RET
If a 'POP' instruction is executed at this point, the address register content is '0011H' (the address next to the CALL instruction).

3.28 POP AR

Pop address register

(1) Instruction code

00111	000	1100	0000

(2) Function

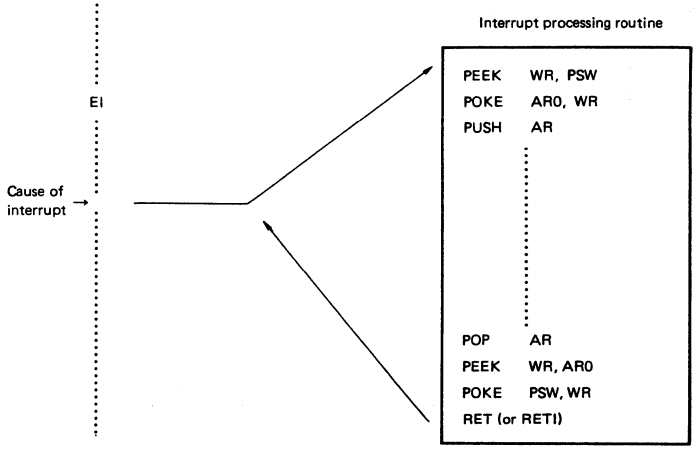
AR ← STACK,

SP ← SP + 1

The content of STACK is taken out to the address register, then the stack pointer SP is incremented.

(3) **Example**

When performing an interrupt processing, PSW may be changed within the interrupt processing routine. In such a case, the content of PSW is transferred to the address register via WR at the beginning of the interrupt processing, and then it is saved into the STACK by a 'PUSH' instruction. Before returning of the routine, the saved content is put into the address register by a 'POP' instruction, and then it is transferred to PSW via WR.



3.29 PEEK WR, rf

Peek register file to window register

(1) Instruction code

00111	rf_H	0011	rf_L

(2) Function

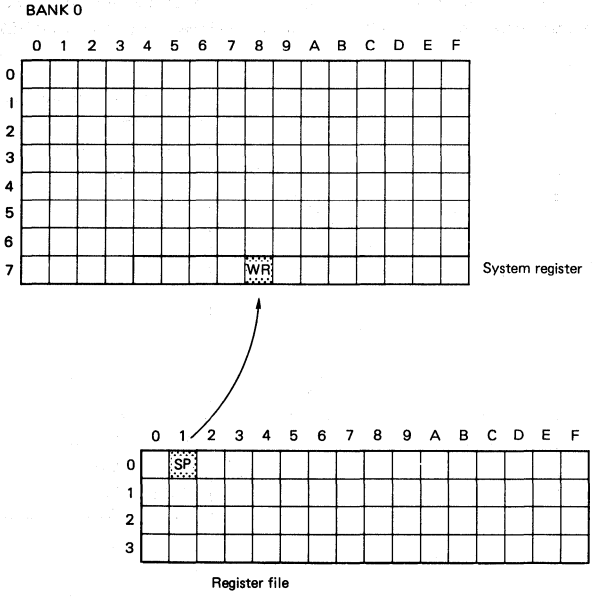
WR ← (rf)

The content of the register file addressed by rf is stored into the window register WR.

(3) **Example 1**

The content of the stack pointer SP of address 01H in the register file is stored into the window register.

```
PEEK   WR, SP
```



3.30 POKE rf, WR

Poke window register to register file

(1) Instruction code

00111	rf_H	0010	rf_L

(2) Function

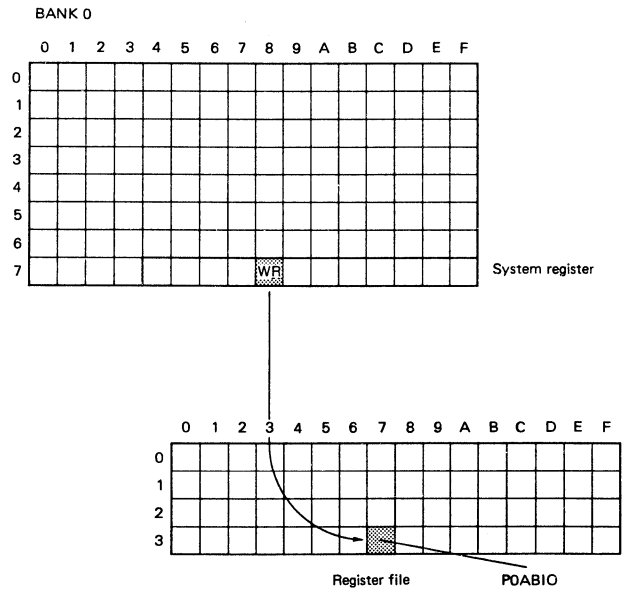
(rf) ← WR

The content of window register WR is stored into the register file addressed by rf.

(3) **Example 1**

The immediate data 0FH is stored into the register file POABIO via the window register.

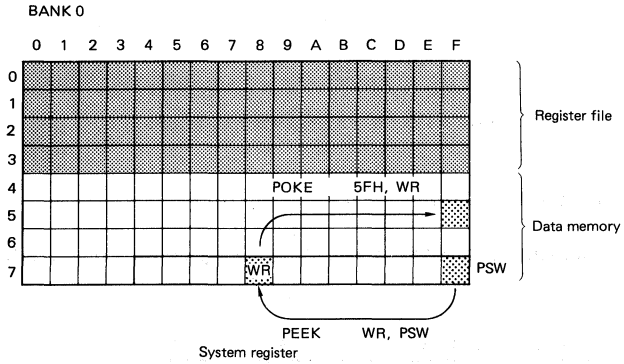
```
MOV   WR, #0FH
POKE  POABIO, WR ;   Each of POA0, POA1, POA2 and POA3 is set in the output mode.
```



(4) **Note**

The 'PEEK, POKE' instruction permits accessing of addresses 40H to 7FH in each bank of the data memory in addition to the register file. For example, this instruction can be used in the following way.

```
PEEK WR, PSW    ;  The content of PSW (7FH) in system register is stored into WR.
POKE 5FH, WR    ;  The content of WR is stored into address 5FH of data memory.
```



3.31 GET DBF, p

Get peripheral data to data buffer

(1) Instruction code

00111	P_H	1011	P_L

(2) Function

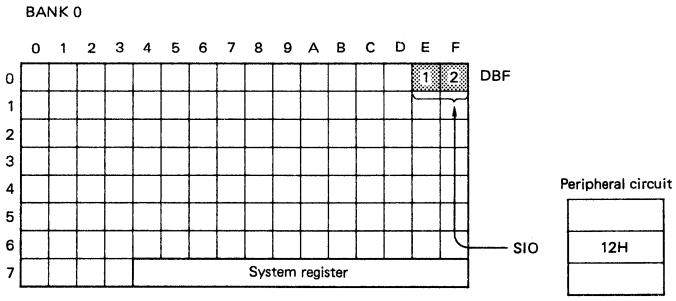
DBF ← (p)

The content of peripheral circuit addressed by p is stored into the data buffer DBF.

(3) **Example 1**

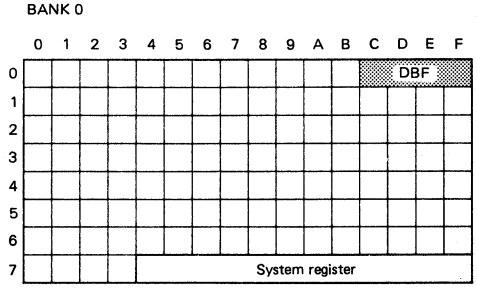
The content (8 bits) of the peripheral shift register (SIO) is stored into data buffers DBF0 and DBF1.

GET DBF, SIO



(4) **Notes**

1. The data buffer is allocated to 0CH, 0DH, 0EH, and 0FH in bank 0 of the data memory, irrespective of the value of the bank register.



2. The data buffer has a total of 16 bits. The number of bits to be used as the unit of input/output varies with the peripheral circuit accessed by 'GET' instruction. For example, if a 'GET' instruction is executed for a peripheral circuit whose input/output is done in units of 8 bits, data is stored to the lower 8 bits (DBF1, DBF0) of the data buffer DBF. Pay attention to the number of bits required as the unit of input/output because it varies with the peripheral circuits of each device.

3.32 PUT p, DBF

Put data buffer to peripheral

(1) Instruction code

00111	PH	1010	PL

(2) Function

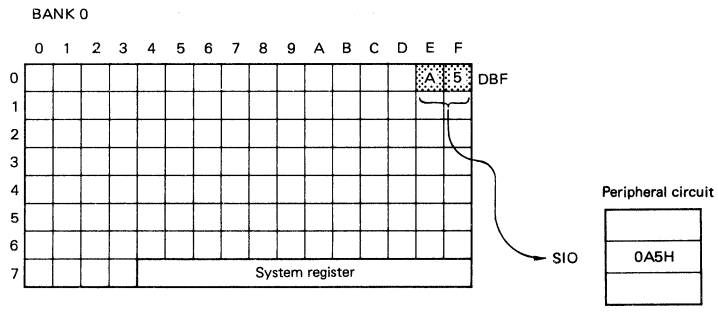
(p) ← DBF

The content of data buffer DBF is stored into the peripheral circuit addressed by p.

(3) **Example 1**

0AH and 05H are set into data buffers DBF1 and DBF0, respectively, and are then transferred to the shift register (SIO) of peripheral circuit.

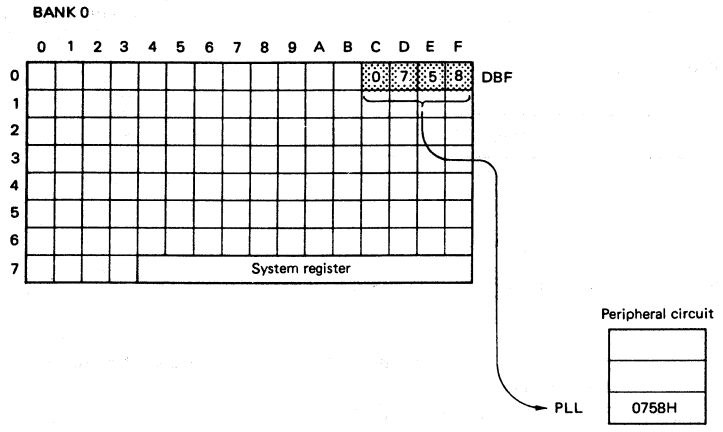
```
MOV BANK, #00H ;  Data memory bank 0
MOV DBF0, #05H
MOV DBF1, #0AH
PUT SIO
    DBF
```



Example 2

The data 0758H is set as PLL data in data buffers DBF0-DBF3, and then it is transferred to PLL register (PLL) of the peripheral circuit.

```
MOV DBF3, #00H
MOV DBF2, #07H
MOV DBF1, #05H
MOV DBF0, #08H
PUT PLL, DBF
```



(4) **Note**

The data buffer size is 16 bits. The number of bits required as the unit of input/output varies with the peripheral circuit accessed by 'PUT' instruction. For example, the shift register SIO requires 8-bit input/output. When a 'PUT' instruction is executed, the contents of lower 8 bits (DBF1, DBF0) of data buffer DBF are transferred to the peripheral circuit. (The contents of DBF3 and DBF2 are not transferred.)

3.33 SKT m, #n

Skip next instruction if data memory bits are true

(1) Instruction code

11110	m_H	m_L	n

(2) Function

If the ANDed result of the content of data memory addressed by M and immediate data n is not 0, then the next one instruction is skipped.

(3) **Example 1**

If bit 0 of address 03H is '1', control jumps to AAA; if '0', it jumps to BBB.

```
SKT  03H, #0001B
BR   BBB
BR   AAA
```

Example 2

If bit 0 and bit 1 of address 03H are both '1', the next instruction is skipped.

```
SKT  03H, #0011B
```

	B_3	B_2	B_1	B_0	
Skip condition 03H	x	x	1	1	x: don't care

Example 3

The following two instructions provide the same execution result.

- SKT 13H, #1111B
- SKE 13H, #0FH

3.34 SKF m, #n

Skip next instruction if data memory bits are false

(1) Instruction code

11111	m_H	m_L	n

(2) Function

When the result of AND of the content of data memory addressed by M and the immediate data n is 0, the next one instruction is skipped.

(3) **Example 1**

If bit 2 of address 13H is '0', 00H of the immediate data is stored into address 0FH in the data memory; if '1', control jumps to ABC.

```
SKF  13H, #0100B
BR   ABC
MOV  0FH, #00H
```

Example 2

If bit 3 and bit 0 of address 29H are both '0', the next instruction is skipped.

```
SKF  29H, #1001B
```

	B_3	B_2	B_1	B_0	
Skip condition 29H	0	x	x	0	x: don't care

Example 3

The following two instructions provide the same execution result.

- SKF 34H, #1111B
- SKE 34H, #00H

3.35 BR addr

Branch to the address

(1) Instruction code

011	addr

(2) Function

PC ← addr

Control branches to the address indicated by addr.

The range of address to which direct branch by this instruction is allowed is 8K steps from address 0000H to address 1FFFH. When branching is required to address 2000H or after, use the following 'BR @AR' instruction.

(3) **Example**

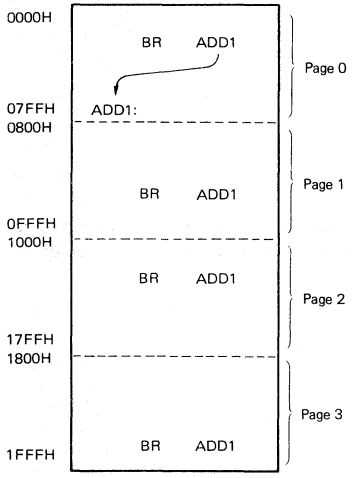
```
FLY   LAB   0FH   ;  FLY = 0FH is defined.
        :
        :
      BR    FLY   ;  Jumps to address 0F.
        :
        :
      BR    LOOP1;  Jumps to LOOP1.
        :
        :
      BR    $+2   ;  Jumps to the address which is lower by 2 than the current address.
        :
        :
      BR    $-3   ;  Jumps to the address which is higher by 3 than the current address.
        :
        :
LOOP1:
```

(4) **Note**

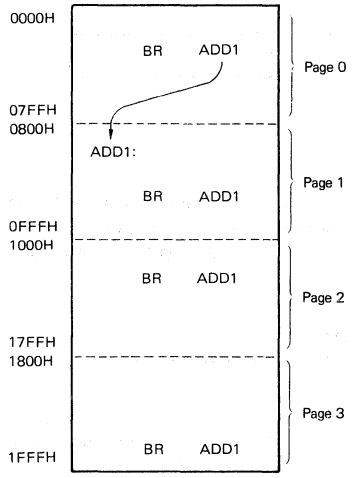
The BR instruction can be described in assembler without mentioning the page. The same description can be used between ROM addresses 0000H and 1FFFH. However, the BR instruction into page 0 (addresses 0000H to 07FFH), BR instruction into page 1 (addresses 07FFH to 0FFFH), BR instruction into page 2 (addresses 1000H to 17FFH), and BR instruction into page 3 (addresses 17FFH to 1FFFH) have respectively different operation codes.

The operation code in page 0 is '0C', in page 1, '0D', in page 2, '0E', and in page 3, '0F'. If the μPD17000 series assembler is used, these operation codes are automatically converted by the assembler by referencing the respective jump destinations.

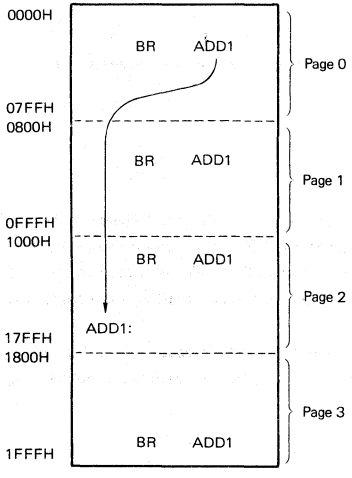
When operation code is '0C'
(The jumping destination address is in page 0)



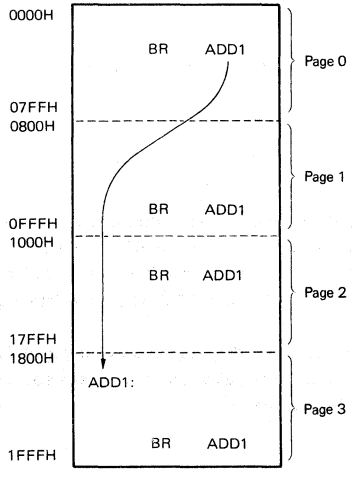
When operation code is '0D'
(The jumping destination address is in page 1)



When operation code is '0E'
(The jumping destination address is in page 2)

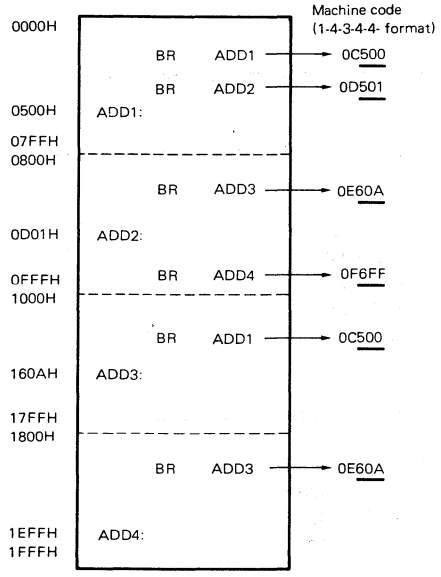


When operation code is '0F'
(The jumping destination address is in page 3)



When batch correction is required in debugging, the programmer is required to convert each of the operation codes '0C', '0D', '0E', and '0F' by himself.

Address must also be converted if the jump destination of BR instruction is in any of address 0000H to 07FFH, address 0800H to 0FFFH, address 1000H to 17FFH, and address 1800H to 1FFFH. In other words, each of address 0000H, address 0800H, address 1000H and address 1800H can be assumed as address 000H, which is incremented by 1, respectively.



Note: The number of pages varies from device to device of the μPD17000 series. Please refer to the manual of the device to be used.

3.36 BR @AR

Branch to the address specified by address register

(1) Instruction code

00111	000	0100	0000

(2) Function

PC ← AR

Control branches to the address indicated by the address register (AR).

(3) **Example 1**

003FH is set in the address register AR (AR0-AR3), and execution jumps to address 003FH by the 'BR @AR' instruction.

```
MOV  AR3, #00H  ;  AR3 ← 00H
MOV  AR2, #00H  ;  AR2 ← 00H
MOV  AR1, #03H  ;  AR1 ← 03H
MOV  AR0, #0FH  ;  AR0 ← 0FH
BR   @AR        ;  Jump to address 003FH
```

Example 2

The branching destination is changed as shown below depending on the content of address 0.10H of the data memory.

```
        Content of 0.10H      Label of destination
              00H       →          AAA
              01H       →          BBB
              02H       →          CCC
              03H       →          DDD
              04H       →          EEE
              05H       →          FFF
              06H       →          GGG
              07H       →          HHH
            08H-0FH     →          ZZZ
```

```
          ;*
          ;** Jump table
Address   ;*
0010H     BR      AAA
0011H     BR      BBB
0012H     BR      CCC
0013H     BR      DDD
0014H     BR      EEE
0015H     BR      FFF
0016H     BR      GGG
0017H     BR      HHH
0018H     BR      ZZZ
              :
              :
```

```
MOV   RPH, #00H   ;  General-purpose register bank 0
MOV   RPL, #02H   ;  General-purpose register row address 1
MOV   AR3, #00H   ;  AR3 ← 00H AR is set to 001 x H.
MOV   AR2, #00H   ;  AR2 ← 00H
MOV   AR1, #01H   ;  AR1 ← 01H
ST    AR0, 10H    ;  AR0 ← 0.10H
SKF   AR0, #1000B;  If the content of AR0 is greater than
AND   AR0, #1000B;  08H, the content of AR0 is changed to
BR    @AR         ;  08H.
```

(4) **Note**

The number of bits of address registers (AR3, AR2, AR1, AR0) allowed for use varies with the device types. When using the address register, reference should be made to the manual of the appropriate device.

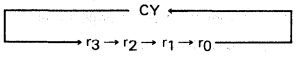
3.37 RORC r

Rotate right general register with carry flag

(1) Instruction code

00111	000	0111	r

(2) Function



The content of the general-purpose register indicated by R is shifted to the right by one bit, with carry flag included.

(3) **Example 1**

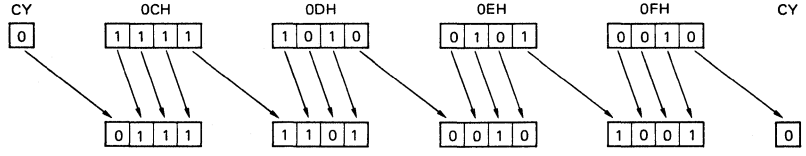
When row address 0 (0.00H to 0.0FH) of bank 0 is specified as general-purpose register (RPH = 0, RPL = 0), the value of address 0.00H (1000B) is shifted to the right by one bit, and the value becomes 0100B.

0.00H ← (0.00H) ÷ 2

```
MOV   RPH, #00H   ;  General-purpose register bank 0
MOV   RPL, #00H   ;  General-purpose register row address 0
CLR1  CY          ;  Carry flag ← 0
RORC  00H
```

Example 2

When row address 0 (0.00H to 0.0FH) of bank 0 is specified as general-purpose register (RPH = 0, RPL = 0), the value 0FA52H of data buffer (DBF) is shifted to the right by one bit, and the content of DBF is changed to 7D29H.




```
MOV   RPH, #00H   ;  General-purpose register bank 0
MOV   RPL, #00H   ;  General-purpose register row address 0
CLR1  CY          ;  Carry flag ← 0
RORC  0CH
RORC  0DH
RORC  0EH
RORC  0FH
```

3.38 CALL addr

Call subroutine

(1) Instruction code

11100	addr

(2) Function

$SP \leftarrow SP - 1$,

$STACK \leftarrow PC + 1$,

$PC_{0\text{-}10} \leftarrow addr$,

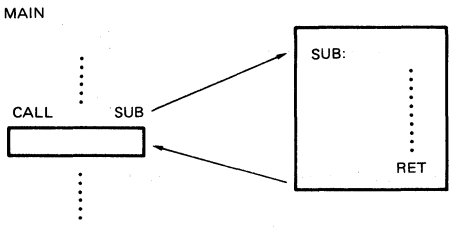
$PC_{11\text{-}15} \leftarrow 0$

The value of the program counter (PC) is incremented, and then it is stored into the stack. After this, execution branches to the subroutine indicated by addr.

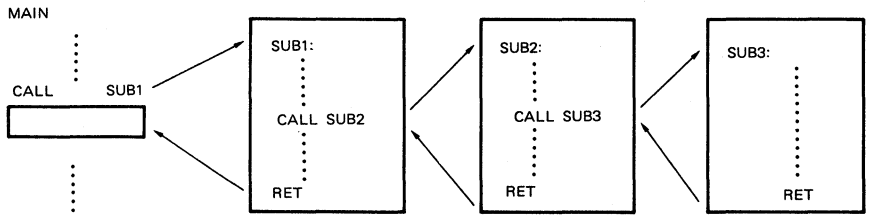
This instruction can be used to call subroutines contained within 2K steps from address 0000H to address 07FFH. It is therefore advisable to allocate frequently using subroutines in the range from address 0000H to 07FFH.

To call a subroutine allocated after address 0800H, use the 'CALL @AR' instruction to be mentioned in the next section.

(3) **Example 1**



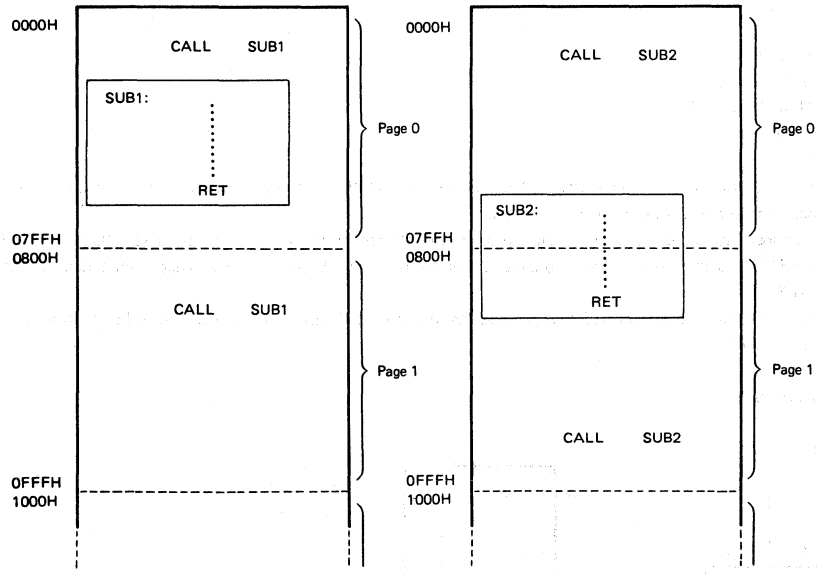
Example 2



(4) **Note**

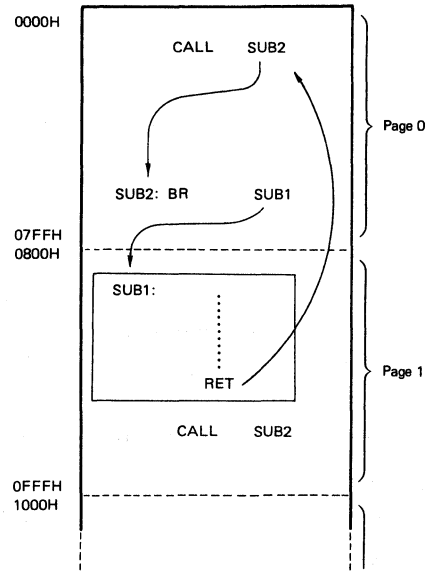
When using a 'CALL' instruction, the calling address, or the initial address of the subroutine to be called must be placed within page 0 (0000H to 07FFH). When calling a subroutine whose initial address is not positioned in page 0, use 'CALL @AR' instruction.

When initial address of subroutine is put in page 0



If the initial address of the subroutine is placed within page 0, the end address of the subroutine ('RET' or 'RETSK' instruction) may be placed outside of page 0.

The 'CALL' instruction can be used without considering page as far as the initial address of the subroutine to be called is placed within page 0. However, the following technique is useful when it is impracticable to place the initial address of a subroutine within page 0.



In this method, 'BR' instruction is set within page 0, and the actual subroutine is called by using this 'BR' instruction.

3.39 CALL @AR

Call subroutine specified by address register

(1) Instruction code

00111	000	0101	0000

(2) Function

SP ← SP – 1,
STACK ← PC + 1,
PC ← AR

The value of program counter (PC) is incremented, and stored into the stack, then execution branches to the subroutine indicated by address register (AR).

(3) **Example 1**

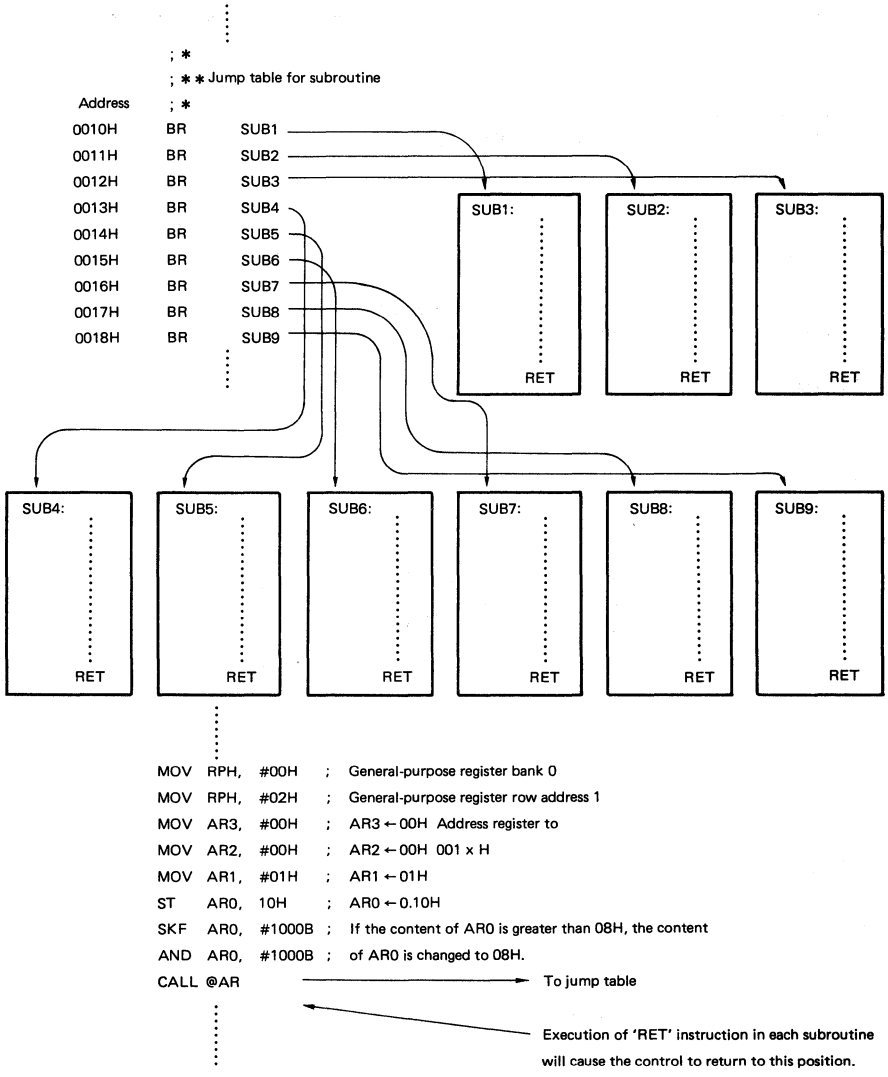
Value 0020H is set in the address register AR (AR0-AR3), and the subroutine of address 0020H is called by the 'CALL @AR' instruction.

```
MOV  AR3, #00H  ;  AR3 ← 00H
MOV  AR2, #00H  ;  AR2 ← 00H
MOV  AR1, #02H  ;  AR1 ← 02H
MOV  AR0, #00H  ;  AR0 ← 00H
CALL @AR        ;  Subroutine at address 0020H is called.
```

Example 2

The following subroutines are called depending on the contents of address 0.10H of the data memory.

Content of 0.10H		Subroutine name
00H	→	SUB1
01H	→	SUB2
02H	→	SUB3
03H	→	SUB4
04H	→	SUB5
05H	→	SUB6
06H	→	SUB7
07H	→	SUB8
08H-0FH	→	SUB9



(4) **Note**

The number of bits of address registers (AR3, AR2, AR1, AR0) allowed for use varies with the device types. When using the address register, reference should be made to the manual of the appropriate device.

3.40 RET

Return to the main program from subroutine

(1) Instruction code

00111	000	1110	0000

(2) Function

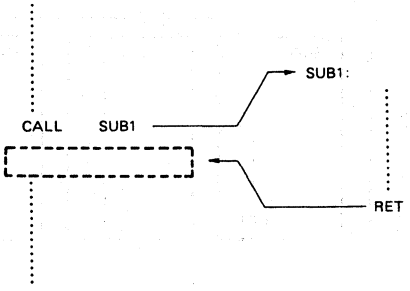
PC ← STACK,

SP ← SP + 1

This instruction is used to return to the main program from a subroutine.

The return address saved into the stack by CALL instruction is restored to the program counter.

(3) **Example**



3.41 RETSK

Return to the main program then skip next instruction

(1) Instruction code

00111	001	1110	0000

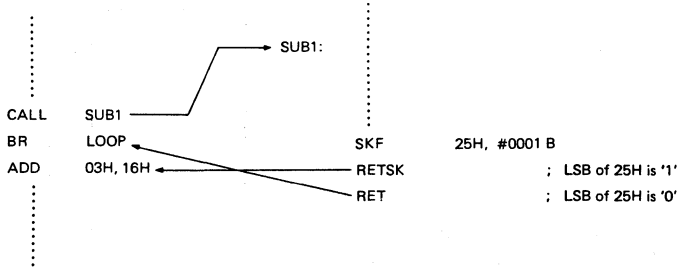
(2) Function

PC ← STACK,
SP ← SP + 1,
PC ← PC + 1

This instruction is used to return to the main program from a subroutine. The instruction following the 'CALL' instruction is skipped. That is, the return address saved to the stack by 'CALL' instruction is restored in the program counter (PC), then the program counter is incremented.

(3) **Example**

If the content of LSB (least significant bit) of address 25H of the data memory (RAM) is '0', the 'RET' instruction is executed, then control returns to the instruction next to the 'CALL' instruction. If the content is '1', 'RETSK' instruction is executed, and control returns to the instruction (in this example, ADD 03H, 16H) that follows the 'CALL' instruction.



3.42 RETI

Return to the main program from interrupt service routine

(1) Instruction code

00111	100	1110	0000

(2) Function

PC ← STACK,

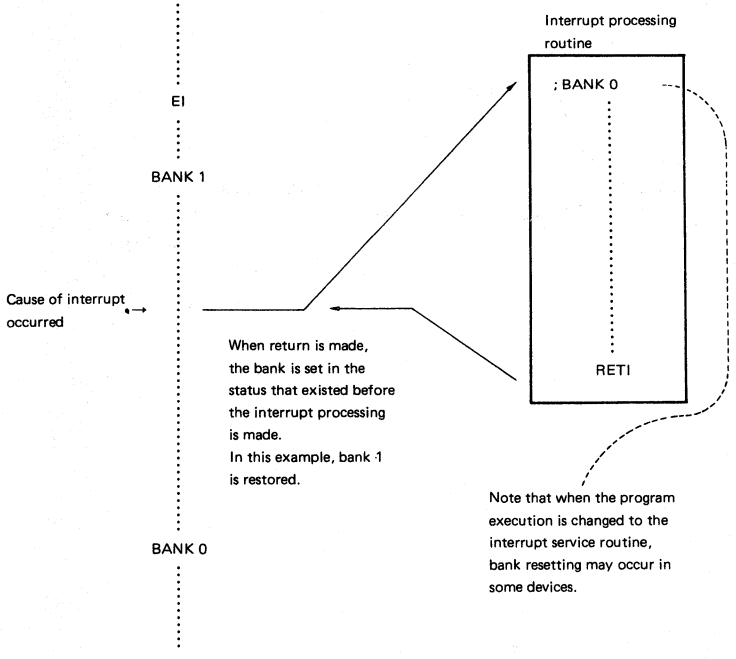
SP ← SP + 1

This instruction is used to return to the main program from an interrupt processing program. The return address which was saved into the stack by vector interrupt is restored in the program counter.

In some devices, a part of the system register is also returned to the status that existed before occurrence of vector interrupt.

(3) **Example**

A vector interrupt occurred when the data memory is placed in bank 1. Saving of data memory bank is needed since the data memory bank 0 is required for interrupt processing.



(4) **Notes**

1. The content of system register saved automatically by interrupt (this content can be restored by 'RETI' instruction) varies from device to device. Reference should be made to the manual of the device to be used.

2. If 'RETI' instruction is used in place of the 'RET' instruction in an ordinary subroutine, the bank and other data (saved by the interrupt) are restored when program execution returns to the return address. This may result in undefined status after returning. To avoid this, be sure to use the 'RET' (or 'RETSK') instruction when returning from a subroutine.

3.43 EI

Enable interrupt

(1) Instruction code

00111	000	1111	0000

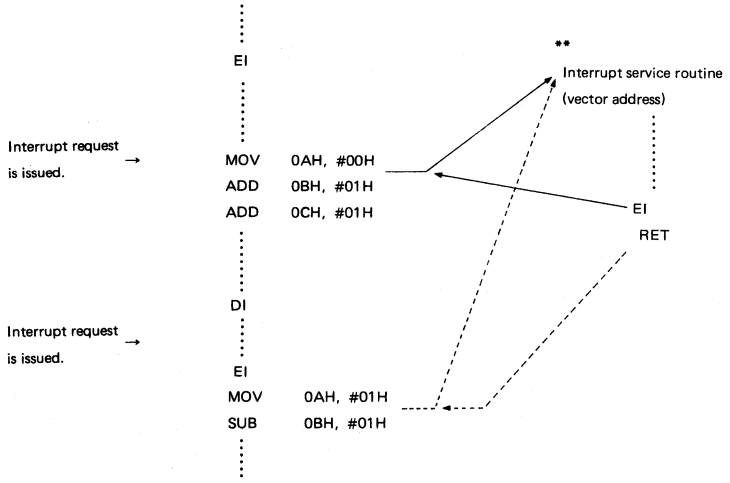
(2) Function

This instruction enables vector interrupt.

Vector interrupt is enabled after executing the instruction that follows the 'EI' instruction.

(3) **Example 1**

As shown in the following example, the interrupt request is actually accepted and program execution changes to the vector address after completing execution of the instruction (except program counter operating instruction) that follows this EI instruction.*

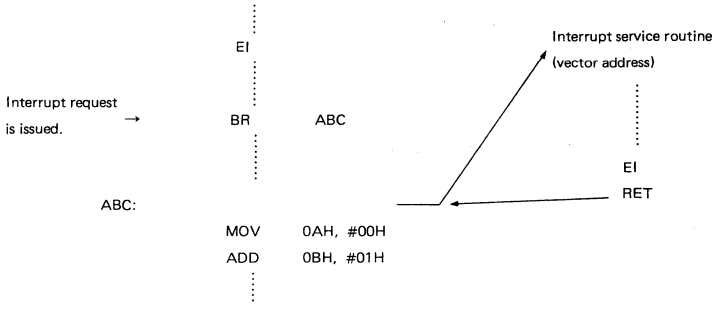


*: The vector address varies with the interrupt accepted. For details, refer to the manual of the device to be used.

**: Assume that the interrupt to be accepted here (Interrupt request is issued after execution of EI instruction and the flow of program execution changes to the interrupt service routine) is provided with the interrupt permission flag (IP) for that interrupt. No change will occur in the flow of program execution (that is, interrupt will not be accepted) if an interrupt request is issued after execution of the EI instruction, provided no interrupt permission flag is set for such interrupt. However, this causes the interrupt request flag (IREQ) to be set, hence the interrupt request will be accepted at the time when the interrupt permission flag is set. (For details, refer to the device manual.)

Example 2

Shown below is an example of interrupt caused by the interrupt request which is accepted during execution of an instruction for operating program counter (PC).



3.44 DI

Disable interrupt

(1) Instruction code

00111	001	1111	0000

(2) Function

This instruction is used to disable vector interrupt.

(3) **Example**

See Example 1 of Section 3.43.

3.45 STOP s

Stop CPU and release by condition s

(1) Instruction code

00111	010	1111	s

(2) Function

This instruction stops main clock, and turns the device to STOP mode.

The current consumption can be minimized by setting a device in the STOP mode.

The operand (s) specifies the condition by which the STOP mode is released and main clock oscillation re-started.

3.46 HALT h

Halt CPU and release by condition h

(1) Instruction code

00111	011	1111	h

(2) Function

This instruction turns the device into HALT mode.

The current consumption can be reduced by setting the device in HALT mode.

The operand (h) specifies the condition by which the HALT mode is released and main clock oscillation started.

3.47 NOP

No operation

(1) Instruction code

00111	100	1111	0000

(2) Function

This instruction causes one machine cycle to be consumed by executing nothing.

Development Tools

Section 4 - Development tools

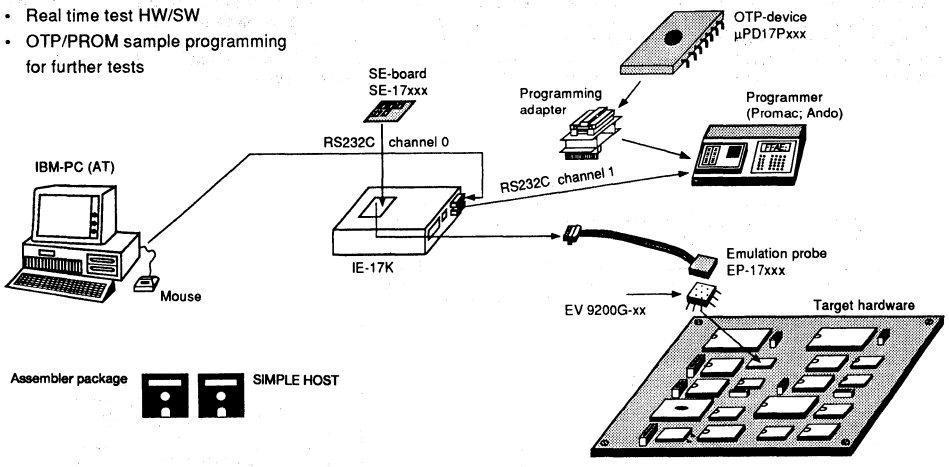
1. Development tools for the μPD17K-Family

This section gives a brief explanation of the development environment of the μPD17K-Family.

Hardware Tools: - IE-17K
- SE-17xxx
- EP-17xxx
- EV-9200G-xx

Software Tools:
- Absolute assembler (μS7B11AS17K)
- Device files (μSB10AS170xx)
  (μSB10AS171xx)
  (μSB10AS172xx)
- Simplehost, source-level debugger (μS7B10IE17K)

- SW development
- HW/SW debugging
- Real time test HW/SW
- OTP/PROM sample programming for further tests



Development Environment

IE-17K

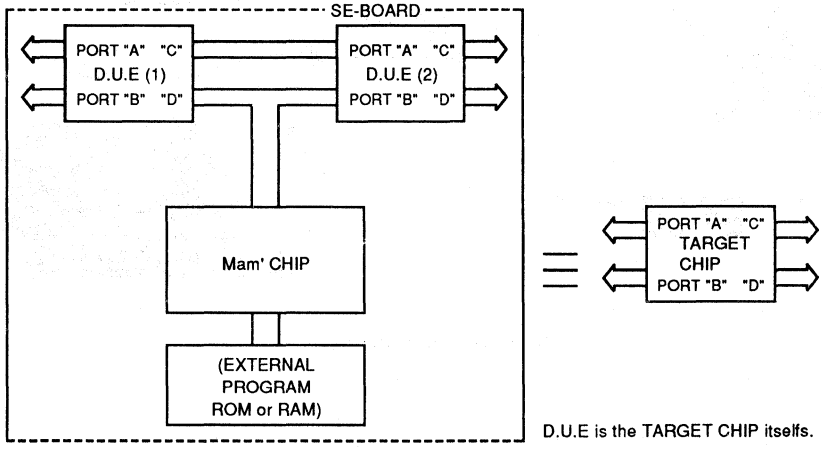
The IE-17K is a software development support tool applicable to every model of the μPD17K-Family. It consists of two boards:
a memory board and a supervisor board.

Features:

- Real-time emulation and one step emulation are available.
- Programmable break/trace function by which various break/trace conditions can be set hierarchically.
- Real-time trace function with a large-capacity trace memory (32K steps)
- Data memory coverage function which displays the state of writing in the data memory.
- Program memory coverage function which increments a counter every time an instruction which references to an address location is executed. The maximum count is 255.
- Incorporated programmable pattern generator (PPG) with 14 channels.

SE-17xxx

The SE-17xxx is the device-specific emulator board which completes the in-circuit-emulator. To ensure that the system evaluation (SE) board exhibits the same electrical behaviour as the original IC, a method known as „MAM chip" (implemented as an ASIC) device is applied. Two μPD17000 devices and a MAM chip are mounted on the SE board as shown in the diagram. Half the I/O-lines of each 17000 device are passed outside the board, so that they can be used to evaluate the I/O-lines of the real chip. Together with the MAM chip the other device form a bus system. All data sent out from the SE board or received by the SE board from outside are routed through the two μPD17000 devices. Therefore an observer outside the SE board gets the impression that a real chip is being used. The external memory which is connected to the MAM chip stores the developed software in the case the SE board is used as a stand alone system.



Emulation Chip Set Configuration

EP-17xxx

To connect the SE board with the printed circuit board a special cable is required. This device-specific emulation probe is called EP-17xxx.

EV-9200G-xx

The EV-9200G-xx is a special adapter socket to connect the emulation probe EP-17xxx with the target hardware in the case that the target device is mounted in a QFP package. This conversion socket is soldered onto the PCB.

μS7B11AS17K, μS7B10AS170xx
μS7B11AS17K, μS7B10AS171xx
μS7B11AS17K, μS7B10AS172xx

These are absolute macro assembler packages used for all devices of the 170xx, 171xx and the 172xx device group. They all comprise two parts. One part is the main unit used for all devices of the corresponding device group, the other is a device file for the particular μPD17000 device. The device file includes device-specific information, like ROM and RAM size, reserved words and addresses of the on-chip hardware functions. The assembler has a unique feature which supports software assembly of the code configured in modules. The assembler handles up to 99 modules. This feature, however, belongs to a relocatable assembler. The assembler is not able to assemble each module separately. Nevertheless, after the software is assembled for the first time, the assembler can be directed to assemble only those parts of the user program which were changed. Therefore the software development is speeded up.
The assembler also performs linkage operations to produce an executable code. In addition, this assembler supports powerful macro functions to end up in a versatile development tool for execution in a MS-DOS environment.

SIMPLEHOST (μS7B10IE17K)

SIMPLEHOST is a full-screen debugger which improves the interface between the in-circuit-emulator and the operator. SIMPLEHOST runs under Microsoft Windows, which means that all emulator commands can be selected and activated with a mouse. The contents of the ROM and RAM size of the emulator are shown on the screen together with the source program.

Development Tools for 17K Family of Microcontrollers To Develop and Debug Code

Device	Full Emulator	Mini Emulator	Evaluation Board	Assembler	Device File	Debugger (Simplehost)
μPD17001	IE-17K	IE-17K-ET	SE-17001	μS7B11AS17K	μS7B10AS17001	μS7B10IE17K
μPD17002	IE-17K	IE-17K-ET	SE-17002	μS7B11AS17K	μS7B10AS17002	μS7B10IE17K
μPD17003A	IE-17K	IE-17K-ET	SE-17003	μS7B11AS17K	μS7B10AS17003	μS7B10IE17K
μPD17005	IE-17K	IE-17K-ET	SE-17003	μS7B11AS17K	μS7B10AS17005	μS7B10IE17K
μPD17006	IE-17K	IE-17K-ET	SE-17001	μS7B11AS17K	μS7B10AS17006	μS7B10IE17K
μPD17008	IE-17K	IE-17K-ET	SE-17008	μS7B11AS17K	μS7B10AS17008	μS7B10IE17K
μPD17010	IE-17K	IE-17K-ET	SE-17003	μS7B11AS17K	μS7B10AS17010	μS7B10IE17K
μPD17051	IE-17K	IE-17K-ET	SE-17051	μS7B11AS17K	μS7B10AS17051	μS7B10IE17K
μPD17052	IE-17K	IE-17K-ET	SE-17052	μS7B11AS17K	μS7B10AS17052	μS7B10IE17K
μPD17053	IE-17K	IE-17K-ET	SE-17053	μS7B11AS17K	μS7B10AS17053	μS7B10IE17K
μPD17102	IE-17K	IE-17K-ET	SE-17102	μS7B11AS17K	μS7B10AS17102	μS7B10IE17K
μPD17103	IE-17K	IE-17K-ET	SE-17103	μS7B11AS17K	μS7B10AS17103	μS7B10IE17K
μPD17103L	IE-17K	IE-17K-ET	SE-17103	μS7B11AS17K	μS7B10AS17103	μS7B10IE17K
μPD17104	IE-17K	IE-17K-ET	SE-17104	μS7B11AS17K	μS7B10AS17104	μS7B10IE17K
μPD17104L	IE-17K	IE-17K-ET	SE-17104	μS7B11AS17K	μS7B10AS17104	μS7B10IE17K
μPD17106	IE-17K	IE-17K-ET	SE-17106	μS7B11AS17K	μS7B10AS17106	μS7B10IE17K
μPD17107	IE-17K	IE-17K-ET	SE-17107	μS7B11AS17K	μS7B10AS17107	μS7B10IE17K
μPD17107L	IE-17K	IE-17K-ET	SE-17107	μS7B11AS17K	μS7B10AS17107	μS7B10IE17K
μPD17108	IE-17K	IE-17K-ET	SE-17108	μS7B11AS17K	μS7B10AS17108	μS7B10IE17K
μPD17108L	IE-17K	IE-17K-ET	SE-17108	μS7B11AS17K	μS7B10AS17108	μS7B10IE17K
μPD17134A	IE-17K	IE-17K-ET	SE-17134	μS7B11AS17K	μS7B10AS17134	μS7B10IE17K
μPD17135A	IE-17K	IE-17K-ET	SE-17134	μS7B11AS17K	μS7B10AS17135	μS7B10IE17K
μPD17136A	IE-17K	IE-17K-ET	SE-17134	μS7B11AS17K	μS7B10AS17136	μS7B10IE17K
μPD17137A	IE-17K	IE-17K-ET	SE-17134	μS7B11AS17K	μS7B10AS17137	μS7B10IE17K
μPD17201A	IE-17K	IE-17K-ET	SE-17207	μS7B11AS17K	μS7B10AS17201	μS7B10IE17K
μPD17202A	IE-17K	IE-17K-ET	SE-17202	μS7B11AS17K	μS7B10AS17202	μS7B10IE17K
μPD17203A	IE-17K	IE-17K-ET	SE-17203	μS7B11AS17K	μS7B10AS17203	μS7B10IE17K
μPD17204	IE-17K	IE-17K-ET	SE-17204	μS7B11AS17K	μS7B10AS17204	μS7B10IE17K
μPD17207	IE-17K	IE-17K-ET	SE-17207	μS7B11AS17K	μS7B10AS17207	μS7B10IE17K

Development Tools for the 17K Family of Microcontrollers To Exercise Customer Hardware

Device	Probe	Receptacle	PROM Burner PROMAC P2A (Ando)	PROM Burner Adapter (Ando)
μPD17001	EP-17001GH	EV-9200G-48	AF-9704	AF-9796
μPD17002	EP-17002CU	EV-9200G-64	AF-9704	–
μPD17003A	EP-17003GF	EV-9200G-80	AF-9704	AF-9803
μPD17005	EP-17003GF	EV-9200G-80	AF-9704	AF-9803
μPD17006	EP-17201GF	EV-9200G-80	AF-9704	AF-9808E
μPD17008	EP-17008CW	–	AF-9704	AF-9803
μPD17010	EP-17003GF	EV-9200G-80	AF-9704	AF-9803
μPD17051	EP-17051CU	–	AF-9704	–
μPD17052	EP-17052CW	–	AF-9704	–
μPD17053	EP-17052CW	–	AF-9704	–
μPD17102	EP-17102G	–	AF-9704	–
μPD17103	EP-17103CX	–	AF-9704	AF-9799
μPD17103L	EP-17103CX	–	AF-9704	AF-9799
μPD17104	EP-17104CS	–	AF-9704	AF-9799
μPD17104L	EP-17104CS	–	AF-9704	AF-9799
μPD17106	EP-17106GC	EV-9200G-64	AF-9704	AF-9803
μPD17107	EP-17103CX	–	AF-9704	AF-9799
μPD17107L	EP-17103CX	–	AF-9704	AF-9799
μPD17108	EP-17104CS	–	AF-9704	AF-9799
μPD17108L	EP-17104CS	–	AF-9704	AF-9799
μPD17134A	EP-17134CT	–	AF-9704	AF-9808F
μPD17135A	EP-17134CT	–	AF-9704	AF-9808F
μPD17136A	EP-17134CT	–	AF-9704	AF-9808F
μPD17137A	EP-17134CT	–	AF-9704	AF-9808F
μPD17201A	EP-17201GF	EV-9200G-80	AF-9704	AF-9808A
μPD17202A	EP-17202GF	EV-9200G-64	AF-9704	AF-9808B
μPD17203A	EP-17203GC	EV-9200G-52	AF-9704	AF-9808B
μPD17204	EP-17203GC	EV-9200G-52	AF-9704	AF-9808B
μPD17207	EP-17201GF	EV-9200G-80	AF-9704	AF-9808A

Packaging Information

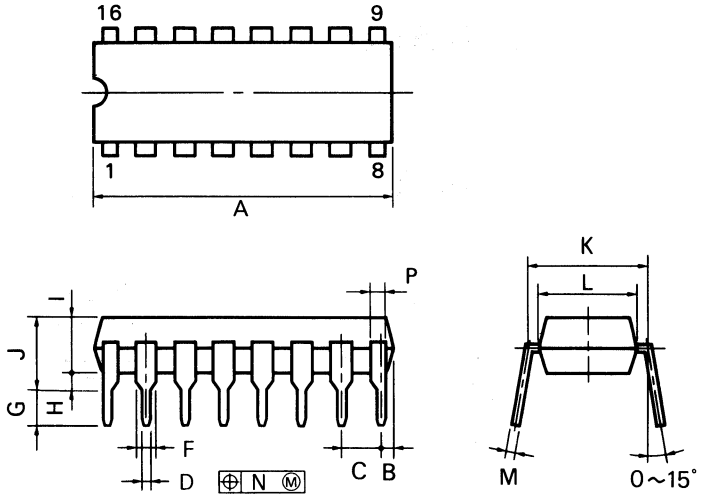
Package/device cross reference

Section 5 - Packaging Information

Package/device cross reference

16-Pin Plastic DIP (300 mil)

μPD17103CX
μPD17P103CX
μPD17107CX
μPD17P107CX



P16C-100-300B

NOTES

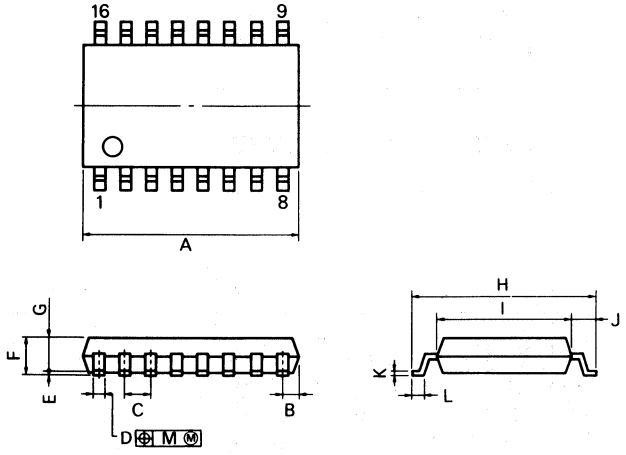
1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	20.32 MAX.	0.800 MAX.
B	1.27 MAX.	0.050 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	$0.50^{+0.10}$	$0.020^{+0.004}_{-0.005}$
F	1.1 MIN.	0.043 MIN.
G	$3.5^{+0.3}$	$0.138^{\pm0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.5	0.256
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.25	0.01
P	1.1 MIN.	0.043 MIN.

16-Pin Plastic SOP (300 mil)

μPD17103GS
μPD17P103GS
μPD17107GS
μPD17P107GS



P16GM-50-300B

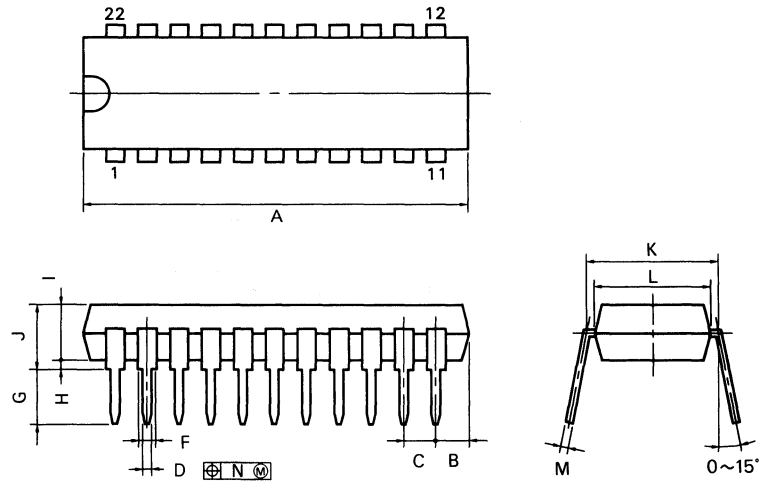
NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	10.46 MAX.	0.412 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.1 ± 0.1	0.004 ± 0.004
F	1.8 MAX.	0.071 MAX.
G	1.55	0.061
H	7.7 ± 0.3	0.303 ± 0.012
I	5.6	0.220
J	1.1	0.043
K	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$
L	0.6 ± 0.2	$0.024^{+0.008}_{-0.009}$
M	0.12	0.005

22-Pin Plastic DIP (300 mil)

μPD17104CS
μPD17P104CS
μPD17108CS
μPD17P108CS



S22C-70-300B

NOTES

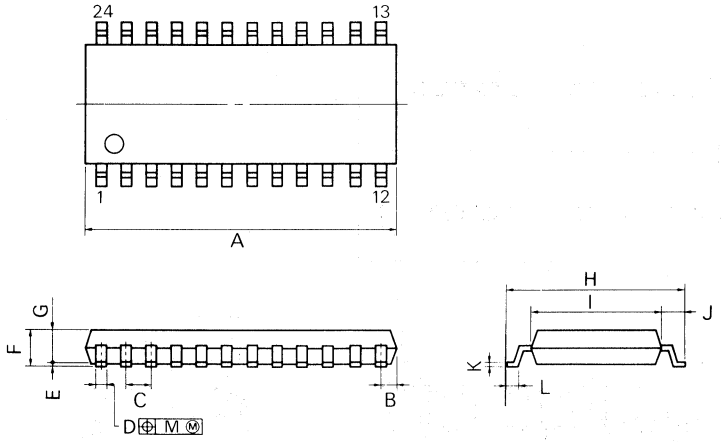
1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	23.12 MAX.	0.911 MAX.
B	2.67 MAX.	0.106 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	$0.50^{+0.10}$	$0.020^{+0.004}_{-0.005}$
F	0.85 MIN.	0.033 MIN.
G	$3.2^{+0.3}$	$0.126^{+0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.5	0.256
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007

24-Pin Plastic SOP (300 mil)

μPD17104GS
μPD17P104GS
μPD17108GS
μPD17P108GS



P24GM-50-300B-1

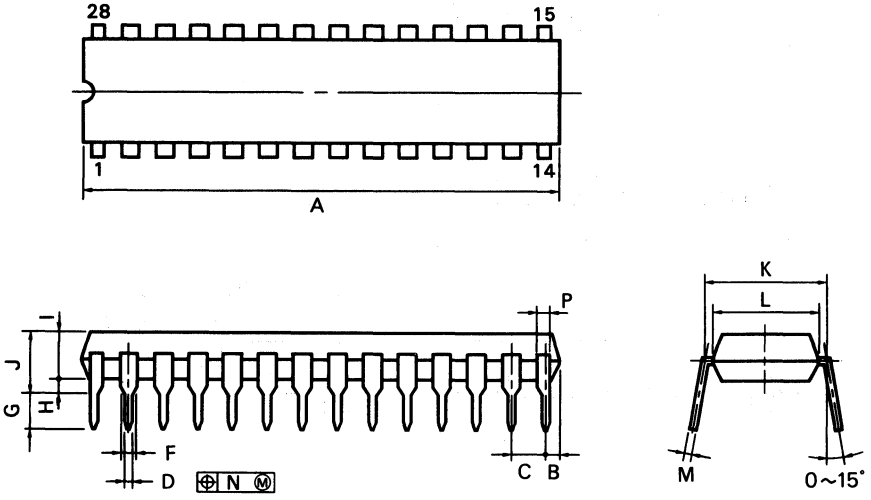
NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	15.54 MAX.	0.612 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.1 ± 0.1	0.004 ± 0.004
F	1.8 MAX.	0.071 MAX.
G	1.55	0.061
H	7.7 ± 0.3	0.303 ± 0.012
I	5.6	0.220
J	1.1	0.043
K	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$
L	0.6 ± 0.2	$0.024^{+0.008}_{-0.009}$
M	0.12	0.005

28-Pin Plastic Shrink DIP (400 mil)

μPD17134ACT
μPD17135ACT
μPD17136ACT
μPD17P136ACT
μPD17137ACT
μPD17P137ACT



P28C-100-400

NOTES

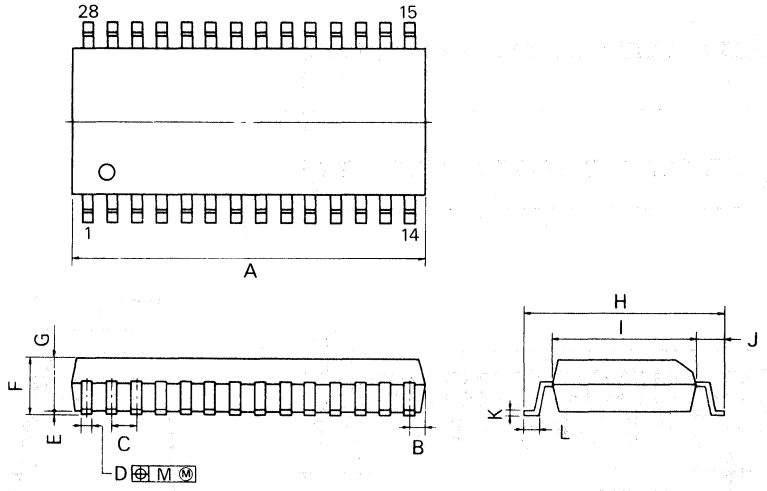
1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	35.56 MAX.	1.400 MAX.
B	1.27 MAX.	0.050 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	$0.50^{\pm 0.10}$	$0.020^{+0.004}_{-0.005}$
F	1.1 MIN.	0.043 MIN.
G	$3.5^{\pm 0.3}$	$0.138^{\pm 0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.72 MAX.	0.226 MAX.
K	10.16 (T.P.)	0.400 (T.P.)
L	8.6	0.339
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.25	0.01
P	0.9 MIN.	0.035 MIN.

28-Pin Plastic SOP (375 mil)

μPD17134AGT
μPD17135AGT
μPD17136AGT
μPD17P136AGT
μPD17137AGT
μPD17P137AGT



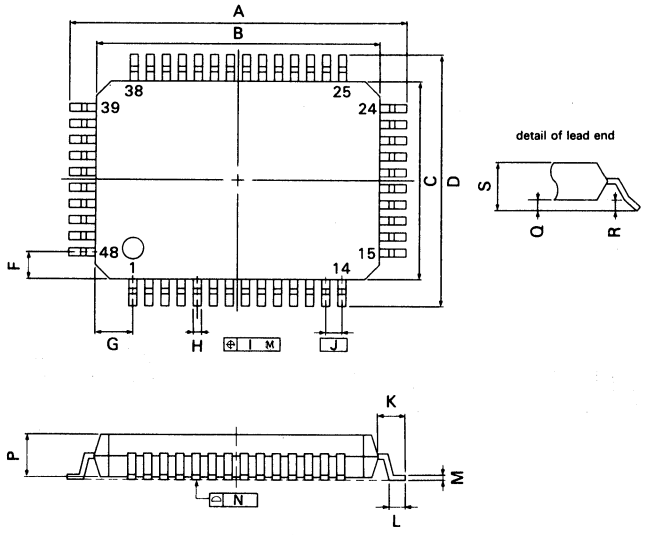
P28GM-50-375B

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	18.07 MAX.	0.712 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.1 ± 0.1	0.004 ± 0.004
F	2.9 MAX.	0.115 MAX.
G	2.50	0.098
H	10.3 ± 0.3	$0.406^{+0.012}_{-0.013}$
I	7.2	0.283
J	1.6	0.063
K	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.002}$
L	0.8 ± 0.2	$0.031^{+0.009}_{-0.008}$
M	0.12	0.005

48-Pin Plastic QFP (10x14)
μPD17001GH-xxx-2A5
μPD17P001GH-2A5

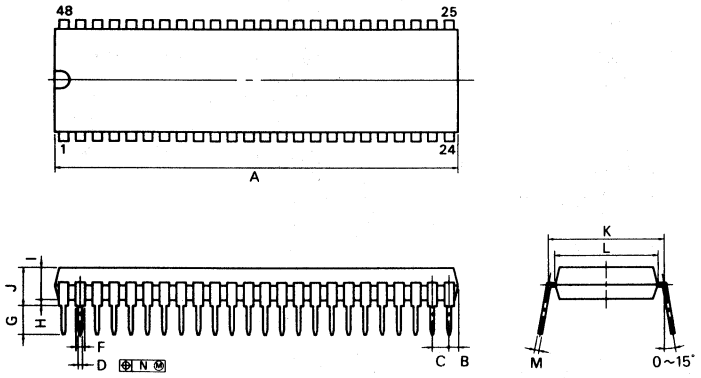


P48GH-80-2A5-1

NOTE
Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	$16.8^{\pm 0.4}$	$0.661^{+0.017}_{-0.016}$
B	$14.0^{\pm 0.2}$	$0.551^{\pm 0.008}$
C	$10.0^{\pm 0.2}$	$0.394^{\pm 0.008}$
D	$12.8^{\pm 0.4}$	$0.504^{\pm 0.016}$
F	1.4	0.055
G	1.8	0.071
H	$0.35^{\pm 0.10}$	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	$1.4^{\pm 0.2}$	$0.055^{\pm 0.008}$
L	$0.6^{\pm 0.2}$	$0.024^{\pm 0.008}$
M	$0.20^{+0.10}_{-0.05}$	$0.079^{+0.008}_{-0.003}$
N	0.15	0.006
P	$2.2^{\pm 0.1}$	$0.087^{+0.004}_{-0.005}$
Q	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
R	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
S	2.5 MAX.	0.099 MAX.

48-Pin Plastic Shrink DIP (600 mil)
μPD17002CU
μPD17051CU



P48C-70-600B

NOTES

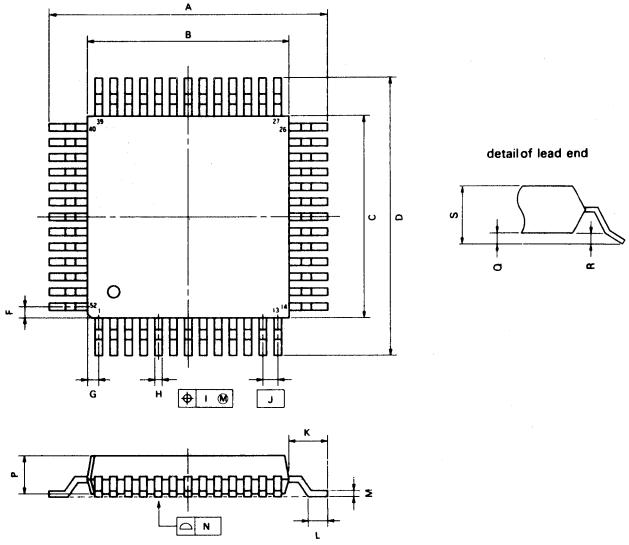
1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	44.46 MAX.	1.751 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	$0.50^{\pm 0.10}$	$0.020^{+0.004}_{-0.005}$
F	0.85 MIN.	0.033 MIN.
G	$3.2^{\pm 0.3}$	$0.126^{\pm 0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.72 MAX.	0.226 MAX.
K	15.24 (T.P.)	0.600 (T.P.)
L	13.2	0.520
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007

52-Pin Plastic QFP (14x14)

μPD17203AGC-xxx-3BH
μPD17P203AGC-001-3BH
μPD17P203AGC-002-3BH
μPD17P203AGC-003-3BH
μPD17204GC-xxx-3BH

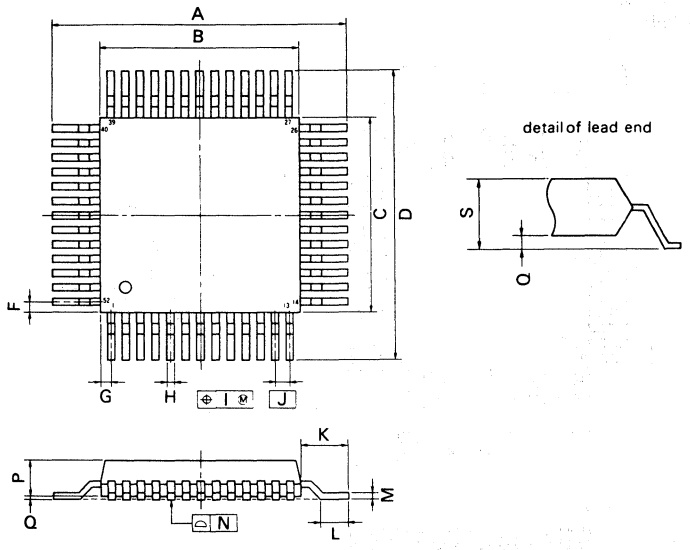


S52GC-100-3BH

NOTE
Each lead centerline is located within 0.20 mm (0.008 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	$17.2^{+0.4}$	$0.677^{\pm 0.016}$
B	$14.0^{+0.2}$	$0.551^{+0.009}_{-0.008}$
C	$14.0^{+0.2}$	$0.551^{+0.009}_{-0.008}$
D	$17.2^{+0.4}$	$0.677^{\pm 0.016}$
F	1.0	0.039
G	1.0	0.039
H	$0.40^{+0.10}$	$0.016^{+0.004}_{-0.005}$
I	0.20	0.008
J	1.0 (T.P.)	0.039 (T.P.)
K	$1.6^{+0.2}$	$0.063^{\pm 0.008}$
L	$0.8^{+0.2}$	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.15	0.006
P	2.7	0.106
Q	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
R	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
S	3.0 MAX.	0.119 MAX.

52-Pin Plastic QFP (14x14)
bent lead
μPD17102G-xxx-00

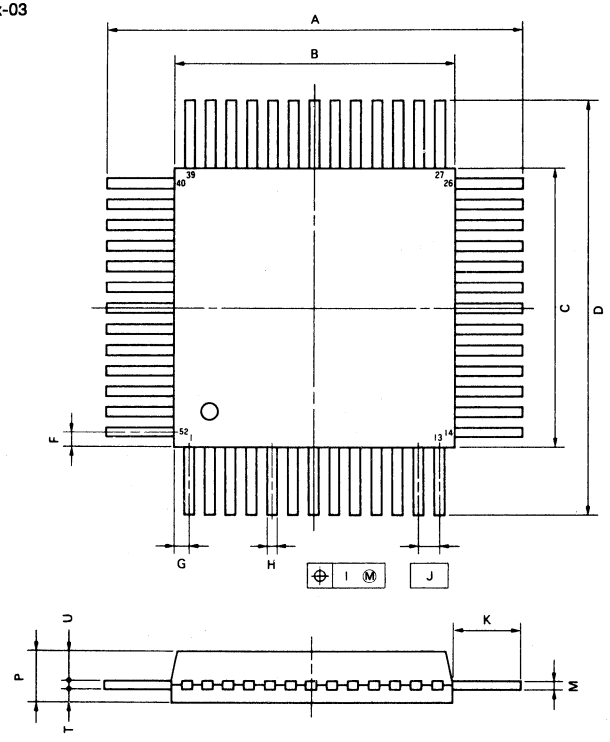


P52G-100-00-1

NOTE
Each lead centerline is located within 0.20 mm (0.008 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	$21.0^{\pm 0.4}$	$0.827^{\pm 0.016}$
B	$14.0^{\pm 0.2}$	$0.551^{+0.009}_{-0.008}$
C	$14.0^{\pm 0.2}$	$0.551^{+0.009}_{-0.008}$
D	$21.0^{\pm 0.4}$	$0.827^{\pm 0.016}$
F	1.0	0.039
G	1.0	0.039
H	$0.40^{+0.10}_{-0.}$	$0.016^{+0.004}_{-0.005}$
I	0.20	0.008
J	1.0 (T.P.)	0.039 (T.P.)
K	$3.5^{\pm 0.2}$	$0.138^{+0.008}_{-0.009}$
L	$2.2^{\pm 0.2}$	$0.087^{+0.008}_{-0.009}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.15	0.006
P	$2.6^{+0.2}_{-0.1}$	$0.102^{+0.008}_{-0.004}$
Q	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
S	3.0 MAX.	0.119 MAX.

52-Pin Plastic QFP (14x14)
straight lead
μPD17102G-xxx-03

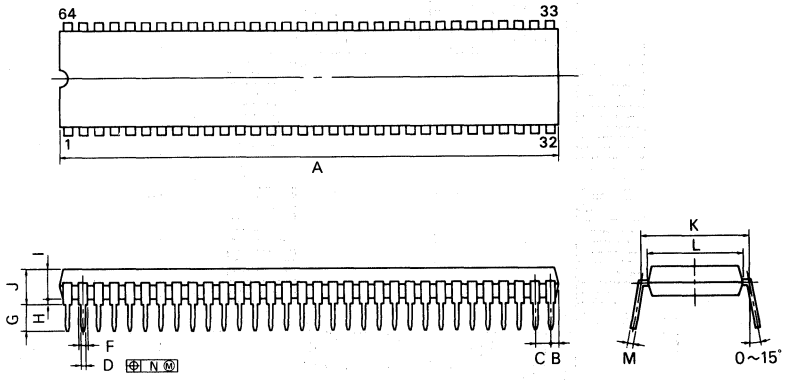


P52G-100-03-1

NOTE
Each lead centerline is located within 0.20 mm (0.008 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	$19.8^{\pm 0.4}$	$0.780^{+0.016}_{-0.017}$
B	$14.0^{\pm 0.2}$	$0.551^{+0.008}_{-0.009}$
C	$14.0^{\pm 0.2}$	$0.551^{+0.008}_{-0.009}$
D	$19.8^{\pm 0.4}$	$0.780^{+0.016}_{-0.017}$
F	1.0	0.039
G	1.0	0.039
H	$0.40^{\pm 0.10}$	$0.016^{+0.004}_{-0.005}$
I	0.20	0.008
J	1.0 (T.P.)	0.039 (T.P.)
K	$2.9^{\pm 0.2}$	$0.114^{+0.008}_{-0.009}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
P	$2.6^{+0.2}_{-0.1}$	$0.102^{+0.008}_{-0.009}$
T	1.0	0.039
U	1.45	0.057

64-Pin Plastic Shrink DIP (750 mil)
μPD17052CW
μPD17053CW



P64C-70-750A,C

NOTES

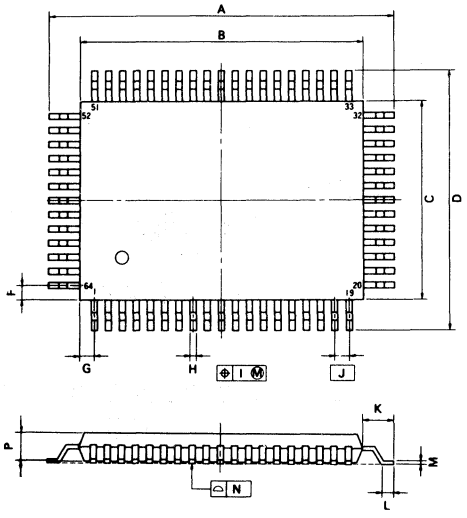
1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	58.68 MAX.	2.311 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	$0.50^{+0.10}$	$0.020^{+0.004}_{-0.005}$
F	0.9 MIN.	0.035 MIN.
G	$3.2^{+0.3}$	$0.126^{+0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	17.0	0.669
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007

64-Pin Plastic QFP (14x20)

μPD17106GC
μPD17P106GC
μPD17202AGF-xxx-3BE
μPD17P202AGF-3BE
μPD17301GF-xxx-3BE



P64GF-100-3B8,3BE-1

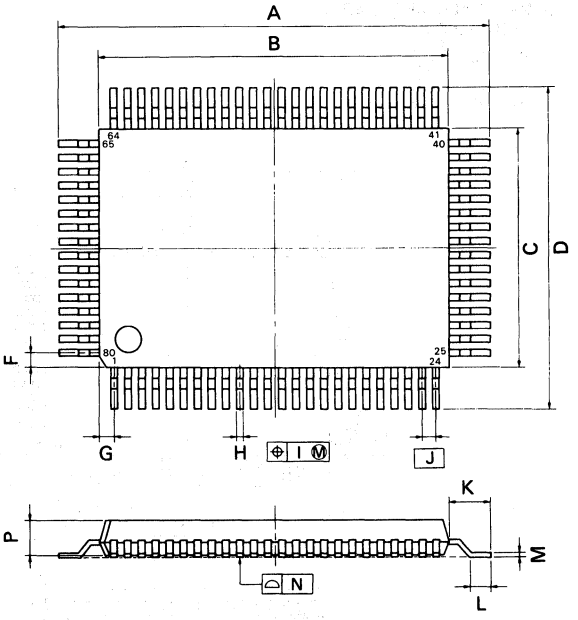
NOTE

Each lead centerline is located within 0.20 mm (0.008 inch) of its true position (T.P.) at maximum material condition.

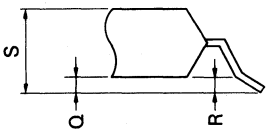
ITEM	MILLIMETERS	INCHES
A	$23.6^{\pm 0.4}$	$0.929^{\pm 0.016}$
B	$20.0^{\pm 0.2}$	$0.795^{+0.009}_{-0.008}$
C	$14.0^{\pm 0.2}$	$0.551^{+0.009}_{-0.008}$
D	$17.6^{\pm 0.4}$	$0.693^{\pm 0.016}$
F	1.0	0.039
G	1.0	0.039
H	$0.40^{\pm 0.10}$	$0.016^{+0.004}_{-0.005}$
I	0.20	0.008
J	1.0 (T.P.)	0.039 (T.P.)
K	$1.8^{\pm 0.2}$	$0.071^{+0.008}_{-0.009}$
L	$0.8^{\pm 0.2}$	$0.031^{+0.008}_{-0.009}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.15	0.006
P	2.7	0.106
Q	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
R	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
S	3.0 MAX.	0.119 MAX.

80-Pin Plastic QFP (14x20)

μPD17003AGF-xxx-3B9
μPD17005GF-xxx-3B9
μPD17P005GF-3B9
μPD17006GF-xxx-3B9
μPD17P006GF-3B9
μPD17010GF-xxx-3B9
μPD17P010GF-3B9
μPD17201AGF-xxx-3B9
μPD17207GF-xxx-3B9
μPD17P207GF-3B9



detail of lead end



S80GF-80-3B9

NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	$23.2^{+0.4}$	$0.913^{+0.017}_{-0.016}$
B	$20^{+0.2}$	$0.787^{+0.009}_{-0.008}$
C	$14^{+0.2}$	$0.551^{+0.009}_{-0.008}$
D	$17.2^{+0.4}$	$0.677^{\pm 0.016}$
F	1.0	0.039
G	0.8	0.031
H	$0.35^{+0.10}$	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	$1.6^{+0.2}$	$0.063^{\pm 0.008}$
L	$0.8^{+0.2}$	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.15	0.006
P	2.7	0.106
Q	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
R	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
S	3.0 MAX.	0.119 MAX.

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