Considerations for Interfacing the NEC765 to the CDC 9404 and 9406-2, -3 Flexible Disk Drives

Introduction

Although the NEC 765 performs most of the controller functions required by a Flexible Disk Drive Controller (FDC), external logic is required to have a complete interface with the Flexible Disk Drive (FDD).

Shown in Figures 1 and 2 is an FDC interface for 2 single-sided or double-sided 8 in. FDDs operating in single density or double density mode. External logic is required for the following functions: decoding unit select outputs, demultiplexing status and control lines, data recovery, determination of the amount of write precompensation, write clock generation, and interface drivers and receivers. The polling feature of the NEC 765 affects the first two areas and must be carefully considered when using the NEC 765. Write precompensation is an important part of the FDC and is fairly straightforward. The area of data recovery is more complex and will be discussed first.

Data Recovery

The NEC 765 requires two signals, RDD and RDW, to be generated from the READ DATA signal from the FDD. The NEC 765 requirements for these signals are shown in Figure 3 for 8 in. MFM operation. RDD is a signal which has a positive going pulse for every flux reversal whether it is a clock bit or a data bit. The RDW signal is derived from the incoming pulse train and is a clock signal which is used by the NEC 765 to determine if a flux reversal is a clock bit or a data bit.

In order to have reliable operation with 8 in. MFM and to meet the NEC 765 requirements, a phase-lock oscillator (PLO) data separator circuit is required to generate these signals. A block diagram (Figure 4) of the PLO circuit (Figure 2) to generate these signals shows the functions performed by the circuit.

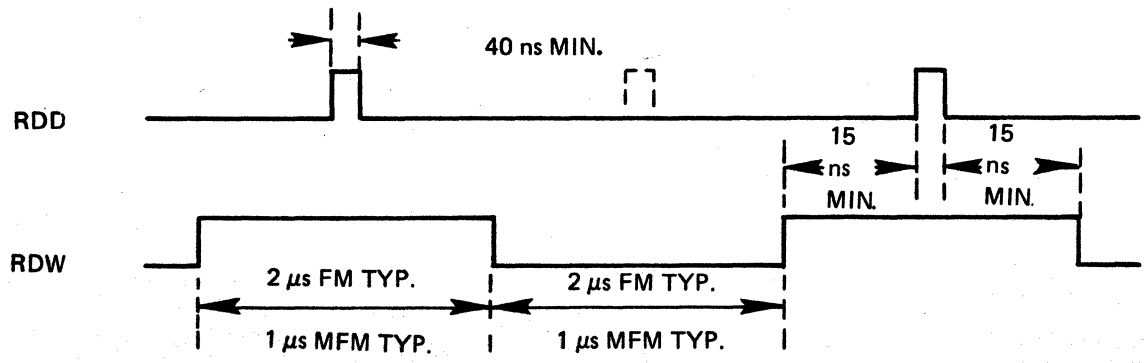
The PLO circuit operates basically the same for either MFM or FM operation, the only difference being that the data cell time for MFM is 2 μs (as opposed to 4 μs for FM), so the SHAPED DATA pulse is 500 ns wide for MFM and 1 μs wide for FM. For MFM the VCO output is divided by two and for FM it is divided by four.

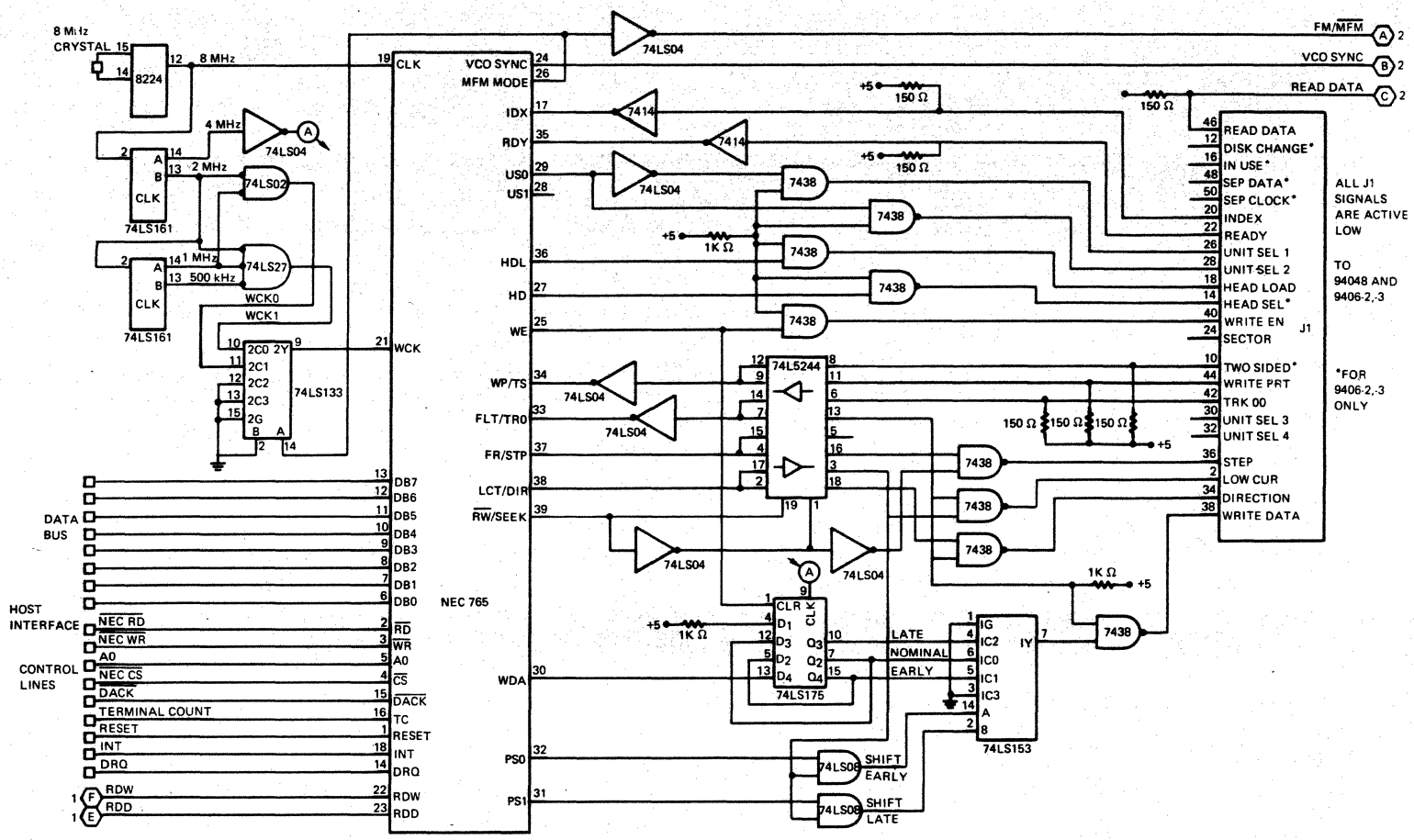
The incoming READ DATA signal is pulsewidth shaped by the one shot to match the feedback pulsewidth from the voltage controlled oscillator (VCO) in either MFM or FM mode. The VCO SYNC signal is used to disable the READ DATA input when a read is not taking place. This prevents the VCO from being driven off frequency by write splices.

The phase detector compares the phase of the SHAPED DATA to the phase of the counted down VCO. The MFM/FM input determines if the VCO is divided by two or by four (VFO CLK ÷ 2 OR 4).

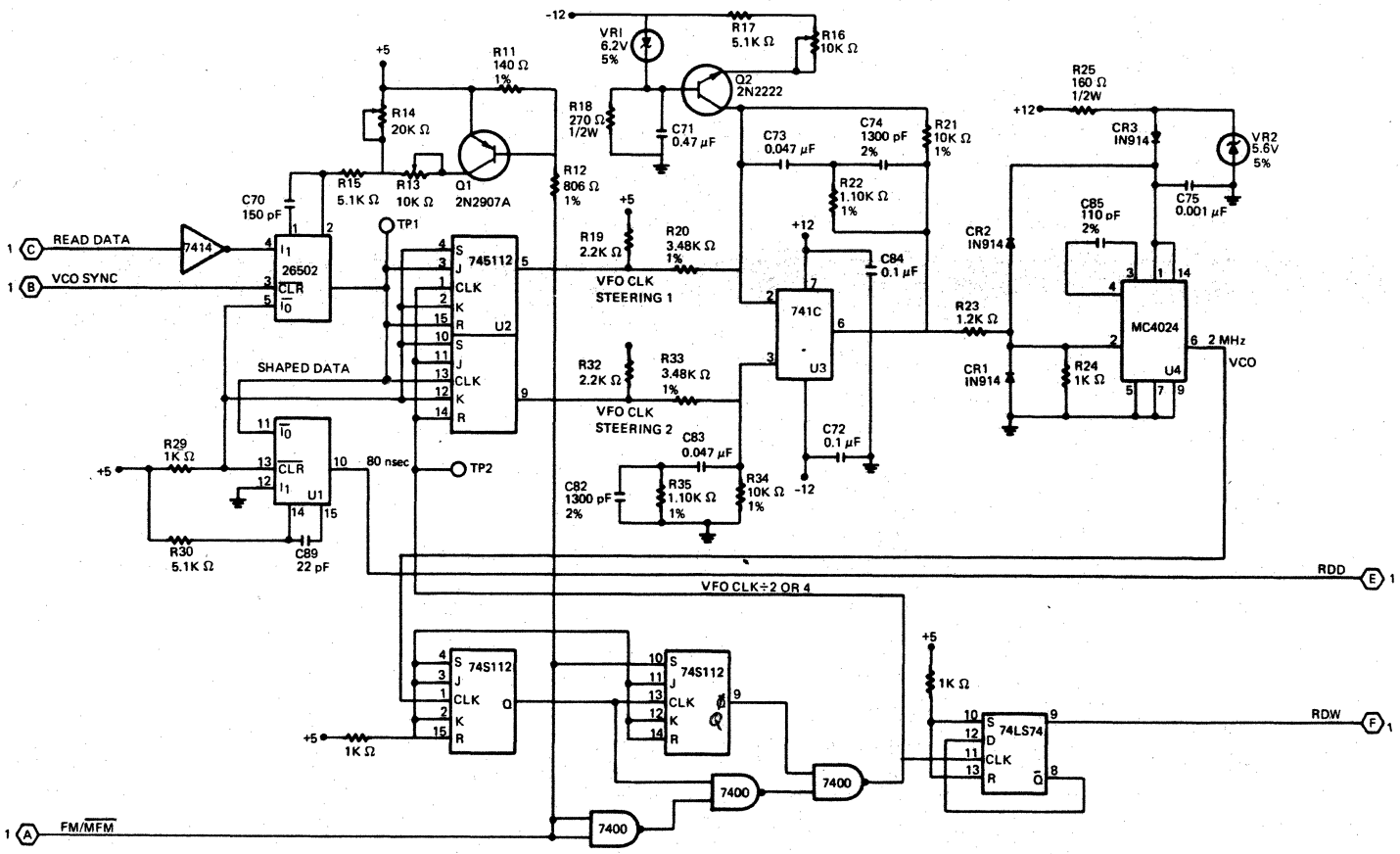
RDW is then generated by dividing VFO CLK ÷ 2 OR 4 by two. The SHAPED DATA pulses are retimed and reshaped to form the RDD signal which is sent to the NEC 765.

NEC 765 INPUT DATA TIMING Figure 3

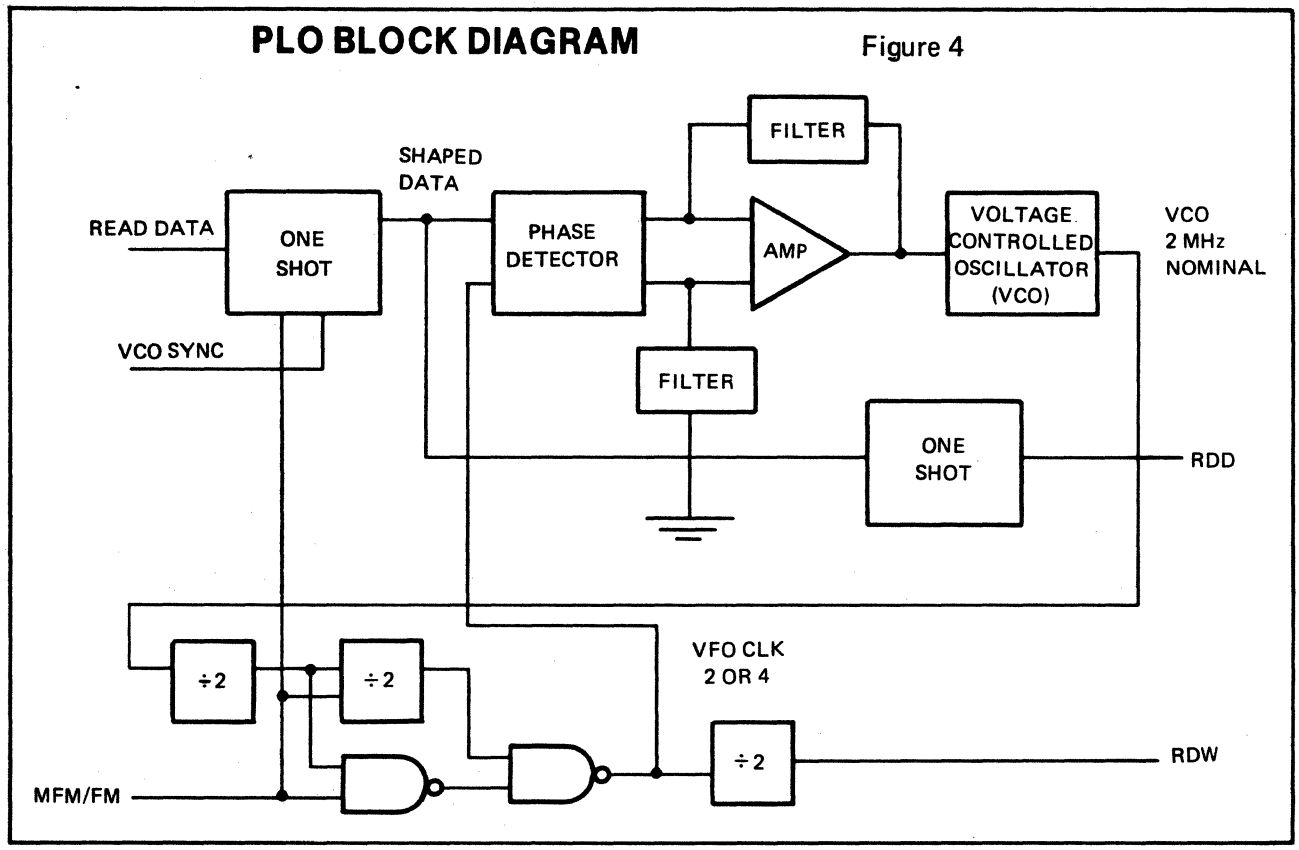




NEC 765 BASED FDC (sheet 1). Figure 1



NEC 765 BASED FDC (sheet 2) Figure 2



PLO Circuit Operation

Now that a general understanding of the PLO circuit operation has been obtained, a more detailed discussion is appropriate.

The phase detector (U2, Figure 2) compares the phase of the SHAPED DATA pulse to the phase of VFO CLK ÷ 2 OR 4. See Figure 5. If VFO CLK ÷ 2 (for MFM) is lagging the SHAPED DATA pulse, an output pulse on No. 9, U2 is generated. The filter/amplifier converts this pulse into a DC signal which increases the frequency of the VCO. Correspondingly if VFO CLK ÷ 2 is leading the SHAPED DATA pulse, an output pulse on No. 5, U2 is generated. This pulse is converted into a DC signal which decreases the frequency of the VCO. These two actions cause the VCO to track the frequency of the incoming READ DATA pulses. This correction process to keep the two signals in phase is constantly occurring because of spindle speed variation and circuit parameter variations.

The operating specifications for this circuit are as follows:

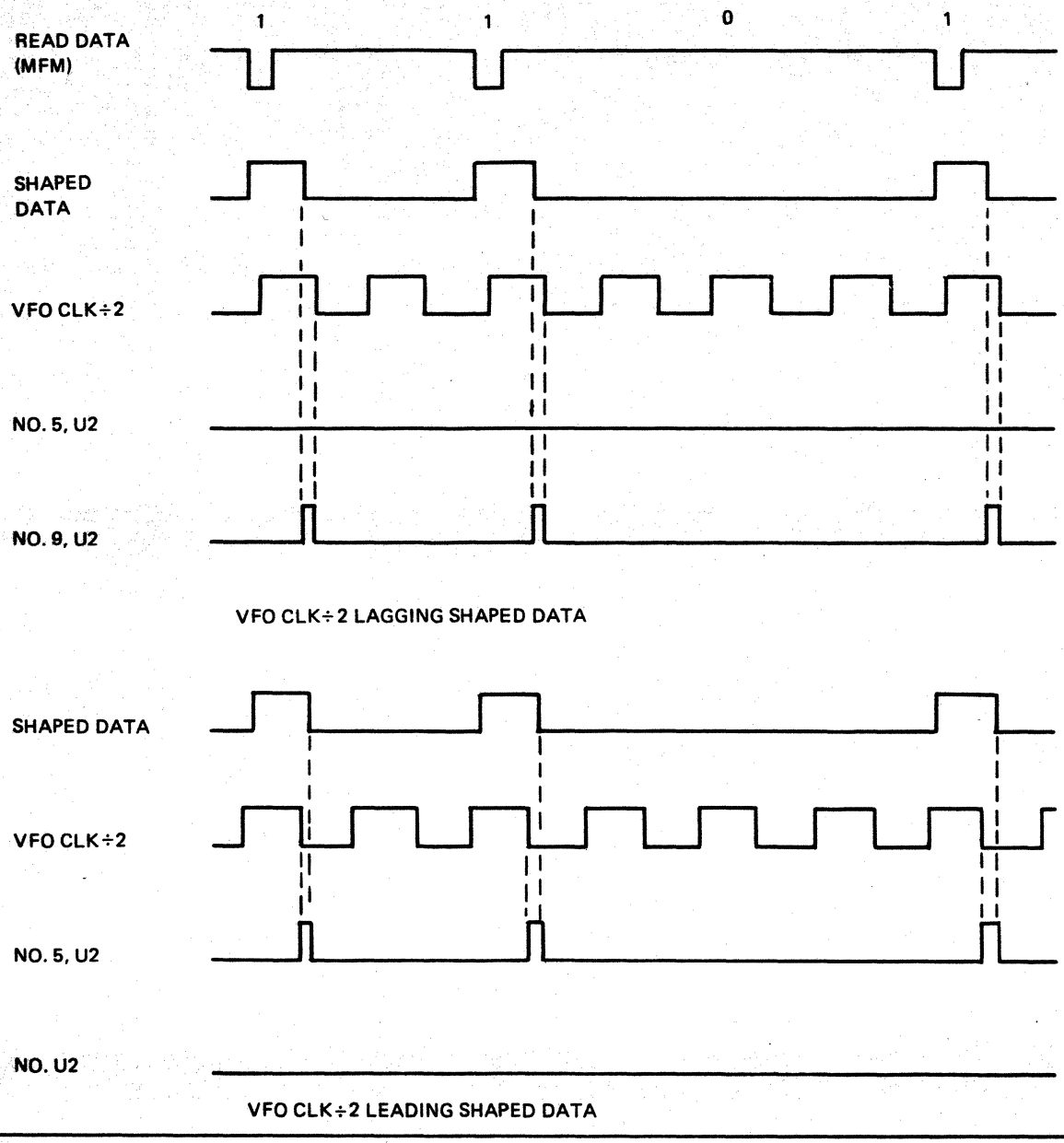
Free Running Frequency	2 MHz
Capture Range	±15 Percent
Lock Up Time	50 μs "1111" or "0000" Pattern 100 μs "1010" Pattern

The outputs of the circuit, RDD and RDW, have the relationships shown in Figure 6.

The RDD pulses are generated from the falling edge of the SHAPED DATA pulses. The pulses are also reshaped to be sent to the NEC 765. VFO CLK ÷ 2 OR 4 is divided by 2 once again to obtain a clock signal whose frequency is that required by the NEC 765 input.

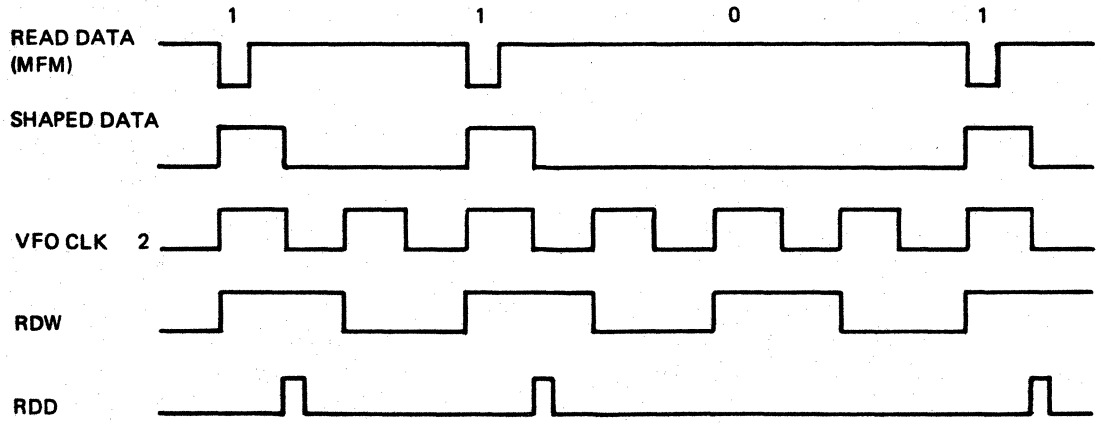
PLO CIRCUIT PHASE DETECTOR OPERATION

Figure 5



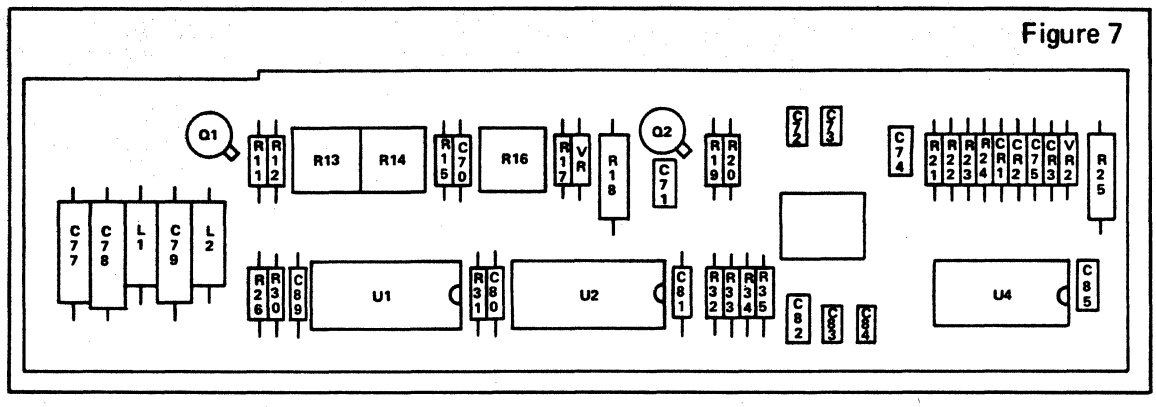
PLO CIRCUIT SIGNAL RELATIONSHIPS

Figure 6



7 RECOMMENDED PLO CIRCUIT LAYOUT AND GROUND PLANE 8

Figure 7



PLO Circuit Layout, Voltage Tolerances, Component Tolerances

The PLO circuit contains some analog circuitry that requires close attention to layout, voltage tolerances, and component tolerances. Figure 7 shows a recommended layout and ground plane for this portion of the PLO circuit. Also shown are the recommended supply voltage filter components which have the following values:

+5V	C77 – 33 μF	10V
-12V	C78 – 10 μF	15V
	L1 – 10 mH	
+12V	C79 – 10 μF	15V
	L2 – 10 mH	

The voltage tolerances on this circuit for all voltages is ±5 percent. Component tolerances are as follows unless noted otherwise.

Capacitors	±20 Percent
Resistors	±5 Percent 1/4W
Potentiometers	±20 Percent

PLO Circuit Test Points A and Adjustments

Adjustments to the phase-lock loop will be a rare necessity. However, should it be necessary alignment of the phase-lock loop is described below. Should data recovery errors become excessive, an investigation of the phase-lock loop operation as described below may help pinpoint the problem.

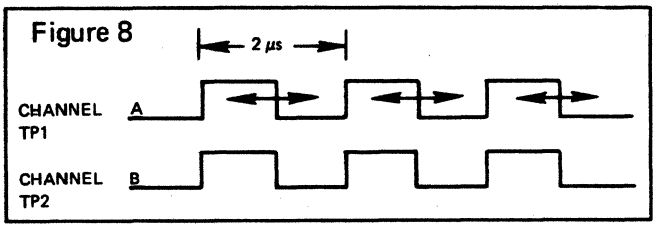
Procedure for Aligning the Phase-Lock Loop

Equipment needed: Oscilloscope, Diskette with all ones or use header area of preformatted all ones or all zeros.

1. Connect Channel A of the oscilloscope to TP1, output of composite read data and clock one-shot, and set the horizontal sensitivity to about 1 μs/div and the vertical sensitivity to about 5V/div. After loading the head and selecting FM make sure that data is displayed on Channel A. See Figure 8. Connect Channel B of the oscilloscope to TP2, output of VFO clock divide by 2 or 4. Sync oscilloscope on Channel A.

DATA TP1 AND VCO TP2 COMPARED

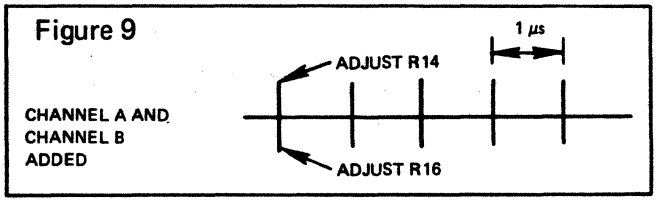
Figure 8



2. Adjust R14 for 1 μs pulses on Channel A. Adjust R16 for the waveform on Channel B to be as shown in Figure 8. With the oscilloscope controls invert Channel B and add the two channels. The oscilloscope display should be as in Figure 9.

PHASE DIFFERENCE BETWEEN FM DATA TP1 AND VCO TP2 10

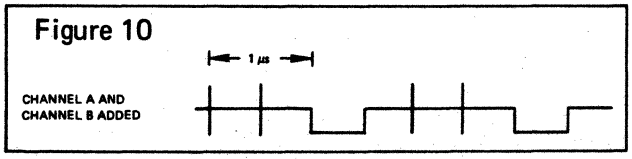
Figure 9

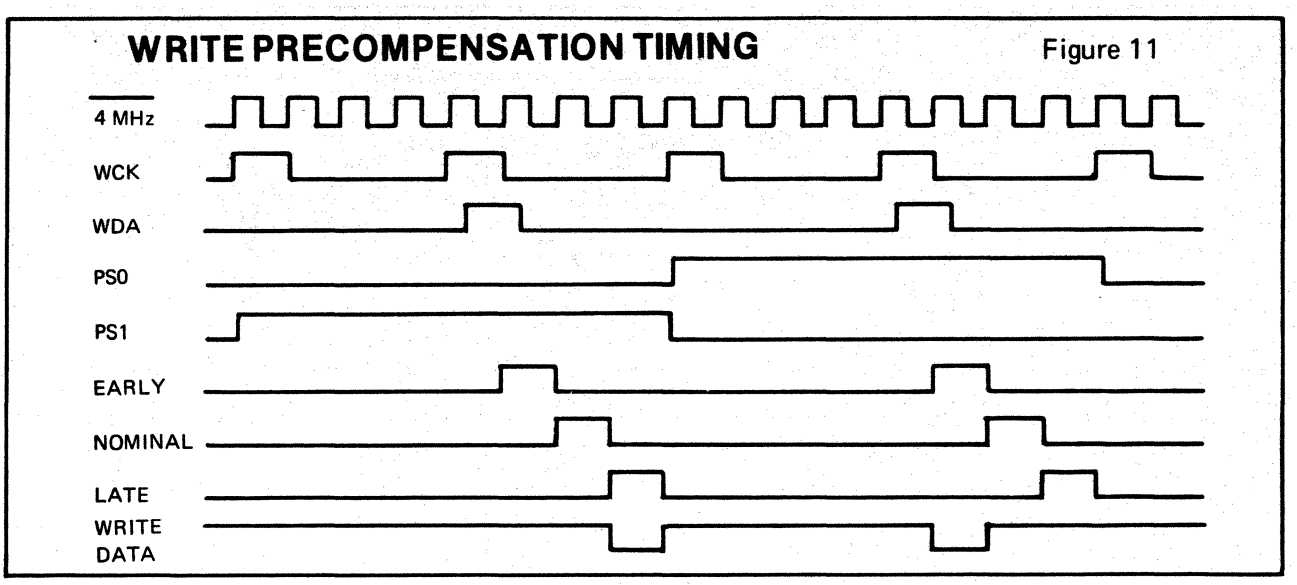


3. Minimize the width of the spikes of the added signal shown in Figure 9 by adjusting R14 and R16.
4. Select MFM operation and change the oscilloscope horizontal sensitivity to 0.5 μs per division.
5. Adjust R13 for the picture shown in Figure 10.

PHASE DIFFERENCE BETWEEN MFM DATA (TP1) AND VCO (TP2)

Figure 10





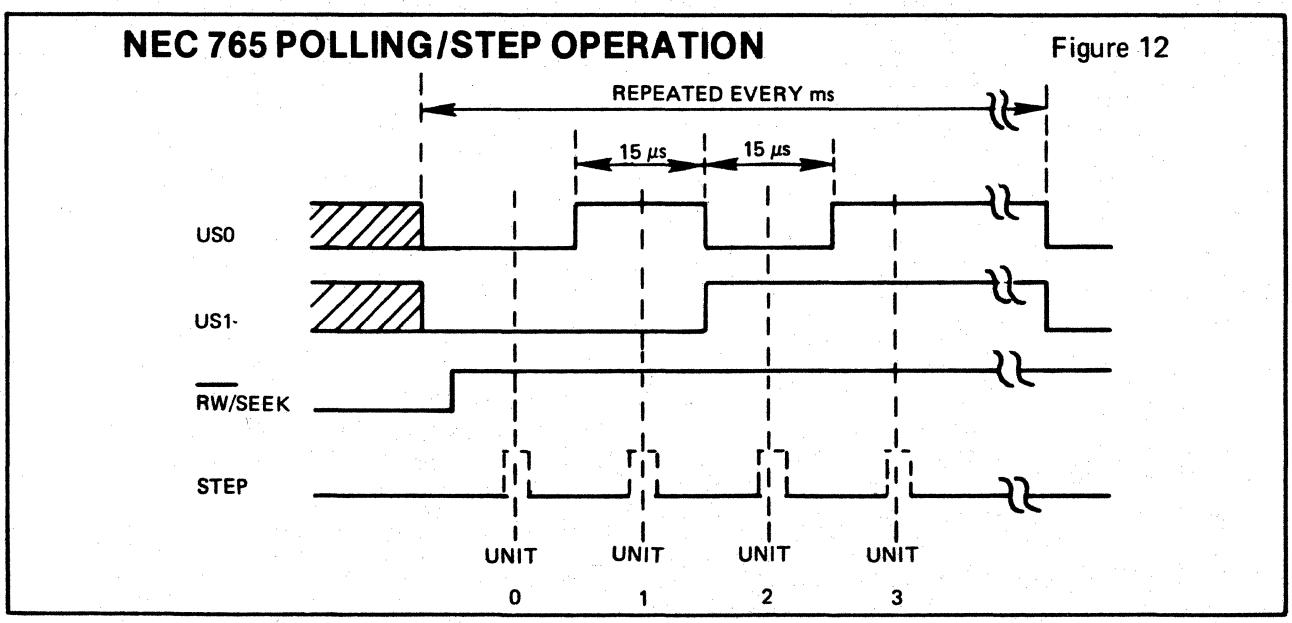
WRITE PRECOMPENSATION

External logic is required to determine the amount of precompensation and to which tracks it is to be applied when operating in the MFM mode. The NEC 765 provides two signals, PS0 and PS1, that determine whether a WDA pulse should be written early, late or nominal. These signals can then be used to generate the 250 ns of precompensation on the inner tracks that is recommended for the CDC FDDs. The circuit used to do this is shown in Figure 1 with the associated timing in Figure 11. When enabled by WE (WDA is always active), the WDA pulse is shifted through the 74LS175 by the 4 MHz clock. Then, depending upon the states of PS0, PS1, and EN PRECOMP, the EARLY, NOMINAL or LATE pulse is selected to be sent to the FDD. This results in a WRITE DATA pulse 250 ns early when PS0 and EN PRECOMP are active. When PS1 and EN PRECOMP are active, the WRITE DATA pulse is written 250 ns late. The WRITE DATA is written at the nominal time if EN PRECOMP is inactive or if both PS0 and PS1 are inactive.

DEMULTIPLEXING STATUS AND CONTROL LINES

The NEC 765 has 6 lines that must be decoded or demultiplexed for up to 12 lines. Four unit select lines can be decoded from 2 of these lines while the other 4 lines are demultiplexed to 8 lines under control of the NEC 765's RW/SEEK line.

The unit select lines, US0 and US1, are software controllable during read and write commands. However, after powerup, between commands, and between step pulses in seek commands, these lines go into a polling mode. Typical timing for a polling operation is shown in Figure 12. The US0 and US1 lines are toggled so that each possible drive is selected in succession with the NEC 765 checking the ready line each time. A result of the polling



feature and the implementation in Figure 1 is that the heads unload during a seek command. This occurs because the HDL output of the NEC 765 goes inactive during a seek command. If this is objectionable an additional hardware head unload delay can be implemented. Also, the drives should be configured so that head loading is independent of unit selection because of the rapid selection and deselection occurring during polling.

Of the other 4 lines, 2 are inputs and 2 are outputs. Each of these lines have a function in the read/write mode and a separate function in the seek mode. The 74LS244 is used as a demultiplexer for these signals and is controlled by the $\overline{RW}$/SEEK output of the NEC 765. The STEP bus driver must also be controlled by the $\overline{RW}$/SEEK signal to prevent erroneous stepping by the drive which might otherwise occur while $\overline{RW}$/SEEK is switching. This erroneous stepping would otherwise occur because the STEP line would go low when the 74LS244 output goes into the high impedance state.

Clock Generation

Two clock signals must be generated for the NEC 765: an 8 MHz square wave clock (CLK), and a write clock (WCK) which contains 250 ns pulses at twice the data rate. The 8 MHz is generated by the 8224 and is fed to the NEC 765 and a 74LS161. This 74LS161 generates the 4 MHz required by the write precompensation circuit and a 2 MHz clock required for WCK generation. The 2 MHz clock is sent to a second 74LS161 which is used to generate 1 MHz and 500 kHz clock signals. The 2 MHz, 1 MHz, and 500 kHz are then gated to form the WCK signals required for FM and MFM operation. See Figure 13. The two WCK signals (WCK0 and WCK1) are then sent to a multiplexer (74LS153) which is controlled by the NEC 765 MFM output. The output of the multiplexer is then sent to the NEC 765 WCK input.

Other Conttroller Considerations

There are several other items, involving both hardware and software, that must be considered when designing a FDC using the NEC 765. These are pointed out below.

Open collector bus drivers are required when the FDD system is in a daisy chain configuration such as this one. 7438 drivers are recommended with terminators placed in the last drive of the system. Correspondingly 150Ω terminating resistors and receivers are required on all inputs from the FFDs.

Output loading should be checked to insure that overloading of a NEC 765 output does not occur. An example of this is the $\overline{RW}$/SEEK output in Figure 1. The NEC 765 cannot drive the TTL and 2 LSTTL loads on this output, so a buffer is needed.

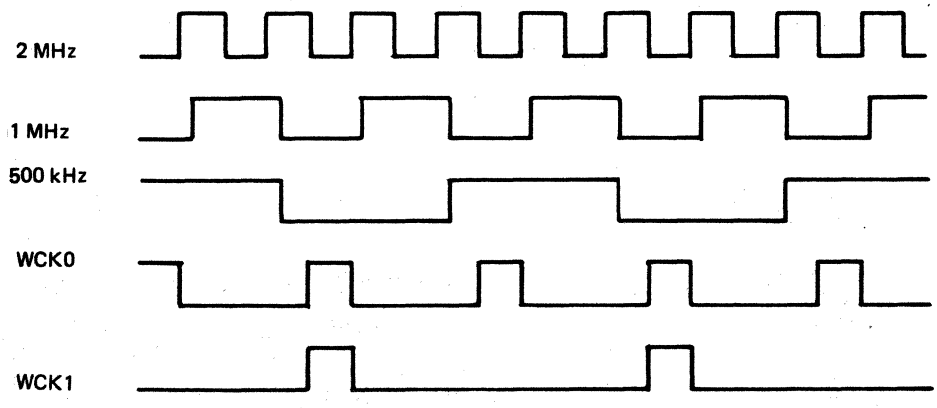
The timing specifications for the CDC FDDs that must be considered when programming the NEC 765 are shown in Table 1. These are straightforward with two possible exceptions.

PERFORMANCE SPECIFICATIONS FOR CDC 9404B AND 9406-2,3 FDD'S.

Parameter	Flexible Disk Drive	
	CDC 9404B	CDC 9406-2, -3
Step Time	10 ms	3 ms
Step Settle Time	15 ms	20 ms
Head Load Time	60 ms	40 ms
Write to Valid Read Data[1]	850 μs	750 μs

[1] Unit deselection, head unloading, head switching, or reading should not be attempted during this time.

WRITE CLOCK GENERATION (FM AND MFM) Figure 13



The NEC 765 does not have a step settle delay incorporated into it. This is not a problem because the NEC 765 always unloads the heads during a seek. Then any subsequent command will load the heads and wait the specified head load time before continuing. Since the head load delay is greater than the step settle time the head will be fully settled. If external logic is used to keep the heads loaded during a seek, the full head load timeout is not required although it is still executed by the NEC 765.

The "write to valid read data" specification also requires further explanation. During this time following a write operation none of the following should occur: deselecting of the unit, attempting to read, head unloading, or head switching. This delay is required to insure that all data just written on the diskette has been fully tunnel erased and that valid read data is available.

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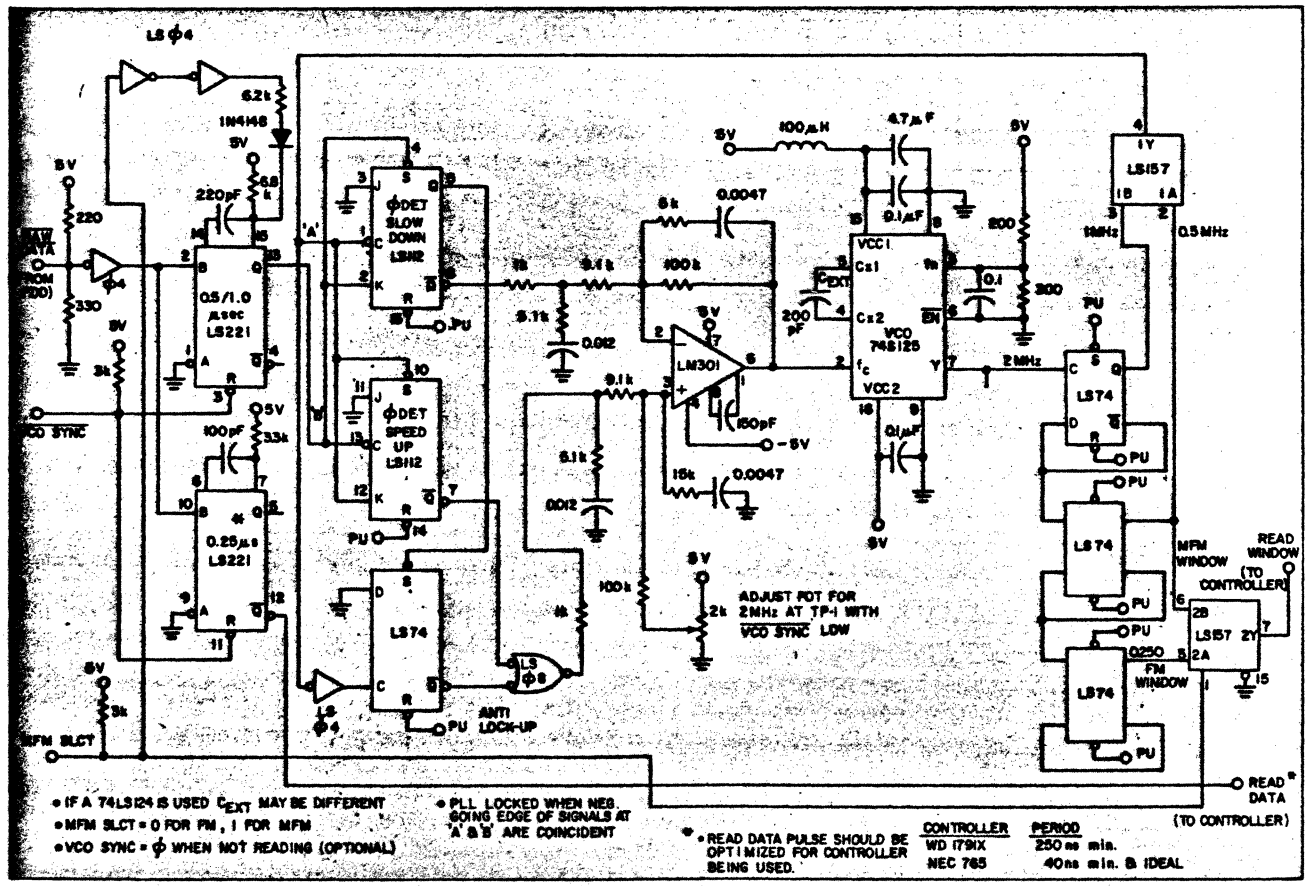
Wide effective margin makes double-density recording reliable

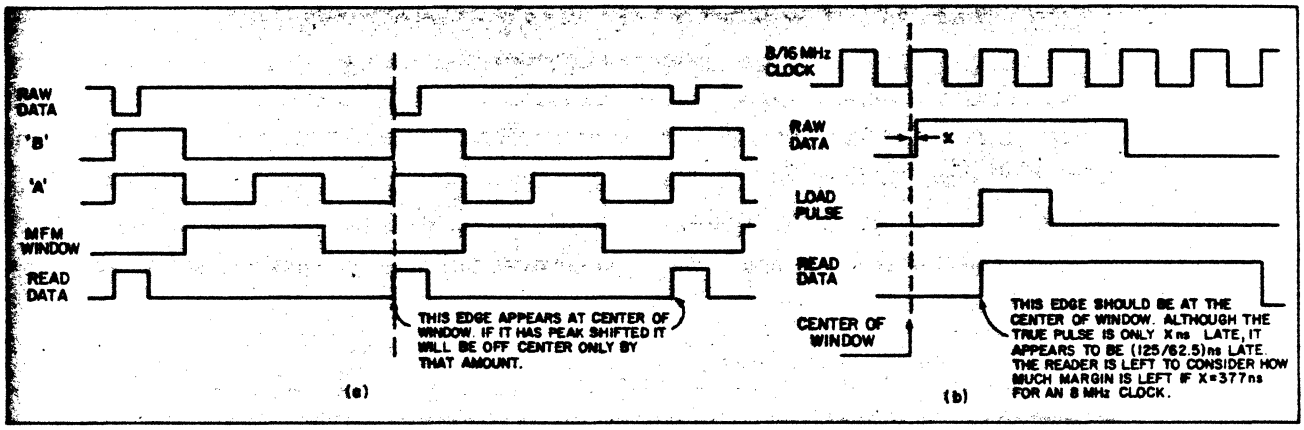
Unlike single-density recording, double-density recording contains no fixed clock pulses and the pulses appear at 2, 3 or 4 μs intervals instead of just 2 or 4 μs. This means a phase-locked loop must be used for reliable data recovery. And since the window required to recover this type of data is only 1 μs wide, as opposed to 2 μs for single-density recording, the phenomenon of peak shift must be considered. This effect becomes much more pronounced on the floppy disk's inner tracks where the packing density is highest.

Precompensation during writing will help offset this. However, that alone will not provide acceptable results. A well-designed data-recovery circuit is needed to provide noise immunity, a fast lock, and maximum margin.

Most manufacturers' application notes for LSI floppy-disk controllers contain suggested data-recovery circuits. For double-density recording, reliable data recovery is a significant problem. The



1. This data-recovery circuit, for use with double-density floppy-disk recording, has an effective window size (margin) close to the theoretical 500 ns limit. Other well-publicized designs exhibit smaller margins. This means disk drives must be hand-selected or error rates become unacceptably high.



2. Timing diagrams for Fig. 1 illustrate that the margin loss associated with the improved digital PLL circuit is not significant (a). For comparison, the timing diagram for an alternate circuit exhibiting serious margin loss is also shown (b).

methods outlined in widely distributed literature contain a very serious shortcoming. Most all use a digital one-shot consisting of flip-flops driven by an external clock to reconstruct the read data pulse. This leads to the problem outlined in Fig. 2b. The circuit of Fig. 1 provides a maximum effective margin, eliminating this problem and the resulting high error rates that have thus far restricted the acceptance of double-density floppy-disk drives.

Margin is a measure of how far from the ideal location the pulse can be without being lost (effective window size). Ideally, this is 500 ns. All floppy-disk data-recovery circuits are built with that goal, and most contain windows that *appear* to be 500 ns.

In practice, the effective margin or window actually available could mean the system will not work. A PLL that locks up in 20 μs and has a margin of about 325 ns will work only with a disk drive hand-selected for maximum margin and superior media. (Since a good double-density floppy disk drive has a maximum inherent peak-shift effect of 300 ns, operation with a typical disk drive requires perfect media. Any drop in bit amplitude will increase the peak shift.)

Margin is lost in two ways. IC propagation delays account for some loss in the recovery circuit, but the biggest culprit is the digital PLL. That's because a reference oscillator is required to support the digital one-shots which generate read data for the controller and load pulses for the feedback clock divider. Since the raw data pulses are asynchronous with respect to the synchronous reference-oscillator pulses of 16 MHz, up to 62.5 ns can be lost right here. Increasing the clock frequency can decrease this loss if extra frequency-divider circuits and more layout problems can be tolerated.

With the circuit of Fig. 1, the read data pulse is reconstructed by an analog (RC) one-shot. Any margin loss is due entirely to IC propagation delays, so that the total effective circuit margin is as close to the theoretical 500 ns limit as possible.

A tradeoff is involved in the simultaneous requirement for good noise immunity and a short lock time. The PLL should be able to lock within 20 to 100 μs, the limit set by the length of the sync field on the diskette. A lock time of 30 μs will operate with most formats in current use. A faster lock will only make the system more noise sensitive.

The PLL portion of Fig. 1 was specifically designed for this application. Here lock is achieved from a 180° out-of-phase condition in approximately 30 μs. There are other detector and filter designs very similar to Fig. 1. They fall short because they have no gain in their active filters. In Fig. 1, an LM 301 provides the necessary gain. This allows tailoring the circuit to lock in 30 μs with a damping factor of 0.5. Performance of the loop is matched with the application.

For the total system, margin loss due to the controller must also be considered. Two popular LSI controller chips are listed with the associated margin loss inherent in the controller. Early spec sheets reported a 200 ns margin loss for the NEC 765. This, according to NEC, was "conservative." A realistic value is indicated here.

Controller	Margin loss
Western Digital 1791 Series	40 ns
NEC 765	55 ns

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